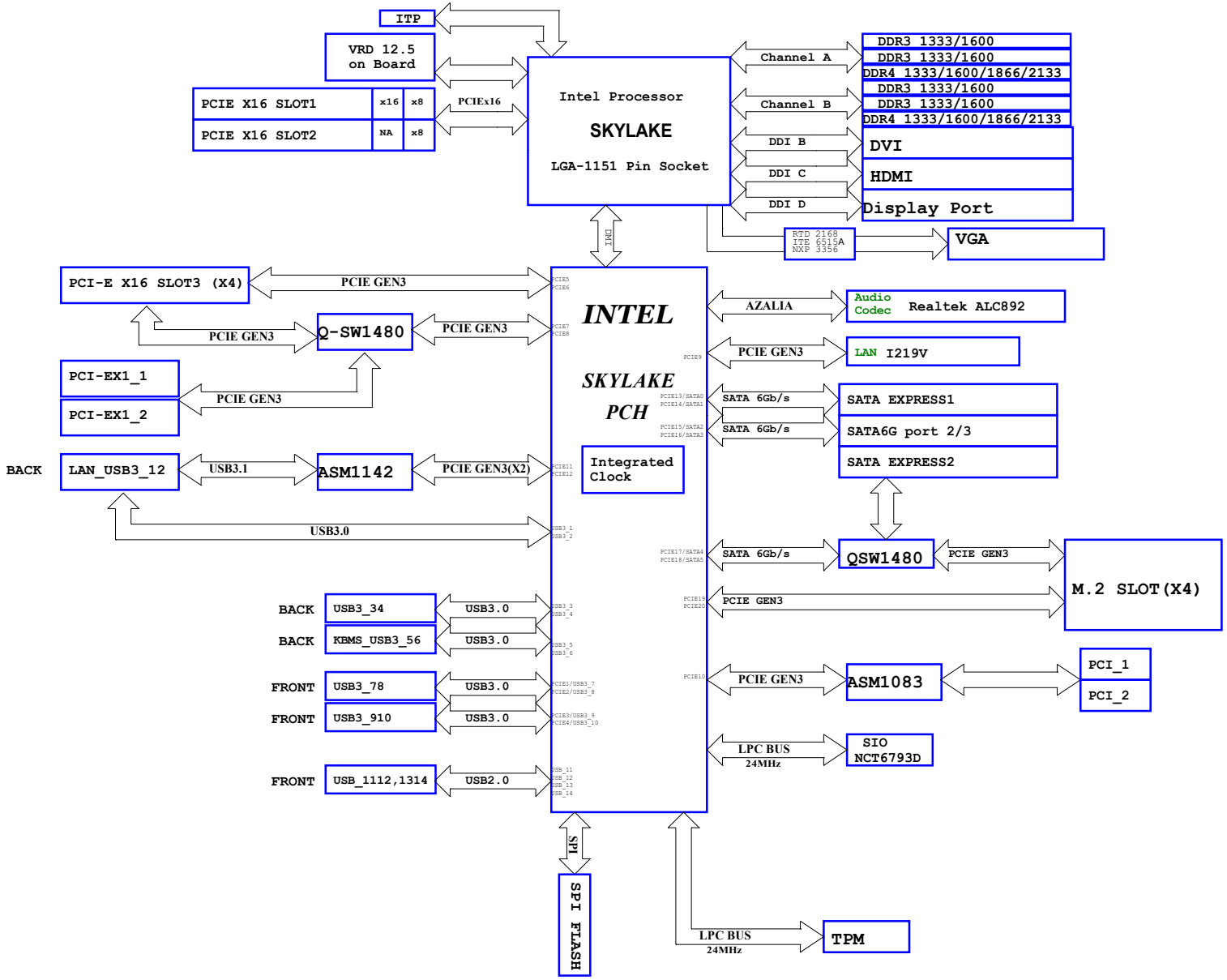
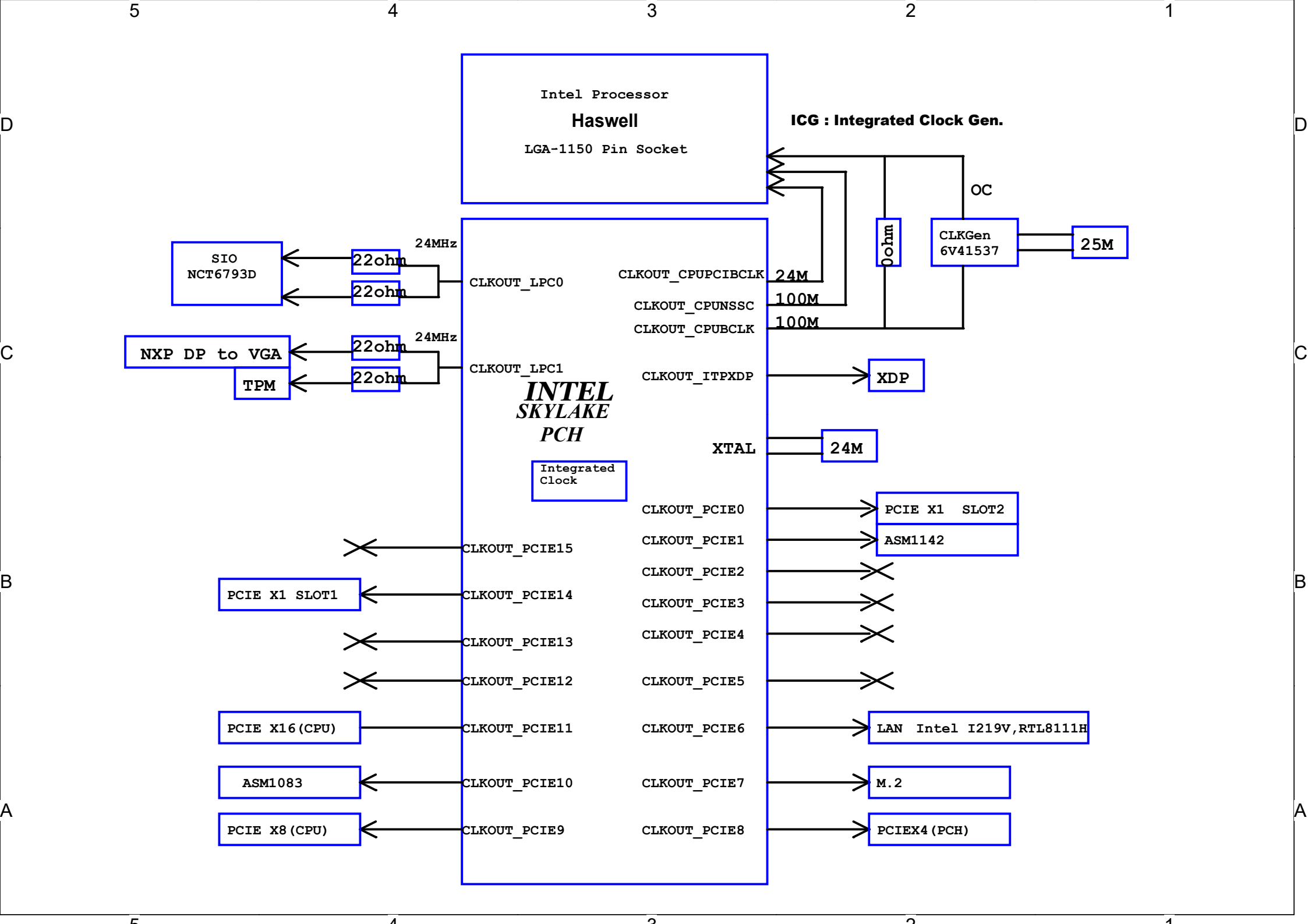
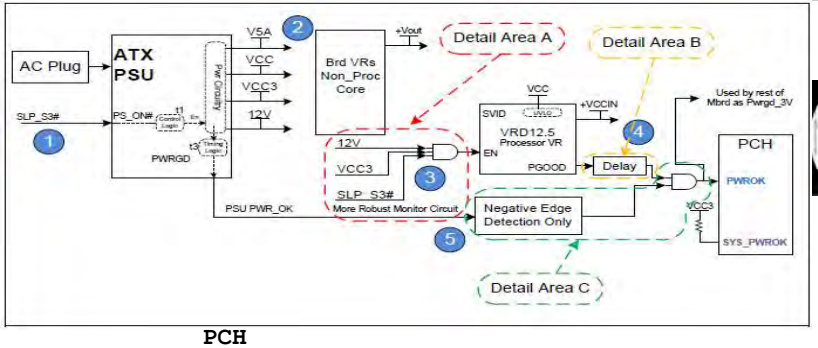
B150 PRO GAMING

Rev 1.00 2014.01 SkyLake




Intel Processor
Haswell
LGA-1150 Pin Socket
ICG : Integrated Clock Gen.
OC
0ohm
CLKGen
6V41537
25M
SIO
NCT6793D
24MHz
22ohm
22ohm
CLKOUT_LPC0
CLKOUT_CPUPCIBCLK
24M
CLKOUT_CPUNSSC
100M
CLKOUT_CPUBCLK
100M
NXP DP to VGA
TPM
24MHz
22ohm
22ohm
CLKOUT_LPC1
CLKOUT_ITPXDP
XDP
INTEL
SKYLAKE
PCH
XTAL
24M
Integrated
Clock
CLKOUT_PCIE0
PCIE X1 SLOT2
CLKOUT_PCIE1
ASM1142
CLKOUT_PCIE15
CLKOUT_PCIE2
PCIE X1 SLOT1
CLKOUT_PCIE14
CLKOUT_PCIE3
CLKOUT_PCIE13
CLKOUT_PCIE4
CLKOUT_PCIE12
CLKOUT_PCIE5
PCIE X16(CPU)
CLKOUT_PCIE11
CLKOUT_PCIE6
LAN Intel I219V,RTL8111H
ASM1083
CLKOUT_PCIE10
CLKOUT_PCIE7
M.2
PCIE X8(CPU)
CLKOUT_PCIE9
CLKOUT_PCIE8
PCIEX4(PCH)



RESET_SWITCH

PCI_Express x 16_1 PWRGD <19>O_X16_RST#

PCI_Express x 16_2 PWRGD <19>O_X16_RST#

PCI_Express x 1_1,2 & x16_3 PWRGD <19>O_X1_RST#

POWER_SWITCH

<5>PWRBTN#

SIO NCT6793D

PS_IN# PCIRST1# PCIRST2# PCIRST3# LRESET# KBRST# RSMRST# PS_OUT# SUSC# SUSB# PSON# *1 ATXPGD *2 PWROK

<17>S_PLTRST# *8

O_KB_RST#

<4>O_RSMRST#

<6>O_IOPWRBTN#

<4.1> / <8>S_SLP_S4#

<4.2> / <7>S_SLP_S3#

<7>S_SLP_A#

<7.1>S_SLP_LAN#

POWER SUPPLY

Main PWR VSB PSON# PWROK

<10>12V,5V,3V

<3>+5VSB, +3VSB

<9>ATX_PSON#_R

<11>P_PWROK_PS

11.Some SIO don't use, use +3V

<2>AC Power Switch On

PCH skylake

HDA_RST# SYS_RESET# PLTRST# PLTRST_PROC# RCIN# RSMRST# PWRBTN# SLP_S5# SLP_S4# *4 SLP_S3# *5 SLP_A# *3 SLP_LAN# SYS_PWROK PCH_PWROK RTCRST# SRTCRST# PROCPUPWRGD DPWROK

AZ_RST#

RESET# AUDIO ALC898

<1>S_RTCRST#

<1>S_SRTCRST#

BATTERY

*7 <13>H_CPUPWRGD

<3.1>S_DPWROK(if NO DSW, S_DPWROK=S_RSMRST#)

<12>O_PWROK

SPI Power (AMT) intel LAN

XDP DBR# RESET# OBSDATA

SYS_RESET#

H_CPURST#

PROCESSOR skylake

DBR# RESET# CFG PWRGOOD SVID VCORE

SYS_RESET#

*9 <18>H_CPURST#

*5

<14>VRM_SVID

<15>VCORE

Vcore Controller

SVID VCORE VR_ON PGOOD

<16>P_VR_READY_10

*6 S_SLP_S3#

+12V

+3V

ASP1400(ASP1401)

CHIP

SOCKET or SLOT

*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3

*4 SLP_S4# controls +1.5VDual and +VTTDDR

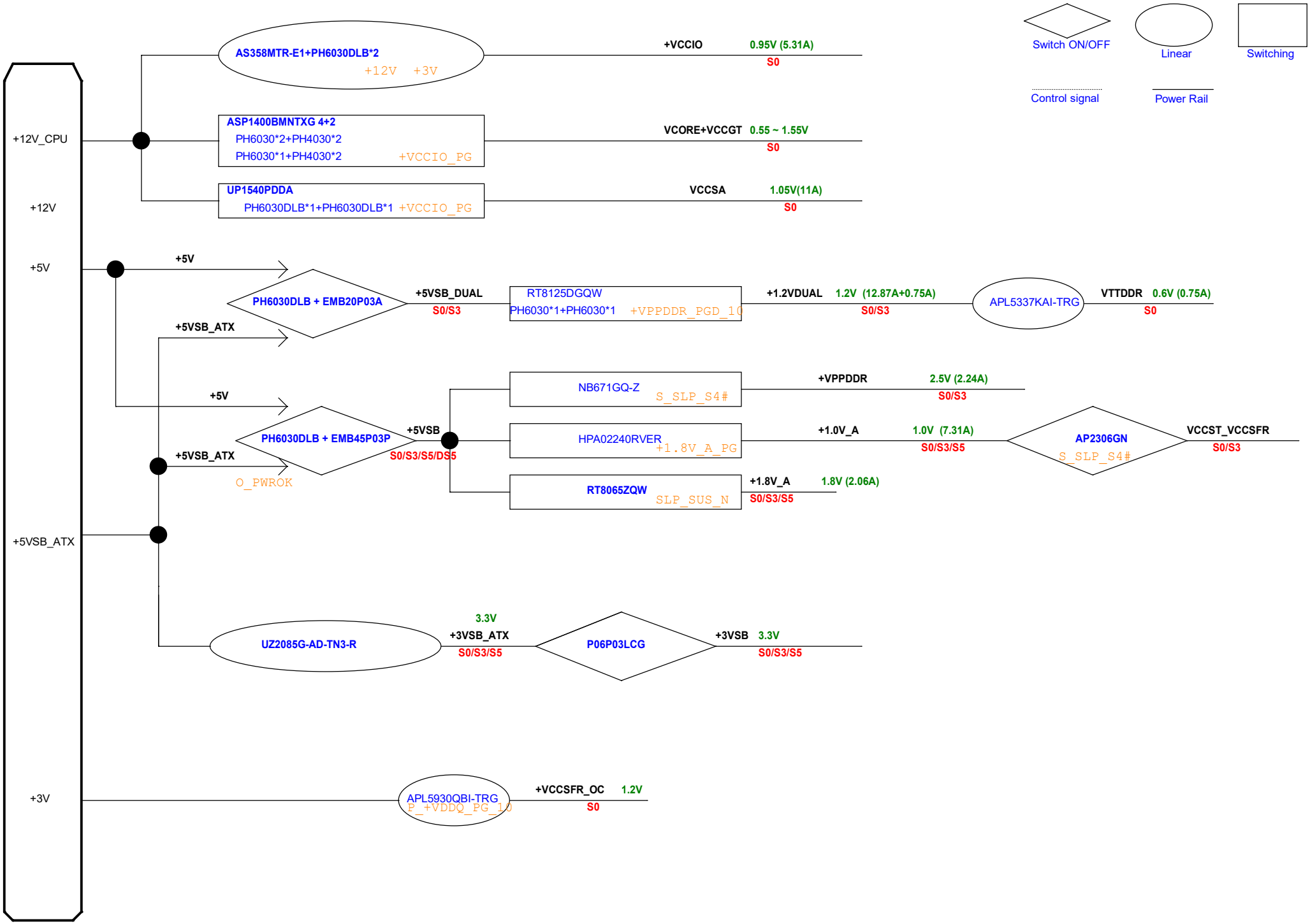
*5 Come with 1.5VDUAL

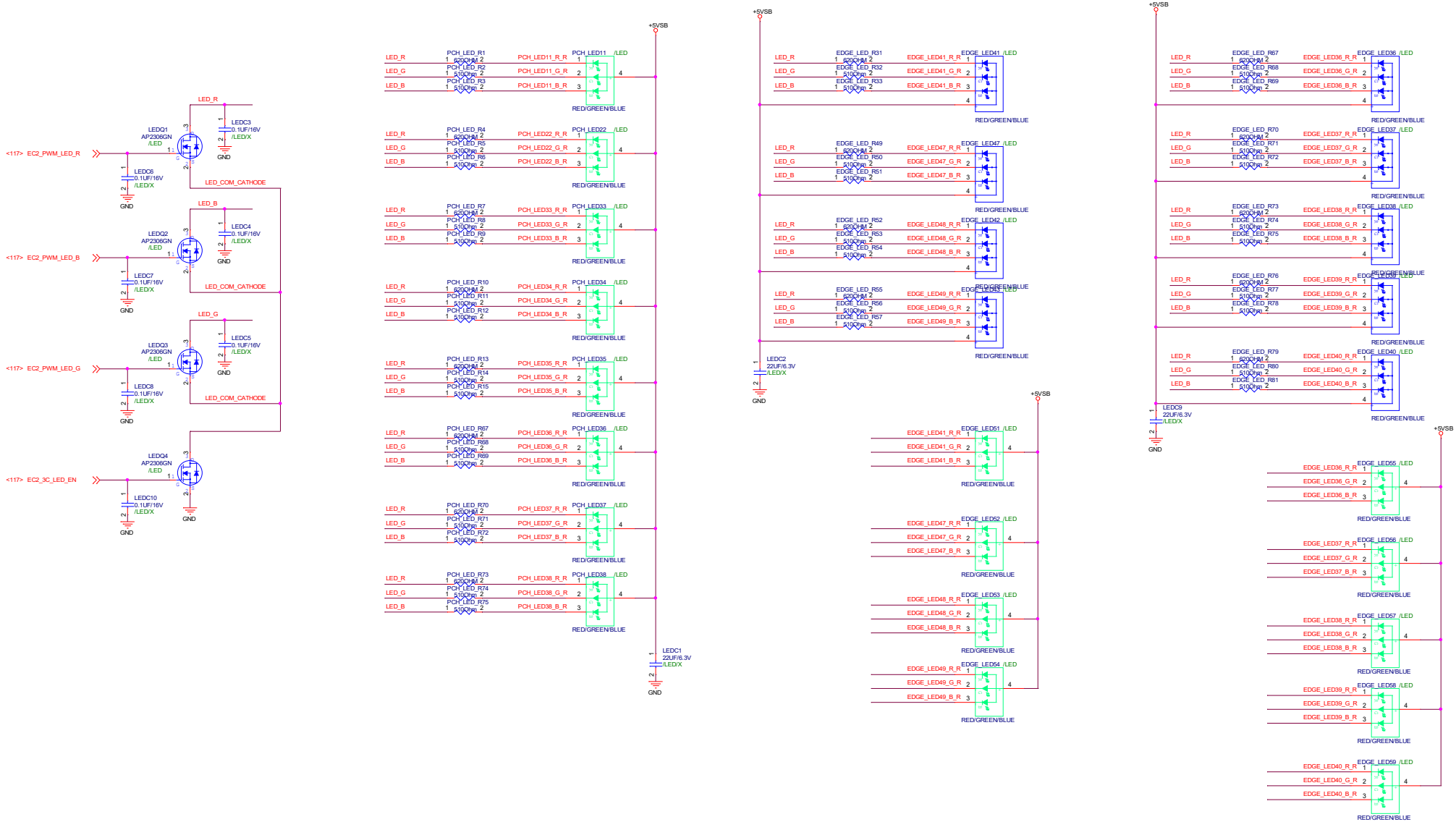
*6 Come with +3V,+12V and gated by SLP_S3#

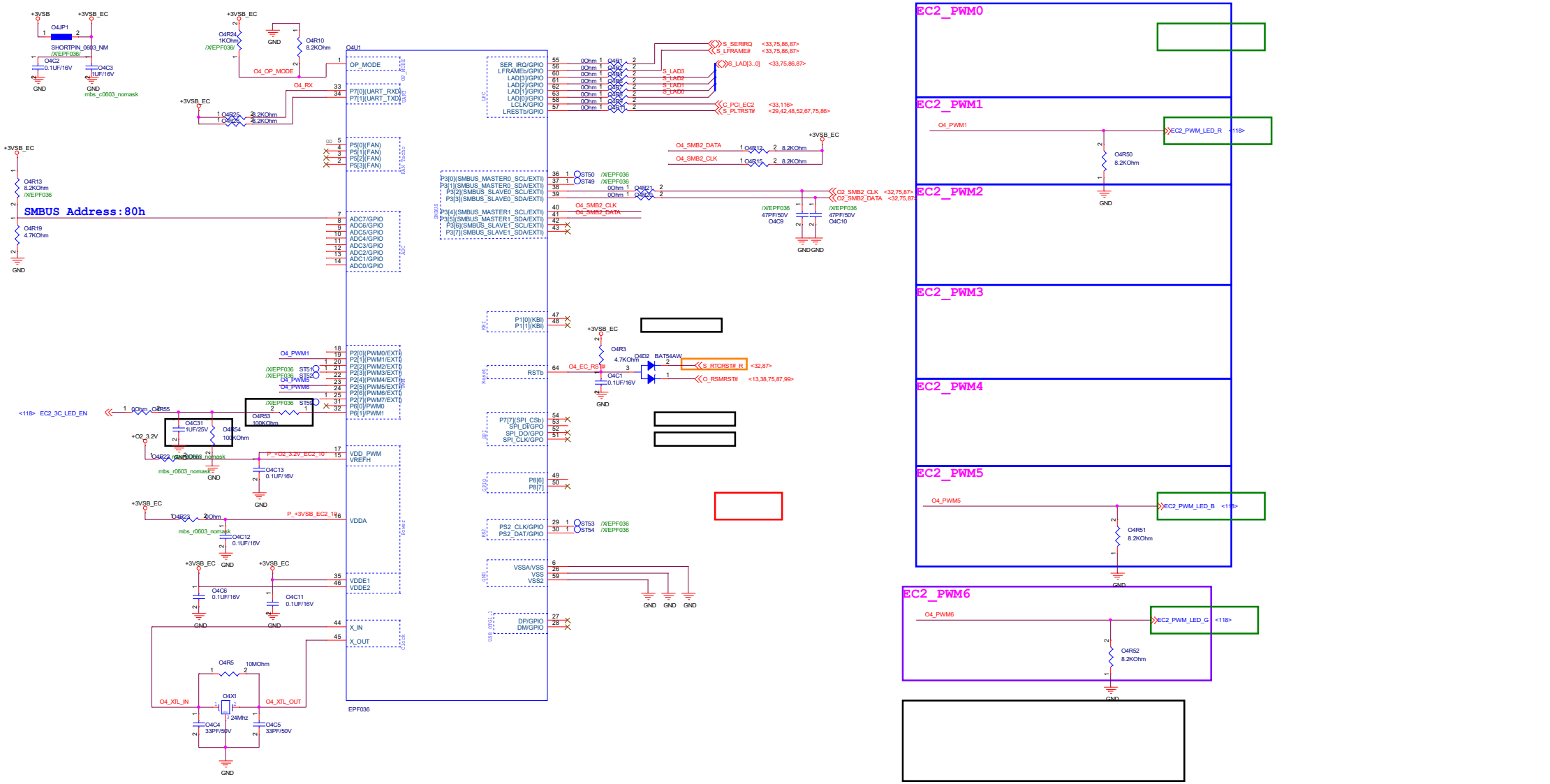
*7 CPUPWRGD= After PWROK

*8 PLTRST# = PCH PWROK "AND" PCH SYS_PWROK

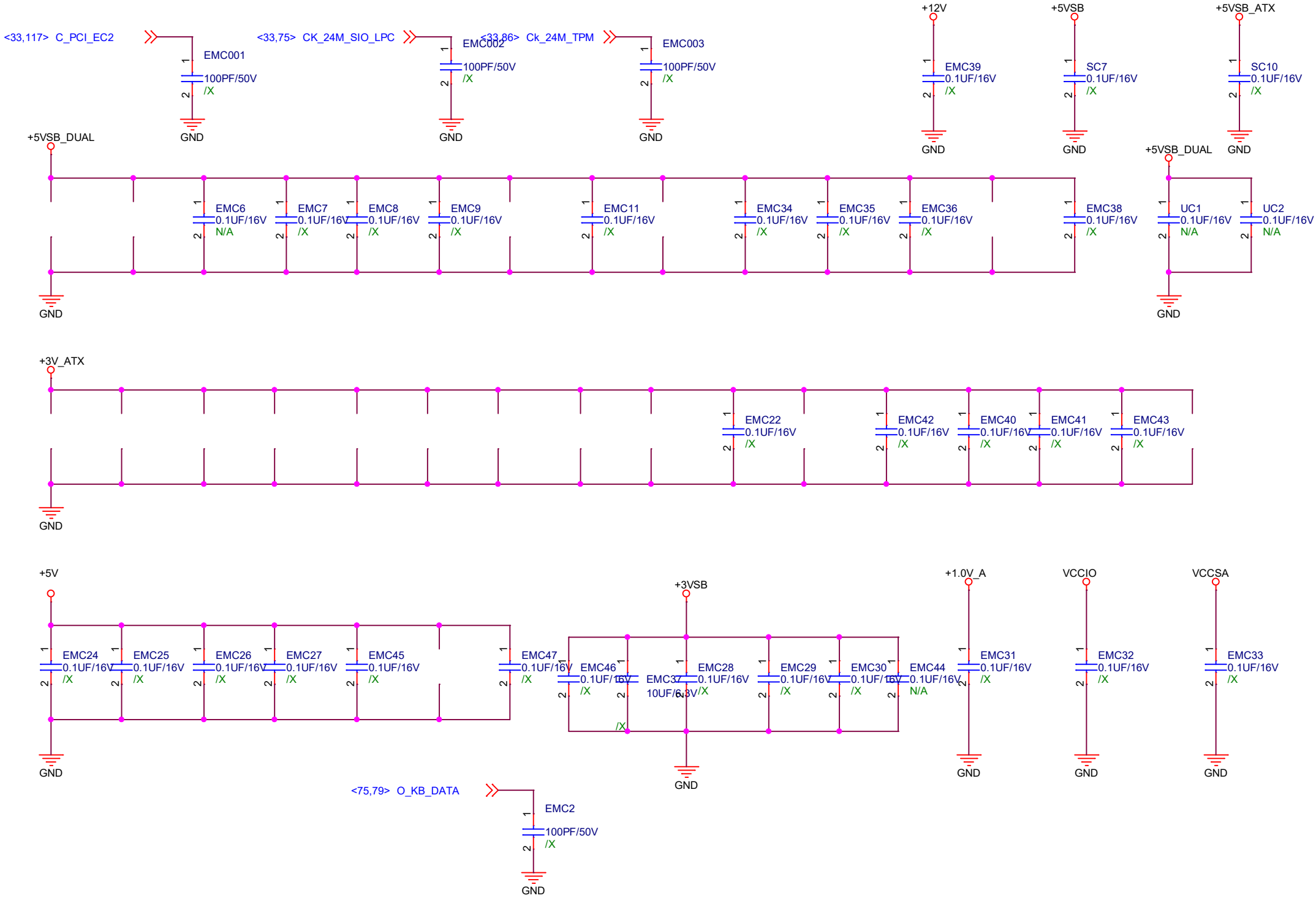
*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU

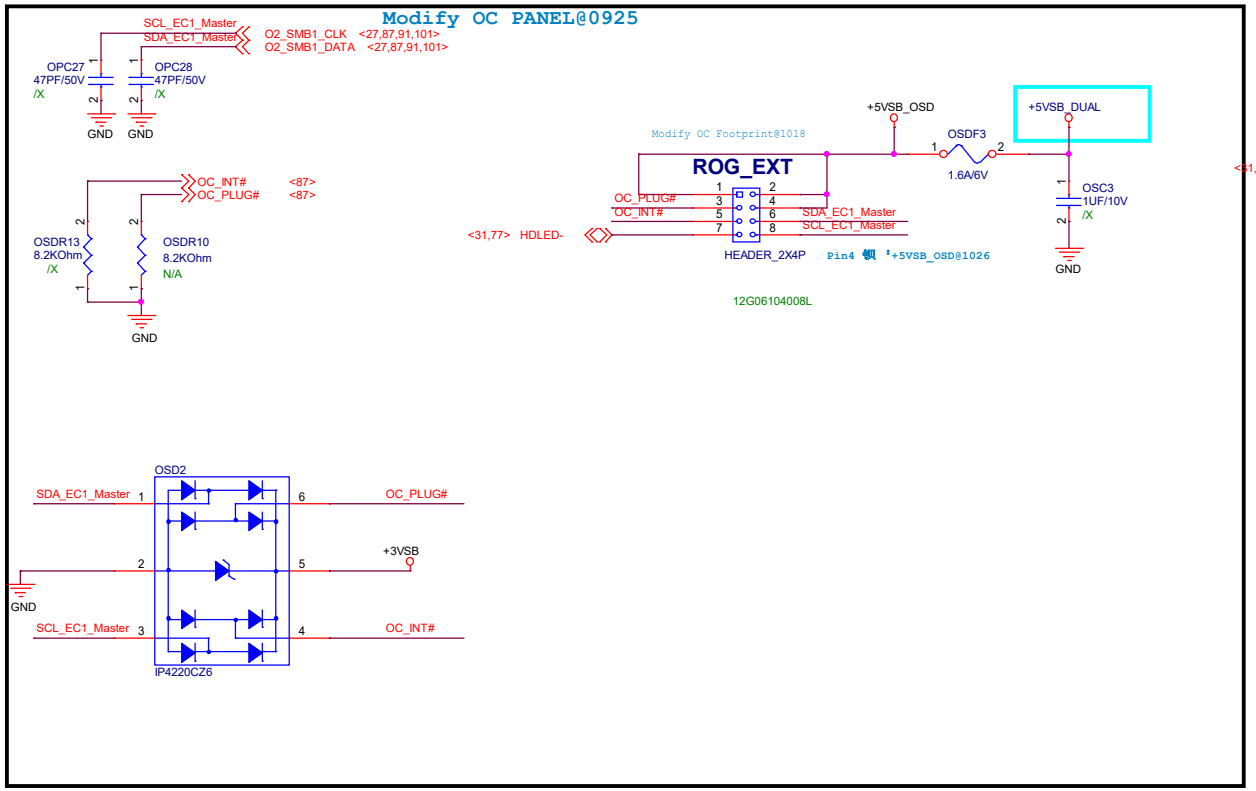

Switch ON/OFF
Linear
Switching
Control signal
Power Rail
+12V_CPU
+12V
+5V
+5VSB_ATX
+3V
AS358MTR-E1+PH6030DLB*2
+12V +3V
+VCCIO
0.95V (5.31A)
S0
ASP1400BMNTXG 4+2
PH6030*2+PH4030*2
PH6030*1+PH4030*2
+VCCIO_PG
VCORE+VCCGT
0.55 ~ 1.55V
S0
UP1540PDDA
PH6030DLB*1+PH6030DLB*1
+VCCIO_PG
VCCSA
1.05V(11A)
S0
+5V
PH6030DLB + EMB20P03A
+5VSB_DUAL
S0/S3
RT8125DGQW
PH6030*1+PH6030*1
+VPPDDR_PGD_10
+1.2VDUAL
1.2V (12.87A+0.75A)
S0/S3
APL5337KAI-TRG
VTTDDR
0.6V (0.75A)
S0
+5VSB_ATX
+5V
PH6030DLB + EMB45P03P
+5VSB
S0/S3/S5/DS5
+5VSB_ATX
O_PWROK
NB671GQ-Z
S_SLP_S4#
+VPPDDR
2.5V (2.24A)
S0/S3
HPA02240RVER
+1.8V_A_PG
+1.0V_A
1.0V (7.31A)
S0/S3/S5
AP2306GN
S_SLP_S4#
VCCST_VCCSFR
S0/S3
RT8065ZQW
SLP_SUS_N
+1.8V_A
1.8V (2.06A)
S0/S3/S5
UZ2085G-AD-TN3-R
3.3V
+3VSB_ATX
S0/S3/S5
P06P03LCG
+3VSB
3.3V
S0/S3/S5
APL5930QBI-TRG
P_+VDDQ_PG_10
+VCCSFR_OC
1.2V
S0

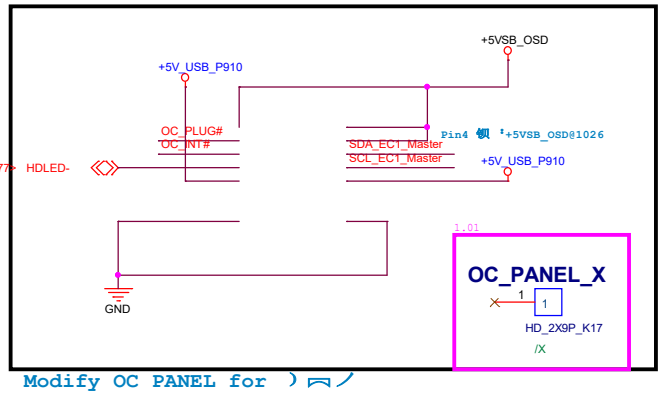

LED_R
LEDQ1
AP2306GN
/LED
<117> EC2_PWM_LED_R
LEDC6
0.1UF/16V
/LED/X
GND
LEDC3
0.1UF/16V
/LED/X
GND
LED_COM_CATHODE
LED_B
LEDQ2
AP2306GN
/LED
<117> EC2_PWM_LED_B
LEDC7
0.1UF/16V
/LED/X
GND
LEDC4
0.1UF/16V
/LED/X
GND
LED_COM_CATHODE
LED_G
LEDQ3
AP2306GN
/LED
<117> EC2_PWM_LED_G
LEDC8
0.1UF/16V
/LED/X
GND
LEDC5
0.1UF/16V
/LED/X
GND
LED_COM_CATHODE
LEDQ4
AP2306GN
/LED
<117> EC2_3C_LED_EN
LEDC10
0.1UF/16V
/LED/X
GND
GND
+5VSB
LED_R
LED_G
LED_B
PCH_LED_R1
PCH_LED_R2
PCH_LED_R3
620OHM
510Ohm
PCH_LED11_R_R
PCH_LED11_G_R
PCH_LED11_B_R
PCH_LED11
/LED
RED/GREEN/BLUE
PCH_LED_R4
PCH_LED_R5
PCH_LED_R6
PCH_LED22_R_R
PCH_LED22_G_R
PCH_LED22_B_R
PCH_LED22
PCH_LED_R7
PCH_LED_R8
PCH_LED_R9
PCH_LED33_R_R
PCH_LED33_G_R
PCH_LED33_B_R
PCH_LED33
PCH_LED_R10
PCH_LED_R11
PCH_LED_R12
PCH_LED34_R_R
PCH_LED34_G_R
PCH_LED34_B_R
PCH_LED34
PCH_LED_R13
PCH_LED_R14
PCH_LED_R15
PCH_LED35_R_R
PCH_LED35_G_R
PCH_LED35_B_R
PCH_LED35
PCH_LED_R67
PCH_LED_R68
PCH_LED_R69
PCH_LED36_R_R
PCH_LED36_G_R
PCH_LED36_B_R
PCH_LED36
PCH_LED_R70
PCH_LED_R71
PCH_LED_R72
PCH_LED37_R_R
PCH_LED37_G_R
PCH_LED37_B_R
PCH_LED37
PCH_LED_R73
PCH_LED_R74
PCH_LED_R75
PCH_LED38_R_R
PCH_LED38_G_R
PCH_LED38_B_R
PCH_LED38
LEDC1
22UF/6.3V
/LED/X
GND
+5VSB
LED_R
LED_G
LED_B
EDGE_LED_R31
EDGE_LED_R32
EDGE_LED_R33
EDGE_LED41_R_R
EDGE_LED41_G_R
EDGE_LED41_B_R
EDGE_LED41
/LED
RED/GREEN/BLUE
EDGE_LED_R49
EDGE_LED_R50
EDGE_LED_R51
EDGE_LED47_R_R
EDGE_LED47_G_R
EDGE_LED47_B_R
EDGE_LED47
/LED
RED/GREEN/BLUE
EDGE_LED_R52
EDGE_LED_R53
EDGE_LED_R54
EDGE_LED48_R_R
EDGE_LED48_G_R
EDGE_LED48_B_R
EDGE_LED42
/LED
RED/GREEN/BLUE
EDGE_LED_R55
EDGE_LED_R56
EDGE_LED_R57
EDGE_LED49_R_R
EDGE_LED49_G_R
EDGE_LED49_B_R
EDGE_LED49
/LED
RED/GREEN/BLUE
LEDC2
22UF/6.3V
/LED/X
GND
+5VSB
EDGE_LED41_R_R
EDGE_LED41_G_R
EDGE_LED41_B_R
EDGE_LED51
/LED
RED/GREEN/BLUE
EDGE_LED47_R_R
EDGE_LED47_G_R
EDGE_LED47_B_R
EDGE_LED52
/LED
RED/GREEN/BLUE
EDGE_LED48_R_R
EDGE_LED48_G_R
EDGE_LED48_B_R
EDGE_LED53
/LED
RED/GREEN/BLUE
EDGE_LED49_R_R
EDGE_LED49_G_R
EDGE_LED49_B_R
EDGE_LED54
/LED
RED/GREEN/BLUE
+5VSB
LED_R
LED_G
LED_B
EDGE_LED_R67
EDGE_LED_R68
EDGE_LED_R69
EDGE_LED36_R_R
EDGE_LED36_G_R
EDGE_LED36_B_R
EDGE_LED36
/LED
RED/GREEN/BLUE
EDGE_LED_R70
EDGE_LED_R71
EDGE_LED_R72
EDGE_LED37_R_R
EDGE_LED37_G_R
EDGE_LED37_B_R
EDGE_LED37
/LED
RED/GREEN/BLUE
EDGE_LED_R73
EDGE_LED_R74
EDGE_LED_R75
EDGE_LED38_R_R
EDGE_LED38_G_R
EDGE_LED38_B_R
EDGE_LED38
/LED
RED/GREEN/BLUE
EDGE_LED_R76
EDGE_LED_R77
EDGE_LED_R78
EDGE_LED39_R_R
EDGE_LED39_G_R
EDGE_LED39_B_R
EDGE_LED39
/LED
RED/GREEN/BLUE
EDGE_LED_R79
EDGE_LED_R80
EDGE_LED_R81
EDGE_LED40_R_R
EDGE_LED40_G_R
EDGE_LED40_B_R
EDGE_LED40
/LED
RED/GREEN/BLUE
LEDC9
22UF/6.3V
/LED/X
GND
+5VSB
EDGE_LED36_R_R
EDGE_LED36_G_R
EDGE_LED36_B_R
EDGE_LED55
/LED
RED/GREEN/BLUE
EDGE_LED37_R_R
EDGE_LED37_G_R
EDGE_LED37_B_R
EDGE_LED56
/LED
RED/GREEN/BLUE
EDGE_LED38_R_R
EDGE_LED38_G_R
EDGE_LED38_B_R
EDGE_LED57
/LED
RED/GREEN/BLUE
EDGE_LED39_R_R
EDGE_LED39_G_R
EDGE_LED39_B_R
EDGE_LED58
/LED
RED/GREEN/BLUE
EDGE_LED40_R_R
EDGE_LED40_G_R
EDGE_LED40_B_R
EDGE_LED59
/LED
RED/GREEN/BLUE



Voltage	SMB Address	Torlence
0 V	80	(+/-) 0.25V
0.5V	82	(+/-) 0.25V
1.0V	84	(+/-) 0.25V
1.5V	86	(+/-) 0.25V
2.0V	88	(+/-) 0.25V
2.5V	90	(+/-) 0.25V
3.0V	92	(+/-) 0.25V


<33,117> C_PCI_EC2
EMC001
100PF/50V
/X
GND
<33,75> CK_24M_SIO_LPC
EMC002
100PF/50V
/X
GND
<33,86> Ck_24M_TPM
EMC003
100PF/50V
/X
GND
+12V
EMC39
0.1UF/16V
/X
GND
+5VSB
SC7
0.1UF/16V
/X
GND
+5VSB_ATX
SC10
0.1UF/16V
/X
GND
+5VSB_DUAL
EMC6
0.1UF/16V
N/A
EMC7
0.1UF/16V
/X
EMC8
0.1UF/16V
/X
EMC9
0.1UF/16V
/X
EMC11
0.1UF/16V
/X
EMC34
0.1UF/16V
/X
EMC35
0.1UF/16V
/X
EMC36
0.1UF/16V
/X
EMC38
0.1UF/16V
/X
GND
+5VSB_DUAL
UC1
0.1UF/16V
N/A
UC2
0.1UF/16V
N/A
GND
+3V_ATX
EMC22
0.1UF/16V
/X
EMC42
0.1UF/16V
/X
EMC40
0.1UF/16V
/X
EMC41
0.1UF/16V
/X
EMC43
0.1UF/16V
/X
GND
+5V
EMC24
0.1UF/16V
/X
EMC25
0.1UF/16V
/X
EMC26
0.1UF/16V
/X
EMC27
0.1UF/16V
/X
EMC45
0.1UF/16V
/X
EMC47
0.1UF/16V
/X
GND
+3VSB
EMC46
0.1UF/16V
/X
EMC37
10UF/6.3V
/X
EMC28
0.1UF/16V
/X
EMC29
0.1UF/16V
/X
EMC30
0.1UF/16V
/X
EMC44
0.1UF/16V
N/A
GND
+1.0V_A
EMC31
0.1UF/16V
/X
GND
VCCIO
EMC32
0.1UF/16V
/X
GND
VCCSA
EMC33
0.1UF/16V
/X
GND
<75,79> O_KB_DATA
EMC2
100PF/50V
/X
GND





Modify OC PANEL for

Fiducial Mask
(　厩骽)

Delete it for EMS

蛾　　厩骽

LayoutRD稹为　丁　，
被　　聋|　聋　厩骽；
丁　马贺　厩骽常惠礴　結隔い，
程诧　暗　埃.

聋　厩骽

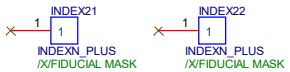
聋　厩骽

Delete it for EMS

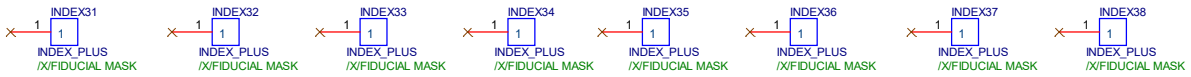
厩骽

LayoutRD稹为　丁　，
被　　聋|　聋　厩骽；
丁　马贺　厩骽常惠礴　結隔い，
程诧　暗　埃.

聋　厩骽

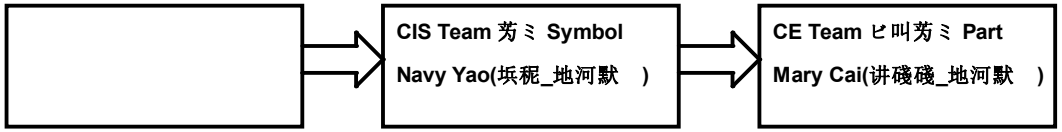


聋　厩骽

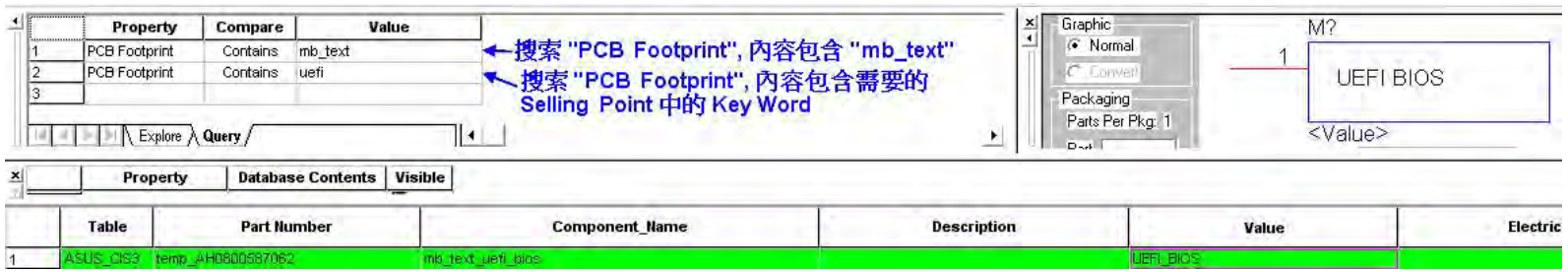


Selling Point

1. Selling Point 穝糤琛祘の怠　　磟



2.　⋮ъ　Selling Point Part,　　瓜



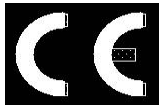
3. Example

New Project Logo

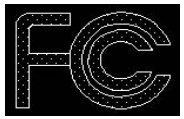
LOGO8
1 VCCI
VCCI
/X

LOGO4
1 MARK_L
MARK_L
/X

LOGO6
1 CE
CE
/X



LOGO2
1 FCC
FCC
/X



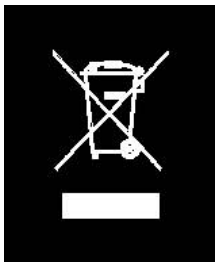
LOGO3
1 RCM
RCM
/X

LOGO1
1 EMI_D33005_H
EMI_D33005_H
/X

LOGO9
1 CAN ICES-3(B)/NMB-3(B)
CAN_ICES_3B_NMB_3B
/X

LOGO10
1 KC_MSQ
KC_MSQ
/X

LOGO7
1 PCB MADE IN CHINA
PCB_MADE_IN_CHINA
/X

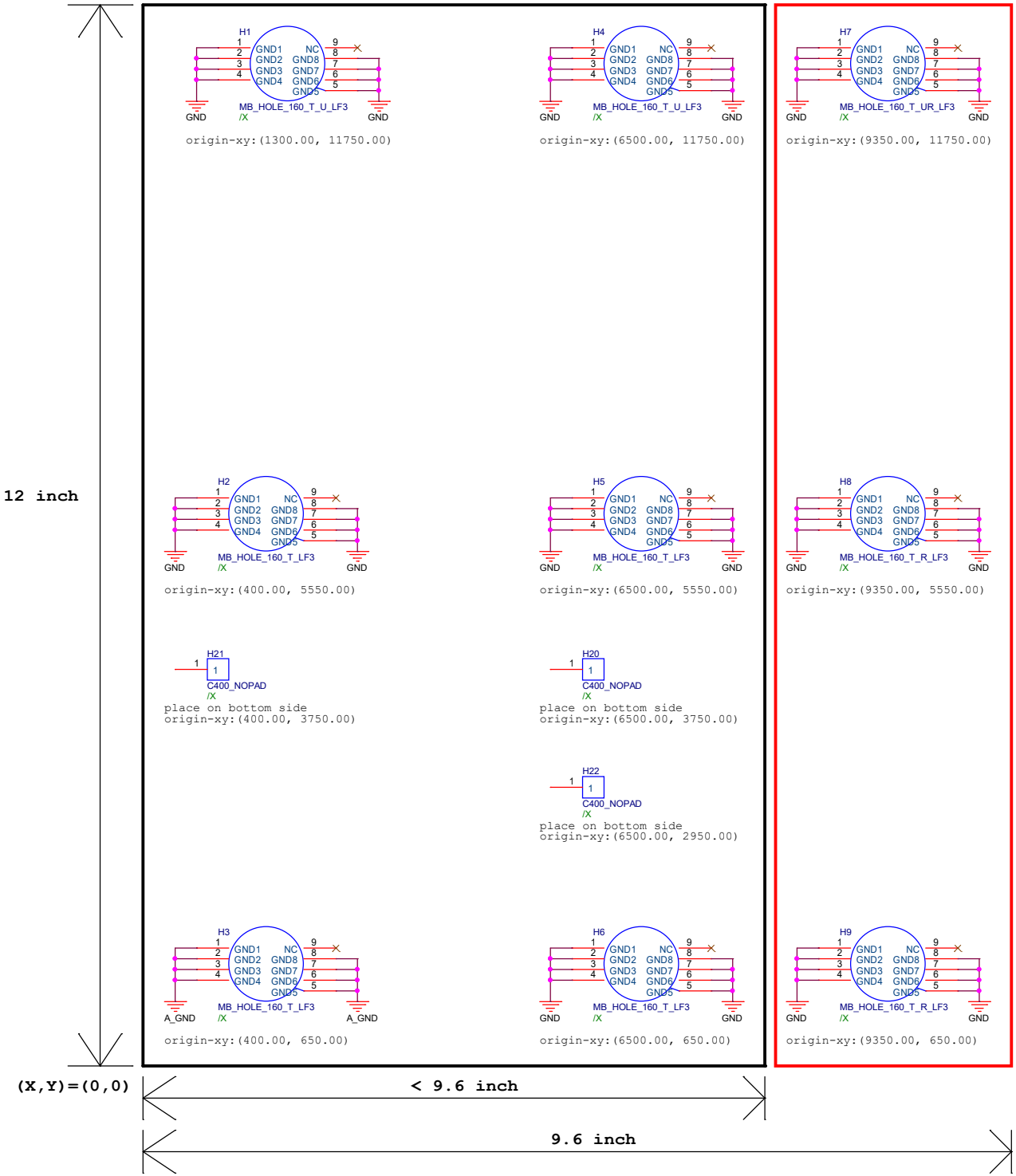


LOGO5
1 WEEE_LOGO
WEEE_LOGO
/X

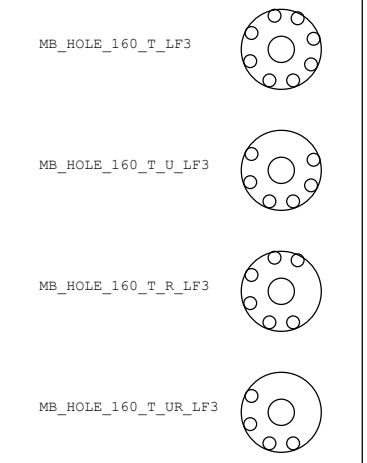
Old Project Logo

Delete it for EMS

ATX Screw Hole



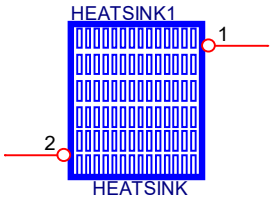
MB SCREW FOOTPRINT



ATX Screw Select

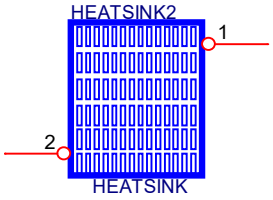
	Standard (12 x 9.6)	Scale down (12 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H9	V	X
H20	V	V
H21	V	V
H22	V	V

Z170-A Heat Sink Part Number:

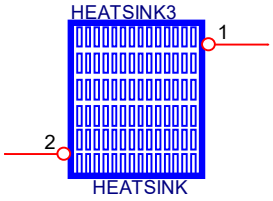


13071-01760000

/X



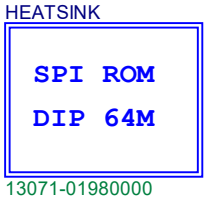
/X



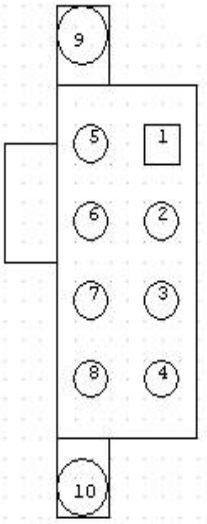
/X

13071-01760600Z170 PRO GAMING HS ASM SET//YS/T-98TM098-01
├(10)13071-01760000Z170 PRO GAMING MOSN HS 2PP//YS/T-80TMA098-01
├(20)13071-01760100Z170 PRO GAMING MOSW HS 2PP//YS/T-80TMB098-01
├(30)13071-01760400Z170 PRO GAMING PCH HS 2PP//YS/T-80TMC098-01

13071-01760700Z170 PRO GAMING HS ASM SET//HSINWEI
├(10)13071-01760300Z170 PRO GAMING MOSN HS 2PP//HW/202296PGX73BK1
├(20)13071-01760200Z170 PRO GAMING MOSW HS 2PP//HW/202295PGX73BK1
├(30)13071-01760500Z170 PRO GAMING PCH HS 2PP//HW/207297PGX14BS0



8 Pin +12V Connector



肅ㄟ: CHL

Z97 : 12015-00053200

+12V_CPU

EATX12V

10

9

8
7
6
5
4
2X4_GND
3
2
1

PWR_2X4P

12015-00053200

GND

BC6
0.1UF/16V
/X/PWR_CON

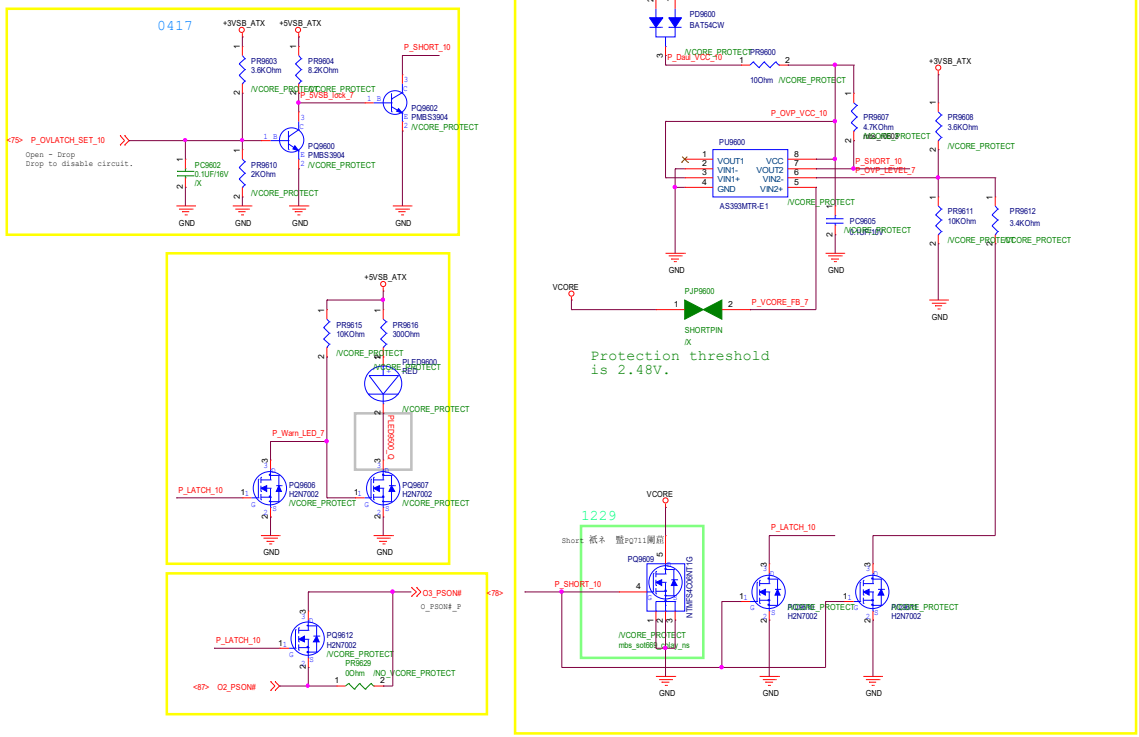
GND

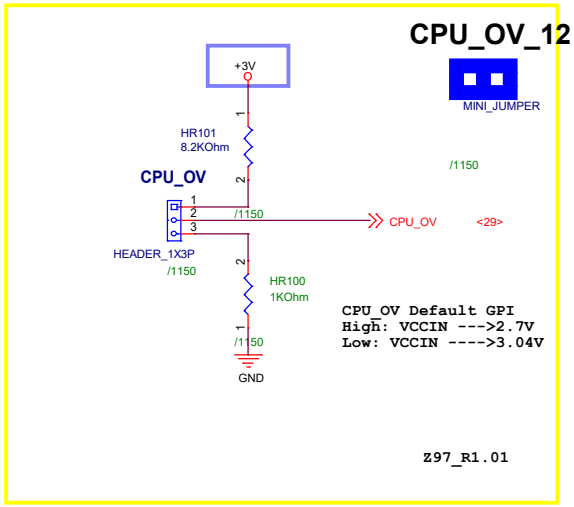
BR1
1KOhm

2X4_POWER_DETECT <33>

USED TO DETECT 2X4 PRESENCE

All Gaming only





MN_LED_SW GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-high/pull-down resistor)
2. stand by power plane, 3V tolerance
3. GPI to turn on Model Name LED
4. GPO low to turn off Model Name LED

5 4 3 2 1

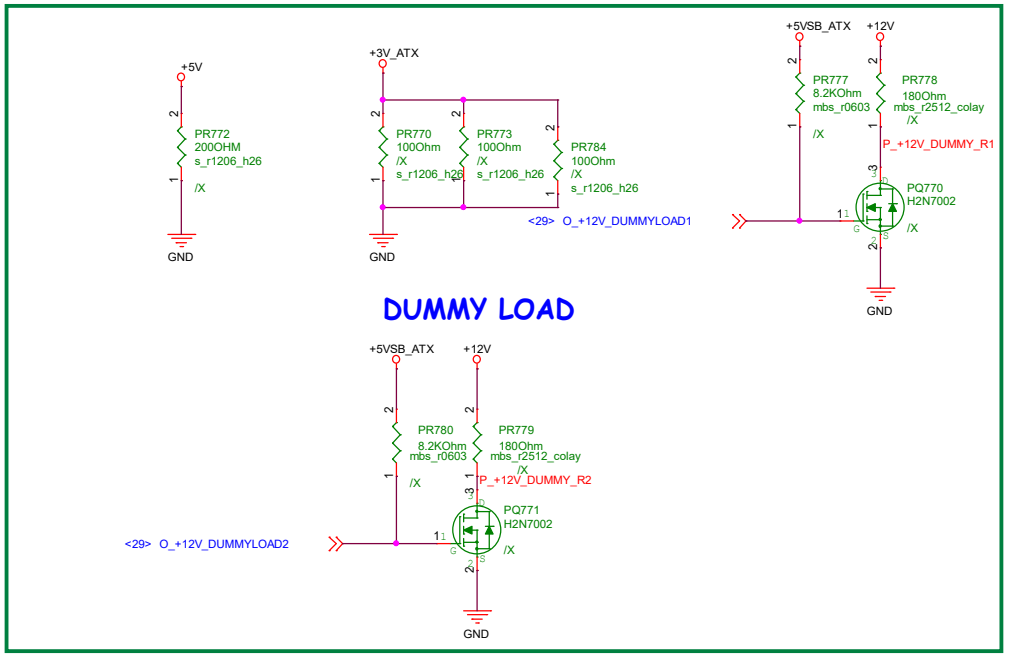
D

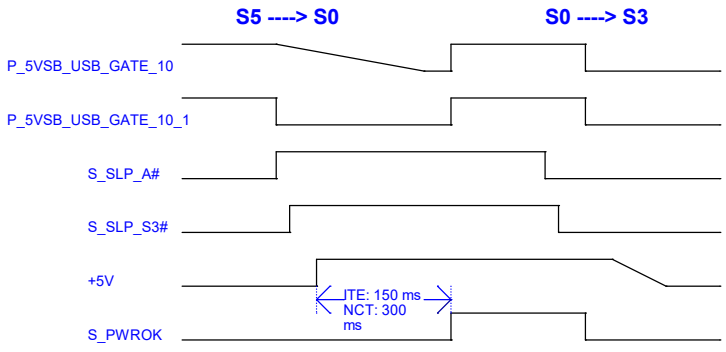
C

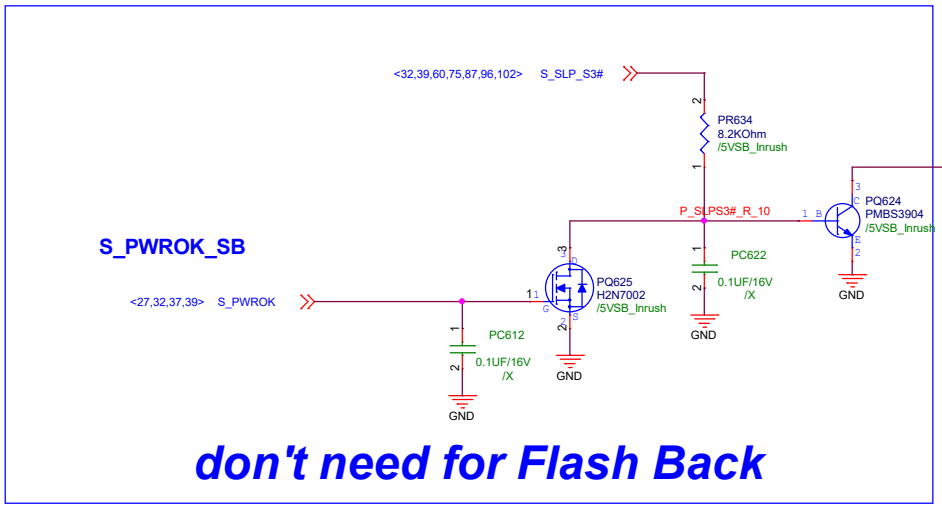
B

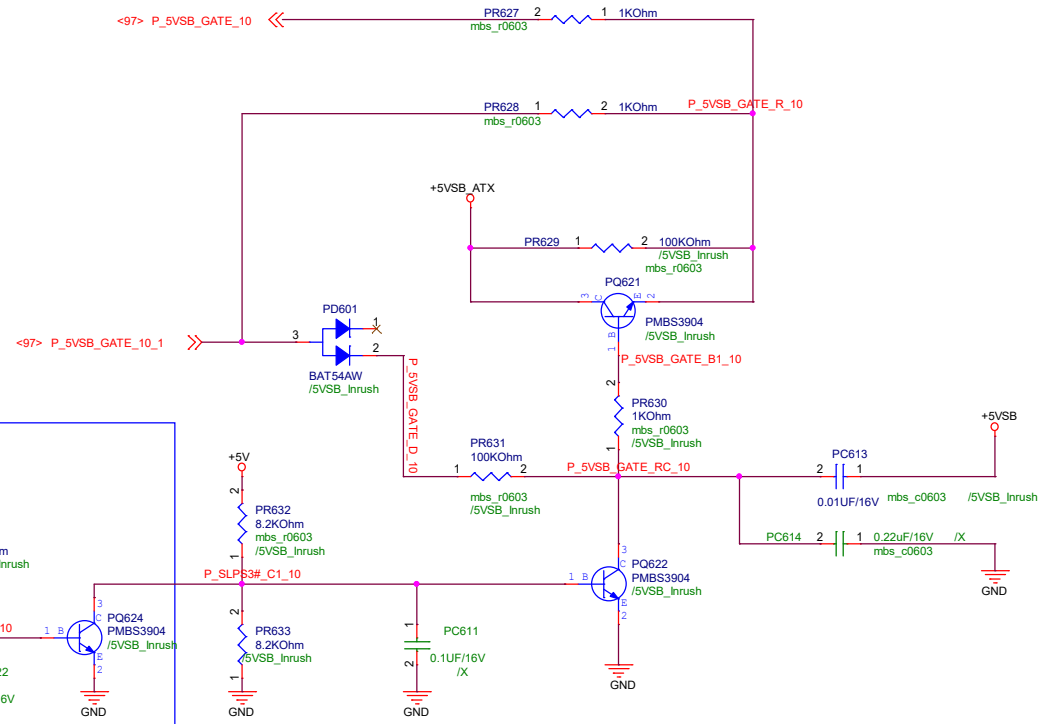
A

+VCCCMP
1.05V 1A

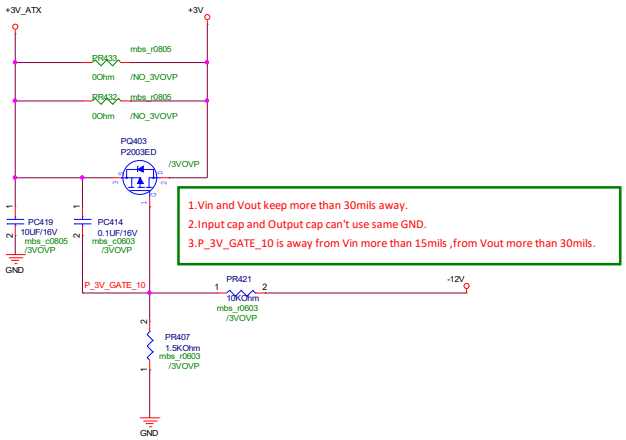

+5V
PR772
200OHM
s_r1206_h26
/X
GND
+3V_ATX
PR770
100Ohm
/X
s_r1206_h26
PR773
100Ohm
/X
s_r1206_h26
PR784
100Ohm
/X
s_r1206_h26
<29> O_+12V_DUMMYLOAD1
GND
+5VSB_ATX
+12V
PR777
8.2KOhm
mbs_r0603
/X
PR778
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R1
PQ770
H2N7002
/X
GND
DUMMY LOAD
+5VSB_ATX
+12V
PR780
8.2KOhm
mbs_r0603
/X
PR779
180Ohm
mbs_r2512_colay
/X
P_+12V_DUMMY_R2
PQ771
H2N7002
/X
<29> O_+12V_DUMMYLOAD2
GND



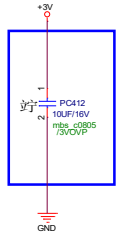




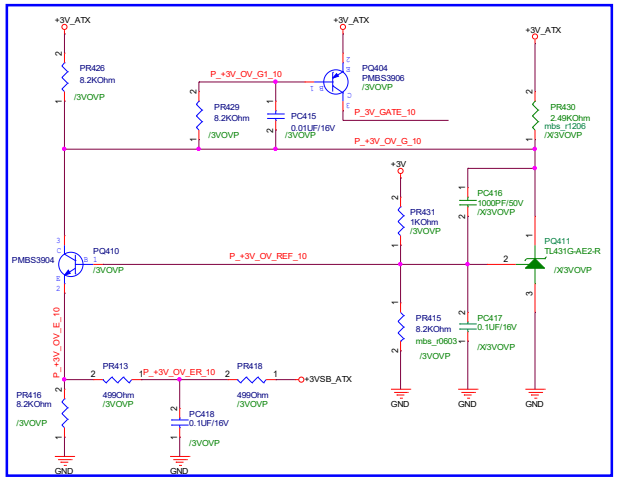
Inrush Circuit for USB Port default have Power or Flash Back Function

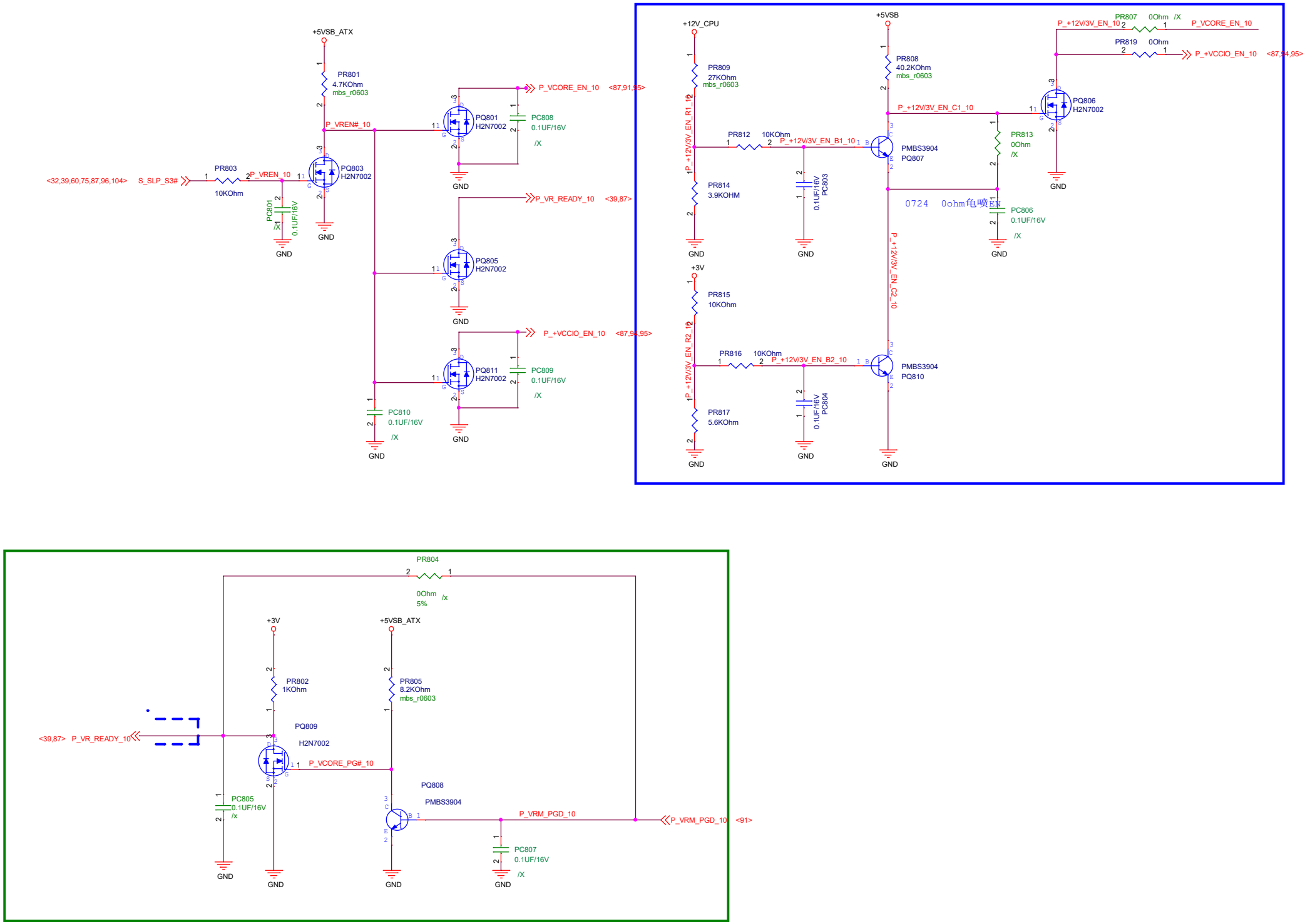


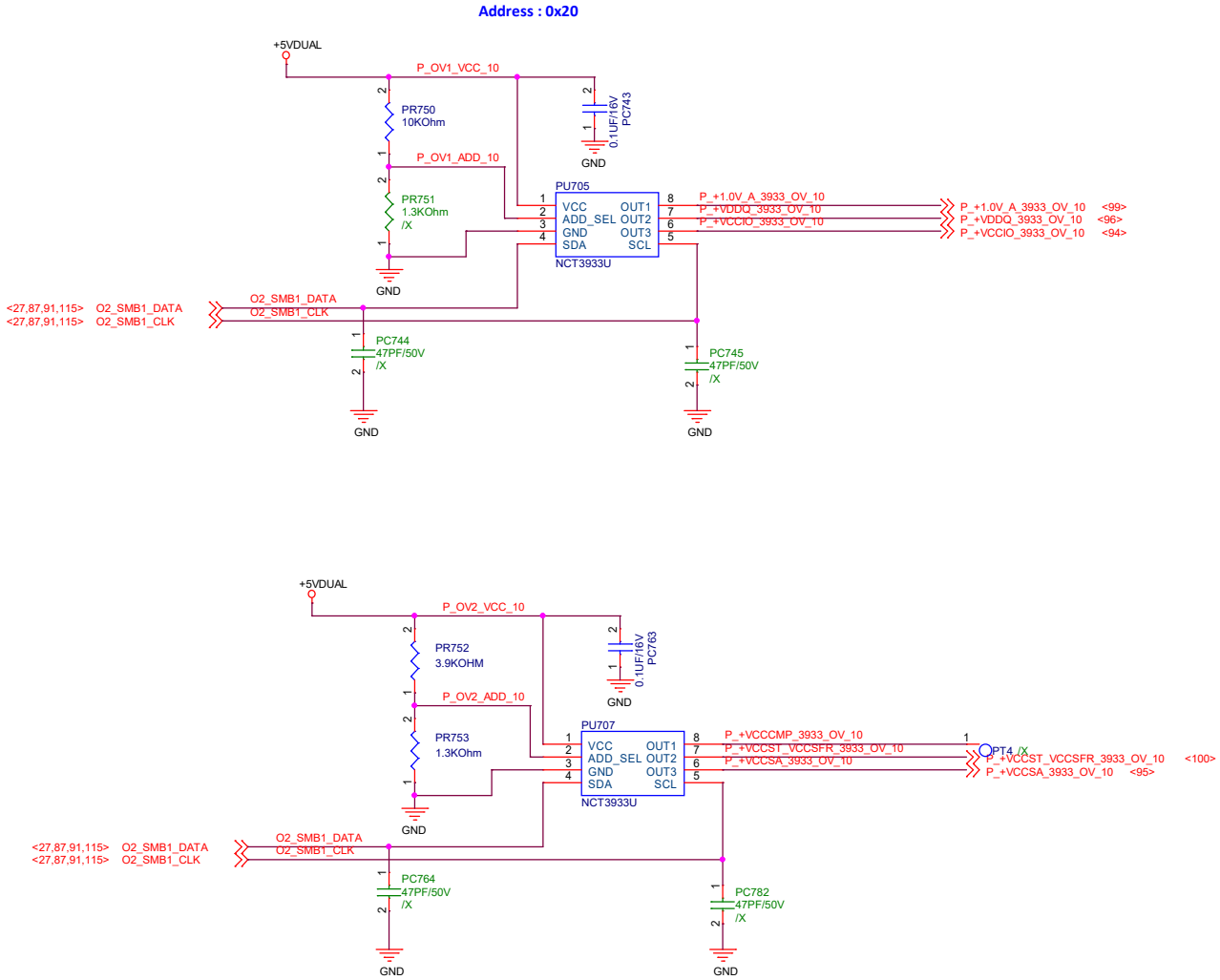
PC412綁併PQ403

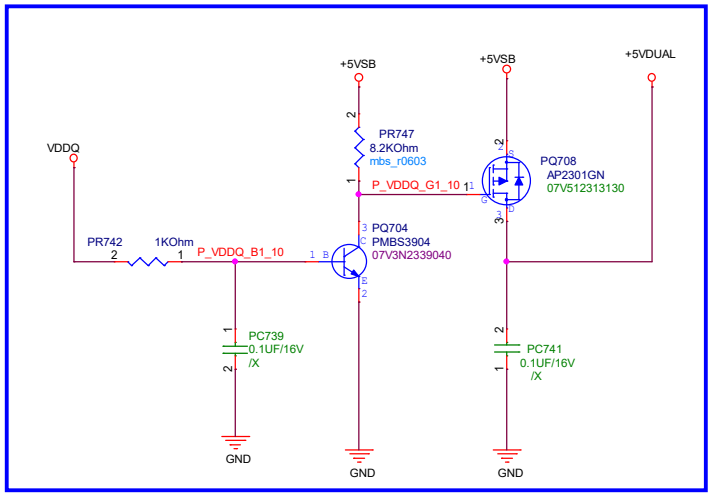


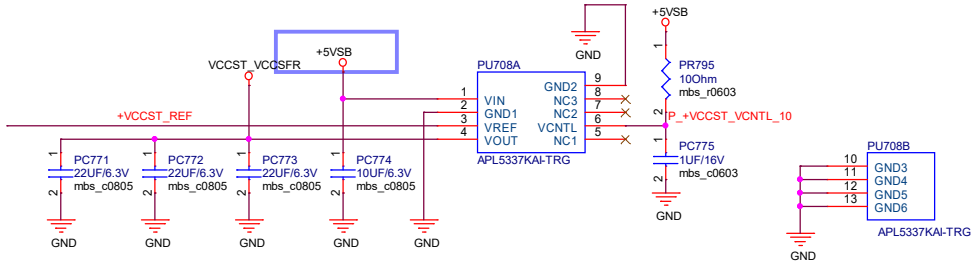
PQ404,PQ410 and other components are better to place close to PQ403.

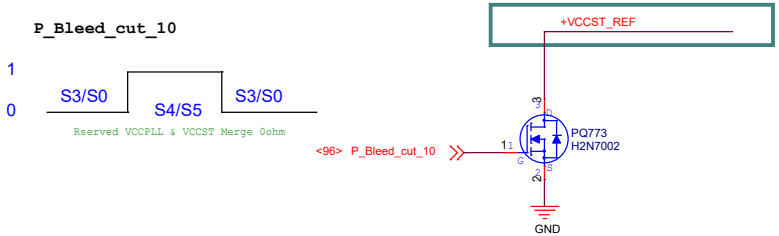


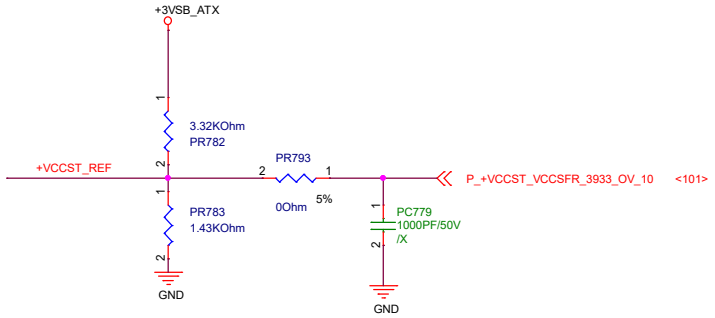

+5VSB_ATX
PR801
4.7KOhm
mbs_r0603
P_VREN#_10
PR803
10KOhm
<32,39,60,75,87,96,104>
S_SLP_S3#
P_VREN_10
PQ803
H2N7002
PC801
/X
0.1UF/16V
GND
PQ801
H2N7002
PC808
0.1UF/16V
/X
P_VCORE_EN_10
<87,91,95>
P_VR_READY_10
<39,87>
PQ805
H2N7002
PQ811
H2N7002
PC809
0.1UF/16V
/X
P_+VCCIO_EN_10
PC810
0.1UF/16V
/X
+12V_CPU
+5VSB
PR809
27KOhm
mbs_r0603
PR808
40.2KOhm
mbs_r0603
P_+12V/3V_EN_R1_10
P_+12V/3V_EN_C1_10
PR812
10KOhm
P_+12V/3V_EN_B1_10
PR814
3.9KOHM
PC803
0.1UF/16V
PMBS3904
PQ807
PR807
0Ohm
/X
P_+12V/3V_EN_10
P_VCORE_EN_10
PR819
0Ohm
P_+VCCIO_EN_10
<87,94,95>
PQ806
H2N7002
PR813
0Ohm
/X
PC806
0.1UF/16V
/X
0724 0ohm龟喷EN
P_+12V/3V_EN_C2_10
+3V
PR815
10KOhm
P_+12V/3V_EN_R2_10
PR816
10KOhm
P_+12V/3V_EN_B2_10
PR817
5.6KOhm
PC804
0.1UF/16V
PMBS3904
PQ810
PR804
0Ohm
5%
/x
PR802
1KOhm
PR805
8.2KOhm
mbs_r0603
PQ809
H2N7002
P_VCORE_PG#_10
PC805
0.1UF/16V
/x
PQ808
PMBS3904
P_VRM_PGD_10
P_VRM_PGD_10
<91>
PC807
0.1UF/16V
/X


Address : 0x20
+5VDUAL
P_OV1_VCC_10
PR750
10KOhm
PC743
0.1UF/16V
GND
P_OV1_ADD_10
PR751
1.3KOhm
/X
PU705
VCC
ADD_SEL
GND
SDA
OUT1
OUT2
OUT3
SCL
NCT3933U
P_+1.0V_A_3933_OV_10
P_+VDDQ_3933_OV_10
P_+VCCIO_3933_OV_10
P_+1.0V_A_3933_OV_10 <99>
P_+VDDQ_3933_OV_10 <96>
P_+VCCIO_3933_OV_10 <94>
<27,87,91,115> O2_SMB1_DATA
<27,87,91,115> O2_SMB1_CLK
O2_SMB1_DATA
O2_SMB1_CLK
PC744
47PF/50V
/X
PC745
47PF/50V
/X
GND
+5VDUAL
P_OV2_VCC_10
PR752
3.9KOHM
PC783
0.1UF/16V
GND
P_OV2_ADD_10
PR753
1.3KOhm
PU707
VCC
ADD_SEL
GND
SDA
OUT1
OUT2
OUT3
SCL
NCT3933U
P_+VCCCMP_3933_OV_10
P_+VCCST_VCCSFR_3933_OV_10
P_+VCCSA_3933_OV_10
PT4 /X
P_+VCCST_VCCSFR_3933_OV_10 <100>
P_+VCCSA_3933_OV_10 <95>
<27,87,91,115> O2_SMB1_DATA
<27,87,91,115> O2_SMB1_CLK
O2_SMB1_DATA
O2_SMB1_CLK
PC764
47PF/50V
/X
PC782
47PF/50V
/X
GND

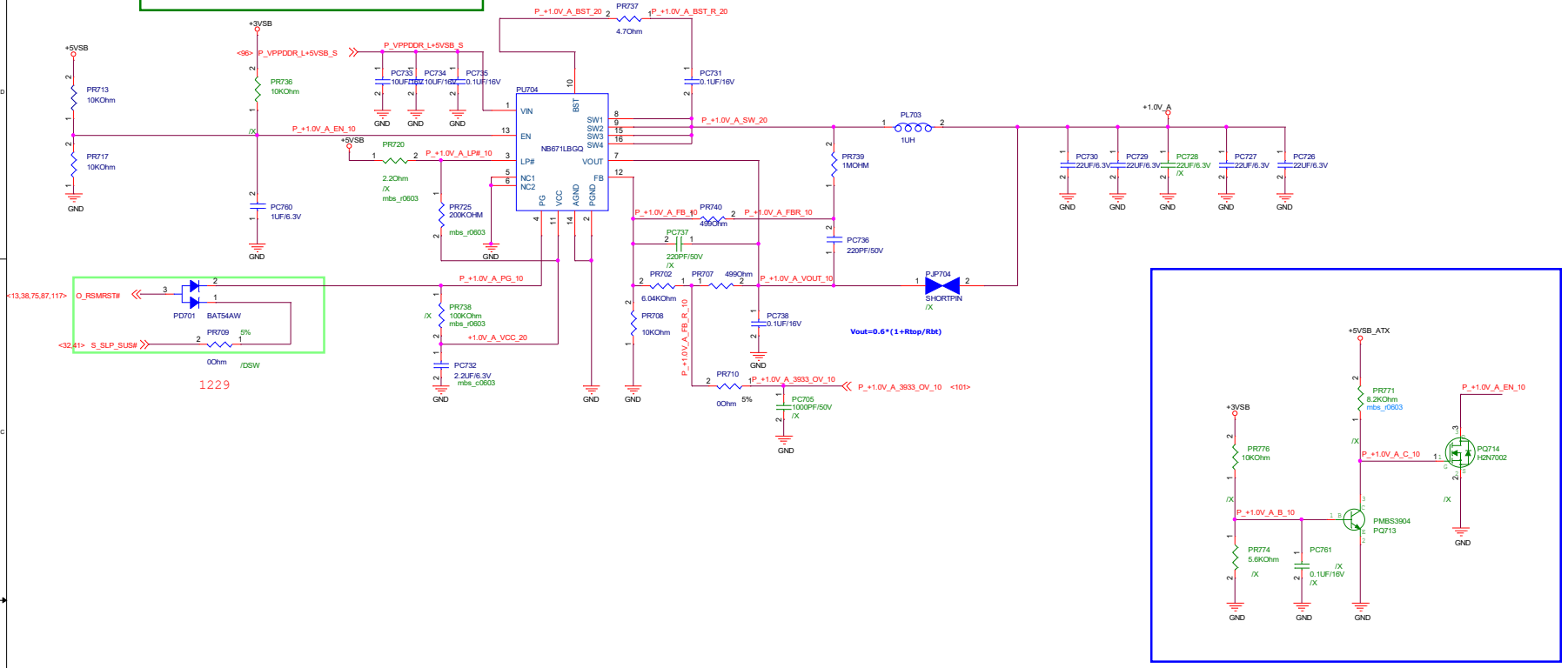

+5VSB
+5VSB
+5VDUAL
VDDQ
PR747
8.2KOhm
mbs_r0603
PQ708
AP2301GN
07V512313130
P_VDDQ_G1_10
PR742
2
1KOhm
1
P_VDDQ_B1_10
PQ704
PMBS3904
07V3N2339040
PC739
0.1UF/16V
/X
PC741
0.1UF/16V
/X
GND
GND
GND


VCCST_VCCSFR
+5VSB
+VCCST_REF
PU708A
GND
VIN
GND1
VREF
VOUT
GND2
NC3
NC2
VCNTL
NC1
APL5337KAI-TRG
+5VSB
PR795
10Ohm
mbs_r0603
P_+VCCST_VCNTL_10
PC775
1UF/16V
mbs_c0603
PC771
22UF/6.3V
mbs_c0805
PC772
22UF/6.3V
mbs_c0805
PC773
22UF/6.3V
mbs_c0805
PC774
10UF/6.3V
mbs_c0805
PU708B
GND3
GND4
GND5
GND6
APL5337KAI-TRG
GND
GND
GND
GND
GND
GND
GND

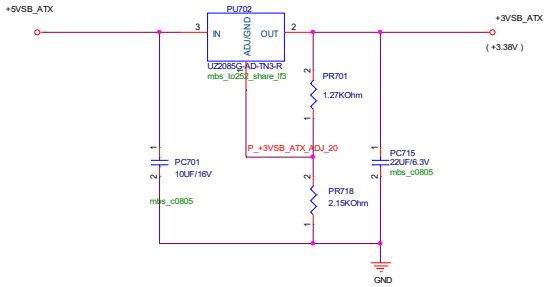

P_Bleed_cut_10
1
0
S3/S0
S4/S5
S3/S0
Rserved VCCPLL & VCCST Merge 0ohm
+VCCST_REF
<96> P_Bleed_cut_10
PQ773
H2N7002
GND


+3VSB_ATX
3.32KOhm
PR782
+VCCST_REF
PR793
0Ohm
5%
P_+VCCST_VCCSFR_3933_OV_10
<101>
PR783
1.43KOhm
PC779
1000PF/50V
/X
GND
GND

If IC is NB671LB,then PR720's optional is /X and PR725's optional is N/A.
If IC is RT6220A,then PR720's optional is N/A and PR725s optional is /X.

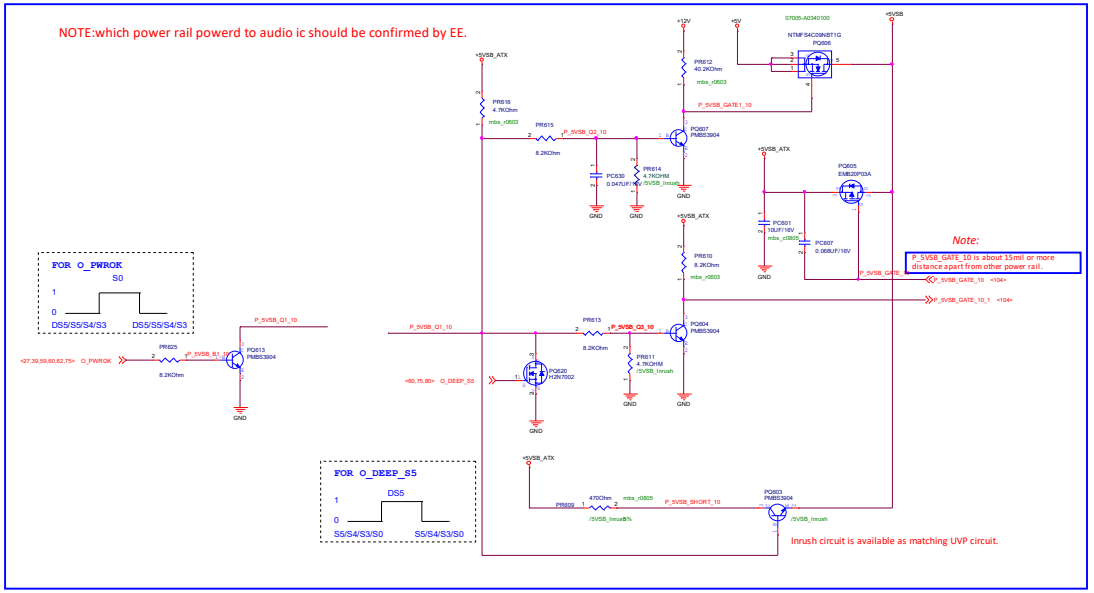


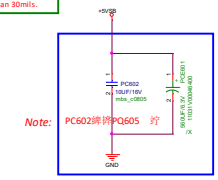
+5VSB_ATX ====>+3VSB_ATX Io:1.5A

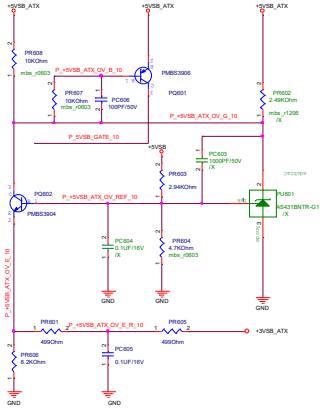


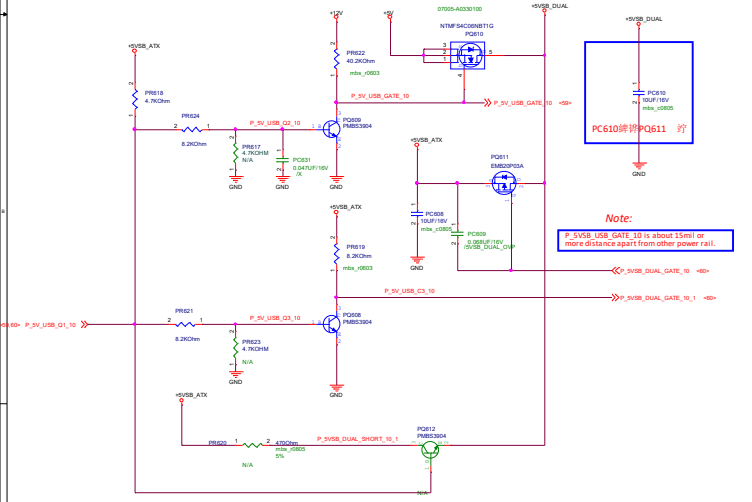
1.Vin and Vout keep more than 30mils away.
2.Input cap and Output cap can't use same GND.
3.P_5VSB_GATE_10 is away from Vin more than 15mils ,from Vout more than 30mils.

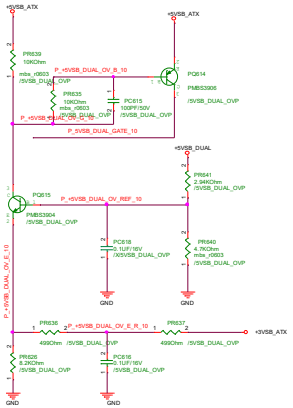
NOTE:which power rail powerd to audio ic should be confirmed by EE.











If iC is NB671LB,then PR521's optional is /X and PR519's optional is N/A.
If iC is RT6220A,then PR521's optional is N/Aand PR519's optional is /X.

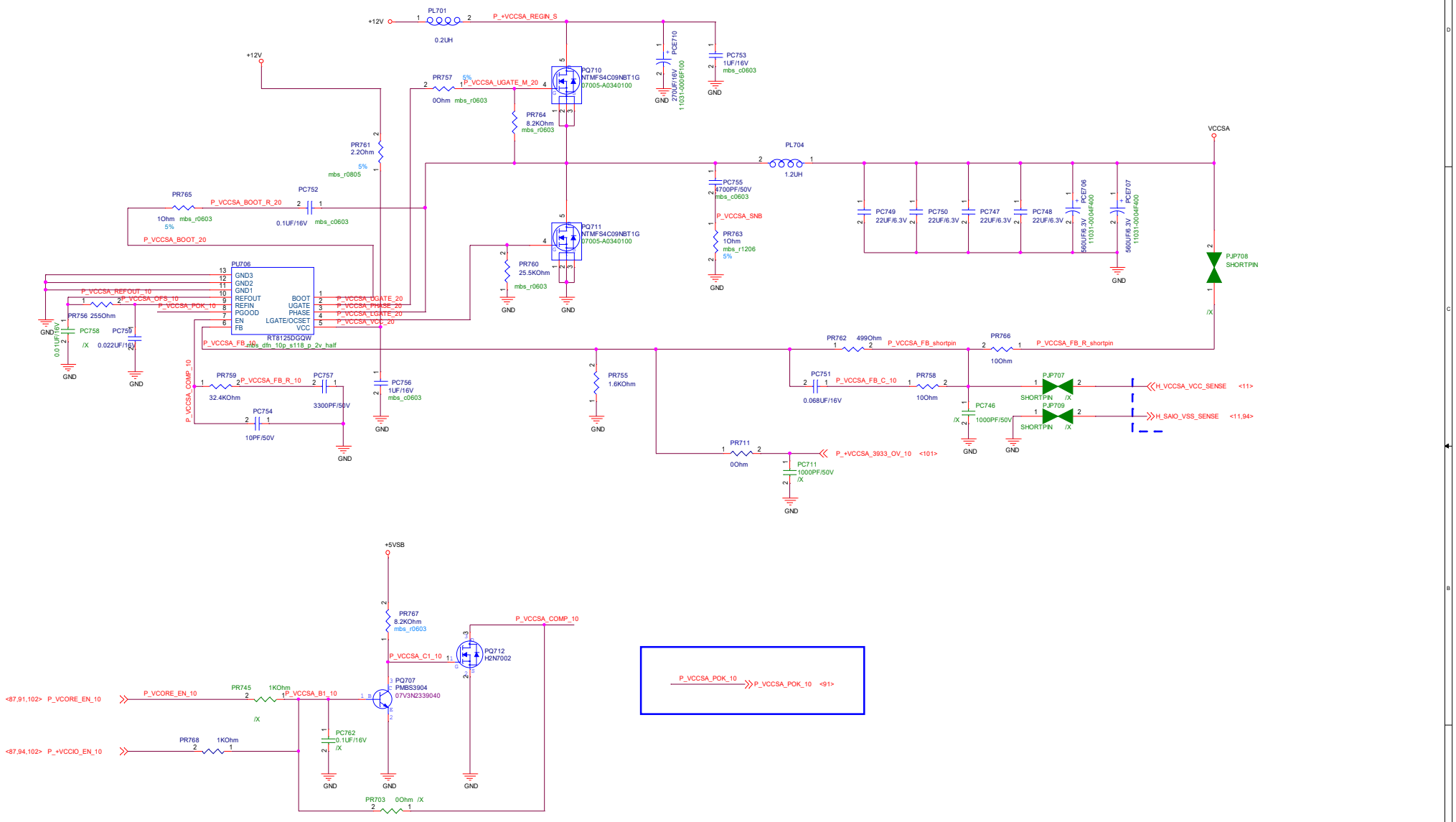
If using P_VDDQ_SIO_EN_10 from SIO control VDDQ EN,then +VPPDDR_PGD_10 need to VPPDDR pull high,that is,PR520 need mounted and PR516 need /X.

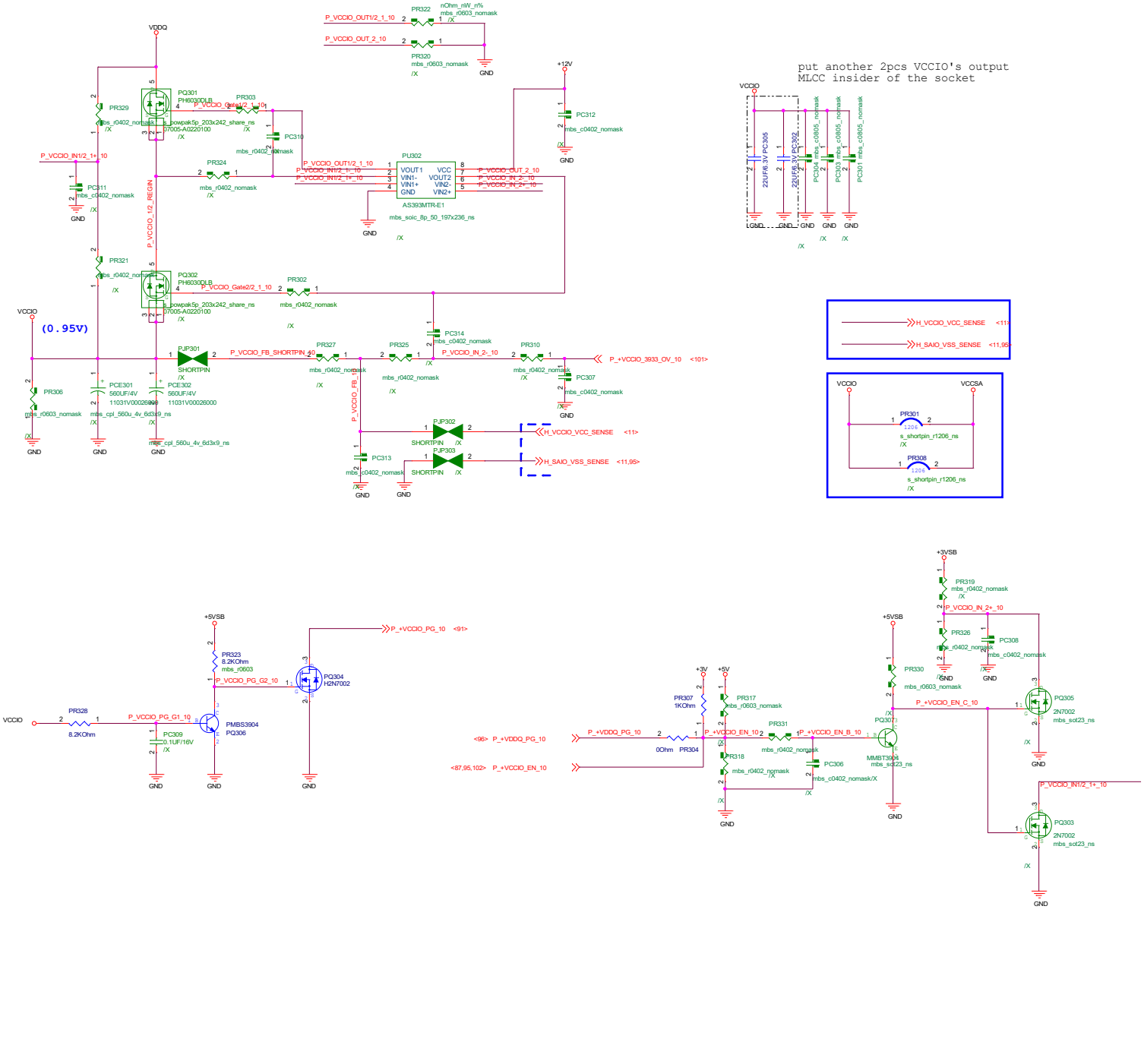
Irms,cin=Io(D(1-D))^0.5

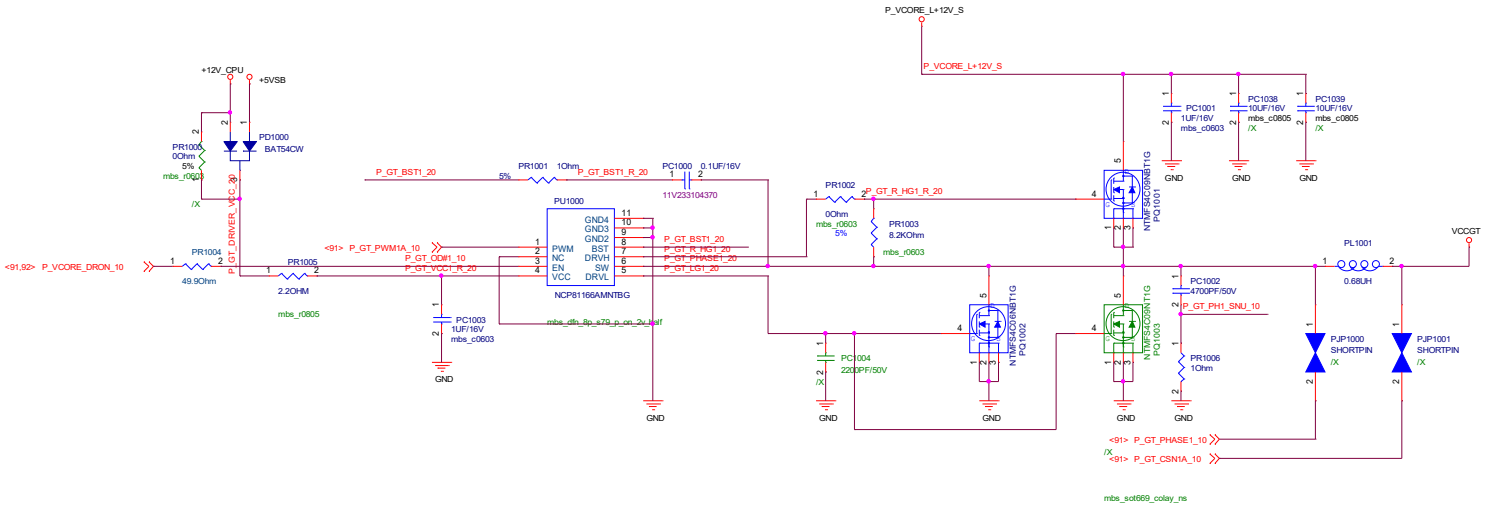
VDDQ Bleed circuit

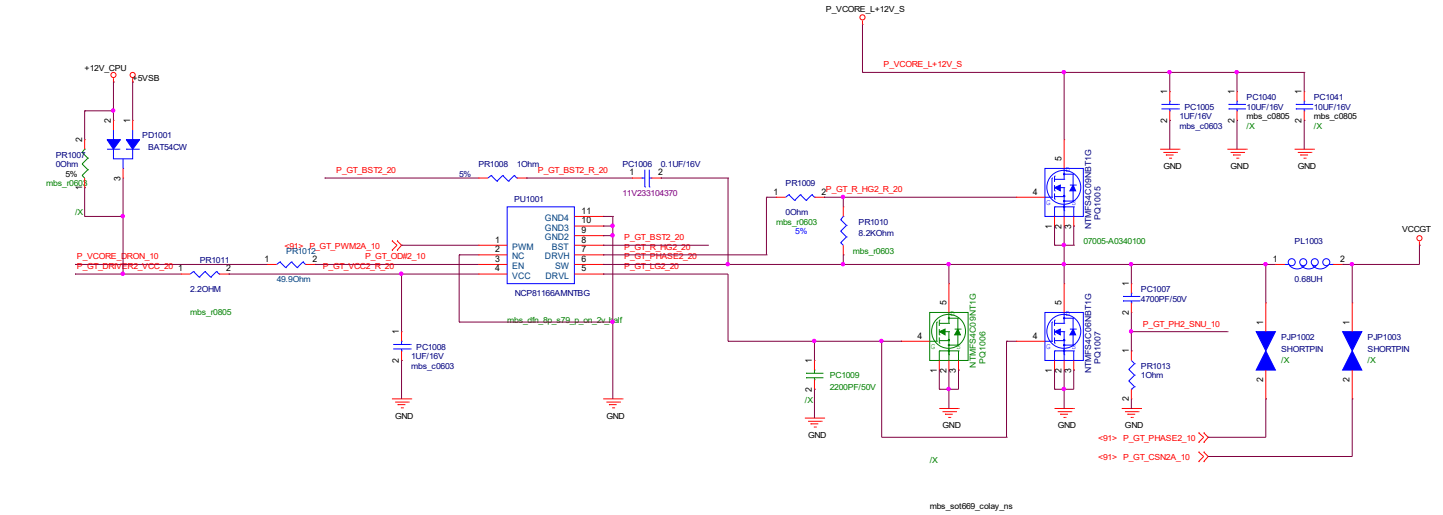
VDDQ ===> VTT_DDR
Io:0.75A
combine RT9040

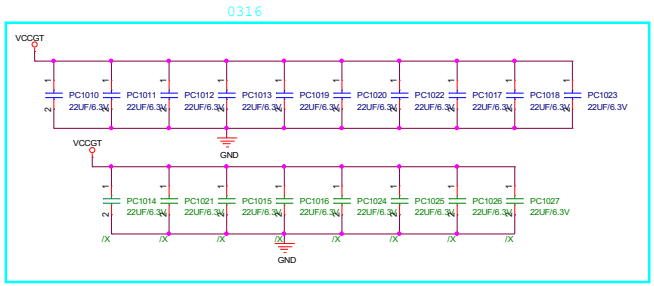
If we use P_VDDQ_SIO_EN_10 from SIO to control VDDQ EN,then PR573,PQ506,PR574,PR507,PQ505 need mounted.Otherwise,we still use S_SLP_S4# and +VPPDDR_PGD_10 to control VDDQ EN.

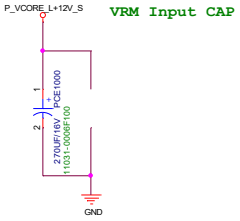

PL701
+12V
P_+VCCSA_REGIN_S
0.2UH
PCE710
270UF/16V
11001-0005F100
PC753
1UF/16V
mbs_c0603
GND
PR757
5%
P_VCCSA_UGATE_M_20
0Ohm mbs_r0603
PQ710
NTMFS4C09NBT1G
D7005-A0340100
PR764
8.2KOhm
mbs_r0603
PR761
2.2Ohm
5%
mbs_r0805
PR765
P_VCCSA_BOOT_R_20
1Ohm mbs_r0603
5%
PC752
0.1UF/16V mbs_c0603
P_VCCSA_BOOT_20
PQ711
NTMFS4C09NBT1G
D7005-A0340100
PR760
25.5KOhm
mbs_r0603
PL704
1.2UH
PC755
4700PF/50V
mbs_c0603
P_VCCSA_SNB
PR763
1Ohm
mbs_r1206
5%
PC749
22UF/6.3V
PC750
22UF/6.3V
PC747
22UF/6.3V
PC748
22UF/6.3V
PCE706
560UF/6.3V
11031-0004F400
PCE707
560UF/6.3V
11031-0004F400
VCCSA
PJP708
SHORTPIN
/X
PU706
GND3
GND2
GND1
REFOUT
REFIN
PGOOD
EN
FB
BOOT
UGATE
PHASE
LGATE/OCSET
VCC
RT8125DGQW
mbs_dfn_10p_s118_p_2v_half
P_VCCSA_REFOUT_10
P_VCCSA_OPS_10
P_VCCSA_POK_10
P_VCCSA_FB_10
P_VCCSA_UGATE_20
P_VCCSA_PHASE_20
P_VCCSA_LGATE_20
P_VCCSA_VCC_20
PR756 255Ohm
PC758
0.01UF/50V
/X
PC759
0.022UF/16V
/X
PR759
32.4KOhm
P_VCCSA_FB_R_10
PR757
3300PF/50V
PC754
10PF/50V
P_VCCSA_COMP_10
PC756
1UF/16V
mbs_c0603
PR755
1.6KOhm
PR762
499Ohm
P_VCCSA_FB_shortpin
PR766
10Ohm
P_VCCSA_FB_R_shortpin
PC751
0.068UF/16V
P_VCCSA_FB_C_10
PR758
10Ohm
PJP707
SHORTPIN
/X
H_VCCSA_VCC_SENSE
<11>
PC746
1000PF/50V
/X
PJP709
SHORTPIN
/X
H_SAIO_VSS_SENSE
<11,94>
PR711
0Ohm
P_+VCCSA_3933_OV_10
<101>
PC711
1000PF/50V
/X
+5VSB
PR767
8.2KOhm
mbs_r0603
P_VCCSA_C1_10
PQ712
H2N7002
P_VCCSA_COMP_10
PQ707
PMBS3904
07V3N2339040
P_VCCSA_B1_10
<87,91,102> P_VCORE_EN_10
PR745
1KOhm
/X
<87,94,102> P_+VCCIO_EN_10
PR768
1KOhm
PC762
0.1UF/16V
/X
PR703
0Ohm
/X
P_VCCSA_POK_10
P_VCCSA_POK_10
<91>

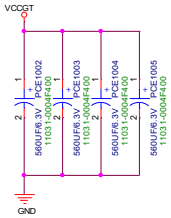

put another 2pcs VCCIO's output
MLCC insider of the socket
VDDQ
VCCIO
(0.95V)
+12V
+5VSB
+3V
+3VSB
VCCSA
GND
PU302
AS393MTR-E1
PQ301
PH6030DLB
PQ302
PJP301
PJP302
PJP303
SHORTPIN
PQ304
H2N7002
PQ305
PQ303
2N7002
PMBS3904
MMBT3904
P_VCCIO_1/2_REGN
P_VCCIO_FB_1
P_VCCIO_FB_SHORTPIN_10
P_VCCIO_PG_G1_10
P_VCCIO_PG_G2_10
P_VCCIO_EN_C_10
P_VCCIO_IN1/2_1+_10
P_VCCIO_IN_2-_10
P_VCCIO_IN_2+_10
P_+VCCIO_3933_OV_10
P_+VCCIO_PG_10
P_+VDDQ_PG_10
P_+VCCIO_EN_10
P_+VCCIO_EN_B_10
H_VCCIO_VCC_SENSE
H_SAIO_VSS_SENSE
PR301
PR308
s_shortpin_r1206_ns

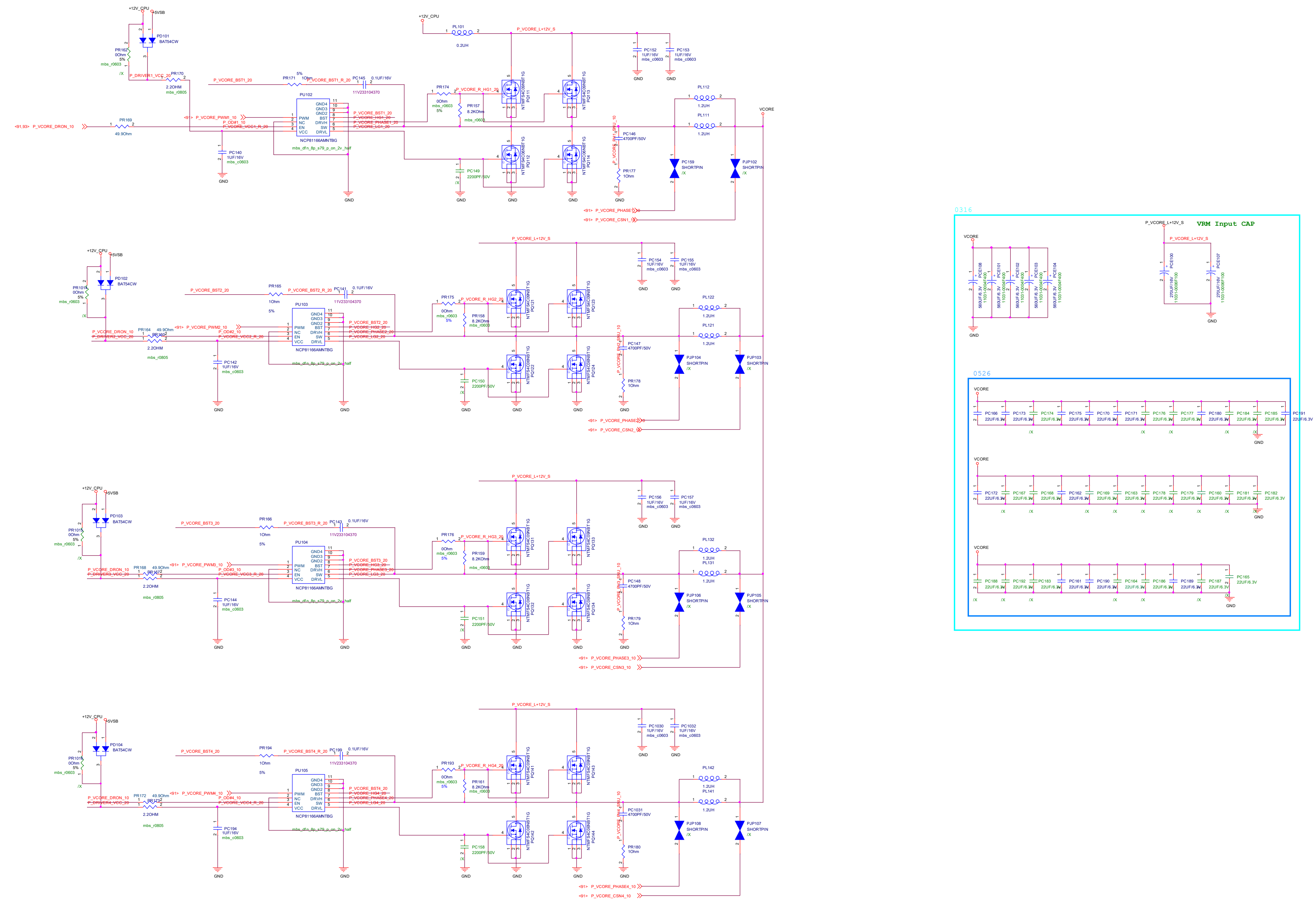

P_VCORE_L+12V_S
+12V_CPU
+5VSB
PD1000
BAT54CW
PR1000
0Ohm
5%
mbs_r0603
/X
P_GT_DRIVER_VCC_20
P_GT_BST1_20
PR1001 1Ohm
5%
P_GT_BST1_R_20
PC1000 0.1UF/16V
11V233104370
PU1000
GND4
GND3
GND2
PWM
BST
NC
DRVH
EN
SW
VCC
DRVL
NCP81166AMNTBG
<91> P_GT_PWM1A_10
P_GT_ODI1_10
P_GT_VCC1_R_20
P_GT_BST1_20
P_GT_R_HG1_20
P_GT_PHASE1_20
P_GT_LG1_20
PR1002
0Ohm
mbs_r0603
5%
PR1003
8.2KOhm
mbs_r0603
PR1004
49.9Ohm
PR1005
2.2OHM
mbs_r0805
<91,92> P_VCORE_DRON_10
PC1001
1UF/16V
mbs_c0603
PC1038
10UF/16V
mbs_c0805
/X
PC1039
10UF/16V
mbs_c0805
/X
GND
NTMFS4C06NBT1G
PQ1001
NTMFS4C09NT1G
PQ1003
NTMFS4C09NBT1G
PQ1002
PC1003
1UF/16V
mbs_c0603
PC1004
2200PF/50V
/X
PC1002
4700PF/50V
P_GT_PH1_SNU_10
PR1006
1Ohm
PL1001
0.68UH
VCCGT
PJP1000
SHORTPIN
/X
PJP1001
SHORTPIN
/X
<91> P_GT_PHASE1_10
<91> P_GT_CSN1A_10
mbs_dfn_8p_s79_p_on_2v_leaf
mbs_sot669_colay_ns

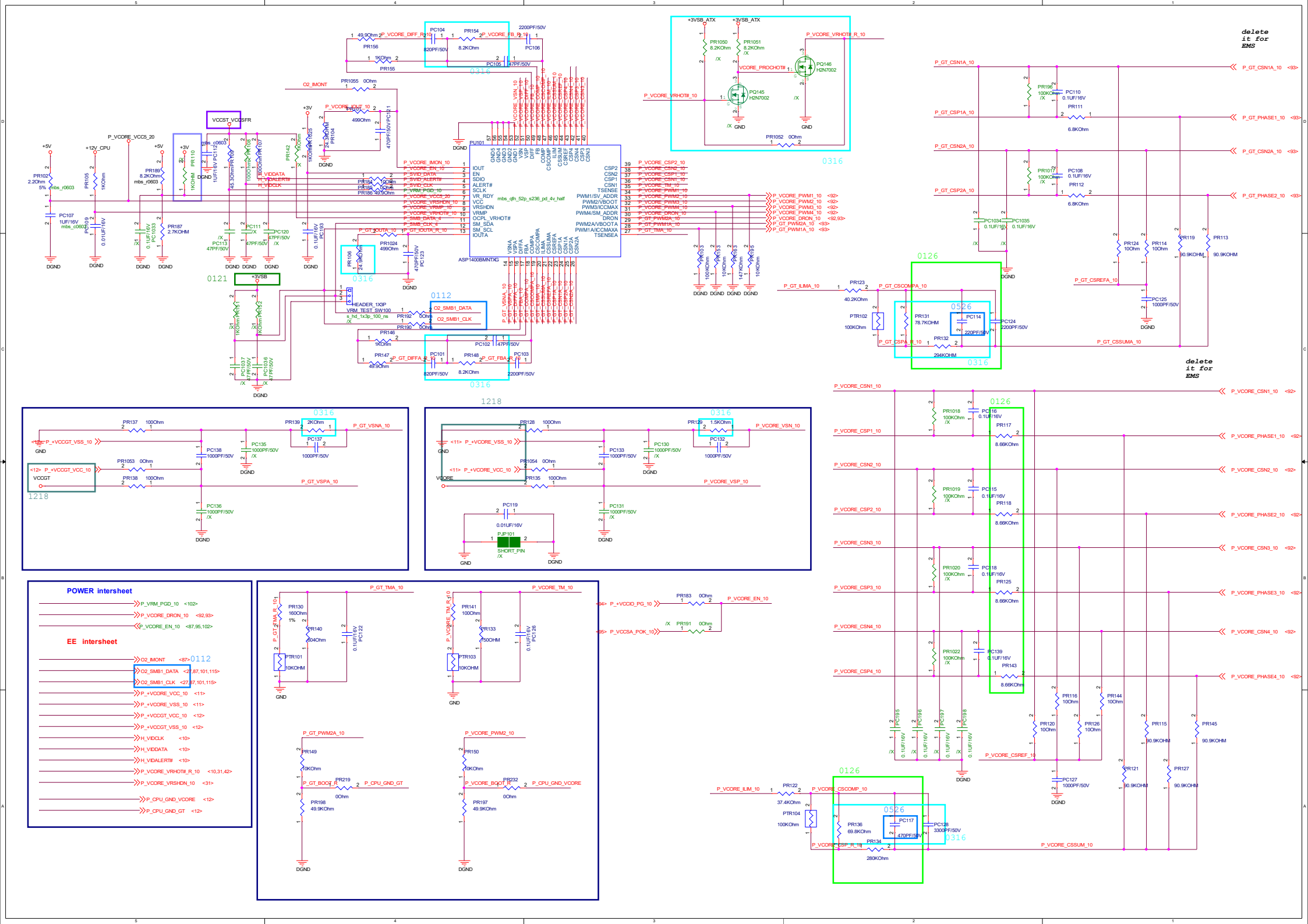

P_VCORE_L+12V_S
+12V_CPU
5VSB
PD1001
BAT54CW
PR1007
0Ohm
5%
mbs_r0603
/X
P_GT_BST2_20
PR1008 1Ohm
5%
P_GT_BST2_R_20
PC1006 0.1UF/16V
11V233104370
PU1001
GND4
GND3
GND2
PWM
BST
NC
DRVH
EN
SW
VCC
DRVL
NCP81166AMNTBG
<91> P_GT_PWM2A_10
P_GT_ODI2_10
P_GT_VCC2_R_20
P_GT_BST2_20
P_GT_R_HG2_20
P_GT_PHASE2_20
P_GT_LG2_20
PR1009
0Ohm
mbs_r0603
5%
PR1010
8.2KOhm
mbs_r0603
PR1012
49.9Ohm
PR1011
2.2OHM
mbs_r0805
P_VCORE_DRON_10
P_GT_DRIVER_VCC_20
PC1005
1UF/16V
mbs_c0603
PC1040
10UF/16V
mbs_c0805
/X
PC1041
10UF/16V
mbs_c0805
/X
GND
NTMFS4C09NT1G
PQ1005
07005-A0340100
NTMFS4C09NT1G
PQ1006
NTMFS4C06NBT1G
PQ1007
PC1008
1UF/16V
mbs_c0603
PC1009
2200PF/50V
/X
PC1007
4700PF/50V
P_GT_PH2_SNU_10
PR1013
1Ohm
PL1003
0.68UH
VCCGT
PJP1002
SHORTPIN
/X
PJP1003
SHORTPIN
/X
<91> P_GT_PHASE2_10
<91> P_GT_CSN2A_10
mbs_dfn_8p_s79_p_on_2v_leaf
mbs_sot669_colay_ns


0316
VCCGT
PC1010
PC1011
PC1012
PC1013
PC1019
PC1020
PC1022
PC1017
PC1018
PC1023
22UF/6.3V
GND
PC1014
PC1021
PC1015
PC1016
PC1024
PC1025
PC1026
PC1027
/X


P_VCORE_L+12V_S
VRM Input CAP
PCE1000
270UF/16V
11031-0006F100
GND

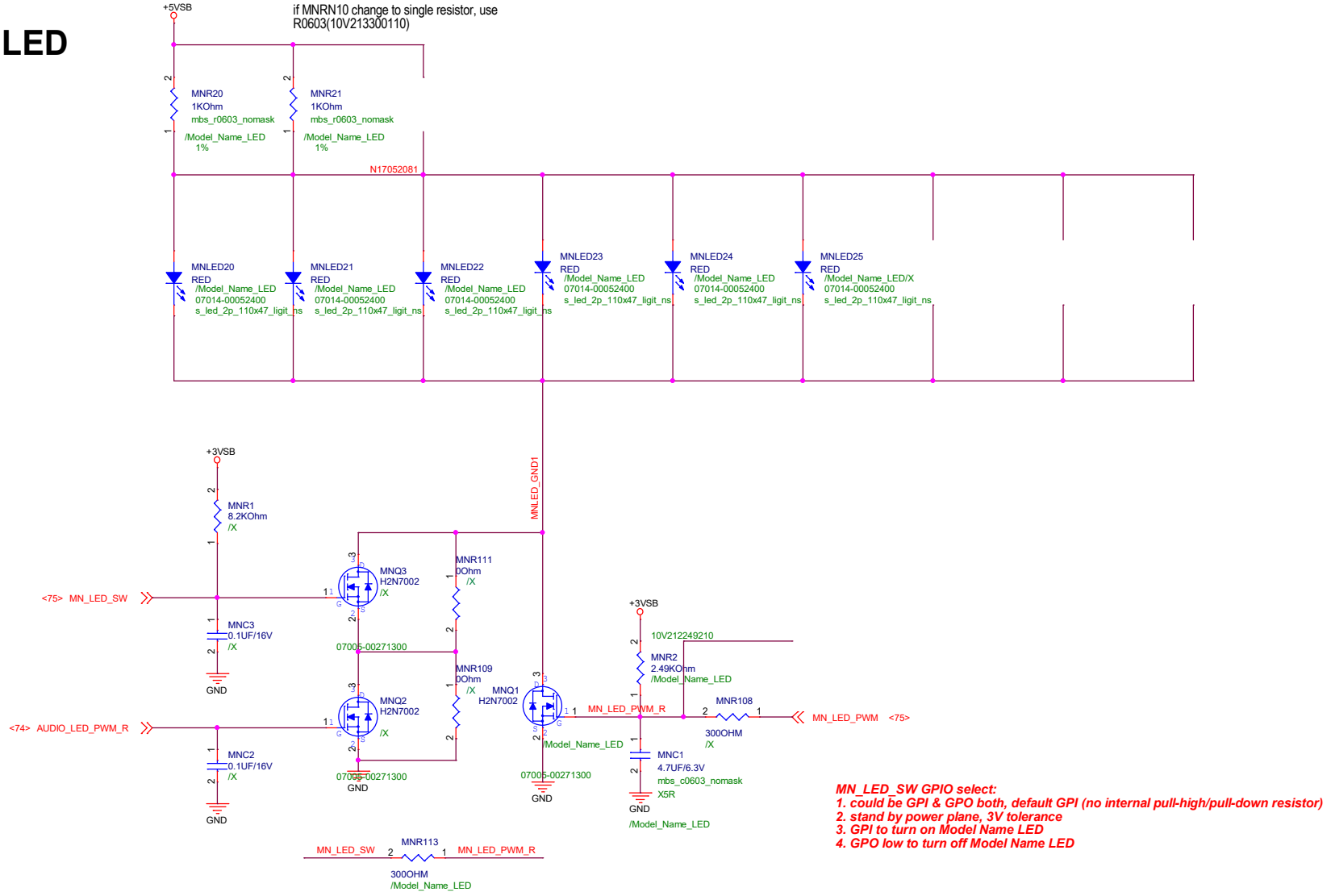

VCCGT
PCE1002
PCE1003
PCE1004
PCE1005
560UF/6.3V
11031-0004F400
GND


+12V_CPU
5VSB
PD101
BAT54CW
PR162
0Ohm
5%
mbs_r0603
/X
P_DRIVER1_VCC_20
PR170
2.2OHM
mbs_r0805
P_VCORE_BST1_20
PR171
1Ohm
5%
P_VCORE_BST1_R_20
PC145
0.1UF/16V
11V233104370
PU102
NCP81166AMNTBG
mbs_dfn_8p_s79_p_on_2v_half
GND4
GND3
GND2
BST
DRVH
SW
DRVL
PWM
NC
EN
VCC
<91> P_VCORE_PWM1_10
P_OD#1_10
P_VCORE_VCC1_R_20
<91,93> P_VCORE_DRON_10
PR169
49.9Ohm
PC140
1UF/16V
mbs_c0603
GND
P_VCORE_HG1_20
P_VCORE_PHASE1_20
P_VCORE_LG1_20
PL101
0.2UH
P_VCORE_L+12V_S
PR174
P_VCORE_R_HG1_20
PR157
8.2KOhm
PC149
2200PF/50V
PQ111
PQ112
PQ113
PQ114
NTMFS4C09NT1G
PC152
1UF/16V
mbs_c0603
PC153
1UF/16V
mbs_c0603
PL112
1.2UH
PL111
1.2UH
VCORE
PC146
4700PF/50V
PR177
1Ohm
PC159
SHORTPIN
PJP102
SHORTPIN
<91> P_VCORE_PHASE1_10
<91> P_VCORE_CSN1_10
PD102
PR1015
PU103
PC141
PR165
P_VCORE_BST2_20
<91> P_VCORE_PWM2_10
PR164
PC142
PR175
PR158
PC150
PQ121
PQ122
PQ123
PQ124
PC154
PC155
PL122
PL121
PC147
PR178
PJP104
PJP103
<91> P_VCORE_PHASE2_10
<91> P_VCORE_CSN2_10
PD103
PU104
PC143
PR166
P_VCORE_BST3_20
PR168
PC144
PR176
PR159
PC151
PQ131
PQ132
PQ133
PQ134
PC156
PC157
PL132
PL131
PC148
PR179
PJP106
PJP105
<91> P_VCORE_PHASE3_10
<91> P_VCORE_CSN3_10
PD104
PU105
PC199
PR194
P_VCORE_BST4_20
<91> P_VCORE_PWM4_10
PR172
PC194
PR193
PR161
PC158
PQ141
PQ142
PQ143
PQ144
PC1030
PC1032
PL142
PL141
PC1031
PR180
PJP108
PJP107
<91> P_VCORE_PHASE4_10
<91> P_VCORE_CSN4_10
0316
VRM Input CAP
P_VCORE_L+12V_S
PCE106
PCE101
PCE102
PCE103
PCE104
560UF/6.3V
PCE100
PCE107
270UF/16V
0526
PC166
PC173
PC174
PC175
PC170
PC171
PC176
PC177
PC180
PC184
PC185
PC191
PC172
PC167
PC168
PC162
PC169
PC163
PC178
PC179
PC160
PC181
PC182
PC188
PC192
PC183
PC161
PC190
PC164
PC186
PC189
PC187
PC165
22UF/6.3V

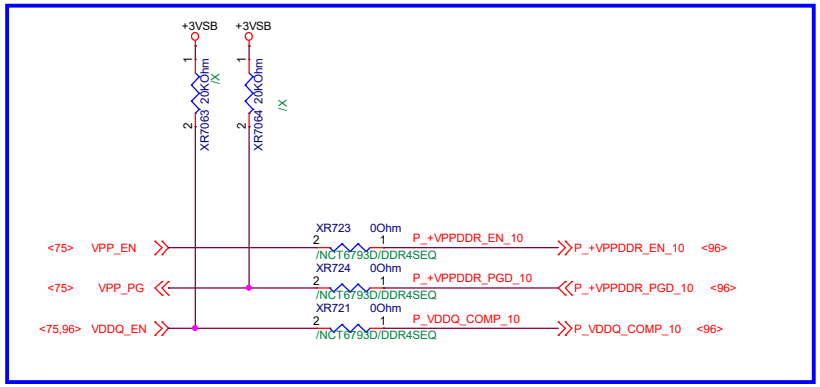

delete it for EMS
delete it for EMS
POWER intersheet
P_VRM_PGD_10 <102>
P_VCORE_DRON_10 <92,93>
P_VCORE_EN_10 <87,95,102>
EE intersheet
O2_IMONT <87>
O2_SMB1_DATA <27,87,101,115>
O2_SMB1_CLK <27,87,101,115>
P_+VCORE_VCC_10 <11>
P_+VCORE_VSS_10 <11>
P_+VCCGT_VCC_10 <12>
P_+VCCGT_VSS_10 <12>
H_VIDCLK <10>
H_VIDDATA <10>
H_VIDALERT# <10>
P_VCORE_VRHOT#_R_10 <10,31,42>
P_VCORE_VRSHDN_10 <31>
P_CPU_GND_VCORE <12>
P_CPU_GND_GT <12>
ASP1400BMNTXG
mbs_qfn_52p_s236_pd_4v_half

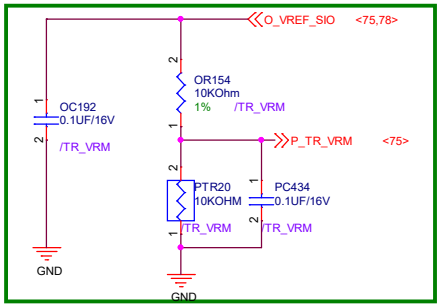
Model Name LED

Model Name LED
Yellow: 07014-00090400
Red : 07G015700750



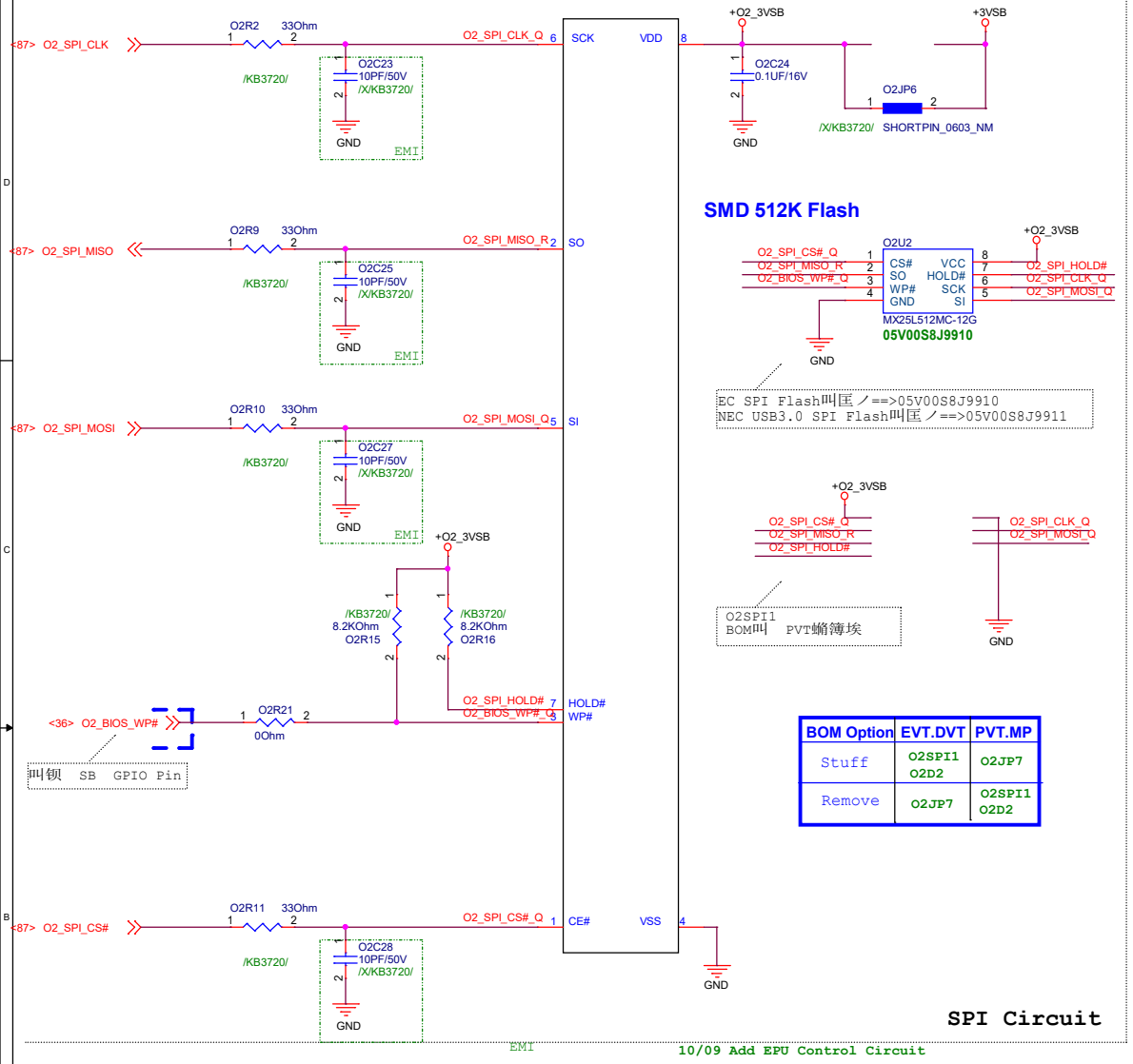
MN_LED_SW GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-high/pull-down resistor)
2. stand by power plane, 3V tolerance
3. GPI to turn on Model Name LED
4. GPO low to turn off Model Name LED





FOR POWER TR FOR COST

0.7B Beta

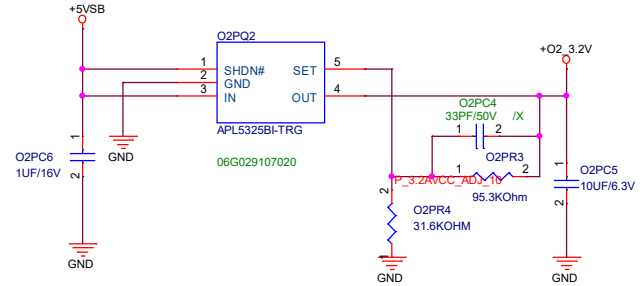


SMD 512K Flash

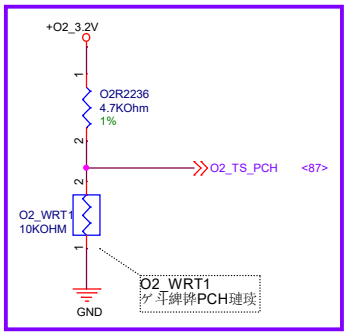
EC SPI Flash叫匡ノ==>05V00S8J9910
NEC USB3.0 SPI Flash叫匡ノ==>05V00S8J9911

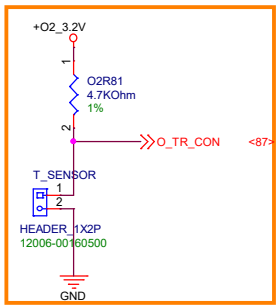
BOM Option	EVT.DVT	PVT.MP
Stuff	O2SPI1 O2D2	O2JP7
Remove	O2JP7	O2SPI1 O2D2

璜ADC/PWM VREF匡ノ+3VSB玥LDO紡隔 埃



*Vout=0.8 * (1 + R_hign/R_low) = 3.214V*

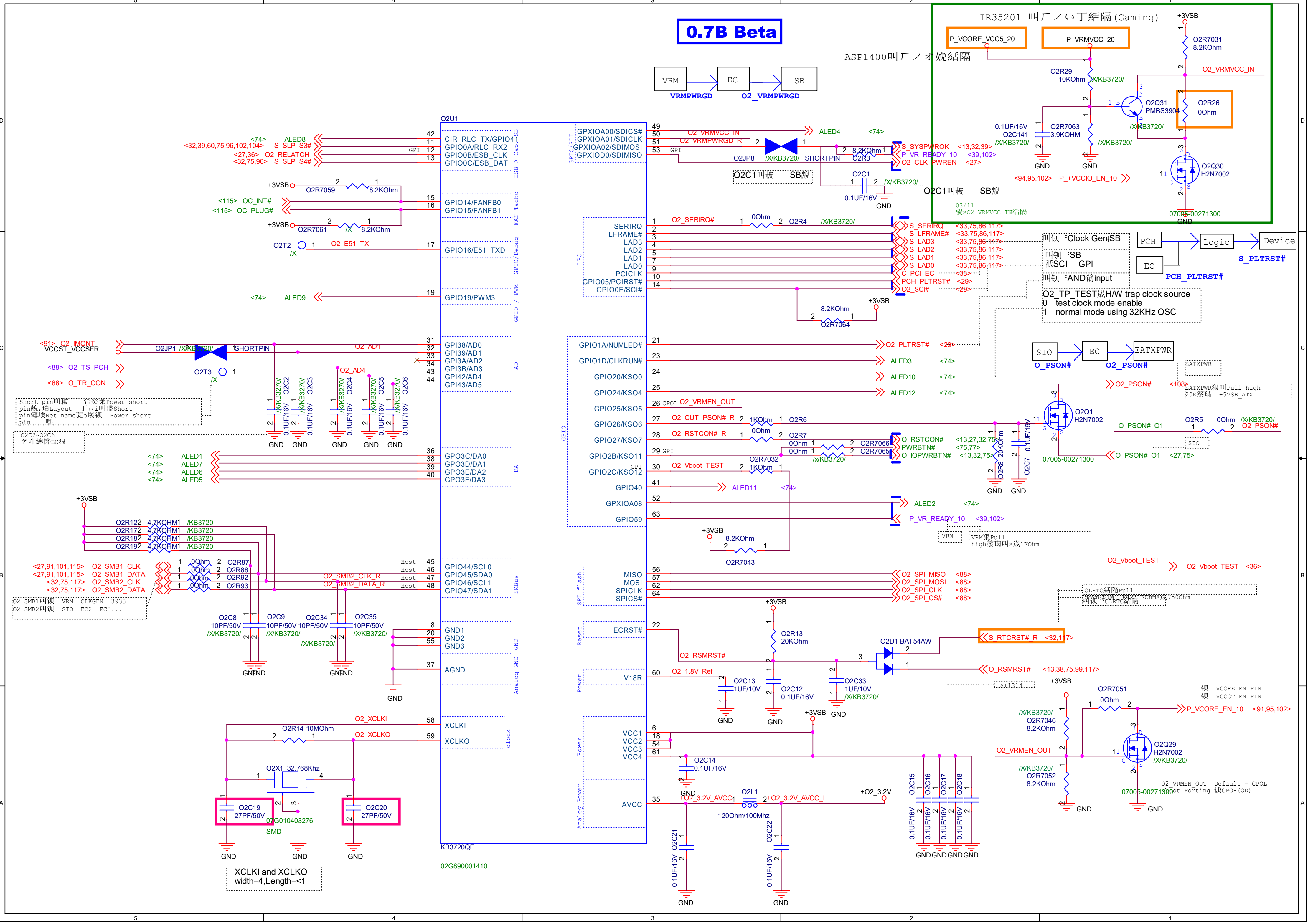




SPI Circuit

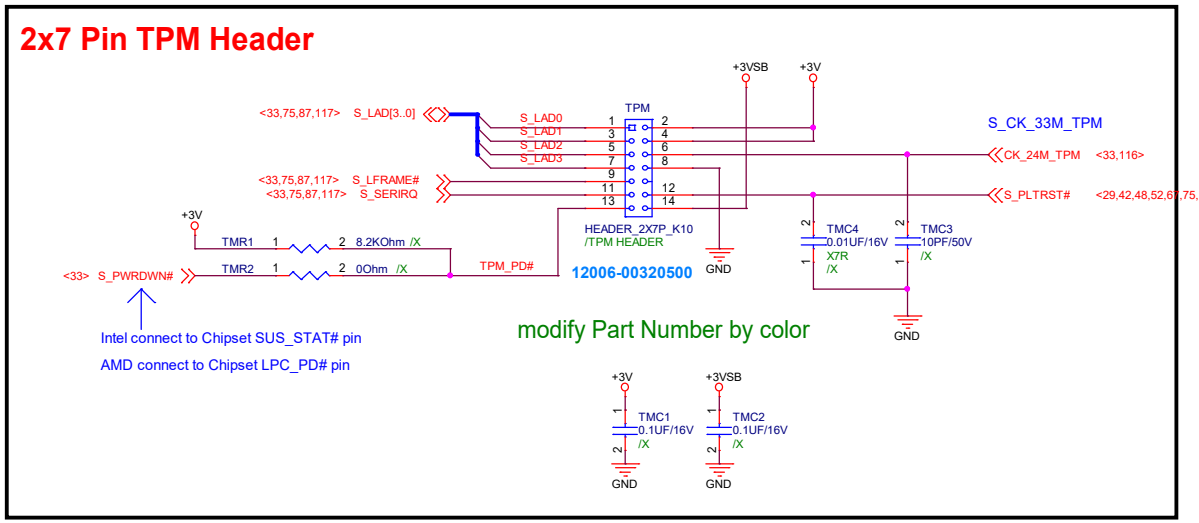
10/09 Add EPU Control Circuit

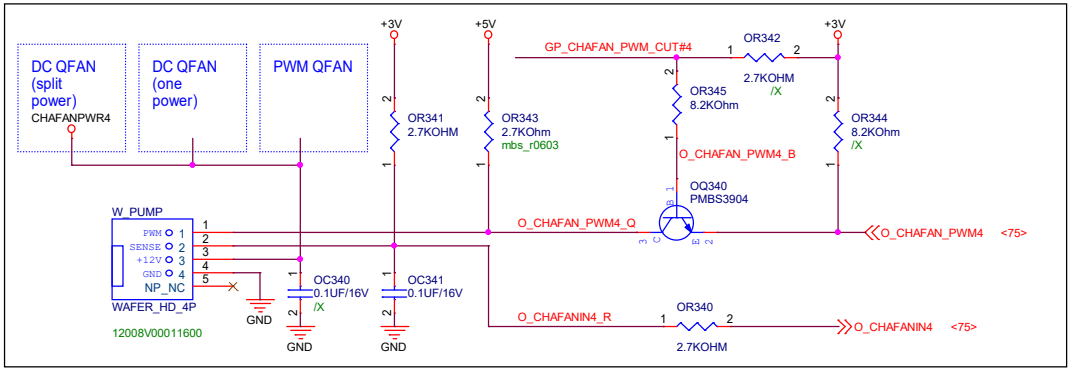
EUP control

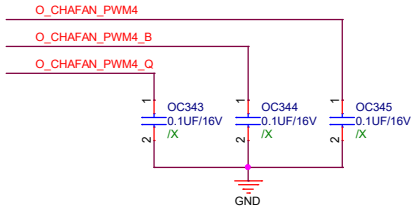

0.7B Beta
IR35201
P_VCORE_VCC5_20
P_VRMVCC_20
ASP1400
VRM
EC
SB
VRMPWRGD
O2_VRMPWRGD
O2U1
CIR_RLC_TX/GPIO4
GPIO0A/RLC_RX2
GPIO0B/ESB_CLK
GPIO0C/ESB_DAT
GPIO14/FANFB0
GPIO15/FANFB1
GPIO16/E51_TXD
GPIO19/PWM3
GPI38/AD0
GPI39/AD1
GPI3A/AD2
GPI3B/AD3
GPI42/AD4
GPI43/AD5
GPO3C/DA0
GPO3D/DA1
GPO3E/DA2
GPO3F/DA3
GPIO44/SCL0
GPIO45/SDA0
GPIO46/SCL1
GPIO47/SDA1
GND1
GND2
GND3
AGND
XCLKI
XCLKO
KB3720QF
02G890001410
GPXIOA00/SDICS#
GPXIOA01/SDICLK
GPXIOA02/SDIMOSI
GPXIOD0/SDIMISO
SERIRQ
LFRAME#
LAD3
LAD2
LAD1
LAD0
PCICLK
GPIO05/PCIRST#
GPIO0E/SCI#
GPIO1A/NUMLED#
GPIO1D/CLKRUN#
GPIO20/KSO0
GPIO24/KSO4
GPIO25/KSO5
GPIO26/KSO6
GPIO27/KSO7
GPIO2B/KSO11
GPIO2C/KSO12
GPIO40
GPXIOA08
GPIO59
MISO
MOSI
SPICLK
SPICS#
ECRST#
V18R
VCC1
VCC2
VCC3
VCC4
AVCC
S_SYSPWROK
P_VR_READY_10
O2_CLK_PWREN
O2_PLTRST#
O2_VRMEN_OUT
O2_Vboot_TEST
S_RTCRST#_R
O_RSMRST#
P_VCORE_EN_10
O2_PSON#
O_PSON#_O1
PCH
Logic
Device
S_PLTRST#
PCH_PLTRST#
SIO
EATXPWR
O2_TP_TEST
0 test clock mode enable
1 normal mode using 32KHz OSC
O2X1 32.768Khz
O2C19 27PF/50V
O2C20 27PF/50V
XCLKI and XCLKO
width=4,Length=<1
+3VSB
GND

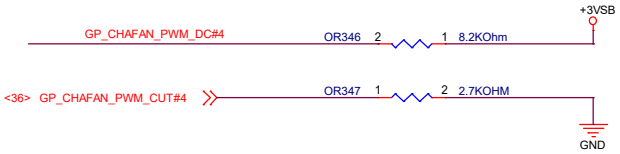
BOM	mount TPM	unmount TPM
/TPM	mount	unmount
/X	unmount	unmount

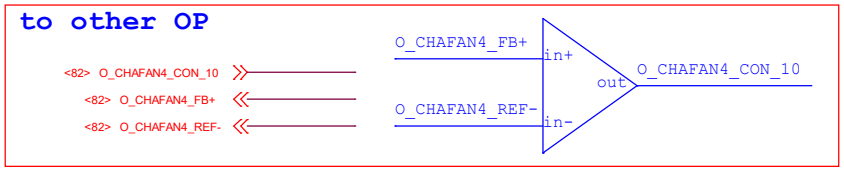
Delete it for EMS

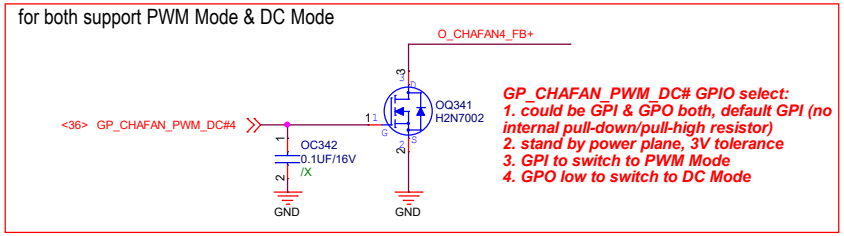


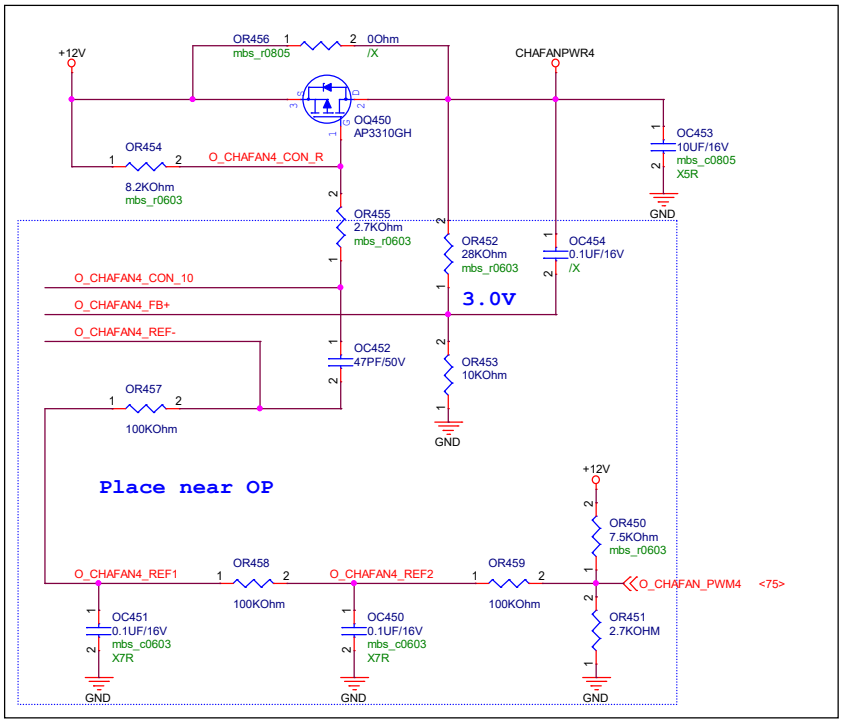

DC QFAN (split power)
CHAFANPWR4
DC QFAN (one power)
PWM QFAN
+3V
+5V
+3V
GP_CHAFAN_PWM_CUT#4
OR342
2.7KOHM
/X
OR341
2.7KOHM
OR343
2.7KOhm
mbs_r0603
OR345
8.2KOhm
OR344
8.2KOhm
/X
O_CHAFAN_PWM4_B
OQ340
PMBS3904
W_PUMP
PWM
SENSE
+12V
GND
NP_NC
WAFER_HD_4P
12008V00011600
O_CHAFAN_PWM4_Q
O_CHAFAN_PWM4
<75>
OC340
0.1UF/16V
/X
OC341
0.1UF/16V
O_CHAFANIN4_R
OR340
2.7KOHM
O_CHAFANIN4
<75>
GND


O_CHAFAN_PWM4
O_CHAFAN_PWM4_B
O_CHAFAN_PWM4_Q
OC343
0.1UF/16V
/X
OC344
0.1UF/16V
/X
OC345
0.1UF/16V
/X
GND

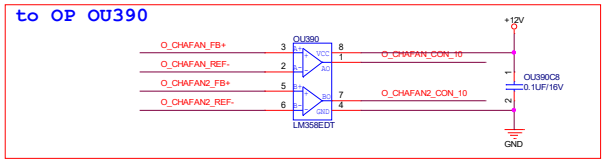

+3VSB
GP_CHAFAN_PWM_DC#4
OR346
8.2KOhm
<36> GP_CHAFAN_PWM_CUT#4
OR347
2.7KOHM
GND

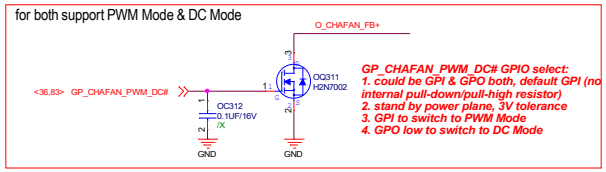

to other OP
<82> O_CHAFAN4_CON_10
<82> O_CHAFAN4_FB+
<82> O_CHAFAN4_REF-
O_CHAFAN4_FB+
O_CHAFAN4_REF-
in+
in-
out
O_CHAFAN4_CON_10

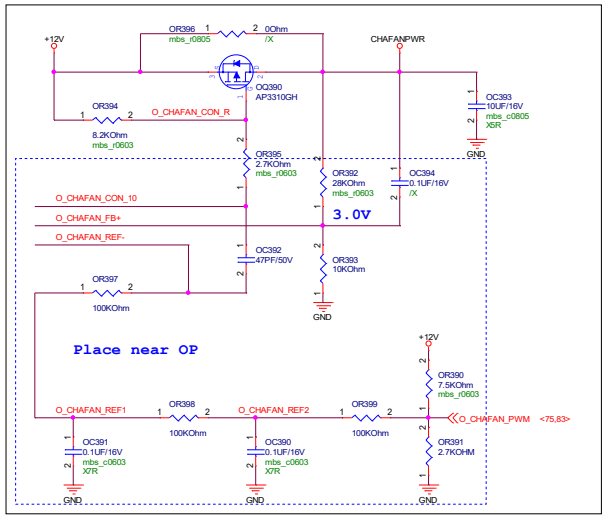

for both support PWM Mode & DC Mode
O_CHAFAN4_FB+
<36> GP_CHAFAN_PWM_DC#4
OQ341
H2N7002
OC342
0.1UF/16V
/X
GND
GP_CHAFAN_PWM_DC# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance
3. GPI to switch to PWM Mode
4. GPO low to switch to DC Mode

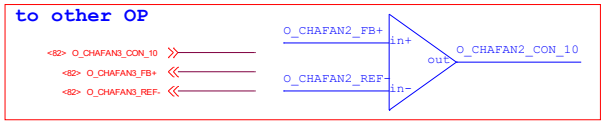

+12V
OR456
mbs_r0805
0Ohm
/X
CHAFANPWR4
OQ450
AP3310GH
OR454
8.2KOhm
mbs_r0603
O_CHAFAN4_CON_R
OC453
10UF/16V
mbs_c0805
X5R
GND
OR455
2.7KOhm
mbs_r0603
OR452
28KOhm
mbs_r0603
OC454
0.1UF/16V
/X
3.0V
O_CHAFAN4_CON_10
O_CHAFAN4_FB+
O_CHAFAN4_REF-
OC452
47PF/50V
OR453
10KOhm
OR457
100KOhm
Place near OP
+12V
OR450
7.5KOhm
mbs_r0603
O_CHAFAN4_REF1
OR458
100KOhm
O_CHAFAN4_REF2
OR459
100KOhm
O_CHAFAN_PWM4
<75>
OC451
0.1UF/16V
mbs_c0603
X7R
OC450
0.1UF/16V
mbs_c0603
X7R
OR451
2.7KOHM
GND

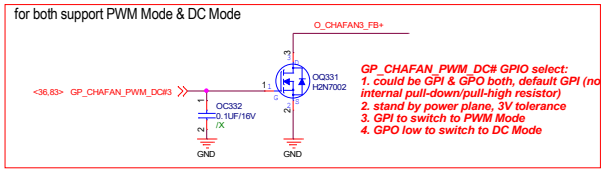
OP + MOS Power Solution

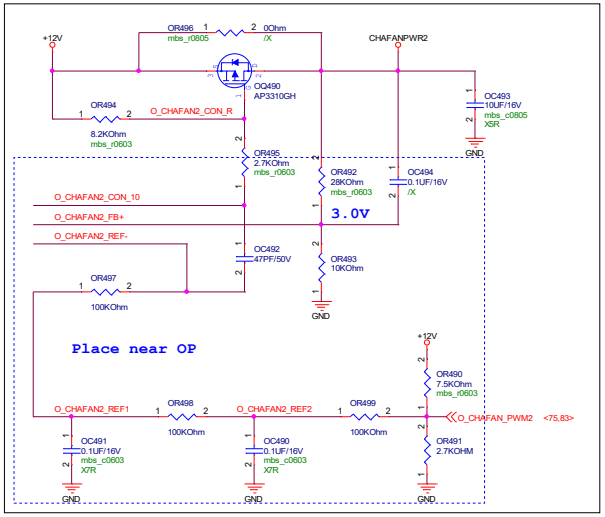


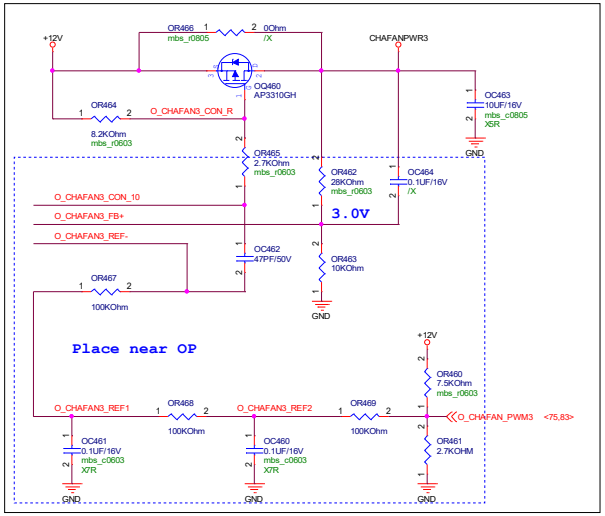


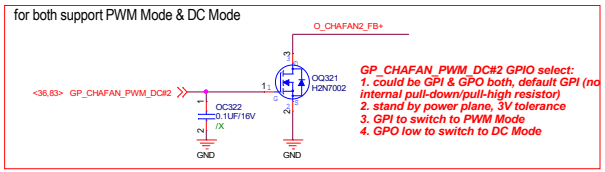




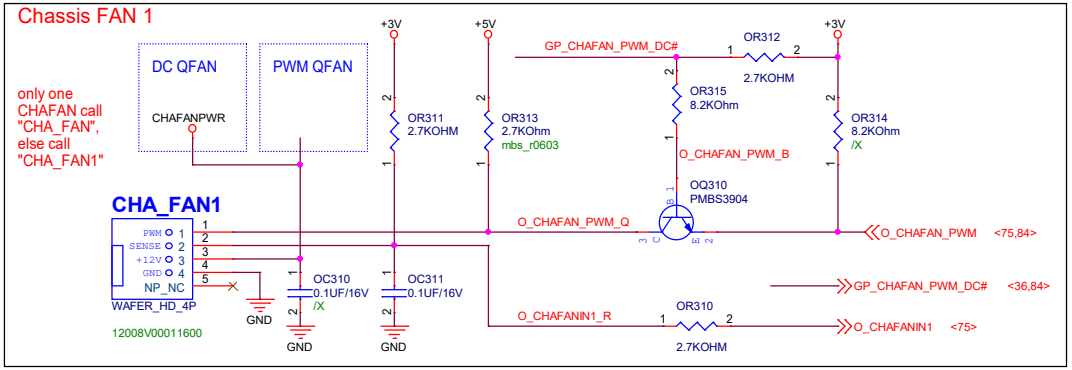


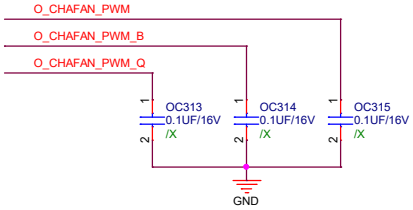


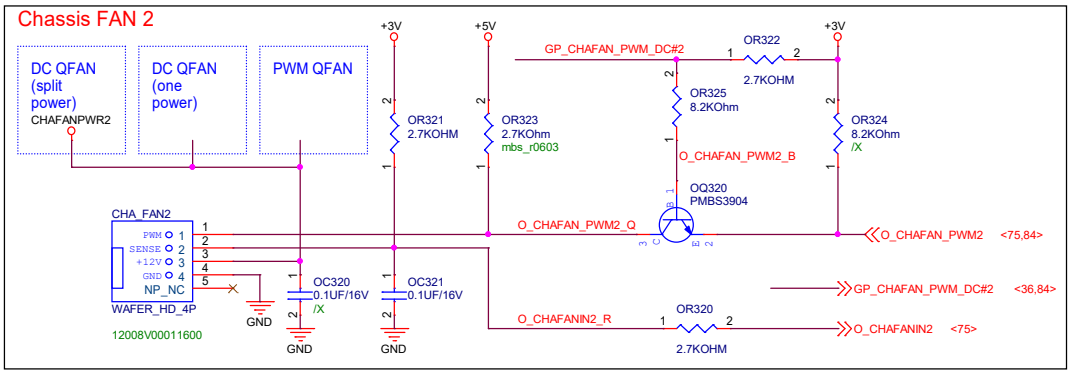


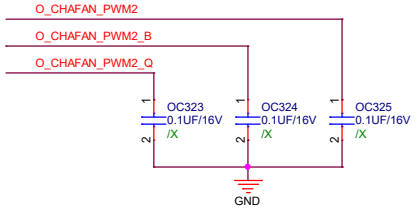


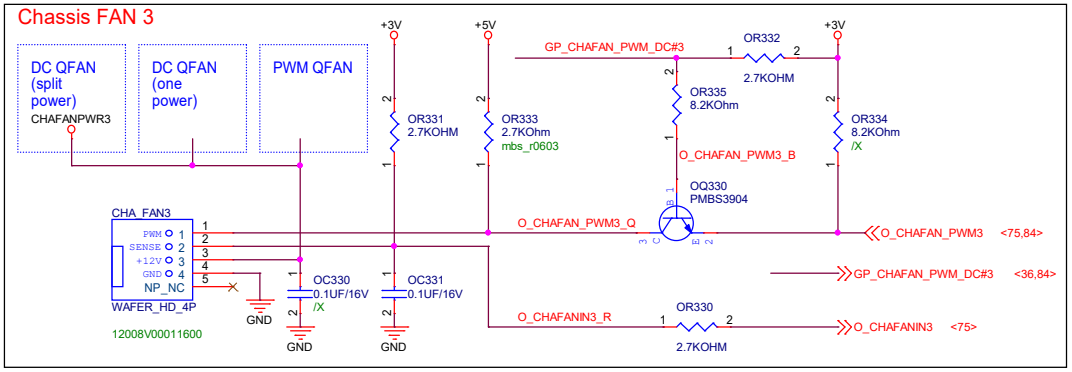
4 Pin PWM Mode & DC Mode

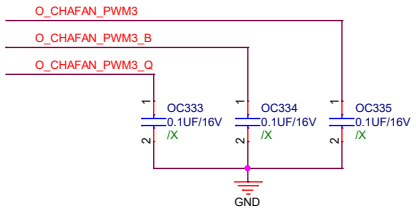


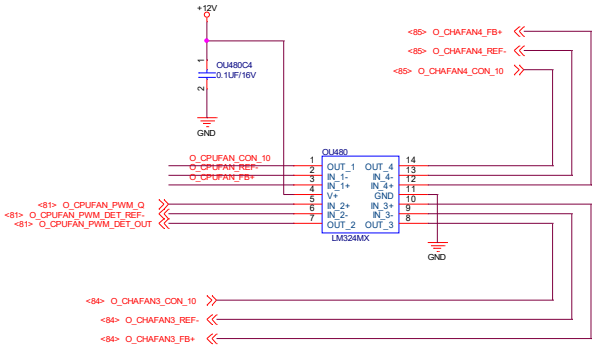


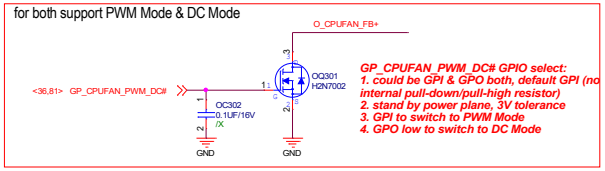


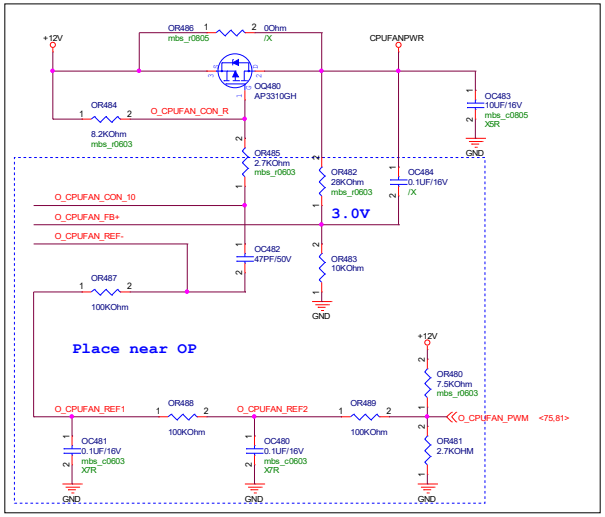


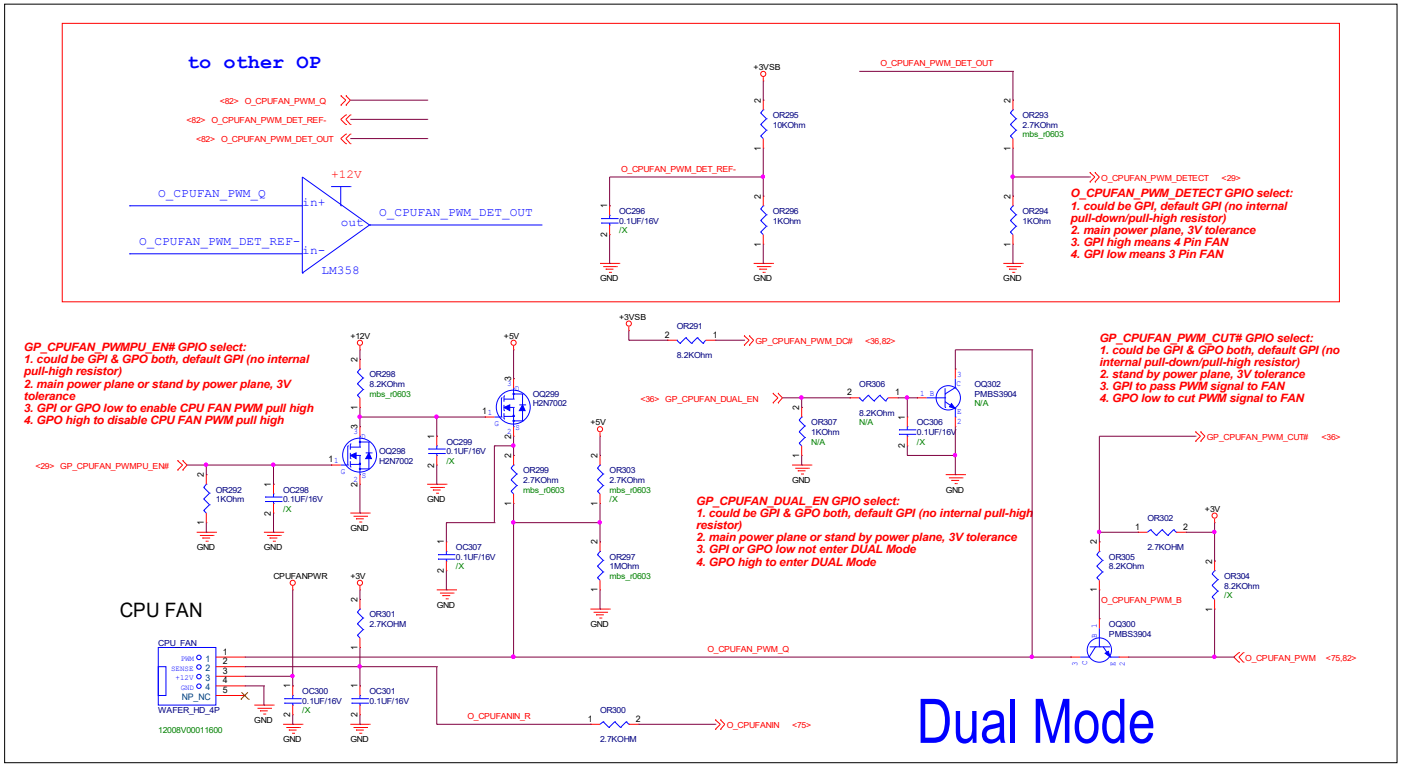


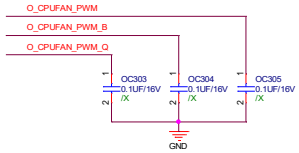



+12V
OU480C4
0.1UF/16V
GND
<85> O_CHAFAN4_FB+
<85> O_CHAFAN4_REF-
<85> O_CHAFAN4_CON_10
O_CPUFAN_CON_10
O_CPUFAN_REF-
O_CPUFAN_FB+
OU480
OUT_1
IN_1-
IN_1+
V+
IN_2+
IN_2-
OUT_2
OUT_4
IN_4-
IN_4+
GND
IN_3+
IN_3-
OUT_3
LM324MX
<81> O_CPUFAN_PWM_O
<81> O_CPUFAN_PWM_DET_REF-
<81> O_CPUFAN_PWM_DET_OUT
<84> O_CHAFAN3_CON_10
<84> O_CHAFAN3_REF-
<84> O_CHAFAN3_FB+


for both support PWM Mode & DC Mode
O_CPUFAN_FB+
<36,81> GP_CPUFAN_PWM_DC#
OQ301
H2N7002
OC302
0.1UF/16V
/X
GND
GND
GP_CPUFAN_PWM_DC# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance
3. GPI to switch to PWM Mode
4. GPO low to switch to DC Mode

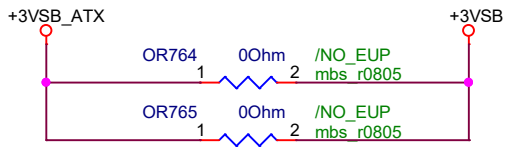

+12V
OR486
mbs_r0805
0Ohm
/X
CPUFANPWR
OQ480
AP3310GH
OR484
8.2KOhm
mbs_r0603
O_CPUFAN_CON_R
OC483
10UF/16V
mbs_c0805
X5R
GND
OR485
2.7KOhm
mbs_r0603
OR482
28KOhm
mbs_r0603
OC484
0.1UF/16V
/X
3.0V
O_CPUFAN_CON_10
O_CPUFAN_FB+
O_CPUFAN_REF-
OC482
47PF/50V
OR483
10KOhm
OR487
100KOhm
Place near OP
+12V
OR480
7.5KOhm
mbs_r0603
O_CPUFAN_REF1
OR488
100KOhm
O_CPUFAN_REF2
OR489
100KOhm
O_CPUFAN_PWM <75,81>
OC481
0.1UF/16V
mbs_c0603
X7R
OC480
0.1UF/16V
mbs_c0603
X7R
OR481
2.7KOHM
GND
GND
GND

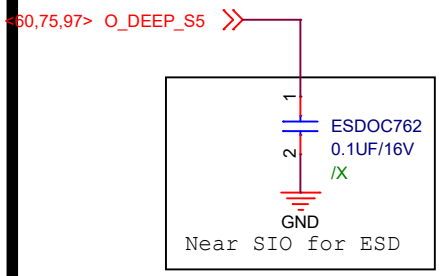

to other OP
<82> O_CPUFAN_PWM_Q
<82> O_CPUFAN_PWM_DET_REF-
<82> O_CPUFAN_PWM_DET_OUT
+12V
O_CPUFAN_PWM_Q
O_CPUFAN_PWM_DET_REF-
in+
in-
out
O_CPUFAN_PWM_DET_OUT
LM358
+3VSB
OR295
10KOhm
O_CPUFAN_PWM_DET_REF-
OC296
0.1UF/16V
/X
OR296
1KOhm
GND
O_CPUFAN_PWM_DET_OUT
OR293
2.7KOhm
mbs_r0603
O_CPUFAN_PWM_DETECT <29>
OR294
1KOhm
O_CPUFAN_PWM_DETECT GPIO select:
1. could be GPI, default GPI (no internal pull-down/pull-high resistor)
2. main power plane, 3V tolerance
3. GPI high means 4 Pin FAN
4. GPI low means 3 Pin FAN
GP_CPUFAN_PWMPU_EN# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-high resistor)
2. main power plane or stand by power plane, 3V tolerance
3. GPI or GPO low to enable CPU FAN PWM pull high
4. GPO high to disable CPU FAN PWM pull high
+12V
+5V
OR298
8.2KOhm
mbs_r0603
OQ299
H2N7002
OQ298
H2N7002
<29> GP_CPUFAN_PWMPU_EN#
OR292
1KOhm
OC298
0.1UF/16V
/X
OC299
0.1UF/16V
/X
OR299
2.7KOhm
mbs_r0603
OR303
2.7KOhm
mbs_r0603
/X
OC307
0.1UF/16V
/X
OR297
1MOhm
mbs_r0603
+3VSB
OR291
8.2KOhm
GP_CPUFAN_PWM_DC# <36,82>
<36> GP_CPUFAN_DUAL_EN
OR306
8.2KOhm
N/A
OQ302
PMBS3904
N/A
OR307
1KOhm
N/A
OC306
0.1UF/16V
/X
GP_CPUFAN_DUAL_EN GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-high resistor)
2. main power plane or stand by power plane, 3V tolerance
3. GPI or GPO low not enter DUAL Mode
4. GPO high to enter DUAL Mode
GP_CPUFAN_PWM_CUT# GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down/pull-high resistor)
2. stand by power plane, 3V tolerance
3. GPI to pass PWM signal to FAN
4. GPO low to cut PWM signal to FAN
GP_CPUFAN_PWM_CUT# <36>
+3V
OR302
2.7KOHM
OR305
8.2KOhm
OR304
8.2KOhm
/X
O_CPUFAN_PWM_B
OQ300
PMBS3904
O_CPUFAN_PWM <75,82>
CPUFANPWR
+3V
OR301
2.7KOHM
CPU FAN
CPU_FAN
PWM
SENSE
+12V
GND
NP_NC
WAFER_HD_4P
12008V00011600
OC300
0.1UF/16V
/X
OC301
0.1UF/16V
/X
O_CPUFAN_PWM_Q
O_CPUFANIN_R
OR300
2.7KOHM
O_CPUFANIN <75>
Dual Mode

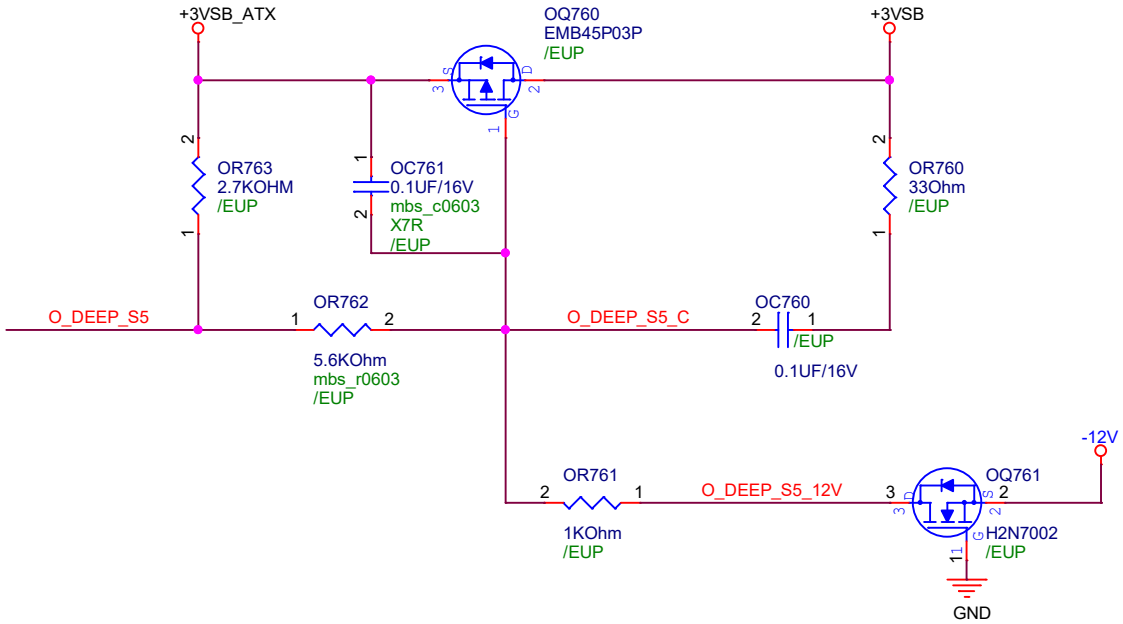

O_CPUFAN_PWM
O_CPUFAN_PWM_B
O_CPUFAN_PWM_Q
OC303
0.1UF/16V
/X
OC304
0.1UF/16V
/X
OC305
0.1UF/16V
/X
GND

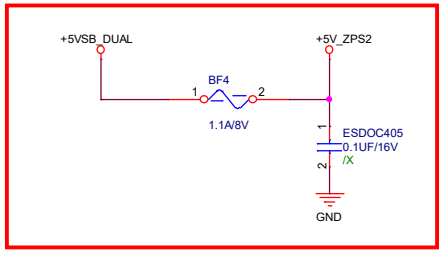
ERP Circuit

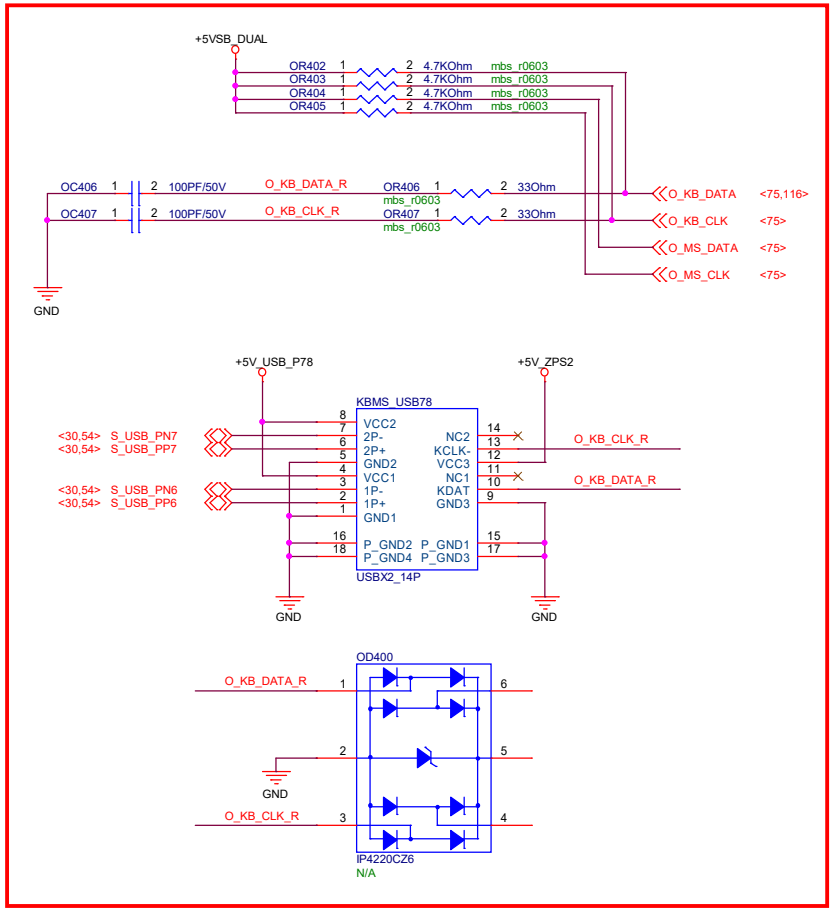
Resistor



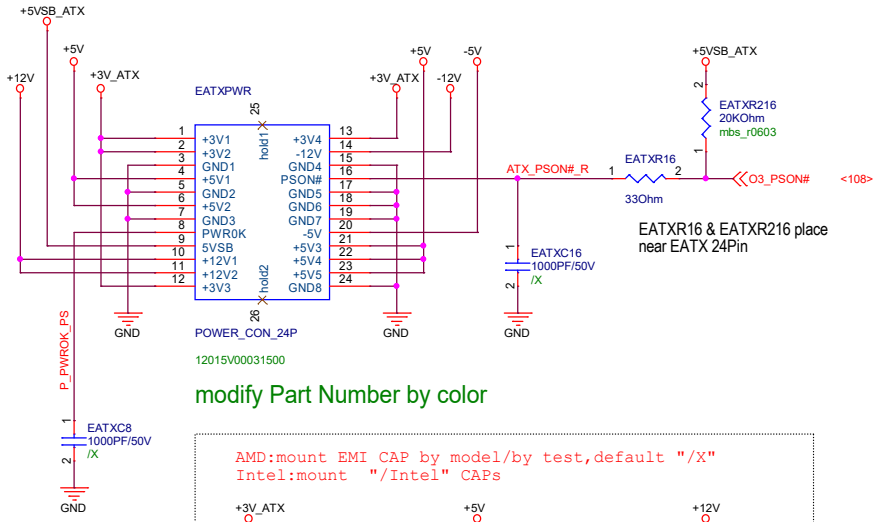





+5VSB_DUAL
+5V_ZPS2
BF4
1
2
1.1A/8V
ESDOC405
0.1UF/16V
/X
GND


+5VSB_DUAL
OR402 1 2 4.7KOhm mbs_r0603
OR403 1 2 4.7KOhm mbs_r0603
OR404 1 2 4.7KOhm mbs_r0603
OR405 1 2 4.7KOhm mbs_r0603
OC406 1 2 100PF/50V
O_KB_DATA_R
OR406 1 2 33Ohm mbs_r0603
OC407 1 2 100PF/50V
O_KB_CLK_R
OR407 1 2 33Ohm mbs_r0603
O_KB_DATA <75,116>
O_KB_CLK <75>
O_MS_DATA <75>
O_MS_CLK <75>
GND
+5V_USB_P78
+5V_ZPS2
KBMS_USB78
<30,54> S_USB_PN7
<30,54> S_USB_PP7
<30,54> S_USB_PN6
<30,54> S_USB_PP6
VCC2
2P-
2P+
GND2
VCC1
1P-
1P+
GND1
NC2
KCLK-
VCC3
NC1
KDAT
GND3
P_GND2 P_GND1
P_GND4 P_GND3
O_KB_CLK_R
O_KB_DATA_R
USBX2_14P
GND
GND
OD400
O_KB_DATA_R
O_KB_CLK_R
GND
IP4220CZ6
N/A

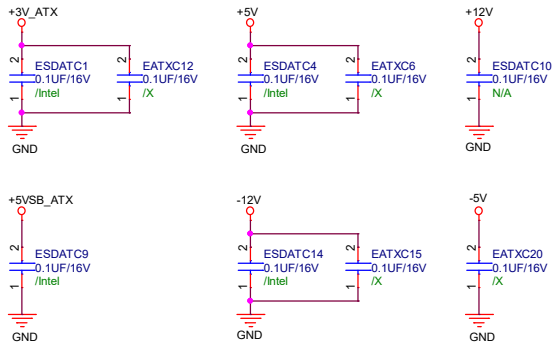
EATX POWER



12015V00031500

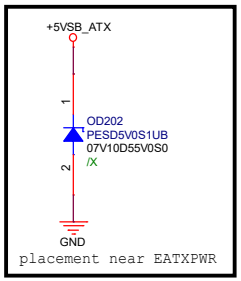
modify Part Number by color

AMD:mount EMI CAP by model/by test,default "/X"
Intel:mount "/Intel" CAPs



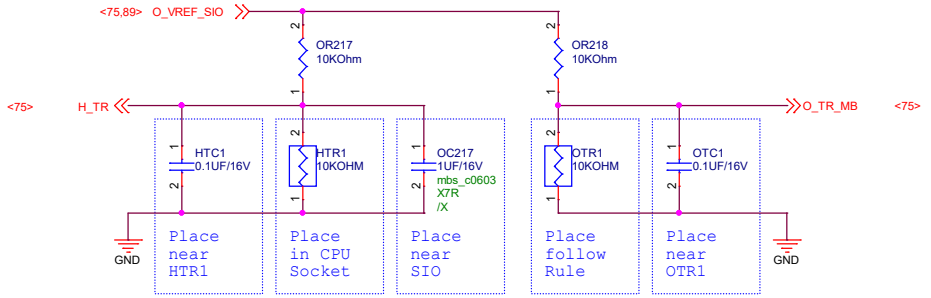
place near EATXPWR

Delete it for EMS

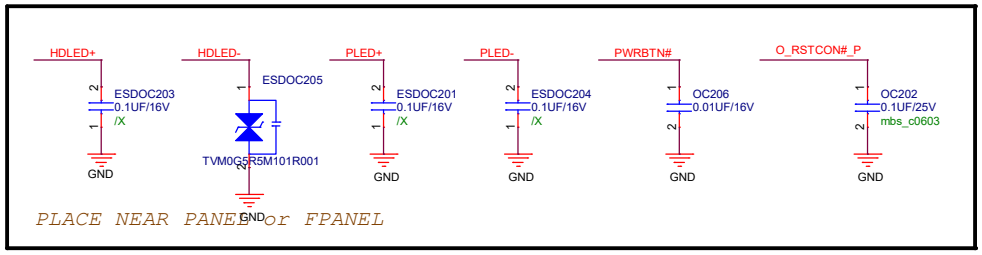


placement near EATXPWR

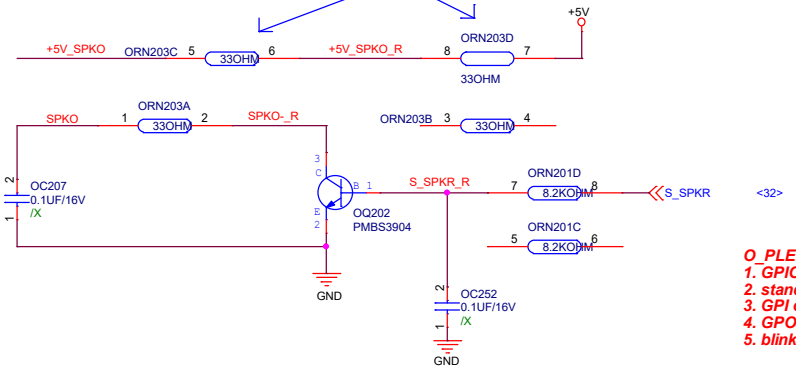
HW Monitor

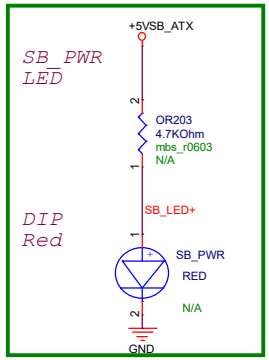


If no CPU thermistor, unmount components HTR1, OC430, OR431
If no MB thermistor, unmount components OTR1, OC432, OR433

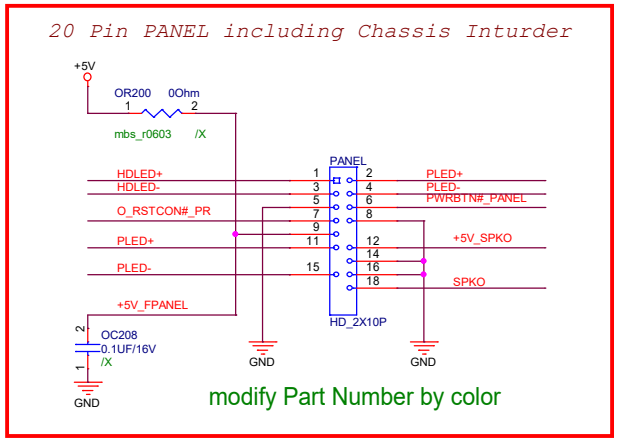


If change to single resistor, use
75 Ohm(10V213750010)

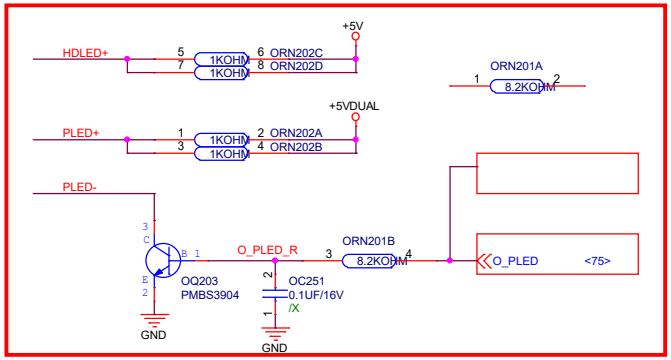




O_PLED/S_PLED GPIO select:
1. GPIO with blink function, default GPI (no internal pull-down resistor)
2. stand by power plane, 3V tolerance
3. GPI or GPO high to turn on Power LED
4. GPO low to turn off Power LED
5. blink under S3

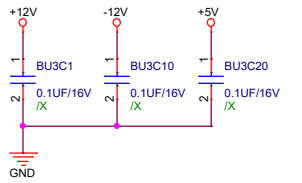


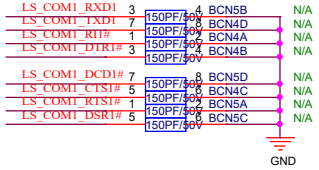
Power LED power source use +5VDUAL

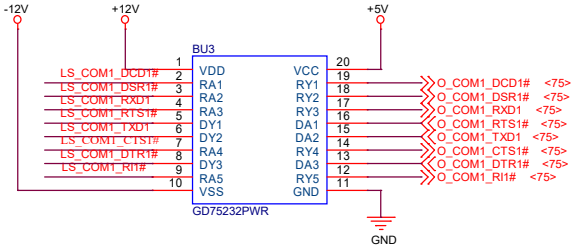


LPT PORT

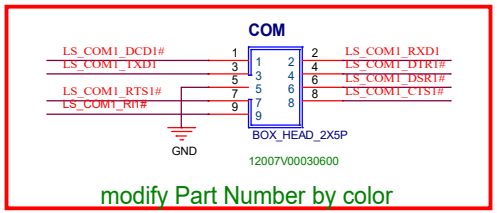
COM PORT

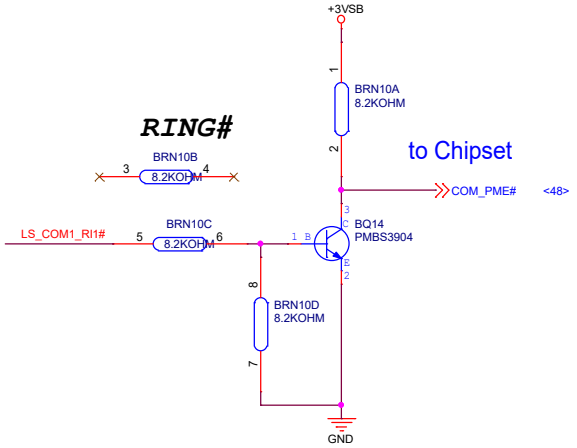


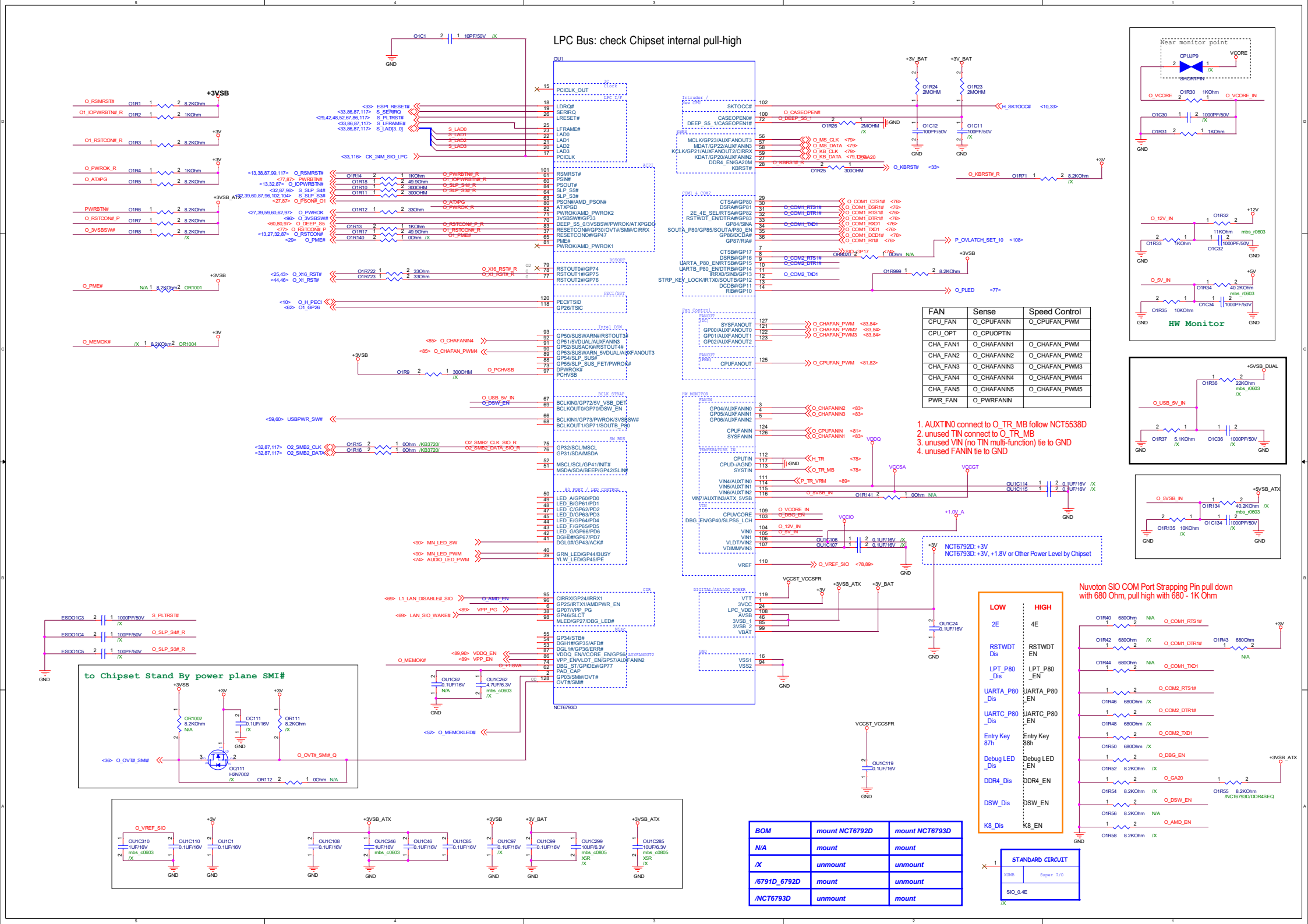




COM Box Header





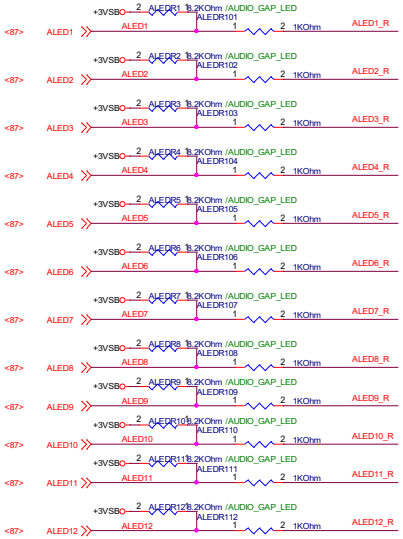


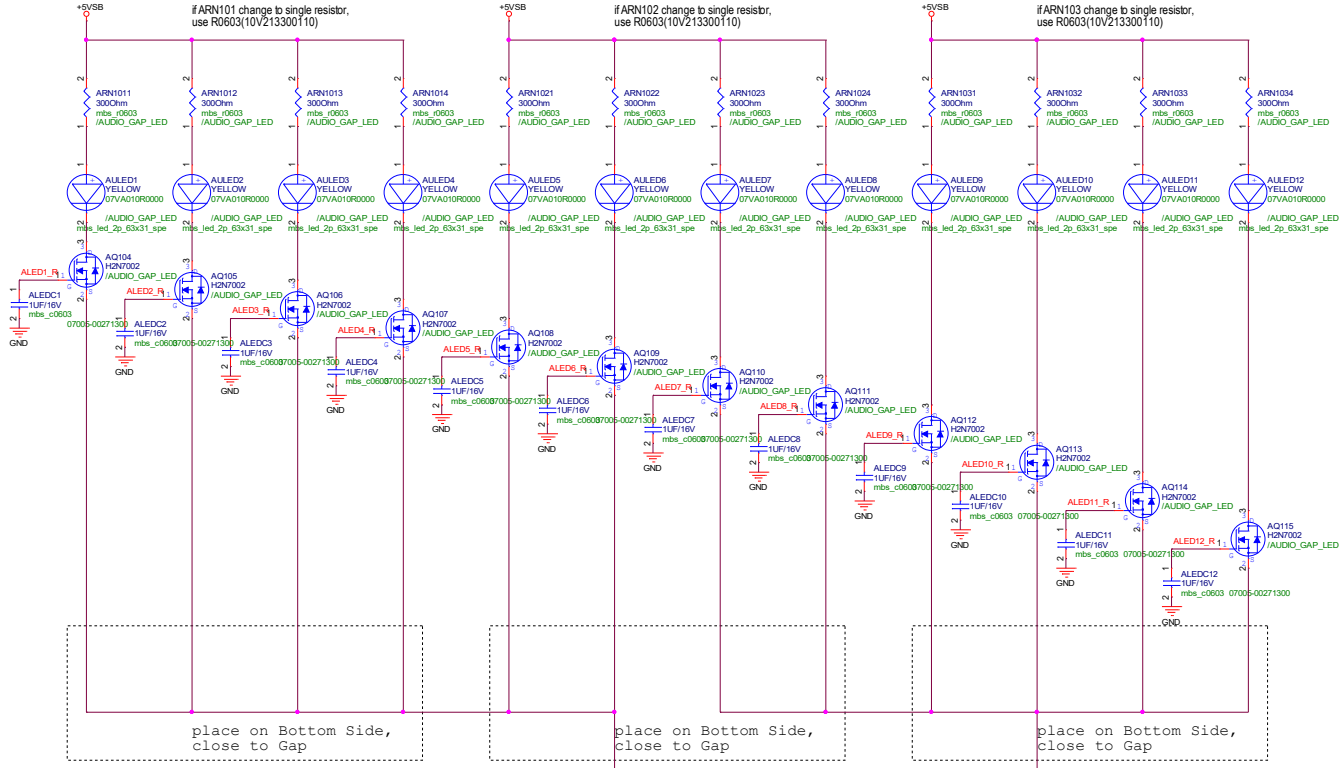
FAN	Sense	Speed Control
CPU_FAN	O_CPUFANIN	O_CPUFAN_PWM
CPU_OPT	O_CPUOPTIN	
CHA_FAN1	O_CHAFANIN1	O_CHAFAN_PWM
CHA_FAN2	O_CHAFANIN2	O_CHAFAN_PWM2
CHA_FAN3	O_CHAFANIN3	O_CHAFAN_PWM3
CHA_FAN4	O_CHAFANIN4	O_CHAFAN_PWM4
CHA_FAN5	O_CHAFANIN5	O_CHAFAN_PWM5
PWR_FAN	O_PWRFANIN	

LOW	HIGH
2E	4E
RSTWDT Dis	RSTWDT EN
LPT_P80 _Dis	LPT_P80 _EN
UARTA_P80 _Dis	UARTA_P80 EN
UARTC_P80 _Dis	UARTC_P80 EN
Entry Key 87h	Entry Key 88h
Debug LED _Dis	Debug LED _EN
DDR4_Dis	DDR4_EN
DSW_Dis	DSW_EN
K8_Dis	K8_EN

BOM	mount NCT6792D	mount NCT6793D
N/A	mount	mount
/X	unmount	unmount
/6791D_6792D	mount	unmount
/NCT6793D	unmount	mount

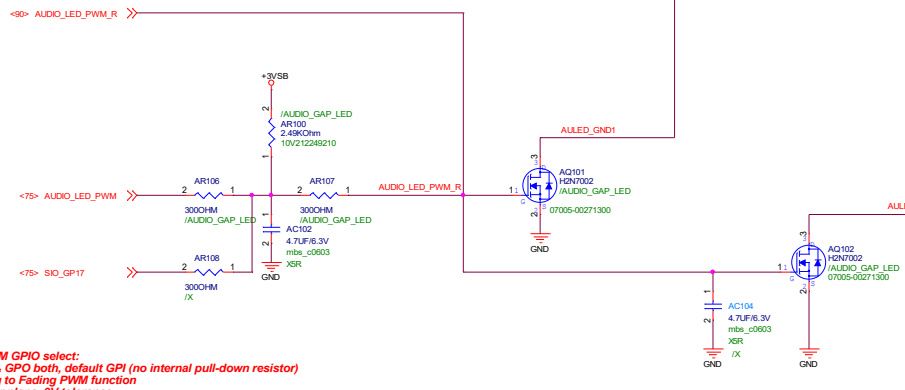
AUDIO LED





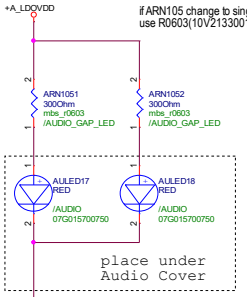
ATX normal 12 pcs LED, m-ATX normal 6 pcs LED

Audio LED
Yellow: 07014-00091400
Red : 07VA010R0000

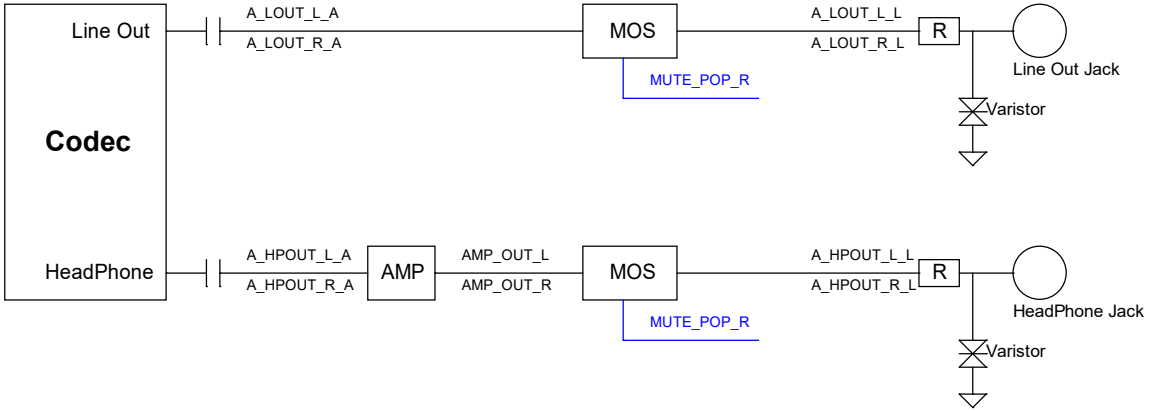


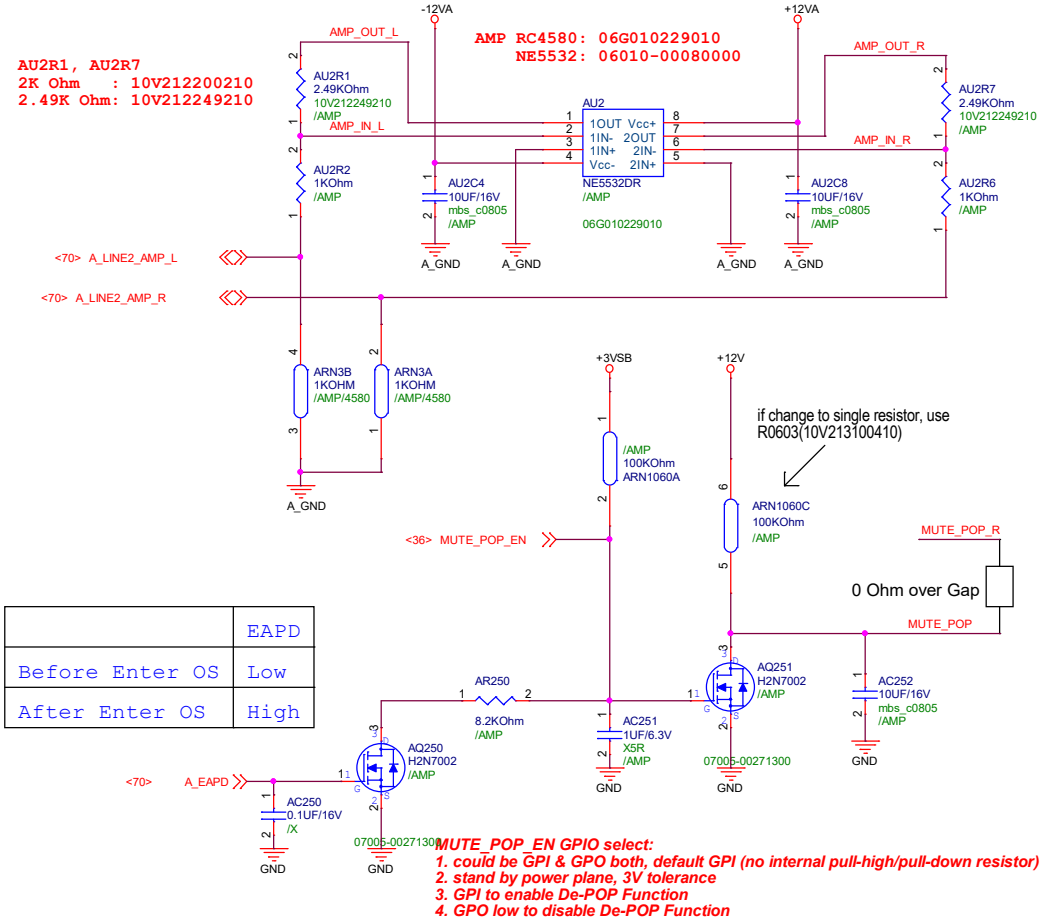
AUDIO_LED_PWM GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down resistor)
2. could mapping to Fading PWM function
3. stand by power plane, 3V tolerance
4. GPI or GPO high to turn on Audio LED
5. GPO low to turn off Audio LED
6. Fading PWM to be Respiration Lamp

AUDIO COVER

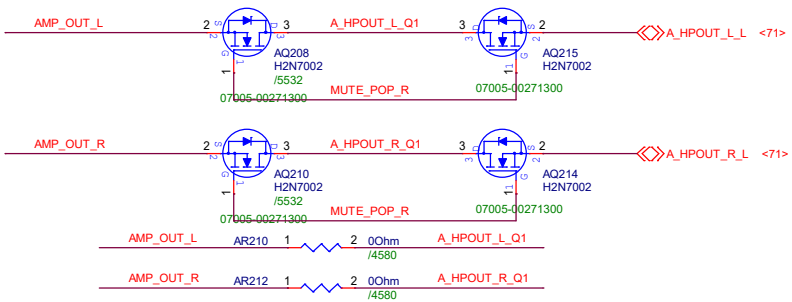


for ALC887-VD2/ALC892/ALC1150



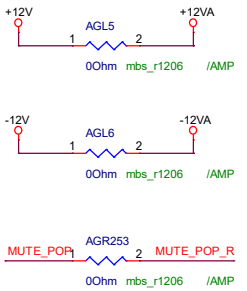


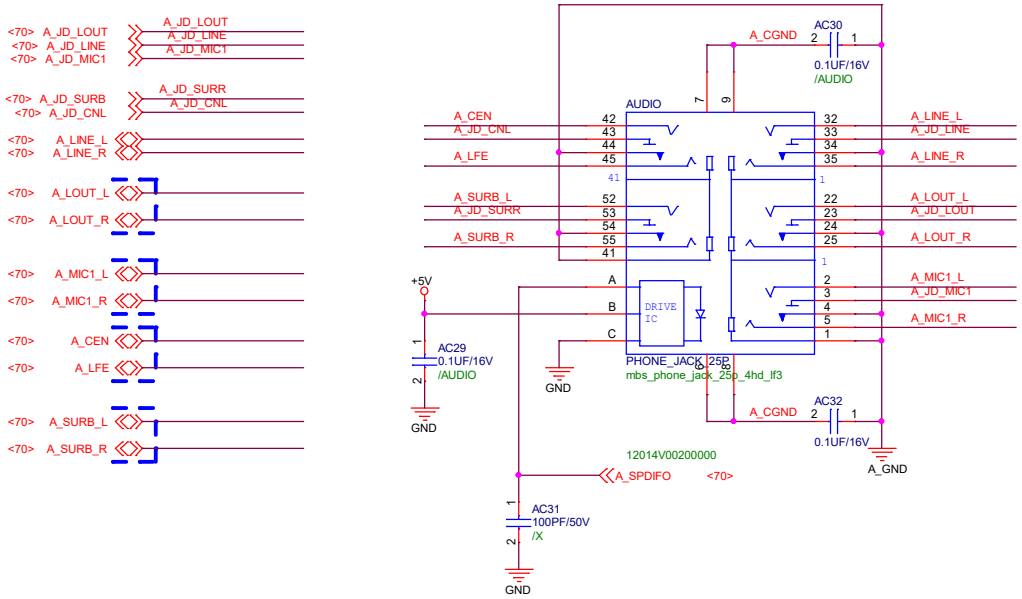
	EAPD
Before Enter OS	Low
After Enter OS	High



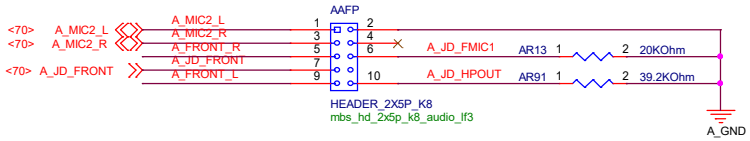
also for XU reserve AMP

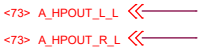
for AMP with De-POP

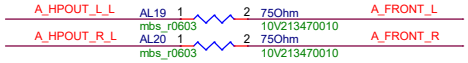


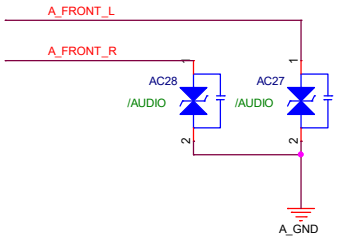

<70> A_JD_LOUT
<70> A_JD_LINE
<70> A_JD_MIC1
A_JD_LOUT
A_JD_LINE
A_JD_MIC1
<70> A_JD_SURB
<70> A_JD_CNL
A_JD_SURR
A_JD_CNL
<70> A_LINE_L
<70> A_LINE_R
<70> A_LOUT_L
<70> A_LOUT_R
<70> A_MIC1_L
<70> A_MIC1_R
<70> A_CEN
<70> A_LFE
<70> A_SURB_L
<70> A_SURB_R
A_CGND
AC30
0.1UF/16V
/AUDIO
AUDIO
A_CEN
A_JD_CNL
A_LFE
A_SURB_L
A_JD_SURR
A_SURB_R
A_LINE_L
A_JD_LINE
A_LINE_R
A_LOUT_L
A_JD_LOUT
A_LOUT_R
A_MIC1_L
A_JD_MIC1
A_MIC1_R
+5V
DRIVE IC
AC29
0.1UF/16V
/AUDIO
GND
PHONE_JACK_25P
mbs_phone_jack_25p_4hd_lf3
AC32
0.1UF/16V
A_GND
12014V00200000
A_SPDIFO
<70>
AC31
100PF/50V
/X

for ALC1150





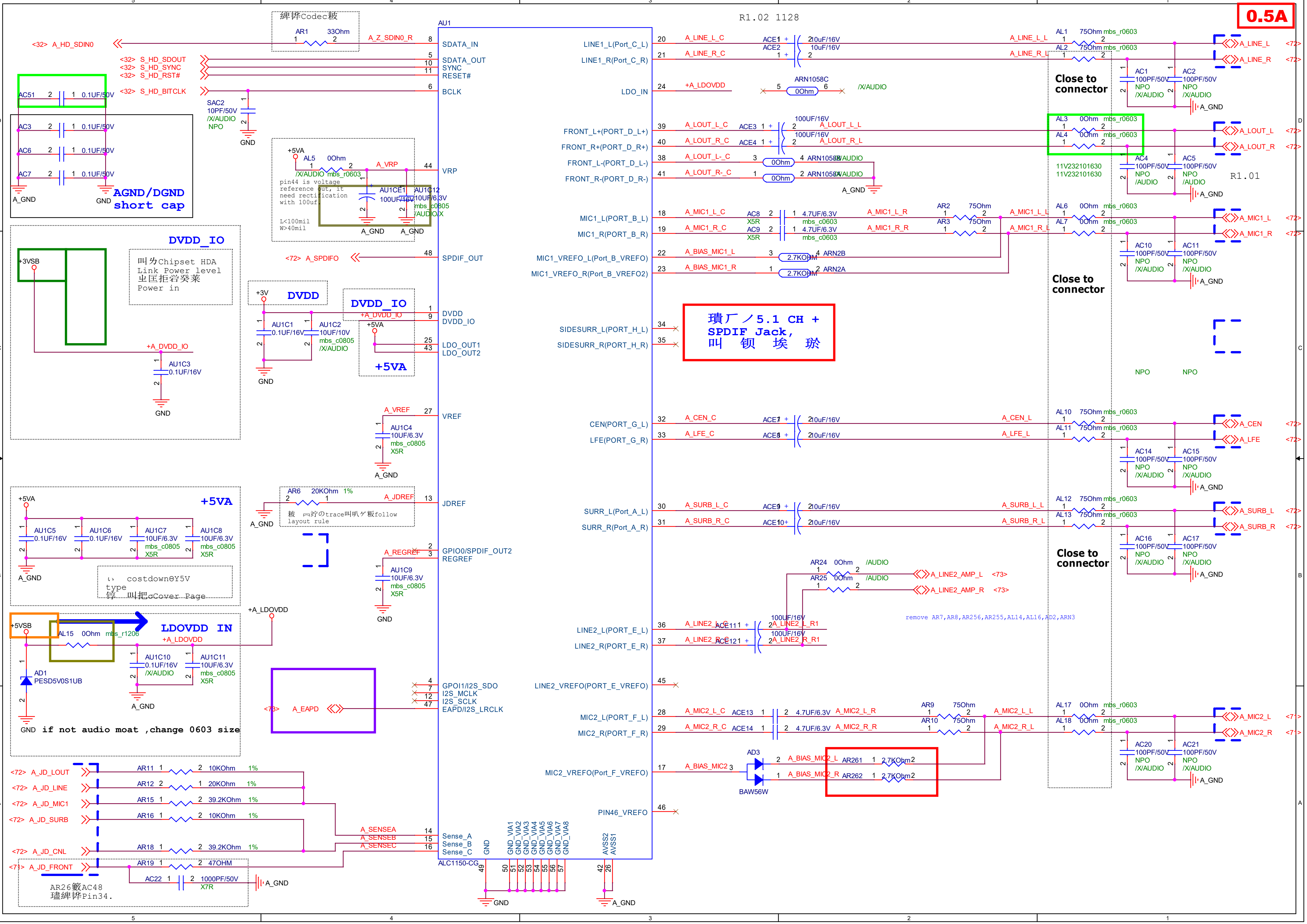




DIP CAP
EL 100U : 11G040810743
PL 100U : 11031V0001F000
Audio 100U: 11011-00026000
Gamer 100U: 11011-0002Z000

AL13, AL14
75 Ohm: 10V213750010
47 Ohm: 10V213470010

Delete it for EMS

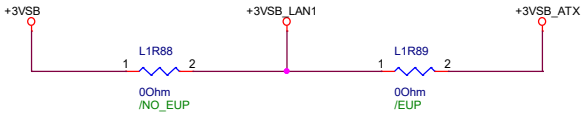


0.5A
R1.02 1128
R1.01
AU1
ALC1150-CG
SDATA_IN
SDATA_OUT
SYNC
RESET#
BCLK
VRP
SPDIF_OUT
DVDD
DVDD_IO
LDO_OUT1
LDO_OUT2
VREF
JDREF
GPIO0/SPDIF_OUT2
REGREF
GPIO1/I2S_SDO
I2S_MCLK
I2S_SCLK
EAPD/I2S_LRCLK
Sense_A
Sense_B
Sense_C
LINE1_L(Port_C_L)
LINE1_R(Port_C_R)
LDO_IN
FRONT_L+(PORT_D_L+)
FRONT_R+(PORT_D_R+)
FRONT_L-(PORT_D_L-)
FRONT_R-(PORT_D_R-)
MIC1_L(PORT_B_L)
MIC1_R(PORT_B_R)
MIC1_VREFO_L(Port_B_VREFO)
MIC1_VREFO_R(Port_B_VREFO2)
SIDESURR_L(PORT_H_L)
SIDESURR_R(PORT_H_R)
CEN(PORT_G_L)
LFE(PORT_G_R)
SURR_L(Port_A_L)
SURR_R(Port_A_R)
LINE2_L(PORT_E_L)
LINE2_R(PORT_E_R)
LINE2_VREFO(PORT_E_VREFO)
MIC2_L(PORT_F_L)
MIC2_R(PORT_F_R)
MIC2_VREFO(Port_F_VREFO)
PIN46_VREFO
<32> A_HD_SDIN0
<32> S_HD_SDOUT
<32> S_HD_SYNC
<32> S_HD_RST#
<32> S_HD_BITCLK
<72> A_SPDIFO
<72> A_EAPD
AGND/DGND short cap
DVDD_IO
DVDD
+5VA
LDOVDD IN
Close to connector
SPDIF Jack,
pin44 is voltage reference out, it need rectification with 100uf.
L<100mil
W>40mil
if not audio moat ,change 0603 size
remove AR7,AR8,AR256,AR255,AL14,AL16,AD2,ARN3
AD1 PESD5V0S1UB
AD3 BAW56W
A_LINE_L
A_LINE_R
A_LOUT_L
A_LOUT_R
A_MIC1_L
A_MIC1_R
A_CEN
A_LFE
A_SURB_L
A_SURB_R
A_LINE2_AMP_L <73>
A_LINE2_AMP_R <73>
A_MIC2_L
A_MIC2_R
<72> A_JD_LOUT
<72> A_JD_LINE
<72> A_JD_MIC1
<72> A_JD_SURB
<72> A_JD_CNL
<73> A_JD_FRONT
A_SENSEA
A_SENSEB
A_SENSEC
GND
A_GND

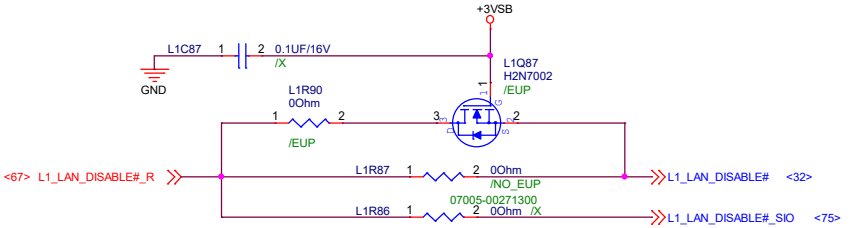
Note:

1. LAN IC power change to +3VSB_ATX (remove short-pin L1R88, add resistor L1R88 & L1R89)
2. for Intel PHY LAN, L1_LAN_DISABLE# renamed L1_LAN_DISABLE#_R in LAN IC Page, and change BOM to use +3VSB_ATX power plane GPIO
3. for Intel PHY LAN, L1_LAN_DISABLE# pull high resistor L1R7 Optional change to /EUP
4. for Intel PHY LAN, L1_LAN_WAKE# renamed L1_LAN_WAKE#_R in LAN IC Page
5. for Intel PCIE LAN, L1_DEV_OFF# choose +3VSB_ATX power plane GPIO
6. for PCIE LAN, S_WAKE# renamed S_WAKE#_LAN1 in LAN IC Page

POWER

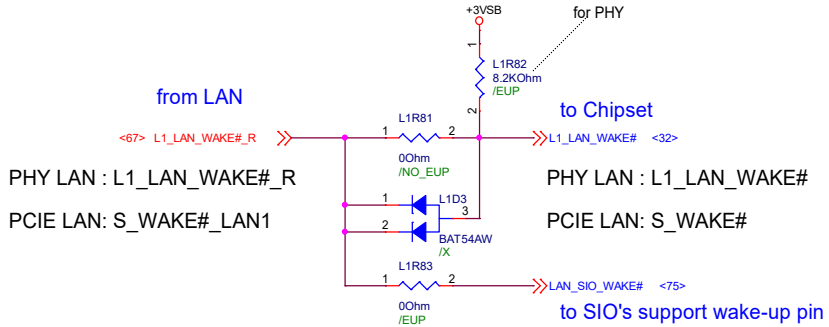


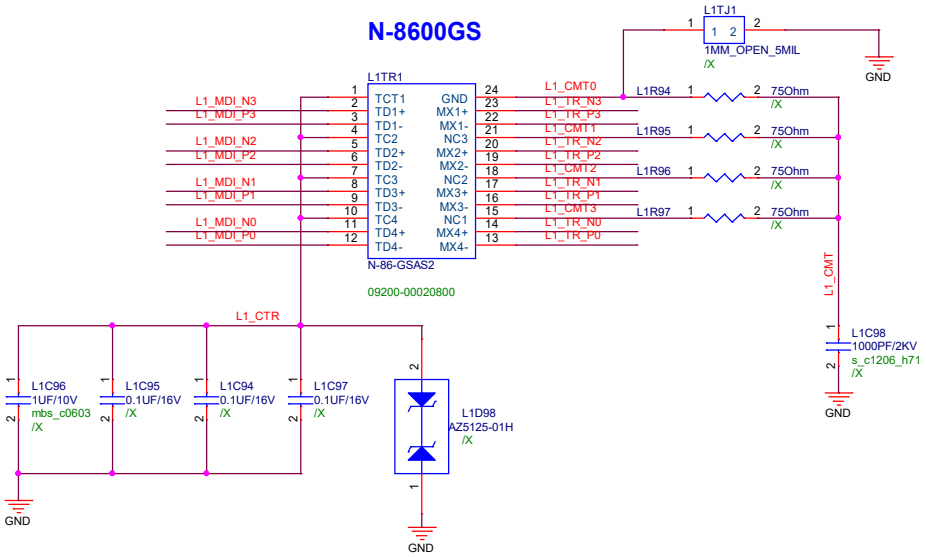
Hardware Solution

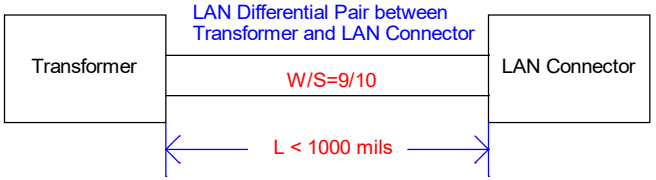


L1_LAN_DISABLE#_SIO GPIO select:
1. could be GPI & GPO both, default GPI (no internal pull-down resistor)
2. +3VSB_ATX power plane, 3V tolerance
3. GPI or GPO high to enable Intel PHY
4. GPO low to disable Intel PHY

SIO Solution

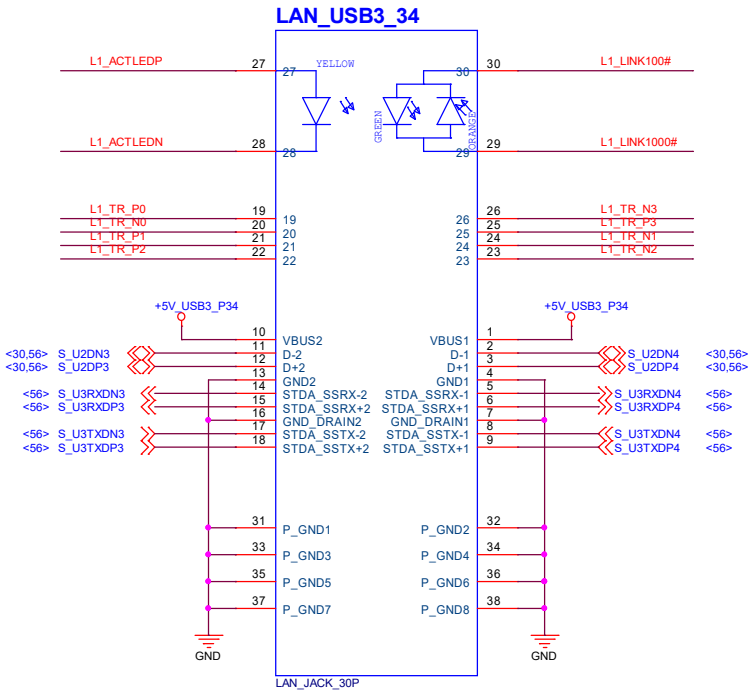




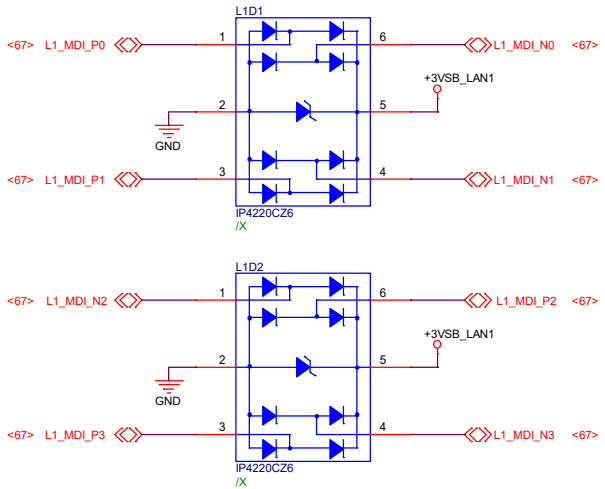


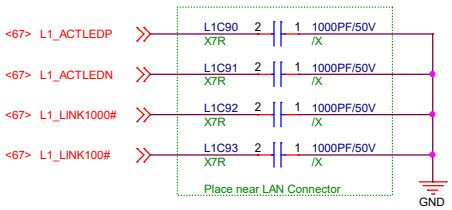
OP1 - Connector

GLAN + USB3 *2 Connector without Transformer



Delete it for EMS





瑣platform T 溦LAN controller,
钡厂ノ+3VSB power;
瑣platform 蝻T马溦LAN controller,
叫ゅノ+3V_DUAL power.

+3VSB_LAN1

1. Peak to peak = 70mV
2. Rise time = 0.1~100ms
3. 132mA @ S0
4. Use SLP_LAN# to gate PHY power and the ME must be off in Sx state.

PCIE IF
づ钡 chipset
PCIE port0

<28> CK_100M_LAN1P
<28> CK_100M_LAN1N
<30> S_X1_LAN1_RXP
<30> S_X1_LAN1_RXN
<30> S_X1_LAN1_TXP
<30> S_X1_LAN1_TXN

L1C13 10PF/50V NPO /X
L1C12 10PF/50V NPO /X
Close to PHY
L1C3 0.1UF/16V X7R
L1C4 0.1UF/16V X7R
Close to PHY
SL1C1 0.1UF/16V X7R
SL1C2 0.1UF/16V X7R
Close to Chipset

S_X1_LAN1_RXP_C
S_X1_LAN1_RXN_C
S_X1_LAN1_TXP_C
S_X1_LAN1_TXN_C

L1_SMBCLK & L1_SMBDATA

Connect to PCH SML0CLK and SML0DATA and need to pull-up 499ohm resistors to +3VSB at PCH side.

<32> L1_SMBCLK
<32> L1_SMBDATA
L1C15 10PF/50V NPO /X
L1C16 10PF/50V NPO /X
Close to PHY

<69> L1_LAN_DISABLE#_R
L1R7 8.2KOhm /EUP
+3VSB_LAN1

L1_LAN_DISABLE#

PCH's GPIO12 pin must be set as "LAN_PHY_PWR_CTRL" function through FITC tool.

L1U1

PE_CLKP
PE_CLKN
PETp
PETn
PERp
PERn
SMB_CLK
SMB_DATA
LAN_DISABLE_N
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
TEST_EN
CLK_REQ_N
PE_RST_N
VDD0P9_46
VDD0P9_47
VDD0P9_37
VDD0P9_43
VDD0P9_11
VDD0P9_8
VDD0P9_40
VDD0P9_22
VDD0P9_16
CTRL0P9
WGI218V

MDI_PLUS[0] MDI_MINUS[0] MDI_PLUS[1] MDI_MINUS[1] MDI_PLUS[2] MDI_MINUS[2] MDI_PLUS[3] MDI_MINUS[3]
L1_MDI_P0 <68>
L1_MDI_N0 <68>
L1_MDI_P1 <68>
L1_MDI_N1 <68>
L1_MDI_P2 <68>
L1_MDI_N2 <68>
L1_MDI_P3 <68>
L1_MDI_N3 <68>

MDI differential impedance = 100ohm ± 15%
Trace length = 8inch

XTAL_OUT XTAL_IN
L1_XOUT L1_XIN

L1X1,L1C10,L1C11

Placement rule:
1.Place close to L1U1
2.Trace length <1inch

L1X1 25Mhz
L1C10 27PF/50V NPO
L1C11 27PF/50V NPO
07V900125000

LED2 LED1 LED0
L1_LINK100#_R
L1R5 300OHM
L1_LINK100# <68>
L1_LINK1000# <68>
L1_ACTLEDN <68>
L1R6 300OHM
L1_ACTLEDP <68>

VDD3P3_IN
L1U1C5 0.1UF/16V /X
L1U1C205 22UF/6.3V X5R
L1R9 4.7KOHM
L1R10 4.7KOHM

RSVD1_VCC3P3
LANWAKE_N
SVR_EN_N
L1_RSVD1
L1_SVR_EN
L1_LAN_WAKE#_R <69>
L1R4 SHORTPIN_0402_NM /X

L1_LAN_WAKE#

Must be connected to PCH's GPIO27

叫紘粄I218V 籔 PCH's GPIO27
ゲ斗璶 蝻T荼 蝻⊿荼

VDD3P3_4
VDD3P3_15
VDD3P3_19
VDD3P3_29
L1U1C4 1UF/10V

RBIAS
GND_EPAD
L1_LREXT
L1R1 3.01KOHM 1%

L1R1

被 ⇨貯のtrace叫叭ゲ粄follow layout rule

Placement rule:
1.Place close to L1U1
2.Trace length < 1 inch

GND1 GND2 GND3 GND4
02001V00430000

Internal SVR

Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0

+L1_0.9V
L1U1C8 0.1UF/16V
L1U1C16 0.1UF/16V
L1U1C40 0.1UF/16V
L1U1C47 0.1UF/16V
L1L7 /X SHORTPIN_0603_NM

+L1_0.9V_VOUT_L
L1L1 4.7UH
+L1_0.9V_VOUT
L1U1C407 0.1UF/16V
L1U1C207 10UF/6.3V mbs_c0805 X5R /X
L1U1C7 22UF/6.3V X5R
L1L1 Idc_min=500 mA Rdc_max=100 mohm

Placement rule:
1.Place close to L1U1
2.+L1_0.9V_VOUT Trace length < 500mil
3.Trace wide > 20mil
4.L1U1C407,L1U1C207,L1U1C7 close to L1L1 pin1

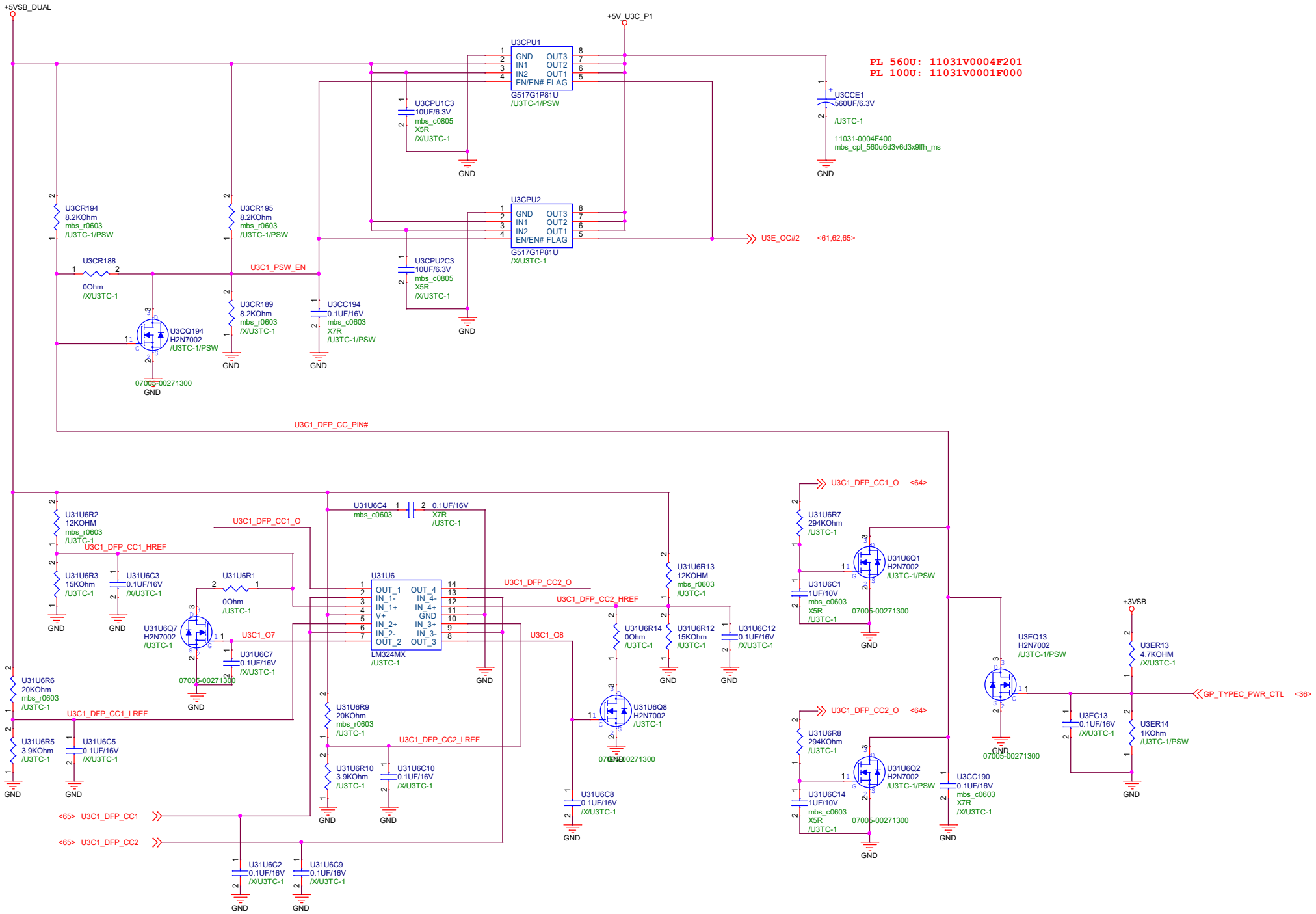
<29,42,48,52,75,86,117> S_PLTRST#
L1C14 10PF/50V NPO /X

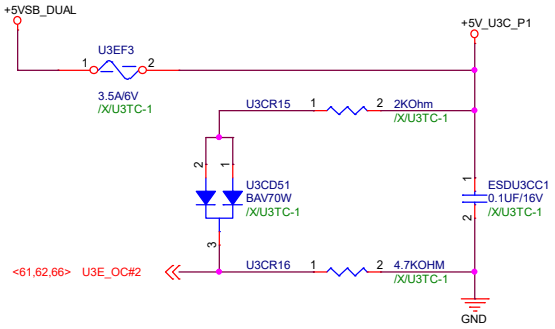
+3VSB
L1R17 8.2KOhm N/A
L1R8 1KOhm
L1_TEST_EN
<28> L1_LAN_CLKREQ2#
L1R16 0Ohm N/A
CLKREQ#_LAN1_R

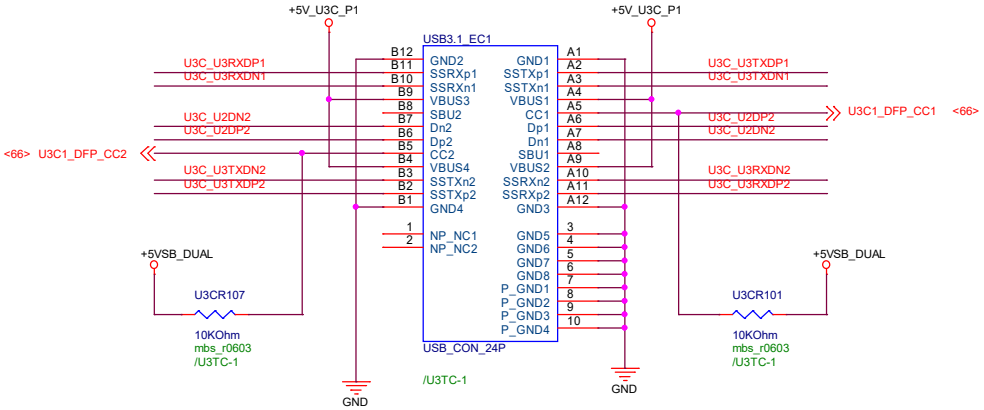
BOM	
N/A	mount
/X	unmount

STANDARD CIRCUIT
XUMB | LAN
LAN_0.4E
LOGO_HD_DEMO_LAN
/X

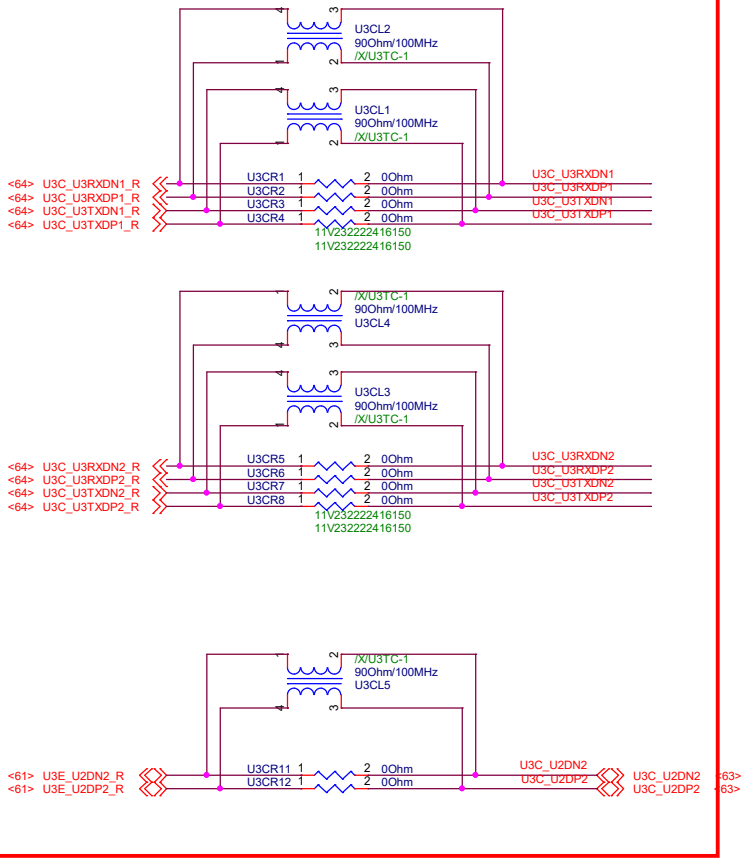
I218V: 02001-00300100
I219V: 02001-00430000


+5VSB_DUAL
+5V_U3C_P1
U3CPU1
GND OUT3
IN1 OUT2
IN2 OUT1
EN/EN# FLAG
G517G1P81U
/U3TC-1/PSW
U3CPU1C3
10UF/6.3V
mbs_c0805
X5R
/X/U3TC-1
U3CCE1
560UF/6.3V
/U3TC-1
11031-0004F400
mbs_cpl_560u6d3v6d3x9lfh_ms
PL 560U: 11031V0004F201
PL 100U: 11031V0001F000
U3CPU2
G517G1P81U
/X/U3TC-1
U3CPU2C3
10UF/6.3V
mbs_c0805
X5R
/X/U3TC-1
U3E_OC#2 <61,62,65>
U3CR194
8.2KOhm
mbs_r0603
/U3TC-1/PSW
U3CR195
8.2KOhm
mbs_r0603
/U3TC-1/PSW
U3CR188
0Ohm
/X/U3TC-1
U3C1_PSW_EN
U3CR189
8.2KOhm
mbs_r0603
/X/U3TC-1
U3CC194
0.1UF/16V
mbs_c0603
X7R
/U3TC-1/PSW
U3CQ194
H2N7002
/U3TC-1/PSW
07005-00271300
GND
U3C1_DFP_CC_PIN#
U31U6R2
12KOHM
mbs_r0603
/U3TC-1
U3C1_DFP_CC1_HREF
U31U6R3
15KOhm
/U3TC-1
U31U6C3
0.1UF/16V
/X/U3TC-1
U31U6R1
0Ohm
/U3TC-1
U31U6Q7
H2N7002
/U3TC-1
U3C1_O7
U31U6C7
0.1UF/16V
/X/U3TC-1
U31U6R6
20KOhm
mbs_r0603
/U3TC-1
U3C1_DFP_CC1_LREF
U31U6R5
3.9KOhm
/U3TC-1
U31U6C5
0.1UF/16V
/X/U3TC-1
U31U6C4
0.1UF/16V
X7R
/U3TC-1
U3C1_DFP_CC1_O
U31U6
OUT_1 OUT_4
IN_1- IN_4-
IN_1+ IN_4+
V+ GND
IN_2+ IN_3+
IN_2- IN_3-
OUT_2 OUT_3
LM324MX
/U3TC-1
U3C1_DFP_CC2_O
U3C1_DFP_CC2_HREF
U3C1_O8
U31U6R9
20KOhm
mbs_r0603
/U3TC-1
U3C1_DFP_CC2_LREF
U31U6R10
3.9KOhm
/U3TC-1
U31U6C10
0.1UF/16V
/X/U3TC-1
U31U6C8
0.1UF/16V
/X/U3TC-1
<65> U3C1_DFP_CC1
<65> U3C1_DFP_CC2
U31U6C2
0.1UF/16V
/X/U3TC-1
U31U6C9
0.1UF/16V
/X/U3TC-1
U31U6R13
12KOHM
mbs_r0603
/U3TC-1
U31U6R14
0Ohm
/U3TC-1
U31U6R12
15KOhm
/U3TC-1
U31U6C12
0.1UF/16V
/X/U3TC-1
U31U6Q8
H2N7002
/U3TC-1
U3C1_DFP_CC1_O <64>
U31U6R7
294KOhm
/U3TC-1
U31U6Q1
H2N7002
/U3TC-1/PSW
U31U6C1
1UF/10V
mbs_c0603
X5R
/U3TC-1
U3C1_DFP_CC2_O <64>
U31U6R8
294KOhm
/U3TC-1
U31U6Q2
H2N7002
/U3TC-1/PSW
U31U6C14
1UF/10V
mbs_c0603
X5R
/U3TC-1
U3CC190
0.1UF/16V
mbs_c0603
X7R
/X/U3TC-1
U3EQ13
H2N7002
/U3TC-1/PSW
+3VSB
U3ER13
4.7KOHM
/X/U3TC-1
U3EC13
0.1UF/16V
/X/U3TC-1
U3ER14
1KOhm
/U3TC-1/PSW
GP_TYPEC_PWR_CTL <36>
GND

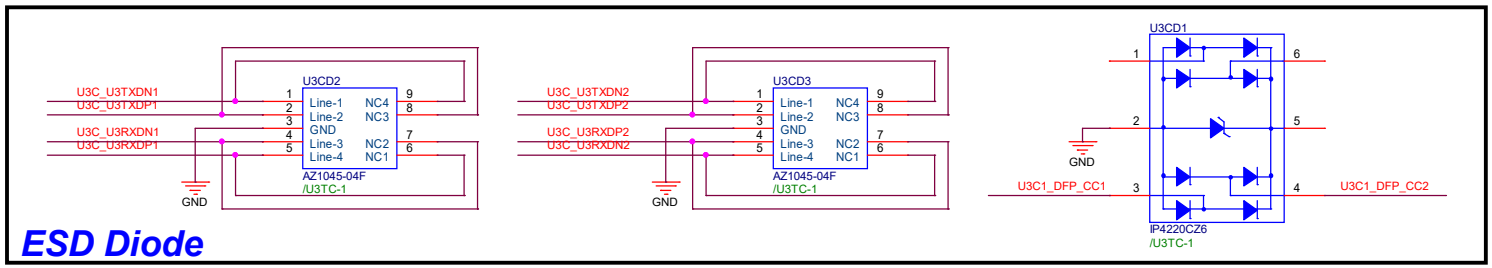




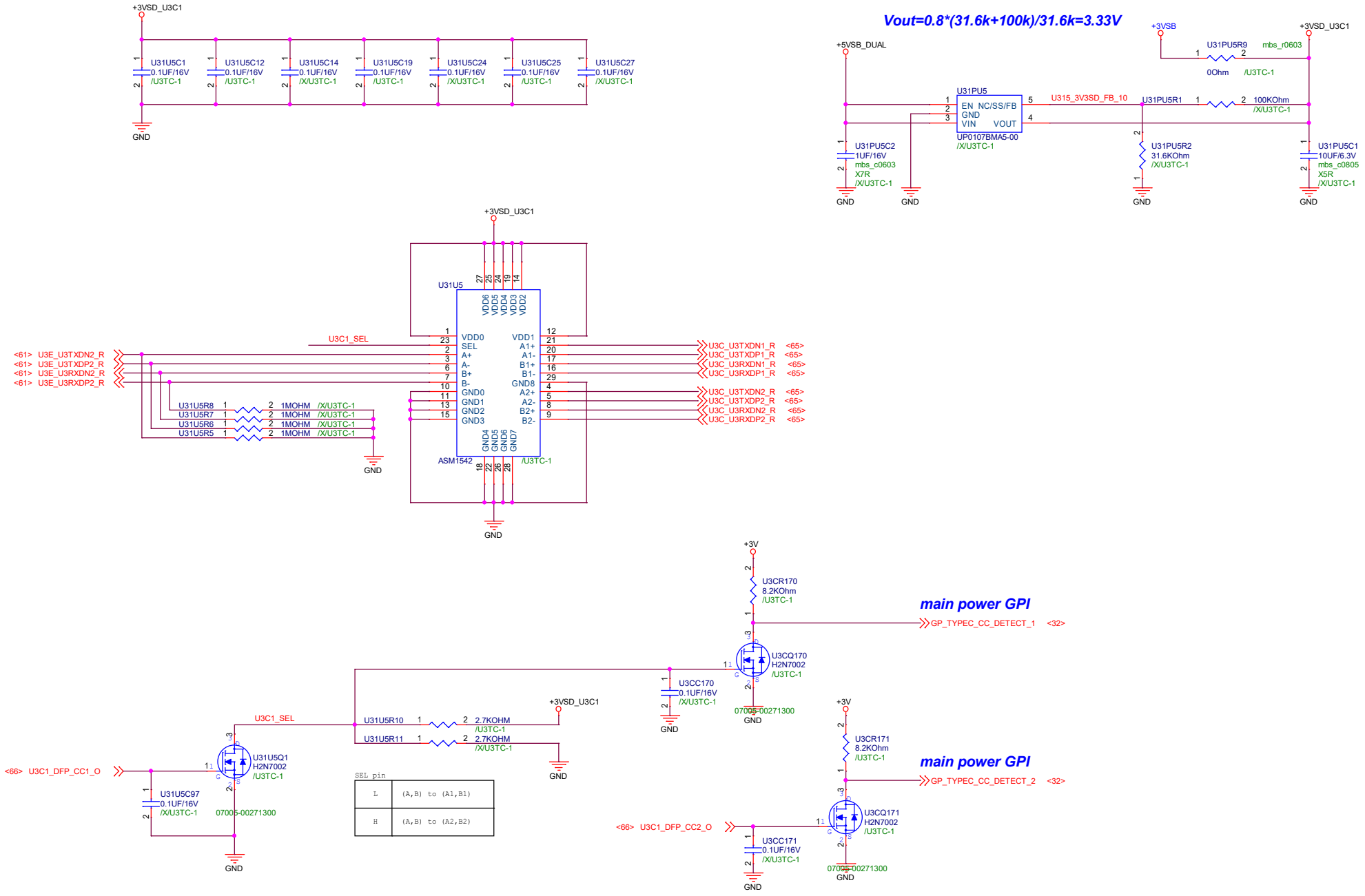
Reserve EMI Choke (Single RES)



Delete it for EMS



ESD Diode


+3VSD_U3C1
U31U5C1 0.1UF/16V /U3TC-1
U31U5C12 0.1UF/16V /U3TC-1
U31U5C14 0.1UF/16V /X/U3TC-1
U31U5C19 0.1UF/16V /U3TC-1
U31U5C24 0.1UF/16V /X/U3TC-1
U31U5C25 0.1UF/16V /U3TC-1
U31U5C27 0.1UF/16V /X/U3TC-1
GND
Vout=0.8*(31.6k+100k)/31.6k=3.33V
+5VSB_DUAL
+3VSB
+3VSD_U3C1
U31PU5R9 mbs_r0603 0Ohm /U3TC-1
U31PU5
EN NC/SS/FB
GND
VIN VOUT
UP0107BMA5-00 /X/U3TC-1
U315_3V3SD_FB_10
U31PU5R1 100KOhm /X/U3TC-1
U31PU5R2 31.6KOhm /X/U3TC-1
U31PU5C2 1UF/16V mbs_c0603 X7R /X/U3TC-1
U31PU5C1 10UF/6.3V mbs_c0805 X5R /X/U3TC-1
U31U5
ASM1542 /U3TC-1
VDD0 SEL A+ A- B+ B- GND0 GND1 GND2 GND3
VDD1 A1+ A1- B1+ B1- GND8 A2+ A2- B2+ B2-
U3C1_SEL
<61> U3E_U3TXDN2_R
<61> U3E_U3TXDP2_R
<61> U3E_U3RXDN2_R
<61> U3E_U3RXDP2_R
U31U5R8 1MOHM /X/U3TC-1
U31U5R7 1MOHM /X/U3TC-1
U31U5R6 1MOHM /X/U3TC-1
U31U5R5 1MOHM /X/U3TC-1
U3C_U3TXDN1_R <65>
U3C_U3TXDP1_R <65>
U3C_U3RXDN1_R <65>
U3C_U3RXDP1_R <65>
U3C_U3TXDN2_R <65>
U3C_U3TXDP2_R <65>
U3C_U3RXDN2_R <65>
U3C_U3RXDP2_R <65>
+3V
U3CR170 8.2KOhm /U3TC-1
main power GPI
GP_TYPEC_CC_DETECT_1 <32>
U3CQ170 H2N7002 /U3TC-1
U3CC170 0.1UF/16V /X/U3TC-1
07005-00271300
U3CR171 8.2KOhm /U3TC-1
main power GPI
GP_TYPEC_CC_DETECT_2 <32>
U3CQ171 H2N7002 /U3TC-1
<66> U3C1_DFP_CC2_O
U3CC171 0.1UF/16V /X/U3TC-1
U3C1_SEL
U31U5R10 2.7KOHM /U3TC-1
U31U5R11 2.7KOHM /X/U3TC-1
<66> U3C1_DFP_CC1_O
U31U5Q1 H2N7002 /U3TC-1
U31U5C97 0.1UF/16V /X/U3TC-1
SEL pin
L (A,B) to (A1,B1)
H (A,B) to (A2,B2)

PL CAP

+5VSB_DUAL

PL 560U: 11031V0004F201
PL 100U: 11031V0001F000

GND

OP2

+5VSB_DUAL

U3EF1
3.5A/6V
/ASM1142-1

+5V_U3E_P1

U3ER15 2KOhm /ASM1142-1

U3ED51
BAV70W
/ASM1142-1

ESDU3EC1
0.1UF/16V
/X

<61,62> U3E_OC#1

U3ER16 4.7KOHM /ASM1142-1

GND

OP3 - Connector

Ext USB 3.1 Connector 1&2

+5V_U3E_P1

USB3.1_EA1

U3E_U2DN1	2	D-
U3E_U2DP1	3	D+
	1	VBUS
	4	GND
U3E_U3RXDN1	5	STDA_SSRX-
U3E_U3RXDP1	6	STDA_SSRX+
	7	GND_DRAIN
U3E_U3TXDN1	8	STDA_SSTX-
U3E_U3TXDP1	9	STDA_SSTX+
	10	P_GND1
	11	P_GND3
	12	P_GND4
	13	P_GND2

USB_CON_9P
/ASM1142-1

12013-00051100

GND

OP3

OP1 - EMI Choke

Reserve EMI Choke (Single RES)

U3EL2
90Ohm/100MHz
/X/ASM1142-1

U3EL1
90Ohm/100MHz
/X/ASM1142-1

<61> U3E_U3RXDN1_R	U3ER1	0Ohm /ASM1142-1	U3E_U3RXDN1
<61> U3E_U3RXDP1_R	U3ER2	0Ohm /ASM1142-1	U3E_U3RXDP1
<61> U3E_U3TXDN1_R	U3ER3	0Ohm /ASM1142-1	U3E_U3TXDN1
<61> U3E_U3TXDP1_R	U3ER4	0Ohm /ASM1142-1	U3E_U3TXDP1

U3EL6
90Ohm/100MHz
/X/ASM1142-1

<61> U3E_U2DN1_R	U3ER9	0Ohm /ASM1142-1	U3E_U2DN1
<61> U3E_U2DP1_R	U3ER10	0Ohm /ASM1142-1	U3E_U2DP1

OP1

Delete it for EMS

U3ED2

U3E_U3RXDN1	1	Line-1	NC4 9
U3E_U3RXDP1	2	Line-2	NC3 8
	3	GND	
U3E_U3TXDN1	4	Line-3	NC2 7
U3E_U3TXDP1	5	Line-4	NC1 6

AZ1045-04F
/ASM1142-1

GND

U3ED1

U3E_U2DP1 — 1 — 6 — U3E_U2DN1

+5VSB — 5

2 — GND

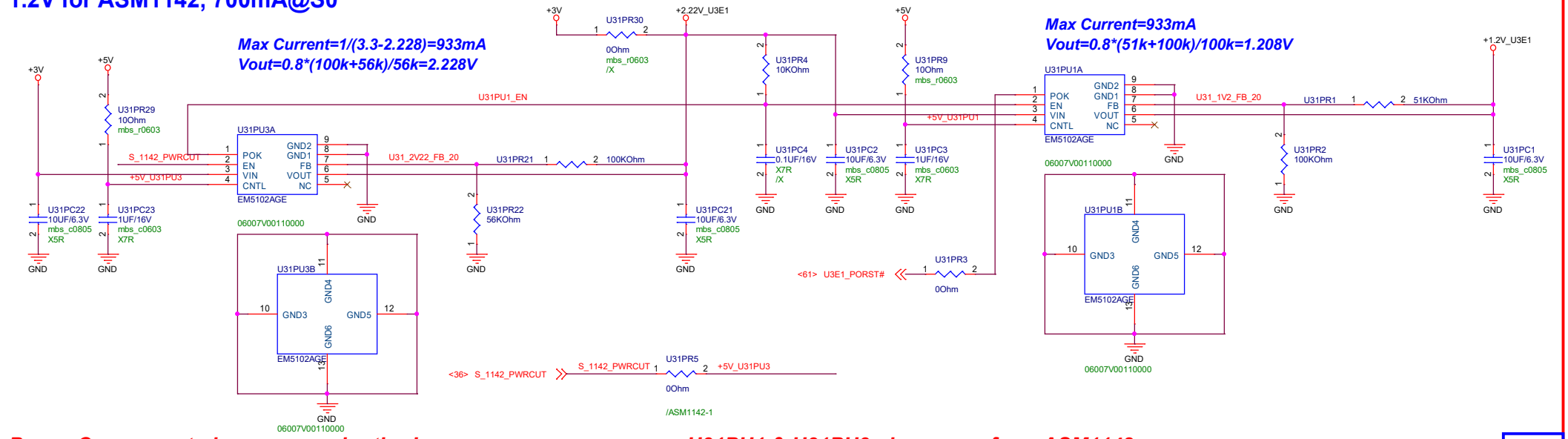
<65> U3C_U2DP2 — 3 — 4 — U3C_U2DN2 <65>

IP4220CZ6
/ASM1142-1

ESD Diode

OP5 - Core Power

1.2V for ASM1142, 700mA@S0



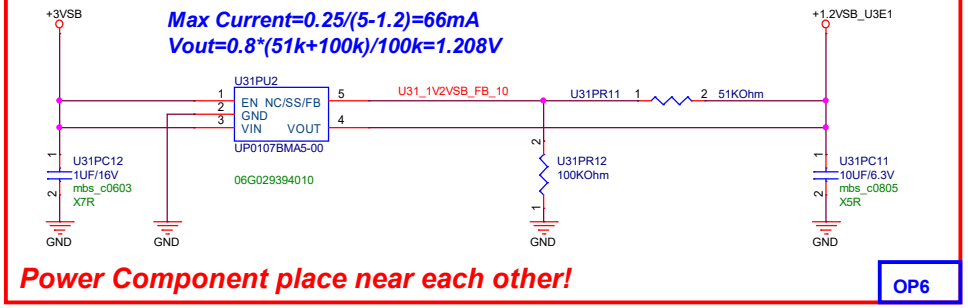
Power Component place near each other!

U31PU1 & U31PU3 place away from ASM1142

OP5

OP6 - Stand By Power

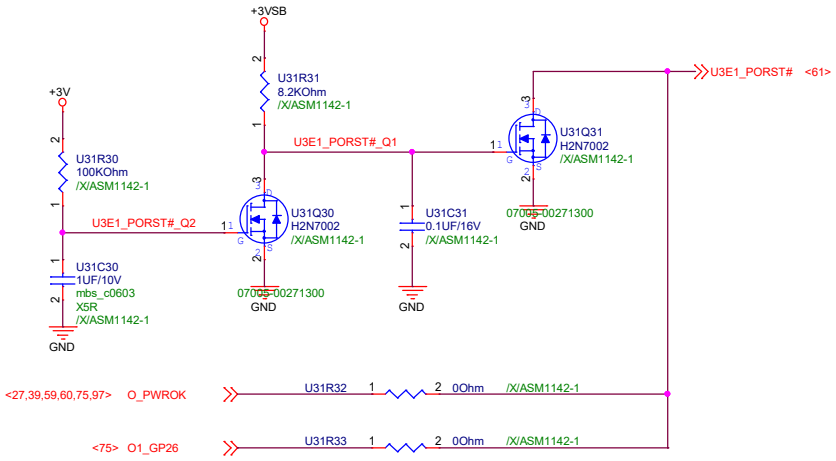
1.2VSB for ASM1142, 5mA@S0, 1mA@S3/S4/S5



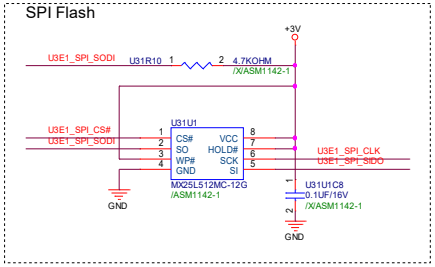
Power Component place near each other!

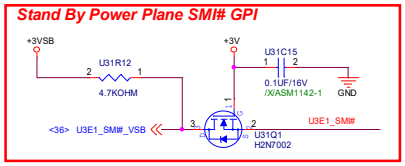
OP6

ASM1142 Power On Reset Sequence

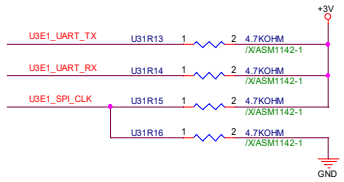


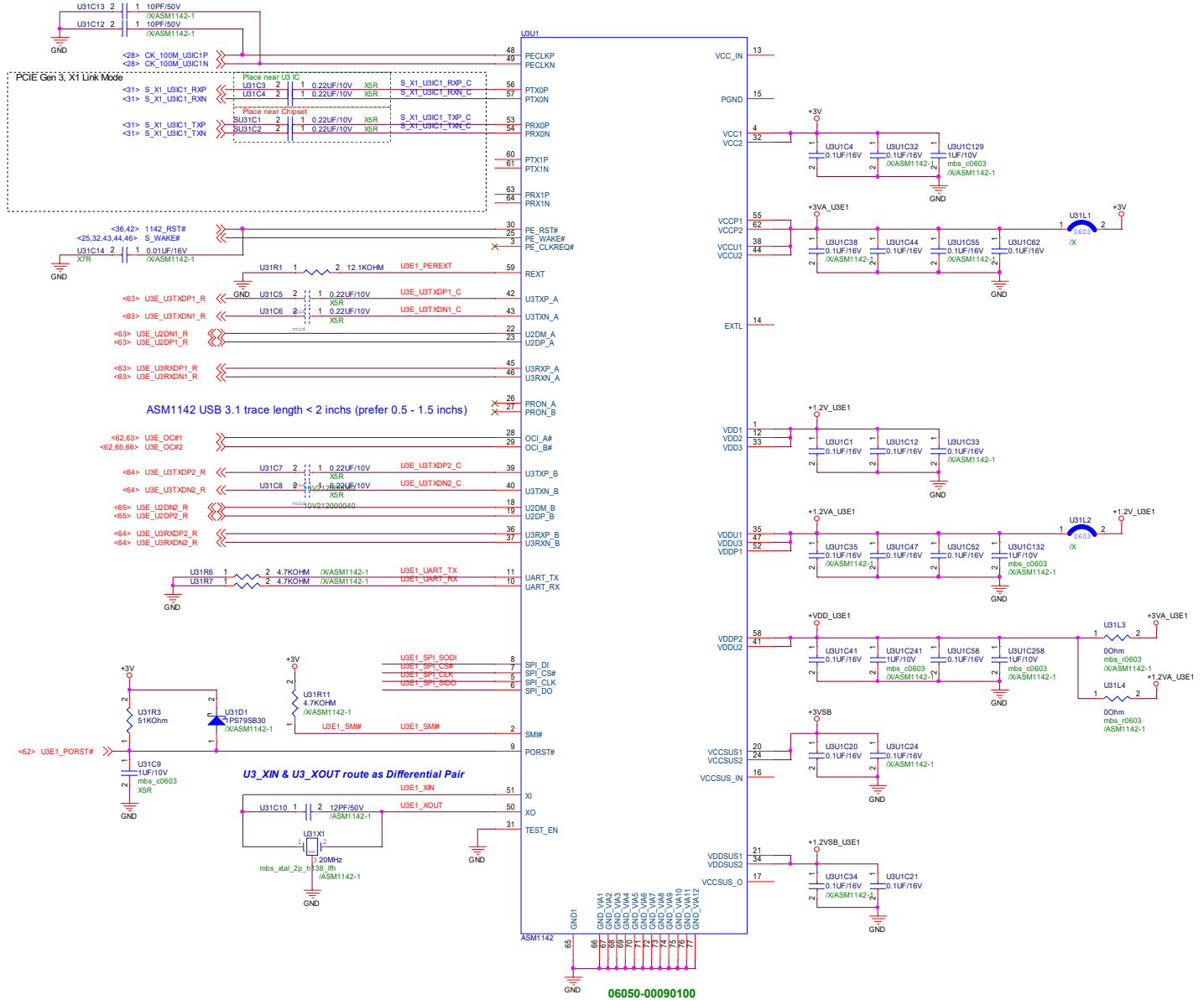
	PCIE Speed	PCIE Link Mode	AC Cap
ASM1042AE	Gen 2	X1 Link Mode	0.1UF
ASM1142	Gen 2	X2 Link Mode	0.1UF
	Gen 3	X1 Link Mode	0.22UF





07005-00271300



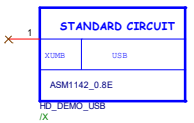


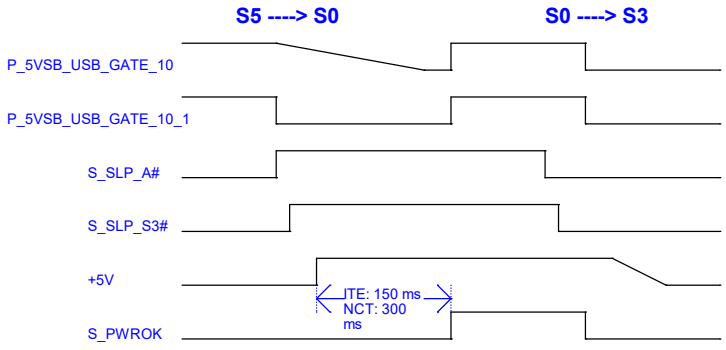
06050-00090100

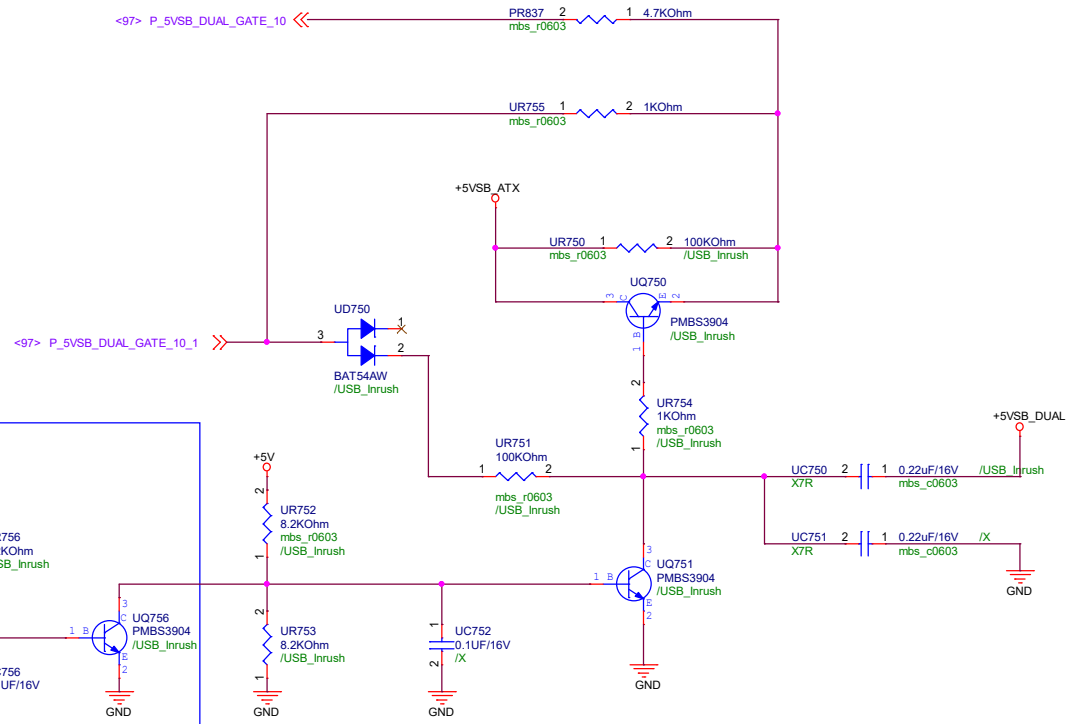
ASM1142 A2: 06050-00090100

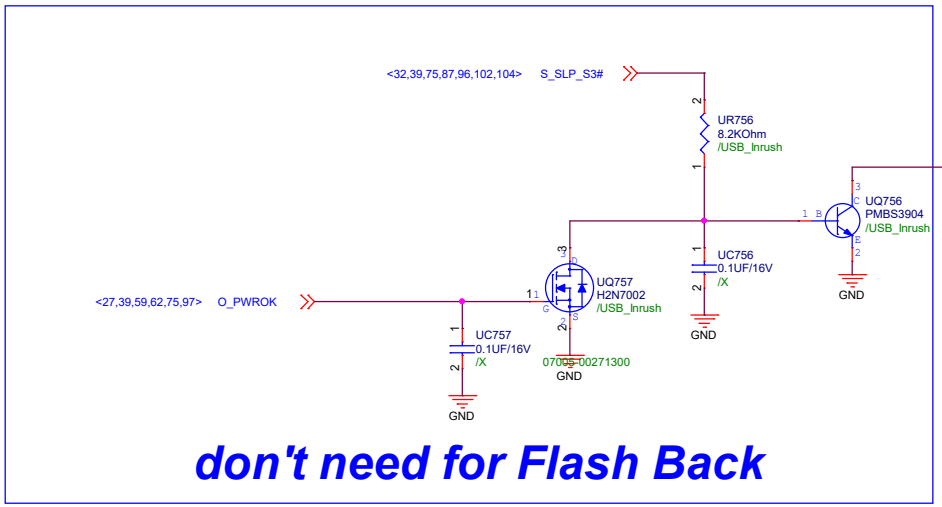
BOM	20MHz Crystal	48MHz Clock
U31X1	mount	unmount
U31C10	mount	unmount
U31R4	unmount	mount
U31R7	unmount	mount

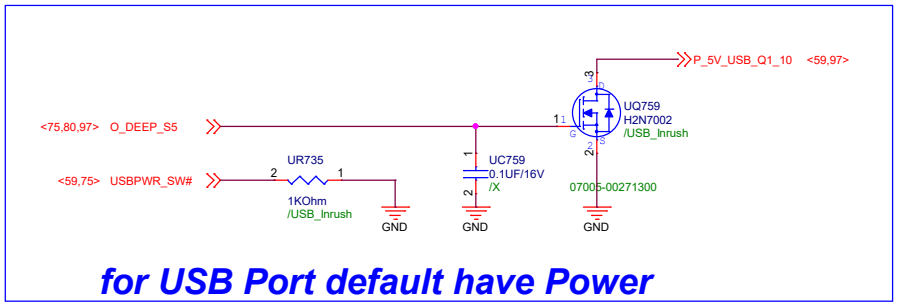
BOM	
N/A	mount
/X	unmount
/ASM1142-1	mount
/X/ASM1142-1	unmount



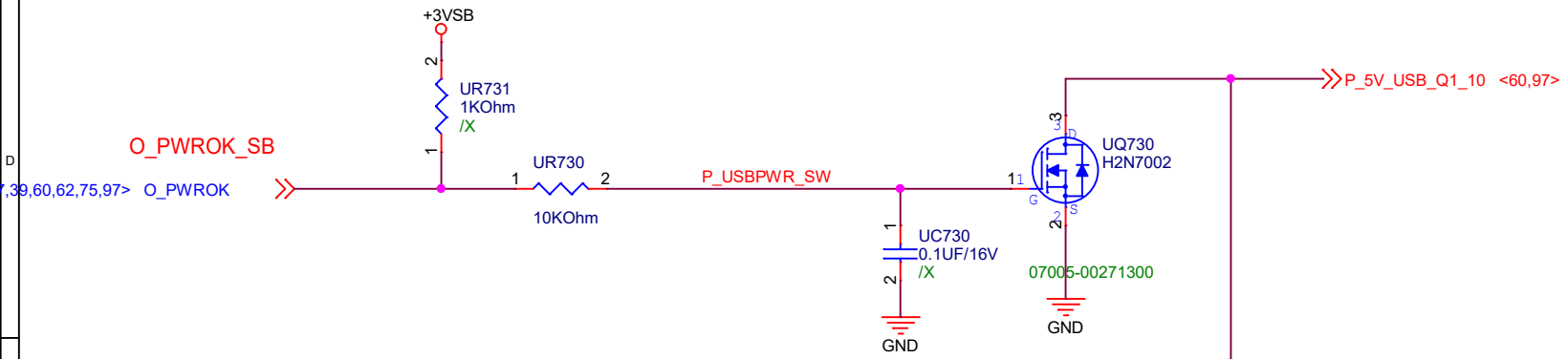




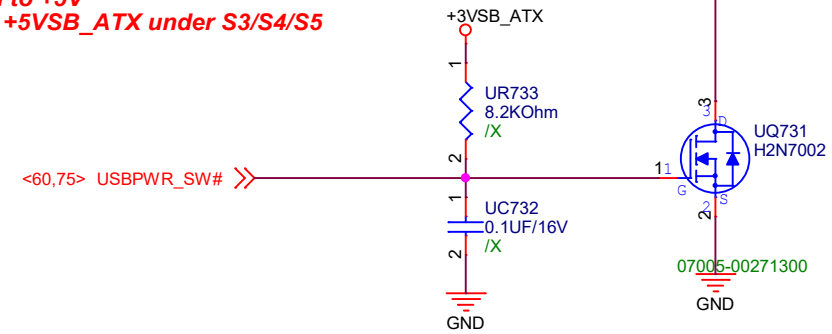


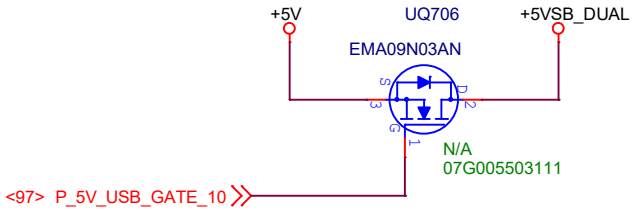


Inrush Circuit for USB Port default have Power or Flash Back Function



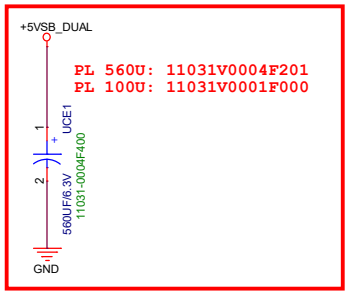
USBPWR_SW# GPIO select:
1. could be GPI & GPO both
2. default GPI (no internal pull-down/pull-high resistor)
3. +3VSB_ATX power plane, 3V tolerance
4. High level to force +5VSB_DUAL switch to +5V
5. Low level to let +5VSB_DUAL switch to +5VSB_ATX under S3/S4/S5
6. default need High level



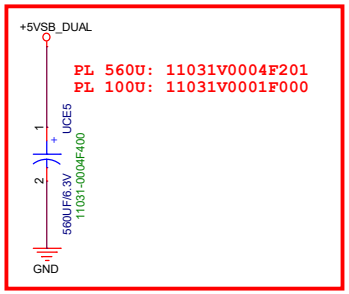


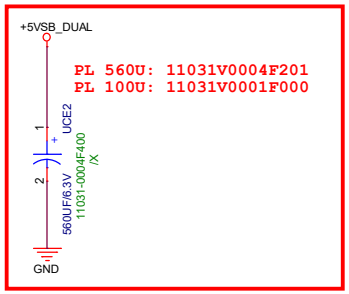
+5VSB_DUAL current:
DIMM*4=7A, DIMM*2=5A
USB 2.0=0.5A/port
USB 3.0=1A/port
if +5VSB_DUAL current (DIMM+USB 2.0 Port+USB 3.0 Port) > 15A, add UQ706

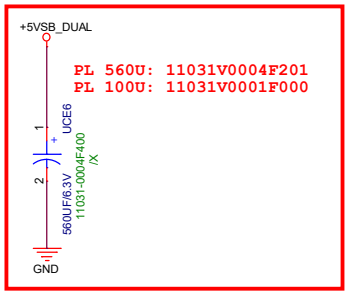
PL CAP



PL CAP





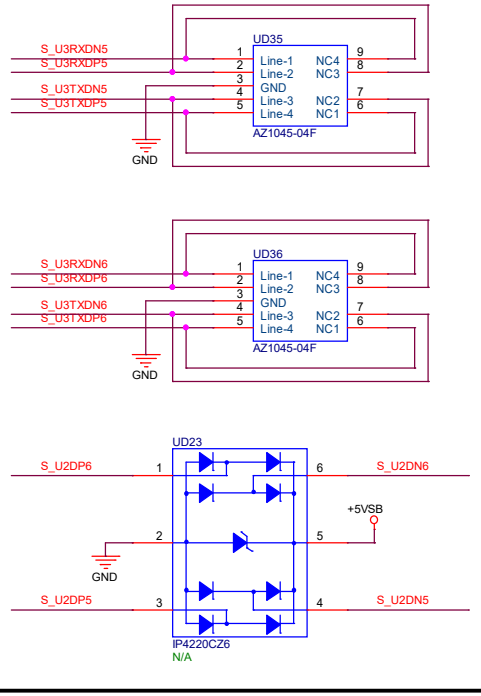


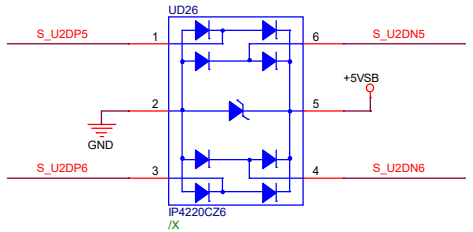
BOM	
N/A	mount
/X	unmount

Port 56

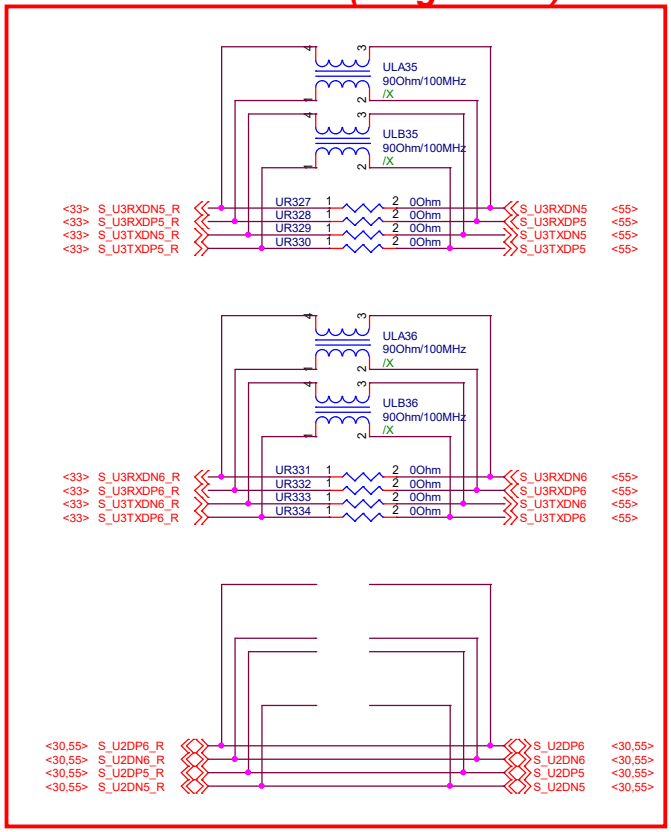
Delete it for EMS

ESD Diode





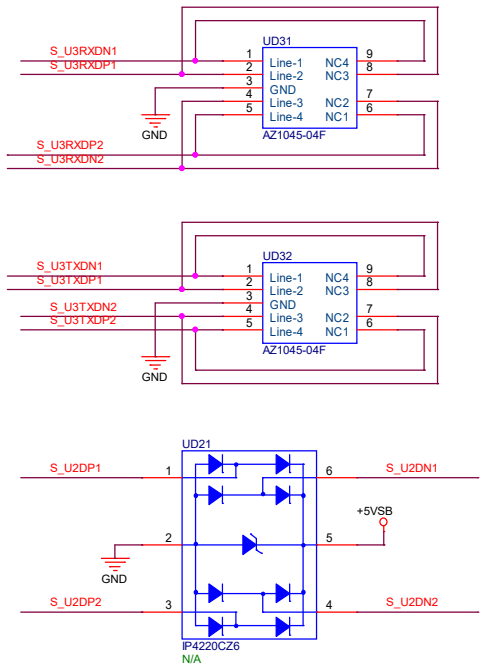
Reserve EMI Choke (Single RES)



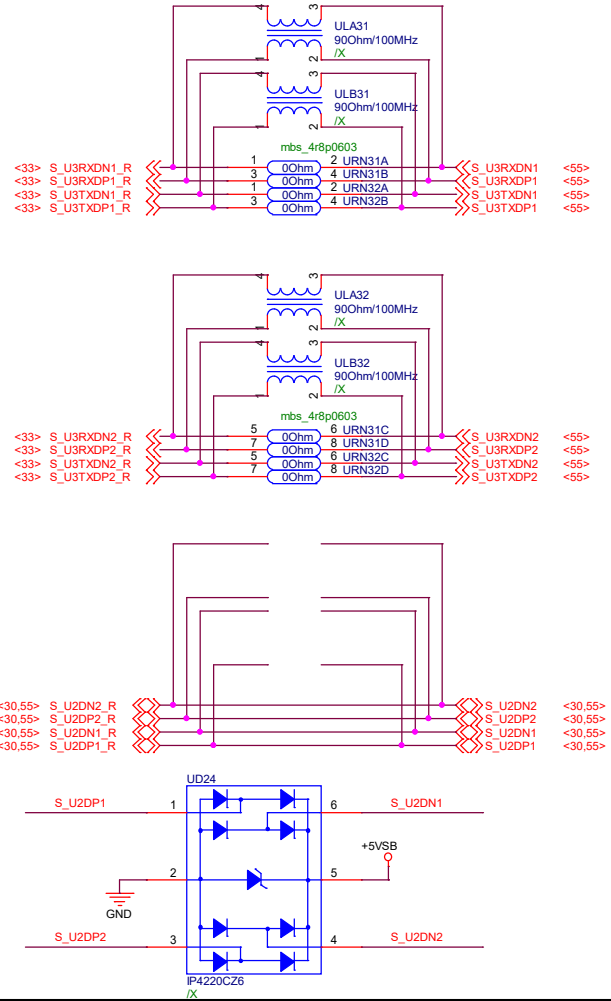
Port 12

Delete it for EMS

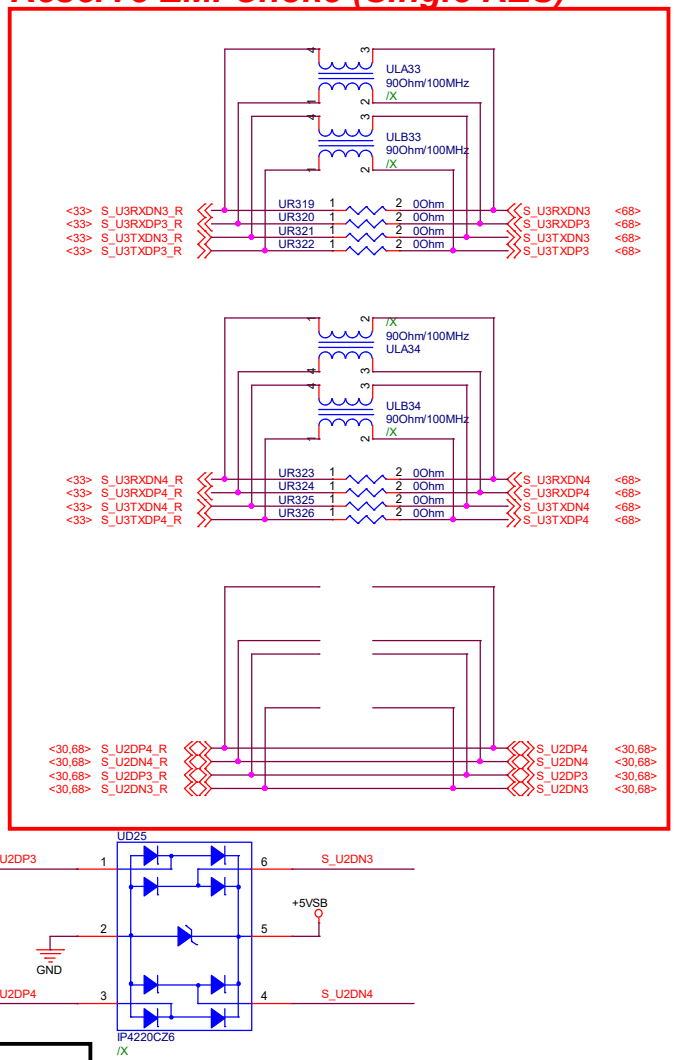
ESD Diode



Reserve EMI Choke (RES A)



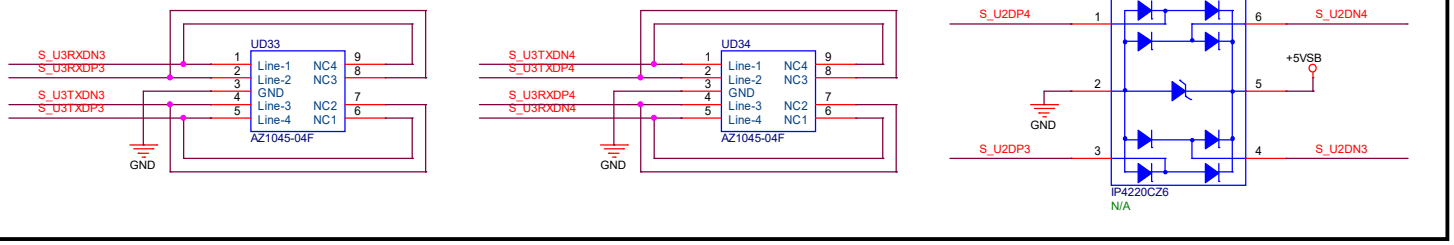
Reserve EMI Choke (Single RES)



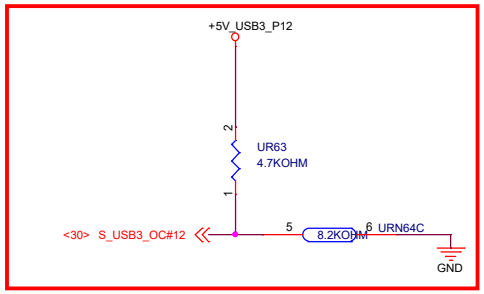
Port 34

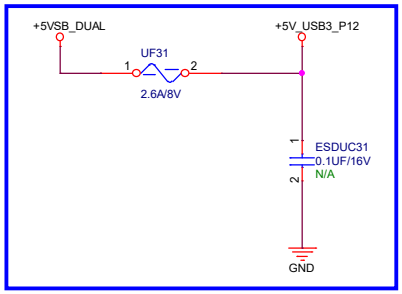
Delete it for EMS

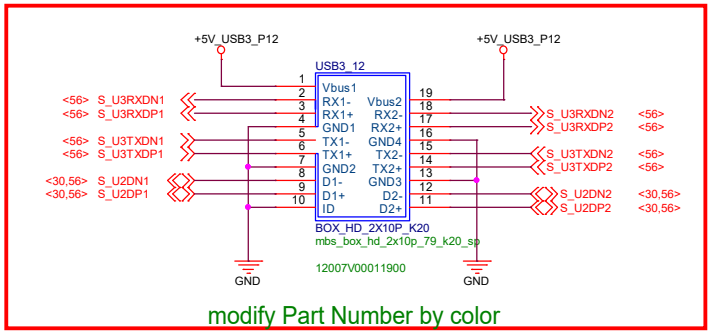
ESD Diode

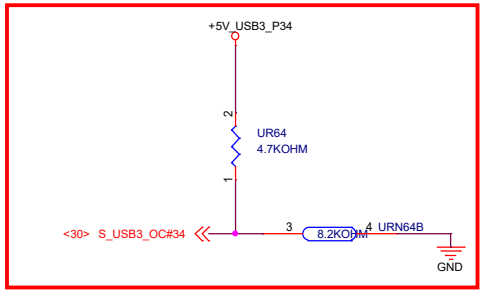


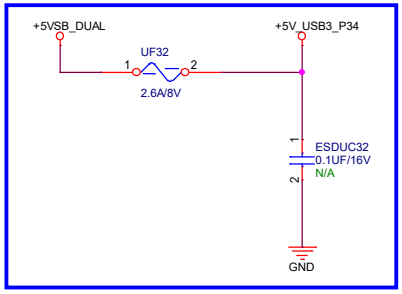
OC# circuit for Intel

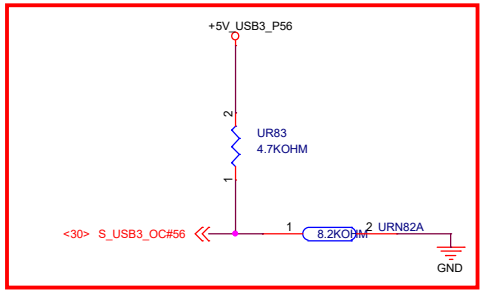


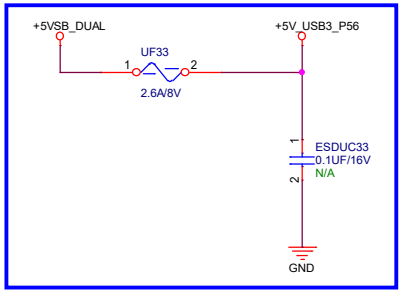


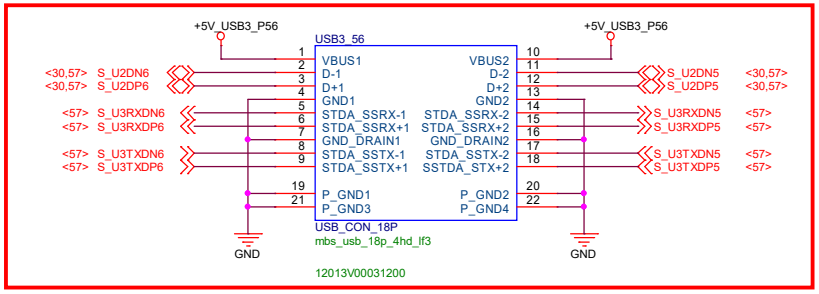


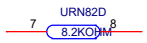






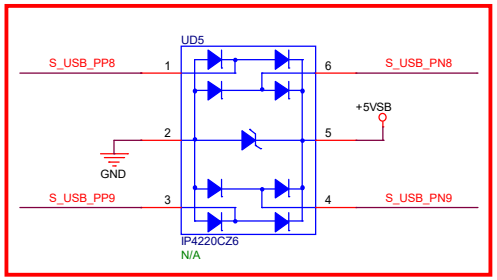


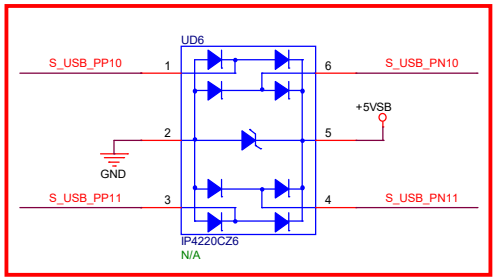




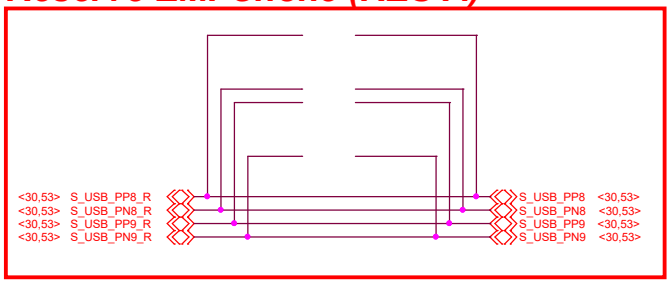
Delete it for EMC

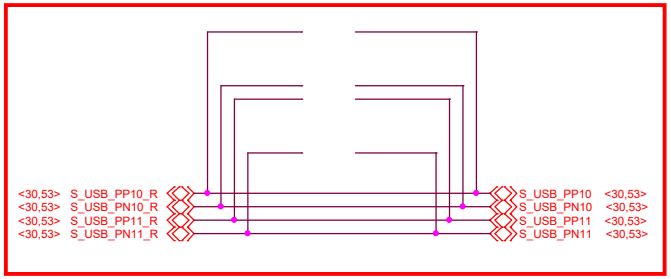
ESD Diode



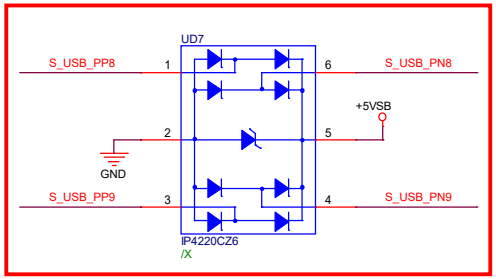


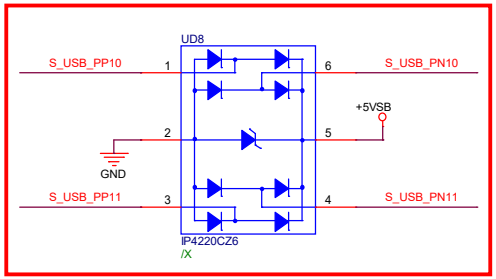
Reserve EMI Choke (RES A)



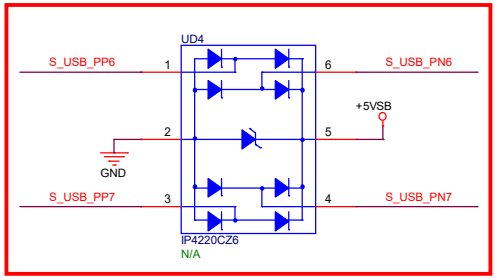


ESD Diode

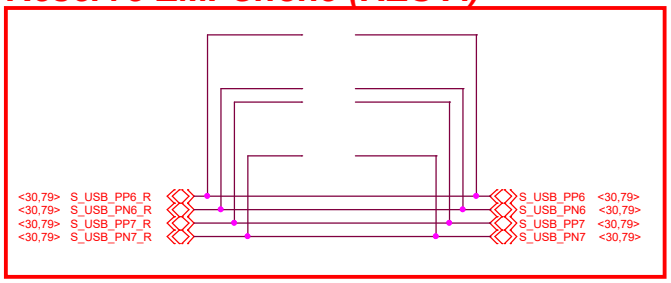




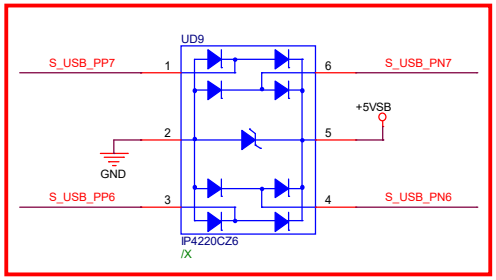
ESD Diode



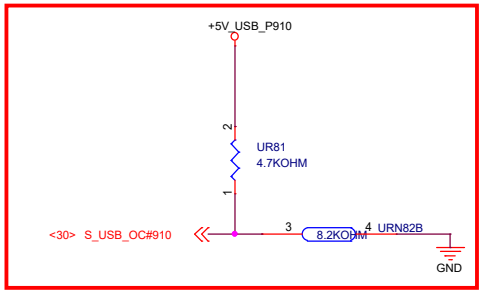
Reserve EMI Choke (RES A)

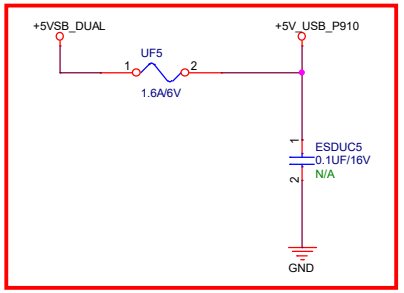


ESD Diode

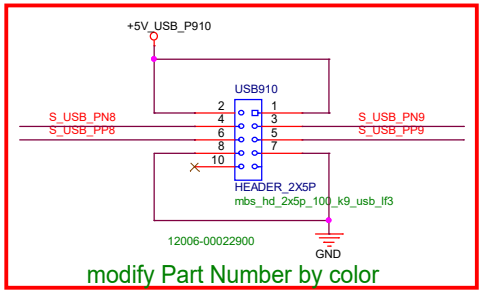


OC# circuit for Intel

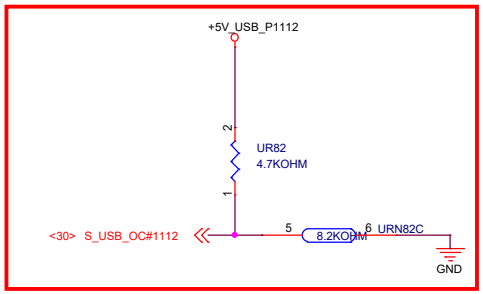


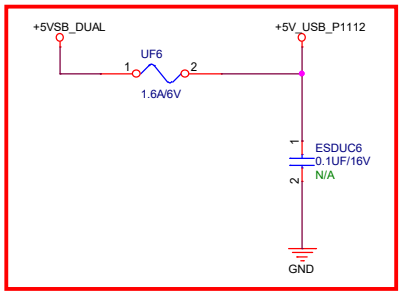


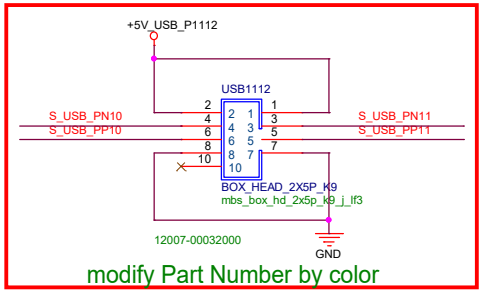
USB2 Box Header



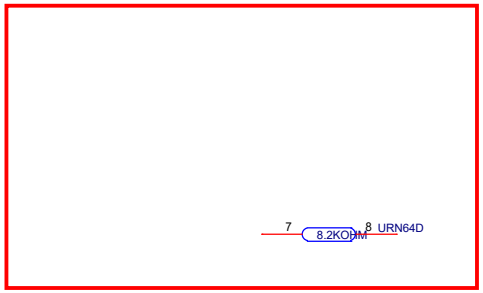
<30,54> S_USB_PN8
<30,54> S_USB_PP8
<30,54> S_USB_PN9
<30,54> S_USB_PP9



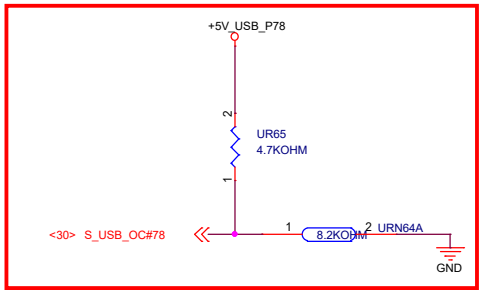


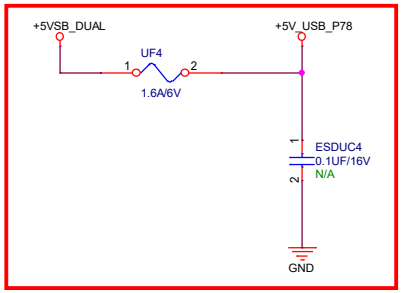


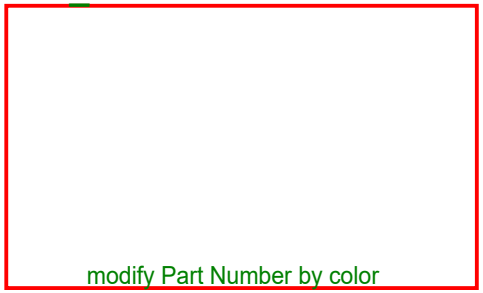
<30,54> S_USB_PN10
<30,54> S_USB_PP10
<30,54> S_USB_PN11
<30,54> S_USB_PP11

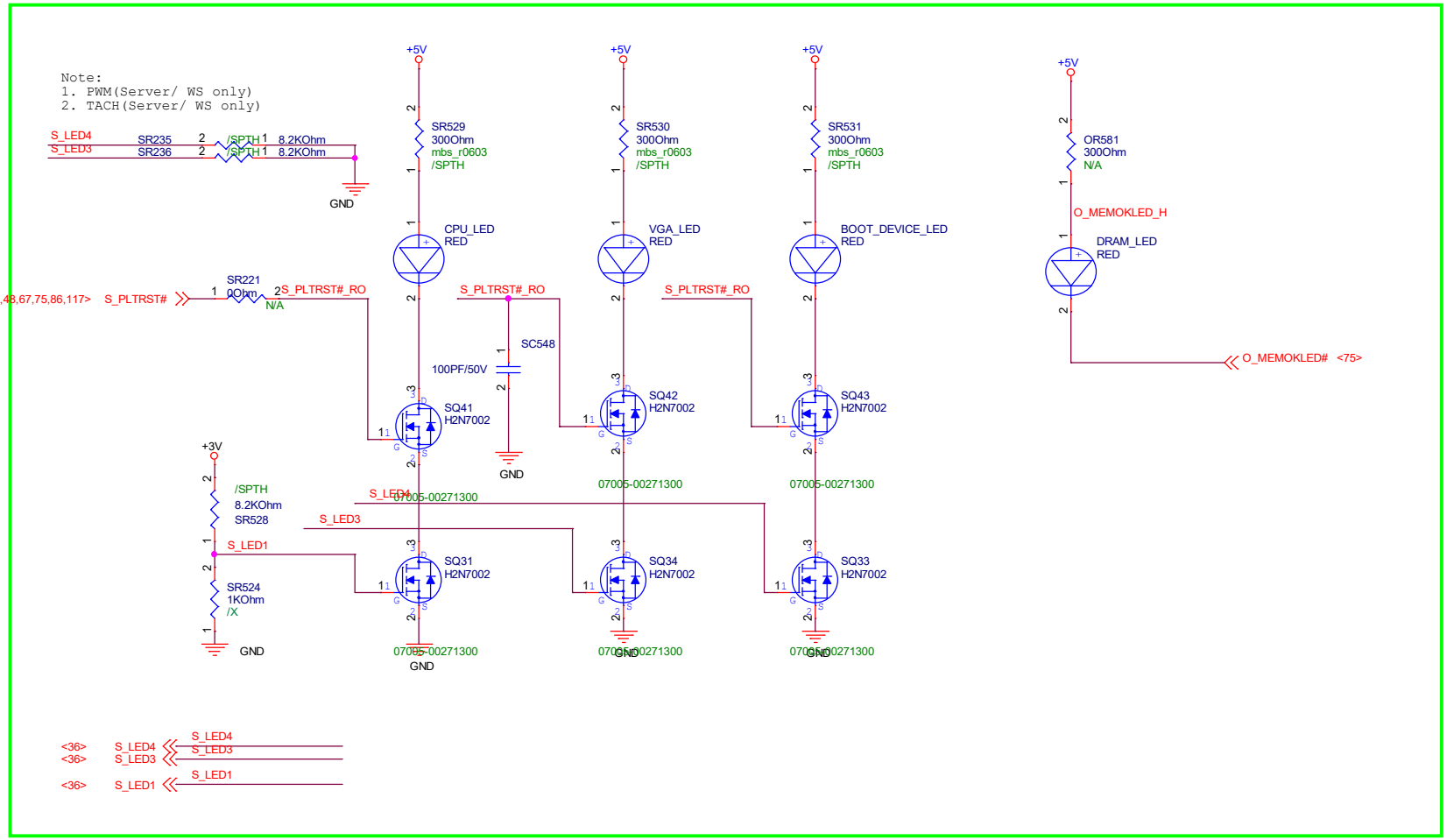


USB2 Box Header FOR OC_PANEL





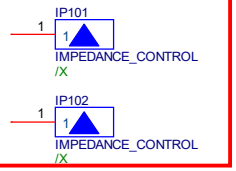



Note:
1. PWM(Server/ WS only)
2. TACH(Server/ WS only)
S_LED4
S_LED3
SR235
SR236
/SPTH
8.2KOhm
GND
+5V
SR529
SR530
SR531
300Ohm
mbs_r0603
CPU_LED
VGA_LED
BOOT_DEVICE_LED
RED
SR221
0Ohm
N/A
S_PLTRST#
S_PLTRST#_RO
SC548
100PF/50V
SQ41
SQ42
SQ43
H2N7002
07005-00271300
+3V
SR528
SR524
1KOhm
/X
S_LED1
SQ31
SQ34
SQ33
OR581
O_MEMOKLED_H
DRAM_LED
O_MEMOKLED# <75>
<36> S_LED4
<36> S_LED3
<36> S_LED1

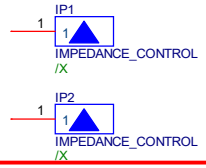
Priority1, must choose if MB have these functions

80 Ohm +/- 10%

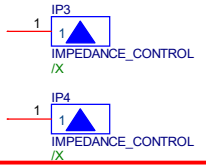
U3.1



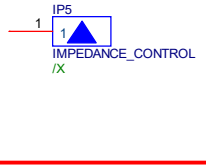
1 LAN



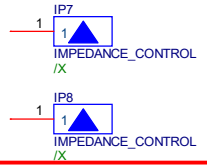
2 PCIE GEN2/3



3 DDR3 DATA&CTRL

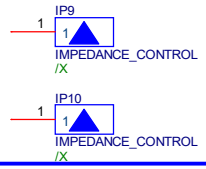


4 USB2.0

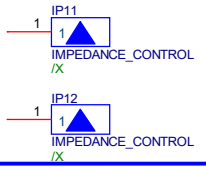


Priority2, can choose if MB have these functions (by project)

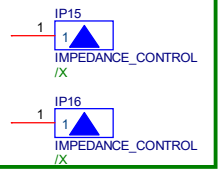
1 DP/DVI/HDMI



2 USB3.0



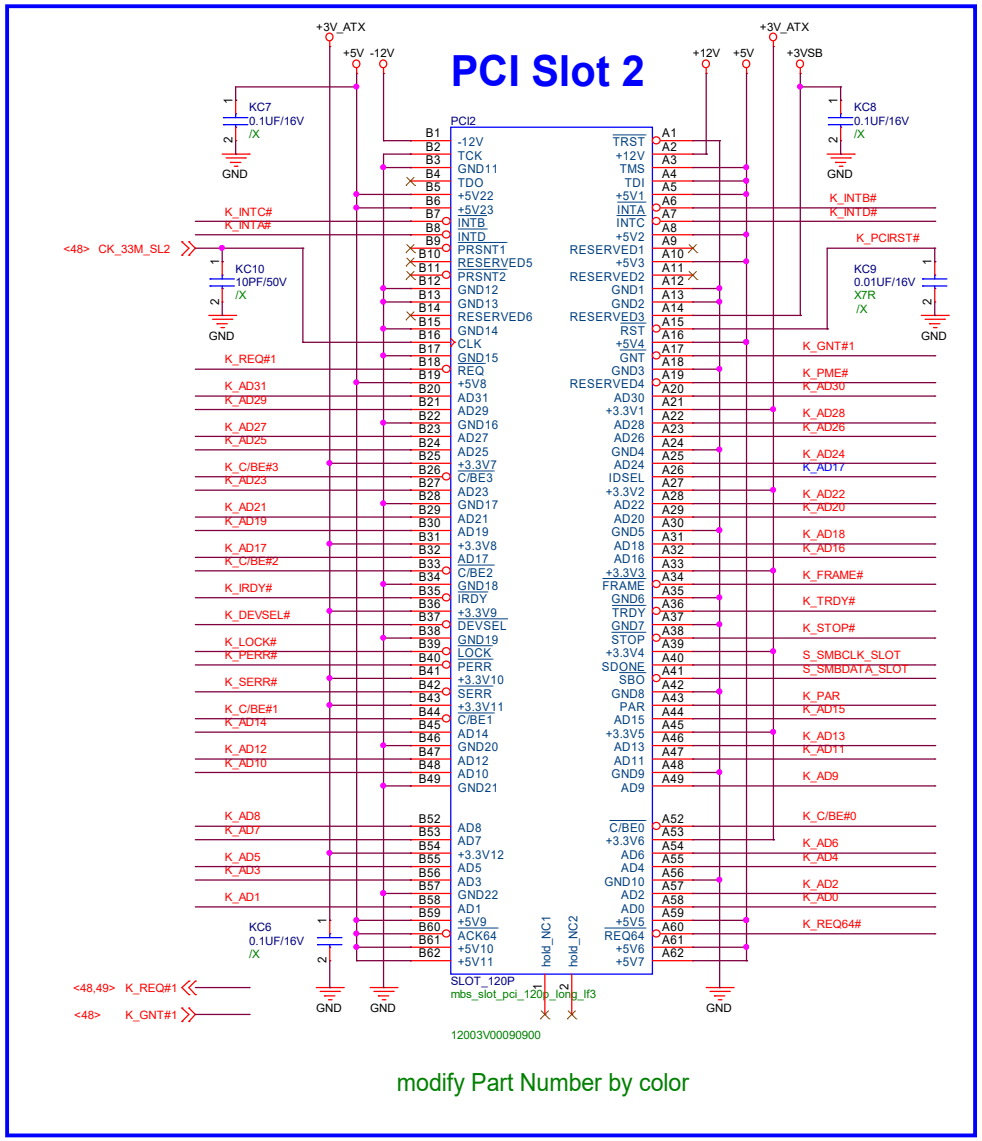
DDR3 CLK



2

signal	W/P	Impedance
LAN	4/8	100 ohm +- 15%
USB/SATA/ PCIE/DP/HDMI	4/4	85 ohm +- 15%
DDR CLK	8/5	62 ohm +- 15%
DDRDATA&CTRL	6.5	40 ohm +- 15%
USB3.1	4.5/4	80 ohm +- 10%

***** You can only choose 1 function to place point per block.**



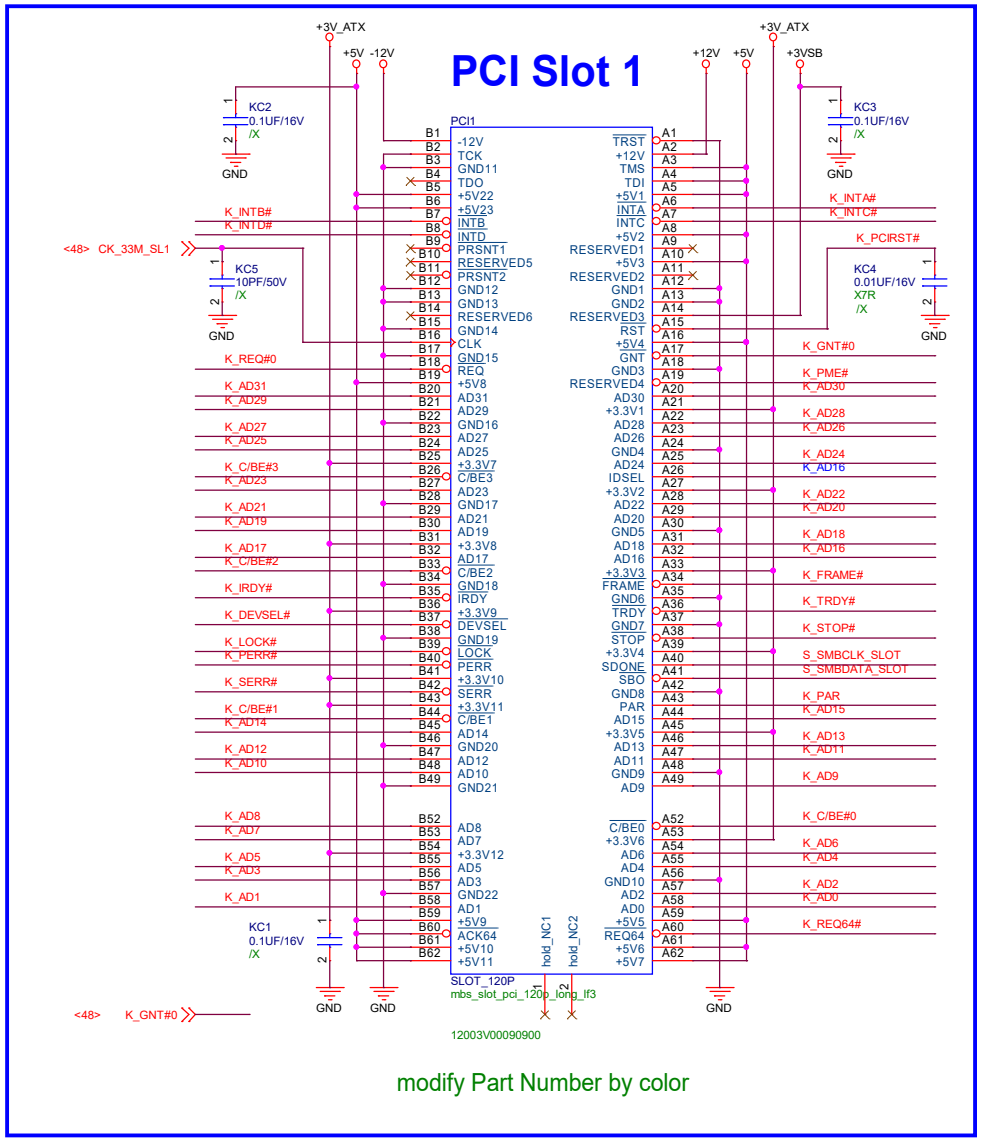
<48,49> K_PERR#
<48,49> K_FRAME#
<48,49> K_IRDY#
<48,49> K_TRDY#
<48,49> K_DEVSEL#
<48,49> K_STOP#
<48,49> K_LOCK#
<48,49> K_SERR#

<48,49> K_INTA#
<48,49> K_INTB#
<48,49> K_INTC#
<48,49> K_INTD#

<48,49> K_PCIRST#
<48,49> K_AD[31..0]
<48,49> K_C/BE#[3..0]
<48,49> K_PAR

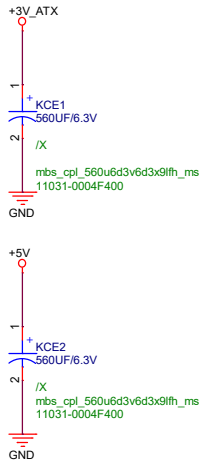
<49> K_REQ64#
<48,49> K_PME#

<25,37,43,44,49> S_SMBCLK_SLOT
<25,37,43,44,49> S_SMBDATA_SLOT

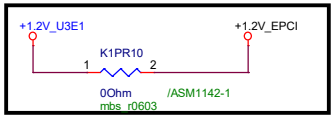


modify Part Number by color

PL CAP



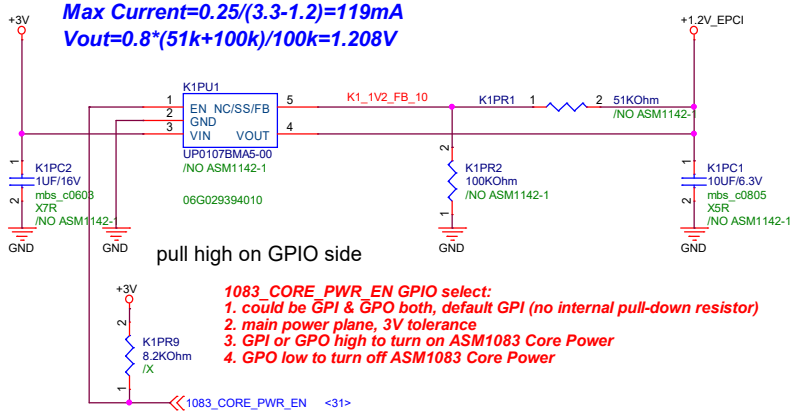
Delete it for EMS



OP1- Core Power

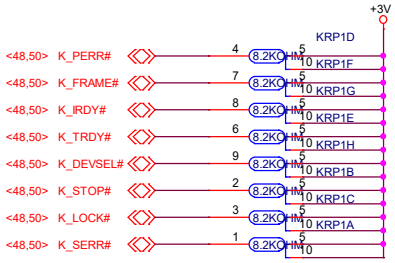
1.2V for ASM108x, 115mA@S0, controll by GPIO

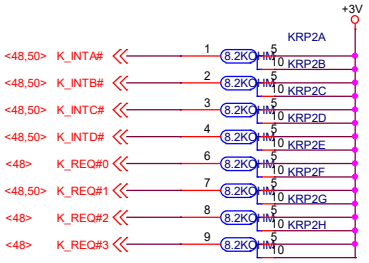
Max Current=0.25/(3.3-1.2)=119mA
Vout=0.8(51k+100k)/100k=1.208V*

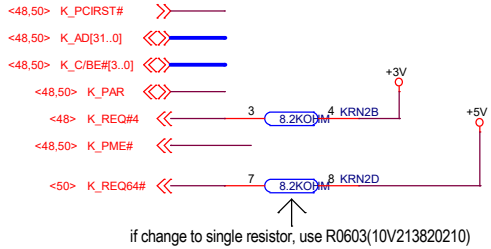


Power Component place near each other!

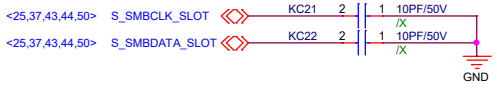
OP1

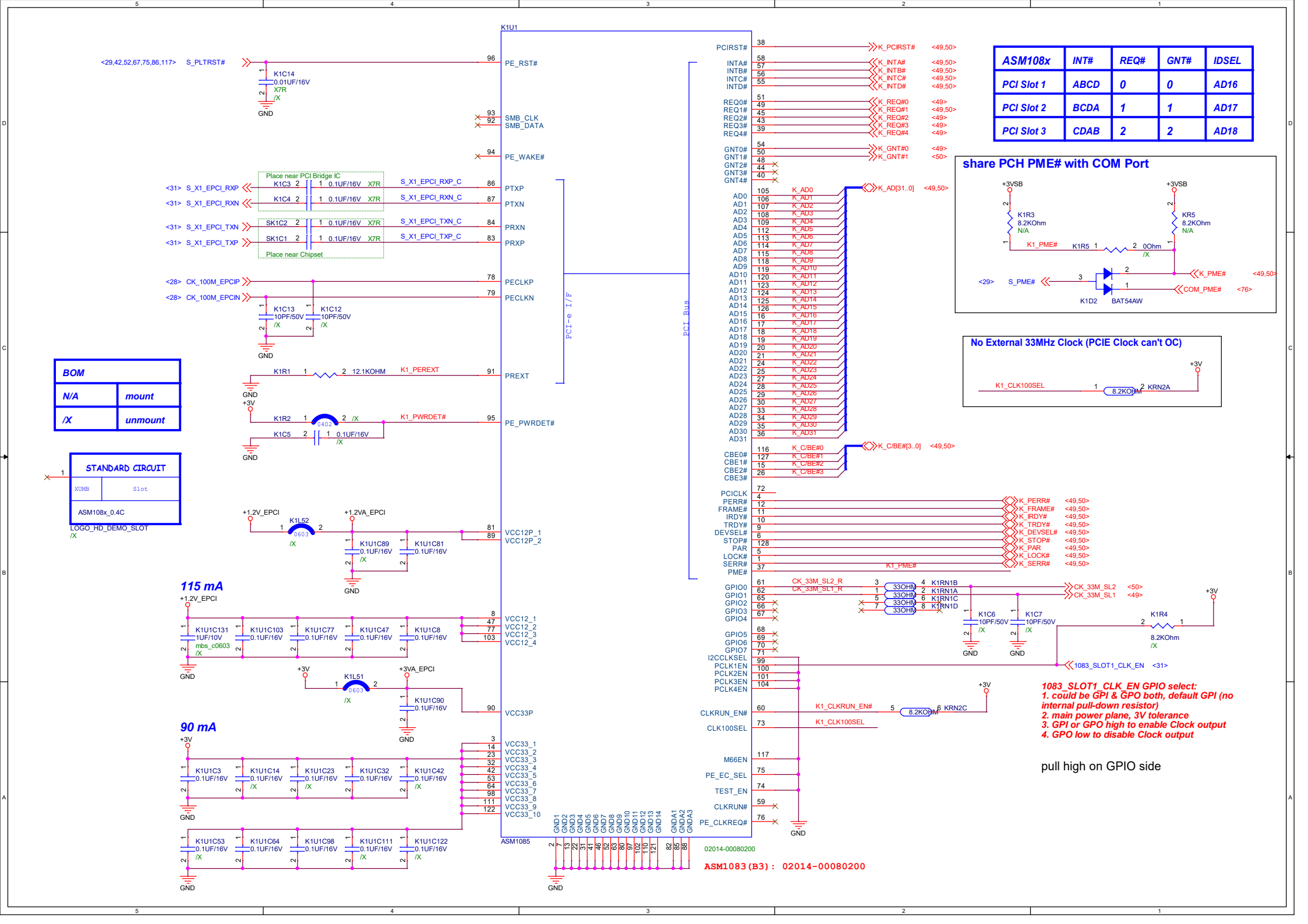




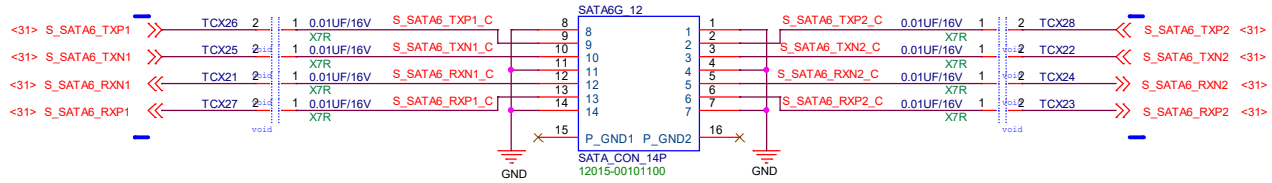


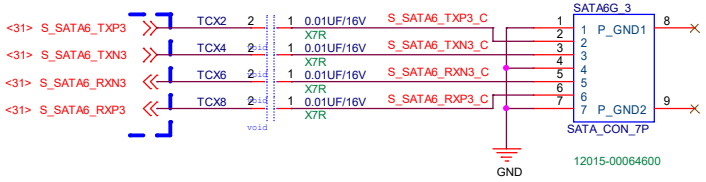
if change to single resistor, use R0603(10V213820210)

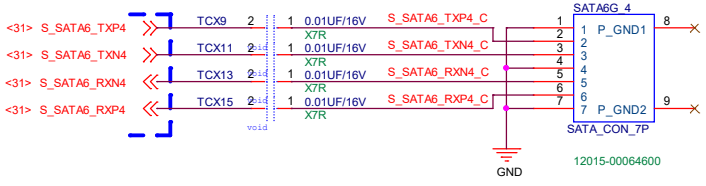




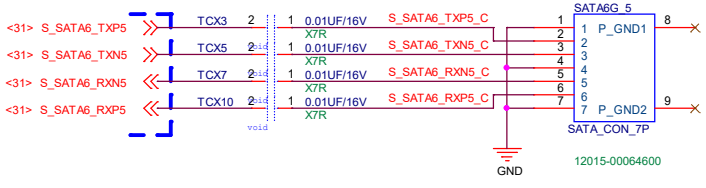
ASM108x	INT#	REQ#	GNT#	IDSEL
PCI Slot 1	ABCD	0	0	AD16
PCI Slot 2	BCDA	1	1	AD17
PCI Slot 3	CDAB	2	2	AD18

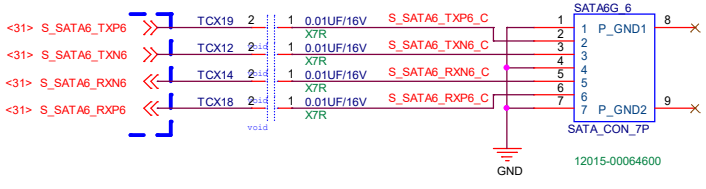


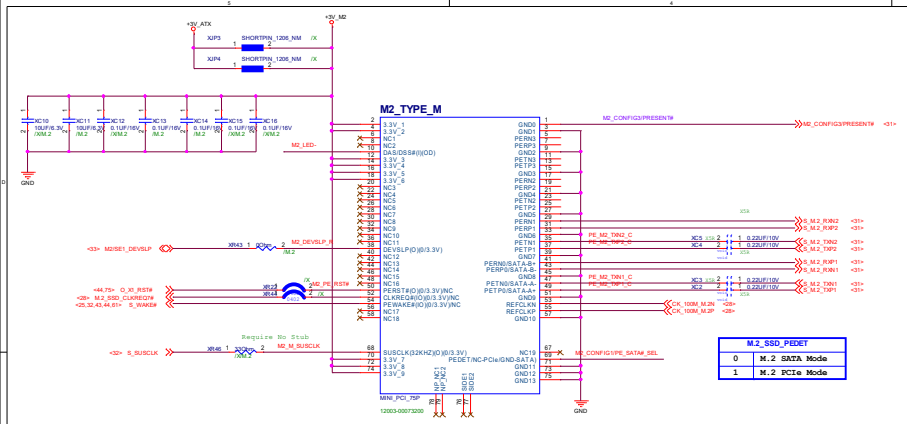


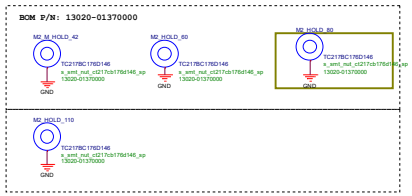


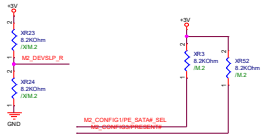
90牟connector

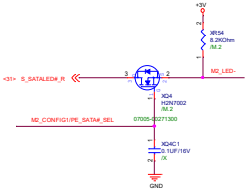


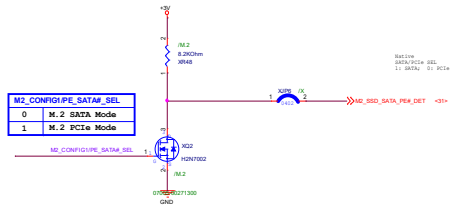








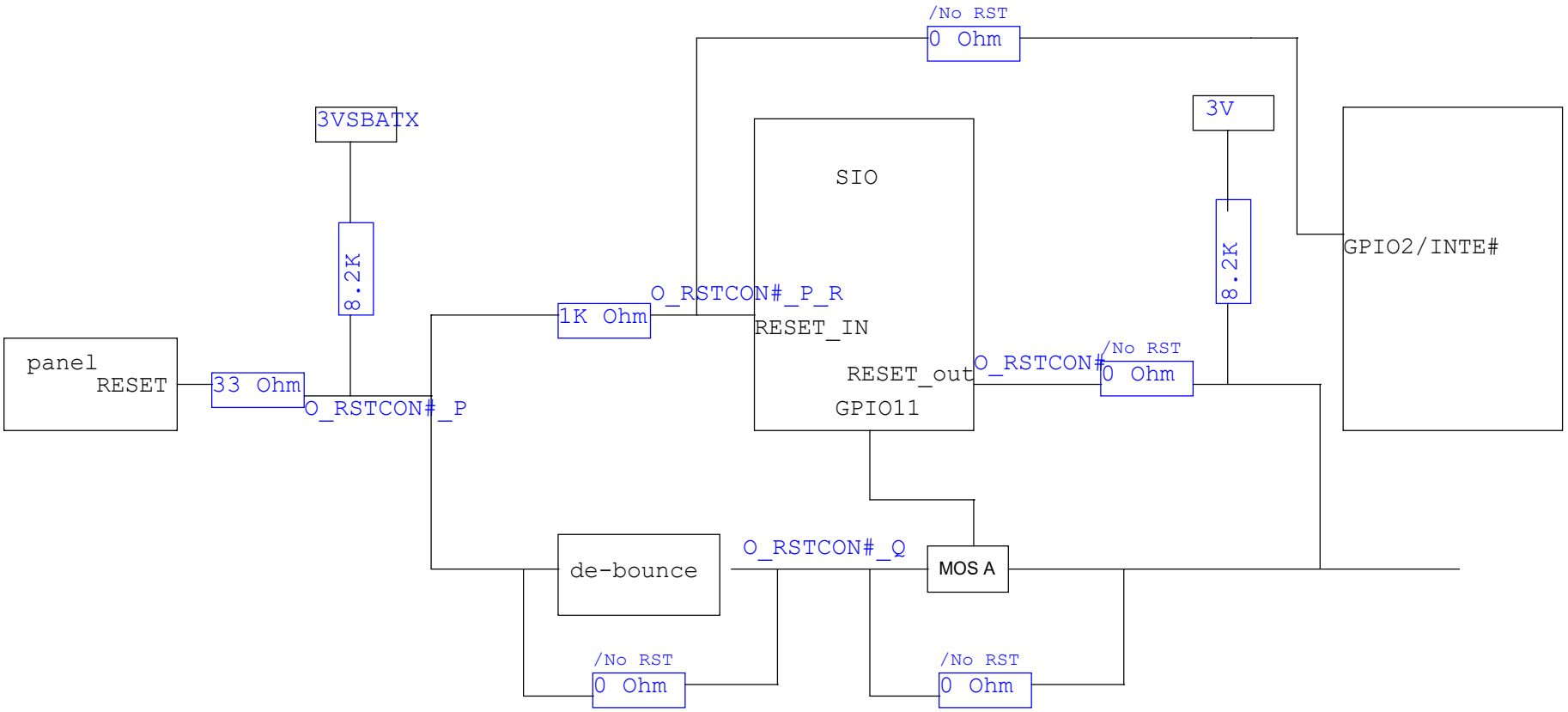


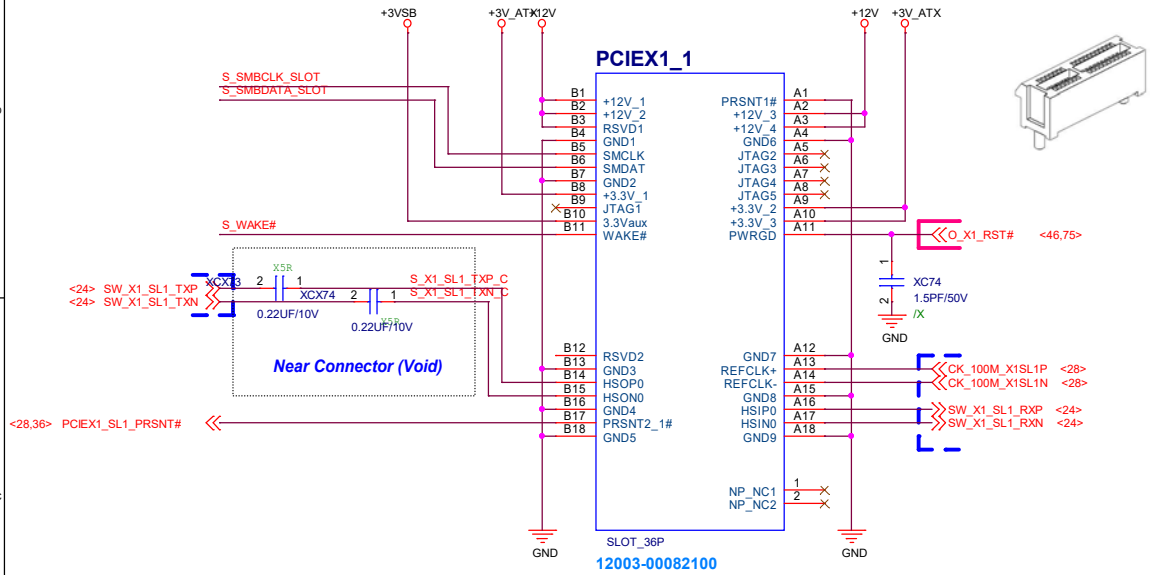


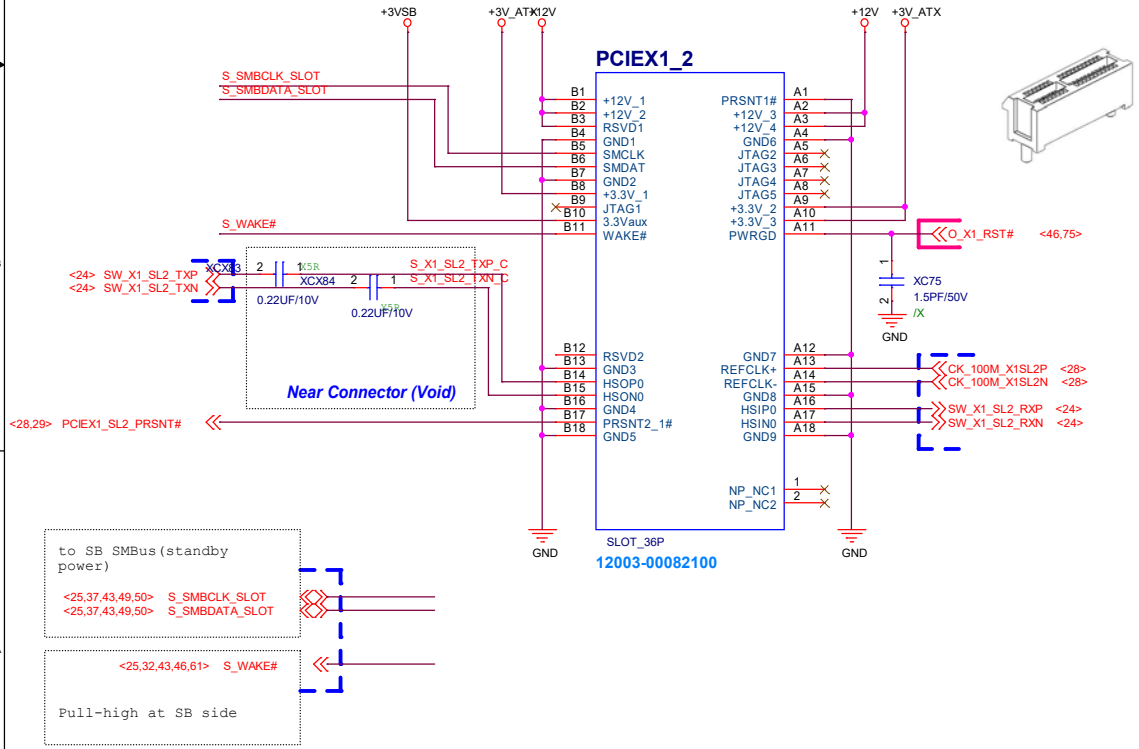
If no SATA EXPRESS SWITCH with M.2 or SATAE switch with M.2 by ME ,Choose this block

If no M.2&6*SATA ,Choose this block

M2_CONFIG1/PE_SATA#_SEL	SATAE1_PDET	M2_CONFIG3/PRESENT#	Result
0	0	0	M.2 change to SATA mode,PCIe #14 change to SATA,PCIe #13 change to PCIE
0	0	1	M.2 change to SATA mode,PCIe #13&14 change to SATA mode
0	1	0	M.2 change to SATA mode,PCIe #13&14 change to PCIE mode
0	1	1	M.2 keep to SATA mode,PCIe #13&14 change to PCIE mode
1	0	0	M.2 change to PCIE mode,PCIe #13&14 change to SATA mode
1	0	1	M.2 keep to PCIE mode,PCIe #13&14 change to SATA mode
1	1	0	M.2 change to PCIE mode,PCIe #13&14 change to PCIE mode
1	1	1	M.2 keep to PCIE mode,PCIe #13&14 change to PCIE mode


/No RST
0 Ohm
3VSBATX
3V
SIO
8.2K
8.2K
GPIO2/INTE#
O_RSTCON#_P_R
1K Ohm
RESET_IN
panel
RESET
33 Ohm
O_RSTCON#_P
RESET_out
GPIO11
O_RSTCON#
/No RST
0 Ohm
de-bounce
O_RSTCON#_Q
MOS A
/No RST
0 Ohm
/No RST
0 Ohm



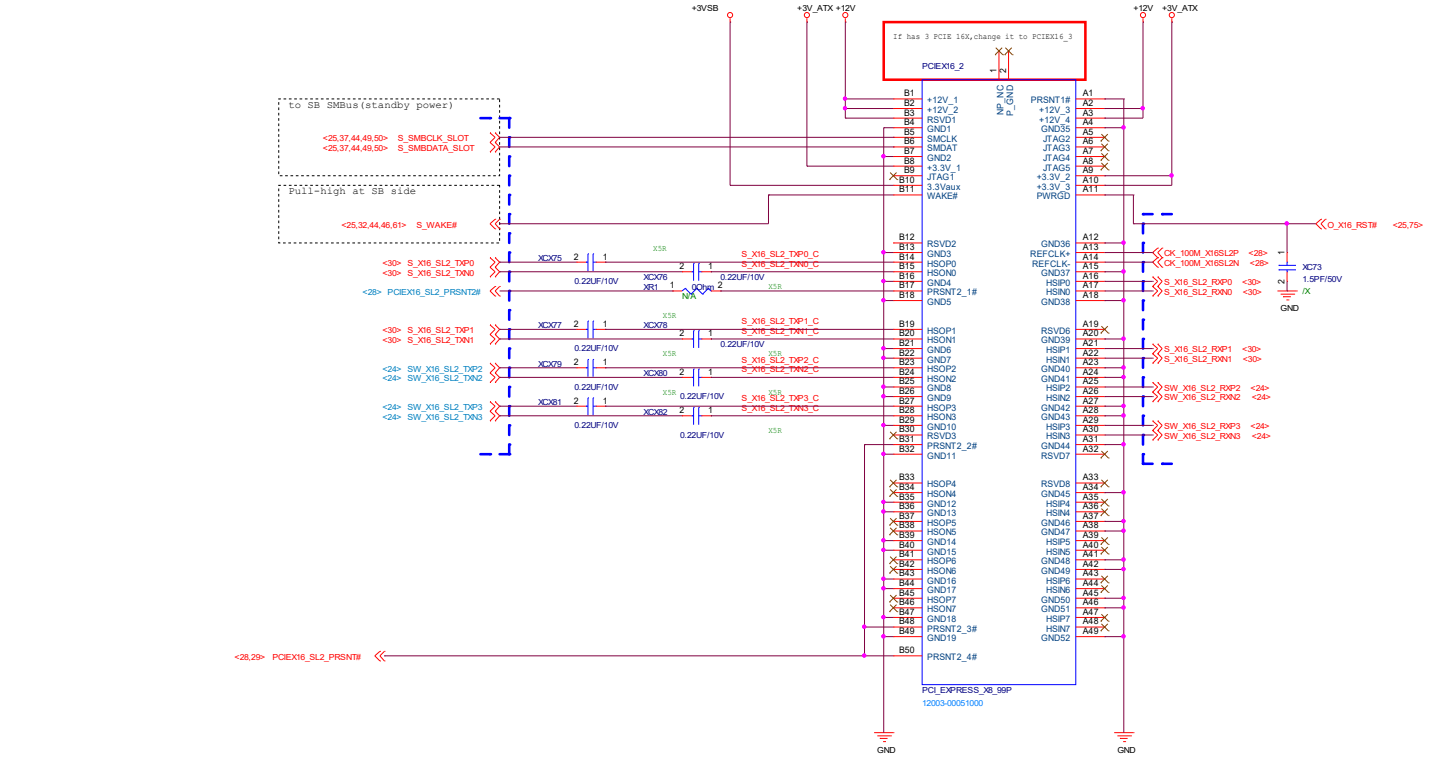


to SB SMBus(standby power)

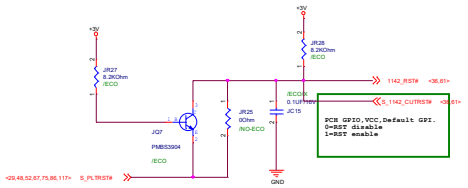
<25,37,43,49,50> S_SMBCLK_SLOT
<25,37,43,49,50> S_SMBDATA_SLOT

<25,32,43,46,61> S_WAKE#

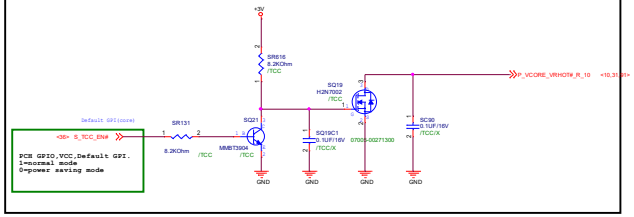
Pull-high at SB side


+3VSB
+3V_ATX
+12V
If has 3 PCIE 16X,change it to PCIEX16_3
PCIEX16_2
to SB SMBus(standby power)
<25,37,44,49,50> S_SMBCLK_SLOT
<25,37,44,49,50> S_SMBDATA_SLOT
Pull-high at SB side
<25,32,44,46,61> S_WAKE#
O_X16_RST# <25,75>
CK_100M_X16SL2P <28>
CK_100M_X16SL2N <28>
XC73
1.5PF/50V
/X
GND
<30> S_X16_SL2_TXP0
<30> S_X16_SL2_TXN0
<28> PCIEX16_SL2_PRSNT2#
<30> S_X16_SL2_TXP1
<30> S_X16_SL2_TXN1
<24> SW_X16_SL2_TXP2
<24> SW_X16_SL2_TXN2
<24> SW_X16_SL2_TXP3
<24> SW_X16_SL2_TXN3
0.22UF/10V
0Ohm
N/A
X5R
S_X16_SL2_RXP0 <30>
S_X16_SL2_RXN0 <30>
S_X16_SL2_RXP1 <30>
S_X16_SL2_RXN1 <30>
SW_X16_SL2_RXP2 <24>
SW_X16_SL2_RXN2 <24>
SW_X16_SL2_RXP3 <24>
SW_X16_SL2_RXN3 <24>
<28,29> PCIEX16_SL2_PRSNT#
PCI_EXPRESS_X8_99P
12003-00051000

1142 PWR CUT



TCC control

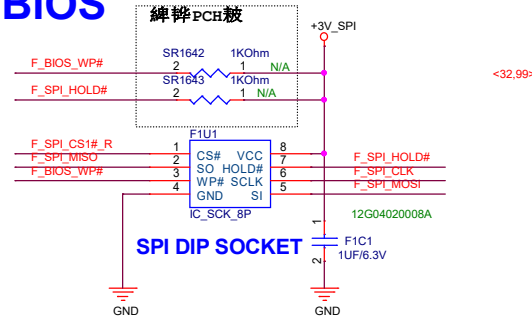


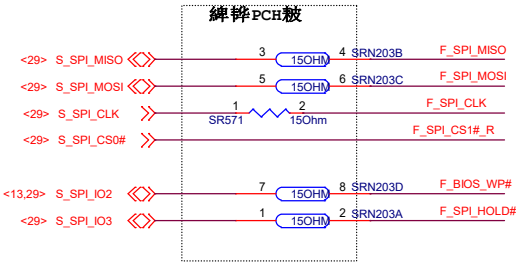
0.3G Beta

Standard Circuit	
BIOS	SPI
REV.	F1_0.3G_Beta

SPI /X/SPI

BIOS

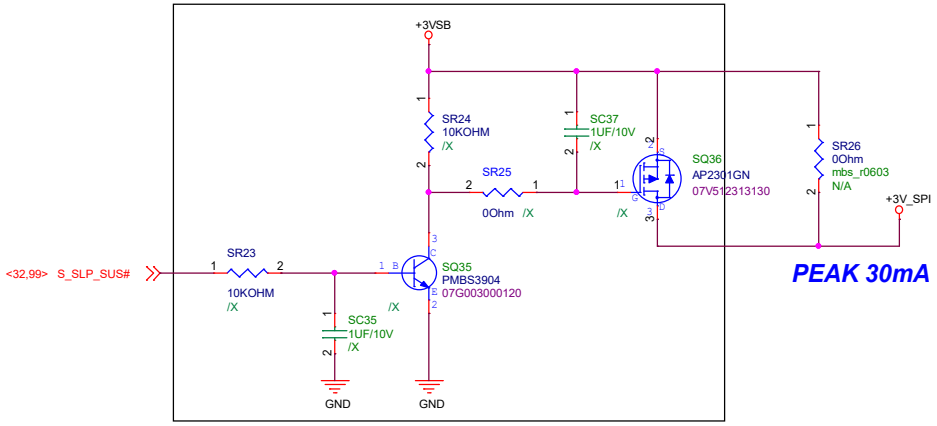




SPI DIP 64M Flash P/N:
05006-00010600

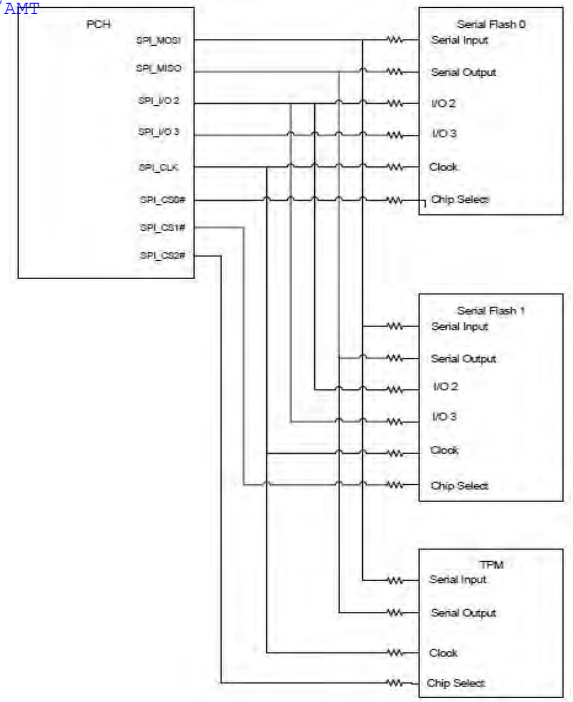
SPI DIP 128M Flash P/N:
05006-00090700

F1U2
SPI ROM
DIP 64M
05006-00090700

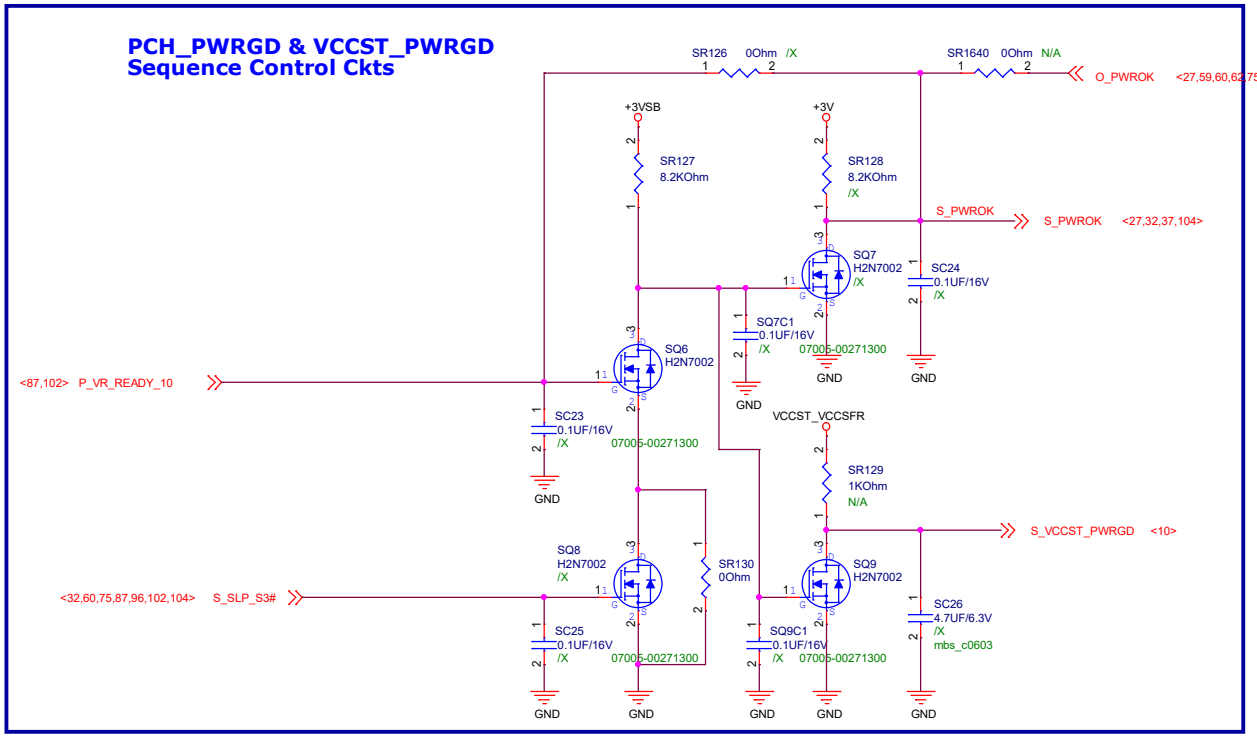


PEAK 30mA

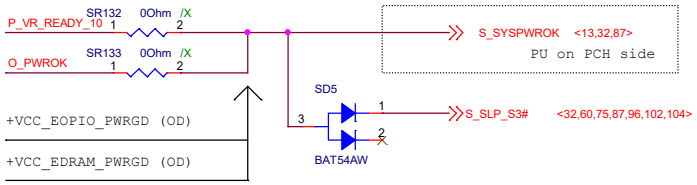
Reserved for support SBA/AMT



PCH_PWRGD & VCCST_PWRGD Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



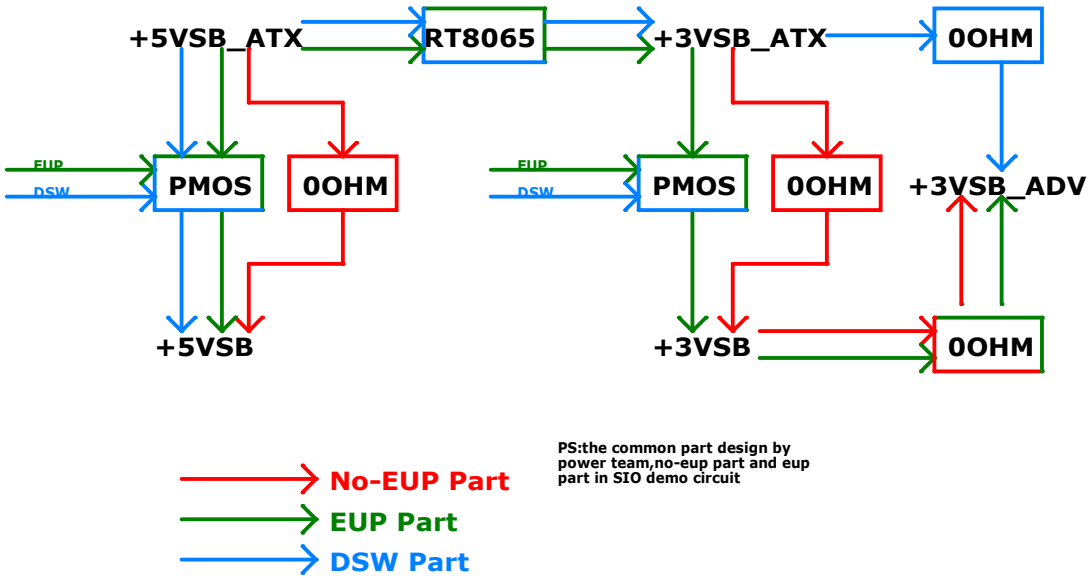
1. PCH will have a minimum of a 1ms delay from PCH_PWROK to assertion of PROCPWRGD.

2. PLTRST# = AND (PCH_PWROK, SYS_PWROK, PROCPWRGD) Refer to PDG Figure 40-1 SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

3. It is recommended that SYS_PWROK be asserted after both PWROK assertion and processor PCH does not monitor

4. PCH_PWROK and SYS_PWROK both needs to be high to exit reset, but either signal can come up first. SYS_PWROK be asserted after both PWROK assertion and processor core VR PWRGD assertion.

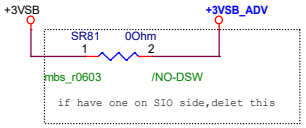
POWER FLOW



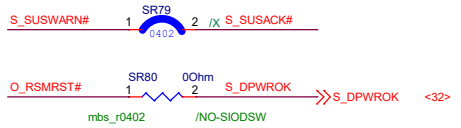
PS:the common part design by power team,no-eup part and eup part in SIO demo circuit

NOT SUPPORT DSW

Power plane

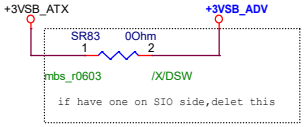


Control link

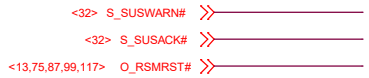


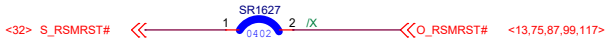
SUPPORT DSW

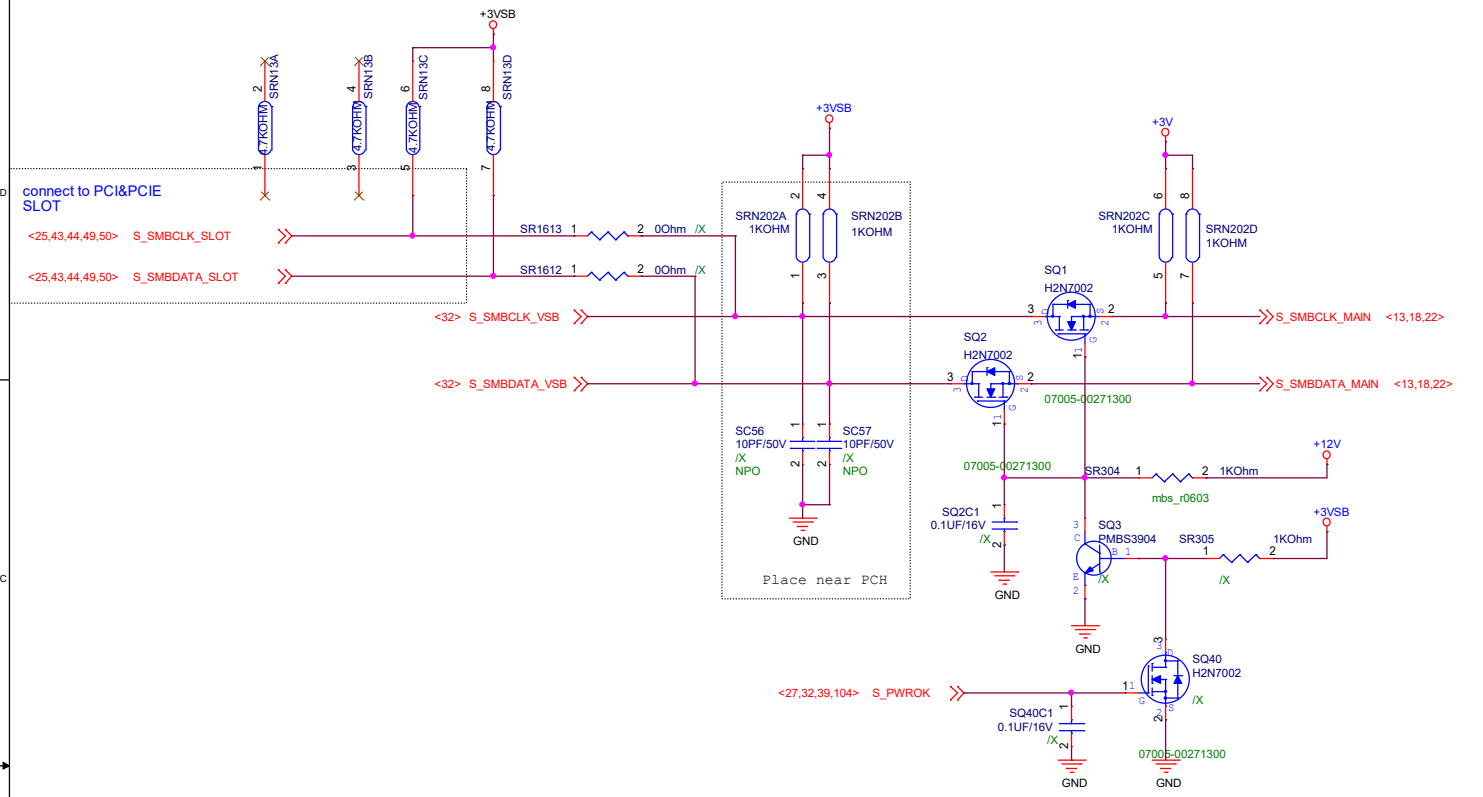
Power plane

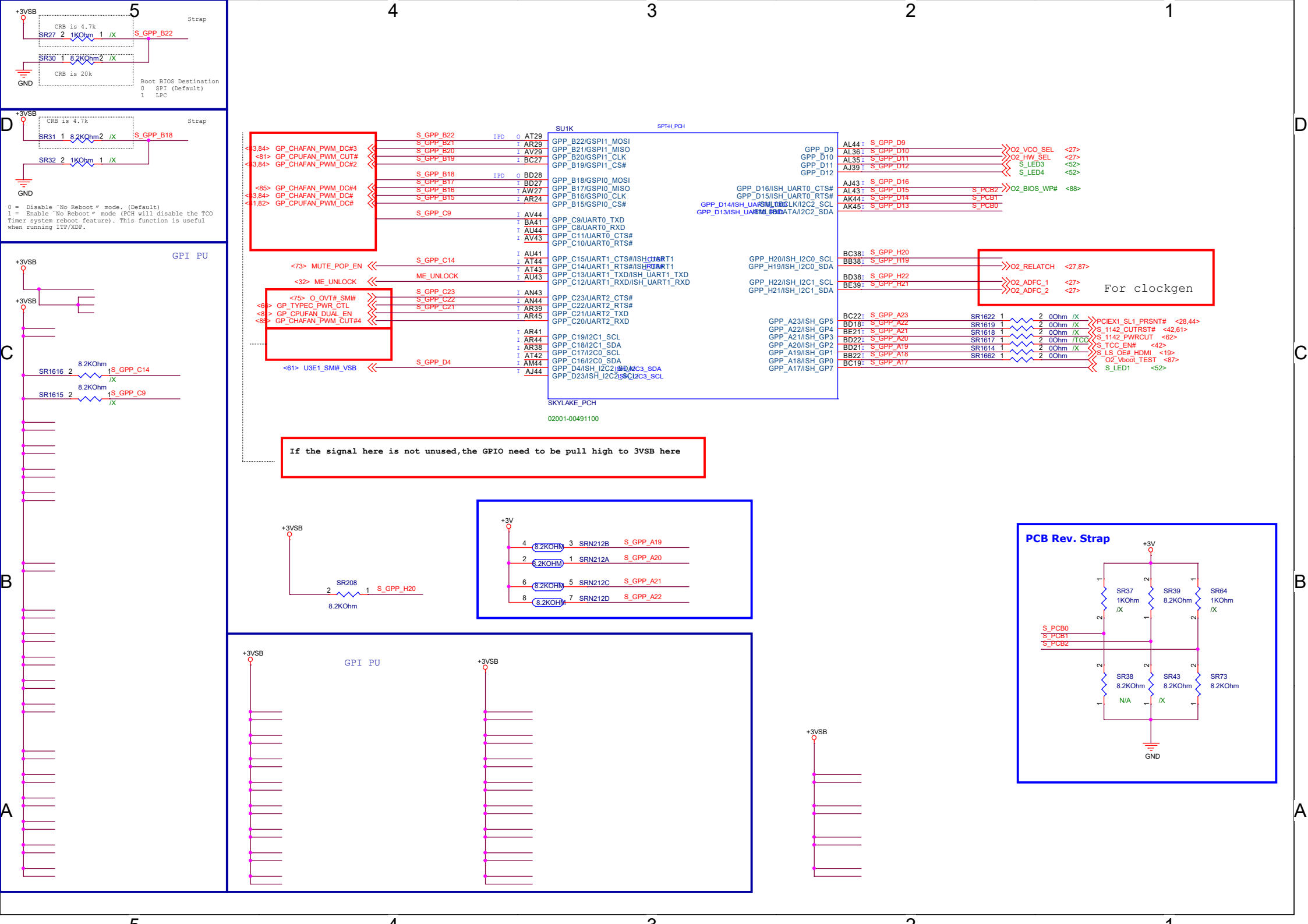


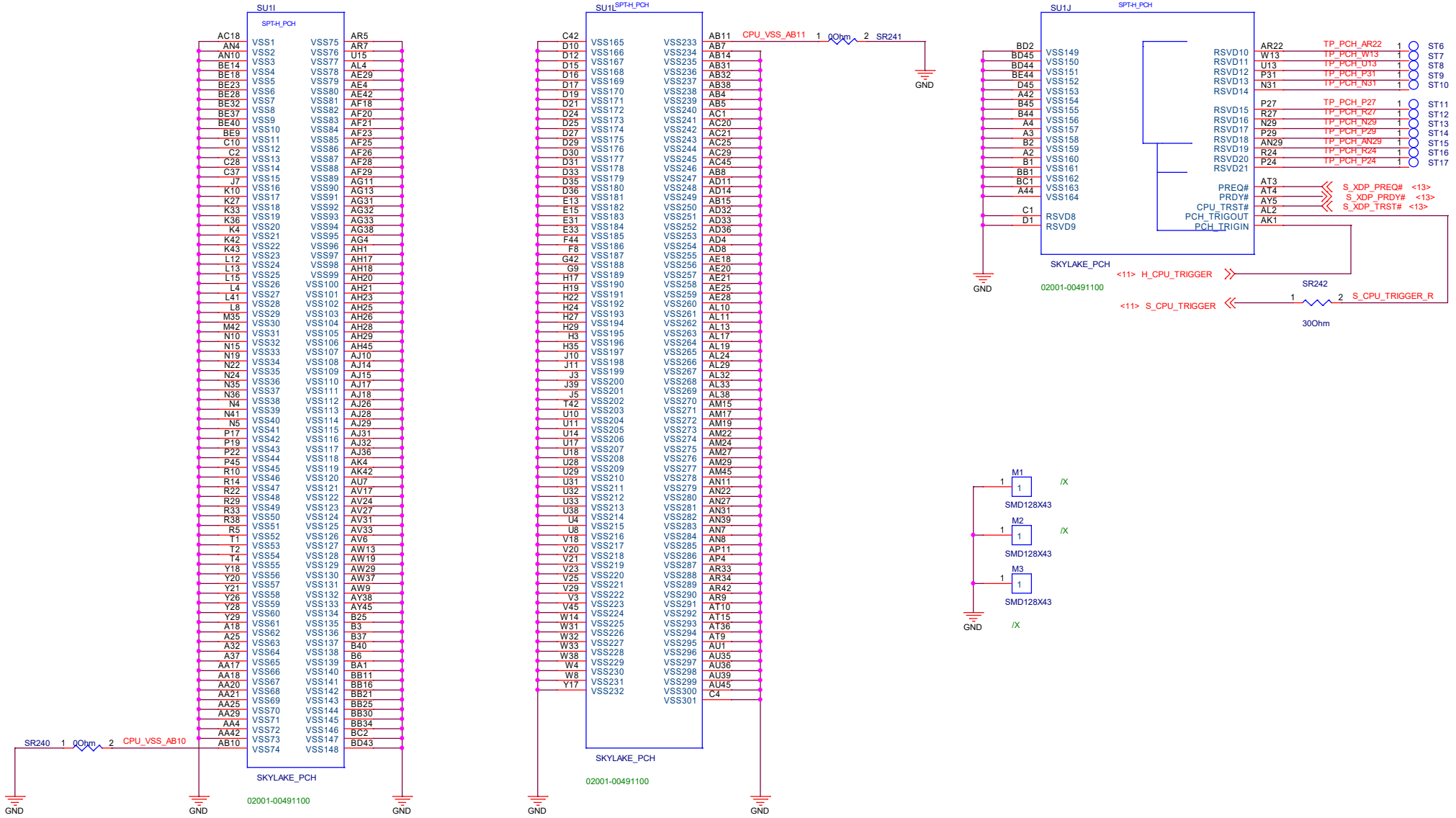
Control link

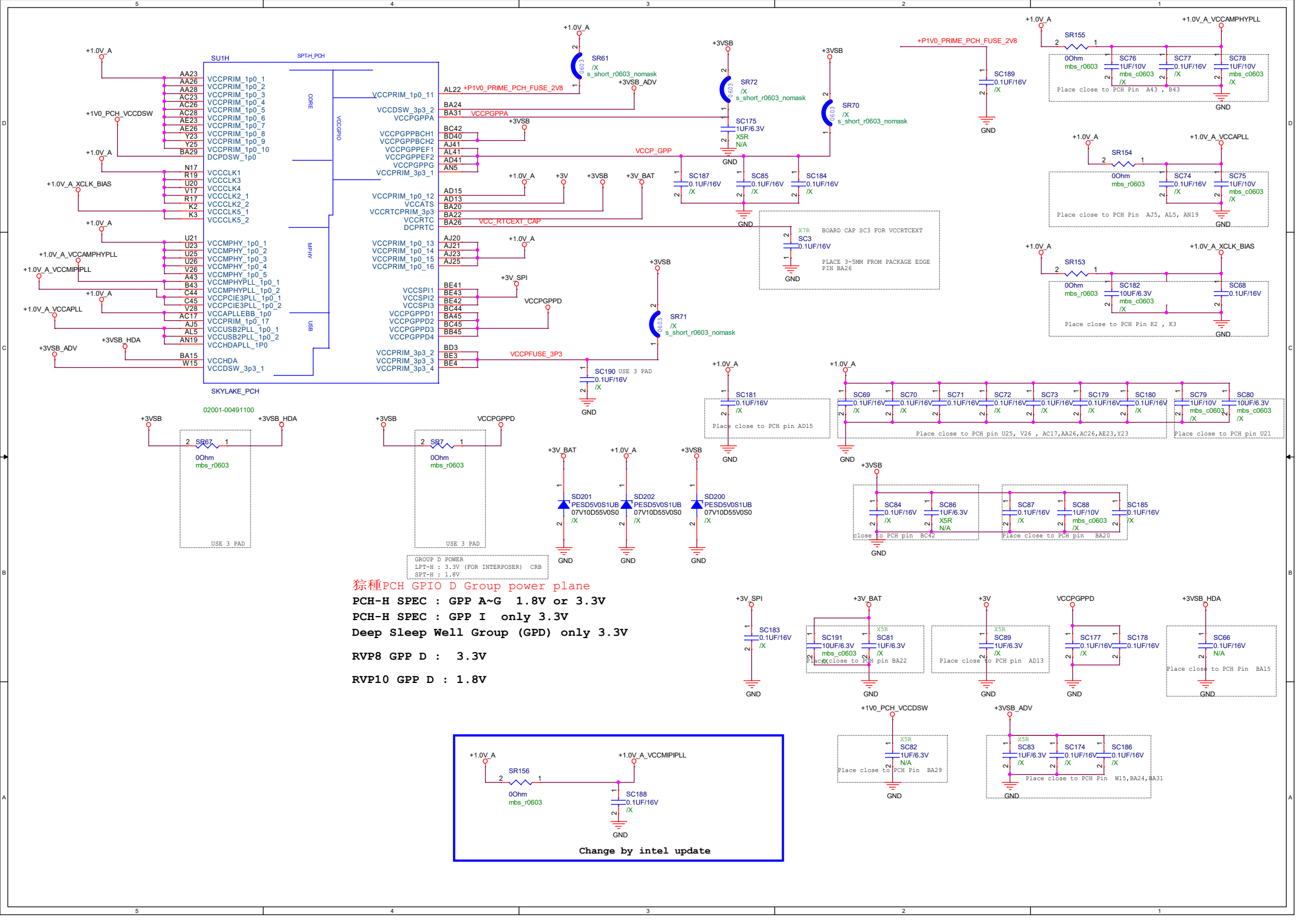


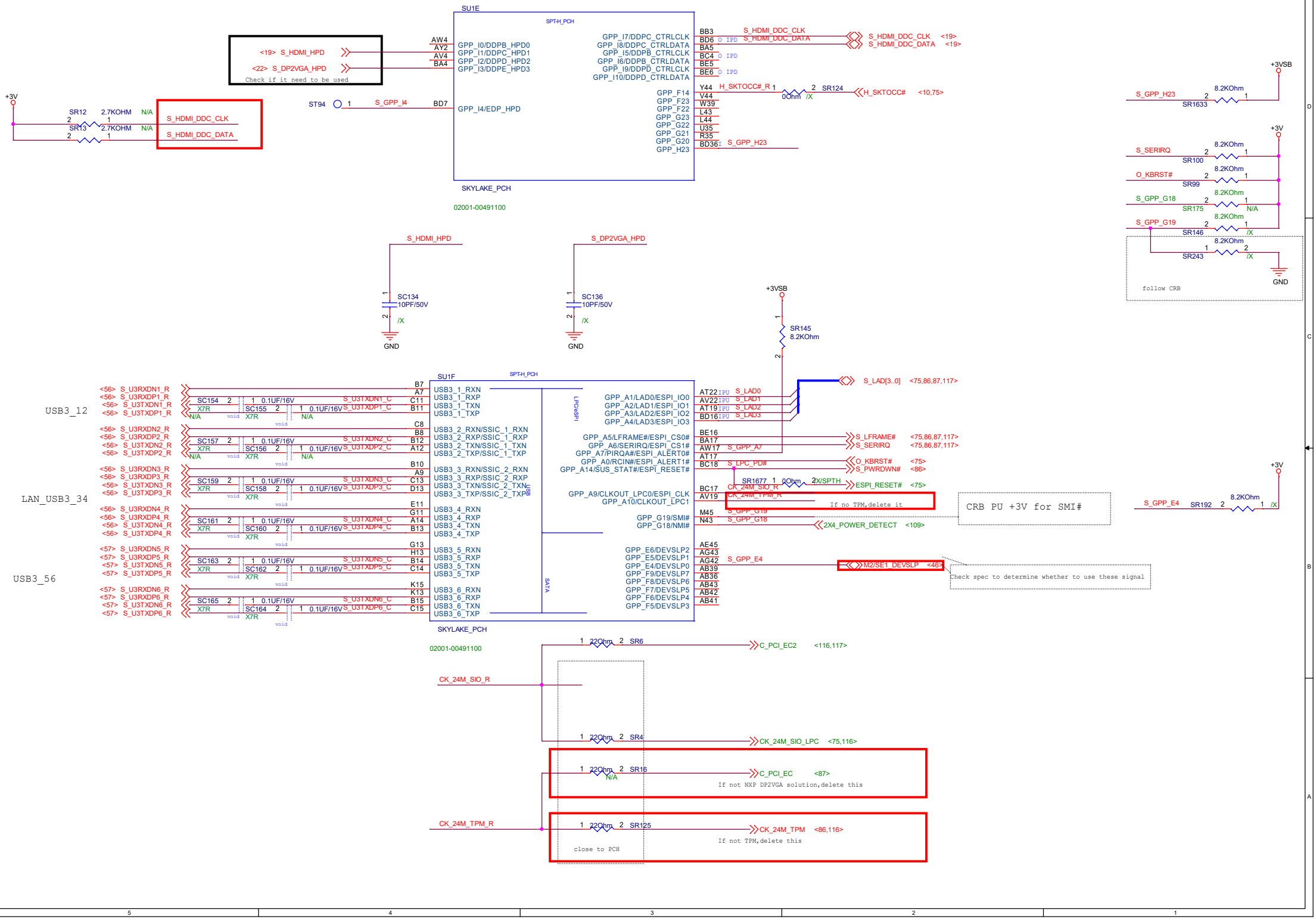


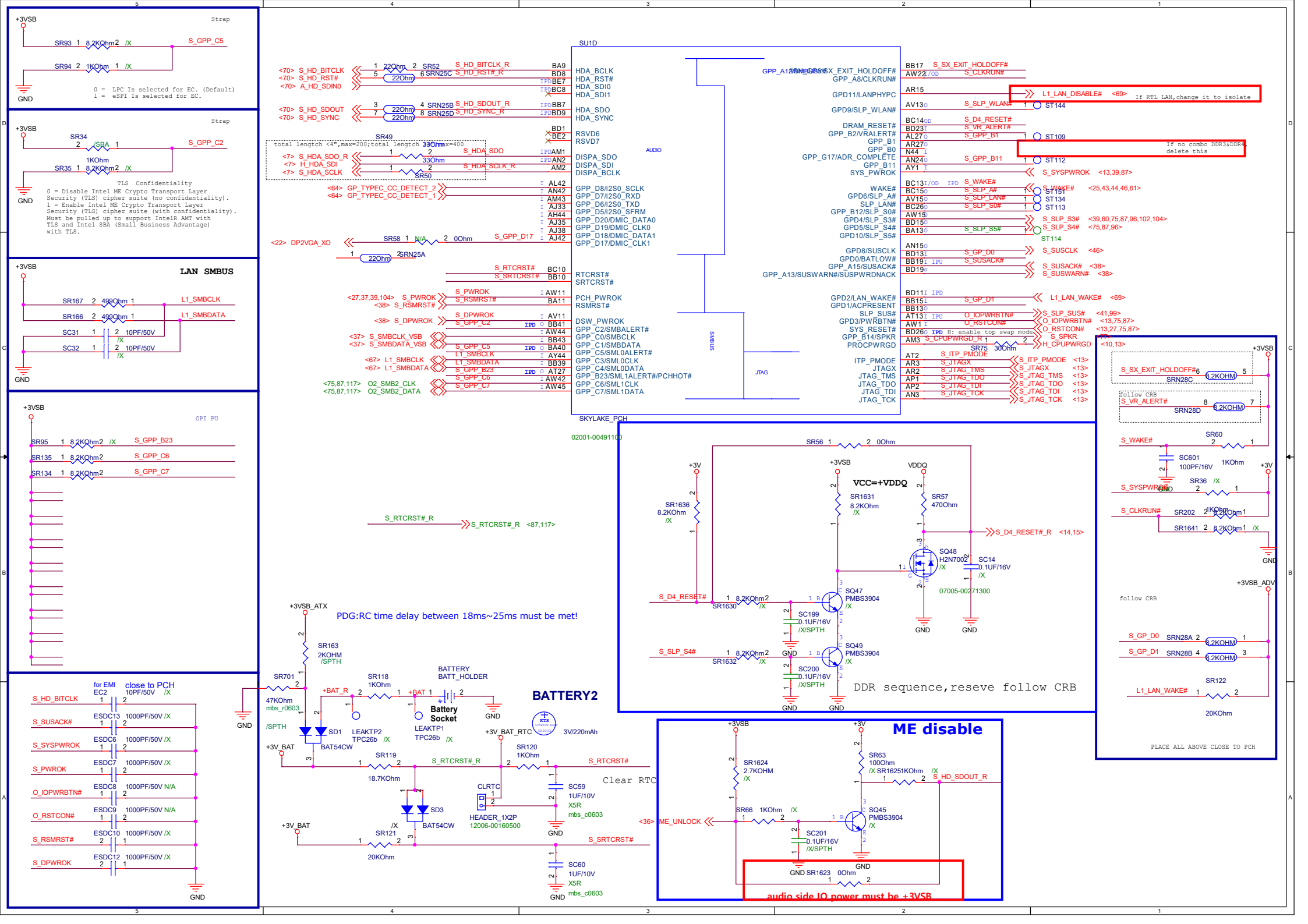

+3VSB
SRN13A
SRN13B
SRN13C
SRN13D
4.7KOHM
connect to PCI&PCIE SLOT
<25,43,44,49,50> S_SMBCLK_SLOT
<25,43,44,49,50> S_SMBDATA_SLOT
SR1613 1 2 0Ohm /X
SR1612 1 2 0Ohm /X
SRN202A 1KOHM
SRN202B 1KOHM
SRN202C 1KOHM
SRN202D 1KOHM
+3V
SQ1 H2NZ002
SQ2 H2NZ002
<32> S_SMBCLK_VSB
<32> S_SMBDATA_VSB
S_SMBCLK_MAIN <13,18,22>
S_SMBDATA_MAIN <13,18,22>
07005-00271300
SC56 10PF/50V /X NPO
SC57 10PF/50V /X NPO
GND
Place near PCH
+12V
SR304 1 2 1KOhm
mbs_r0603
SQ2C1 0.1UF/16V /X
SQ3 PMBS3904
SR305 1KOhm
<27,32,39,104> S_PWROK
SQ40 H2N7002
SQ40C1 0.1UF/16V /X

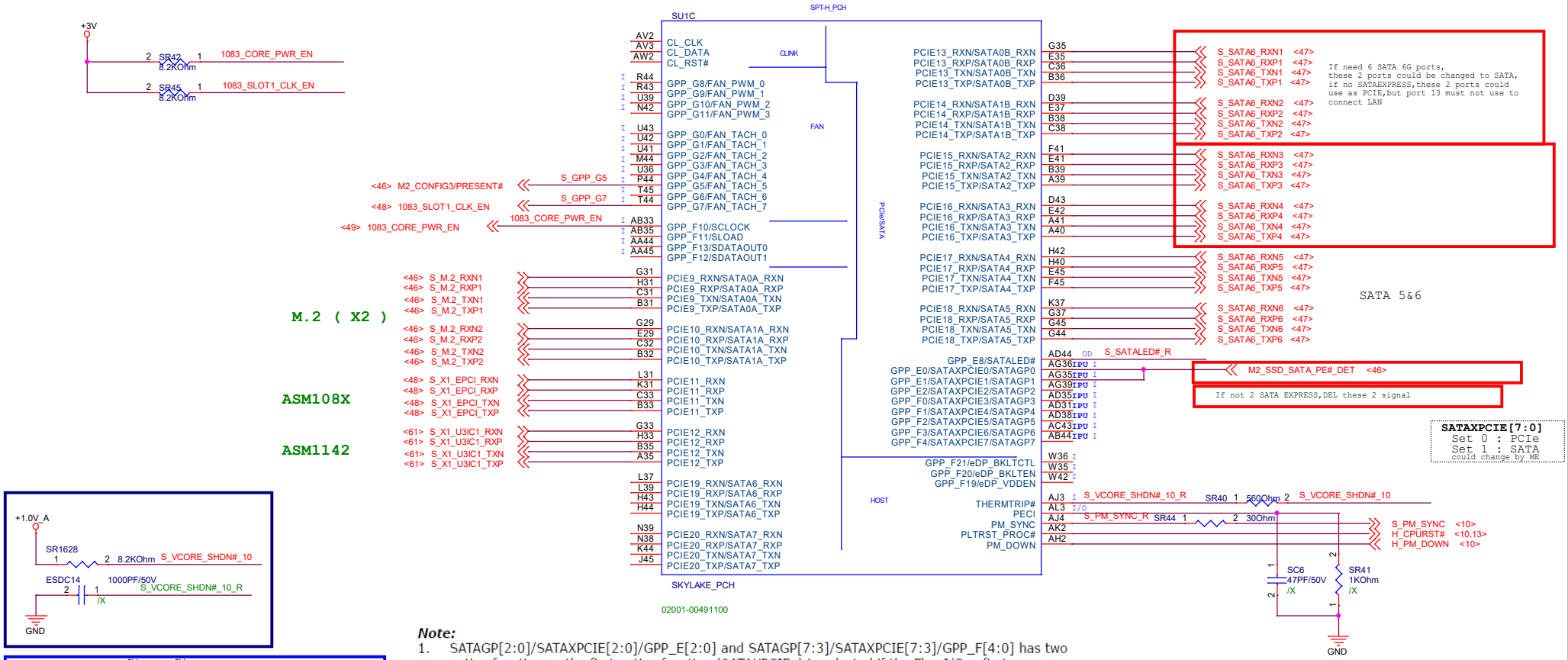

Strap
CRB is 4.7k
SR27 2 1KOhm 1 /X
S_GPP_B22
SR30 1 8.2KOhm 2 /X
CRB is 20k
GND
Boot BIOS Destination
0 SPI (Default)
1 LPC
SR31 1 8.2KOhm 2 /X
S_GPP_B18
SR32 2 1KOhm 1 /X
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
GPI PU
SR1616 2 8.2KOhm 1 S_GPP_C14 /X
SR1615 2 8.2KOhm 1 S_GPP_C9 /X
SU1K
SPT-H_PCH
SKYLAKE_PCH
02001-00491100
GP_CHAFAN_PWM_DC#3
GP_CPUFAN_PWM_CUT#
GP_CHAFAN_PWM_DC#2
GP_CHAFAN_PWM_DC#4
GP_CHAFAN_PWM_DC#
GP_CPUFAN_PWM_DC#
MUTE_POP_EN
ME_UNLOCK
GP_TYPEC_PWR_CTL
GP_CPUFAN_DUAL_EN
GP_CHAFAN_PWM_CUT#4
U3E1_SMI#_VSB
O2_VCO_SEL
O2_HW_SEL
S_LED3
S_LED4
O2_BIOS_WP#
O2_RELATCH
O2_ADFC_1
O2_ADFC_2
For clockgen
PCIEX1_SL1_PRSNT#
S_1142_CUTRST#
S_1142_PWRCUT
S_TCC_EN#
S_LS_OE#_HDMI
O2_Vboot_TEST
S_LED1
If the signal here is not unused,the GPIO need to be pull high to 3VSB here
SR208 2 8.2KOhm 1 S_GPP_H20
SRN212B S_GPP_A19
SRN212A S_GPP_A20
SRN212C S_GPP_A21
SRN212D S_GPP_A22
PCB Rev. Strap
SR37 1KOhm /X
SR39 8.2KOhm
SR64 1KOhm /X
SR38 8.2KOhm N/A
SR43 8.2KOhm /X
SR73 8.2KOhm
S_PCB0
S_PCB1
S_PCB2
GPI PU


SU1I
SPT-H_PCH
SKYLAKE_PCH
02001-00491100
SR240 1 0Ohm 2 CPU_VSS_AB10
GND
SU1L SPT-H_PCH
SKYLAKE_PCH
02001-00491100
CPU_VSS_AB11 1 0Ohm 2 SR241
GND
SU1J SPT-H_PCH
SKYLAKE_PCH
02001-00491100
TP_PCH_AR22
TP_PCH_W13
TP_PCH_U13
TP_PCH_P31
TP_PCH_N31
TP_PCH_P27
TP_PCH_R27
TP_PCH_N29
TP_PCH_P29
TP_PCH_AN29
TP_PCH_R24
TP_PCH_P24
S_XDP_PREQ# <13>
S_XDP_PRDY# <13>
S_XDP_TRST# <13>
<11> H_CPU_TRIGGER
<11> S_CPU_TRIGGER
SR242
1 2 S_CPU_TRIGGER_R
30Ohm
M1
M2
M3
SMD128X43
/X


SU1H
SPT-H_PCH
SKYLAKE_PCH
CORE
VCCGPIO
MPHY
USB
VCCPRIM_1p0_1
VCCPRIM_1p0_2
VCCPRIM_1p0_3
VCCPRIM_1p0_4
VCCPRIM_1p0_5
VCCPRIM_1p0_6
VCCPRIM_1p0_7
VCCPRIM_1p0_8
VCCPRIM_1p0_9
VCCPRIM_1p0_10
DCPDSW_1p0
VCCCLK1
VCCCLK3
VCCCLK4
VCCCLK2_1
VCCCLK2_2
VCCCLK5_1
VCCCLK5_2
VCCMPHY_1p0_1
VCCMPHY_1p0_2
VCCMPHY_1p0_3
VCCMPHY_1p0_4
VCCMPHY_1p0_5
VCCMPHYPLL_1p0_1
VCCMPHYPLL_1p0_2
VCCPCIE3PLL_1p0_1
VCCPCIE3PLL_1p0_2
VCCAPLLEBB_1p0
VCCPRIM_1p0_17
VCCUSB2PLL_1p0_1
VCCUSB2PLL_1p0_2
VCCHDAPLL_1P0
VCCHDA
VCCDSW_3p3_1
VCCPRIM_1p0_11
VCCDSW_3p3_2
VCCPGPPA
VCCPGPPBCH1
VCCPGPPBCH2
VCCPGPPEF1
VCCPGPPEF2
VCCPGPPG
VCCPRIM_3p3_1
VCCPRIM_1p0_12
VCCATS
VCCRTCPRIM_3p3
VCCRTC
DCPRTC
VCCPRIM_1p0_13
VCCPRIM_1p0_14
VCCPRIM_1p0_15
VCCPRIM_1p0_16
VCCSPI1
VCCSPI2
VCCSPI3
VCCPGPPD1
VCCPGPPD2
VCCPGPPD3
VCCPGPPD4
VCCPRIM_3p3_2
VCCPRIM_3p3_3
VCCPRIM_3p3_4
+1.0V_A
+1V0_PCH_VCCDSW
+1.0V_A_XCLK_BIAS
+1.0V_A_VCCAMPHYPLL
+1.0V_A_VCCMIPIPLL
+1.0V_A_VCCAPLL
+3VSB_ADV
+3VSB_HDA
+3VSB
+3V_SPI
+3V_BAT
+3V
+P1V0_PRIME_PCH_FUSE_2V8
VCCPGPPA
VCCP_GPP
VCC_RTCEXT_CAP
VCCPGPPD
VCCPFUSE_3P3
SR61 /X s_short_r0603_nomask
SR72 /X s_short_r0603_nomask
SR70 /X s_short_r0603_nomask
SR71 /X s_short_r0603_nomask
SC175 1UF/6.3V X5R N/A
SC187 0.1UF/16V /X
SC85 0.1UF/16V /X
SC184 0.1UF/16V /X
X7R BOARD CAP SC3 FOR VCCRTCEXT
SC3 0.1UF/16V
PLACE 3-5MM FROM PACKAGE EDGE PIN BA26
SC190 USE 3 PAD 0.1UF/16V /X
SC189 0.1UF/16V /X
SR155 0Ohm mbs_r0603
SC76 1UF/10V mbs_c0603 /X
SC77 0.1UF/16V /X
SC78 1UF/10V mbs_c0603 /X
Place close to PCH Pin A43 , B43
SR154 0Ohm mbs_r0603
SC74 0.1UF/16V /X
SC75 1UF/10V mbs_c0603 /X
Place close to PCH Pin AJ5, AL5, AN19
SR153 0Ohm mbs_r0603
SC182 10UF/6.3V mbs_c0603 /X
SC68 0.1UF/16V
Place close to PCH Pin K2 , K3
SC181 0.1UF/16V /X
Place close to PCH pin AD15
SC69 SC70 SC71 SC72 SC73 SC179 SC180 0.1UF/16V /X
Place close to PCH pin U25, V26 , AC17,AA26,AC26,AE23,Y23
SC79 1UF/10V mbs_c0603 /X
SC80 10UF/6.3V mbs_c0603 /X
Place close to PCH pin U21
02001-00491100
SR67 0Ohm mbs_r0603
USE 3 PAD
SR7 0Ohm mbs_r0603
USE 3 PAD
SD201 PESD5V0S1UB 07V10D55V0S0 /X
SD202 PESD5V0S1UB 07V10D55V0S0 /X
SD200 PESD5V0S1UB 07V10D55V0S0 /X
SC84 0.1UF/16V /X
SC86 1UF/6.3V X5R N/A
Close to PCH pin BC42
SC87 0.1UF/16V /X
SC88 1UF/10V mbs_c0603 /X
SC185 0.1UF/16V /X
Place close to PCH pin BA20
GROUP D POWER
LPT-H : 3.3V (FOR INTERPOSER) CRB
SPT-H : 1.8V
猓種PCH GPIO D Group power plane
PCH-H SPEC : GPP A~G 1.8V or 3.3V
PCH-H SPEC : GPP I only 3.3V
Deep Sleep Well Group (GPD) only 3.3V
RVP8 GPP D : 3.3V
RVP10 GPP D : 1.8V
SC183 0.1UF/16V /X
SC191 10UF/6.3V mbs_c0603 /X
SC81 1UF/6.3V /X
Place close to PCH pin BA22
SC89 1UF/6.3V /X
Place close to PCH pin AD13
SC177 0.1UF/16V /X
SC178 0.1UF/16V
SC66 0.1UF/16V N/A
Place close to PCH Pin BA15
SC82 1UF/6.3V N/A
Place close to PCH Pin BA29
SC83 1UF/6.3V /X
SC174 0.1UF/16V /X
SC186 0.1UF/16V /X
Place close to PCH Pin W15,BA24,BA31
SR156 0Ohm mbs_r0603
SC188 0.1UF/16V /X
Change by intel update
GND

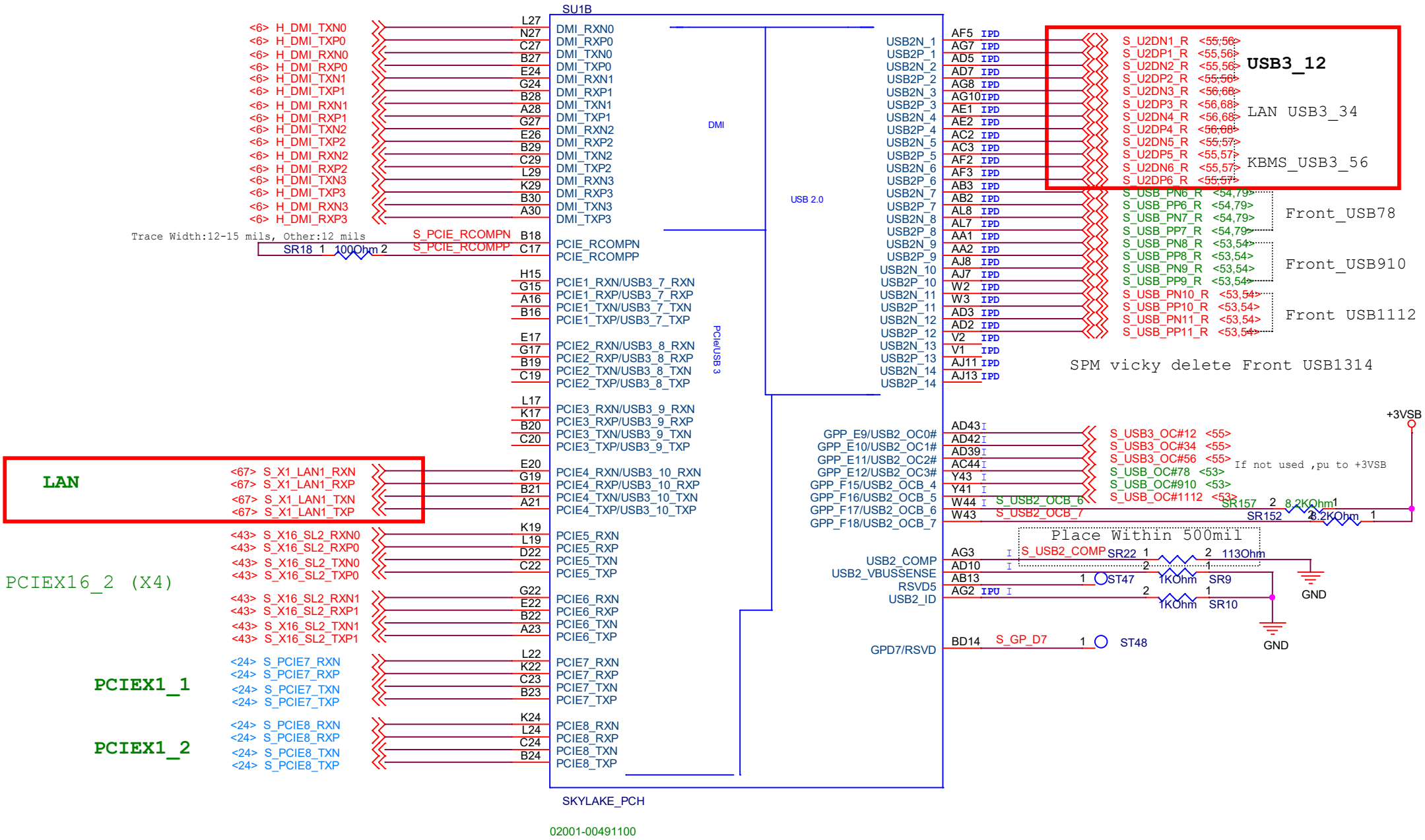

SU1E
SPT-H_PCH
SKYLAKE_PCH
02001-00491100
<19> S_HDMI_HPD
<22> S_DP2VGA_HPD
Check if it need to be used
GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_I4/EDP_HPD
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
S_HDMI_DDC_CLK
S_HDMI_DDC_DATA
H_SKTOCC#
S_GPP_H23
ST94
SR12 2.7KOHM N/A
SR13 2.7KOHM N/A
SR124 0Ohm /X
SR1633 8.2KOhm
SR100 8.2KOhm
SR99 8.2KOhm
SR175 8.2KOhm N/A
SR146 8.2KOhm /X
SR243 8.2KOhm /X
follow CRB
+3V
+3VSB
GND
SC134 10PF/50V /X
SC136 10PF/50V /X
SR145 8.2KOhm
SU1F
USB3_12
LAN_USB3_34
USB3_56
USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP
USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP
USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP
USB3_4_RXN
USB3_4_RXP
USB3_4_TXN
USB3_4_TXP
USB3_5_RXN
USB3_5_RXP
USB3_5_TXN
USB3_5_TXP
USB3_6_RXN
USB3_6_RXP
USB3_6_TXN
USB3_6_TXP
LPC/eSPI
SATA
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS0#
GPP_A6/SERIRQ/ESPI_CS1#
GPP_A7/PIRQA#/ESPI_ALERT0#
GPP_A0/RCIN#/ESPI_ALERT1#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_G19/SMI#
GPP_G18/NMI#
GPP_E6/DEVSLP2
GPP_E5/DEVSLP1
GPP_E4/DEVSLP0
GPP_F9/DEVSLP7
GPP_F8/DEVSLP6
GPP_F7/DEVSLP5
GPP_F6/DEVSLP4
GPP_F5/DEVSLP3
S_LAD[3..0]
S_LFRAME#
S_SERIRQ
O_KBRST#
S_PWRDWN#
S_LPC_PD#
ESPI_RESET#
CK_24M_SIO_R
CK_24M_TPM_R
If no TPM,delete it
2X4_POWER_DETECT
M2/SE1_DEVSLP
Check spec to determine whether to use these signal
CRB PU +3V for SMI#
SR1677 0Ohm 2X/SPTH
SR192 8.2KOhm /X
SR6 22Ohm
SR4 22Ohm
SR16 22Ohm N/A
SR125 22Ohm
C_PCI_EC2
CK_24M_SIO_LPC
C_PCI_EC
CK_24M_TPM
If not NXP DP2VGA solution,delete this
If not TPM,delete this
close to PCH

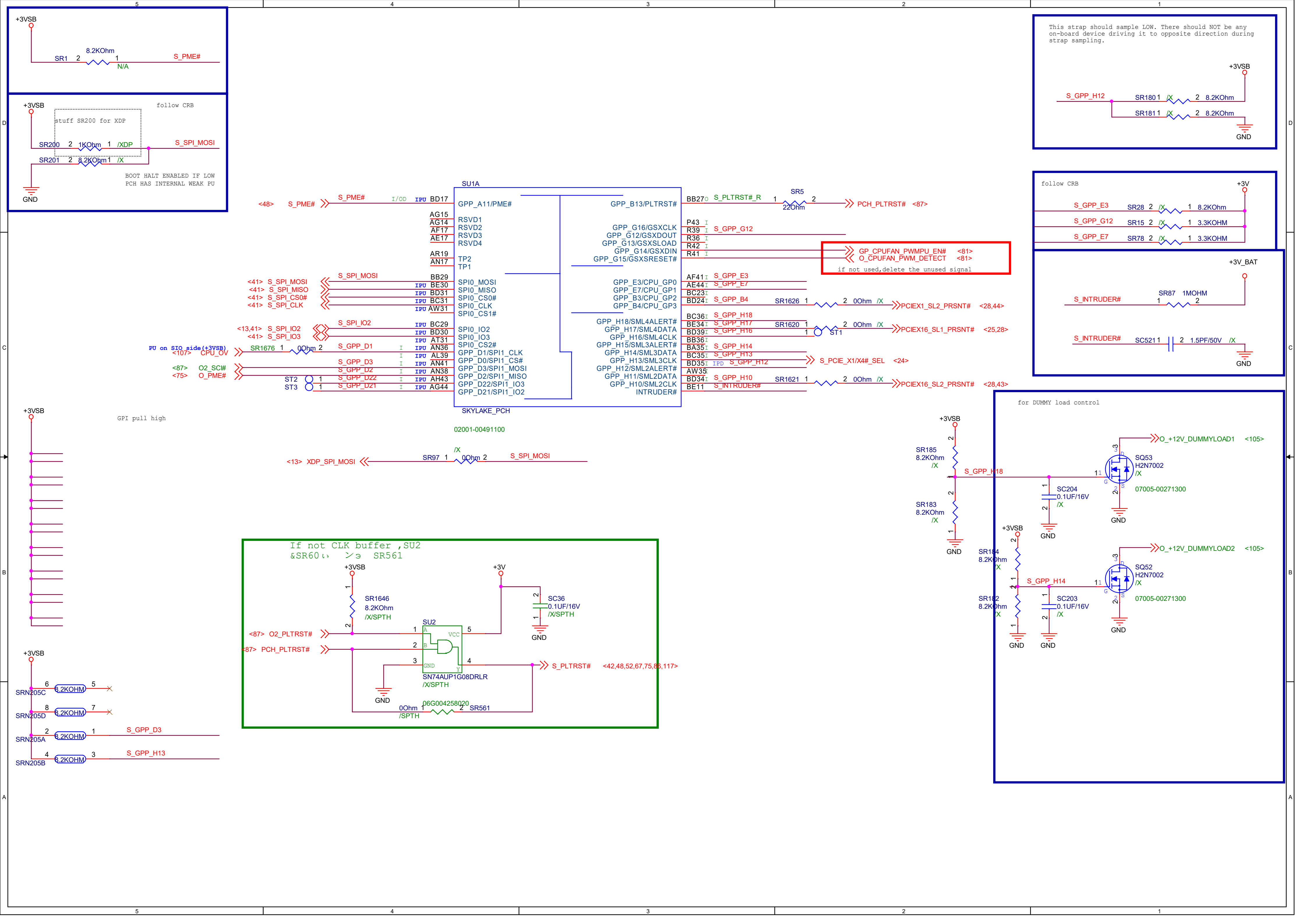

Strap
+3VSB
SR93 1 8.2KOhm 2 /X
S_GPP_C5
SR94 2 1KOhm 1 /X
GND
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
Strap
SR34
/SBA
S_GPP_C2
1KOhm
SR35 1 8.2KOhm 2 /X
TLS Confidentiality
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
Must be pulled up to support IntelR AMT with TLS and Intel SBA (Small Business Advantage) with TLS.
LAN SMBUS
SR167 2 499Ohm 1
L1_SMBCLK
SR166 2 499Ohm 1
L1_SMBDATA
SC31 1 2 10PF/50V /X
SC32 1 2 10PF/50V /X
GPI PU
S_GPP_B23
S_GPP_C6
S_GPP_C7
for EMI
close to PCH
ESDC13 1000PF/50V /X
ESDC6 1000PF/50V /X
ESDC7 1000PF/50V /X
ESDC8 1000PF/50V N/A
ESDC9 1000PF/50V N/A
ESDC10 1000PF/50V /X
ESDC12 1000PF/50V /X
S_HD_BITCLK
S_SUSACK#
S_SYSPWROK
S_PWROK
O_IOPWRBTN#
O_RSTCON#
S_RSMRST#
S_DPWROK
SU1D
SKYLAKE_PCH
02001-00491100
HDA_BCLK
HDA_RST#
HDA_SDI0
HDA_SDI1
HDA_SDO
HDA_SYNC
RSVD6
RSVD7
DISPA_SDO
DISPA_SDI
DISPA_BCLK
GPP_D8/I2S0_SCLK
GPP_D7/I2S0_RXD
GPP_D6/I2S0_TXD
GPP_D5/I2S0_SFRM
GPP_D20/DMIC_DATA0
GPP_D19/DMIC_CLK0
GPP_D18/DMIC_DATA1
GPP_D17/DMIC_CLK1
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_A12/SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD9/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1
GPP_B0
GPP_G17/ADR_COMPLETE
GPP_B11
SYS_PWROK
WAKE#
GPD6/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD8/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
PROCPWRGD
ITP_PMODE
JTAGX
JTAG_TMS
JTAG_TDO
JTAG_TDI
JTAG_TCK
AUDIO
SMBUS
JTAG
L1_LAN_DISABLE# <69>
If RTL LAN,change it to isolate
ST144
ST109
If no combo DDR3&DDR4 delete this
ST112
S_SYSPWROK <13,39,87>
S_WAKE# <25,43,44,46,61>
ST131
ST134
ST113
S_SLP_S3# <39,60,75,87,96,102,104>
S_SLP_S4# <75,87,96>
ST114
S_SUSCLK <46>
S_SUSACK# <38>
S_SUSWARN# <38>
L1_LAN_WAKE# <69>
S_SLP_SUS# <41,99>
O_IOPWRBTN# <13,75,87>
O_RSTCON# <13,27,75,87>
S_SPKR
H_CPUPWRGD
S_ITP_PMODE <13>
S_JTAGX <13>
S_JTAG_TMS <13>
S_JTAG_TDO <13>
S_JTAG_TDI <13>
S_JTAG_TCK <13>
<70> S_HD_BITCLK
<70> S_HD_RST#
<70> A_HD_SDIN0
<70> S_HD_SDOUT
<70> S_HD_SYNC
<7> S_HDA_SDO_R
<7> H_HDA_SDI
<7> S_HDA_SCLK
total length <4",max=200;total length 330hm<x=400
<64> GP_TYPEC_CC_DETECT_2
<64> GP_TYPEC_CC_DETECT_1
<22> DP2VGA_XO
<27,37,39,104> S_PWROK
<38> S_RSMRST#
<38> S_DPWROK
<37> S_SMBCLK_VSB
<37> S_SMBDATA_VSB
<67> L1_SMBCLK
<67> L1_SMBDATA
<75,87,117> O2_SMB2_CLK
<75,87,117> O2_SMB2_DATA
S_RTCRST#_R
S_RTCRST#_R <87,117>
S_D4_RESET#_R <14,15>
DDR sequence,reseve follow CRB
+3VSB_ATX
PDG:RC time delay between 18ms~25ms must be met!
BATTERY2
BATTERY
BATT_HOLDER
Battery Socket
3V/220mAh
Clear RTC
HEADER_1X2P
12006-00160500
ME disable
<36> ME_UNLOCK
audio side IO power must be +3VSB
<10,13>
follow CRB
PLACE ALL ABOVE CLOSE TO PCH



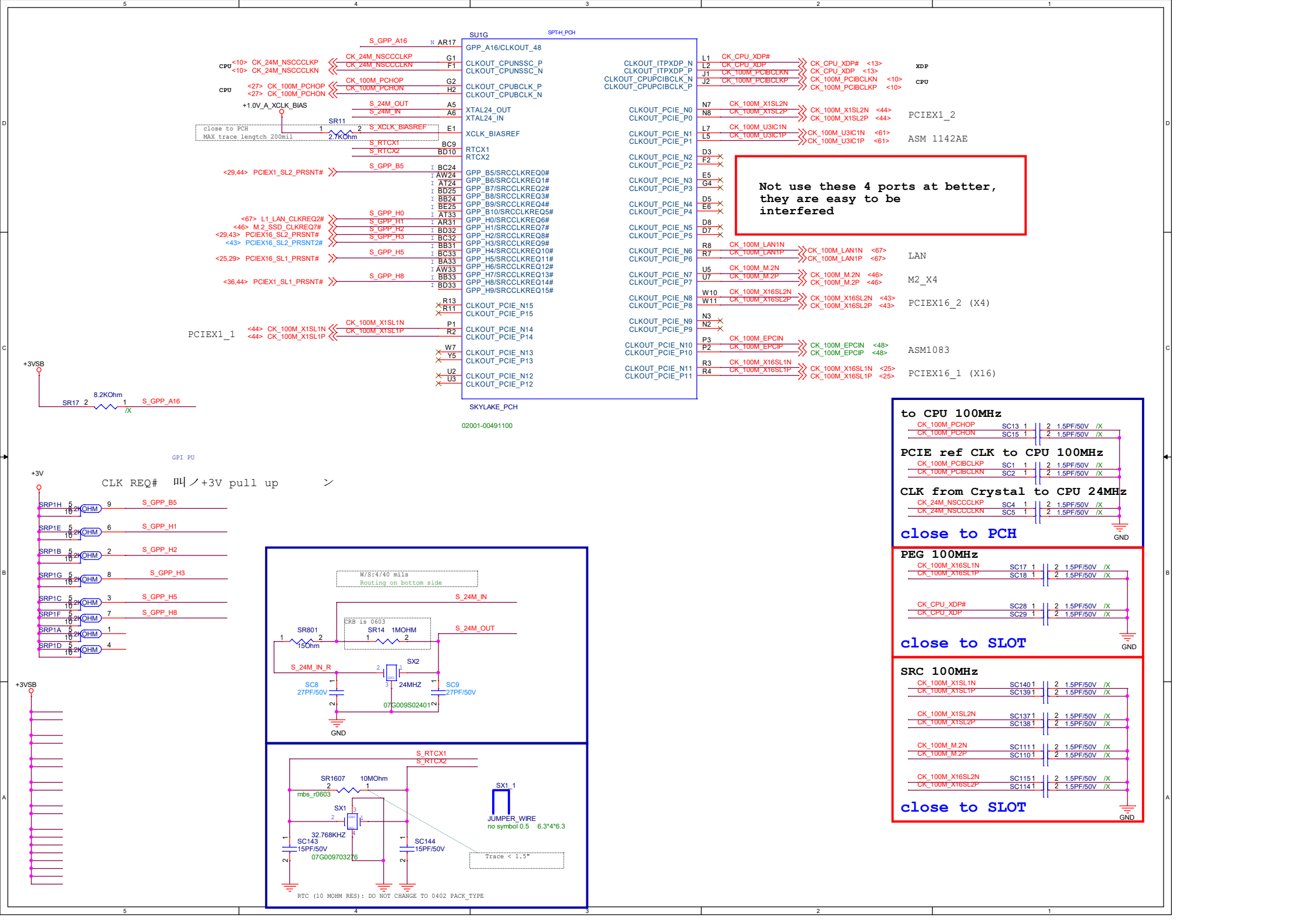
Note:

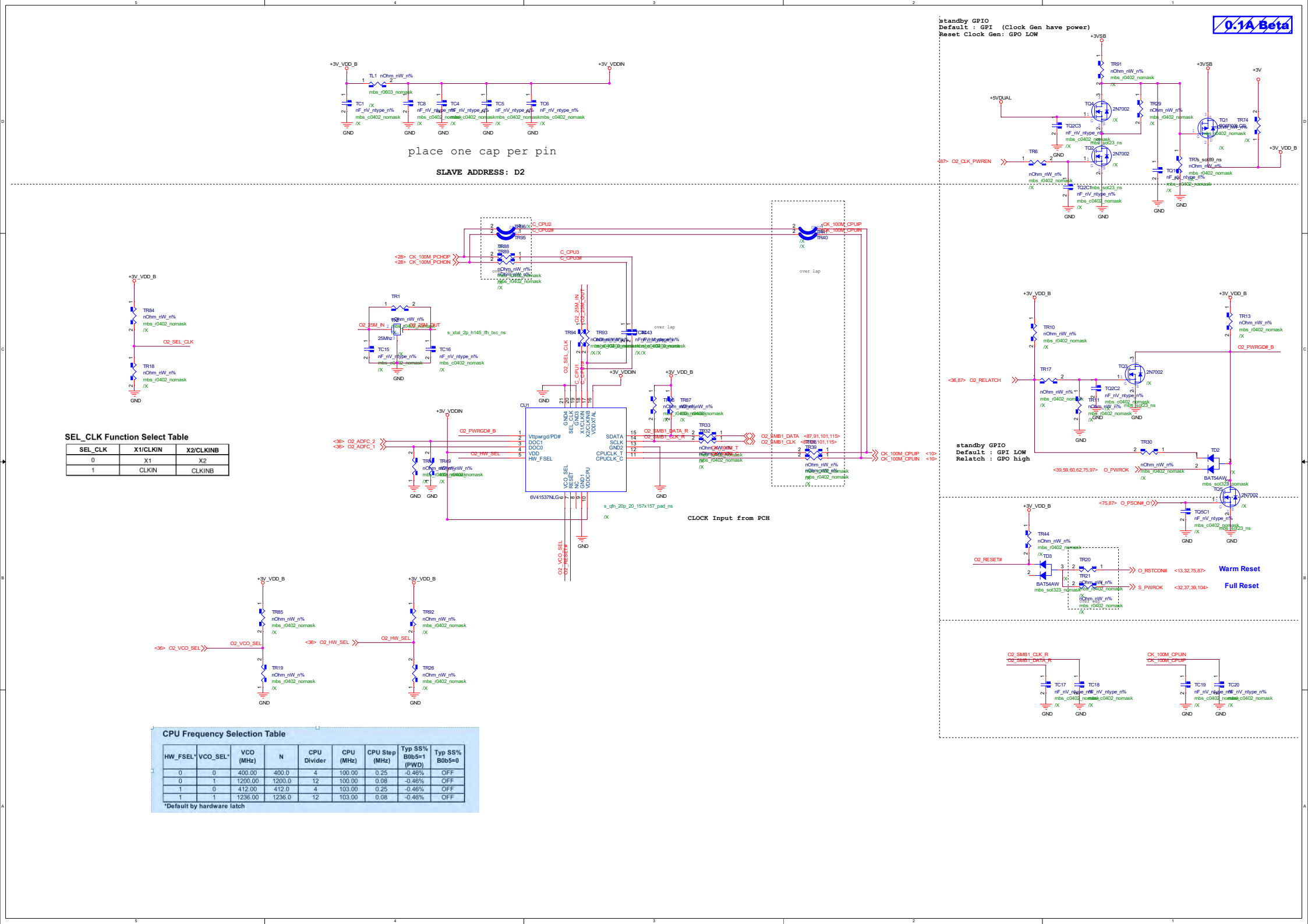
1. SATAGP[2:0]/SATAXPCIE[2:0]/GPP_E[2:0] and SATAGP[7:3]/SATAXPCIE[7:3]/GPP_F[4:0] has two native functions – the first native function (SATAXPCIEx) is selected if the Flex I/O soft strap SATA_PCIE_Select_for_Port_x = 11b. Setting SATA_PCIE_Select_for_Port_x = 11b also enables an internal pull-up resistor in this pin to allow Flexible I/O selection of SATA Port x or PCIe* Port x to be assigned based on the type of card installed and based on the SATAXPCIEx mux selector with the polarity for SATA or PCIe* (When SPSGPx = 0, PCIe* will be selected if the sampled value is "0" and SATA will be selected if the sampled value is "1"; When SPSGPx = 1, SATA will be selected if the sampled value is "0" and PCIe* will be selected if the sampled value is "1"). SATA/PCIe Select GPIO polarity for SATA Port x (SPSGPx) and Soft straps are handled through FITC and described in Skylake PCH SPI Flash Programming Guide (CDI doc #TBD).

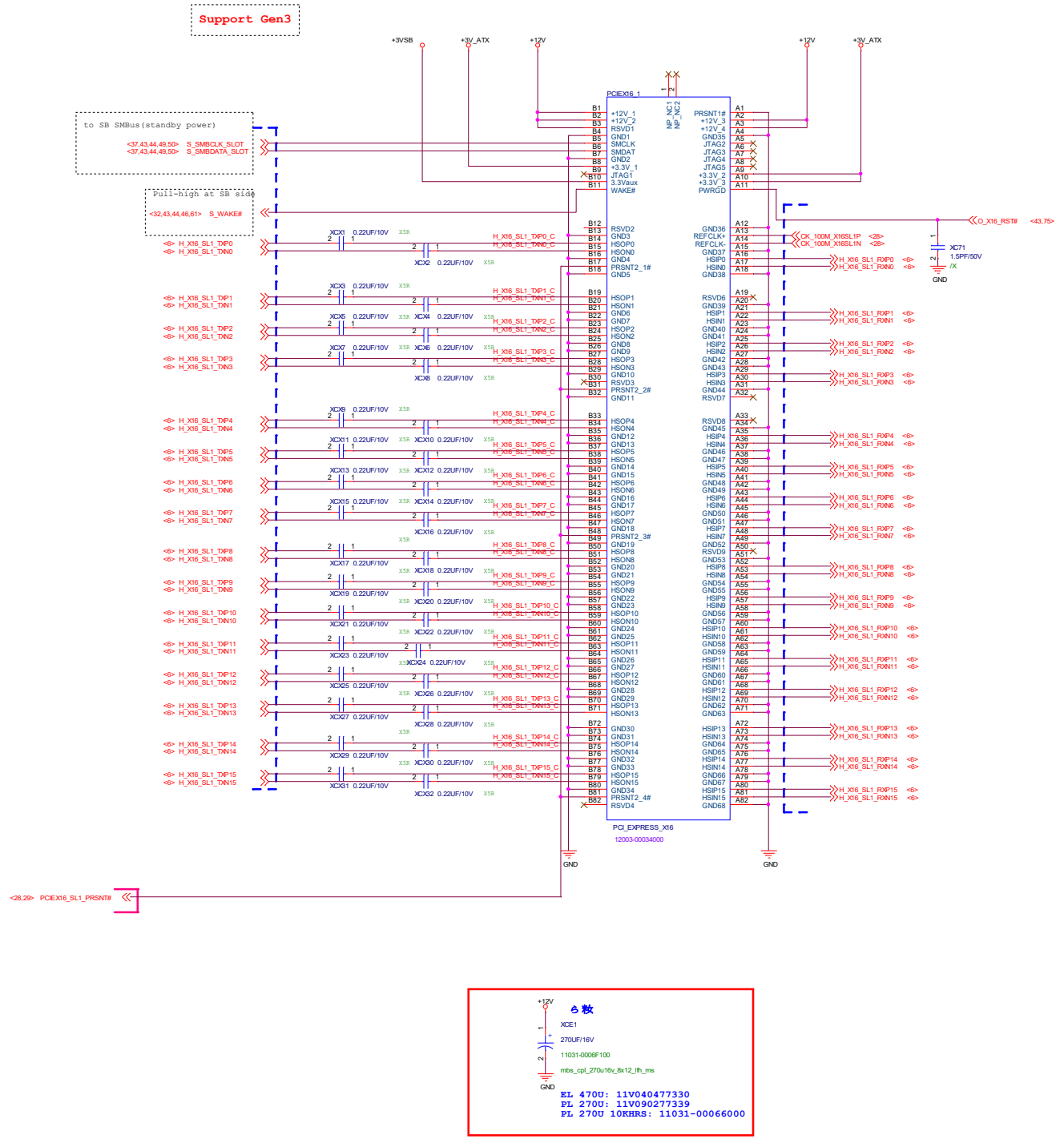

SU1B
<6> H_DMI_TXN0
<6> H_DMI_TXP0
<6> H_DMI_RXN0
<6> H_DMI_RXP0
<6> H_DMI_TXN1
<6> H_DMI_TXP1
<6> H_DMI_RXN1
<6> H_DMI_RXP1
<6> H_DMI_TXN2
<6> H_DMI_TXP2
<6> H_DMI_RXN2
<6> H_DMI_RXP2
<6> H_DMI_TXN3
<6> H_DMI_TXP3
<6> H_DMI_RXN3
<6> H_DMI_RXP3
L27 N27 C27 B27 E24 G24 B28 A28 G27 E26 B29 C29 L29 K29 B30 A30
DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0 DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1 DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2 DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3
DMI
Trace Width:12-15 mils, Other:12 mils
S_PCIE_RCOMPN B18
S_PCIE_RCOMPP C17
SR18 1 100Ohm 2
PCIE_RCOMPN PCIE_RCOMPP
H15 G15 A16 B16
PCIE1_RXN/USB3_7_RXN PCIE1_RXP/USB3_7_RXP PCIE1_TXN/USB3_7_TXN PCIE1_TXP/USB3_7_TXP
E17 G17 B19 C19
PCIE2_RXN/USB3_8_RXN PCIE2_RXP/USB3_8_RXP PCIE2_TXN/USB3_8_TXN PCIE2_TXP/USB3_8_TXP
L17 K17 B20 C20
PCIE3_RXN/USB3_9_RXN PCIE3_RXP/USB3_9_RXP PCIE3_TXN/USB3_9_TXN PCIE3_TXP/USB3_9_TXP
E20 G19 B21 A21
PCIE4_RXN/USB3_10_RXN PCIE4_RXP/USB3_10_RXP PCIE4_TXN/USB3_10_TXN PCIE4_TXP/USB3_10_TXP
PCIe/USB 3
LAN
<67> S_X1_LAN1_RXN
<67> S_X1_LAN1_RXP
<67> S_X1_LAN1_TXN
<67> S_X1_LAN1_TXP
PCIEX16_2 (X4)
<43> S_X16_SL2_RXN0
<43> S_X16_SL2_RXP0
<43> S_X16_SL2_TXN0
<43> S_X16_SL2_TXP0
<43> S_X16_SL2_RXN1
<43> S_X16_SL2_RXP1
<43> S_X16_SL2_TXN1
<43> S_X16_SL2_TXP1
K19 L19 D22 C22 G22 E22 B22 A23
PCIE5_RXN PCIE5_RXP PCIE5_TXN PCIE5_TXP PCIE6_RXN PCIE6_RXP PCIE6_TXN PCIE6_TXP
PCIEX1_1
<24> S_PCIE7_RXN
<24> S_PCIE7_RXP
<24> S_PCIE7_TXN
<24> S_PCIE7_TXP
L22 K22 C23 B23
PCIE7_RXN PCIE7_RXP PCIE7_TXN PCIE7_TXP
PCIEX1_2
<24> S_PCIE8_RXN
<24> S_PCIE8_RXP
<24> S_PCIE8_TXN
<24> S_PCIE8_TXP
K24 L24 C24 B24
PCIE8_RXN PCIE8_RXP PCIE8_TXN PCIE8_TXP
SKYLAKE_PCH
02001-00491100
USB 2.0
USB2N_1 USB2P_1 USB2N_2 USB2P_2 USB2N_3 USB2P_3 USB2N_4 USB2P_4 USB2N_5 USB2P_5 USB2N_6 USB2P_6 USB2N_7 USB2P_7 USB2N_8 USB2P_8 USB2N_9 USB2P_9 USB2N_10 USB2P_10 USB2N_11 USB2P_11 USB2N_12 USB2P_12 USB2N_13 USB2P_13 USB2N_14 USB2P_14
AF5 AG7 AD5 AD7 AG8 AG10 AE1 AE2 AC2 AC3 AF2 AF3 AB3 AB2 AL8 AL7 AA1 AA2 AJ8 AJ7 W2 W3 AD3 AD2 V2 V1 AJ11 AJ13 IPD
S_U2DN1_R <55,56>
S_U2DP1_R <55,56>
S_U2DN2_R <55,56>
S_U2DP2_R <55,56>
S_U2DN3_R <56,68>
S_U2DP3_R <56,68>
S_U2DN4_R <56,68>
S_U2DP4_R <56,68>
S_U2DN5_R <55,57>
S_U2DP5_R <55,57>
S_U2DN6_R <55,57>
S_U2DP6_R <55,57>
USB3_12
LAN USB3_34
KBMS_USB3_56
S_USB_PN6_R <54,79>
S_USB_PP6_R <54,79>
S_USB_PN7_R <54,79>
S_USB_PP7_R <54,79>
S_USB_PN8_R <53,54>
S_USB_PP8_R <53,54>
S_USB_PN9_R <53,54>
S_USB_PP9_R <53,54>
S_USB_PN10_R <53,54>
S_USB_PP10_R <53,54>
S_USB_PN11_R <53,54>
S_USB_PP11_R <53,54>
Front_USB78
Front_USB910
Front USB1112
SPM vicky delete Front USB1314
GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_F15/USB2_OCB_4
GPP_F16/USB2_OCB_5
GPP_F17/USB2_OCB_6
GPP_F18/USB2_OCB_7
AD43 AD42 AD39 AC44 Y43 Y41 W44 W43
S_USB3_OC#12 <55>
S_USB3_OC#34 <55>
S_USB3_OC#56 <55>
S_USB_OC#78 <53>
S_USB_OC#910 <53>
S_USB_OC#1112 <53>
S_USB2_OCB_6
S_USB2_OCB_7
If not used ,pu to +3VSB
+3VSB
SR157 2 8.2KOhm 1
SR152 2 8.2KOhm 1
Place Within 500mil
USB2_COMP
USB2_VBUSSENSE
RSVD5
USB2_ID
AG3 AD10 AB13 AG2
S_USB2_COMP
SR22 1 2 113Ohm
1KOhm SR9
1KOhm SR10
ST47
GND
GPD7/RSVD
BD14 S_GP_D7
ST48

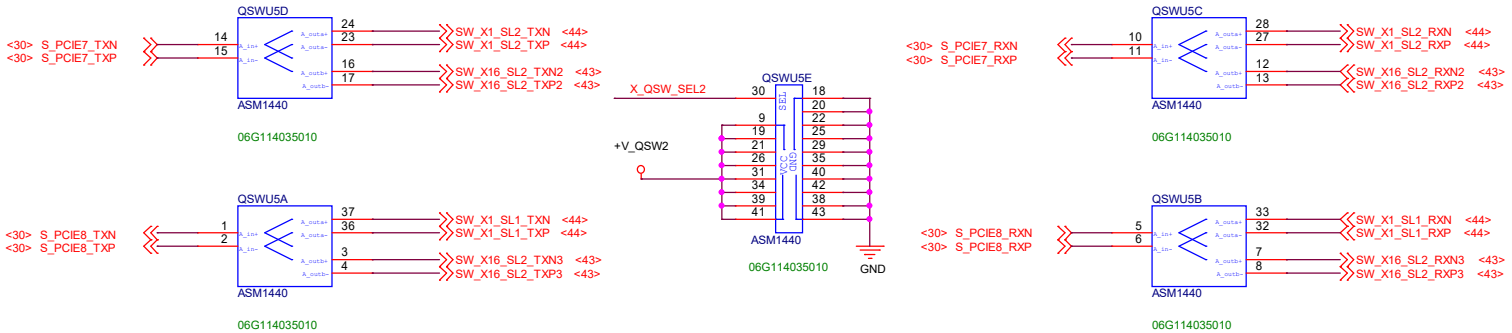


+3VSB
SR1 8.2KOhm N/A S_PME#
follow CRB
stuff SR200 for XDP
SR200 1KOhm /XDP S_SPI_MOSI
SR201 8.2KOhm /X
BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
GND
SU1A
SKYLAKE_PCH
02001-00491100
GPP_A11/PME#
RSVD1
RSVD2
RSVD3
RSVD4
TP2
TP1
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_CS2#
GPP_D1/SPI1_CLK
GPP_D0/SPI1_CS#
GPP_D3/SPI1_MOSI
GPP_D2/SPI1_MISO
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
GPP_B13/PLTRST#
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXRESET#
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
<48> S_PME#
<41> S_SPI_MOSI
<41> S_SPI_MISO
<41> S_SPI_CS0#
<41> S_SPI_CLK
<13,41> S_SPI_IO2
<41> S_SPI_IO3
PU on SIO side(+3VSB)
<107> CPU_OV
SR1676 0Ohm S_GPP_D1
<87> O2_SCI#
<75> O_PME#
S_GPP_D3
S_GPP_D2
S_GPP_D22
S_GPP_D21
ST2
ST3
S_PLTRST#_R SR5 22Ohm PCH_PLTRST# <87>
S_GPP_G12
GP_CPUFAN_PWMPU_EN# <81>
O_CPUFAN_PWM_DETECT <81>
if not used,delete the unused signal
S_GPP_E3
S_GPP_E7
S_GPP_B4 SR1626 0Ohm /X PCIEX1_SL2_PRSNT# <28,44>
S_GPP_H18
S_GPP_H17
S_GPP_H16 SR1620 0Ohm /X ST1 PCIEX16_SL1_PRSNT# <25,28>
S_GPP_H14
S_GPP_H13
S_GPP_H12 S_PCIE_X1/X4#_SEL <24>
S_GPP_H10 SR1621 0Ohm /X PCIEX16_SL2_PRSNT# <28,43>
S_INTRUDER#
<13> XDP_SPI_MOSI SR97 /X 0Ohm S_SPI_MOSI
GPI pull high
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
S_GPP_H12 SR180 /X 8.2KOhm SR181 /X 8.2KOhm
+3V
S_GPP_E3 SR28 /X 8.2KOhm
S_GPP_G12 SR15 /X 3.3KOHM
S_GPP_E7 SR78 /X 3.3KOHM
+3V_BAT
S_INTRUDER# SR87 1MOHM
S_INTRUDER# SC521 1.5PF/50V /X
for DUMMY load control
SR185 8.2KOhm /X
S_GPP_H18
SR183 8.2KOhm /X
SC204 0.1UF/16V /X
SQ53 H2N7002 /X 07005-00271300
O_+12V_DUMMYLOAD1 <105>
SR184 8.2KOhm /X
S_GPP_H14
SR182 8.2KOhm /X
SC203 0.1UF/16V /X
SQ52 H2N7002 /X 07005-00271300
O_+12V_DUMMYLOAD2 <105>
If not CLK buffer ,SU2
&SR60
SR561
SR1646 8.2KOhm /X/SPTH
SC36 0.1UF/16V /X/SPTH
<87> O2_PLTRST#
<87> PCH_PLTRST#
SU2 SN74AUP1G08DRLR /X/SPTH
S_PLTRST# <42,48,52,67,75,86,117>
0Ohm /SPTH 06G004258020 SR561
SRN205C 8.2KOHM
SRN205D 8.2KOHM
SRN205A 8.2KOHM S_GPP_D3
SRN205B 8.2KOHM S_GPP_H13

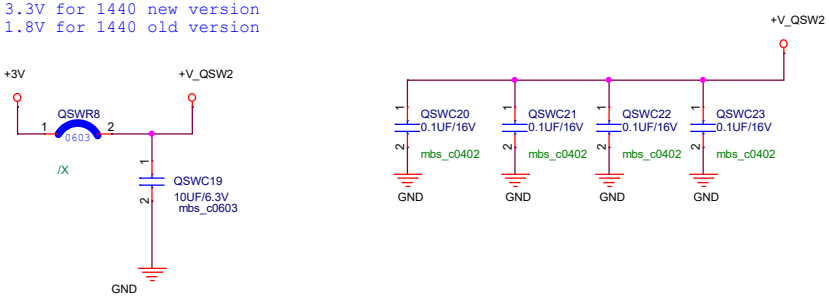

SU1G
SPT-H_PCH
SKYLAKE_PCH
02001-00491100
GPP_A16/CLKOUT_48
CLKOUT_CPUNSSC_P
CLKOUT_CPUNSSC_N
CLKOUT_CPUBCLK_P
CLKOUT_CPUBCLK_N
XTAL24_OUT
XTAL24_IN
XCLK_BIASREF
RTCX1
RTCX2
GPP_B5/SRCCLKREQ0#
GPP_B6/SRCCLKREQ1#
GPP_B7/SRCCLKREQ2#
GPP_B8/SRCCLKREQ3#
GPP_B9/SRCCLKREQ4#
GPP_B10/SRCCLKREQ5#
GPP_H0/SRCCLKREQ6#
GPP_H1/SRCCLKREQ7#
GPP_H2/SRCCLKREQ8#
GPP_H3/SRCCLKREQ9#
GPP_H4/SRCCLKREQ10#
GPP_H5/SRCCLKREQ11#
GPP_H6/SRCCLKREQ12#
GPP_H7/SRCCLKREQ13#
GPP_H8/SRCCLKREQ14#
GPP_H9/SRCCLKREQ15#
CLKOUT_PCIE_N15
CLKOUT_PCIE_P15
CLKOUT_PCIE_N14
CLKOUT_PCIE_P14
CLKOUT_PCIE_N13
CLKOUT_PCIE_P13
CLKOUT_PCIE_N12
CLKOUT_PCIE_P12
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_CPUPCIBCLK_N
CLKOUT_CPUPCIBCLK_P
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
CLKOUT_PCIE_N8
CLKOUT_PCIE_P8
CLKOUT_PCIE_N9
CLKOUT_PCIE_P9
CLKOUT_PCIE_N10
CLKOUT_PCIE_P10
CLKOUT_PCIE_N11
CLKOUT_PCIE_P11
CK_CPU_XDP#
CK_CPU_XDP
CK_100M_PCIBCLKN
CK_100M_PCIBCLKP
CK_100M_X1SL2N
CK_100M_X1SL2P
CK_100M_U3IC1N
CK_100M_U3IC1P
CK_100M_LAN1N
CK_100M_LAN1P
CK_100M_M.2N
CK_100M_M.2P
CK_100M_X16SL2N
CK_100M_X16SL2P
CK_100M_EPCIN
CK_100M_EPCIP
CK_100M_X16SL1N
CK_100M_X16SL1P
XDP
CPU
PCIEX1_2
ASM 1142AE
LAN
M2_X4
PCIEX16_2 (X4)
ASM1083
PCIEX16_1 (X16)
Not use these 4 ports at better, they are easy to be interfered
CK_24M_NSCCCLKP
CK_24M_NSCCCLKN
CK_100M_PCHOP
CK_100M_PCHON
S_24M_OUT
S_24M_IN
S_XCLK_BIASREF
S_RTCX1
S_RTCX2
+1.0V_A_XCLK_BIAS
SR11
2.7KOhm
close to PCH
MAX trace length 200mil
S_GPP_B5
S_GPP_H0
S_GPP_H1
S_GPP_H2
S_GPP_H3
S_GPP_H5
S_GPP_H8
PCIEX1_1
CK_100M_X1SL1N
CK_100M_X1SL1P
+3VSB
8.2KOhm
SR17
S_GPP_A16
/X
GPI PU
+3V
CLK REQ# 씨ノ+3V pull up ン
SRP1H
SRP1E
SRP1B
SRP1G
SRP1C
SRP1F
SRP1A
SRP1D
10K OHM
W/S:4/40 mils
Routing on bottom side
CRB is 0603
SR801
15Ohm
SR14 1MOHM
S_24M_IN_R
SX2
24MHZ
SC8
27PF/50V
SC9
27PF/50V
07G009S02401
GND
S_RTCX1
S_RTCX2
SR1607
10MOhm
mbs_r0603
SX1
32.768KHZ
SC143
15PF/50V
SC144
15PF/50V
07G009703276
SX1_1
JUMPER_WIRE
no symbol 0.5 6.3*4*6.3
Trace < 1.5"
RTC (10 MOHM RES): DO NOT CHANGE TO 0402 PACK_TYPE
to CPU 100MHz
CK_100M_PCHOP
CK_100M_PCHON
SC13
SC15
1.5PF/50V
/X
PCIE ref CLK to CPU 100MHz
CK_100M_PCIBCLKP
CK_100M_PCIBCLKN
SC1
SC2
CLK from Crystal to CPU 24MHz
CK_24M_NSCCCLKP
CK_24M_NSCCCLKN
SC4
SC5
close to PCH
GND
PEG 100MHz
CK_100M_X16SL1N
CK_100M_X16SL1P
SC17
SC18
CK_CPU_XDP#
CK_CPU_XDP
SC28
SC29
close to SLOT
GND
SRC 100MHz
CK_100M_X1SL1N
CK_100M_X1SL1P
SC1401
SC1391
CK_100M_X1SL2N
CK_100M_X1SL2P
SC1371
SC1381
CK_100M_M.2N
CK_100M_M.2P
SC1111
SC1101
CK_100M_X16SL2N
CK_100M_X16SL2P
SC1151
SC1141
close to SLOT
GND


0.1A Beta
standby GPIO
Default : GPI (Clock Gen have power)
Reset Clock Gen: GPO LOW
place one cap per pin
SLAVE ADDRESS: D2
SEL_CLK Function Select Table
SEL_CLK | X1/CLKIN | X2/CLKINB
0 | X1 | X2
1 | CLKIN | CLKINB
CLOCK Input from PCH
standby GPIO
Default : GPI LOW
Relatch : GPO high
Warm Reset
Full Reset
CPU Frequency Selection Table
HW_FSEL* | VCO_SEL* | VCO (MHz) | N | CPU Divider | CPU (MHz) | CPU Step (MHz) | Typ SS% B0b5=1 (PWD) | Typ SS% B0b5=0
0 | 0 | 400.00 | 400.0 | 4 | 100.00 | 0.25 | -0.46% | OFF
0 | 1 | 1200.00 | 1200.0 | 12 | 100.00 | 0.08 | -0.46% | OFF
1 | 0 | 412.00 | 412.0 | 4 | 103.00 | 0.25 | -0.46% | OFF
1 | 1 | 1236.00 | 1236.0 | 12 | 103.00 | 0.08 | -0.46% | OFF
*Default by hardware latch


Support Gen3
to SB SMBus(standby power)
<37,43,44,49,50> S_SMBCLK_SLOT
<37,43,44,49,50> S_SMBDATA_SLOT
Pull-high at SB side
<32,43,44,46,61> S_WAKE#
+3VSB
+3V_ATX
+12V
PCIEX16_1
PCI_EXPRESS_X16
12003-00034000
GND
<28,29> PCIEX16_SL1_PRSNT#
O_X16_RST# <43,75>
CK_100M_X16SL1P <28>
CK_100M_X16SL1N <28>
XC71
1.5PF/50V
/X
XCE1
270UF/16V
11031-0006F100
mbs_cpl_270u16v_8x12_lfh_ms
EL 470U: 11V040477330
PL 270U: 11V090277339
PL 270U 10KHRS: 11031-00066000



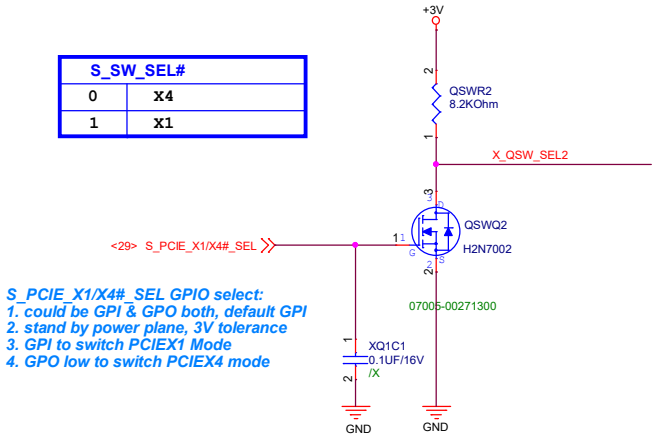
3.3V for 1440 new version
1.8V for 1440 old version



Sel Pin	Function		
L	N_in to N_outa	X1	M.2
H	N_in to N_outb	X4	PCIEX1.2

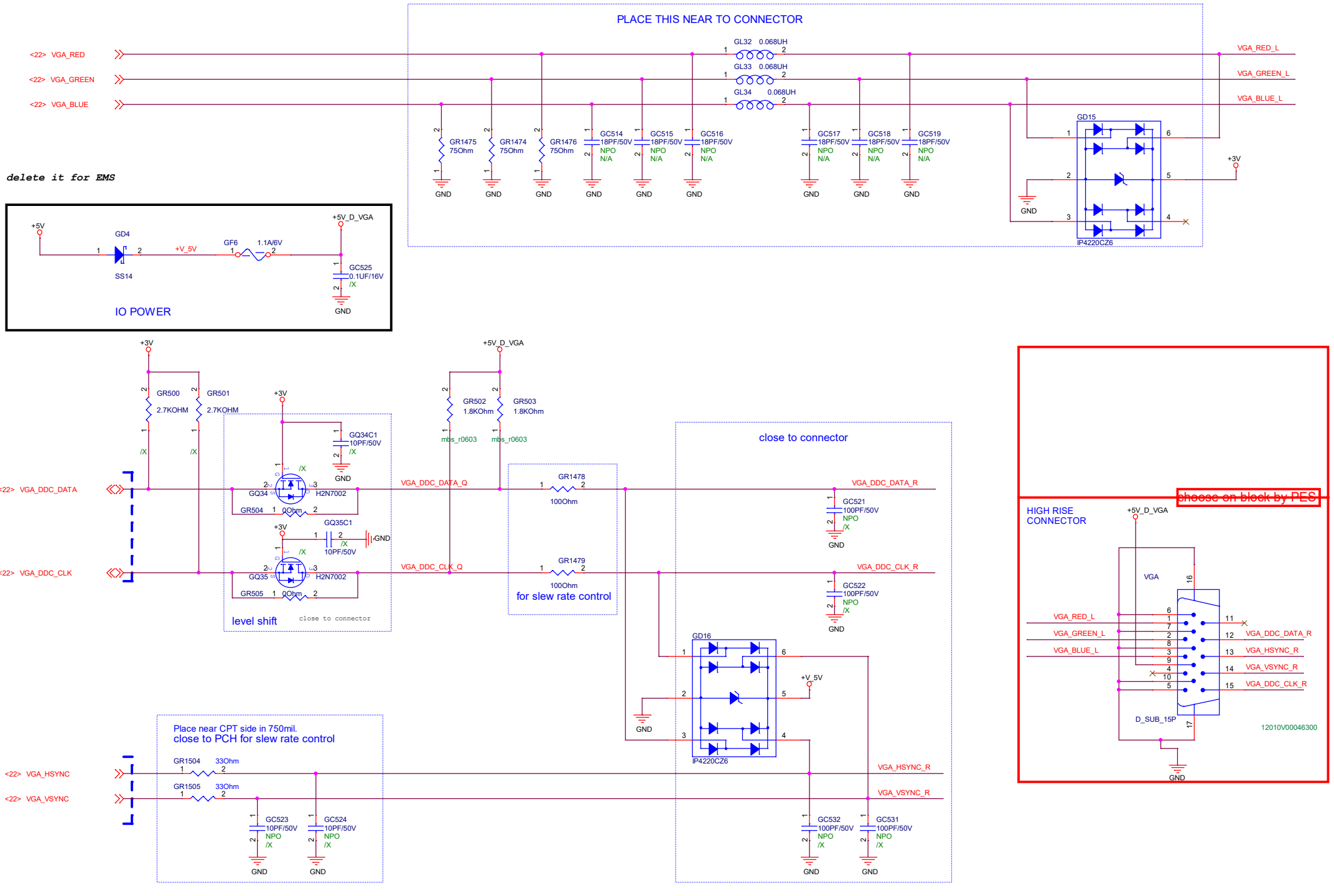
S_M2_SEL#	
0	PCIE1
1	M.2

S_SW_SEL#	
0	X4
1	X1

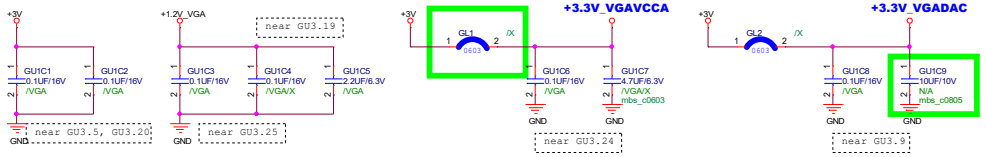


S_PCIE_X1/X4#_SEL GPIO select:
1. could be GPI & GPO both, default GPI
2. stand by power plane, 3V tolerance
3. GPI to switch PCIEX1 Mode
4. GPO low to switch PCIEX4 mode

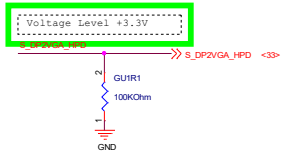
M2_CONFIG3/PRESENT#	
0	M.2 Present
1	M.2 Unplug

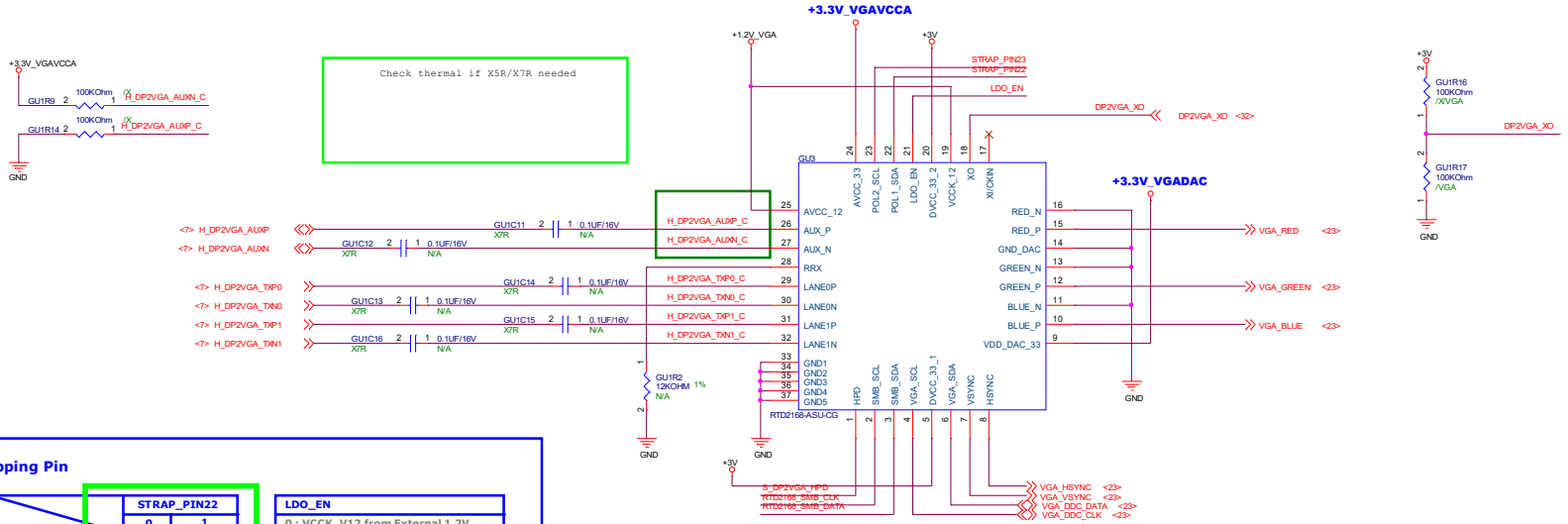

PLACE THIS NEAR TO CONNECTOR
<22> VGA_RED
<22> VGA_GREEN
<22> VGA_BLUE
GL32 0.068UH
GL33 0.068UH
GL34 0.068UH
VGA_RED_L
VGA_GREEN_L
VGA_BLUE_L
GR1475 75Ohm
GR1474 75Ohm
GR1476 75Ohm
GC514 18PF/50V NPO N/A
GC515 18PF/50V NPO N/A
GC516 18PF/50V NPO N/A
GC517 18PF/50V NPO N/A
GC518 18PF/50V NPO N/A
GC519 18PF/50V NPO N/A
GD15
IP4220CZ6
+3V
GND
delete it for EMS
+5V
GD4
SS14
+V_5V
GF6 1.1A/6V
+5V_D_VGA
GC525 0.1UF/16V /X
IO POWER
+3V
GR500 2.7KOHM
GR501 2.7KOHM
+5V_D_VGA
GR502 1.8KOhm
GR503 1.8KOhm
mbs_r0603
GQ34C1 10PF/50V /X
GQ35C1 10PF/50V /X
GQ34 H2N7002
GQ35 H2N7002
GR504 0Ohm
GR505 0Ohm
<22> VGA_DDC_DATA
<22> VGA_DDC_CLK
VGA_DDC_DATA_Q
VGA_DDC_CLK_Q
level shift
close to connector
GR1478 100Ohm
GR1479 100Ohm
for slew rate control
close to connector
VGA_DDC_DATA_R
VGA_DDC_CLK_R
GC521 100PF/50V NPO /X
GC522 100PF/50V NPO /X
GD16
IP4220CZ6
+V_5V
Place near CPT side in 750mil.
close to PCH for slew rate control
<22> VGA_HSYNC
<22> VGA_VSYNC
GR1504 33Ohm
GR1505 33Ohm
GC523 10PF/50V NPO /X
GC524 10PF/50V NPO /X
VGA_HSYNC_R
VGA_VSYNC_R
GC532 100PF/50V NPO /X
GC531 100PF/50V NPO /X
choose on block by PES
HIGH RISE CONNECTOR
+5V_D_VGA
VGA
VGA_RED_L
VGA_GREEN_L
VGA_BLUE_L
VGA_DDC_DATA_R
VGA_HSYNC_R
VGA_VSYNC_R
VGA_DDC_CLK_R
D_SUB_15P
12010V00046300

RTD2168 Power Caps and Beads



Hot-Plug Detect

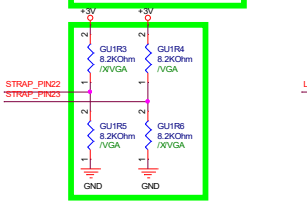


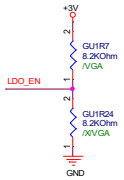


Strapping Pin

STRAP_PIN23 \ STRAP_PIN22	0	1
0	X	EP Mode
1	ROM	EEPROM

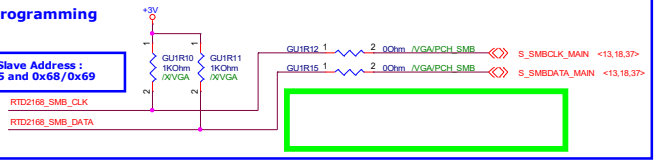
LDO_EN
0 : VCCK_V12 from External 1.2V
1 : VCCK_V12 from Embedded LDO



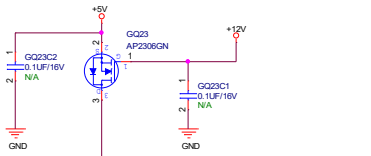


SMBus Programming

RTD2168 Slave Address : 0x64/0x65 and 0x68/0x69

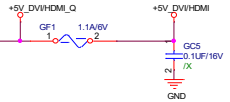


delete it
for EMS

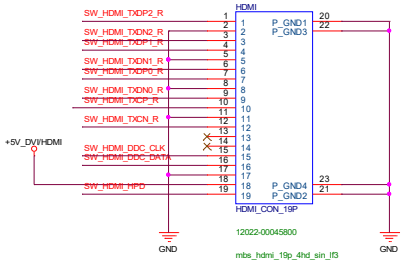


POWER for HDMI & DVI

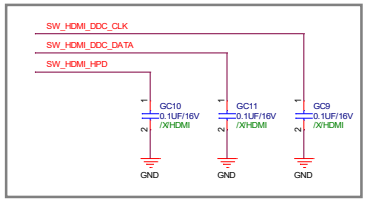
If only HDMI,this power must still need

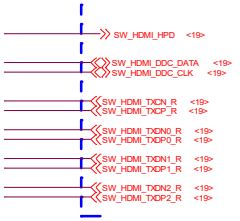


Passive/Active Devices					
Max Capacitance (Backdrive I Protection)	Schottky Diode	NA	pF	10	10
Resistor Value (+/- 5%)	R1/R2	NA	Ω	680	NA
ESD Protection	ESD	NA	NA	Optional	Optional
Max nFET Ron/Cout	NA	NA	Ω/pF	3ohm/10pF	NA



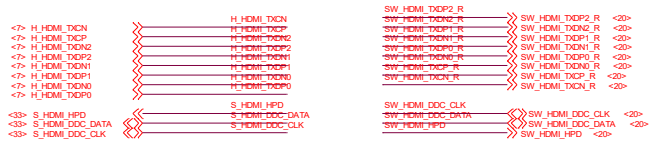
HDMI: 12022-00046900

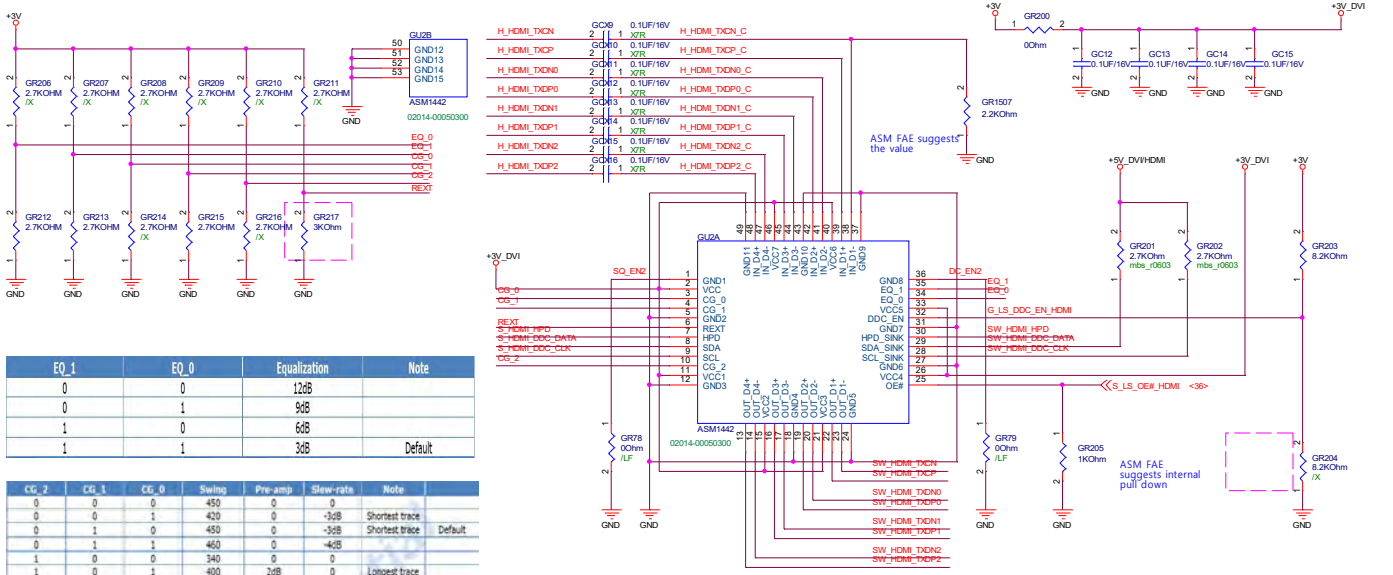




delete
it for
EMS

delete this page for HDMI/DVI colay

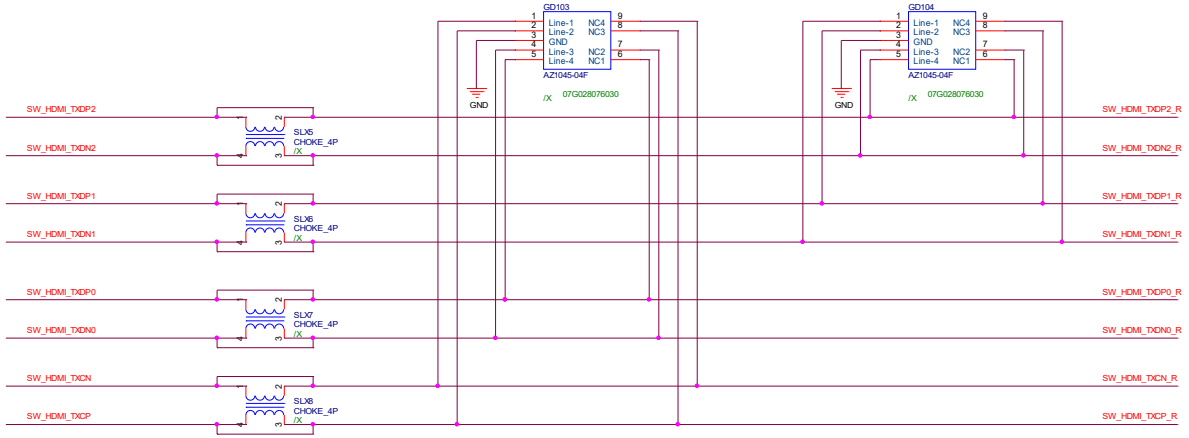


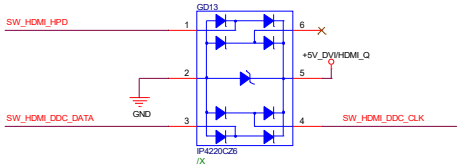


EQ_1	EQ_0	Equalization	Note
0	0	12dB	
0	1	9dB	
1	0	6dB	
1	1	3dB	Default

CG_2	CG_1	CG_0	Swing	Pre-amp	Slew-rate	Note	
0	0	0	450	0	0		
0	0	1	420	0	-3dB	Shortest trace	
0	1	0	450	0	-3dB	Shortest trace	Default
0	1	1	460	0	-4dB		
1	0	0	340	0	0		
1	0	1	400	2dB	0	Longest trace	
1	0	0	400	2dB	0	Longest trace	
1	1	1	420	0	0		

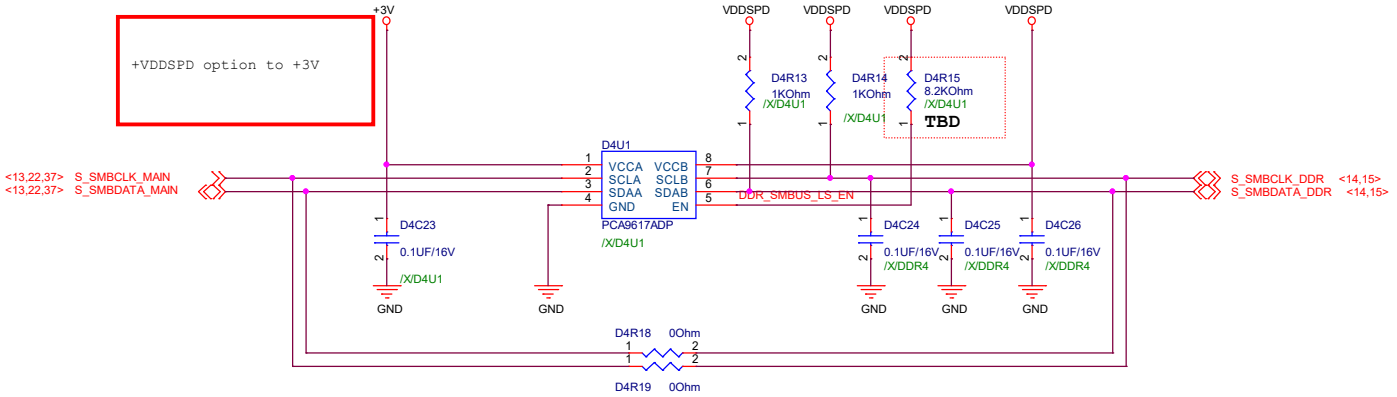
Level Shifter





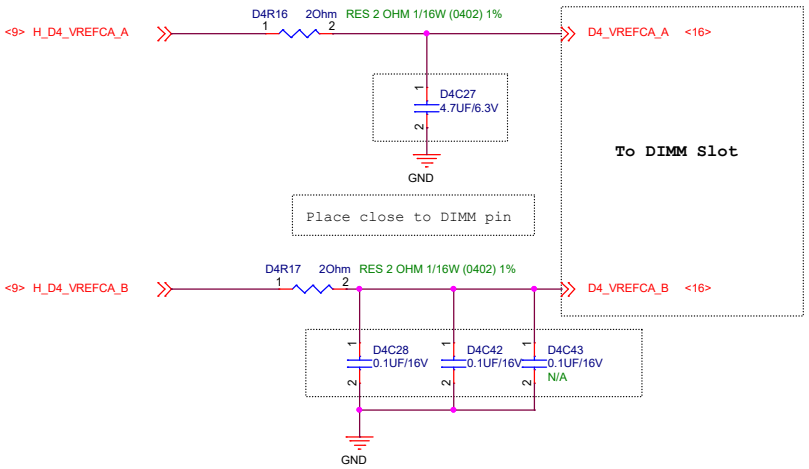
ESD

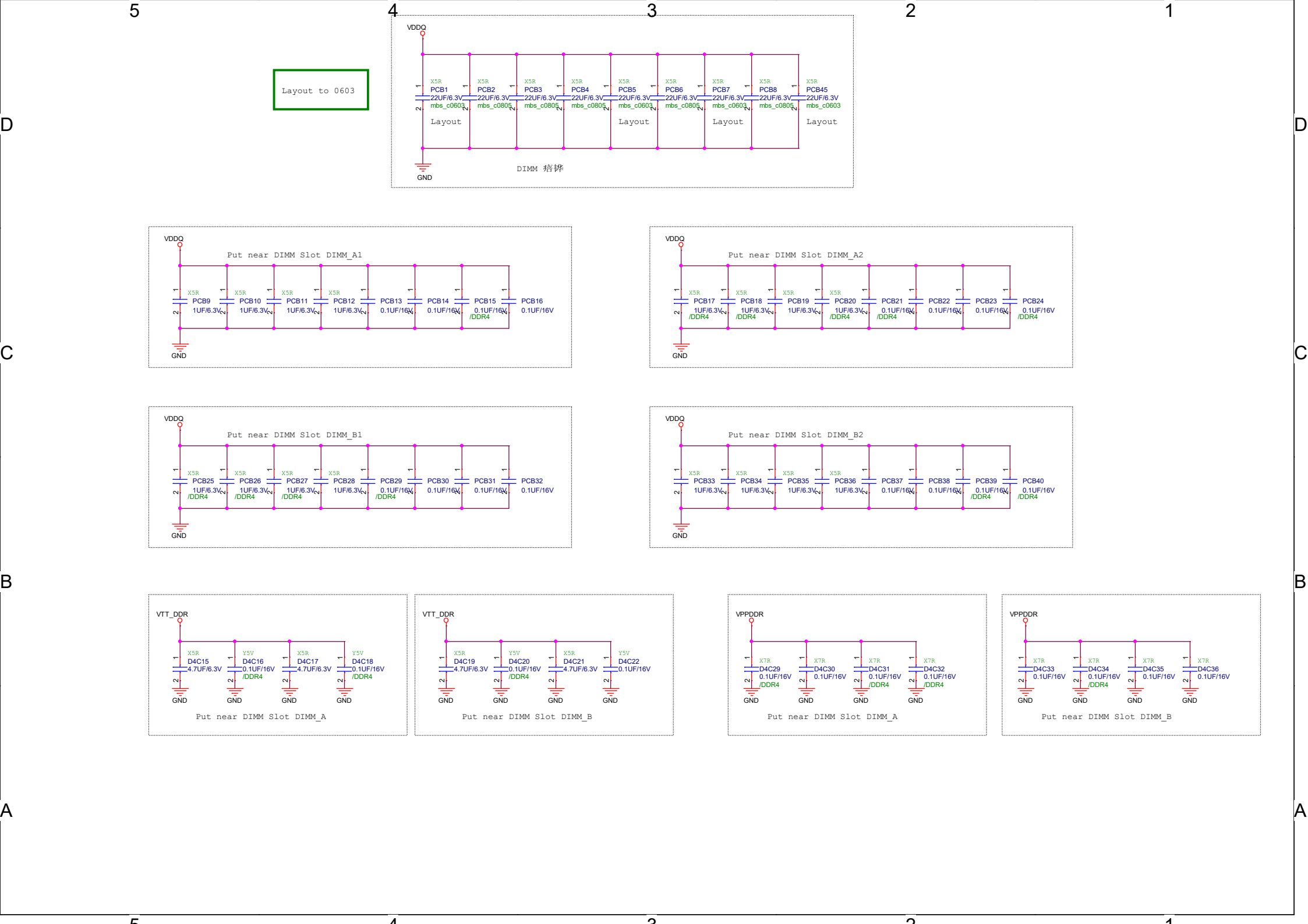
DRAM SMBUS From PCH (Thru Level Shift)

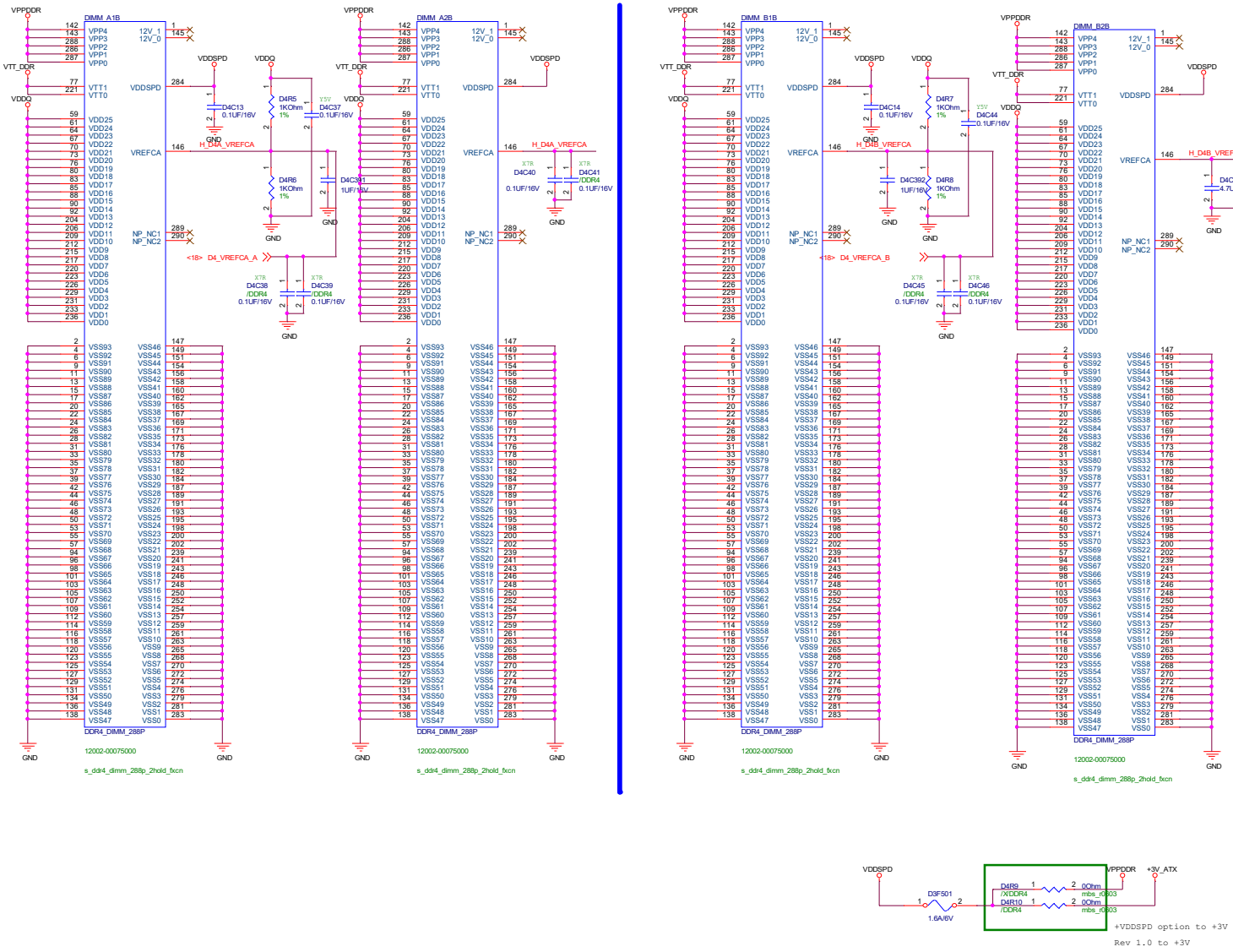


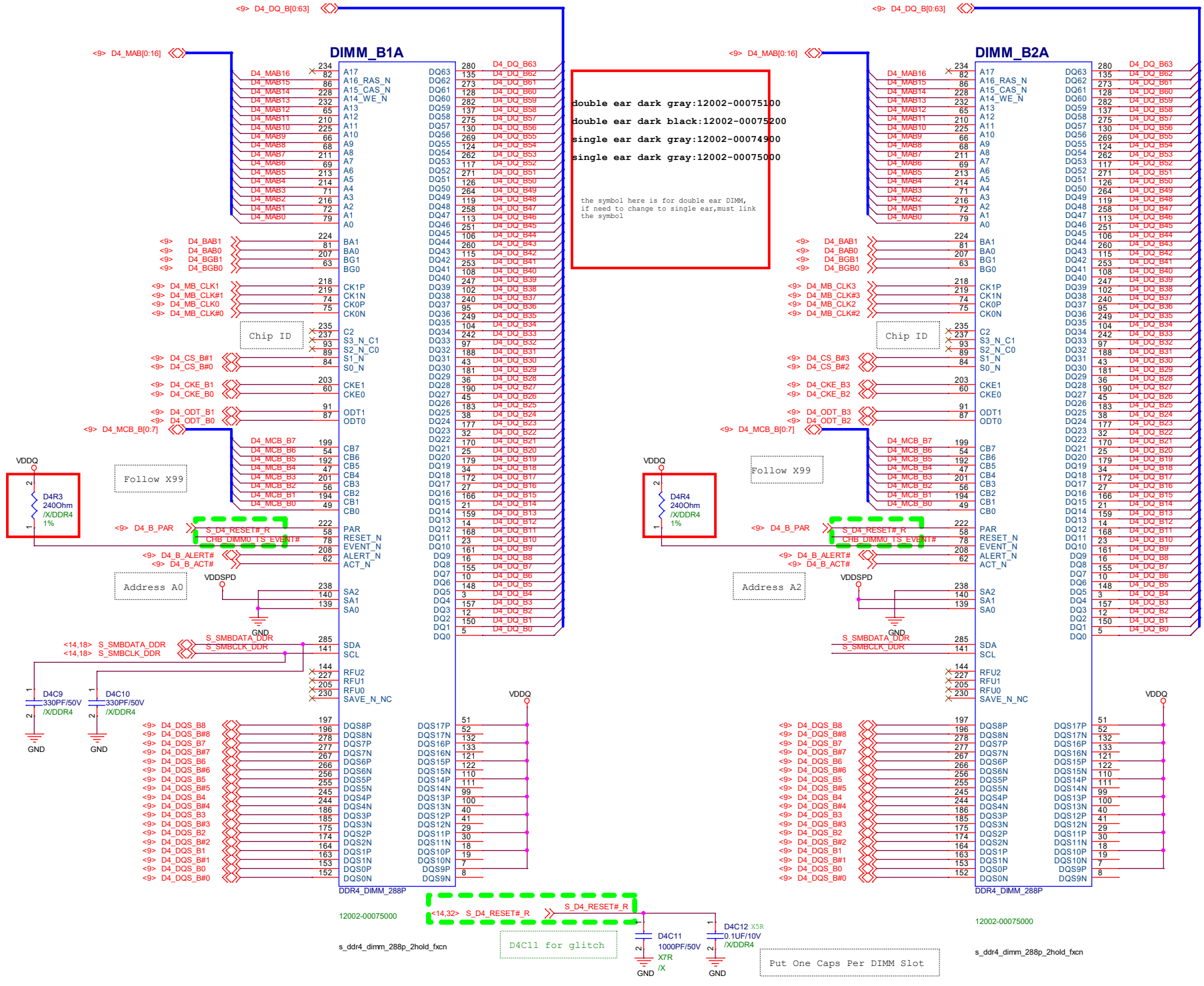
CPU DDR Vref

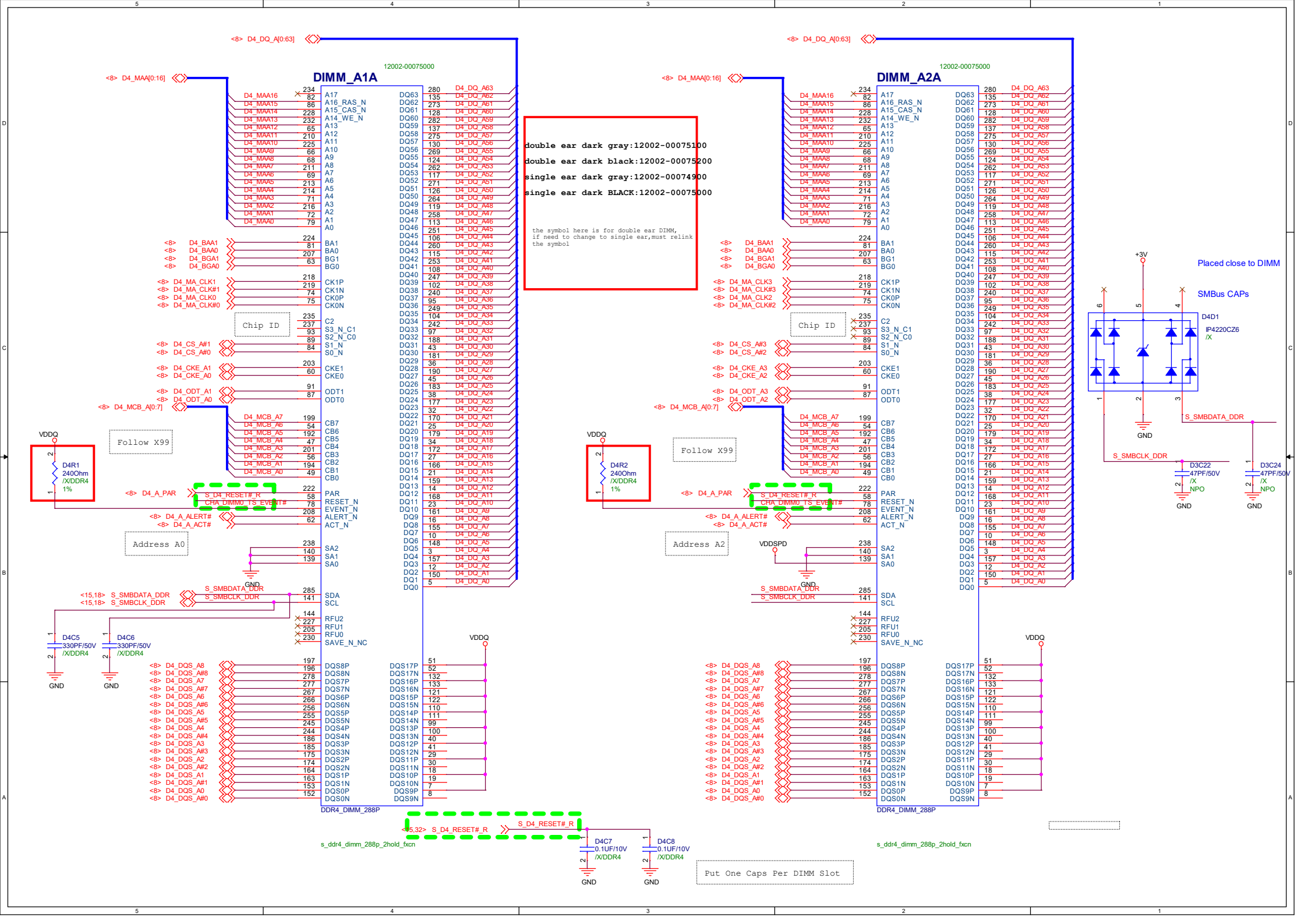
For CPU DDR Vref




Layout to 0603
VDDQ
X5R PCB1 22UF/6.3V mbs_c0603 Layout
X5R PCB2 22UF/6.3V mbs_c0805
X5R PCB3 22UF/6.3V mbs_c0805
X5R PCB4 22UF/6.3V mbs_c0805
X5R PCB5 22UF/6.3V mbs_c0603 Layout
X5R PCB6 22UF/6.3V mbs_c0805
X5R PCB7 22UF/6.3V mbs_c0603 Layout
X5R PCB8 22UF/6.3V mbs_c0805
X5R PCB45 22UF/6.3V mbs_c0603 Layout
GND
DIMM 痞斡
VDDQ
Put near DIMM Slot DIMM_A1
X5R PCB9 1UF/6.3V
X5R PCB10 1UF/6.3V
X5R PCB11 1UF/6.3V
X5R PCB12 1UF/6.3V
PCB13 0.1UF/16V
PCB14 0.1UF/16V
PCB15 0.1UF/16V /DDR4
PCB16 0.1UF/16V
GND
VDDQ
Put near DIMM Slot DIMM_A2
X5R PCB17 1UF/6.3V /DDR4
X5R PCB18 1UF/6.3V /DDR4
X5R PCB19 1UF/6.3V
X5R PCB20 1UF/6.3V /DDR4
PCB21 0.1UF/16V /DDR4
PCB22 0.1UF/16V
PCB23 0.1UF/16V
PCB24 0.1UF/16V /DDR4
GND
VDDQ
Put near DIMM Slot DIMM_B1
X5R PCB25 1UF/6.3V /DDR4
X5R PCB26 1UF/6.3V /DDR4
X5R PCB27 1UF/6.3V /DDR4
X5R PCB28 1UF/6.3V
PCB29 0.1UF/16V /DDR4
PCB30 0.1UF/16V
PCB31 0.1UF/16V
PCB32 0.1UF/16V
GND
VDDQ
Put near DIMM Slot DIMM_B2
X5R PCB33 1UF/6.3V
X5R PCB34 1UF/6.3V
X5R PCB35 1UF/6.3V
X5R PCB36 1UF/6.3V
PCB37 0.1UF/16V
PCB38 0.1UF/16V
PCB39 0.1UF/16V /DDR4
PCB40 0.1UF/16V /DDR4
GND
VTT_DDR
X5R D4C15 4.7UF/6.3V
Y5V D4C16 0.1UF/16V /DDR4
X5R D4C17 4.7UF/6.3V
Y5V D4C18 0.1UF/16V /DDR4
GND
Put near DIMM Slot DIMM_A
VTT_DDR
X5R D4C19 4.7UF/6.3V
Y5V D4C20 0.1UF/16V /DDR4
X5R D4C21 4.7UF/6.3V
Y5V D4C22 0.1UF/16V
GND
Put near DIMM Slot DIMM_B
VPPDDR
X7R D4C29 0.1UF/16V /DDR4
X7R D4C30 0.1UF/16V
X7R D4C31 0.1UF/16V /DDR4
X7R D4C32 0.1UF/16V /DDR4
GND
Put near DIMM Slot DIMM_A
VPPDDR
X7R D4C33 0.1UF/16V
X7R D4C34 0.1UF/16V /DDR4
X7R D4C35 0.1UF/16V
X7R D4C36 0.1UF/16V
GND
Put near DIMM Slot DIMM_B


DIMM_A1B
DIMM_A2B
DIMM_B1B
DIMM_B2B
DDR4_DIMM_288P
12002-00075000
s_ddr4_dimm_288p_2hold_fxcn
VPPDDR
VTT_DDR
VDDQ
VDDSPD
GND
H_D4A_VREFCA
H_D4B_VREFCA
D4_VREFCA_A
D4_VREFCA_B
D4C13 0.1UF/16V
D4C14 0.1UF/16V
D4C44 0.1UF/16V
D4R5 1KOhm 1%
D4R6 1KOhm 1%
D4R7 1KOhm 1%
D4R8 1KOhm 1%
D4C37 0.1UF/16V
D4C381 1UF/16V
D4C382 1UF/16V
D4C38 /DDR4 0.1UF/16V
D4C39 /DDR4 0.1UF/16V
D4C40 0.1UF/16V
D4C41 /DDR4 0.1UF/16V
D4C45 /DDR4 0.1UF/16V
D4C46 /DDR4 0.1UF/16V
D4C47 4.7UF/6.3V
D4C48 /DDR4 0.1UF/16V
D3F501 1.6A/6V
D4R9 /XDDR4 0Ohm mbs_r0603
D4R10 /DDR4 0Ohm mbs_r0603
+3V_ATX
+VDDSPD option to +3V
Rev 1.0 to +3V


DIMM_B1A
DIMM_B2A
<9> D4_DQ_B[0:63]
<9> D4_MAB[0:16]
<9> D4_BAB1
<9> D4_BAB0
<9> D4_BGB1
<9> D4_BGB0
<9> D4_MB_CLK1
<9> D4_MB_CLK#1
<9> D4_MB_CLK0
<9> D4_MB_CLK#0
<9> D4_MB_CLK3
<9> D4_MB_CLK#3
<9> D4_MB_CLK2
<9> D4_MB_CLK#2
Chip ID
<9> D4_CS_B#1
<9> D4_CS_B#0
<9> D4_CS_B#3
<9> D4_CS_B#2
<9> D4_CKE_B1
<9> D4_CKE_B0
<9> D4_CKE_B3
<9> D4_CKE_B2
<9> D4_ODT_B1
<9> D4_ODT_B0
<9> D4_ODT_B3
<9> D4_ODT_B2
<9> D4_MCB_B[0:7]
VDDQ
D4R3
240Ohm
/X/DDR4
1%
D4R4
240Ohm
/X/DDR4
1%
Follow X99
<9> D4_B_PAR
S_D4_RESET#_R
CHB_DIMM0_TS_EVENT#
<9> D4_B_ALERT#
<9> D4_B_ACT#
Address A0
Address A2
VDDSPD
GND
<14,18> S_SMBDATA_DDR
<14,18> S_SMBCLK_DDR
S_SMBDATA_DDR
S_SMBCLK_DDR
D4C9
330PF/50V
/X/DDR4
D4C10
330PF/50V
/X/DDR4
<9> D4_DQS_B8
<9> D4_DQS_B#8
<9> D4_DQS_B7
<9> D4_DQS_B#7
<9> D4_DQS_B6
<9> D4_DQS_B#6
<9> D4_DQS_B5
<9> D4_DQS_B#5
<9> D4_DQS_B4
<9> D4_DQS_B#4
<9> D4_DQS_B3
<9> D4_DQS_B#3
<9> D4_DQS_B2
<9> D4_DQS_B#2
<9> D4_DQS_B1
<9> D4_DQS_B#1
<9> D4_DQS_B0
<9> D4_DQS_B#0
DDR4_DIMM_288P
12002-00075000
s_ddr4_dimm_288p_2hold_fxcn
<14,32> S_D4_RESET#_R
D4C11 for glitch
D4C11
1000PF/50V
X7R
/X
D4C12 X5R
0.1UF/10V
/X/DDR4
Put One Caps Per DIMM Slot
double ear dark gray:12002-00075100
double ear dark black:12002-00075200
single ear dark gray:12002-00074900
single ear dark gray:12002-00075000
the symbol here is for double ear DIMM,
if need to change to single ear,must link
the symbol


DIMM_A1A
12002-00075000
DIMM_A2A
12002-00075000
double ear dark gray:12002-00075100
double ear dark black:12002-00075200
single ear dark gray:12002-00074900
single ear dark BLACK:12002-00075000
the symbol here is for double ear DIMM,
if need to change to single ear,must relink
the symbol
Chip ID
Follow X99
Address A0
Address A2
Put One Caps Per DIMM Slot
Placed close to DIMM
SMBus CAPs
D4D1
IP4220CZ6
/X
D4R1
240Ohm
/X/DDR4
1%
D4R2
240Ohm
/X/DDR4
1%
D4C5
330PF/50V
/X/DDR4
D4C6
330PF/50V
/X/DDR4
D4C7
0.1UF/10V
/X/DDR4
D4C8
0.1UF/10V
/X/DDR4
D3C22
47PF/50V
/X
NPO
D3C24
47PF/50V
/X
NPO
DDR4_DIMM_288P
s_ddr4_dimm_288p_2hold_fxcn
VDDQ
VDDSPD
+3V
GND
S_SMBDATA_DDR
S_SMBCLK_DDR
S_D4_RESET#_R
CHA_DIMM0_TS_EVENT#


XDP Card USB3 CON1
CT1P1 1 H_CFG0 <10>
CT1P2 1 H_CFG1 <10>
CT1P3 1 H_CFG2 <10>
CT1P5 1 H_CFG3 <10>
CT1P6 1 H_CFG4 <10>
CT1P8 1 H_CFG5 <10>
CT1P9 1 H_CFG6 <10>
CT1P11 1 H_CFG13 <10>
CT1P12 1 H_CFG12 <10>
CT1P13 1 H_CFG11 <10>
CT1P14 1 H_CFG10 <10>
CT1P15 1 H_CFG9 <10>
CT1P17 1 H_CFG8 <10>
CT1P18 1 H_CFG7 <10>
CT1P19 1 H_TRST# <10>
/X/1151
XDP Card USB3 CON4
+3VSB叫昵DIP桊骬铬絬 ˙XDP Card CON4 Pin1
CT4P2 1 H_CPUPWRGD <10,32>
CT4P5 S_SYSPWROK <32,39,87>
CT4P6 H_CPURST# <10,31>
CT4P8 S_SMBCLK_MAIN <18,22,37>
CT4P9 S_SMBDATA_MAIN <18,22,37>
CT4P11 H_TCK <10>
CT4P12 H_TMS <10>
CT4P14 CK_CPU_XDP <28>
CT4P15 CK_CPU_XDP# <28>
CT4P17 H_TDO <10>
CT4P18 S_JTAG_TDO <32>
+3VSB_ATX叫昵DIP桊骬铬絬 ˙XDP Card CON4 Pin19
XDP Card USB3 CON2
+VCCIO叫昵DIP桊骬铬絬 ˙XDP Card CON2 Pin1
CT2P2 1 H_CFG14 <10>
CT2P3 1 H_CFG15 <10>
CT2P5 1 H_CFG16 <10>
CT2P6 1 H_CFG17 <10>
GND叫铬絬 ˙XDP Card CON2 Pin7
CT2P8 1 H_CFG18 <10>
CT2P9 1 H_CFG19 <10>
CT2P11 1 SKL_XDP_MBP_1 <10>
CT2P12 1 SKL_XDP_MBP_0 <10>
CT2P14 1 H_TDI <10>
CT2P15 1 H_PRDY# <10>
CT2P17 1 H_PREQ# <10>
CT2P18 1 XDP_PCUDEBUG <10>
+1.0V_A叫昵DIP桊骬铬絬 ˙XDP Card CON2 Pin19
XDP Card USB3 CON3
CT3P1 1 S_XDP_PREQ# <35>
CT3P2 S_XDP_PRDY# <35>
CT3P3 O_RSMRST# <38,75,87,99,117>
CT3P5 O_IOPWRBTN# <32,75,87>
CT3P6 S_ITP_PMODE <32>
CT3P8 XDP_SPI_MOSI <29>
CT3P9 O_RSTCON# <27,32,75,87>
CT3P11 S_SPI_IO2 <29,41>
琵VCCST 础 XDP ㄣ蛸T桊
CT311叫铬絬 ˙CON3 Pin11
CT3P12 1 S_JTAG_TMS <32>
CT3P14 S_JTAG_TDI <32>
CT3P15 S_JTAG_TCK <32>
CT3P17 S_XDP_TRST# <35>
CT3P18 S_JTAGX <32>
+VCCST叫昵DIP桊骬铬絬 ˙XDP Card CON3 Pin19

Naming Rule:
CTxPy==>叫铬絬 XDP Card CONx connector Piny

Placement Rule:
琺琎代攡 场 竚璉琎緽梓块 狠,
Layout穁 pReferenceゅ 琎柞 ,
瓆T惠– 戳PCB セ 琝璉琎ゅ ,
顶诀贺PVT PCB セ叫瘑罘砒 猘紅ぃ琝璉琎ゅ

Power Rework:
+1.0V_A叫昵DIP桊骬铬絬 ˙XDP Card CON2 Pin19
+3VSB叫昵DIP桊骬铬絬 ˙XDP Card CON4 Pin1
+VCCST叫昵DIP桊骬铬絬 ˙XDP Card CON3 Pin19
+VCCIO叫昵DIP桊骬铬絬 ˙XDP Card CON2 Pin1
+3VSB_ATX叫昵DIP桊骬铬絬 ˙XDP Card CON4 Pin19
GND叫铬絬 ˙XDP Card CON2 Pin7

LGA1151F

SOCKET1151

12001-00180100

LGA1151G

SOCKET1151

12001-00180100

LGA1151H

SOCKET1151

12001-00180100

P_CPU_GND_GT

P_CPU_GND_VCORE

VCCGT

LGA1151J

SOCKET1151

12001-00180100

HT136 /X/1151

HT133 /X/1151

HT134 /X/1151

P_+VCCGT_VCC_10 <91>

P_+VCCGT_VSS_10 <91>

P_CPU_GND_GT <91>

P_CPU_GND_VCORE <91>

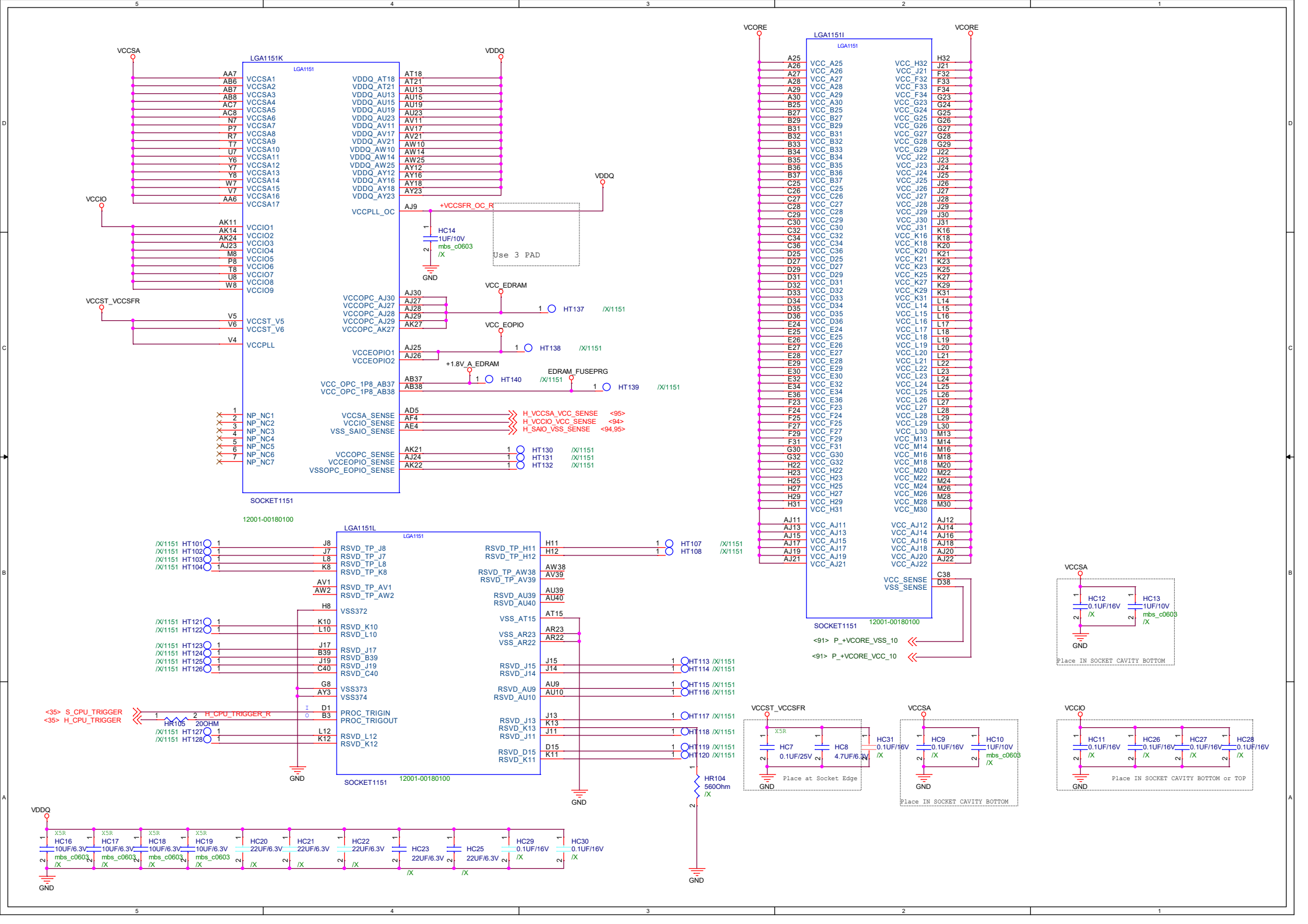
HR156
0Ohm
mbs_r0603
/X

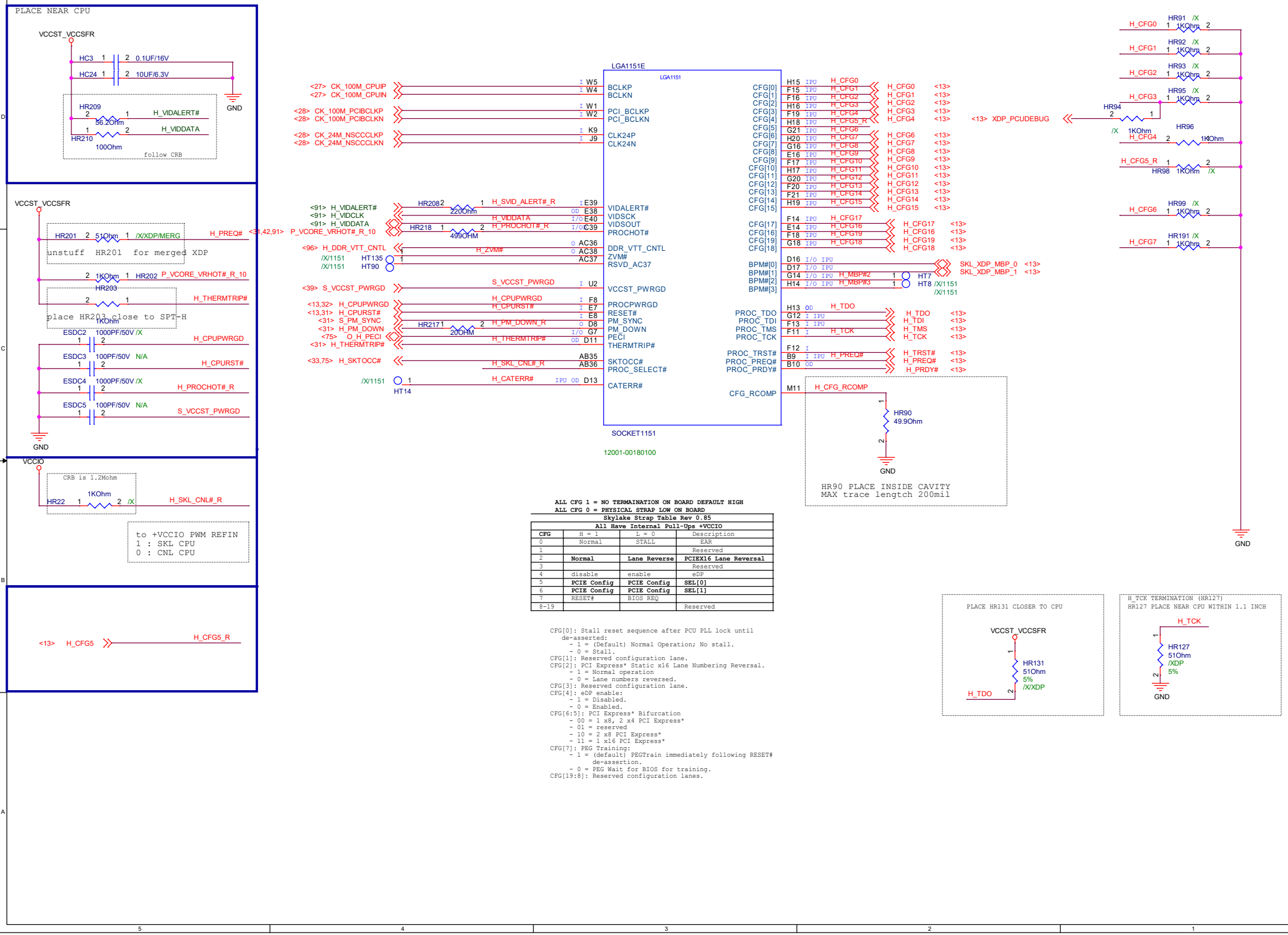
HR158
0Ohm
mbs_r0603
/X

GND

ILM1 13020-00063300

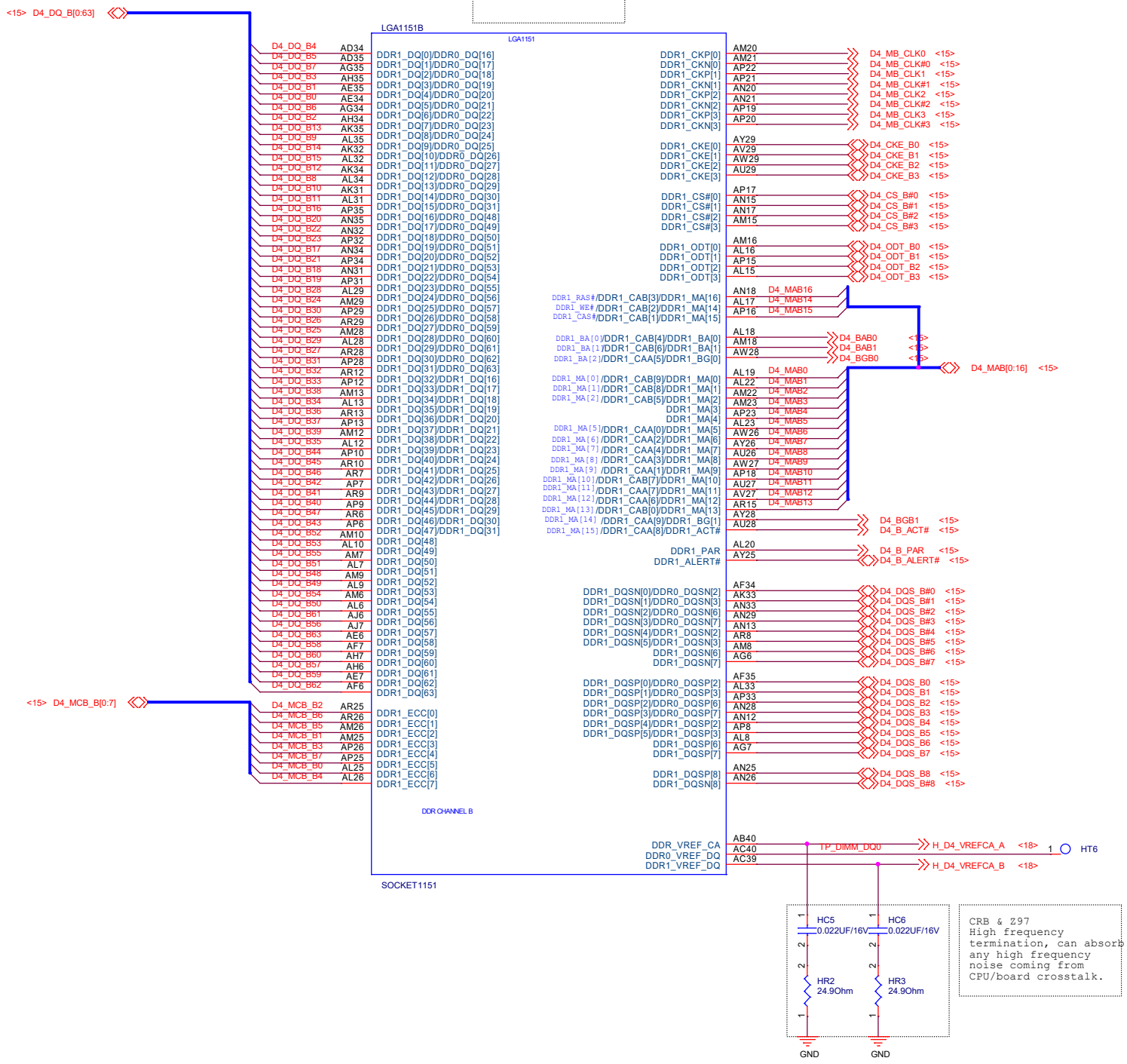
ILM2 13020-00062000


LGA1151K
LGA1151
SOCKET1151
12001-00180100
LGA1151L
LGA1151
SOCKET1151
12001-00180100
LGA1151I
LGA1151
SOCKET1151
12001-00180100
VCCSA
VDDQ
VCCIO
VCCST_VCCSFR
VCCPLL_OC
+VCCSFR_OC_R
HC14
1UF/10V
mbs_c0603
/X
Use 3 PAD
GND
VCC_EDRAM
VCC_EOPIO
+1.8V_A_EDRAM
EDRAM_FUSEPRG
HT137
HT138
HT140
HT139
/X/1151
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
H_VCCSA_VCC_SENSE
H_VCCIO_VCC_SENSE
H_SAIO_VSS_SENSE
VCCOPC_SENSE
VCCEOPIO_SENSE
VSSOPC_EOPIO_SENSE
HT130
HT131
HT132
NP_NC1
NP_NC2
NP_NC3
NP_NC4
NP_NC5
NP_NC6
NP_NC7
VCORE
VCC_SENSE
VSS_SENSE
<91> P_+VCORE_VSS_10
<91> P_+VCORE_VCC_10
HT101
HT102
HT103
HT104
HT107
HT108
HT113
HT114
HT115
HT116
HT117
HT118
HT119
HT120
HT121
HT122
HT123
HT124
HT125
HT126
HT127
HT128
<35> S_CPU_TRIGGER
<35> H_CPU_TRIGGER
H_CPU_TRIGGER_R
HR105
20OHM
HR104
560Ohm
PROC_TRIGIN
PROC_TRIGOUT
VSS372
VSS373
VSS374
VSS_AT15
VSS_AR23
VSS_AR22
HC12
0.1UF/16V
HC13
1UF/10V
Place IN SOCKET CAVITY BOTTOM
HC7
0.1UF/25V
HC8
4.7UF/6.3V
HC31
0.1UF/16V
Place at Socket Edge
HC9
0.1UF/16V
HC10
1UF/10V
Place IN SOCKET CAVITY BOTTOM
HC11
0.1UF/16V
HC26
0.1UF/16V
HC27
0.1UF/16V
HC28
0.1UF/16V
Place IN SOCKET CAVITY BOTTOM or TOP
HC16
10UF/6.3V
HC17
10UF/6.3V
HC18
10UF/6.3V
HC19
10UF/6.3V
HC20
22UF/6.3V
HC21
22UF/6.3V
HC22
22UF/6.3V
HC23
22UF/6.3V
HC25
22UF/6.3V
HC29
0.1UF/16V
HC30
0.1UF/16V
X5R
mbs_c0603
/X

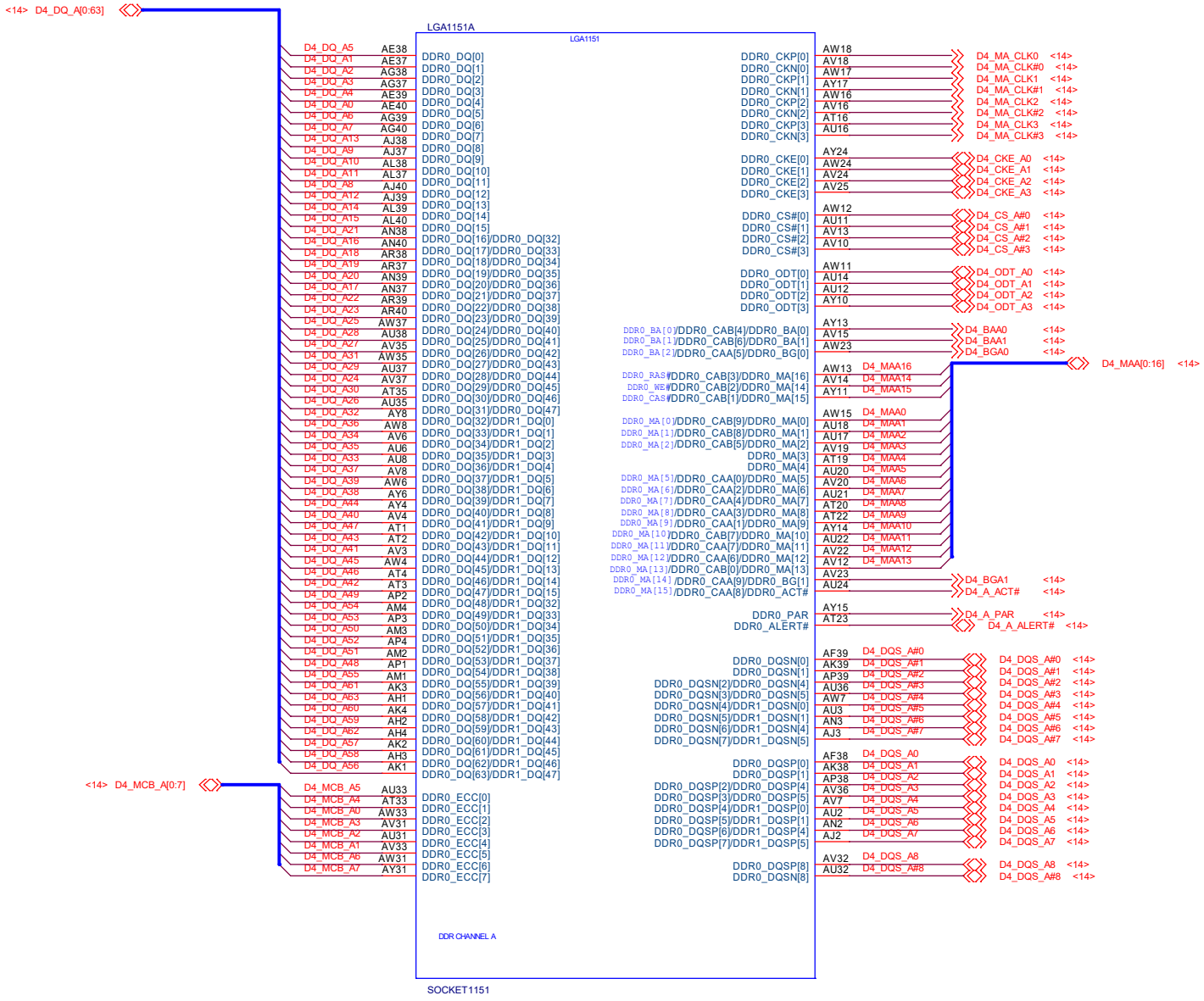

PLACE NEAR CPU
VCCST_VCCSFR
HC3 1 2 0.1UF/16V
HC24 1 2 10UF/6.3V
GND
HR209 2 1 H_VIDALERT#
56.2OHm
HR210 1 2 H_VIDDATA
100Ohm
follow CRB
VCCST_VCCSFR
HR201 2 51Ohm 1 /X/XDP/MERG H_PREQ#
unstuff HR201 for merged XDP
2 1KOhm 1 HR202 P_VCORE_VRHOT#_R_10
HR203
2 1 H_THERMTRIP#
place HR203 close to SPT-H
1KOhm
ESDC2 1000PF/50V /X H_CPUPWRGD
ESDC3 100PF/50V N/A H_CPURST#
ESDC4 1000PF/50V /X H_PROCHOT#_R
ESDC5 100PF/50V N/A S_VCCST_PWRGD
GND
VCCIO
CRB is 1.2Mohm
1KOhm
HR22 1 2 /X H_SKL_CNL#_R
to +VCCIO PWM REFIN
1 : SKL CPU
0 : CNL CPU
<13> H_CFG5 H_CFG5_R
LGA1151E
LGA1151
<27> CK_100M_CPUIP I W5 BCLKP
<27> CK_100M_CPUIN I W4 BCLKN
<28> CK_100M_PCIBCLKP I W1 PCI_BCLKP
<28> CK_100M_PCIBCLKN I W2 PCI_BCLKN
<28> CK_24M_NSCCCLKP I K9 CLK24P
<28> CK_24M_NSCCCLKN I J9 CLK24N
<91> H_VIDALERT# HR208 2 220Ohm 1 H_SVID_ALERT#_R I E39 VIDALERT#
<91> H_VIDCLK OD E38 VIDSCK
<91> H_VIDDATA H_VIDDATA I/O E40 VIDSOUT
HR218 1 499OHM 2 H_PROCHOT#_R I/O C39 PROCHOT#
<96> H_DDR_VTT_CNTL O AC36 DDR_VTT_CNTL
/X/1151 HT135 1 H_ZVM# O AC38 ZVM#
/X/1151 HT90 1 AC37 RSVD_AC37
<39> S_VCCST_PWRGD S_VCCST_PWRGD I U2 VCCST_PWRGD
<13,32> H_CPUPWRGD H_CPUPWRGD I F8 PROCPWRGD
<13,31> H_CPURST# H_CPURST# I E7 RESET#
<31> S_PM_SYNC I E8 PM_SYNC
<31> H_PM_DOWN HR2171 2 20OHM H_PM_DOWN_R O D8 PM_DOWN
<75> O_H_PECI I/O G7 PECI
<31> H_THERMTRIP# H_THERMTRIP# OD D11 THERMTRIP#
<33,75> H_SKTOCC# AB35 SKTOCC#
H_SKL_CNL#_R AB36 PROC_SELECT#
/X/1151 1 HT14 H_CATERR# IPU OD D13 CATERR#
CFG_RCOMP
SOCKET1151
12001-00180100
H15 IPU H_CFG0 CFG[0]
F15 IPU H_CFG1 CFG[1]
F16 IPU H_CFG2 CFG[2]
H16 IPU H_CFG3 CFG[3]
F19 IPU H_CFG4 CFG[4]
H18 IPU H_CFG5_R CFG[5]
G21 IPU H_CFG6 CFG[6]
H20 IPU H_CFG7 CFG[7]
G16 IPU H_CFG8 CFG[8]
E16 IPU H_CFG9 CFG[9]
F17 IPU H_CFG10 CFG[10]
H17 IPU H_CFG11 CFG[11]
G20 IPU H_CFG12 CFG[12]
F20 IPU H_CFG13 CFG[13]
F21 IPU H_CFG14 CFG[14]
H19 IPU H_CFG15 CFG[15]
F14 IPU H_CFG17 CFG[17]
E14 IPU H_CFG16 CFG[16]
F18 IPU H_CFG19 CFG[19]
G18 IPU H_CFG18 CFG[18]
H_CFG0 <13>
H_CFG1 <13>
H_CFG2 <13>
H_CFG3 <13>
H_CFG4 <13>
<13> XDP_PCUDEBUG
H_CFG6 <13>
H_CFG7 <13>
H_CFG8 <13>
H_CFG9 <13>
H_CFG10 <13>
H_CFG11 <13>
H_CFG12 <13>
H_CFG13 <13>
H_CFG14 <13>
H_CFG15 <13>
H_CFG17 <13>
H_CFG16 <13>
H_CFG19 <13>
H_CFG18 <13>
D16 I/O IPU BPM#[0]
D17 I/O IPU BPM#[1]
G14 I/O IPU H_MBP#2 1 HT7 BPM#[2]
H14 I/O IPU H_MBP#3 1 HT8 /X/1151 BPM#[3]
/X/1151
SKL_XDP_MBP_0 <13>
SKL_XDP_MBP_1 <13>
H13 OD H_TDO PROC_TDO
G12 I IPU PROC_TDI
F13 I IPU PROC_TMS
F11 I H_TCK PROC_TCK
H_TDO <13>
H_TDI <13>
H_TMS <13>
H_TCK <13>
F12 I PROC_TRST#
B9 I IPU H_PREQ# PROC_PREQ#
B10 OD PROC_PRDY#
H_TRST# <13>
H_PREQ# <13>
H_PRDY# <13>
M11 H_CFG_RCOMP
HR90 49.9Ohm
GND
HR90 PLACE INSIDE CAVITY
MAX trace lengtch 200mil
HR91 /X H_CFG0 1 1KOhm 2
HR92 /X H_CFG1 1 1KOhm 2
HR93 /X H_CFG2 1 1KOhm 2
HR95 /X H_CFG3 1 1KOhm 2
HR94 2 1 /X 1KOhm
HR96 H_CFG4 2 1KOhm
H_CFG5_R 1 2 HR98 1KOhm /X
HR99 /X H_CFG6 1 1KOhm 2
HR191 /X H_CFG7 1 1KOhm 2
GND
ALL CFG 1 = NO TERMAINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW ON BOARD
Skylake Strap Table Rev 0.85
All Have Internal Pull-Ups +VCCIO
CFG | H = 1 | L = 0 | Description
0 | Normal | STALL | EAR
1 | | | Reserved
2 | Normal | Lane Reverse | PCIEX16 Lane Reversal
3 | | | Reserved
4 | disable | enable | eDP
5 | PCIE Config | PCIE Config | SEL[0]
6 | PCIE Config | PCIE Config | SEL[1]
7 | RESET# | BIOS REQ |
8-19 | | | Reserved
CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
- 1 = (Default) Normal Operation; No stall.
- 0 = Stall.
CFG[1]: Reserved configuration lane.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
- 1 = Normal operation
- 0 = Lane numbers reversed.
CFG[3]: Reserved configuration lane.
CFG[4]: eDP enable:
- 1 = Disabled.
- 0 = Enabled.
CFG[6:5]: PCI Express* Bifurcation
- 00 = 1 x8, 2 x4 PCI Express*
- 01 = reserved
- 10 = 2 x8 PCI Express*
- 11 = 1 x16 PCI Express*
CFG[7]: PEG Training:
- 1 = (default) PEGTrain immediately following RESET# de-assertion.
- 0 = PEG Wait for BIOS for training.
CFG[19:8]: Reserved configuration lanes.
PLACE HR131 CLOSER TO CPU
VCCST_VCCSFR
HR131 51Ohm 5% /XDP
H_TDO
H_TCK TERMINATION (HR127)
HR127 PLACE NEAR CPU WITHIN 1.1 INCH
H_TCK
HR127 51Ohm /XDP 5%
GND

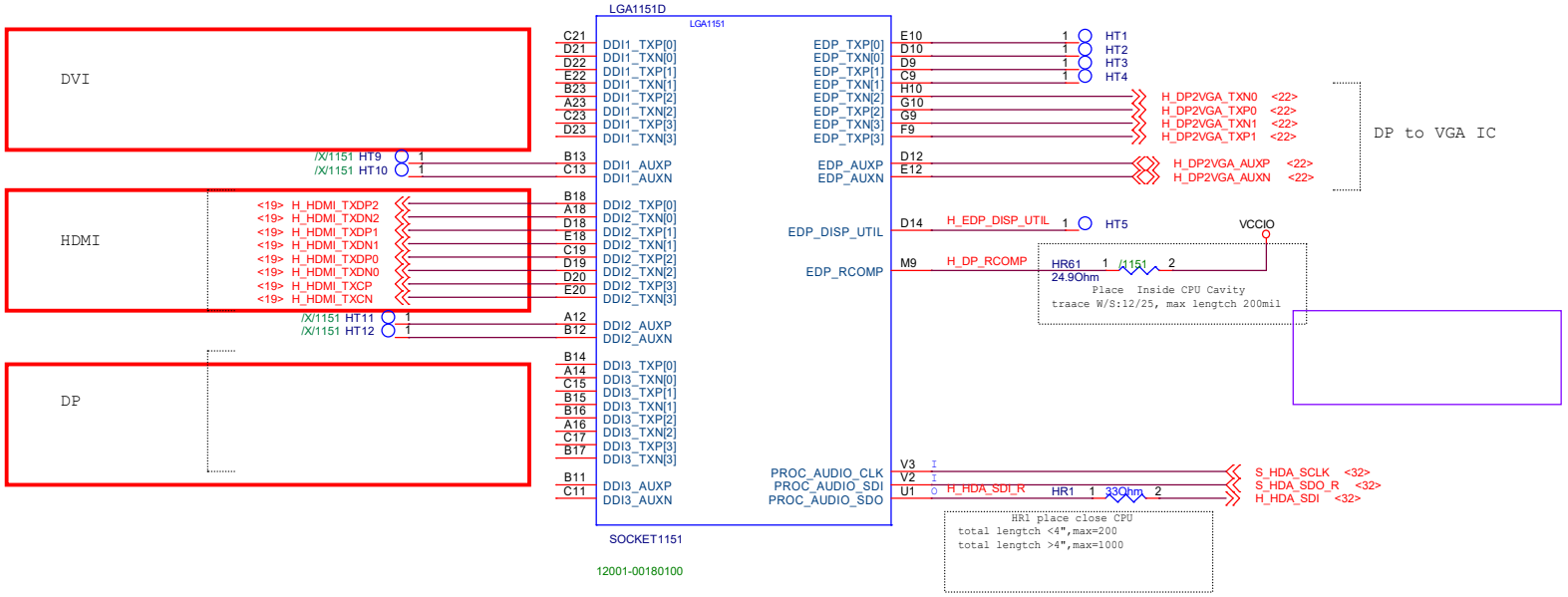
Follow CRB

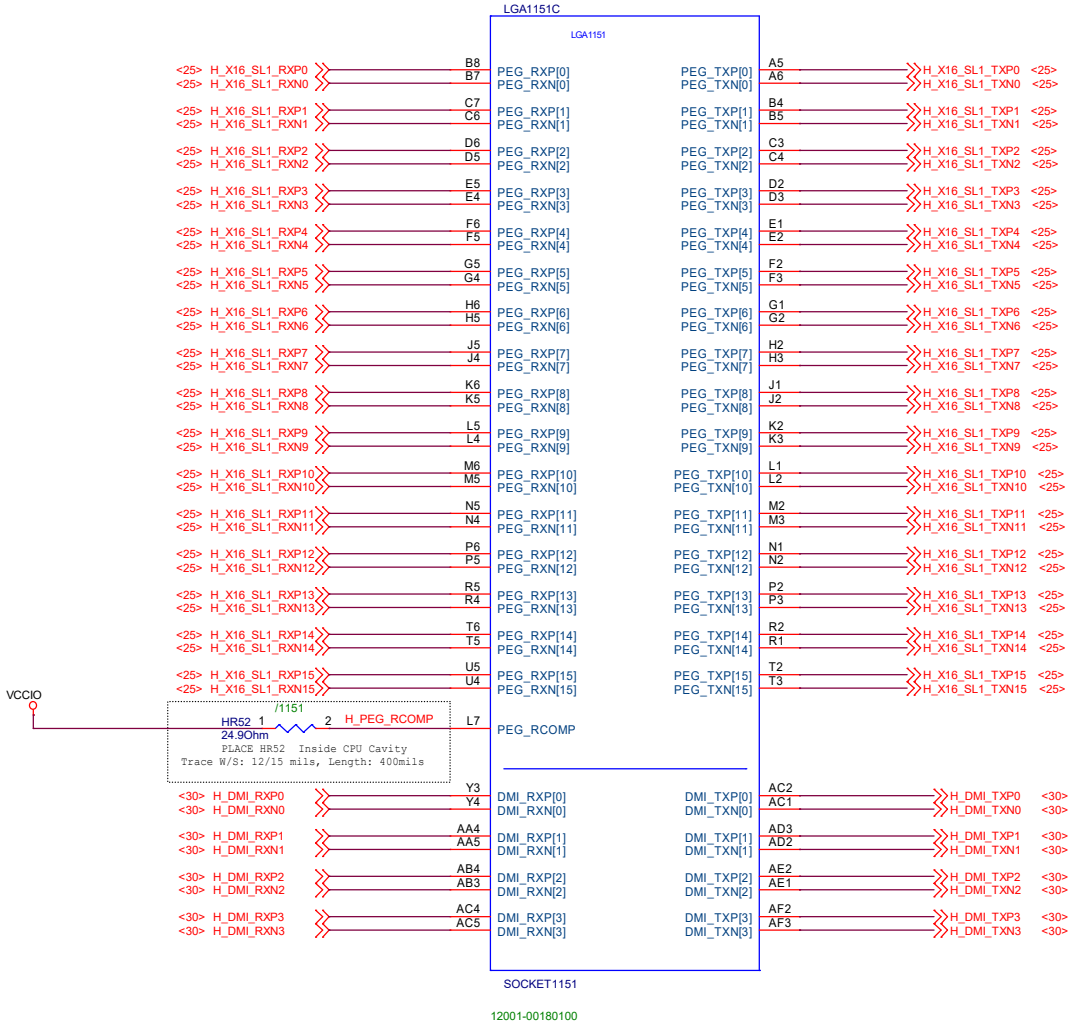
Channel B
4 Layer routing



Channel A
4 Layer routing




LGA1151D
LGA1151
DVI
HDMI
DP
C21 DDI1_TXP[0]
D21 DDI1_TXN[0]
D22 DDI1_TXP[1]
E22 DDI1_TXN[1]
B23 DDI1_TXP[2]
A23 DDI1_TXN[2]
C23 DDI1_TXP[3]
D23 DDI1_TXN[3]
/X/1151 HT9 1
/X/1151 HT10 1
B13 DDI1_AUXP
C13 DDI1_AUXN
B18 DDI2_TXP[0]
A18 DDI2_TXN[0]
D18 DDI2_TXP[1]
E18 DDI2_TXN[1]
C19 DDI2_TXP[2]
D19 DDI2_TXN[2]
D20 DDI2_TXP[3]
E20 DDI2_TXN[3]
<19> H_HDMI_TXDP2
<19> H_HDMI_TXDN2
<19> H_HDMI_TXDP1
<19> H_HDMI_TXDN1
<19> H_HDMI_TXDP0
<19> H_HDMI_TXDN0
<19> H_HDMI_TXCP
<19> H_HDMI_TXCN
/X/1151 HT11 1
/X/1151 HT12 1
A12 DDI2_AUXP
B12 DDI2_AUXN
B14 DDI3_TXP[0]
A14 DDI3_TXN[0]
C15 DDI3_TXP[1]
B15 DDI3_TXN[1]
B16 DDI3_TXP[2]
A16 DDI3_TXN[2]
C17 DDI3_TXP[3]
B17 DDI3_TXN[3]
B11 DDI3_AUXP
C11 DDI3_AUXN
SOCKET1151
12001-00180100
EDP_TXP[0] E10
EDP_TXN[0] D10
EDP_TXP[1] D9
EDP_TXN[1] C9
EDP_TXN[2] H10
EDP_TXP[2] G10
EDP_TXN[3] G9
EDP_TXP[3] F9
1 HT1
1 HT2
1 HT3
1 HT4
H_DP2VGA_TXN0 <22>
H_DP2VGA_TXP0 <22>
H_DP2VGA_TXN1 <22>
H_DP2VGA_TXP1 <22>
DP to VGA IC
EDP_AUXP D12
EDP_AUXN E12
H_DP2VGA_AUXP <22>
H_DP2VGA_AUXN <22>
EDP_DISP_UTIL D14
H_EDP_DISP_UTIL 1 HT5
VCCIO
EDP_RCOMP M9
H_DP_RCOMP
HR61 1 /1151 2
24.9Ohm
Place Inside CPU Cavity
traace W/S:12/25, max lengtch 200mil
PROC_AUDIO_CLK V3 I
PROC_AUDIO_SDI V2 I
PROC_AUDIO_SDO U1 O
H_HDA_SDI_R
HR1 1 33Ohm 2
S_HDA_SCLK <32>
S_HDA_SDO_R <32>
H_HDA_SDI <32>
HR1 place close CPU
total lengtch <4",max=200
total lengtch >4",max=1000


LGA1151C
LGA1151
<25> H_X16_SL1_RXP0
<25> H_X16_SL1_RXN0
B8
B7
PEG_RXP[0]
PEG_RXN[0]
PEG_TXP[0]
PEG_TXN[0]
A5
A6
H_X16_SL1_TXP0 <25>
H_X16_SL1_TXN0 <25>
<25> H_X16_SL1_RXP1
<25> H_X16_SL1_RXN1
C7
C6
PEG_RXP[1]
PEG_RXN[1]
PEG_TXP[1]
PEG_TXN[1]
B4
B5
H_X16_SL1_TXP1 <25>
H_X16_SL1_TXN1 <25>
<25> H_X16_SL1_RXP2
<25> H_X16_SL1_RXN2
D6
D5
PEG_RXP[2]
PEG_RXN[2]
PEG_TXP[2]
PEG_TXN[2]
C3
C4
H_X16_SL1_TXP2 <25>
H_X16_SL1_TXN2 <25>
<25> H_X16_SL1_RXP3
<25> H_X16_SL1_RXN3
E5
E4
PEG_RXP[3]
PEG_RXN[3]
PEG_TXP[3]
PEG_TXN[3]
D2
D3
H_X16_SL1_TXP3 <25>
H_X16_SL1_TXN3 <25>
<25> H_X16_SL1_RXP4
<25> H_X16_SL1_RXN4
F6
F5
PEG_RXP[4]
PEG_RXN[4]
PEG_TXP[4]
PEG_TXN[4]
E1
E2
H_X16_SL1_TXP4 <25>
H_X16_SL1_TXN4 <25>
<25> H_X16_SL1_RXP5
<25> H_X16_SL1_RXN5
G5
G4
PEG_RXP[5]
PEG_RXN[5]
PEG_TXP[5]
PEG_TXN[5]
F2
F3
H_X16_SL1_TXP5 <25>
H_X16_SL1_TXN5 <25>
<25> H_X16_SL1_RXP6
<25> H_X16_SL1_RXN6
H6
H5
PEG_RXP[6]
PEG_RXN[6]
PEG_TXP[6]
PEG_TXN[6]
G1
G2
H_X16_SL1_TXP6 <25>
H_X16_SL1_TXN6 <25>
<25> H_X16_SL1_RXP7
<25> H_X16_SL1_RXN7
J5
J4
PEG_RXP[7]
PEG_RXN[7]
PEG_TXP[7]
PEG_TXN[7]
H2
H3
H_X16_SL1_TXP7 <25>
H_X16_SL1_TXN7 <25>
<25> H_X16_SL1_RXP8
<25> H_X16_SL1_RXN8
K6
K5
PEG_RXP[8]
PEG_RXN[8]
PEG_TXP[8]
PEG_TXN[8]
J1
J2
H_X16_SL1_TXP8 <25>
H_X16_SL1_TXN8 <25>
<25> H_X16_SL1_RXP9
<25> H_X16_SL1_RXN9
L5
L4
PEG_RXP[9]
PEG_RXN[9]
PEG_TXP[9]
PEG_TXN[9]
K2
K3
H_X16_SL1_TXP9 <25>
H_X16_SL1_TXN9 <25>
<25> H_X16_SL1_RXP10
<25> H_X16_SL1_RXN10
M6
M5
PEG_RXP[10]
PEG_RXN[10]
PEG_TXP[10]
PEG_TXN[10]
L1
L2
H_X16_SL1_TXP10 <25>
H_X16_SL1_TXN10 <25>
<25> H_X16_SL1_RXP11
<25> H_X16_SL1_RXN11
N5
N4
PEG_RXP[11]
PEG_RXN[11]
PEG_TXP[11]
PEG_TXN[11]
M2
M3
H_X16_SL1_TXP11 <25>
H_X16_SL1_TXN11 <25>
<25> H_X16_SL1_RXP12
<25> H_X16_SL1_RXN12
P6
P5
PEG_RXP[12]
PEG_RXN[12]
PEG_TXP[12]
PEG_TXN[12]
N1
N2
H_X16_SL1_TXP12 <25>
H_X16_SL1_TXN12 <25>
<25> H_X16_SL1_RXP13
<25> H_X16_SL1_RXN13
R5
R4
PEG_RXP[13]
PEG_RXN[13]
PEG_TXP[13]
PEG_TXN[13]
P2
P3
H_X16_SL1_TXP13 <25>
H_X16_SL1_TXN13 <25>
<25> H_X16_SL1_RXP14
<25> H_X16_SL1_RXN14
T6
T5
PEG_RXP[14]
PEG_RXN[14]
PEG_TXP[14]
PEG_TXN[14]
R2
R1
H_X16_SL1_TXP14 <25>
H_X16_SL1_TXN14 <25>
<25> H_X16_SL1_RXP15
<25> H_X16_SL1_RXN15
U5
U4
PEG_RXP[15]
PEG_RXN[15]
PEG_TXP[15]
PEG_TXN[15]
T2
T3
H_X16_SL1_TXP15 <25>
H_X16_SL1_TXN15 <25>
VCCIO
/1151
HR52 1
2 H_PEG_RCOMP
24.9Ohm
PLACE HR52 Inside CPU Cavity
Trace W/S: 12/15 mils, Length: 400mils
L7
PEG_RCOMP
<30> H_DMI_RXP0
<30> H_DMI_RXN0
Y3
Y4
DMI_RXP[0]
DMI_RXN[0]
DMI_TXP[0]
DMI_TXN[0]
AC2
AC1
H_DMI_TXP0 <30>
H_DMI_TXN0 <30>
<30> H_DMI_RXP1
<30> H_DMI_RXN1
AA4
AA5
DMI_RXP[1]
DMI_RXN[1]
DMI_TXP[1]
DMI_TXN[1]
AD3
AD2
H_DMI_TXP1 <30>
H_DMI_TXN1 <30>
<30> H_DMI_RXP2
<30> H_DMI_RXN2
AB4
AB3
DMI_RXP[2]
DMI_RXN[2]
DMI_TXP[2]
DMI_TXN[2]
AE2
AE1
H_DMI_TXP2 <30>
H_DMI_TXN2 <30>
<30> H_DMI_RXP3
<30> H_DMI_RXN3
AC4
AC5
DMI_RXP[3]
DMI_RXN[3]
DMI_TXP[3]
DMI_TXN[3]
AF2
AF3
H_DMI_TXP3 <30>
H_DMI_TXN3 <30>
SOCKET1151
12001-00180100

1.page7~8 page13~17---change DDR3 to DDR4
2.change page88 add vddq enable schematic
3.page74 add GP07,GP56,GP57
4.update power schematic from power rd neil_zhang
5.page52 delete USB78 header, change USB910 to header from box
6.page78 change KBMS to KBMS_USB78
7.page89 delete PCHLED2,PCHLED3
8.add page116~117,add EPF036 control RGB LED
9.modify page116,delete MSBUS of EPF side
10.change 24M clk to another pin on chipset side
11.modify KBMS power
12.modify front base power from +5V_USB_P78 to +5V_USB_P910
13.XR721 pin 1 э钡 P_VDDQ_COMP_10 PR573 pin 2 э钡 VDDQ_EN
14.USB3.1_EC1 骓ъ
15.add L1D3
16.OR291 pin 2 э钡 +3VSB add PUMP_FAN page118 SIO IC 俱琐骓褪 (remove DSW, remove 6791 co-lay单)
17.follow chipset demo,箇痤SR182~185 箇痤SC191 SD200~202

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