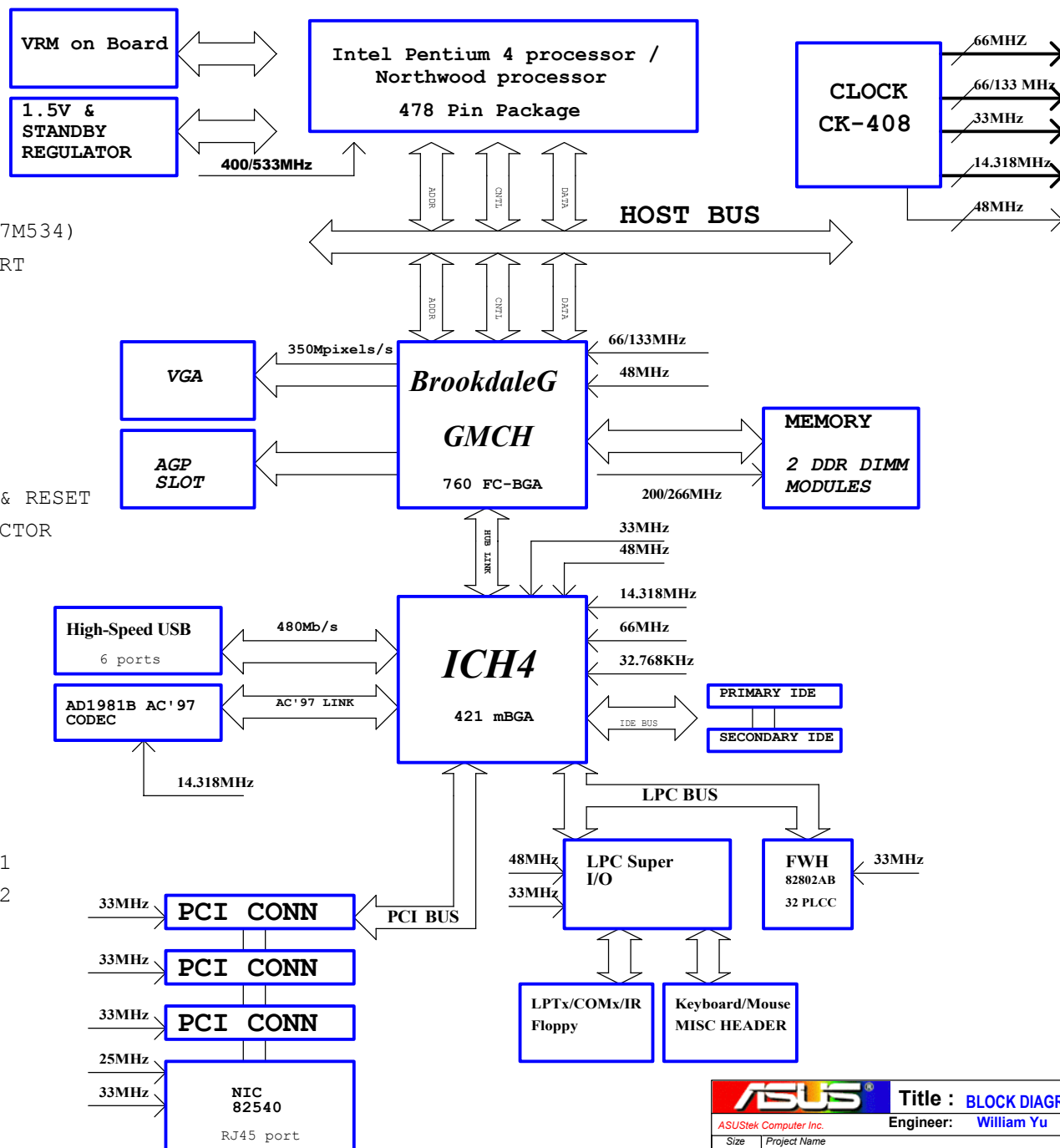


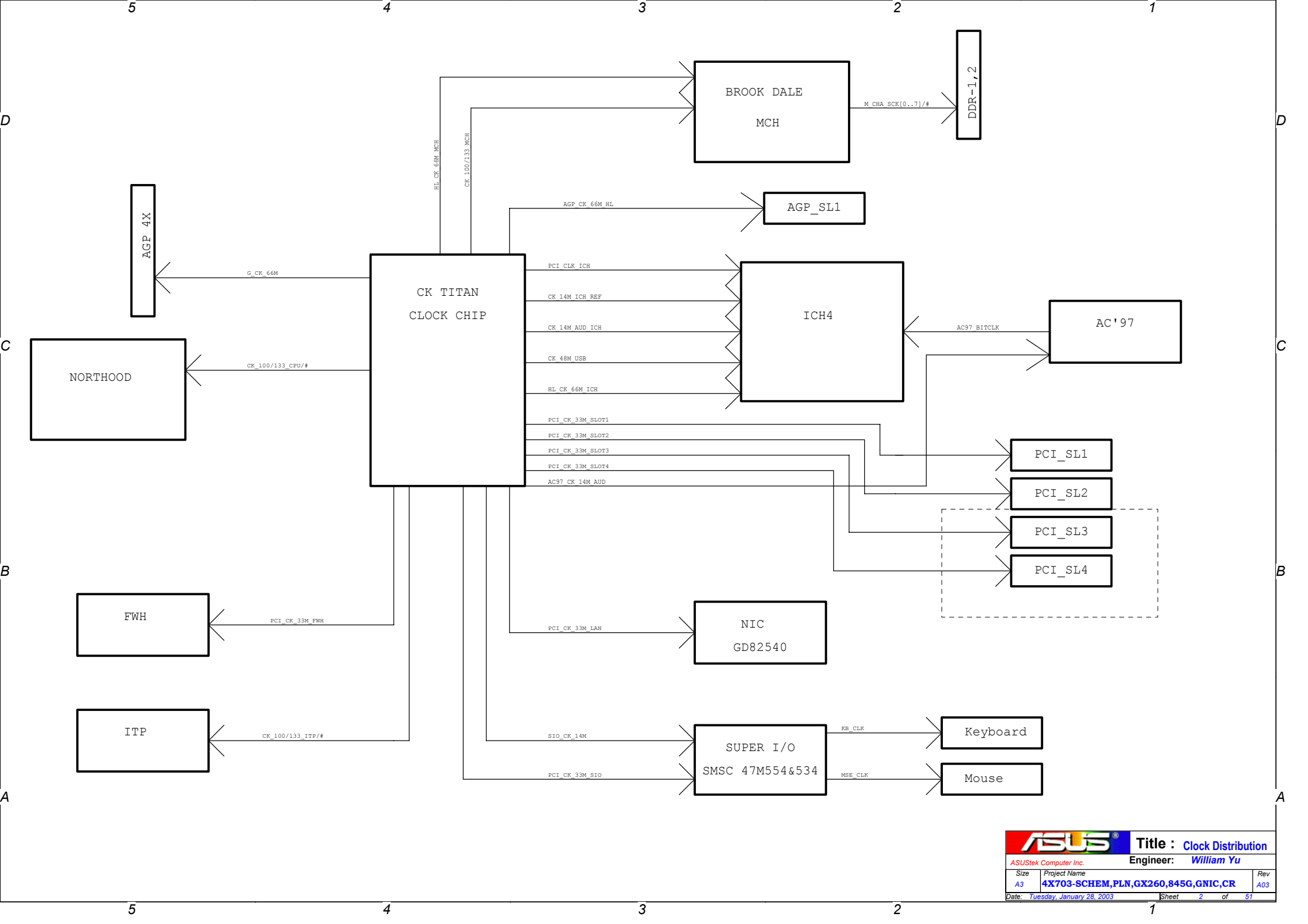
RAINIER-CR PROJECT

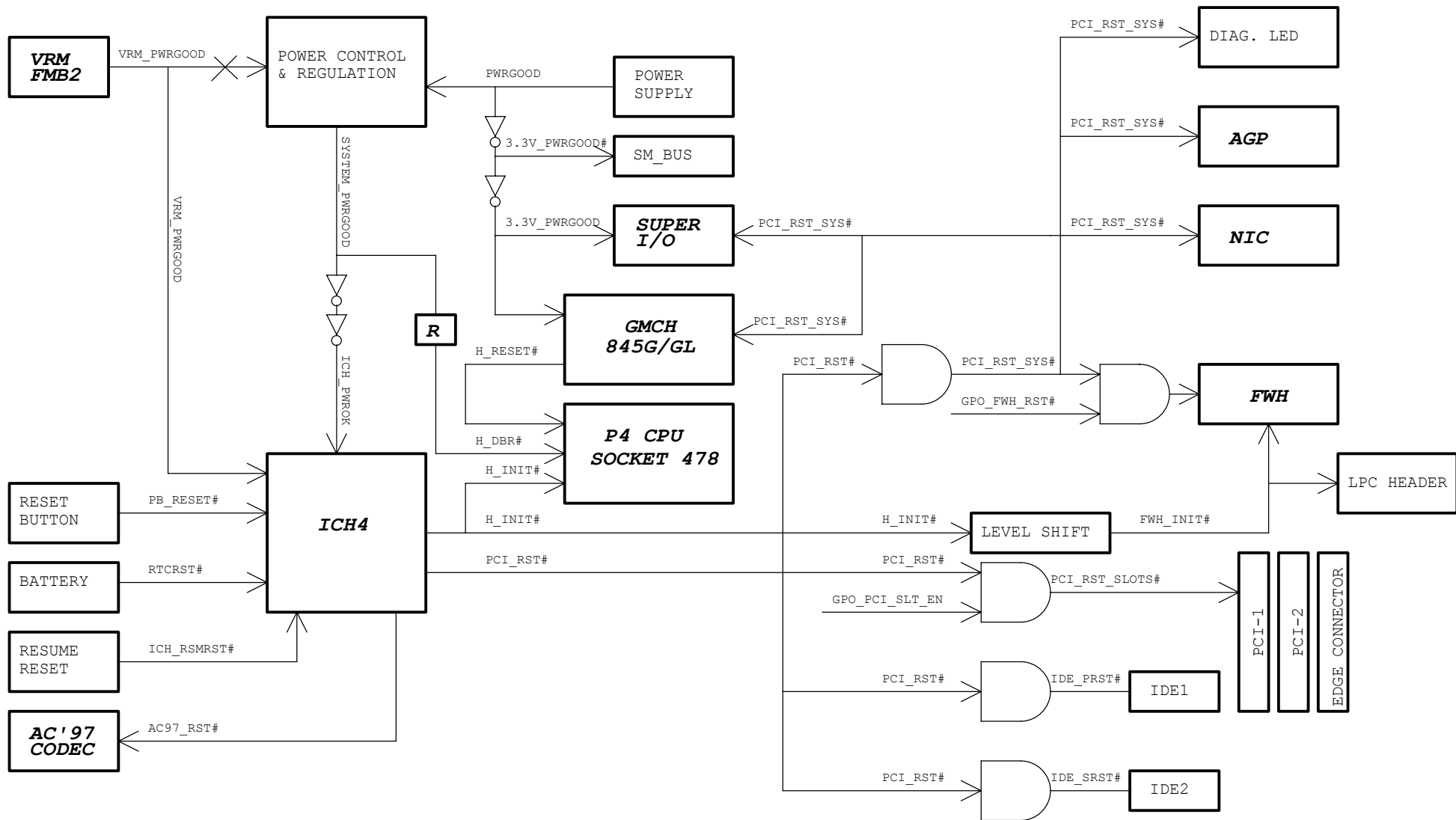
Rev.A03 : 01/28/2003

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Page 5.	POWER FLOW
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Page 36.	FLOPPY
Page 37.	DIAGLED
Page 38.	FRONTPANEL
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Page 40.	POWER CONNECTOR
Page 41.	CPUCORE
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Page 46.	BATTERY
Page 47.	EMI
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Page 49.	H-RISER
Page 50.	BOM OPTION 1
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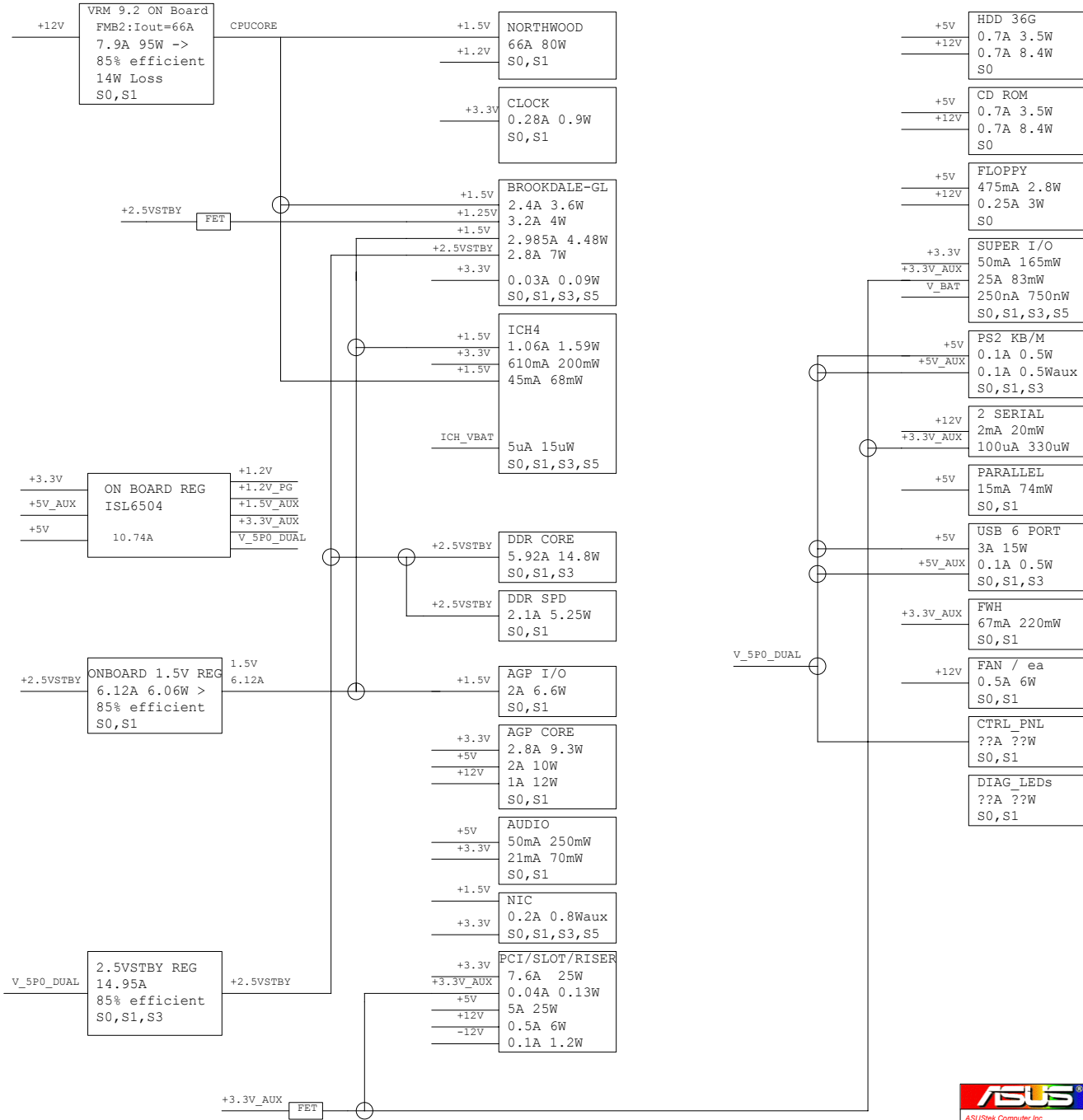


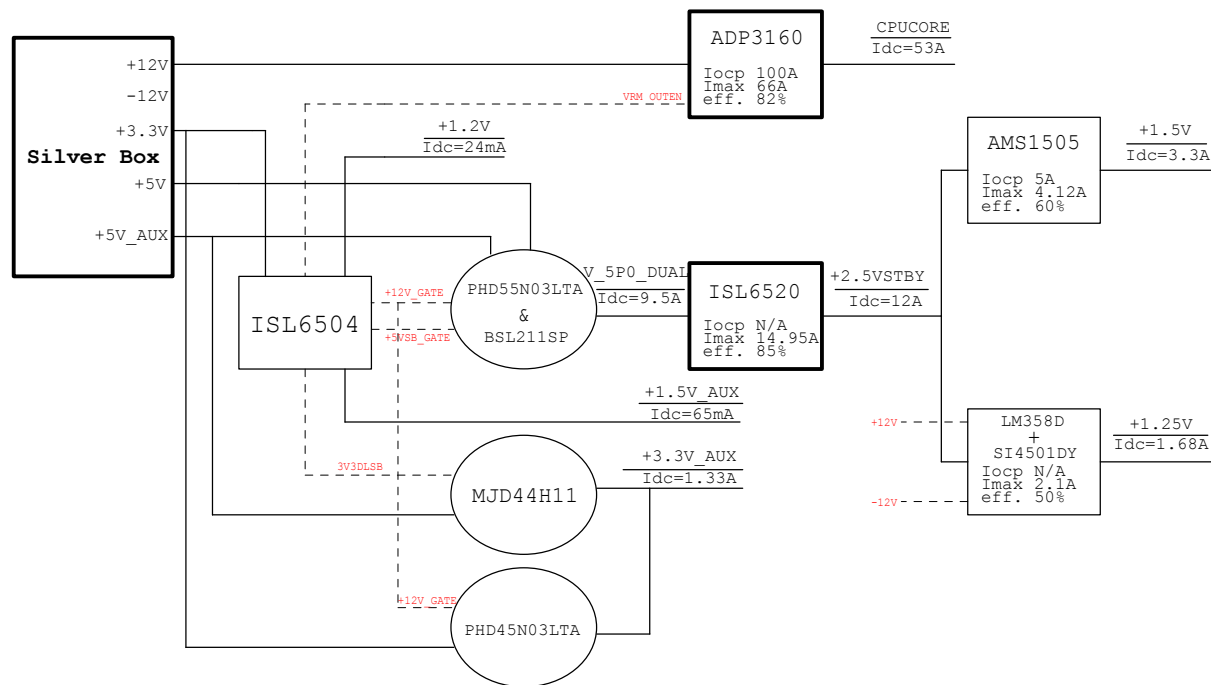
POWER SUPPLY
FOR JAZZ
200W TOTAL
80W SHARED

+12V	10A 120W
+5V	12.6A 63W
+3.3V	10A 33W
+5V_AUX	2A 10W
-5V	POWER SUPPLY
-12V	POWER SUPPLY

3.0 Volt
BATTERY
CR2032
220 mAh
20mA Max

VBAT	0.25uA 0.75uW
ICH_VBAT	5uA 15uW





Note: 1. Reference document: Brookdale-G Chipset Platform Design Guide, REV. 1.5, page 250, Fig. 14-1.

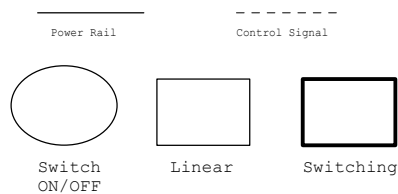
2. There is no power sequencing requirements for 3.3V and 1.5V rails on Intel ICH4, page 260.

3. V5REF must be powered up before or simultaneously to 3.3V and there must not exist a difference of more than two volts between the planes. This criterion had been down by power supply vender, page 260.

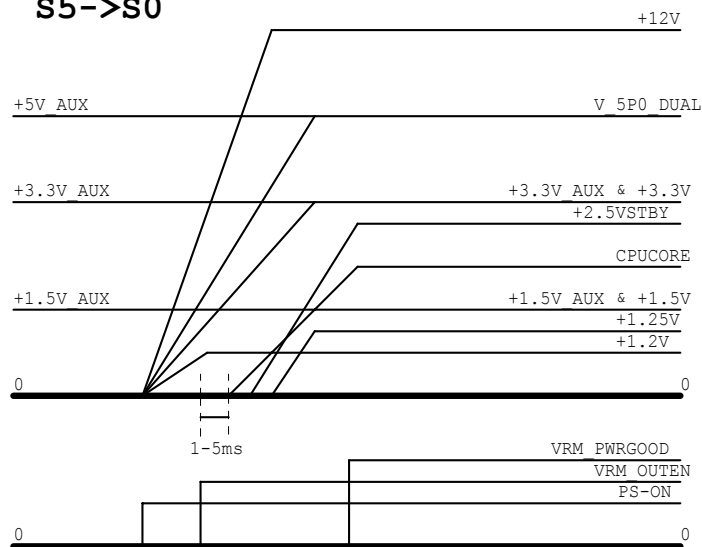
4. Imax is mean to peak current refered to power distribution on page 4.

5. Idc is mean to the sustain current , and is 80% of Imax current.

6. Iocp is 1.5~2.0 times of Imax.



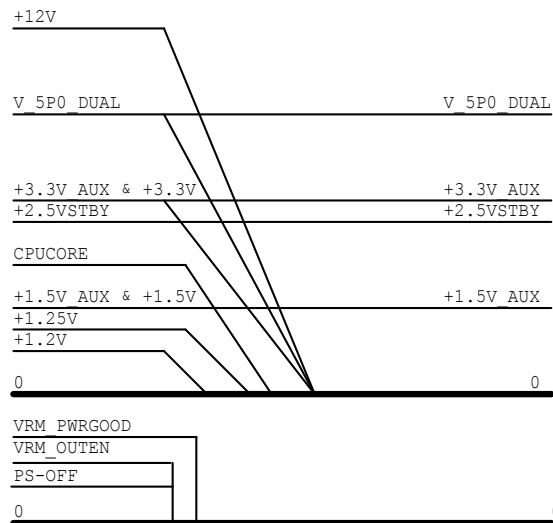
S5->S0



1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms

2.VRM_OUTEN rises after the voltage across 90% of its specified value

S0->S3

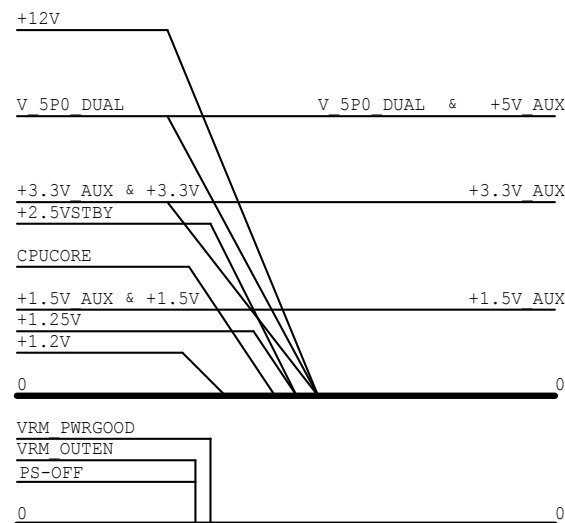


S0:Windows Running +12V,V_5P0_DUAL,+3.3V,+3.3V_AUX,+2.5VSTBY,CPUCORE,+1.5V,+1.5V_AUX,+1.25V,+1.2V existed

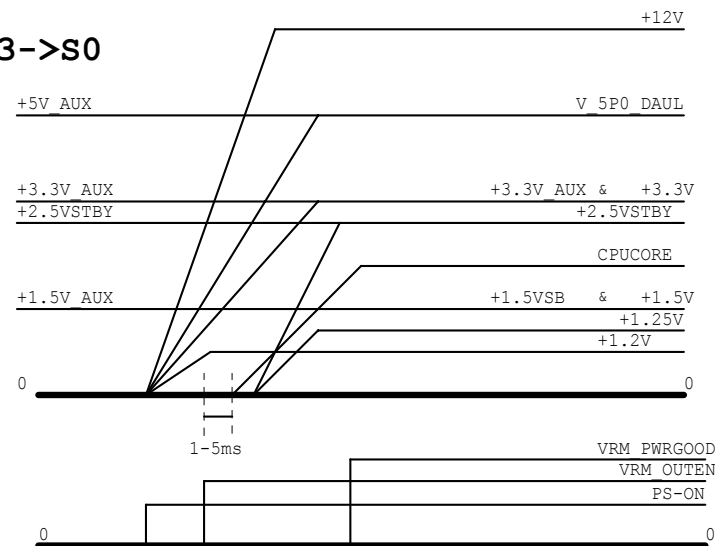
S3:Windows Standby v_5P0_DUAL,+3.3V_AUX,+1.5V_AUX,+2.5VSTBY existed

S5:AC Power On Only +5V_AUX,+3.3V_AUX,+1.5V_AUX existed

S0->S5



S3->S0



1.CPUCORE must rise after the voltage across 90% of +1.2V,andthe interval is within 1-5ms

2.VRM_OUTEN rises after the voltage across 90% of its specified value



Title : POWER SEQUENCE

ASUSTek Computer Inc.

Engineer: William Yu

Size

A

Project Name

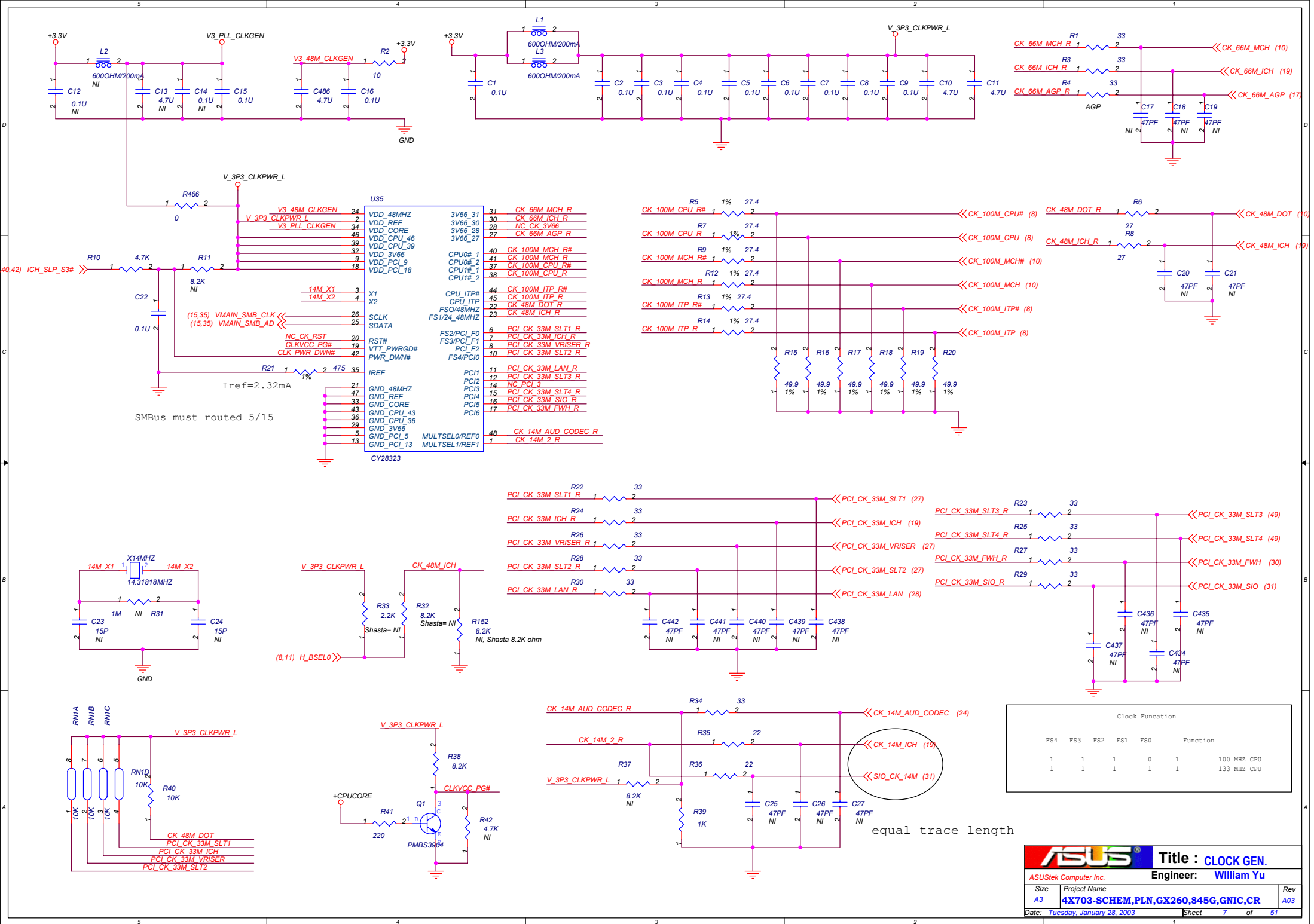
4X703-SCHEM,PLN,GX260,845G,GNIC,CR

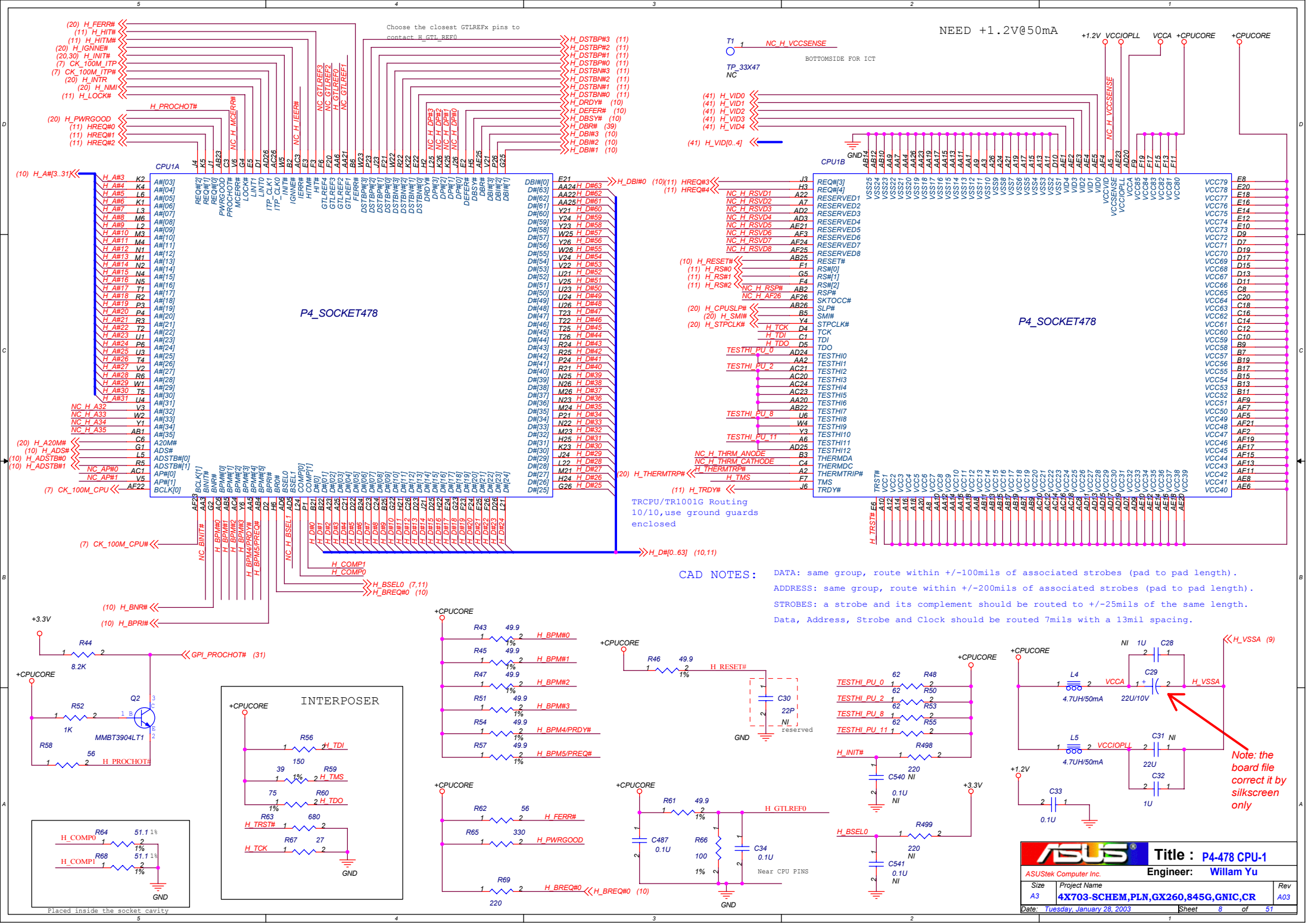
Rev

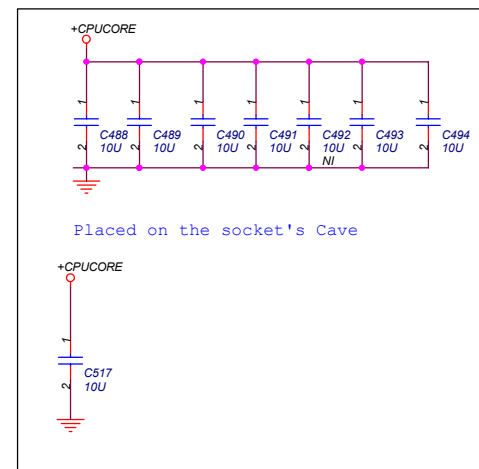
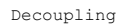
A03

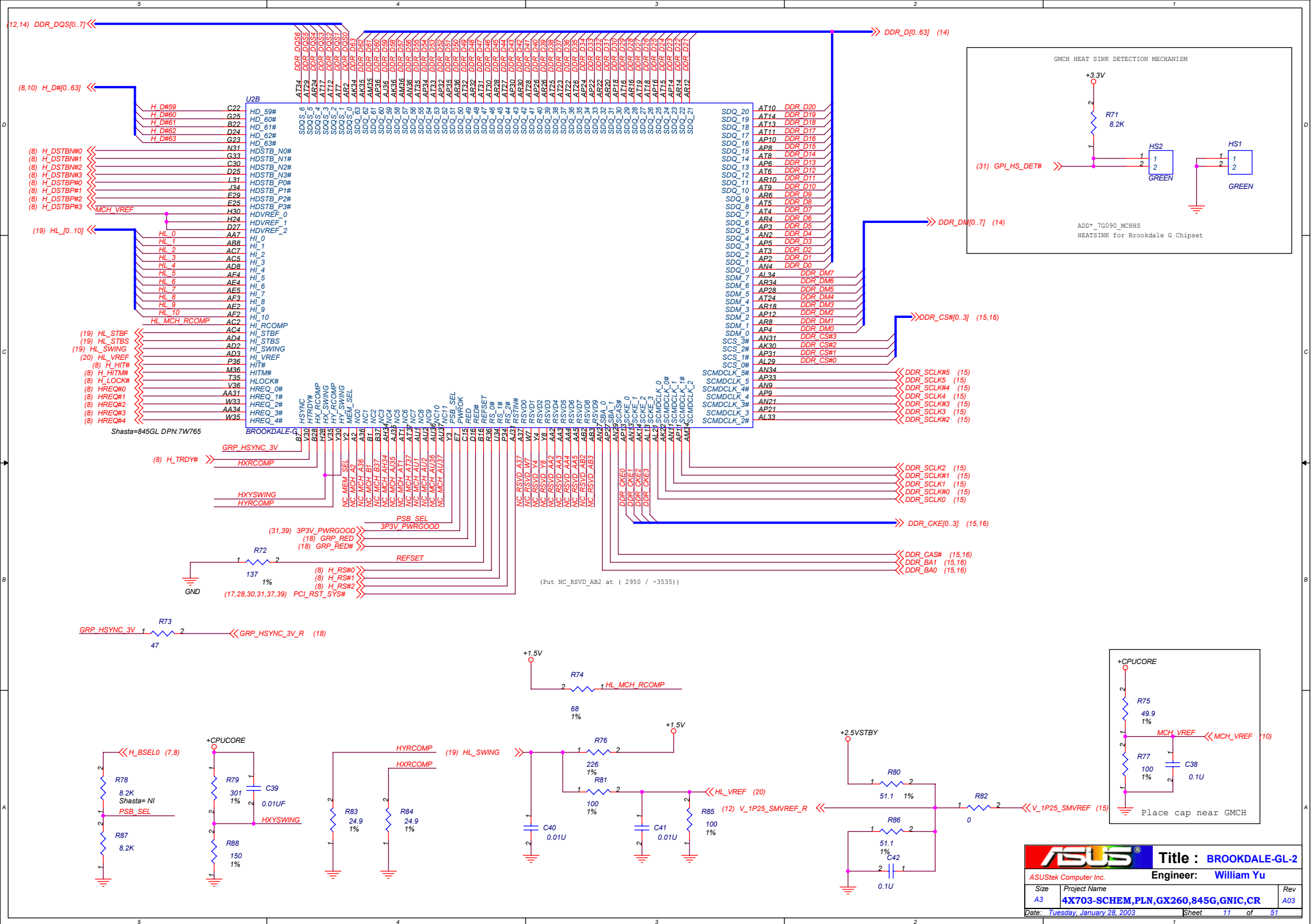
Date: Tuesday, January 28, 2003

Sheet 6 of 51

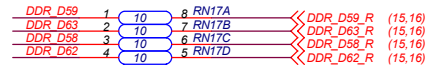
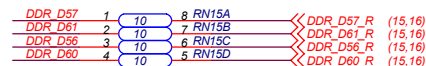
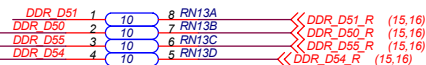
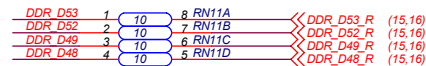
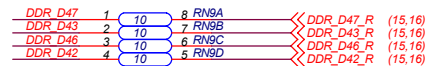
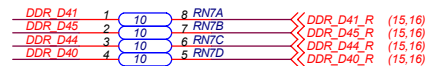
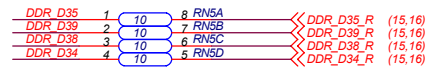
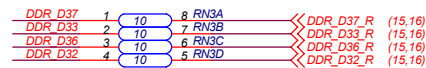
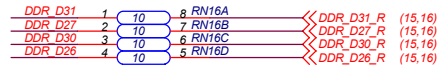
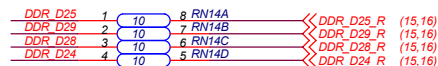
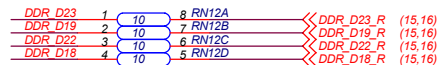
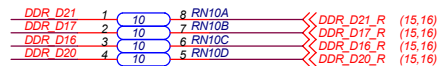
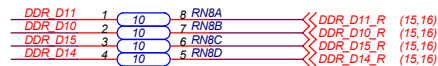
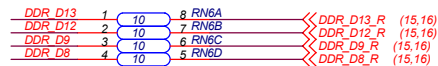
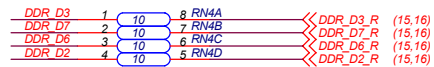
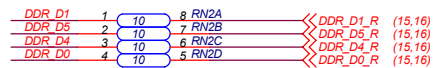




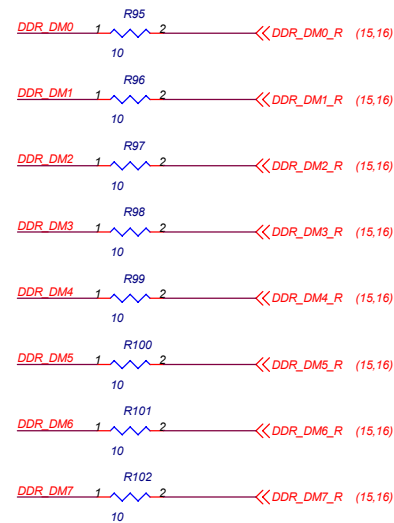




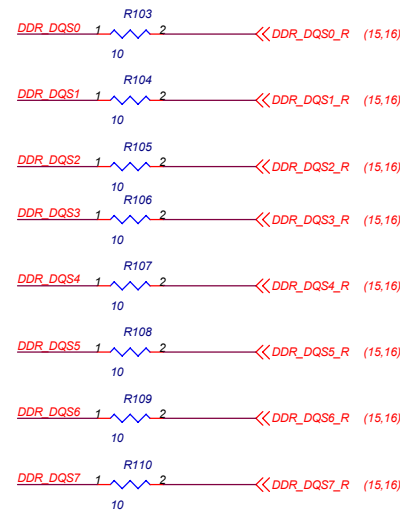
(11) DDR_D[0..63] >>



(11) DDR_DM[0..7] >>



(11,12) DDR_DQS[0..7] >>



DDR_MAB1 (12,16)
DDR_MAB2 (12,16)
DDR_MAB4 (12,16)
DDR_MAB5 (12,16)



CAD NOTES:DDR Channel Referencing Stack-up :

Layer 1 = Signal , Layer 2=Ground Flood, Layer 3 = Ground, Layer 4=Power/Signal

Data : MDD[0..63] , DM[0..7] , DDQS[0..8] = 5mil width, Spacing: MCH to 1st DIMM = 12mil, within DIMM pin field = 7mil min.

DIMM to DIMM = 12mil, 2nd DIMM to Rtt = 7mil min.

Control : DCS#[0..3] , CKE[0..3] = 5 mil width , Spacing : MCH to 1st DIMM =12 mil , within DIMM pin field = 7 mil min.

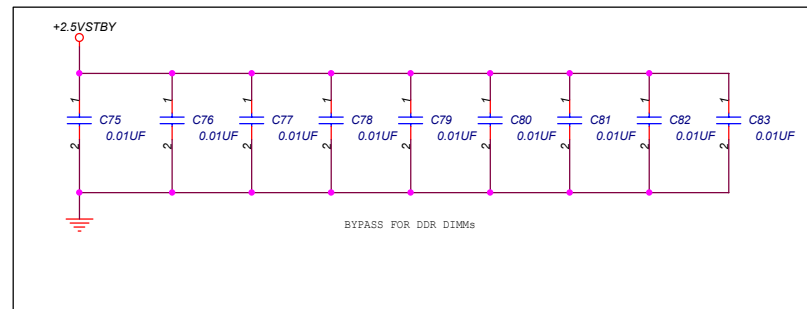
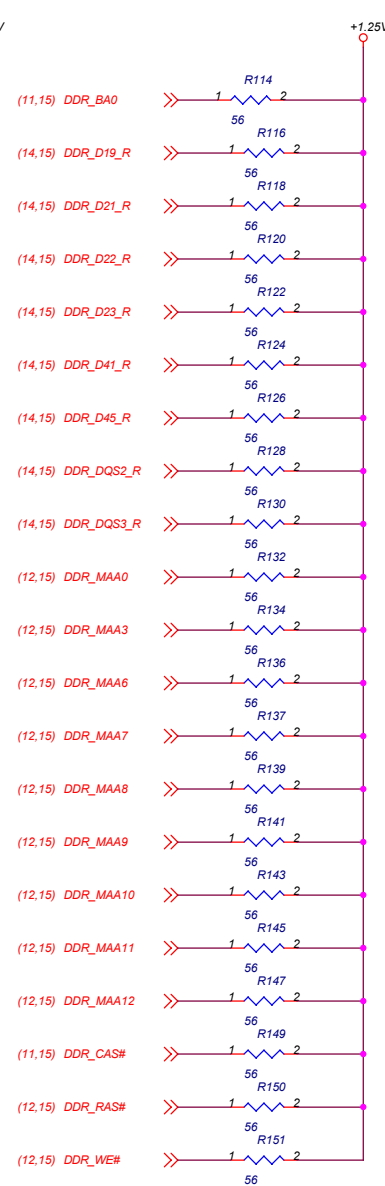
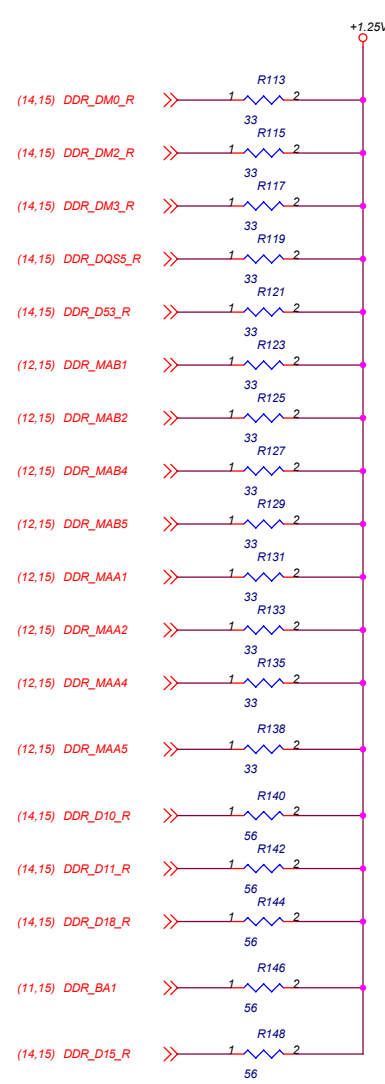
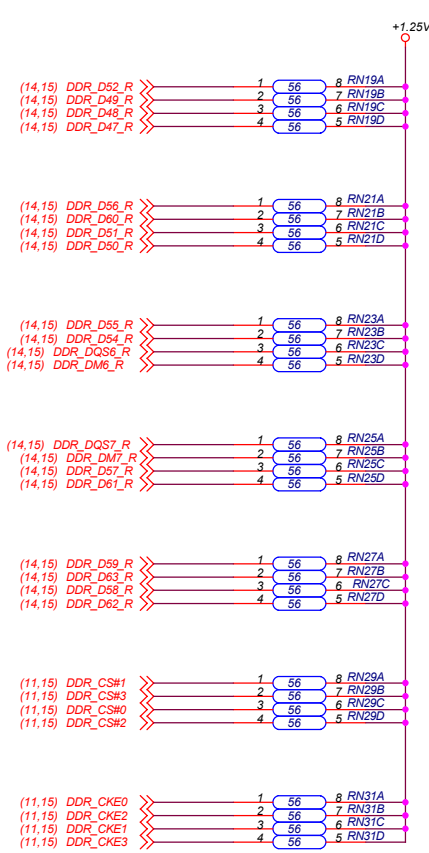
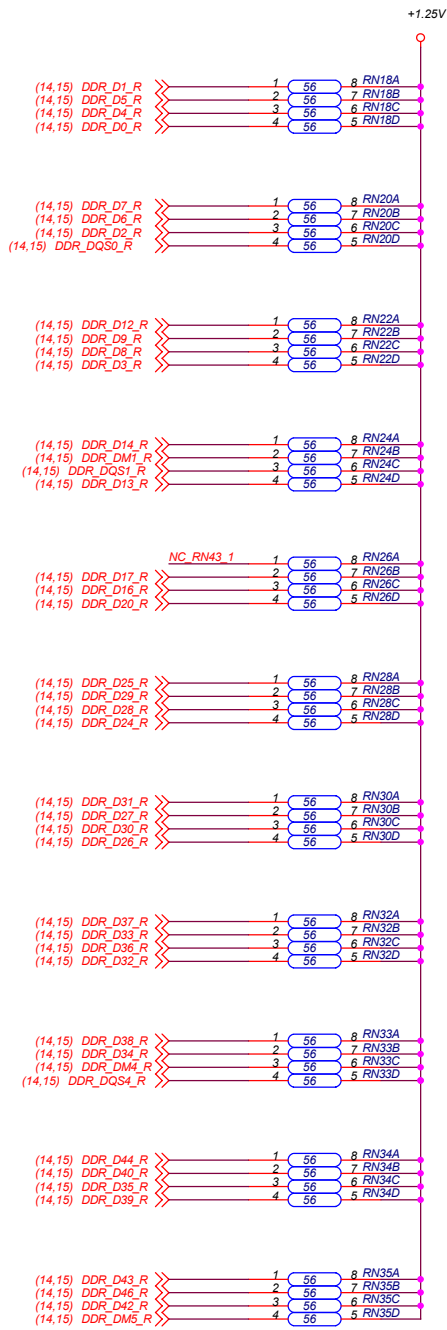
DIMM to DIMM = 12 mil, 2nd DIMM to Rtt = 7 mil min.

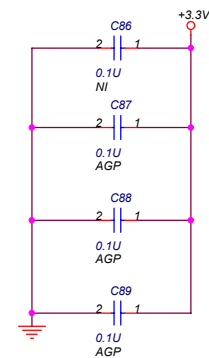
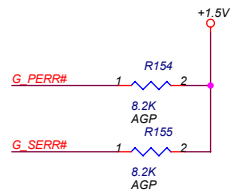
Command : MAA[0..12] , MAB[1..4] , SBNA[0..1] , SCAS# , SRAS# , SWE# = 5 mil width , Spacing : MCH to 1st DIMM = 12 mil , within DIMM pin field = 7 mil min. DIMM to DIMM = 12 mil , 2nd DIMM to Rtt = 7 mil min.

Clock : DCLK[0..5] , DCLK#[0..5] = 5 mil width , 7 mil Differential trace spacing , Group spacing = 20 mil. point to point.

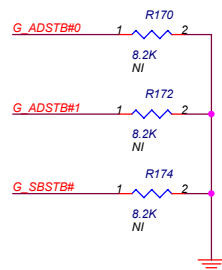
Clock signal Mapping : DCLK[0..2] , DCLK#[0..2] = DIMM0 ; DCLK[3..5] , DCLK#[3..5] = DIMM1

Feedback : VTT_REF = 5 mil width , 12 mil spacing , Group spacing = 20 mil. point to point.

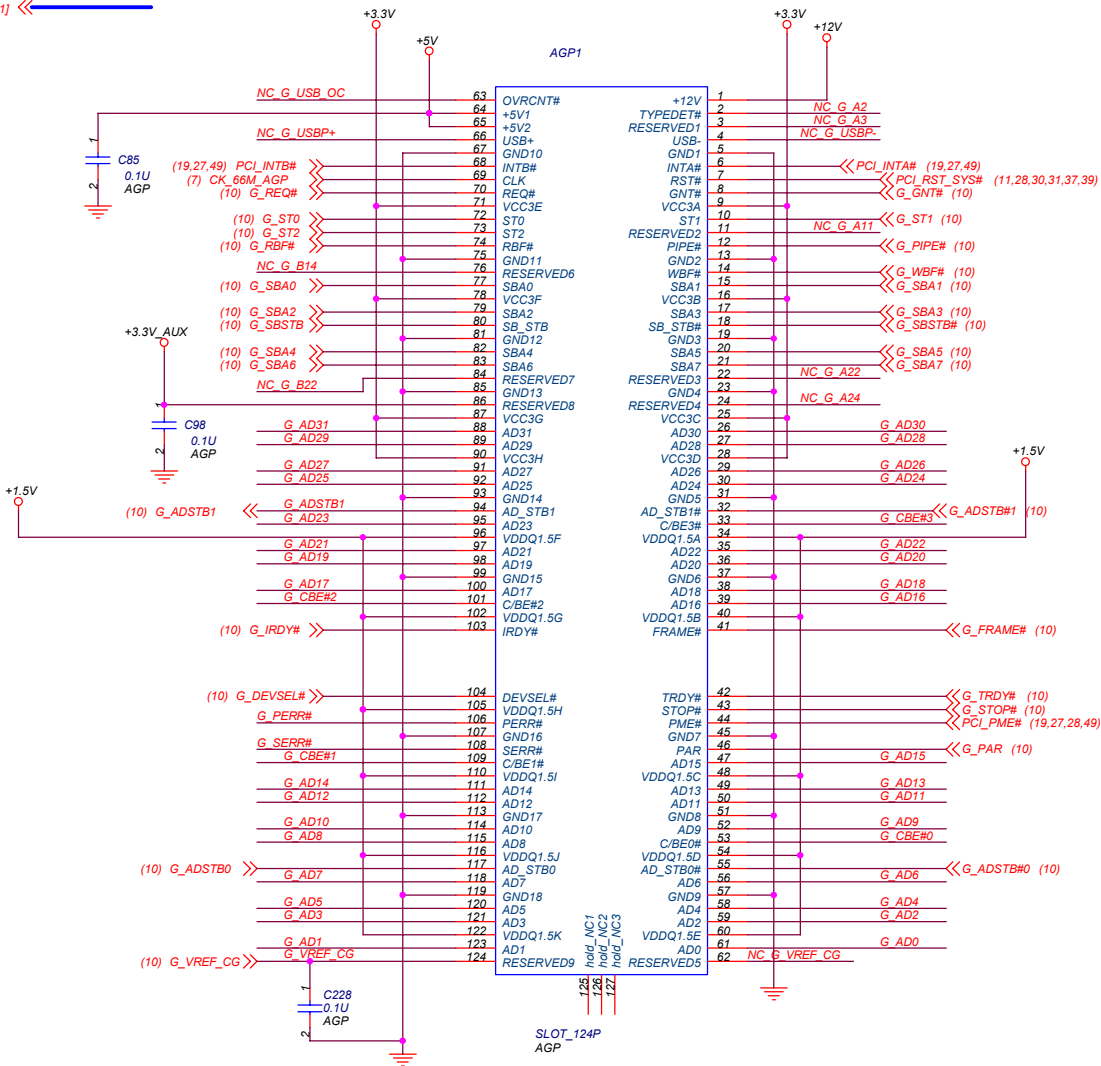




Place cap near AGP 3.3V pins

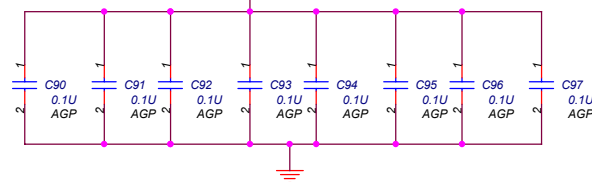


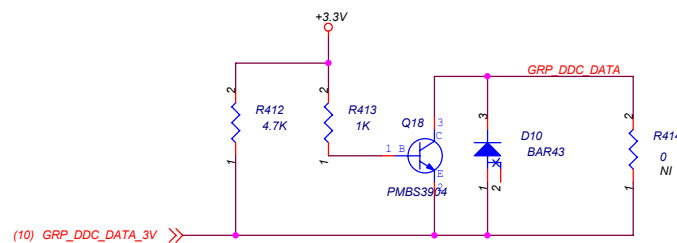
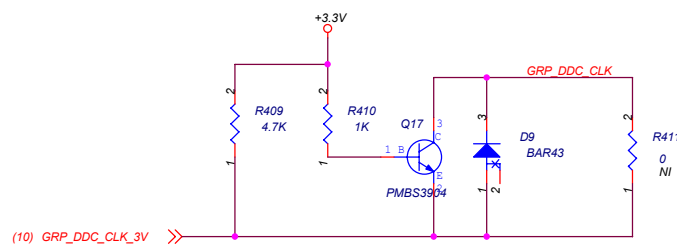
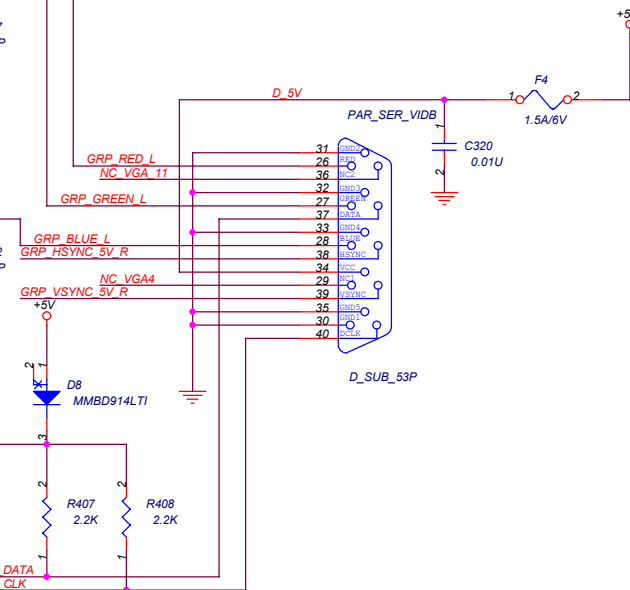
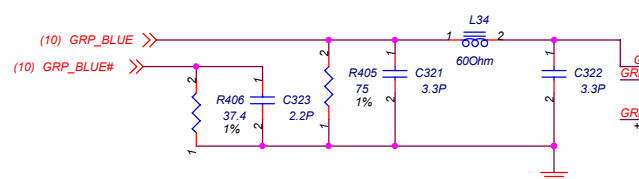
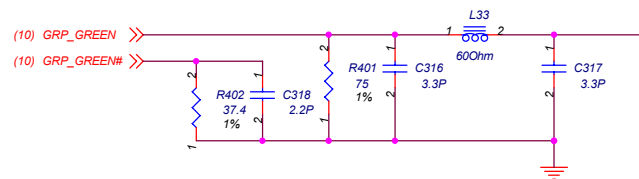
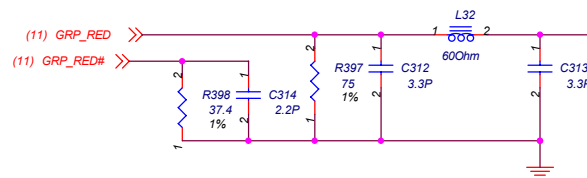
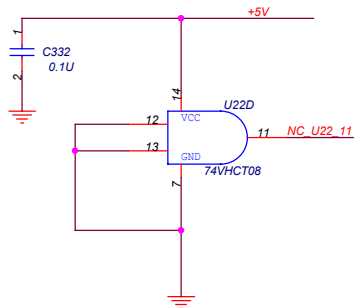
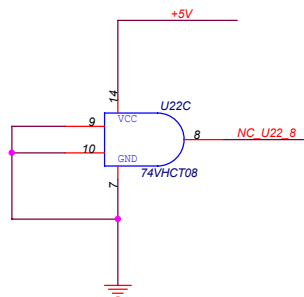
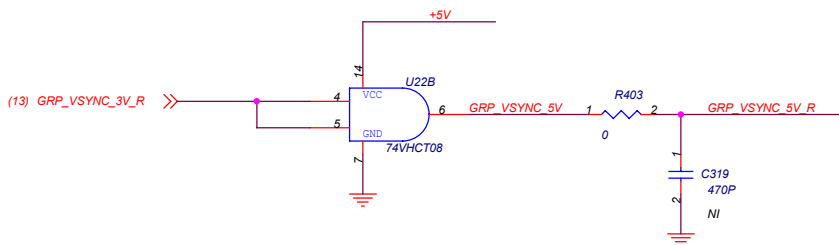
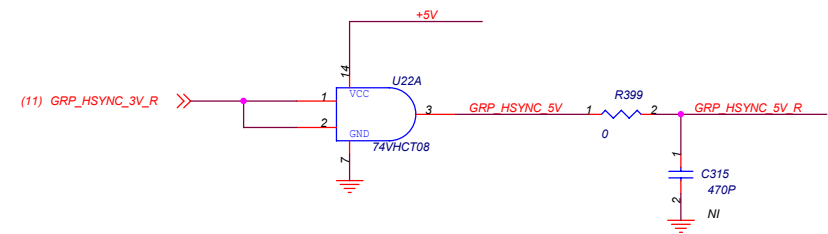
(10) G_AD[0..31] <<

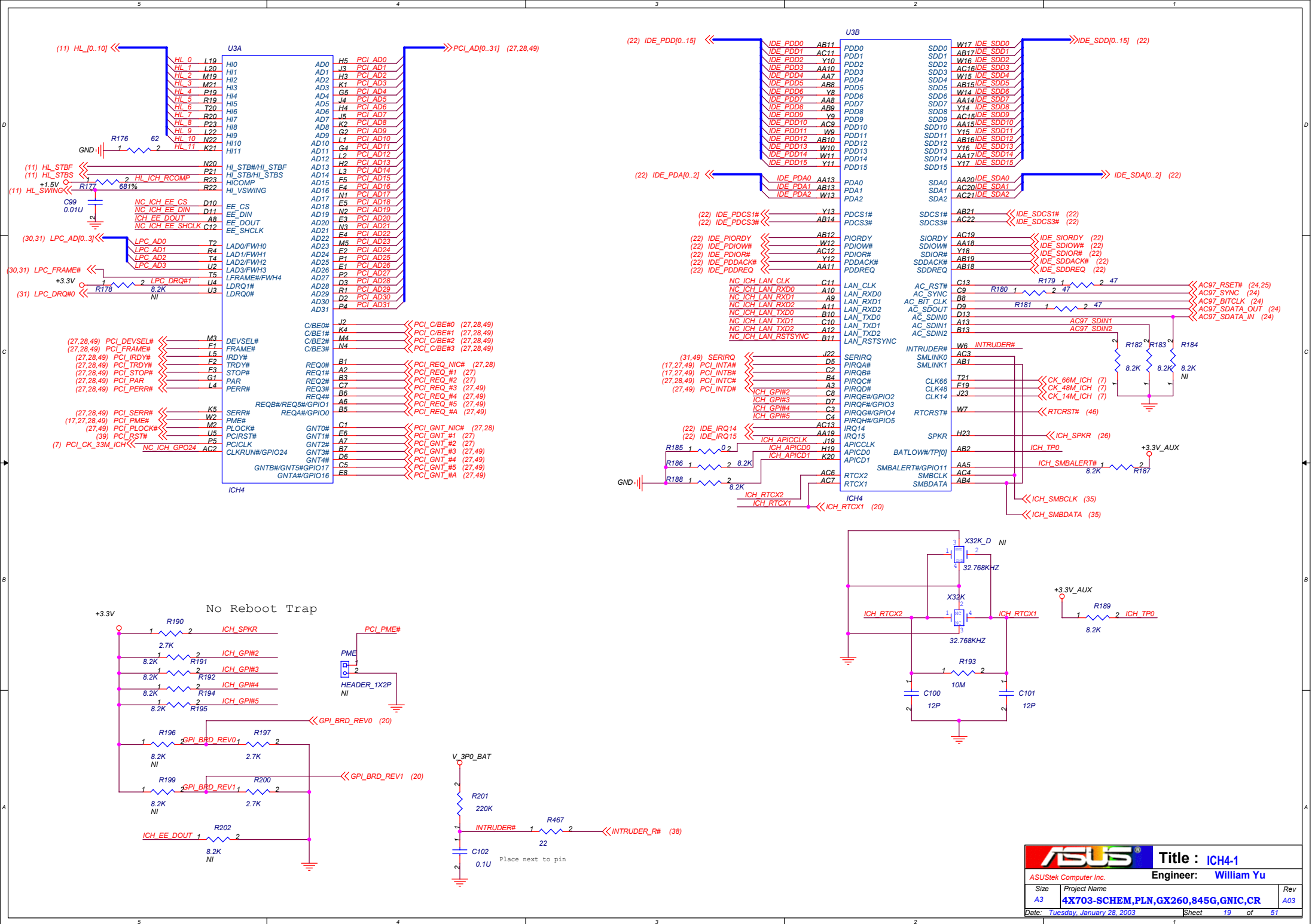


SLOT_124P
AGP

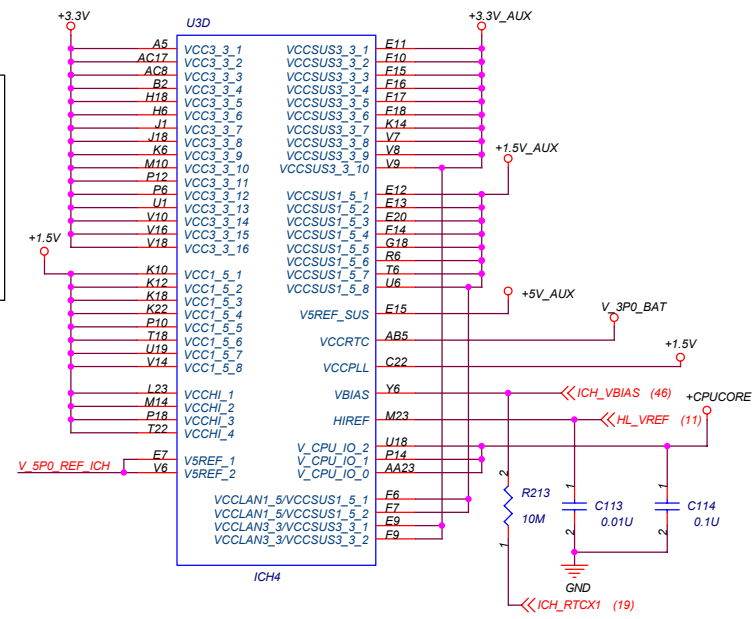
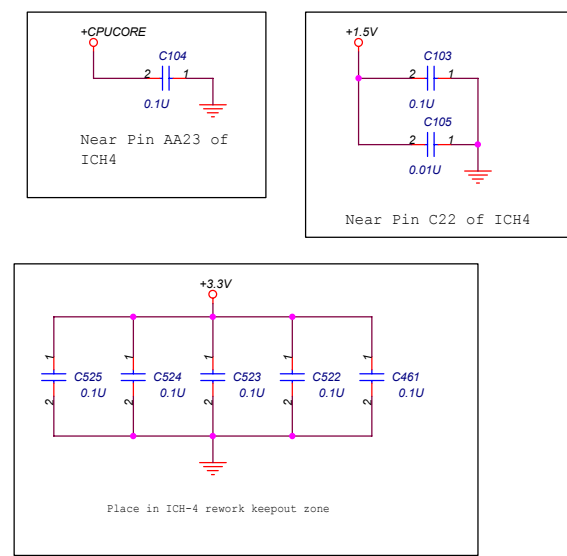
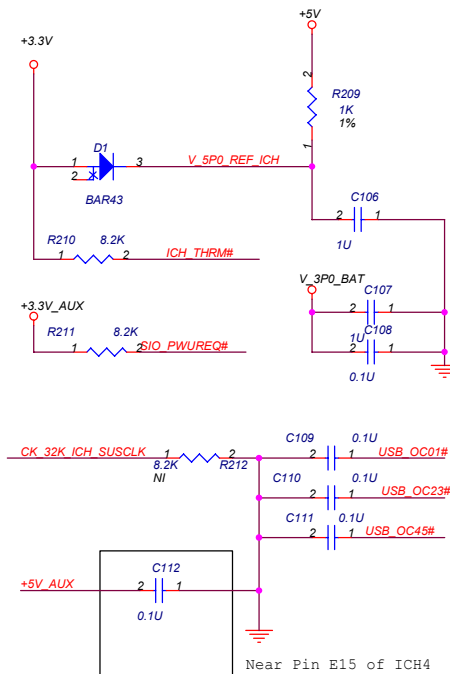
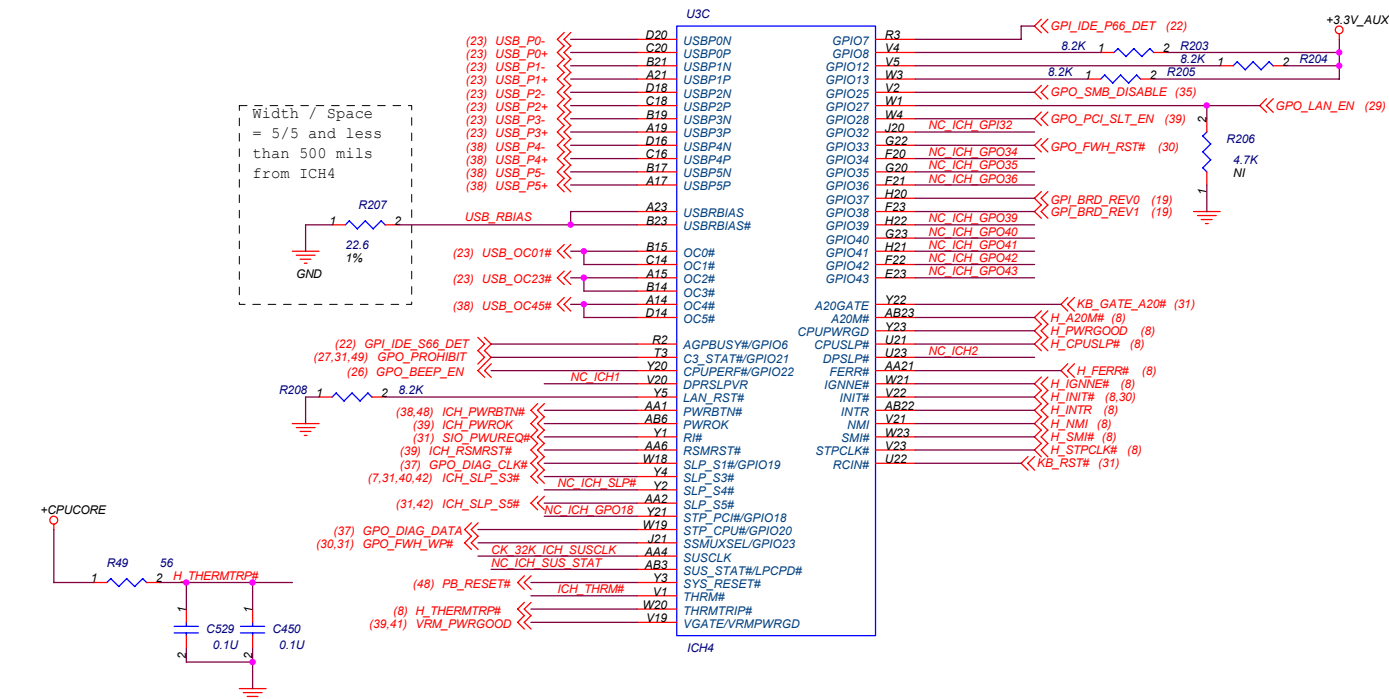
Place cap near AGP_VDDQ pins

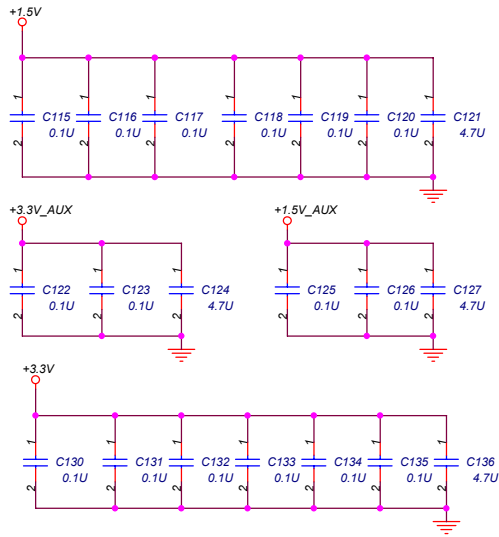




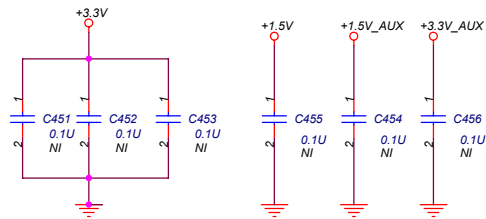


USB0-/USB0+, USB1-/USB1+, USB2-,USB2+,USB3-/USB3+ trace width = 7.5 mils and space = 7.5 mils , the length = 17" max.
USB4-/USB4+, USB5-/USB5+ trace width = 7.5 mils and space = 7.5 mils , the length = 6" max.

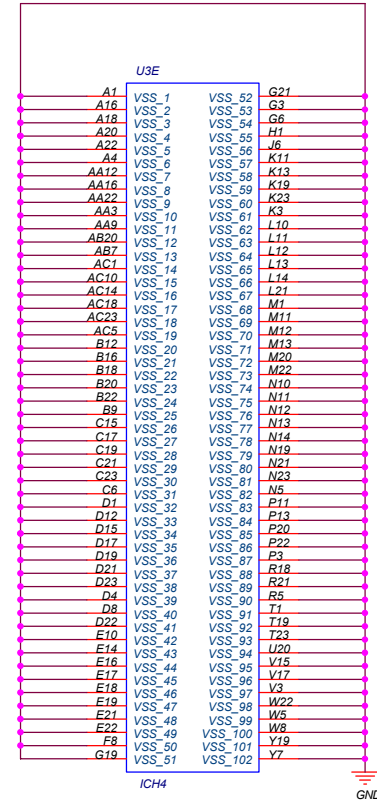


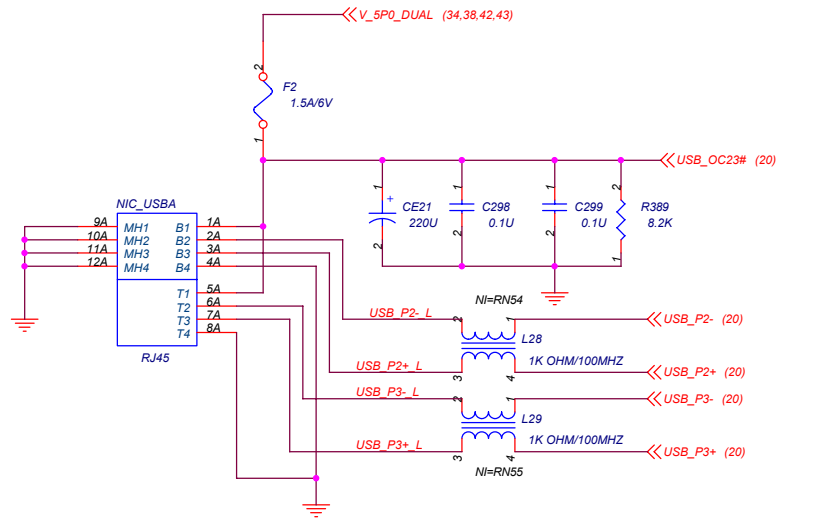


BY PASS CAP AROUND ICH4



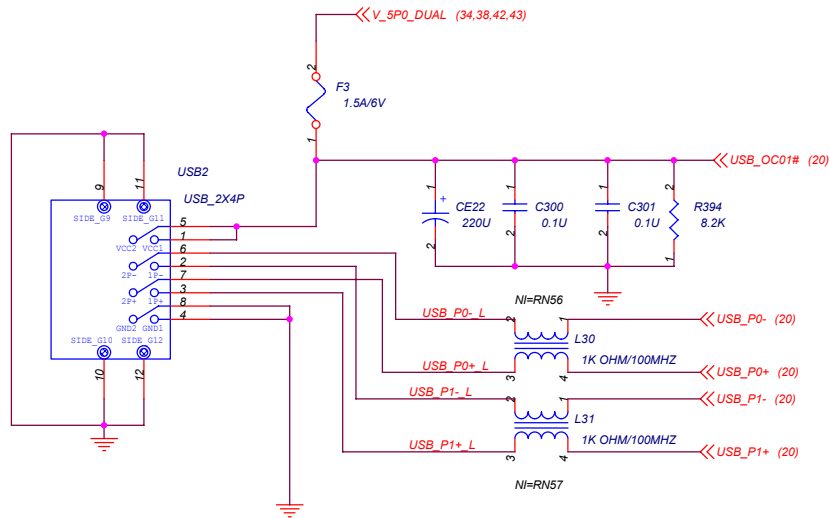
BACKSIDE CAPS OF ICH4





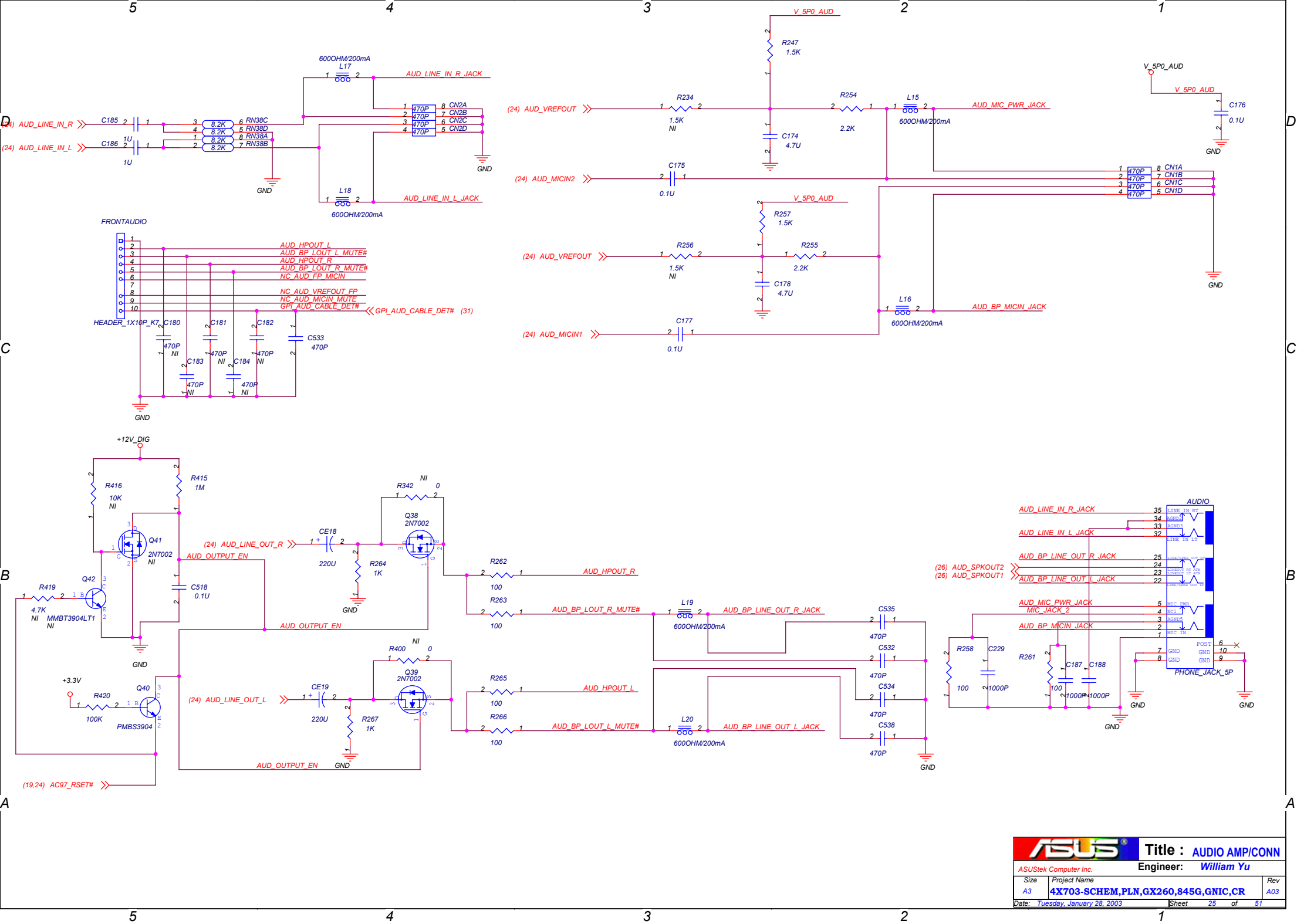
USB P2- L 1 0 2 RN54A USB P2-
USB P2+ L 3 0 4 RN54B USB P2+

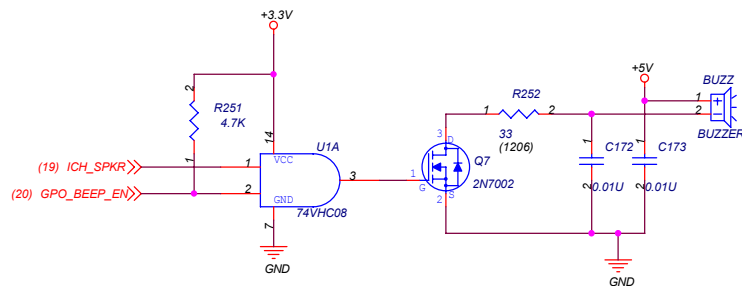
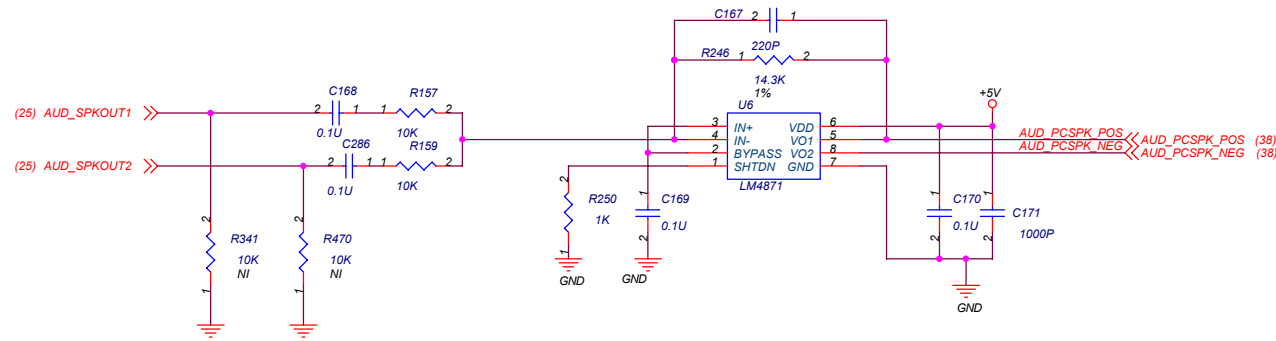
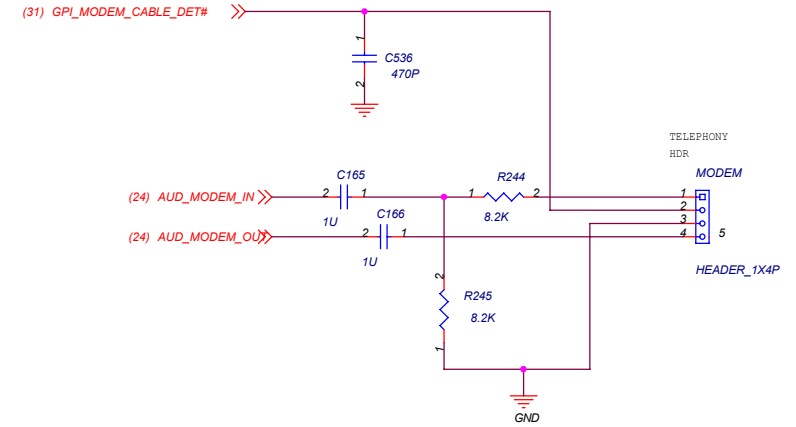
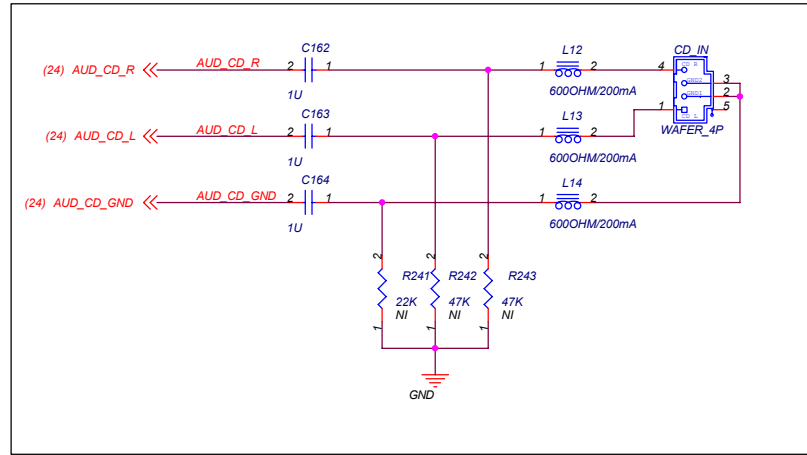
USB P3- L 1 0 2 RN55A USB P3-
USB P3+ L 3 0 4 RN55B USB P3+



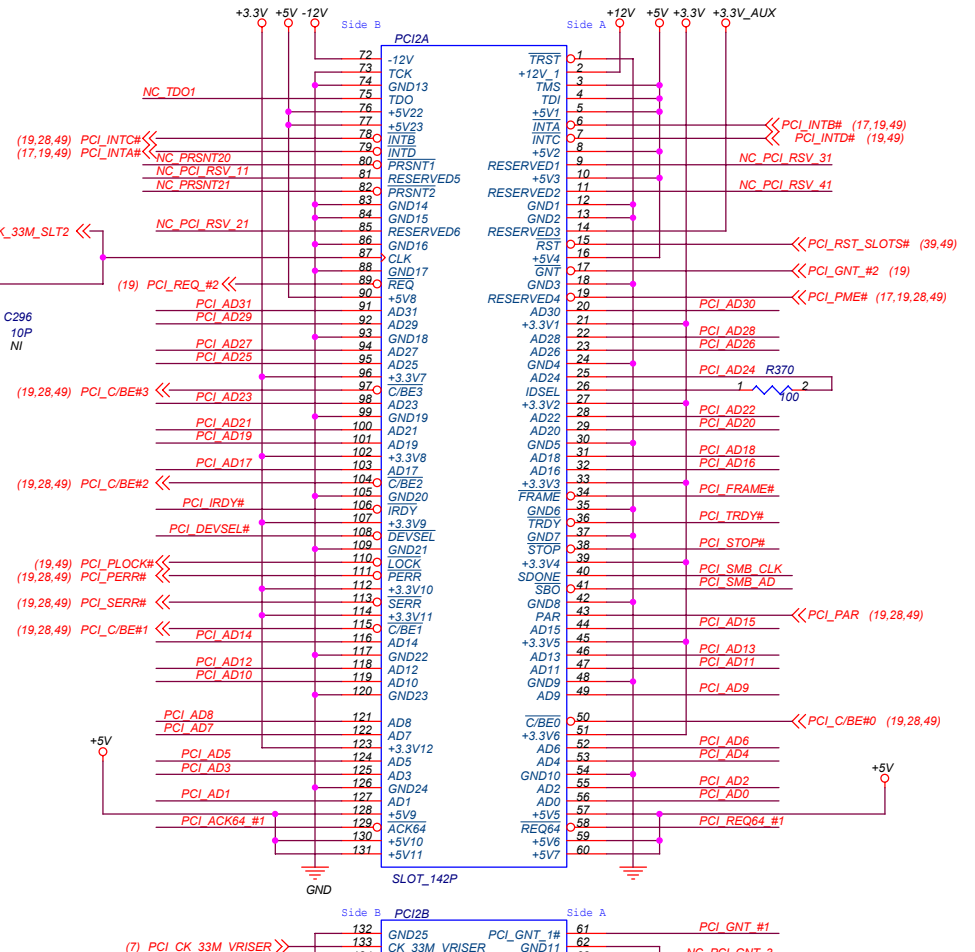
USB P0- L 1 0 2 RN56A USB P0-
USB P0+ L 3 0 4 RN56B USB P0+

USB P1- L 1 0 2 RN57A USB P1-
USB P1+ L 3 0 4 RN57B USB P1+

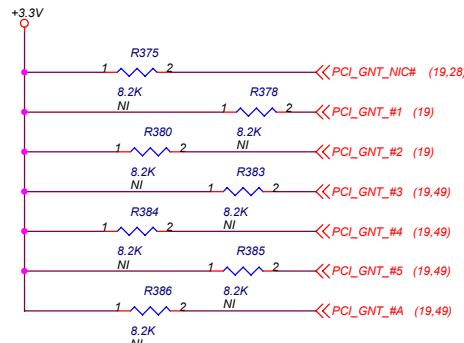




(19,28,49) PCI_AD[0..31] <<————



The schematic shows the +5V supply rail connected to a network of resistors. The resistors are labeled R373, R374, R376, R377, R379, R381, and R382. Each resistor is connected to a signal line, and the signal name is shown in parentheses next to the resistor value. The signal names are PCI_REQ_NIC#, PCI_REQ_#1, PCI_REQ_#2, PCI_REQ_#3, PCI_REQ_#4, PCI_REQ_#5, and PCI_REQ_#A.



PCI DEVICE	PCI REQ/GNT	PCI IDSEL	PCI Clocks	INTA on device mapped to INTx	Device Number
PCI SLOT 1	REQ/GNT 1	PCI_AD23	PCI_CLK0	INT ABCD	07
PCI SLOT 2	REQ/GNT 2	PCI_AD24	PCI_CLK1	INT BCDA	08

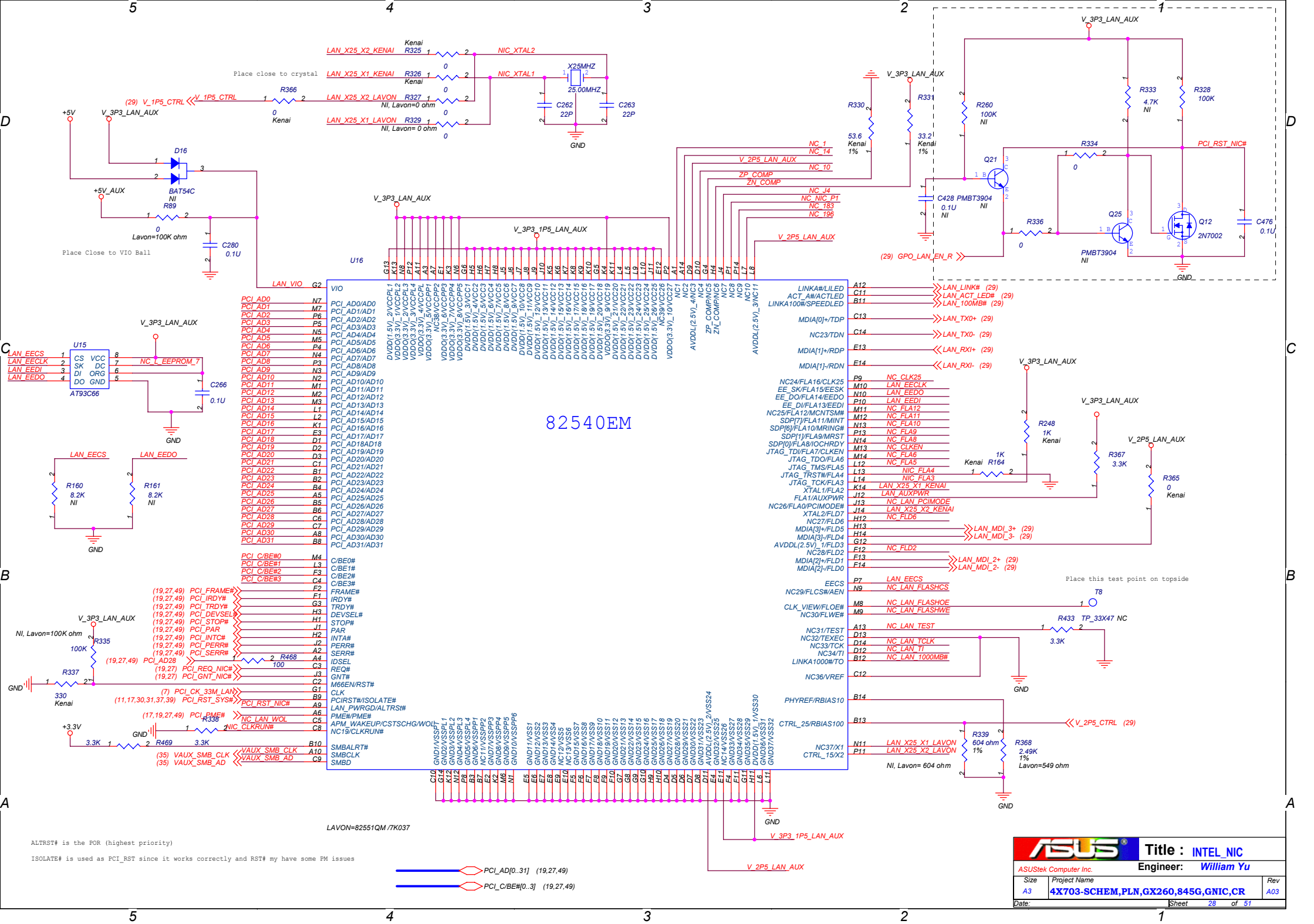


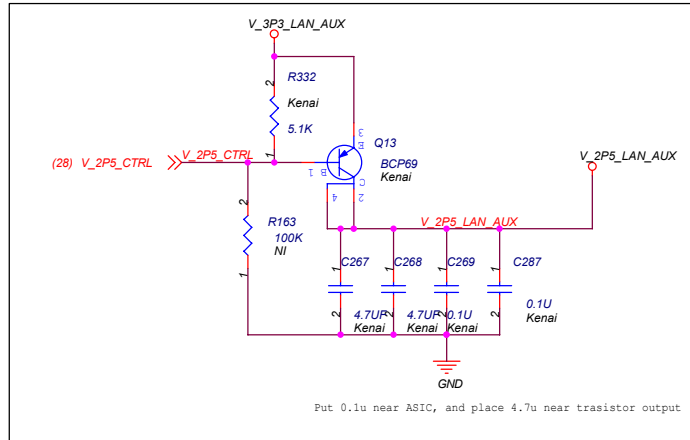
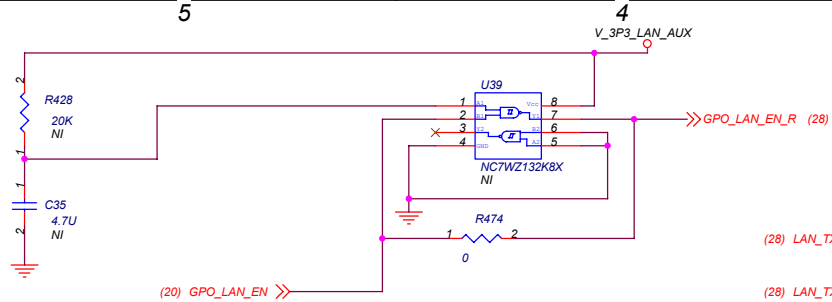
Engineer: William Yu

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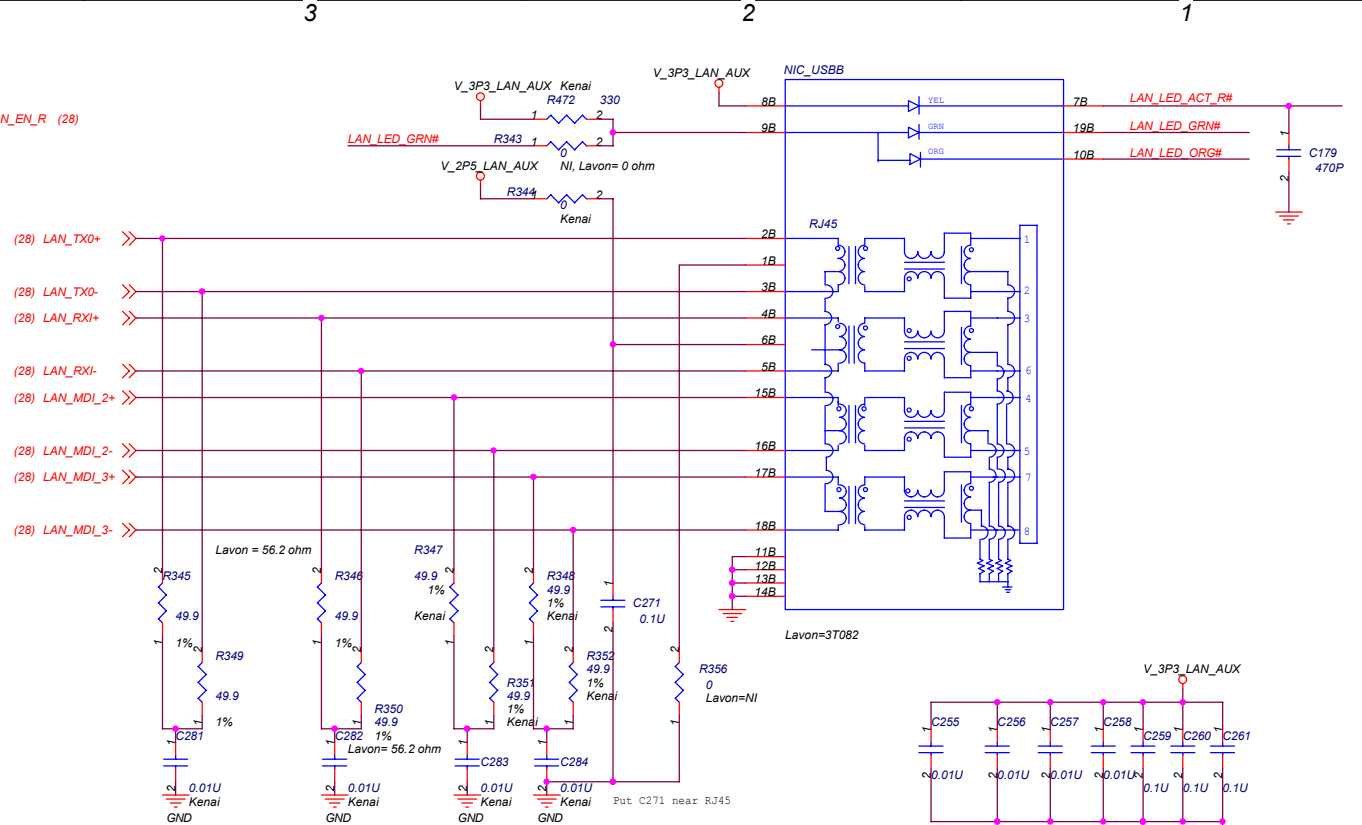
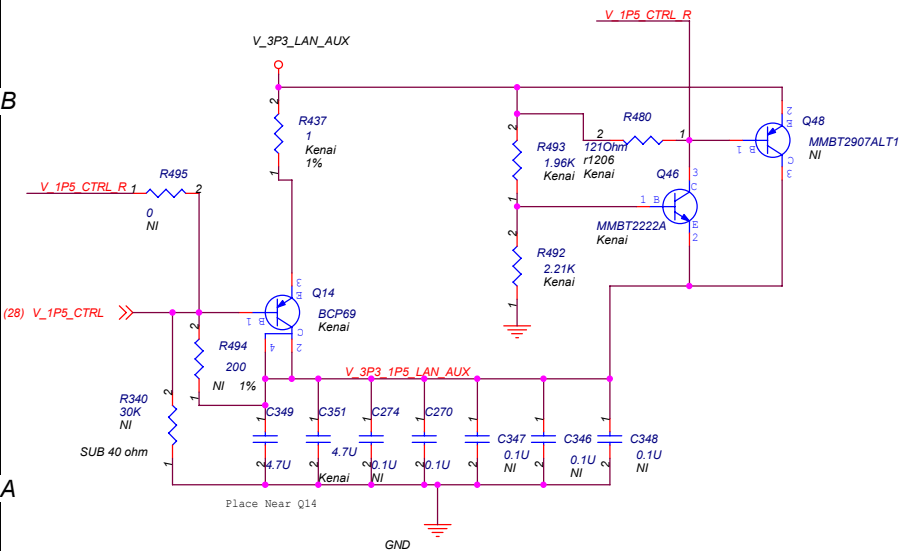
R	
	E1

CAD NOTE : PCI trace width / space = 5/7 , the ICH4 to 1st PCI length = 4" to 10" , 1st to 2rd PCI length = 1" , 2rd to 3th PCI length = 1" .

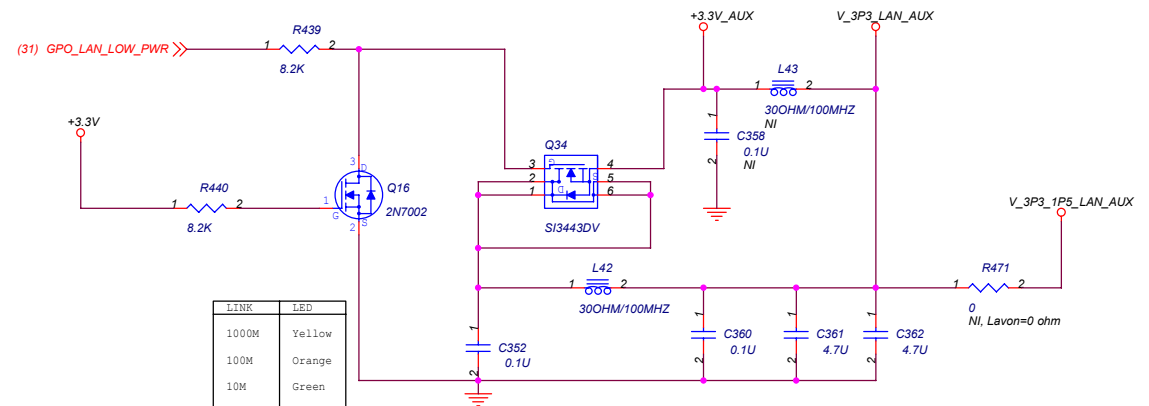




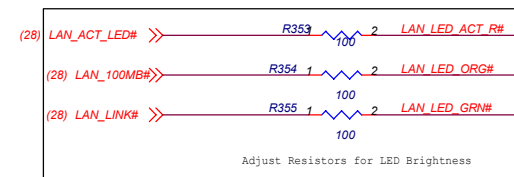
Find a smaller package fro the 1 ohm 1/2 W resistor

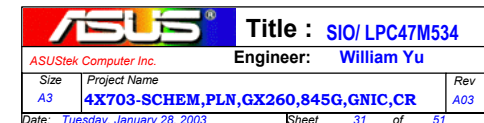


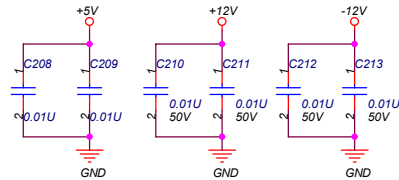
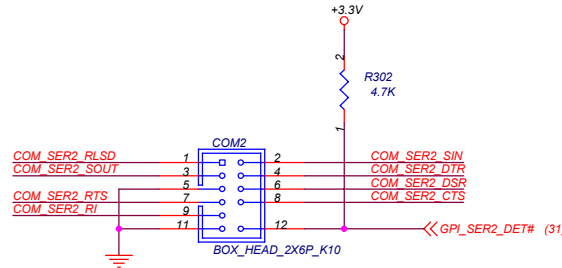
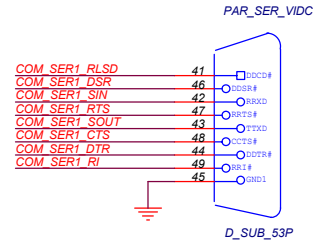
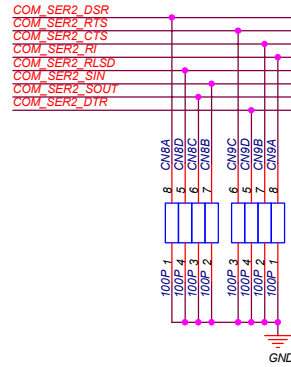
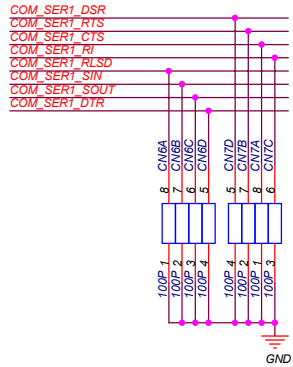
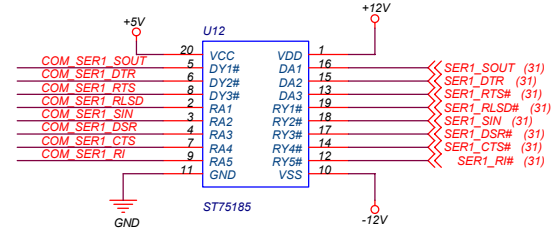
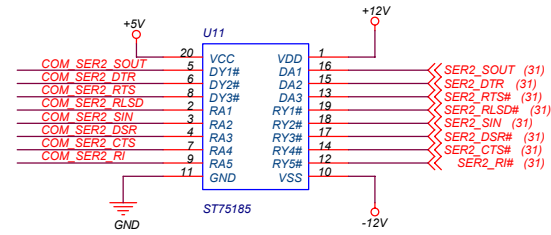
Termination Close to ASIC

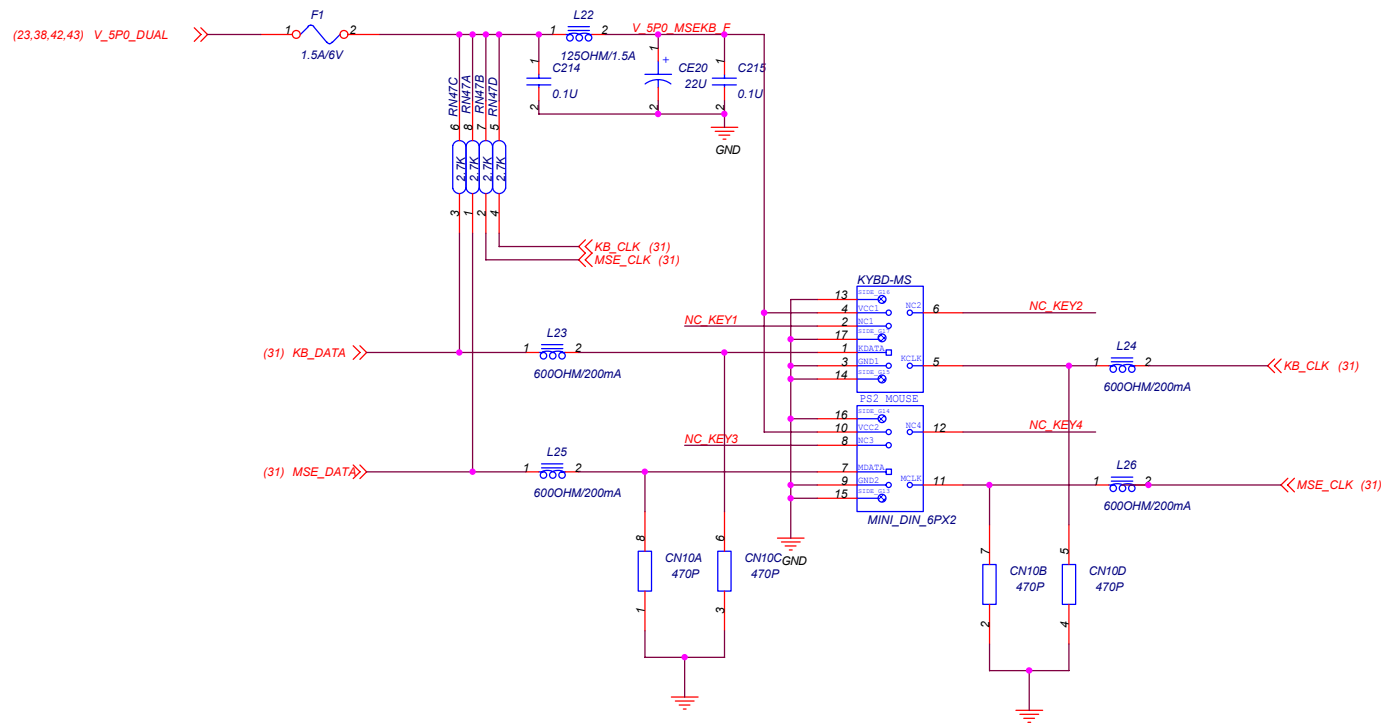


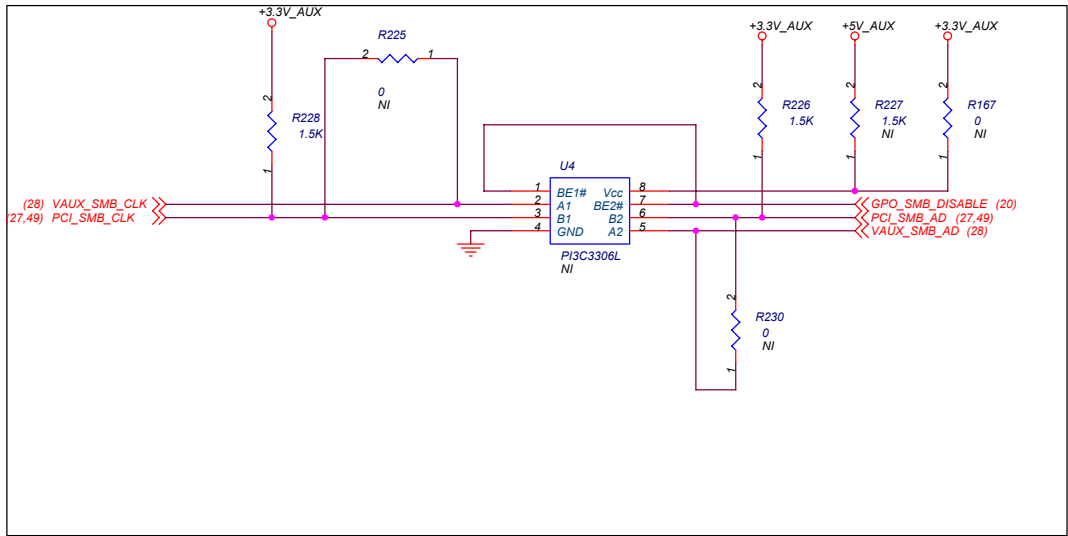
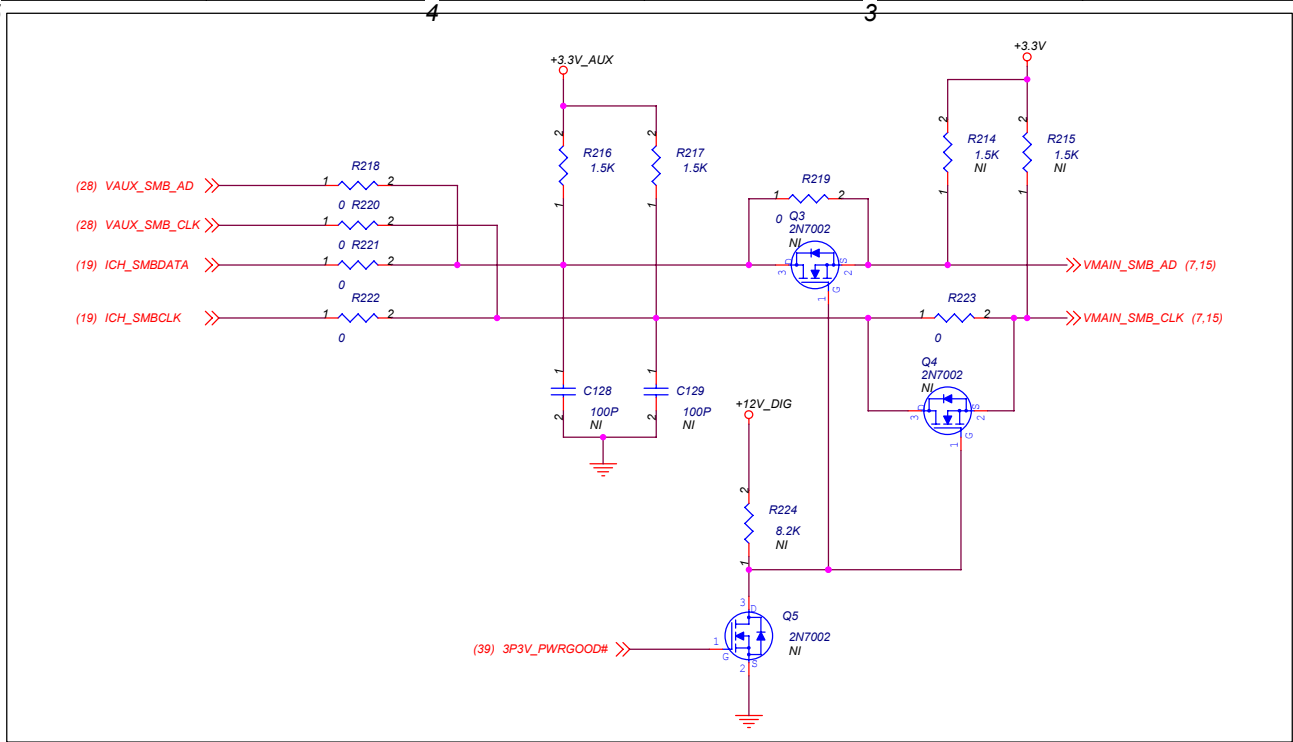
LINK	LED
1000M	Yellow
100M	Orange
10M	Green

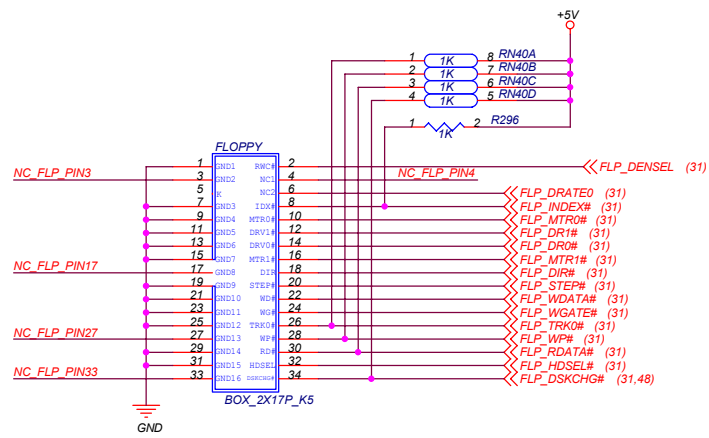


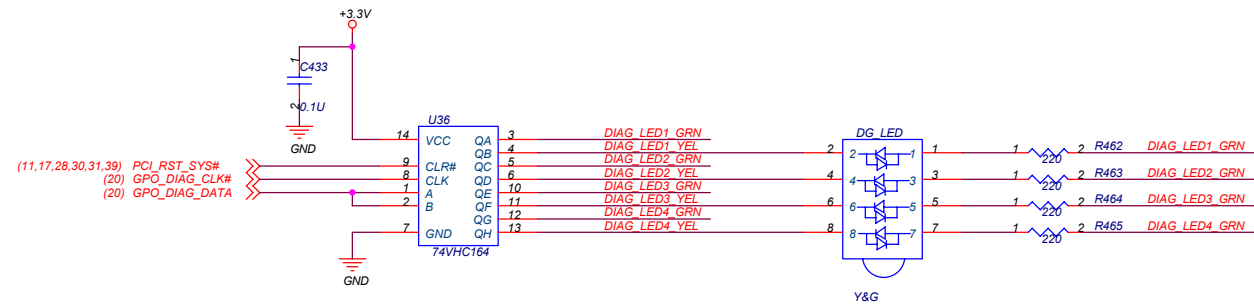


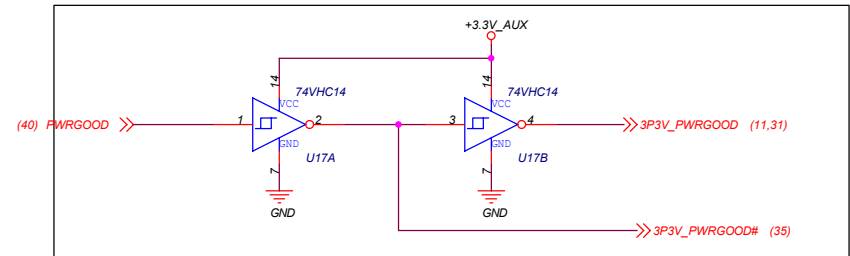
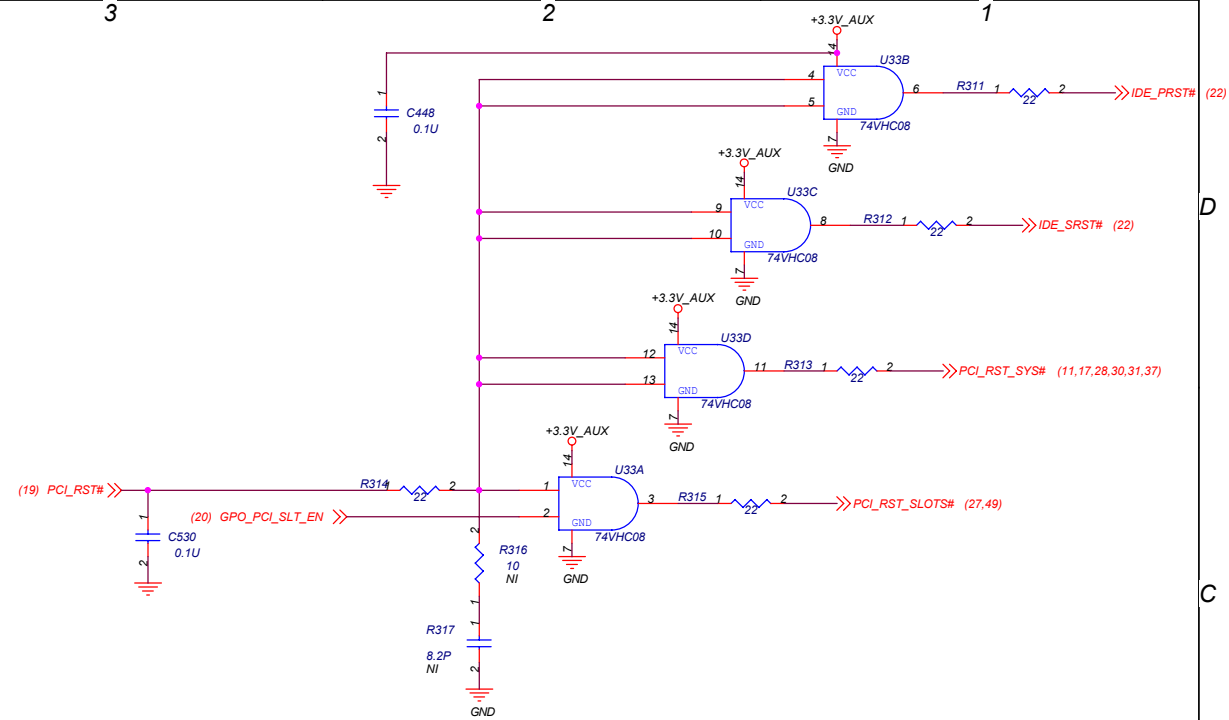
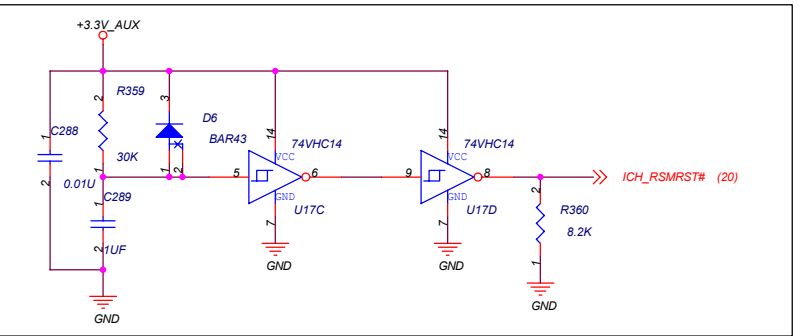
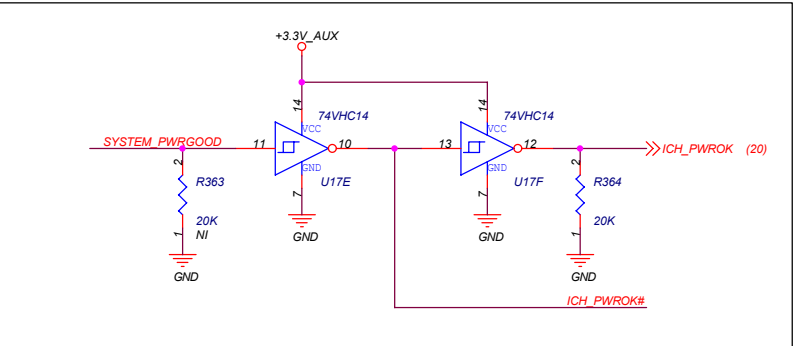
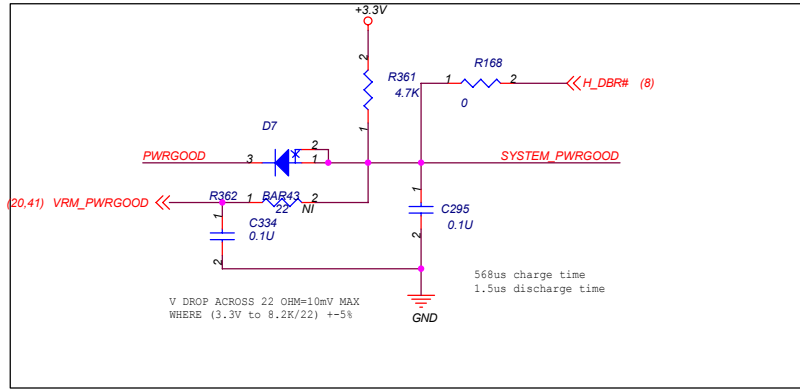


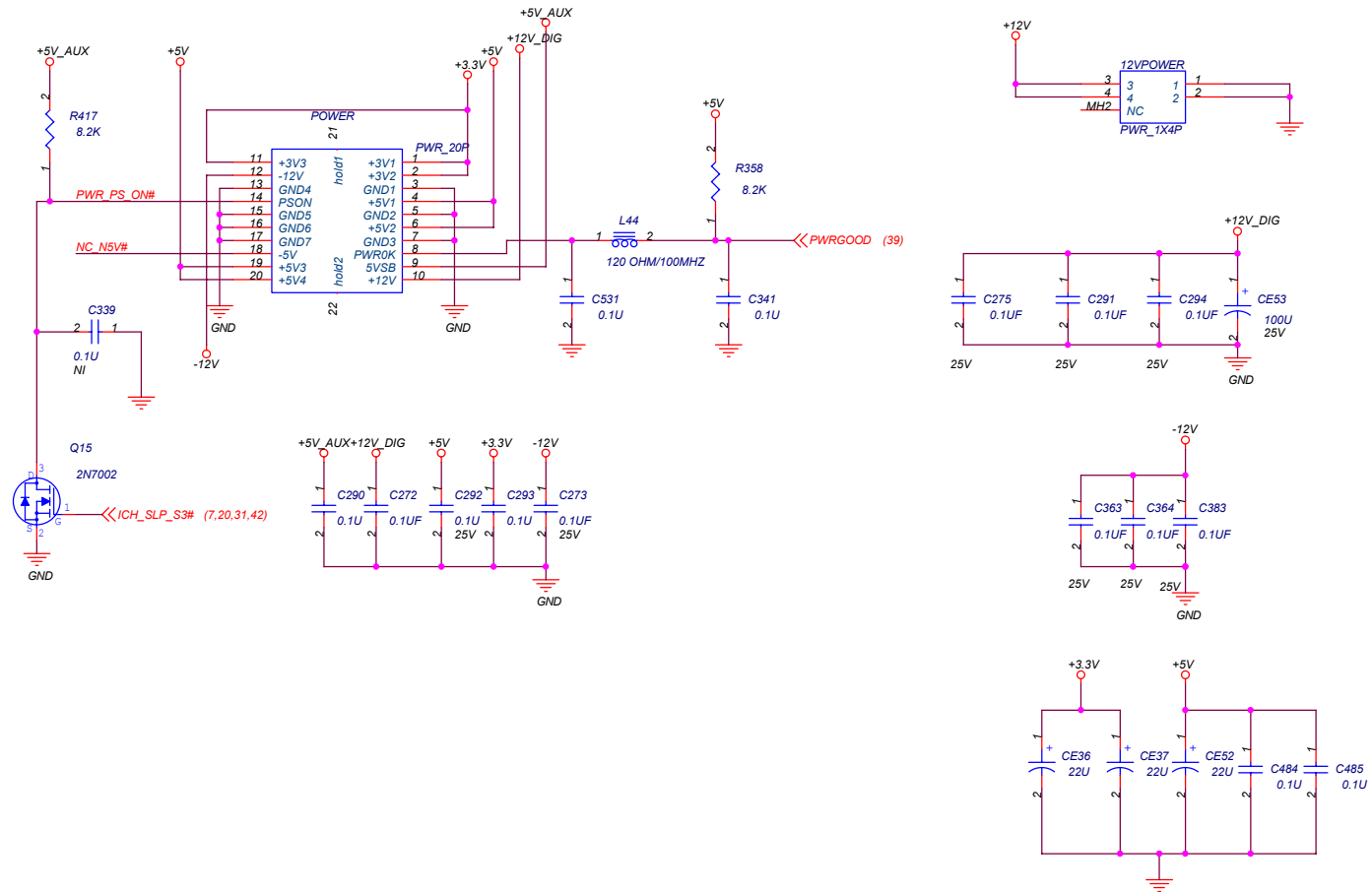


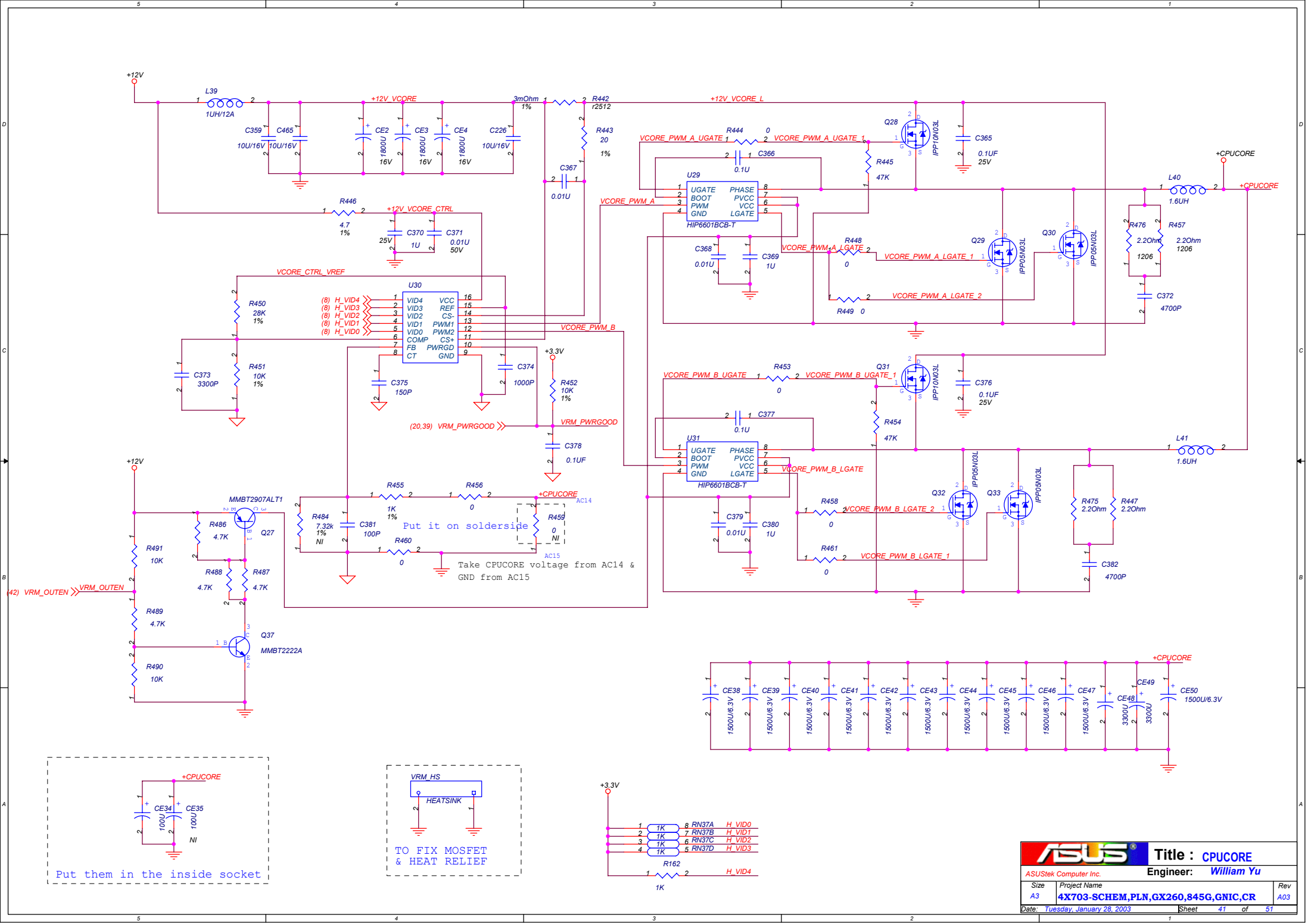


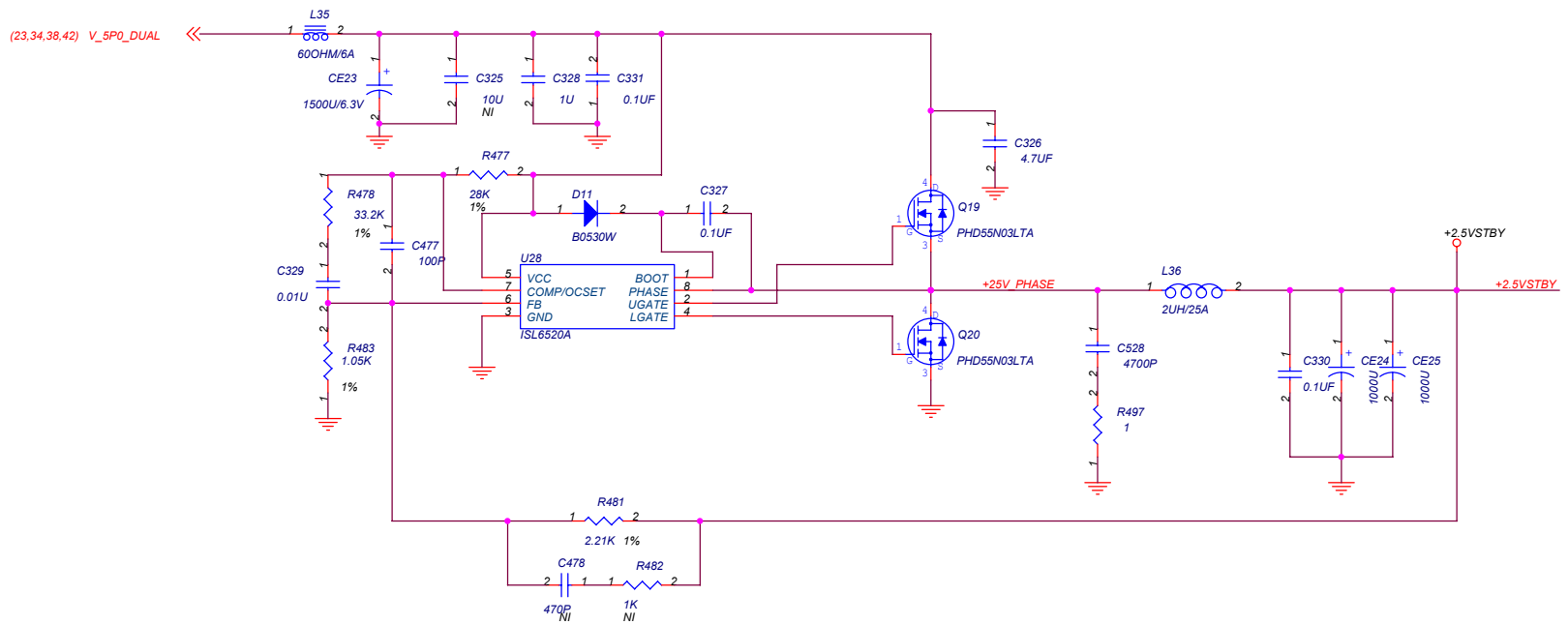


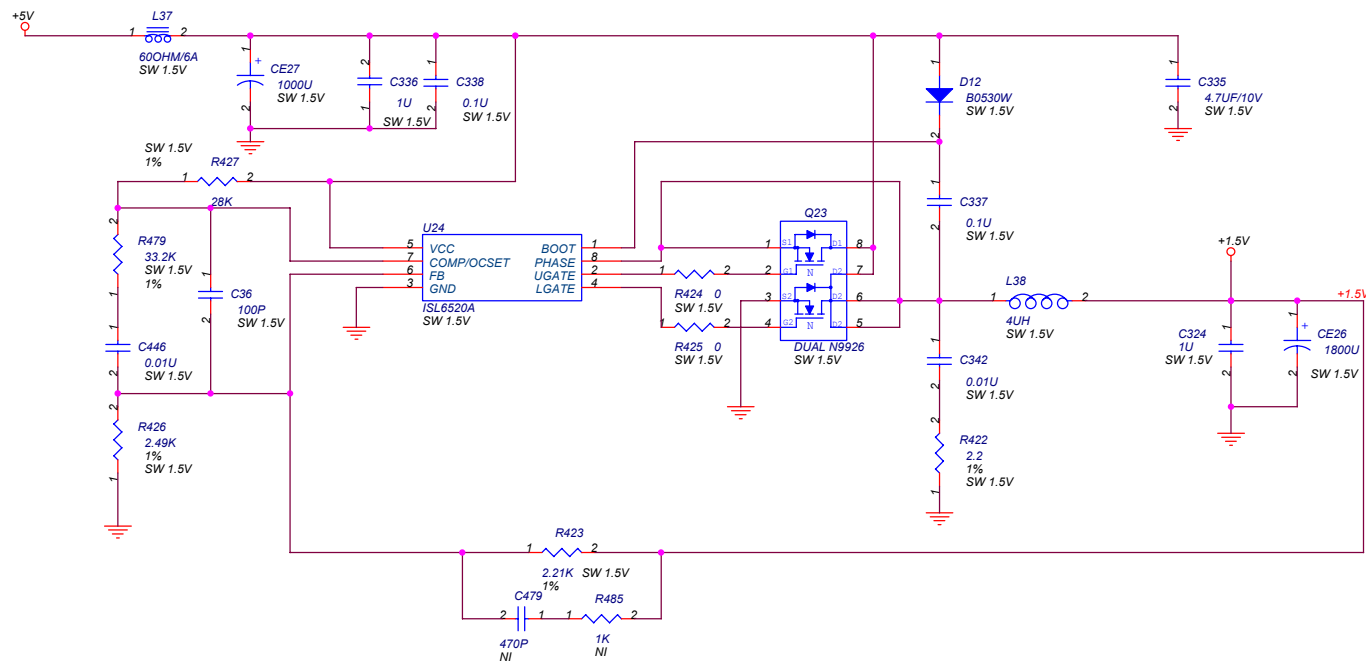




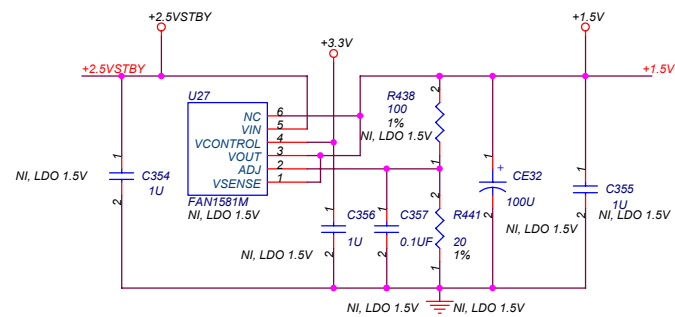




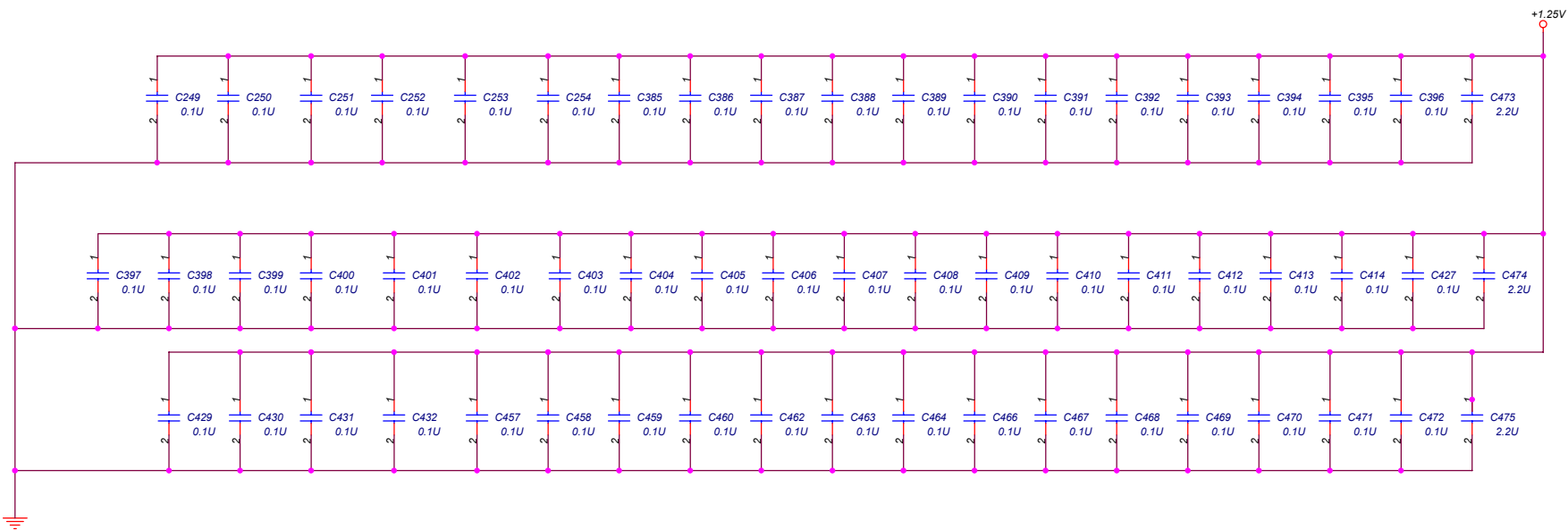
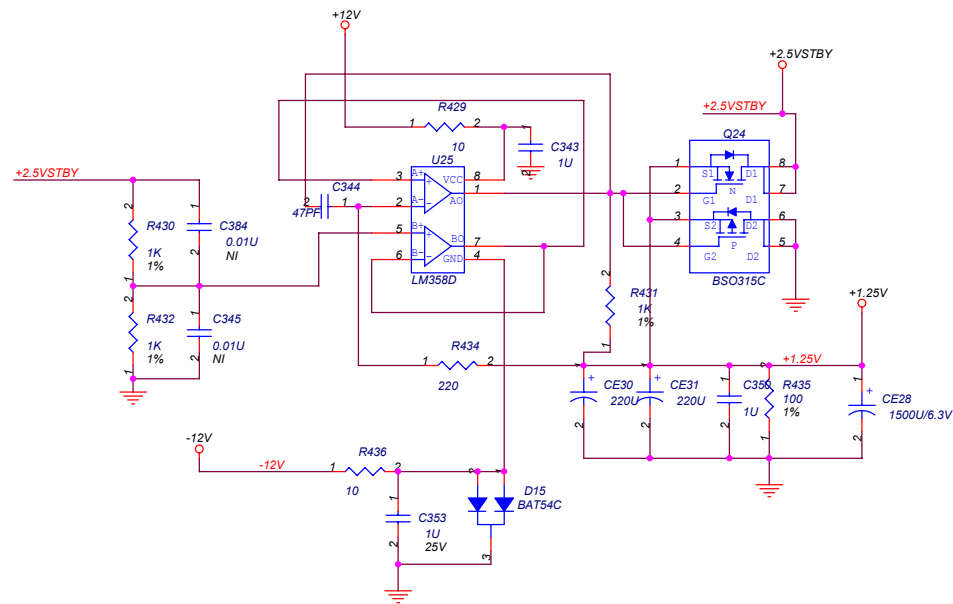


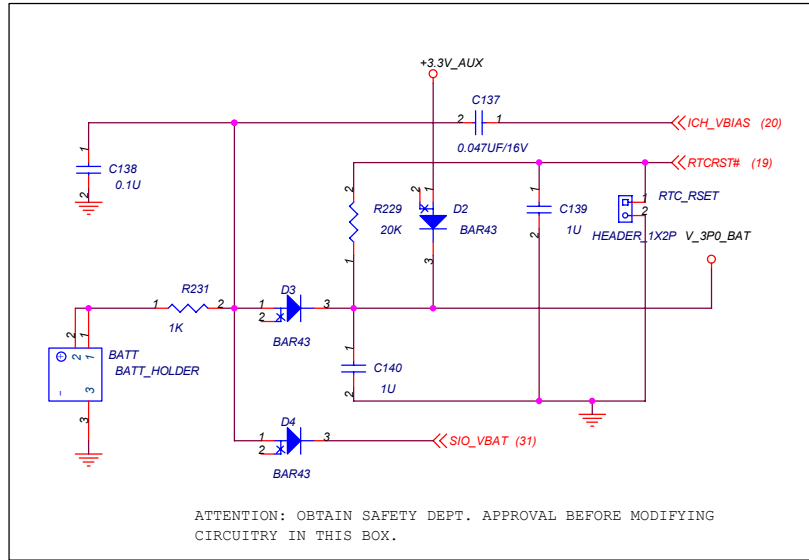


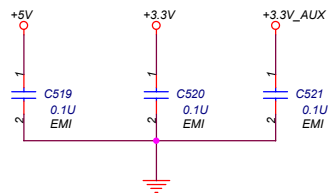
SW 1.5V for Rainier-CR & Fender-CR



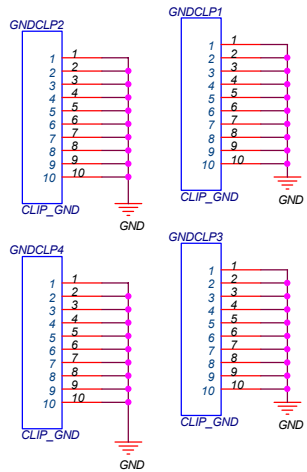
LDO 1.5V for SHASTA



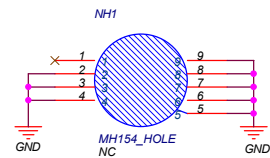
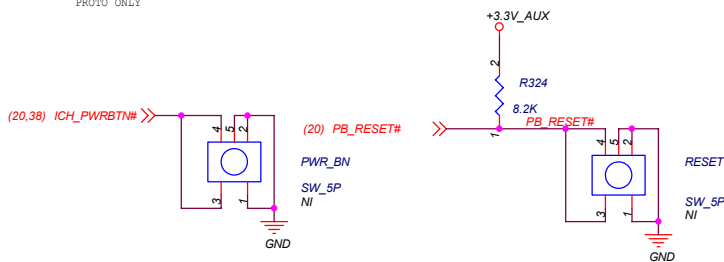




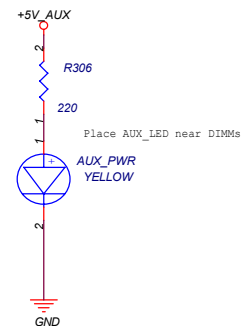
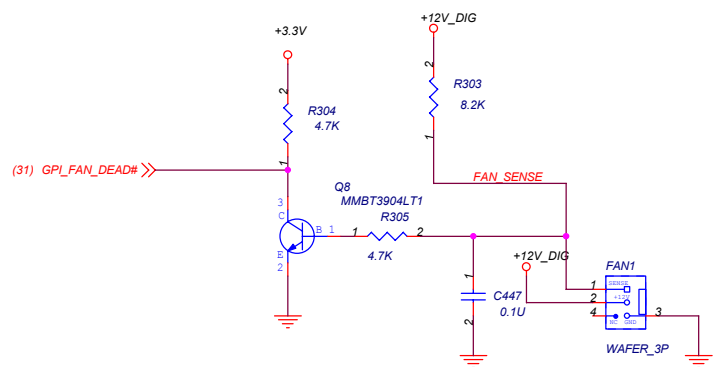
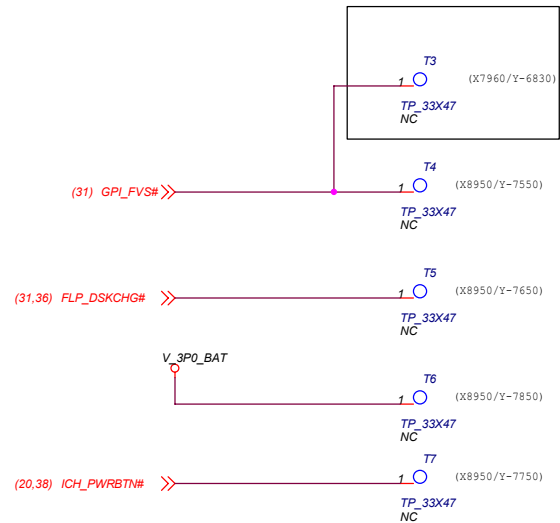
This page is left for EMI solution.

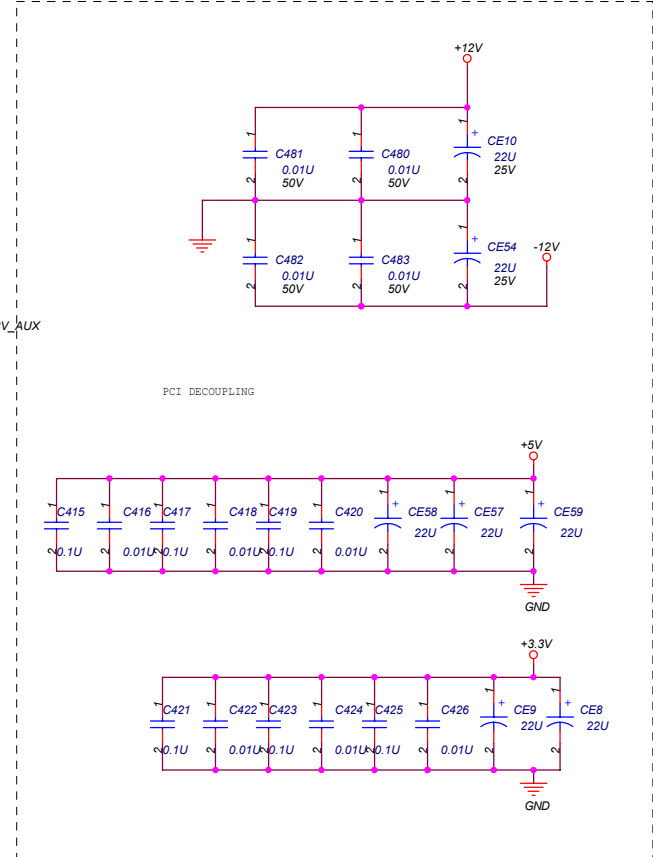
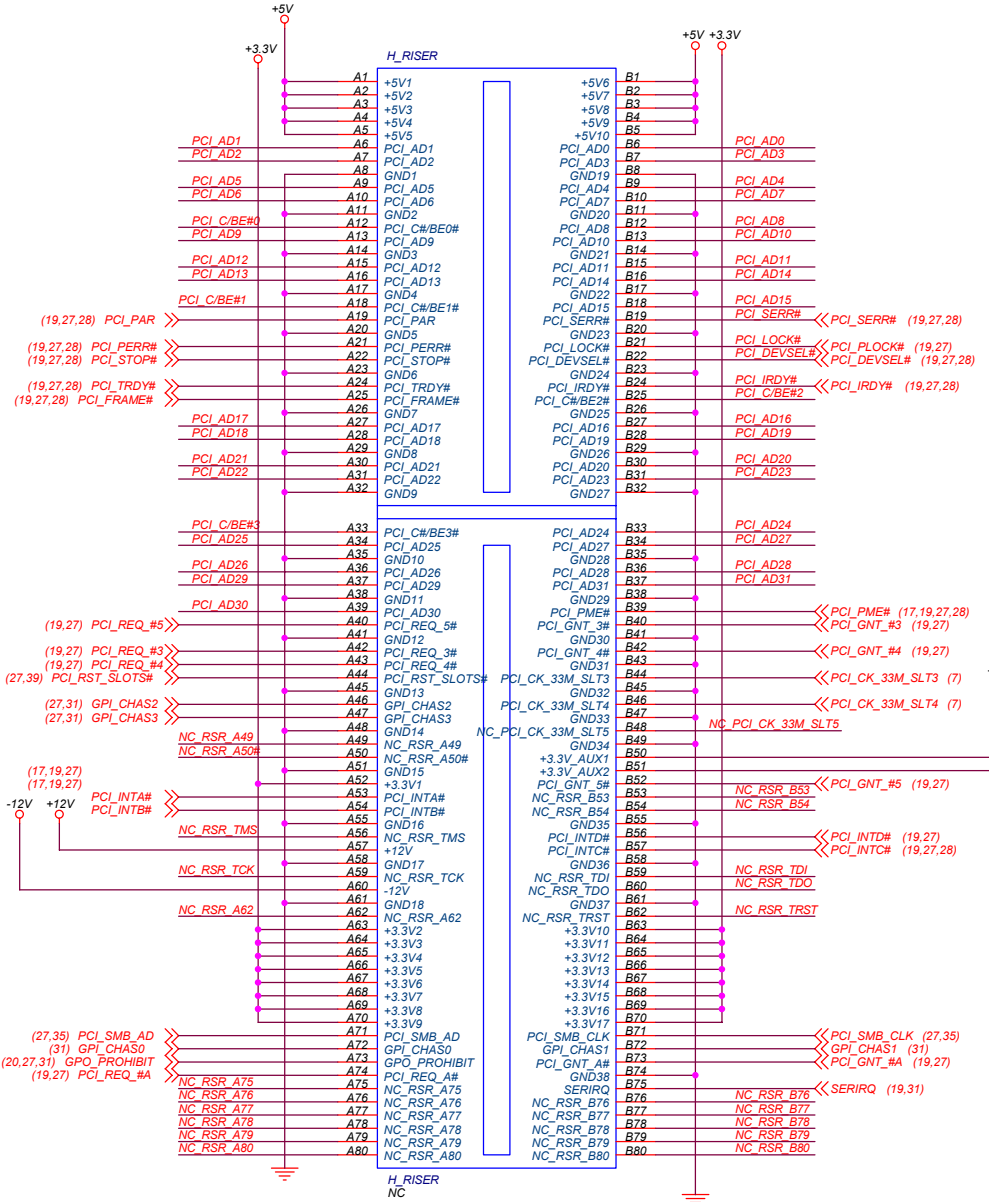
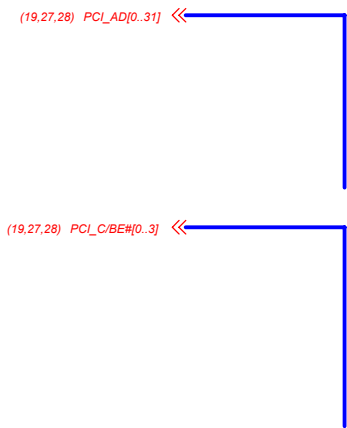


PROTO ONLY



Put it on Backside and follow Rainier's position





REFERENCE	Rainier-CR	Fender-CR	SHASTA	Sub-System
AGP1	SLOT_124P	SLOT_124P	NI	AGP
C85,C87-C98, C228	0.1U	0.1U	NI	AGP
R4	33OHM	33OHM	NI	AGP
R273, R154, R155	8.2KOHM	8.2KOHM	NI	AGP
R280	NI	NI	220OHM	AGP
U2	845G	845G	845GL	AGP
NIC_USB	0862-1J1T-43	0812-1X1T-03	0812-1X1T-03	LAN
U16	KENAI	LAVON	LAVON	LAN
R356	0OHM	NI	NI	LAN
R368	2.49KOHM	549OHM	549OHM	LAN
R437	1OHM (1%)	NI	NI	LAN
C351	4.7U	NI	NI	LAN
R274	8.2KOHM	NI	NI	LAN
R281	NI	220OHM	220OHM	LAN
R347,R348,R351,R352	49.9OHM	NI	NI	LAN
R493	1.96KOHM	NI	NI	LAN
R492	2.21KOHM	NI	NI	LAN
Q13,Q14	BCP69	NI	NI	LAN
R480	121OHM (1206)	NI	NI	LAN
C281,C282,C283,C284	0.01U	NI	NI	LAN
R248,R164	1KOHM	NI	NI	LAN
C287,C269	0.1U	NI	NI	LAN
C268,C267	4.7UF	NI	NI	LAN
R325,R326,R344,R365,R366	0OHM	NI	NI	LAN
R327,R329,R343,R471	NI	0OHM	0OHM	LAN
R330	53.6OHM	NI	NI	LAN
R331	33.2OHM	NI	NI	LAN
R332	5.1KOHM	NI	NI	LAN
R335	NI	100KOHM	100KOHM	LAN
R472,R337	330OHM	NI	NI	LAN
R339	NI	604OHM	604OHM	LAN
R340	NI	NI	NI	LAN
R350,R346	49.9OHM	56.2OHM	56.2OHM	LAN

REFERENCE	Rainier-CR	Fender-CR	SHASTA	Sub-System
Q46	MMBT2222A	NI	NI	LAN
R89	0 Ohm	100K Ohm	100K Ohm	LAN
R422	2.2OHM	2.2OHM	NI	SW 1.5V
R423	2.21KOHM	2.21KOHM	NI	SW 1.5V
R424,R425	0OHM	0OHM	NI	SW 1.5V
R426	2.49KOHM	2.49KOHM	NI	SW 1.5V
R427	28 KOHM	28 KOHM	NI	SW 1.5V
D12	SS0520	SS0520	NI	SW 1.5V
L37	60OHM/6A	60OHM/6A	NI	SW 1.5V
L38	4UH/10A	4UH/10A	NI	SW 1.5V
R479	33.2KOHM	33.2KOHM	NI	SW 1.5V
U24	ISL6520A	ISL6520A	NI	SW 1.5V
Q23	DUAL N9926	DUAL N9926	NI	SW 1.5V
CE27	1000U	1000U	NI	SW 1.5V
C36	100p	100p	NI	SW 1.5V
C335	4.7U	4.7U	NI	SW 1.5V
C336, C324	1U	1U	NI	SW 1.5V
C337,C338	0.1U	0.1U	NI	SW 1.5V
C446,C342	0.01U	0.01U	NI	SW 1.5V
CE26	1800U	1800U	NI	SW 1.5V
CE12	1000U	1000U	NI	SW 1.5V
CE32	NI	NI	100U	LDO 1.5V
C357	NI	NI	0.1UF	LDO 1.5V
C354,C355,C356	NI	NI	1U	LDO 1.5V
R438	NI	NI	100OHM	LDO 1.5V
R441	NI	NI	20OHM	LDO 1.5V
U27	NI	NI	AMS1505	LDO 1.5V

1. Rainier-CR
2. Fender-CR AGP+LAVON
3. SHASTA LAVON+ non-AGP

ASUS		Title :Different mount part - 1	
ASUSTek Computer Inc.		Engineer: William Yu	
Size	Project Name		Rev
A3	4X703-SCHEM,PLN,GX260,845G,GNIC,CR		A03
Date: Tuesday, January 28, 2003	Sheet 50	of	51

REFERENCE	Rainier-CR	Fender-CR	SHASTA	Sub-System
RN53	NI	NI	NI	LPC47M534
C340	NI	NI	NI	LPC47M534
R166	NI	NI	NI	LPC47M534
R169	NI	NI	NI	LPC47M534
R171	NI	NI	NI	LPC47M534
R173	NI	NI	NI	LPC47M534
R175	NI	NI	NI	LPC47M534
R232	NI	NI	NI	LPC47M534
C264	NI	NI	NI	LPC47M534
C265	NI	NI	NI	LPC47M534
R233	22 Ohm	22 Ohm	22 Ohm	LPC47M534
R233	220 Ohm	220 Ohm	220 Ohm	LPC47M564
R32, R78	8.2KOHM	8.2KOHM	NI	400 FSB
R33	2.2KOHM	2.2KOHM	NI	400 FSB
R152	NI	NI	8.2KOHM	400 FSB