AVALON

GRANTSDALE / DDR1 / ICH6 / UATX

FAB D

REV 4.0

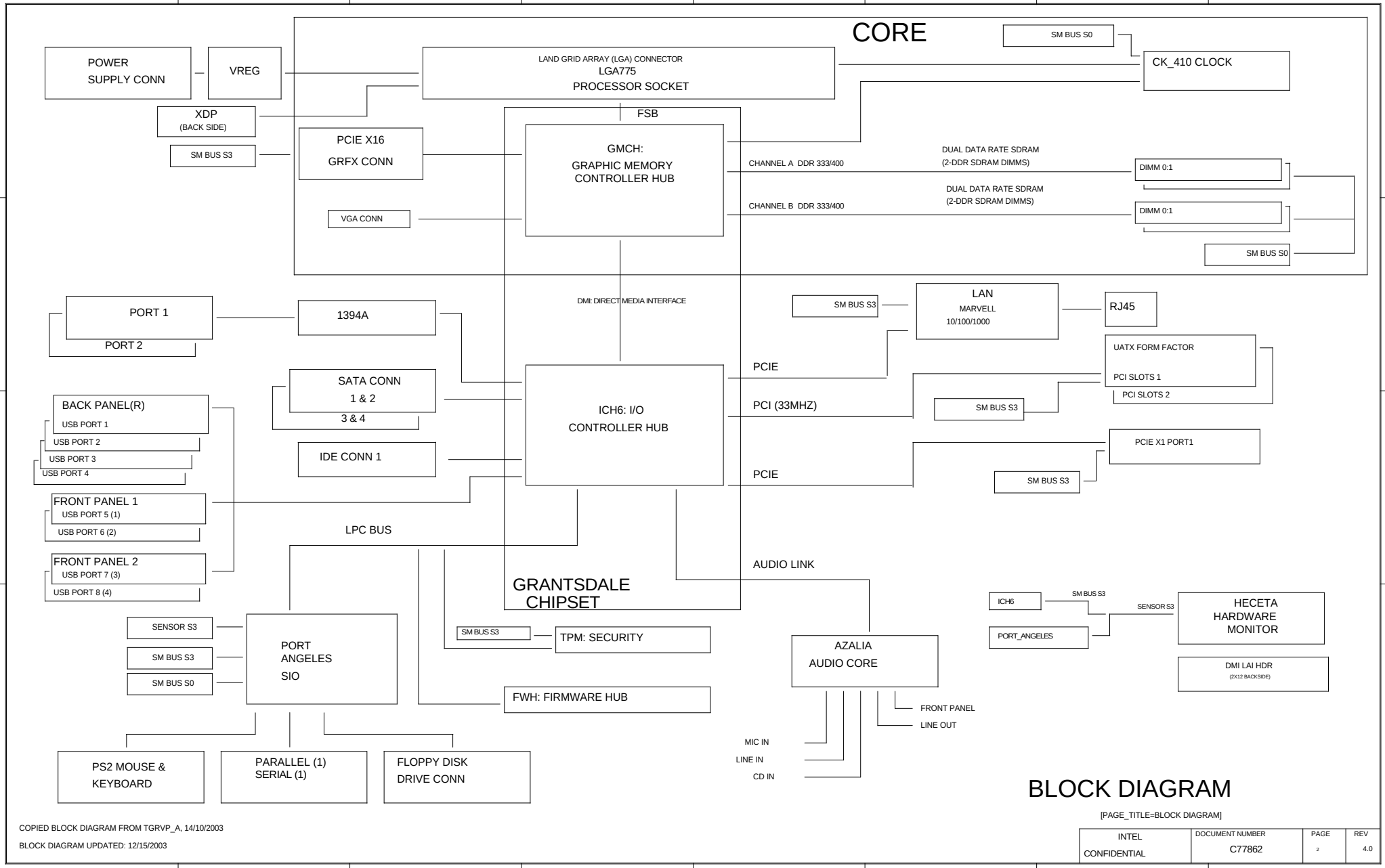
TAPE-OUT:

POWER SYMBOLS USED:

VCC3
VCC
+12V
-12V

NOTES:

1. THIS SCHEMATIC DOCUMENTS THE GENERIC PRODUCT WITH ALL POSSIBLE CONFIGURATIONS. PLEASE REFER TO SPECIFIC PRODUCT PBA EPL FOR ITEMS SHOWN AS OPTIONAL IN THE SCHEMATIC.
2. RESISTORS ARE IN OHMS UNLESS OTHERWISE SPECIFIED.
3. VCC = +5V UNLESS OTHERWISE SPECIFIED.
4. * SUFFIX INDICATES ACTIVE LOW SIGNAL.
5. \I SUFFIX INDICATES SIGNAL EXITS HIERARCHICAL BLOCK.
6. THIS DOCUMENT ALSO EXISTS ON ELECTRONIC MEDIA.



BLOCK DIAGRAM

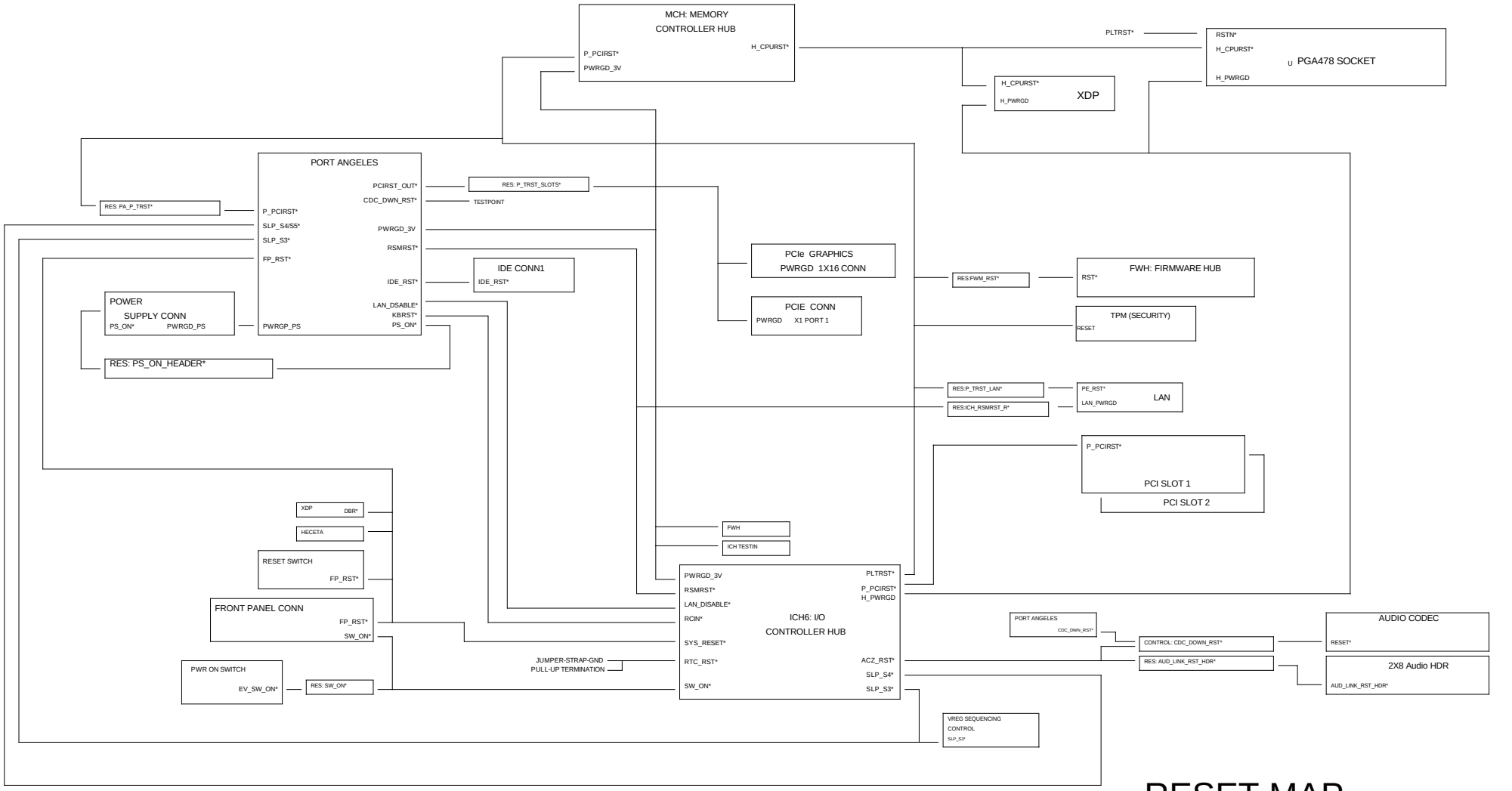
[PAGE_TITLE=BLOCK DIAGRAM]

COPIED BLOCK DIAGRAM FROM TGRVP_A, 14/10/2003

BLOCK DIAGRAM UPDATED: 12/15/2003

CORE

AFTER P_PCIRST*, HANDSHAKE (ON HL BUS) BETWEEN ICH/MCH MUST HAPPEN BEFORE H_CPURST* WILL BE ASSERTED/DE-ASSERTED

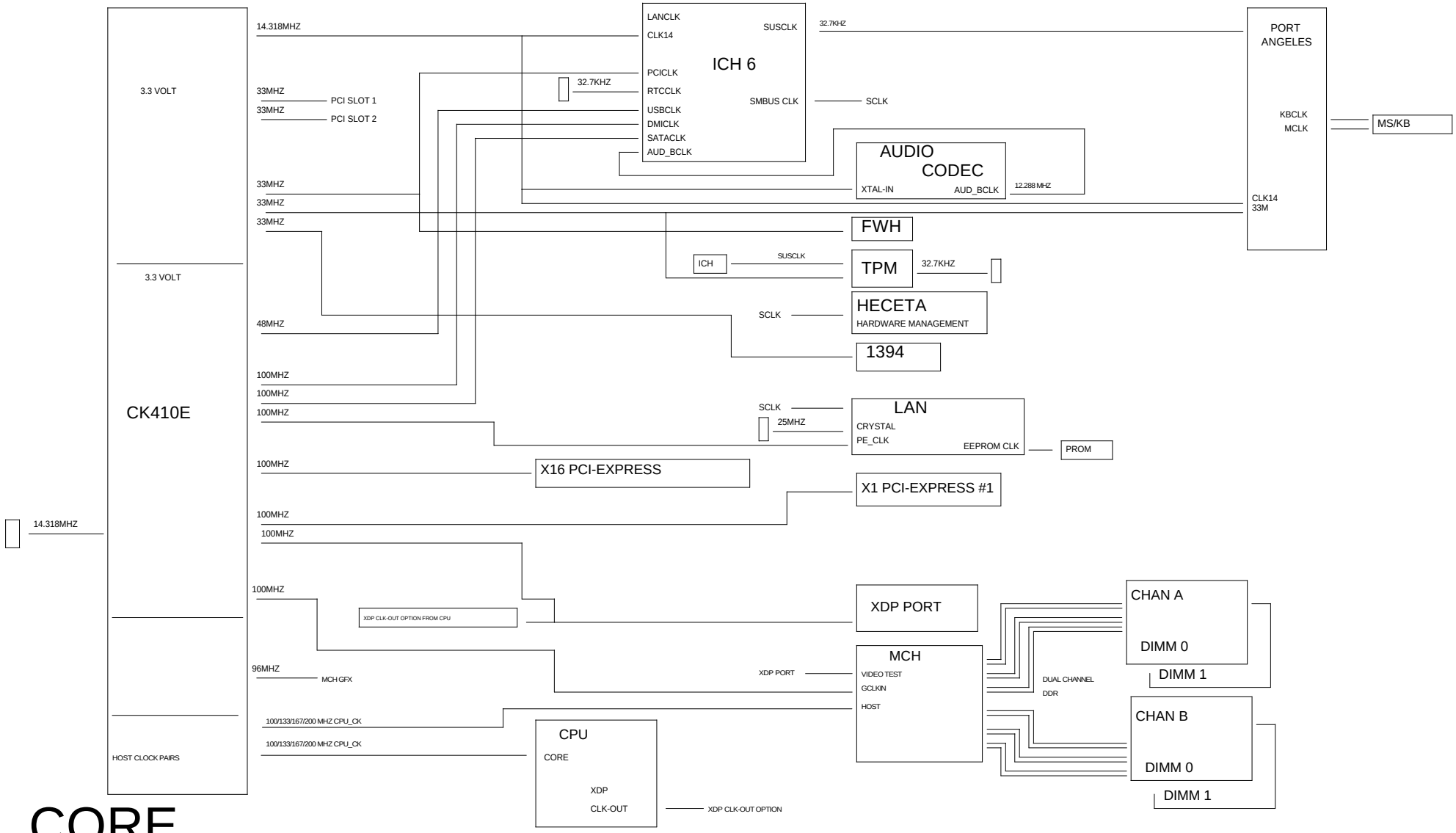


RESET MAP

[PAGE_TITLE=RESET MAP]

COPIED RESET MAP FROM TGRVP_A, 14/10/2003

RESET MAP UPDATED: XX/XX/2003



CORE

COPIED CLOCK DISTRIBUTION FROM TGRVP_A, 14/10/2003

CLOCK DISTRIBUTION UPDATED: 12/15/2003

CLOCK DISTRIBUTION

[PAGE_TITLE=CLOCK DISTRIBUTION]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	4	4.0

ICH 6

PIN NAME	WELL	USAGE	DURING RESET	S3/S5	NOTES
GPI[0]	MAIN	P_REQ6*	---	---	P/U ON PAGE 54, 2.7K TO VCC
GPI[2]	MAIN	P_REQ5*	---	---	P/U ON PAGE 54, 2.7K TO VCC
GPI[2]	MAIN	P_INTE*	---	---	P/U ON PAGE 54, 8.2K TO VCC3
GPI[3]	MAIN	P_INTF*	---	---	P/U ON PAGE 54, 8.2K TO VCC3
GPI[4]	MAIN	P_INTG*	---	---	P/U ON PAGE 54, 8.2K TO VCC3
GPI[5]	MAIN	P_INTH*	---	---	P/U ON PAGE 54, 8.2K TO VCC3
GPI[6]	MAIN	1X4_DETECT	---	OFF	
GPI[7]	MAIN	FP_AUD_DETECT	---	---	10K P/D TO 3.3V PG 43
GPI[8]	RESUME	AC_OK (FOR DEBUG HDR) - NOT USED	---	---	10K P/D TO 3.3V STBY PG 43
GPI[9]	RESUME	OC[4]*	HIGH	DRIVEN	
GPI[10]	RESUME	OC[5]*	HIGH	DRIVEN	
GPI[11]	RESUME	SMBALERT*	---	---	10K P/U TO 3.3V STBY PG 43
GPI[12]	MAIN	SATA HOT SWAP NOT USED	---	---	10K P/D TO GND PG 43
GPI[13]	RESUME	IO_PME*	---	DRIVEN	
GPI[14]	RESUME	OC[6]*	HIGH	DRIVEN	
GPI[15]	RESUME	OC[7]*	HIGH	DRIVEN	
GPO[16]	MAIN	GNT[6]*	HI-Z	OFF	
GPO[17]	MAIN	GNT[5]*	HI-Z	OFF	
GPO[18]	MAIN	STP_PCI# NOT USE	---	---	
GPO[19]	MAIN	OEM_LED0	---	---	
GPO[20]	MAIN	STP_PCI#	---	---	
GPO[21]	MAIN	NOT ASSIGN	---	---	
GPO[22]	---	---	---	---	
GPO[23]	MAIN	1394 ENABLE CTRL	---	---	
GPIO[24]	RESUME	BOARD ID 0	HIGH	OFF	
GPIO[25]	RESUME	INTERNAL VRM STRAP	HIGH	DEFINED	
GPIO[26]	MAIN	SATAGP0	---	---	4.7K P/U TO 3.3V PG 39
GPIO[27]	RESUME	BOARD ID 1	HIGH	DEFINED	
GPIO[28]	RESUME	RPS_OFF* (FOR DEBUG HDR) - NOT USED	HIGH	DEFINED	10K P/D TO GND PG 43
GPIO[29]	MAIN	SATAGP1	---	---	4.7K P/U TO 3.3V PG 39
GPIO[30]	MAIN	SATAGP2	---	---	4.7K P/U TO 3.3V PG 39
GPIO[31]	MAIN	SATAGP3	---	---	4.7K P/U TO 3.3V PG 39
GPIO[32]	MAIN	NOT USED	HIGH	OFF	
GPIO[33]	MAIN	BOARD ID 2	HIGH	OFF	
GPIO[34]	MAIN	BOARD ID 3	HIGH	OFF	
GPI[40]	MAIN	REQ[4]*	---	LOW	
GPI[41]	MAIN	LDRQ[1]*	---	LOW	
GPO[48]	MAIN	GNT[4]*	HIGH	OFF	
GPO[49]	CPU	CPUPWRGD	HI-Z	OFF	

FWH

GPI4	CORE	NORM	INPUT	DEFINED	CONFIG JUMPER
GPI3	CORE	MFG_MODE*	INPUT	DEFINED	MANUF MODE
GPI2	CORE	BSKU4	INPUT	DEFINED	
GPI1	CORE	BAT_WARN (FOR DEBUG HDR) - NOT USED	INPUT	DEFINED	
GPI0	CORE	DMA66_DETECT_PRI	INPUT	DEFINED	HI/LOW BIOS CONFIG FOR IDE PRI (FEATURE IS DEFAULT LOW)

PORT ANGELES

		PA1.5	PA3.0			
GPO0		NA	SENSOR_SDA	OUTPUT	DEFINED	DESIGN FEATURE WITH RESISTOR STRAPPING
GPO1		NA	FANTACH3	INPUT	DEFINED	DESIGN FEATURE WITH RESISTOR STRAPPING
GPO2		GPO_LAN_DISABLE	FANTACH4	INPUT		
GPO3		NA	FANPWM1	OUTPUT		
GPO4		BSKUS/1_WATT	FANPWM2	OUTPUT		
GPO5		NA	FANPWM3	OUTPUT	DEFINED	
GPI6		FAN_TACH1	FAN_TACH1	INPUT	DEFINED	
GPI7		FAN_TACH2	FAN_TACH2	INPUT	DEFINED	
GPI010		5V_DDCSDA	5V_DDCSDA	INPUT		
GPIO11		5V_DDCSCL	5V_DDCSCL	INPUT		
GPIO12		3V_DDCSDA	3V_DDCSDA	INPUT		
GPI013		3V_DDCSCL	3V_DDCSCL	INPUT		
GPI14		CDC_DWN_ENAB*	CDC_DWN_ENAB*	INPUT		2X12_DETECT
IO_PME*		IO_PME*		OUTPUT		
GRN_LED		GRN_LED		OUTPUT		
YLW_LED		YLW_LED		OUTPUT		

IRQ ROUTING TABLE

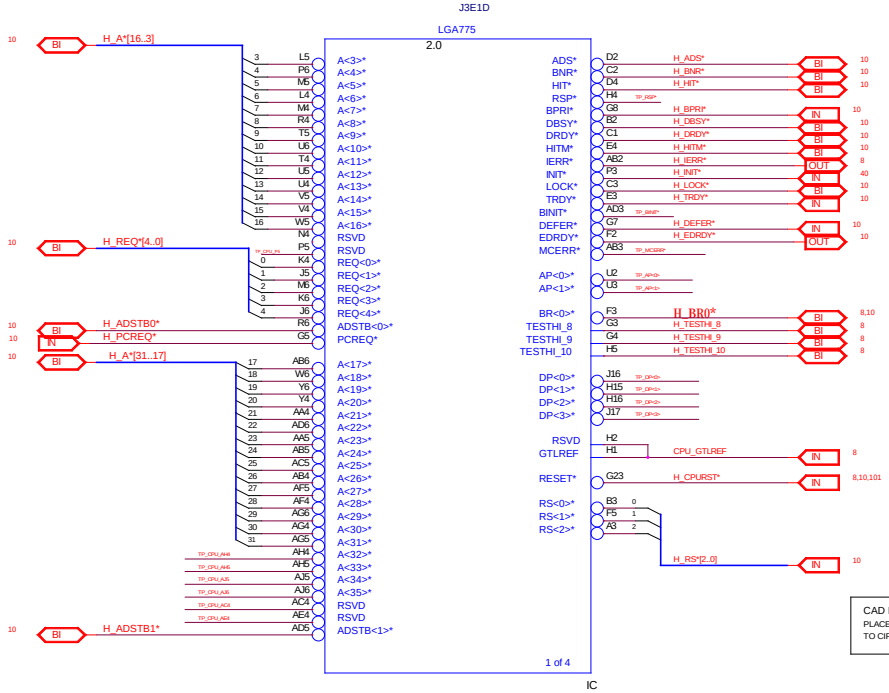
		SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6 1394	PCIE X16	PCIE X1_1	LAN	USB1-F0	USB1-F1	USB1-F2	USB1-F3	USB #2	SMBUS	AZALIA
P_INTA*								IRQA						IRQD			
P_INTB*							IRQA		IRQA								IRQA
P_INTC*													IRQC				
P_INTD*												IRQB				IRQB	
P_INTE*		IRQD	IRQC							IRQA							
P_INTF*		IRQA	IRQB														
P_INTG*		IRQB	IRQA														
P_INTH*		IRQC	IRQD								IRQA				IRQA		
REQ/GNT		0	1				5										
IDSEL		16	17				21			24							

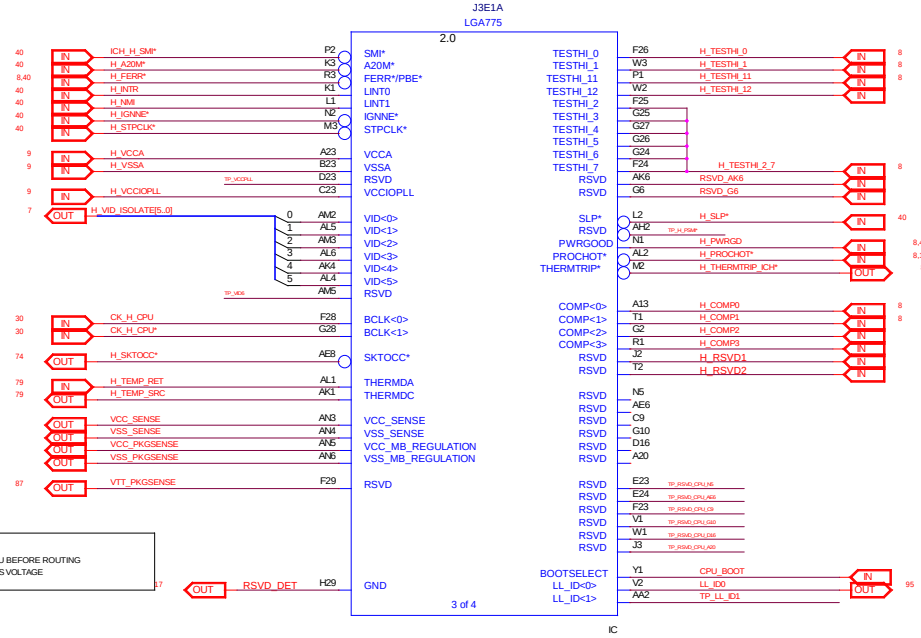
COPIED INFO FROM TGRVP_A, 10/14/2003

INFORMATION UPDATED: 12/12/2003

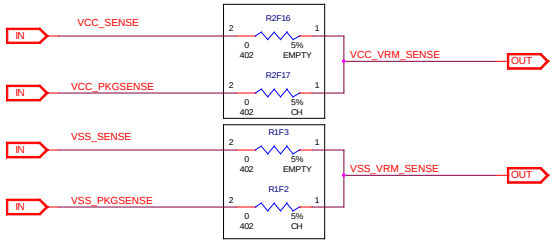
GPIO, IRQ, IDSEL MAPS

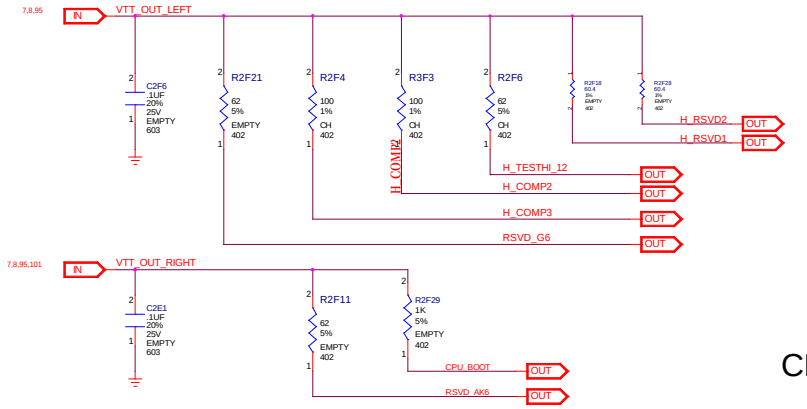
[PAGE_TITLE=GPIO, IRQ, IDSEL MAP]





CAD NOTE:
PLACE CAPS CLOSE TO CPU BEFORE ROUTING
TO CIRCUITS THAT USE THIS VOLTAGE





CPU SOCKET

[PAGE_TITLE=CPU-SOCKET]

CORE PAGE

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	C77862	6	4.0

BOM NOTE:
ALWAYS STUFF ON
PRODUCT BOARDS

H_VID_ISOLATE[5..0] → H_VID[5..0]

R1F17 R1F19 R1F15 R1F18 R1F20 R1F16 — 0 402 5% CH

J3E1C
LGA775
2.0

H_TCK	AE1	TCK	
H_TDI	AD1	TDI	
H_TDO	AF1	TDO	
H_TMS	AC1	TMS	
H_TRST*	AG1	TRST*	
H_BPM*[5..0]	AJ2 AJ1 AD2 AG2 AF2 AG3	BPM<0>* BPM<1>* BPM<2>* BPM<3>* BPM<4>* BPM<5>*	
FP_RST*	AC2	DBR*	
XDP_CLKOUT	AK3	ITPCLK<0>	
XDP_CLKOUT*	AJ3	ITPCLK<1>	
	G29	BSEL<0>	
	H30	BSEL<1>	
	G30	BSEL<2>	
V_FSB_VTT	A29 B25 B29 B30 C29 A26 B27 C28 A25 A28 A27 C30 A30 C25 C26 C27 B26 D27 D28 D25 D26 B28 D29 D30	VTT	
VTT_PWRGD	AM5	VTT_PWRGD	
	AA1	VTT_OUT_RIGHT	
	J1	VTT_OUT_LEFT	
	F27	VTT_SEL	

4 of 4
IC

TPEV_VCCFUSEPRG, TPEV_VIDFUSEPRG

H_FSBSEL0 → H_FSBSEL0_ISOL (R4C20)
H_FSBSEL1 → H_FSBSEL1_ISOL (R4C25)
H_FSBSEL2 → H_FSBSEL2_ISOL (R4C21)

VCC3 — R4C22 1K 5% EMPTY 402

J3E1B
LGA775
2.0

H_D*[15..0]	B4 C5 A4 C6 A5 B6 B7 A7 A10 A11 B10 C11 D8 B12 C12 D11	D<0>* D<1>* D<2>* D<3>* D<4>* D<5>* D<6>* D<7>* D<8>* D<9>* D<10>* D<11>* D<12>* D<13>* D<14>* D<15>*	
H_DBI0*	A8	DBI<0>*	
H_STBN0*	C8	DSTBN<0>*	
H_STBP0	B9	DSTBP<0>	
H_D*[31..16]	G9 F8 F9 E9 D7 E10 D10 F11 F12 D13 E13 G13 F14 G14 F15 G15 G11 G12 E12	D<16>* D<17>* D<18>* D<19>* D<20>* D<21>* D<22>* D<23>* D<24>* D<25>* D<26>* D<27>* D<28>* D<29>* D<30>* D<31>*	
H_DBI1*		DBI<1>*	
H_STBN1*		DSTBN<1>*	
H_STBP1		DSTBP<1>	
H_D*[47..32]	G16 E15 E16 G18 G17 F17 F18 E18 E19 F20 E21 F21 G21 E22 D22 G22 D19 C20 G19 D20 D17 A14 C15 C14 B15 C18 B16 A17 B18 C21 B21 B19 A19 A22 B22 C20 A16 C17	D<32>* D<33>* D<34>* D<35>* D<36>* D<37>* D<38>* D<39>* D<40>* D<41>* D<42>* D<43>* D<44>* D<45>* D<46>* D<47>*	
H_DBI2*		DBI<2>*	
H_STBN2*		DSTBN<2>*	
H_STBP2		DSTBP<2>	
H_D*[63..48]		D<48>* D<49>* D<50>* D<51>* D<52>* D<53>* D<54>* D<55>* D<56>* D<57>* D<58>* D<59>* D<60>* D<61>* D<62>* D<63>*	
H_DBI3*		DBI<3>*	
H_STBN3*		DSTBN<3>*	
H_STBP3		DSTBP<3>	

2 of 4
IC

VCCP=AG22,K29,AM26,AL8,AE12,AE11
VCCP=W23,W24,W25,T25,Y28,AL18,AC25,W30,Y30,AN14,AD28,Y26,AC29,M29,U24,J23,AC27,AM18,AM19,AB8
VCCP=AC26,J8,J28,T30,AM9,AF15,AC8,AE14,N23,W29,U29,AC24,AC23,Y23,AN26,AN25,AN11,AN18,Y27,Y25
VCCP=AD24,AE23,AE22,AN19,V8,K8,AE21,AM30,AE19,AC30,AE15,M30,K27,M24,AN21,T8,AC28,N25,AE18,W26
VCCP=AD25,M8,N30,AD26,AJ26,AM29,M25,M26,L8,U25,Y8,AJ12,AD27,U23,M23,AG29,N27,AM22,U28,K28
VCCP=U8,AK18,AD8,K24,AH28,AH21,AK12,AH22,T29,AM14,AM25,AE9,Y29,AK25,AK19,AG15,J22,T24,AG21,AM21
VCCP=U25,U30,AL21,AG25,AJ18,J19,AH30,J15,AG12,AJ22,J20,AH18,AH26,W27,AL25,AN8,AH14,U27,T23,R8
VCCP=AK22,AN29,AG11,AK26,J10,AL15,AG26,AN9,AH15,AF18,AL15,J26,J18,J21,AG27,AK15,AF11,AD23,AM15,AF8
VCCP=AK21,AG30,AJ21,AM11,AL11,AJ11,K30,AL14,AN30,AH25,AL12,AJ9,AK11,AG14,N29,AL30,AJ25,AH9,J29,J11
VCCP=K25,P8,K23,AL19,AM8,T26,N28,AH12,AL22,AN15,AJ8,U26,AJ19,T27,AK8,AN12,AG9,N26,AF9,AF22
VCCP=AH11,AJ14,AH19,AH29,AH27,AG28,AL26,AM12,J24,J13,T28,W28,J12,J27,AG19,AL9,AD30,AF21,Y24,AK14
VCCP=J9,M27,AF14,J30,AG18,AA8,AG8,AL29,AD29,W8,AH8,N24,AN22,J14,K26,AF19,N8,AF12,M28,AK9
GND=C10,D12,AM7,C24,K2,C22,AN1,B14,K7,AE16,B11,AL10,AK23,H12,AF7,AK7
GND=H7,E14,L28,Y5,E11,AL16,AL24,AK13,AL3,D21,AL20,D18,AN2,AK16,AK20,AM27,AM1,AL13,AL17,C19
GND=E28,AH7,AK30,D24,AL23,A12,L25,J7,AE28,AE29,K5,J4,AE30,AN20,AF10,AE24,AM24,AN23,H9,H8
GND=H13,AC6,AC7,AH6,C16,AM16,AE25,AE27,AJ28,AJ7,F19,AH13,AD7,AH16,AK17,E17,AH17,AH20,AE5,AH23
GND=AE7,AM13,AH24,AJ30,AJ10,AF3,AK5,AJ16,AF6,AK29,AJ17,F22,AH3,AK10,AM10,F16,AJ23,F13,AG7,F10
GND=L26,AD4,H11,L24,L23,AM23,A15,AH10,B24,L3,H27,A21,AE2,AJ29,A24,AK27,AK28,B20,AM20
GND=H26,B17,H25,H24,AA3,AA7,H23,AA6,H10,H22,H21,H20,H19,H18,AB7,H17,AJ24,AM17,AC3,H14
GND=P28,V6,AK2,P27,P26,AM28,AJ13,W4,P25,AJ20,W7,P23,C7,Y2,L30,L29,D15,AL27,Y7,L27
GND=AA29,N6,N7,AA28,AN13,AA27,AA26,P4,AA25,AA24,P7,E26,V30,R2,V29,V28,R5,V27,R7,E20
GND=AN10,V25,T3,V24,V23,T6,AL7,E25,U1,R29,R28,R27,R26,R25,U7,R24,R23,P30,V3,P29
GND=AF16,AE10,AF13,H6,A18,A2,E2,D9,C4,A6,D6,D5,A9,D3,B1,B5,B8,AJ4,AE26,AH1
GND=E29,V7,C13,AK24,AB30,L6,L7,AB29,M1,AB28,AN17,AB27,AB26,AN16,M7,AB25,AB24,AB23,N3,AA30
GND=F4,AG10,AE13,AF30,H28,F7,AF29,AF28,G1,AF27,AF26,AF25,AN28,AN27,AF24,AF23,AG24,AF17,AN24,H3
GND=AN7,P24,AE20,AE17,E27,T7,R30,AJ27,AB1,AM4,V26,AA23,AL28,AF20,AG23,AG20,E8,AG17,AG16,AG13
NC=F6,Y3,AE3,E7,B13,D14,E6,D1,E5,

BOM NOTE:
ALWAYS STUFF ON
PRODUCT BOARDS

V_FSB_VTT → R4C26 0 5% CH 402, R4C27 0 5% CH 402 → TPEV_VIDFUSEPRG, TPEV_VCCFUSEPRG

VTT_OUT_RIGHT → R1F26 R1F25 R1F24 R2F42 R2F40 R1F28 — 680 5% CH 402

H_VID[5..0]

CORE PAGE

[PAGE_TITLE=CPU-SOCKET]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	7	4.0

CAD NOTE: PLACE AT CPU END OF ROUTE

CAD NOTE: PLACE AT ICH END OF ROUTE

6,7,95,101 IN VTT_OUT_RIGHT

6,7,95 IN VTT_OUT_LEFT

7,9,12,17,18,41,43,87 IN V_FSB_VTT

R3F1 62 5% CH 402

R2F31 62 5% CH 402

R2F2 100 5% CH 402

R2F19 62 5% EMPTY 402

R2F25 62 5% CH 402

R7H2 62 5% CH 402

R7H3 62 5% CH 402

H_BR0*

H_THERMTRIP_ICH* OUT 6,40

H_FERR* OUT 6,40

H_IERR* OUT 6

H_CPURST* OUT 6,10,101

H_PROCHOT* OUT 6,103

H_PWRGD OUT 6,40,101

H_BR0* OUT 6,10

CPU SIGNAL TERMINATION

7,9,12,17,18,41,43,87 IN V_FSB_VTT

R4C18 470 5% CH 402

R4C19 470 5% CH 402

R4C17 470 5% CH 402

H_FSBSEL0 OUT 7,17,29

H_FSBSEL1 OUT 7,17,29

H_FSBSEL2 OUT 7,17,29

R4C15 1K 5% EMPTY 402

R4C16 1K 5% EMPTY 402

R4C14 1K 5% EMPTY 402

DESIGN NOTE:

STRAPPING OPTION FOR DEBUG

TESTHI PULLUPS

7,9,12,17,18,41,43,87 IN V_FSB_VTT

6,7,95 IN VTT_OUT_LEFT

R2F3 62 5% CH 402

R2F1 62 5% CH 402

R3F2 62 5% CH 402

R3F4 62 5% CH 402

R2F7 62 5% CH 402

R4C24 62 5% CH 402

R4C23 62 5% EMPTY 402

H_TESTHI_0 OUT 6

H_TESTHI_2_7 OUT 6

H_TESTHI_1 OUT 6

H_TESTHI_8 OUT 6

H_TESTHI_9 OUT 6

H_TESTHI_10 OUT 6

H_TESTHI_11 OUT 6

TESTHI PIN NAME MAPPING	
TESTHI[0]	BYPASSEN
TESTHI[1]	ODT
TESTHI[5:2]	MCLK[3:0]
TESTHI[7:6]	MCLKIO[1:0]
TESTHI[10:8]	BR#[3:1]
TESTHI[11]	DPSLP#
TESTHI[12]	DT_SVR#

6,95 IN VCC_VRM_SENSE

NEVER JUMPER THIS HEADER!!!

J1F1 1X2HDR EMPTY 102276-001

6,95 IN VSS_VRM_SENSE

DESIGN NOTE:
THE PINS WILL BE USED AS TEST/PROBE POINTS ONLY.

CAD NOTE:
PLACE HEADERS AS CLOSE TO CPU PINS AS POSSIBLE

PRECISION FSB COMPENSATION RESISTORS

R4D1 60.4 1% 402 CH

H_COMP0 OUT 6

R2F5 60.4 1% 402 CH

H_COMP1 OUT 6

PLACE RESISTORS OUTSIDE SOCKET CAVITY

IF NO ROOM FOR VARIABLE RESISTOR DON'T PLACE.

GTLREF VOLTAGE SHOULD BE 0.67*VTT = 0.8V

(FOR THIS DESIGN)
100 OHMS OVER 210 OHMS RESISTORS

6,7,95,101 IN VTT_OUT_RIGHT

R2F23 100 1% CH 402

R2F24 210 1% CH 402

CPU_GTLREF_DIVIDER

EVAL FEATURE

R2F20 30 5% CH 402

CPU_GTLREF OUT 6

VCC3

R4C29 240 1% CH 402

R4C11 110 CH 402

H_TESTHI_0 OUT 6

6,17 RSVD_DET RSVD_DET

R4C13 61.9 CH 402

C4C3 .1UF 16V Y5V 402

[PAGE_TITLE=CPU TERMINATION & MISC]

CORE PAGE

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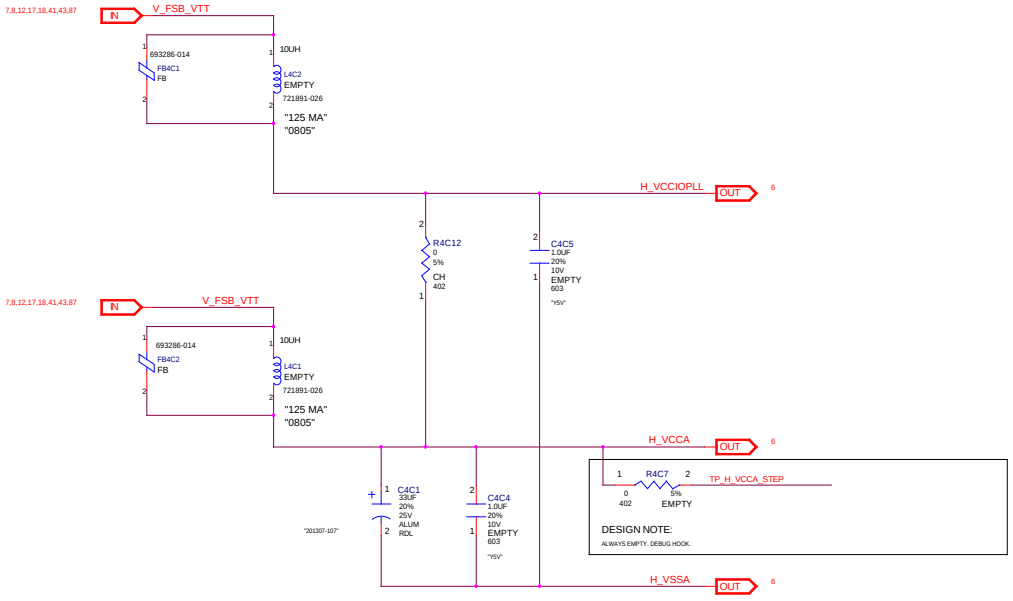
CONFIDENTIAL	C77862	8	4.0

CPU PLL SUPPLY FILTER



CAD NOTE:
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

CORE PAGE

[PAGE_TITLE=CPU ANALOG PLL FILTER]

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	9	4.0

J4D1 J6F1 J4F1 J6D1

NC NC NC NC

EMPTY EMPTY EMPTY EMPTY

A13494-005

HS6D1

GDG_WAVEHS

NC_1 NC_2 NC_4 NC_3

HEATSINK

C44993-001

WAVE SOLDER HEAT-SINK = WSHS

U6D1G

GDG_DDR1_1210

1.0

H_A*[31..3] (BI)

HA3* HA4* HA5* HA6* HA7* HA8* HA9* HA10* HA11* HA12* HA13* HA14* HA15* HA16* HA17* HA18* HA19* HA20* HA21* HA22* HA23* HA24* HA25* HA26* HA27* HA28* HA29* HA30* HA31*

H_REQ*[4..0] (BI)

HREQ0* HREQ1* HREQ2* HREQ3* HREQ4*

H_ADSTB0* (BI) H_ADSTB1* (BI) H_PCREQ* (OUT)

HADSTB0* HADSTB1* HPCREQ*

H_STBP0 (BI) H_STBN0* (BI) H_DBI0* (BI) H_STBP1 (BI) H_STBN1* (BI) H_DBI1* (BI) H_STBP2 (BI) H_STBN2* (BI) H_DBI2* (BI) H_STBP3 (BI) H_STBN3* (BI) H_DBI3* (BI)

HDSTBP0 HDSTBN0* HDINV0* HDSTBP1 HDSTBN1* HDINV1* HDSTBP2 HDSTBN2* HDINV2* HDSTBP3 HDSTBN3* HDINV3*

H_ADS* (BI) H_BNR* (BI) H_BPRI* (OUT) H_BR0* (OUT) H_CPURST* (OUT) H_DBSY* (BI) H_DEFER* (OUT) H_DRDY* (OUT) H_EDRDY* (IN) H_HIT* (OUT) H_HITM* (OUT) H_LOCK* (IN)

HADS* HBNR* HBPRI* HBREQ0* HCPURST* HDBSY* HDEFER* HDRDY* HEDRDY* HHIT* HHITM* HLOCK*

H_RS*[2..0] (BI) H_TRDY* (OUT)

HRS0* HRS1* HRS2* HTRDY*

1 of 7

IC

H_D*[63..0] (BI)

HD0* HD1* HD2* HD3* HD4* HD5* HD6* HD7* HD8* HD9* HD10* HD11* HD12* HD13* HD14* HD15* HD16* HD17* HD18* HD19* HD20* HD21* HD22* HD23* HD24* HD25* HD26* HD27* HD28* HD29* HD30* HD31* HD32* HD33* HD34* HD35* HD36* HD37* HD38* HD39* HD40* HD41* HD42* HD43* HD44* HD45* HD46* HD47* HD48* HD49* HD50* HD51* HD52* HD53* HD54* HD55* HD56* HD57* HD58* HD59* HD60* HD61* HD62* HD63*

HXSWING HXSCOMP HXRCOMP HVREF

HXSWING (IN) HXSCOMP (IN) HXRCOMP (IN) MCH_GTLREF (IN)

HCLKINP HCLKINN

CK_H_MCH (IN) CK_H_MCH* (IN)

[PAGE_TITLE=MCH SECTIONS PAGE 1 OF 6]

CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	10	4.0

SIGNAL NAMING CONVENTION

EXP: PCI EXPRESS

DMI: DIRECT MEDIA INTERFACE

ITP: ICH TRANSMIT POSITIVE

ITN: ICH TRANSMIT NEGATIVE

IRP: ICH RECEIVE POSITIVE

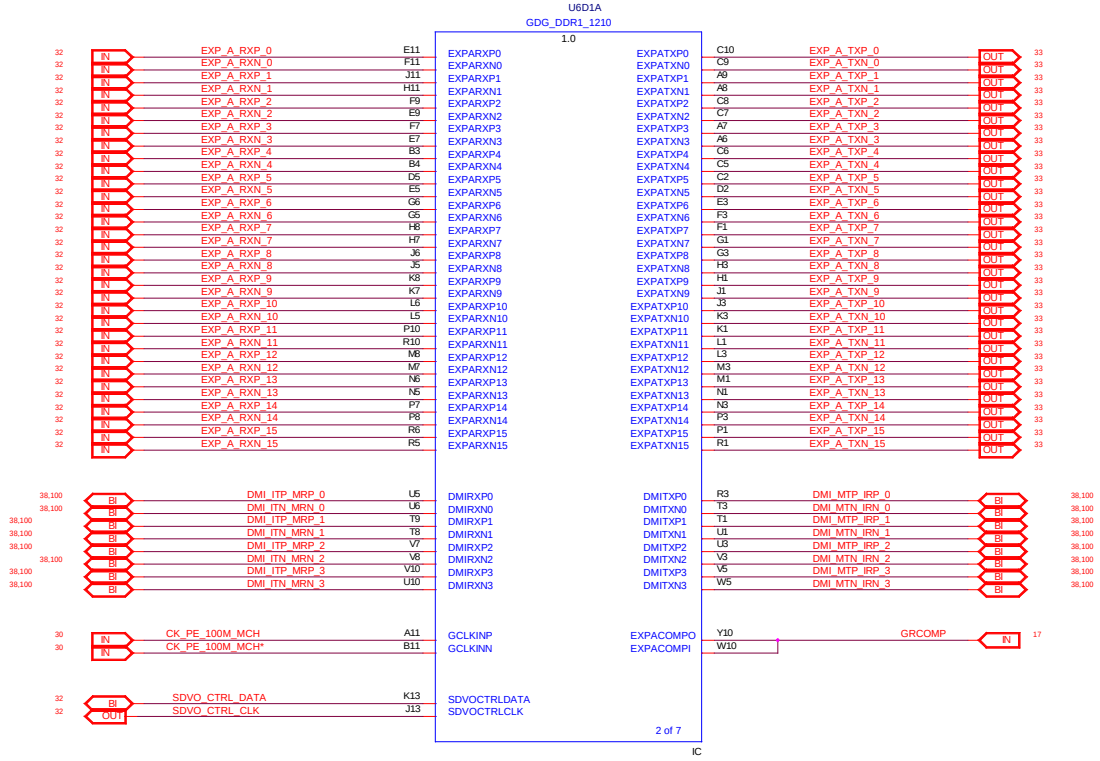
IRN: ICH RECEIVE NEGATIVE

MTP: MCH TRANSMIT POSITIVE

MTN: MCH TRANSMIT NEGATIVE

MRP: MCH RECEIVE POSITIVE

MRN: MCH RECEIVE NEGATIVE



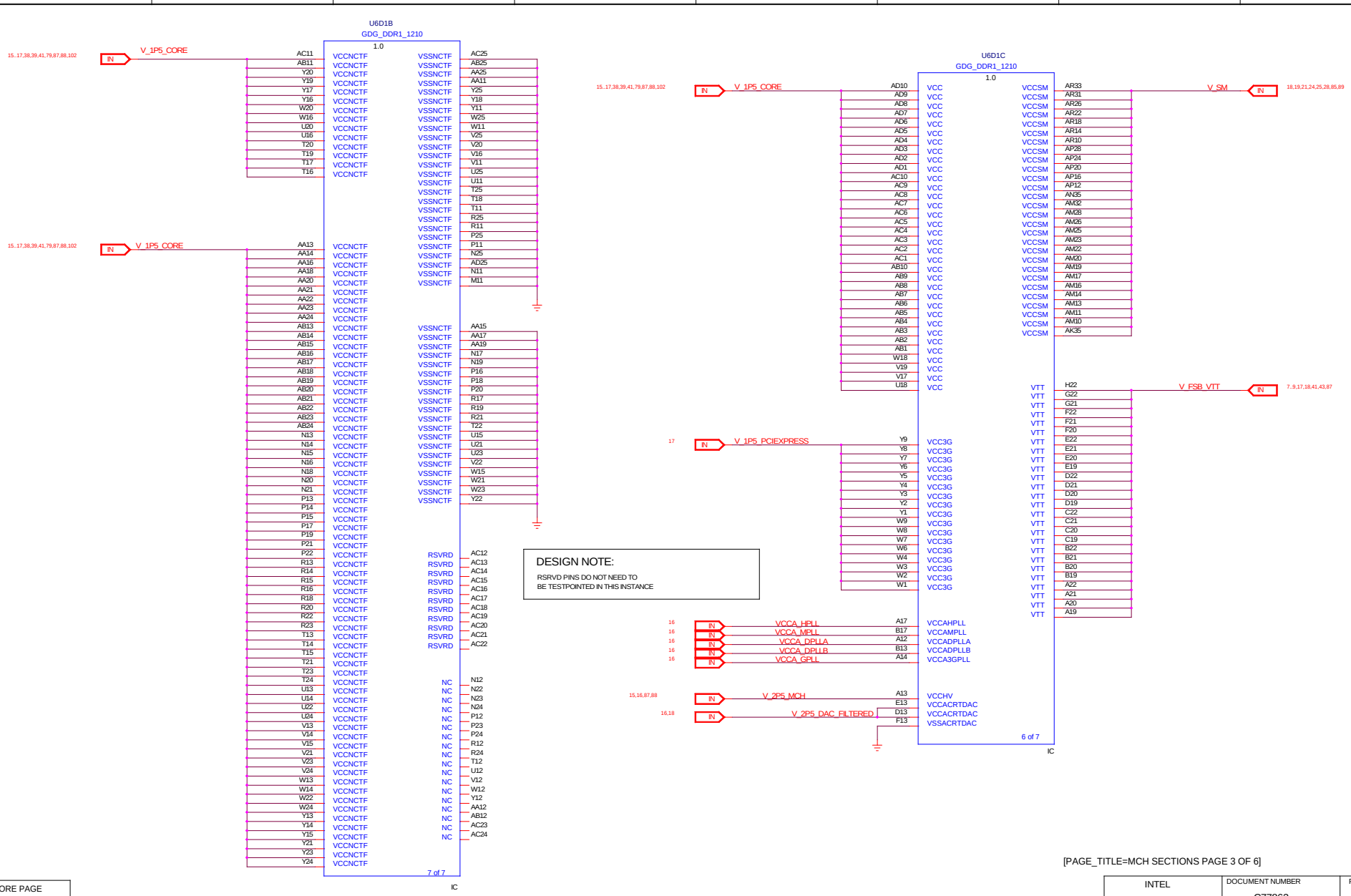
SDVO CTRL DATA

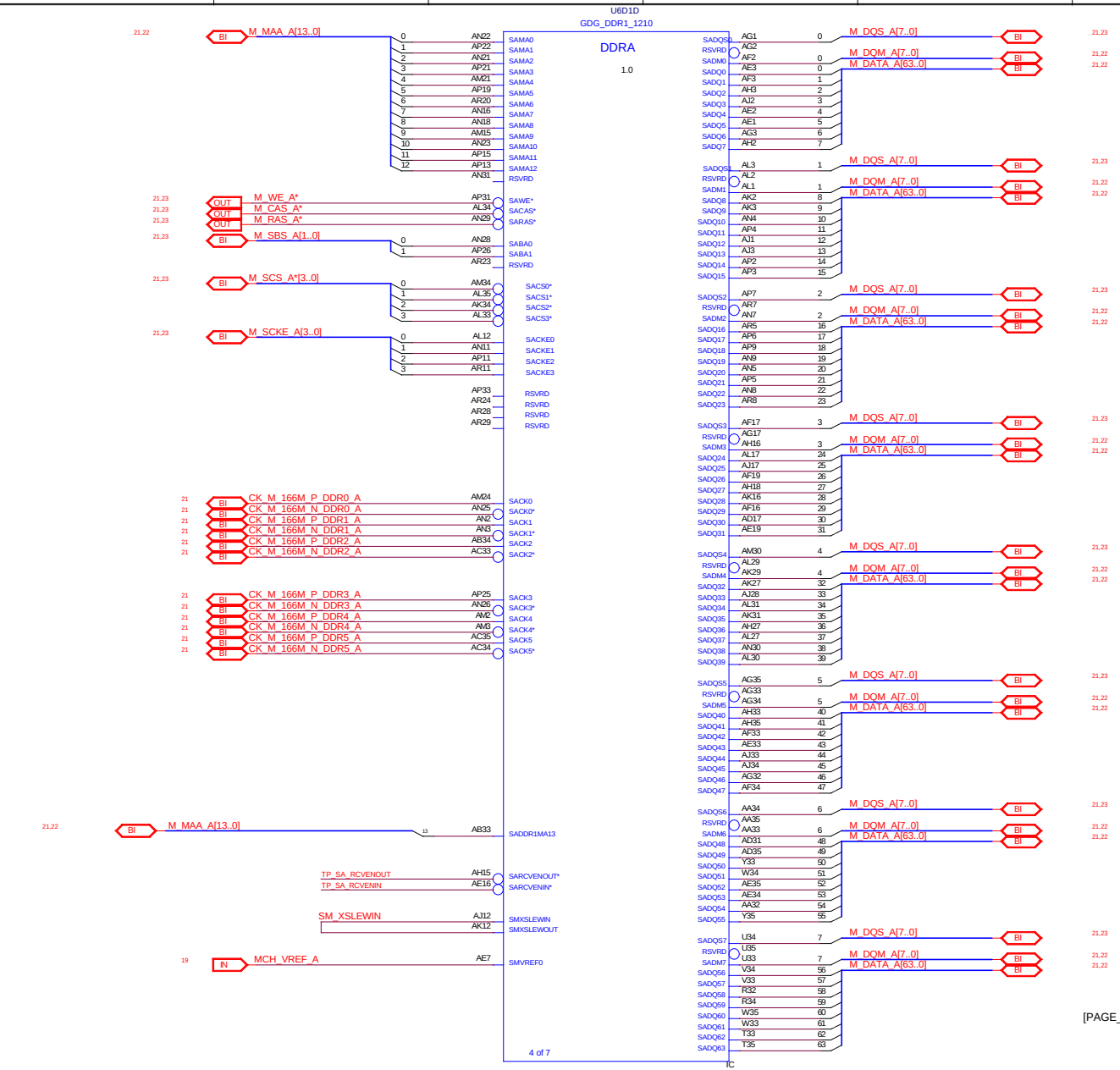
1	SDVO CARD PRESENT, PEG DISABLED
0	SDVO DISABLED (DEFAULT)

CORE PAGE

[PAGE_TITLE=MCH SECTIONS PAGE 2 OF 6]

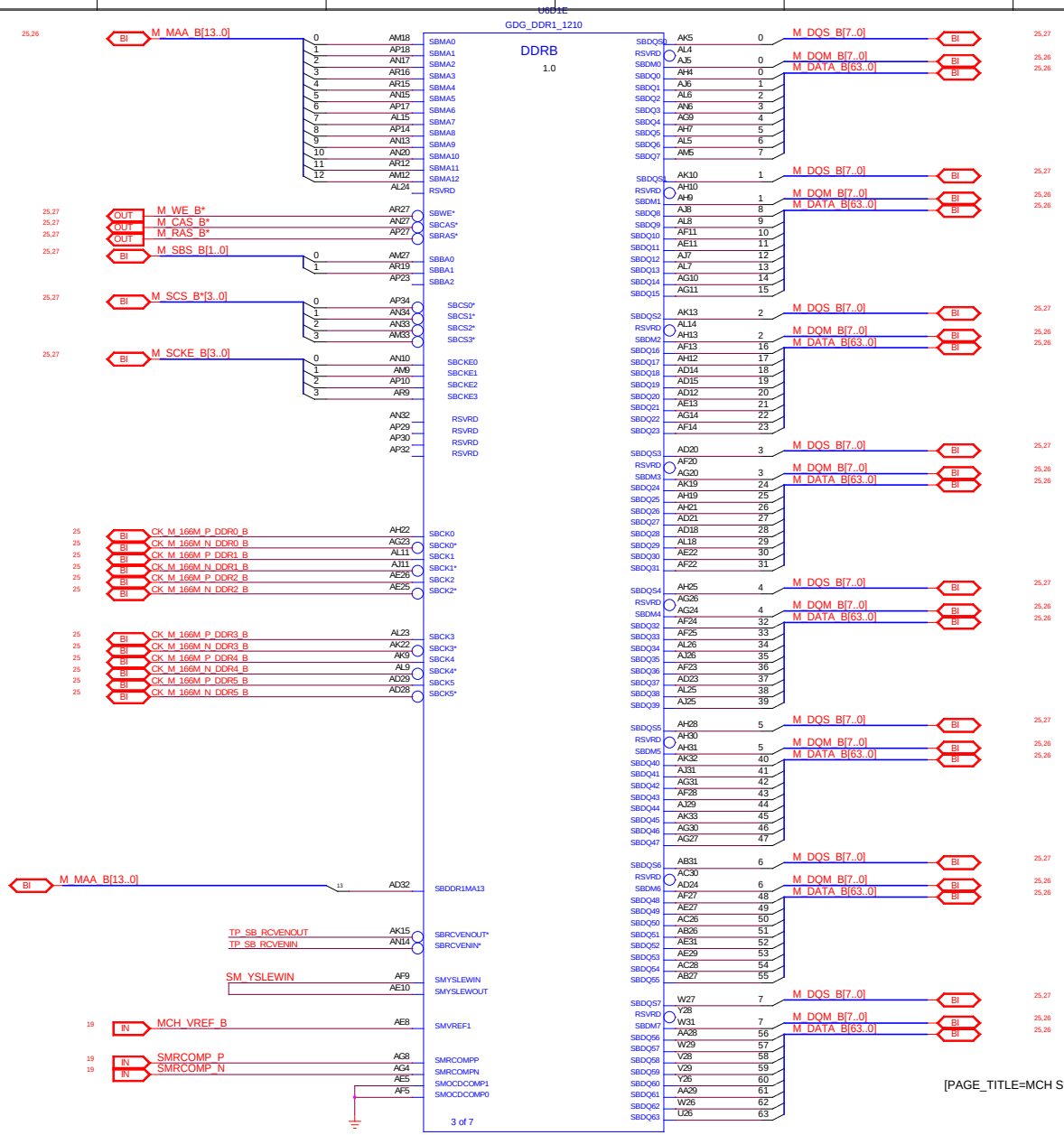
<XR_PAGE_TITLE>





CORE PAGE

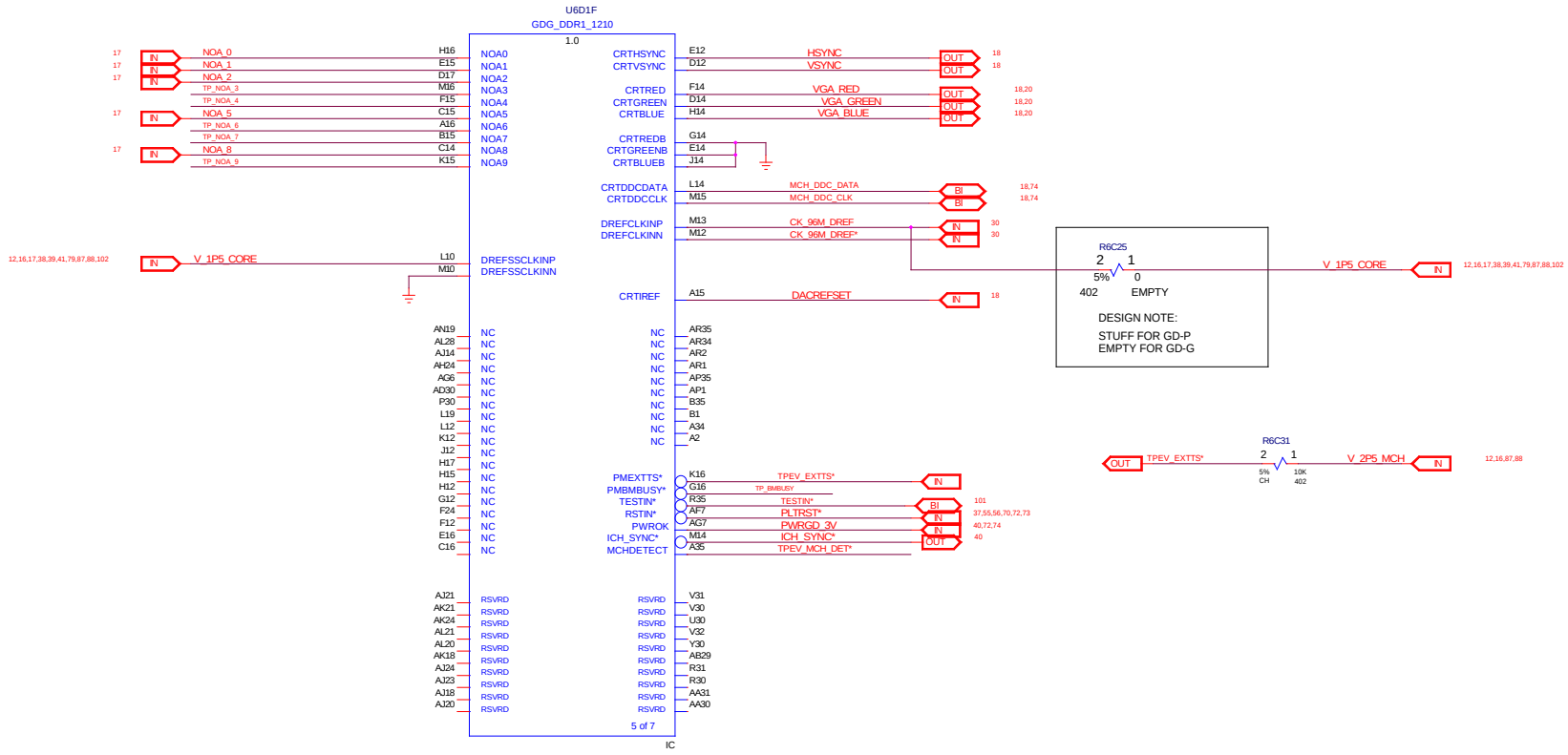
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	13	4.0



[PAGE_TITLE=MCH SECTIONS PAGE 5 OF 6]

CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	14	4.0



R6C25
2 1
5%
0
402 EMPTY

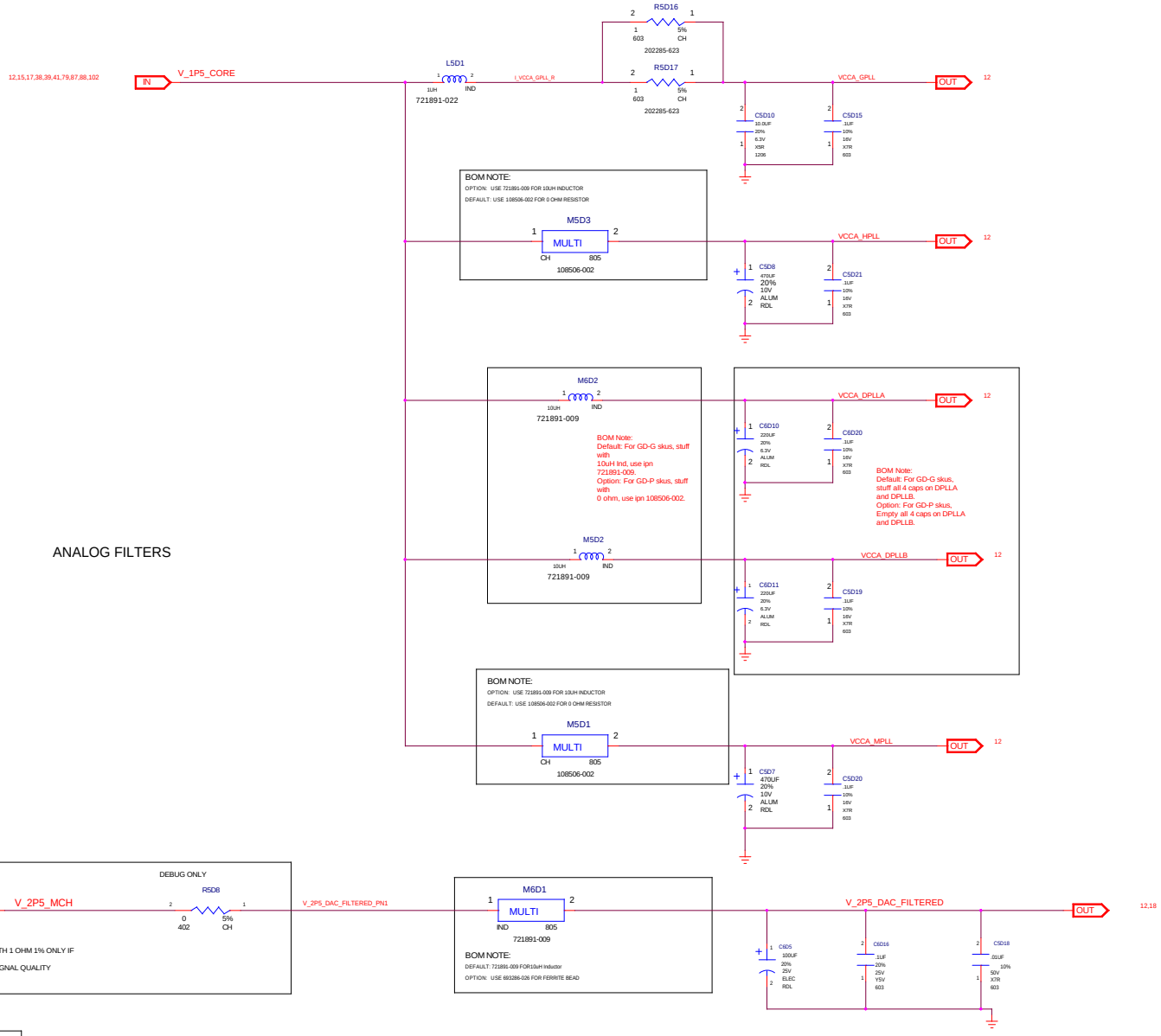
DESIGN NOTE:
STUFF FOR GD-P
EMPTY FOR GD-G

R6C31
2 1
5% 10K
CH 402
TPEV_EXTTS* V_2P5_MCH

[PAGE_TITLE=MCH SECTIONS PAGE 6 OF 6]

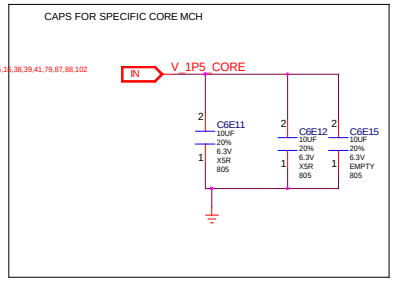
CORE PAGE

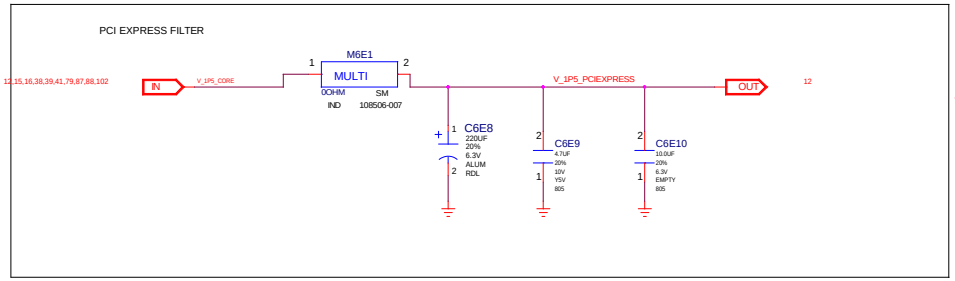
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	15	4.0

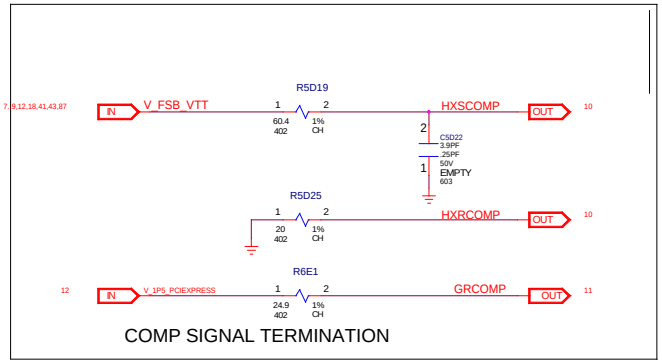


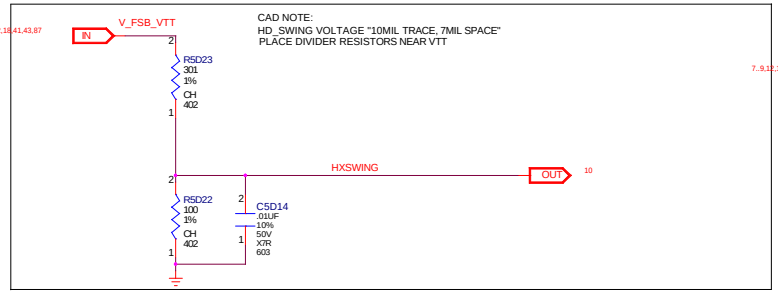
[PAGE_TITLE=MCH 2P5_DAC & 1P5 FILTER]

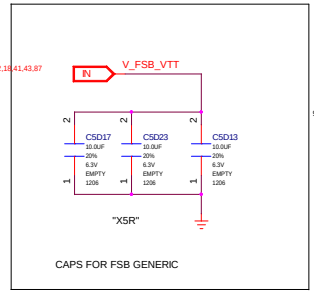
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	16	4.0

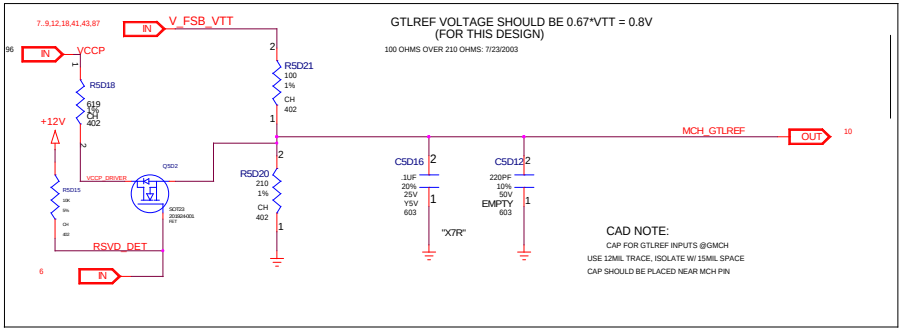






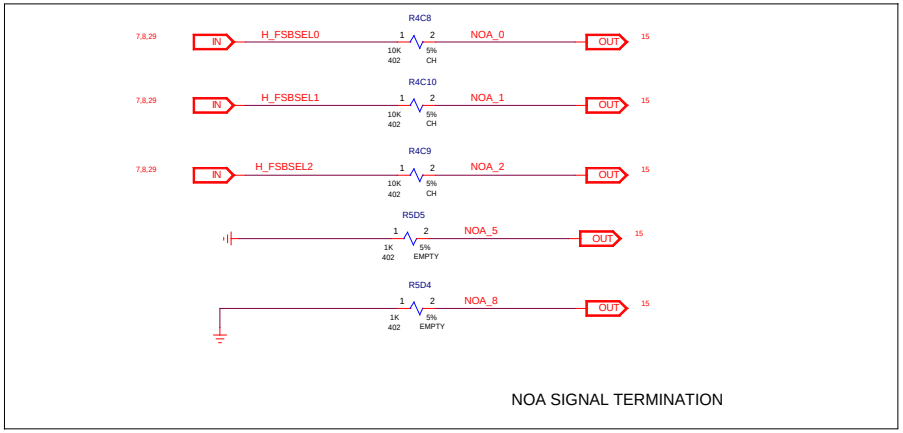






NOA	H	L	DESCRIPTION
0	SEE BSEL TABLE		BSEL0
1	SEE BSEL TABLE		BSEL1
2	SEE BSEL TABLE		BSEL2
3	NORM	ALL-Z	ALL-Z TEST MODE
4	NORM	XOR	XOR CHAIN
5	DDR1	DDR2	MEMORY TYPE
6	NORM	REVERSE	PCI-EXPRESS LANE REVERSAL
7	DIS	ENABLE	FSB HARDWARE STRAPS
8	NEW LTSSM	OLD LTSSM	LTSSM MODE (1.0 OLD, 1.0A NEW)
9	NORM	BYPASS	ICH PCI-EXPRESS RST BYPASS

3,4,5,6,7,8,9 ALL HAVE INTERNAL PULL-UP

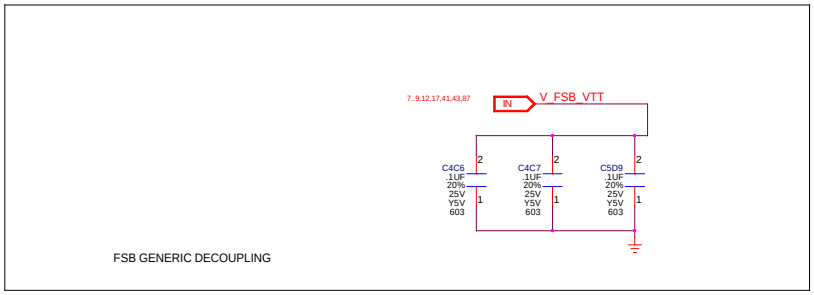


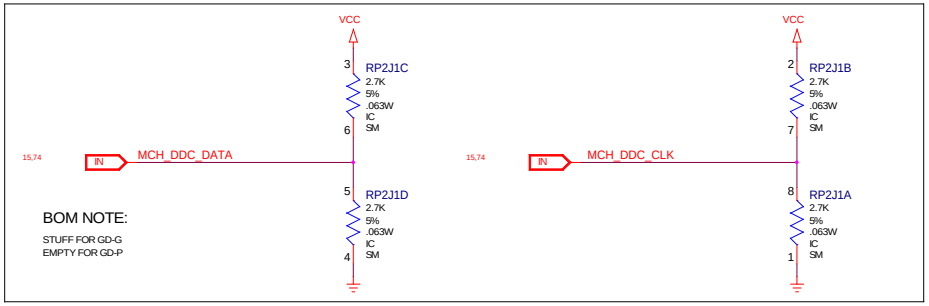
BSEL TABLE

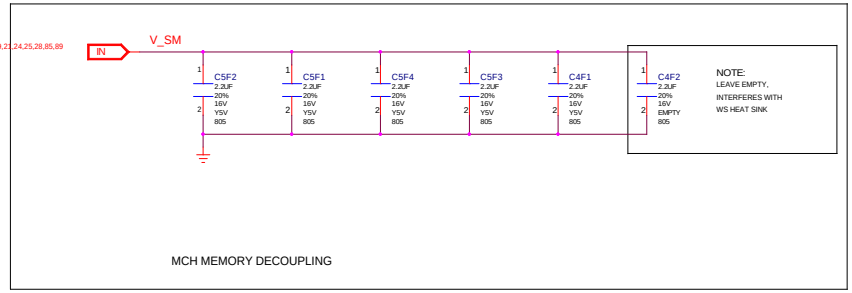
2	1	0	PSB FREQUENCY
0	0	0	267 MHZ (1067)
0	0	1	133 MHZ (533)
0	1	0	200 MHZ (800)
0	1	1	167 MHZ (667)
1	0	0	333 MHZ (RSVD)
1	0	1	100 MHZ (400)
1	1	0	400 MHZ (RSVD)
1	1	1	RESERVED

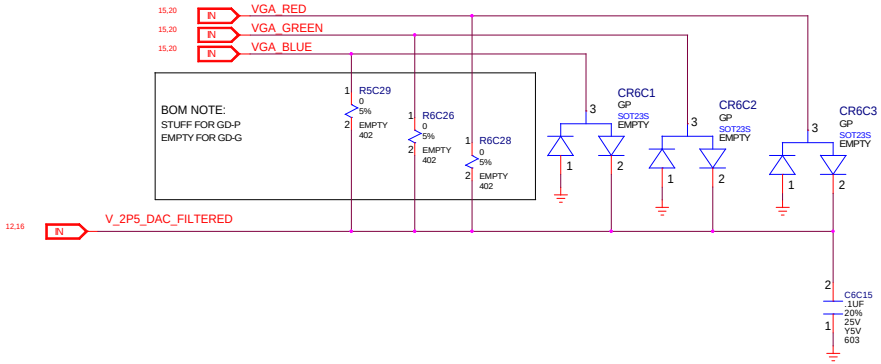
CORE PAGE

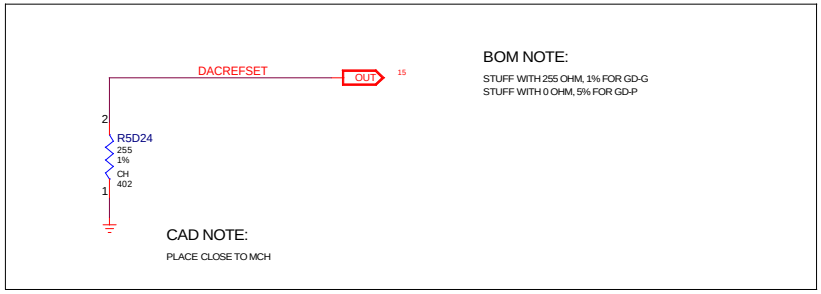
[PAGE_TITLE=MCH DECOUPLING AND COMP]

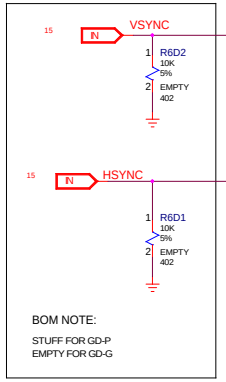


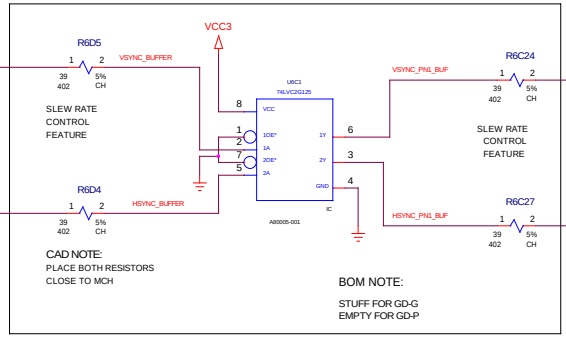


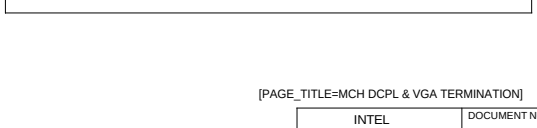


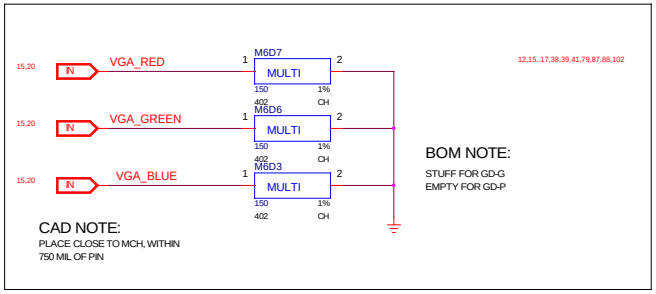


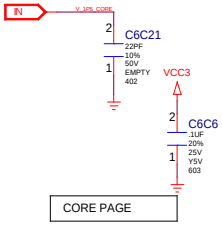






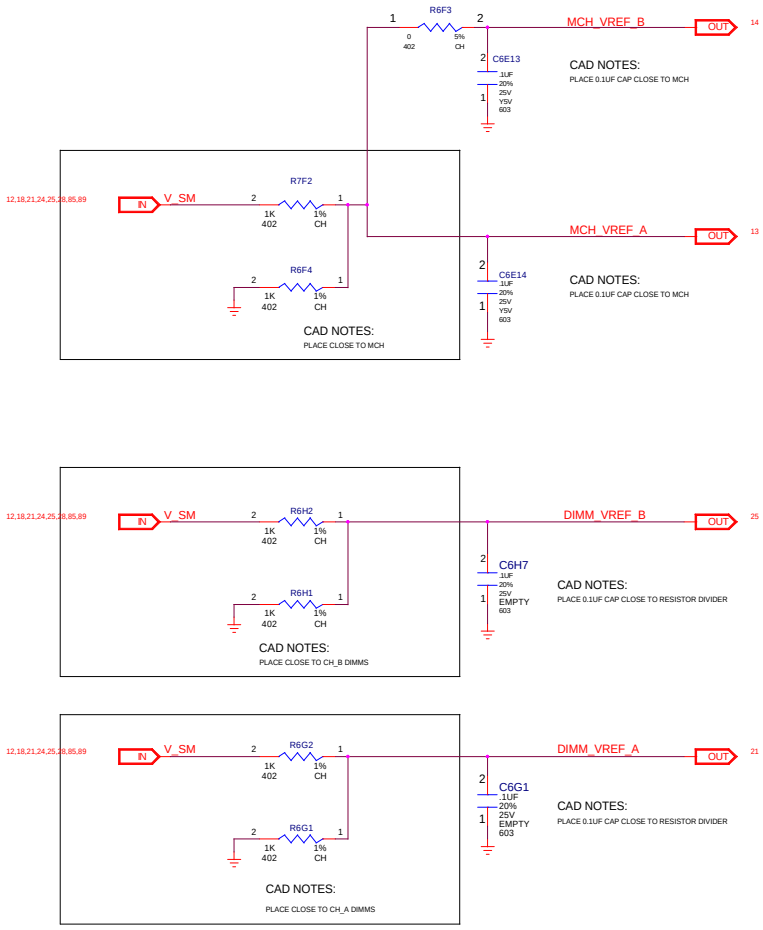


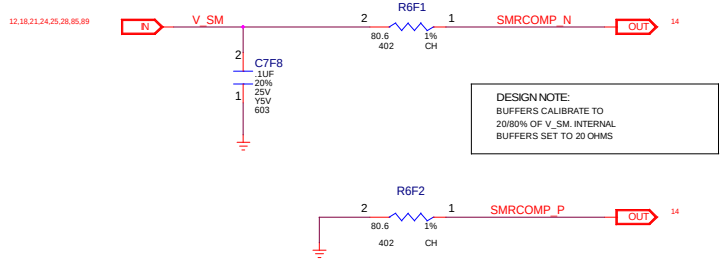




[PAGE_TITLE=MCH DCPL & VGA TERMINATION]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	18	4.0





CORE PAGE

[PAGE_TITLE=MCH CHIPSET TERMINATION]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	19	4.0

<XR_PAGE_TITLE>

BOM NOTE:
DEFAULT: STUFF WITH FERRITE BEAD (693286-006) FOR 5 POINT FILTER
OPTION: STUFF 0 OHM 0603 FOR 3 POINT FILTER

VGA_RED
VGA_GREEN
VGA_BLUE
HSYNC_3V
VSYNC_3V

M3A1 MULTI FB 603
M3A2 MULTI FB 603
M3A3 MULTI FB 603
M3A4 MULTI CH 805

FB3A2 FB4A1 FB3A1 693286-006 "47 OHM" FB

BOM NOTE:
STUFF WITH 3.3PF (A35094-006) FOR 3 POINT FILTER
STUFF WITH 10PF (A36094-001) FOR 5 POINT FILTER

C4A13 C4A12 C4A6 10PF 5% 50V COG 402

BOM NOTE:
STUFF WITH 3.3PF (A35094-006) FOR 3 POINT FILTER
STUFF WITH 22PF (A36095-006) FOR 5 POINT FILTER

C3A14 22PF 10% 50V NPO 402
C4A9 C4A4 22PF 10% 50V NPO 402

BOM NOTE:
EMPTY FOR 3 POINT FILTER
STUFF WITH 10PF (A36094-001) FOR 5 POINT FILTER

C3A1 A36094-001 "COG"
C4A8 "COG"
C4A2 "COG"

CAD NOTE:
PLACE RESISTORS CLOSE TO FILTERS (CAPS/FERITE-BEADS)

R4A8 R4A6 R4A1 150 1% CH 402

VCC
RT3A1 THRMSTR VDO_THERM_PN1
C3A2 1UF 20% 25V Y5V 603

J3A1 RCPT
VDO_RED_L
VDO_THERM_9
VDO_GREEN_L
VDO_BLUE_L
TP_VDOCONN_11_CORE
TP_VDOCONN_4_CORE

C4A3 C4A1 100PF 5% 50V EMPTY 402

R4A3 R4A5 2.2K 5% CH 402
R4A4 R4A2 100 5% CH 402

DDCSDA_5V
DDCSCL_5V
VDO_MONID1_R
VDO_MONID2_R

I36 CR4A2 TVS6_2V 6.2V EMPTY

C4A7 C4A5 100PF 5% 50V EMPTY 402

CORE PAGE

COMPONENTS ARE DFM29

[PAGE_TITLE=VGA CONNECTOR]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	20	4.0

<XR_PAGE_TITLE>

DDR CHANNEL A DIMM 1

BOM NOTE:

USE A87935-007 FOR
BLACK CONN WITH WHITE TABS

USE A87935-008 FOR
BLACK CONN WITH BLACK TABS

J6G2
DIMM2P_184_1Gb

I2C = 001

M_DATA_A[63..0]
M_WE_A*
M_RAS_A*
M_CAS_A*
M_MAA_A[13..0]
M_DQM_A[7..0]
M_DQS_A[7..0]
M_SCS_A*[3..0]
CK_M_166M_P_DDR3_A
CK_M_166M_N_DDR3_A
M_SCKE_A[3..0]
M_SBS_A[1..0]
V_SM

CK_M_166M_P_DDR4_A
CK_M_166M_N_DDR4_A
CK_M_166M_N_DDR5_A
CK_M_166M_P_DDR5_A

TP_DIMM1_SCS2*
TP_DIMM1_SCS3*
TP_VDDID_82_DIMM1_A
TP_WP_90_DIMM1_A
TP_RESET_10_DIMM1_A
TP_FETEN_103_DIMM1_A
TP_BA2_113_DIMM1_A

C6G3
1UF
20%
25V
Y5V
603
NEAR DIMM PIN

SMB_CLK_MAIN
SMB_DATA_MAIN
DIMM_VREF_A

DDR CHANNEL A DIMM 0

BOM NOTE:

USE A87935-006 FOR
BLUE CONN WITH WHITE TABS

USE A87935-007 FOR
BLACK CONN WITH WHITE TABS

J6G1
DIMM2P_184_1Gb

I2C = 000

M_DATA_A[63..0]
M_WE_A*
M_RAS_A*
M_CAS_A*
M_MAA_A[13..0]
M_DQM_A[7..0]
M_DQS_A[7..0]
M_SCS_A*[3..0]
CK_M_166M_P_DDR0_A
CK_M_166M_N_DDR0_A
M_SCKE_A[3..0]
M_SBS_A[1..0]
V_SM

CK_M_166M_P_DDR1_A
CK_M_166M_N_DDR1_A
CK_M_166M_N_DDR2_A
CK_M_166M_P_DDR2_A

TP_DIMM0_SCS2*
TP_DIMM0_SCS3*
TP_VDDID_82_DIMM0_A
TP_WP_90_DIMM0_A
TP_RESET_10_DIMM0_A
TP_FETEN_103_DIMM0_A
TP_BA2_113_DIMM0_A

C6G2
1UF
20%
25V
Y5V
603
NEAR DIMM PIN

SMB_CLK_MAIN
SMB_DATA_MAIN
DIMM_VREF_A

[PAGE_TITLE=DDR1 DIMM-A 0/1]

CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	21	4.0

DDR RESISTOR TERMINATION

SPARE SECTIONS

RP3G3D 4 5 56 SM 5% .063W IC

CAD NOTE: FLOOD VTT THROUGH PIN 5

DESIGN NOTE;

KEEP 603 RESISTORS

DO NOT CHANGE TO 402

23,24,26..28,89 IN V_SM_VTT

M_DQM_A[7..0] 23,21 BI

M_DATA_A[63..0] 23,21 BI

M_MAA_A[13..0] 23,21 BI

RP6G2D 0 4 5 56 SM 5% .063W IC
RP5G1A 1 1 8 56 SM 5% .063W IC
RP5G5C 2 3 6 56 SM 5% .063W IC
RP4G3A 3 1 8 56 SM 5% .063W IC
RP3G2B 4 2 7 56 SM 5% .063W IC
R2G1 5 2 1 56 603 5% CH
RP2G4D 6 4 5 56 SM 5% .063W IC
RP2G6B 7 2 7 56 SM 5% .063W IC

RP1G1C 63 3 6 56 SM 5% .063W IC
RP1G1D 62 4 5 56 SM 5% .063W IC
RP2G5A 61 1 8 56 SM 5% .063W IC
RP2G5B 60 2 7 56 SM 5% .063W IC
RP1G1A 59 1 8 56 SM 5% .063W IC
RP1G1B 58 2 7 56 SM 5% .063W IC
RP2G6C 57 3 6 56 SM 5% .063W IC
RP2G6D 56 4 5 56 SM 5% .063W IC
RP2G4A 55 1 8 56 SM 5% .063W IC
RP2G4B 54 2 7 56 SM 5% .063W IC
RP2G3C 53 3 6 56 SM 5% .063W IC
RP2G3D 52 4 5 56 SM 5% .063W IC
RP2G5C 51 3 6 56 SM 5% .063W IC
RP2G5D 50 4 5 56 SM 5% .063W IC
RP2G3A 49 1 8 56 SM 5% .063W IC
RP2G3B 48 2 7 56 SM 5% .063W IC

RP2G2C 47 3 6 56 SM 5% .063W IC
RP2G2D 46 4 5 56 SM 5% .063W IC
R3G2 45 2 1 56 603 5% CH
RP3G3A 44 1 8 56 SM 5% .063W IC
RP2G2A 43 1 8 56 SM 5% .063W IC
RP2G2B 42 2 7 56 SM 5% .063W IC
R3G4 41 2 1 56 603 5% CH
R3G3 40 2 1 56 603 5% CH
RP3G2A 39 1 8 56 SM 5% .063W IC
RP3G2D 38 4 5 56 SM 5% .063W IC
RP3G1B 37 2 7 56 SM 5% .063W IC
RP3G1C 36 3 6 56 SM 5% .063W IC
RP3G3B 35 2 7 56 SM 5% .063W IC
RP3G3C 34 3 6 56 SM 5% .063W IC
RP3G1D 33 4 5 56 SM 5% .063W IC
RP3G1A 32 1 8 56 SM 5% .063W IC

RP4G4B 31 2 7 56 SM 5% .063W IC
RP4G4D 30 4 5 56 SM 5% .063W IC
RP4G2A 29 1 8 56 SM 5% .063W IC
RP4G2B 28 2 7 56 SM 5% .063W IC
RP4G4A 27 1 8 56 SM 5% .063W IC
RP4G4C 26 3 6 56 SM 5% .063W IC
RP4G3B 25 2 7 56 SM 5% .063W IC
RP4G3D 24 4 5 56 SM 5% .063W IC
RP5G5A 23 1 8 56 SM 5% .063W IC
RP5G5B 22 2 7 56 SM 5% .063W IC
RP5G4C 21 3 6 56 SM 5% .063W IC
RP5G4D 20 4 5 56 SM 5% .063W IC
RP4G2C 19 3 6 56 SM 5% .063W IC
RP4G2D 18 4 5 56 SM 5% .063W IC
RP5G4A 17 1 8 56 SM 5% .063W IC
RP5G4B 16 2 7 56 SM 5% .063W IC

RP5G2C 15 3 6 56 SM 5% .063W IC
RP5G2D 14 4 5 56 SM 5% .063W IC
RP6G3A 13 1 8 56 SM 5% .063W IC
RP6G3B 12 2 7 56 SM 5% .063W IC
RP5G2A 11 1 8 56 SM 5% .063W IC
RP5G2B 10 2 7 56 SM 5% .063W IC
RP5G1C 9 3 6 56 SM 5% .063W IC
RP5G1D 8 4 5 56 SM 5% .063W IC
RP6G2A 7 1 8 56 SM 5% .063W IC
RP6G2B 6 2 7 56 SM 5% .063W IC
RP6G1C 5 3 6 56 SM 5% .063W IC
RP6G1D 4 4 5 56 SM 5% .063W IC
RP6G3C 3 3 6 56 SM 5% .063W IC
RP6G3D 2 4 5 56 SM 5% .063W IC
RP6G1A 1 1 8 56 SM 5% .063W IC
RP6G1B 0 2 7 56 SM 5% .063W IC

R2G3 13 2 1 47 603 5% CH
R5G1 12 2 1 47 603 5% CH
R5G2 11 2 1 47 603 5% CH
RP4G5A 10 1 8 47 SM 5% .063W IC
R5G3 9 2 1 47 603 5% CH
RP4G1C 8 3 6 47 SM 5% .063W IC
RP4G1D 7 4 5 47 SM 5% .063W IC
RP4G1A 6 1 8 47 SM 5% .063W IC
RP4G1B 5 2 7 47 SM 5% .063W IC
R4G1 4 2 1 47 603 5% CH
R4G2 3 2 1 47 603 5% CH
RP4G5D 2 4 5 47 SM 5% .063W IC
RP4G5C 1 3 6 47 SM 5% .063W IC
RP4G5B 0 2 7 47 SM 5% .063W IC

[PAGE_TITLE=DDR1 DIMM-A 0/1 TERM]

CORE PAGE

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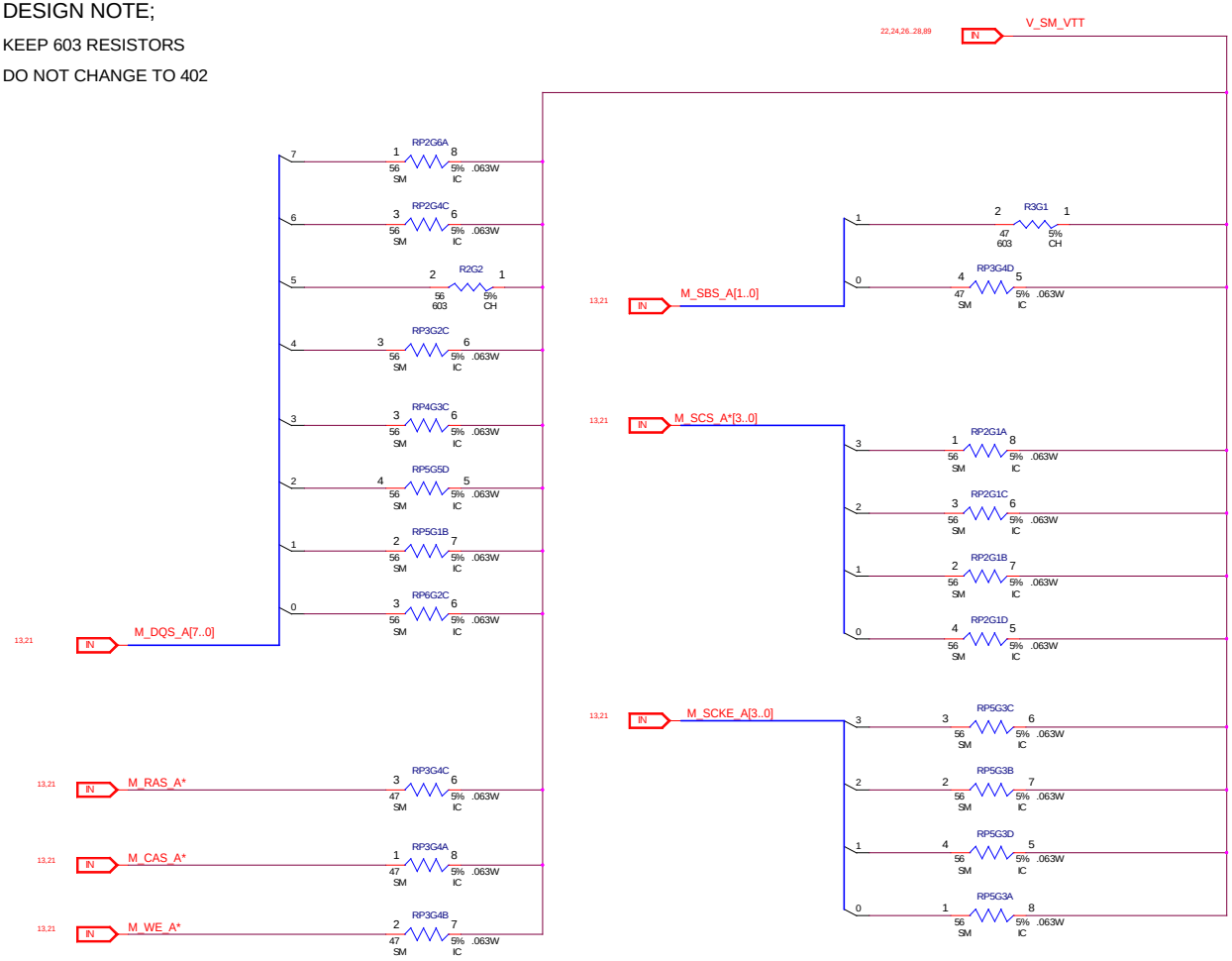
CHANNEL A

DESIGN NOTE;

KEEP 603 RESISTORS

DO NOT CHANGE TO 402



DDR RESISTOR TERMINATION

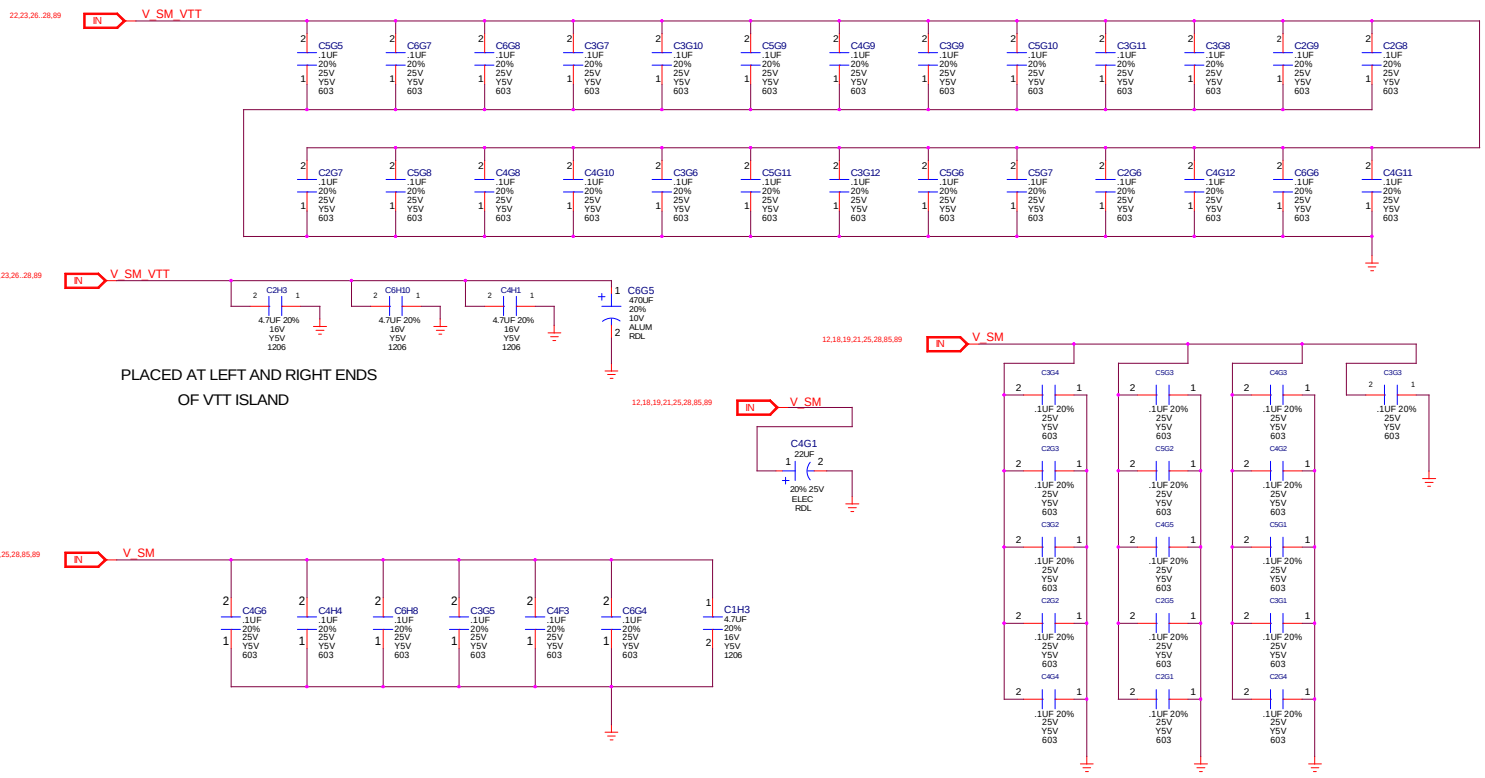
CORE PAGE

[PAGE_TITLE=DDR1 DIMM-A 0/1 TERM]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	23	4.0

DDR CHANNEL A

DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS



CHANNEL A

DIMM TO MCH
BIT SWAPPING

DIMM	MCH
DQ0	DQ0
DQ1	DQ1
DQ2	DQ2
DQ3	DQ3
DQ4	DQ4
DQ5	DQ5
DQ6	DQ6
DQ7	DQ7
DQ8	DQ13
DQ9	DQ9
DQ10	DQ10
DQ11	DQ11
DQ12	DQ12
DQ13	DQ8
DQ14	DQ14
DQ15	DQ15
DQ16	DQ21
DQ17	DQ16
DQ18	DQ22
DQ19	DQ18
DQ20	DQ20
DQ21	DQ17
DQ22	DQ23
DQ23	DQ19
DQ24	DQ28
DQ25	DQ24
DQ26	DQ30
DQ27	DQ26
DQ28	DQ29
DQ29	DQ25
DQ30	DQ31
DQ31	DQ27

DIMM	MCH
DQ32	DQ36
DQ33	DQ32
DQ34	DQ38
DQ35	DQ35
DQ36	DQ37
DQ37	DQ33
DQ38	DQ39
DQ39	DQ34
DQ40	DQ45
DQ41	DQ41
DQ42	DQ46
DQ43	DQ47
DQ44	DQ44
DQ45	DQ40
DQ46	DQ42
DQ47	DQ43
DQ48	DQ52
DQ49	DQ53
DQ50	DQ50
DQ51	DQ51
DQ52	DQ48
DQ53	DQ49
DQ54	DQ54
DQ55	DQ55
DQ56	DQ56
DQ57	DQ57
DQ58	DQ58
DQ59	DQ59
DQ60	DQ60
DQ61	DQ61
DQ62	DQ62
DQ63	DQ63

CORE PAGE

[PAGE_TITLE=DDR1 DIMM-A 0/1 TERM DCPL]

DDR CHANNEL B DIMM 1

J6H2
DIMM2P_184_1Gb

BOM NOTE:
USE A87935-007 FOR
BLACK CONN WITH WHITE TABS

USE A87935-008 FOR
BLACK CONN WITH BLACK TABS

DESIGN NOTE:
I2C = 011

M_DATA_B[63..0]
M_WE_B*
M_RAS_B*
M_CAS_B*
M_MAA_B[13..0]
M_DQM_B[7..0]
M_DQS_B[7..0]
M_SCS_B*[3..0]
CK_M_166M_P_DDR3_B
CK_M_166M_N_DDR3_B
M_SCKE_B[3..0]
M_SBS_B[1..0]
V_SM

CK_M_166M_P_DDR4_B
CK_M_166M_N_DDR4_B
CK_M_166M_N_DDR5_B
CK_M_166M_P_DDR5_B

V_SM
DIMM_VREF_B
SMB_CLK_MAIN
SMB_DATA_MAIN

C6H9
.1UF
20%
25V
Y5V
603
NEAR DIMM PIN

DDR CHANNEL B DIMM 0

J6H1
DIMM2P_184_1Gb

BOM NOTE:
USE A87935-006 FOR
BLUE CONN WITH WHITE TABS

USE A87935-007 FOR
BLACK CONN WITH WHITE TABS

DESIGN NOTE:
I2C = 010

M_DATA_B[63..0]
M_WE_B*
M_RAS_B*
M_CAS_B*
M_MAA_B[13..0]
M_DQM_B[7..0]
M_DQS_B[7..0]
M_SCS_B*[3..0]
CK_M_166M_P_DDR0_B
CK_M_166M_N_DDR0_B
M_SCKE_B[3..0]
M_SBS_B[1..0]
V_SM

CK_M_166M_P_DDR1_B
CK_M_166M_N_DDR1_B
CK_M_166M_N_DDR2_B
CK_M_166M_P_DDR2_B

V_SM
DIMM_VREF_B
SMB_CLK_MAIN
SMB_DATA_MAIN

C6H2
.1UF
20%
25V
Y5V
603
NEAR DIMM PIN

[PAGE_TITLE=DDR1 DIMM-B 0/1]

CORE PAGE

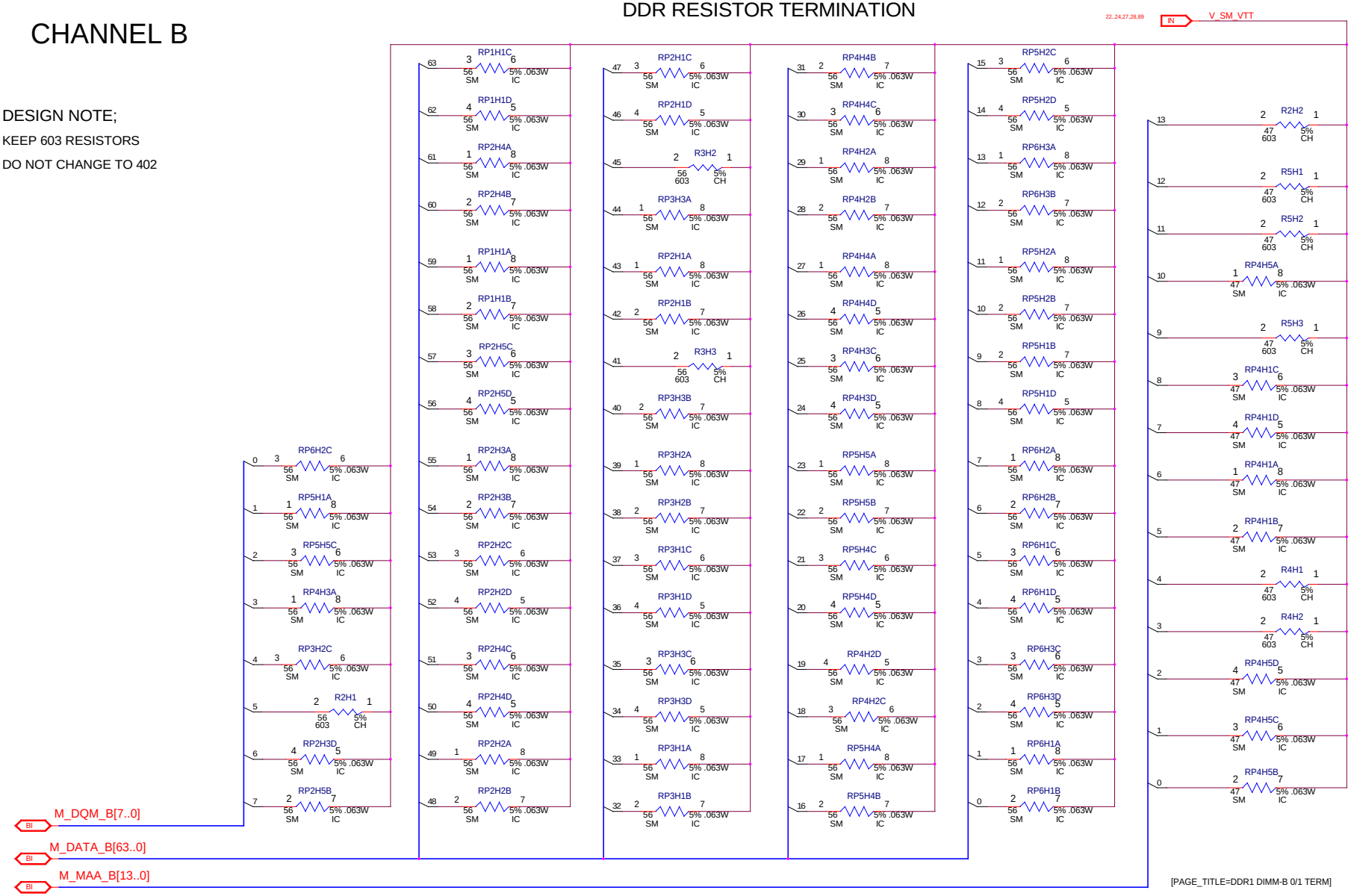
DDR RESISTOR TERMINATION

CHANNEL B

DESIGN NOTE;

KEEP 603 RESISTORS

DO NOT CHANGE TO 402



[PAGE_TITLE=DDR1 DIMM-B 0/1 TERM]

CORE PAGE

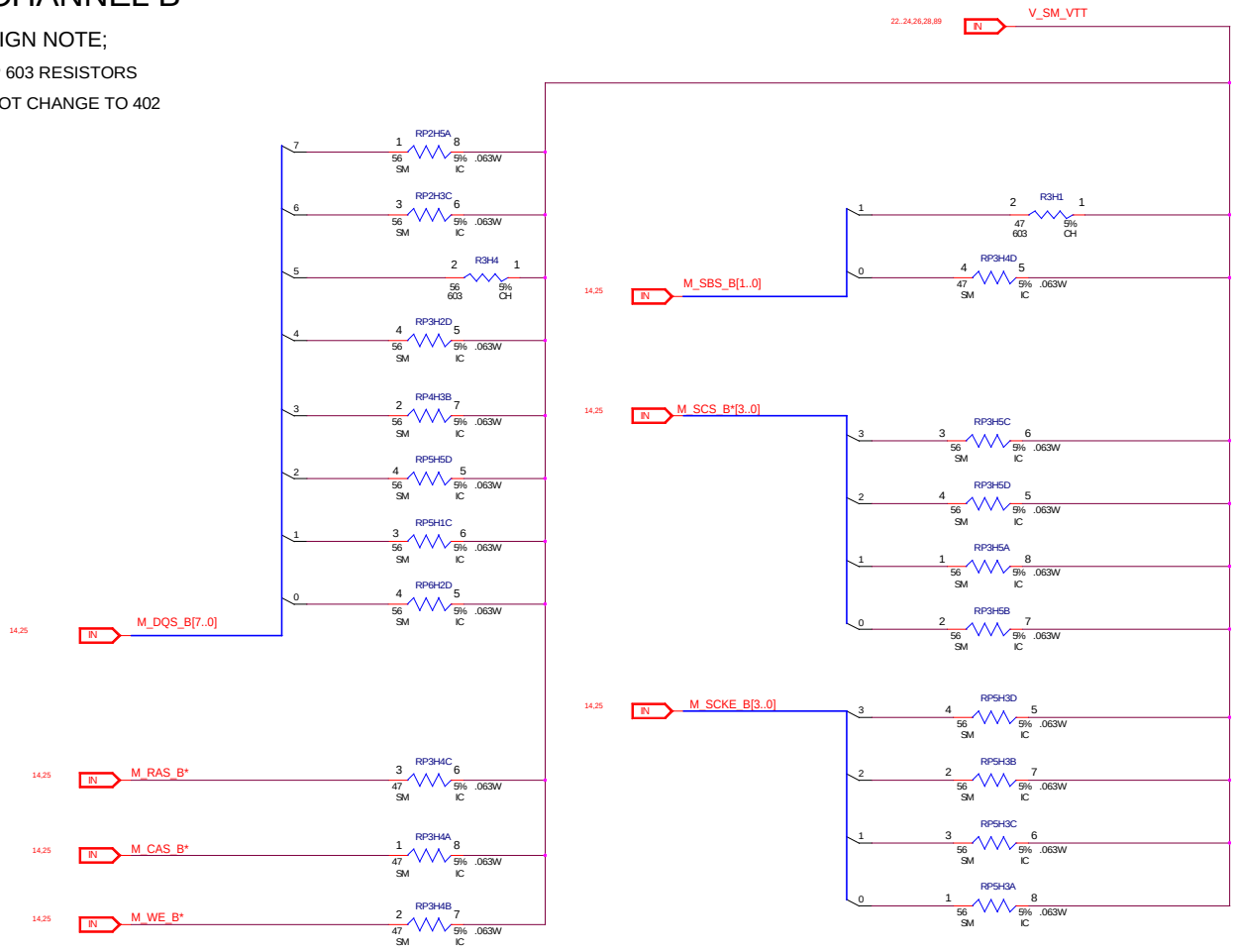
INTEL CONFIDENTIAL	DOCUMENT NUMBER C77862	PAGE 26	REV 4.0

CHANNEL B

DESIGN NOTE;

KEEP 603 RESISTORS

DO NOT CHANGE TO 402



DDR RESISTOR TERMINATION

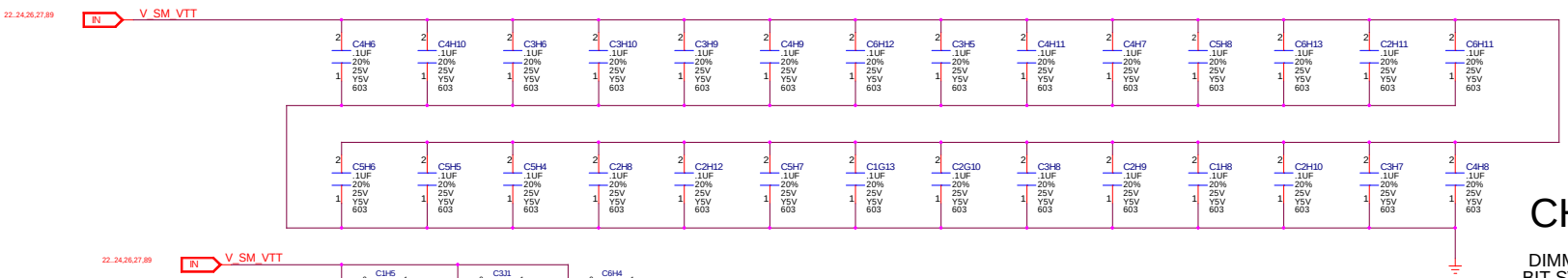
[PAGE_TITLE=DDR1 DIMM-B 0/1 TERM]

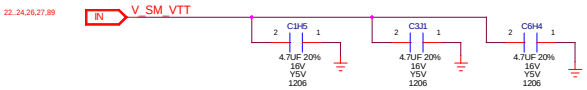
CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	27	4.0

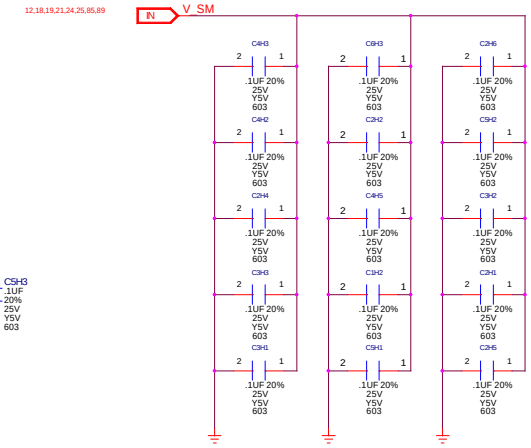
DDR CHANNEL B

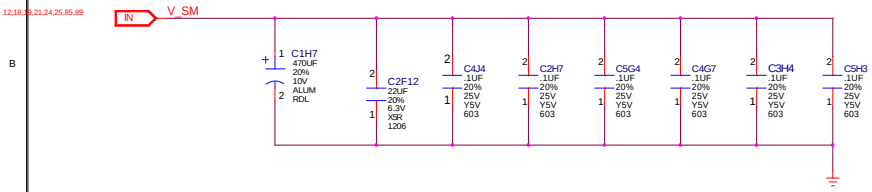
DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

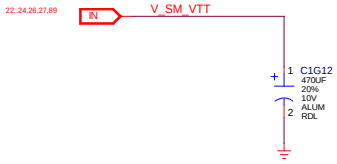




PLACED AT LEFT AND RIGHT ENDS
OF VTT ISLAND







CHANNEL B

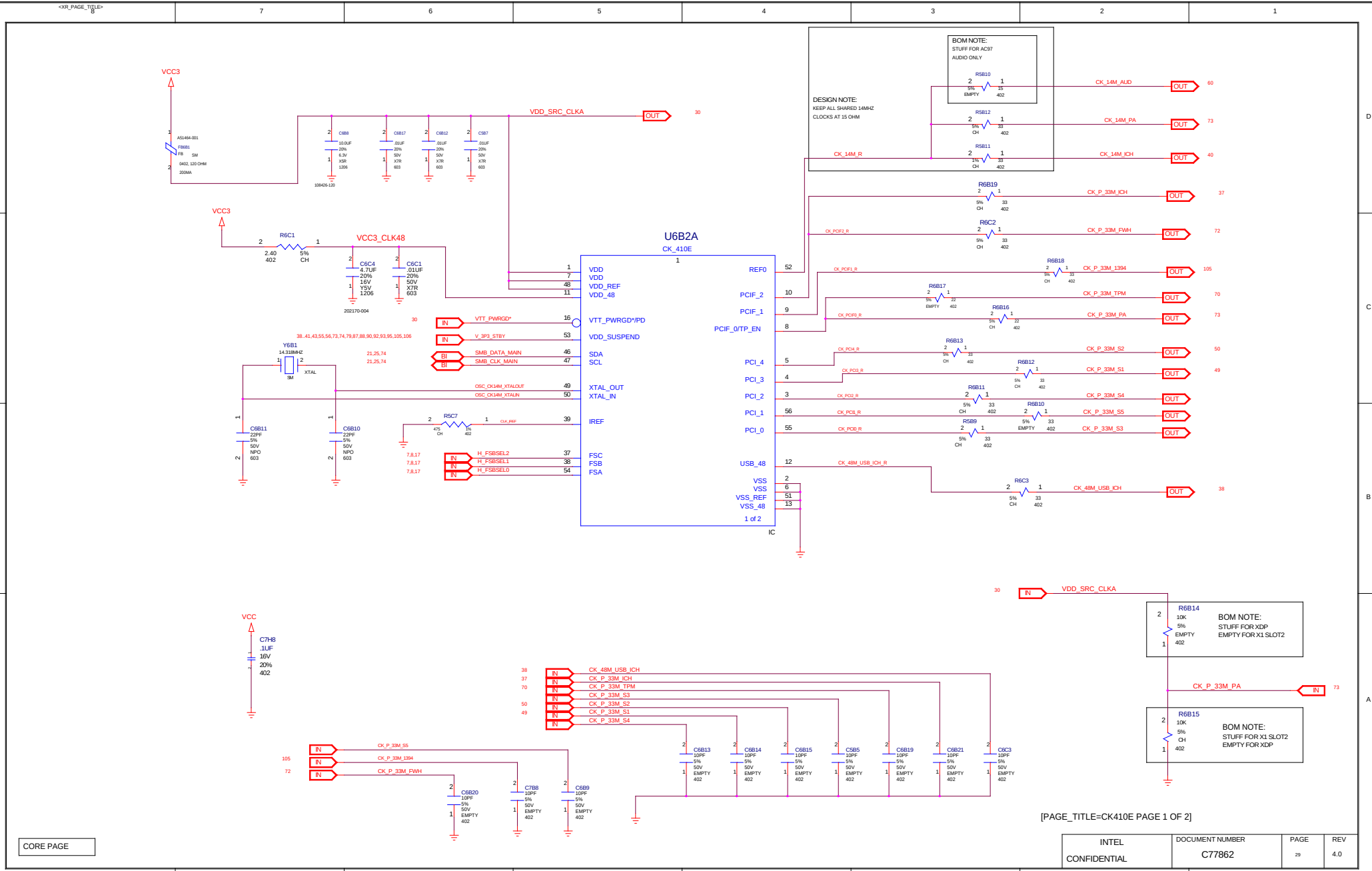
DIMM TO MCH
BIT SWAPPING

DIMM	MCH
DQ0	DQ5
DQ1	DQ1
DQ2	DQ6
DQ3	DQ3
DQ4	DQ4
DQ5	DQ0
DQ6	DQ7
DQ7	DQ2
DQ8	DQ12
DQ9	DQ13
DQ10	DQ10
DQ11	DQ11
DQ12	DQ8
DQ13	DQ9
DQ14	DQ14
DQ15	DQ15
DQ16	DQ21
DQ17	DQ16
DQ18	DQ23
DQ19	DQ18
DQ20	DQ20
DQ21	DQ17
DQ22	DQ22
DQ23	DQ19
DQ24	DQ28
DQ25	DQ24
DQ26	DQ30
DQ27	DQ26
DQ28	DQ29
DQ29	DQ25
DQ30	DQ31
DQ31	DQ27

DIMM	MCH
DQ32	DQ36
DQ33	DQ33
DQ34	DQ38
DQ35	DQ35
DQ36	DQ37
DQ37	DQ32
DQ38	DQ39
DQ39	DQ34
DQ40	DQ44
DQ41	DQ41
DQ42	DQ46
DQ43	DQ42
DQ44	DQ45
DQ45	DQ40
DQ46	DQ47
DQ47	DQ43
DQ48	DQ52
DQ49	DQ48
DQ50	DQ55
DQ51	DQ51
DQ52	DQ53
DQ53	DQ49
DQ54	DQ54
DQ55	DQ50
DQ56	DQ61
DQ57	DQ57
DQ58	DQ63
DQ59	DQ59
DQ60	DQ60
DQ61	DQ56
DQ62	DQ62
DQ63	DQ58

[PAGE_TITLE=DDR1 DIMM-B 0/1 DCPL]

CORE PAGE


BOM NOTE:
STUFF FOR AC97
AUDIO ONLY
DESIGN NOTE:
KEEP ALL SHARED 14MHZ
CLOCKS AT 15 OHM
U6B2A
CK_410E
VCC3
VCC3_CLK48
VDD_SRC_CLKA
VTT_PWRGD*
V_3P3_STBY
SMB_DATA_MAIN
SMB_CLK_MAIN
H_FSBSEL2
H_FSBSEL1
H_FSBSEL0
CK_48M_USB_ICH
CK_P_33M_ICH
CK_P_33M_TPM
CK_P_33M_S3
CK_P_33M_S2
CK_P_33M_S1
CK_P_33M_S4
CK_P_33M_S5
CK_P_33M_1394
CK_P_33M_FWH
CK_P_33M_PA
CK_14M_AUD
CK_14M_PA
CK_14M_ICH
CK_14M_R
CK_48M_USB_ICH
BOM NOTE:
STUFF FOR XDP
EMPTY FOR X1 SLOT2
BOM NOTE:
STUFF FOR X1 SLOT2
EMPTY FOR XDP
[PAGE_TITLE=CK410E PAGE 1 OF 2]
CORE PAGE
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
C77862
PAGE
29
REV
4.0

DESIGN NOTE:
STUFF FOR EVALUATION OF COST REDUCTION ON VOLTAGE SOURCE

CAD NOTE:
PLACE (1) PER PIN

CORE PAGE

LOCATION	X1 SLOT2	XDP
R5C12	STUFF	EMPTY
R5C13	STUFF	EMPTY
R5C15	EMPTY	STUFF
R5C16	EMPTY	STUFF

DESIGN NOTE:
REMOVE OFF-PAGE FOR UATX

DESIGN NOTE:
SATA MUST BE ON PIN_26, PIN_27

VREG FEATURE

[PAGE_TITLE=CK410E PAGE 2 OF 2]

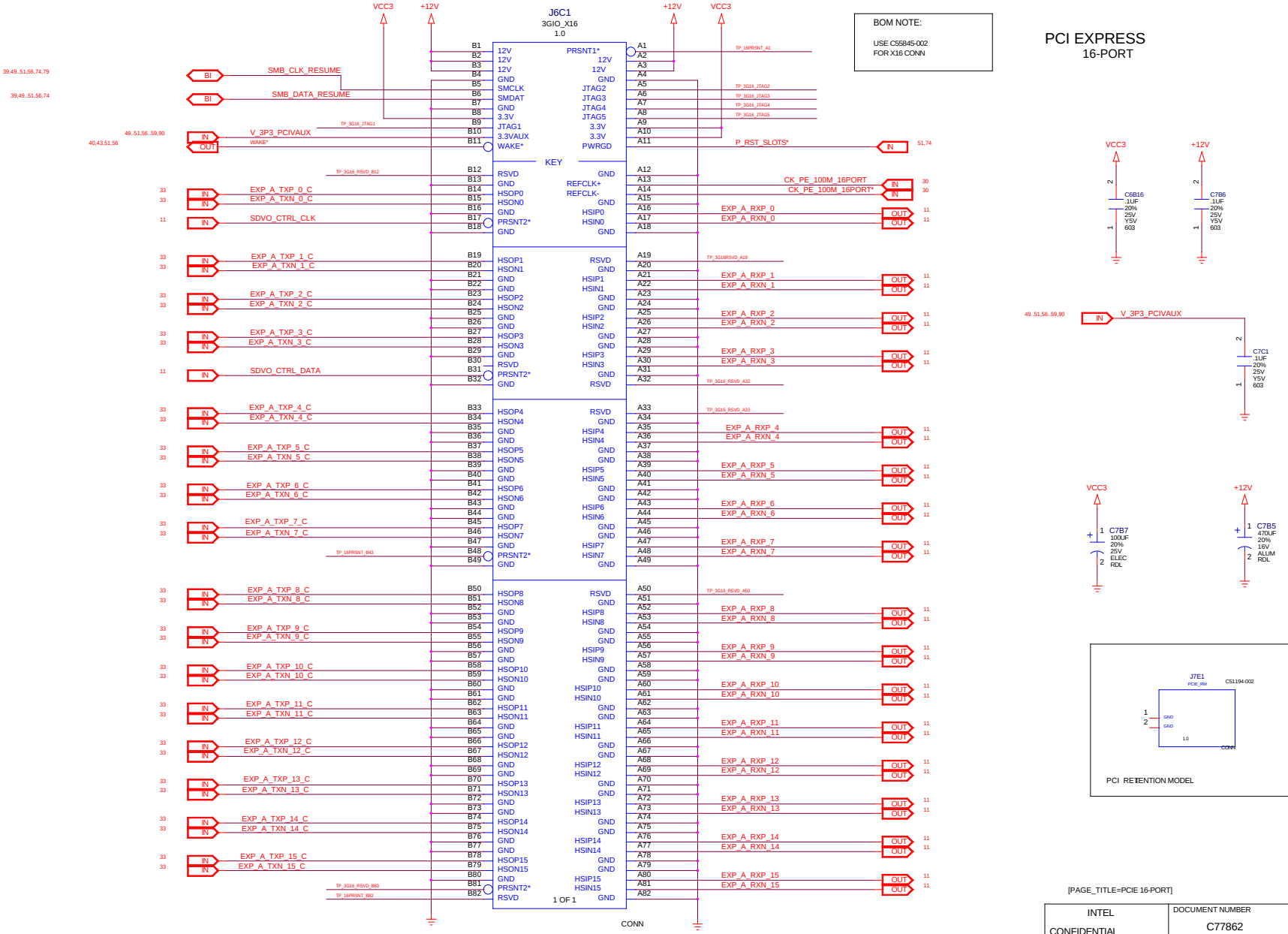
BLANK PAGE

[PAGE_TITLE=BLANK]

PCI EXPRESS 16-PORT

J6C1
3GIO_X16
1.0

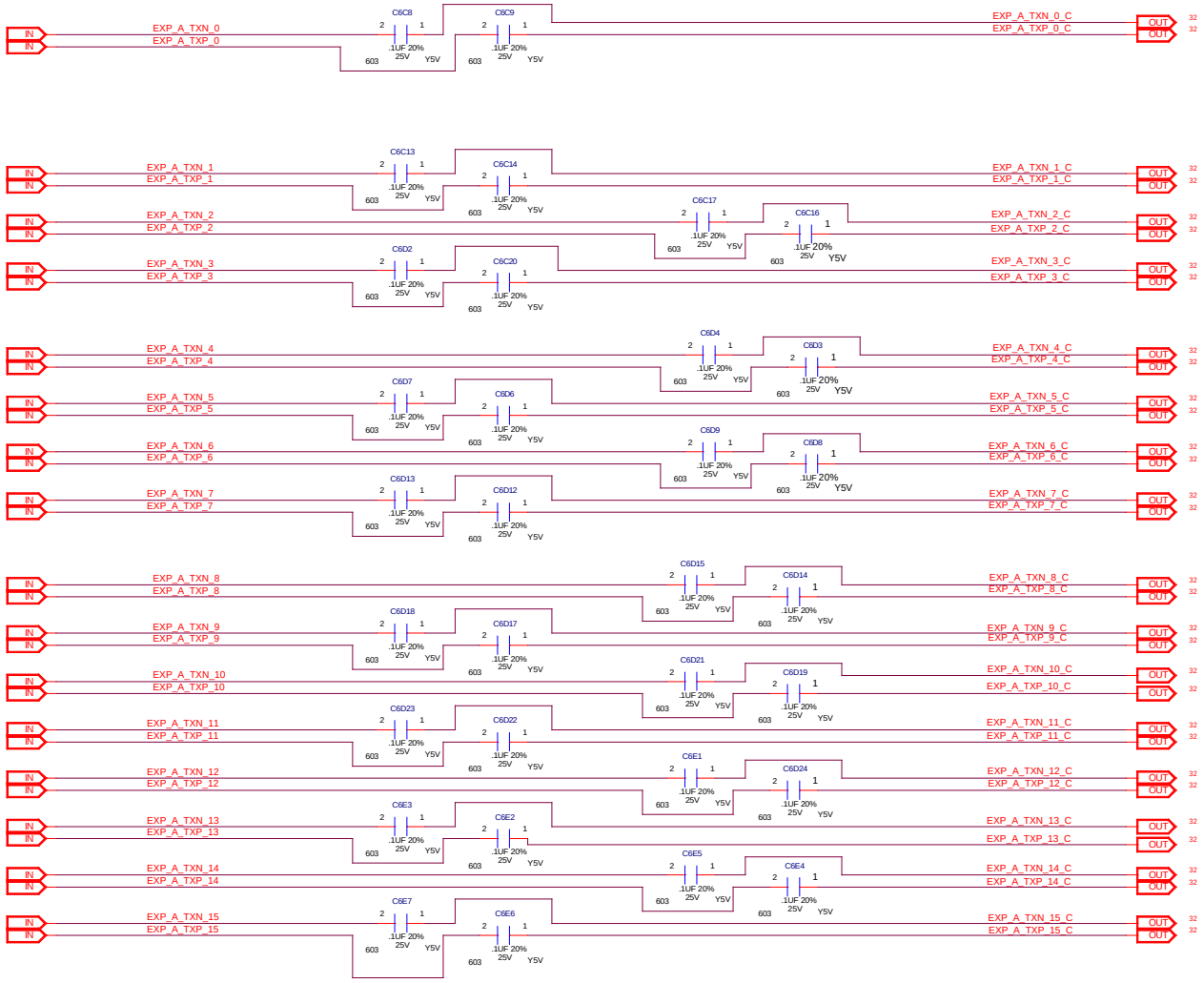
BOM NOTE:
USE C55845-002
FOR X16 CONN



[PAGE_TITLE=PCIE 16-PORT]

CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER C77862	PAGE 32	REV 4.0



[PAGE_TITLE=PCIE COUPLING]

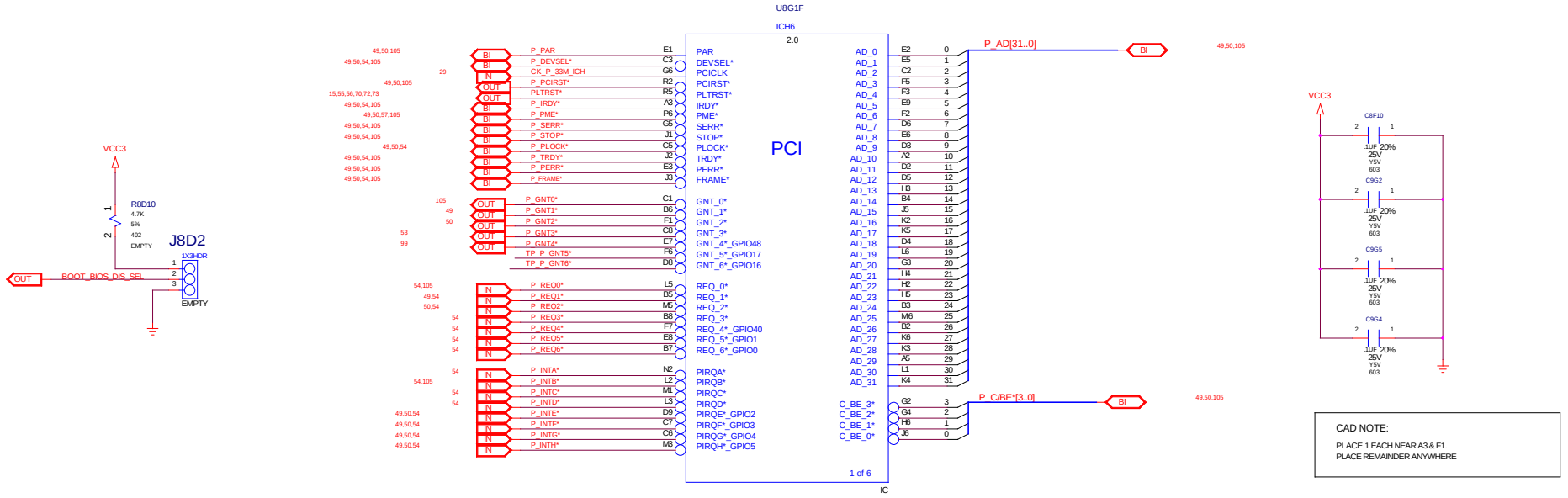
CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	33	4.0

BLANK PAGE

BLANK PAGE

BLANK PAGE



CAD NOTE:

PLACE 1 EACH NEAR A3 & F1.
PLACE REMAINDER ANYWHERE

[PAGE_TITLE=ICH 1 OF 6 - CONTROL]

INTEL CONFIDENTIAL	DOCUMENT NUMBER C77862	PAGE 37	REV 4.0

DESIGN NOTE:
FOR PCI_E X1 SLOT 1

HSO_P0 — C7G5 — .1UF 20% 25V Y5V 603 — HSO_P0_C
HSO_N0 — C7G3 — .1UF 20% 25V Y5V 603 — HSO_N0_C

DESIGN NOTE: FOR LAN

HSO_P1 — C7G7 — .1UF 20% 25V EMPTY 603 — HSO_P1_C
HSO_N1 — C7G4 — .1UF 20% 25V EMPTY 603 — HSO_N1_C
HSI_P1 — C8A7 — .1UF 20% 16V EMPTY 402 — HSI_P1_C
HSI_N1 — C8A8 — .1UF 20% 16V EMPTY 402 — HSI_N1_C

DESIGN NOTE: FOR PCI_E X1 SLOT 2 (ATX)

HSO_P2 — C7G9 — .1UF 20% 25V CH 603 — HSO_P2_C
HSO_N2 — C7G6 — .1UF 20% 25V CH 603 — HSO_N2_C

HSO_P3 — C7G11 — .1UF 20% 25V EMPTY 603 — TP_HSO_P3_C
HSO_N3 — C7G10 — .1UF 20% 25V EMPTY 603 — TP_HSO_N3_C

U8G1A
ICH6
2.0

DMI: DMI_MTN_IRN_0 T25, DMI_MTP_IRP_0 T24, DMI_ITN_MRN_0 R27, DMI_ITP_MRP_0 R26, DMI_MTN_IRN_1 V25, DMI_MTP_IRP_1 V24, DMI_ITN_MRN_1 U27, DMI_ITP_MRP_1 U26, DMI_MTN_IRN_2 Y25, DMI_MTP_IRP_2 Y24, DMI_ITN_MRN_2 W27, DMI_ITP_MRP_2 W26, DMI_MTN_IRN_3 AB24, DMI_MTP_IRP_3 AB23, DMI_ITN_MRN_3 AA27, DMI_ITP_MRP_3 AA26
DMI_0RXN, DMI_0RXP, DMI_0TXN, DMI_0TXP, DMI_1RXN, DMI_1RXP, DMI_1TXN, DMI_1TXP, DMI_2RXN, DMI_2RXP, DMI_2TXN, DMI_2TXP, DMI_3RXN, DMI_3RXP, DMI_3TXN, DMI_3TXP

PCI EXPRESS: HSI_N0 H25, HSI_P0 H24, HSO_N0 G27, HSO_P0 G26, HSI_N1 K25, HSI_P1 K24, HSO_N1 J27, HSO_P1 J26, HSI_N2 M25, HSI_P2 M24, HSO_N2 L27, HSO_P2 L26, TP_HSI_N3 P24, TP_HSI_P3 P23, HSO_N3 N27, HSO_P3 N26
PERN_1, PERP_1, PETN_1, PETP_1, PERN_2, PERP_2, PETN_2, PETP_2, PERN_3, PERP_3, PETN_3, PETP_3, PERN_4, PERP_4, PETN_4, PETP_4

DMI_ZCOMP F28, DMI_IRCOMP F23
DMI_CLKN AD25, DMI_CLKP AC25

USB: USBP_0N C21, USBP_0P D21, USBP_1N A20, USBP_1P B20, USBP_2N D19, USBP_2P C19, USBP_3N A18, USBP_3P B18, USBP_4N E17, USBP_4P D17, USBP_5N B16, USBP_5P A16, USBP_6N C15, USBP_6P D15, USBP_7N A14, USBP_7P B14
OC_0* C27, OC_1* B27, OC_2* B26, OC_3* C26, OC_4*_GPIO9 C23, OC_5*_GPIO10 D23, OC_6*_GPIO14 C25, OC_7*_GPIO15 C24
USBRBIAS B22, USBRBIAS* A22
CLK48 A27

2 of 6
IC

V_PCIEXPRESS_PWR — R7G1 402 24.9 1% — DMICOMP_ICH

CAD NOTE:
CONNECT TRACES TOGETHER CLOSE TO ICH PINS

CK_PE_100M_ICH*
CK_PE_100M_ICH

USB_FRONT1* USB_FRONT1 USB_FRONT2* USB_FRONT2 USB_BACK4* USB_BACK4 USB_FRONT3* USB_FRONT3 USB_BACK3* USB_BACK3 USB_FRONT4* USB_FRONT4 USB_BACK2* USB_BACK2 USB_BACK1* USB_BACK1

USB_OC_FRONT12*
USB_OC_FRONT34_BACK56*
USB_OC_BACK_RIGHT*
USB_OC_BACK_LEFT*

USBRBIAS_ICH — R8F12 402 22.6 1% CH

CAD NOTE:
TRACES TIED TOGETHER CLOSE TO PINS.
LENGTH NO LONGER THAN 200 MIL TO RESISTOR

CK_48M_USB_ICH

USB CLASSIC FILTER

V_3P3_STBY — C8F12 .1UF 10% 16V X7R 603 — C8F13 .1UF 10% 16V X7R 603

CAD NOTE:
PLACE (2) 0.1UF NEAR A17
PLACE 0.01UF NEAR A24

USB HS (HI-SPEED) FILTER

V_1P5_CORE — C7F12 .01UF 20% 50V X7R 603 — C7F11 .1UF 10% 16V X7R 603

CAD NOTE:
PLACE 0.01UF NEAR A25
PLACE 0.1UF NEAR D27

[PAGE_TITLE=ICH 2 OF 6 - CONTROL]

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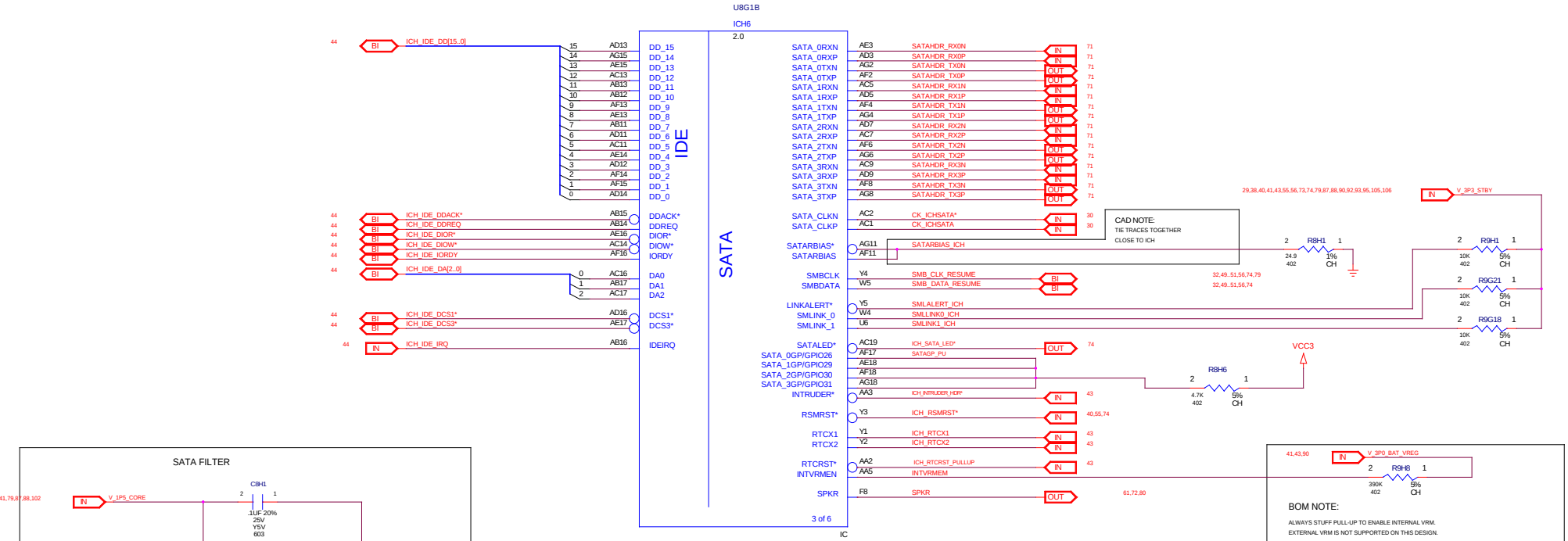
<XR_PAGE_TITLE>



[PAGE_TITLE=ICH 3 OF 6 - CONTROL]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	39	4.0

<XR_PAGE_TITLE>

U8G1C

ICH6

2.0

LPC
AUDIO
EPROM
LAN
HOST
MISC

4 of 6

IC

DESIGN NOTE:
VALIDATION FEATURE

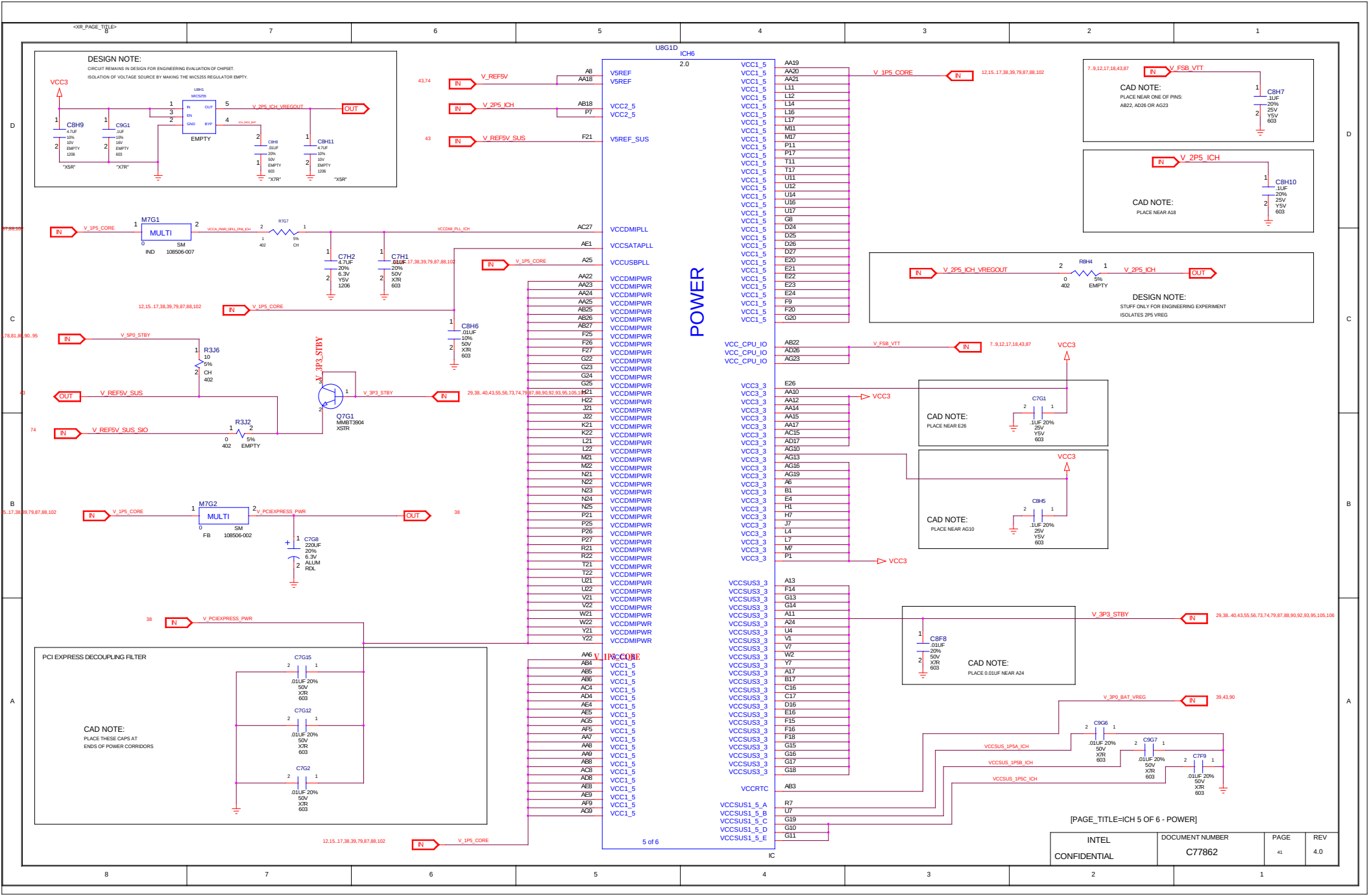
CAD NOTE:
PLACE AWAY FROM CPU AREA
NEAR ICH IS BEST

DESIGN NOTE:
MOBILE BATTERY STRAP

BOARDID[5..0]

[PAGE_TITLE=ICH 4 OF 6 - CONTROL]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	40	4.0


DESIGN NOTE:
CIRCUIT REMAINS IN DESIGN FOR ENGINEERING EVALUATION OF CHIPSET.
ISOLATION OF VOLTAGE SOURCE BY MAKING THE MIC5255 REGULATOR EMPTY.
U8G1D
ICH6
2.0
POWER
5 of 6
IC
V_REF5V
V_2P5_ICH
V_REF5V_SUS
V_1P5_CORE
V_FSB_VTT
V_2P5_ICH_VREGOUT
V_5P0_STBY
V_3P3_STBY
V_REF5V_SUS_SIO
V_PCIEXPRESS_PWR
V_3P0_BAT_VREG
VCCSUS1P5A_ICH
VCCSUS_1P5B_ICH
VCCSUS_1P5C_ICH
PCI EXPRESS DECOUPLING FILTER
CAD NOTE:
PLACE THESE CAPS AT
ENDS OF POWER CORRIDORS
CAD NOTE:
PLACE NEAR ONE OF PINS:
AB22, AD26 OR AG23
CAD NOTE:
PLACE NEAR A18
CAD NOTE:
PLACE NEAR E26
CAD NOTE:
PLACE NEAR AG10
CAD NOTE:
PLACE 0.01UF NEAR A24
DESIGN NOTE:
STUFF ONLY FOR ENGINEERING EXPERIMENT
ISOLATES 2P5 VREG
[PAGE_TITLE=ICH 5 OF 6 - POWER]
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
C77862
PAGE
41
REV
4.0

U8G1E
ICH6
2.0

A1	VSS	VSS	G21
A12	VSS	VSS	G7
A15	VSS	VSS	G9
A19	VSS	VSS	H23
A21	VSS	VSS	H26
A23	VSS	VSS	H27
A26	VSS	VSS	J23
A4	VSS	VSS	J24
A7	VSS	VSS	J25
A9	VSS	VSS	J4
AA11	VSS	VSS	K1
AA13	VSS	VSS	K23
AA16	VSS	VSS	K26
AA4	VSS	VSS	K27
AB1	VSS	VSS	K7
AB10	VSS	VSS	L13
AB19	VSS	VSS	L15
AB2	VSS	VSS	L23
AB7	VSS	VSS	L24
AB9	VSS	VSS	L25
AC10	VSS	VSS	M12
AC12	VSS	VSS	M13
AC22	VSS	VSS	M14
AC23	VSS	VSS	M15
AC24	VSS	VSS	M16
AC26	VSS	VSS	M23
AC3	VSS	VSS	M26
AC6	VSS	VSS	M27
AD1	VSS	VSS	M4
AD10	VSS	VSS	N1
AD15	VSS	VSS	N11
AD18	VSS	VSS	N12
AD2	VSS	VSS	N13
AD24	VSS	VSS	N14
AD6	VSS	VSS	N15
AE10	VSS	VSS	N16
AE11	VSS	VSS	N17
AE12	VSS	VSS	N7
AE2	VSS	VSS	P12
AE21	VSS	VSS	P13
AE25	VSS	VSS	P14
AE6	VSS	VSS	P15
AE7	VSS	VSS	P16
AF1	VSS	VSS	P22
AF12	VSS	VSS	R11
AF26	VSS	VSS	R12
AF3	VSS	VSS	R13
AF7	VSS	VSS	R14
AG1	VSS	VSS	R15
AG12	VSS	VSS	R16
AG14	VSS	VSS	R17
AG17	VSS	VSS	R23
AG20	VSS	VSS	R24
AG22	VSS	VSS	R25
AG3	VSS	VSS	R4
AG7	VSS	VSS	T1
B13	VSS	VSS	T12
B15	VSS	VSS	T13
B19	VSS	VSS	T14
B21	VSS	VSS	T15
B23	VSS	VSS	T16
B25	VSS	VSS	T23
C14	VSS	VSS	T26
C18	VSS	VSS	T27
C20	VSS	VSS	T7
C22	VSS	VSS	U13
C4	VSS	VSS	U15
D1	VSS	VSS	U23
D10	VSS	VSS	U24
D13	VSS	VSS	U25
D14	VSS	VSS	V23
D18	VSS	VSS	V26
D20	VSS	VSS	V27
D22	VSS	VSS	V4
D7	VSS	VSS	W1
E14	VSS	VSS	W23
E15	VSS	VSS	W24
E18	VSS	VSS	W25
E19	VSS	VSS	W7
E25	VSS	VSS	Y23
F17	VSS	VSS	Y26
F19	VSS	VSS	Y27
F22	VSS	VSS	Y6
F4	VSS	VSS	E27
G1	VSS	VSS	AF10
G12	VSS	VSS	B24

GND
6 of 6
IC

HS8G1
C46655-001
ICH6_HSK
NC_1
NC_2
NC_4
NC_3
EMPTY

NOTE:
NO PHYSICAL PINS
ON ALLEGRO MODEL

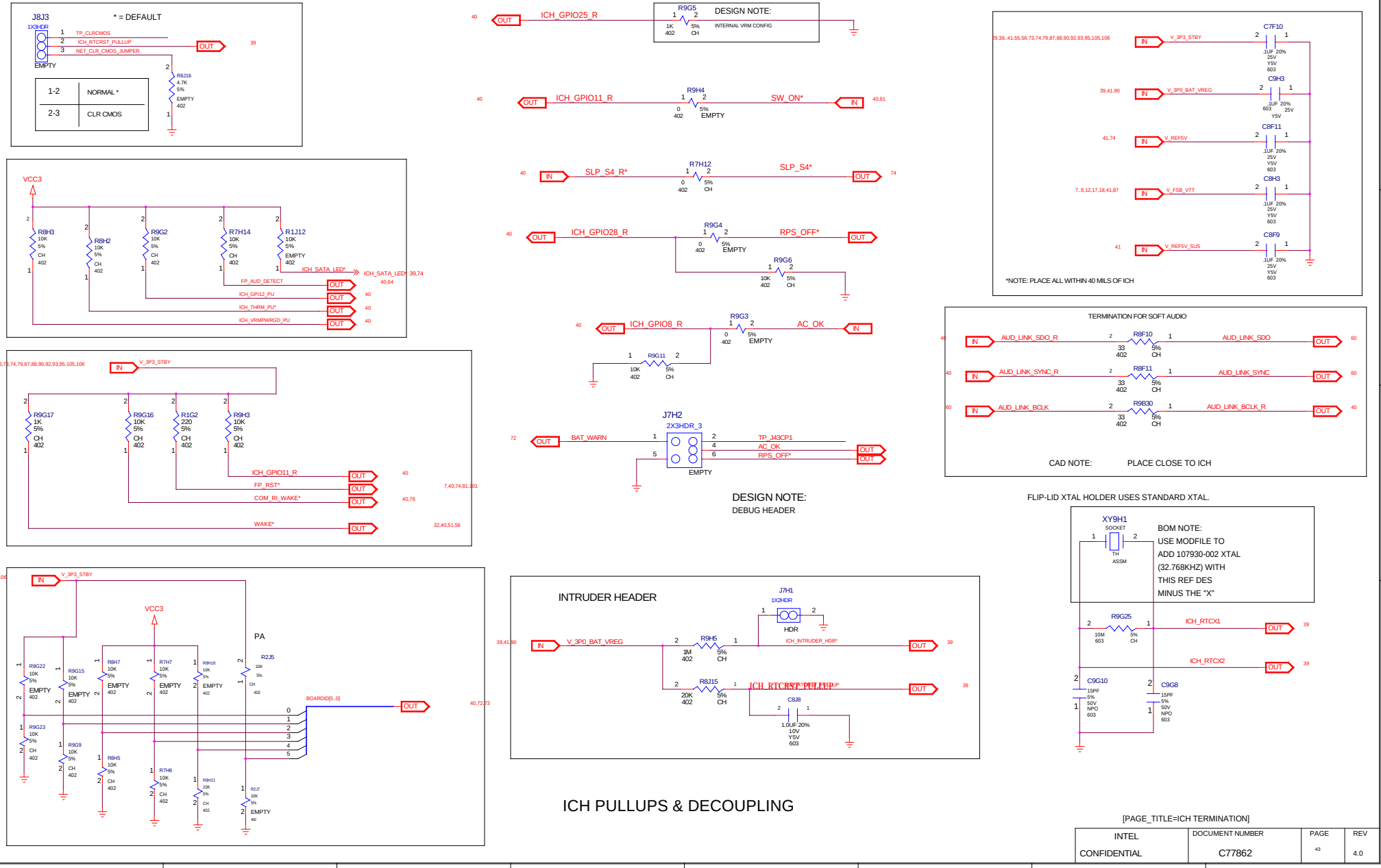
TH
J9H1
NC
EMPTY
A13494-005

TH
J7F1
NC
EMPTY
A13494-005

[PAGE_TITLE=ICH 6 OF 6 - GROUND]

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	42	4.0

<XR_PAGE_TITLE>



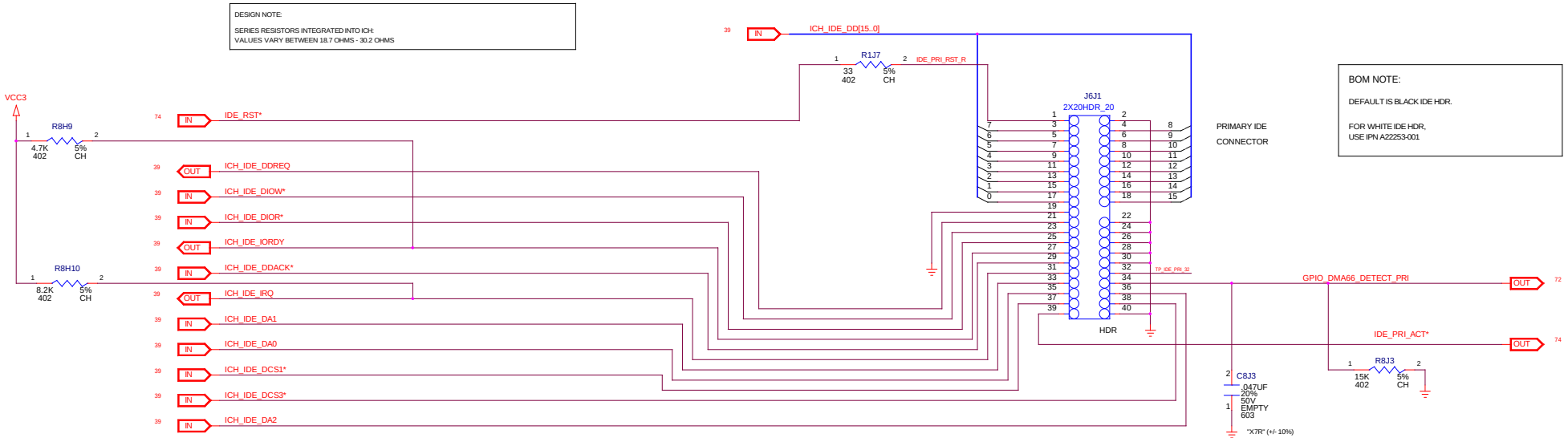
ICH PULLUPS & DECOUPLING

[PAGE_TITLE=ICH TERMINATION]

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	43	4.0

DESIGN NOTE:

SERIES RESISTORS INTEGRATED INTO ICH:
VALUES VARY BETWEEN 18.7 OHMS - 30.2 OHMS



BOM NOTE:

DEFAULT IS BLACK IDE HDR.

FOR WHITE IDE HDR,
USE IPN A22253-001

CAD NOTE:
PLACE CLOSE TO CONNECTOR PIN

DESIGN NOTE:

DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR*, XIORDY*) WITHIN +/-250MIL

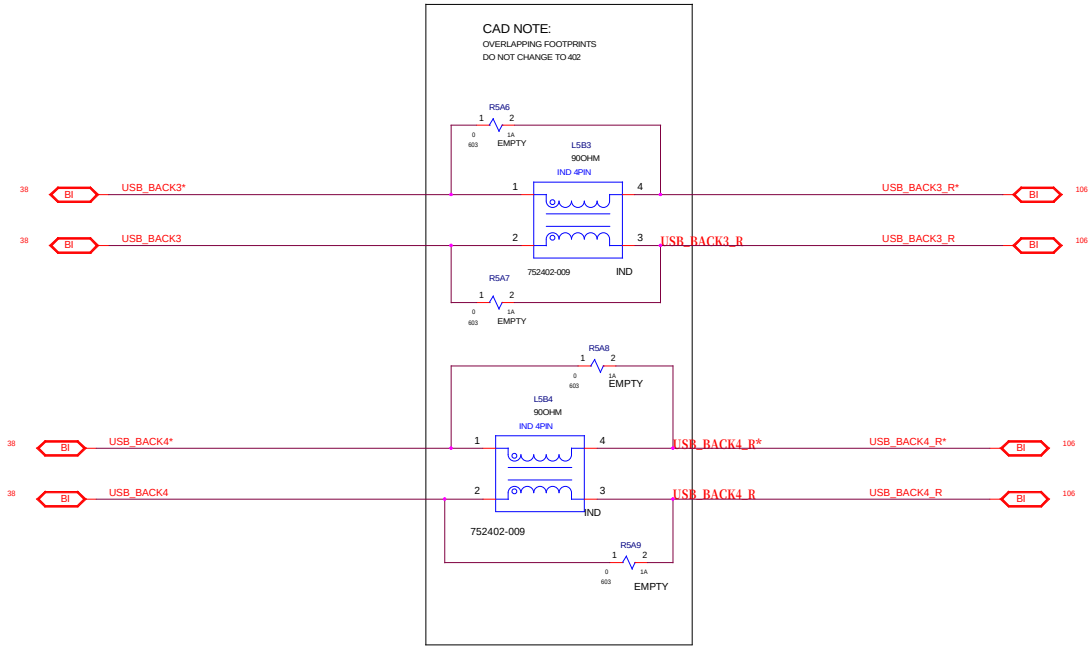
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/-10MIL

[PAGE_TITLE=IDE_SOUTH_BRIDGE]

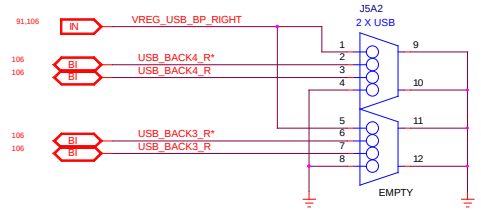
PCI IDE

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	44	4.0

CAD NOTE:
OVERLAPPING FOOTPRINTS
DO NOT CHANGE TO 402



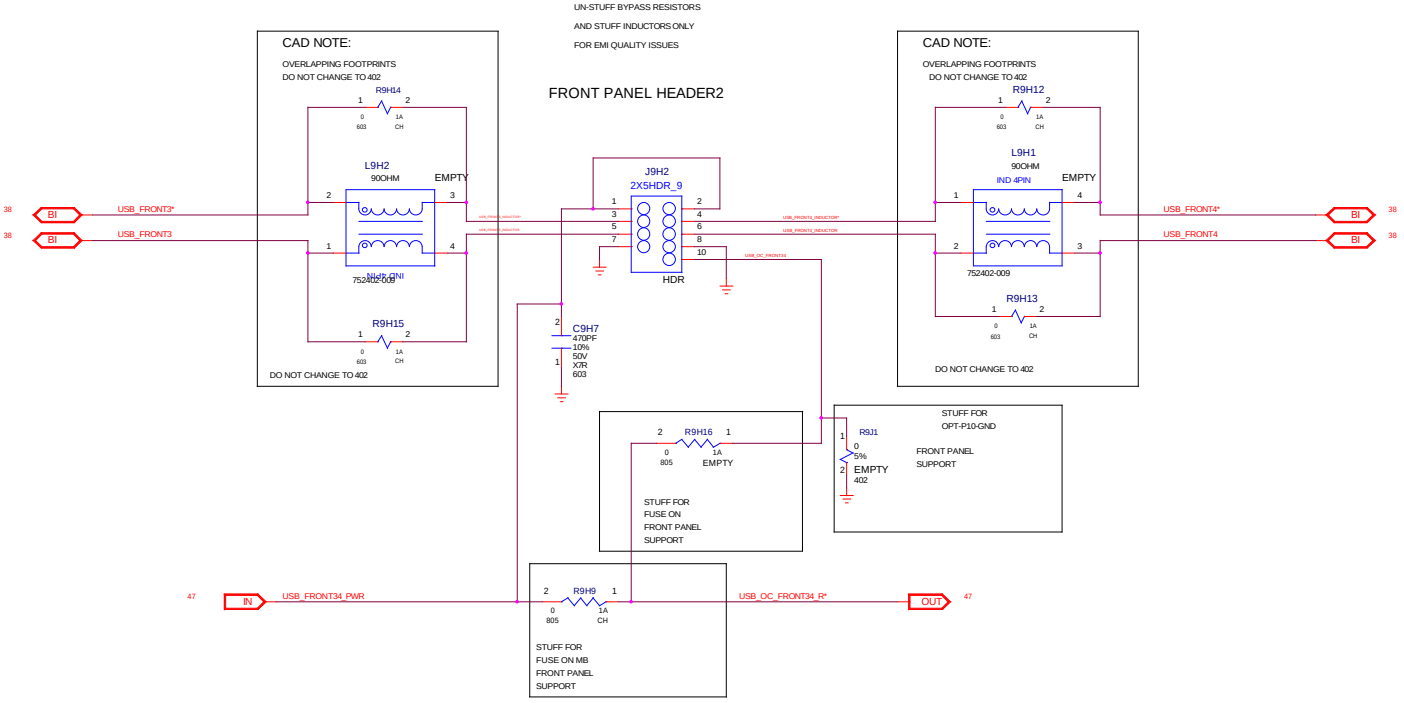
DOUBLE STACK USB



[PAGE_TITLE=USB_BACKPANEL_CONN]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	45	4.0

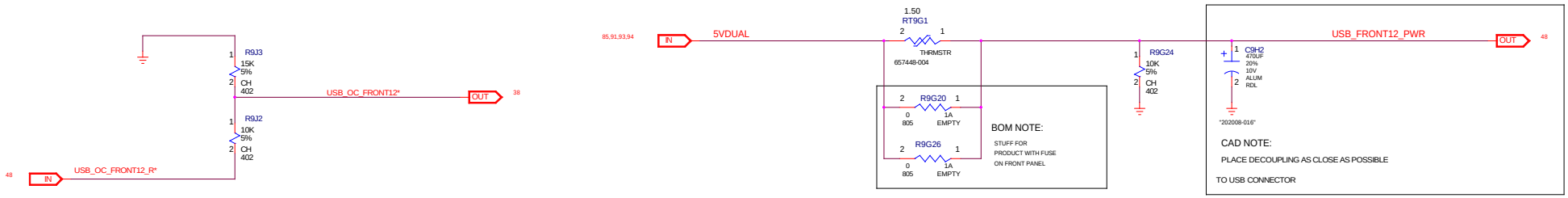
USB FRONT PANEL HEADER #2



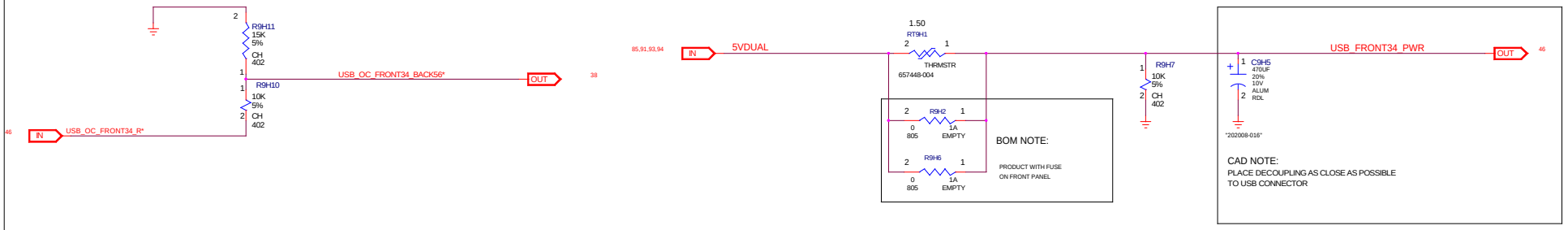
[PAGE_TITLE=USB_FP #2 HEADER]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	46	4.0

POWER FOR USB FRONT PANEL #1



POWER FOR USB FRONT PANEL #2



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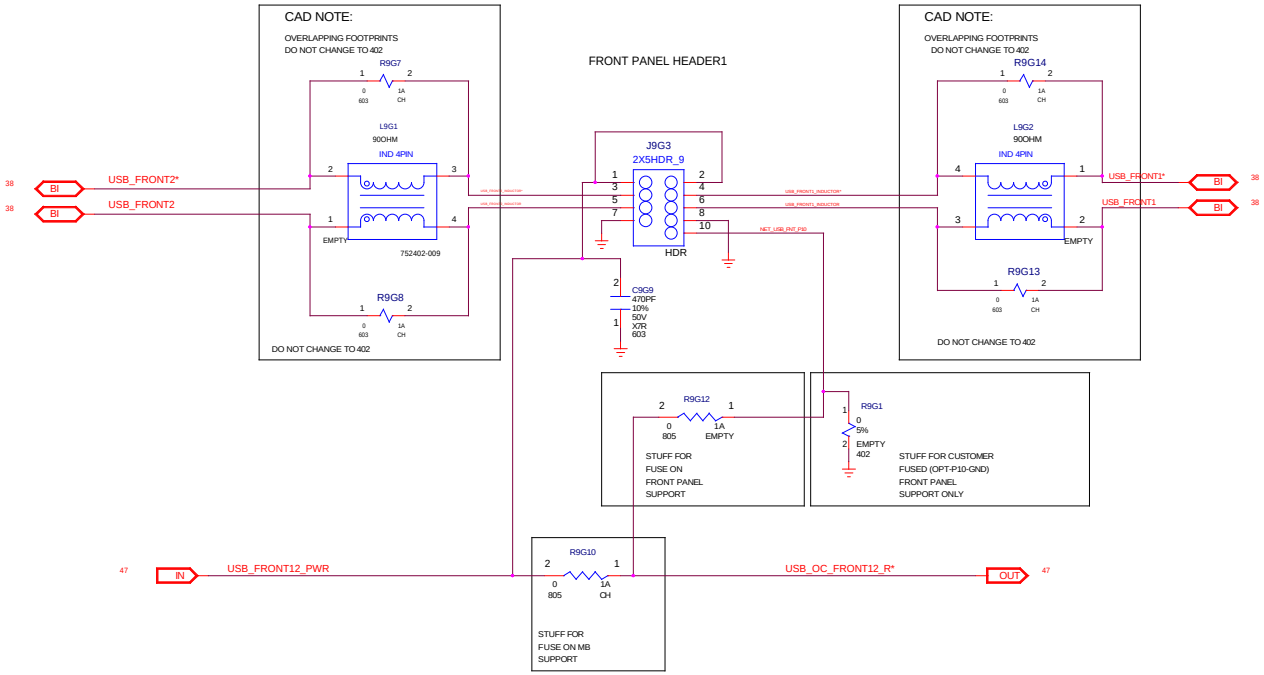
USB FRONT PANEL HEADER #1



[PAGE_TITLE=USB_FP_HEADER #1]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	48	4.0

<XR_PAGE_TITLE>

BACK PANEL SLOT 6

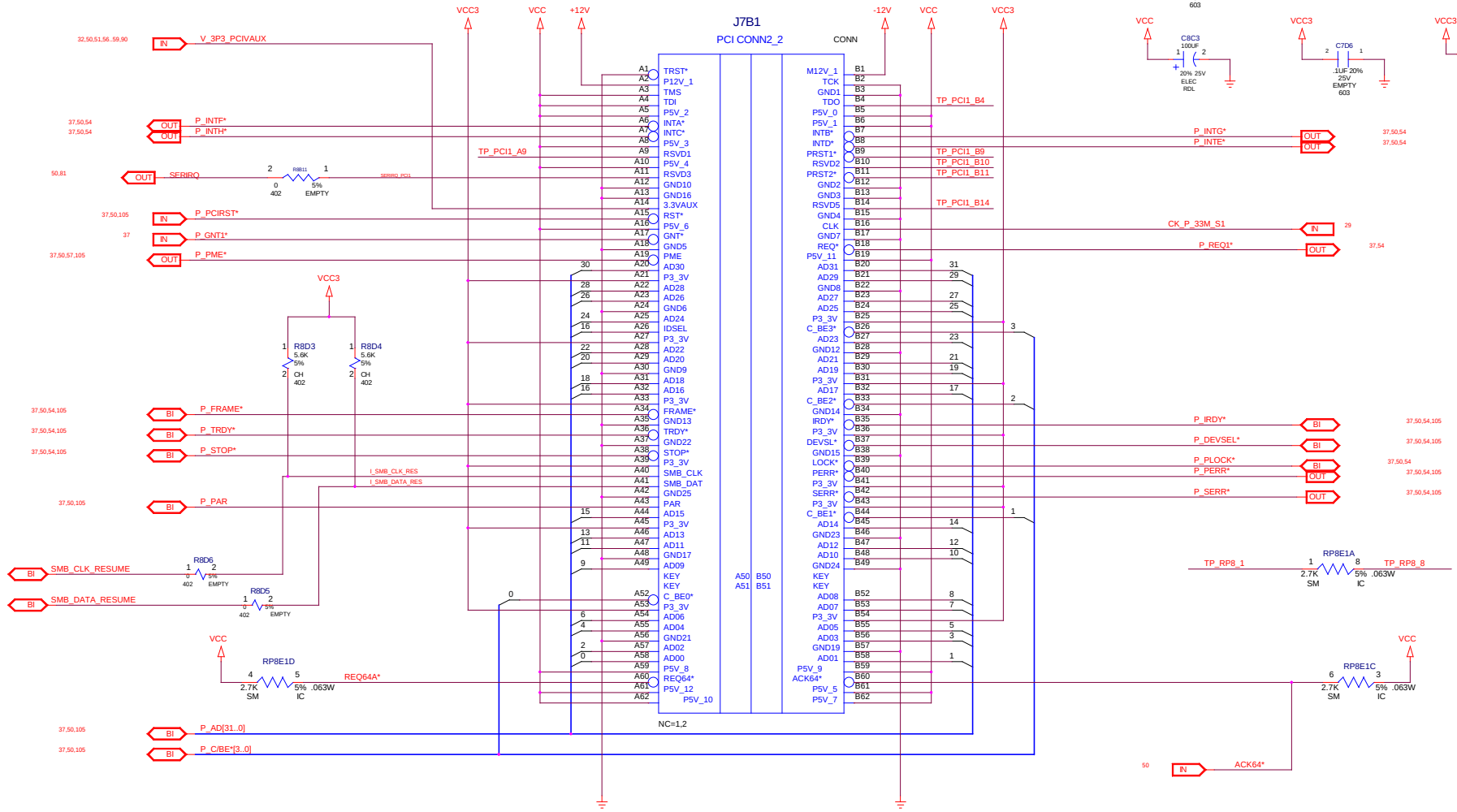
PCI SLOT 1

(CLOSEST TO CPU)

J7B1

PCI CONN2_2

CONN



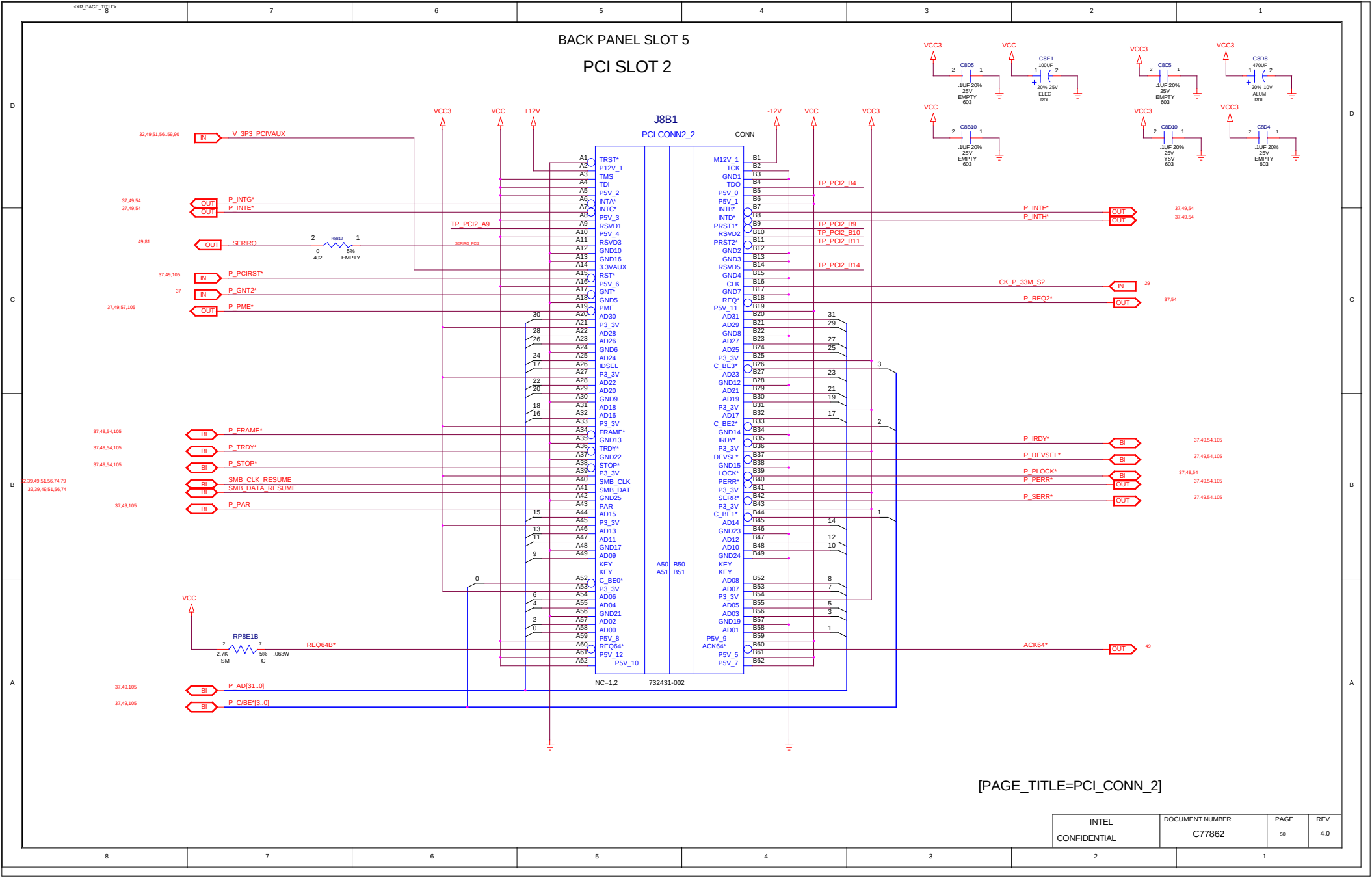
[PAGE_TITLE=PCI_CONN_1]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	49	4.0

<XR_PAGE_TITLE>

BACK PANEL SLOT 5

PCI SLOT 2



[PAGE_TITLE=PCI_CONN_2]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	50	4.0

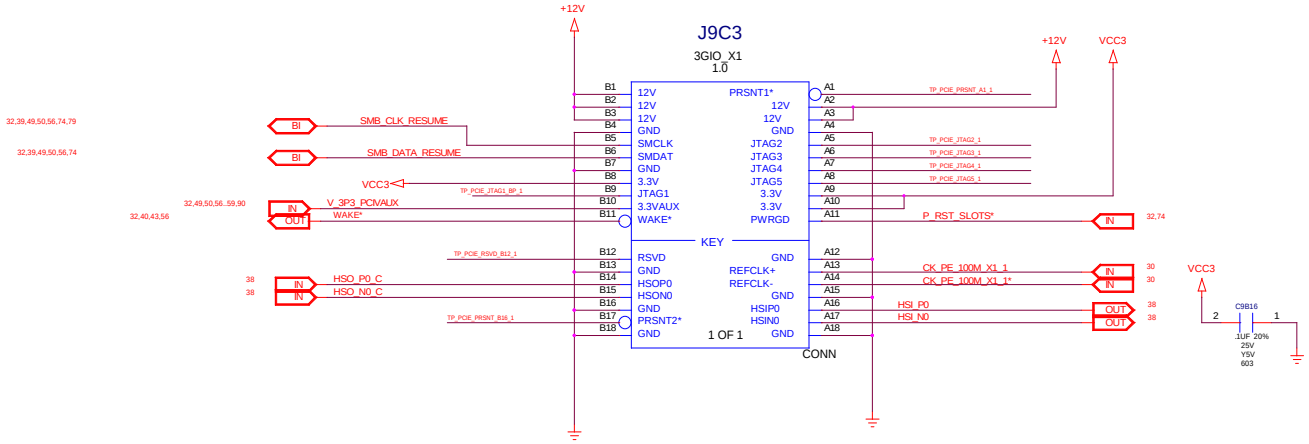
BACK PANEL SLOT 4

PCI EXPRESS X1 SLOT 1

BOM NOTE:

USE C55845-001

FOR X1 CONN



[TITLE=PCIE_X1_CONN_2]

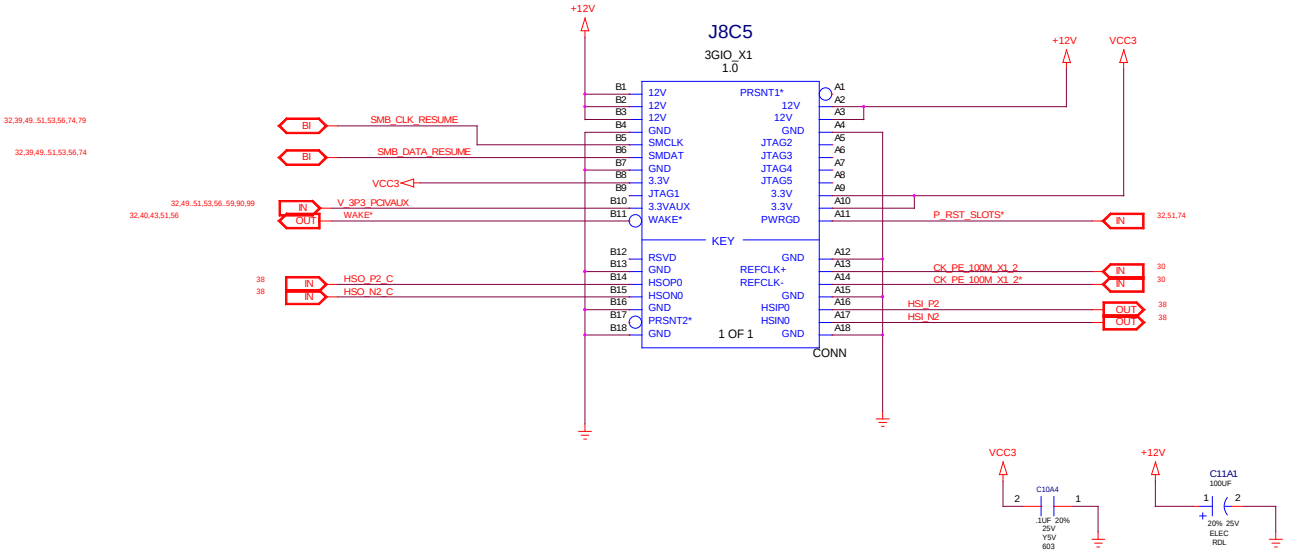
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	s1	4.0

BACK PANEL SLOT 3

PCI EXPRESS X1 SLOT 2

BOM NOTE:

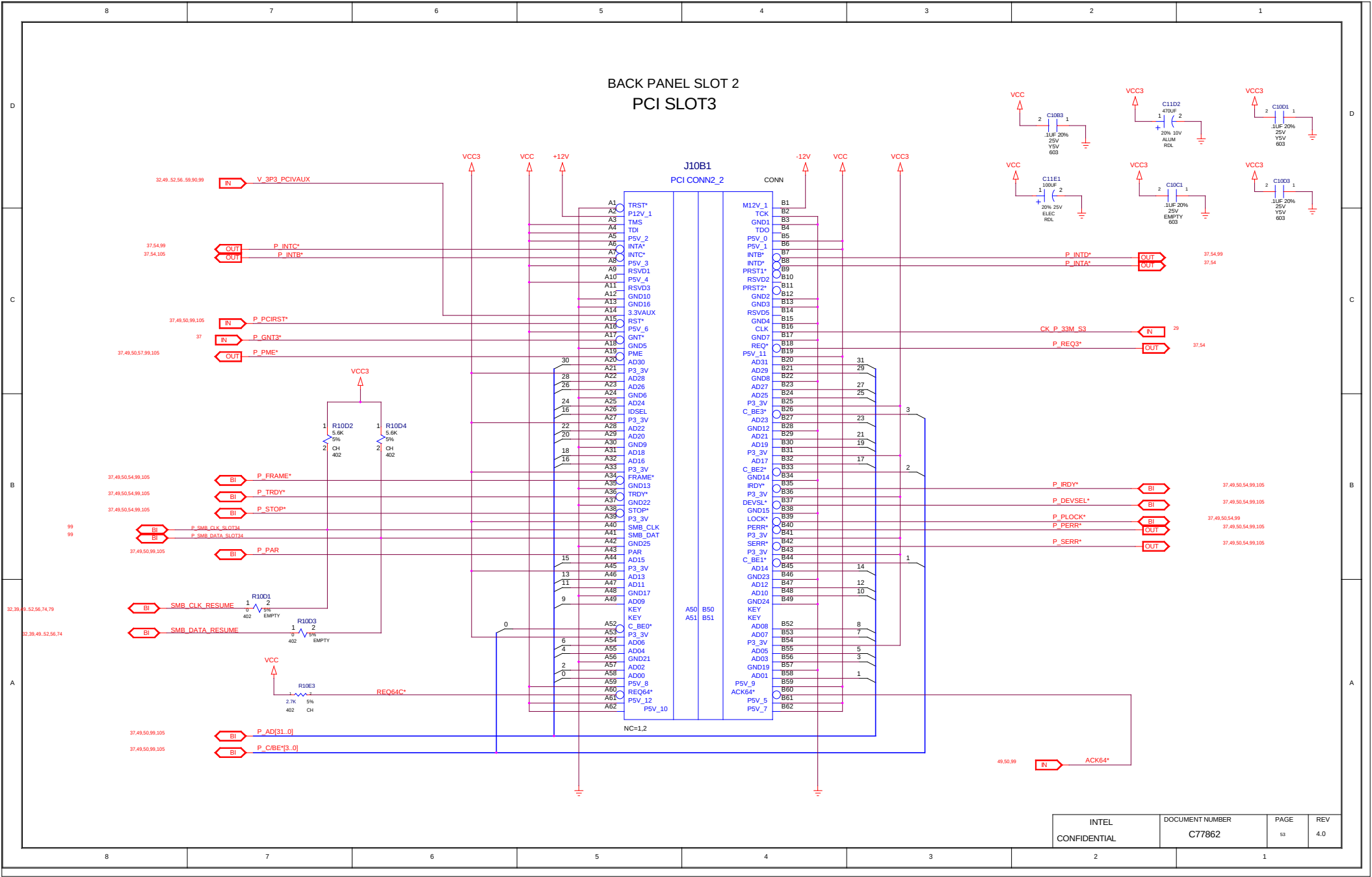
USE C55845-001
FOR X1 CONN



INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	52	4.0

BACK PANEL SLOT 2

PCI SLOT3



INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	53	4.0

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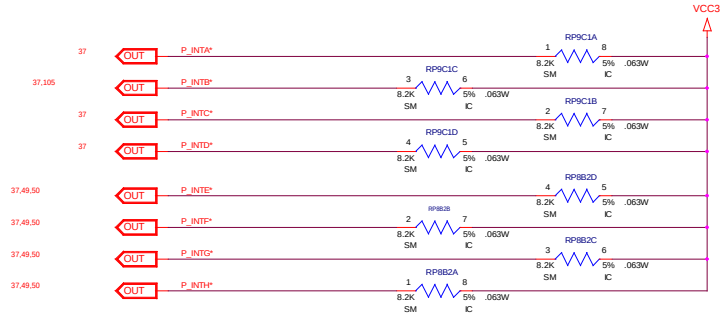

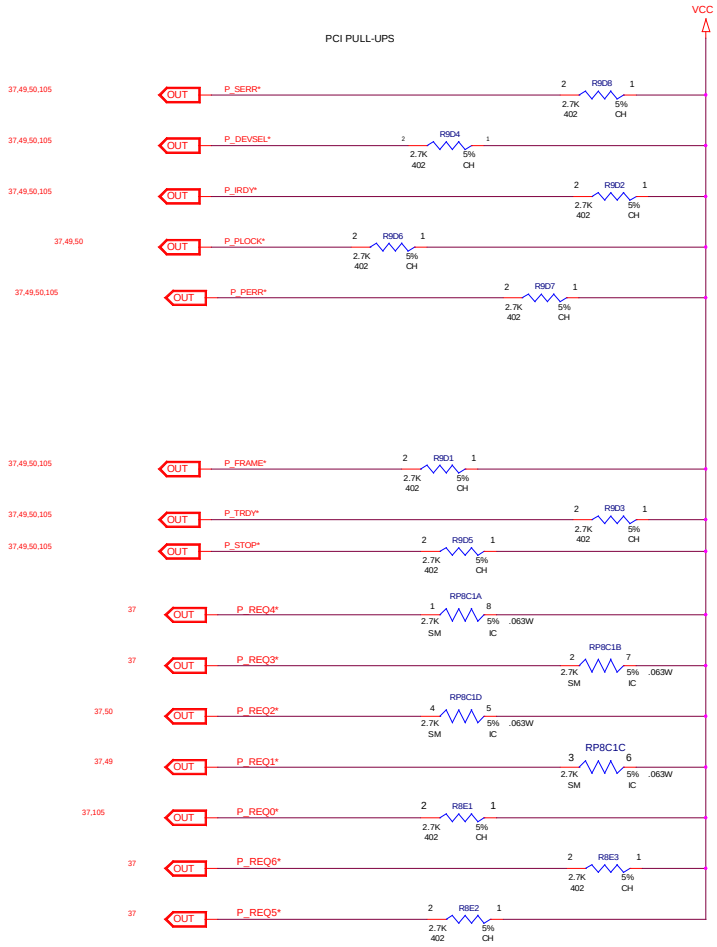

[MODULE=ICH]

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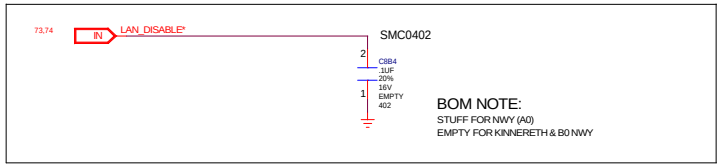
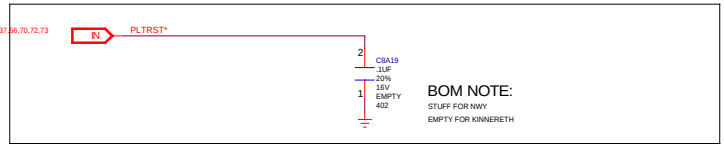
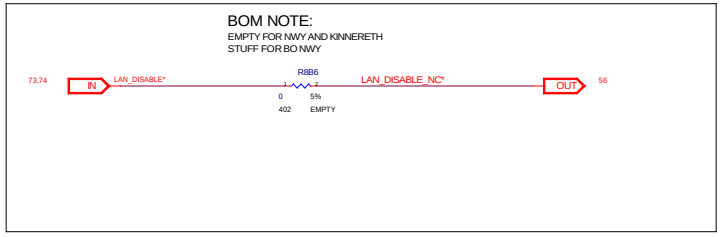
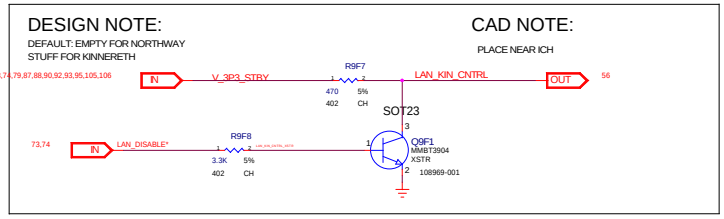
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	54	4.0









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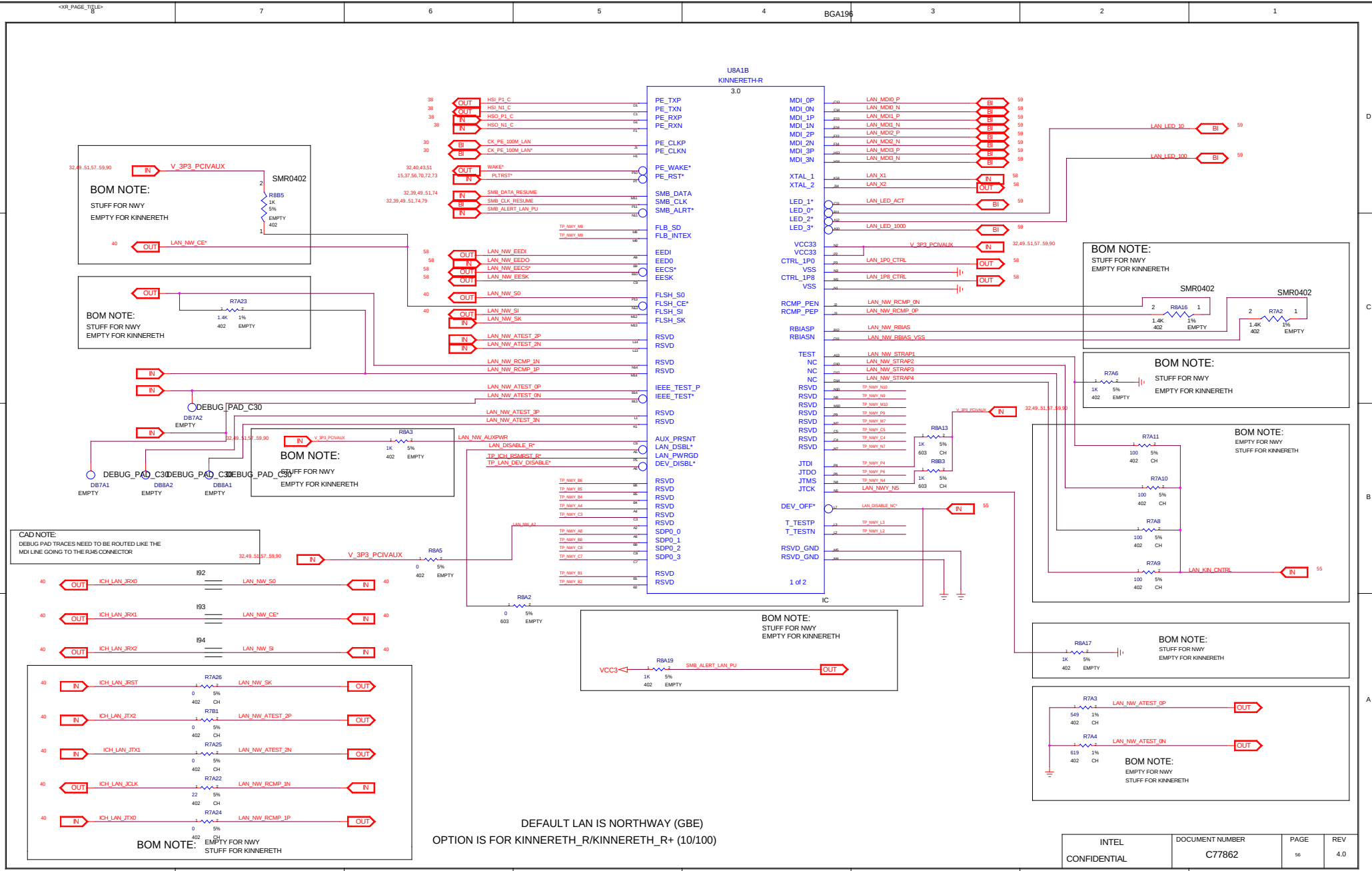
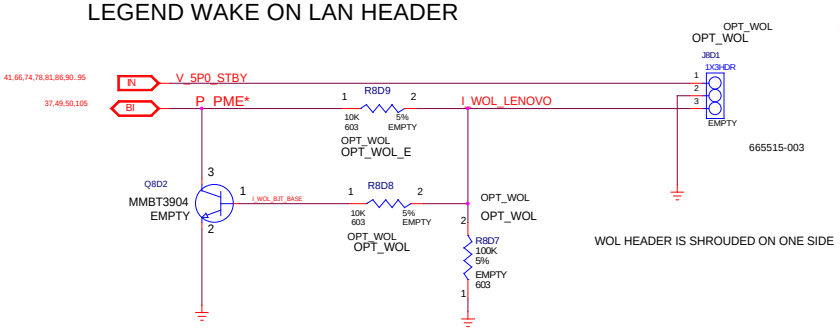

U8A1B
KINNERETH-R
3.0
PE_TXP
PE_TXN
PE_RXP
PE_RXN
PE_CLKP
PE_CLKN
PE_WAKE*
PE_RST*
SMB_DATA
SMB_CLK
SMB_ALERT*
FLB_SD
FLB_INTEX
EEDI
EED0
EECS*
EESK
FLSH_S0
FLSH_CE*
FLSH_SI
FLSH_SK
RSVD
IEEE_TEST_P
IEEE_TEST*
AUX_PRSNT
LAN_DSBL*
LAN_PWRGD
DEV_DISBL*
MDI_0P
MDI_0N
MDI_1P
MDI_1N
MDI_2P
MDI_2N
MDI_3P
MDI_3N
XTAL_1
XTAL_2
LED_1*
LED_0*
LED_2*
LED_3*
VCC33
CTRL_1P0
VSS
CTRL_1P8
RCMP_PEN
RCMP_PEP
RBIASP
RBIASN
TEST
NC
JTDI
JTDO
JTMS
JTCK
DEV_OFF*
T_TESTP
T_TESTN
RSVD_GND
1 of 2
IC
BOM NOTE:
STUFF FOR NWY
EMPTY FOR KINNERETH
SMR0402
R8B5
1K
5%
EMPTY
402
V_3P3_PCIVAUX
LAN_NW_CE*
R7A23
1.4K
1%
DEBUG_PAD_C30
DB7A2
DB7A1
DB8A2
DB8A1
R8A3
LAN_NW_AUXPWR
LAN_DISABLE_R*
TP_ICH_RSMRST_R*
TP_LAN_DEV_DISABLE*
R8A5
R8A2
603
CAD NOTE:
DEBUG PAD TRACES NEED TO BE ROUTED LIKE THE
MDI LINE GOING TO THE RJ45 CONNECTOR
I92
I93
I94
ICH_LAN_JRX0
ICH_LAN_JRX1
ICH_LAN_JRX2
LAN_NW_S0
LAN_NW_SI
ICH_LAN_JRST
ICH_LAN_JTX2
ICH_LAN_JTX1
ICH_LAN_JCLK
ICH_LAN_JTX0
LAN_NW_SK
LAN_NW_ATEST_2P
LAN_NW_ATEST_2N
LAN_NW_RCMP_1N
LAN_NW_RCMP_1P
R7A26
R7B1
R7A25
R7A22
R7A24
CH
22
VCC3
SMB_ALERT_LAN_PU
R8A19
LAN_LED_10
LAN_LED_100
LAN_LED_ACT
LAN_LED_1000
LAN_X1
LAN_X2
LAN_1P0_CTRL
LAN_1P8_CTRL
LAN_NW_RCMP_0N
LAN_NW_RCMP_0P
LAN_NW_RBIAS
LAN_NW_RBIAS_VSS
LAN_NW_STRAP1
LAN_NW_STRAP2
LAN_NW_STRAP3
LAN_NW_STRAP4
R7A6
R8A16
R7A2
R8A13
R8B3
R7A11
R7A10
R7A8
R7A9
LAN_KIN_CNTRL
R8A17
R7A3
R7A4
LAN_NW_ATEST_0P
LAN_NW_ATEST_0N
549
619
DEFAULT LAN IS NORTHWAY (GBE)
OPTION IS FOR KINNERETH_R/KINNERETH_R+ (10/100)
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
C77862
PAGE
56
REV
4.0

LEGEND WAKE ON LAN HEADER



WOL HEADER IS SHROUDED ON ONE SIDE

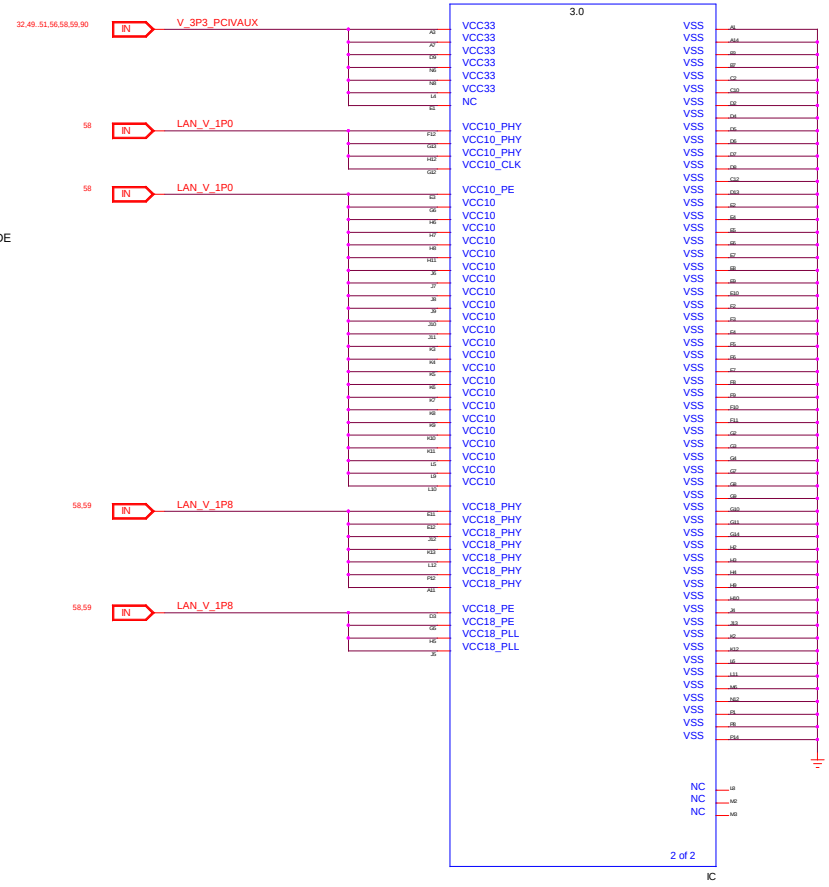
ADD WOL HEADER CIRCUIT

BGA196

U8A1A

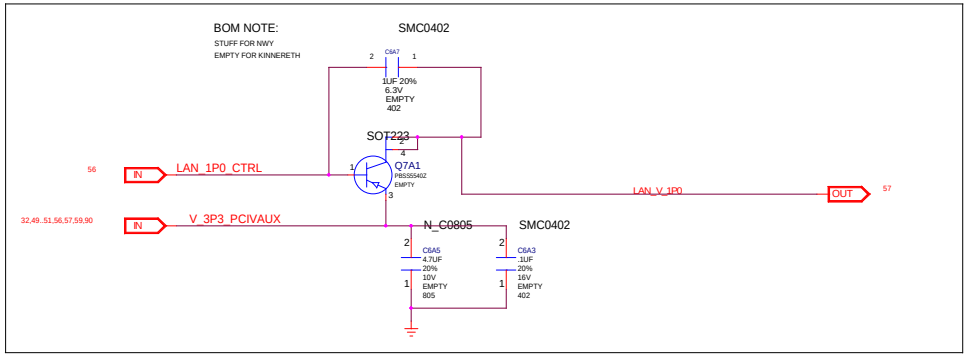
KINNERETH-R

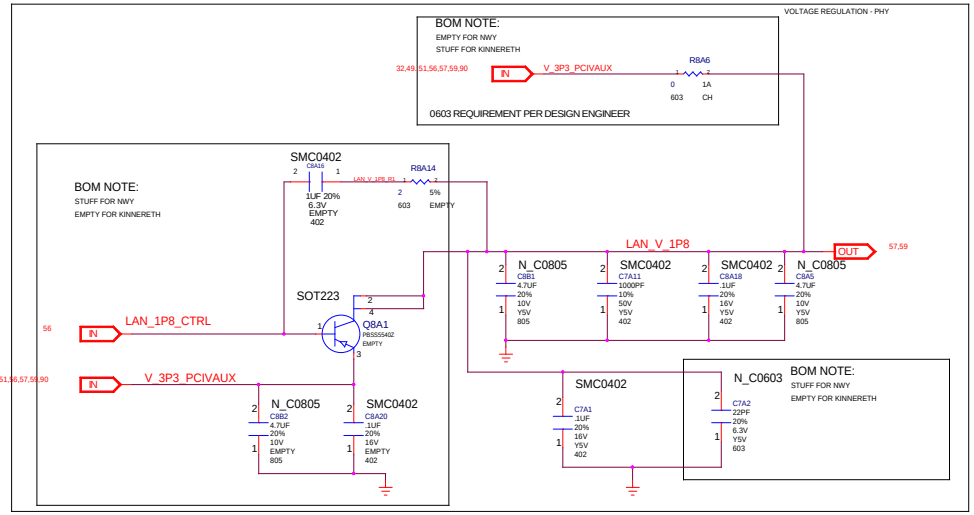
3.0

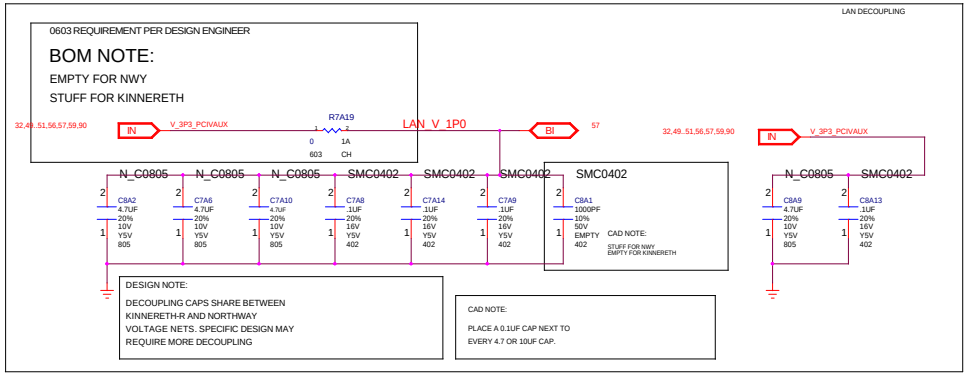


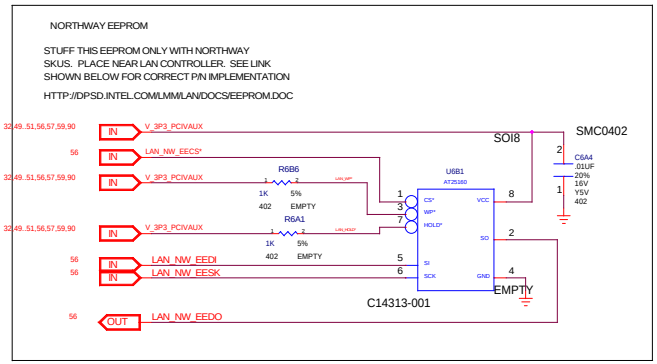
IC

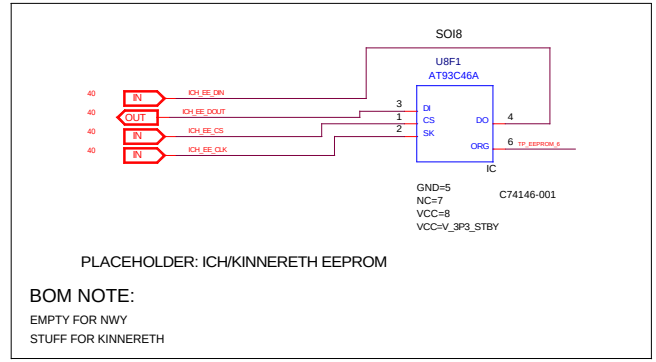
INTEL CONFIDENTIAL	DOCUMENT NUMBER C77862	PAGE 57	REV 4.0

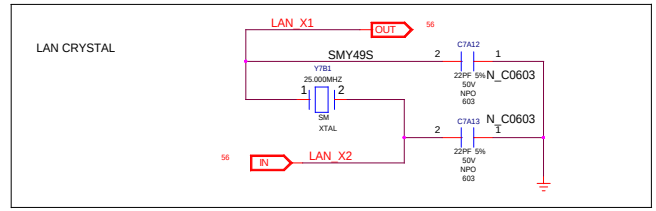








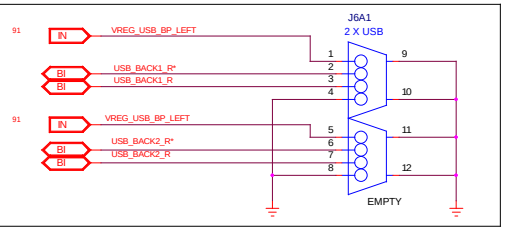


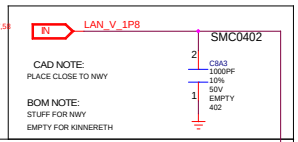


INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	58	4.0

CAD NOTE:
OVERLAP WITH MAGJACK FOOTPRINT
* MODEL HAS DIFFERENT PIN ORIENTTION
THAN MAGJACK FOOTPRINT

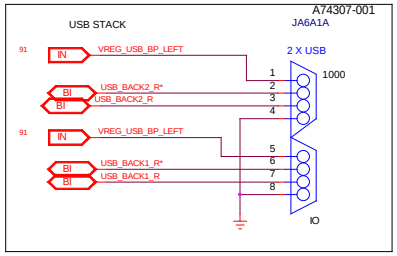
BOM NOTE:
EMPTY EXCEPT FOR USB W/NO-LAN OPTION



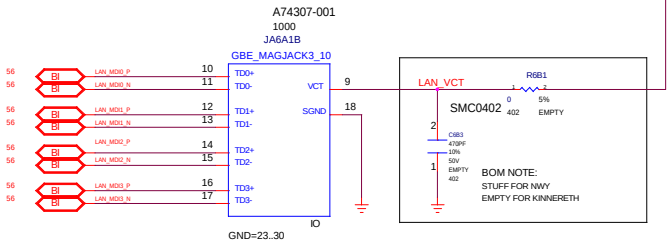


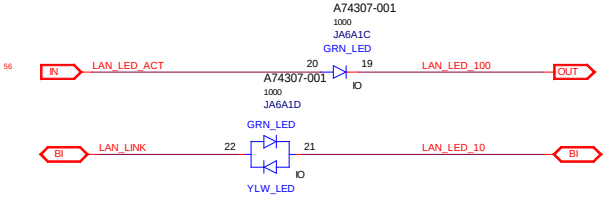
LAN CONNECTOR
DEFAULT GIGABIT

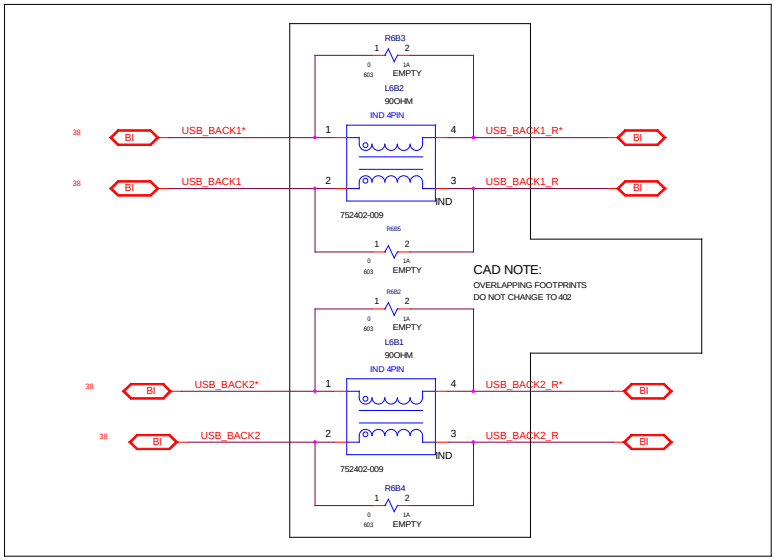
MAGJACK	SPEED LED
10 MBPS	OFF
100 MBPS	GREEN
1000 MBPS	YELLOW

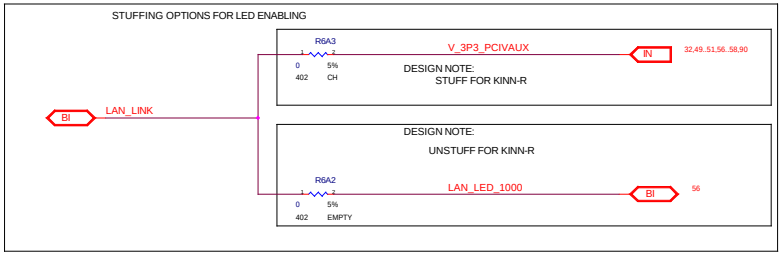


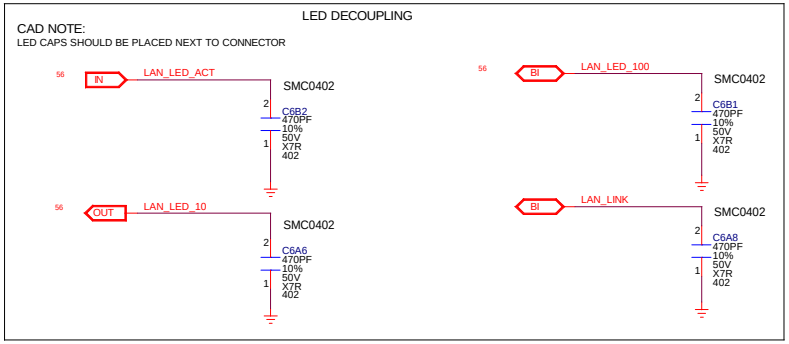
DESIGN NOTE:
USE CONNECTOR A74307-001 WITH NORTHWAY
USE CONNECTOR A74314-002 WITH KINNERETH-R

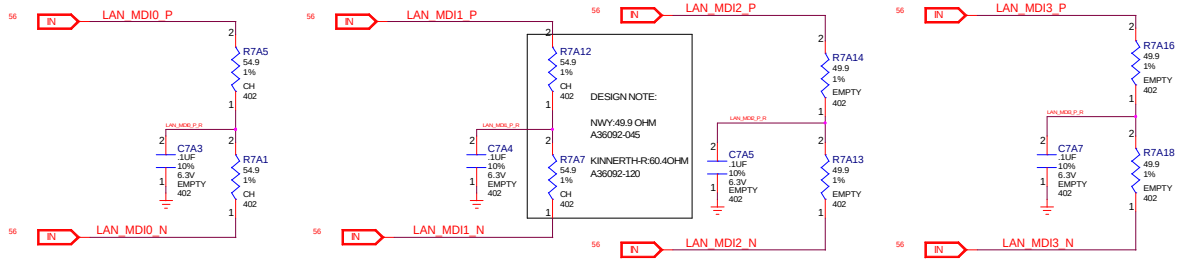










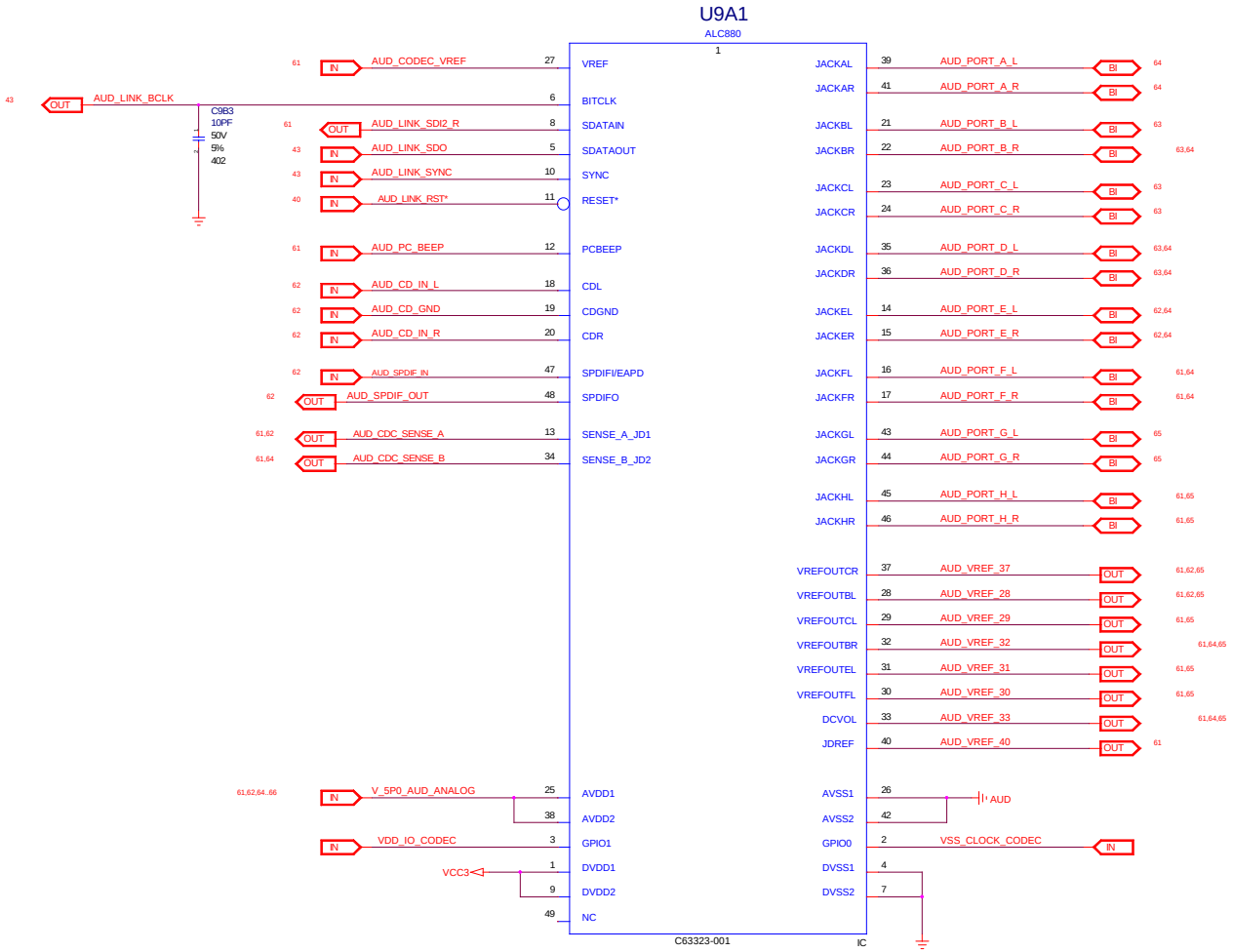


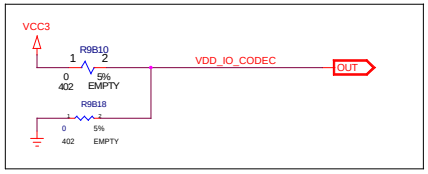
DIFFERENTIAL PAIR TERMINATION

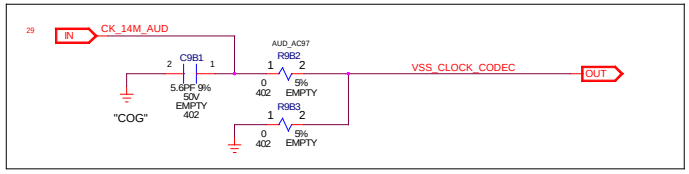
[PAGE_TITLE=LAN CONN]

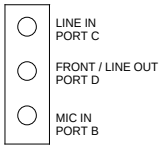
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	59	4.0

DEFAULT AUDIO CODEC: AZALIA REALTEK









PORT E
PORT F
ON FRONT PANEL

DESIGN NOTE:

AZALIA:

CMEDIA: CMI9880
REALTEK: ALC880,ALC860

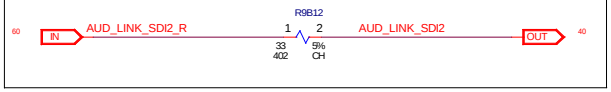
AC97:

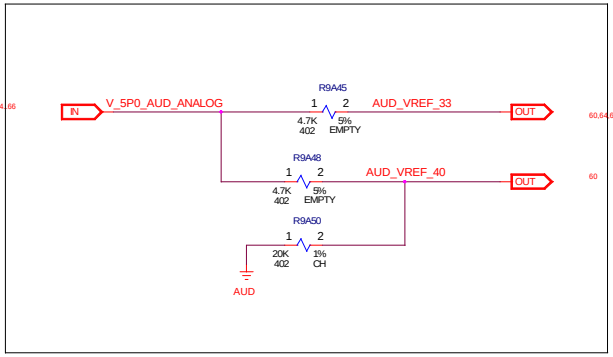
CMEDIA: CMI9762+,9780
REALTEK: ALC650,655,658,850, ALC202A

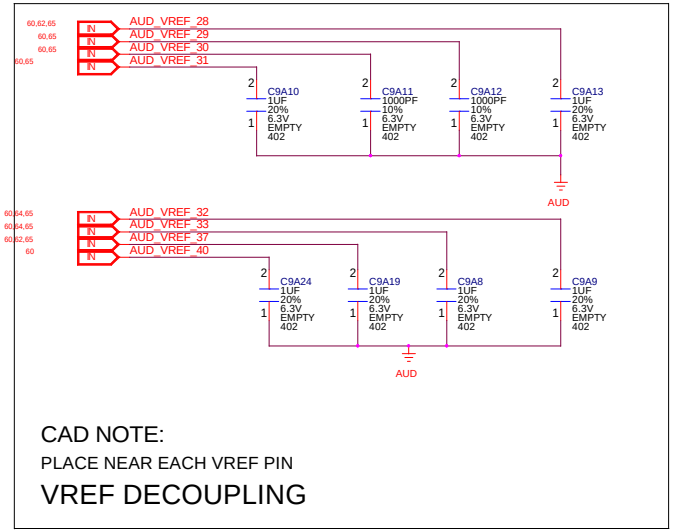
AUDIO CODEC

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	60	4.0

CAD NOTE:
PLACE NEAR ICH PINS

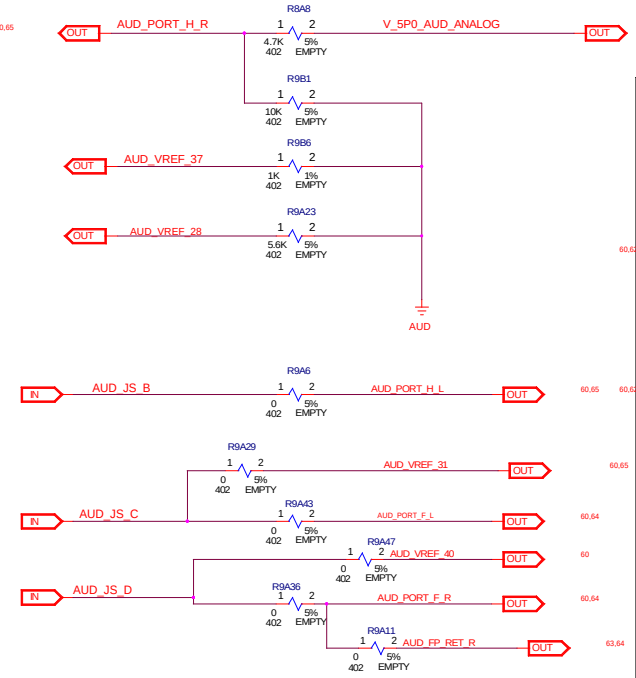


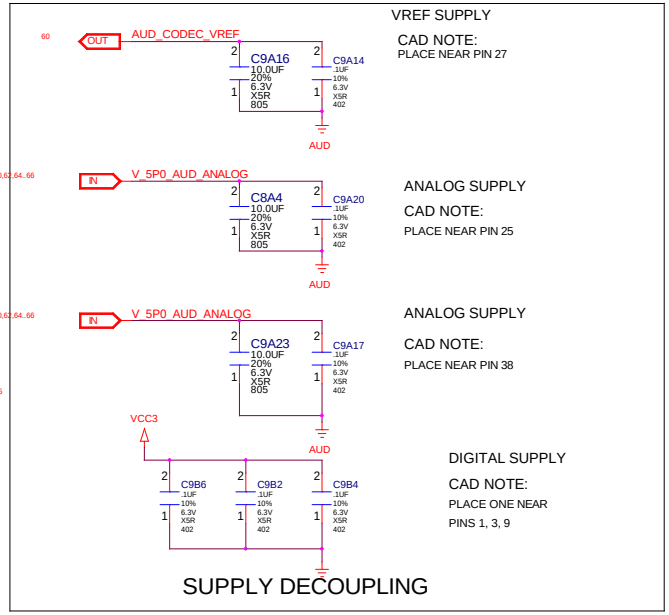




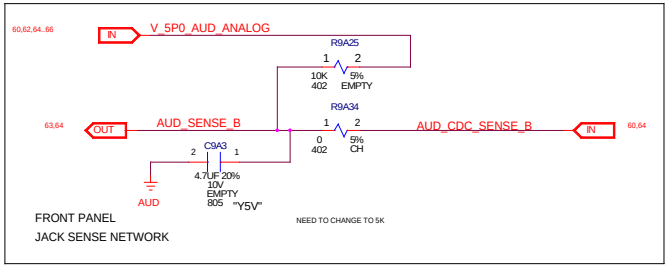
CAD NOTE:
PLACE NEAR EACH VREF PIN

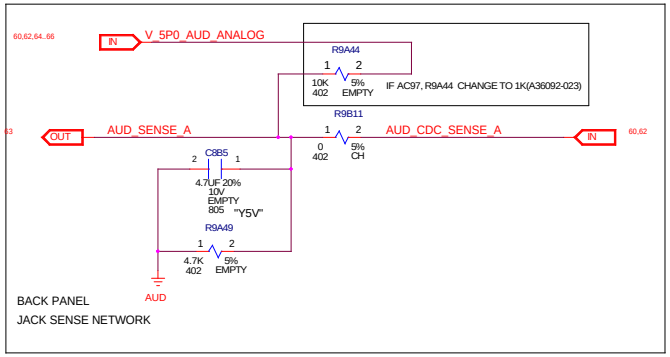
VREF DECOUPLING

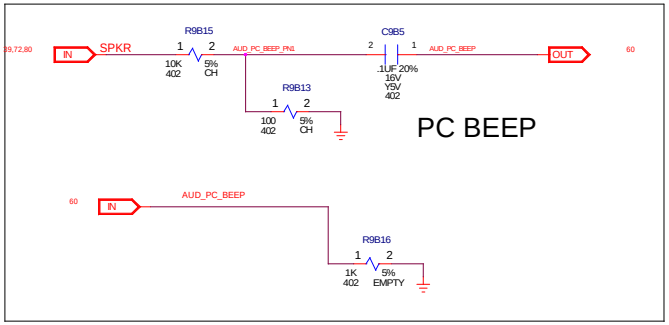




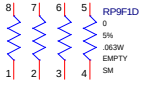
SUPPLY DECOUPLING



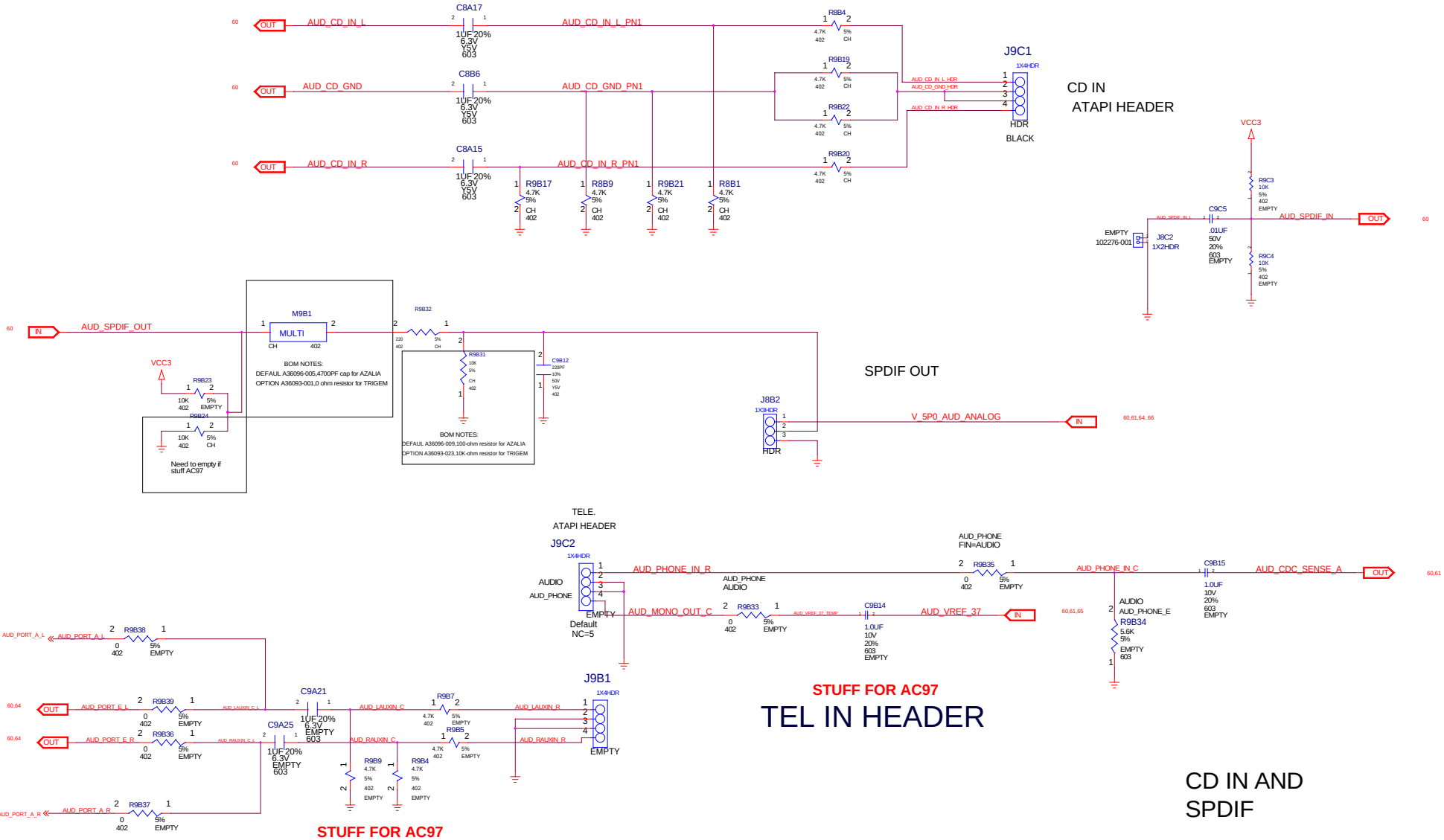




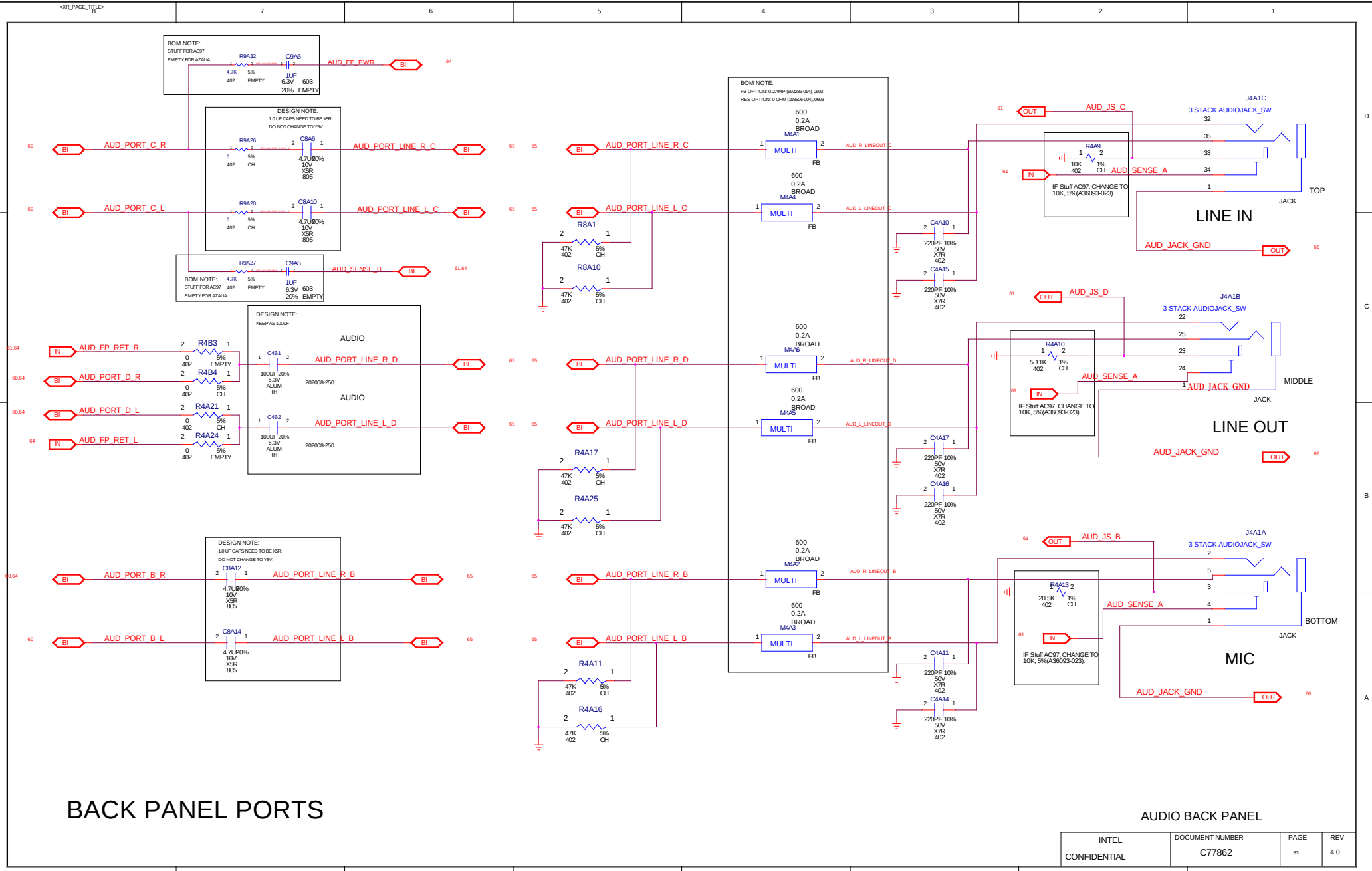
DECOUPLING AND JACK SENSE

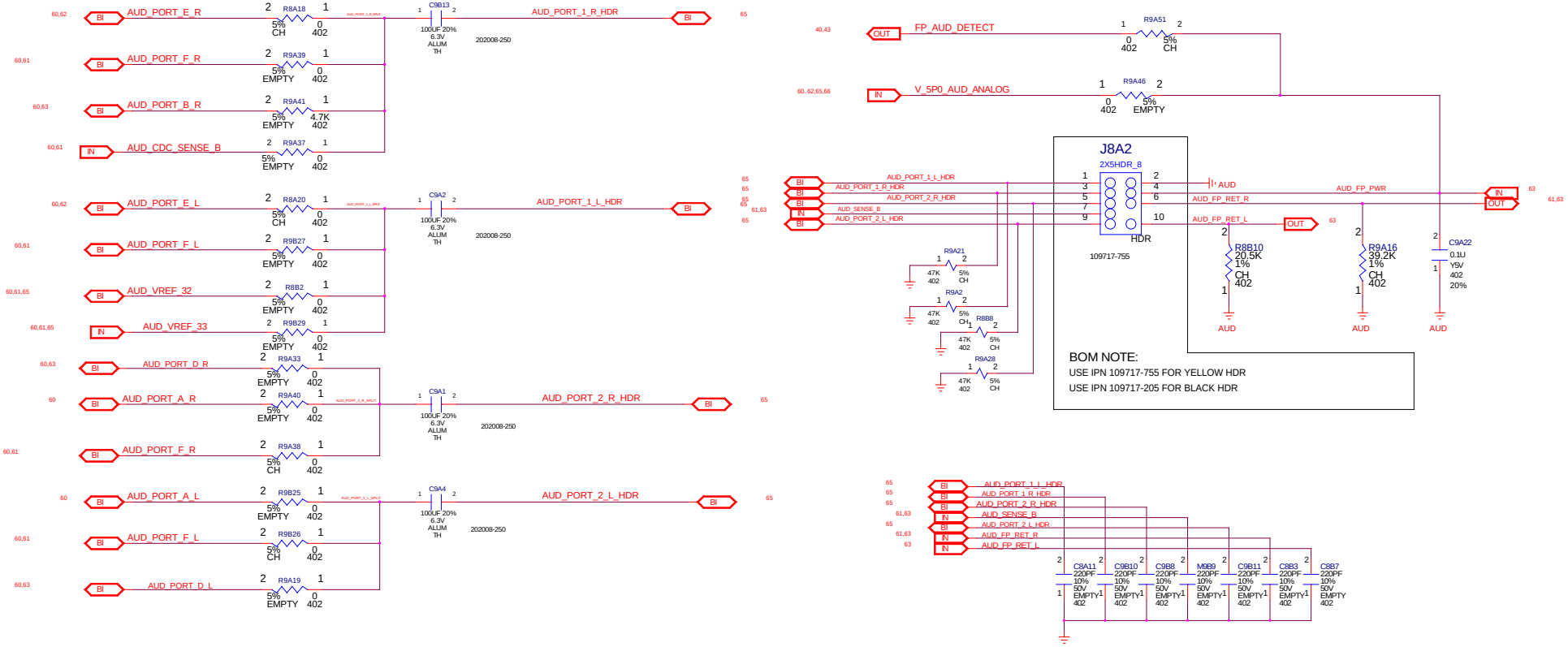


INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	61	4.0



INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	62	4.0


BACK PANEL PORTS
AUDIO BACK PANEL
LINE IN
LINE OUT
MIC
TOP
MIDDLE
BOTTOM
J4A1C
J4A1B
J4A1A
3 STACK AUDIOJACK_SW
JACK
AUD_PORT_C_R
AUD_PORT_C_L
AUD_PORT_B_R
AUD_PORT_B_L
AUD_PORT_LINE_R_C
AUD_PORT_LINE_L_C
AUD_PORT_LINE_R_D
AUD_PORT_LINE_L_D
AUD_PORT_LINE_R_B
AUD_PORT_LINE_L_B
AUD_FP_PWR
AUD_FP_RET_R
AUD_FP_RET_L
AUD_PORT_D_R
AUD_PORT_D_L
AUD_SENSE_A
AUD_SENSE_B
AUD_JACK_GND
AUD_JS_C
AUD_JS_D
AUD_JS_B
IF Stuff AC97, CHANGE TO 10K, 5%(A36093-023).
DESIGN NOTE:
BOM NOTE:
AUDIO
MULTI
FB
INTEL
CONFIDENTIAL
C77862
4.0



AC HEADER
FRONT PANEL PORTS

INTEL	DOCUMENT NUMBER	PAGE	REV
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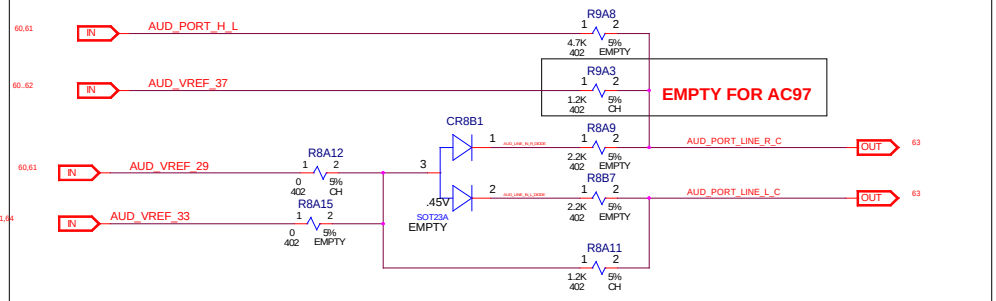
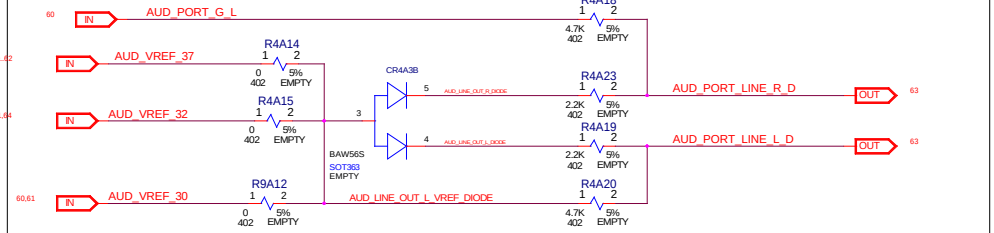
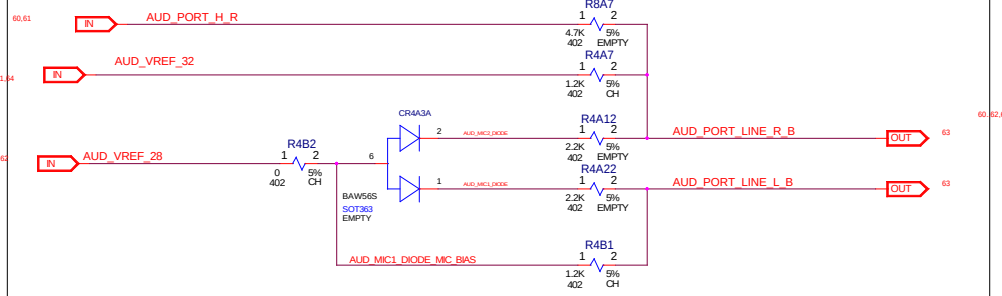
3 STACK

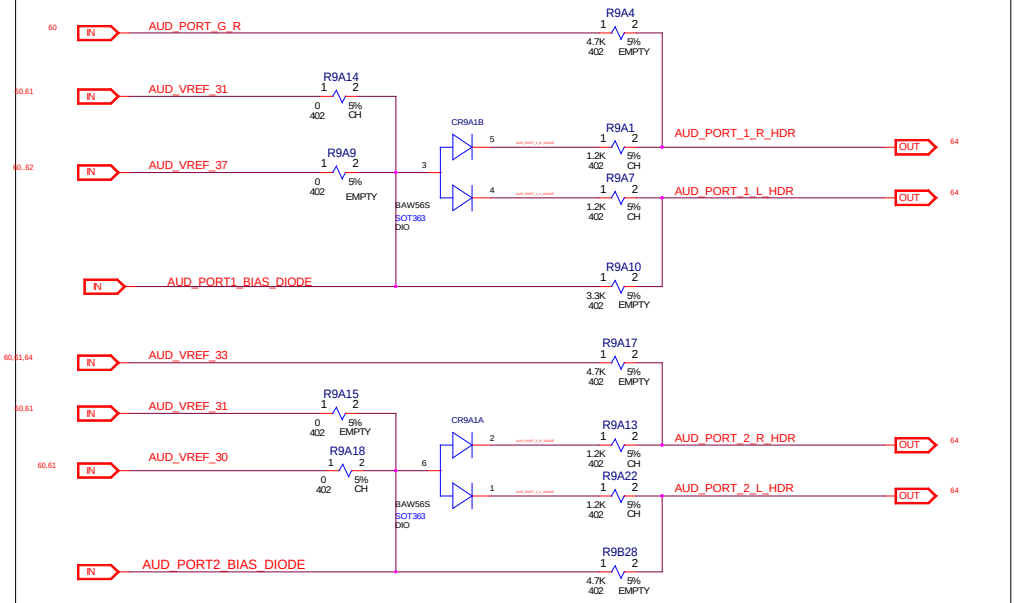




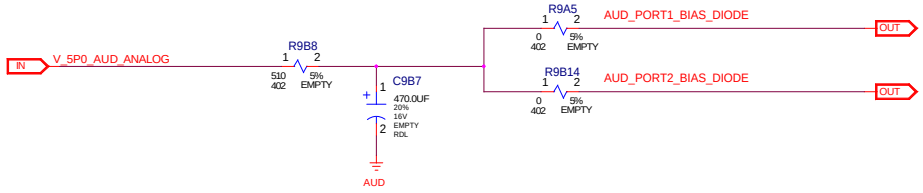


TERMINATION/PULL-UPS

FRONT PANEL



TERMINATION/PULL-UPS



VREF NETWORKS

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	65	4.0

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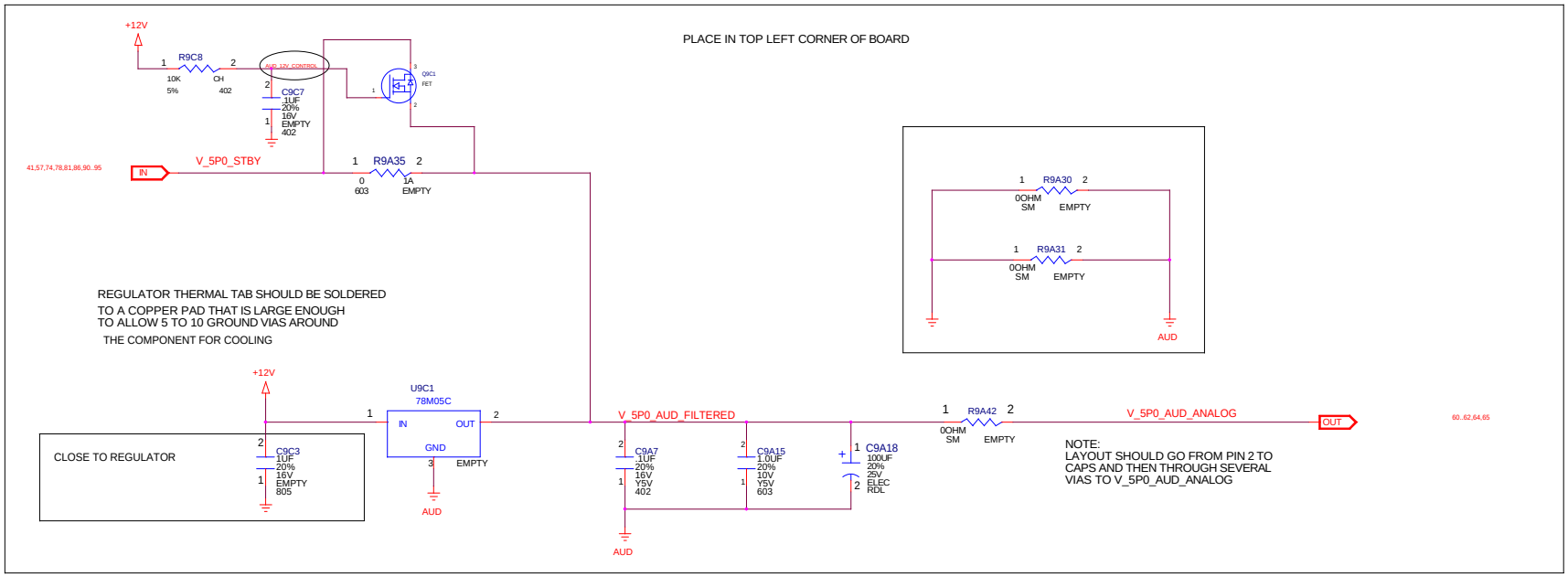
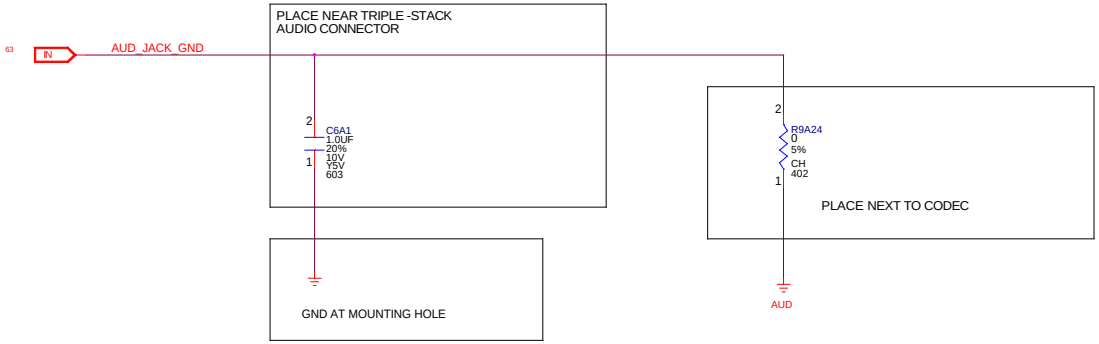




[PAGE_TITLE=AUDIO_VREG]

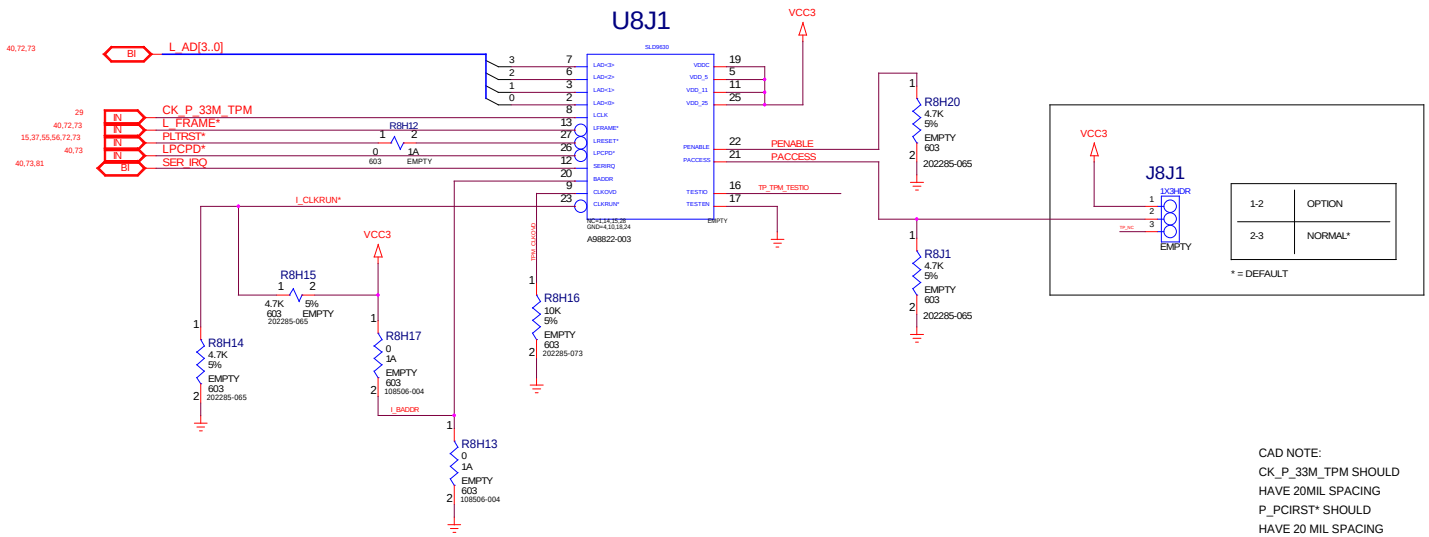
INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	66	4.0

BLANK

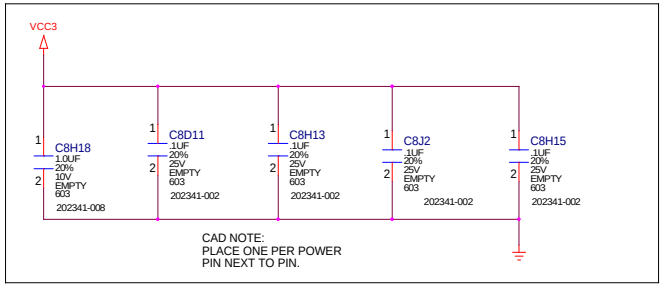
BLANK

BLANK

SECURITY: TPM (TRUSTED PLATFORM MODULE)



CAD NOTE:
CK_P_33M_TPM SHOULD
HAVE 20MIL SPACING
P_PCIRST* SHOULD
HAVE 20 MIL SPACING
LAD<3..0> HAS 5 MIL
SPACING BETWEEN OTHER LAD
SIGNALS, BUT 10 MILS TO ALL
OTHER SIGNALS.



CAD NOTE:
PLACE ONE PER POWER
PIN NEXT TO PIN.

TPM (TRUSTED PLATFORM MODULE)

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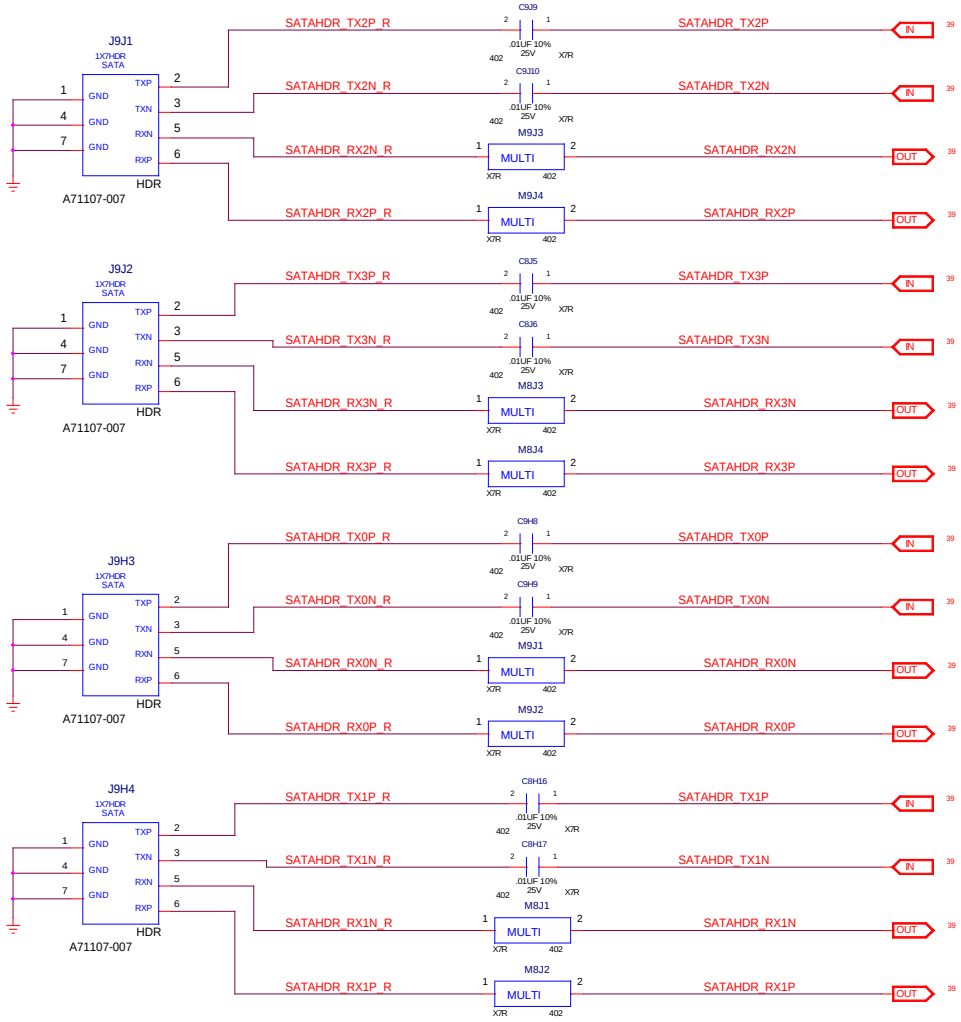
	C77862	70	4.0

BOM NOTE:

FOR M-SITES, USE
A36096-008 (.01UF, 0402)



[PAGE_TITLE=SATA CONNECTORS]

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

BOM NOTE:
USING IPN C55248-001

J8J4
1X3HDR
HDR

BOM NOTE:
FOR YELLOW JUMPER
USE IPN 634479-005

U8J2
FWH
IC

J7J2
JUMPER
EMPTY
ALWAYS EMPTY
MFG MODE PADS

EMPTY
102276-001
BIOS_WP
J8H1

FIRMWARE HUB DECOUPLING

<XR_PAGE_TITLE>

IR HEADER

ADD IR HEADER CIRCUIT

[PAGE_TITLE=PORT ANGELES (1 OF 2)]

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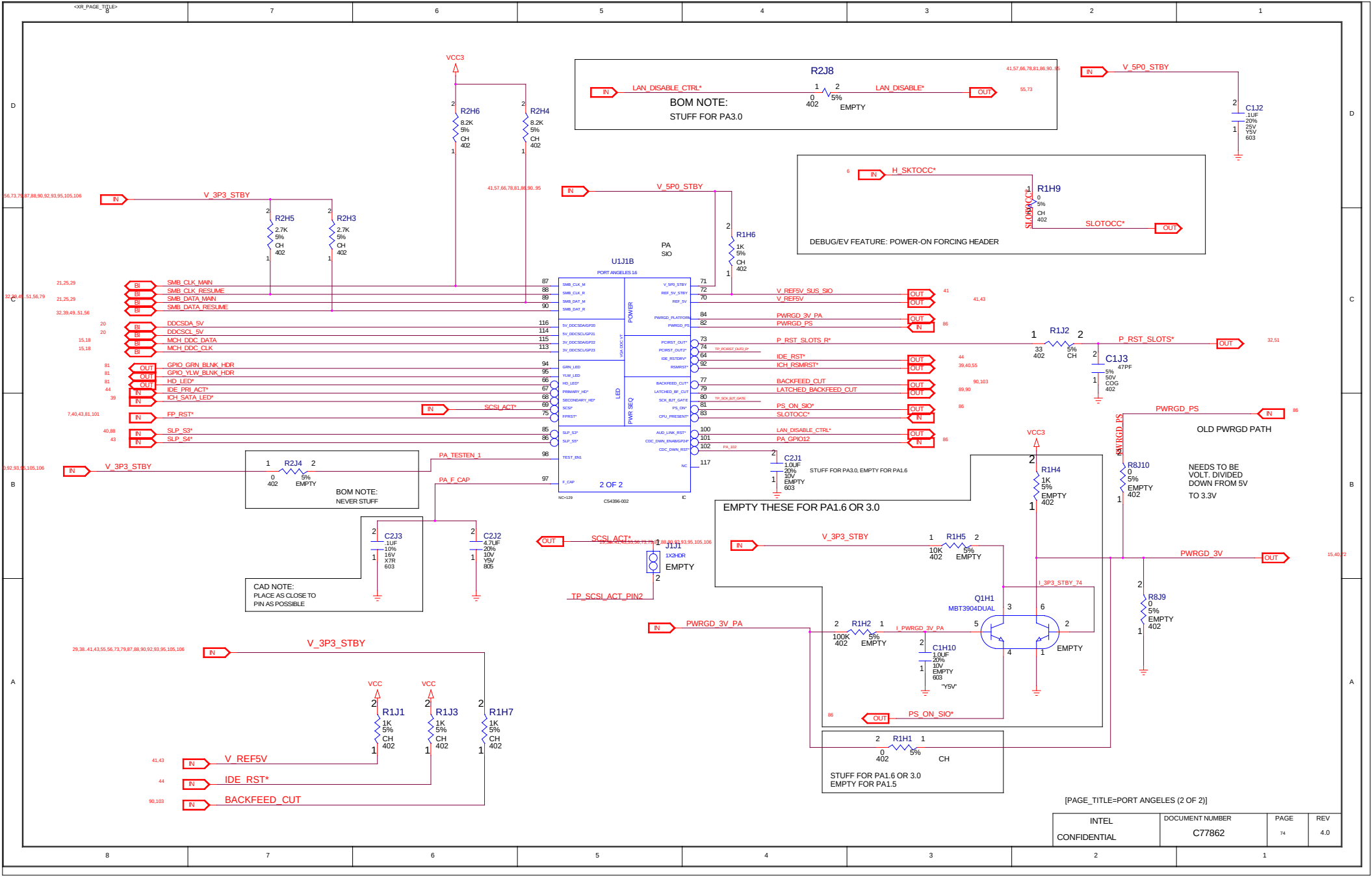
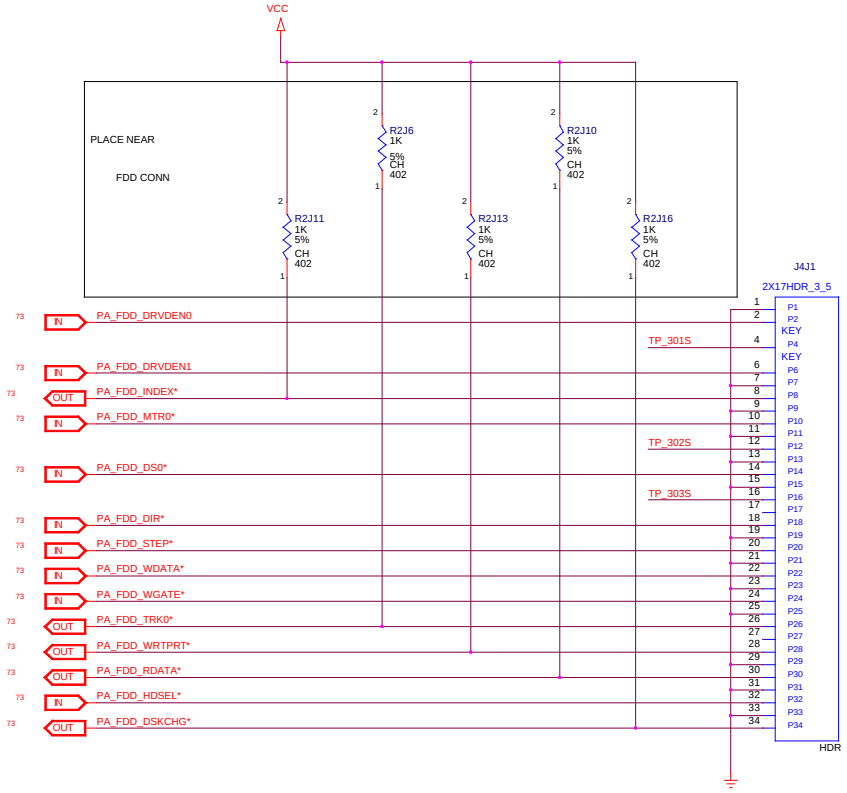

R2J8
LAN_DISABLE_CTRL*
LAN_DISABLE*
BOM NOTE:
STUFF FOR PA3.0
EMPTY
V_5P0_STBY
C1J2
H_SKTOCC*
R1H9
SLOTOCC*
DEBUG/EV FEATURE: POWER-ON FORCING HEADER
VCC3
R2H6
R2H4
8.2K
V_3P3_STBY
R2H5
R2H3
2.7K
U1J1B
PORT ANGELES 16
PA
SIO
R1H6
1K
SMB_CLK_MAIN
SMB_CLK_RESUME
SMB_DATA_MAIN
SMB_DATA_RESUME
DDCSDA_5V
DDCSCL_5V
MCH_DDC_DATA
MCH_DDC_CLK
GPIO_GRN_BLNK_HDR
GPIO_YLW_BLNK_HDR
HD_LED*
IDE_PRI_ACT*
ICH_SATA_LED*
FP_RST*
SLP_S3*
SLP_S4*
SCSI_ACT*
V_REF5V_SUS_SIO
V_REF5V
PWRGD_3V_PA
PWRGD_PS
P_RST_SLOTS_R*
IDE_RST*
ICH_RSMRST*
BACKFEED_CUT
LATCHED_BACKFEED_CUT
PS_ON_SIO*
SLOTOCC*
LAN_DISABLE_CTRL*
PA_GPIO12
R1J2
33
P_RST_SLOTS*
C1J3
47PF
R2J4
PA_TESTEN_1
PA_F_CAP
BOM NOTE:
NEVER STUFF
C2J1
1.0UF
STUFF FOR PA3.0, EMPTY FOR PA1.6
C2J3
.1UF
C2J2
4.7UF
CAD NOTE:
PLACE AS CLOSE TO
PIN AS POSSIBLE
J1J1
1X2HDR
TP_SCSI_ACT_PIN2
EMPTY THESE FOR PA1.6 OR 3.0
R1H4
R1H5
10K
R8J10
0
PWRGD_PS
OLD PWRGD PATH
NEEDS TO BE
VOLT. DIVIDED
DOWN FROM 5V
TO 3.3V
PWRGD_3V
R8J9
Q1H1
MBT3904DUAL
R1H2
100K
C1H10
1.0UF
"Y5V"
PS_ON_SIO*
R1H1
STUFF FOR PA1.6 OR 3.0
EMPTY FOR PA1.5
R1J1
R1J3
R1H7
V_REF5V
IDE_RST*
BACKFEED_CUT
[PAGE_TITLE=PORT ANGELES (2 OF 2)]
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
C77862
PAGE
74
REV
4.0



[PAGE_TITLE=FDD CONN]

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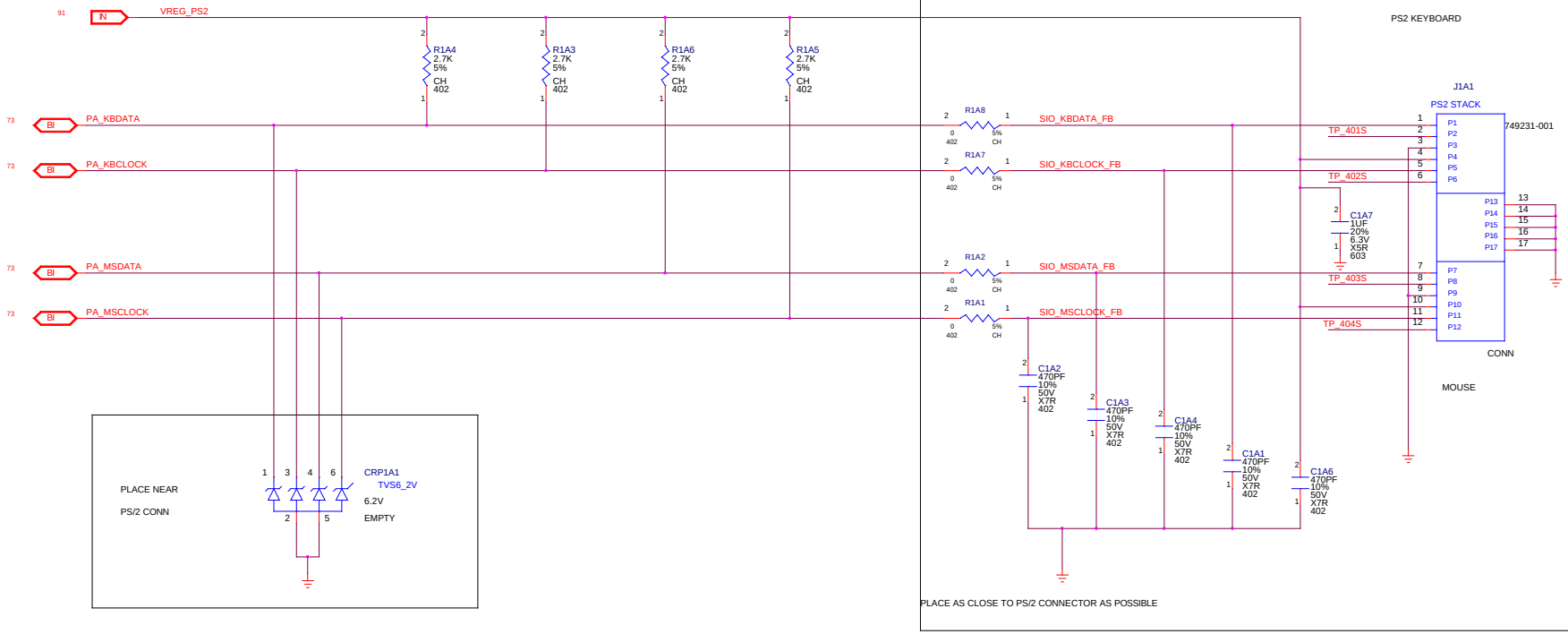
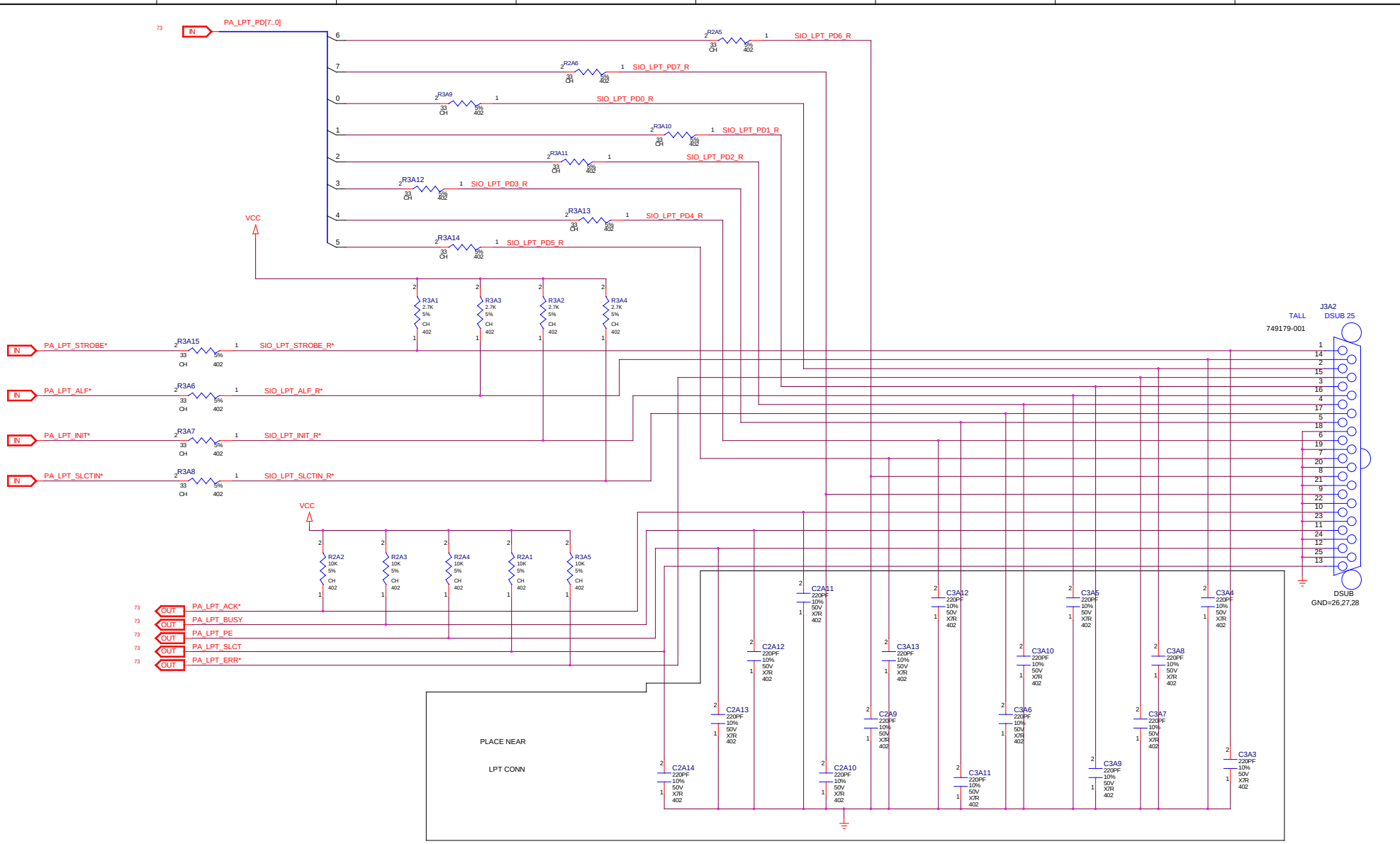
COMPONENTS ARE DFM29



INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	76	4.0



[PAGE_TITLE=LPT CONN]

INTEL CONFIDENTIAL	DOCUMENT NUMBER C77862	PAGE 77	REV 4.0

DO NOT USE NATIONAL
OR GOLDSTAR PARTS OF THIS
BASE P/N

U1H1
GD75232S
621111-103

PA_COM_DCD1*
PA_COM_DSR1*
PA_COM_RXD1
PA_COM_CTS1*
PA_COM_RI1*
PA_COM_RTS1*
PA_COM_TXD1
PA_COM_DTR1*

NOTE DIRECTION
IC
VCC=20
GND=11
VCC=V_5P0_STBY
+12V
-12V

PLACE NEAR CONNECTOR

C2A8 C2A7 C2A6 C2A3 C2A1 C2A5 C2A4 C2A2
470PF 10% 50V X7R 402

SERIAL PORT A
J2A1
749218-001
2 ROW
DSUB

SIO_COM_DCD1_232
SIO_COM_DSR1_232
SIO_COM_RXD1_232*
SIO_COM_RTS1_232
SIO_COM_TXD1_232*
SIO_COM_CTS1_232
SIO_COM_DTR1_232
SIO_COM_RI1_232

R2A7 0 5% 402 EMPTY
2ZA1_GND

VCC
R1J6 330 5% 402 EMPTY
ENABLE_5V_1
R1J10 330 5% 402 CH
IN V_5P0_STBY
41,57,66,74,81,86,90..95

SMC0402
C1A5 470PF 10% 50V Y5V 402

J1J2
1X3HDR
HDR

1-2 = ENABLE 5V (DISABLE WOR)
2-3 = DISABLE 5V (ENABLE WOR)
2-3 = DEFAUL

COM_RI_WAKE* OUT 40,43
R8D2 10K 5% 603 EMPTY
WOM_CTRL
R8D1 2.2K 5% 603 EMPTY
Q8D1 MMBT3904 EMPTY
108969-001
COM1
WAKE_ON_MODEM_E

J9G2
1X3HDR
WAKE_ON_MODEM
OPT_WOM_HDR
COM_RI_WAKE* IN 40,43

+12V -12V
C1H9 C1H4 C9D6
.1UF 20% 25V Y5V 603
202341-002

PLACE DECOUPLING NEAR 232 CNTRL/DRIVER
PINS 1, 10, AND 20 RESPECTIVELY
BOM=CORE_COM1

ADD COM2 HEADER CIRCUIT

OPT_COM2
COM2
U1G1
GD75232S

PA_COM_DCD2*
PA_COM_DSR2*
PA_COM_RXD2
PA_COM_CTS2*
PA_COM_RI2*
PA_COM_RTS2*
PA_COM_TXD2
PA_COM_DTR2*

NOTE DIRECTION
EMPTY
VCC=20
GND=11
VCC=V_5P0_STBY
+12V
-12V

PA_COM_DCD2_232
PA_COM_DSR2_232
PA_COM_RXD2_232*
PA_COM_CTS2_232
PA_COM_RI2_232
PA_COM_RTS2_232
PA_COM_TXD2_232*
PA_COM_DTR2_232

C1G2 C1G3 C1G5 C1G11 C1G9 C1G6 C1G8 C1G10
OPT_COM2 COM2
470PF 10% 50V EMPTY 402

COM2
OPT_COM2
J1G2
SERIAL PORT
2X5HDR_10
EMPTY
SERIAL PORT B

R1G4 0 5% 402 EMPTY
2ZH1_GND

VCC
R1J4 330 5% 402 EMPTY
ENABLE_5V_2
R1H3 330 5% 402 EMPTY
IN V_5P0_STBY
41,57,66,74,81,86,90..95

SMC0402
C1G14 470PF 10% 50V EMPTY 402

J1H1
1X3HDR
EMPTY

1-2 = ENABLE 5V (DISABLE WOR)
2-3 = DISABLE 5V (ENABLE WOR)
2-3 = DEFAUL

+12V -12V
COM2_DCPL
OPT_COM2
202341-002
C1G4 C1G7 C1H6
.1UF 20% 25V EMPTY 603

PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY
BOM= OPT_COM2

[PAGE_TITLE=SERIAL PORT A]

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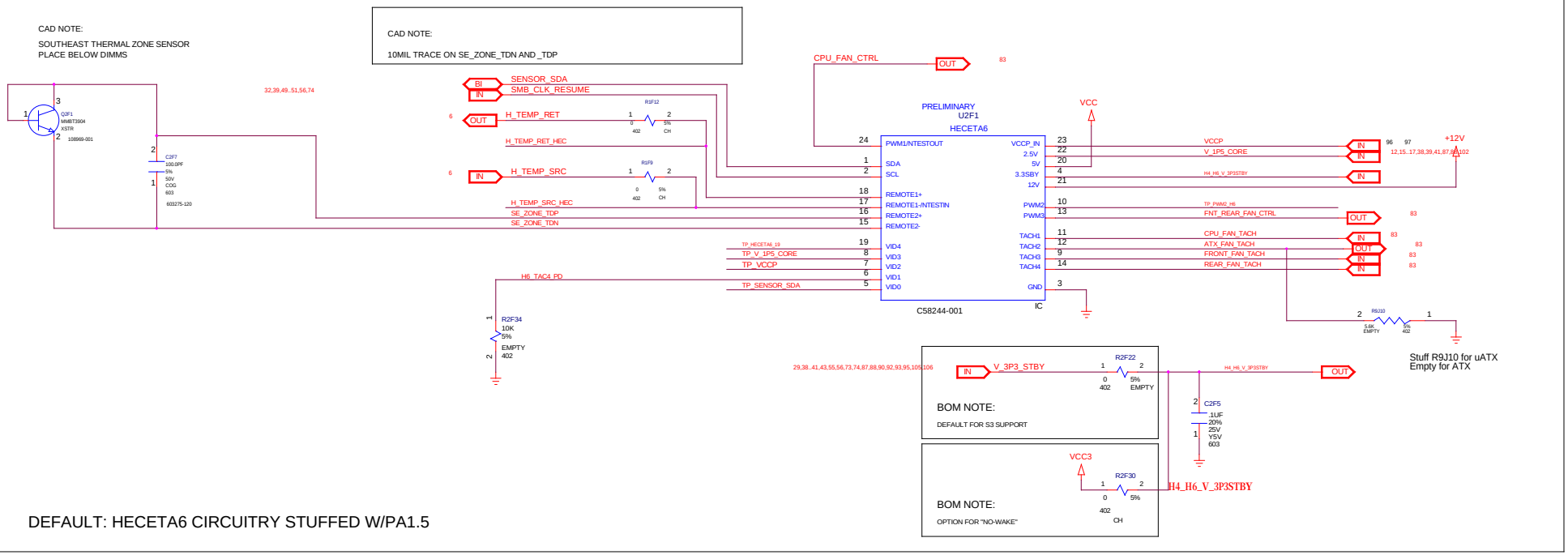
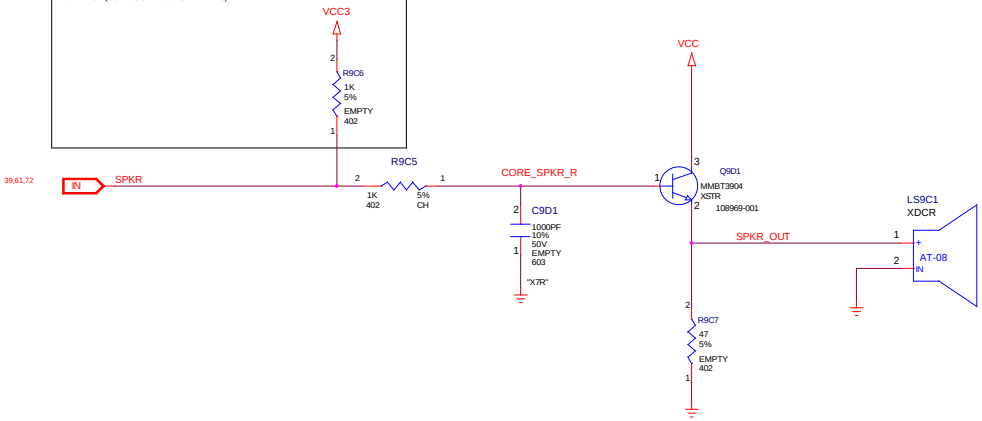
CONFIDENTIAL	C77862	78	4.0



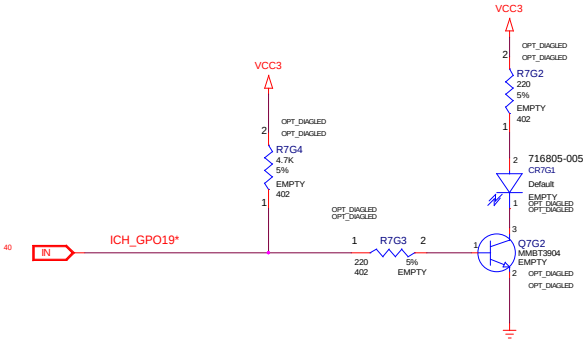
BOM NOTE:

OPTION FOR "SATELLITE HECETA" WHEN PORT ANGELES 3.0 IS USED

BOM NOTE:
STUFF TO DISABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).



DIAGNOSTIC LED (RED)



[PAGE_TITLE=SPEAKER_DIAGNOSTIC_LED]

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	80	4.0

<XR_PAGE_TITLE>

ADD SERIRQ HDR CIRCUIT

BOM NOTE:
UNSTUFF FOR C

BOM NOTE FOR J9J4:
USE IPN 109717-756
FOR 2X5 MULTI-COLOR HDR
USE IPN 109717-742
FOR 2X5 WHITE HDR

DESIGN NOTE:
SHARED WITH LED 1X3 HEADER

DESIGN NOTE:
STUFF ONLY FOR
ENERGY LAKE, THEN
EMPTY 0 OHM BYPASS.

DESIGN NOTE:
IF LED HEADER IS NOT PLACED RIGHT NEXT TO FP HEADER,
THEN NEED TO ADD A 470UF 0603 CAP TO EACH OF THESE SIGNALS.
OTHERWISE, THEY CAN SHARE CAP WITH FP HEADER PINS 2 AND 4...

BOM=CORE_STDFNTPNL_E

602431-005

A36093-023

A36093-005

102276-304

[PAGE_TITLE=STD_FRONT_PANEL_HDR]

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PB MOUNTING HOLES

J8A1
MTG_HOLE
NC9 9
EMPTY

J7J1
MTG_HOLE
NC9 9
EMPTY

J1G1
MTG_HOLE
NC9 9
EMPTY

J1B1
MTG_HOLE
NC9 9
EMPTY

J7G1
MTG_HOLE
NC9 9
EMPTY

J1J3
MTG_HOLE
NC9 9
EMPTY

J7A1
MTG_HOLE
NC9 9
EMPTY

J9G1
MTG_HOLE
NC9 9
EMPTY

J11G1
MTG_HOLE
NC9 9
EMPTY

LABELS

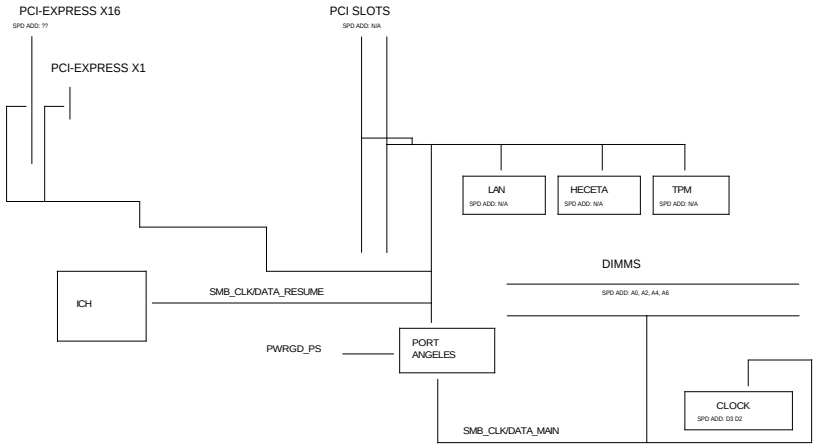
200956-001; "CE" MARK SHOULD BE COVERED WITH A BLANK LABEL UNTIL CERTIFIED
628492-001; "FCC" MARK SHOULD BE COVERED WITH A BLANK LABEL UNTIL CERTIFIED (SECONDARY SIDE)
622954-001; "C-TICK" MARK SHOULD BE COVERED WITH A BLANK LABEL UNTIL CERTIFIED

LB4F2
LABEL
1 SILK
EMPTY
'KOREAN CERT' SILKSCREEN COVERED UNTIL CERTIFIED
MAKE EMPTY ON BOM

C69649-001
1375X250_TARGET
LB3F1
LABEL
1
CHANGE TO PROJECT ISN ON BOM (MOD-FILE CHANGE): CXXXXX-001

LB4F1
LABEL
1
A19202-001
EMPTY
'INTEL-BRANCH"
MAKE EMPTY ON BOM

SMBUS MAP



SMB_CLK/DATA_MAIN

CLOCK
PORT ANGELES
DIMMS (2 TIMES)

SMB_CLK/DATA_RESUME

PCI (2 TIMES)
LAN
HECETA
PORT ANGELES
ICH
PCI-EXPRESS X16
PCI-EXPRESS X1
SECURITY (TPM)

[PAGE_TITLE=MTG_HOLES/LABELS/SMBUS_MAP]

<XR_PAGE_TITLE>

FAN CONTROL

CPU ALWAYS-ON FAN

(PLACE BELOW/RIGHT CPU SOCKET)

BOM NOTE:
STUFF FOR 3-PIN CONTROLLED FAN

BOM NOTE:
STUFF FOR 4-PIN FAN OR 3-PIN ALWAYS ON

BOM NOTE:
USE IPN 201581-103 FOR 3-PIN FAN HEADERS

REAR CHASSIS FAN

(PLACE ABOVE/RIGHT CPU SOCKET)

BOM NOTE:
ALWAYS STUFF. FOR HECETA6 SMBUS ADDRESS

BOM NOTE:
STUFF FOR 4-PIN FAN OR 3-PIN ALWAYS ON

BOM NOTE:
STUFF FOR 4-PIN FAN OR 3-PIN ALWAYS ON

FRONT CHASSIS FAN

(PLACE LOWER LEFT CORNER OF PLATFORM)

BOM NOTE:
STUFF FOR 4-PIN FAN OR 3-PIN ALWAYS ON

REAR CHASIS FAN #2 -ATX

(PLACE ON FULL ATX PORCH NEAR THE BACK)

BOM NOTE:
STUFF FOR 4-PIN FAN OR 3-PIN ALWAYS ON

OPTIONAL SITE FOR ATX FAN

(PLACE ON FULL ATX PORCH NEAR THE FRONT)
STUFF EITHER REAR FAN #2 OR THIS OPTIONAL SITE

BOM NOTE:
STUFF FOR 4-PIN FAN OR 3-PIN ALWAYS ON

BOM NOTE:
EMPTY FOR 4-PIN FAN OR 3-PIN ALWAYS ON

[PAGE_TITLE=FAN CONTROL]

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MCH

X.X (VCCP)

1.5 CORE

2.5 SM

2.5 STBY

ICH

3.3 (VCC3)

1.5 CORE

2.5 STBY

5.0 STBY

CK-410

3.3 (VCC3)

HEC6

3.3 STBY (VCC3 STBY)

5.0 (VCC)

12

X.X (VCCP)

1.5 (CORE)

SIO

3.3 (VCC3)

5.0 (VCC)

3.3 STBY (VCC3 STBY)

GLUECHIP

3.3 STBY (VCC3_STBY)

3.3 STBY (VCC3_STBY)

5.0 STBY (VCC STBY)

MARVELL LAN

3.3 PCIVAUX

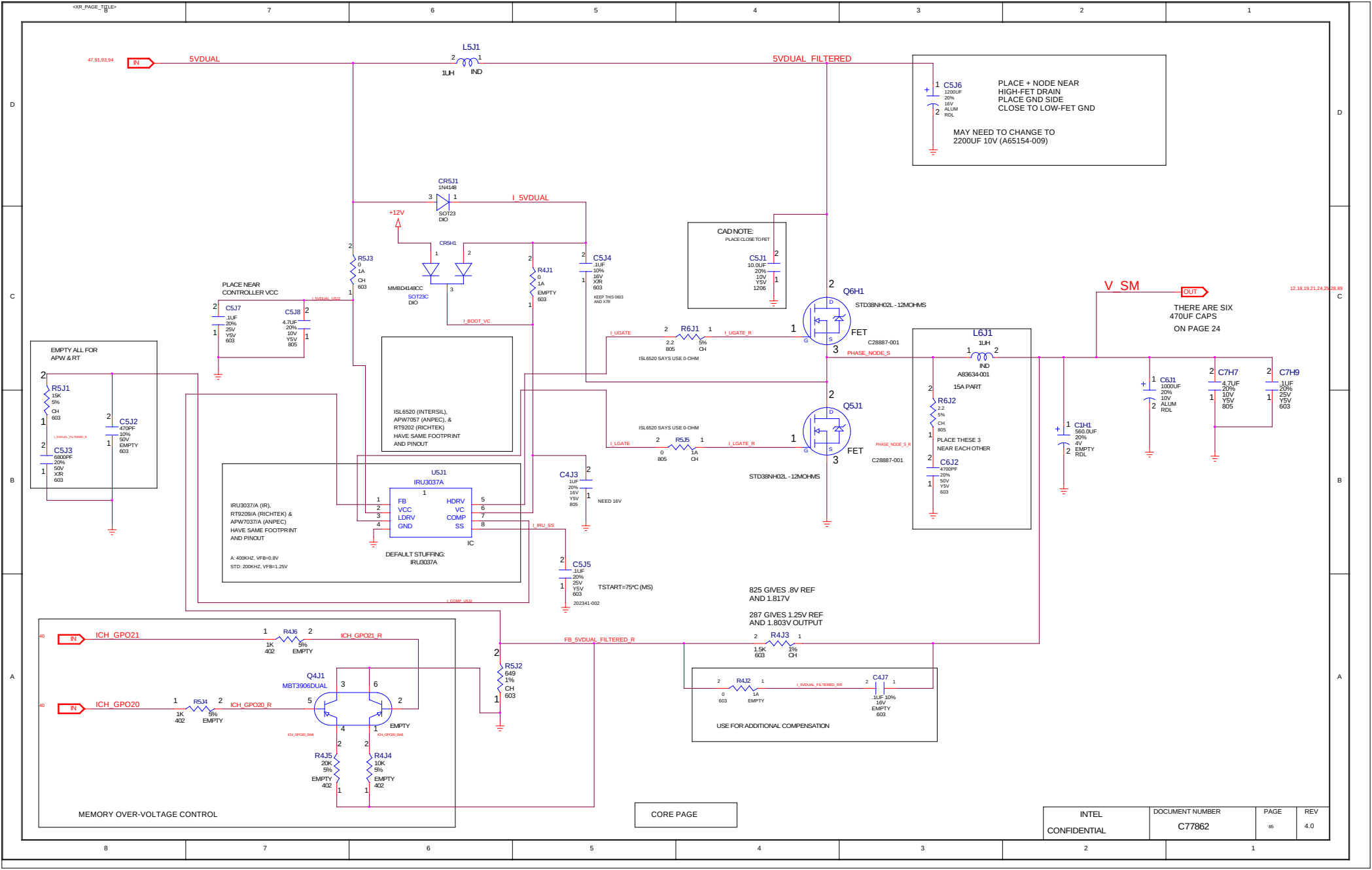
FWH

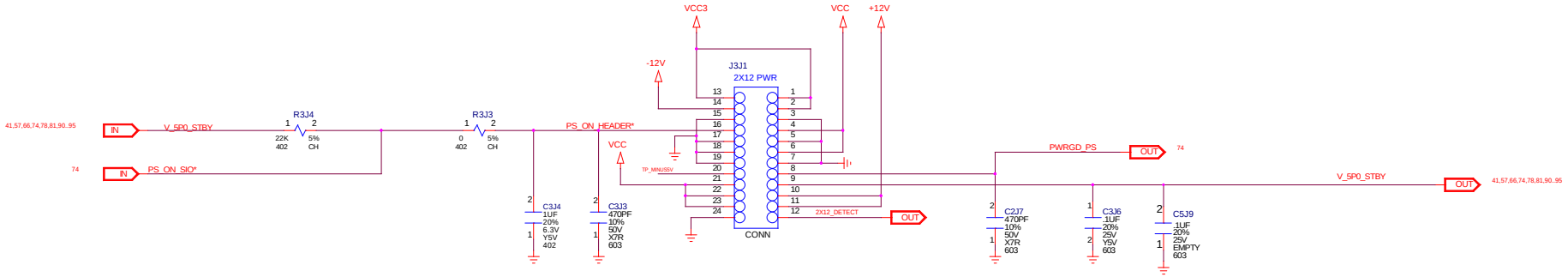
3.3 (VCC3)

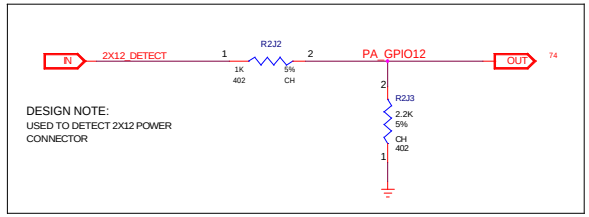
VREG_12V_FILTERED (+12V FILTERED FROM 12V POWER-SUPPLY)
V_SM_VTT (1.3V DERIVED FROM V_SM)
V_SM (2.6V DERIVED FROM 5VDUAL)
VREG_USB_BP_LEFT (5VDUAL)
VREG_USB_BP_RIGHT (5VDUAL)
VREG_USB_BP_MID (5VDUAL)
VREG_PS2 (5VDUAL)
USB_FNT_PWR (5VDUAL)
V_3P3_PCI_VAUX (3.3V OR 3.3-STANDBY SOURCE)
V_3P3_STBY (3.3V DERIVED FROM 5.0-STANDBY)
V_5P0_STBY (5.0V FROM POWER-SUPPLY)
V_BAT_VREG_R_CR (3.0V FROM THE BATTERY)
V_3P0_BAT_VREG (~3.0V FROM THE BATTERY THROUGH A DIODE)
+12V (PLUS 12V FROM POWER-SUPPLY)
-12V (MINUS 12V FROM POWER-SUPPLY)
VCC3 (3.3V FROM POWER-SUPPLY)
VCC (5.0V FROM POWER-SUPPLY)

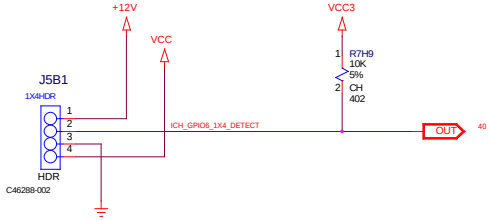
V_1P5_CORE (NOT CONNECTED)
V_1P25_MEMVTT_B (NOT CONNECTED)
V_1P3_NOMINAL (NOT CONNECTED)
V_1P5_AGP (DERVIVED FROM 1.5V CORE) (NOT CONNECTED)
V_12VREG (NOT CONNECTED)
V_AGP_VDDQ (DERVIVED FROM 1.5V CORE) (NOT CONNECTED)

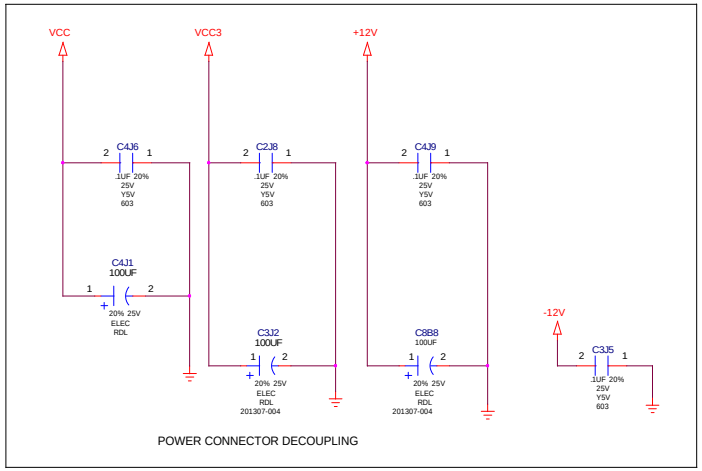
[PAGE_TITLE=VREG: VOLTAGE DISTRIBUTION]

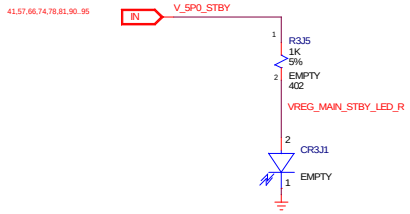

5VDUAL
L5J1
1UH
IND
5VDUAL_FILTERED
C5J6
1200UF
20%
16V
ALUM
RDL
PLACE + NODE NEAR
HIGH-FET DRAIN
PLACE GND SIDE
CLOSE TO LOW-FET GND
MAY NEED TO CHANGE TO
2200UF 10V (A65154-009)
CR5J1
1N4148
SOT23
DIO
I_5VDUAL
+12V
CRSH1
MMBD4148CC
SOT23C
DIO
R5J3
0
1A
CH
603
R4J1
0
1A
EMPTY
603
C5J4
.1UF
10%
16V
X7R
603
CAD NOTE:
PLACE CLOSE TO FET
C5J1
10.0UF
20%
10V
Y5V
1206
Q6H1
STD38NH02L - 12MOHMS
FET
C28887-001
PLACE NEAR
CONTROLLER VCC
C5J7
.1UF
20%
25V
Y5V
603
C5J8
4.7UF
20%
10V
Y5V
805
I_BOOT_VC
I_UGATE
R6J1
2.2
805
5%
CH
I_UGATE_R
ISL6520 SAYS USE 0-OHM
PHASE_NODE_S
V_SM
OUT
THERE ARE SIX
470UF CAPS
ON PAGE 24
12,18,19,21,24,25,28,89
EMPTY ALL FOR
APW & RT
R5J1
15K
5%
CH
603
C5J2
680PF
10%
50V
EMPTY
603
C5J3
6800PF
20%
50V
X7R
603
ISL6520 (INTERSIL),
APW7057 (ANPEC), &
RT9202 (RICHTEK)
HAVE SAME FOOTPRINT
AND PINOUT
Q5J1
FET
C28887-001
STD38NH02L - 12MOHMS
I_LGATE
R5J5
0
805
1A
CH
I_LGATE_R
ISL6520 SAYS USE 0-OHM
PHASE_NODE_S_R
L6J1
1UH
IND
A83634-001
15A PART
R6J2
2.2
5%
CH
805
PLACE THESE 3
NEAR EACH OTHER
C6J2
4700PF
20%
50V
Y5V
603
C1H1
560.0UF
20%
4V
EMPTY
RDL
C6J1
1000UF
20%
10V
ALUM
RDL
C7H7
4.7UF
20%
10V
Y5V
805
C7H9
.1UF
20%
25V
Y5V
603
U5J1
IRU3037A
FB
VCC
LDRV
GND
HDRV
VC
COMP
SS
IC
IRU3037/A (IR),
RT9209/A (RICHTEK) &
APW7037/A (ANPEC)
HAVE SAME FOOTPRINT
AND PINOUT
A: 400KHZ, VFB=0.8V
STD: 200KHZ, VFB=1.25V
DEFAULT STUFFING:
IRU3037A
C4J3
1UF
20%
16V
Y5V
805
NEED 16V
I_IRU_SS
C5J5
.1UF
20%
25V
Y5V
603
202341-002
TSTART=75*C (MS)
825 GIVES .8V REF
AND 1.817V
287 GIVES 1.25V REF
AND 1.803V OUTPUT
I_COMP_U5J2
FB_5VDUAL_FILTERED_R
R4J3
1.5K
603
1%
CH
R5J2
649
1%
CH
603
R4J2
0
603
1A
EMPTY
I_5VDUAL_FILTERED_RR
C4J7
.1UF 10%
16V
EMPTY
603
USE FOR ADDITIONAL COMPENSATION
ICH_GPO21
R4J6
1K
402
5%
EMPTY
ICH_GPO21_R
Q4J1
MBT3906DUAL
ICH_GPO20
R5J4
1K
402
5%
EMPTY
ICH_GPO20_R
ICH_GPO20_SW1
ICH_GPO20_SW1
EMPTY
R4J5
20K
5%
EMPTY
402
R4J4
10K
5%
EMPTY
402
MEMORY OVER-VOLTAGE CONTROL
CORE PAGE
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
C77862
PAGE
85
REV
4.0

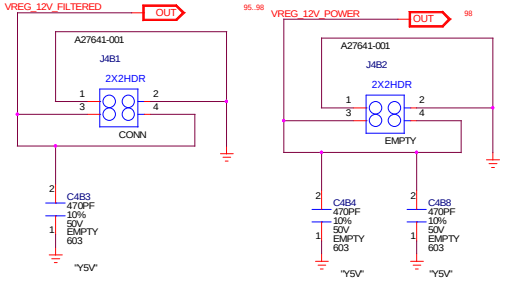






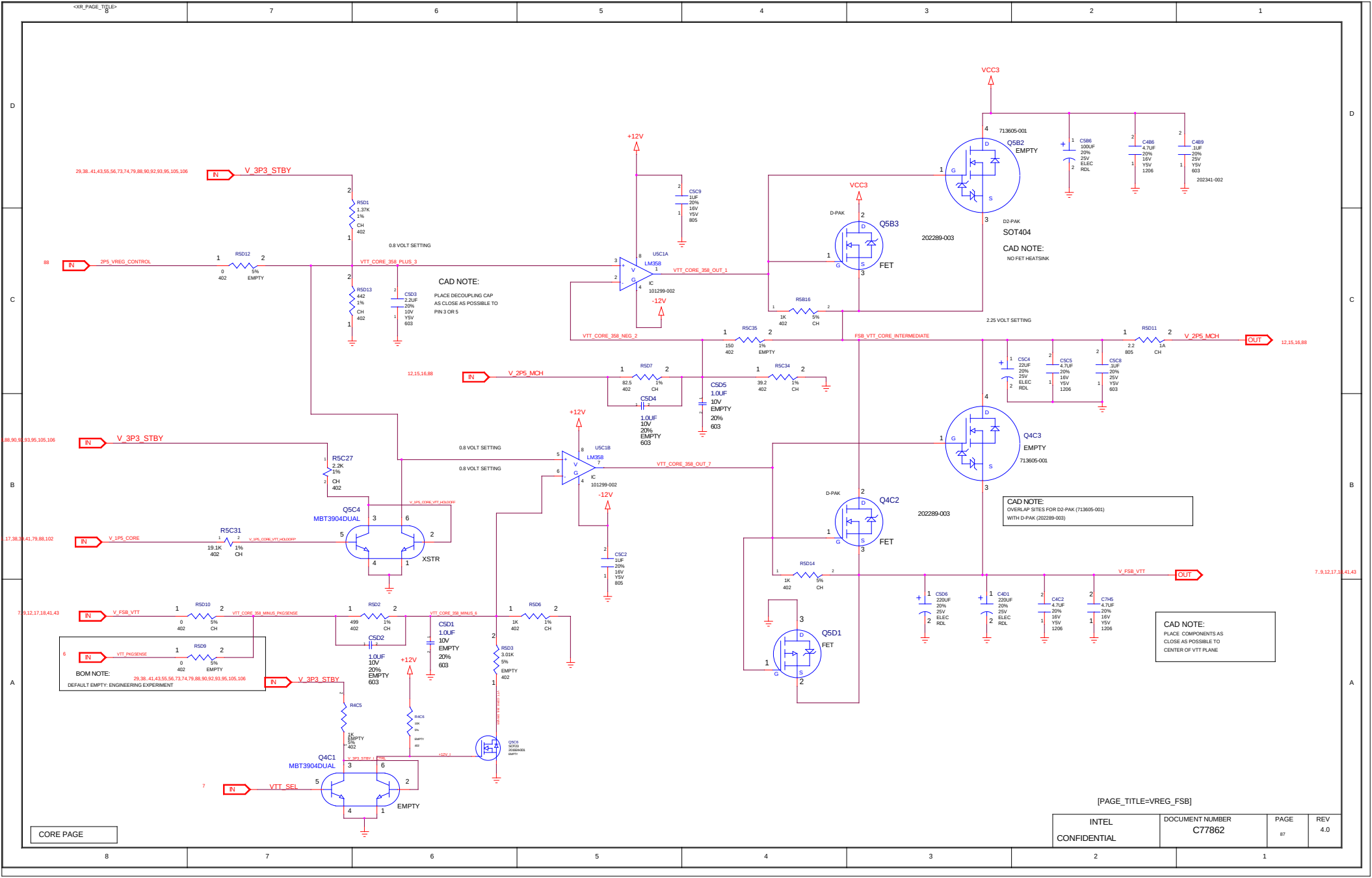






[PAGE_TITLE=STANDARD POWER CONNECTOR]

CORE PAGE


V_3P3_STBY
2P5_VREG_CONTROL
VTT_CORE_358_PLUS_3
0.8 VOLT SETTING
CAD NOTE:
PLACE DECOUPLING CAP
AS CLOSE AS POSSIBLE TO
PIN 3 OR 5
U5C1A
LM358
IC
101299-002
VTT_CORE_358_OUT_1
+12V
-12V
VCC3
Q5B3
FET
D-PAK
202289-003
Q5B2
EMPTY
713605-001
D2-PAK
SOT404
CAD NOTE:
NO FET HEATSINK
2.25 VOLT SETTING
FSB_VTT_CORE_INTERMEDIATE
V_2P5_MCH
OUT
V_1P5_CORE
R5C27
2.2K
R5C31
19.1K
Q5C4
MBT3904DUAL
XSTR
U5C1B
VTT_CORE_358_OUT_7
Q4C3
EMPTY
713605-001
Q4C2
202289-003
CAD NOTE:
OVERLAP SITES FOR D2-PAK (713605-001)
WITH D-PAK (202289-003)
V_FSB_VTT
VTT_CORE_358_MINUS_PKGSENSE
VTT_CORE_358_MINUS_6
VTT_PKGSENSE
BOM NOTE:
DEFAULT EMPTY: ENGINEERING EXPERIMENT
Q5D1
FET
CAD NOTE:
PLACE COMPONENTS AS
CLOSE AS POSSIBLE TO
CENTER OF VTT PLANE
Q4C1
MBT3904DUAL
VTT_SEL
EMPTY
[PAGE_TITLE=VREG_FSB]
CORE PAGE
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
C77862
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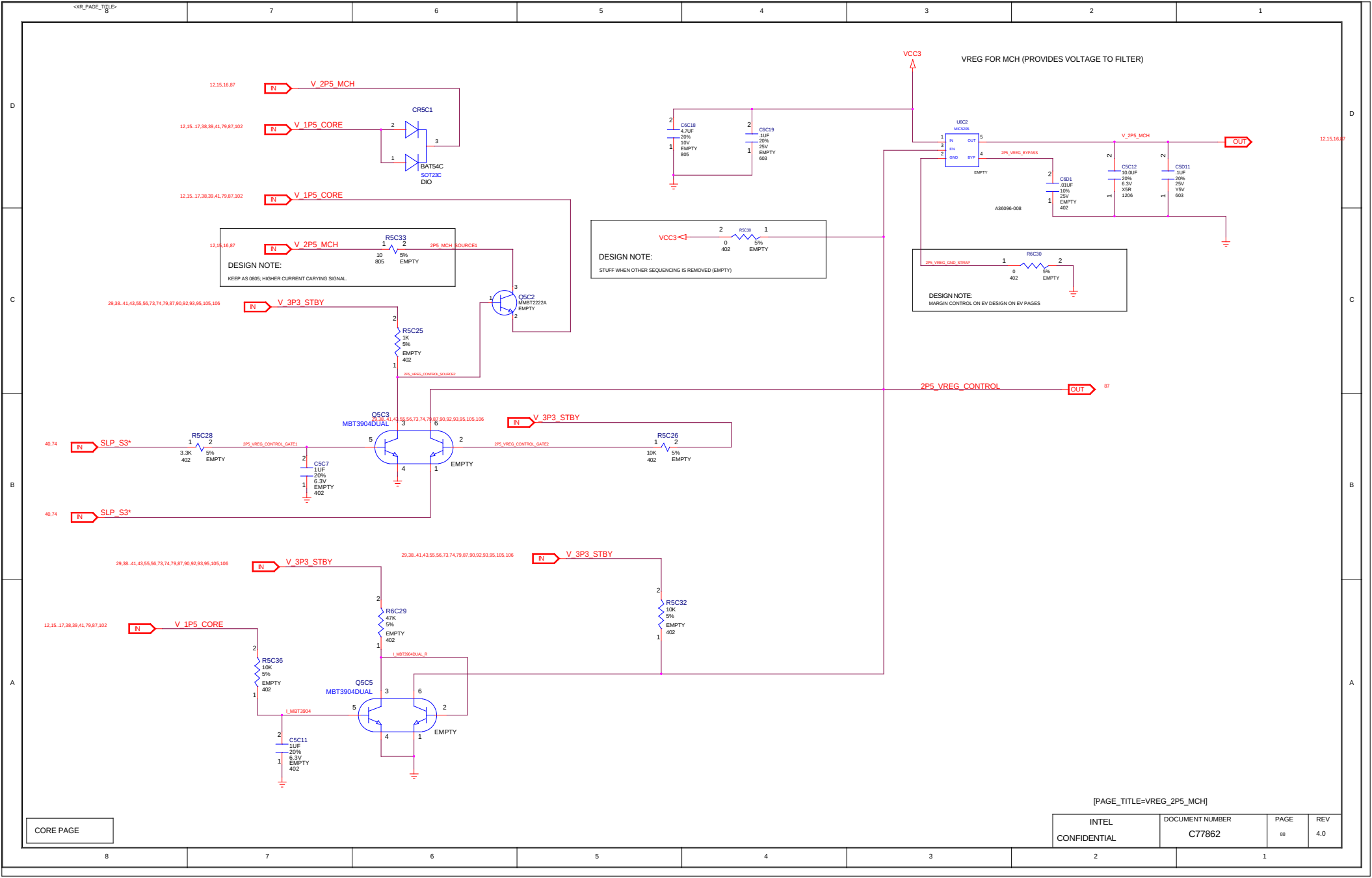
REV
4.0

<XR_PAGE_TITLE>

VREG FOR MCH (PROVIDES VOLTAGE TO FILTER)



[PAGE_TITLE=VREG_2P5_MCH]

CORE PAGE

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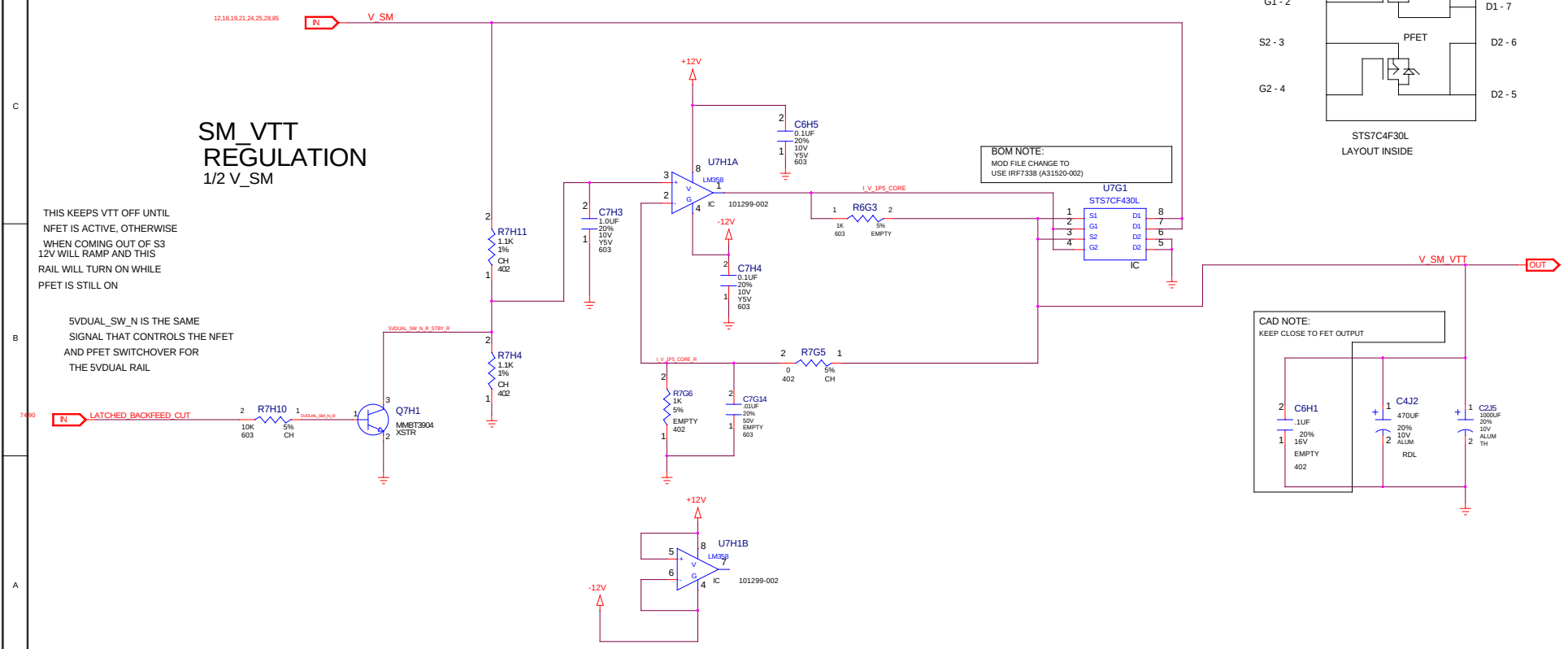
	C77862	88	4.0

SM_VTT REGULATION
1/2 V_SM

THIS KEEPS VTT OFF UNTIL
NFET IS ACTIVE, OTHERWISE
WHEN COMING OUT OF S3
12V WILL RAMP AND THIS
RAIL WILL TURN ON WHILE
PFET IS STILL ON

5VDUAL_SW_N IS THE SAME
SIGNAL THAT CONTROLS THE NFET
AND PFET SWITCHOVER FOR
THE 5VDUAL RAIL



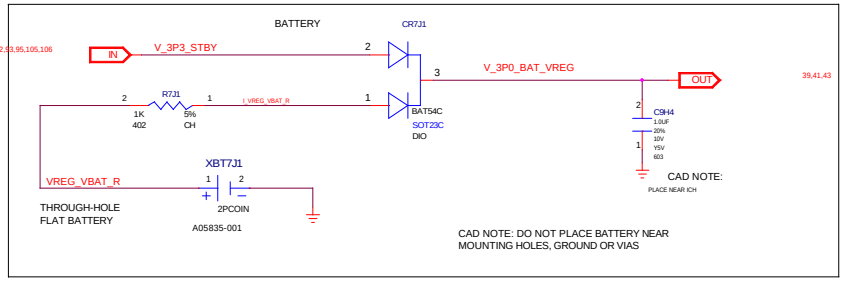
N-FET 18MOHM - 7A
P-FET 70MOHM - 4A

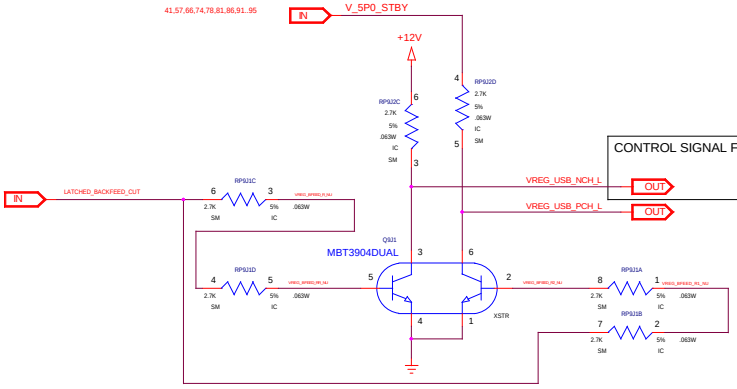
STS7C4F30L
LAYOUT INSIDE

CORE PAGE

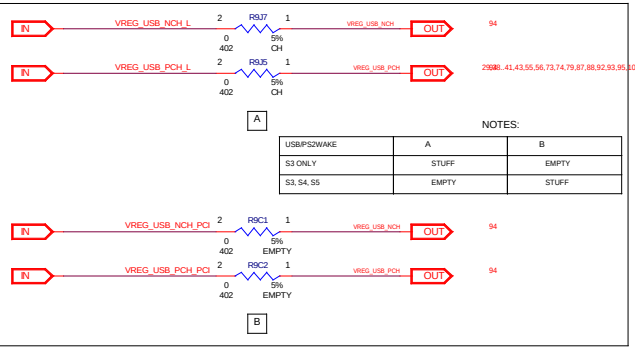
[PAGE_TITLE=VREG_SM_VTT]

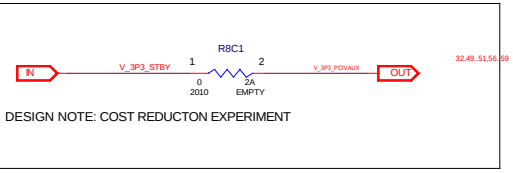
INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	89	4.0

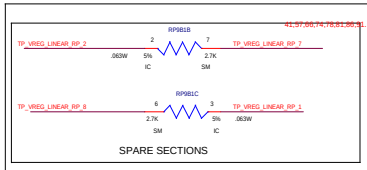


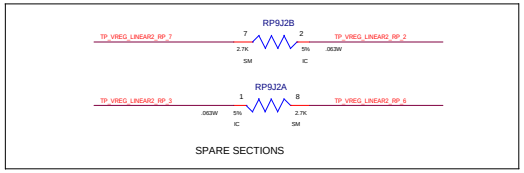


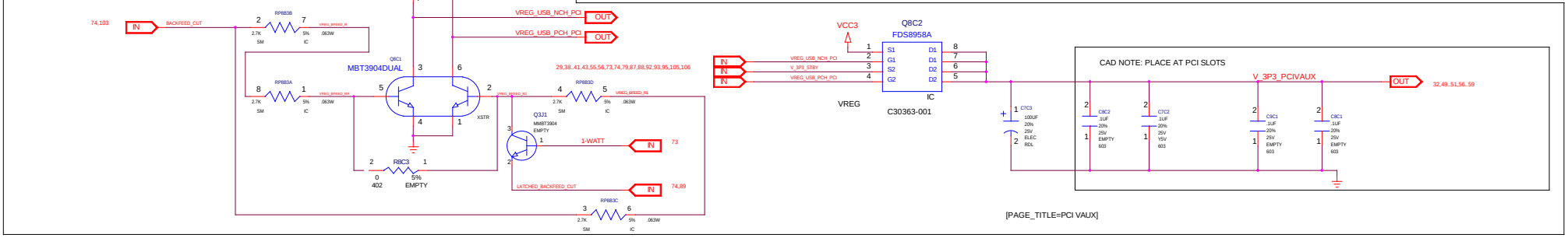
CONTROL SIGNAL FOR 4-DIMM VREG CONTROLLER





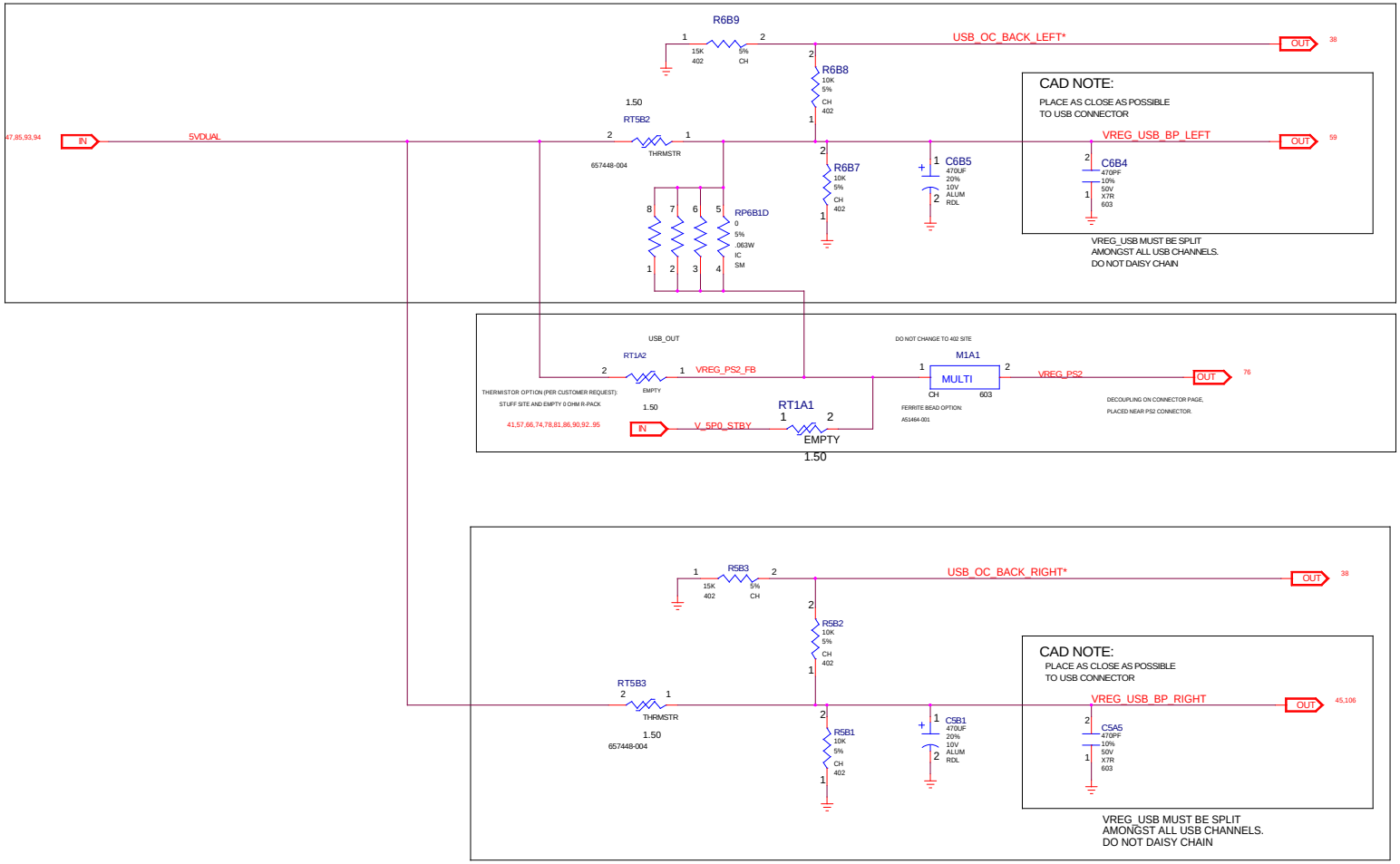




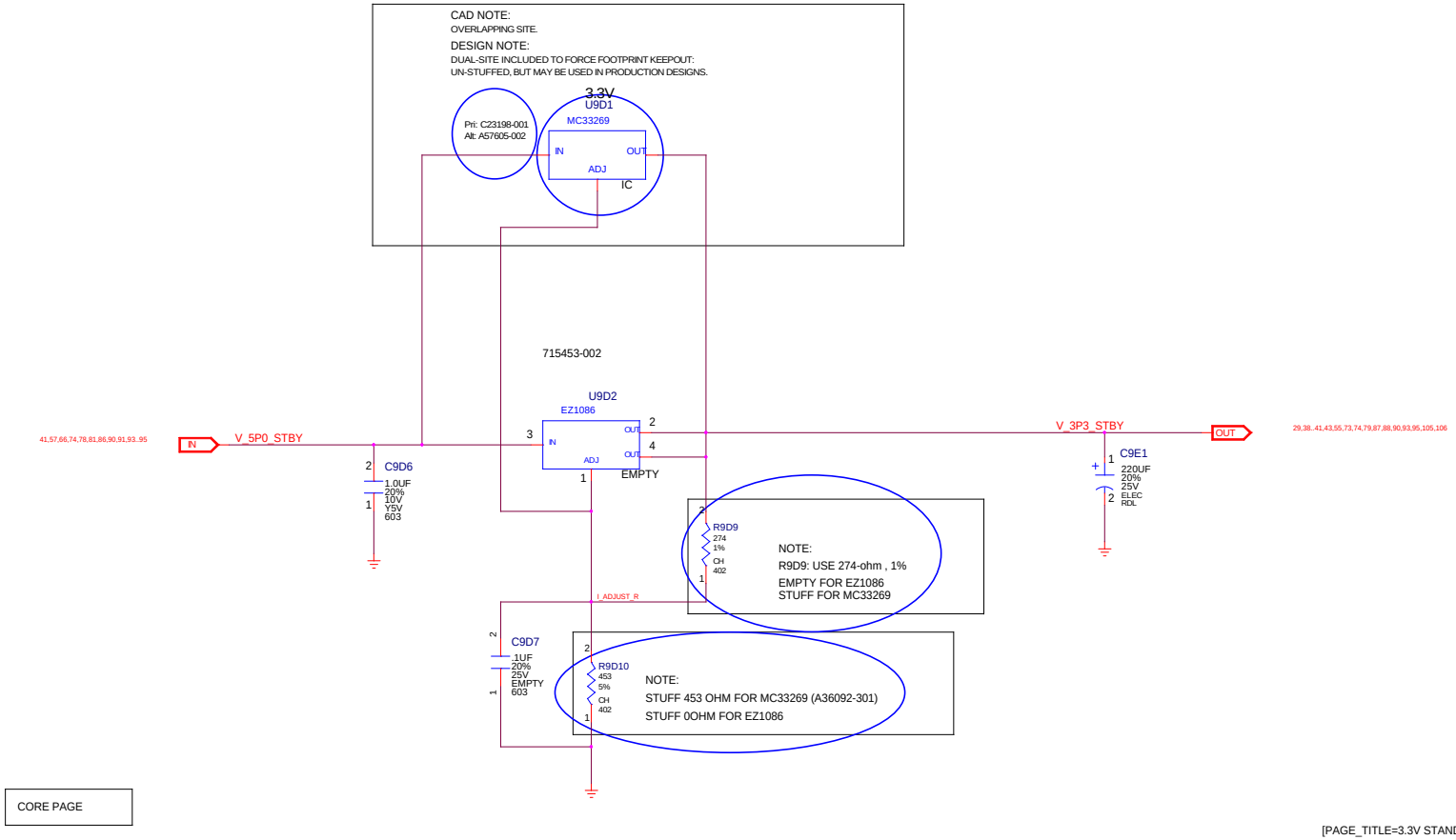


CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	90	4.0



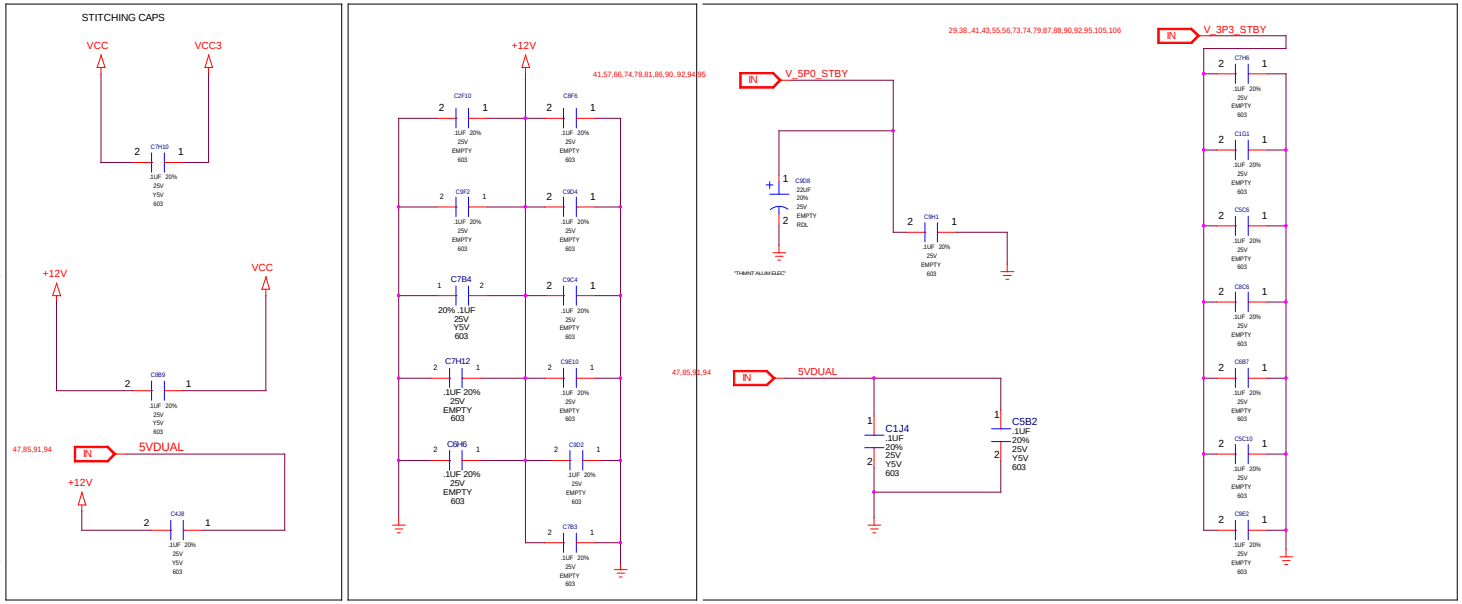
[PAGE_TITLE=USB_BP_RIGHT/LEFT & PS2]

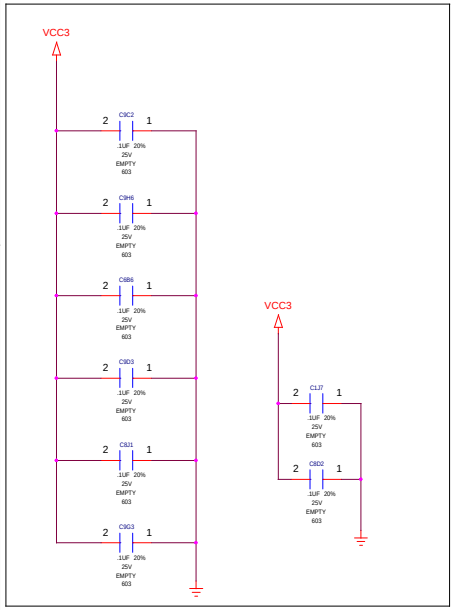


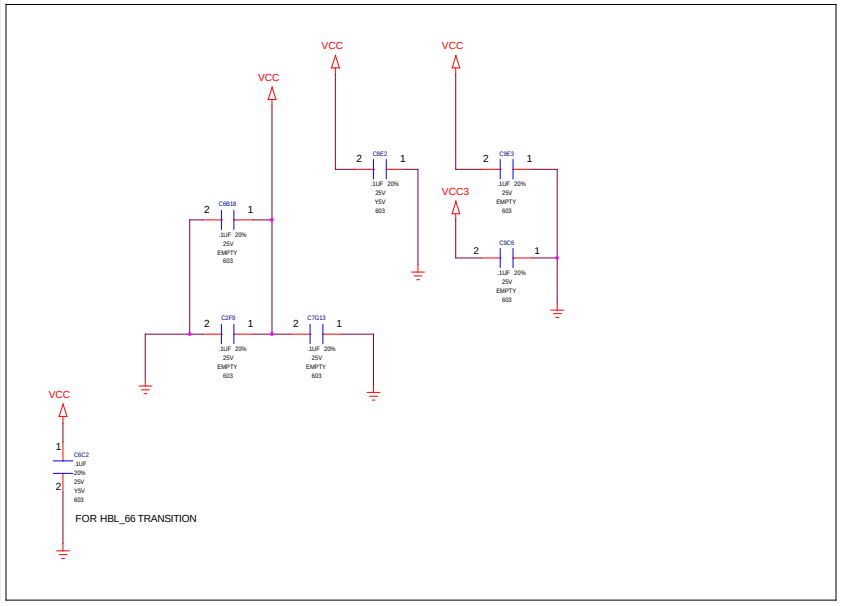
[PAGE_TITLE=3.3V STANDBY]

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	92	4.0

STITCHING CAPS



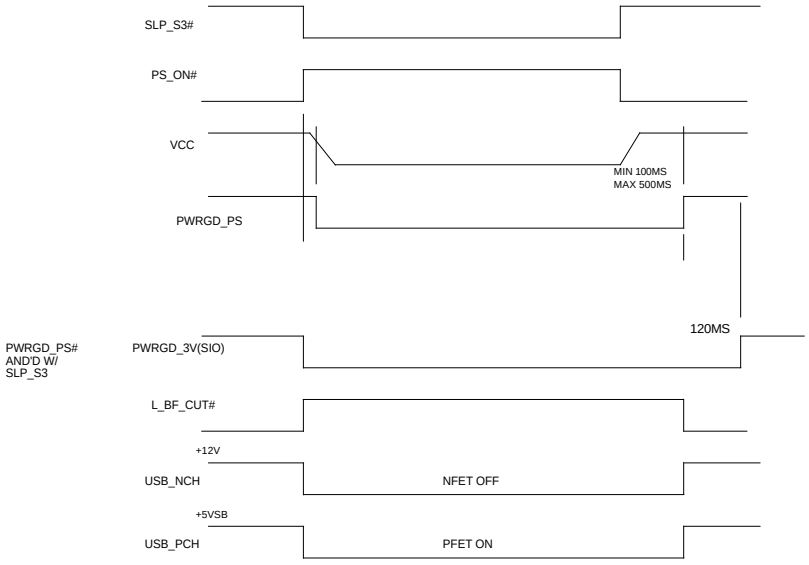


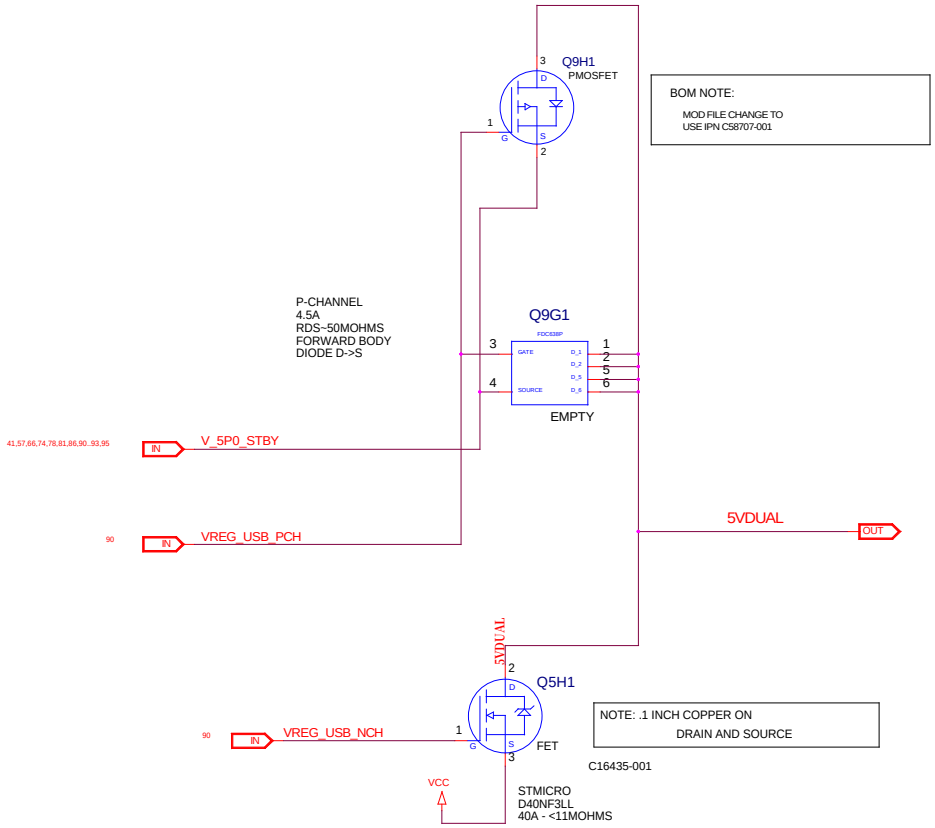


ROOM=DCPL_BULK
BOM=VREG_DCPL_BULK

[PAGE_TITLE=VREG_DCPL_BULK]

INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	93	4.0

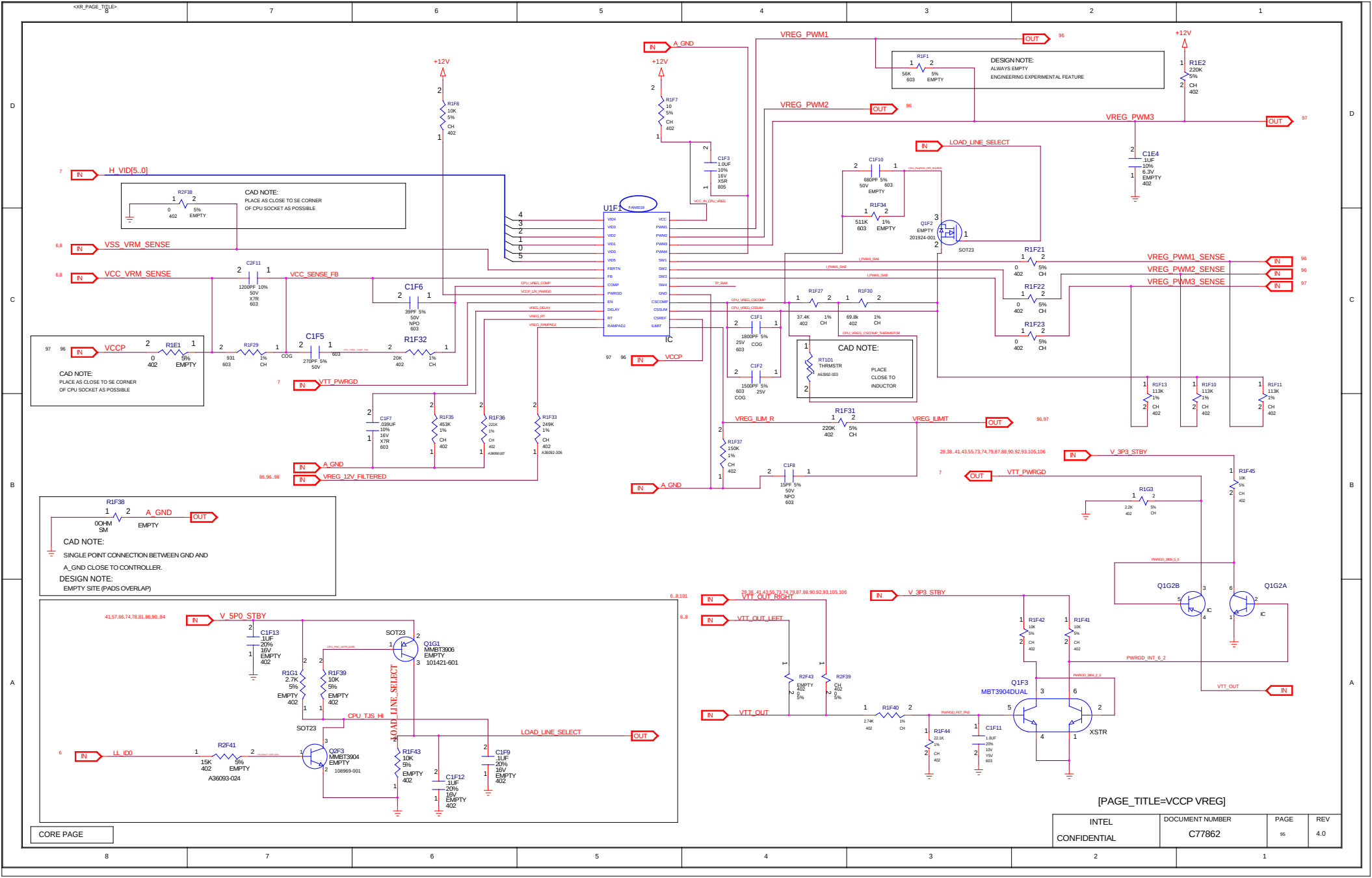




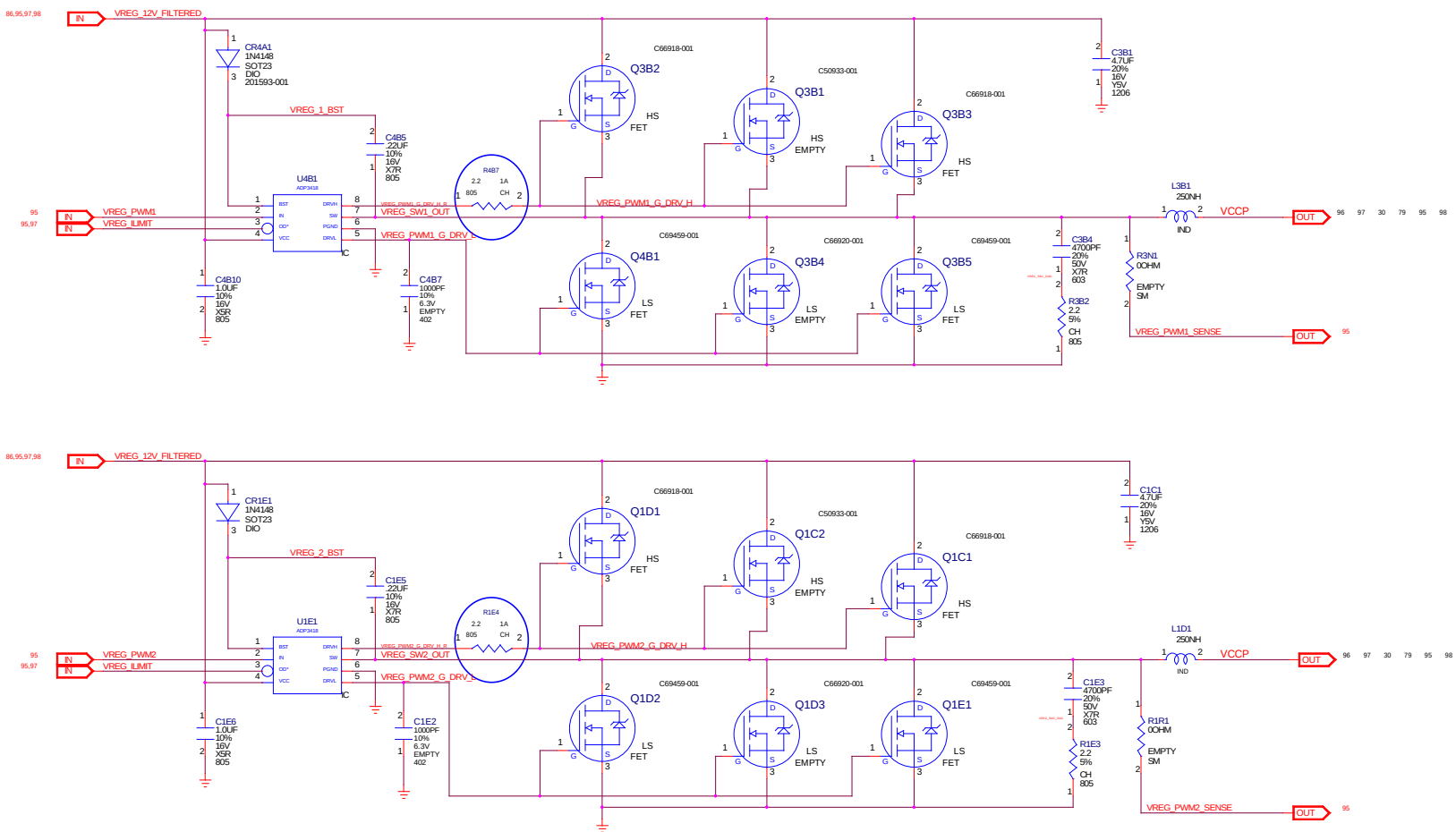
CORE PAGE

[PAGE_TITLE=5VDUAL/USB_BP_MID]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	94	4.0


H_VID[5..0]
VSS_VRM_SENSE
VCC_VRM_SENSE
VCCP
VTT_PWRGD
A_GND
VREG_12V_FILTERED
VREG_PWM1
VREG_PWM2
VREG_PWM3
LOAD_LINE_SELECT
VREG_PWM1_SENSE
VREG_PWM2_SENSE
VREG_PWM3_SENSE
VREG_ILIM_R
VREG_ILIMIT
V_3P3_STBY
V_5P0_STBY
VTT_OUT_RIGHT
VTT_OUT_LEFT
VTT_OUT
LL_ID0
CPU_TJS_HI
PWRGD_INT_6_2
U1F1
IC
CAD NOTE:
PLACE AS CLOSE TO SE CORNER
OF CPU SOCKET AS POSSIBLE
CAD NOTE:
PLACE CLOSE TO INDUCTOR
CAD NOTE:
SINGLE POINT CONNECTION BETWEEN GND AND
A_GND CLOSE TO CONTROLLER.
DESIGN NOTE:
EMPTY SITE (PADS OVERLAP)
DESIGN NOTE:
ALWAYS EMPTY
ENGINEERING EXPERIMENTAL FEATURE
Q1G1
MMBT3906
Q2F3
MMBT3904
Q1F3
MBT3904DUAL
Q1G2B
Q1G2A
XSTR
SOT23
[PAGE_TITLE=VCCP VREG]
CORE PAGE
INTEL
CONFIDENTIAL
DOCUMENT NUMBER
C77862
PAGE
95
REV
4.0

<XR_PAGE_TITLE>



CORE PAGE

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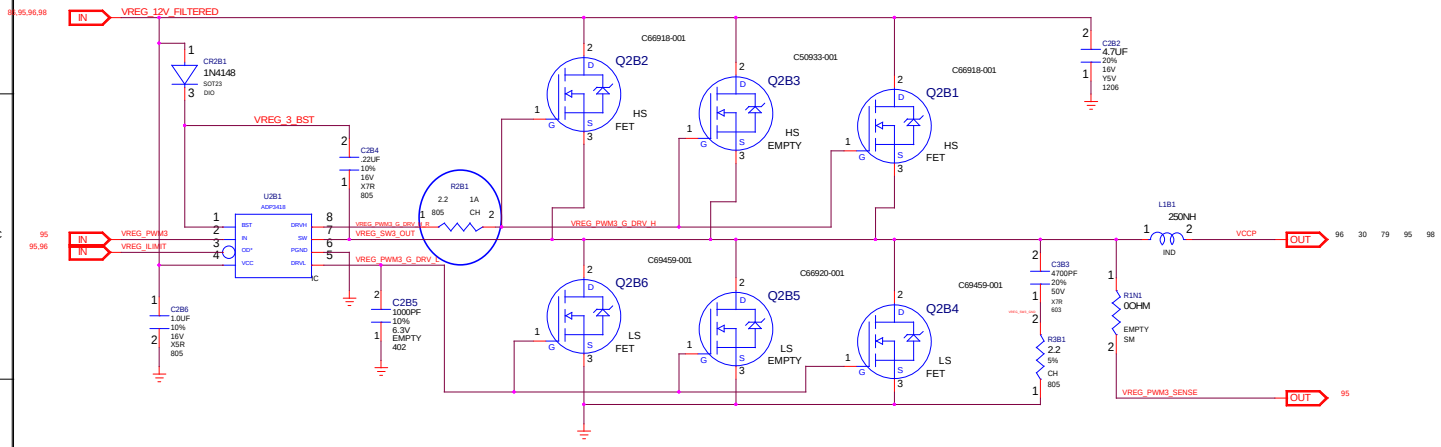

[PAGE_TITLE=VCCP VREG]

CORE PAGE

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CAD NOTE: PLACE AS MANY 1206 CAPACITORS AS POSSIBLE WITHIN CPU CAVITY

644066-024

97 96 IN VCCP

C3D4 C2D12 C2D1 C3D3 C3D6 C3D10 C3D5 C3D9 C3D1 C3D4
10.0UF 20% 6.3V XSR 1206

C2D3 C3D2 C2D11 C2D2 C2D7 C2D6 C2D5 C2D8
10UF 20% 6.3V XSR 1206

PLACEMENT NOTE FOR 1206:
PLACE 18 INSIDE CPU SOCKET (STUFF ALL)

CAD NOTE:
PLACE ON TOP (NORTH SIDE) OF SOCKET

C1D1 C1D2 C1E1 C3C3 C9C2 C3C1
560UF 20% 2.5V ALUM RDL
EMPTY

CAD NOTE:
PLACE ON EAST SIDE OF SOCKET

C1C2 C2C1 C2C3 C2C2
560UF 20% 2.5V ALUM RDL

86 IN VREG_12V_POWER

L4B1
1UH
EMPTY
A83634-001

C3B3 C1B2 C2B3 C1B1 C2B1
1200UF 20% 16V ALUM RDL
EMPTY

VREG_12V_FILTERED OUT 86,95..97

A46887-010

[PAGE_TITLE=VCCP VREG DECOUPLING]

CORE PAGE

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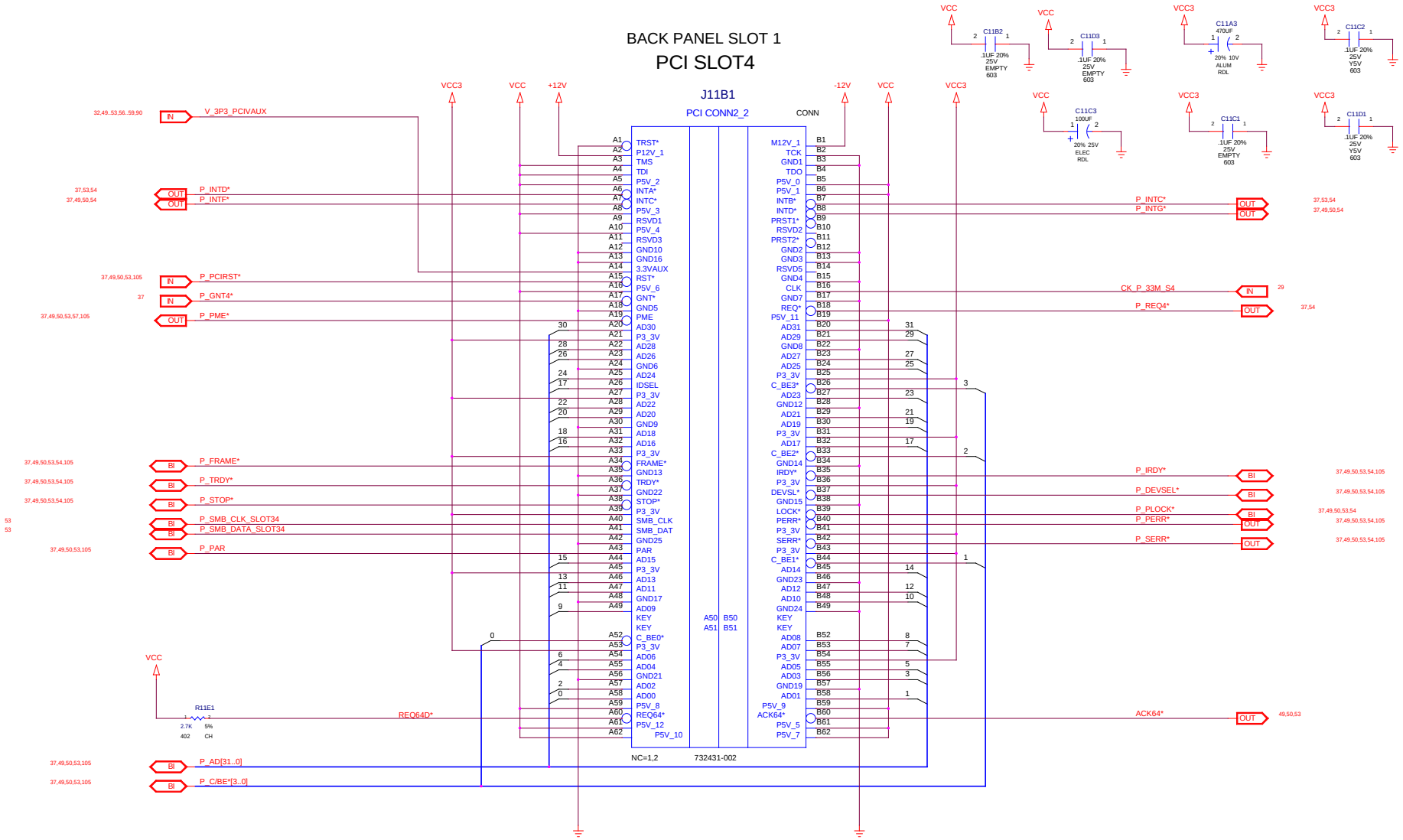
BACK PANEL SLOT 1
PCI SLOT4

J11B1
PCI CONN2_2
CONN



INTEL	DOCUMENT NUMBER	PAGE	REV
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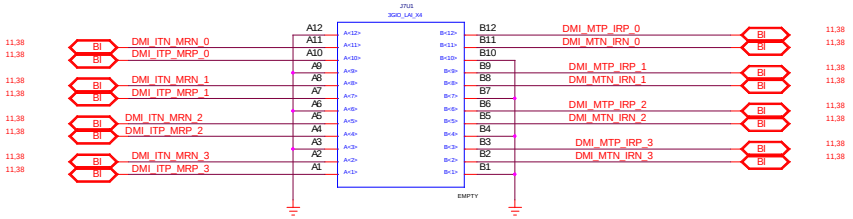
DMI LAI HEADER

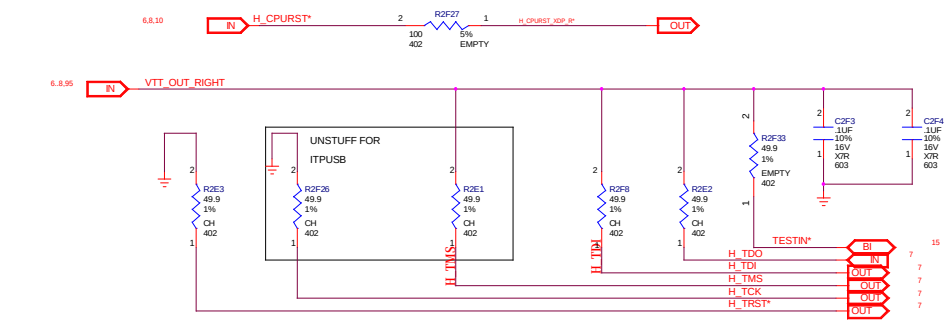


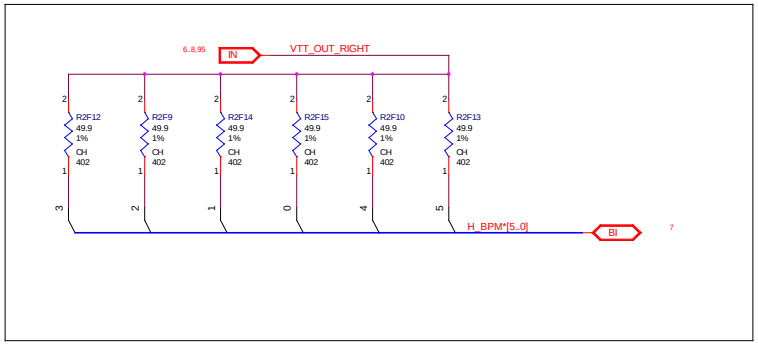
CORE PAGE

DMI = DIRECT MEDIA INTERFACE

[PAGE_TITLE=DMI LAI PORT]

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
	C77862	100	4.0



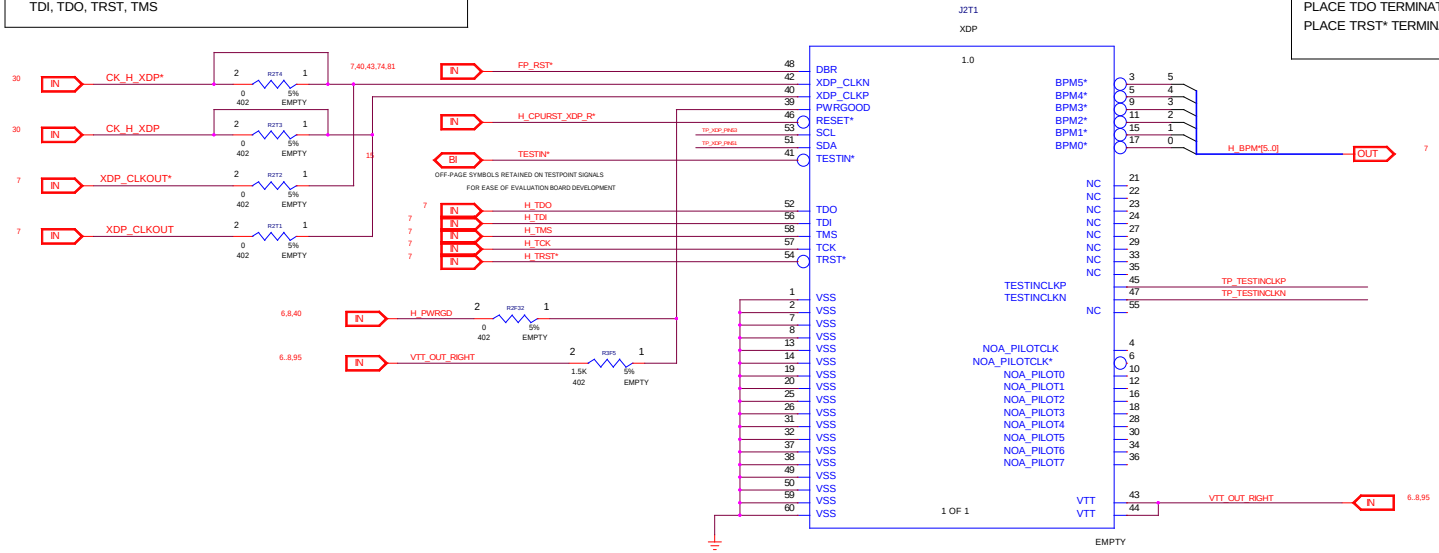


CAD NOTES:

XTG ROUTING RULES:
NOA MATCH LENGTHS WITHIN 50PS *
BPM MATCH LENGTHS WITHIN 50PS *
IDEALLY INCLUDE PACKAGE LENGTHS
NO LENGTH GUIDELINES FOR TCK,
TDI, TDO, TRST, TMS

CAD NOTES:

PLACE BPM TERMINATION NEAR CONNECTOR
PLACE TCK/TDI TERMINATION NEAR CPU
WITHIN 1.5" OF CPU, IDEALLY NEXT TO IT.
PLACE TDO TERMINATION NEAR CONNECTOR
PLACE TRST* TERMINATION ANYWHERE ON ROUTE



XDP

CORE PAGE

INTEL CONFIDENTIAL	DOCUMENT NUMBER	PAGE	REV
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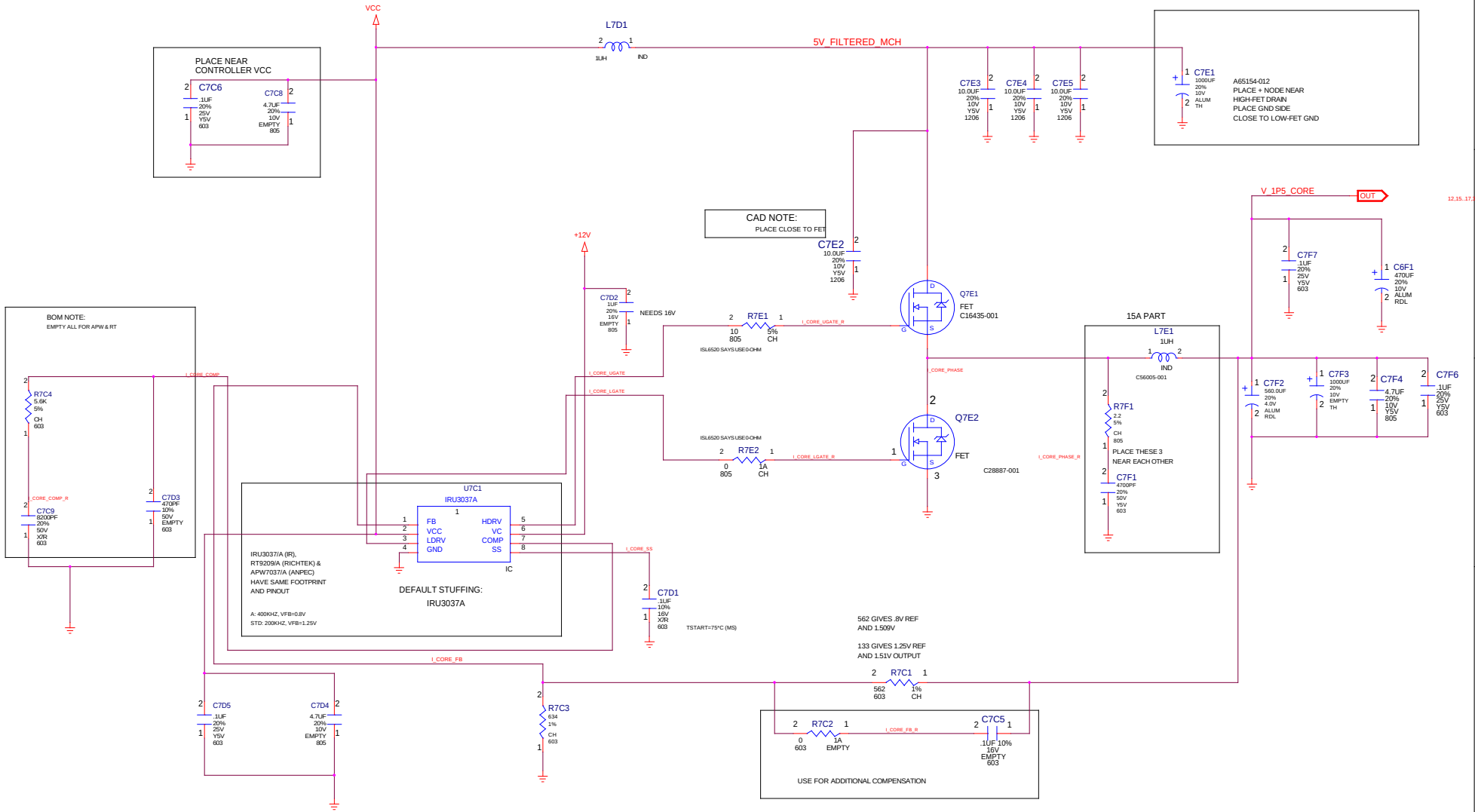
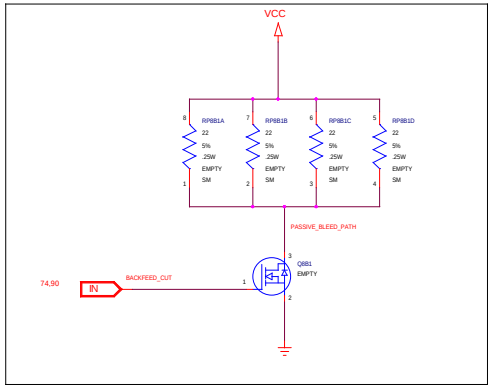
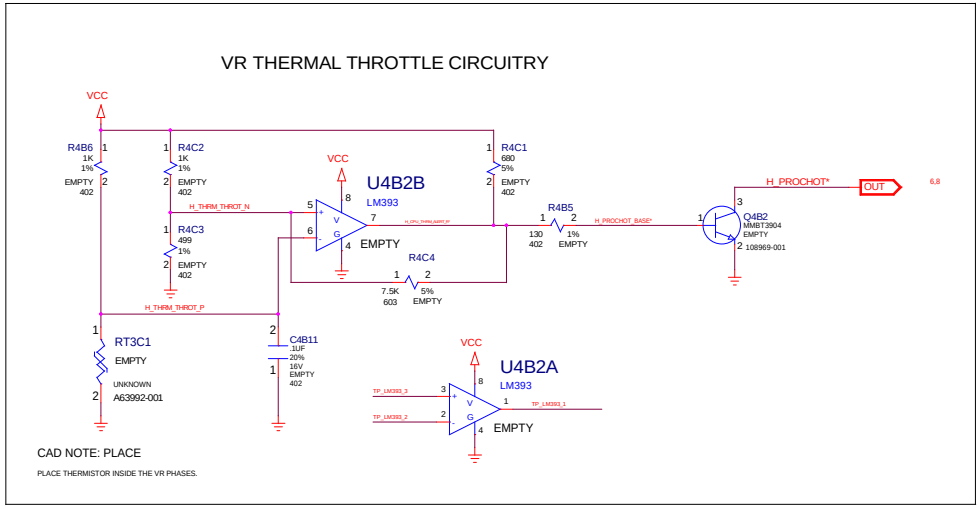


INTEL	DOCUMENT NUMBER	PAGE	REV
CONFIDENTIAL	C77862	102	4.0





CORE PAGE

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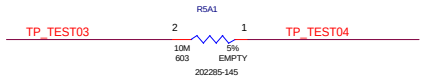
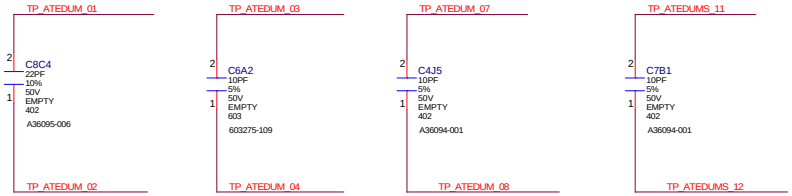
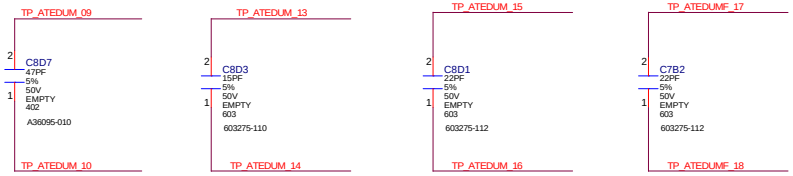
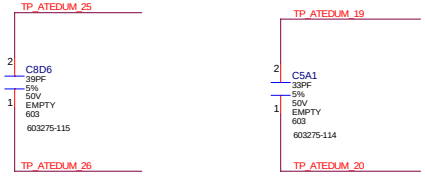
TEST SITE









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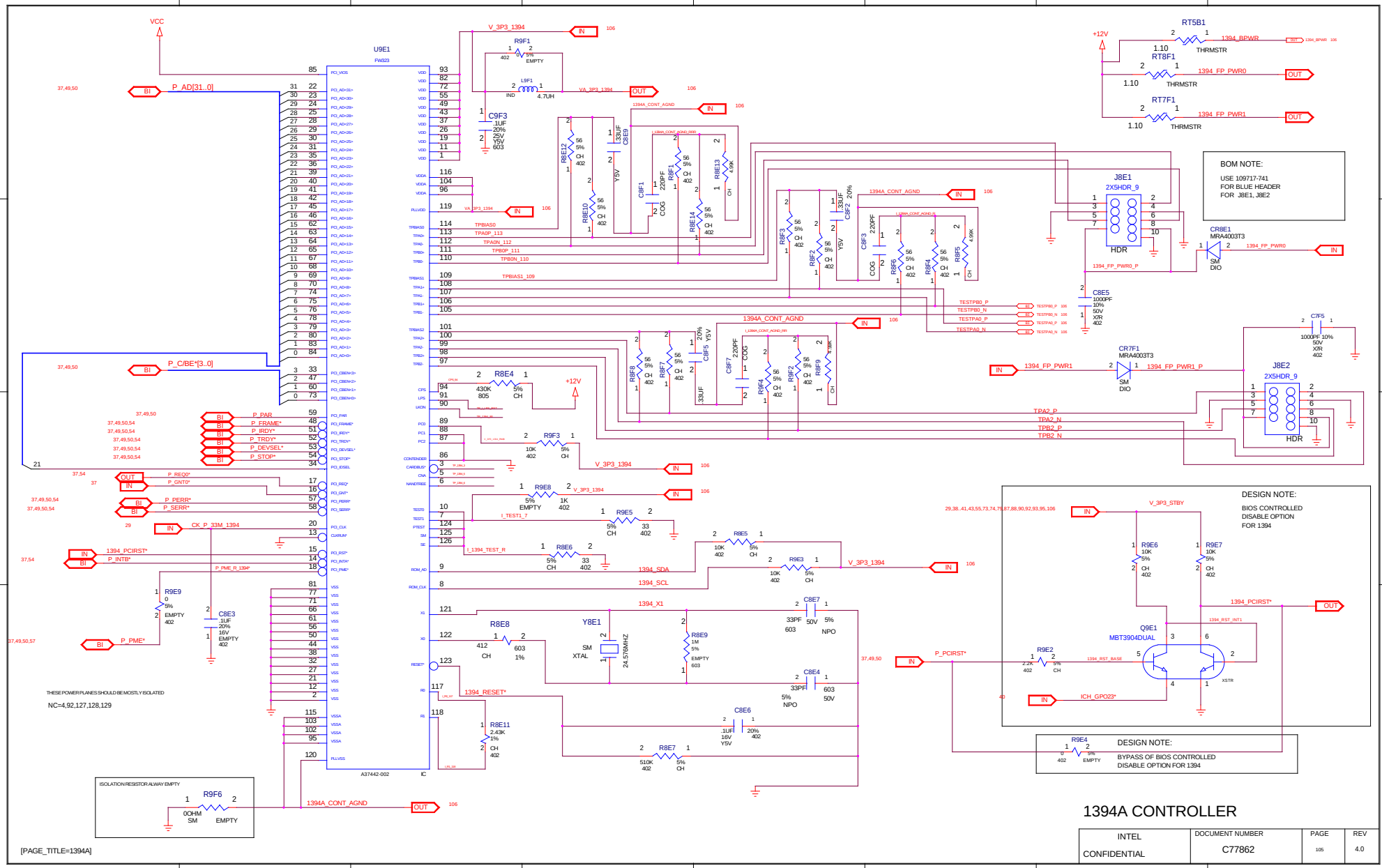
U9E1
FW823
A37442-002
IC
P_AD[31..0]
P_C/BE*[3..0]
P_PAR
P_FRAME*
P_IRDY*
P_TRDY*
P_DEVSEL*
P_STOP*
P_REQ0*
P_GNT0*
P_PERR*
P_SERR*
CK_P_33M_1394
1394_PCIRST*
P_INTB*
P_PME_R_1394*
P_PME*
V_3P3_1394
VA_3P3_1394
1394A_CONT_AGND
1394_SDA
1394_SCL
1394_X1
1394_RESET*
TPA0P_113
TPA0N_112
TPB0P_111
TPB0N_110
TPBIAS0
TPBIAS1_109
TESTPB0_P
TESTPB0_N
TESTPA0_P
TESTPA0_N
TPA2_P
TPA2_N
TPB2_P
TPB2_N
1394_FP_PWR0
1394_FP_PWR1
1394_BPWR
1394_FP_PWR0_P
1394_FP_PWR1_P
P_PCIRST*
ICH_GPO23*
1394_RST_INT1
1394_RST_BASE
THESE POWER PLANES SHOULD BE MOSTLY ISOLATED
NC=4,92,127,128,129
ISOLATION RESISTOR ALWAY EMPTY
R9F6
0OHM
SM
EMPTY
BOM NOTE:
USE 109717-741
FOR BLUE HEADER
FOR J8E1, J8E2
DESIGN NOTE:
BIOS CONTROLLED
DISABLE OPTION
FOR 1394
DESIGN NOTE:
BYPASS OF BIOS CONTROLLED
DISABLE OPTION FOR 1394
1394A CONTROLLER
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[PAGE_TITLE=1394A]

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Add these 1394 BP circuit

CAD NOTE:
OVERLAPPING FOOTPRINTS
DO NOT CHANGE TO 0402

R5A3 0 603 1A CH
L5B1 90OHM EMPTY IND 4PIN
R5A2 0 603 1A CH
DO NOT CHANGE TO 0402

TESTPA0_N
TESTPA0_P
TPA0M_1394
TPA0P_1394

CAD NOTE:
OVERLAPPING FOOTPRINTS
DO NOT CHANGE TO 0402

R5A4 0 603 1A CH
L5B2 90OHM EMPTY IND 4PIN
R5A5 0 603 1A CH
DO NOT CHANGE TO 0402

TESTPB0_N
TESTPB0_P
TPB0M_1394
TPB0P_1394

RIGHT
A74325-002

J5A1B
1394-2USB STACK
TPA0P_1394
TPA0M_1394
TPB0P_1394
TPB0M_1394
1394
CASE
CONN
1394_PWR
BT_GND
1394_BPWR_P
1394_BPWR
C5A3 1UF 20% 50V X7R 805
C5A2 1000PF 10% 50V X7R 402
C5A4 1000PF 10% 50V X7R 402
CR5A1 MRA4003T3 SW DIO

RIGHT
A74325-002

VREG_USB_BP_RIGHT
J5A1A
1394-2USB STACK
USB_BACK3_R*
USB_BACK3_R
USB_BACK4_R*
USB_BACK4_R
CONN

VCC
C9F6 .1UF 20% 16V EMPTY 402

VCC3
R9E1 0 603 1A CH
R9F5 0 603 1A EMPTY
V_3P3_STBY
V_3P3_1394

VA_3P3_1394
C8F4 .01UF 10% 25V X7R 402
C9F8 .01UF 10% 25V X7R 402
C8E8 .01UF 10% 25V X7R 402
C8E10 .01UF 10% 25V X7R 402
C9F9 100UF 20% 25V ELEC RDL
1394A_CONT_AGND

V_3P3_1394
C9E7 .01UF 10% 25V X7R 402
C9E9 .01UF 10% 25V X7R 402
C9F7 .01UF 10% 25V X7R 402
C9F5 .01UF 10% 25V X7R 402
C9F4 .01UF 10% 25V X7R 402
C9F1 .01UF 10% 25V X7R 402
C9E6 .01UF 10% 25V X7R 402
C9E12 .01UF 10% 25V X7R 402
C9E8 .01UF 10% 25V X7R 402
C9E11 .01UF 10% 25V X7R 402
C9E5 .01UF 10% 25V X7R 402
C9E4 100UF 20% 25V ELEC

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