Vegas Schematic

SKL/KBL-U

2016/06/27

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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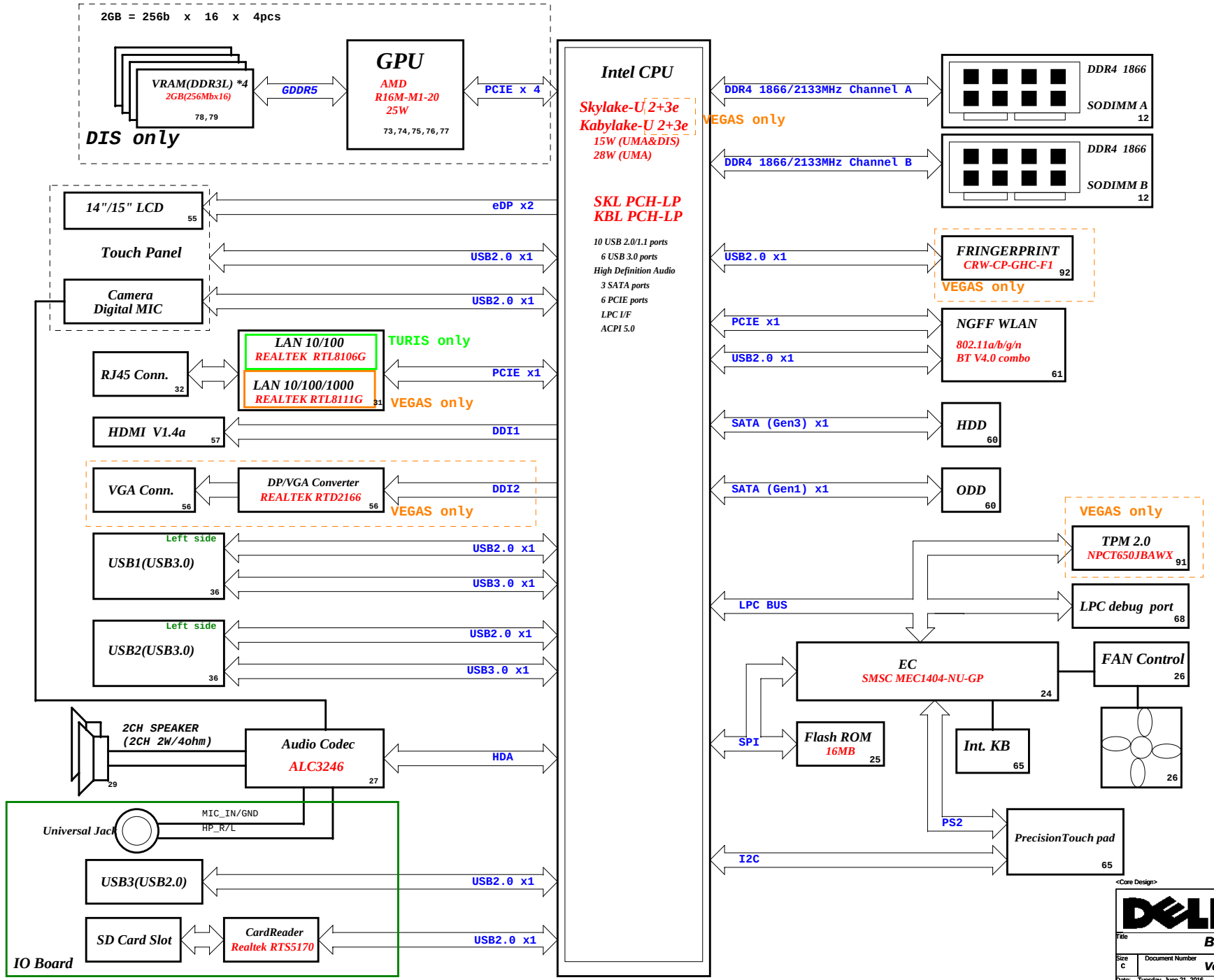
Title: ***Cover Page***

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 1 of 105

Project code:4PD09P010001
PCB P/N: 15341-SD
Revision: A00

Vegas SKL-U/KBL-U Block Diagram



CHARGER — ISL88739 — 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC — TPS51225RUKR-GP — 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power — NCP81208MNTXG — 46~50
NCP81382MNTXG x 2
NCP81382MNTXG (23e)
NCP81253MNTBG

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS — RT8231AGQW-GP / APL5930KAI-TRG — 51

INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1V — 11

INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A — AOZ2262QI-10-GP-U — 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V — APL5930KAI-TRG — 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 — TPS22966DPUR-GP — 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e) — TPS22961DNYT — 40

INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA — AO3419L — 86

INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

VGA_CORE — ISL62771HRTZ-GP-U — 85

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

1D5V_VGA_S0 — Y8288RAC-GP — 86

INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

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Title: Block Diagram
Size: C | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Tuesday, June 21, 2016 | Sheet 2 of 105

(Blanking)

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 3 of 105

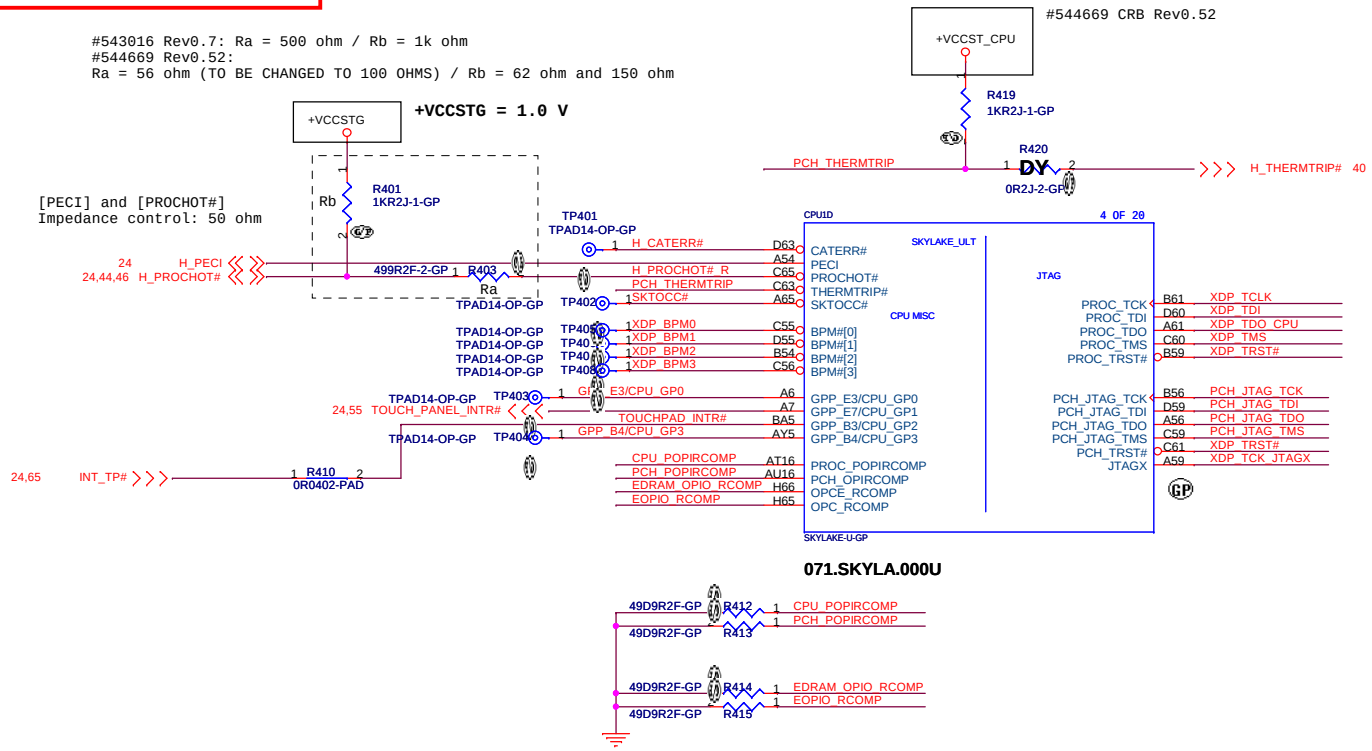
Main Func = CPU

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm

#544669 CRB Rev0.52

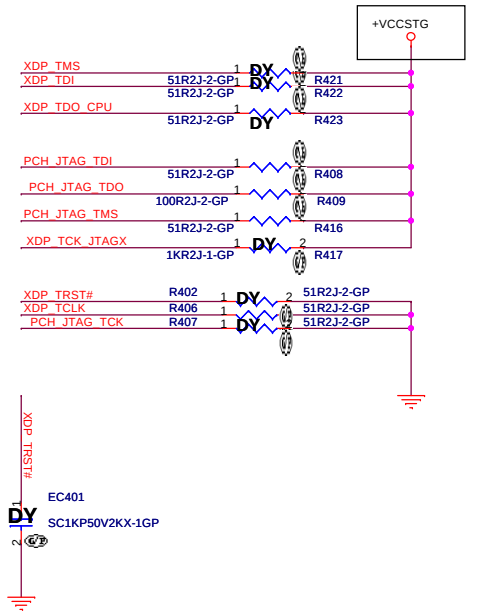
+VCCSTG = 1.0 V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm



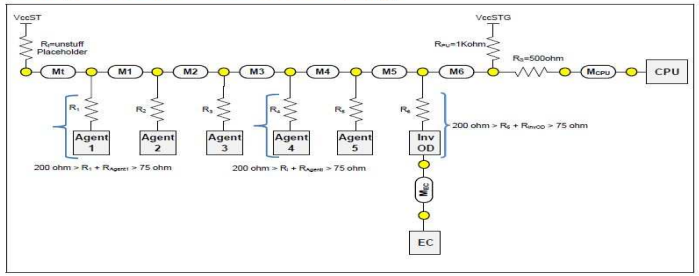
071.SKYLA.000U

+VCCSTG = 1.0 V



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

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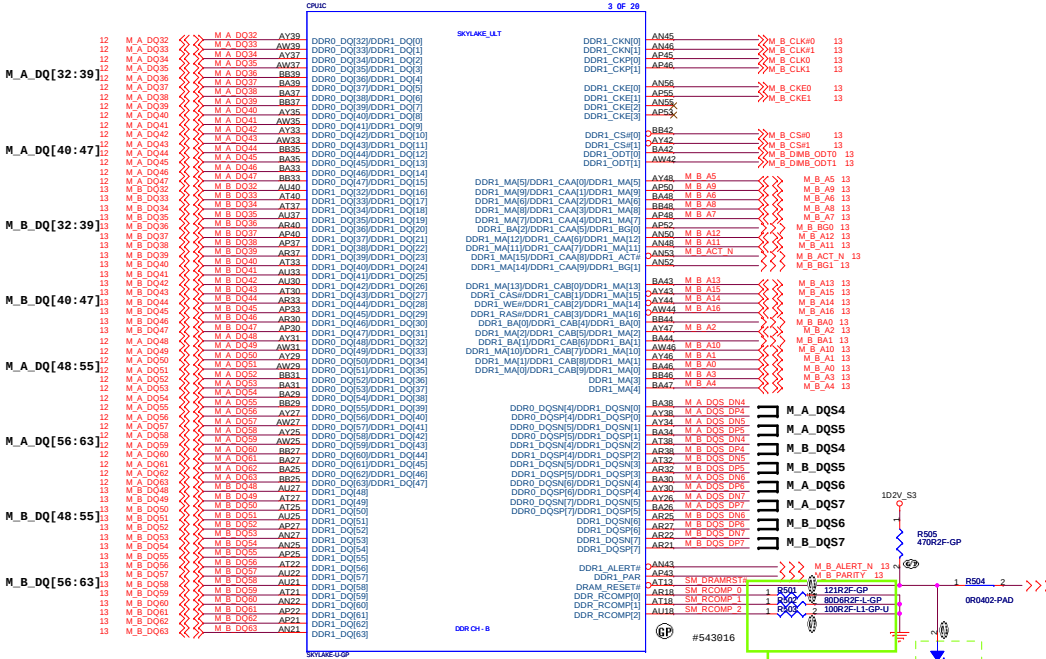
Title	CPU_(JTAG/CPU SIDE BAND)	
Size A3	Document Number: Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 4 of 105	

Main Func = CPU

DDR4 ball type: Interleaved Type

071.SKYLA.000U



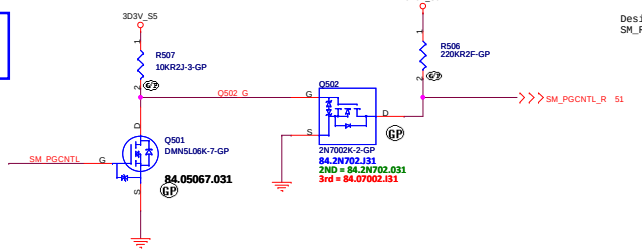
071.SKYLA.000U

#543016

Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.



PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT.	3,4
		DRAMs	ODT[1:0]	Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z).
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

<Core Design>

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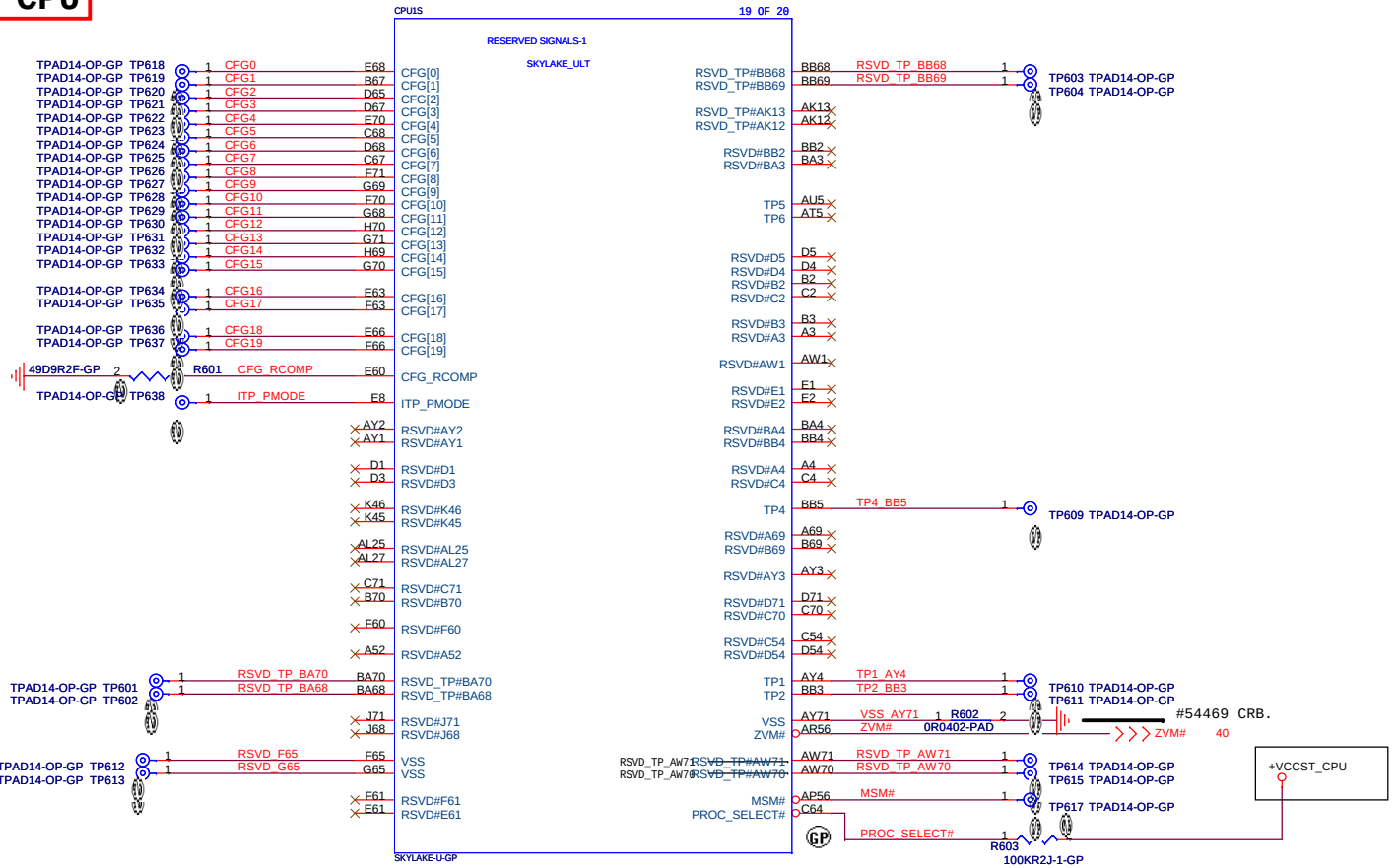
Title: CPU (DDR)

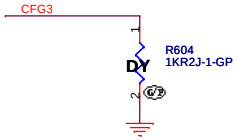
Size	Document Number	Rev
A2	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 5 of 105

Main Func = CPU

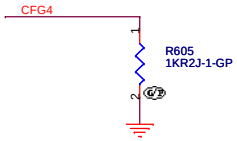


PCH strap pin: **071.SKYLA.000U**



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

(#543016)



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

#544669 Rev0.52 (CRB)

20140807 david

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

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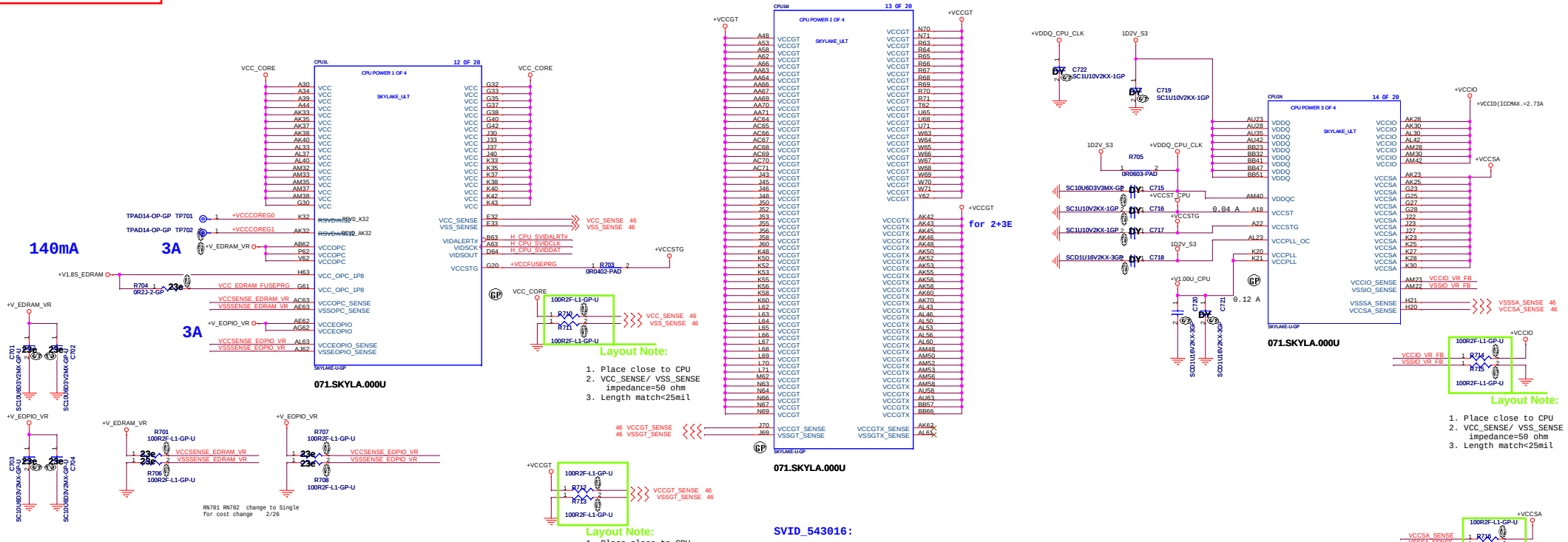
Title: CPU (RESERVED)

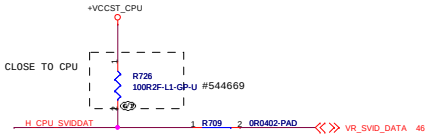
Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 6 of 105

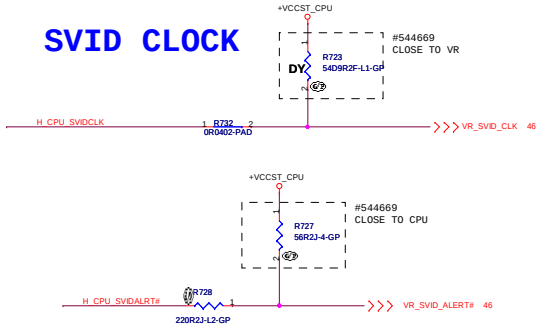
Main Func = CPU



SVID DATA



SVID CLOCK

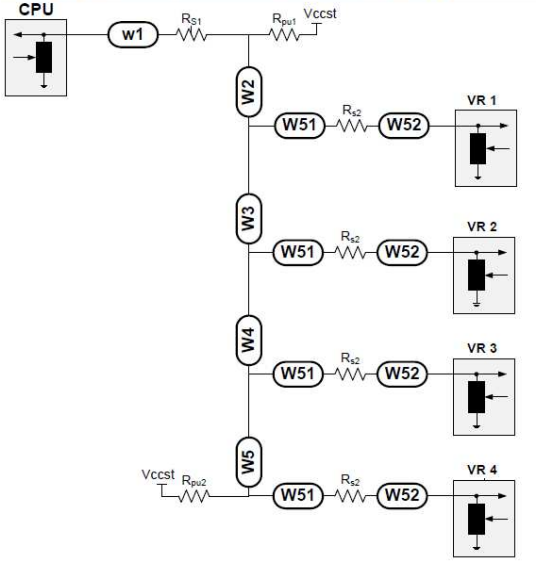


SVID_543016:

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{GT} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Figure 10-7. Routing Illustration for SVID Topology



<Core Design>
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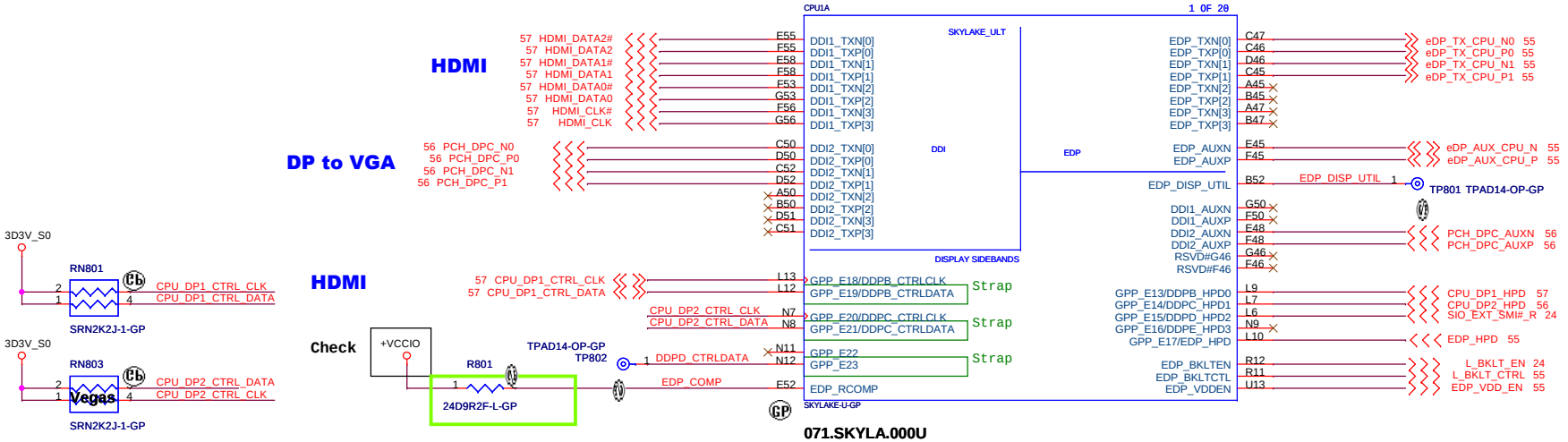
Title: CPU(VCC_CORE)

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 7 of 105

Main Func = CPU

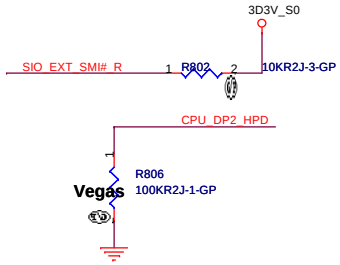


071.SKYLA.000U

(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils



(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title: CPU (DISPLAY)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 8 of 105

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

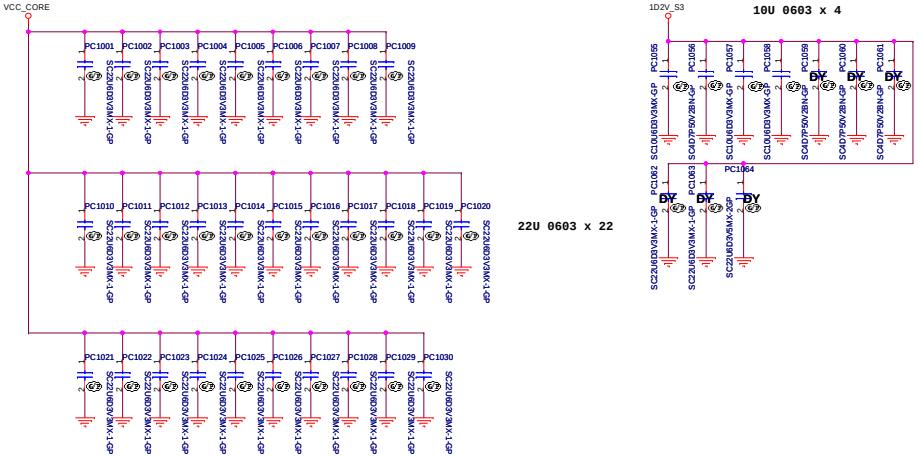
Date: Thursday, June 16, 2016 Sheet 9 of 105

Main Func = CPU

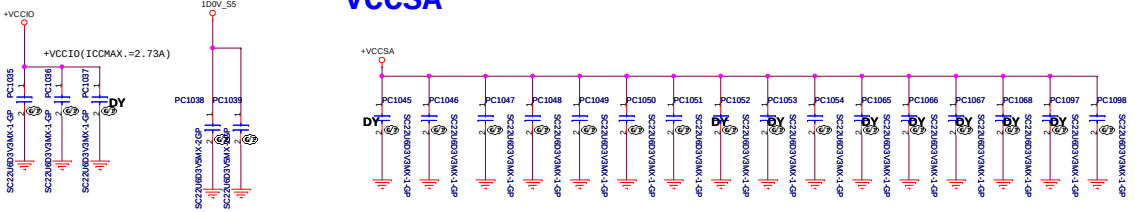
(#543016 PDG)

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A



VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

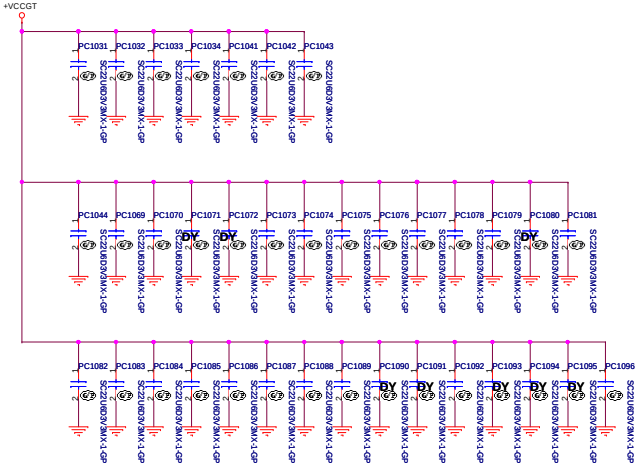


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

<Core Design>

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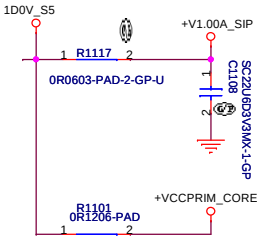
Title: CPU (Power CAP1)

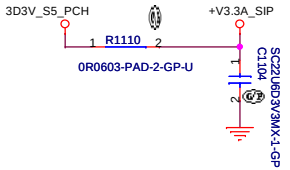
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

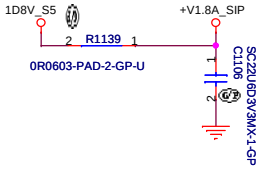
Date: Thursday, June 16, 2016 | Sheet 10 of 105

Main Func = CPU

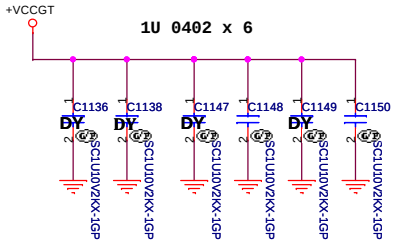
PCH DERIVED RAILS



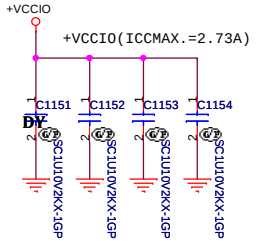


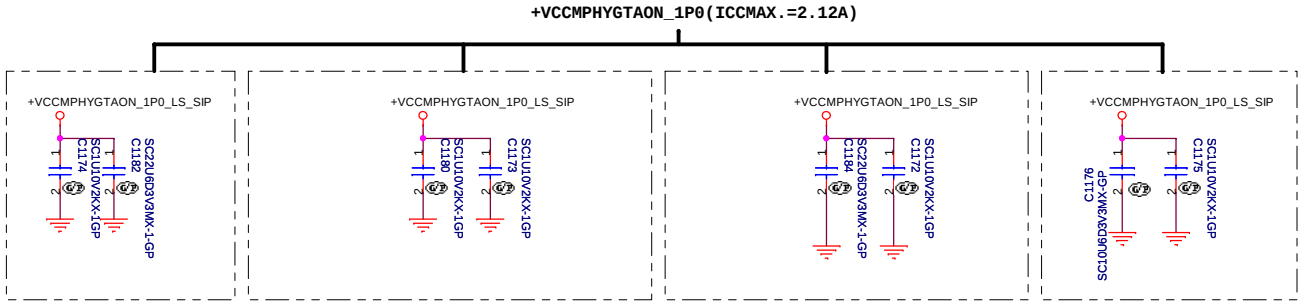


UNSLICED GT



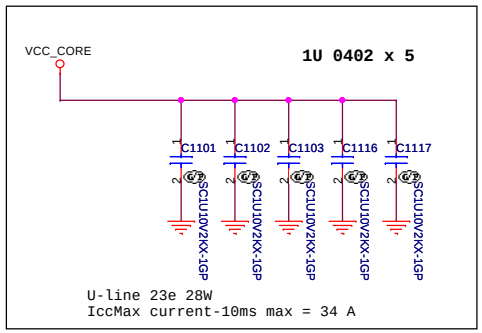
VCCIO

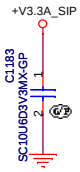


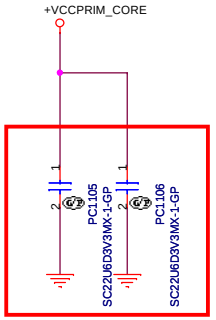


Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15





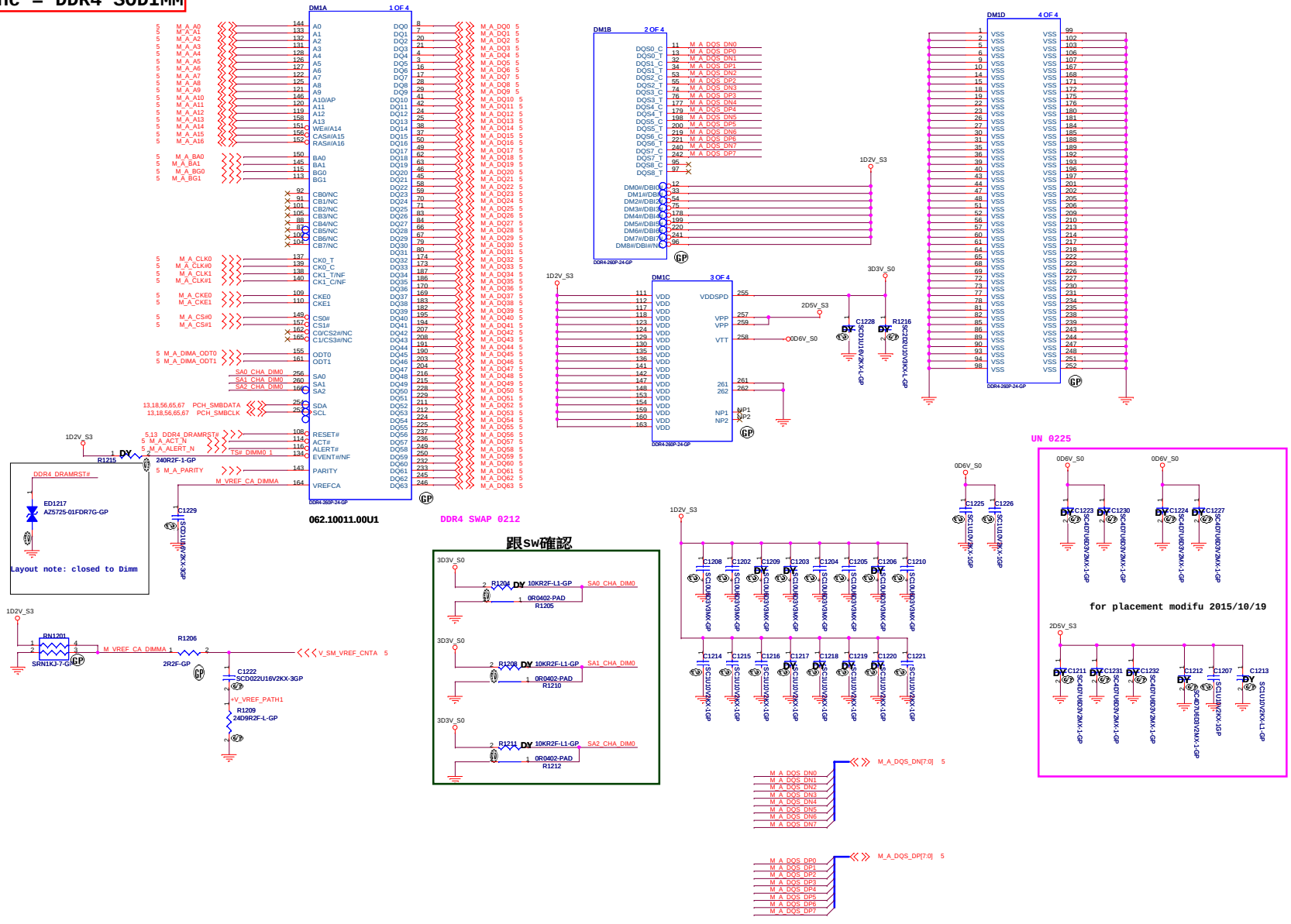


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (Power CAP2)	
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Friday, June 24, 2016	Sheet 11 of 105	

Main Func = DDR4 SODIMM



<Core Design>

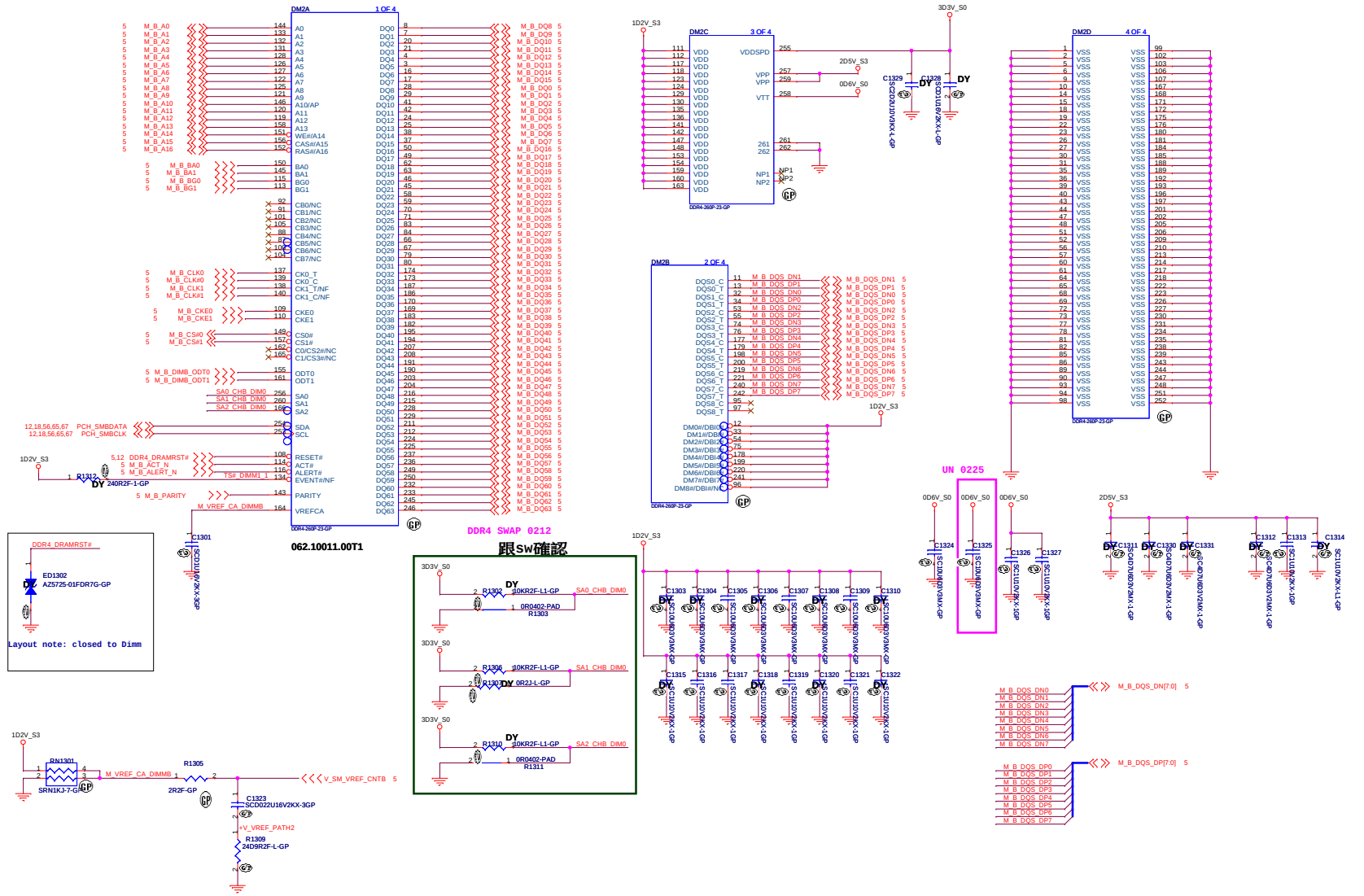
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 12 of 106

Main Func = DDR4 SODIMM



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 13 of 106

(Blanking)

<Core Design>

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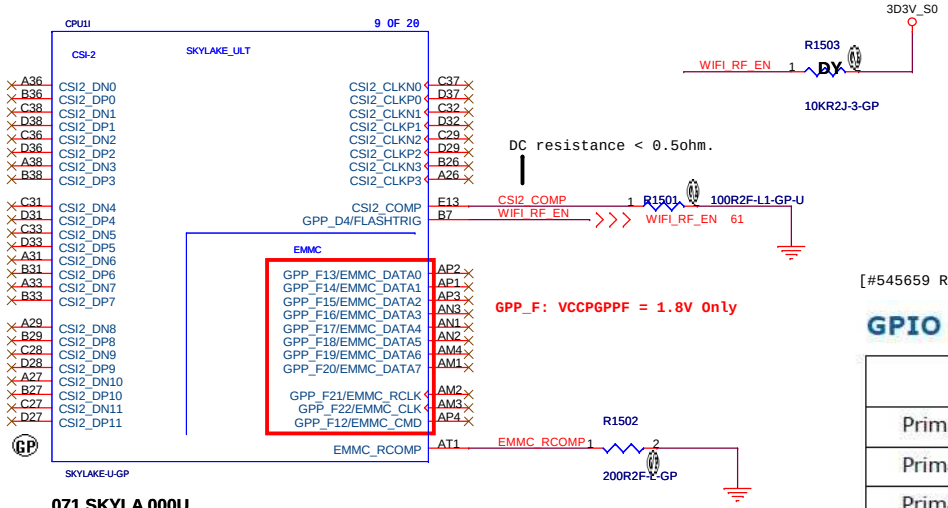
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 14 of 105

Main Func = PCH



071.SKYLA.000U

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

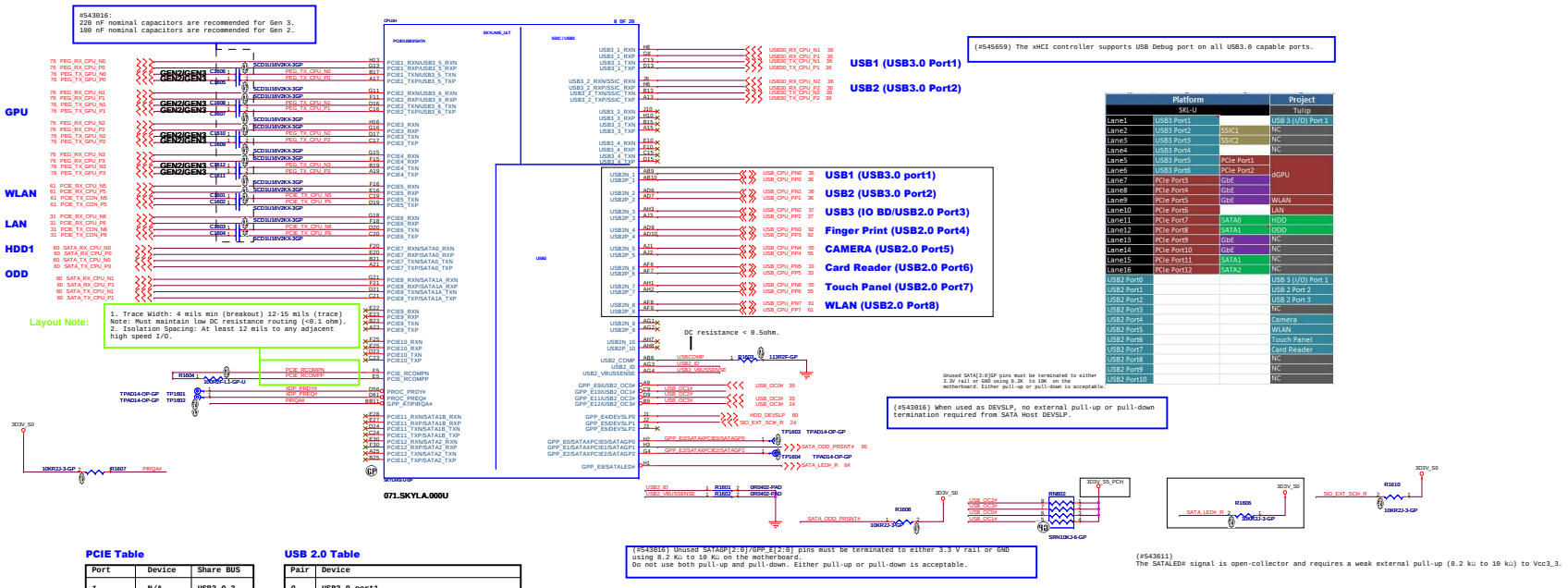
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CS-2/EMMC)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 15 of 105

Main Func = PCH



(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

Platform SKL-U		Project Tulip
Lane1	USB3 Port1	USB 3 (I/O) Port 1
Lane2	USB3 Port2	NC
Lane3	USB3 Port3	NC
Lane4	USB3 Port4	NC
Lane5	USB3 Port5	PCIe Port1
Lane6	USB3 Port6	PCIe Port2
Lane7	PCIe Port3	GbE
Lane8	PCIe Port4	GbE
Lane9	PCIe Port5	GbE
Lane10	PCIe Port6	LAN
Lane11	PCIe Port7	SATA0
Lane12	PCIe Port8	SATA1
Lane13	PCIe Port9	GbE
Lane14	PCIe Port10	GbE
Lane15	PCIe Port11	SATA1
Lane16	PCIe Port12	SATA2
USB2 Port0		USB 3 (I/O) Port 1
USB2 Port1		USB 2 Port 2
USB2 Port2		USB 2 Port 3
USB2 Port3		NC
USB2 Port4		Camera
USB2 Port5		WLAN
USB2 Port6		Touch Panel
USB2 Port7		Card Reader
USB2 Port8		NC
USB2 Port9		NC
USB2 Port10		NC

Unused SATA[3:0]GP pins must be terminated to either 3.3V rail or GND using 8.2k to 10K on the motherboard. Either pull-up or pull-down is acceptable.

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5(L0~L3)	GPU	
6(L3)	HDD	SATA0
6(L2)	ODD	SATA1
6(L0~L1)	N/A	

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3 (IOBD)
3	Finger Print
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

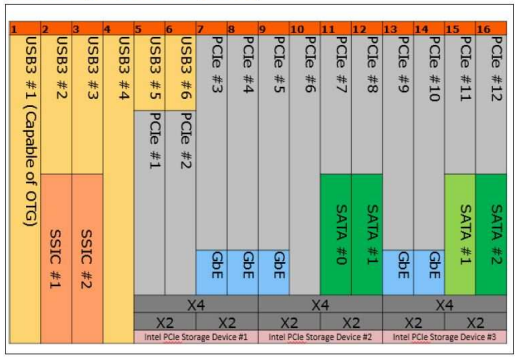


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size	Document Number	Rev
A1	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 16 of 105

Main Func = PCH

3D3V_S5 — RN1704 — AC_PRESENT, PCH_WAKE#, PCH_BATLOW#, GPD11/LANPHYPC — SRN10KJ-6-GP

GPD11 pull high by Intel PDG1.3 request

BATLOW#:
Pull-up required even if not implemented.

3D3V_S5 — R1711 0R0603-PAD — +VCCPDSW_3P3

Layout note: 3 PAD SHARING

RTC_AUX_S5 — #544669 (CRB): 330k. — R1730 330KR2J-L1-GP — SM_INTRUDER#

3D3V_S5_PCH — R1731 20KR2J-L2-GP — EXT_PWR_GATE# — R1718 10KR2J-3-GP — ME_SUS_PWR_ACK_R

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

H_CPUPWRGD — R405 10KR2J-3-GP

RN1701 — PM_RSMRST#, PM_PCH_PWROK — SRN10KJ-5-GP — R1717 10KR2J-3-GP — SYS_PWROK

+VCCMPHYGTAON_1P0

SKL: 1.0V
+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)

1D0V_S5 — R1724 0R0805-PAD — +VCCMPHYGTAON_1P0_LS_SIP — R1735 0R0805-PAD — C1704 SC10U6D3V3MX-GP

24,31,40,55,61,68,76,91 PLT_RST# — R1713 0R0402-PAD — PCH_PLTRST#

R1715 100KR2J-1-GP — C1701 SC220P50V2KX-3GP

+V3.3A_SIP — R1701 10KR2J-3-GP

CPU1K — 11 OF 20 — SYSTEM POWER MANAGEMENT — SKYLAKE_ULT

TPAD14-OP-GP TP1710 — PCH_PLTRST# — XDP_DBRESET# — PM_RSMRST#

40 H_THERMTRIP_EN — 0R2J-2-GP R1734 — H_VCCST_PWRGD_R — 60D4R2F-GP R1733 — H_CPUPWRGD, H_VCCST_PWRGD

24 SYS_PWROK, 24,26,40 RESET_OUT# — R1706 0R0402-PAD — PM_PCH_PWROK — R1704 0R2J-2-GP — PM_RSMRST# — PCH_DPWROK

ME_SUS_PWR_ACK_R — SUSACK# R — PCH_WAKE# — GPD2/LAN_WAKE# — GPD11/LANPHYPC

DY for OBFF disable

+VCCPDSW_3P3 — R1707 10KR2J-3-GP

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

GPP_B13/PLTRST#, SYS_RESET#, RSMRST#
PROCPWRGD, VCCST_PWRGD
SYS_PWROK, PCH_PWROK, DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK, GPP_A15/SUSACK#
WAKE#, GPD2/LAN_WAKE#, GPD11/LANPHYPC, GPD7/RSVD#AT15

GPP_B12/SLP_S0#, GPD4/SLP_S3#, GPD5/SLP_S4#, GPD10/SLP_S5#, SLP_SUS#, SLP_LAN#, GPD9/SLP_WLAN#, GPD6/SLP_A#
GPD3/PWRBTN#, GPD1/ACPRESENT, GPD0/BATLOW#
GPP_A11/PME#, INTRUDER#
GPP_B11/EXT_PWR_GATE#, GPP_B2/VRALERT#

SIO_SLP_S0# — TP17701 — SIO_SLP_S3# 24,27,40,51 — SIO_SLP_S4# 24,40,44,51
SIO_SLP_S5#
SLP_SUS# — TP17703
SLP_LAN# — TP17704
GPD9/SLP_WLAN# — TP17705
SIO_SLP_A# — TP17706
SIO_PWRBTN# 24
AC_PRESENT
PCH_BATLOW#
PME# — SM_INTRUDER# — TP17707 TPAD14-OP-GP
EXT_PWR_GATE#

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

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24 EC_WAKE# — R1710 0R0402-PAD — GPD2/LAN_WAKE#

AC_PRESENT — EC1707 SCD1U16V2KX-3GP

3D3V_S5 — U1702 U74LVC1G07G-AL5-R-GP — 73.01G07.AHG — C1703 SCD1U16V2KX-3GP

24,27,40,51 SIO_SLP_S3#

3D3V_S5, +VCCSTG — C1702 SCD1U16V2KX-3GP — R1722 100KR2J-1-GP

U1701 U74LVC1G07G-AL5-R-GP — 73.01G07.AHG

24,40 ALL_SYS_PWRGD

H_VCCST_PWRGD_R

EC1708 SCD01U50V2KX-1GP

R1716 100KR2F-L1-GP — R1719 47KR2F-GP — EC1709 SCD1U16V2KX-3GP

D1702 RB751V-40H-GP — 83.R2004.G8F — ACOK_IN 24,44

3D3V_AUX_S5 — R1737 100KR2J-1-GP — PM_RSMRST# M — Q1702 2N7002KDW-GP — NON DS3

AC_PRESENT
PM_RSMRST#

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

XDP_DBRESET#
SYS_PWROK
PLT_RST#
RESET_OUT#
3V_5V_POK

EC1706 SC10P50V2KX-1GP — EC1702 SC10P50V2KX-1GP — EC1703 SC10P50V2KX-1GP — EU1101 AZ5325-01FDF7G-GP — EC1705 SC10P50V2KX-1GP — EC1704 SC10U6D3V3MX-GP

ME_SUS_PWR_ACK_R — R1708 0R0402-PAD — SUSACK# R

24 ME_SUS_PWR_ACK — R1709 0R0402-PAD — ME_SUS_PWR_ACK_R

3D3V_AUX_S5 — R1727 100KR2J-1-GP — NON DS3 — R1726 10KR2J-3-GP — Q1701 2N7002KDW-GP

3V_5V_POK# — PM_RSMRST# — R1702 1KR2J-1-GP — 3V_5V_POK_C — R1728 0R0402-PAD — 3V_5V_POK 40,45,53,54 — PCH_RSMRST# 24

EC1712 SCD1U16V2KX-3GP

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Monday, June 27, 2016 | Sheet 17 of 105

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

R1835 and R1834 merge to RN1802
Follow Starlord

RCIN#:
Frequency to Avoid: 33 MHz

SERIRQ PH:
PDG: 8.2k
CRB: 10k

GPU
WLAN
LAN

071.SKYLA.000U

20140820 DAIVD

Layout: Place at the open door area.

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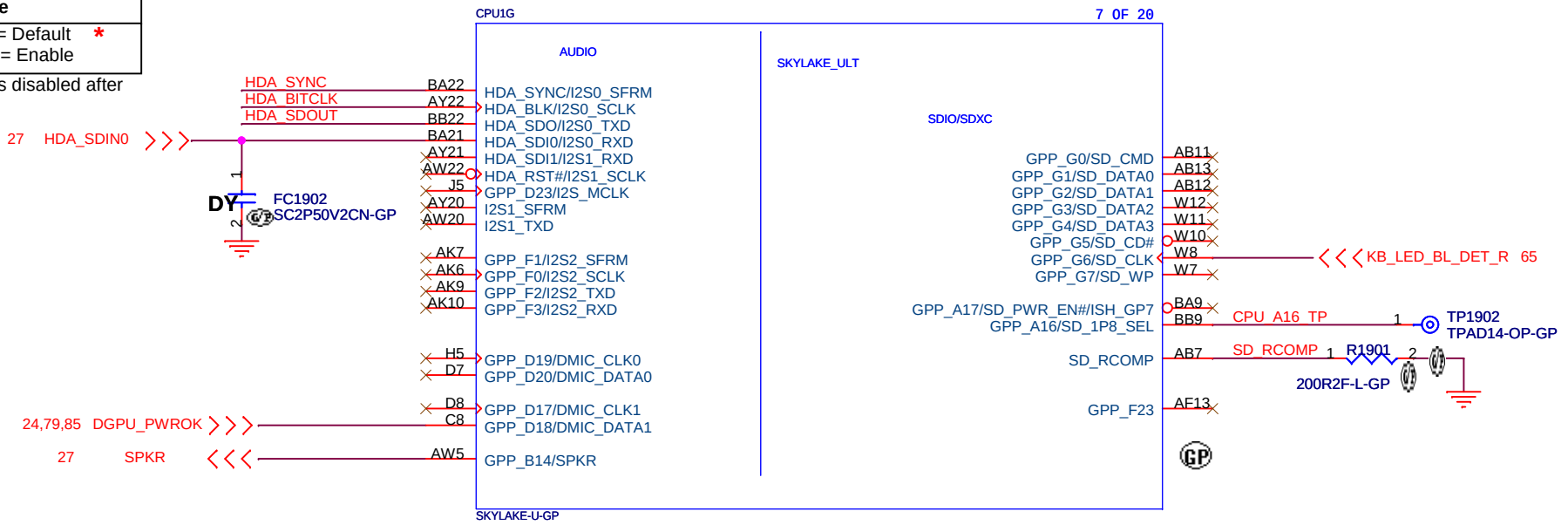
Title: CPU_(LPC/SPI/SMBUS/CL/CLK)
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Monday, June 27, 2016 | Sheet 18 of 105

Main Func = PCH

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

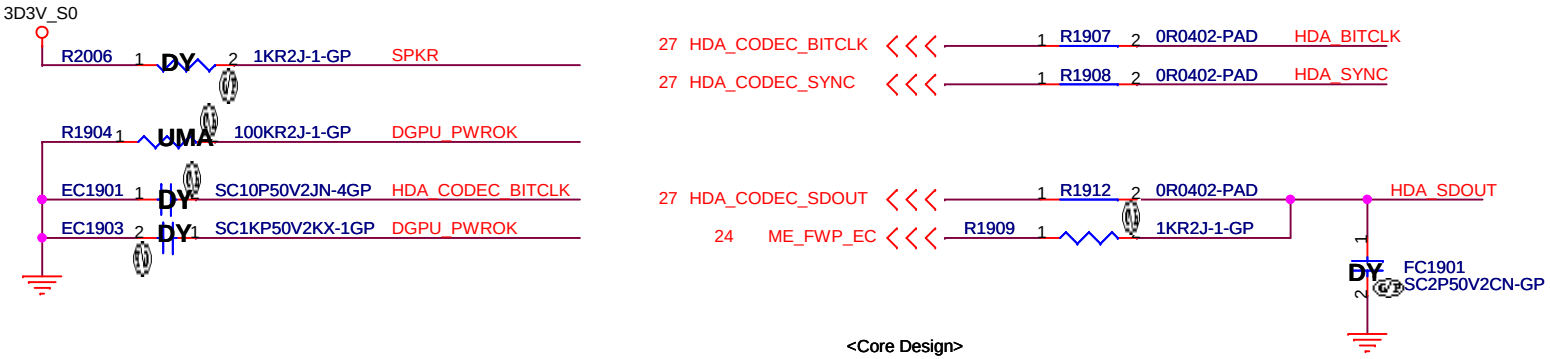


071.SKYLA.000U

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

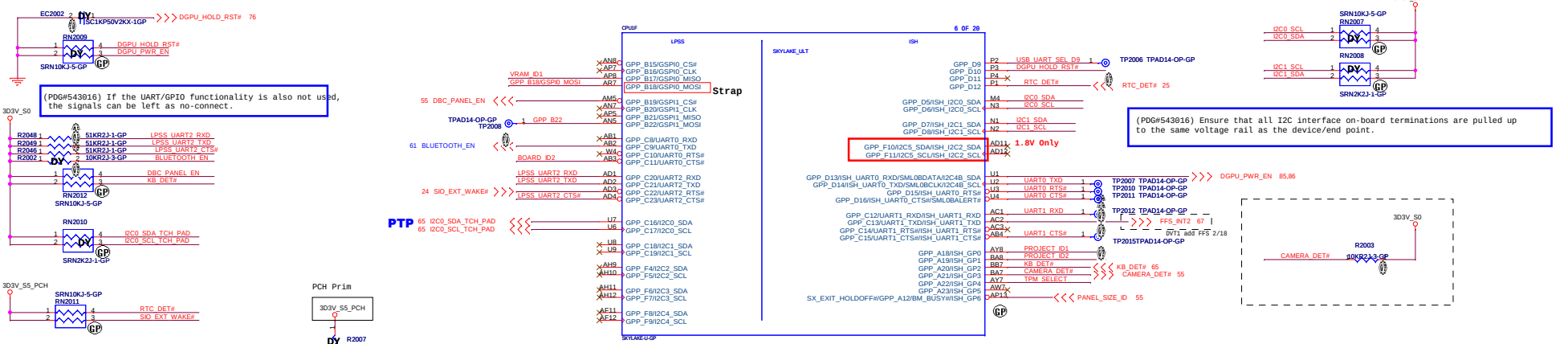
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

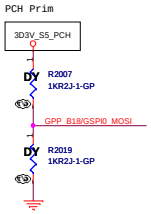
Title: *CPU_(AUDIO/SDIO/SDXC)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Monday, June 27, 2016 Sheet 19 of 105

Main Func = PCH





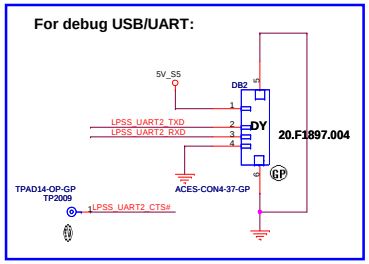
PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

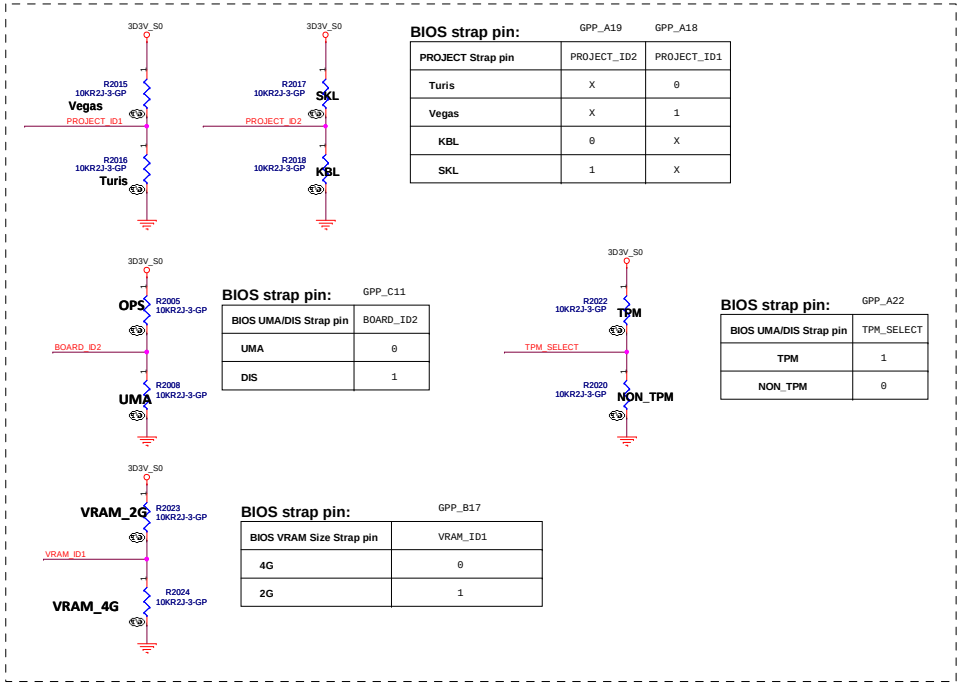
The signal has a weak internal pull-down.

071.SKYLA.000U

For debug USB/UART:



Intel has removed EHCI controller from BDW and proposed to use UART interface for Win7 debug.



BIOS strap pin: GPP_A19 GPP_A18

PROJECT Strap pin	PROJECT_ID2	PROJECT_ID1
Turis	X	0
Vegas	X	1
KBL	0	X
SKL	1	X

BIOS strap pin: GPP_C11

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin: GPP_A22

BIOS UMA/DIS Strap pin	TPM_SELECT
TPM	1
NON_TPM	0

BIOS strap pin: GPP_B17

BIOS VRAM Size Strap pin	VRAM_ID1
4G	0
2G	1

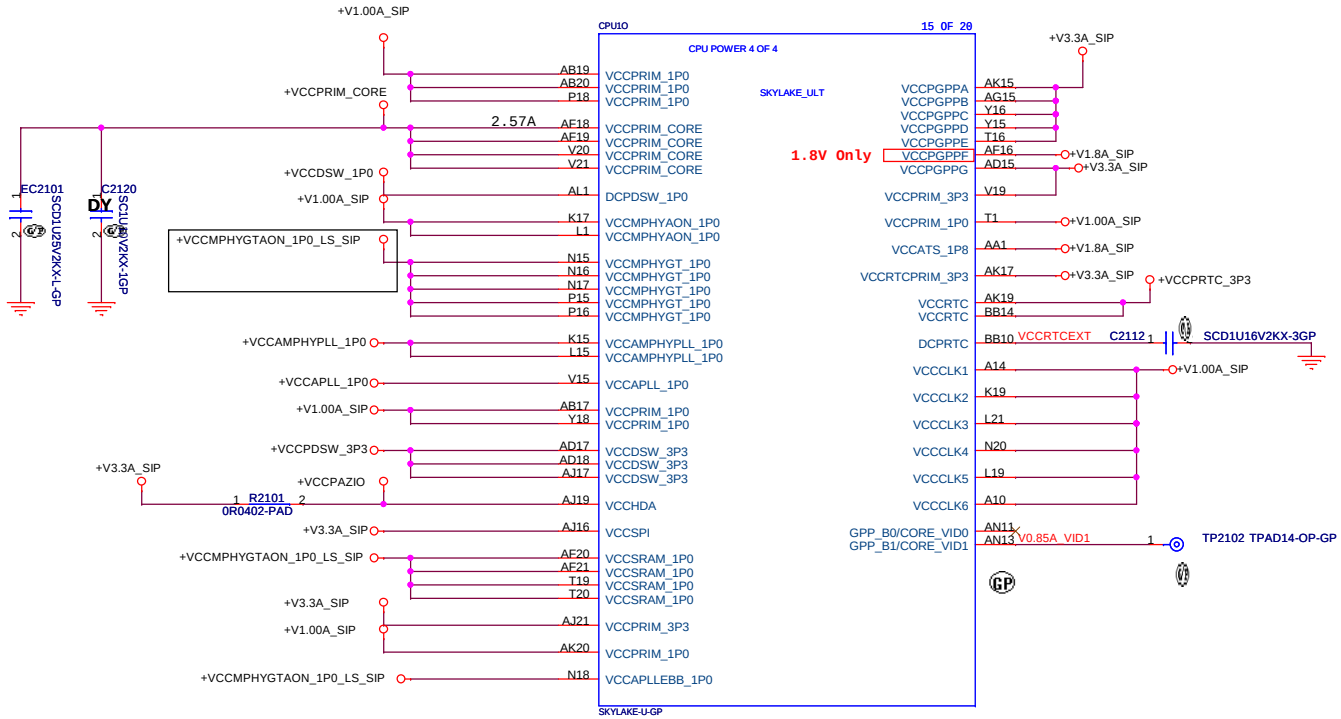
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPSS/ISH)

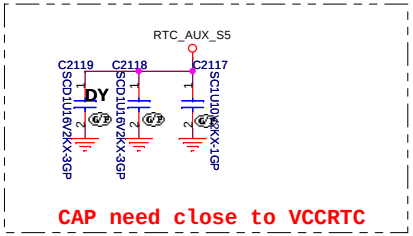
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

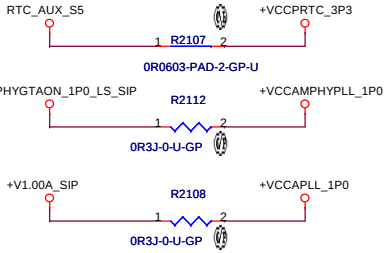
Date: Monday, June 27, 2016 | Sheet 20 of 105

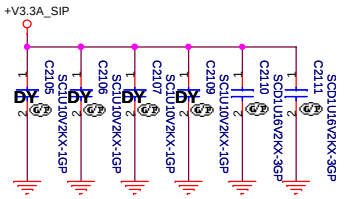
Main Func = PCH



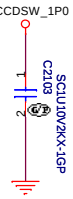
071.SKYLA.000U

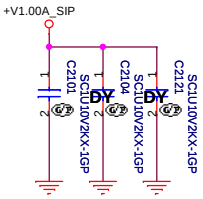




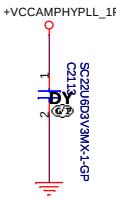


Layout Note:
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19



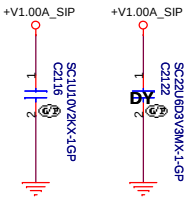


Layout Note:
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1



Layout Note:
22uF:
C2113 near K15

Layout Note:
22uF:
C2113 near K15



Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

<Core Design>

Wistron Corporation
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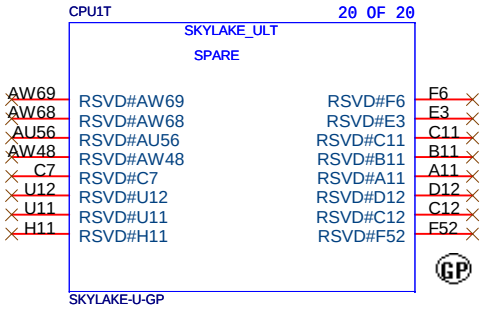
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size	Document Number	Rev
A3	Vegas SKL/KBL-U	A00

Date: Friday, June 24, 2016 Sheet 21 of 105

Main Func = PCH



071.SKYLA.000U

<Core Design>

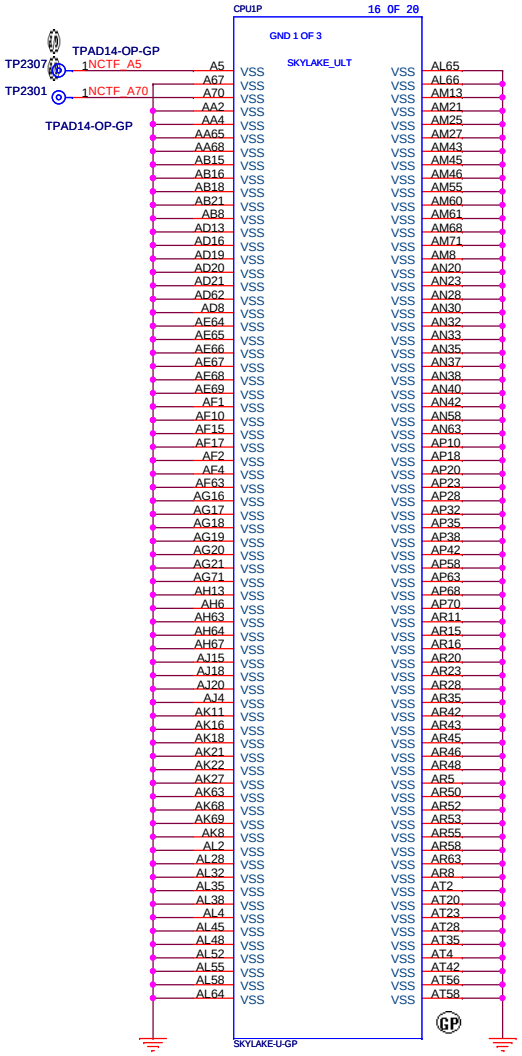
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(RSVD)***

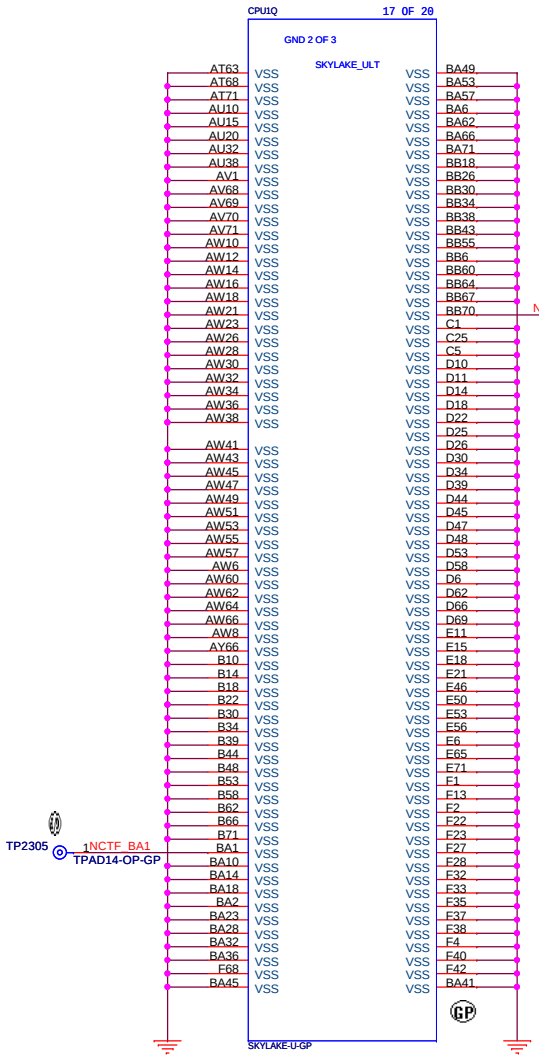
Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 22 of 105

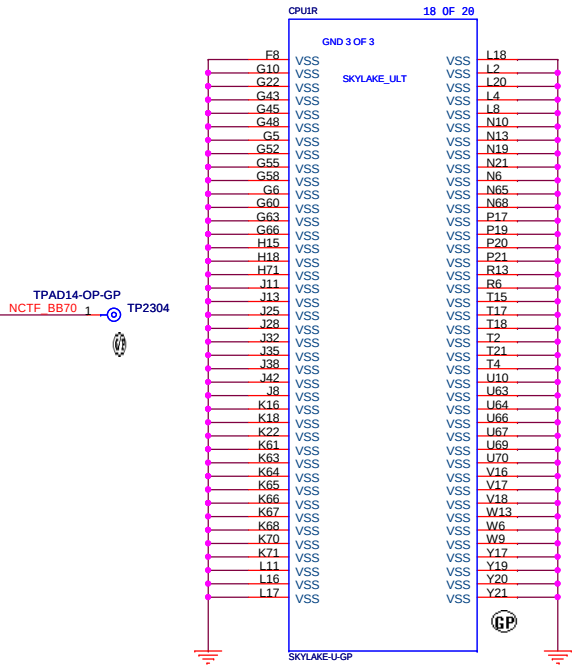
Main Func = PCH



071.SKYLA.000U



071.SKYLA.000U



071.SKYLA.000U

[#543016 Rev0.9]

Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Thursday, June 16, 2016 | Sheet 23 of 105

Main Func = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M00 (SA)	100.0K	10.0K	3.0V
X01 (SB)	100.0K	28.0K	2.75V
X02 (SC)	100.0K	33.0K	2.48V
X03(SD)	100.0K	47.0K	2.24V
A00 (I)	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO97)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Vegas_SKL_UMA	100.0K	10.0K(64.1802% EDI)	3.0V
Vegas_SKL_DIS	100.0K	22.1K(64.2712% EDI)	2.791V
Turis_SKL_UMA	100.0K	37.4K(64.3242% EDI)	2.491V
Turis_SKL_DIS	100.0K	49.9K(64.2995% EDI)	2.261V
Vega_SKL_DIS	100.0K	64.9K(64.6457% EDI)	2.001V
Turis_SKL_DIS	100.0K	93.1K(64.5513% EDI)	1.701V
Turis_SKL_DIS	100.0K	128K(64.1281% EDI)	1.495V
Turis_SKL_DIS	100.0K	200K(64.0807% EDI)	1.099V

Layout Note:
Need very close to EC

Need very close to EC

Layout Note:
Need very close to EC

Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

Layout Note:
Need very close to EC

Q2412 and Q2413 merge
2nd = 84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

D2401
75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D

Q2409
2nd = 84.2N702.I31
3rd = 84.07002.I31

Q2408
2nd = 84.2N702.J31
3rd = 84.07002.I31

Q2414
2nd = 84.2N702.I31
3rd = 84.07002.I31

D2402
83.R2004.G8F

D2403
83.R2004.G8F

D2404
83.R2004.G8F

D2405
83.R2004.G8F

MEC1404
071.01404.000E

KBC24

EC LCD test

EVT1 2014/10/20

XTAL-32D768KHZ-E9-GP
082.30003.0201

Power Switch Logic(PSL)

EC_GPIO47 High Active

EC_DEBUG
20.K0691.006

For T8 TEMP test

<Core Design>

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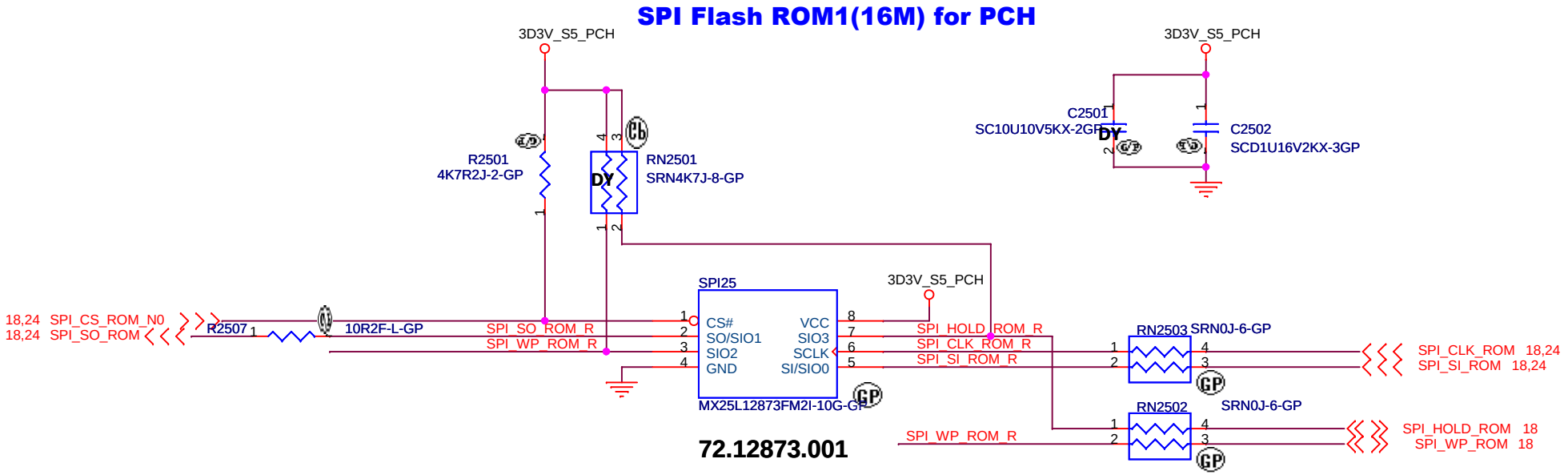
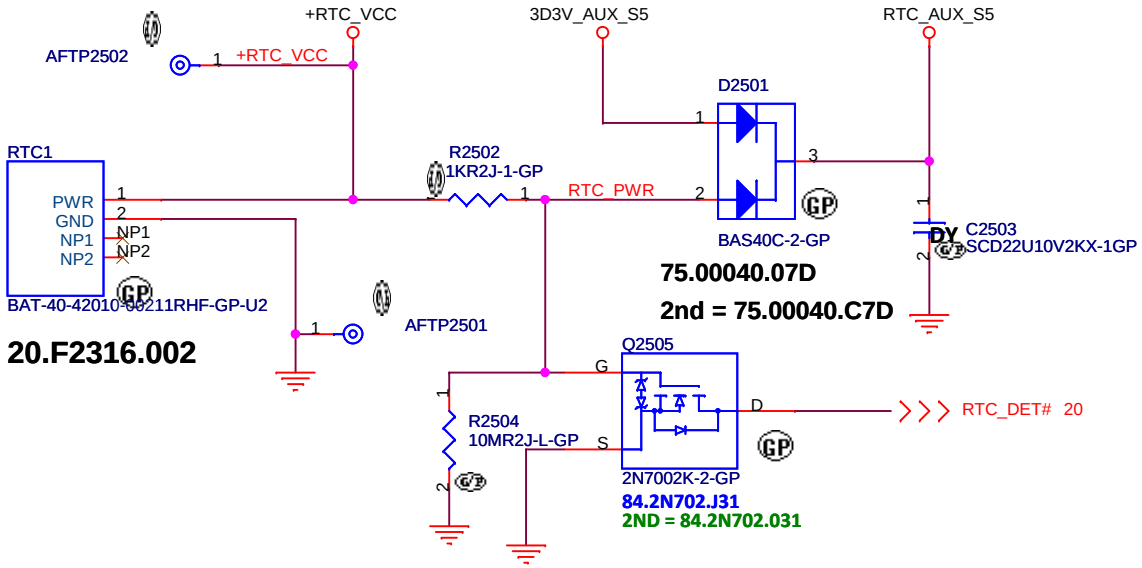
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC SMSC 1404
Size: A3 | Document Number: Vegas SKLIKBL-U | Rev: A00
Date: Monday, June 27, 2016 | Sheet 24 of 105

Main Func = SPI Flash



Main Func = RTC



<Core Design>

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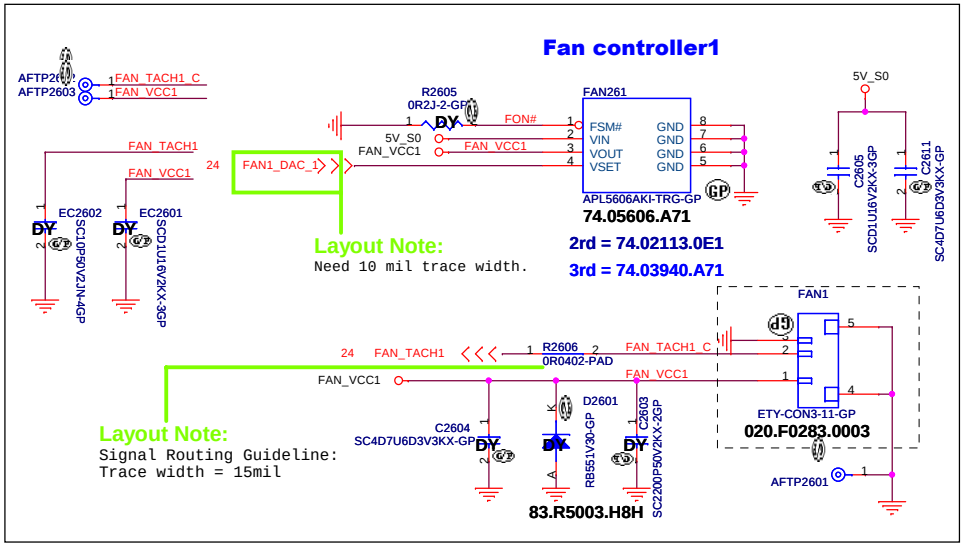
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

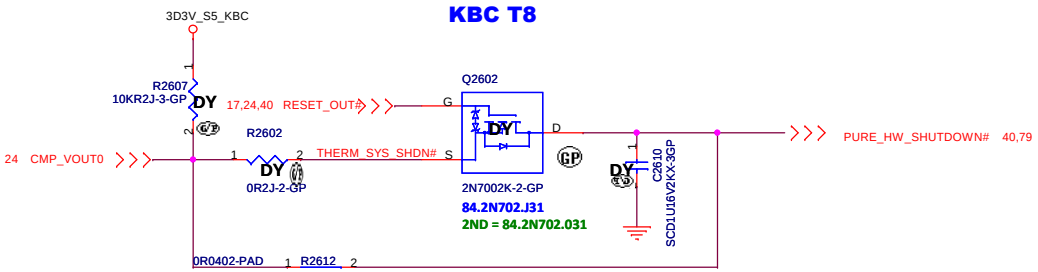
Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

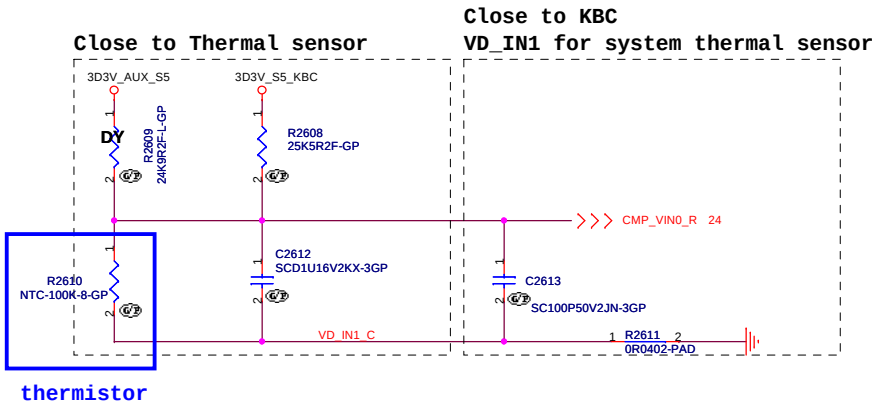
Date: Monday, June 27, 2016 Sheet 25 of 105

Main Func = Thermal Sensor



change the fan define & connect P/N 020.F0283.0003 by Andy 1/27





<Core Design>

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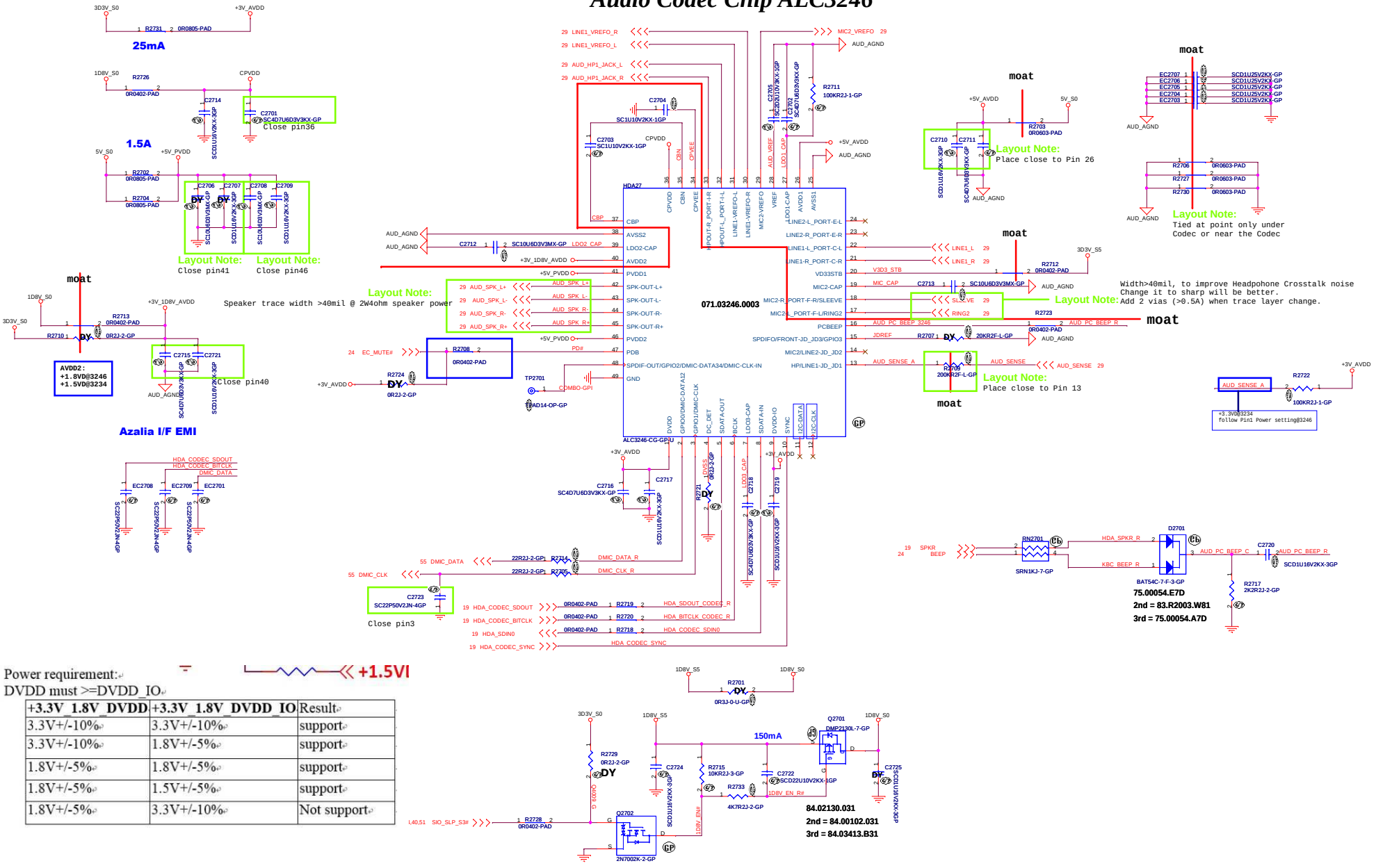
Title	THERMAL NCT7718W/Fan	
Size A3	Document Number Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 26 of 105	

Main Func = Audio

Audio Codec Chip ALC3246



+3.3V_1.8V_DVDD	+3.3V_1.8V_DVDD_IO	Result
3.3V+/-10%	3.3V+/-10%	support
3.3V+/-10%	1.8V+/-5%	support
1.8V+/-5%	1.8V+/-5%	support
1.8V+/-5%	1.5V+/-5%	support
1.8V+/-5%	3.3V+/-10%	Not support

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3246

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 27 of 109

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

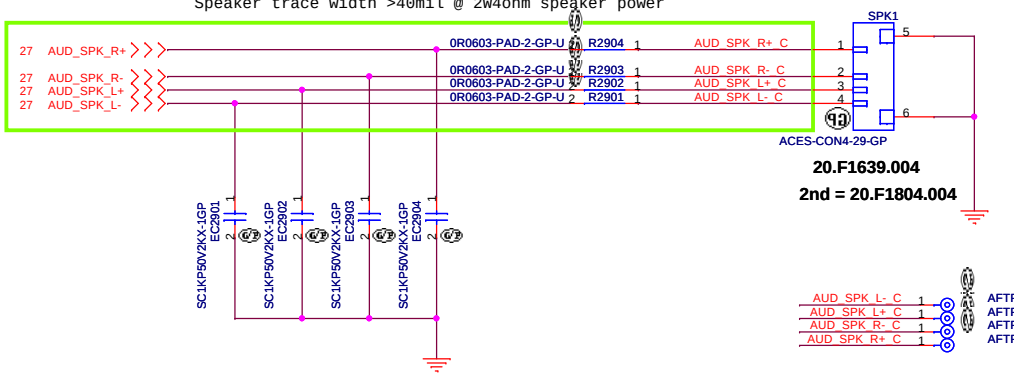
Title: *(Reserved)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 28 of 105

Main Func = Audio

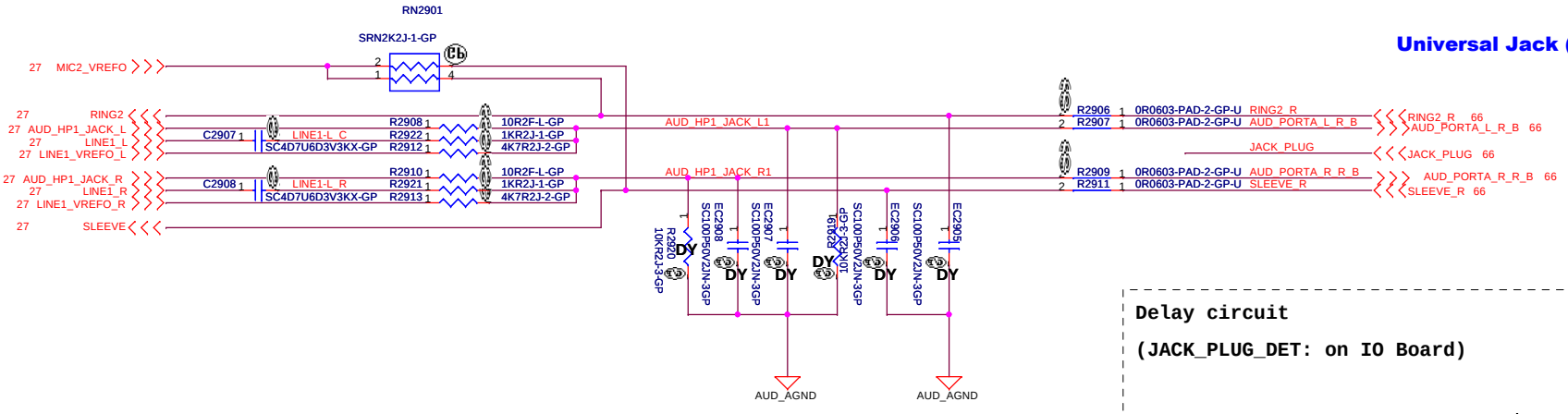
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



Speaker

20.F1639.004
2nd = 20.F1804.004

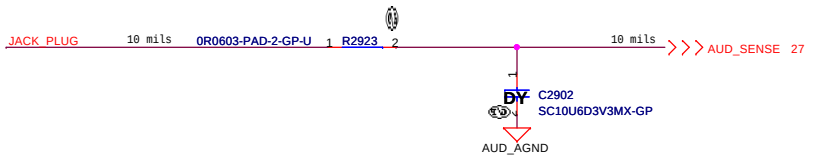
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Universal Jack (Moved to I/O Board)

Delay circuit

(JACK_PLUG_DET: on IO Board)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio IO**

Size: A3 | Document Number: **Vegas SKL/KBL-U** | Rev: **A00**

Date: Monday, June 27, 2016 | Sheet 29 of 105

(Blanking)

<Core Design>

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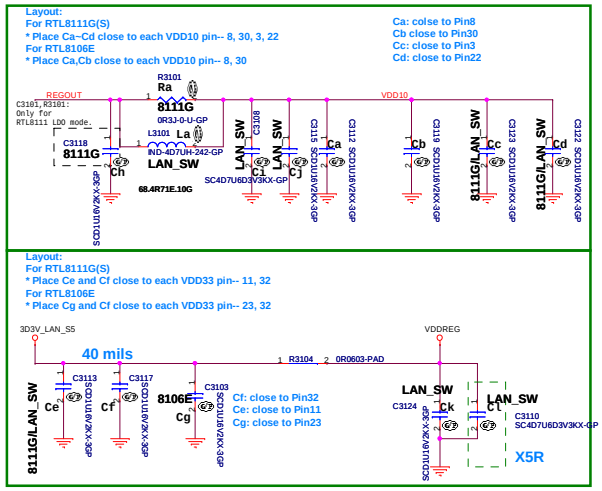
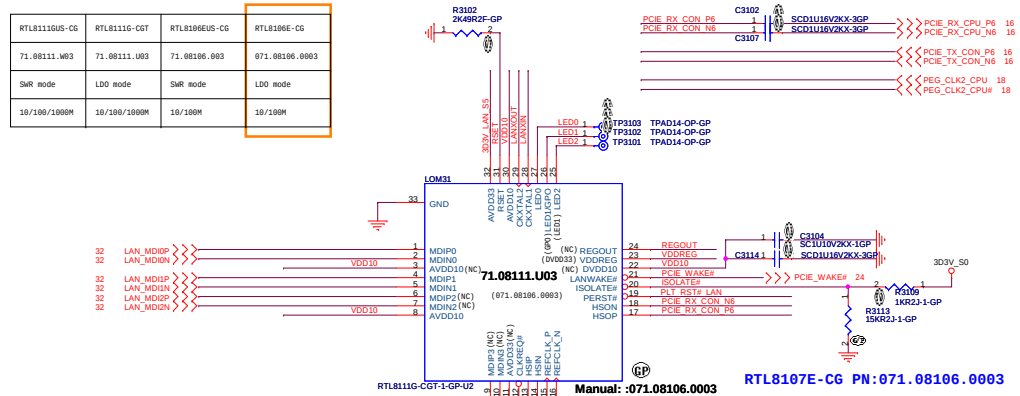
Title *(Reserved)*		
Size A4	Document Number Vegas SKL/KBL-U	Rev A00
Date: Thursday, June 16, 2016	Sheet 30 of 105	

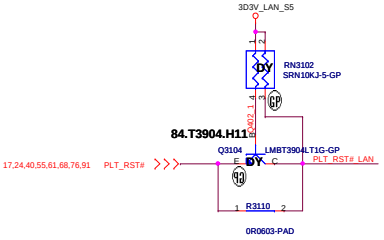
Main Func = LAN

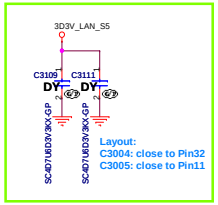
LAN CHIP (10/100/1000M & 10/100M co-lay)



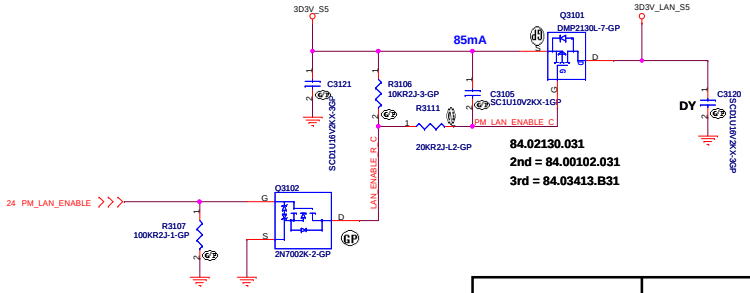
RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

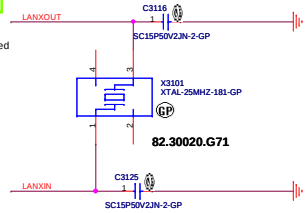


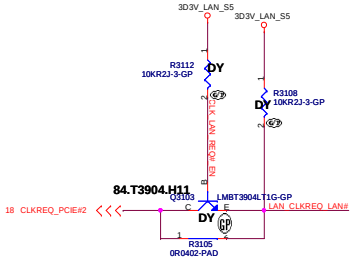




3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.







	BOM Option	1.0V Source	Ra	Ch	Cc	Cd	Ce	La	Ci	Cj	Ck	Cl	Cg
RTL8111G-CGT (71.08111.U03)	8111G	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03)/ RTL8106EUS-CG (71.08106.003)	LAN_SW	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	8106E	LDO	X	X	X	X	X	X	X	X	X	X	O

<Core Design>
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Taipei Hsien 221, Taiwan, R.O.C.

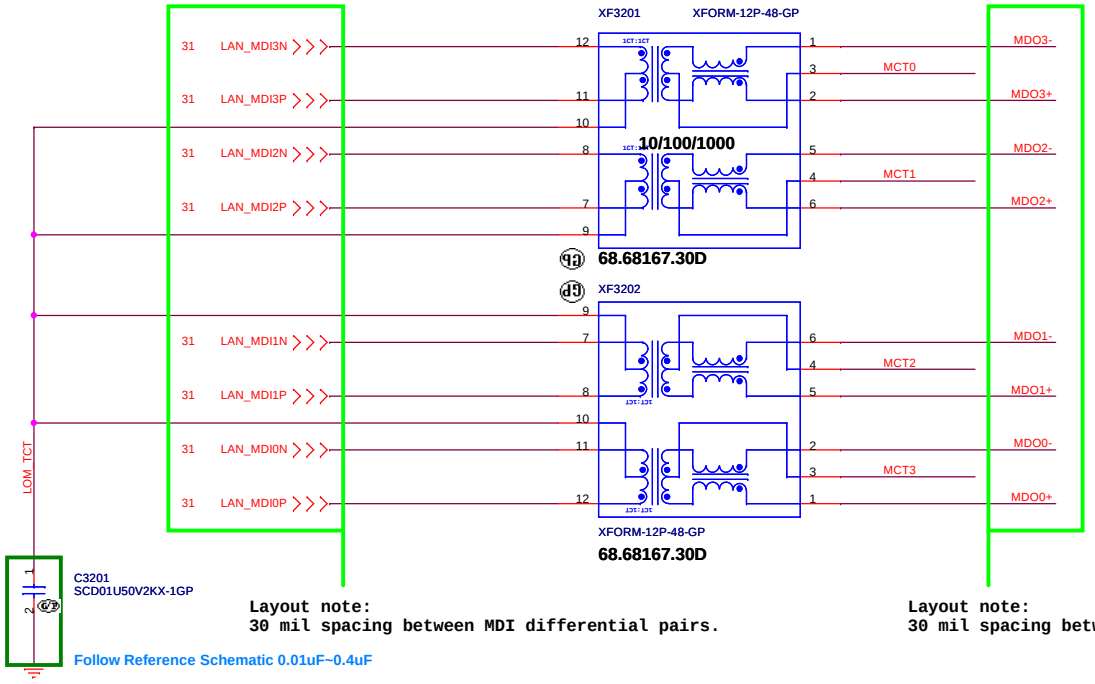
Title: LAN RTL8106

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

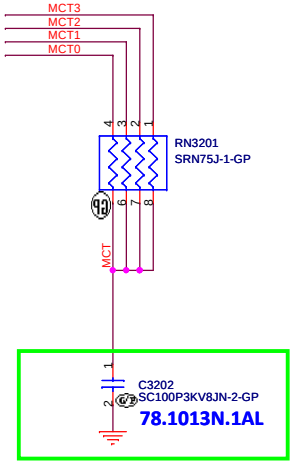
Date: Monday, June 27, 2016 | Sheet 31 of 105

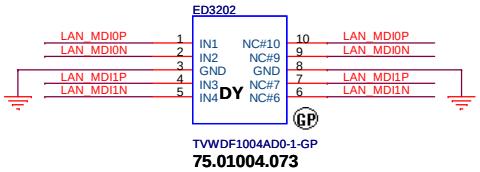
Main Func = LAN

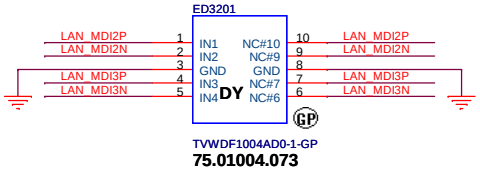
LAN TransFormer (10/100/1000M & 10/100M co-lay)



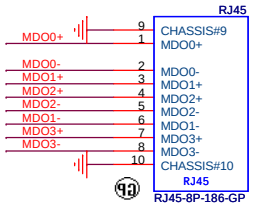
Layout note:
30 mil spacing between MDI differential pairs.



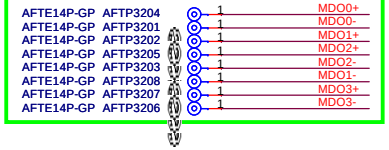




Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



<Core Design>

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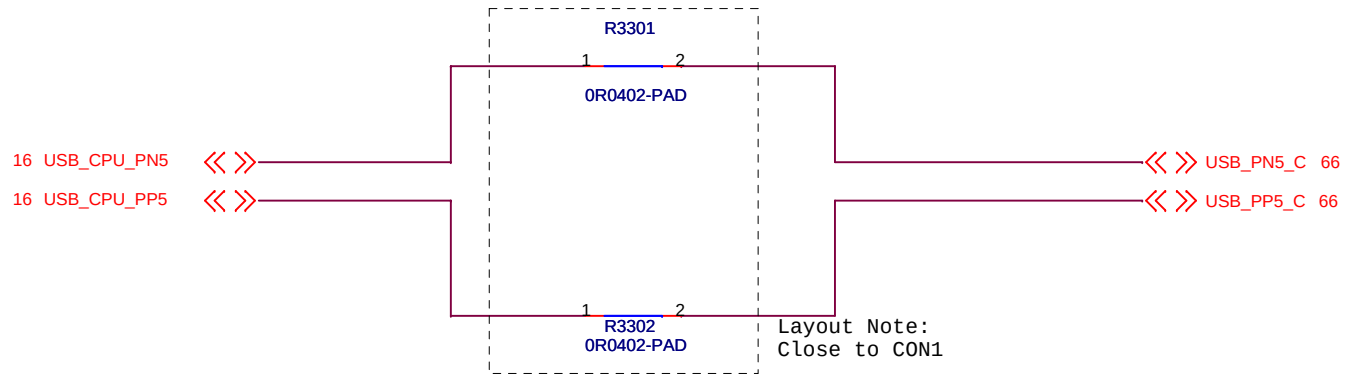
Taipei Hsien 221, Taiwan, R.O.C.

Title		
XFOM&RJ45		
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 32 of 105	

Main Func = Card Reader



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Card Reader-RTS5170***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Monday, June 27, 2016 Sheet 33 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

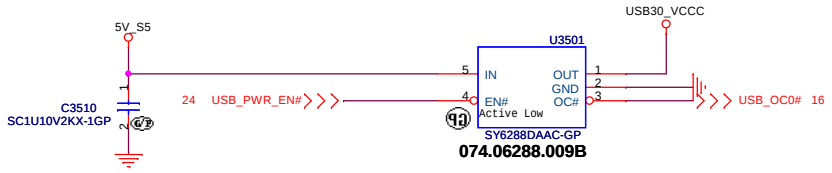
Title

(Reserved)

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

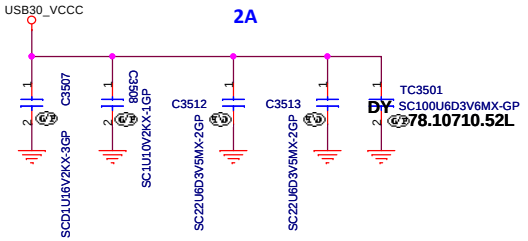
Date: Thursday, June 16, 2016 Sheet 34 of 105

Main Func = USB3.0 Port1

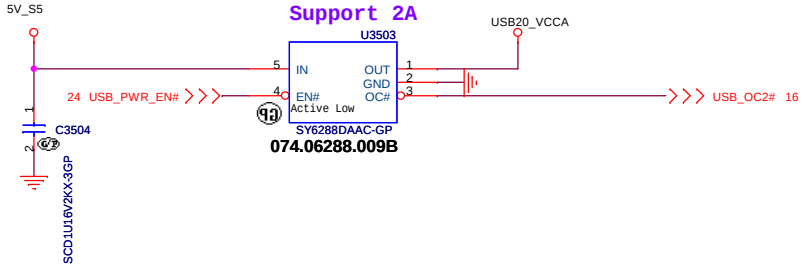


USB3.0 Port1

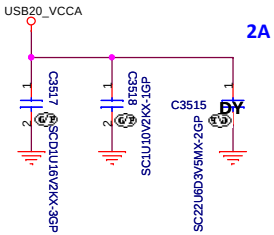
Layout Note: Close USB1



Main Func = USB2.0 Port3



USB2.0 Port3 (IO Board)



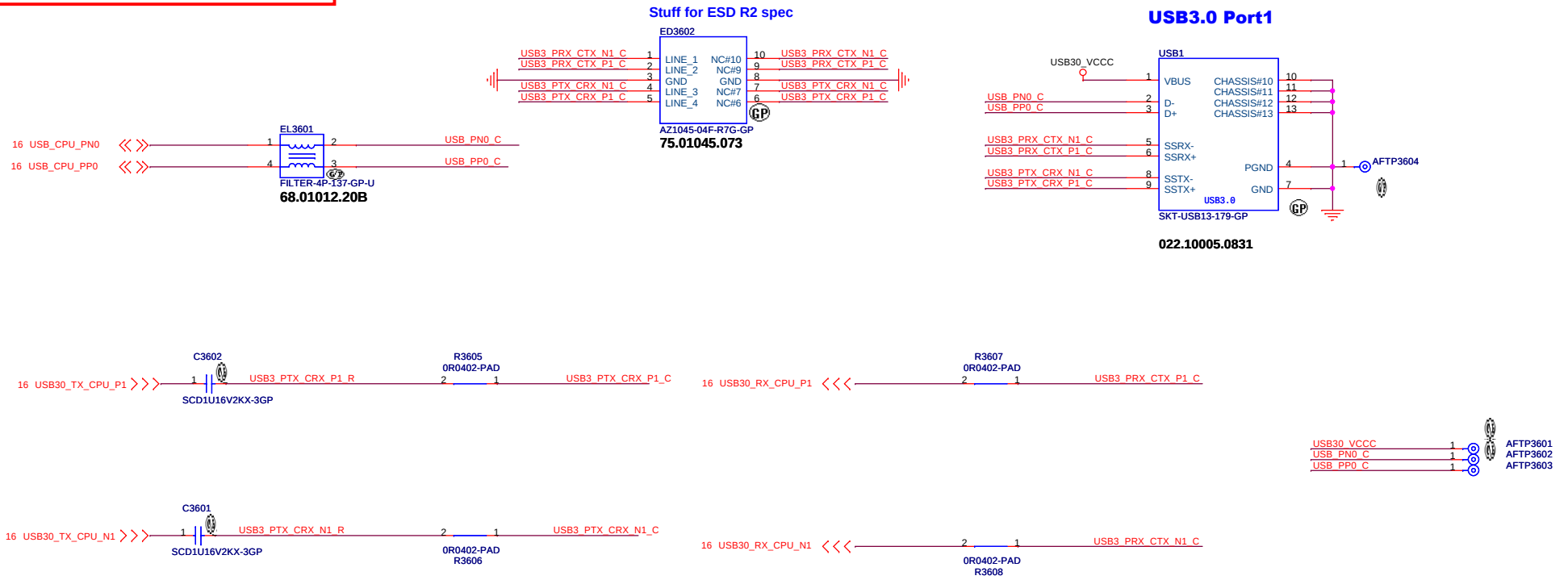
Layout Note: Close CON1

<Core Design>

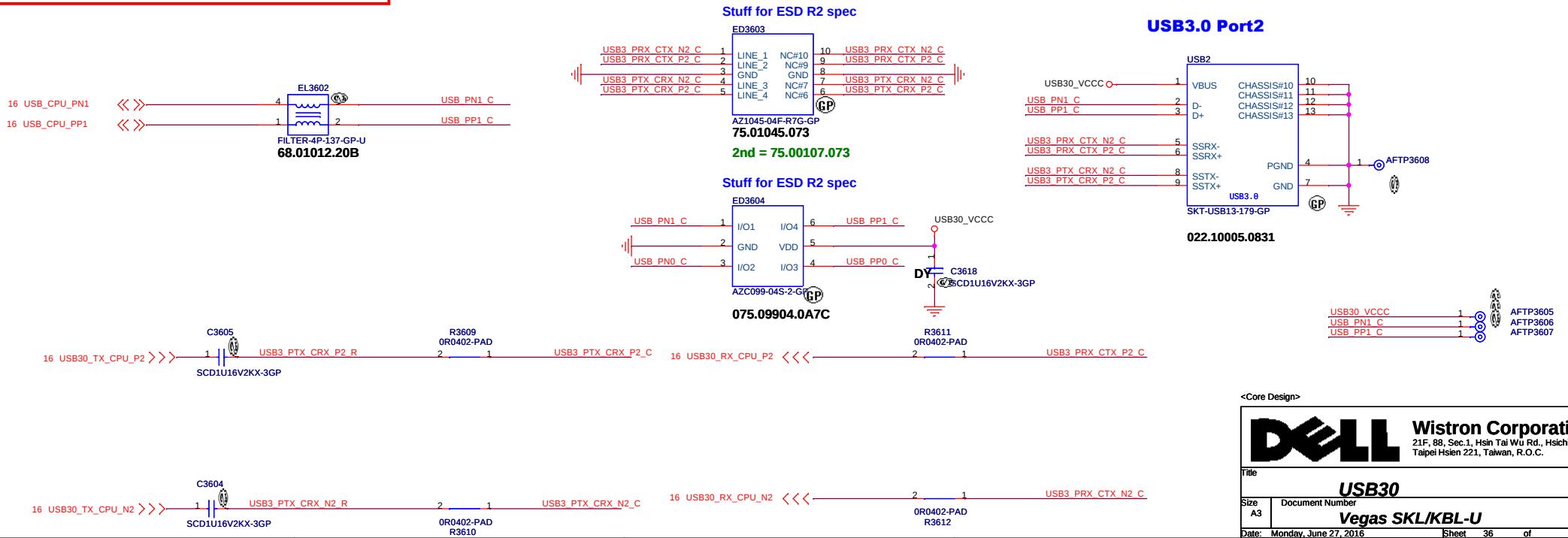
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*USB switch*	
Size	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
Date: Monday, June 27, 2016	Sheet 35 of 105	

Main Func = USB3.0 Port1



Main Func = USB3.0 Port2



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

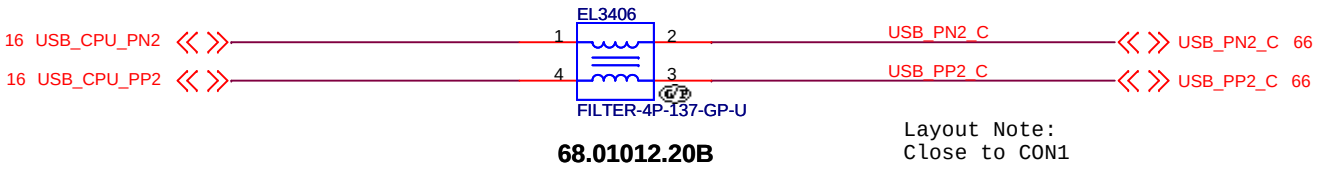
Title: USB30

Size	Document Number	Rev
A3	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 36 of 105

Main Func = USB2.0 Port3

USB port 3 (USB2.0 only) CMC

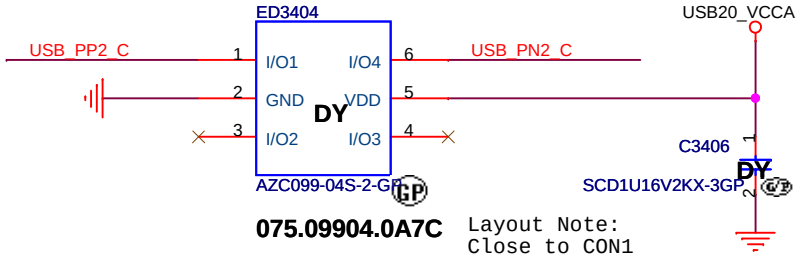


68.01012.20B

Layout Note:
Close to CON1

USB ESD Diode

Stuff for ESD R2 spec



075.09904.0A7C

Layout Note:
Close to CON1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB20		
Size: A4	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 37 of 105	

(Blanking)

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *(Reserved)*		
Size: A4	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
Date: Thursday, June 16, 2016	Sheet 38 of 105	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

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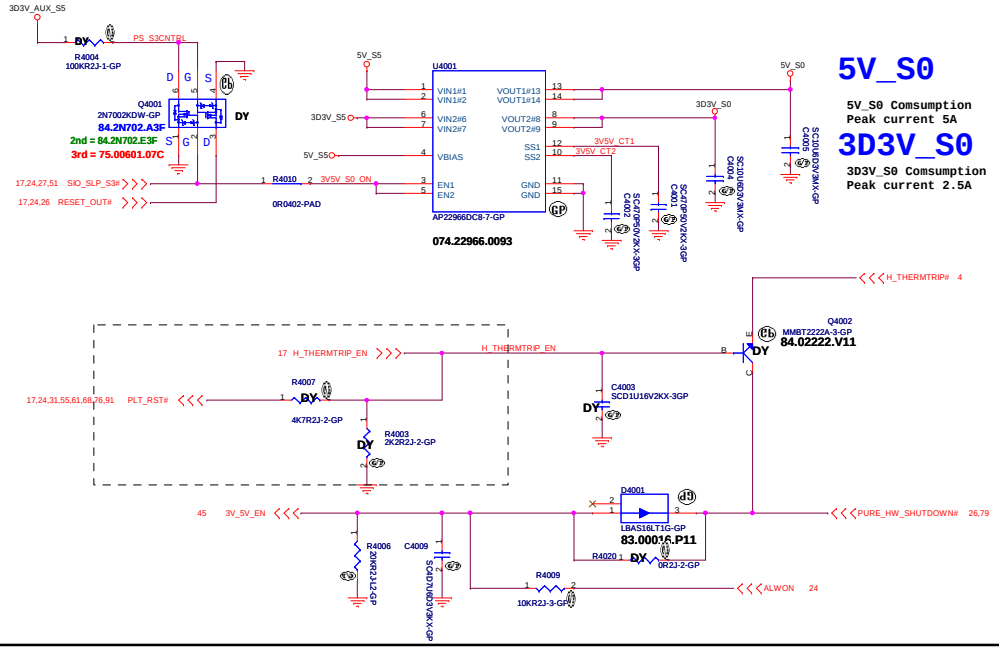
Main Func = Power Plane & Sequence

ROSA Run Power



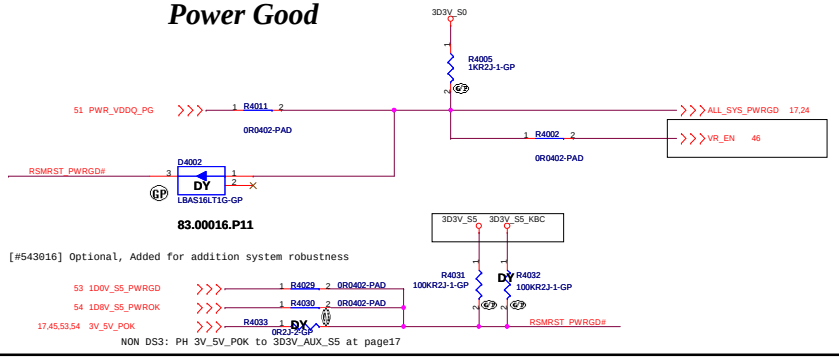
5V_S0

5V_S0 Comsumption
Peak current 5A

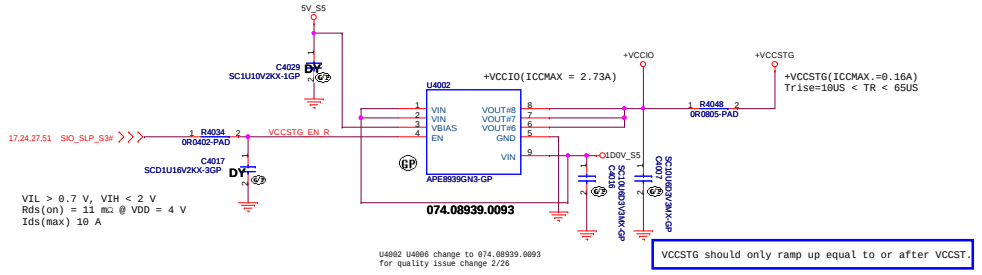
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

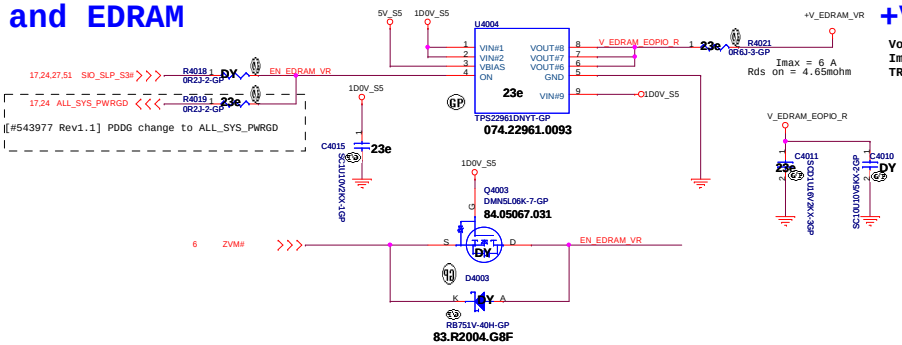
Power Good



VCCSTG and VCCIO



EOPIO and EDRAM



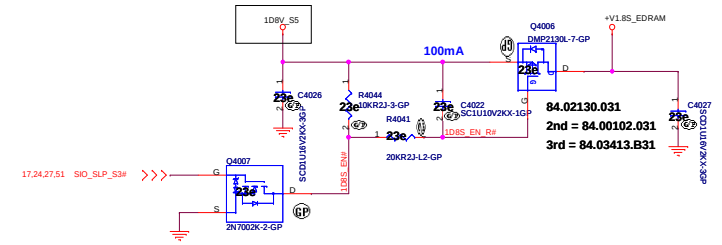
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

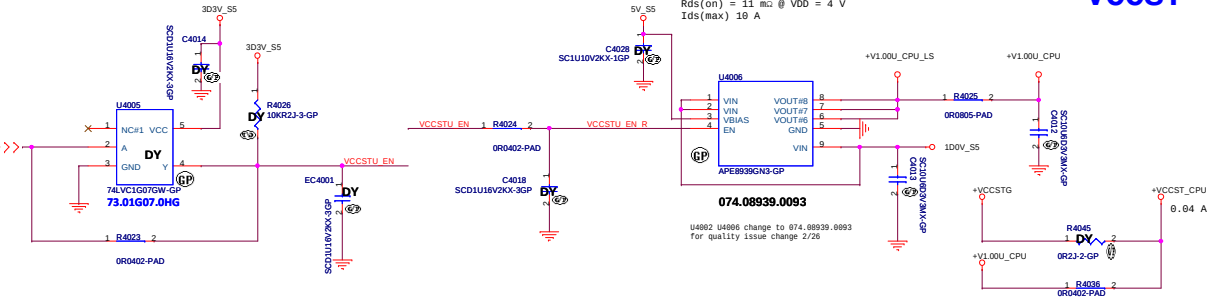
V1.8S



MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

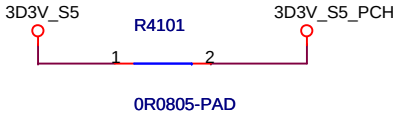
VCCST



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable
Size: A2
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Monday, June 27, 2016
Sheet 40 of 105

Main Func = Power & Sequence



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Connected_Standby(1/2)+DS3***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 41 of 105

(Blanking)

<Core Design>

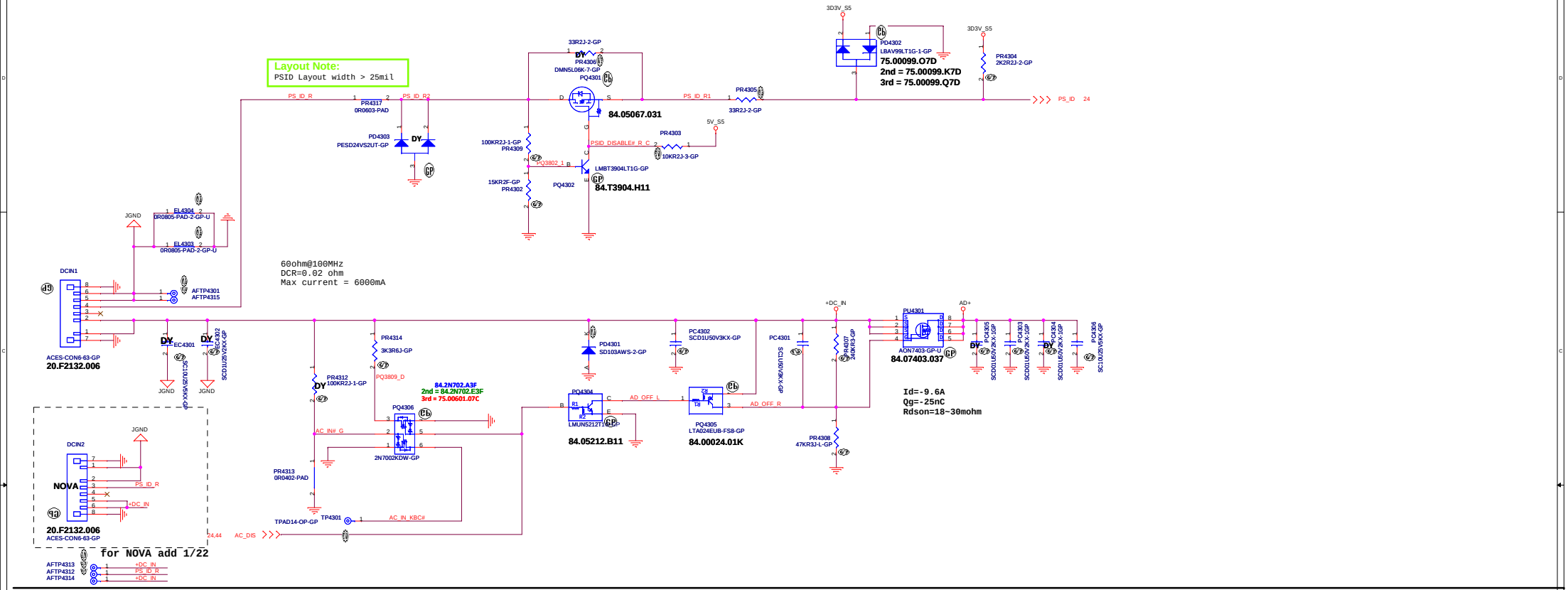
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(2/2)*

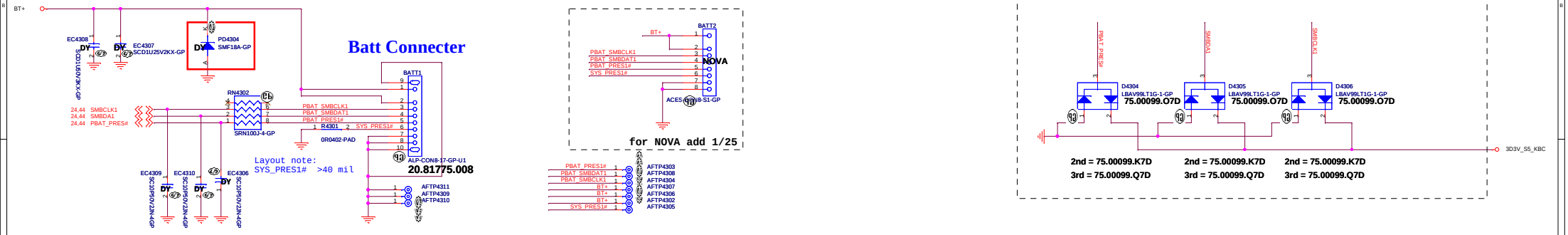
Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Thursday, June 16, 2016 Sheet 42 of 105

Main Func = ADT Input



Main Func = M-BAT Input



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DCIN		
Size: A2	Document Number: Vegas SKL/KBL-U	Rev: A00
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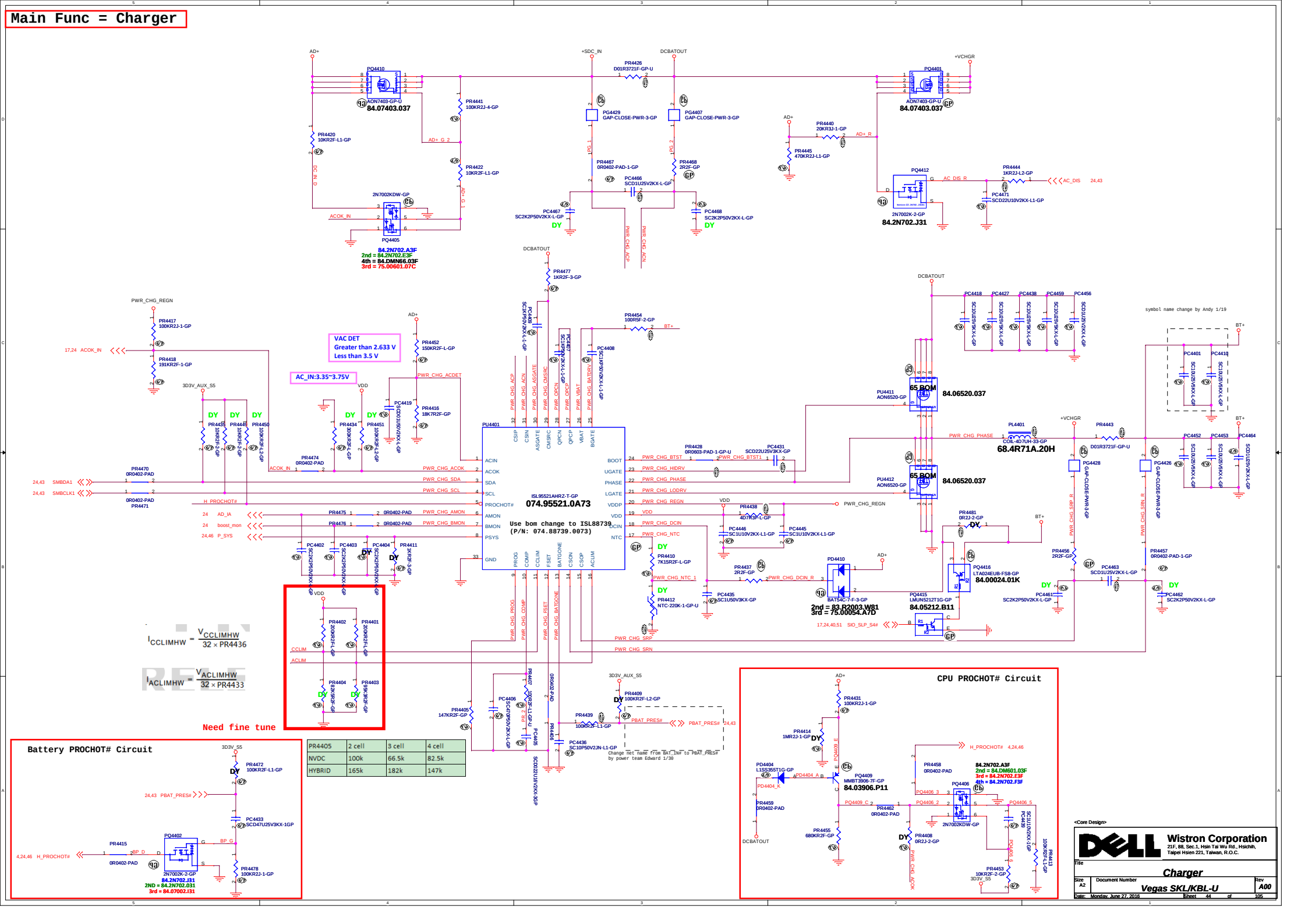
Main Func = Charger



$$I_{CCLIMHW} = \frac{V_{CCLIMHW}}{32 \times PR4436}$$

$$I_{ACLIMHW} = \frac{V_{ACLIMHW}}{32 \times PR4433}$$

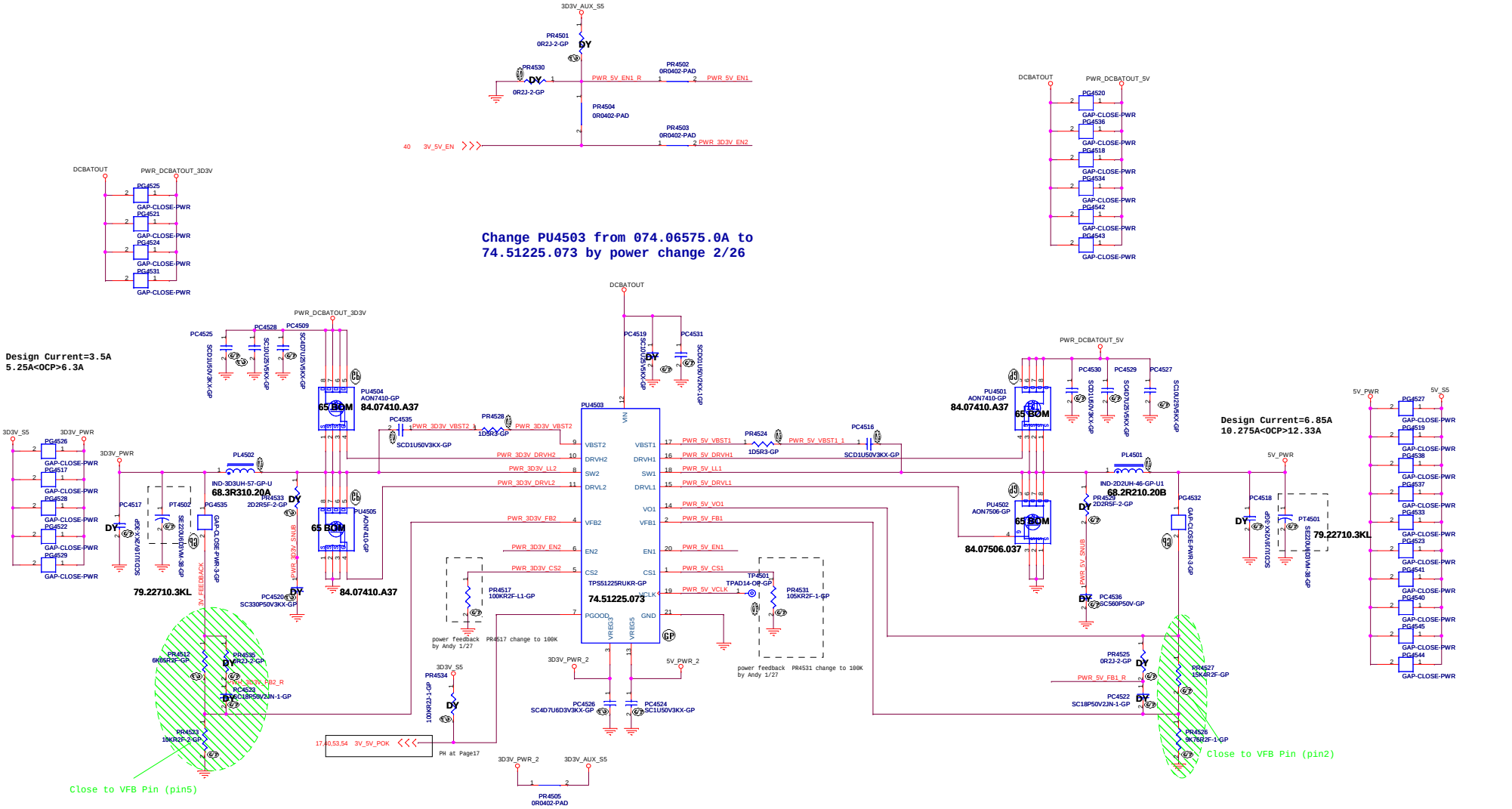
PR4405	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00
Date: Monday, June 27, 2016 | Sheet 44 of 105

Main Func = 3D3V_5V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

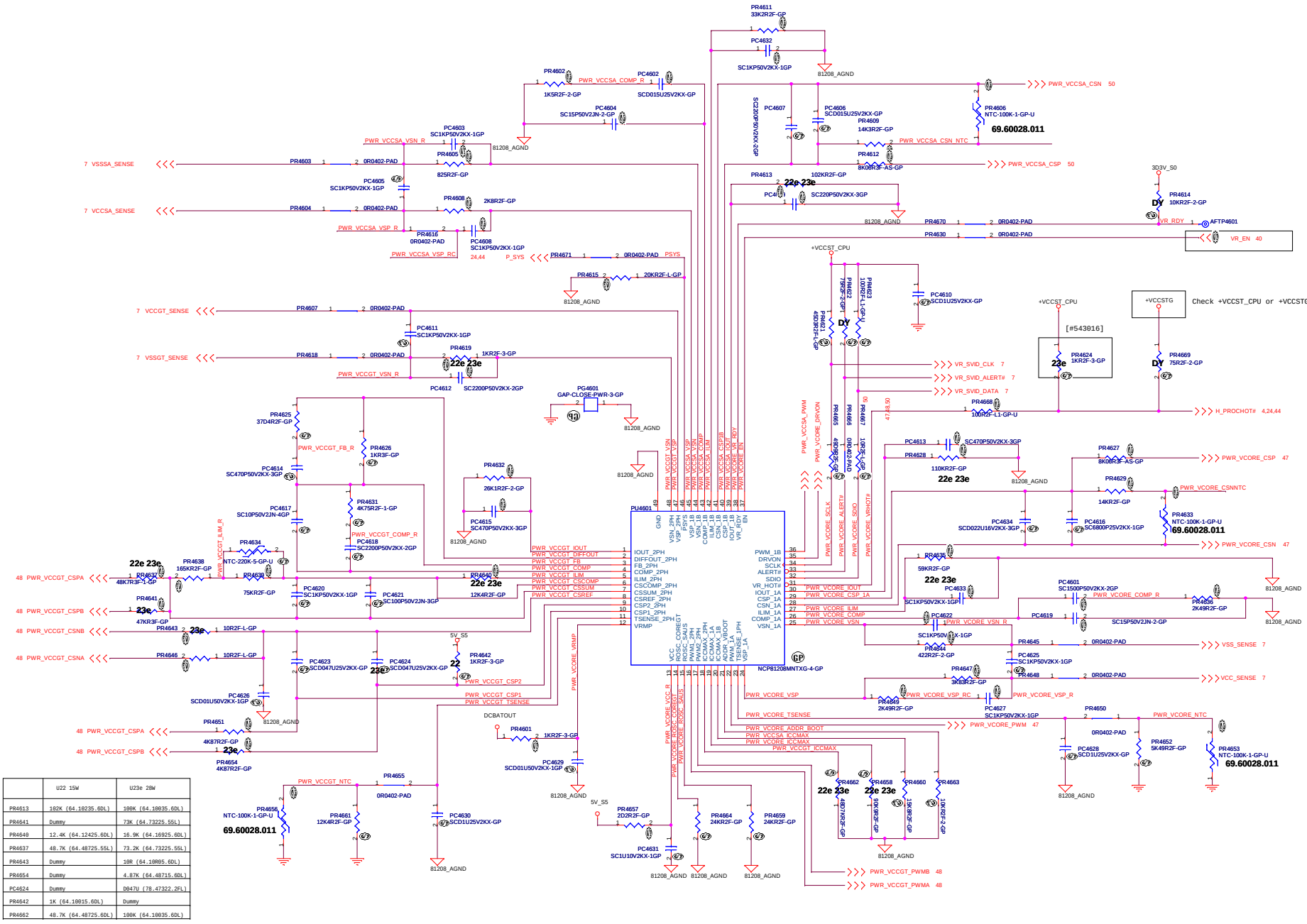
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC-3D3V&5V

Size	Document Number	Rev
A2	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 45 of 105

Main Func = CPU_CORE



	U22 15W	U23e 28W
PR4613	102K (64.10235.6DL)	100K (64.10035.6DL)
PR4641	Dummy	73K (64.73225.55L)
PR4640	12.4K (64.12425.6DL)	16.9K (64.16925.6DL)
PR4637	48.7K (64.48725.55L)	73.2K (64.73225.55L)
PR4643	Dummy	10R (64.10R05.6DL)
PR4654	Dummy	4.87K (64.48715.6DL)
PC4624	Dummy	D047U (78.47322.2FL)
PR4642	1K (64.10015.6DL)	Dummy
PR4662	48.7K (64.48725.6DL)	100K (64.10035.6DL)

<Core Design>

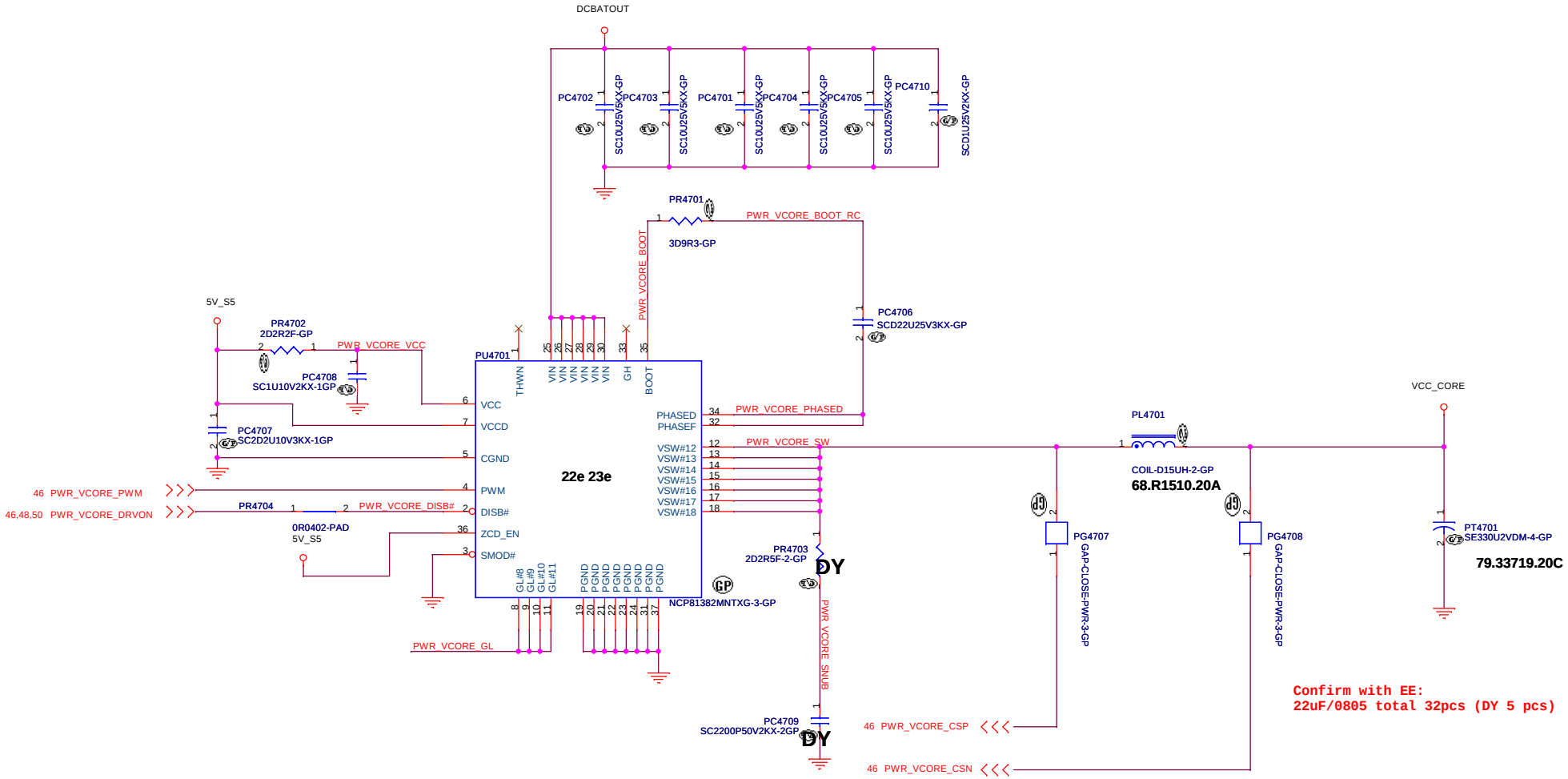
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)

Size	Document Number	Rev
A2	Vegas SKL/KBL-U	A00

Date: Monday, June 27, 2016 Sheet 46 of 105

Main Func = CPU_CORE

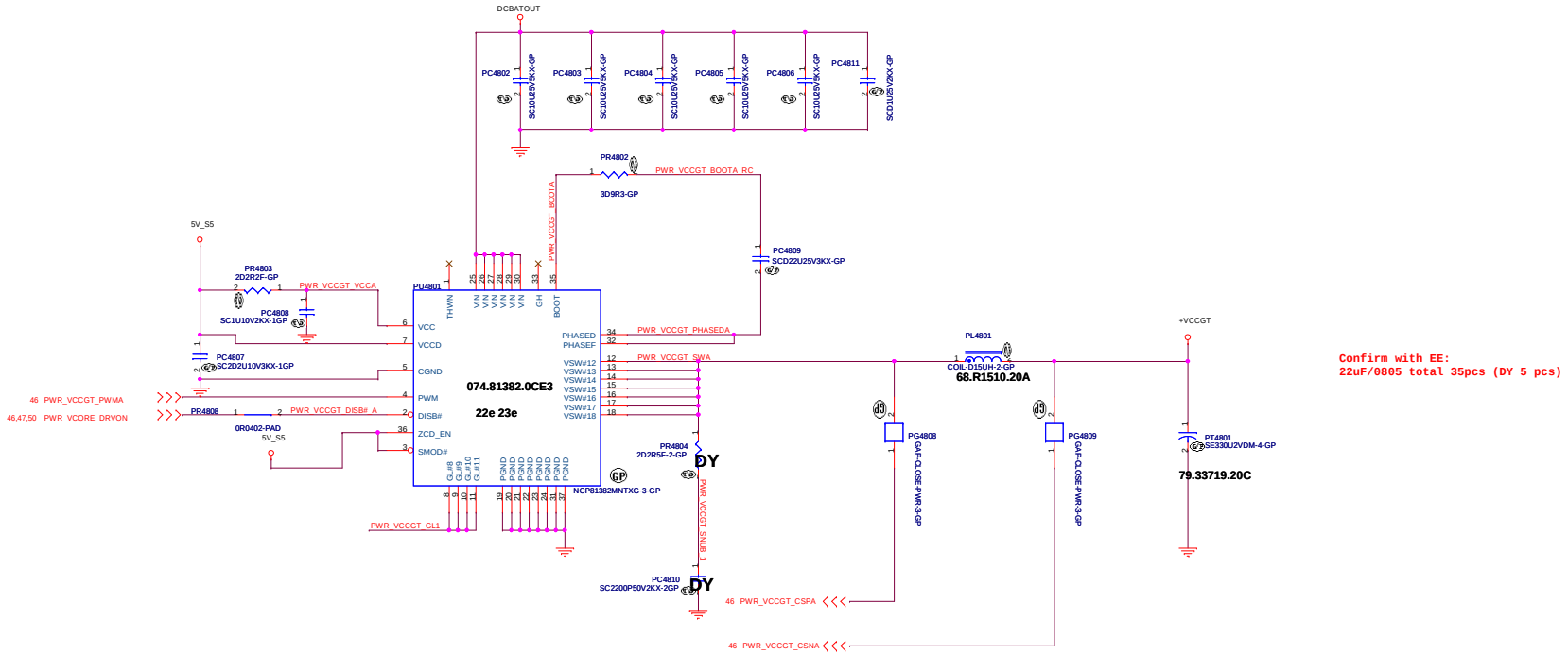


<Core Design>

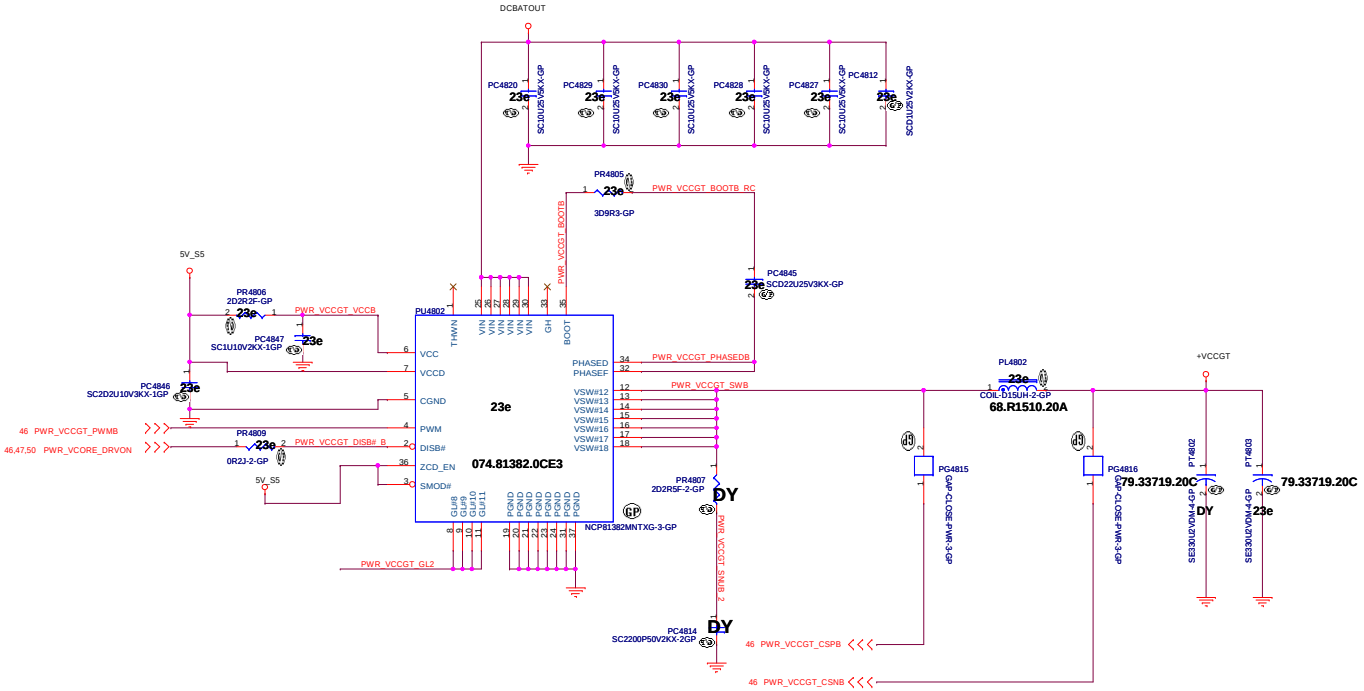
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81382MN_CPU_VCORE(2/3)	
Size A3	Document Number Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 47 of 105	

Main Func = CPU_CORE



Confirm with EE:
22uF/0805 total 35pcs (DY 5 pcs)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 48 of 105

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<Core Design>

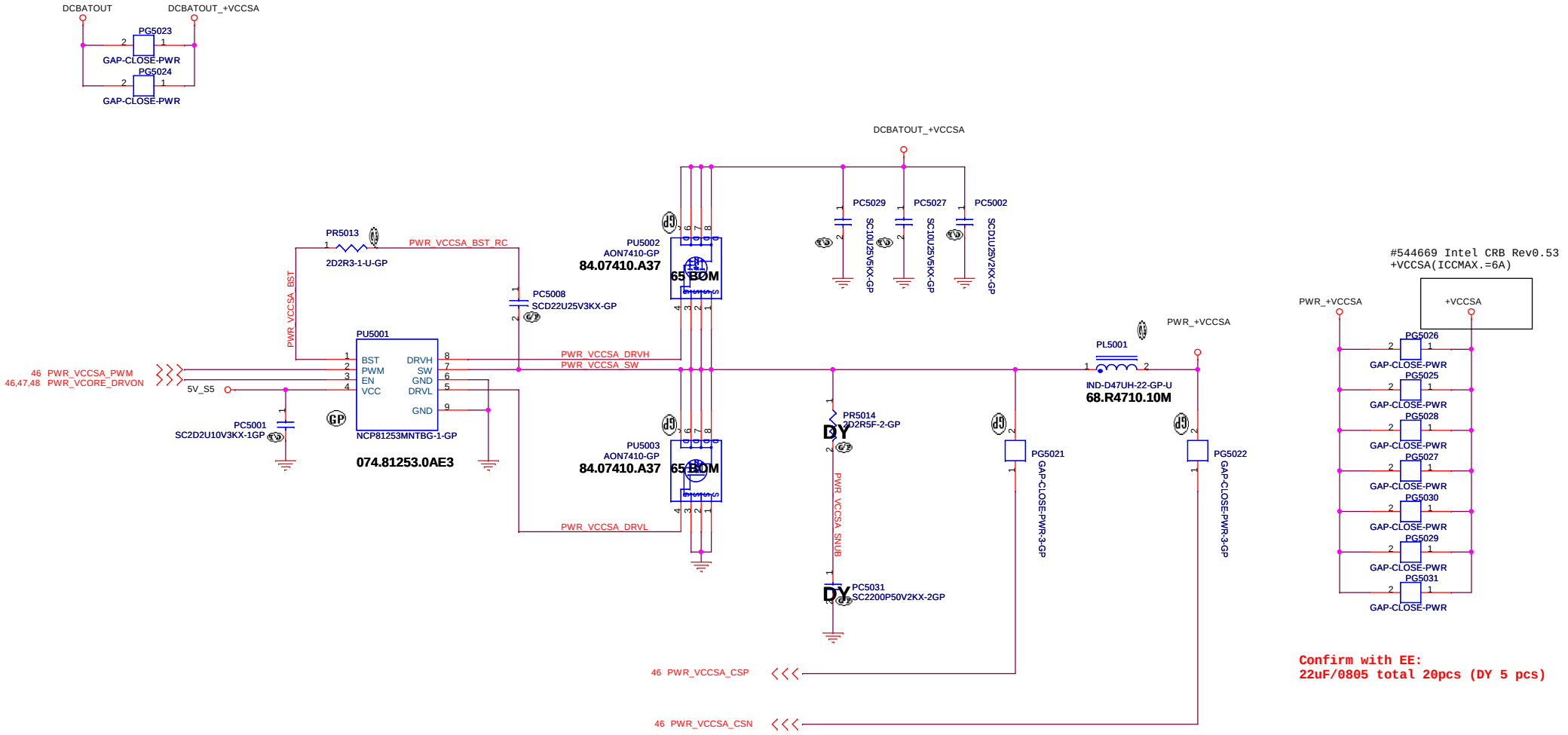
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***NCP81210MN_CPU_VCCGTUS***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 49 of 105

Main Func = CPU_CORE



#544669 Intel CRB Rev0.53
+VCCSA(ICCMAX.=6A)

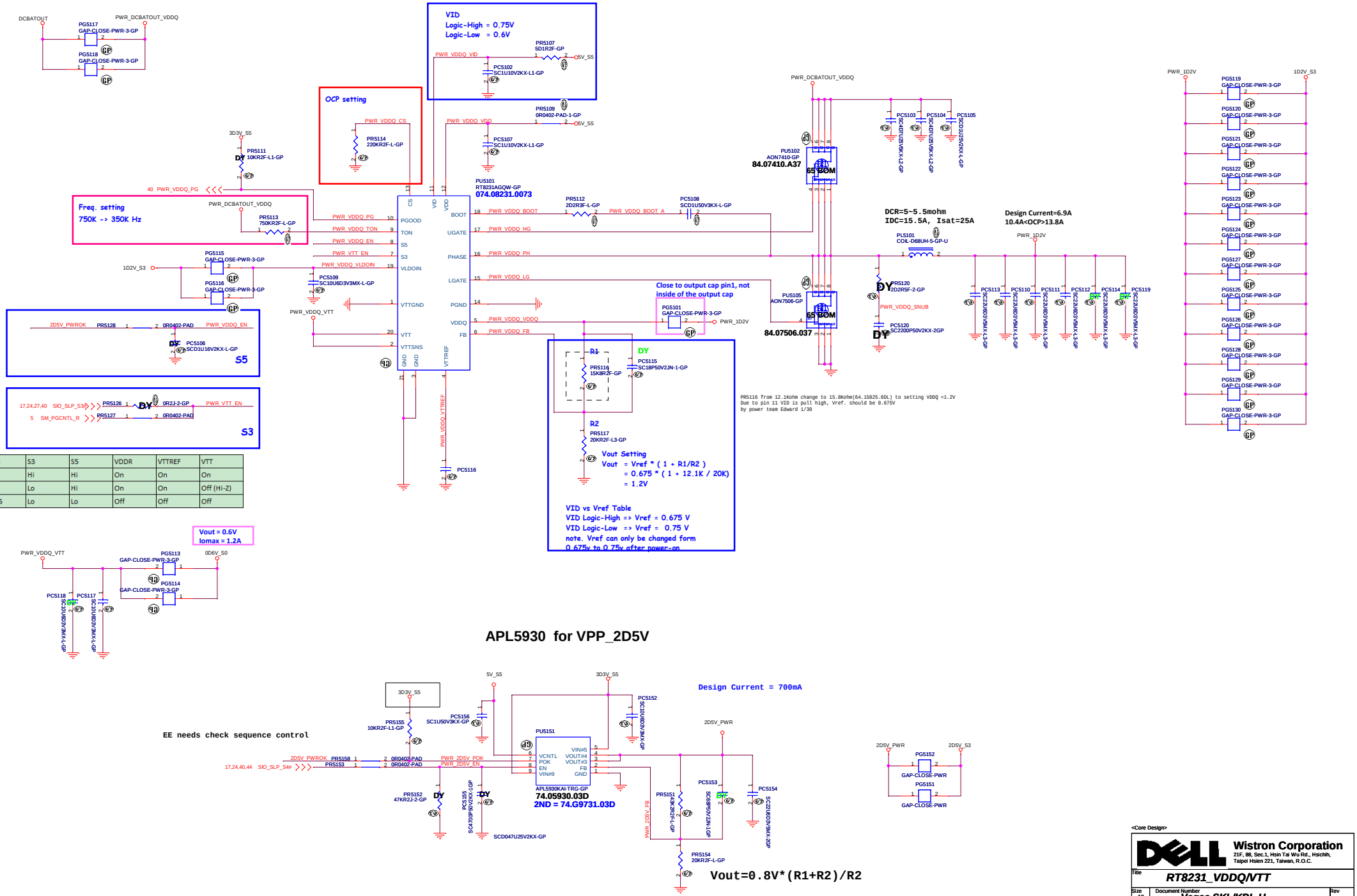
Confirm with EE:
22uF/0805 total 20pcs (DY 5 pcs)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81253MN_CPU_VCCSA	
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 50 of 105	

SSID = PWR.Plane.Regulator_1p2v& 2D5V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8231_VDDQ/VTT

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Monday, June 27, 2016 | Sheet 51 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

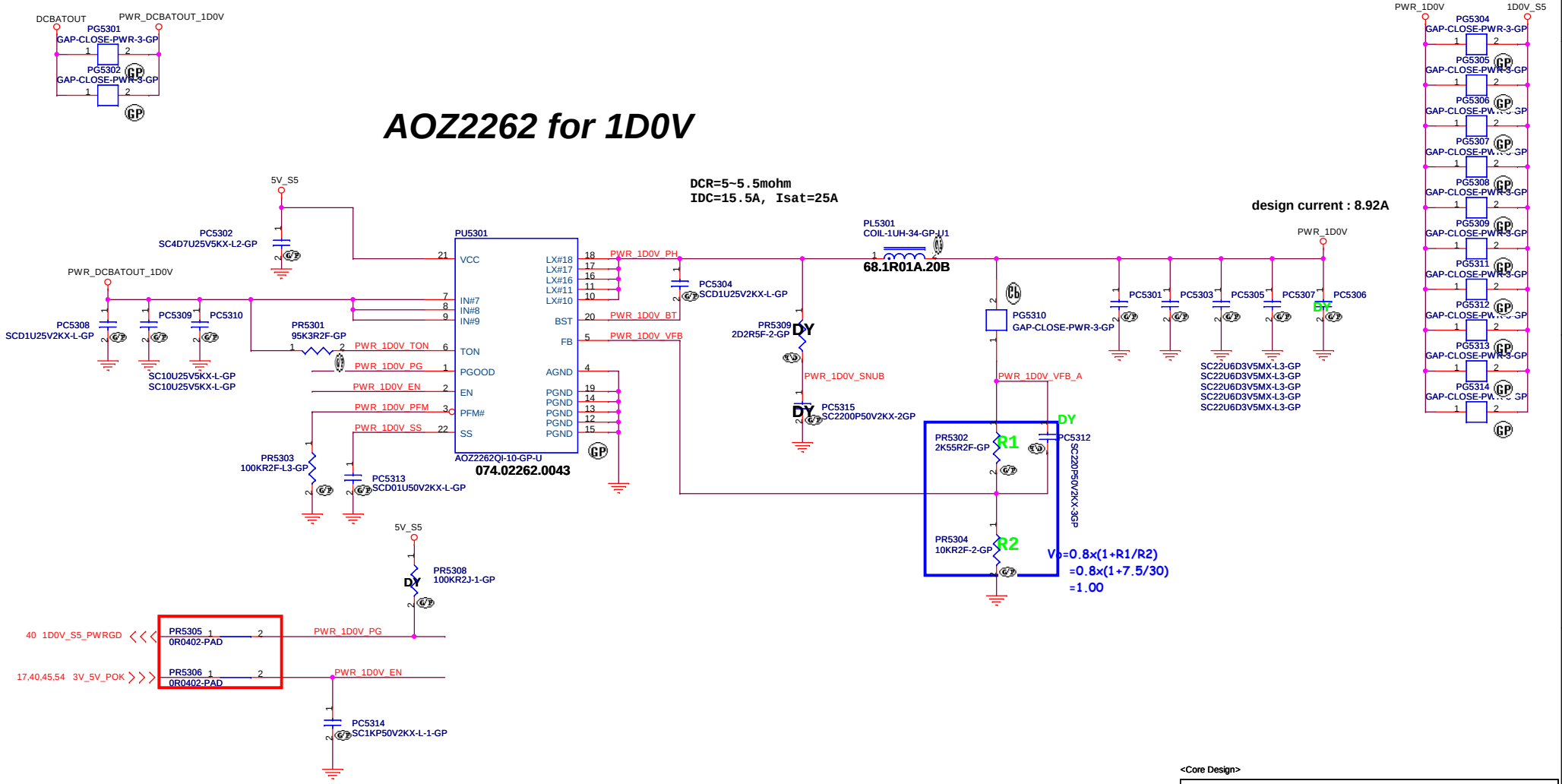
(Reserved)

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 52 of 105

SSID = PWR.Plane.Regulator_1p0v

AOZ2262 for 1D0V



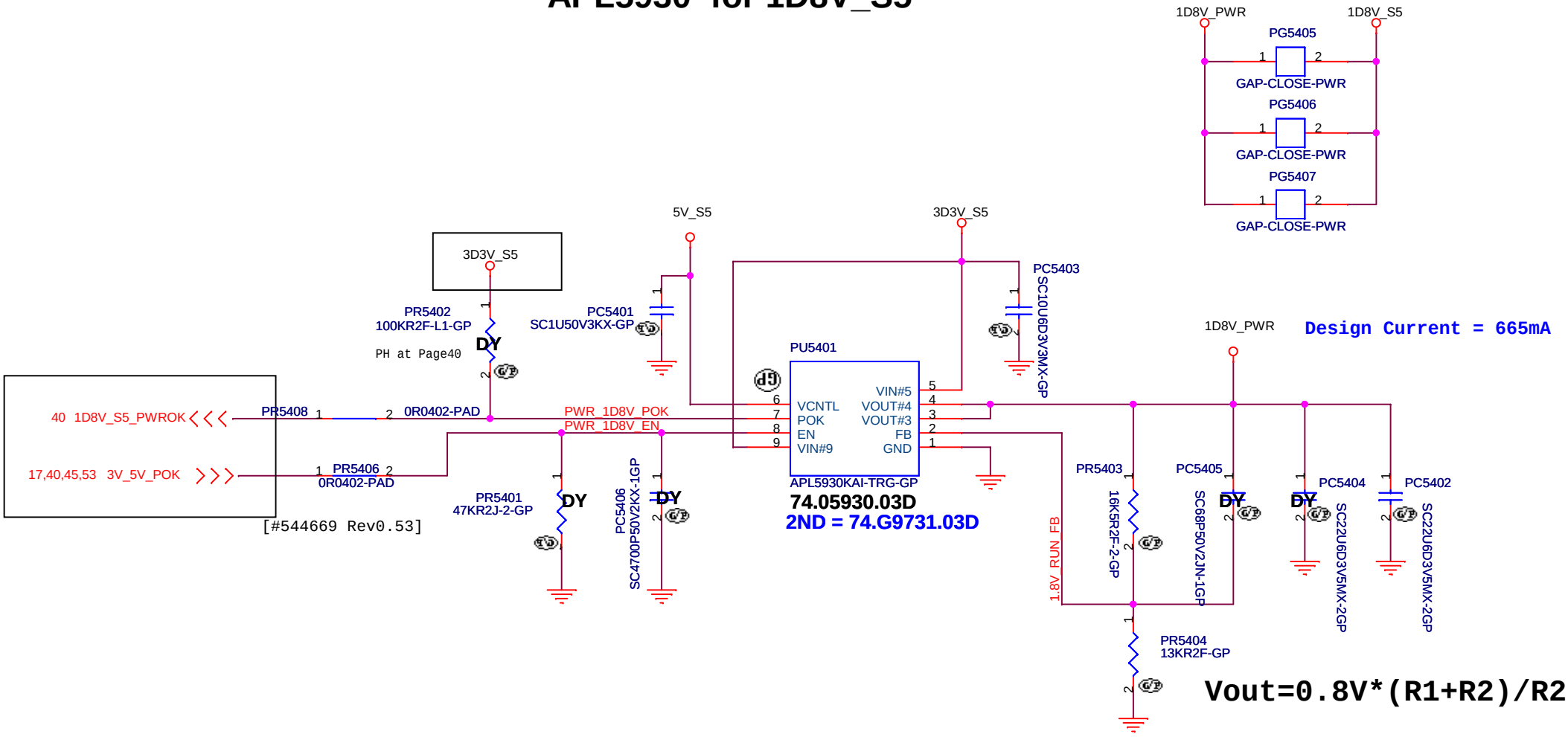
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AOZ2262QI_1D0V	
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 53 of 105	

Main Func = 1D8V

APL5930 for 1D8V_S5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LDO-V1D5V&V1D8V*		
Size: A4	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
Date: Monday, June 27, 2016	Sheet 54 of 105	

Main Func = LCD

LCD1
IPEX-CON40-3-GP
20.F1407.040
Trace width = 80mil
DCBATOUT_LCD
LCDVDD_LCD
C5538 SC1U10V2KX-3GP
C5536 SC1U10V4KX-GP
DBC_EN_R
EDP_HPD_CONN
LCD_TST_C
eDP_AUX_CON_P
eDP_AUX_CON_N
eDP_TX_CON_N0
eDP_TX_CON_P0
eDP_TX_CON_N1
eDP_TX_CON_P1
LCD_BRIGHTNESS
BLON_OUT_C
PANEL_SIZE_ID_CONN
MIC_GND
DMIC_CLK_EDP
DMIC_DATA_EDP
USB_CAMERA_PN4
USB_CAMERA_PP4
3D3V_CAMERA_S0
CAMERA_DET#_R
USB_CON_PN6
USB_CON_PP6
TP_RS
TP_RESET
TPAN_VDD

LCD
Camera
Touch Panel

INVERTER POWER

LCDVDD_LCD — R5523 0R5J-5-GP — LCDVDD

EE note: Never change R5211 to short pad after MP

DCBATOUT — F5503 POLYSW-1D1A24V-GP-U 800mA — DCBATOUT_LCD
69.50007.A31
C5535 DY SCD1U50V3KX-GP
C5515 SC1U50V2KX-GP

DBC_EN_R — R5518 100R2J-2-GP — DBC_PANEL_EN 20

CAMERA_DET#_R — R5501 0R0402-PAD — CAMERA_DET# 20

add for camera detect pin 1/25

3D3V_S0 — R5521 10KR2J-3-GP — PANEL_SIZE_ID_CONN — R5525 DY 100R2J-2-GP (PJ140815_david) — PANEL_SIZE_ID — PANEL_SIZE_ID 20
For ESD
For AUDIO Grade B or C selection.
R5526 0R2J-2-GP DY

PU/PD FOR AUX CHANNEL

SKL PDG (#543016):
Recommends having a pull-up resistor of 100 kΩ for AUXN
and a pull-down resistor of 100 kΩ for AUXP
between the AC capacitor and the connector,
to assist source detection by the sink device.

eDP_AUX_CON_P — R5528 DY 100KR2J-1-GP
eDP_AUX_CON_N — R5529 DY 100KR2J-1-GP — 3D3V_S0

Layout Note:
Colse to LCD1.

MIC_GND — R5531 0R0402-PAD

RN5502 SRN100KJ-5-GP: BKLT_CTRL, BLON_OUT_C, EDP_HPD
RN5503 SRN100J-4-GP: LCD_TST_C, LCD_BRIGHTNESS, BLON_OUT_C, EDP_HPD_CONN → LCD_TST_R 24, BLON_OUT 24, EDP_HPD 8, BKLT_CTRL

R5524 DY 0R2J-2-GP
D5503 BAT54C-7-F-3-GP — eDP_BKLT_CTRL — EC_BRIGHTNESS 24
75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D
EC (BIST MODE)

LCD_BRIGHTNESS — EC5504 DY SC22P50V2JN-4GP

8 eDP_TX_CPU_N0 — C5508 SCD1U16V2KX-3GP — C5532 SCD1U16V2KX-3GP — eDP_TX_CON_N0 / eDP_TX_CON_P0
8 eDP_TX_CPU_N1 — C5534 SCD1U16V2KX-3GP — C5537 SCD1U16V2KX-3GP — eDP_TX_CON_N1 / eDP_TX_CON_P1
8 eDP_AUX_CPU_N — C5533 SCD1U16V2KX-3GP — C5531 SCD1U16V2KX-3GP — eDP_AUX_CON_N / eDP_AUX_CON_P

Brightness
8 L_BKLT_CTRL — R5530 0R0402-PAD — eDP_BKLT_CTRL

3D3V_S0 — DY R5522 0R3J10-4-GP — 5V_S0 — R5527 0R0603-PAD
F5502 POLYSW-1D1A24V-GP-U
69.50007.A31
TPAN_VDD_F — R5520 0R3J-0-U-GP — TPAN_VDD
C5543 DY SCD2U10V3KX-1GP

EE note: Never change R5232 to short pad after MP
Reserved for one time fuse: 69.43001.201

LCDVDD

8 EDP_VDD_EN — D5502 BAT54C-7-F-3-GP — LCDVDD_EN
24 LCD_VCC_TEST_EN
75.00054.E7D
2nd = 83.R2003.W81
3rd = 75.00054.A7D
R5506 100KR2J-1-GP
LCDVDD
U5501 RT9724GB-GP (EN, GND, VOUT, VIN#5, VIN#4)
74.09724.09F
3D3V_S0 — C5505 SC4D7U6D3V3KX-GP

Layout Note:
Trace width = 80mil

Main Func = CAMERA

EE note: Never change R5229 to short pad after MP
Reserved for one time fuse: 69.43001.201

3D3V_S0 — R5532 0R5J-5-GP — 3D3V_CAMERA_S0
EC5503 DY SC33P50V2JN-3GP
C5539 SC4D7U6D3V3KX-GP

R5533 0R0402-PAD — USB_CAMERA_PN4 — USB_CPU_PN4 16
R5534 0R0402-PAD — USB_CAMERA_PP4 — USB_CPU_PP4 16

DMIC_DATA_EDP — R5502 0R0402-PAD — DMIC_DATA 27
DMIC_CLK_EDP — R5503 0R0402-PAD — DMIC_CLK 27
EC5501 DY SC68P50V2CN-1GP
EC5502 DY SC68P50V2CN-1GP

Layout Note: Reduce the stubs.

Main Func = Touch panel

Touch Panel

TP_RS — R5537 0R0402-PAD — TOUCH_PANEL_INTR# 4,24
C5541 DY SC10P50V2JN-4GP

TP_RESET — R5538 0R0402-PAD — PLT_RST# 17,24,31,40,61,68,76,91
C5540 DY SC10P50V2JN-4GP

USB_CON_PN6 — R5535 0R0402-PAD — USB_CPU_PN6 16

USB_CON_PP6 — R5536 0R0402-PAD — USB_CPU_PP6 16

ED5501 AZC099-04S-2-G (I/O1, GND, I/O2, I/O3, I/O4, VDD)
USB_CON_PN6 — USB_CON_PP6 — TPAN_VDD
C5501 DY SCD1U16V2KX-3GP
075.09904.0A7C

<Core Design>

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Title	LCD&CAM&DMC&Touch	
Size: Custom	Document Number: Vegas SKL/KBL-U	Rev: A00
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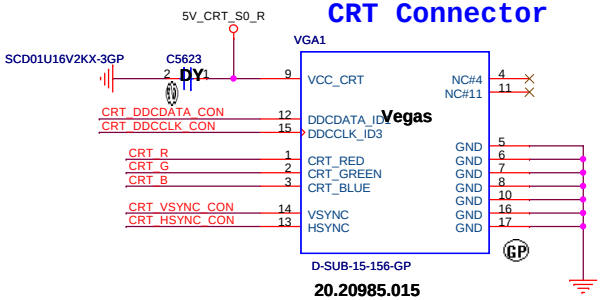
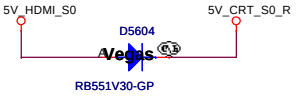
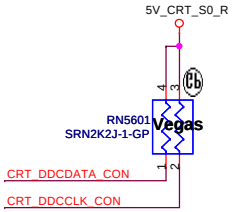
Main Func = CRT

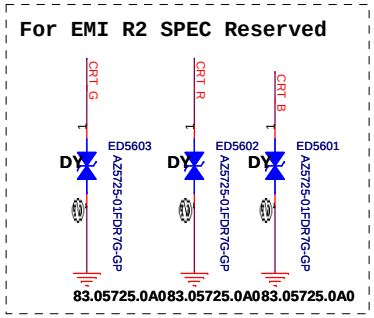
CRT Connector

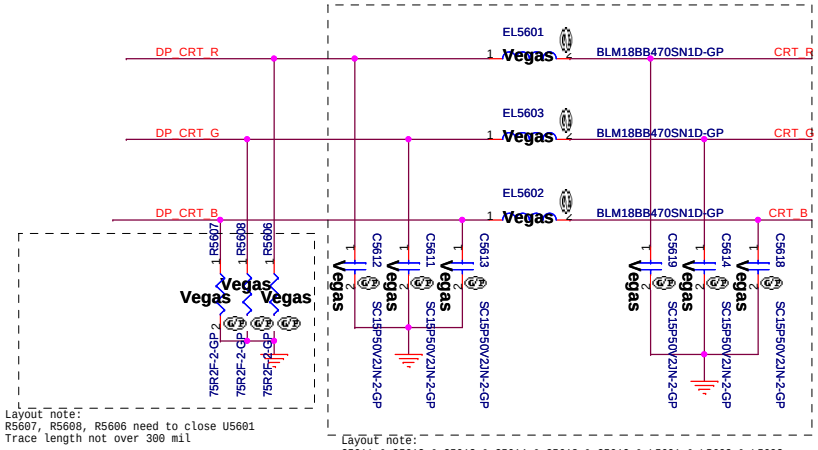


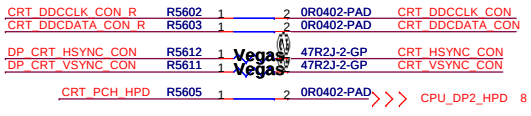
Change the VGA connect by Andy 1/14

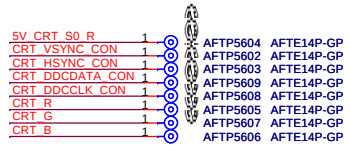


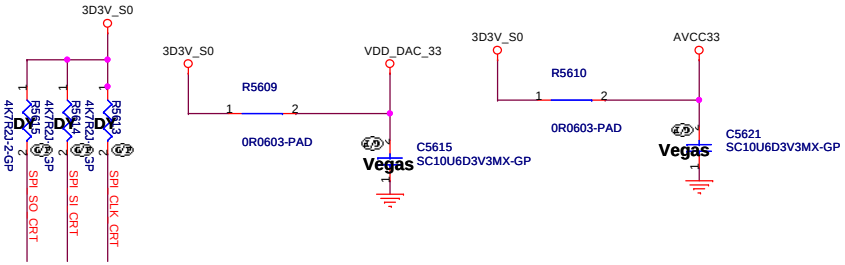


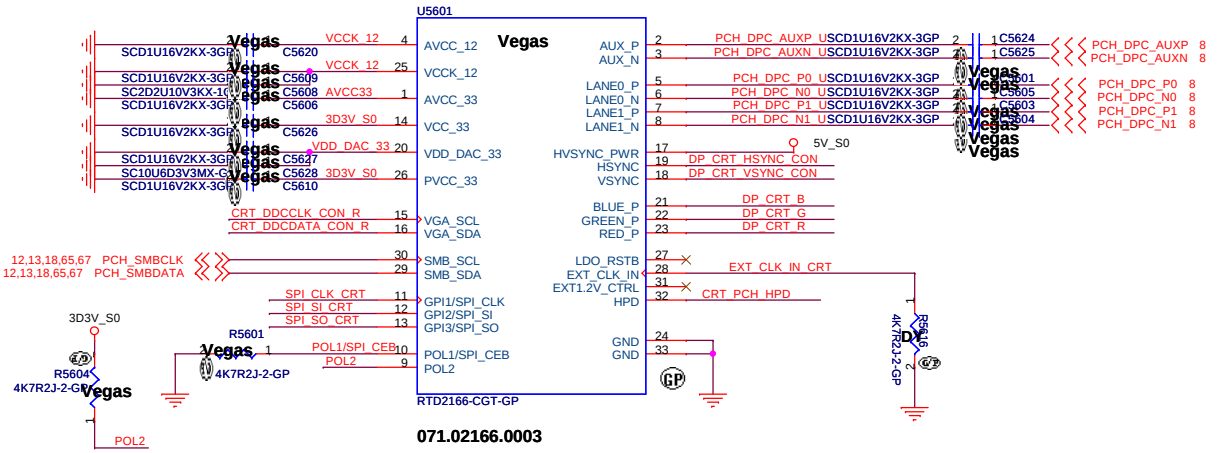


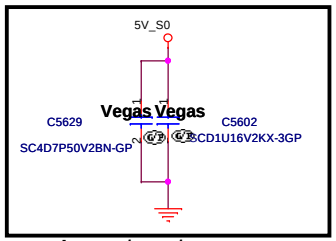


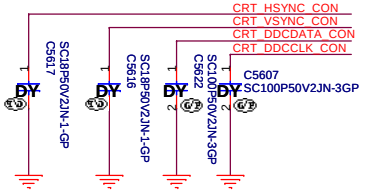












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Title: CRT		
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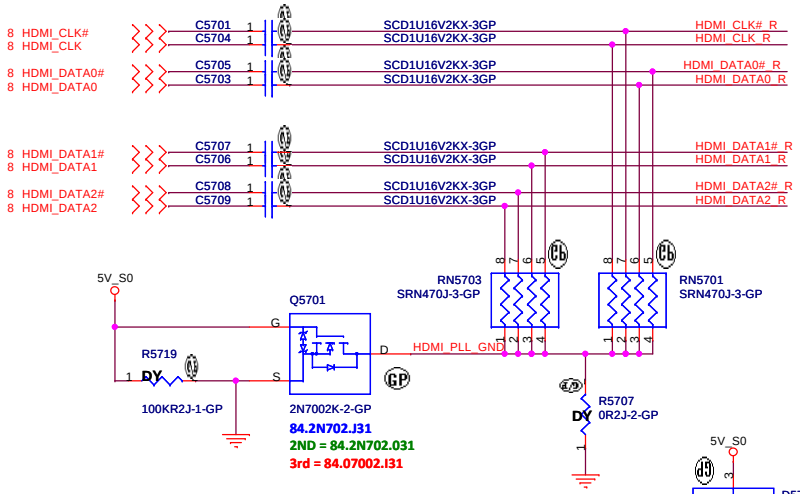
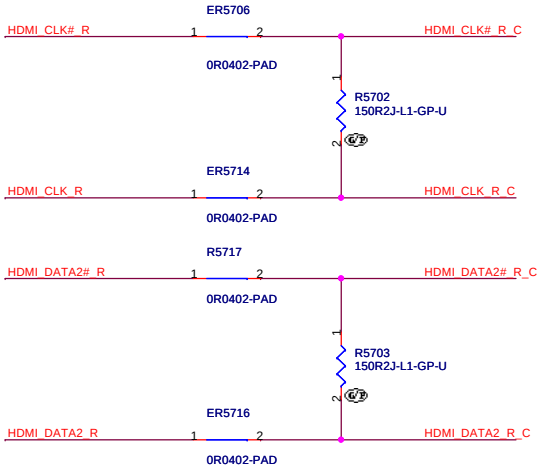
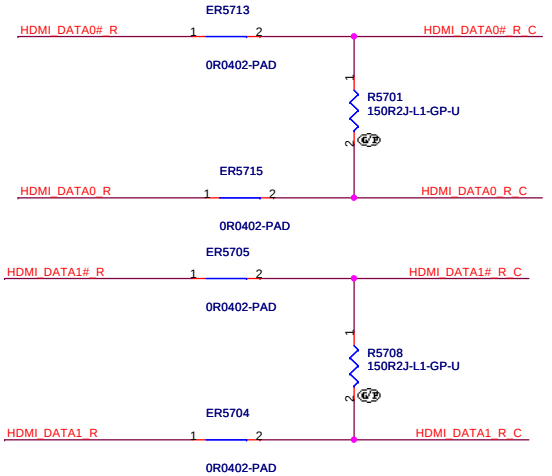
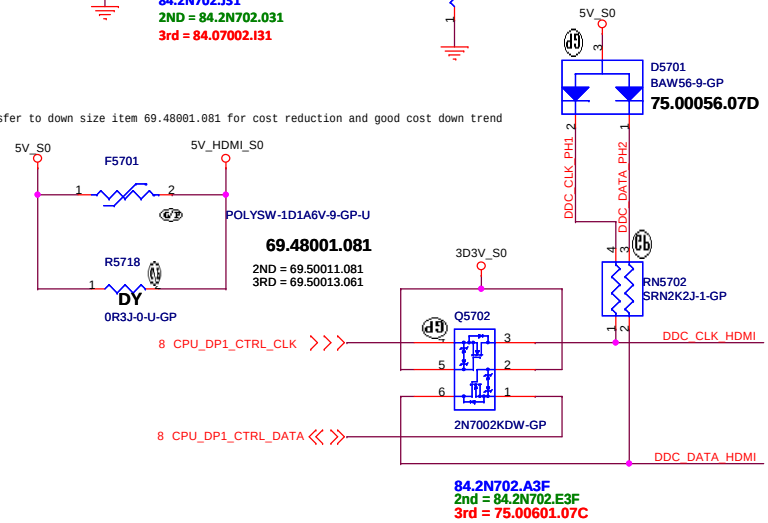
Main Func = HDMI

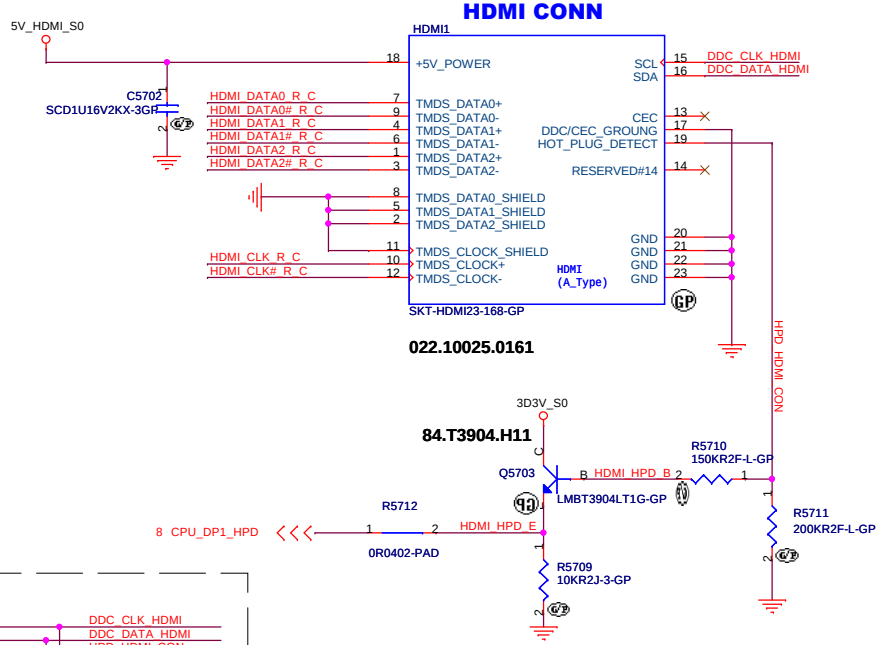


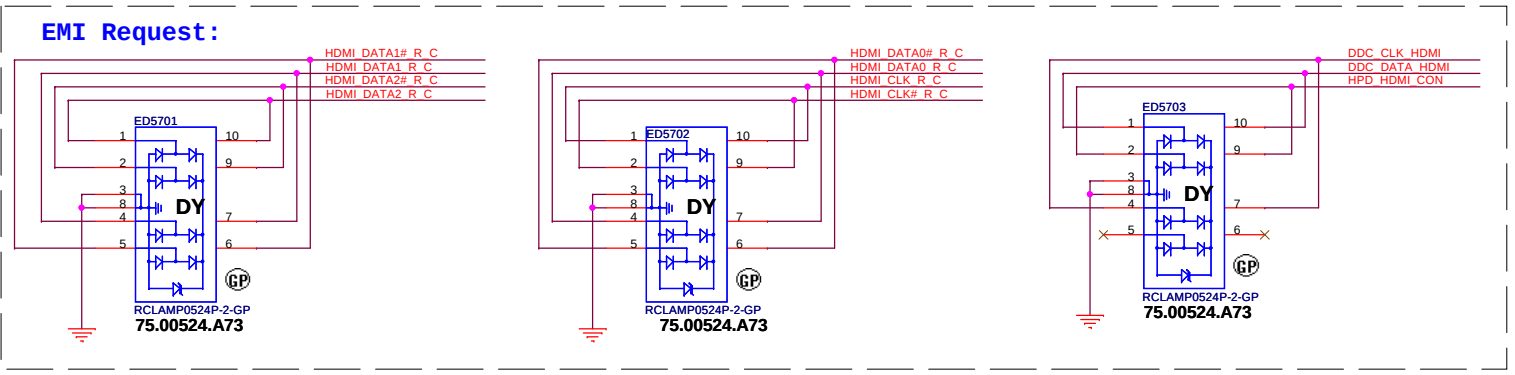




69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend







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Title	HDMI	
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Title
(Reserved)

Size	Document Number	Rev
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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Vegas SKL/KBL-U*	*A00*

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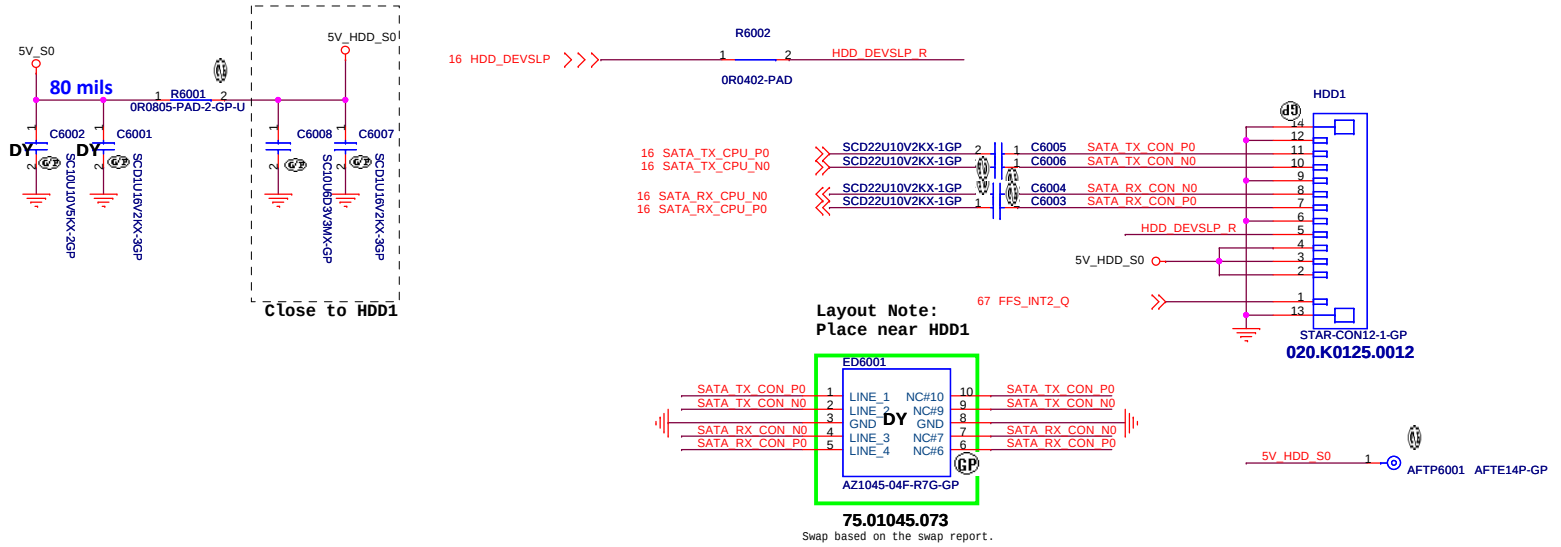
Main Func = HDD

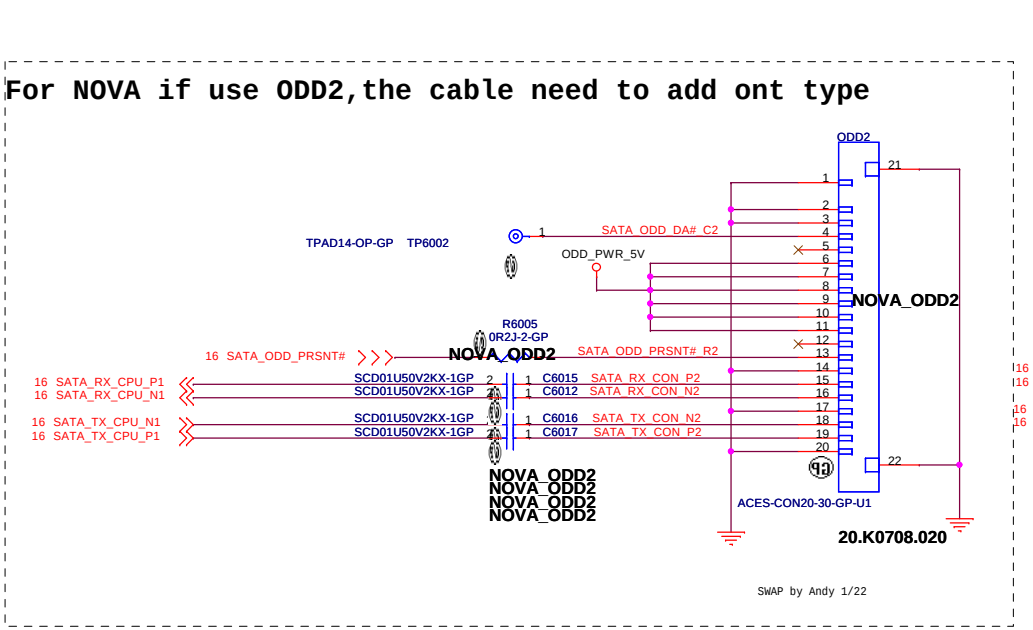
SATA HDD Connector

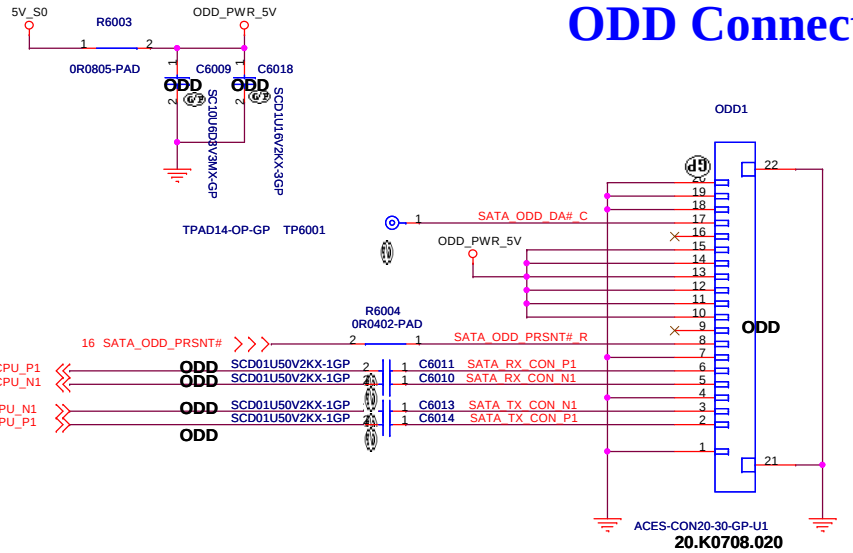


CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD Connector





<Core Design>

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Title: SATA IF_HDD/ODD

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

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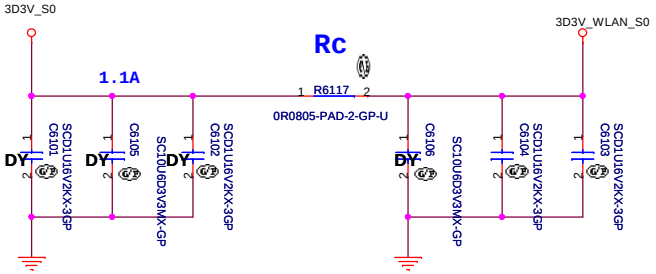
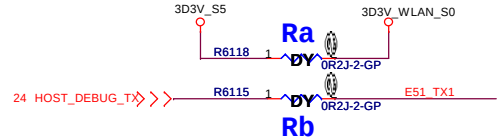
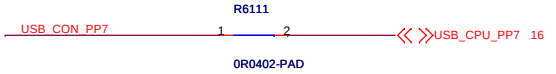
Main Func = WLAN

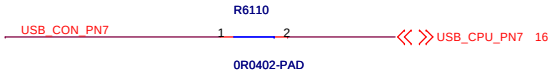


Reserved for NGFF Debug Card

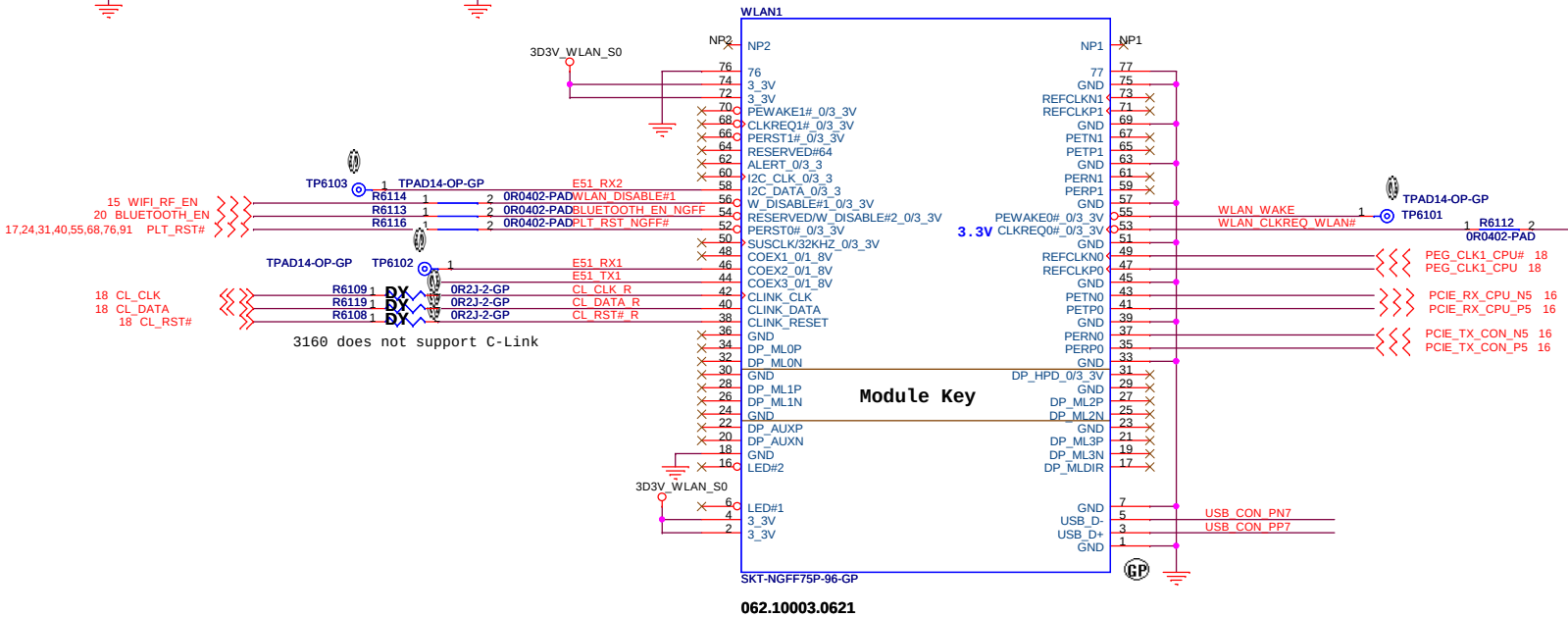


EE Note:
For NFGG Debug Card:
Stuff Ra, Rb; DY Rc.



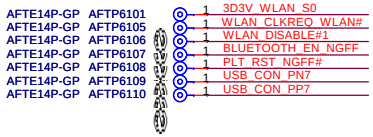


Note:pin 76 and pin 77 need contact to GND



062.10003.0621

Support: Intel Dual Band Wireless-AC 3160



<Core Design>

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Title: NGFF WLAN CONN
Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00
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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

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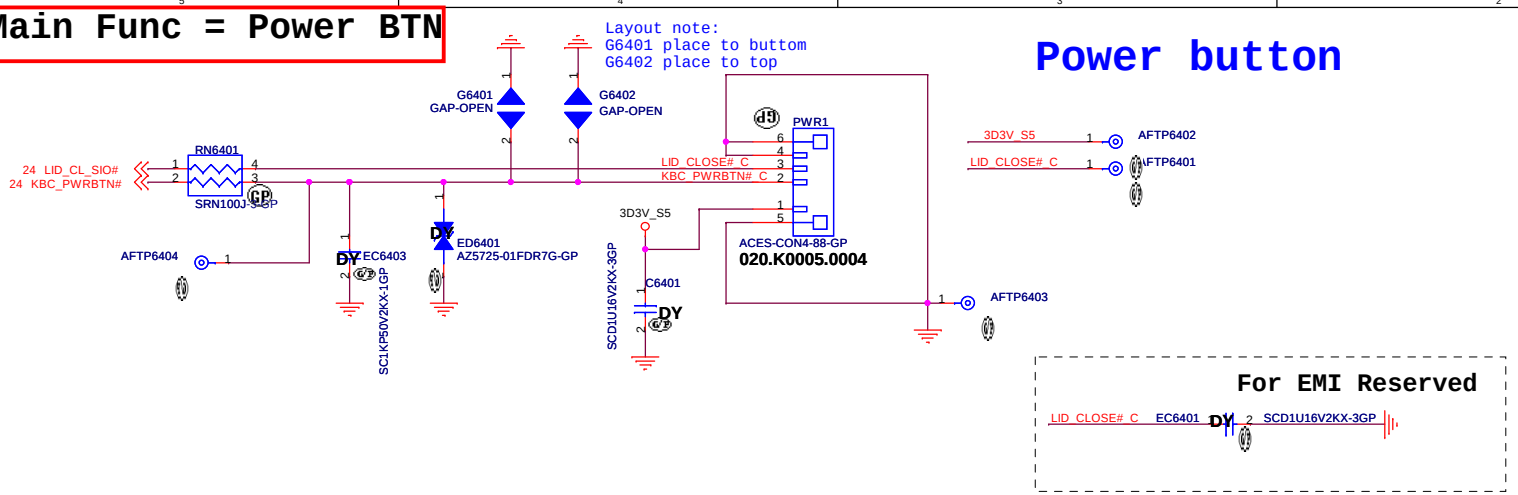
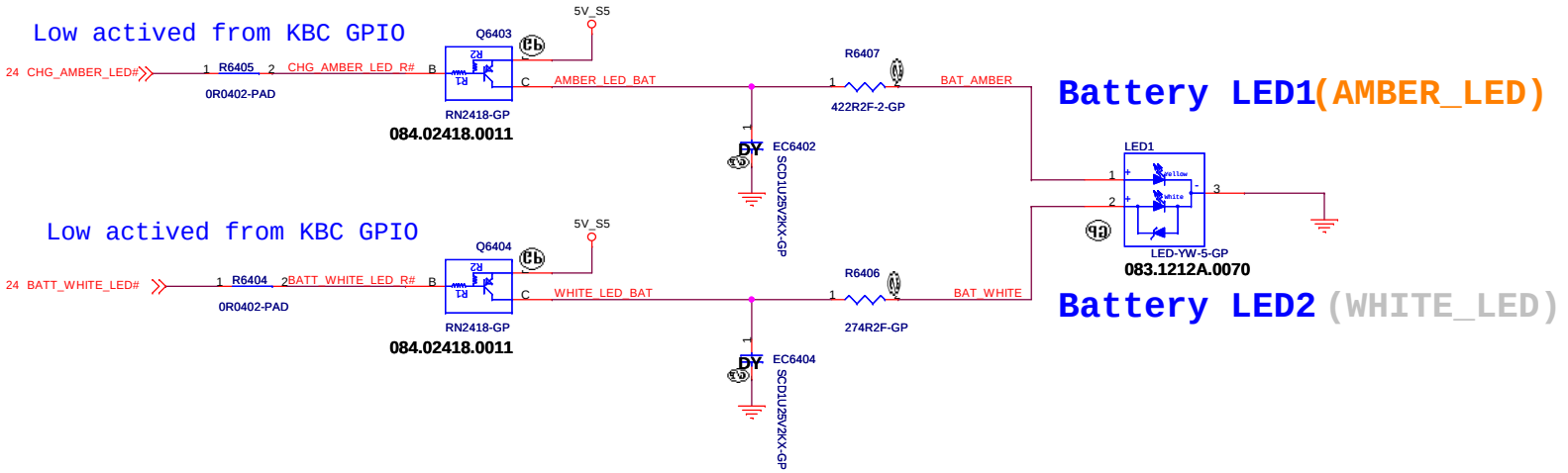
Main Func = Power BTN

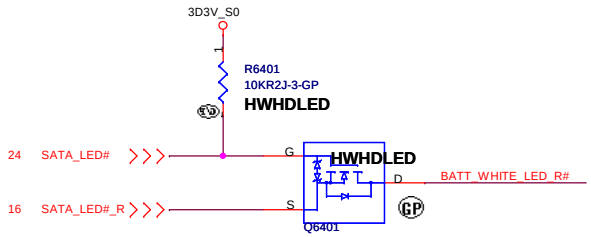


Main Func = Battery LED



Main Func = HDD LED

SATA HDD LED
LOW actived from PCH GPIO



<Core Design>

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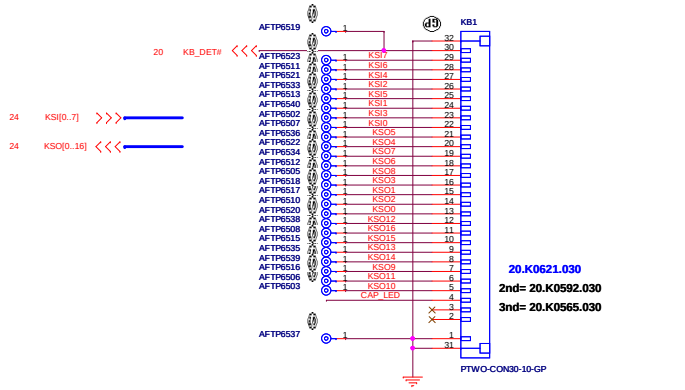
Title	LED Board&Power Button	
Size A3	Document Number Vegas SKL/KBL-U	Rev A00
Date: Monday, June 27, 2016	Sheet 64 of 105	

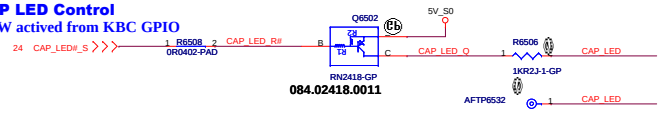
Main Func = KB

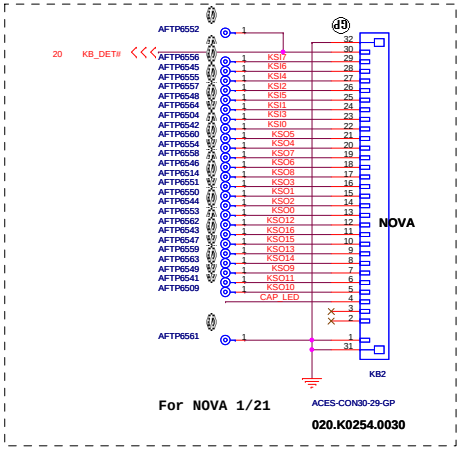
Internal Keyboard Connector



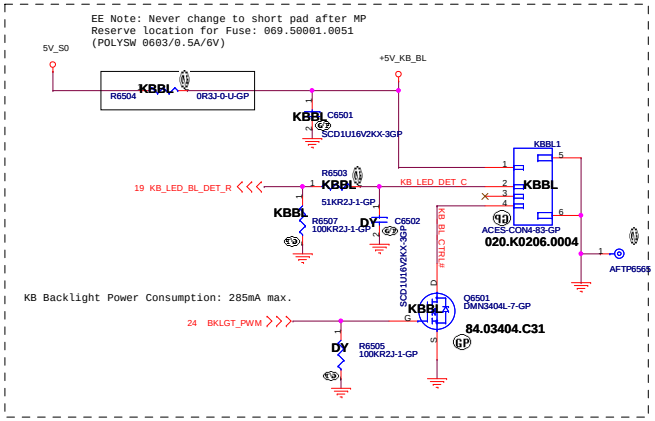
CAP LED Control

LOW actived from KBC GPIO





Keyboard Backlight (Reserved)

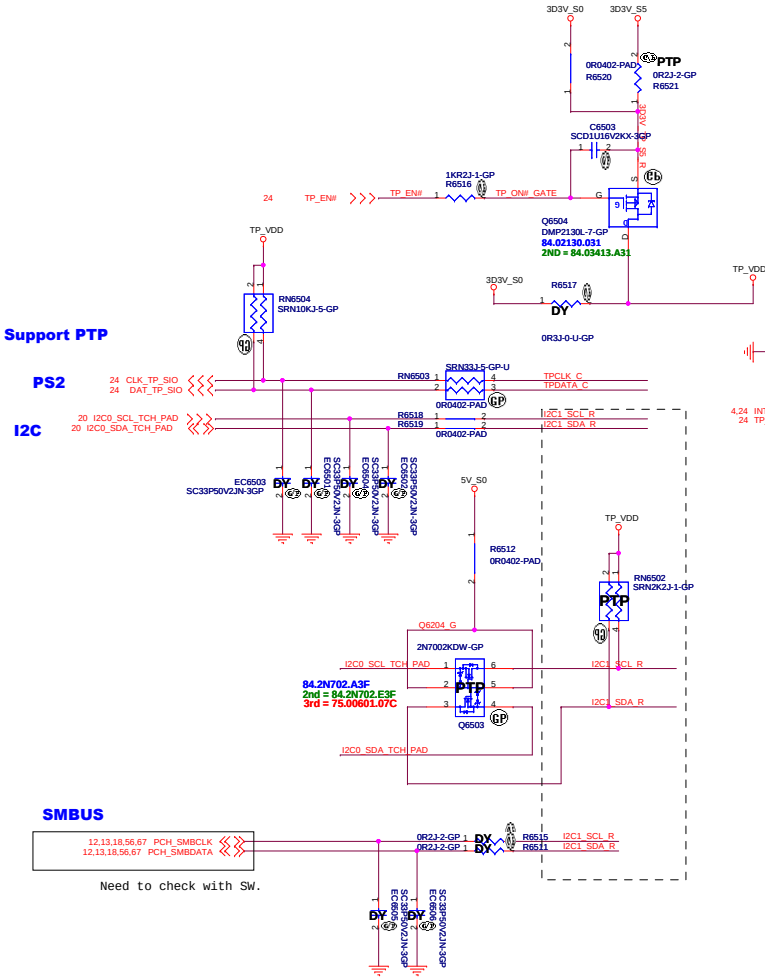


Main Func = TPAD

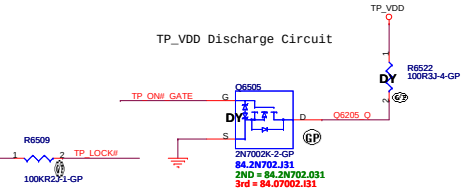
Support PTP

PS2

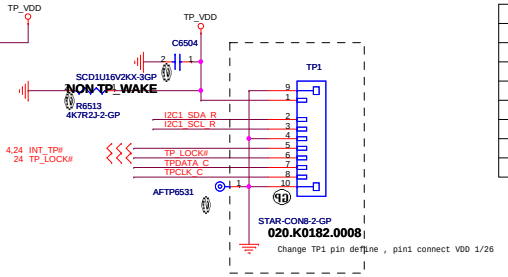
I2C



SMBUS

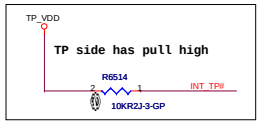


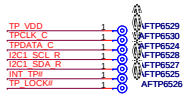
Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.





<Core Design>
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board&Touch Pad

Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

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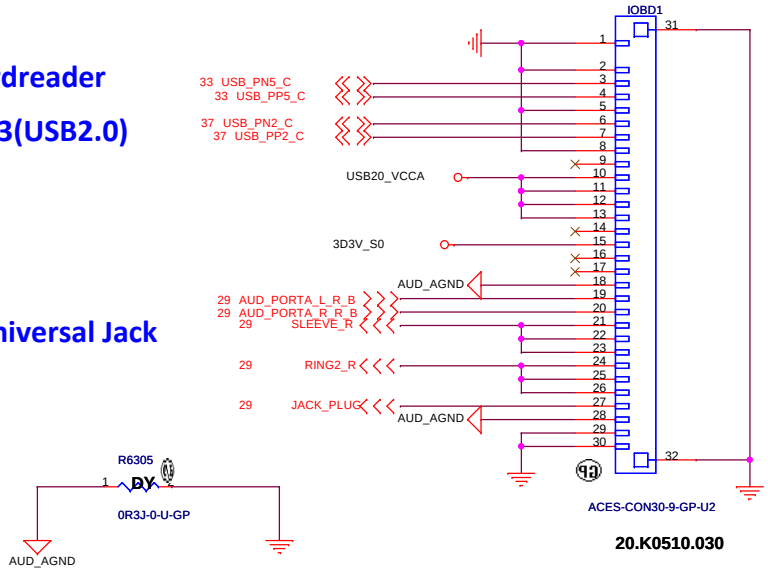
Main Func = IO Connector

I/O Board Connector

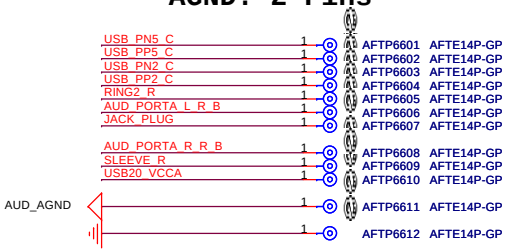
Cardreader

USB3(USB2.0)

Universal Jack



Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins



<Core Design>

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Title: *IO Board Connector*

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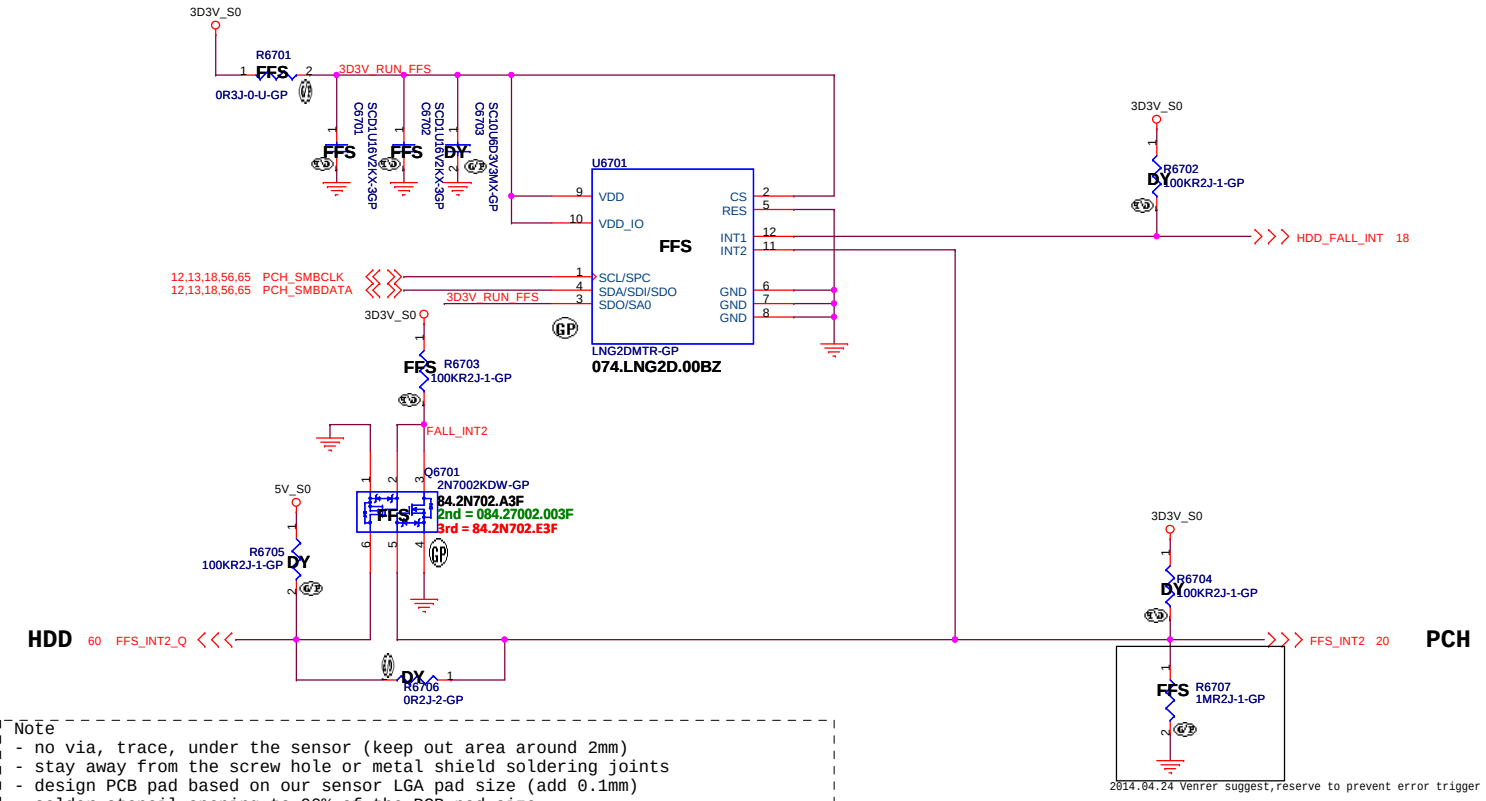
SSID = User.interface

Free Fall Sensor

DVT1 add FFS 2/18



Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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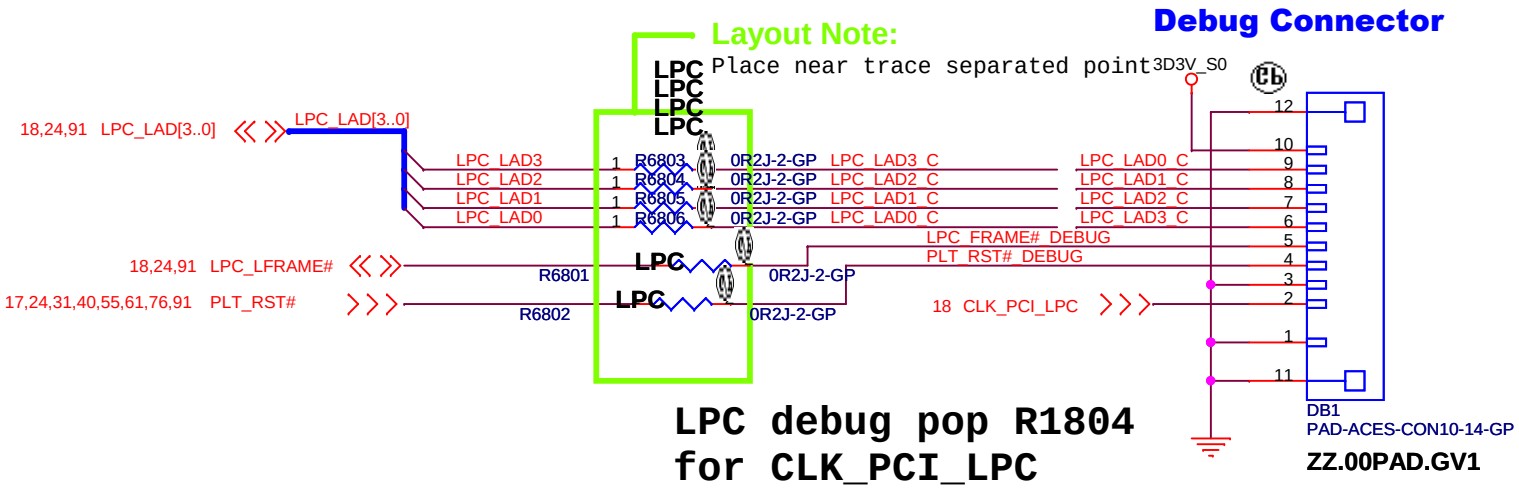
Title		
Free Fall Sensor		
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Monday, June 27, 2016	Sheet 67 of 105	

Main Func = Debug



LPC debug pop R1804 for CLK_PCI_LPC

20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Dubug connector*	
Size: A4	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
Date: Monday, June 27, 2016	Sheet 68 of 105	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 69 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Thursday, June 16, 2016 Sheet 70 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

(Blanking)

<Core Design>

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Title

USB3.0 PORT

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 72 of 105

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Thursday, June 16, 2016 Sheet 73 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Vegas SKL/KBL-U* | Rev: *A00*

Date: Thursday, June 16, 2016 | Sheet 74 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Vegas SKL/KBL-U*	*A00*

Main Func = dGPU

GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω

GPU1A 1 OF 7

16 PEG_TX_GPU_P0	AF30 PCIE_RX0P	PCIE_TX0P AH30	PEG_RX_GPU_P0 C7601 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_P0 16
16 PEG_TX_GPU_N0	AE31 PCIE_RX0N	PCIE_TX0N AG31	PEG_RX_GPU_N0 C7602 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_N0 16
16 PEG_TX_GPU_P1	AE29 PCIE_RX1P	PCIE_TX1P AG29	PEG_RX_GPU_P1 C7603 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_P1 16
16 PEG_TX_GPU_N1	AD28 PCIE_RX1N	PCIE_TX1N AF28	PEG_RX_GPU_N1 C7604 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_N1 16
16 PEG_TX_GPU_P2	AD30 PCIE_RX2P	PCIE_TX2P AF27	PEG_RX_GPU_P2 C7605 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_P2 16
16 PEG_TX_GPU_N2	AC31 PCIE_RX2N	PCIE_TX2N AF26	PEG_RX_GPU_N2 C7606 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_N2 16
16 PEG_TX_GPU_P3	AC29 PCIE_RX3P	PCIE_TX3P AD27	PEG_RX_GPU_P3 C7607 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_P3 16
16 PEG_TX_GPU_N3	AB28 PCIE_RX3N	PCIE_TX3N AD26	PEG_RX_GPU_N3 C7608 1	GEN2/GEN3 SCD1U16V2KX-3GP	PEG_RX_CPU_N3 16

	AB30 PCIE_RX4P	PCIE_TX4P AC25	
	AA31 PCIE_RX4N	PCIE_TX4N AB25	
	AA29 PCIE_RX5P	PCIE_TX5P Y23	
	Y28 PCIE_RX5N	PCIE_TX5N Y24	
	Y30 PCIE_RX6P	PCIE_TX6P AB27	
	W31 PCIE_RX6N	PCIE_TX6N AB26	
	W29 PCIE_RX7P	PCIE_TX7P Y27	
	V28 PCIE_RX7N	PCIE_TX7N Y26	
	V30 NC#V30	NC#W24 W24	
	U31 NC#U31	NC#W23 W23	
	U29 NC#U29	NC#V27 V27	
	T28 NC#T28	NC#U26 U26	
	T30 NC#T30	NC#U24 U24	
	R31 NC#R31	NC#U23 U23	
	R29 NC#R29	NC#T26 T26	
	P28 NC#P28	NC#T27 T27	
	P30 NC#P30	NC#T24 T24	
	N31 NC#N31	NC#T23 T23	
	N29 NC#N29	NC#P27 P27	
	M28 NC#M28	NC#P26 P26	
	M30 NC#M30	NC#P24 P24	
	L31 NC#L31	NC#P23 P23	
	L29 NC#L29	NC#M27 M27	
	K30 NC#K30	NC#N26 N26	

PCI EXPRESS INTERFACE

Table 3–5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

DGPU_HOLD_RST#	
H	dGPU mode
L	IGPU
H	IGPU with BACO

3D3V_VGA_S0

R7625 10KR2J-3-GP DY

20 DGPU_HOLD_RST#

R7623 0R0402-PAD

D7601 BAW56-5-GP DY

17,24,31,40,55,61,68,91 PLT_RST#

ATI_RST#

R7601 OPS 1KR2F-3-GP PWRGOOD_TEST N10 TEST_PG

R7621 0R0402-PAD VGA_RST# AL27 PERST#

C7609 SC47P50V2JN-3GP DY

18 PEG_CLK_CPU AK30 PCIE_REFCLKP
18 PEG_CLK_CPU# AK32 PCIE_REFCLKN
CLOCK

CALIBRATION
PCIE_CALR_TX Y22
PCIE_CALR_RX AA22

PCIE_CALR_TX 1K69R2F-2-GP OPS R7622 0D95V_VGA_S0
PCIE_CALR_RX 1KR2F-3-GP OPS R7618

JET-XT-S3-GP

OPS

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 076_GPU(1/5) PEG
Size | Project Name: <Project Name> | Rev
Date: Monday, June 27, 2016 Sheet 76 of 105

Main Func = dGPU

1.8V and 0.95V for Clock resource

GPU1E — 5 OF 7 — JET-XT-S3-GP

GPU1F — 6 OF 7 — JET-XT-S3-GP

GPU1G — 7 OF 7 — JET-XT-S3-GP

1D8V_VGA_S0 — R7704 — 0R0603-PAD-2-GP-U — DPLL_PVDD — 40mA

0D95V_VGA_S0 — R7705 — 0R0603-PAD-2-GP-U — DPLL_VDDC — 32mA

C7713 SC10U6D3V3MX-GP (DY)

C7711 SC1U10V2KX-1GP (OPS)

C7710 SCD1U16V2KX-3GP (OPS)

C7715 SC1U10V2KX-1GP (OPS)

C7714 SCD1U16V2KX-3GP (OPS)

BALL: AB11, AB12
R16 : NC
MESO : VDDC

VSS_MECH1 — P7701
VSS_MECH2 — P7702
VSS_MECH3 — TP7703

OPS

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

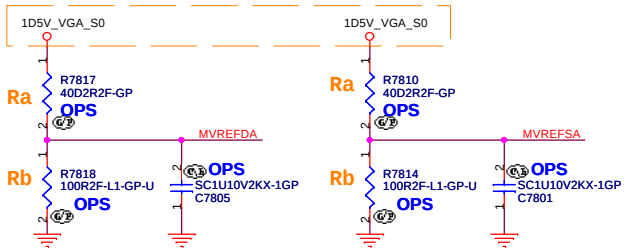
Title	077_GPU (2/5) DIGITALOUT	
Size	Project Name: Vegas SKL/KBL-U	Rev: X00
Date: Friday, June 24, 2016	Sheet 77 of 105	

Main Func = dGPU

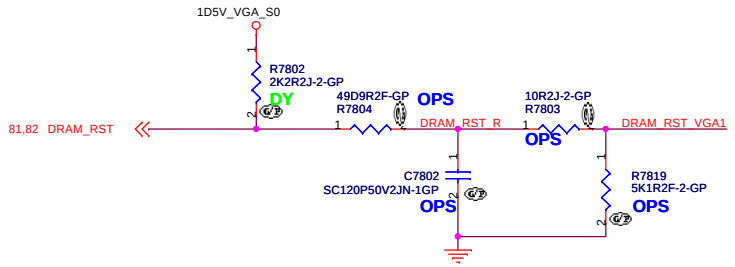
Please MVREF drivers and Caps close to ASIC

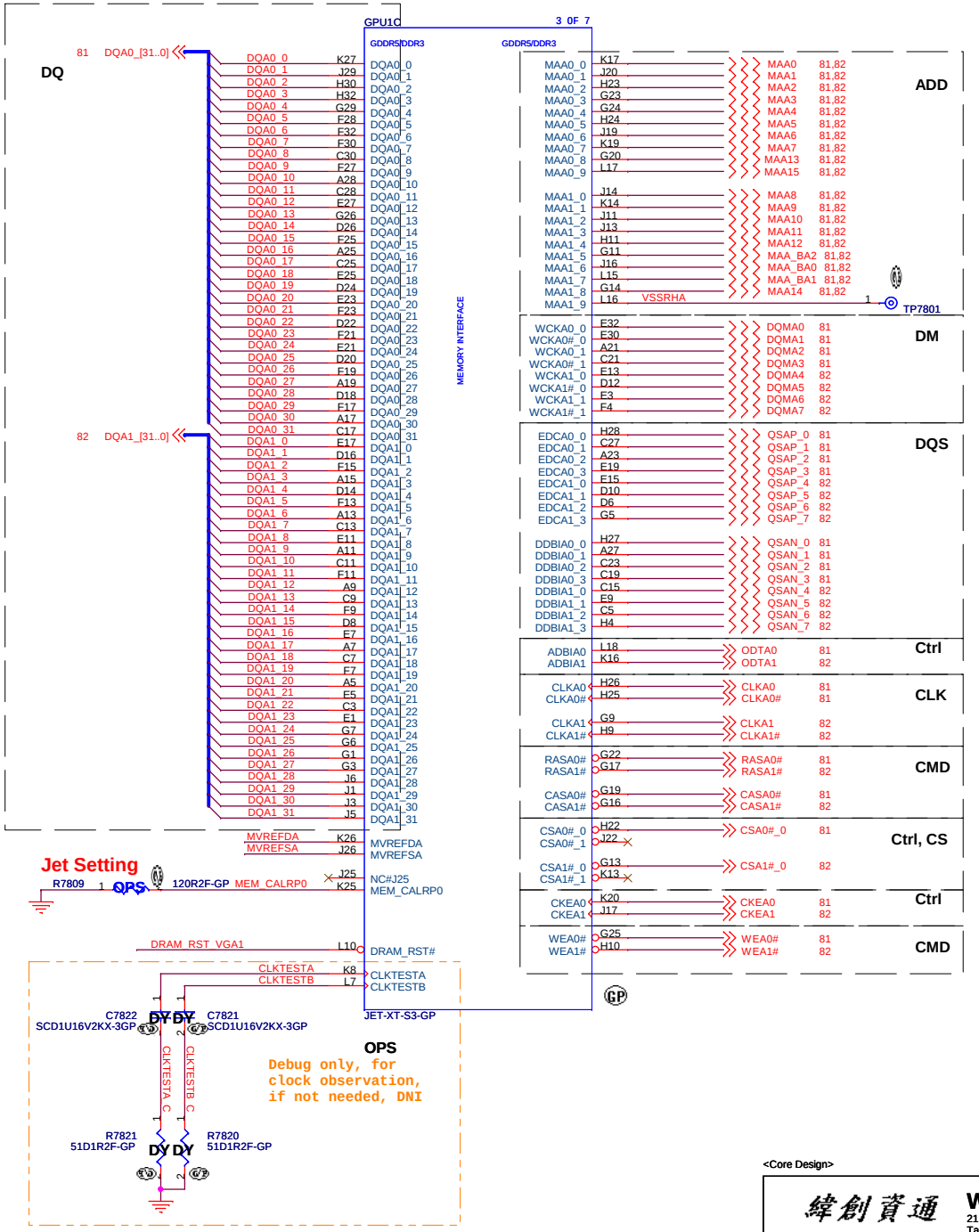
DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R



Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5





<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 078_GPU (3/5) VRAM I/F

Size | Project Name: Vegas SKL/KBL-U | Rev

Date: Monday, June 27, 2016 Sheet 78 of 105

Main Func = dGPU

Pre-PWROK METAL VID CODES

	SVC	SVD	Output Voltage
	0	0	1.1
	0	1	1.0
AMD suggestion	1	0	0.9
	1	1	0.8

Table 8. Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

	SVID	PWR Sequencing
R16	R7919 R7920	PR8611 PC8607 / PR8612 PC8612

R16: DY
MESO : 上件

BALL: U10,T10,Y9,W10
R16: NC
MESO : VDDC

BALL: AB13, W9, AC14
R16: NC
MESO : VDDC

0: Enable MLPS, disable GPIO PINSTRAP
1: Disable MLPS, enable GPIO PINSTRAP

PINs for debug

PS_0	R_pu	R_pd	Bits[3:1]	Size of the Prima
	NC	4750	000	128 MB
	8450	2000	001	256 MB
	4530	2000	010	64 MB
	6980	4990	011	Reserved
	4530	4990	100	N/A
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

AMD suggest Aperture Size = 256MB

11001

11000

11000

PS_1	R_pu	R_pd	Bits[3:1]	
	NC	4750	000	PCIe GEN3 is not supported ; The CLKREQB power management capability is disabled
	8450	2000	001	PCIe GEN3 is supported ; The CLKREQB power management capability is disabled
	4530	2000	010	PCIe GEN3 is not supported ; The CLKREQB power management capability is enabled
	6980	4990	011	PCIe GEN3 is supported ; The CLKREQB power management capability is enabled
	4530	4990	100	N/A
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

PS_2	R_pu	R_pd	Bits[3:1]	
	NC	4750	000	Disable the external BIOS ROM device.
	8450	2000	001	N/A
	4530	2000	010	N/A
	6980	4990	011	N/A
	4530	4990	100	Enable the external BIOS ROM device.
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

MLPS Memory ID setting:

BOARD_CONFIG[2:0]		Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor P/N	SMT quantity	R_pu	R_pd
ID	[2:0]								
0	000	Samsung - DDR3L	256M x 16		2GB	K4W4G1646E-BC1A	4 pcs	NC	4750
1	001	Micron - DDR3L	256M x 16		2GB	MT41J256M16LY-091G:N	4 pcs	8450	2000
2	010	SK hynix - DDR3L	256M x 16		2GB	H5TC4G63EFR-N0C	4 pcs	4530	2000
3	011								
4	100								
5	101								
6	110								
7	111								

GPU thermal sensor

Layout Note:
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Resistor	
4.75Kohm:	PN/64.47515.6DL
8.45Kohm:	PN/64.84515.6DL
2Kohm:	PN/64.20015.6DL
4.53Kohm:	PN/64.45315.6DL
6.98Kohm:	PN/64.69815.6DL
4.99Kohm:	PN/64.49915.6DL
3.24Kohm:	PN/64.32415.6DL
3.4Kohm:	PN/64.34015.6DL
5.62Kohm:	PN/64.56215.6DL
10Kohm:	PN/64.10025.6DL

Capacitor	
680nF:	PN/78.68421.5BL
82nF:	PN/78.82321.2FL
10nF:	PN/78.10324.L0L

Note :
C7501 and C7503 values determine CL value of the oscillation circuit.
If Negative Resistance is too low, that may cause crystal resonator stop oscillation or not easy to oscillate.
If Drive Level is too high, that may cause crystal resonator abnormal oscillation or damaged the main body of quartz.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 079_GPU (4/5) GPIO/STRAP
Size: | Project Name: Vegas SKL/KBL-U | Rev:
Date: Monday, June 27, 2016 | Sheet 79 of 105

Main Func = dGPU

AMD schematic Review need
10uF x 1, 2.2uFx5, 0.1uF x1, 0.01uF x1

1D5V_VGA_S0
C8001 SC10U6D3V3MX-GP OPS
C8003 SC1U10V2KX-1GP OPS
C8009 SC1U10V2KX-1GP DY
C8004 SC1U10V2KX-1GP OPS
1A

1D5V_VGA_S0
C8042 SC1U10V2KX-1GP DY
C8005 SC1U10V2KX-1GP DY
C8006 SC1U10V2KX-1GP DY
C8014 SCD01U50V2KX-1GP DY
SCD1U16V2KX-3GP C8007 DY

C8034 SC1U10V2KX-1GP OPS
C8031 SC1U10V2KX-1GP DY
C8032 SC1U10V2KX-1GP DY
C8033 SC1U10V2KX-1GP DY

1D8V_VGA_S0
C8017 SC1U10V2KX-1GP OPS
13mA

3D3V_VGA_S0
C8024 SC1U10V2KX-1GP OPS
25mA

Memory phase lock loop power: Dedicated analogue power in for memory PLLs

1D8V_VGA_S0
L8001 MMZ1005S241C-GP OPS
MPV18
C8043 SC10U6D3V3MX-GP OPS
C8044 SC10U6D3V3MX-GP OPS
C8045 SC1U10V2KX-1GP OPS

Engine phase loop power: Dedicated analogue power pin for engine PLL

1D8V_VGA_S0
L8002 BLM15BD121SN1D-GP OPS
SPV18
C8053 SC10U6D3V3MX-GP OPS
C8054 SC1U10V2KX-1GP OPS

Engine phase loop power: Dedicated digital power pin for engine PLL

0D95V_VGA_S0
L8003 BLM15BD121SN1D-GP OPS
SPV10
C8055 SC1U10V2KX-1GP OPS
SCD1U16V2KX-3GP C8056 OPS

GPU1D 4 OF 7
JET-XT-S3-GP

MEM I/O: H13 H16 H19 J10 J23 J24 J9 K10 K23 K24 K9 L11 L12 L13 L20 L21 L22 VDDR1
LEVEL TRANSLATION: AA20 AA21 AB20 AB21 VDD_CT
I/O: AA17 AA18 AB17 AB18 VDDR3; V12 Y12 U12 NC_VDDR4#V12 NC_VDDR4#Y12 NC_VDDR4#U12
PLL: MPV18 90mA L8 MPLL_PVDD; SPV18 75mA H7 SPLL_PVDD; SPV10 100mA H8 SPLL_VDDC; J7 SPLL_PVSS
PCIE: AM30 PCIE_PVDD; NC#AB23 NC#AC23 NC#AD24 NC#AE24 NC#AE25 NC#AE26 NC#AF25 NC#AG26; L23 L24 L25 L26 M22 N22 N23 N24 R22 T22 U22 V22 PCIE_VDDC
CORE: AA15 N15 N17 R13 R16 R18 Y21 T12 T15 T17 T20 U13 U16 U18 V21 V15 V17 V20 Y13 Y16 Y18 AA12 M11 N12 U11 VDDC
POWER: R21 U21 BIF_VDDC
ISOLATED CORE I/O: M13 M15 M16 M17 M18 M20 M21 N20 VDDCI

0.1A
1D8V_VGA_S0
C8008 SC1U10V2KX-1GP DY
C8002 SC10U6D3V3MX-GP OPS

0D95V_VGA_S0
C8010 SC10U6D3V3MX-GP DY
C8016 SC10U6D3V3MX-GP OPS

2.5A
AMD schematic Review need 10uF x 2, 1uFx3, 0.1uF x2
0D95V_VGA_S0
C8011 SCD1U16V2KX-3GP OPS
C8012 SCD1U16V2KX-3GP OPS
C8013 SC1U10V2KX-1GP OPS
C8015 SC1U10V2KX-1GP OPS
C8057 SC1U10V2KX-1GP OPS

AMD ORB 10U x 6 2.2U x 16
LF145M 4.7U x 6 1U x 20
VGA_CORE
C8018 SC1U10V2KX-1GP OPS
C8019 SC1U10V2KX-1GP OPS
C8020 SC1U10V2KX-1GP OPS
C8021 SC1U10V2KX-1GP OPS
C8022 SC1U10V2KX-1GP OPS
C8023 SC1U10V2KX-1GP OPS

NC on JET
AB13 U10 W9 Y9 W10 T10 AC14 AB12 AB11 AC11 AC13
VGA_CORE
C8025 SC1U10V2KX-1GP OPS
C8026 SC1U10V2KX-1GP OPS
C8027 SC1U10V2KX-1GP OPS
C8028 SC1U10V2KX-1GP OPS
C8029 SC1U10V2KX-1GP OPS
C8030 SC1U10V2KX-1GP OPS

VGA_CORE
C8035 SC1U10V2KX-1GP OPS
C8036 SC1U10V2KX-1GP OPS
C8037 SC1U10V2KX-1GP OPS
C8058 SC1U10V2KX-1GP OPS
C8059 SC1U10V2KX-1GP OPS
C8060 SC1U10V2KX-1GP OPS

1.4A
0D95V_VGA_S0
C8065 SC1U10V2KX-1GP OPS

VGA_CORE
C8066 SC22U6D3V3MX-1-GP OPS
C8061 SC1U10V2KX-1GP OPS
C8062 SC1U10V2KX-1GP OPS

5A
AMD ORB 10U x 2 1U x 3 0.1U x2
LF145M 4.7U x 2 1U x 3 0.1U x 2
VGA_CORE
C8046 SCD1U16V2KX-3GP OPS
C8047 SCD1U16V2KX-3GP OPS
C8048 SC1U10V2KX-1GP OPS
C8049 SC1U10V2KX-1GP OPS
C8050 SC1U10V2KX-1GP OPS

VGA_CORE
C8051 SC4D7U6D3V3KX-GP OPS
C8052 SC4D7U6D3V3KX-GP OPS

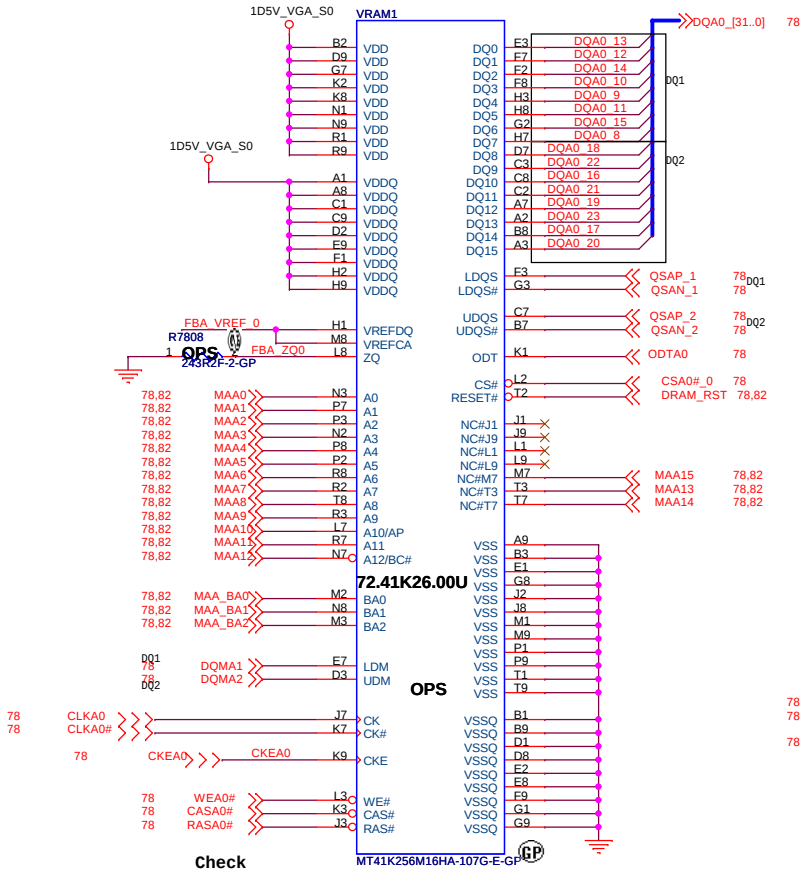
VGA_CORE
C8040 SC10U6D3V3MX-GP OPS
C8041 SC10U6D3V3MX-GP OPS
C8063 SC10U6D3V3MX-GP OPS
C8064 SC10U6D3V3MX-GP OPS
C8038 SC10U6D3V3MX-GP OPS
C8039 SC10U6D3V3MX-GP OPS

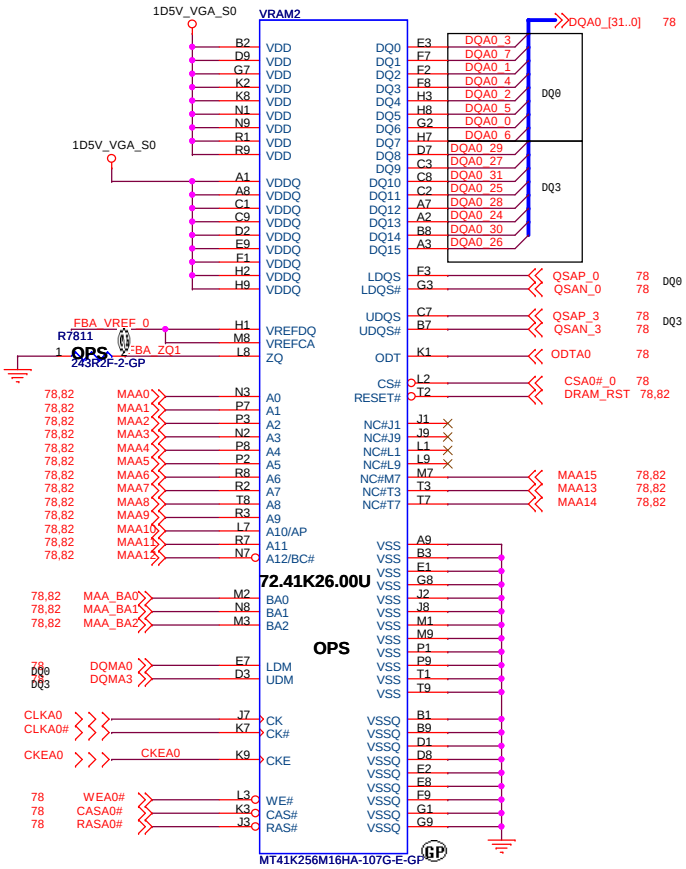
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

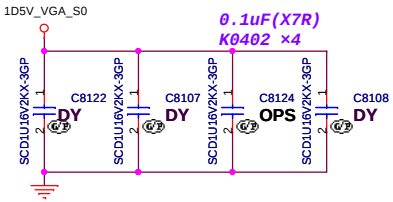
Title: 080_GPU (5/5) PWR/GND
Size | Project Name: <Project Name> | Rev
Date: Thursday, June 16, 2016 Sheet 80 of 105

Main Func = Vram (DDR3L)

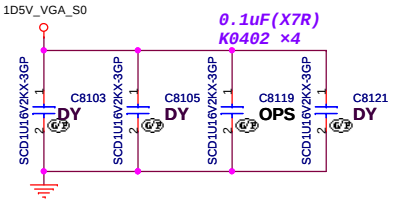




Place close VRAM1VDDQ ball

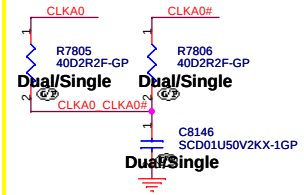


Place close VRAM2 VDD ball

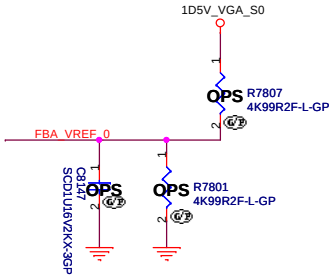


R7805 R7810

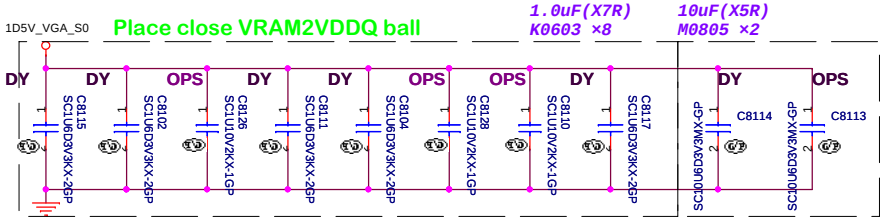
Single Rank, 40.2 Ohm = 64.40R25.6DL
Dual Rank, 80.6 Ohm = 64.80R65.6DL



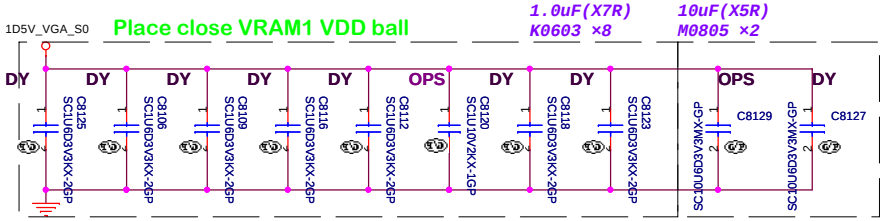
Frame Buffer Patition A-Lower Half



Place close VRAM2VDDQ ball



Place close VRAM1 VDD ball



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Title: GPU-VRAM1,2 (1/4)

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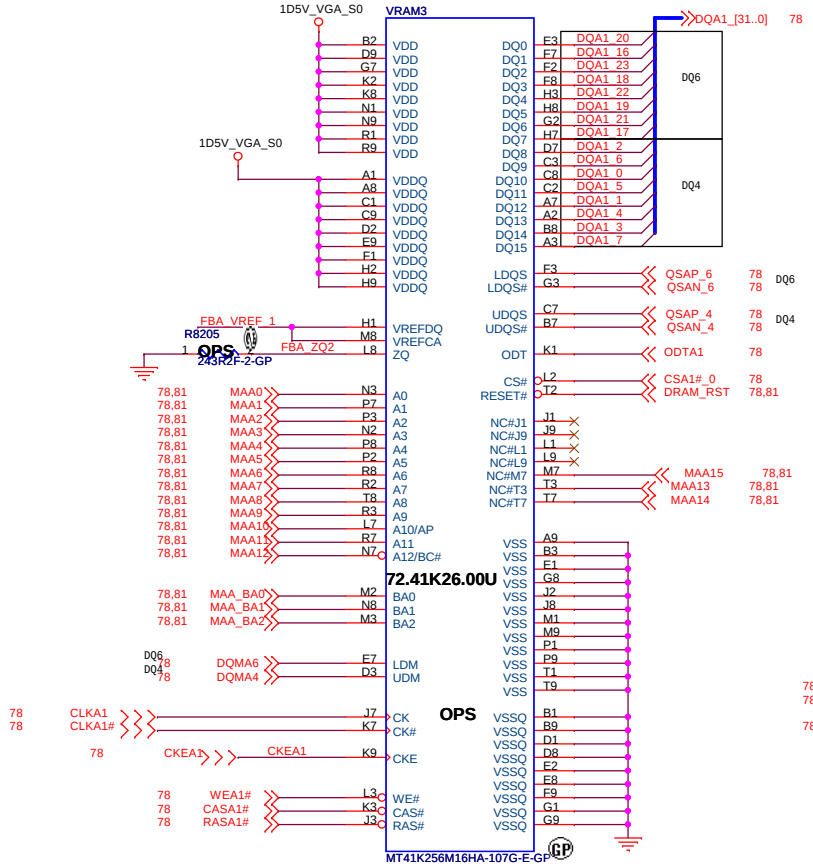
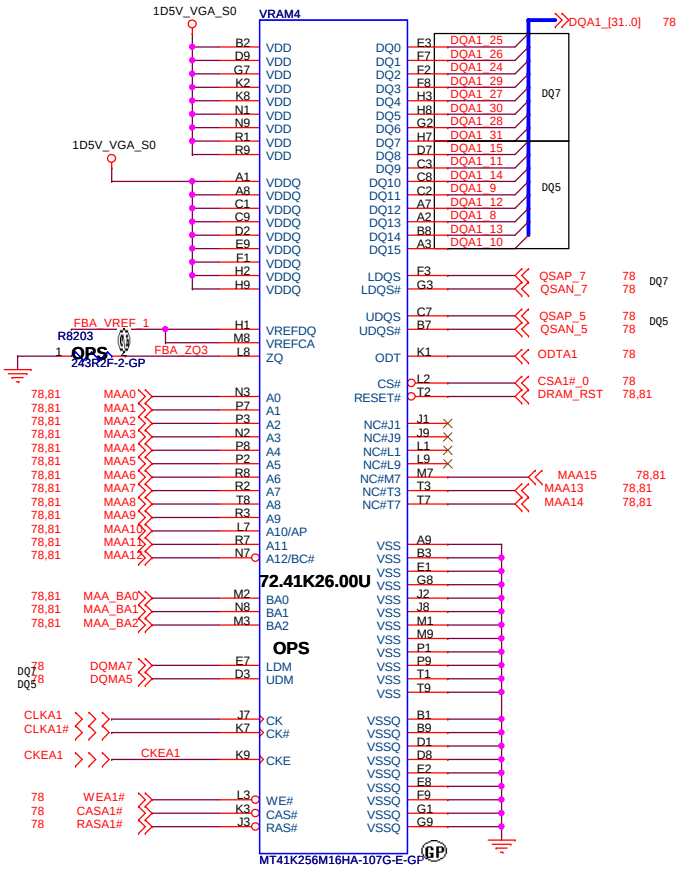
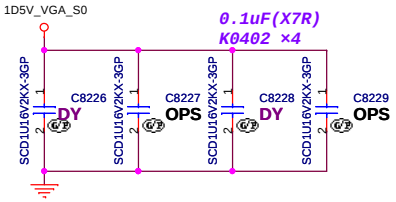
Main Func = Vram (DDR3L)

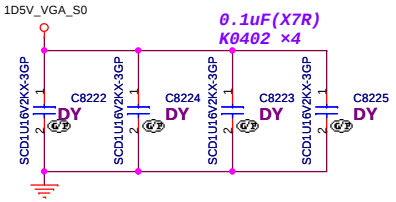




Place close VRAM3VDDQ ball

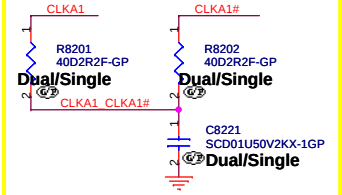


Place close VRAM4VDDQ ball

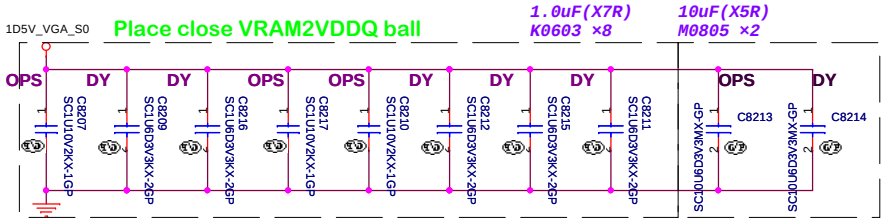


R7905 R7910

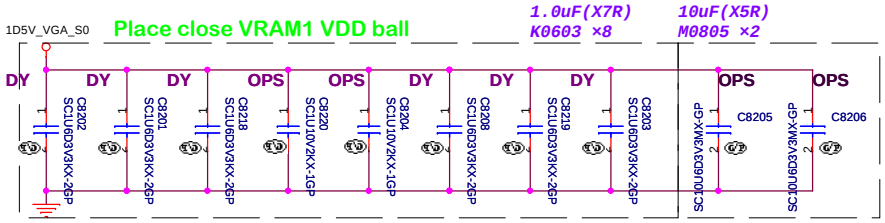
Single Rank, 40.2 Ohm
Dual Rank, 80.6 Ohm



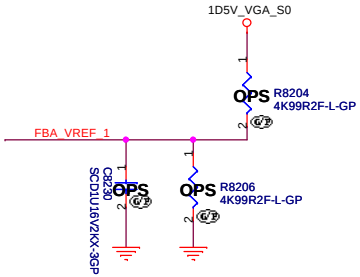
Place close VRAM2VDDQ ball



Place close VRAM1 VDD ball



Frame Buffer Patition A-Lower Half



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Title: GPU-VRAM3,4 (2/4)

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Title: *GPU-VRAM5,6 (3/4)*

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Title: *GPU-VRAM7,8 (4/4)*

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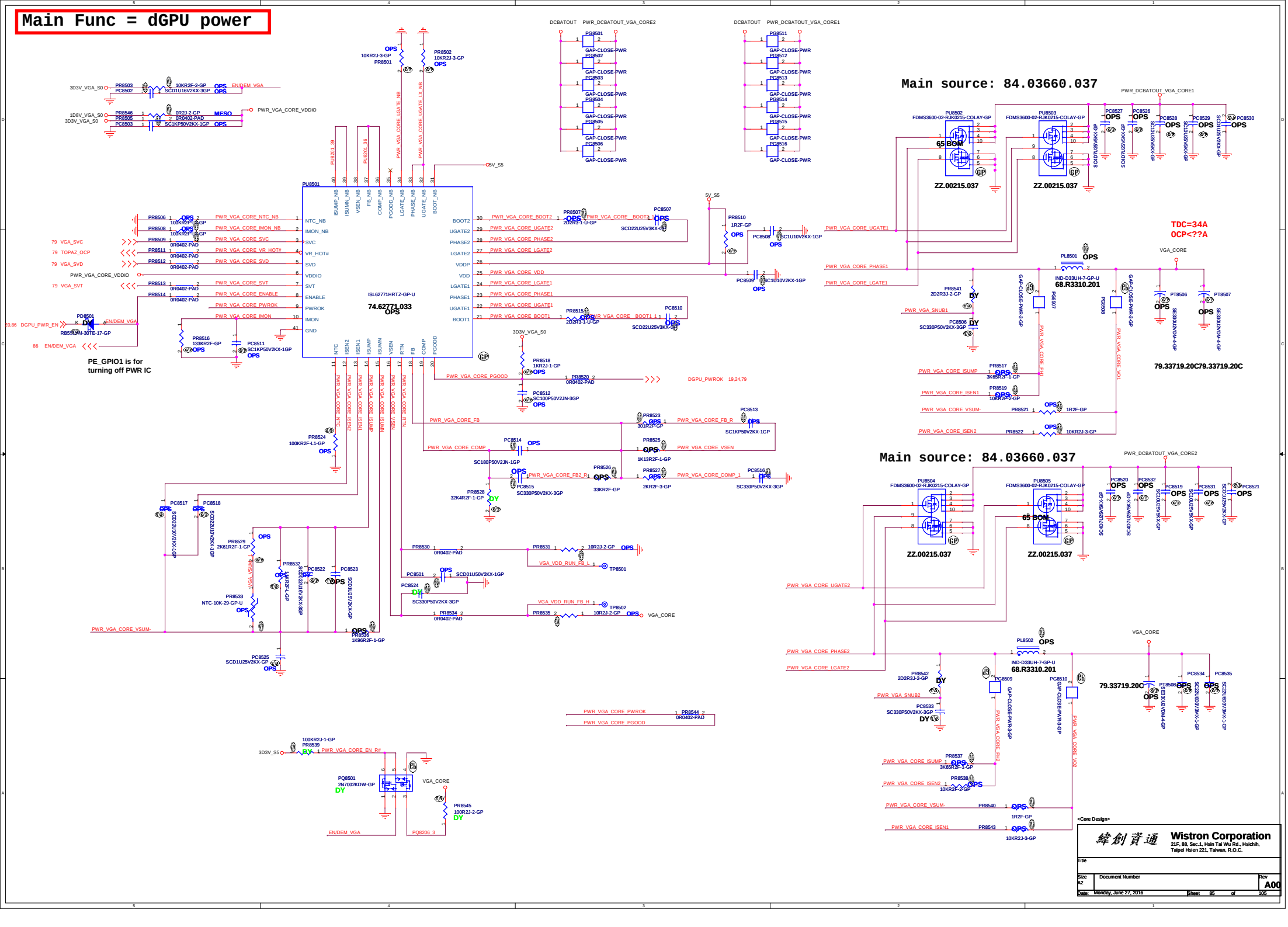
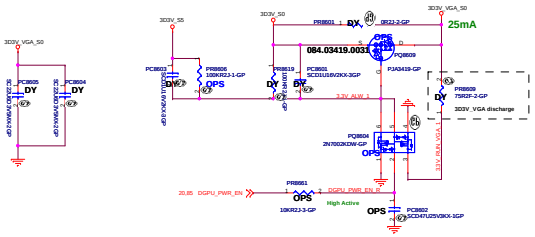
Main Func = dGPU power



Main Func = dGPU

3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing

3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

=> 1D5V_VGA_S0

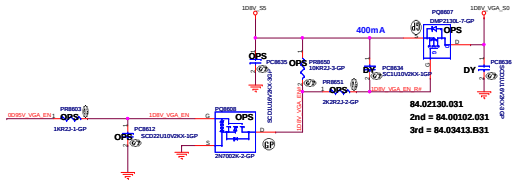
=> VGA_CORE

All the ASIC supplies must reach their respective nominal voltages withing 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

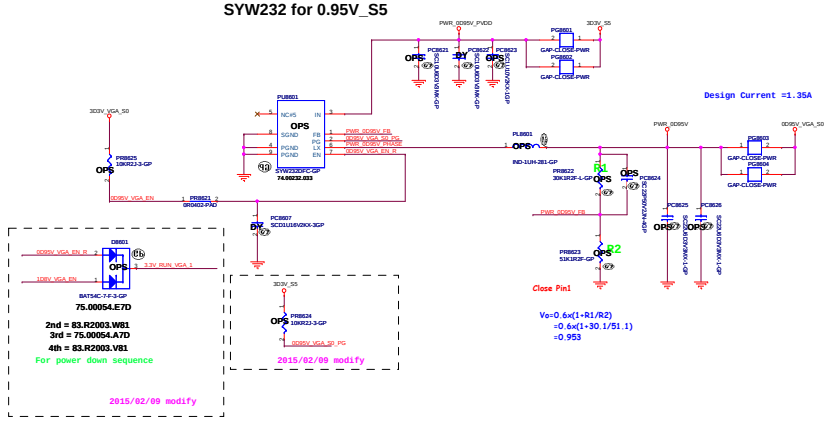
It is recommended that the 3.3V rail ramp up first.

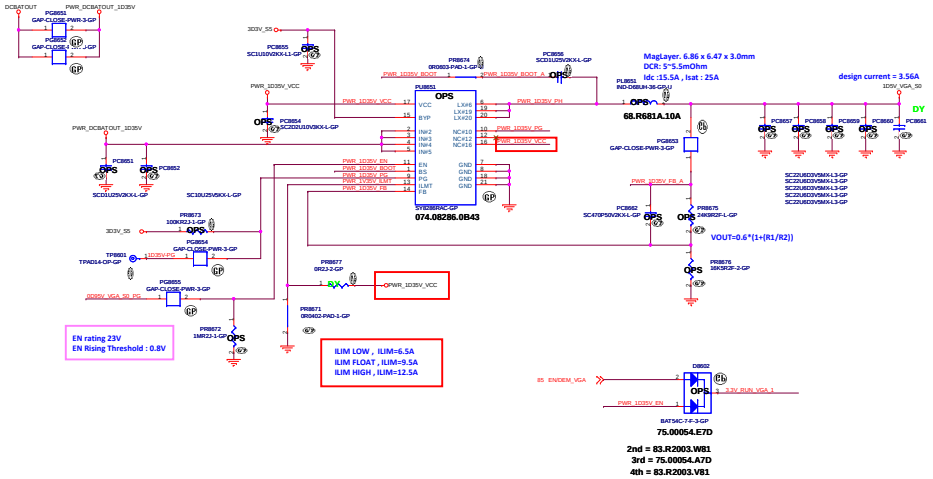
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

1D8V_VGA_S0



SYW232 for 0.95V_S5





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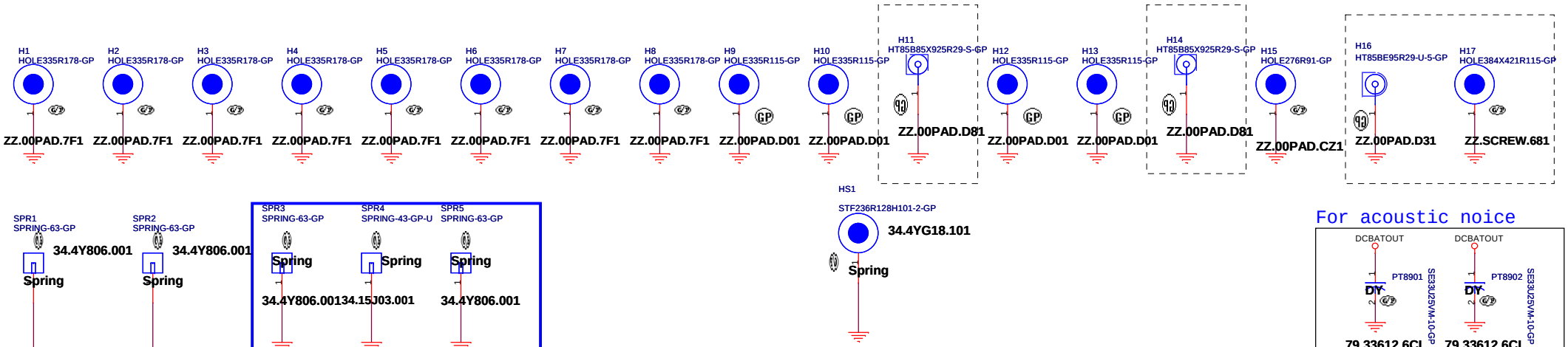
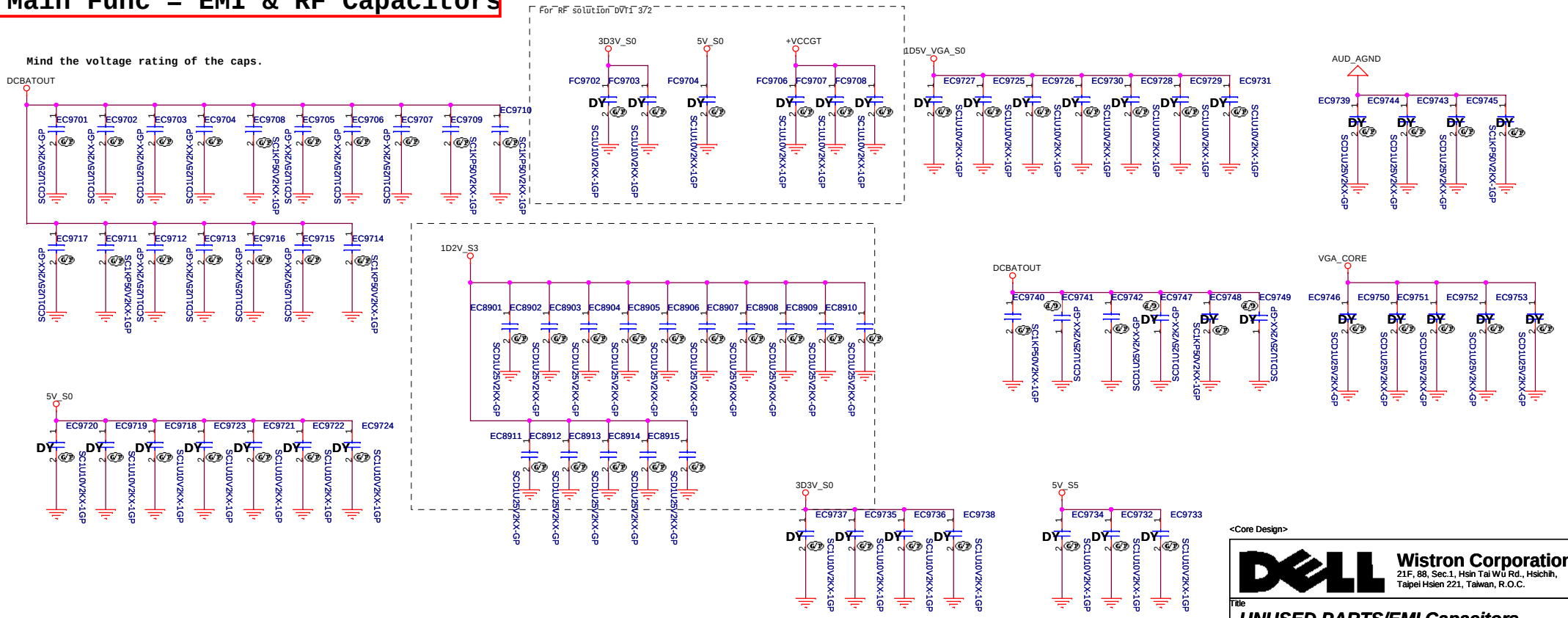
Main Func = UnusedParts



Main Func = EMI & RF Capacitors

Mind the voltage rating of the caps.



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Title: UNUSED PARTS/EMI Capacitors

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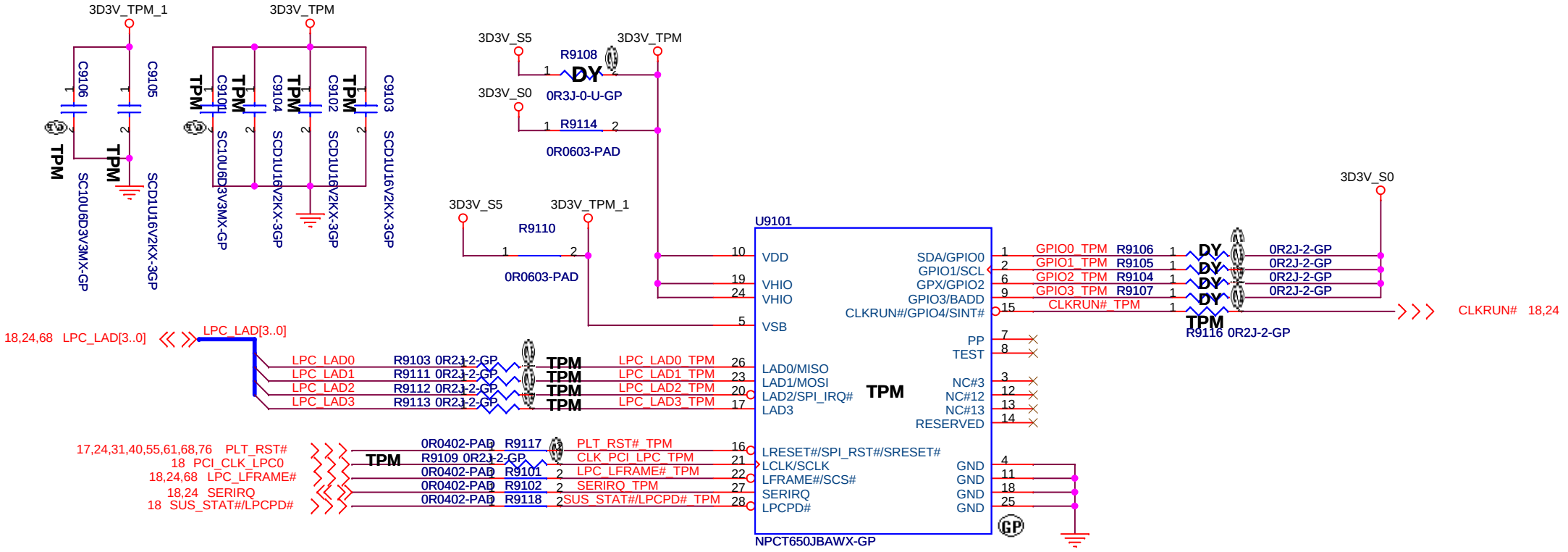
SSID = TPM



071.00650.0G0W

1.6.2 LPC Host Interface

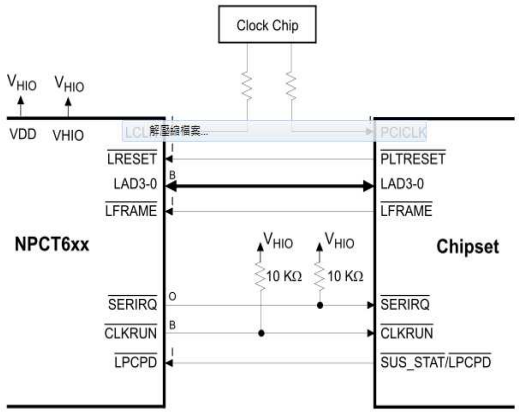


Figure 1-6. Host-LPC Interface Connection

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Size: A4	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
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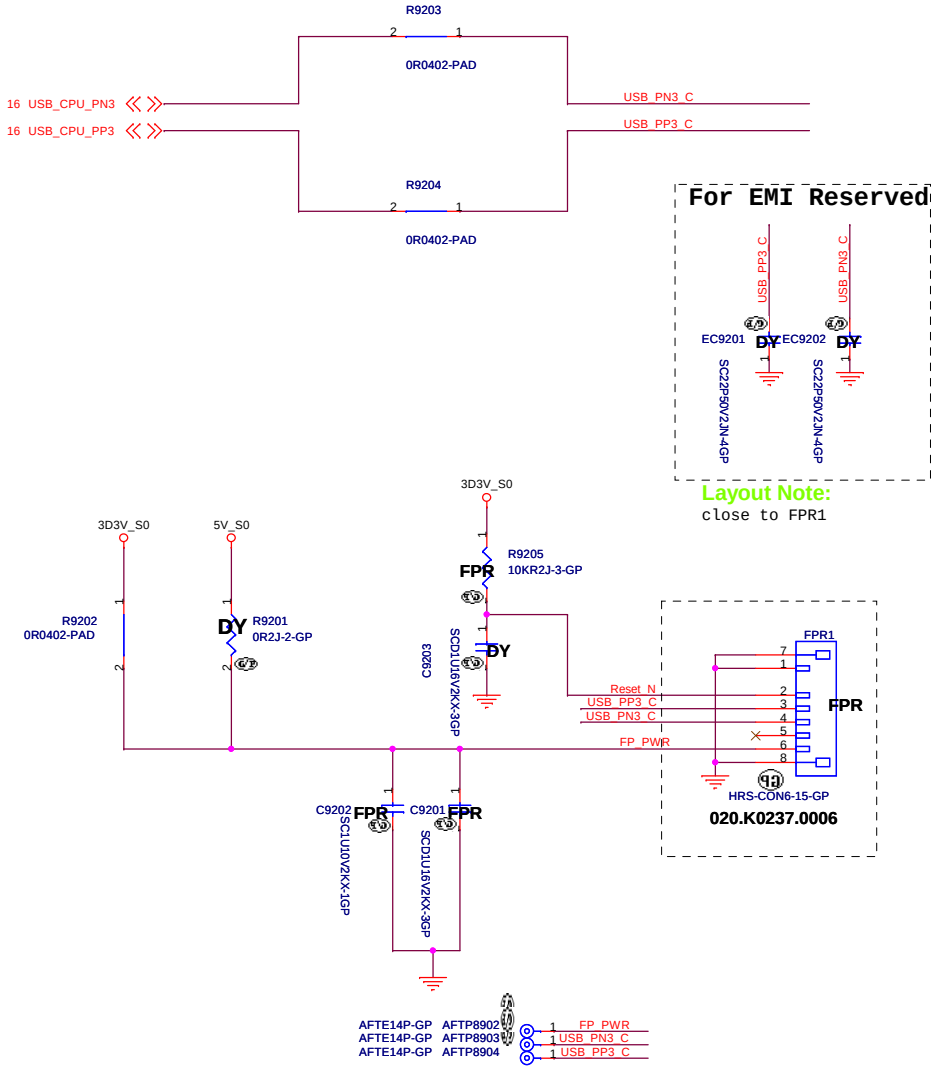
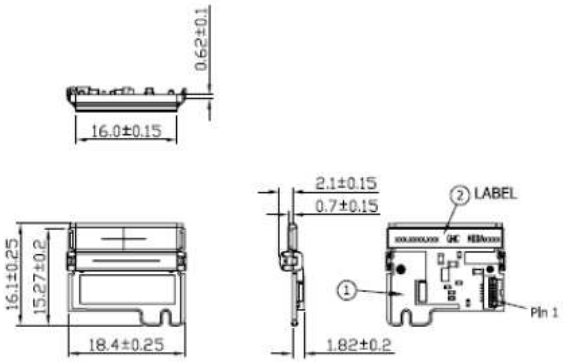
SSID = Finger Print

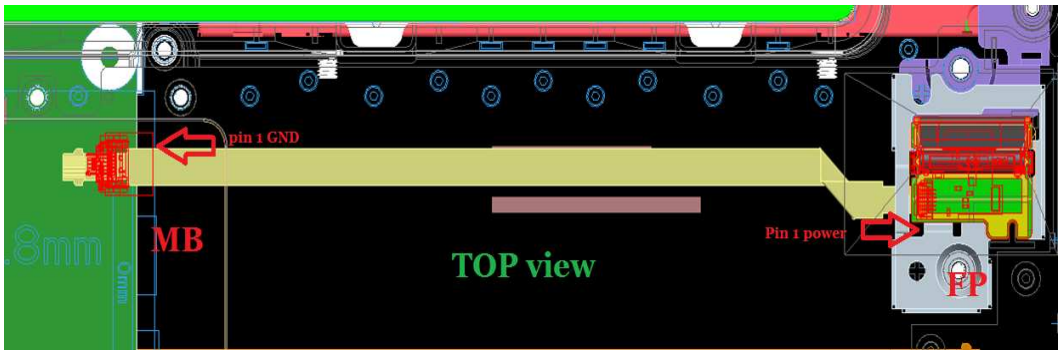




FingerPrint Pin Assignments.

Pin 1 = 3.3Vin
Pin 2 = GND
Pin 3 = D-
Pin 4 = D+
Pin 5 = Reset_N
Pin 6 = GND

Note :
Module:
1.Sensor Type:Semiconductor
2.Interface:USB 1.0 and 2.0 Full Speed



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Title
LVDS_Switch

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Title
CRT_Switch

Size	Document Number	Rev
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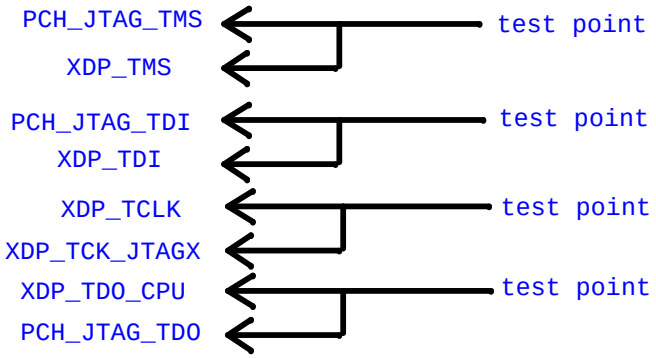

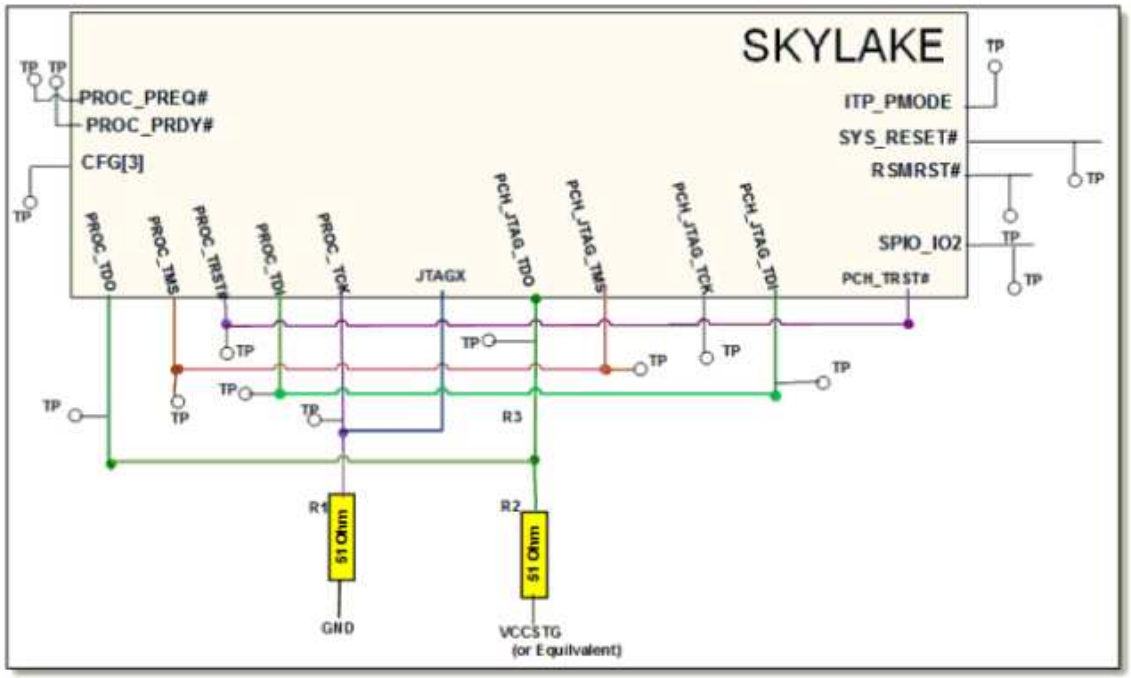

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Title: ***CPU_XDP;PCH_XDP***

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

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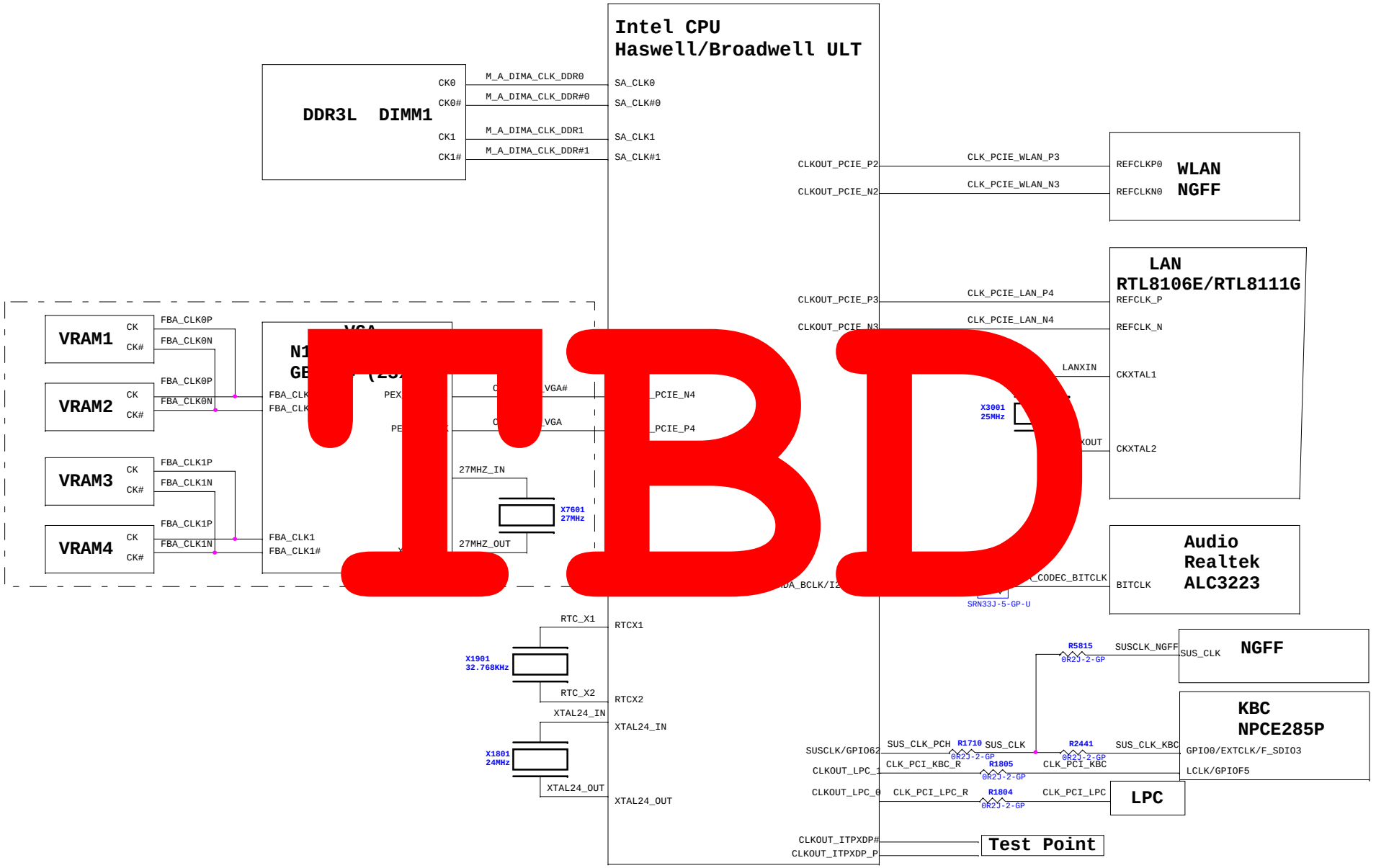
CLK Block Diagram



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Title	CLK Block Diagram	
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Change notes -

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Title: Change History

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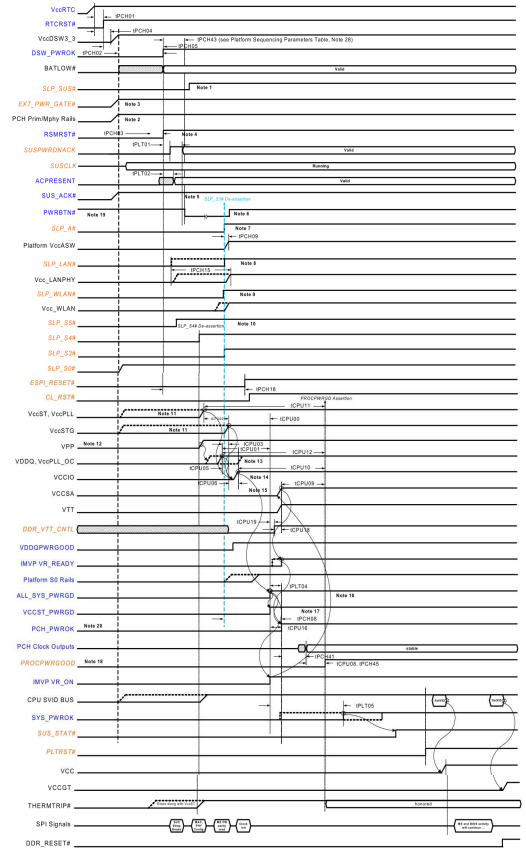
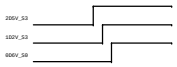
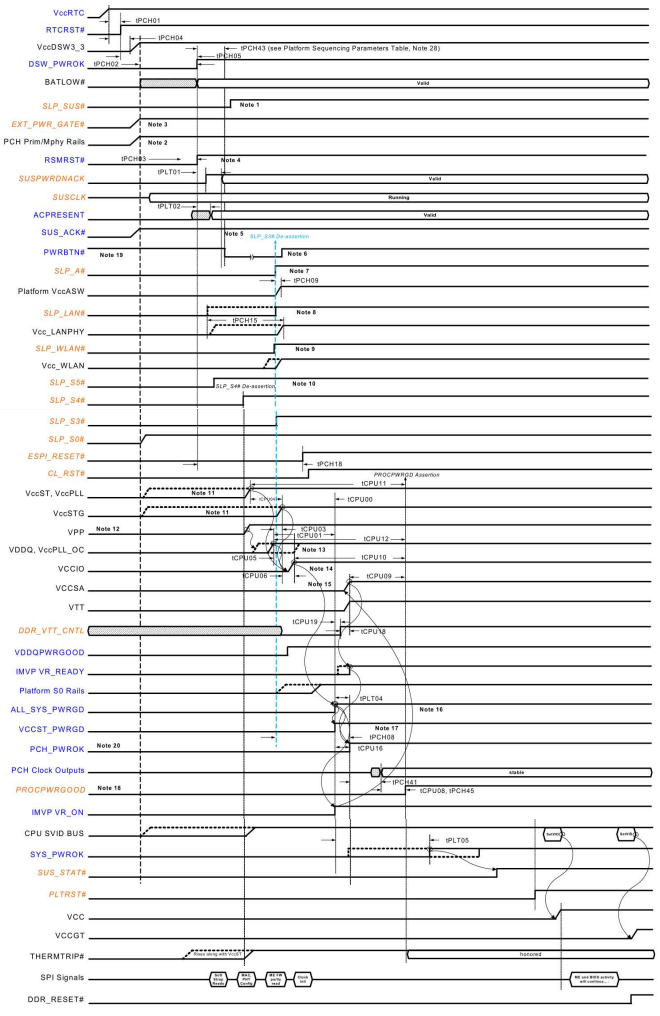
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



For DDR4 power sequence



KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



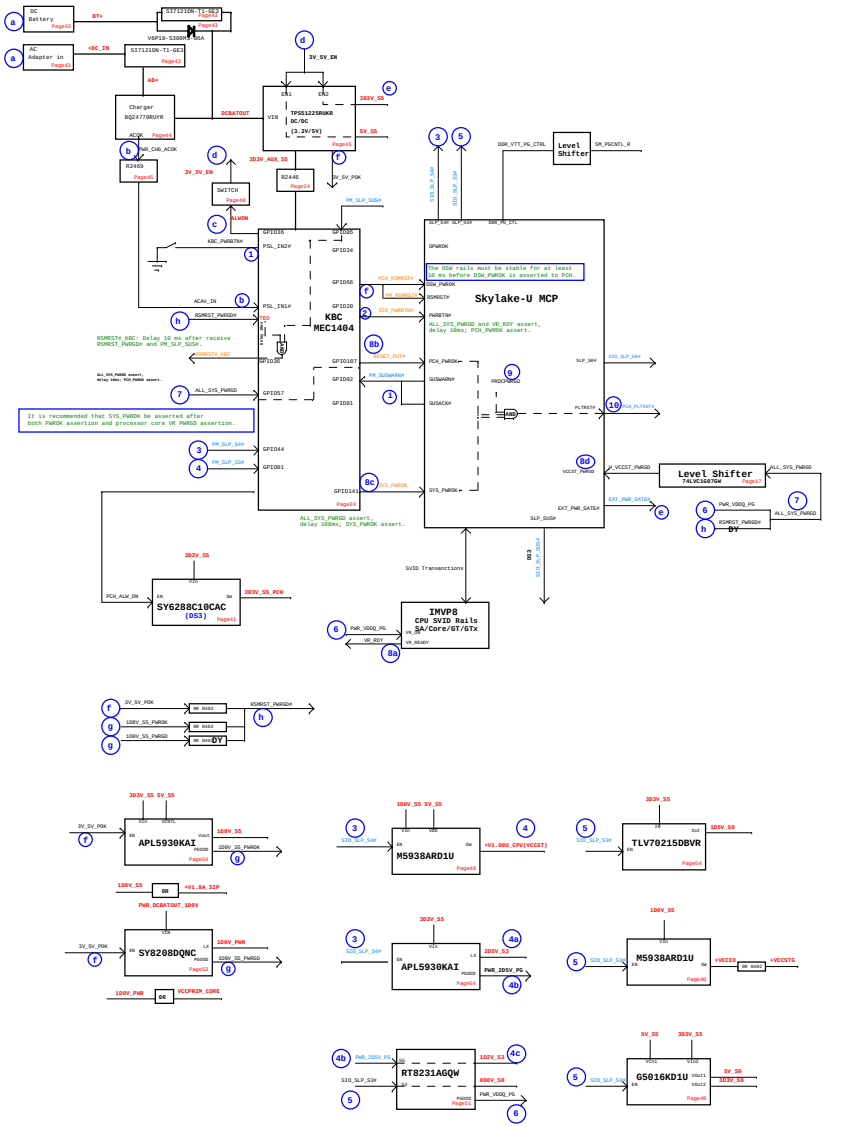
AMD GPU Power sequence

3D3V_VGAS0
=> 0D95V_VGA_S0/1D8V_VGA_S0
=> 1D5V_VGA_S0
=> VGA_CORE

20ms
All the ASIC supplies must reach their respective nominal voltages withing of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.
It is recommended that the 3.3V rail ramp up first.
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)

Red: Power Rail
Orange: Output from KBC
Light Blue: Output from CPU



a → b → c → d → e → f → g → h → i

1 → 2 → 3a → 4 → 4a → 4b → 5 → 6 → 7 → 8 → 8a → 8b → 9 → 10

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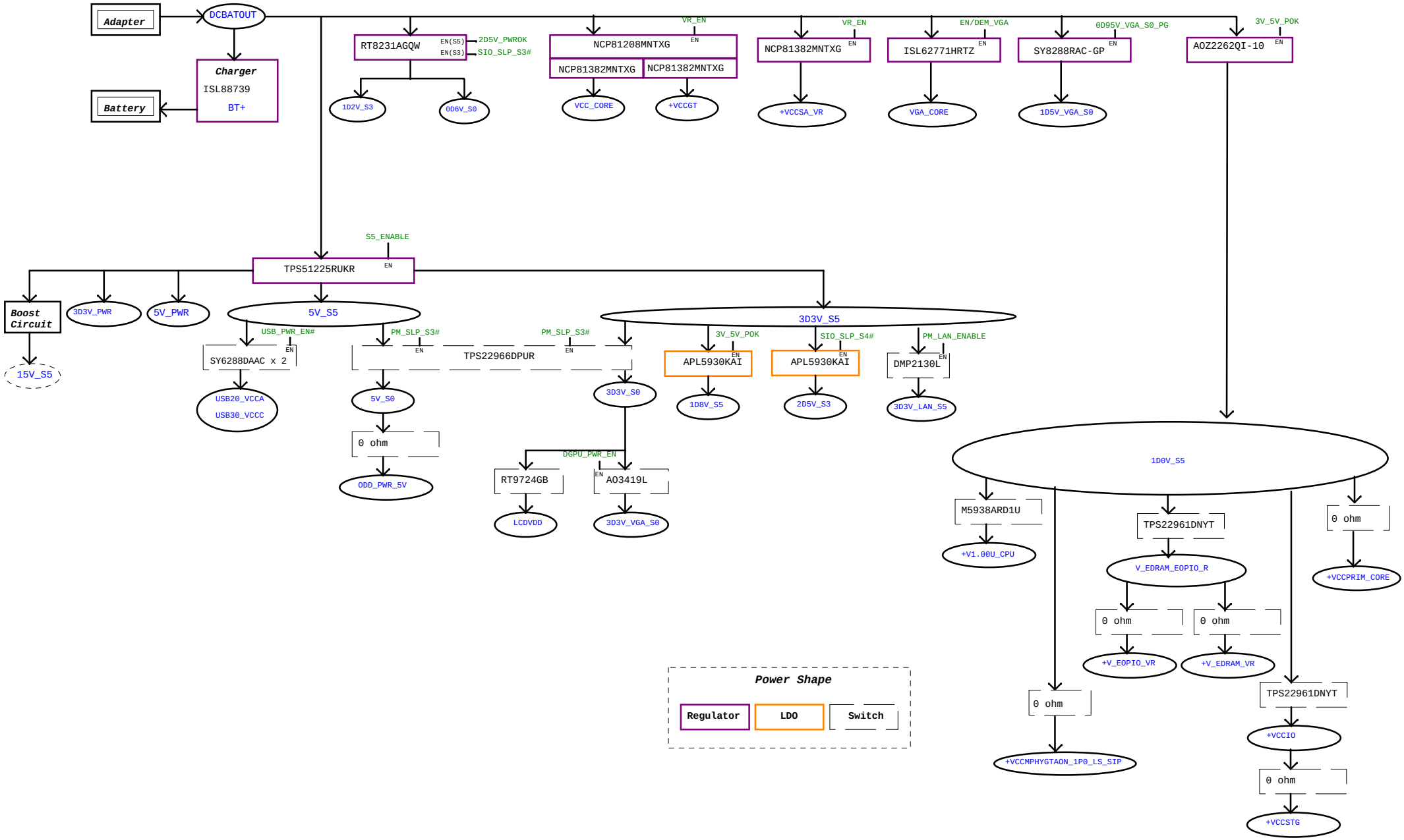
Power Sequence
Vegas SKL/KBL-U



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Title: Power Block Diagram

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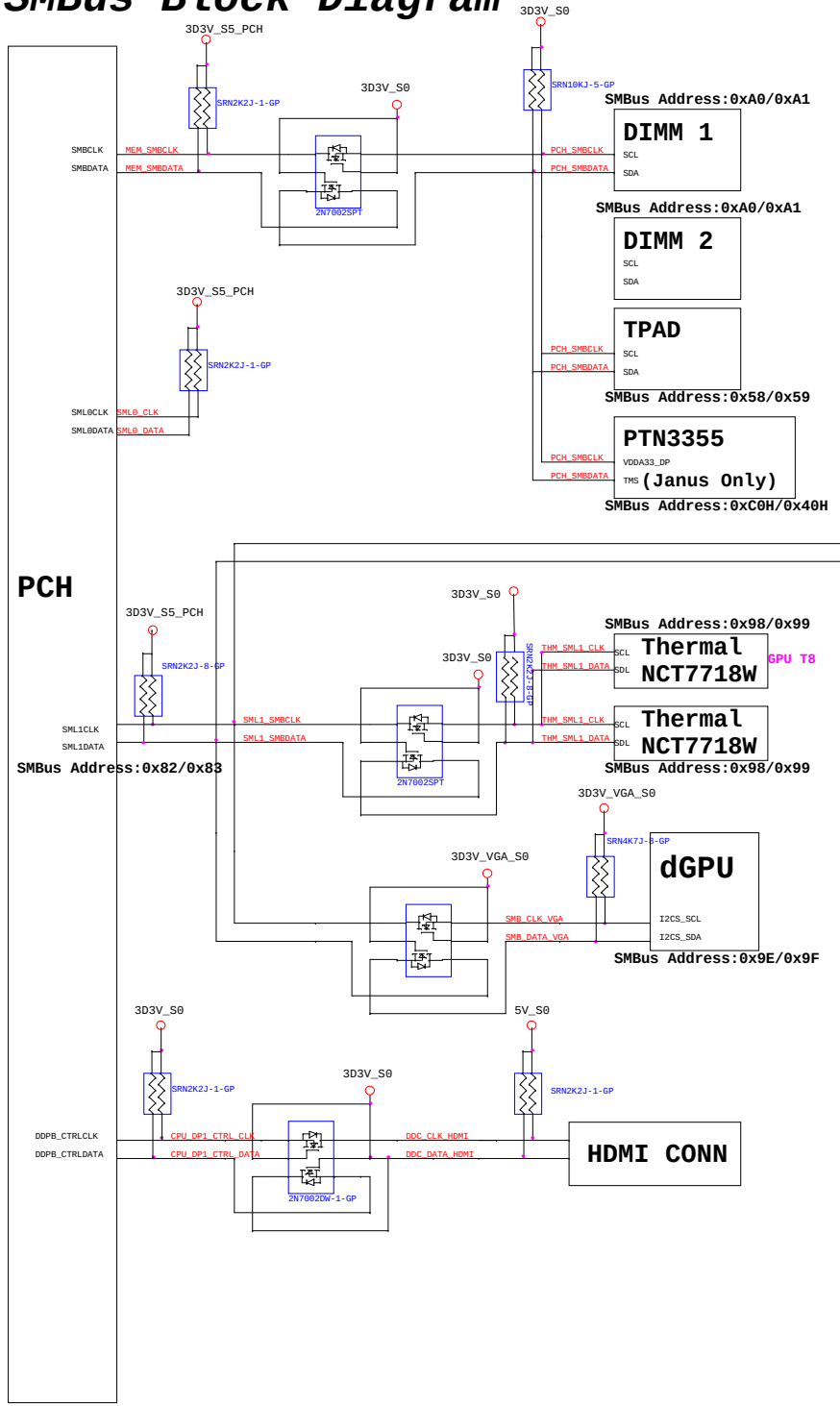
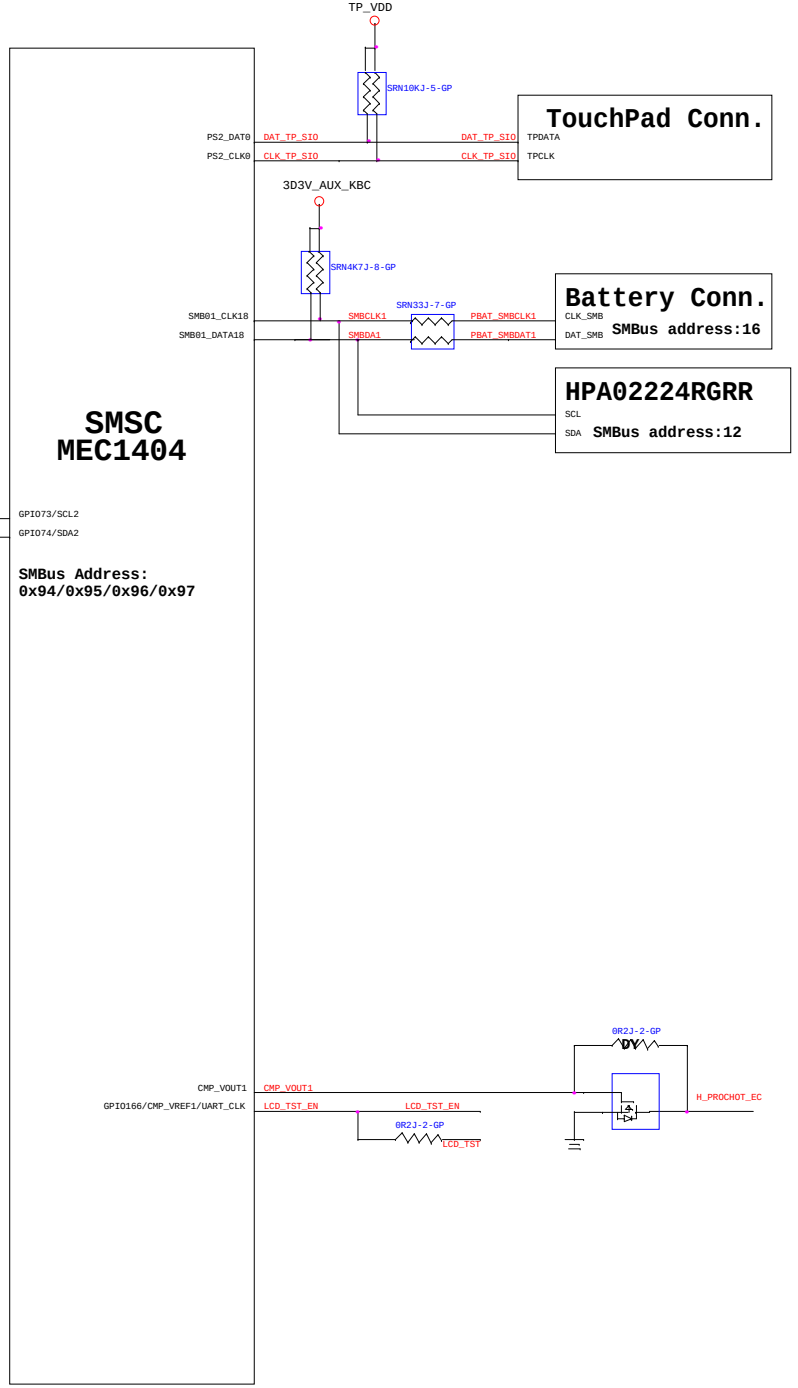
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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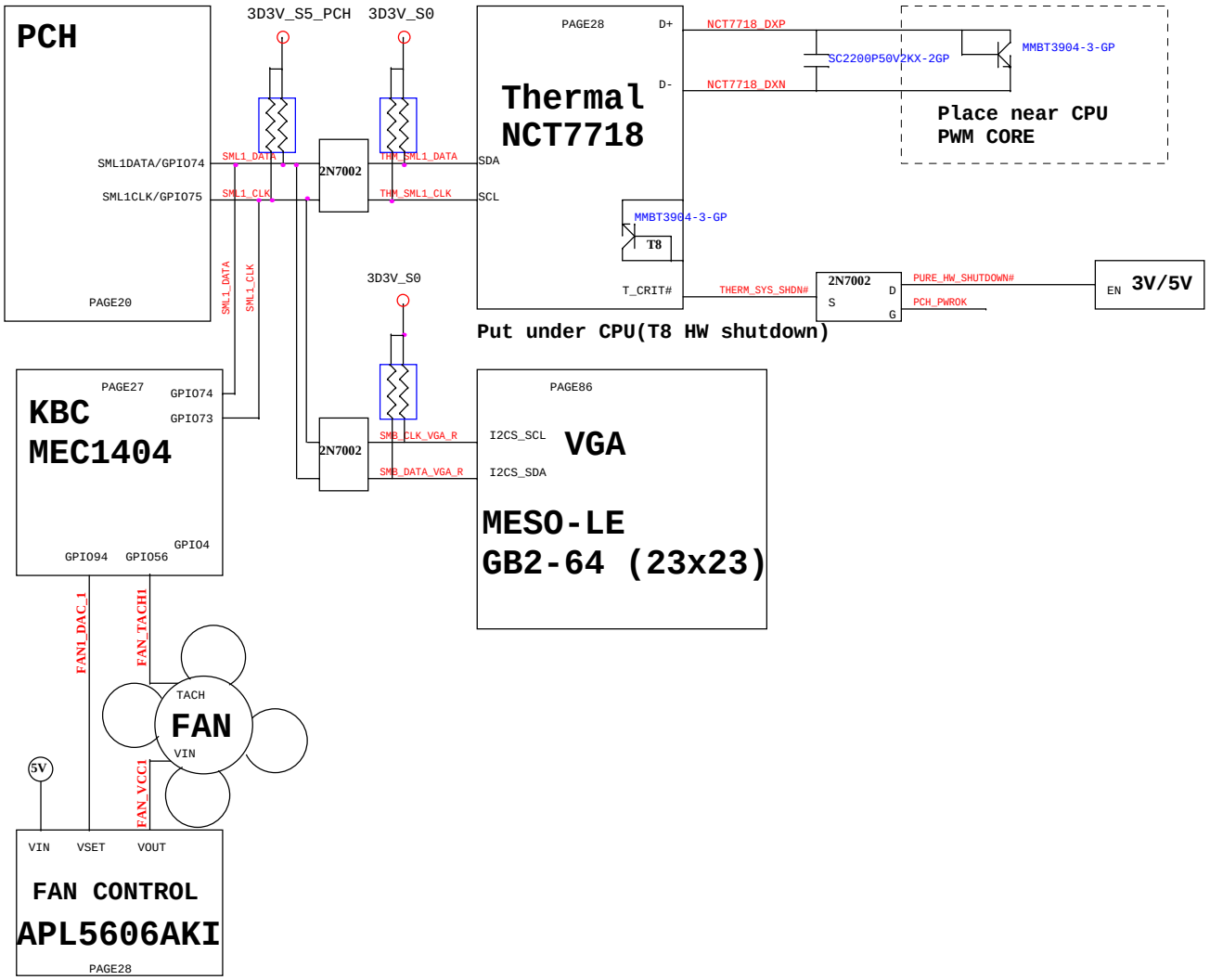
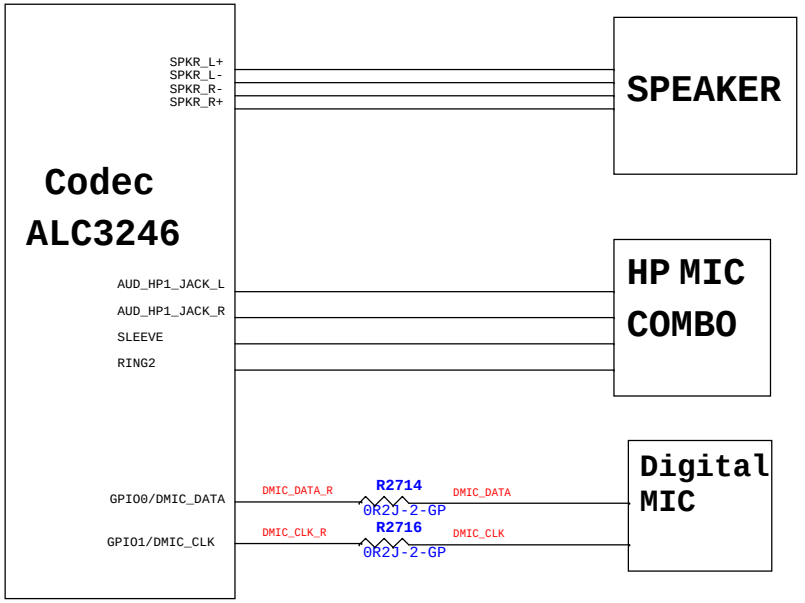
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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