Model Name: EP43-UD3L REV 1.0

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01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	TABLE LIST
05	P4_LGA775_A
06	P4_LGA775_B,D
07	P4_LGA775_C
08	P4_L775_E,F,G,H
09	GMCH-Eaglelake_HOST
10	GMCH-Eaglelake_DDRII
11	GMCH-Eaglelake_PCI E, DMI
12	GMCH-Eaglelake_INT VGA
13	GMCH-Eaglelake_GND
14	GMCH-Eaglelake_PWR
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17	DDRII TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH10 DMI, PCI, USB
20	ICH10 GPIO, CTRL
21	ICH10 SATA, FAN PWM
22	ICH10 VCC, GND
23	CLOCK-ICS9LPRS914
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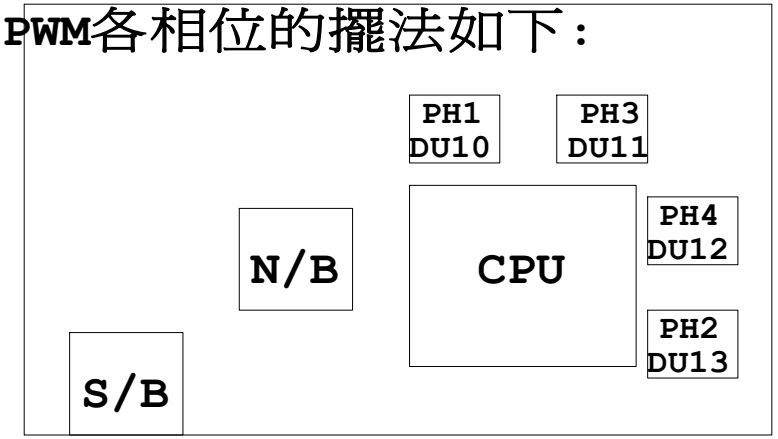
25	ITE8718/GB,RESET DRIVE
26	COM_LPT, -PROHOT,DYNAMIC,RUSB
27	BIOS,CI,HWM,KB/MS

SHEET	TITLE
28	AZALIA ALC888
29	AUDIO JACK
30	VCORE PWM ISL6334CRZ
31	DISCRETE1 POWER,FAN CTRL
32	ATX POWER
33	JMicron JMB368
34	LAN REALTEK RTL8111C
35	FRONT PANEL,FUSB,FDD
36	TPM I/F-1.2

PWM各相位的擺法如下：



Gigabyte Technology

Title: Cover Sheet

Size: Custom | Document Number: EP43-UD3L | Rev: 1.0

Date: Friday, December 05, 2008 | Sheet 1 of 36

Model Name: GA-EP43-UD3L
Rev:.1.0

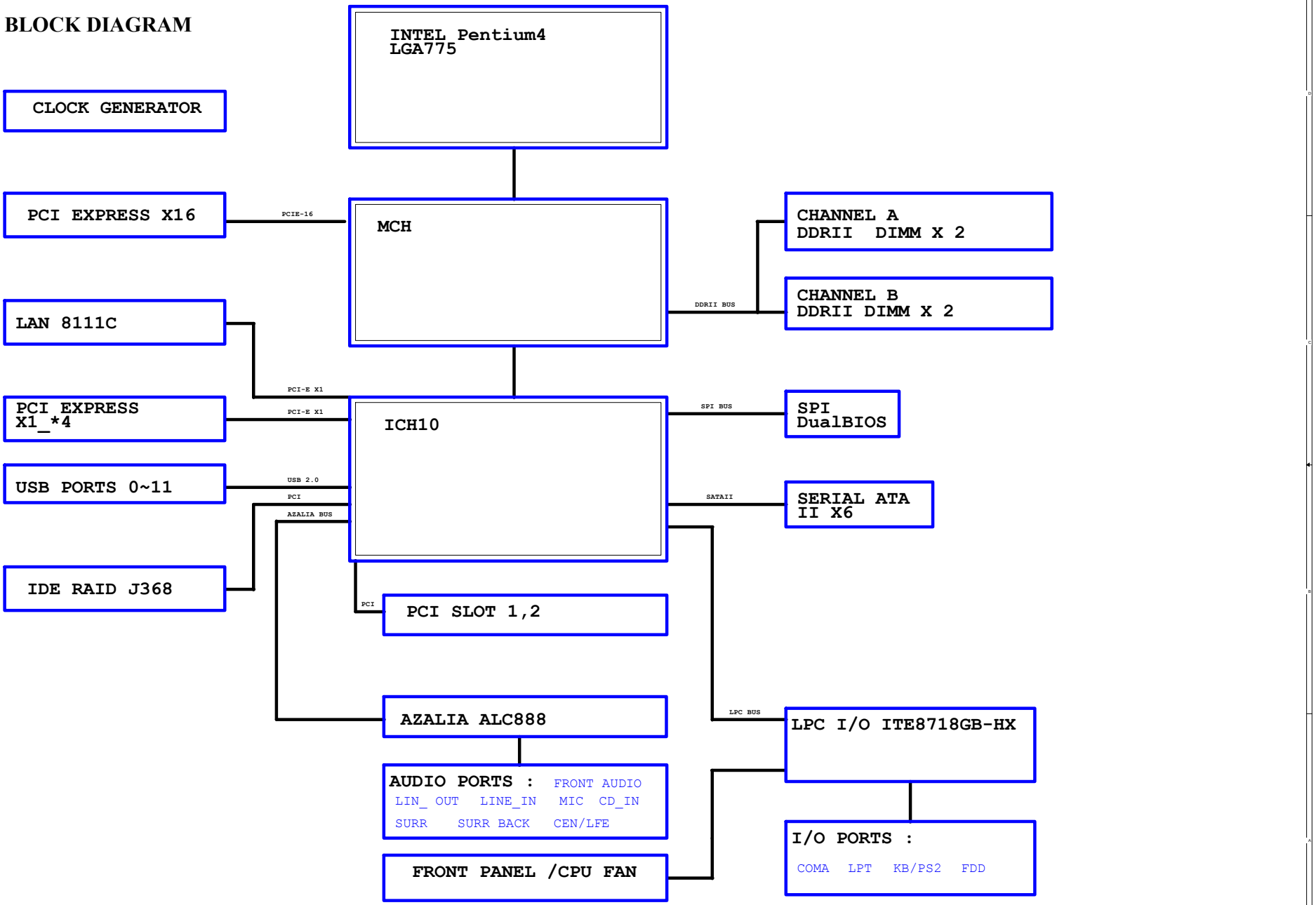
Component value change history

Data	Change Item	Reason
97/04/01 EBOM:01A	1. P43 CHIPSET E-BOM	
97/04/15 EBOM:02	1. 修改LED的OWER及阻值;DEL R484,DR78. ADD DR79,,R348	
	2. ADD DR80,R300 10-->49.9,C158,LBC43 0ohm-->100PF for EMI	
	3. del Q3,Q4,BC11,BC9,R42,R15,PCI_BT1,PCI_BT2,R166,R168	
97/04/28 EBOM:10A	1. DDR2 VOLTAGE 1.83 --> 1.9V --> 2.0V --> 2.1V .....-->2.5V	
97/05/09 PBOM:10B	1. DR59,DR60 14K---->549ohm,del DR69	
	2. ADD U9(uP6262),R436,BC133 FOR CPU 超頻	
97/05/21 PBOM:10C	1.ICH,MCH PCI-E ,JM368的RX,TX串電容BOM 0.1U/Y5V-->0.1U/X7R,RTC RTCVDD -->X7R	
	2.ADD U6 FOR DDR TURN ON 2.1V ISSUE	
97/06/4 PBOM:10D	1.DEL Q107,R620,ADD R621	
	2.Q49(BAT54C) 限用 DII	
97/06/18 PBOM:10E	1.ADD MB_ID R283,DEL R282,Q87,Q91,R452,R498,R499,R500 FOR VTT_GMCH 1.2V	
	2.C197 0.1U/Y5V--->X7R	
	3.R300 49.9--->100 ohm ,C158 Y5V--->X7R for USB	
	4.DC20 0.01u--->1nf FOR CPU PSI ISSUE	
97/08/07 EBOM:20A	1.CPU 改爲SMART FAN	
	2.L4,L7 CHOKE Footprint Change "CHOKE1U2-20A-1PQN"	
	3.獨立南橋1.1V 的電壓	
	4. ADD GPIO37 FOR LOAD LINE CALIBRATION	
	5.J368 改爲1.8V;R209=100 OHM, ADD R640 FOR MB_ID2	
97/08/08 EBOM:30A	1.J368 改爲1.8V;47--->44.2	2.TO252---改爲POWER PACK
97/10/01 PBOM:10A	FOR EP45-UD3L-1.0	
	1.R183 18K-->9.09K;R184 9.76K--->4.3K	2.DR56 1.74K-->1.87K;DR81 1K--->590 OHM
	3.DR38 487--->549 ohm 4.R369 2.26K--->1.5K;R378 13.7K--->15.8K	
	4.NB,SB CHANGE HEAT SINK for UD series; PCIEX1 SLOT改爲白色	
	5.RQ3 由BJT改爲 BAT54A FOR -HDLED ISSUE	
97/11/06 PBOM:10A	FOR EP43-UD3L-1.0	
	1.P43 CHIP,HEAT SINK,UPI	

Circuit or PCB layout change for next version

DATE	Change Item	Reason
97/04/01 PCB:0.1	1.P43-DS3L	
97/04/23 PCB:1.0	1. CE3位置請移至EC24左邊	
	2. 增加 upi6262 VCC Power (R620,R621,Q107)	
	3. 增加R622,R623 FOR DDR18V_OV3	
97/07/23 PCB:2.0	1.由1.0 修改,直接改成2.0	
	2.PCIEX16 和PCIEX1_2對調位置	
	3. DDR2_1~DDR2_4往左移,盡量讓MCH的位置在DDR SLOT中間	
	4.ADD CPU SMART FAN CONTROL	
97/07/23 PCB:3.0	1.由2.0 修改	
	2. cpu Vcore MOS TO252改爲POWER PACK	
97/09/16 PCB:1.0	1.由3.0 修改,改文字面 EP45-UD3L ,ULTRA DURABLE 3,NB /SB 框內文字修改	
97/11/06 PCB:1.0	1.由EP45-UD3L改文字面成EP43-UD3L	
	2.DEL ICH CORE 1.1線路,NET DDR18V_OV2與LAN_DSM互換FOR DDR超壓ISSUE	
	3.UPDATE LL1 ,LGA775 FOOTPRINT	

BLOCK DIAGRAM

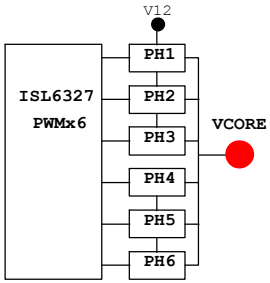


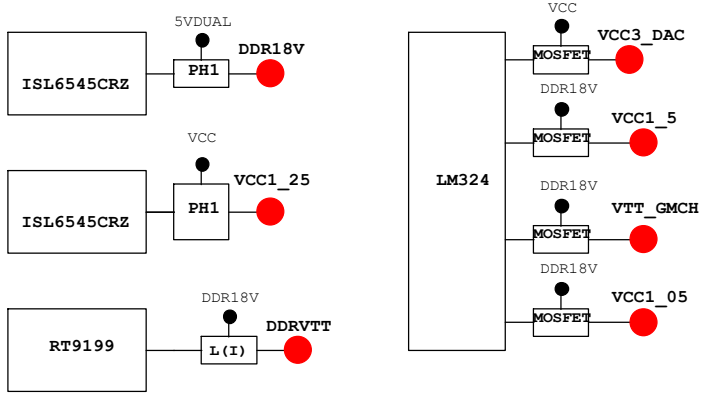
Gigabyte Technology		
Title: BLOCK DIAGRAM		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 3 of 36	

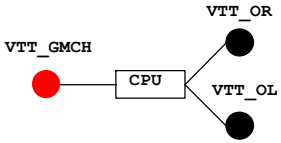
ICH8 GPIO LIST TABLE

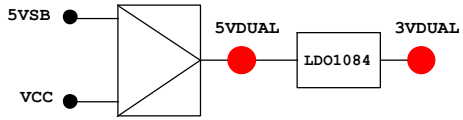
PIN NAME	PWR WELL	AFTER/ PLTRST	USAGE	NOTE
GP0	MAIN	IN	-ACZ_DET	P/U 8.2K VCC3
GP1/TACH1	MAIN	IN	ICH_FAN_TACH1	P/U 8.2K VCC3
GP2/PIRQE#	MAIN	IN	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	IN	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	IN	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	IN	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	IN	ICH_FAN_TACH2	P/U 8.2K VCC3
GP7/TACH3	MAIN	IN	ICH_FAN_TACH3	P/U 8.2K VCC3
GP8	STBY	IN	GPIO8(DUALBIOS_INPUT)	P/U 8.2K 3VDUAL
GP9	STBY	OUT	WOL_ONLY	P/D 100K GND
GP10	STBY	IN	CLGPIO1	P/U 8.2K 3VDUAL
GP11/SMBALERT#	STBY	OUT	-SMBALRT	P/U 8.2K 3VDUAL
GP12	STBY	IN	MB_ID0	P/U 8.2K 3VDUAL
GP13	STBY	IN	-LPCPME	P/U 8.2K 3VDUAL
GP14	STBY	IN	CLGPIO2	P/U 8.2K 3VDUAL
GP15	STBY	OUT	LAN_DISABLE(STP_PCI-)	N/A
GP16	MAIN	OUT/LOW	RESET	N/A
GP17/TACH0	MAIN	IN	ICH_FAN_TACH0	P/U 8.2K VCC3
GP18	MAIN	OUT	MB_ID1	P/U 8.2K VCC3
GP19	MAIN	IN	SATA1GP	P/U 8.2K VCC3
GP20	MAIN	OUT	-SPI_WP0	P/U 1K 3VCL
GP21	MAIN	IN	SATA0GP	P/U 8.2K VCC3
GP22	MAIN	IN	SCLOCK	P/U 8.2K VCC3
GP23	MAIN	OUT	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	OUT	CLGPIO0	P/U 8.2K 3VDUAL
GP25	STBY	IN	MB_ID2(STP_CPU-)	P/U 8.2K 3VDUAL
GP26/S4_STATE#	STBY	OUT	S4_STATE#	P/U 8.2K 3VDUAL
GP27	STBY	OUT/LOW	GPIO27(EL_STATE0)	P/U 8.2K 3VDUAL
GP28	STBY	OUT/LOW	PWR_LED(EL_STATE1)	N/A
GP29/OC5#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP30/OC6#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP31/OC7#	STBY	IN	-USBOC_R	P/U FUSEVCC
GP32	MAIN	OUT	DUAL_BIOS	P/U 100K+1M VCC3
GP33	MAIN	OUT	DUAL_BIOS	P/U 8.2K VCC3
GP34	MAIN	OUT/LOW	GPIO34/SMB_RST	N/A
GP35	MAIN	OUT	SATACLKREQ#	N/A
GP36	MAIN	IN	SATA2GP	P/U 8.2K VCC3
GP37	MAIN	IN	SATA3GP	P/U 8.2K VCC3
GP38	MAIN	IN	SLOAD	P/U 8.2K VCC3
GP39	MAIN	IN	GPIO39	P/D 8.2K GND
GP48	MAIN	IN	GPIO48	P/U 8.2K VCC3
GP49	MAIN	IN	CPUPWROK	P/U 100 VTT_OL

VCORE:6 PHASE PWM--ISL6327CRZ









Gigabyte Technology		
Title: TABLE LIST		
Size: B	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 4 of 36	

0.667 X VTT FOR LGA775 PIN H2/F2

0.635 X VTT FOR LGA775 PIN H1/G10

HA/REQ:50歐姆+-15% [4/11]

ADSTB:50歐姆+-15% [4/14]

LGA775A

LGA775 (1/8)

CPU-SK/775/S/15

SP-CAP X 3PCS

Impedance=50 +- 15% for 4 -layer

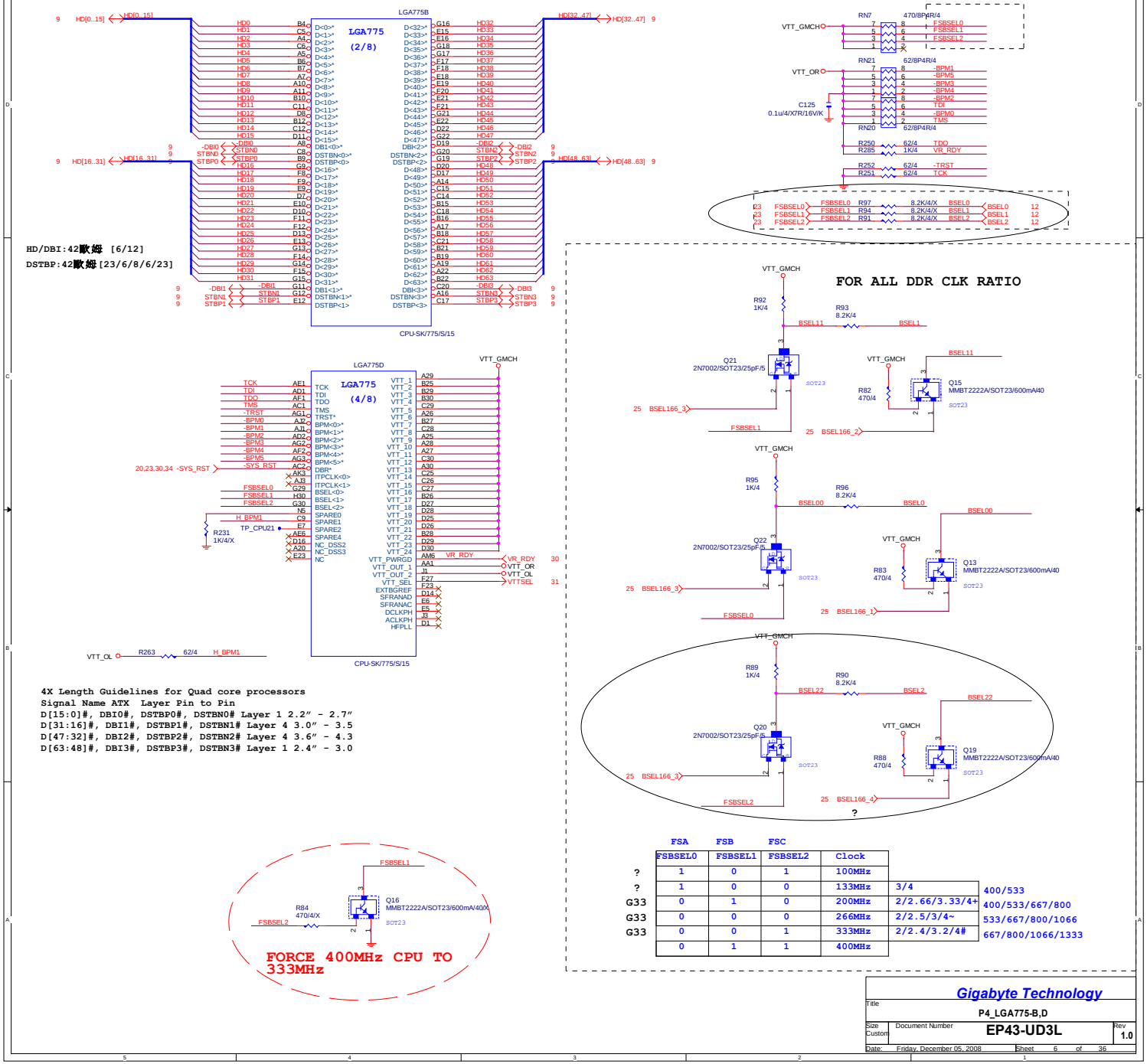
CPU GTLREF RATIO

GTLREF_UV0	GTLREF_UV1	Ratio Set
HIGH	HIGH	0.67
LOW	HIGH	0.65
HIGH	LOW	0.63
LOW	LOW	0.615

CR
CPU RETAINTION/X

Gigabyte Technology

Title	P4_LGA775-A		
Size: Custom	Document Number: EP43-UD3L		Rev: 1.0
Date: Friday, December 05, 2008	Sheet 5 of 36		


LGA775B
LGA775
(2/8)
CPU-SK/775/S/15
HD/DBI:42歐姆 [6/12]
DSTBP:42歐姆[23/6/8/6/23]
LGA775D
LGA775
(4/8)
CPU-SK/775/S/15
4X Length Guidelines for Quad core processors
Signal Name ATX Layer Pin to Pin
D[15:0]#, DBI0#, DSTBP0#, DSTBN0# Layer 1 2.2" - 2.7"
D[31:16]#, DBI1#, DSTBP1#, DSTBN1# Layer 4 3.0" - 3.5
D[47:32]#, DBI2#, DSTBP2#, DSTBN2# Layer 4 3.6" - 4.3
D[63:48]#, DBI3#, DSTBP3#, DSTBN3# Layer 1 2.4" - 3.0
FOR ALL DDR CLK RATIO
FORCE 400MHz CPU TO 333MHz
FSA FSB FSC
FSBSEL0 FSBSEL1 FSBSEL2 Clock
? 1 0 1 100MHz
? 1 0 0 133MHz 3/4 400/533
G33 0 1 0 200MHz 2/2.66/3.33/4+ 400/533/667/800
G33 0 0 0 266MHz 2/2.5/3/4~ 533/667/800/1066
G33 0 0 1 333MHz 2/2.4/3.2/4# 667/800/1066/1333
0 1 1 400MHz
Gigabyte Technology
P4_LGA775-B,D
EP43-UD3L
Rev 1.0
Friday, December 05, 2008
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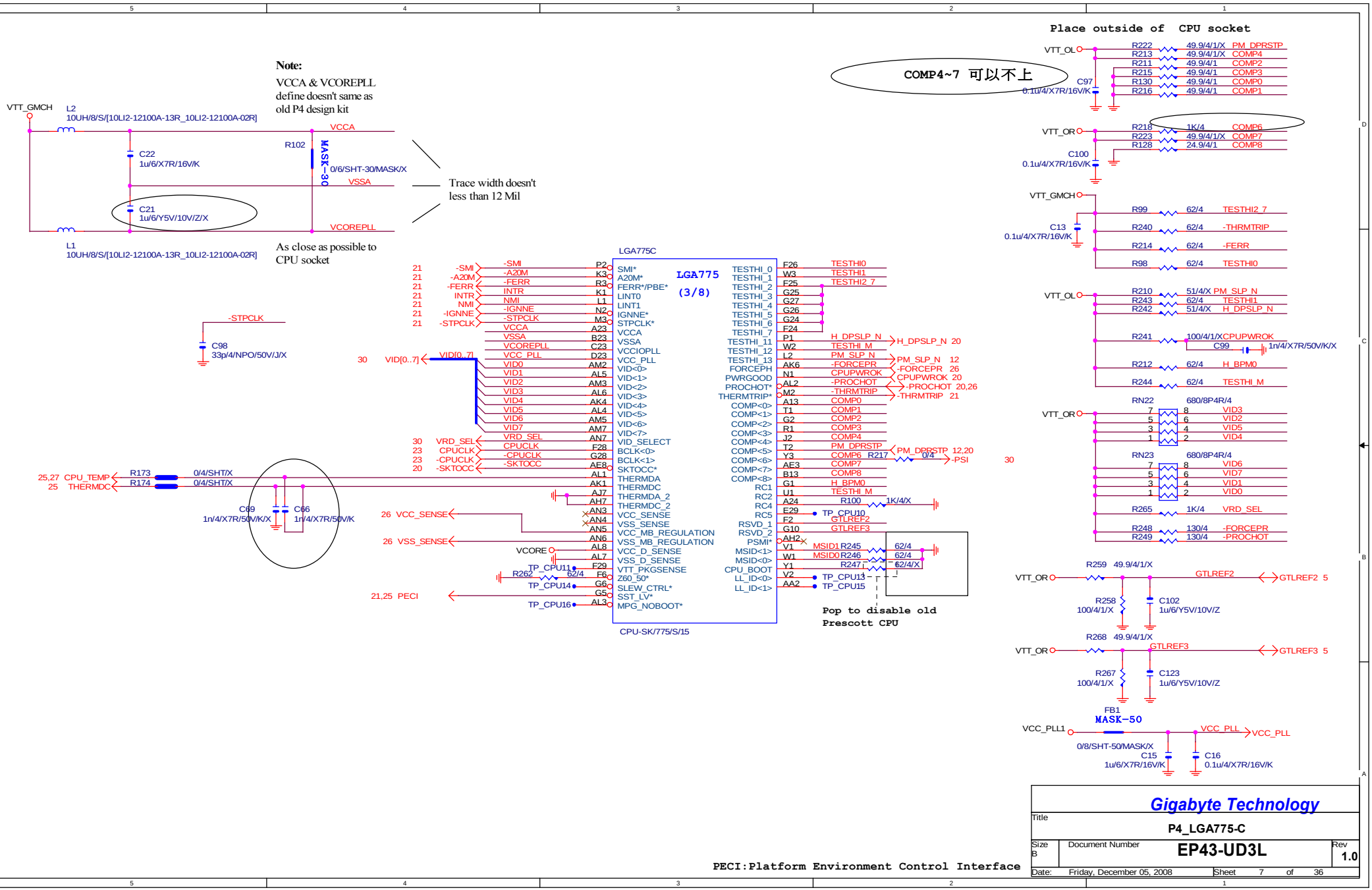
Note:
VCCA & VCOREPLL define doesn't same as old P4 design kit
Trace width doesn't less than 12 Mil
As close as possible to CPU socket
Place outside of CPU socket
COMP4~7 可以不上
LGA775C
LGA775 (3/8)
CPU-SK/775/S/15
Pop to disable old Prescott CPU
PECI:Platform Environment Control Interface
Gigabyte Technology
P4_LGA775-C
EP43-UD3L
Rev 1.0
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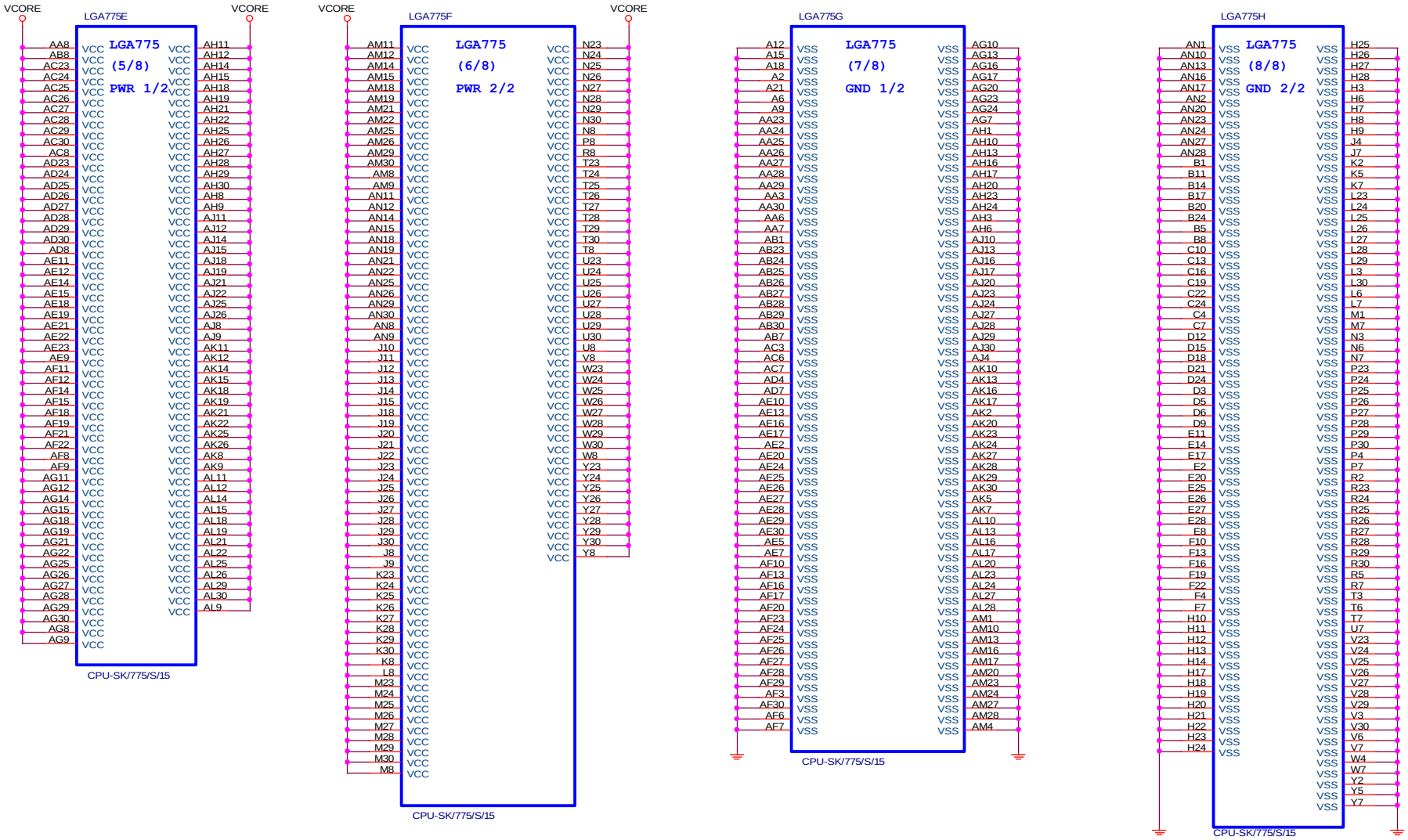
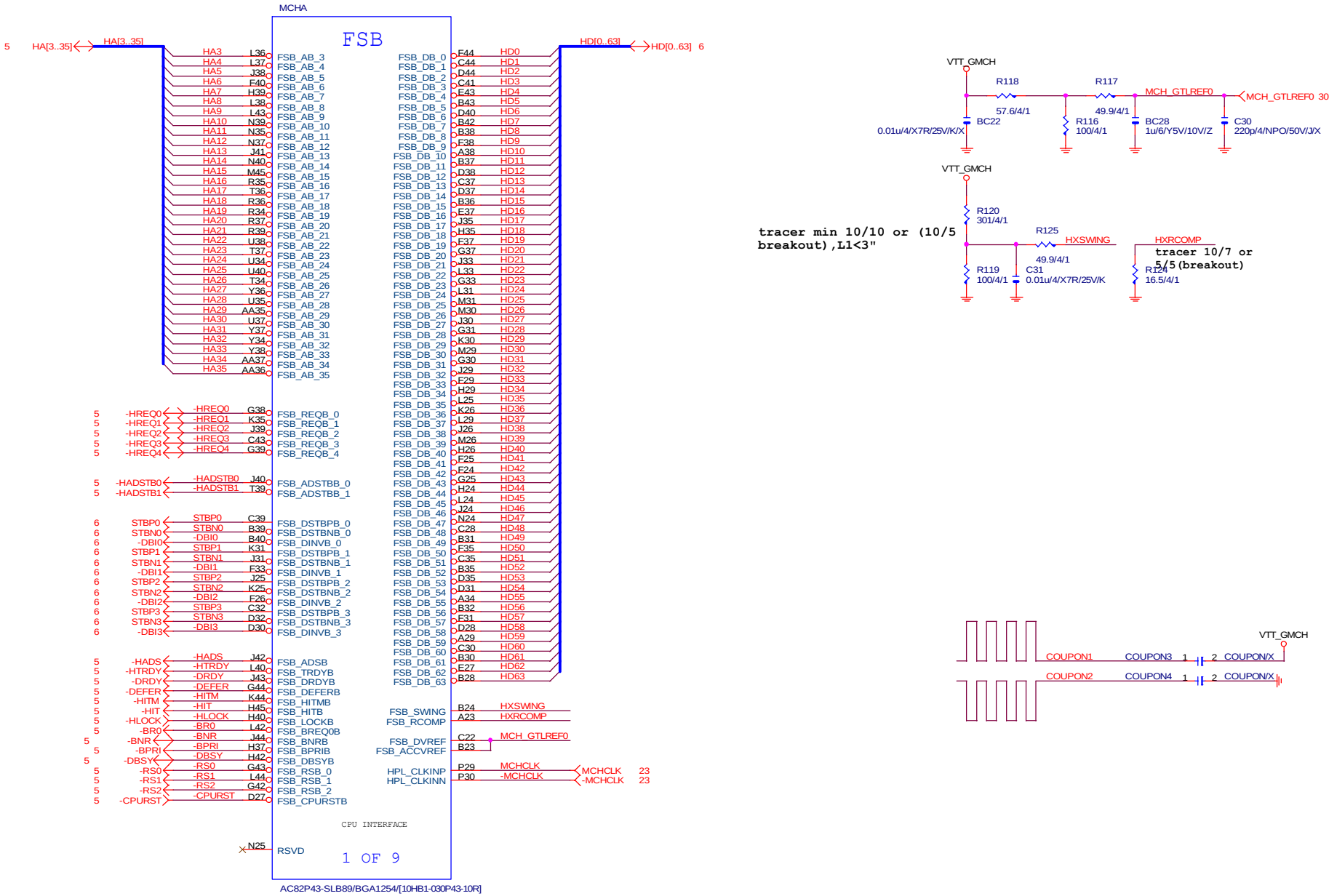
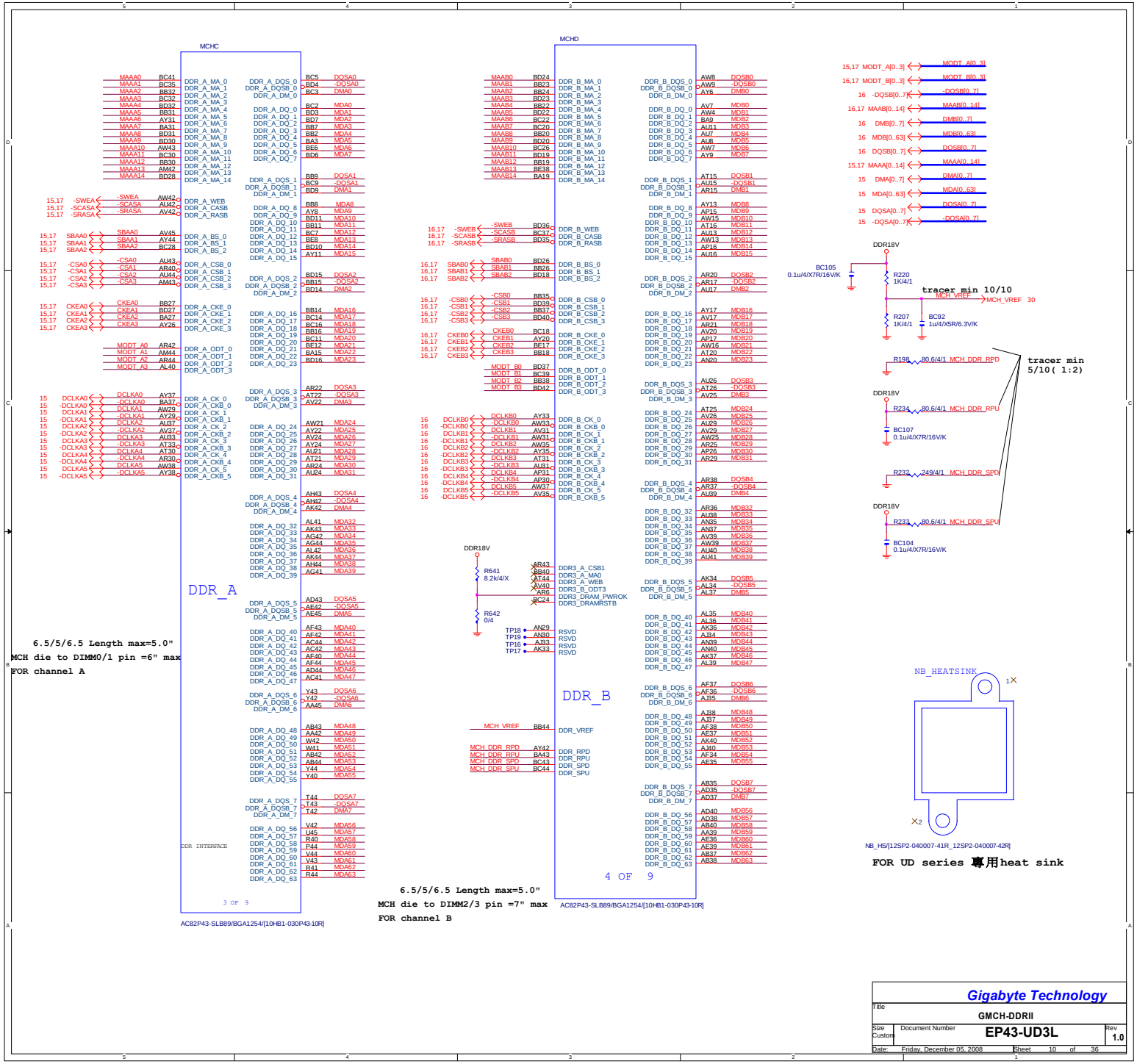


Gigabyte Technology		
Title: P4_LGA775-E,F,G,H		
Size: B	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 8 of 36	



Gigabyte Technology		
Title: GMCH-HOST		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 9 of 36	



Gigabyte Technology		
Title	GMCH-DDRII	
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
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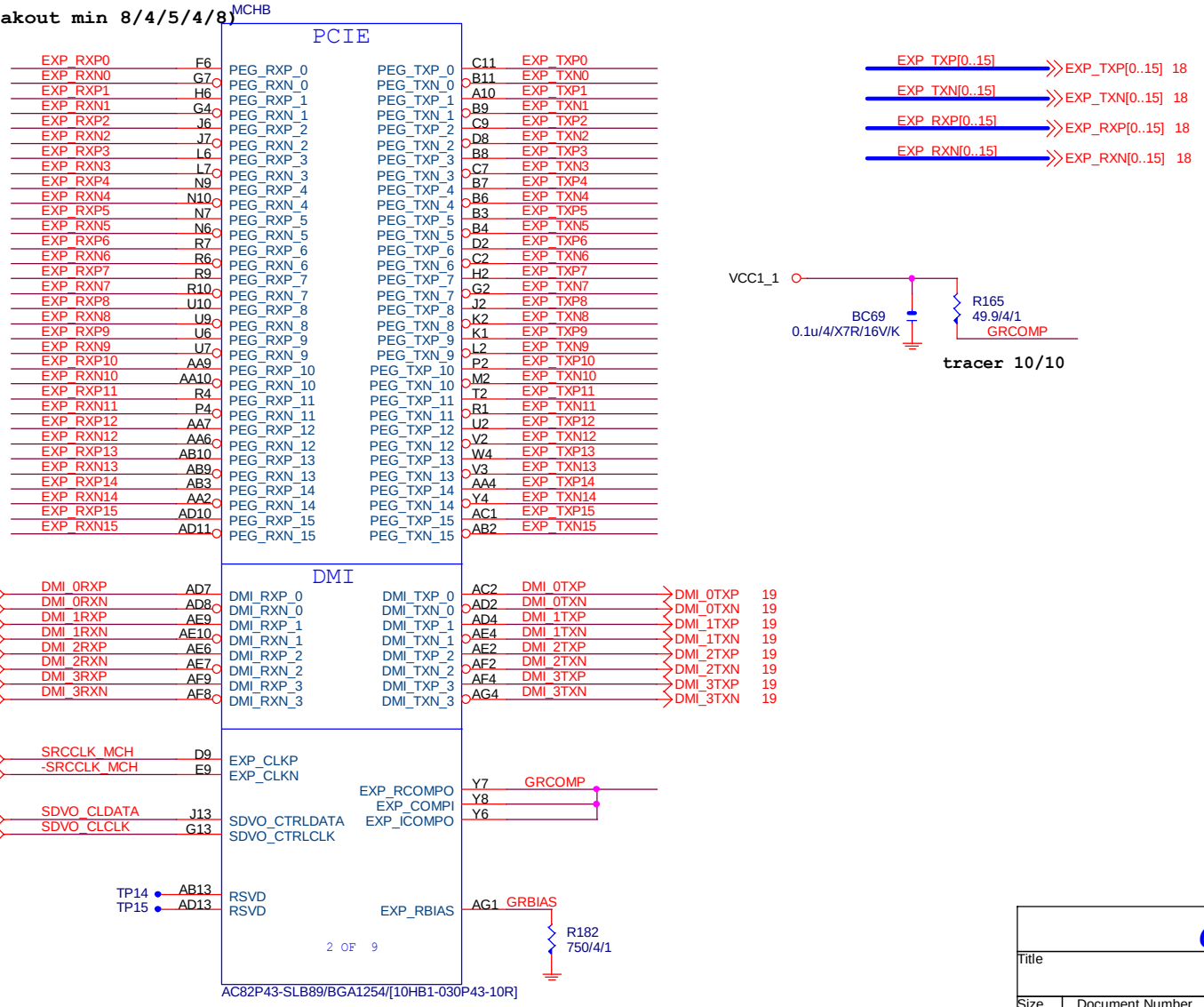
PCIEX16:16/5/5/5/16(breakout min 8/4/5/4/8)

Impedance=85 +- 17.5%

DMI:12/4/8/4/12

Impedance=95 +- 17.5%



Gigabyte Technology		
Title: GMCH-PCI E & DMI		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 11 of 36	

EXP_SM
0:SDVO OR PCIE
1:BOTH SDVO AND PCIE

EXP_SLR:
0:BTX PCIE are reversed
1:ATX PCIE normal

ITPM:
0:ENABLE ITPM
1:DISABLE ITPM

CEN:
0:DISABLE TLS
1:ENABLE TLS

CL_VREF:4/10
0.349V

MCHE

VGA

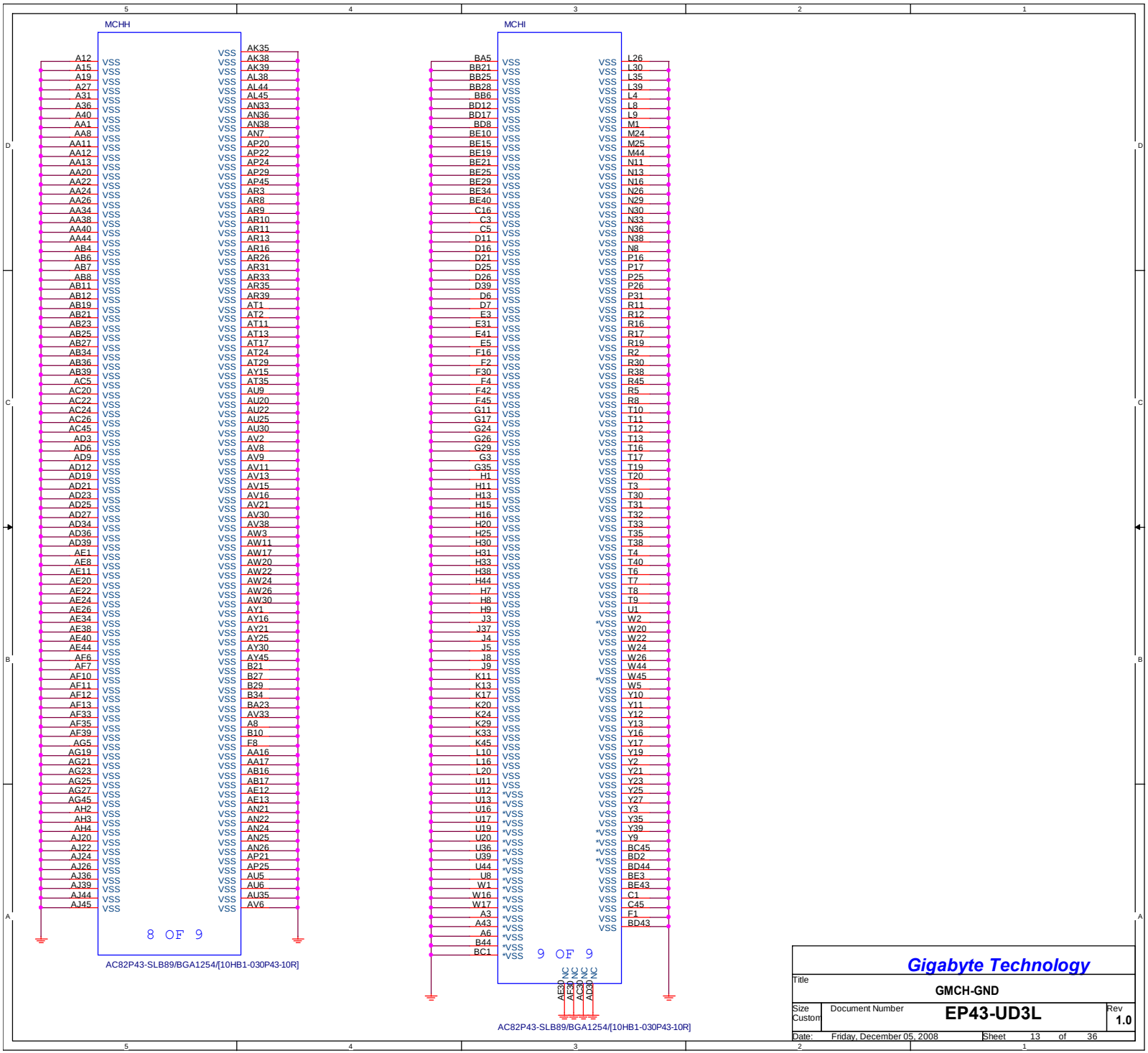
MISC

5 OF 9

AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]

BW+ICH8 不要上(SAMPLE)
BW+ICH7 要上

Gigabyte Technology	
Title	GMCH-INTERNAL VGA
Size: Custom	Document Number: EP43-UD3L
Rev: 1.0	
Date: Friday, December 05, 2008	Sheet 12 of 36


MCHH
A12 A15 A19 A27 A31 A36 A40 AA1 AA8 AA11 AA12 AA13 AA20 AA22 AA24 AA26 AA34 AA38 AA40 AA44 AB4 AB6 AB7 AB8 AB11 AB12 AB19 AB21 AB23 AB25 AB27 AB34 AB36 AB39 AC5 AC20 AC22 AC24 AC26 AC45 AD3 AD6 AD9 AD12 AD19 AD21 AD23 AD25 AD27 AD34 AD36 AD39 AE1 AE8 AE11 AE20 AE22 AE24 AE26 AE34 AE38 AE40 AE44 AF6 AF7 AF10 AF11 AF12 AF13 AF33 AF35 AF39 AG5 AG19 AG21 AG23 AG25 AG27 AG45 AH2 AH3 AH4 AJ20 AJ22 AJ24 AJ26 AJ36 AJ39 AJ44 AJ45
VSS
AK35 AK38 AK39 AL38 AL44 AL45 AN33 AN36 AN38 AN7 AP20 AP22 AP24 AP29 AP45 AR3 AR8 AR9 AR10 AR11 AR13 AR16 AR26 AR31 AR33 AR35 AR39 AT1 AT2 AT11 AT13 AT17 AT24 AT29 AY15 AT35 AU9 AU20 AU22 AU25 AU30 AV2 AV8 AV9 AV11 AV13 AV15 AV16 AV21 AV30 AV38 AW3 AW11 AW17 AW20 AW22 AW24 AW26 AW30 AY1 AY16 AY21 AY25 AY30 AY45 B21 B27 B29 B34 BA23 AV33 A8 B10 F8 AA16 AA17 AB16 AB17 AE12 AE13 AN21 AN22 AN24 AN25 AN26 AP21 AP25 AU5 AU6 AU35 AV6
8 OF 9
AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]
MCHI
BA5 BB21 BB25 BB28 BB6 BD12 BD17 BD8 BE10 BE15 BE19 BE21 BE25 BE29 BE34 BE40 C16 C3 C5 D11 D16 D21 D25 D26 D39 D6 D7 E3 E31 E41 E5 F16 F2 F30 F4 F42 F45 G11 G17 G24 G26 G29 G3 G35 H1 H11 H13 H15 H16 H20 H25 H30 H31 H33 H38 H44 H7 H8 H9 J3 J37 J4 J5 J8 J9 K11 K13 K17 K20 K24 K29 K33 K45 L10 L16 L20 U11 U12 U13 U16 U17 U19 U20 U36 U39 U44 U8 W1 W16 W17 A3 A43 A6 B44 BC1
VSS
*VSS
L26 L30 L35 L39 L4 L8 L9 M1 M24 M25 M44 N11 N13 N16 N26 N29 N30 N33 N36 N38 N8 P16 P17 P25 P26 P31 R11 R12 R16 R17 R19 R2 R30 R38 R45 R5 R8 T10 T11 T12 T13 T16 T17 T19 T20 T3 T30 T31 T32 T33 T35 T38 T4 T40 T6 T7 T8 T9 U1 W2 W20 W22 W24 W26 W44 W45 W5 Y10 Y11 Y12 Y13 Y16 Y17 Y19 Y2 Y21 Y23 Y25 Y27 Y3 Y35 Y39 Y9 BC45 BD2 BD44 BE3 BE43 C1 C45 F1 BD43
9 OF 9
NC
AE20 AE30 AE35 AC30 AD30
AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]
Gigabyte Technology
Title
GMCH-GND
Size
Custom
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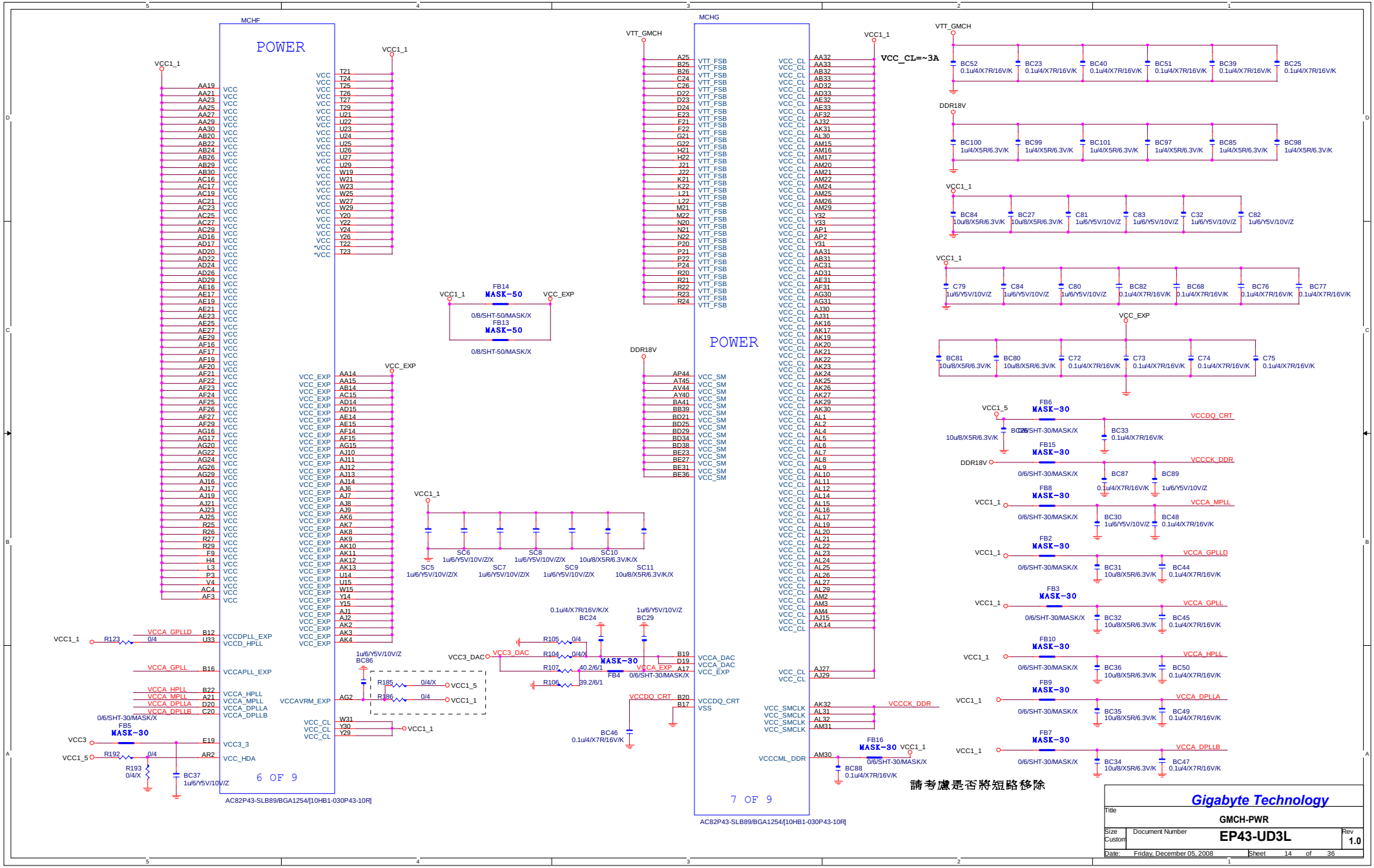
MCHF
POWER
6 OF 9
AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]
MCHG
POWER
7 OF 9
AC82P43-SLB89/BGA1254/[10HB1-030P43-10R]
VCC_CL=~3A
請考慮是否將短路移除
Gigabyte Technology
Title
GMCH-PWR
Size
Custom
Document Number
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Rev
1.0
Date: Friday, December 05, 2008
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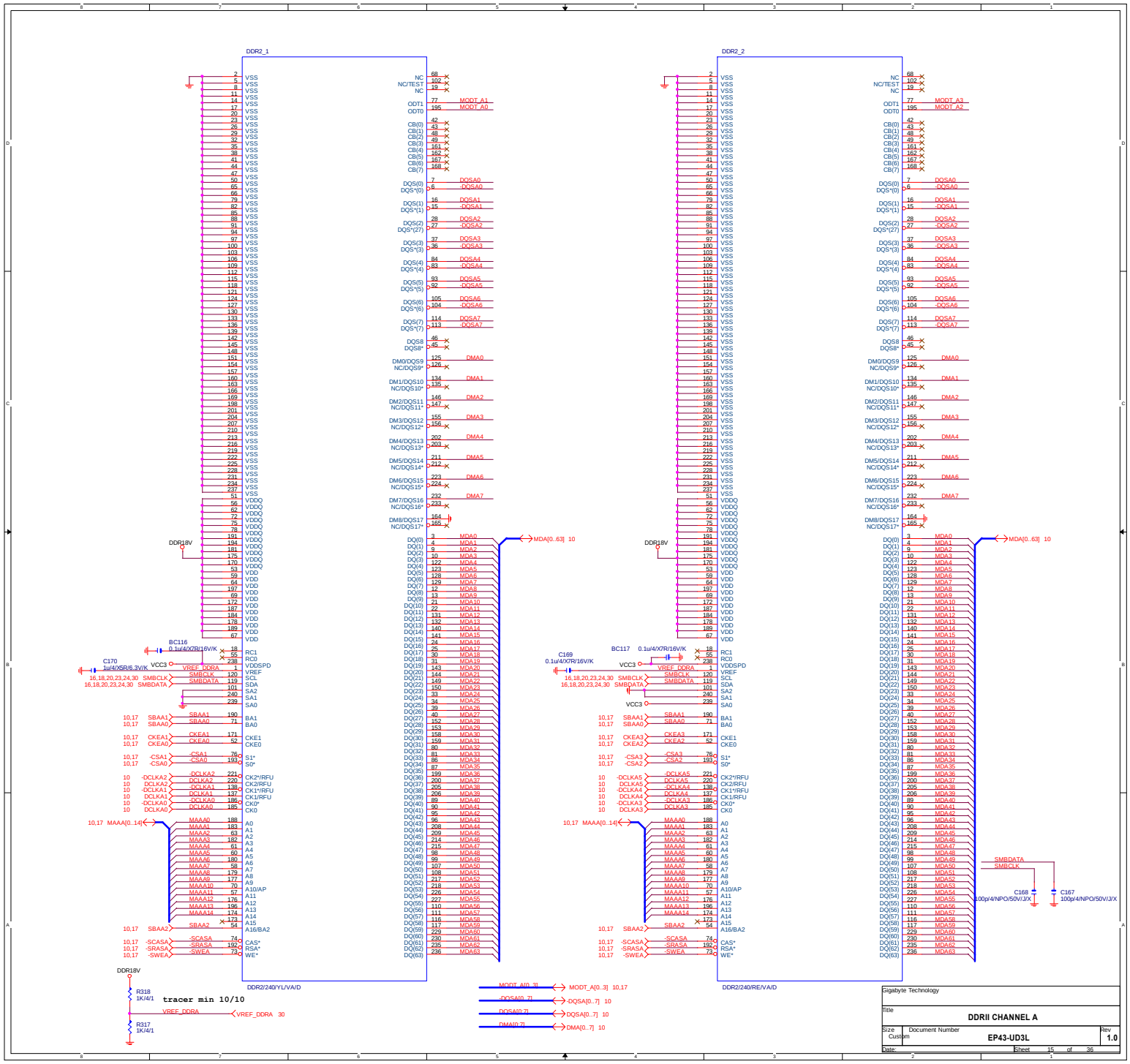
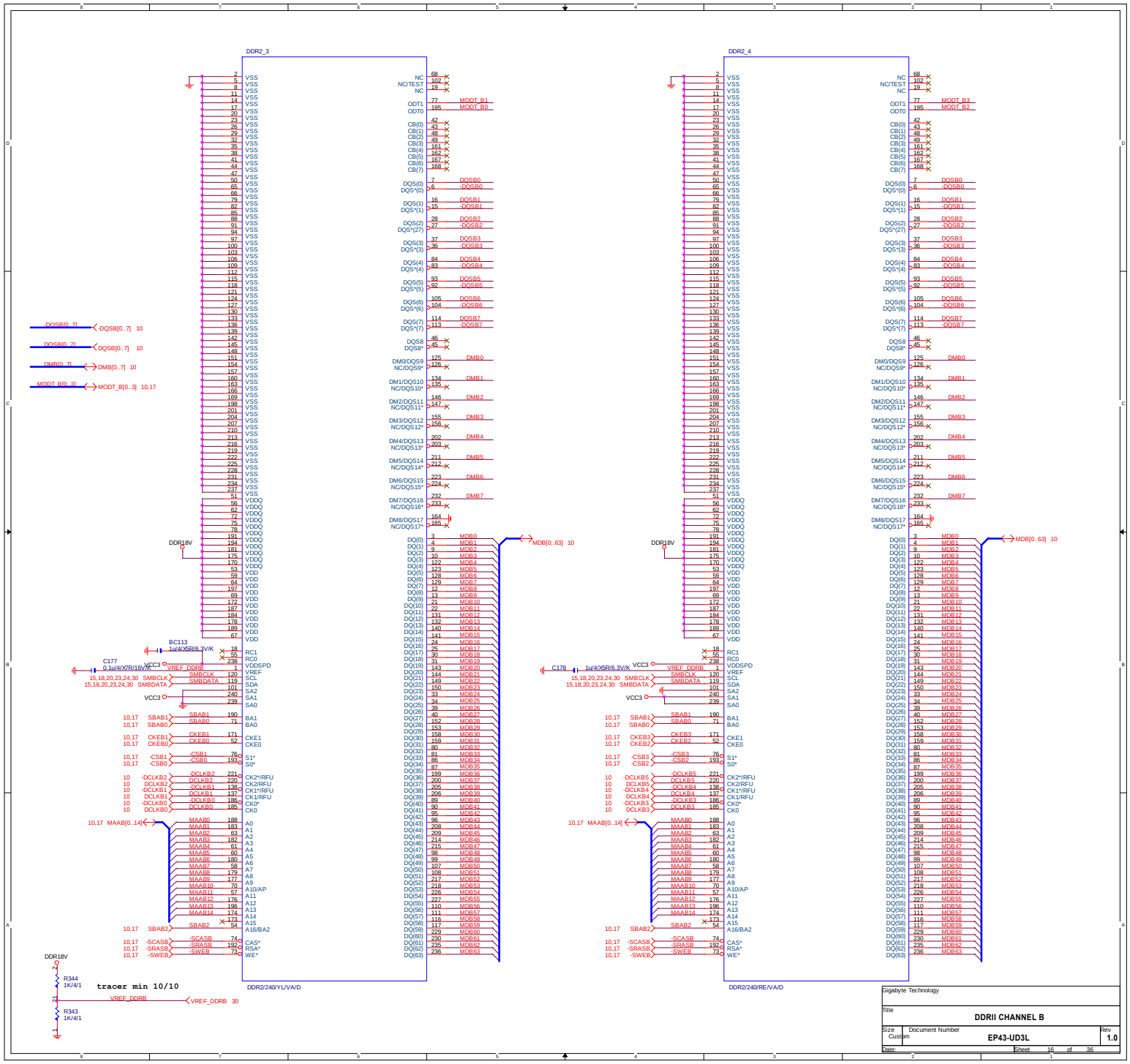
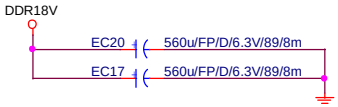
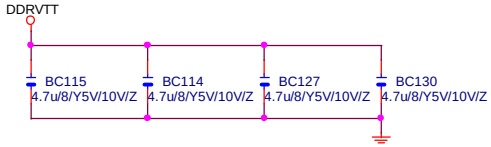

DDR2_1
DDR2_2
DDR2/240/YL/VA/D
DDR2/240/RE/VA/D
DDR18V
VREF_DDRA
SMBCLK
SMBDATA
VCC3
BC116 0.1u/4/X7R/16V/K
BC117 0.1u/4/X7R/16V/K
C169 0.1u/4/X7R/16V/K
C170 1u/4/X5R/6.3V/K
C168 100p/4/NPO/50V/J/X
C167 100p/4/NPO/50V/J/X
R318 1K/4/1
R317 1K/4/1
tracer min 10/10
MDA[0..63] 10
MODT_A[0..3] 10,17
DQSA[0..7] 10
DMA[0..7] 10
Gigabyte Technology
DDRII CHANNEL A
EP43-UD3L
Size Custom
Document Number
Rev 1.0
Date:
Sheet 15 of 36


DDR2_3
DDR2_4
DDR18V
VCC3
MDB[0..63] 10
DDR2/240/YL/VA/D
DDR2/240/RE/VA/D
tracer min 10/10
R344
1K/4/1
R343
1K/4/1
VREF_DDRB
VREF_DDRB 30
Gigabyte Technology
Title
DDRII CHANNEL B
Size
Custom
Document Number
EP43-UD3L
Rev
1.0
Date:
Sheet 16 of 36

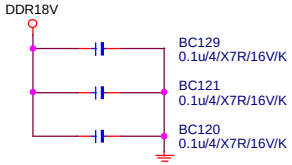
DDR TERMINATION CHANNEL A

DDRVTT Decouple

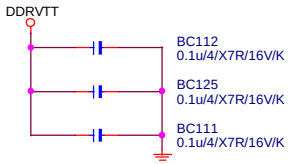


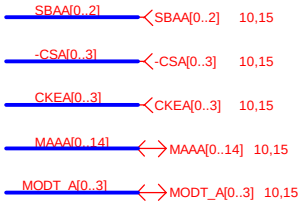


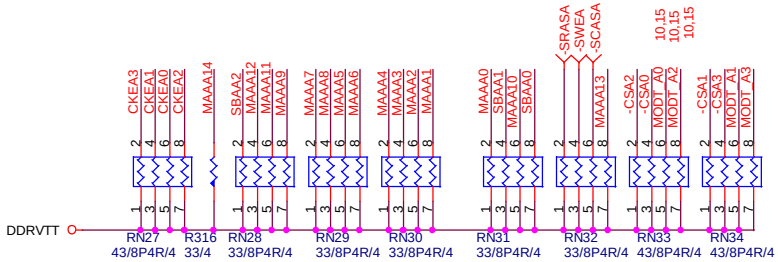
DDR18V Decouple



DDRVTT Decouple

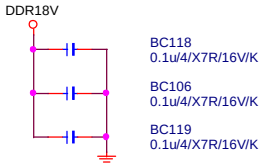




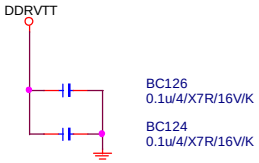


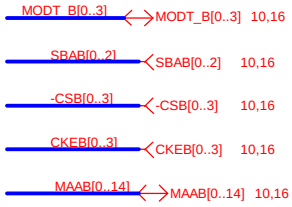
DDR TERMINATION CHANNEL B

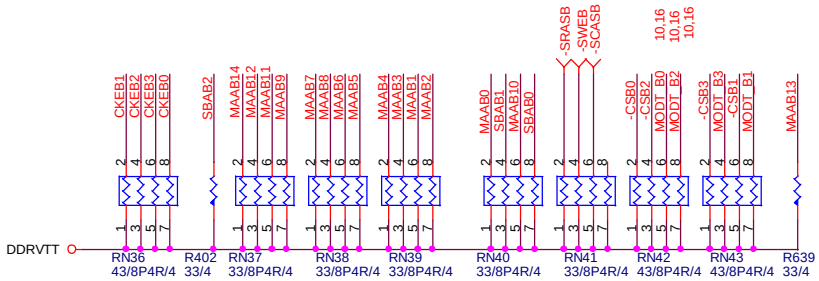
DDR18V Decouple



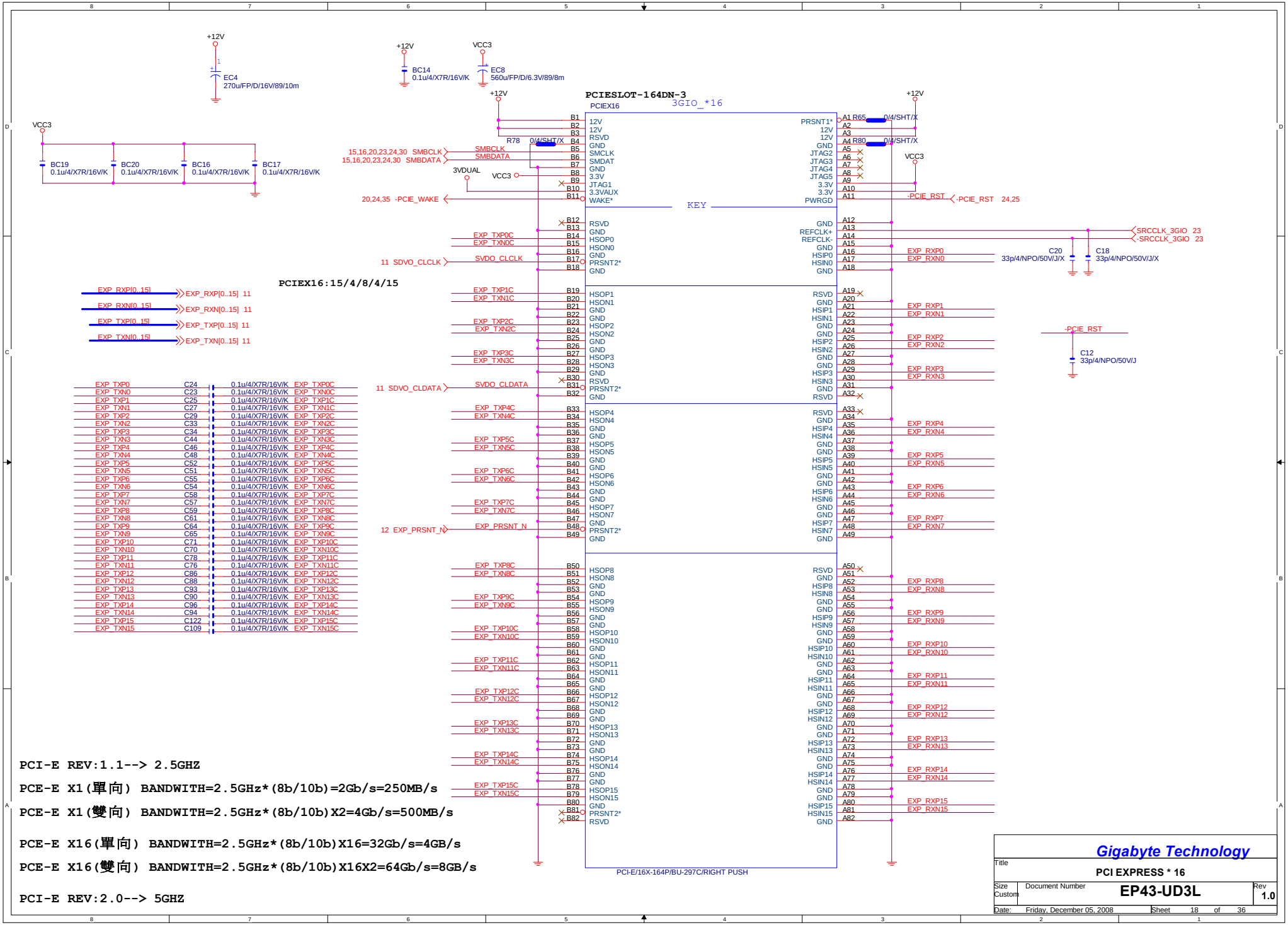
DDRVTT Decouple







Gigabyte Technology		
Title: DDRII TERMINATOR		
Size: Custom	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 17 of 36	


PCIESLOT-164DN-3
PCIEX16
3GIO_*16
KEY
PCIEX16:15/4/8/4/15
PCI-E/16X-164P/BU-297C/RIGHT PUSH
+12V
VCC3
3VDUAL
EC4 270u/FP/D/16V/89/10m
BC14 0.1u/4/X7R/16V/K
EC8 560u/FP/D/6.3V/89/8m
BC19 0.1u/4/X7R/16V/K
BC20 0.1u/4/X7R/16V/K
BC16 0.1u/4/X7R/16V/K
BC17 0.1u/4/X7R/16V/K
R78 0/4/SHT/X
R65 0/4/SHT/X
R80 0/4/SHT/X
SMBCLK
SMBDATA
15,16,20,23,24,30 SMBCLK
15,16,20,23,24,30 SMBDATA
20,24,35 -PCIE_WAKE
-PCIE_RST
-PCIE_RST 24,25
11 SDVO_CLCLK
11 SDVO_CLDATA
12 EXP_PRSNT_N
SRCCLK_3GIO 23
-SRCCLK_3GIO 23
C20 33p/4/NPO/50V/J/X
C18 33p/4/NPO/50V/J/X
C12 33p/4/NPO/50V/J
EXP_RXP[0..15] 11
EXP_RXN[0..15] 11
EXP_TXP[0..15] 11
EXP_TXN[0..15] 11
PCI-E REV:1.1--> 2.5GHZ
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s
PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s
PCI-E REV:2.0--> 5GHZ
Gigabyte Technology
Title
PCI EXPRESS * 16
Size Custom
Document Number
EP43-UD3L
Rev 1.0
Date: Friday, December 05, 2008
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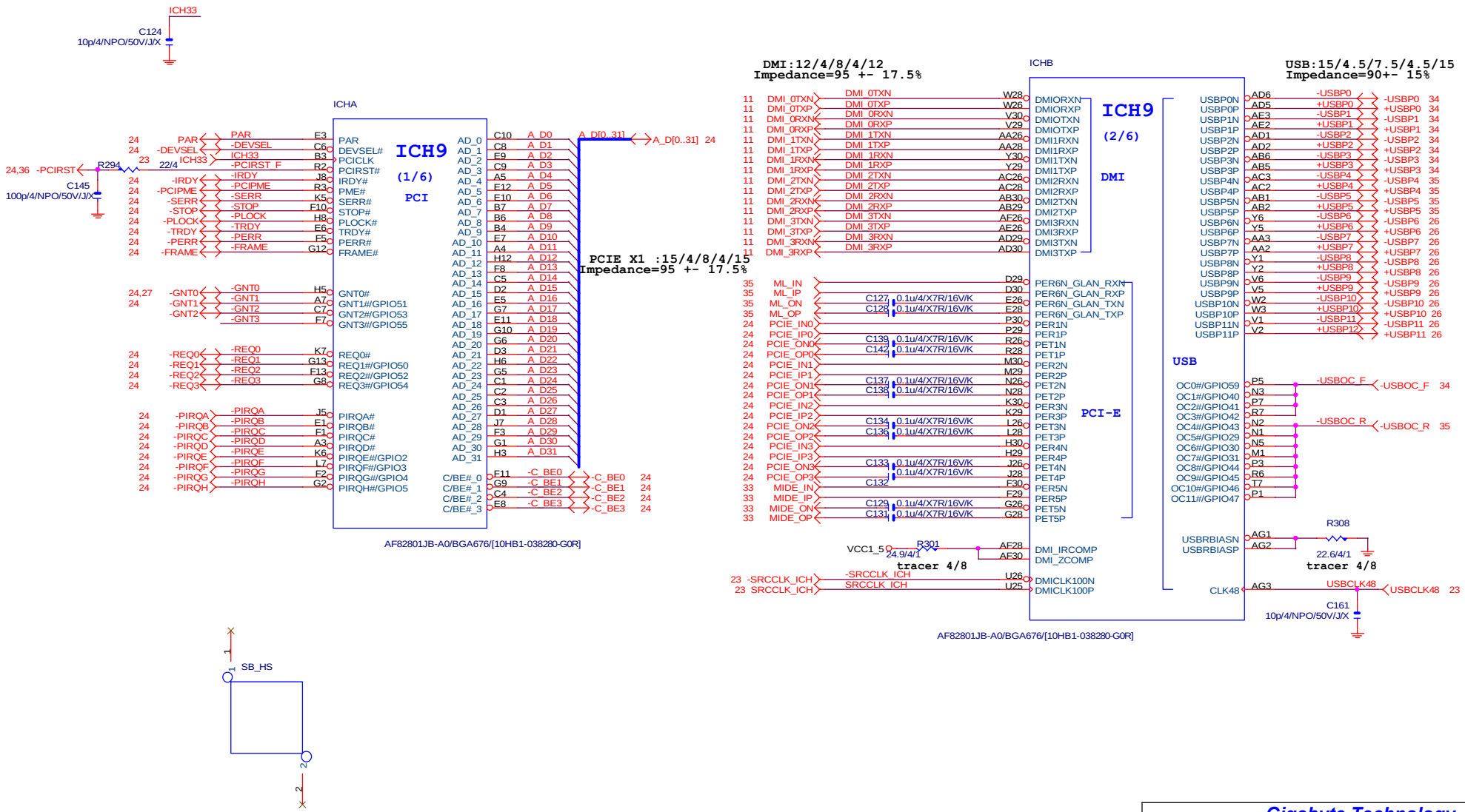
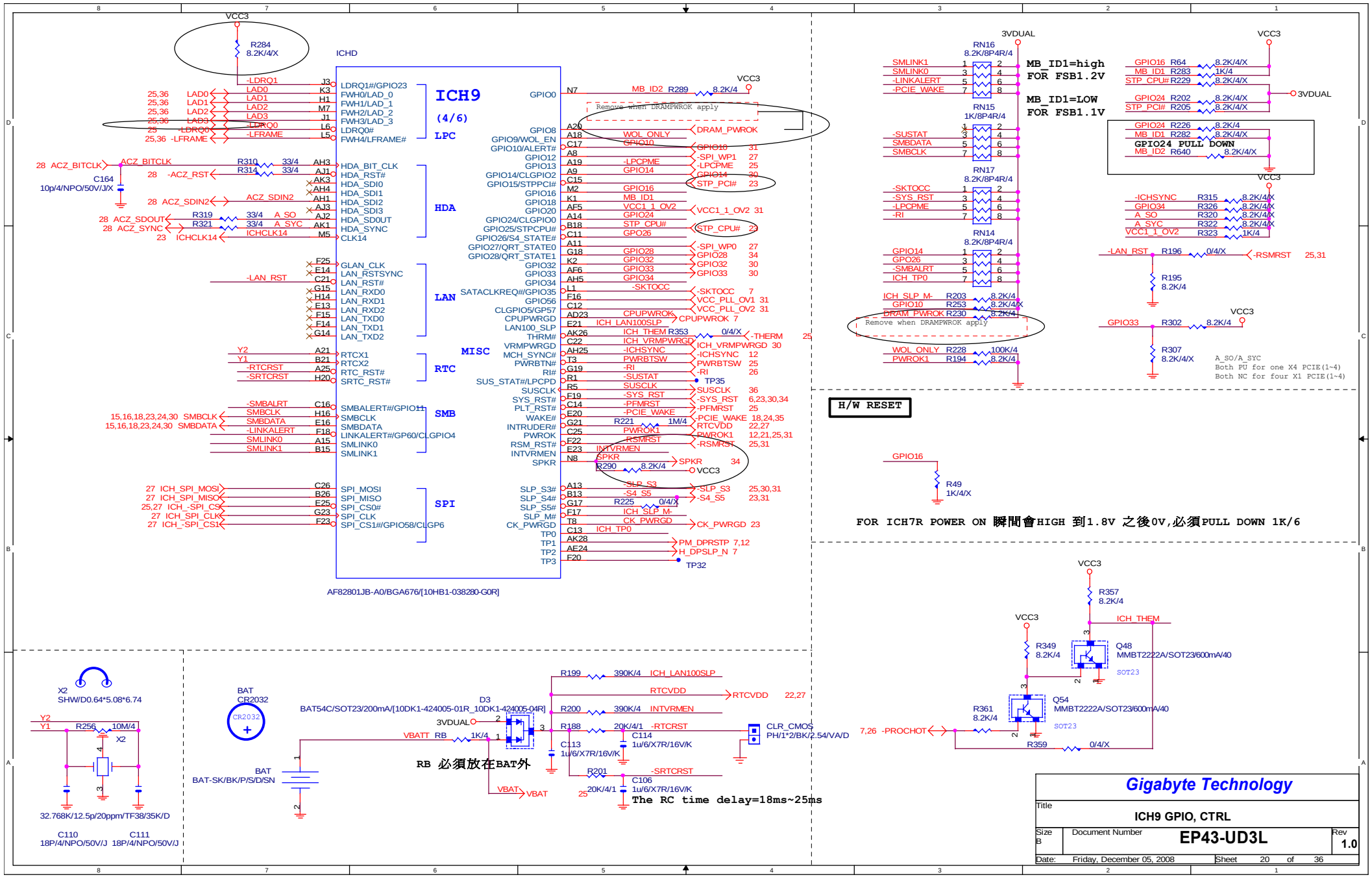
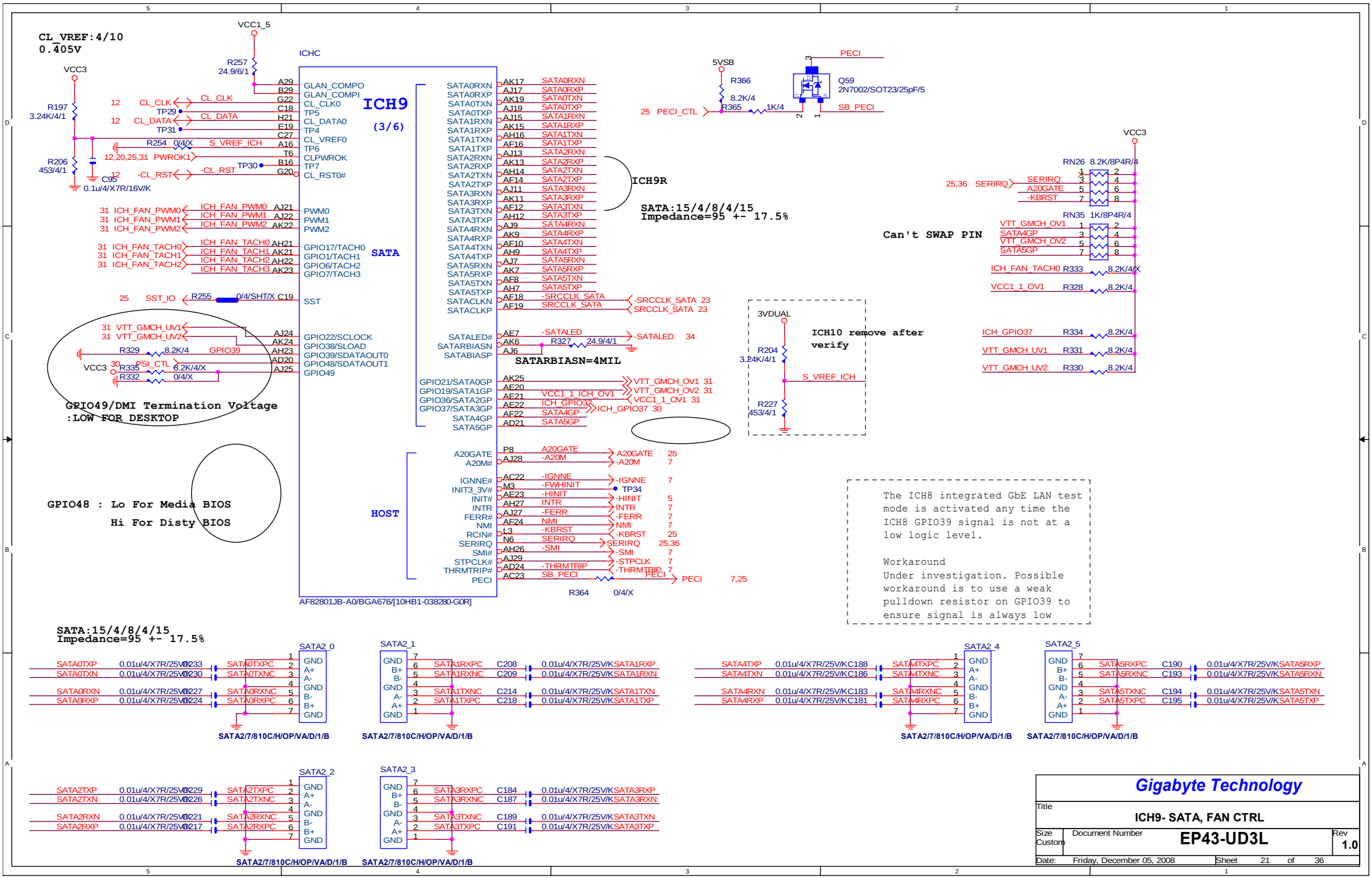


Gigabyte Technology		
Title	ICH9-PCI, DMI, LAN, USB	
Size B	Document Number EP43-UD3L	Rev 1.0
Date: Friday, December 05, 2008	Sheet 19 of 36	


ICH9
(4/6)
LPC
HDA
LAN
RTC
SMB
SPI
MISC
AF82801JB-A0/BGA676/[10HB1-038280-G0R]
MB_ID1=high
FOR FSB1.2V
MB_ID1=LOW
FOR FSB1.1V
GPIO24 PULL DOWN
H/W RESET
FOR ICH7R POWER ON 瞬間會HIGH 到1.8V 之後0V,必須PULL DOWN 1K/6
RB 必須放在BAT外
The RC time delay=18ms~25ms
Gigabyte Technology
ICH9 GPIO, CTRL
EP43-UD3L
Rev 1.0
Friday, December 05, 2008
Sheet 20 of 36


CL_VREF:4/10
0.405V
VCC1_5
R257
24.9/6/1
ICHC
VCC3
R197
3.24K/4/1
R206
453/4/1
C95
0.1u/4/X7R/16V/K
CL_CLK
CL_DATA
R254 0/4/X
S_VREF_ICH
PWROK1
TP30
-CL_RST
GLAN_COMPO
GLAN_COMPI
CL_CLK0
TP5
CL_DATA0
TP4
CL_VREF0
TP6
CLPWROK
TP7
CL_RST0#
ICH9
(3/6)
ICH_FAN_PWM0
ICH_FAN_PWM1
ICH_FAN_PWM2
PWM0
PWM1
PWM2
ICH_FAN_TACH0
ICH_FAN_TACH1
ICH_FAN_TACH2
ICH_FAN_TACH3
GPIO17/TACH0
GPIO1/TACH1
GPIO6/TACH2
GPIO7/TACH3
SATA
SST_IO
R255 0/4/SHT/X
C19
SST
VTT_GMCH_UV1
VTT_GMCH_UV2
GPIO22/SCLOCK
GPIO38/SLOAD
GPIO39/SDATAOUT0
GPIO48/SDATAOUT1
GPIO49
R329 8.2K/4
GPIO39
PSI_CTL
R335 8.2K/4/X
R332 0/4/X
GPIO49/DMI Termination Voltage
:LOW FOR DESKTOP
GPIO48 : Lo For Media BIOS
Hi For Disty BIOS
HOST
AF82801JB-A0/BGA676/[10HB1-038280-G0R]
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATACLKN
SATACLKP
ICH9R
SATA:15/4/8/4/15
Impedance=95 +- 17.5%
SATALED#
SATARBIASN
SATARBIASP
R327 24.9/4/1
SATARBIASN=4MIL
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
SATA4GP
SATA5GP
A20GATE
A20M#
IGNNE#
INIT3_3V#
INIT#
INTR
FERR#
NMI
RCIN#
SERIRQ
SMI#
STPCLK#
THRMTRIP#
PECI
R364 0/4/X
5VSB
R366 8.2K/4
R365 1K/4
PECI_CTL
SB_PECI
Q59
2N7002/SOT23/25pF/5
3VDUAL
R204 3.24K/4/1
R227 453/4/1
S_VREF_ICH
ICH10 remove after
verify
Can't SWAP PIN
RN26 8.2K/8P4R/4
RN35 1K/8P4R/4
SERIRQ
A20GATE
-KBRST
VTT_GMCH_OV1
SATA4GP
VTT_GMCH_OV2
SATA5GP
ICH_FAN_TACH0 R333 8.2K/4/X
VCC1_1_OV1 R328 8.2K/4
ICH_GPIO37 R334 8.2K/4
VTT_GMCH_UV1 R331 8.2K/4
VTT_GMCH_UV2 R330 8.2K/4
The ICH8 integrated GbE LAN test mode is activated any time the ICH8 GPIO39 signal is not at a low logic level.
Workaround
Under investigation. Possible workaround is to use a weak pulldown resistor on GPIO39 to ensure signal is always low
SATA:15/4/8/4/15
Impedance=95 +- 17.5%
SATA2_0
SATA2_1
SATA2_2
SATA2_3
SATA2_4
SATA2_5
SATA2/7/810C/H/OP/VA/D/1/B
Gigabyte Technology
Title
ICH9- SATA, FAN CTRL
Size
Custom
Document Number
EP43-UD3L
Rev
1.0
Date: Friday, December 05, 2008
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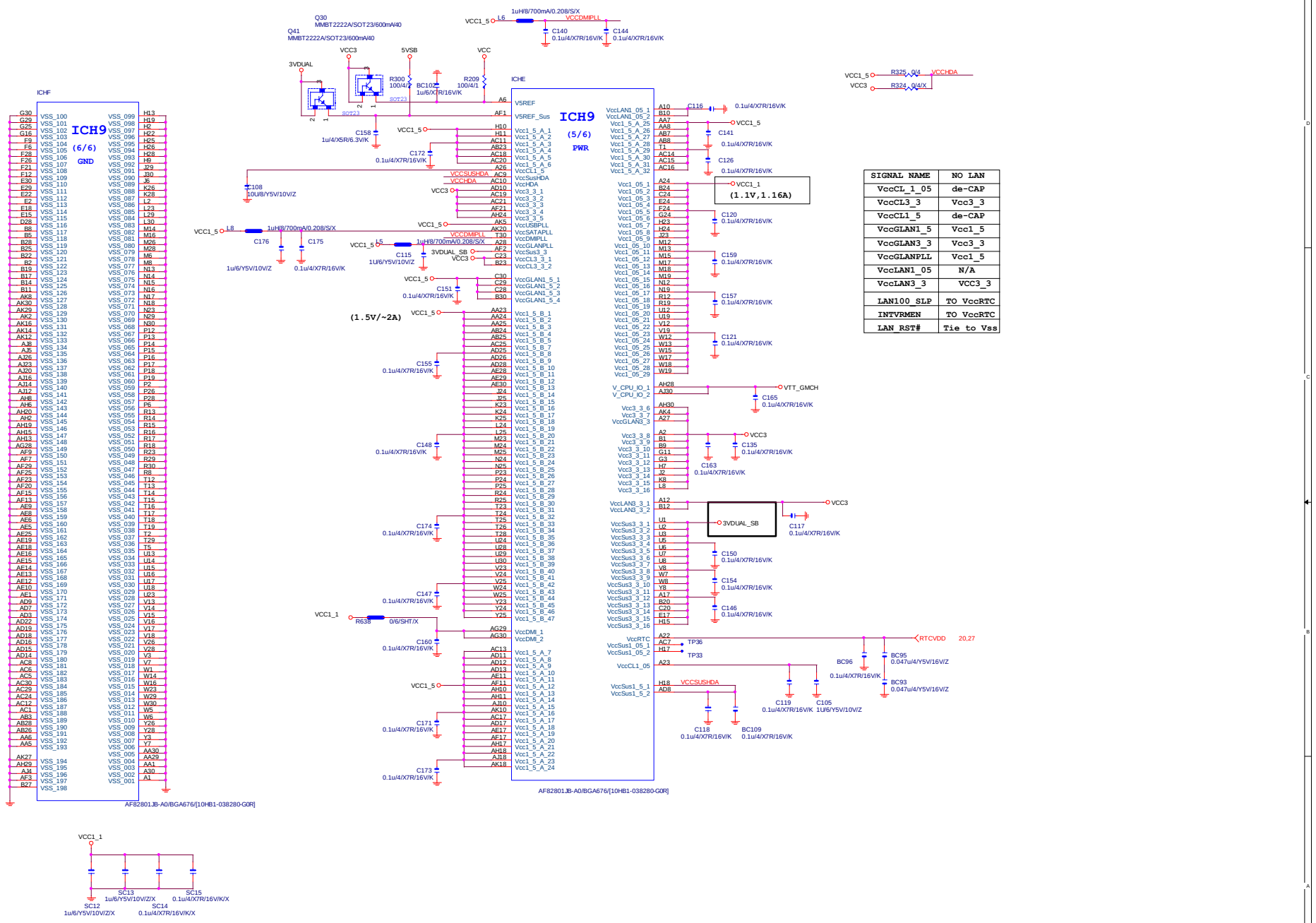
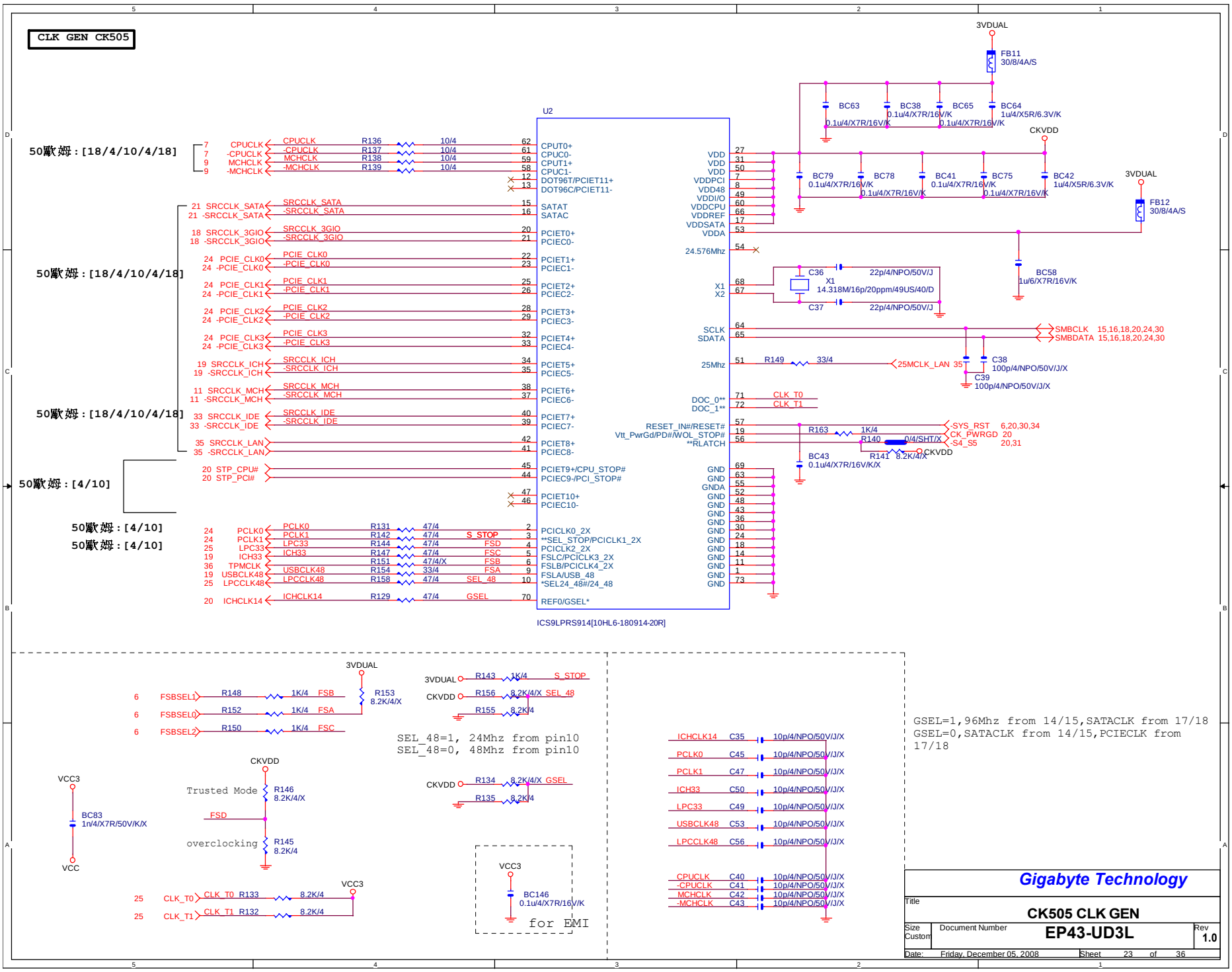


SIGNAL NAME	NO LAN
VccCL_1_05	de-CAP
VccCL3_3	Vcc3_3
VccCL1_5	de-CAP
VccGLAN1_5	Vcc1_5
VccGLAN3_3	Vcc3_3
VccGLANPLL	Vcc1_5
VccLAN1_05	N/A
VccLAN3_3	VCC3_3
LAN100_SLP	TO VccRTC
INTVRMEN	TO VccRTC
LAN_RST#	Tie to Vss

Gigabyte Technology

Title	ICH9-PWR & GND	
Size: C	Document Number: EP43-UD3L	Rev: 1.0
Date: Friday, December 05, 2008	Sheet 22 of 36	


CLK GEN CK505
U2
ICS9LPRS914[10HL6-180914-20R]
50歐姆:[18/4/10/4/18]
50歐姆:[18/4/10/4/18]
50歐姆:[18/4/10/4/18]
50歐姆:[4/10]
50歐姆:[4/10]
50歐姆:[4/10]
3VDUAL
FB11 30/8/4A/S
FB12 30/8/4A/S
CKVDD
BC63 0.1u/4/X7R/16V/K
BC38 0.1u/4/X7R/16V/K
BC65 0.1u/4/X7R/16V/K
BC64 1u/4/X5R/6.3V/K
BC79 0.1u/4/X7R/16V/K
BC78 0.1u/4/X7R/16V/K
BC41 0.1u/4/X7R/16V/K
BC75 0.1u/4/X7R/16V/K
BC42 1u/4/X5R/6.3V/K
BC58 1u/6/X7R/16V/K
C36 22p/4/NPO/50V/J
C37 22p/4/NPO/50V/J
X1 14.318M/16p/20ppm/49US/40/D
C38 100p/4/NPO/50V/J/X
C39 100p/4/NPO/50V/J/X
BC43 0.1u/4/X7R/16V/K/X
R163 1K/4
R140 0/4/SHT/X
R141 8.2K/4/X
R149 33/4
SMBCLK 15,16,18,20,24,30
SMBDATA 15,16,18,20,24,30
-SYS_RST 6,20,30,34
CK_PWRGD 20
-S4_S5 20,31
25MCLK_LAN 35
CPUCLK
-CPUCLK
MCHCLK
-MCHCLK
SRCCLK_SATA
-SRCCLK_SATA
SRCCLK_3GIO
-SRCCLK_3GIO
PCIE_CLK0
-PCIE_CLK0
PCIE_CLK1
-PCIE_CLK1
PCIE_CLK2
-PCIE_CLK2
PCIE_CLK3
-PCIE_CLK3
SRCCLK_ICH
-SRCCLK_ICH
SRCCLK_MCH
-SRCCLK_MCH
SRCCLK_IDE
-SRCCLK_IDE
SRCCLK_LAN
-SRCCLK_LAN
STP_CPU#
STP_PCI#
CLK_T0
CLK_T1
PCLK0
PCLK1
LPC33
ICH33
TPMCLK
USBCLK48
LPCCLK48
ICHCLK14
R136 10/4
R137 10/4
R138 10/4
R139 10/4
R131 47/4
R142 47/4
R144 47/4
R147 47/4
R151 47/4/X
R154 33/4
R158 47/4
R129 47/4
S_STOP
FSD
FSC
FSB
FSA
SEL_48
GSEL
R148 1K/4 FSB
R152 1K/4 FSA
R150 1K/4 FSC
R153 8.2K/4/X
FSBSEL1
FSBSEL0
FSBSEL2
R143 1K/4 S_STOP
R156 8.2K/4/X SEL_48
R155 8.2K/4
SEL_48=1, 24Mhz from pin10
SEL_48=0, 48Mhz from pin10
R134 8.2K/4/X GSEL
R135 8.2K/4
Trusted Mode
overclocking
R146 8.2K/4/X
R145 8.2K/4
BC83 1n/4/X7R/50V/K/X
R133 8.2K/4
R132 8.2K/4
BC146 0.1u/4/X7R/16V/K
for EMI
ICHCLK14 C35 10p/4/NPO/50V/J/X
PCLK0 C45 10p/4/NPO/50V/J/X
PCLK1 C47 10p/4/NPO/50V/J/X
ICH33 C50 10p/4/NPO/50V/J/X
LPC33 C49 10p/4/NPO/50V/J/X
USBCLK48 C53 10p/4/NPO/50V/J/X
LPCCLK48 C56 10p/4/NPO/50V/J/X
CPUCLK C40 10p/4/NPO/50V/J/X
-CPUCLK C41 10p/4/NPO/50V/J/X
MCHCLK C42 10p/4/NPO/50V/J/X
-MCHCLK C43 10p/4/NPO/50V/J/X
GSEL=1,96Mhz from 14/15,SATACLK from 17/18
GSEL=0,SATACLK from 14/15,PCIECLK from 17/18
Gigabyte Technology
Title
CK505 CLK GEN
Size Custom
Document Number
EP43-UD3L
Rev 1.0
Date: Friday, December 05, 2008
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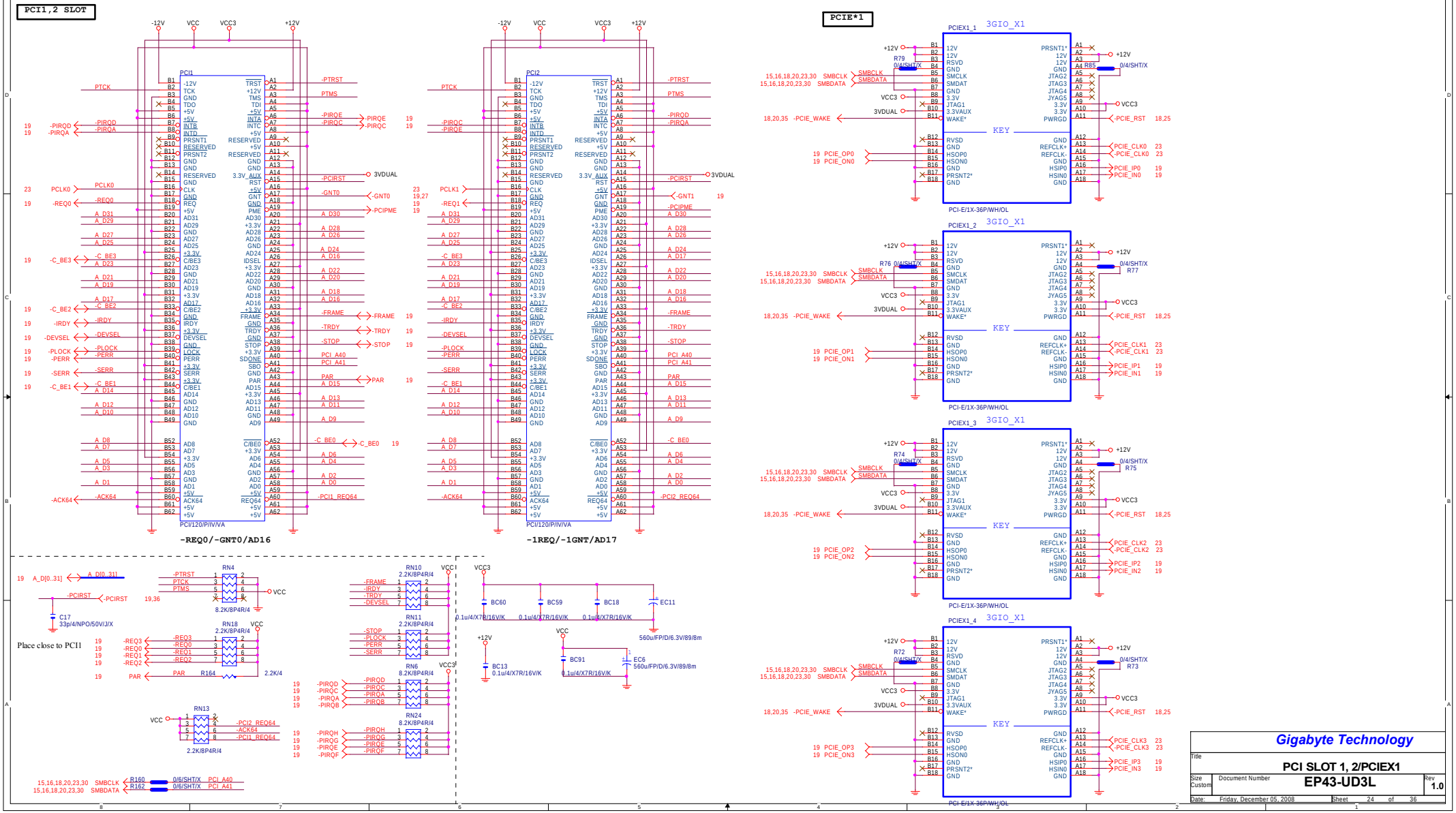
PCI1,2 SLOT
PCI1
PCI2
PCI120/P/IV/VA
-REQ0/-GNT0/AD16
-1REQ/-1GNT/AD17
PCIE*1
PCIEX1_1
PCIEX1_2
PCIEX1_3
PCIEX1_4
3GIO_X1
PCI-E/1X-36P/WH/OL
KEY
Place close to PCI1
Gigabyte Technology
PCI SLOT 1, 2/PCIEX1
EP43-UD3L
Rev 1.0
Friday, December 05, 2008
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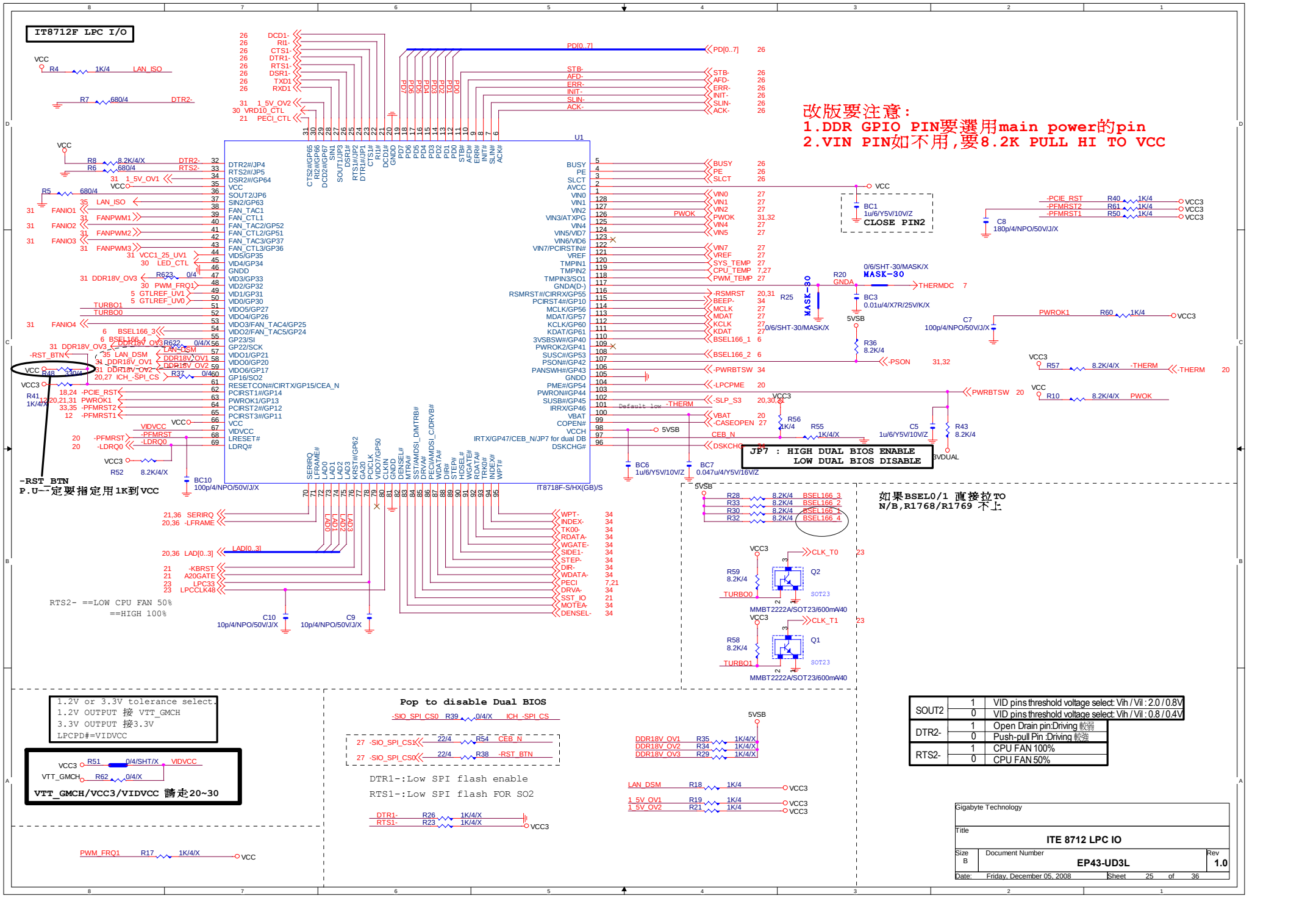
IT8712F LPC I/O
改版要注意:
1.DDR GPIO PIN要選用main power的pin
2.VIN PIN如不用,要8.2K PULL HI TO VCC
U1
IT8718F-S/HX(GB)/S
-RST_BTN
P.U一定要指定用1K到VCC
JP7 : HIGH DUAL BIOS ENABLE
LOW DUAL BIOS DISABLE
如果BSEL0/1 直接拉TO
N/B,R1768/R1769 不上
RTS2- ==LOW CPU FAN 50%
==HIGH 100%
1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接3.3V
LPCPD#=VIDVCC
VTT_GMCH/VCC3/VIDVCC 請走20~30
Pop to disable Dual BIOS
DTR1-:Low SPI flash enable
RTS1-:Low SPI flash FOR SO2
CLOSE PIN2
MASK-30
SOUT2
DTR2-
RTS2-
Gigabyte Technology
ITE 8712 LPC IO
EP43-UD3L
1.0
Friday, December 05, 2008
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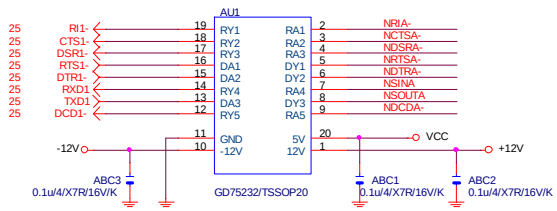
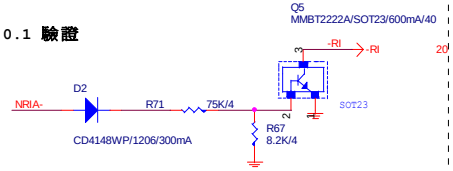
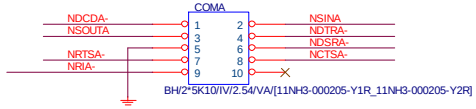
COMA

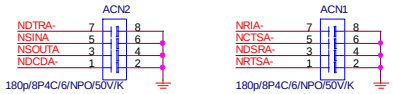


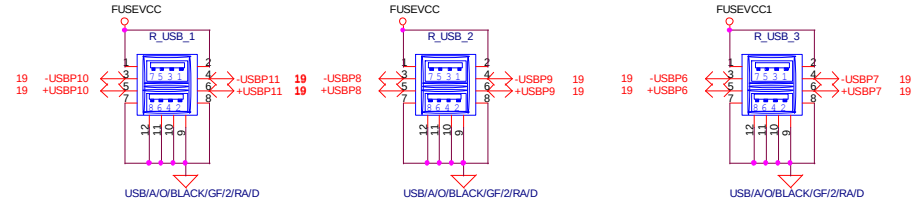
COM RI

REV:0.1 驗證

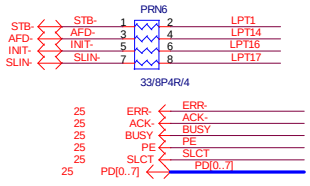


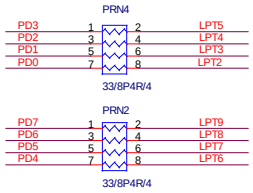


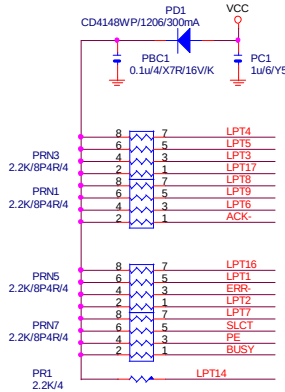


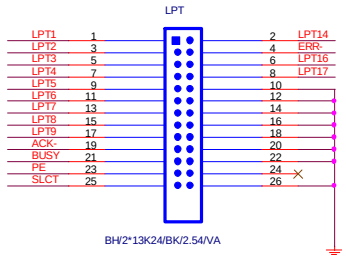


LPT PORT

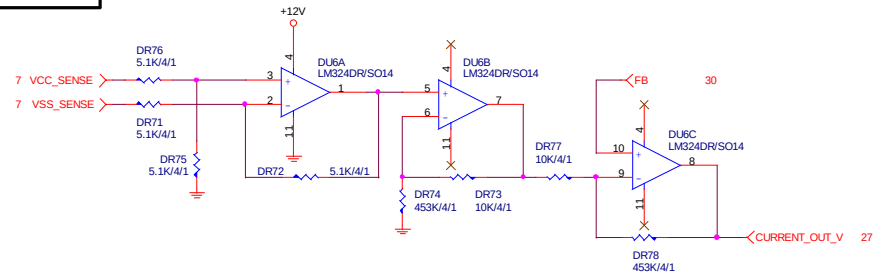








DYNAMIC CURRENT OC

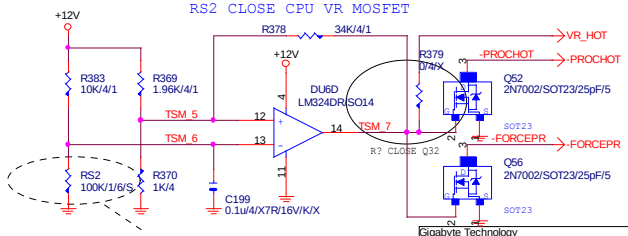


-PROHOT

asserted at 129 degree

deasserted at 116 degree

RS2 CLOSE CPU VR MOSFET



CLOSE PWM HOT MOSFET

Gigabyte Technology

Title: COM & LPT PORT

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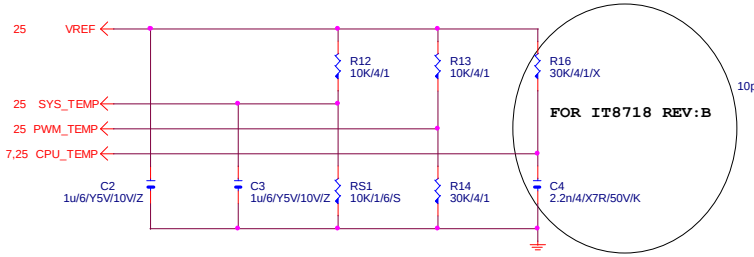
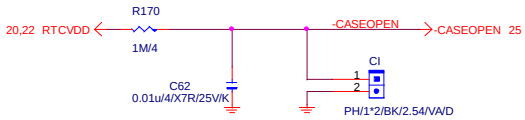
TEMP H/W MONITOR

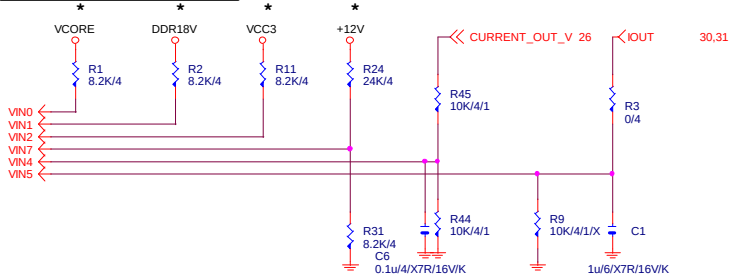


CASE OPEN

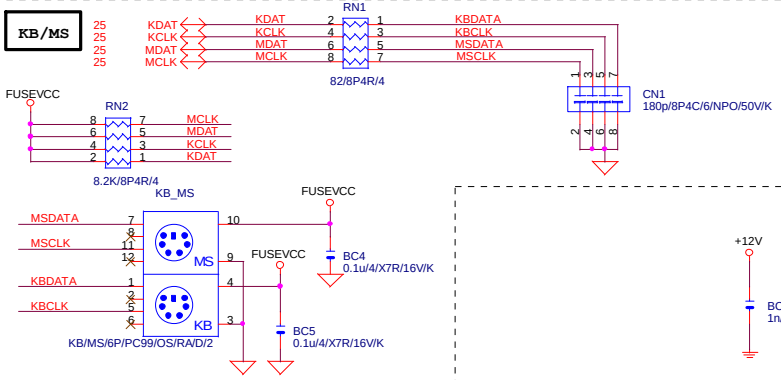


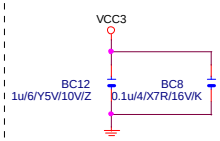
Case Open Circuits

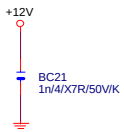
VOLTAGE-- H/W MONITOR

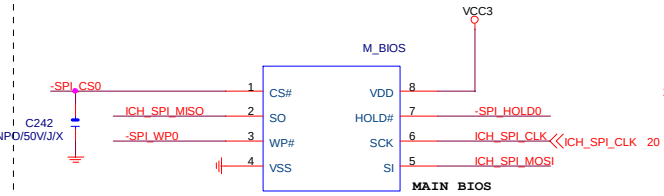


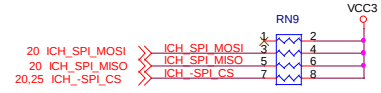
KB/MS

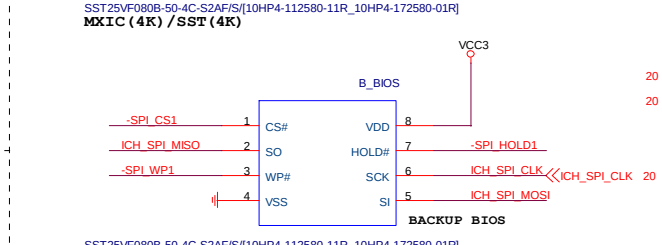


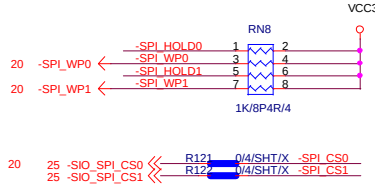




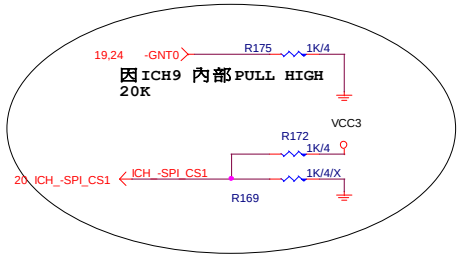








BOOT DEVICE	GNT0	CS1
SPI	0	1
PCI	1	0
FWH	1	1



Gigabyte Technology		
Title: BIOS/HW-MONITOR/CI/KB/MS		
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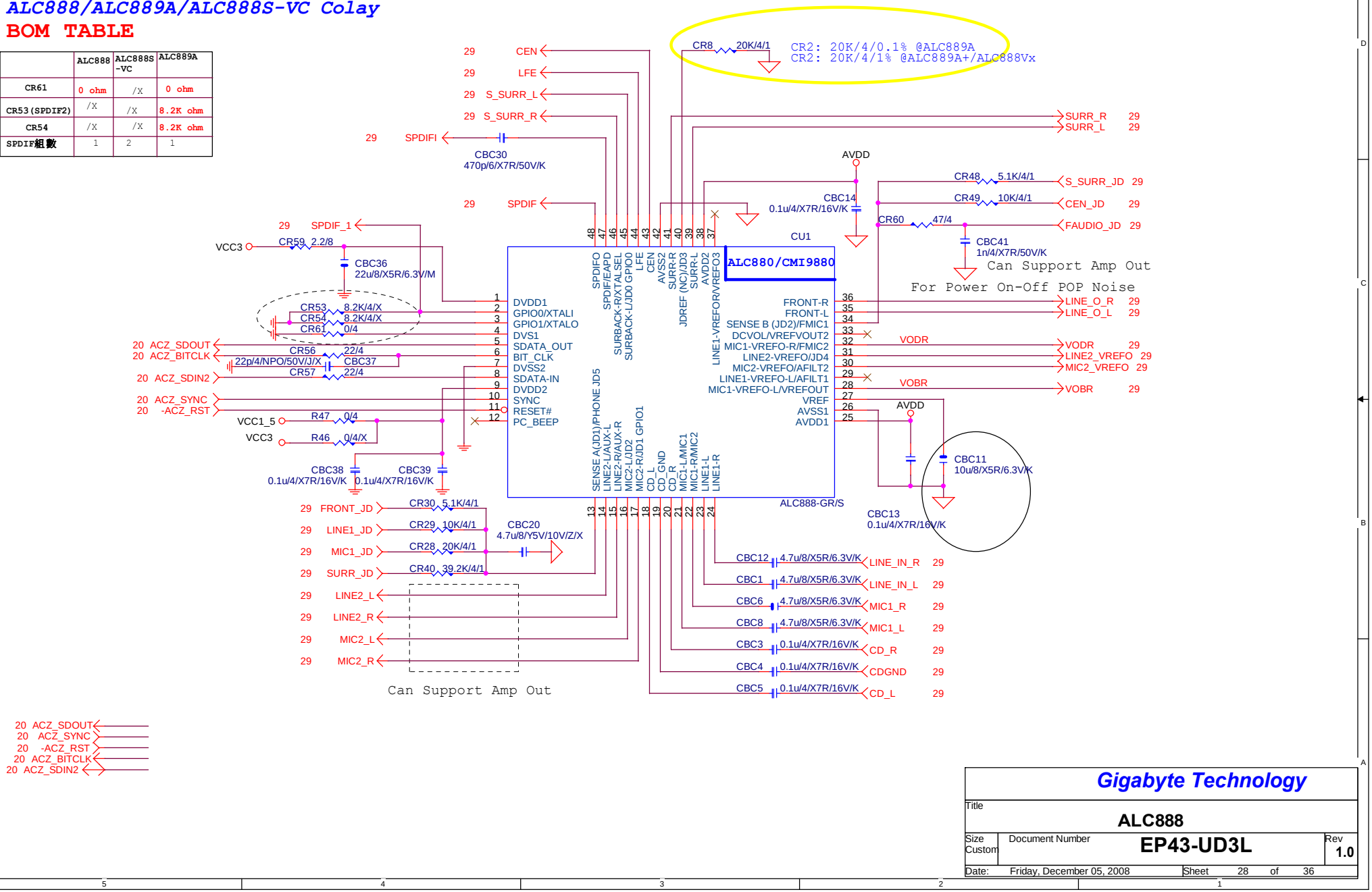
AZALIA CODEC

ALC888/ALC889A/ALC888S-VC Colay

BOM TABLE

	ALC888	ALC888S-VC	ALC889A
CR61	0 ohm	/X	0 ohm
CR53(SPDIF2)	/X	/X	8.2K ohm
CR54	/X	/X	8.2K ohm
SPDIF組數	1	2	1



Gigabyte Technology			
Title: ALC888			
Size: Custom	Document Number: EP43-UD3L		Rev: 1.0
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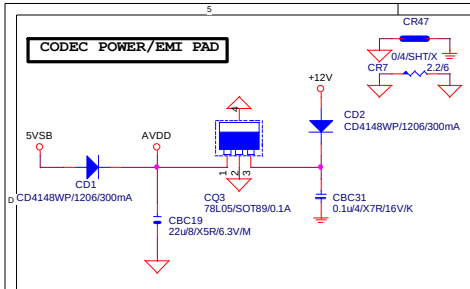
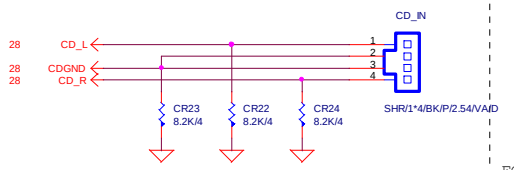
CODEC POWER/EMI PAD

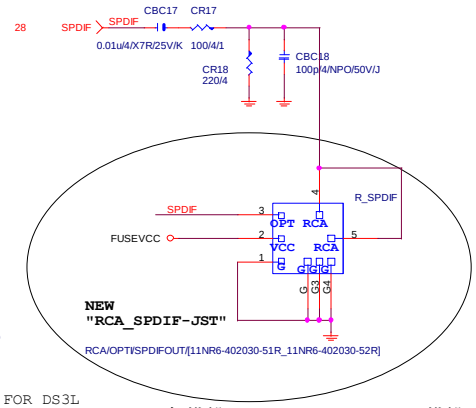


CO-LAYOUT

CD IN



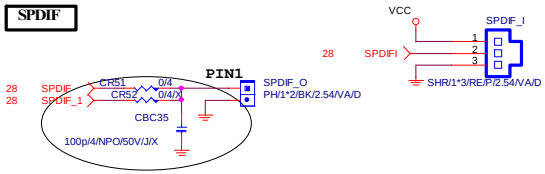
Fpr
EMI



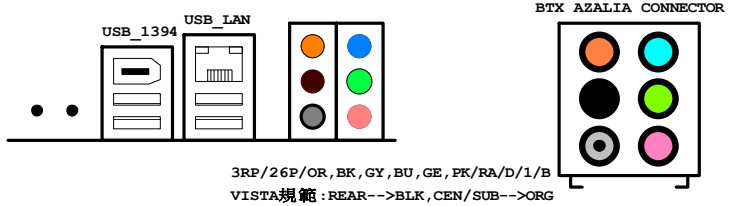
FOR DS3L
11NR6-402030-41R(無鐵殼)11NR6-402030-51R/52R(鐵殼)

FOR S3L 11NR6-501004-G1R ONLY support RCA

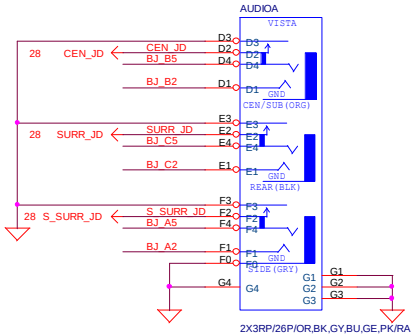
SPDIF

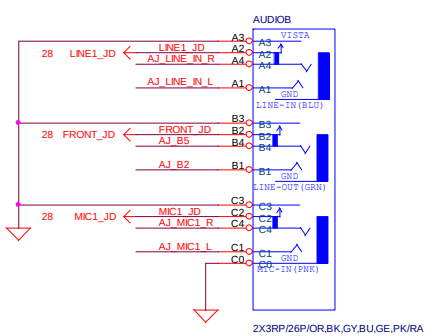


AZALIA JACK

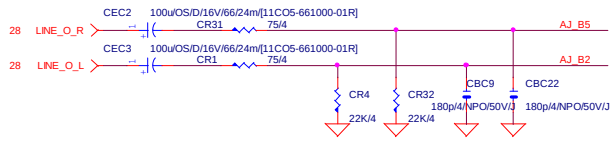


3RP/26P/OR,BK,GY,BU,GE,PK/RA/D/1/B
VISTA規範:REAR-->BLK,CEN/SUB-->ORG



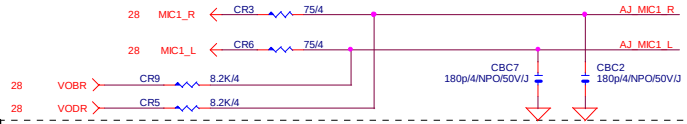


LINE-OUT

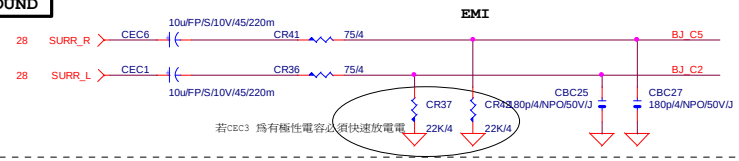


LINE-IN

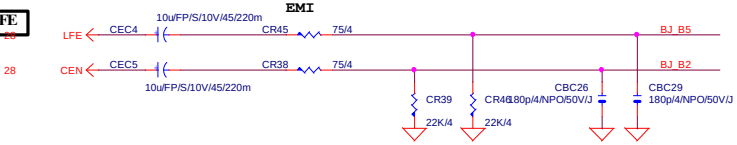
MIC-IN



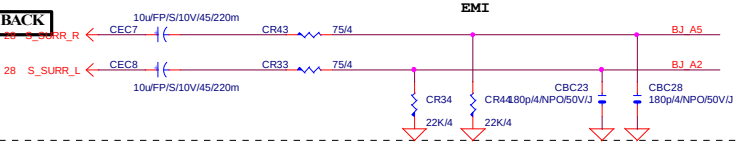
SURROUND



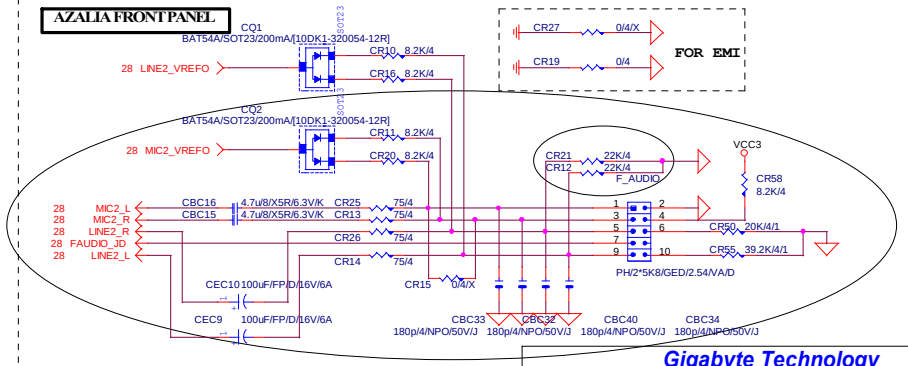
CEN/LFE



SURR BACK



AZALIA FRONT PANEL



Gigabyte Technology

Title: AUDIO JACK

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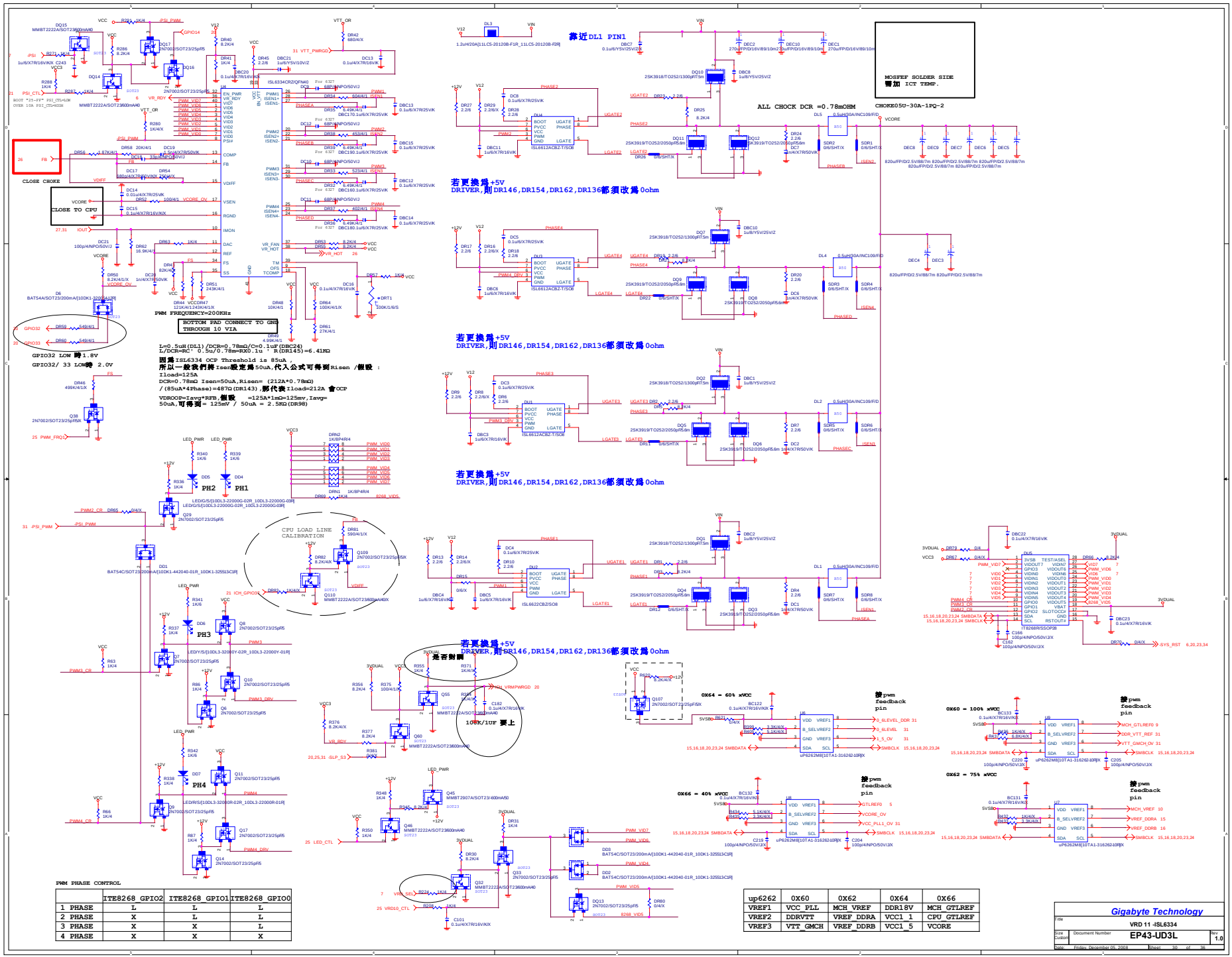
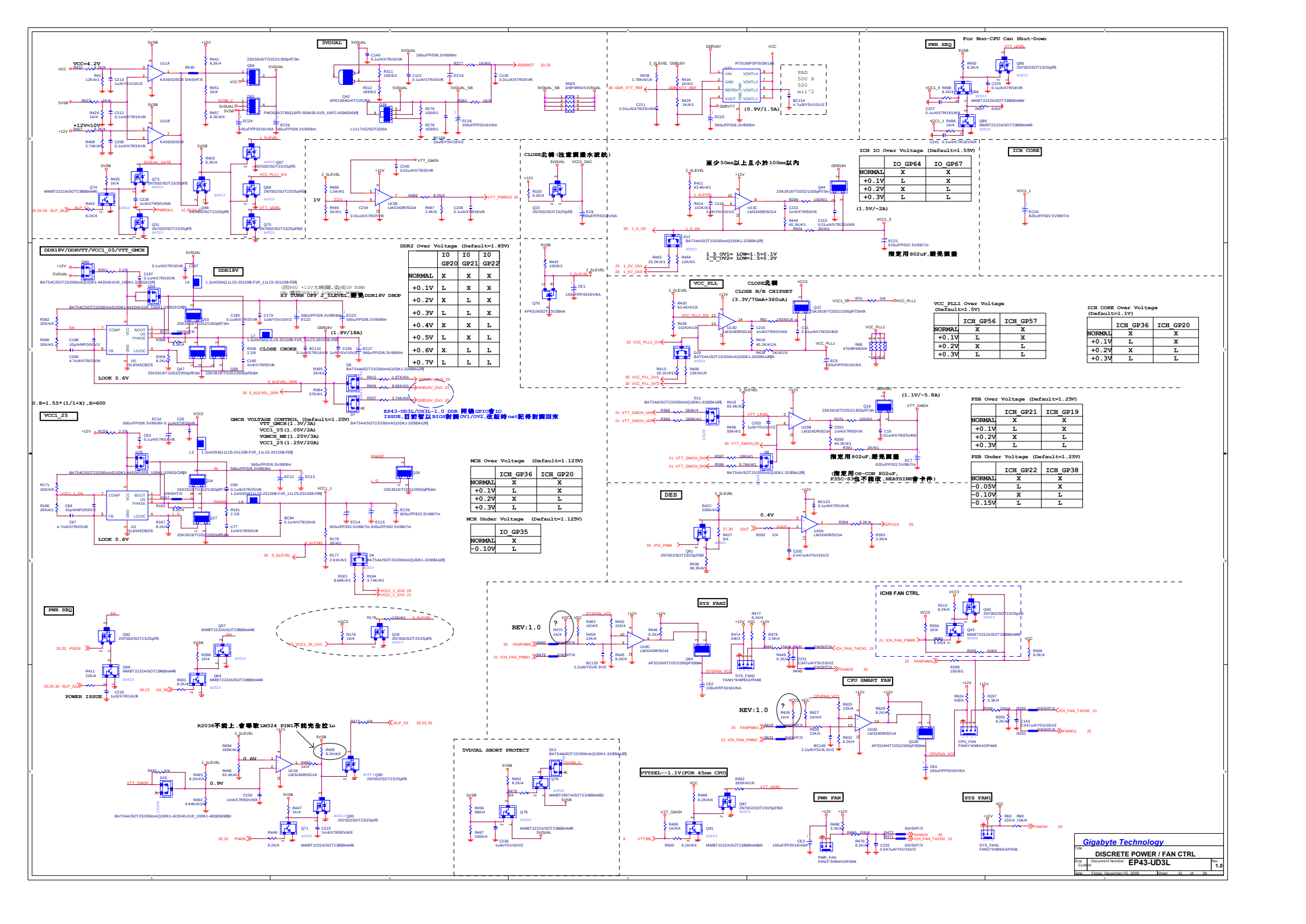


	ITE8268_GPIO2	ITE8268_GPIO1	ITE8268_GPIO0
1 PHASE	L	L	L
2 PHASE	X	L	L
3 PHASE	X	X	L
4 PHASE	X	X	X

up6262	0X60	0X62	0X64	0X66
VREF1	VCC_PLL	MCH_VREF	DDR18V	MCH_GTLREF
VREF2	DDRVTT	VREF_DDRA	VCC1_1	CPU_GTLREF
VREF3	VTT_GMCH	VREF_DDRB	VCC1_5	VCORE



DDR2 Over Voltage (Default=1.85V)	IO GP20	IO GP21	IO GP22
NORMAL	X	X	X
+0.1V	L	X	X
+0.2V	X	L	X
+0.3V	L	L	X
+0.4V	X	X	L
+0.5V	L	X	L
+0.6V	X	L	L
+0.7V	L	L	L

ICH IO Over Voltage (Default=1.55V)	IO_GP64	IO_GP67
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

VCC_PLL1 Over Voltage (Default=1.5V)	ICH_GP56	ICH_GP57
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

ICH CORE Over Voltage (Default=1.1V)	ICH_GP36	ICH_GP20
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

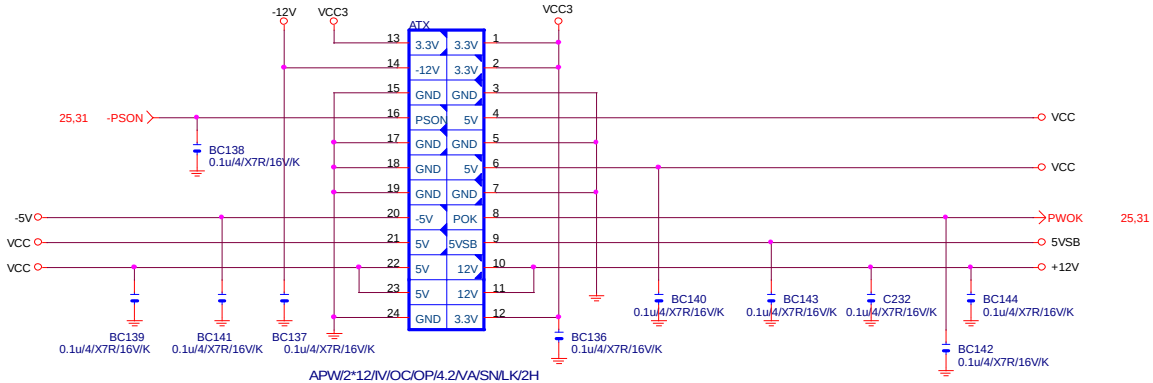
MCH Over Voltage (Default=1.125V)	ICH_GP36	ICH_GP20
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

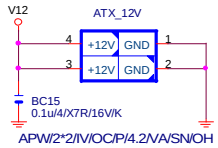
MCH Under Voltage (Default=1.125V)	IO_GP35
NORMAL	X
-0.10V	L

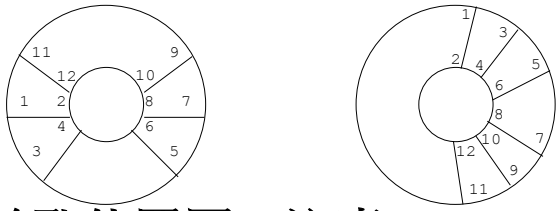
FSB Over Voltage (Default=1.25V)	ICH_GP21	ICH_GP19
NORMAL	X	X
+0.1V	L	X
+0.2V	X	L
+0.3V	L	L

FSB Under Voltage (Default=1.25V)	ICH_GP22	ICH_GP38
NORMAL	X	X
-0.05V	L	X
-0.10V	X	L
-0.15V	L	L

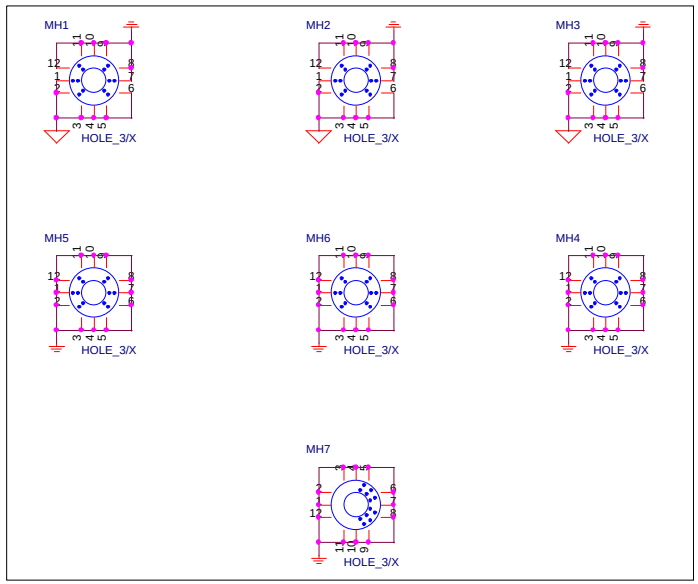
ATX POWER CONNECTOR

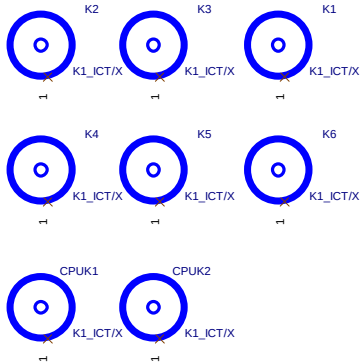


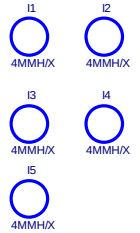




螺絲孔位置圖 （注意Footprint不同）







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Title: ATX POWER CONNECTOR		
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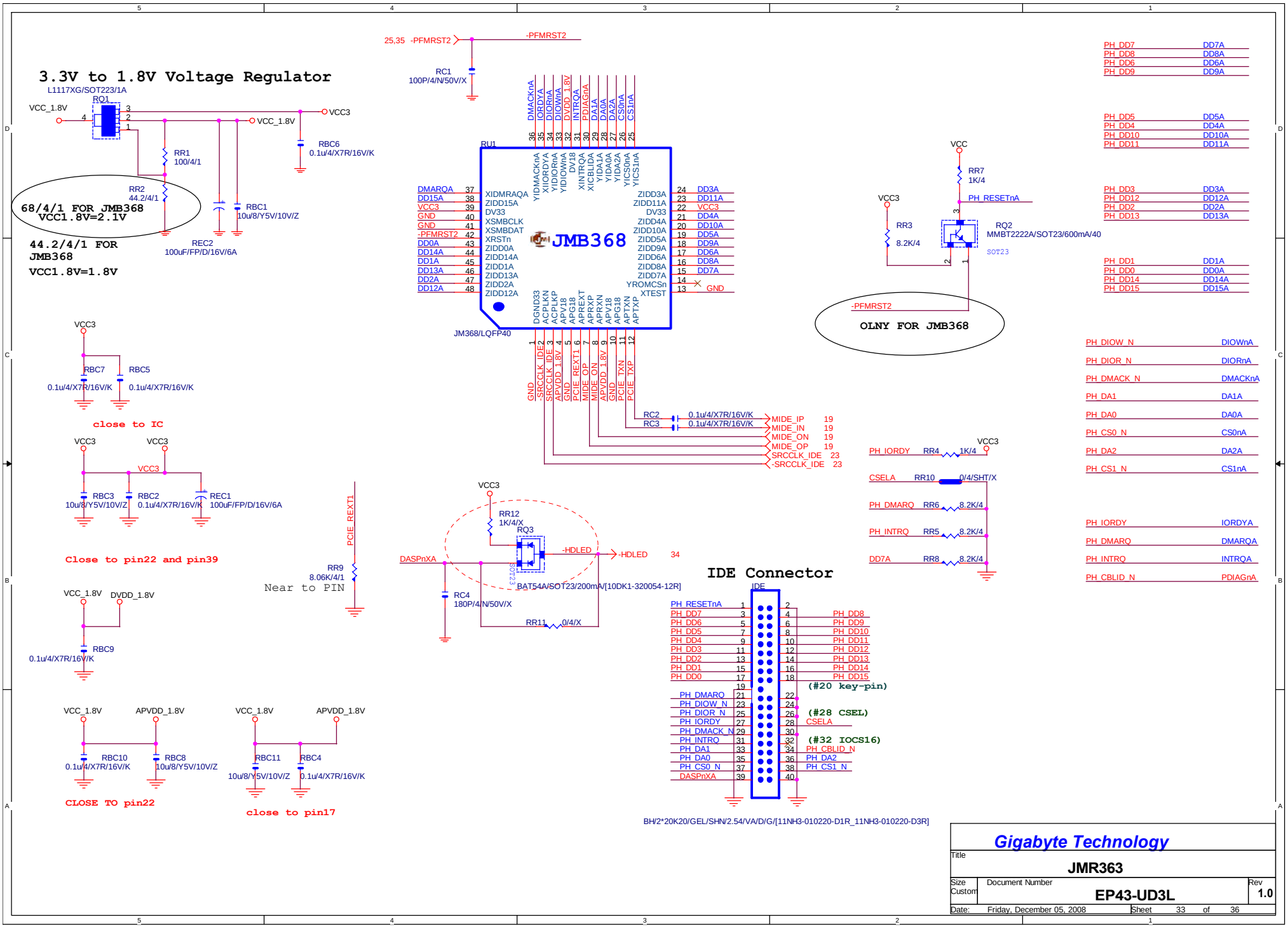
3.3V to 1.8V Voltage Regulator
L1117XG/SOT223/1A
RQ1
VCC_1.8V
VCC3
RR1 100/4/1
RR2 44.2/4/1
RBC6 0.1u/4/X7R/16V/K
RBC1 10u/8/Y5V/10V/Z
REC2 100uF/FP/D/16V/6A
68/4/1 FOR JMB368
VCC1.8V=2.1V
44.2/4/1 FOR JMB368
VCC1.8V=1.8V
25,35 -PFMRST2
RC1 100P/4/N/50V/X
RU1
JMB368
JM368/LQFP40
RC2 0.1u/4/X7R/16V/K
RC3 0.1u/4/X7R/16V/K
MIDE_IP 19
MIDE_IN 19
MIDE_ON 19
MIDE_OP 19
SRCCLK_IDE 23
-SRCCLK_IDE 23
RBC7 0.1u/4/X7R/16V/K
RBC5 0.1u/4/X7R/16V/K
close to IC
RBC3 10u/8/Y5V/10V/Z
RBC2 0.1u/4/X7R/16V/K
REC1 100uF/FP/D/16V/6A
Close to pin22 and pin39
RR9 8.06K/4/1
Near to PIN
PCIE_REXT1
RR12 1K/4/X
RQ3
-HDLED
DASPnXA
RC4 180P/4/N/50V/X
RR11 0/4/X
BAT54A/SOT23/200mA/[10DK1-320054-12R]
RBC9 0.1u/4/X7R/16V/K
RBC10 0.1u/4/X7R/16V/K
RBC8 10u/8/Y5V/10V/Z
CLOSE TO pin22
RBC11 10u/8/Y5V/10V/Z
RBC4 0.1u/4/X7R/16V/K
close to pin17
RR7 1K/4
PH_RESETnA
RR3 8.2K/4
RQ2 MMBT2222A/SOT23/600mA/40
SOT23
-PFMRST2
OLNY FOR JMB368
PH_IORDY RR4 1K/4
CSELA RR10 0/4/SHT/X
PH_DMARQ RR6 8.2K/4
PH_INTRQ RR5 8.2K/4
DD7A RR8 8.2K/4
IDE Connector
IDE
(#20 key-pin)
(#28 CSEL)
(#32 IOCS16)
BH/2*20K20/GEL/SHN/2.54/VA/D/G/[11NH3-010220-D1R_11NH3-010220-D3R]
PH_DD7 DD7A
PH_DD8 DD8A
PH_DD6 DD6A
PH_DD9 DD9A
PH_DD5 DD5A
PH_DD4 DD4A
PH_DD10 DD10A
PH_DD11 DD11A
PH_DD3 DD3A
PH_DD12 DD12A
PH_DD2 DD2A
PH_DD13 DD13A
PH_DD1 DD1A
PH_DD0 DD0A
PH_DD14 DD14A
PH_DD15 DD15A
PH_DIOW_N DIOWnA
PH_DIOR_N DIORnA
PH_DMACK_N DMACKnA
PH_DA1 DA1A
PH_DA0 DA0A
PH_CS0_N CS0nA
PH_DA2 DA2A
PH_CS1_N CS1nA
PH_IORDY IORDYA
PH_DMARQ DMARQA
PH_INTRQ INTRQA
PH_CBLID_N PDIAGnA
Gigabyte Technology
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JMR363
Size Custom
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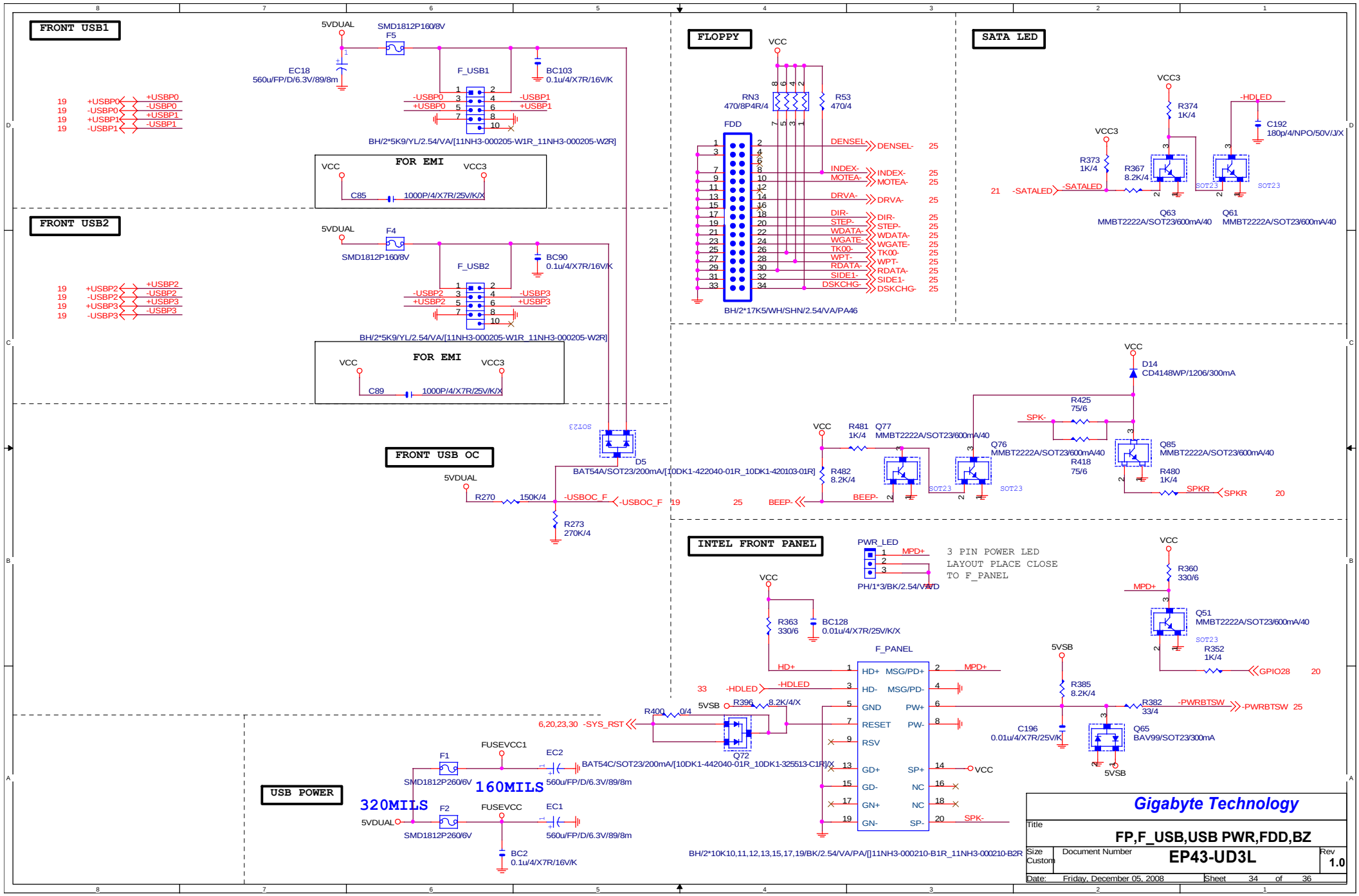
FRONT USB1
5VDUAL
SMD1812P160/8V
F5
EC18
560u/FP/D/6.3V/89/8m
F_USB1
BC103
0.1u/4/X7R/16V/K
19 +USBP0 +USBP0
19 -USBP0 -USBP1
19 +USBP1 -USBP1
19 -USBP1
-USBP0 -USBP1
+USBP0 +USBP1
BH/2*5K9/YL/2.54/VA/[11NH3-000205-W1R_11NH3-000205-W2R]
FOR EMI
VCC
VCC3
C85
1000P/4/X7R/25V/K/X
FRONT USB2
5VDUAL
F4
SMD1812P160/8V
F_USB2
BC90
0.1u/4/X7R/16V/K
19 +USBP2 +USBP2
19 -USBP2 -USBP3
19 +USBP3 -USBP3
19 -USBP3
-USBP2 -USBP3
+USBP2 +USBP3
BH/2*5K9/YL/2.54/VA/[11NH3-000205-W1R_11NH3-000205-W2R]
FOR EMI
VCC
VCC3
C89
1000P/4/X7R/25V/K/X
FRONT USB OC
SOT23
D5
BAT54A/SOT23/200mA/[10DK1-422040-01R_10DK1-420103-01R]
5VDUAL
R270
150K/4
-USBOC_F
-USBOC_F 19
R273
270K/4
FLOPPY
VCC
RN3
470/8P4R/4
R53
470/4
FDD
DENSEL
DENSEL- 25
INDEX-
MOTEA-
INDEX- 25
MOTEA- 25
DRVA-
DRVA- 25
DIR-
STEP-
WDATA-
WGATE-
TK00-
WPT-
RDATA-
SIDE1-
DSKCHG-
DIR- 25
STEP- 25
WDATA- 25
WGATE- 25
TK00- 25
WPT- 25
RDATA- 25
SIDE1- 25
DSKCHG- 25
BH/2*17K5/WH/SHN/2.54/VA/PA46
SATA LED
VCC3
R374
1K/4
-HDLED
C192
180p/4/NPO/50V/J/X
VCC3
R373
1K/4
R367
8.2K/4
SOT23
SOT23
21 -SATALED
-SATALED
Q63
MMBT2222A/SOT23/600mA/40
Q61
MMBT2222A/SOT23/600mA/40
VCC
D14
CD4148WP/1206/300mA
R425
75/6
SPK-
VCC
R481
1K/4
Q77
MMBT2222A/SOT23/600mA/40
Q76
MMBT2222A/SOT23/600mA/40
R418
75/6
Q85
MMBT2222A/SOT23/600mA/40
R480
1K/4
SPKR
SPKR 20
R482
8.2K/4
BEEP-
BEEP- 25
SOT23
SOT23
INTEL FRONT PANEL
PWR_LED
MPD+
3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL
PH/1*3/BK/2.54/VA/D
VCC
R363
330/6
BC128
0.01u/4/X7R/25V/K/X
F_PANEL
HD+
-HDLED
33 -HDLED
5VSB
R396
8.2K/4/X
R400
0/4
6,20,23,30 -SYS_RST
Q72
BAT54C/SOT23/200mA/[10DK1-442040-01R_10DK1-325513-C1R]/X
HD+ MSG/PD+
HD- MSG/PD-
GND PW+
RESET PW-
RSV
GD+ SP+
GD- NC
GN+ NC
GN- SP-
MPD+
VCC
SPK-
BH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/PA/[]11NH3-000210-B1R_11NH3-000210-B2R
VCC
R360
330/6
MPD+
Q51
MMBT2222A/SOT23/600mA/40
SOT23
R352
1K/4
GPIO28 20
5VSB
R385
8.2K/4
R382
33/4
-PWRBTSW
-PWRBTSW 25
C196
0.01u/4/X7R/25V/K
Q65
BAV99/SOT23/300mA
5VSB
USB POWER
FUSEVCC1
F1
SMD1812P260/6V
EC2
560u/FP/D/6.3V/89/8m
160MILS
320MILS
5VDUAL
F2
SMD1812P260/6V
FUSEVCC
EC1
560u/FP/D/6.3V/89/8m
BC2
0.1u/4/X7R/16V/K
Gigabyte Technology
Title
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Size
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Document Number
EP43-UD3L
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1.0
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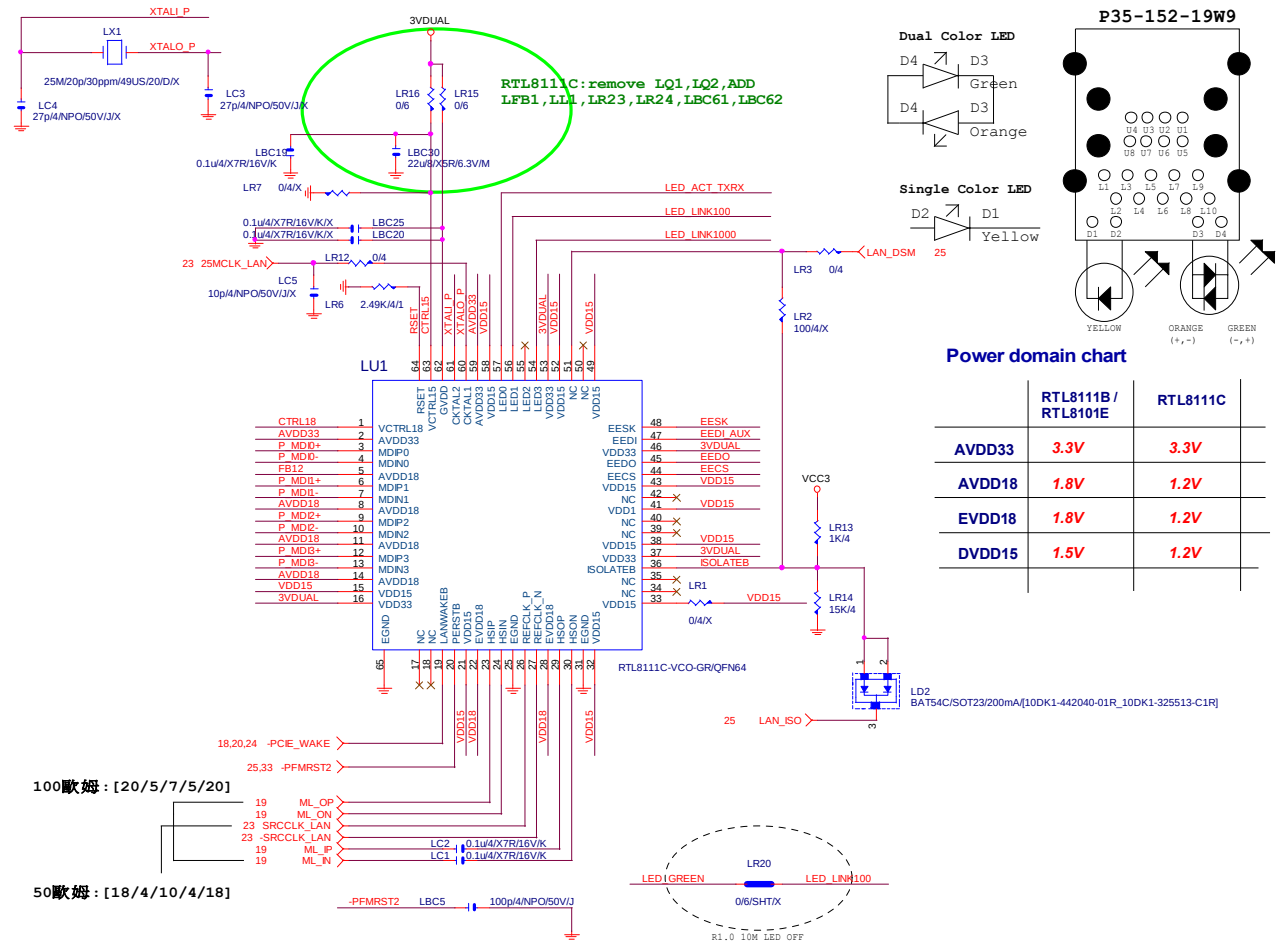
PCIE-1G LAN



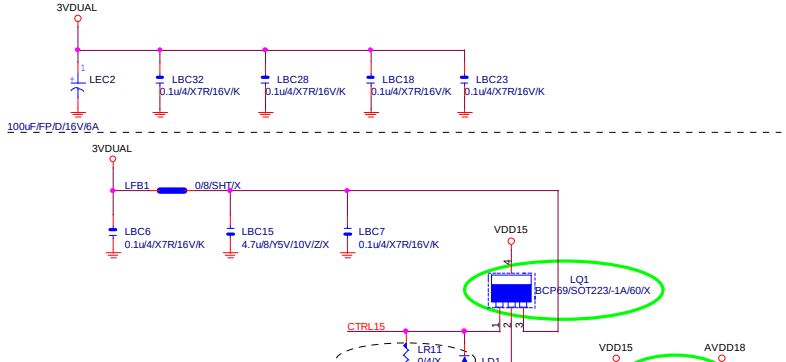
Dual Color LED

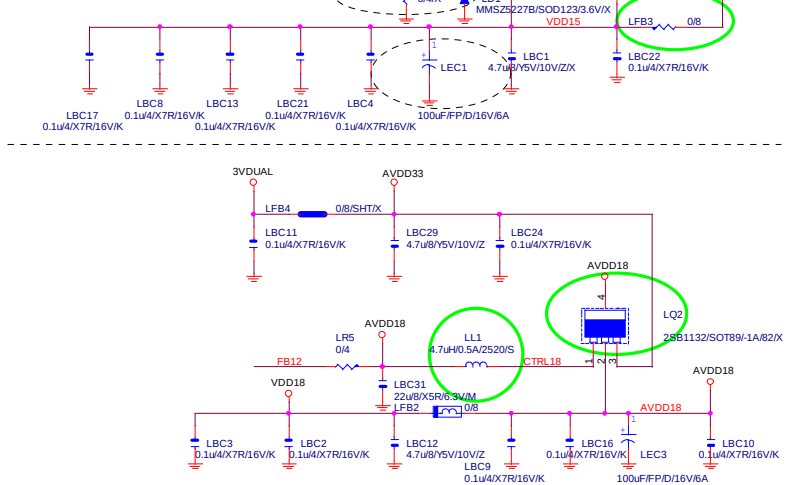
Single Color LED

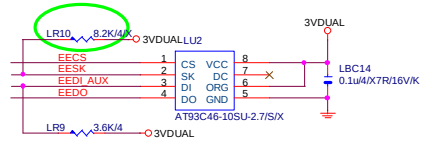
P35-152-19W9

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

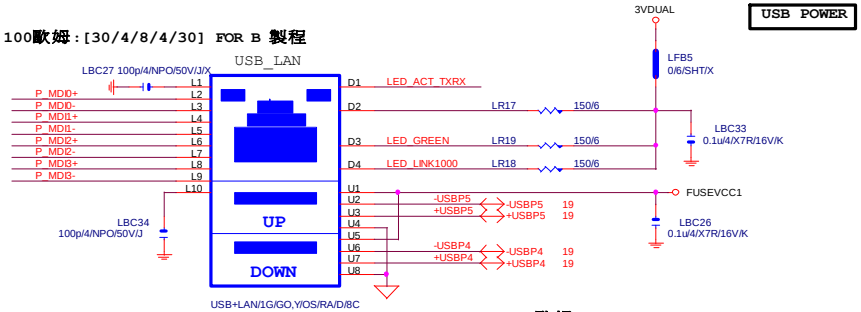






USB_LAN CONNECTOR

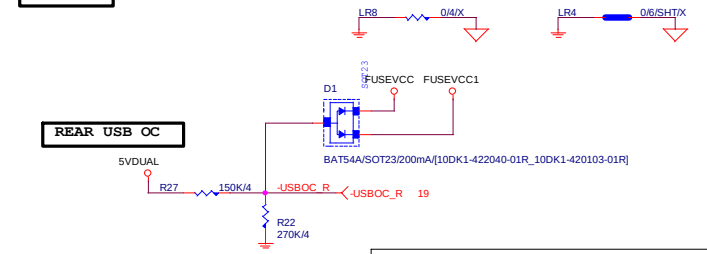
LAN 100歐姆:[30/4/8/4/30] FOR B 製程



USB POWER

90歐姆:[15/4.5/7.5/4.5/15]

USB_LAN



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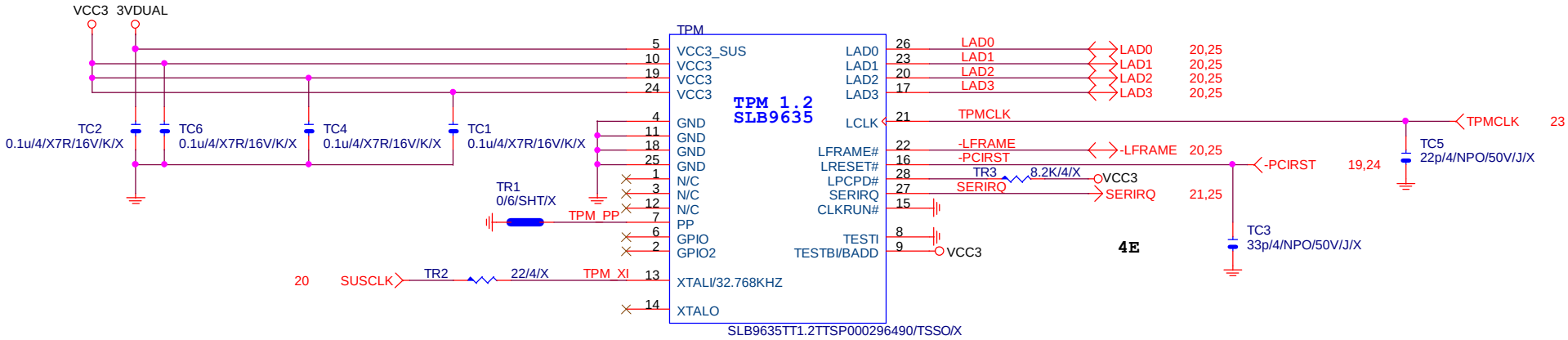

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