H81H3-I

Rev : A

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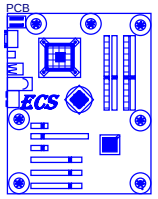
REVISION HISTORY:

Rev	Date	Notes
VA		Modified from H81H3-M4



PCB : 170 x 170

PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

NOTE:

1. Model Code:
2. Modified from H81H3-M4

ECS CONFIDENTIAL

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Title: Cover Page

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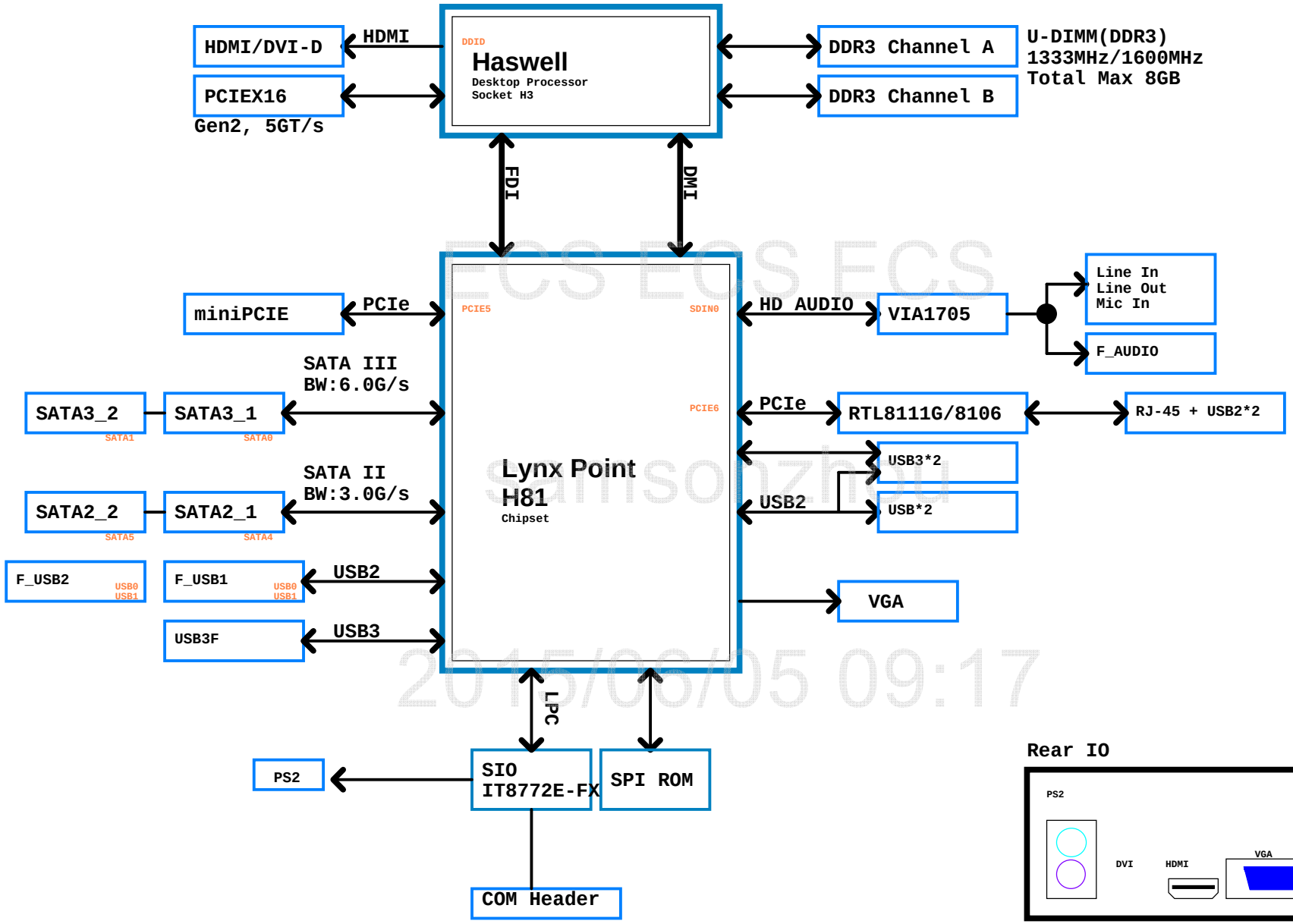
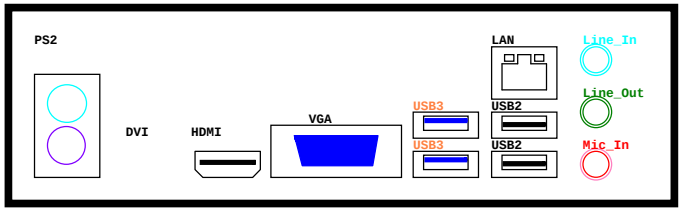


Rear IO



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Title	Block Diagram	
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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status	
GPIO0	VCC3	F_Audio Detection	GPI	Hi : AC97 ; Lo: HD
GPIO1	VCC3	BOM Selection	GPI	Hi : HDMI ; Lo: DVI
GPIO6	VCC3	BOM Selection	GPI	
GPIO7	VCC3	BOM Selection	GPI	
GPIO13	3VSB	LPC_PME	GPI	
GPIO15		DIMM voltage adjust		Hi : 1.35V ; Lo: 1.5V
GPIO24		Me Unlock Control		

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP22	3VSB	G_LED1	GPIO
GP23	3VSB	G_LED2	GPIO
FAN_TAC2		CPU FAN Tac	
FAN_CTL2		CPU FAN Ctl	
VIN0		Vcore Voltage	
VIN1		Vdimm Voltage	

GP22
GP23

	S0	S1	S3	S4/S5
G_LED1	H	H	L	L
G_LED2	L	B	B	L
	G	GB	YB	OFF

B:Blinking

Interrupt mapping

Function	INT# port	PCIe*1 port	Device
PCIEX1	INTD#	port 5	LPT integrate
LAN	INTC#	port 6	RTL8111G
SATA	INTB#	NA	LPT integrate

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Title: GPIO Function/INT Mapping

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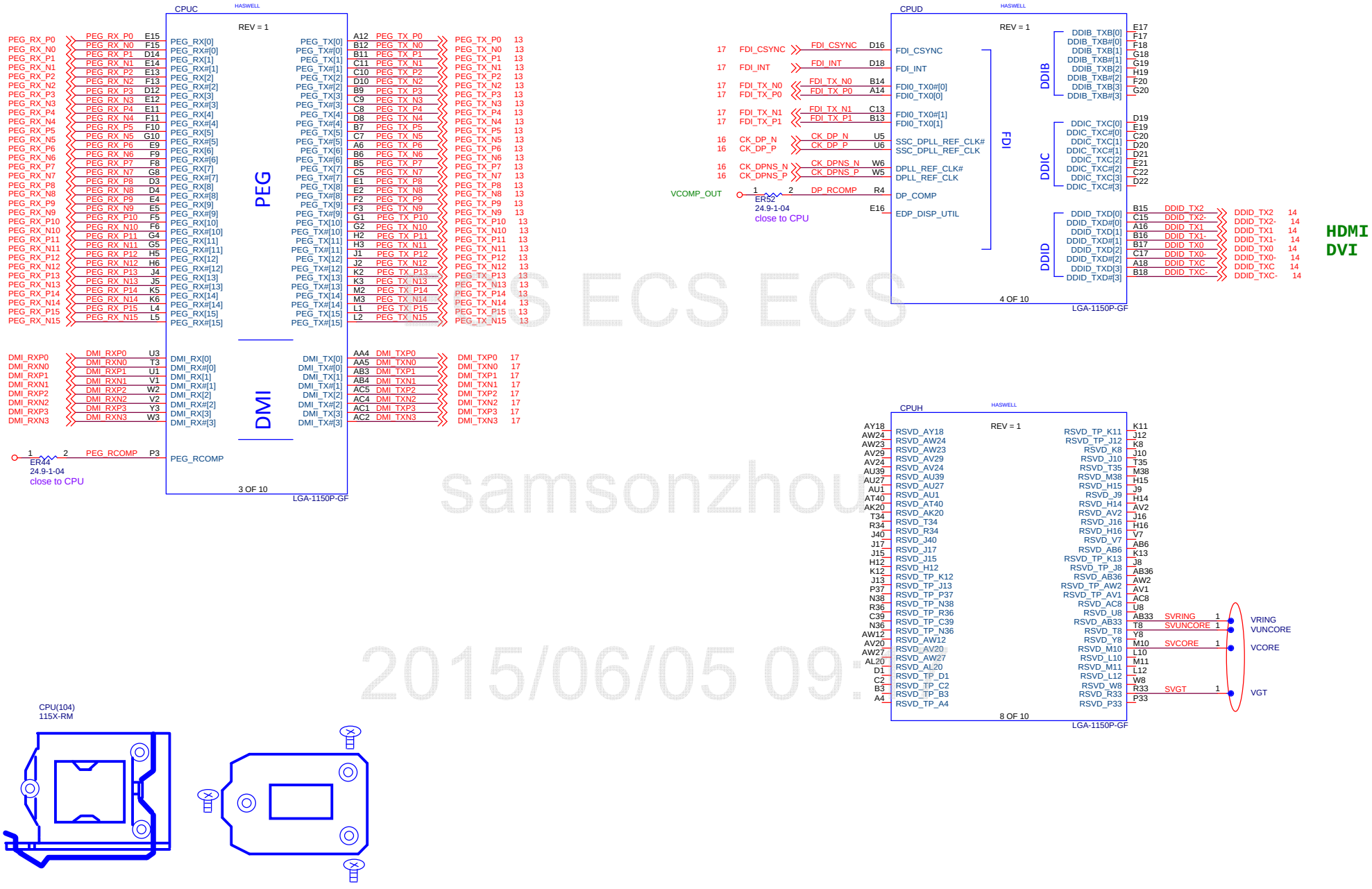

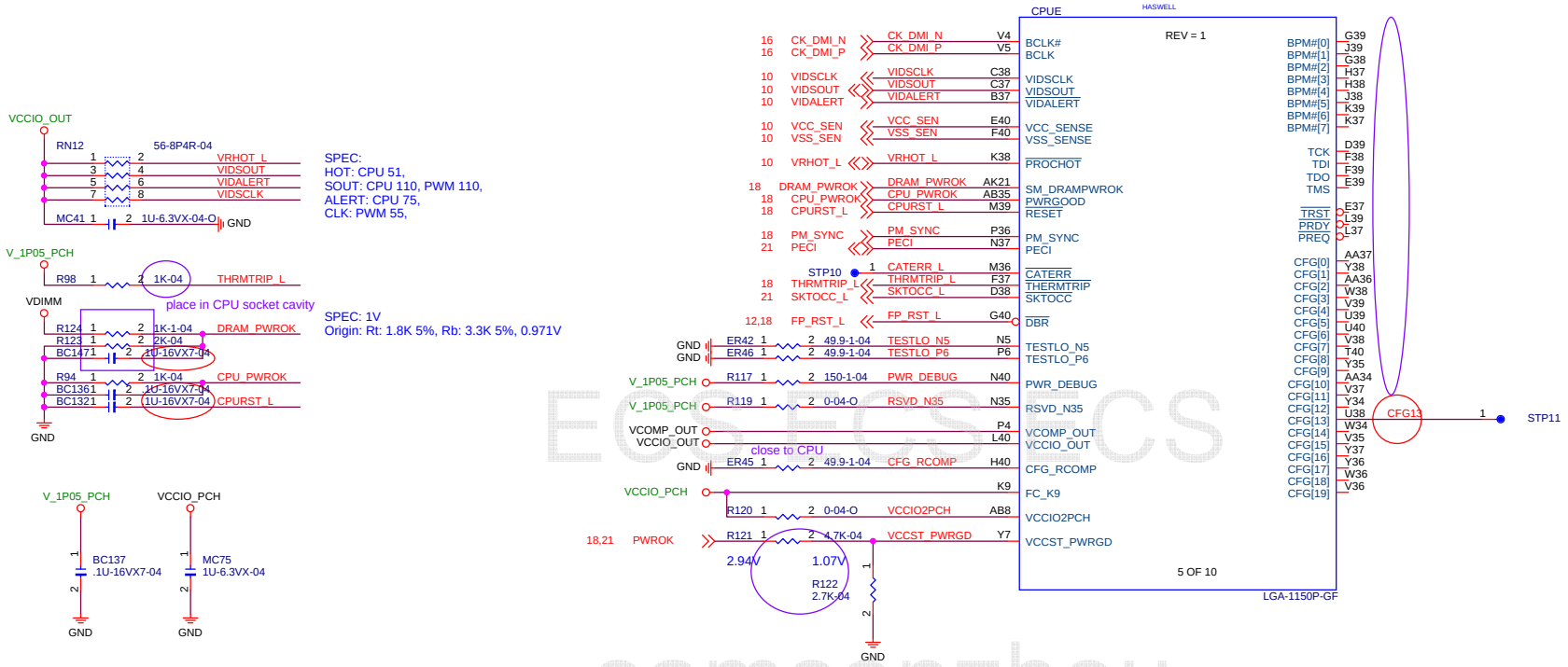

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
1 = Normal operation
0 = Lane numbers reversed.
CFG[3]: MSR Privacy Bit Feature
1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0]
0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden
CFG[5..6]: PCI Express* Bifurcation:
CFG[0..1, 4, 7..19]: Reserved configuration lane.

CFG[0..17] HAVE INTERNAL PULL-UPS

*

PCIE CONFIG	CFG6	CFG5
1 X 16	1	1
2 X 8	1	0
Reserved	0	1
X8 X4 X4	0	0

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Title: CPU-MISC

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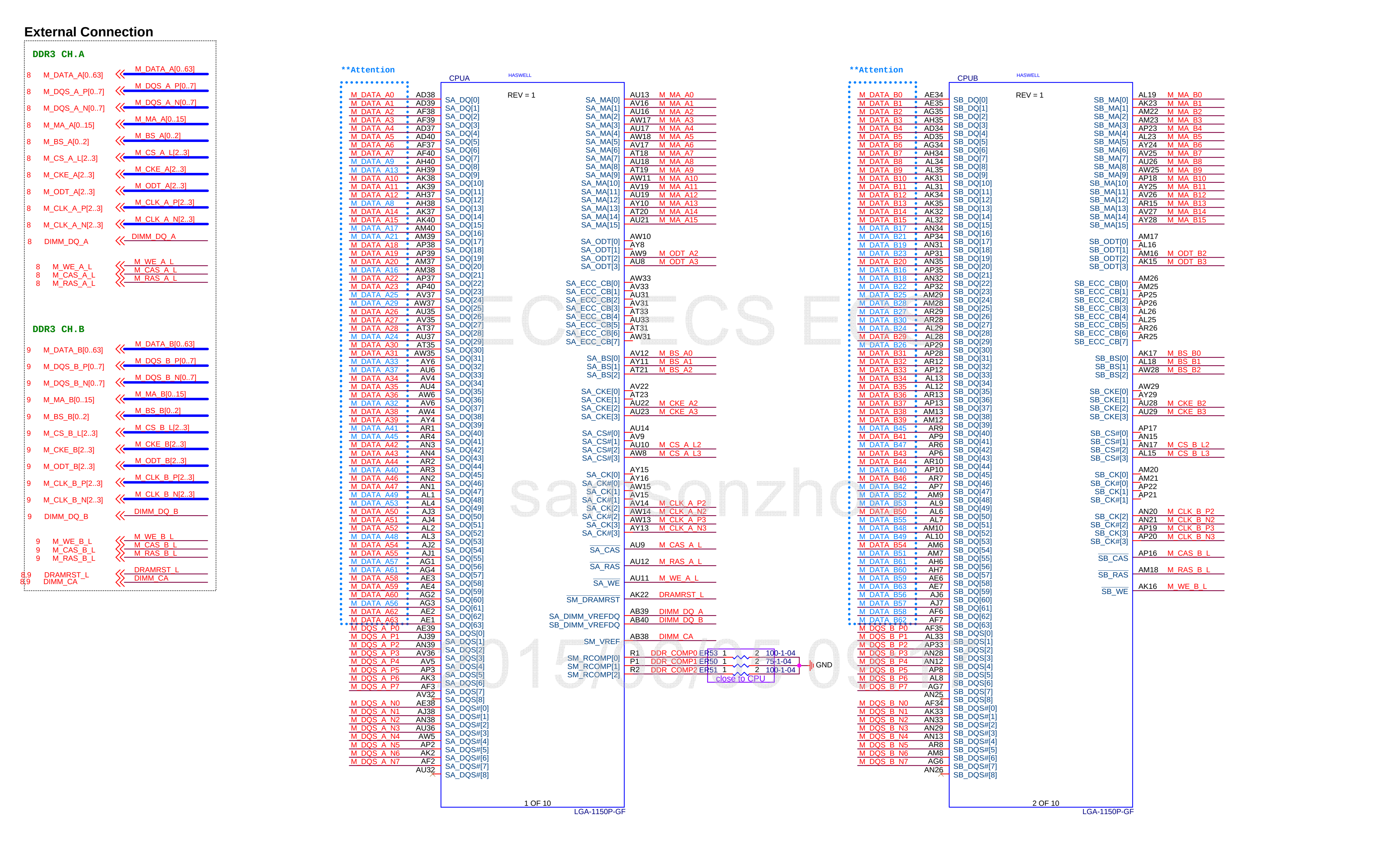

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Title	CPU-DDR3
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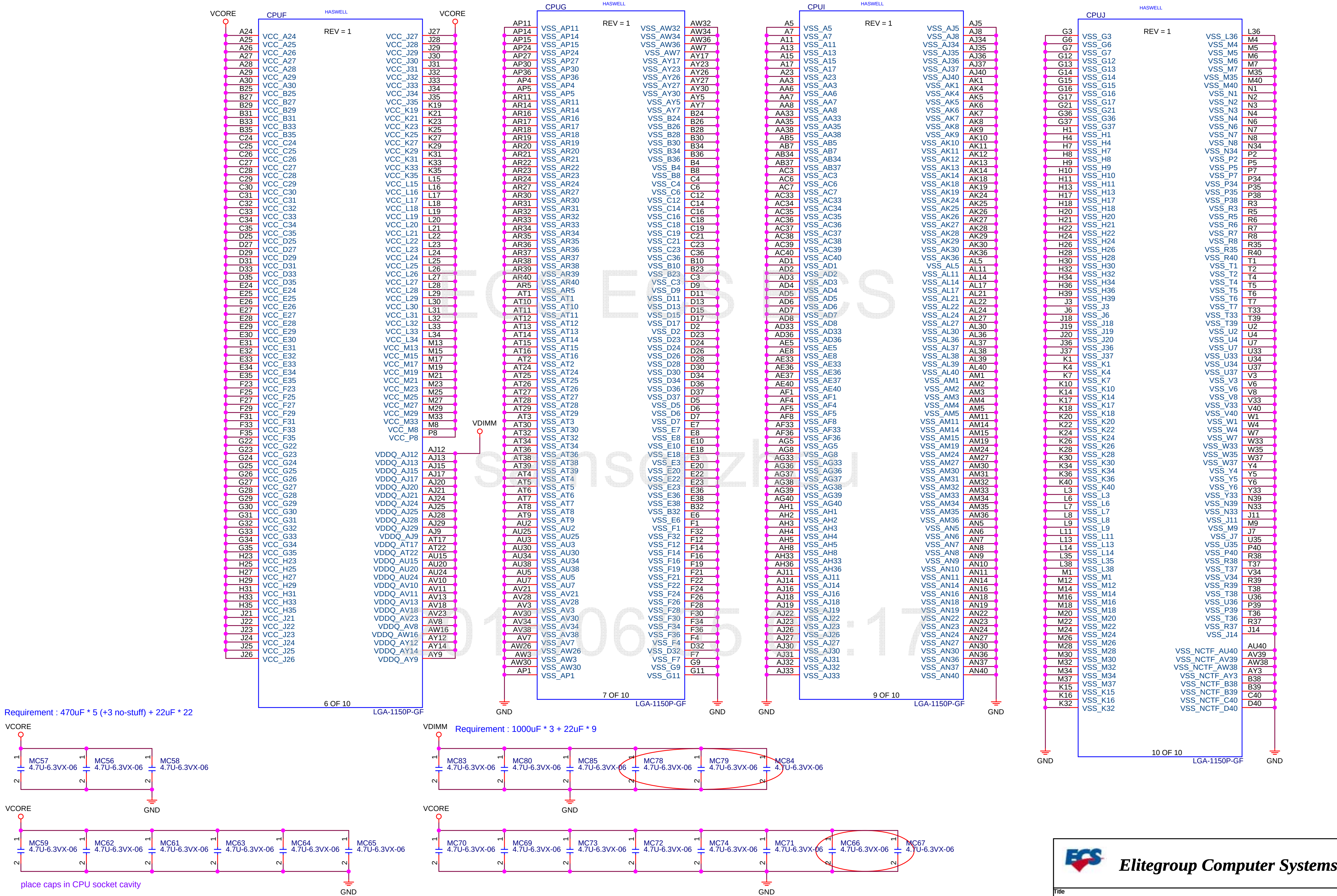

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Title	CPU-PWR/GND
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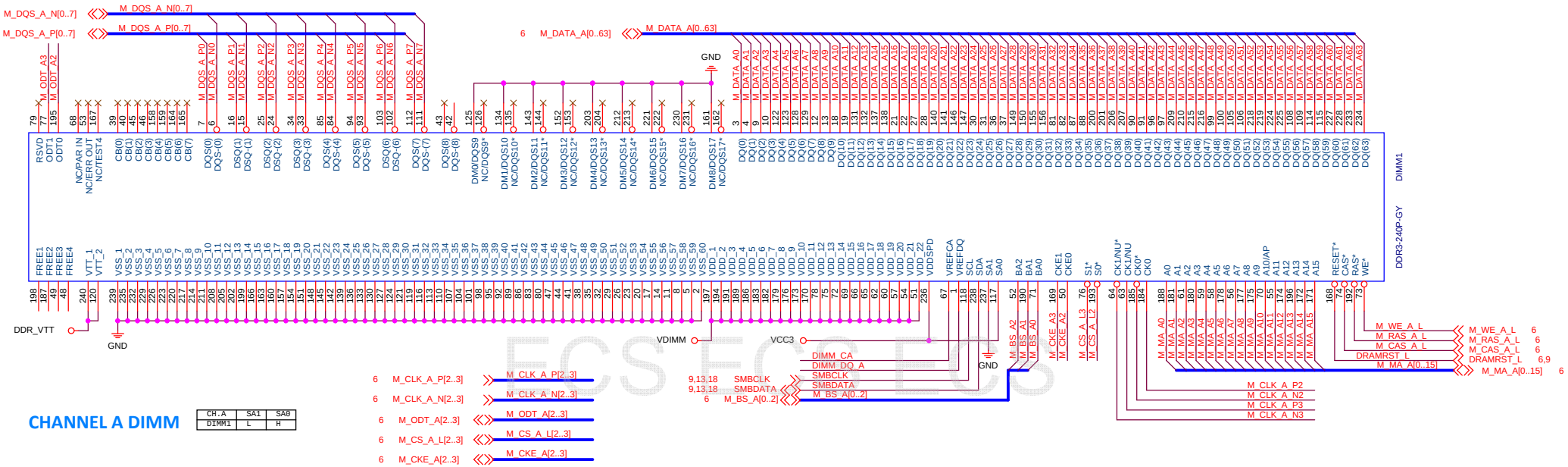
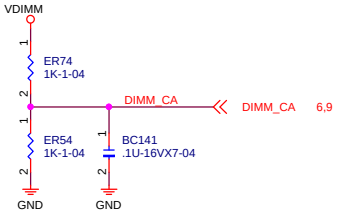


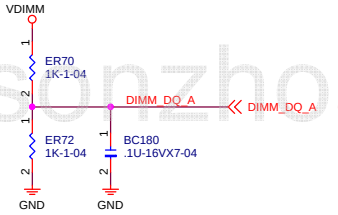
CHANNEL A DIMM

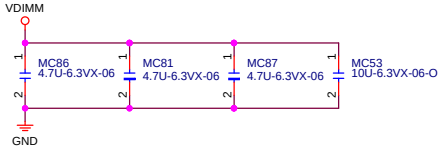
CH.A	SA1	SA0
DIMM1	L	H

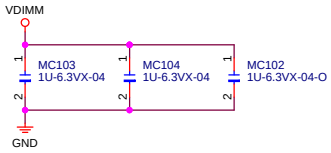
DIMM_VREF_CA Circuit

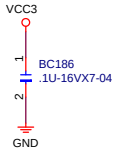


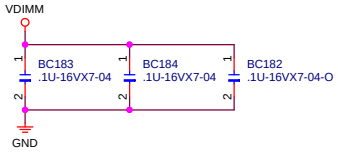
DIMM_VREF_DQ Circuit

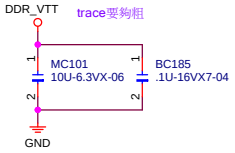












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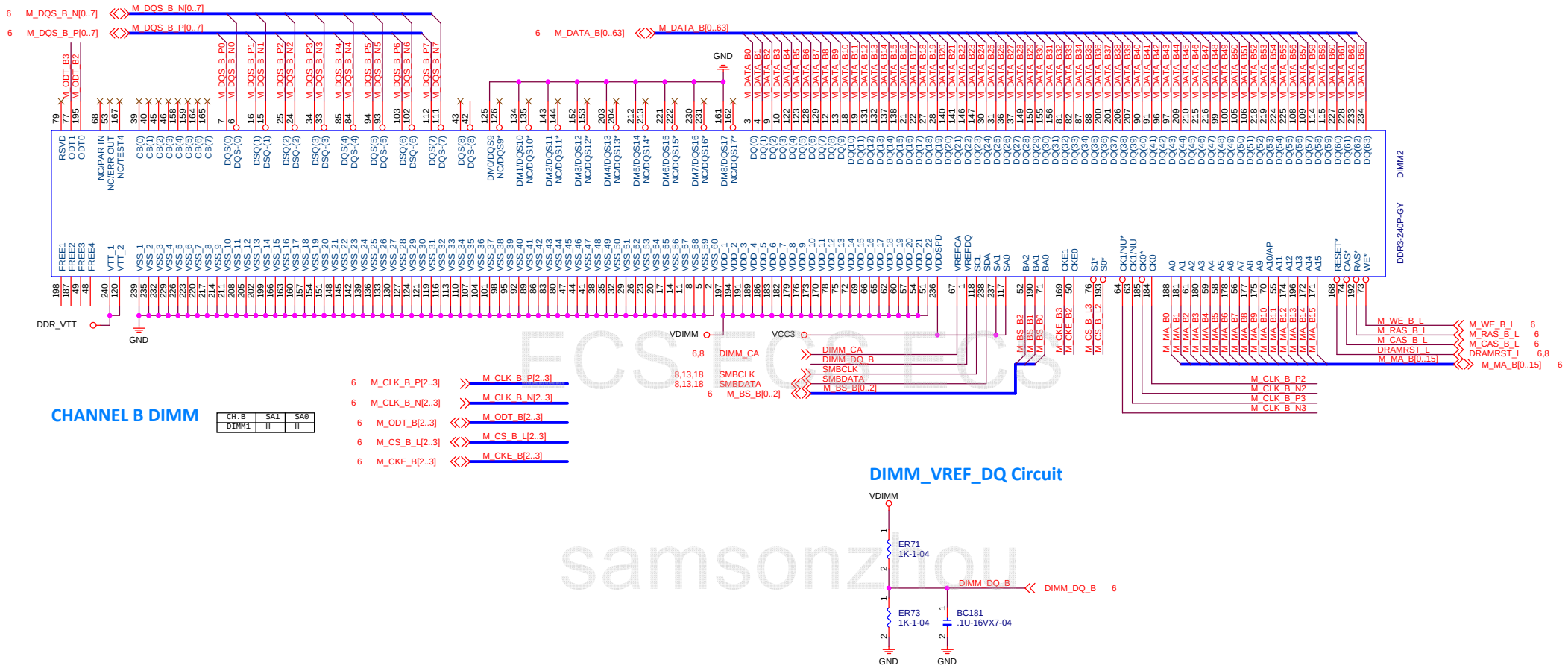

CHANNEL B DIMM

CH.B	SA1	SA0
DIMM1	H	H

DIMM_VREF_DQ Circuit

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External Connection

VCCNS_REF — VCCNS_REF
VCC — VCC
VCORE — VCORE
5VSB — 5VSB

5	VIDALERT	VIDALERT
5	VIDSOUT	VIDSOUT
5	VIDSCLK	VIDSCLK
5	VRHOT_L	VRHOT_L
5	VCC_SEN	VCC_SEN
5	VSS_SEN	VSS_SEN
18	VR_READY	VR_READY

SET1:
Rt1 = 7.5K+475 , Rb1 = 2.67K+23.7,
Ramp (RSET % 130K Rton) = 87.5%, DVID_Width = 192us,
OCP = 150% ICCMAX, DVID_Threshold = 15mV,

SET2:
Rt2 = 8.87K+37.4, Rb2 = 1.2K+22.6,
QR Threshold = disable, QR Width = 111%,
ICCMAX = 96A,

SET3: Rb3 = 0ohm,
Offset = 1/2*(Rt3/Rb3 - 1.2) = 0mv,

When 100度 NTC-100K min value : 5.09K,
Vtsen = 5 * 3.45 /(5.09+3.45) = 1.880 < 1.886,

Rton = 150K, FSW = 270KHz

130325 Vendor suggest

initial voltage = 1.7V

Req = (NTC-100K + 16.5K) // 11K + 2K = 12.05K

130325 Vendor suggest 68K for load line. origin 60.4K

ISEN 680 ohm
IMON network
要盡量靠近IC

PWM1
RT8889BGQW
02-437-889791

RT8889A

VCC, PVCC, VR_READY, VR_HOT#, VCLK, VDIO, ALERT#, VRON, TONSET, TSEN, SET1, SET2, SET3, IBIAS, VREF, IMON, COMP, FB, VSEN, RGND, BOOT1, UGATE1, PHASE1, LGATE1, ISEN1P, ISEN1N, BOOT2, UGATE2, PHASE2, LGATE2, ISEN2P, ISEN2N, BOOT3, UGATE3, PHASE3, LGATE3, ISEN3P, ISEN3N, NC, NC1, GND

Power Down Sequencing Circuit

5VSB — R68 10K-04-O — SLP3_H — QN3 2N3904-S-O — VR_EN
11,18,21 SLP3_L — R69 1K-04-O — QN4 2N3904-S-O
GND

VIN — X7R — R76 2.2-06 — BC98 .1U-16VX7-04 — R83 0-06 — BOOT1 — HG_1 — HG1 — MF2 MNPPAG-9MS — PHASE1 — LG1 — MF5 MNPPAG-6MS — R99 1-06 — BC106 3300P-50VX7-04 — L2 PIND-.56U-D — 08-413-564091 DCR:1mOHM — VCORE — SP2 SHORT PAD — SP5 SHORT PAD — R65 6.2K-04 — ISEN1P — BC81 .1U-16VX7-04 — ISEN1N

VIN — X7R — R77 2.2-06 — BC99 .1U-16VX7-04 — R84 0-06 — BOOT2 — HG_2 — HG2 — MF3 MNPPAG-9MS — PHASE2 — LG2 — MF6 MNPPAG-6MS — R100 1-06 — BC108 3300P-50VX7-04 — L3 PIND-.56U-D — SP3 SHORT PAD — SP6 SHORT PAD — R73 6.2K-04 — ISEN2P — BC85 .1U-16VX7-04 — ISEN2N

VIN — X7R — R75 2.2-06 — BC96 .1U-16VX7-04 — R82 0-06 — BOOT3 — HG_3 — HG3 — MF1 MNPPAG-9MS — PHASE3 — LG3 — MF4 MNPPAG-6MS — R97 1-06 — BC104 3300P-50VX7-04 — L1 PIND-.56U-D — SP1 SHORT PAD — SP4 SHORT PAD — R64 6.2K-04 — ISEN3P — BC75 .1U-16VX7-04 — ISEN3N

12V_4P — ATX12V ATX-PW-4P2R — BC83 .01U-25VX-04
12V_4P — VIN — EC4 470U-16DE-O

VIN — MC22 MC27 MC30 MC24 MC33 MC34 MC28 MC23 MC31 MC26 MC32 MC25 — 10U-16VX-08 / 10U-16VX-08-O

VCORE — ESR: 7m OHM Max per E/C — EC9 EC10 EC8 EC11 — 820U-2.5D6-OS ×4

2 phase option
ISEN_3N — R56 — 0-04-O — 5VSB

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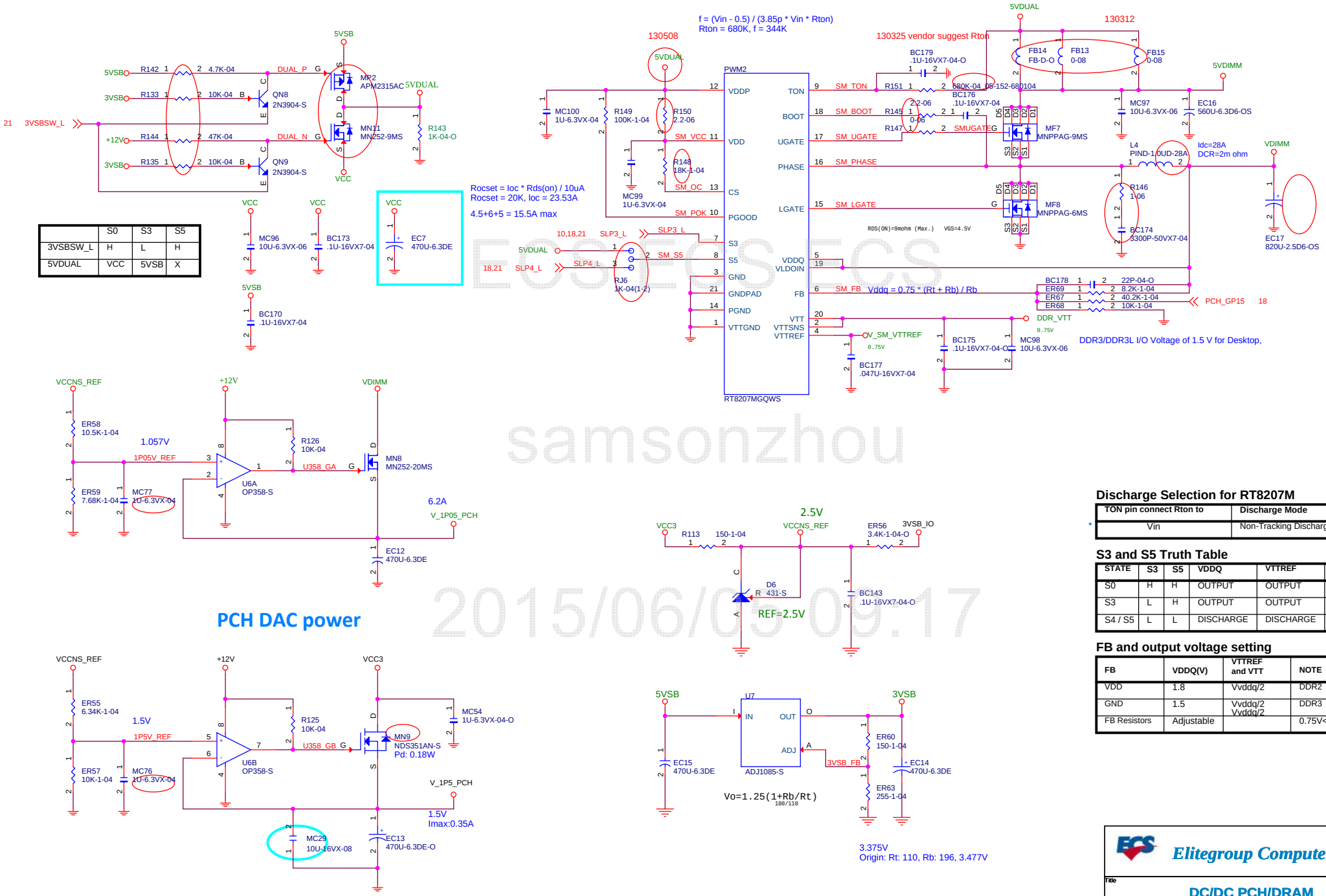

	S0	S3	S5
3VSBSW_L	H	L	H
5VDUAL	VCC	5VSB	X

Discharge Selection for RT8207M

TON pin connect Rton to	Discharge Mode
* Vin	Non-Tracking Discharge

S3 and S5 Truth Table

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	OUTPUT	OUTPUT	OUTPUT
S3	L	H	OUTPUT	OUTPUT	HIGH-Z
S4 / S5	L	L	DISCHARGE	DISCHARGE	DISCHARGE

FB and output voltage setting

FB	VDDQ(V)	VTTREF and VTT	NOTE
VDD	1.8	Vvddq/2	DDR2
GND	1.5	Vvddq/2	DDR3
FB Resistors	Adjustable	Vvddq/2	0.75V<Vvddq<3.3V

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Title: DC/DC PCH/DRAM

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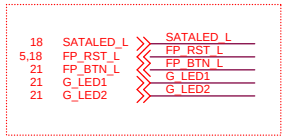
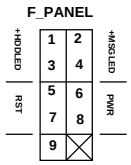
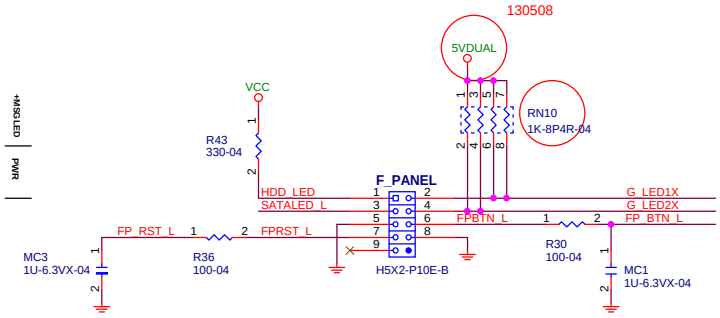
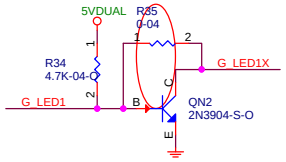
FRONT PANEL

External Connection



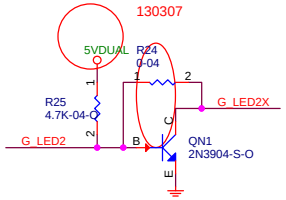






	S0	S1	S3	S4/S5
GP22 G_LED1	L	B	B	L
GP23 G_LED2	H	H	L	L
	G	GB	YB	OFF

B:Blinking

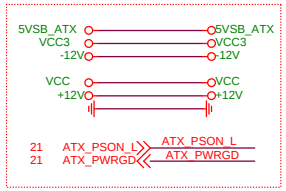


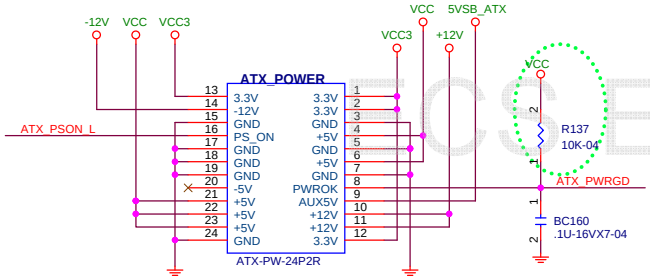
	S0	S1	S3	S4/S5
GP22 G_LED1	H	H	L	L
GP23 G_LED2	L	B	B	L
	G	GB	YB	OFF

B:Blinking

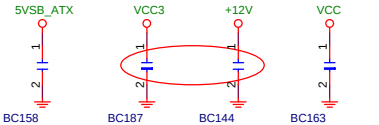
POWER CONNECTOR

External Connection





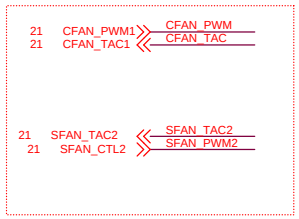
130307 Del VCC EC

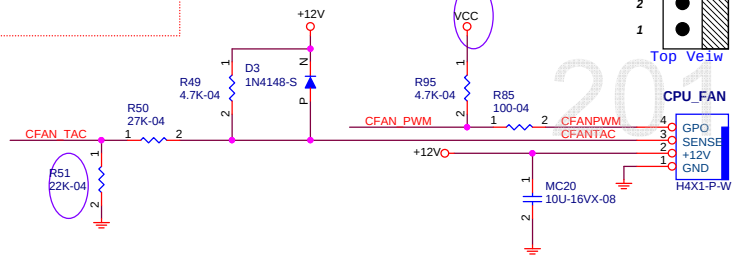


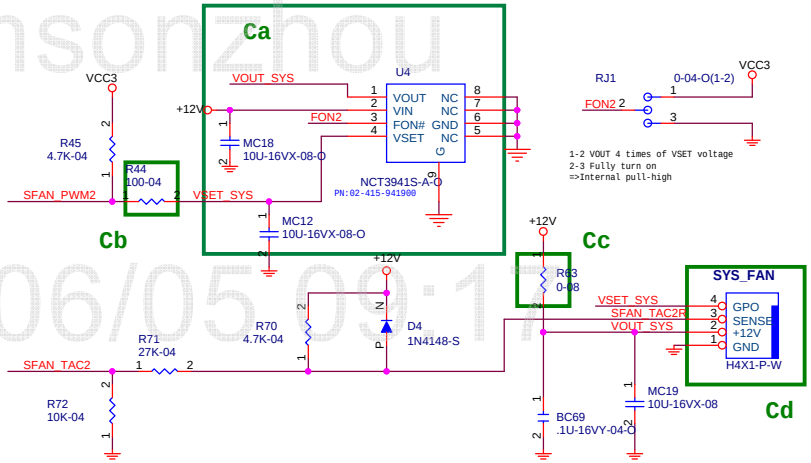
For EMI

FAN

External Connection

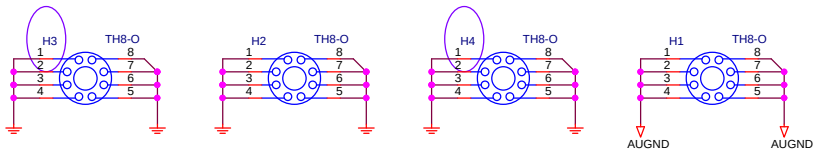






BOM Difference

	SYS_FAN 3PIN	SYS_FAN 4PIN
Ca	V	X
Cb	15k	100
Cc	X	V
Cd	H3X1-P-W	H4X1-P-W



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Title: F_Panel/FAN/PWR Conn

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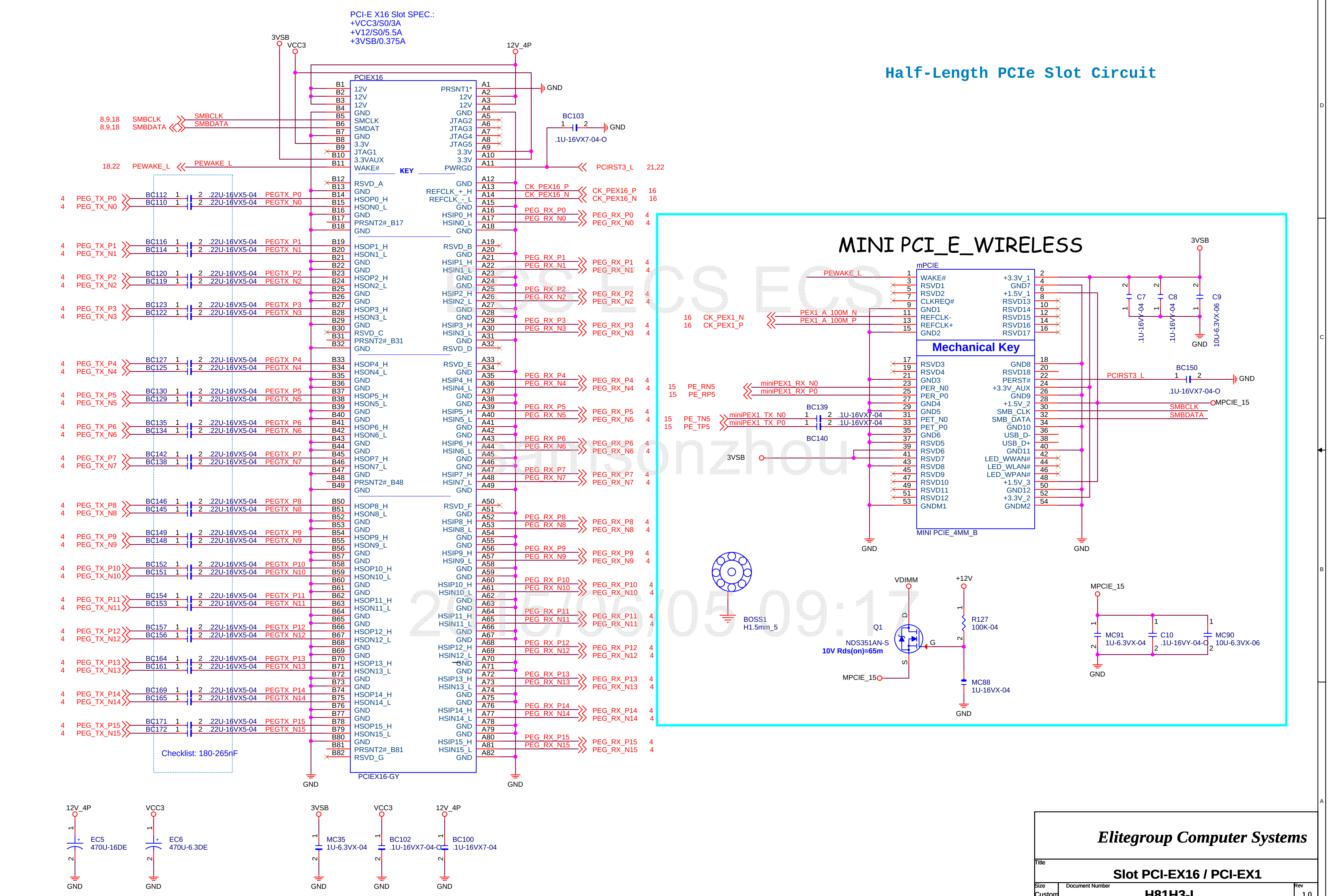

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Title: Slot PCI-EX16 / PCI-EX1

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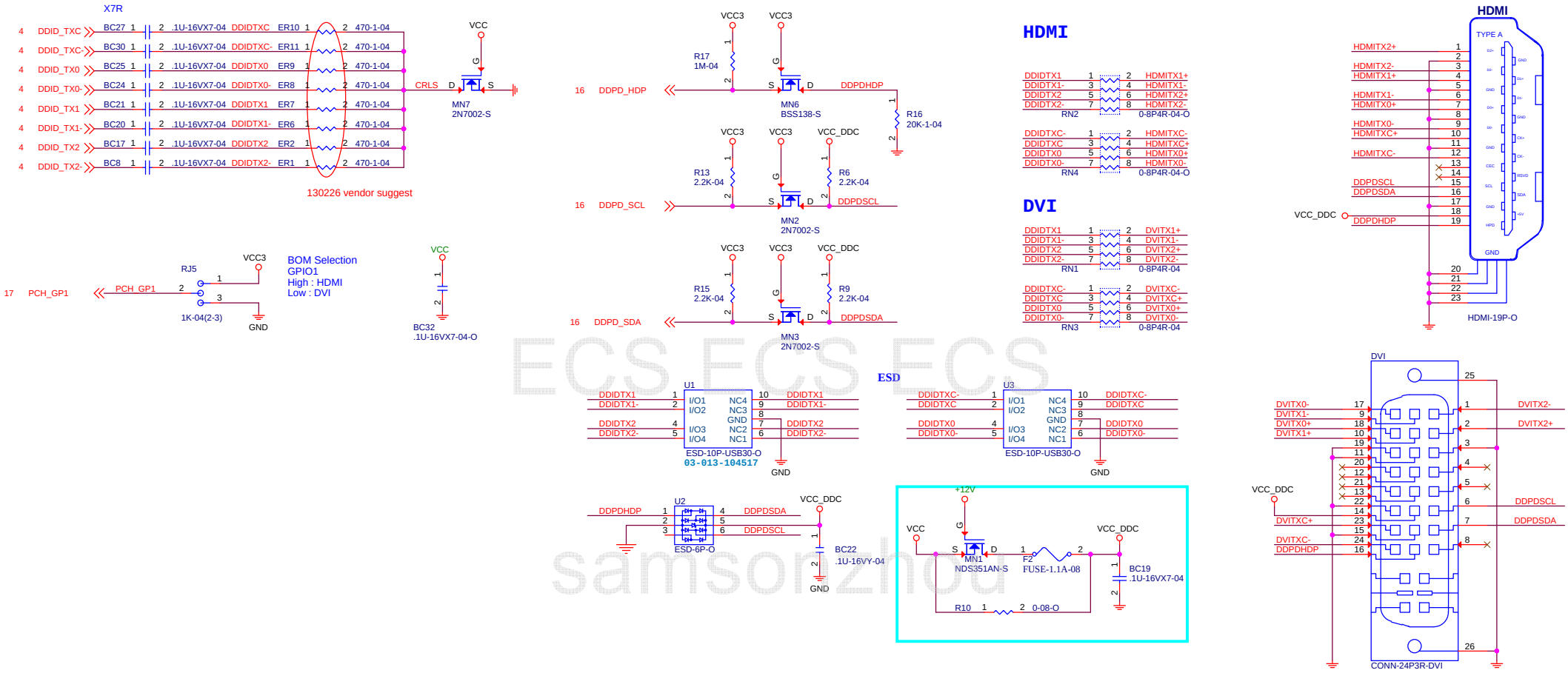

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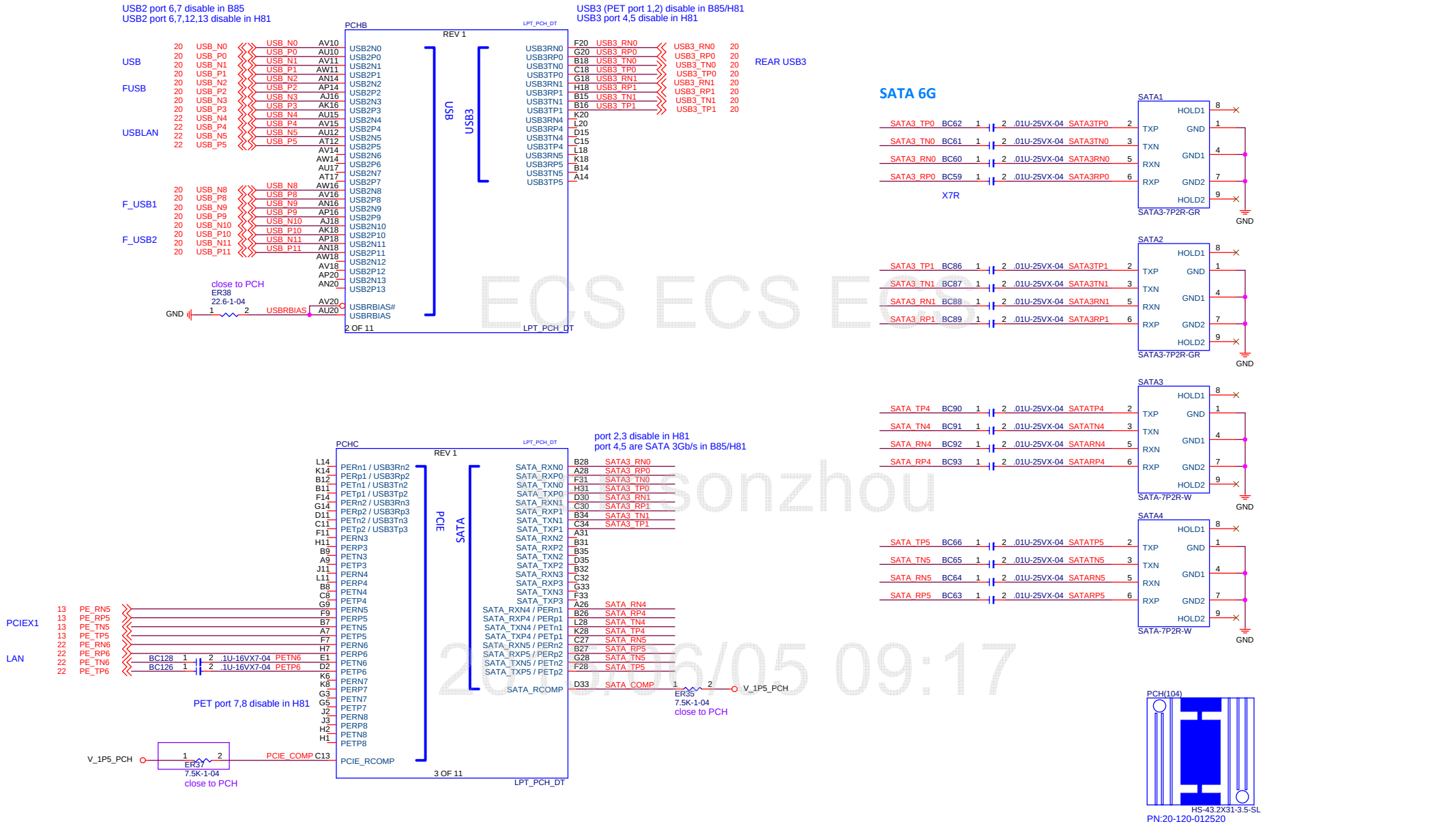

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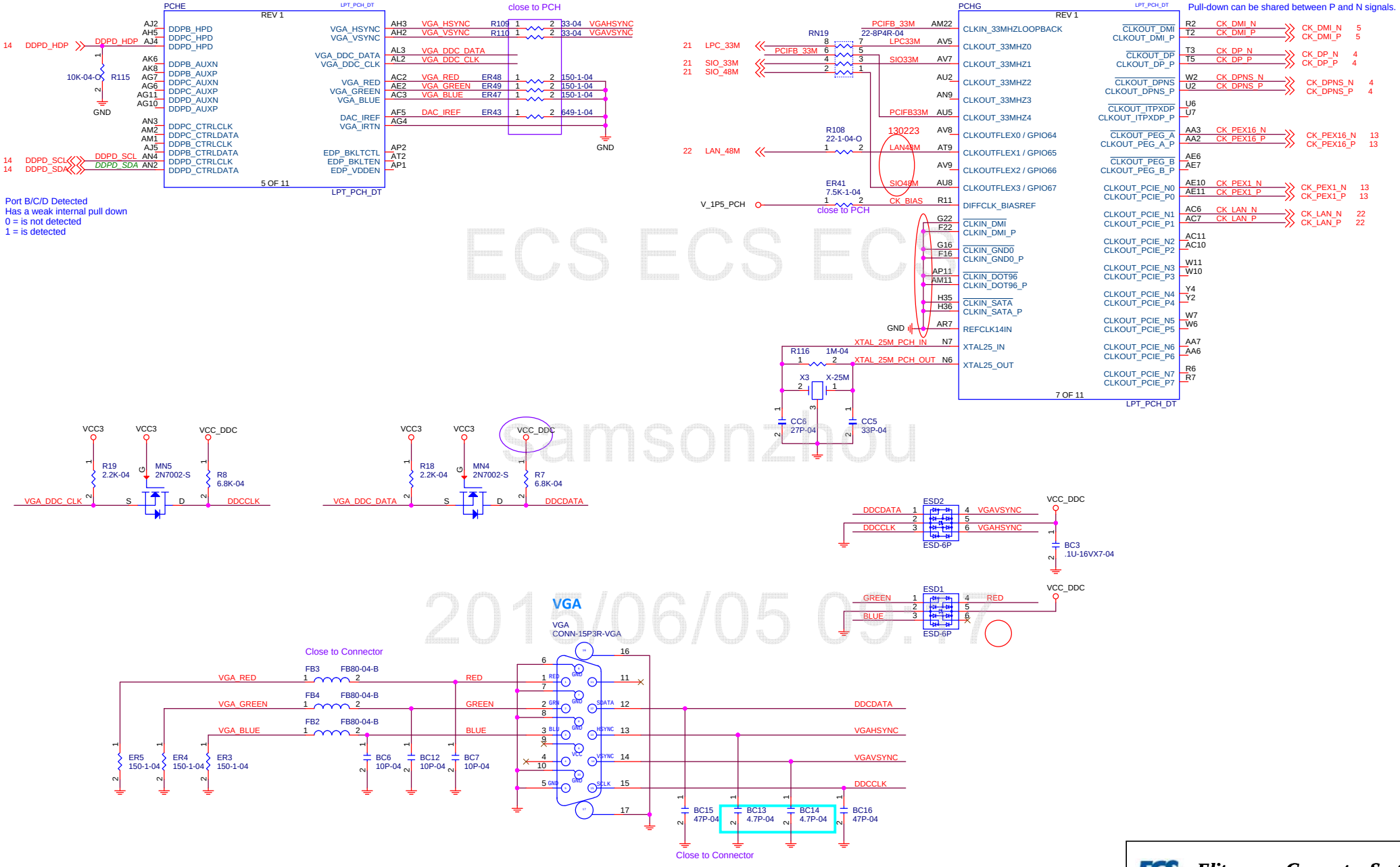

Title	PCH-DDI/VGA/CLK
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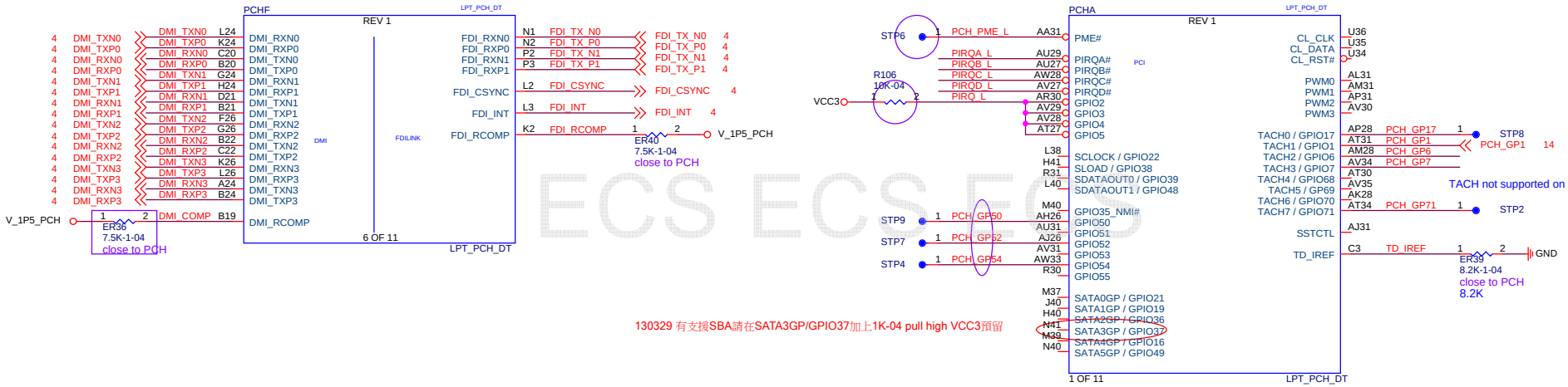


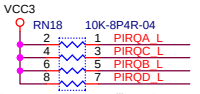
130329 有支援SBA請在SATA3GP/GPIO37加上1K-04 pull high VCC3預留

GPIO51,53,55 with 20Kohm internal pull-up
GPIO53 : DT shouldn't be pulled-down
GPIO55 : TOP-BLOCK swap override when LOW

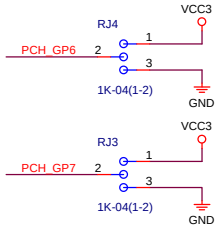
GPIO35,51,53,55 : GPO

GPIO19 with internal pull-up
GPIO36,37 with internal pull-down

Boot Device	GPIO51	GPIO19
LPC	0	0
SPI	1	1



BOM Selection
*GPIO1(Page14)
High : HDMI
Low : DVI
*GPIO6
*GPIO7



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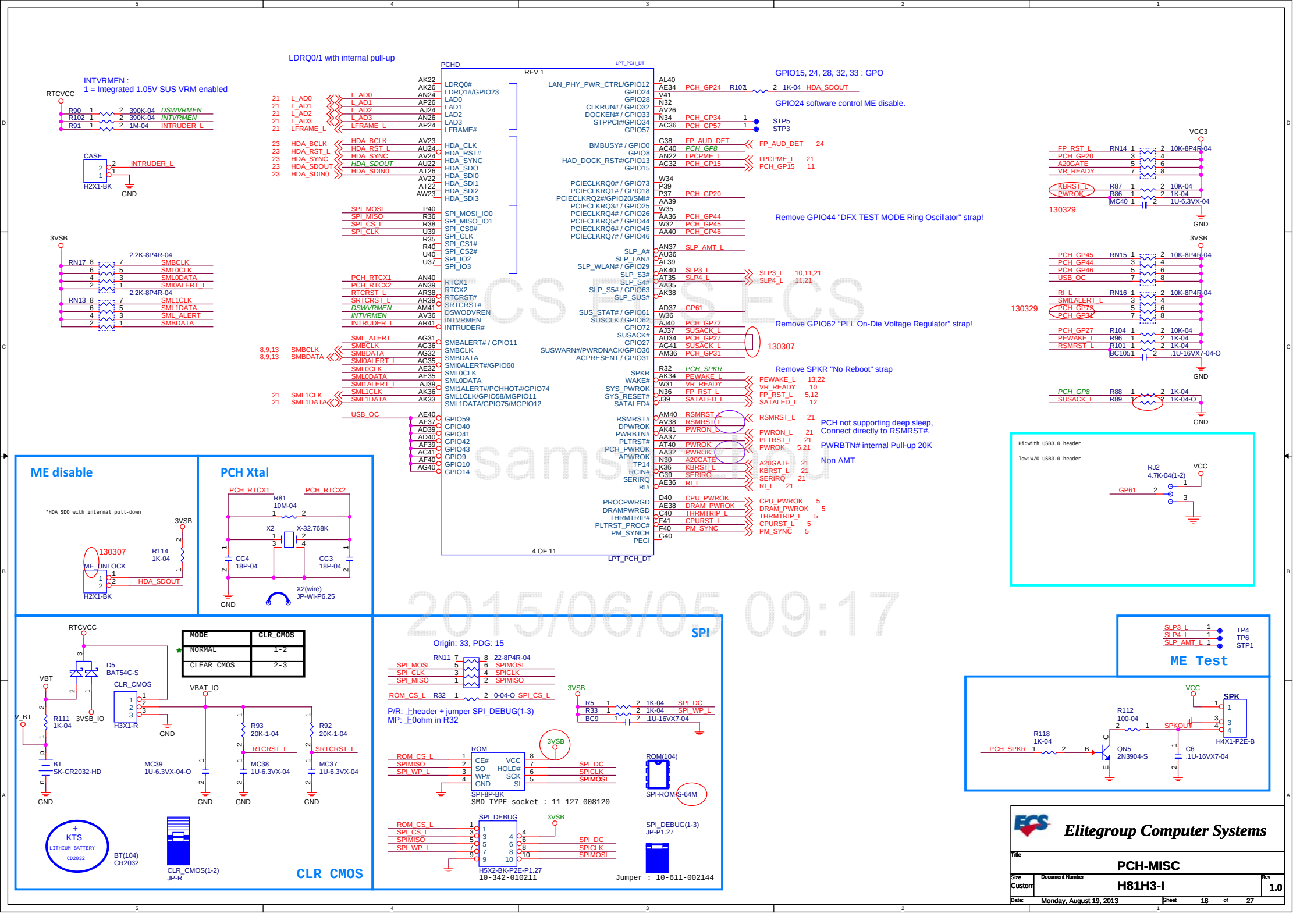
LDRQ0/1 with internal pull-up
INTVRMEN :
1 = Integrated 1.05V SUS VRM enabled
PCHD
REV 1
LPT_PCH_DT
GPIO15, 24, 28, 32, 33 : GPO
GPIO24 software control ME disable.
Remove GPIO44 "DFX TEST MODE Ring Oscillator" strap!
Remove GPIO62 "PLL On-Die Voltage Regulator" strap!
Remove SPKR "No Reboot" strap
PCH not supporting deep sleep,
Connect directly to RSMRST#.
PWRBTN# internal Pull-up 20K
Non AMT
4 OF 11
ME disable
PCH Xtal
CLR CMOS
SPI
ME Test
Origin: 33, PDG: 15
P/R: header + jumper SPI_DEBUG(1-3)
MP: 0ohm in R32
SMD TYPE socket : 11-127-008120
Jumper : 10-611-002144
Hi:with USB3.0 header
low:W/O USB3.0 header
2015/06/05 09:17
Elitegroup Computer Systems
PCH-MISC
H81H3-I
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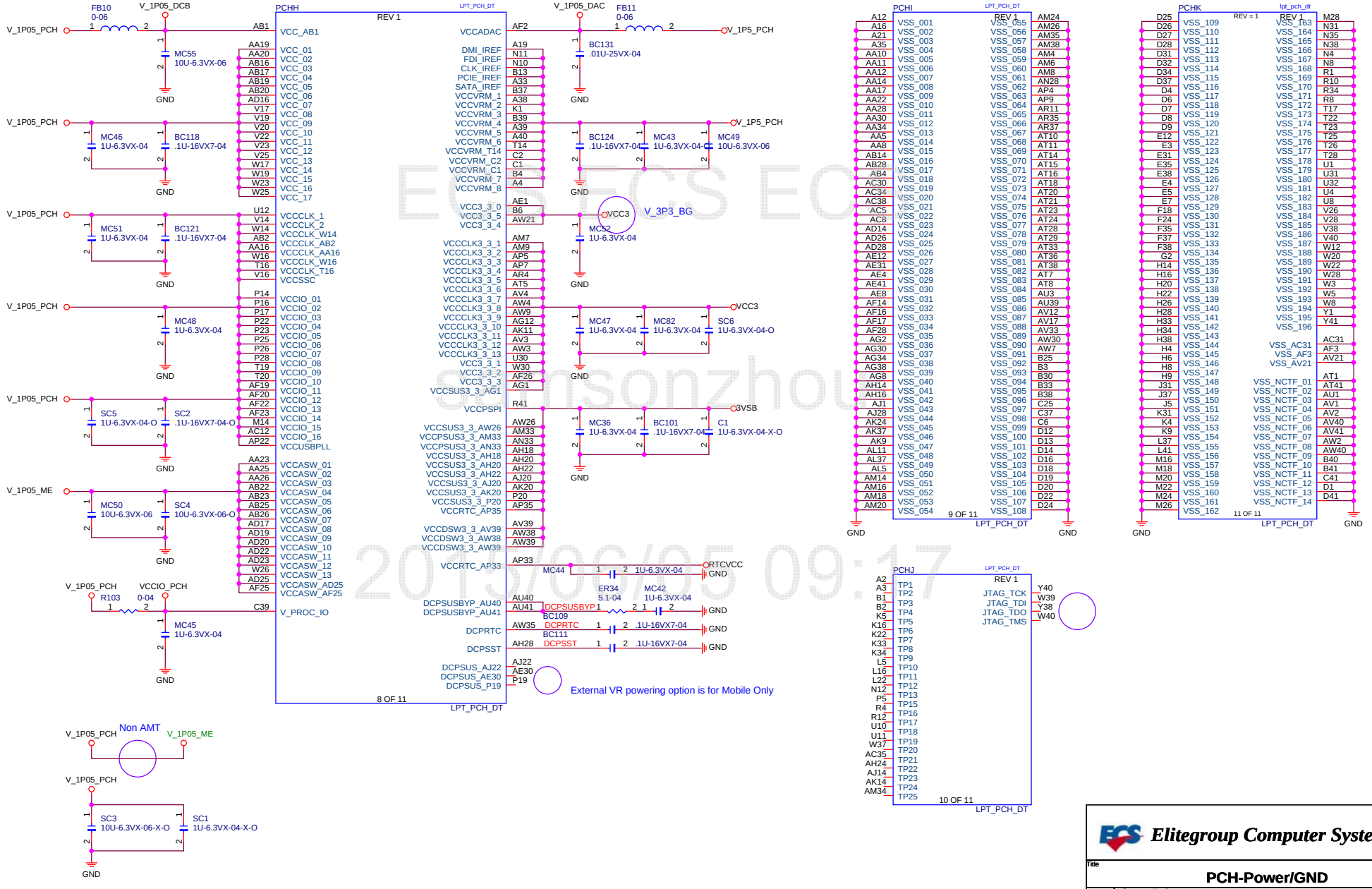
PCHH
REV 1
LPT_PCH_DT
8 OF 11
V_1P05_DCB
V_1P05_DAC
V_1P05_PCH
V_1P05_ME
V_3P3_BG
VCC3
3VSB
RTCVCC
VCCIO_PCH
Non AMT
V_1P05_ME
External VR powering option is for Mobile Only
PCHI
9 OF 11
PCHK
REV = 1
11 OF 11
PCHJ
10 OF 11
Elitegroup Computer Systems
PCH-Power/GND
H81H3-I
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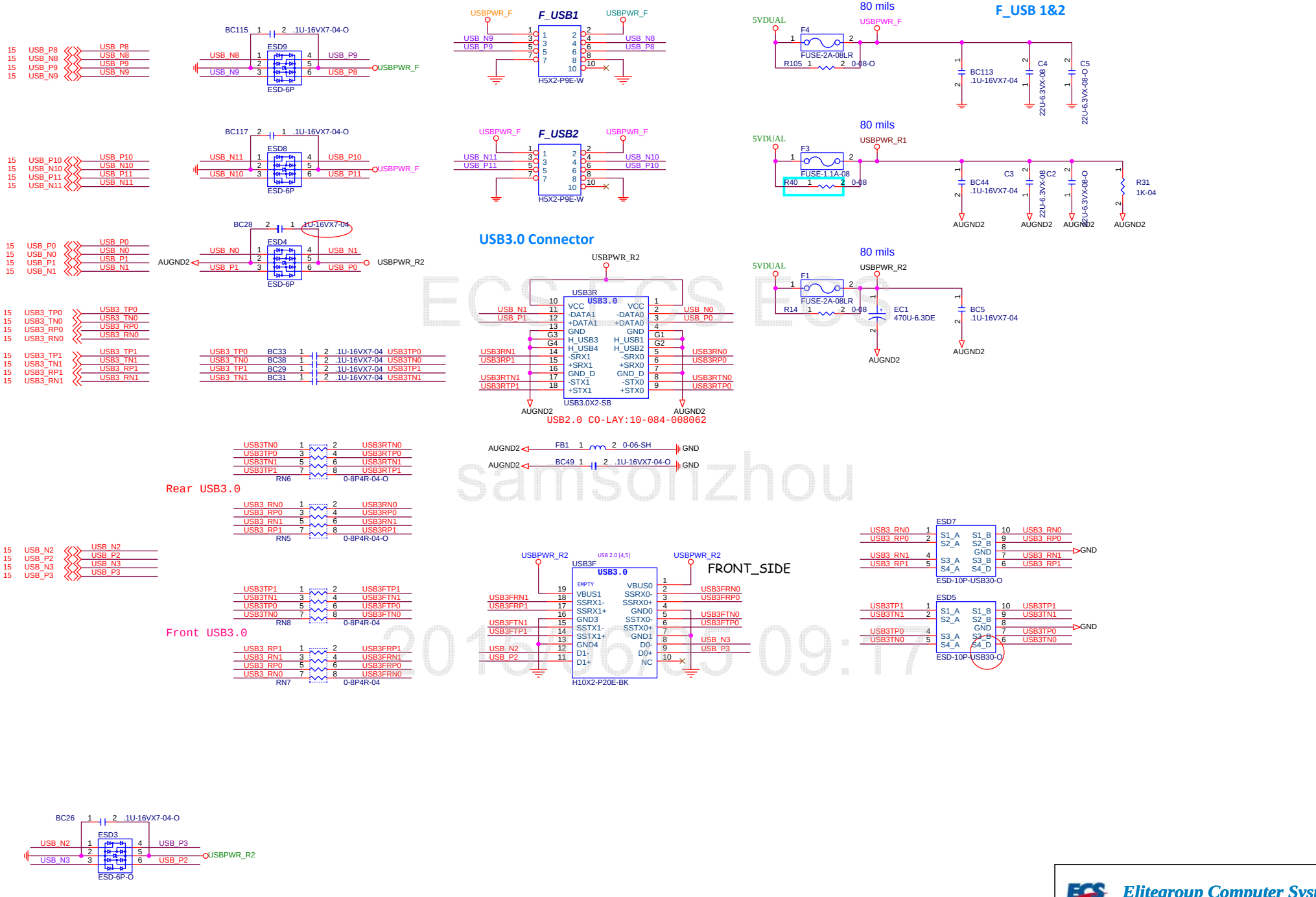

Title	USB/SPI
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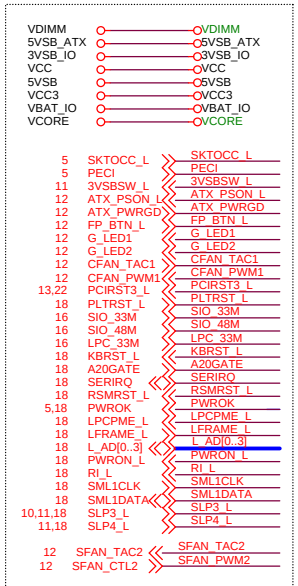
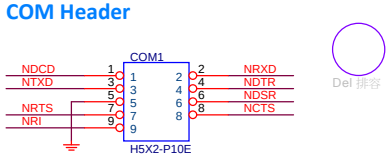
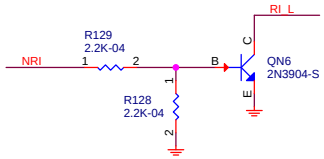
Elitegroup Computer Systems

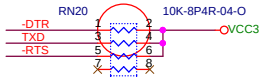
External Connection

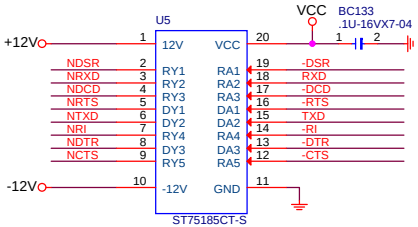


COM Header

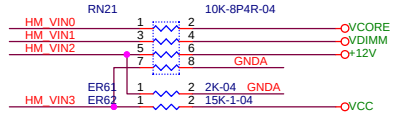






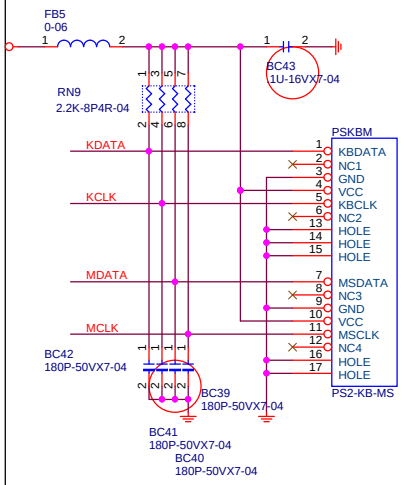


Voltage Monitor

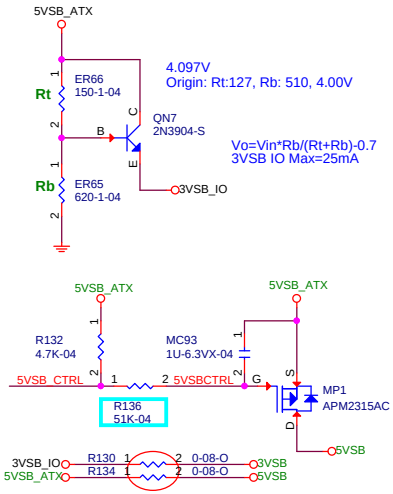


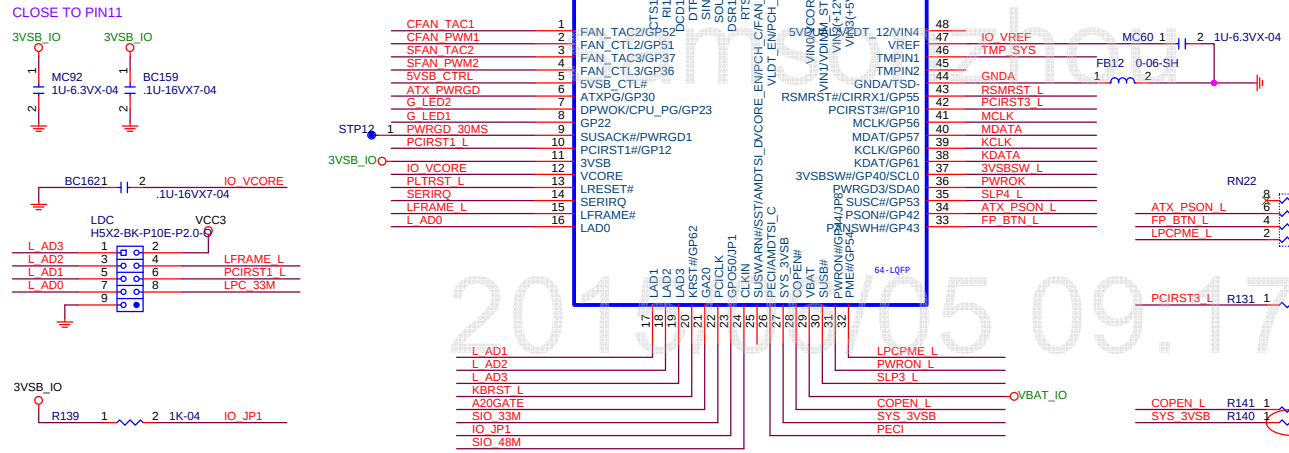
* HM_VIN0 for VCORE
* HM_VIN1 for V_DIMM

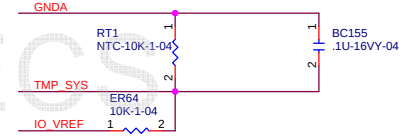
PS2

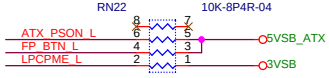


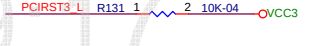
ErP

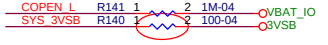


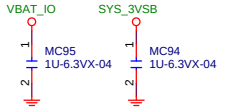


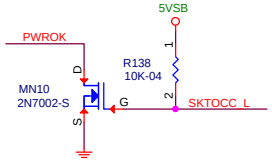












IT8772 Power-On Strapping Options

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP(default)
Pin-23		0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK(default)
Pin-57		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	EC Index 6Bh/73h default = 80h
Pin-59		0	EC Index 6Bh/73h default = 00h
JP4	K8PWR_EN	1	Disable K8 Power Sequence(default)
Pin-61		0	Enable K8 Power Sequence
JP8	RSMRST_SEL	1	RSMRST# output detected by 3VSB
Pin-31		0	RSMRST# output detected by SYS_3VSB

Elitegroup Computer Systems

Title: SIO-IT8772

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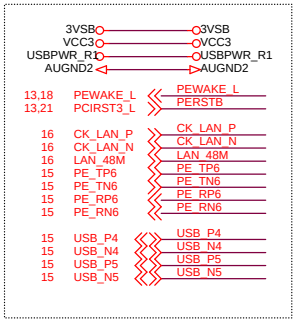
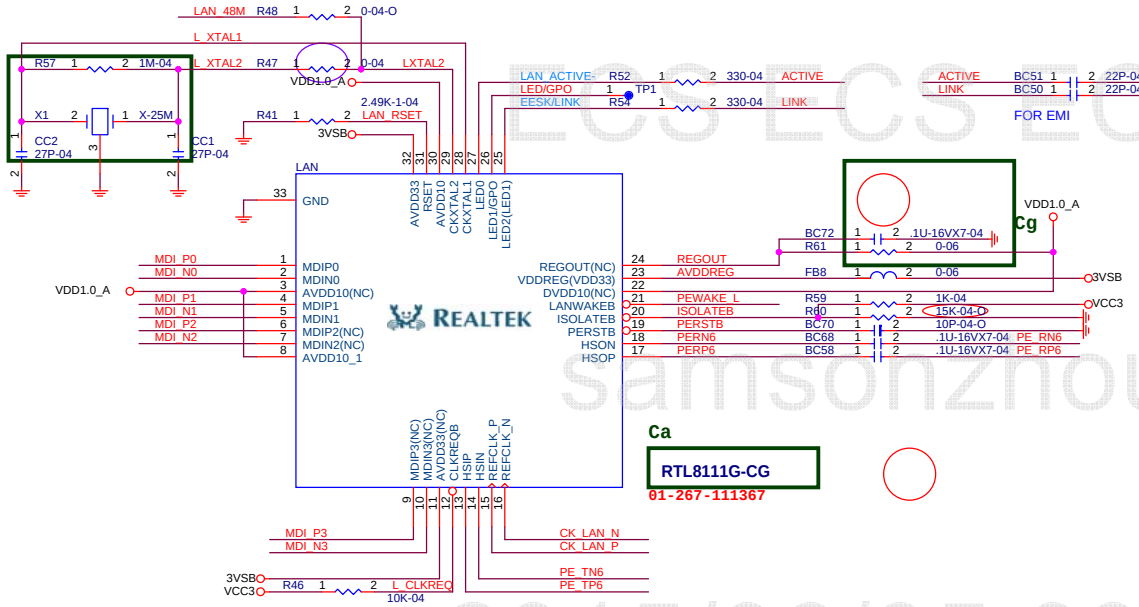
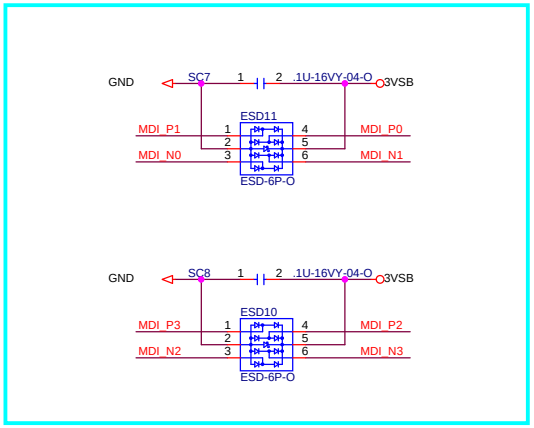
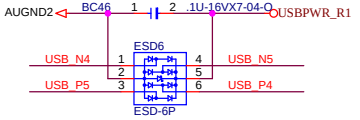
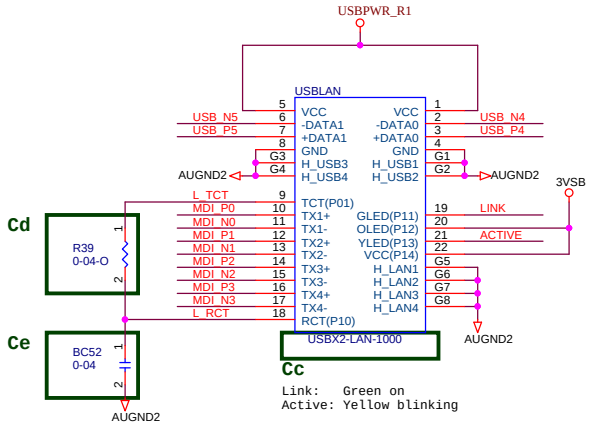
External Connection

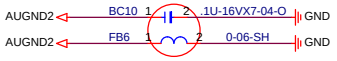












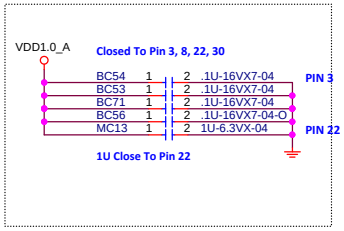
BOM Difference

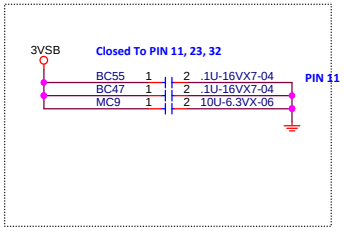
DEFAULT

	RTL8111G-CG (LDO mode) 1000M	RTL8106E-CG (LDO mode) 10/100M
Ca	RTL8111G-CG	RTL8106E-CG
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cg	R	X

8106E : NC PIN - 3,6,7,9,10,11,22,24

MC15,BC46,BC35 -O,BC41 1U-6.3VX-04





Elitegroup Computer Systems

Title: LAN-RT8111GS/8106E

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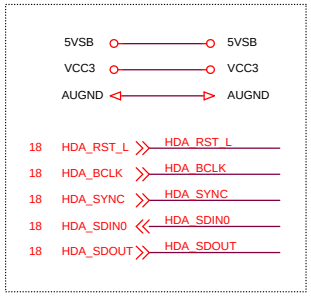
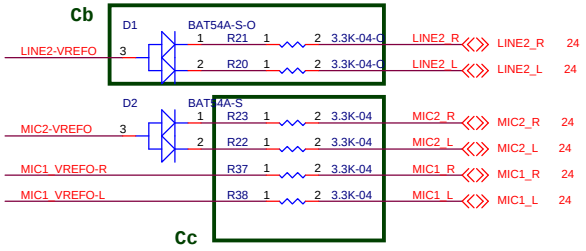
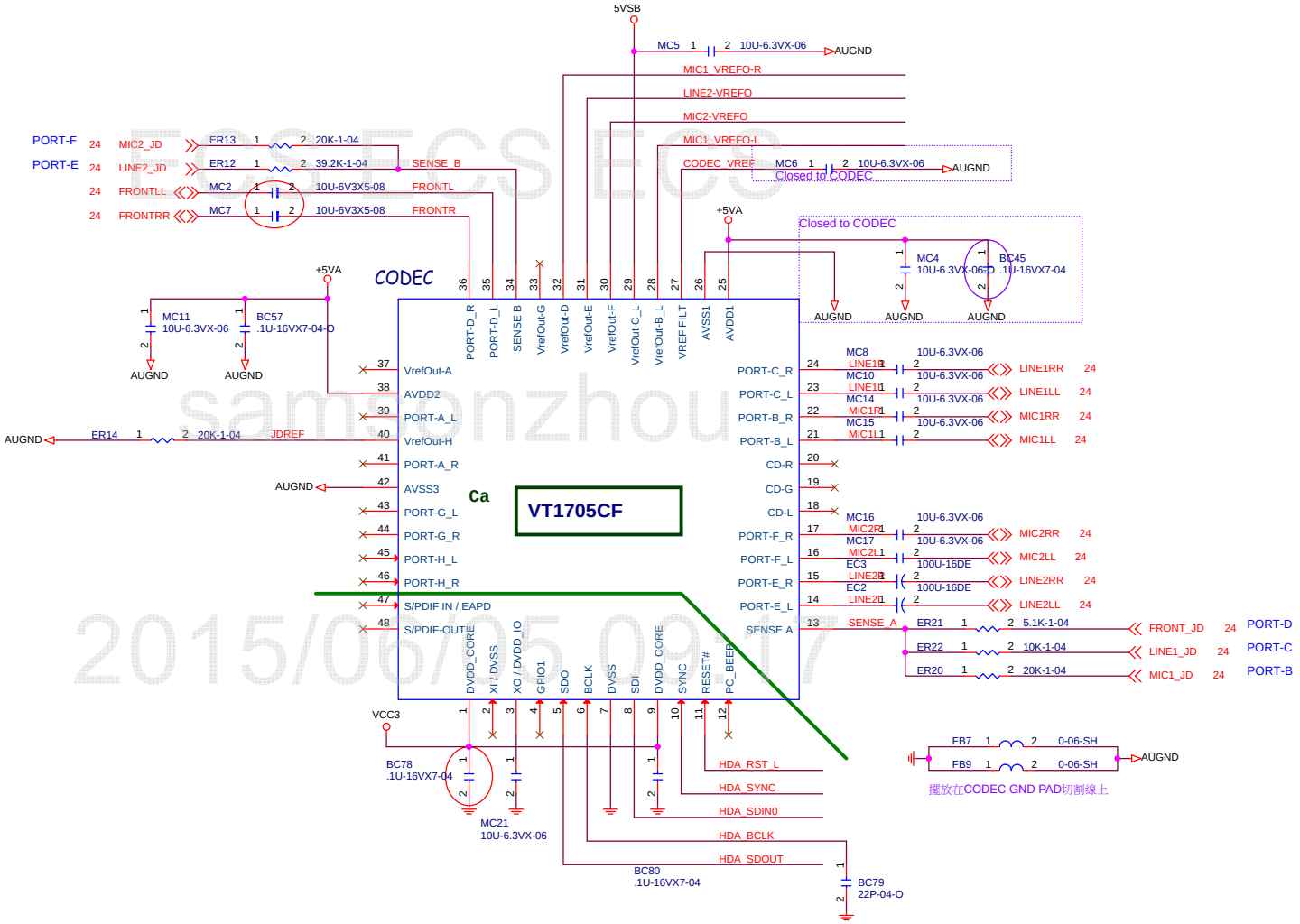
External Connection







Pin Difference

Pin	ALC662VD	VT1705CF
2	GPIO0	GPIO0/SPDIF_TX1/ DMIC_CLK
3	REG VREF	REGREF
4	GPIO1	GPIO1/DMIC_DATA
25	LDO OUTPUT	LDO_OUT1
29	LDO VIN	LDO_IN
33	LINE1 VREF	SENSE_C
37	FRONT VREF ?	VREFOUT_C
38	LDO OUTPUT	LDO_OUT2
45	DMIC DATA	NC
46	DMIC CLK	NC
47	EADP	EADP/SPIDF_RX

01-278-662350 02-301-705622

BOM Difference

Location	ALC662VD	VT1705CF
Ca	ALC662-VD0-GR	VT1705CF
Cb	V	X
Cc	2.2K-04	3.3K-04
Cd	75-04	33-04

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

Elitegroup Computer Systems	
Title	VT1705CF(Chip)
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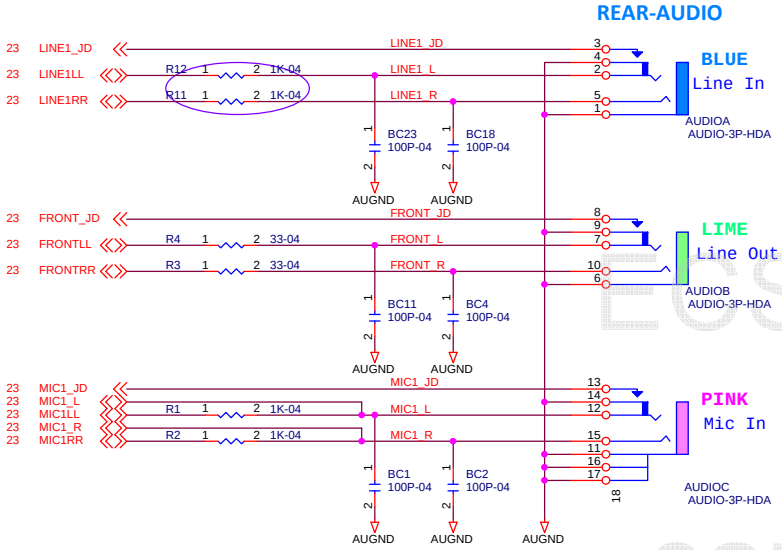
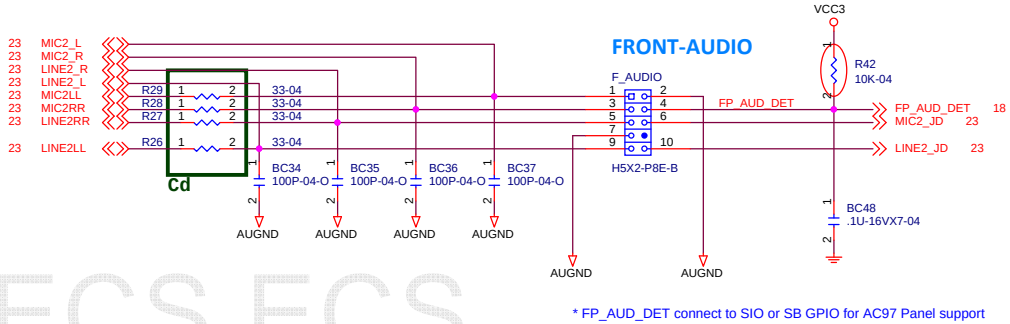
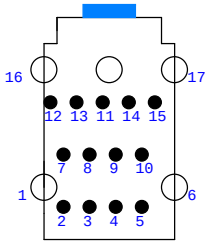
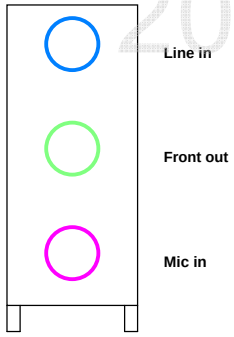


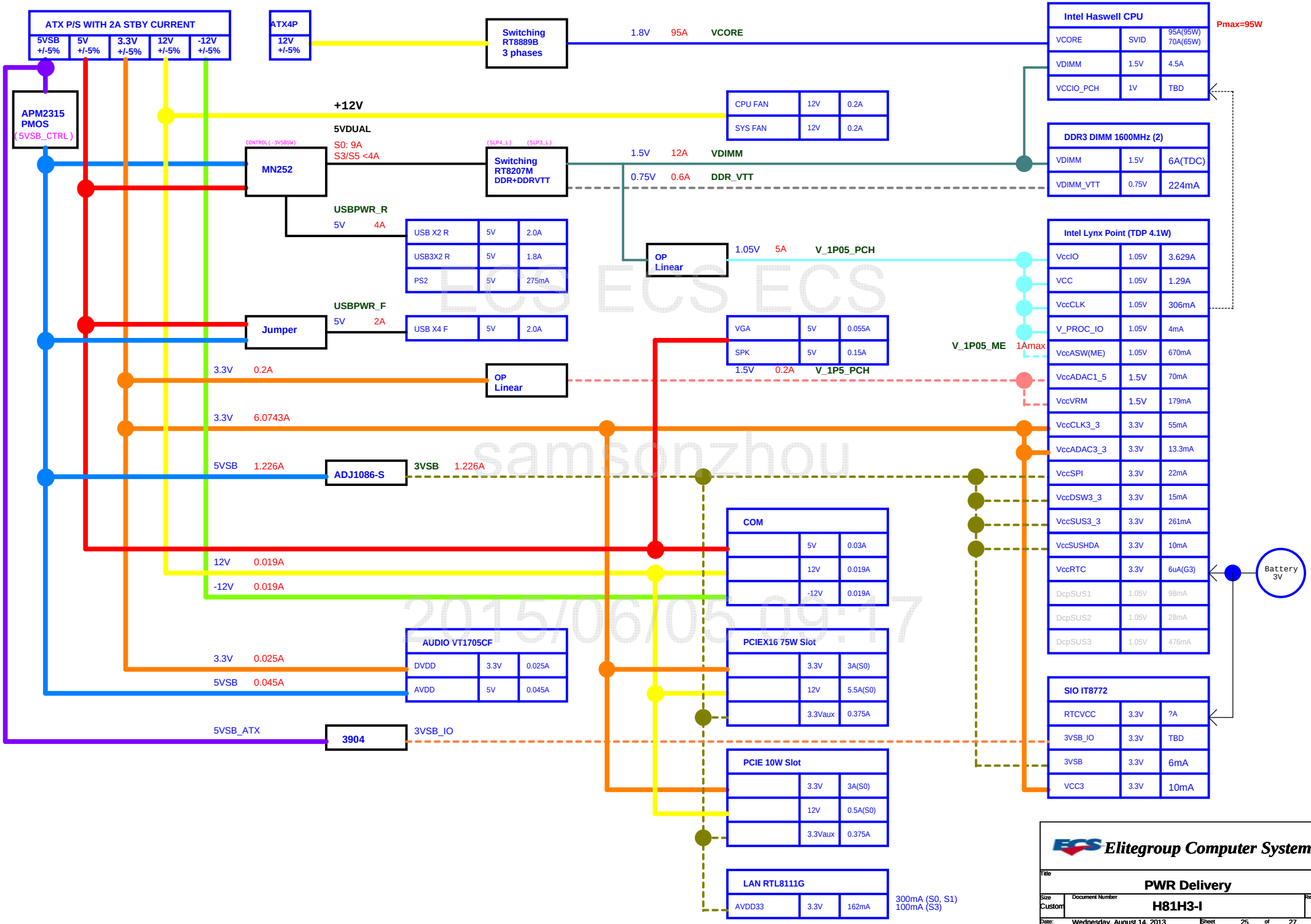


* FP_AUD_DET connect to SIO or SB GPIO for AC97 Panel support





Elitegroup Computer Systems		
Title: VT1705CF(Panel)		
Size: Custom	Document Number: H81H3-I	Rev: 1.0
Date: Wednesday, August 14, 2013	Sheet 24 of 27	


ATX P/S WITH 2A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
Switching RT8889B 3 phases
1.8V 95A VCORE
Intel Haswell CPU
Pmax=95W
VCORE SVID 95A(95W) 70A(65W)
VDIMM 1.5V 4.5A
VCCIO_PCH 1V TBD
APM2315 PMOS (5VSB_CTRL)
+12V
5VDUAL
CPU FAN 12V 0.2A
SYS FAN 12V 0.2A
CONTROL(-3VSBSW)
MN252
S0: 9A
S3/S5 <4A
(SLP4_L) (SLP3_L)
Switching RT8207M DDR+DDRVTT
1.5V 12A VDIMM
0.75V 0.6A DDR_VTT
DDR3 DIMM 1600MHz (2)
VDIMM 1.5V 6A(TDC)
VDIMM_VTT 0.75V 224mA
USBPWR_R
5V 4A
USB X2 R 5V 2.0A
USB3X2 R 5V 1.8A
PS2 5V 275mA
OP Linear
1.05V 5A V_1P05_PCH
Intel Lynx Point (TDP 4.1W)
VccIO 1.05V 3.629A
VCC 1.05V 1.29A
VccCLK 1.05V 306mA
V_PROC_IO 1.05V 4mA
VccASW(ME) 1.05V 670mA
VccADAC1_5 1.5V 70mA
VccVRM 1.5V 179mA
VccCLK3_3 3.3V 55mA
VccADAC3_3 3.3V 13.3mA
VccSPI 3.3V 22mA
VccDSW3_3 3.3V 15mA
VccSUS3_3 3.3V 261mA
VccSUSHDA 3.3V 10mA
VccRTC 3.3V 6uA(G3)
DcpSUS1 1.05V 98mA
DcpSUS2 1.05V 28mA
DcpSUS3 1.05V 476mA
Battery 3V
USBPWR_F
5V 2A
Jumper
USB X4 F 5V 2.0A
VGA 5V 0.055A
SPK 5V 0.15A
V_1P05_ME 1Amax
1.5V 0.2A V_1P5_PCH
OP Linear
3.3V 0.2A
3.3V 6.0743A
5VSB 1.226A
ADJ1086-S
3VSB 1.226A
COM
5V 0.03A
12V 0.019A
-12V 0.019A
12V 0.019A
-12V 0.019A
AUDIO VT1705CF
DVDD 3.3V 0.025A
AVDD 5V 0.045A
3.3V 0.025A
5VSB 0.045A
PCIEX16 75W Slot
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
SIO IT8772
RTCVCC 3.3V ?A
3VSB_IO 3.3V TBD
3VSB 3.3V 6mA
VCC3 3.3V 10mA
5VSB_ATX
3904
3VSB_IO
PCIE 10W Slot
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
LAN RTL8111G
AVDD33 3.3V 162mA
300mA (S0, S1)
100mA (S3)
ECS ECS ECS
samsonzhou
2015/06/05 09:17
Elitegroup Computer Systems
Title
PWR Delivery
Size Custom
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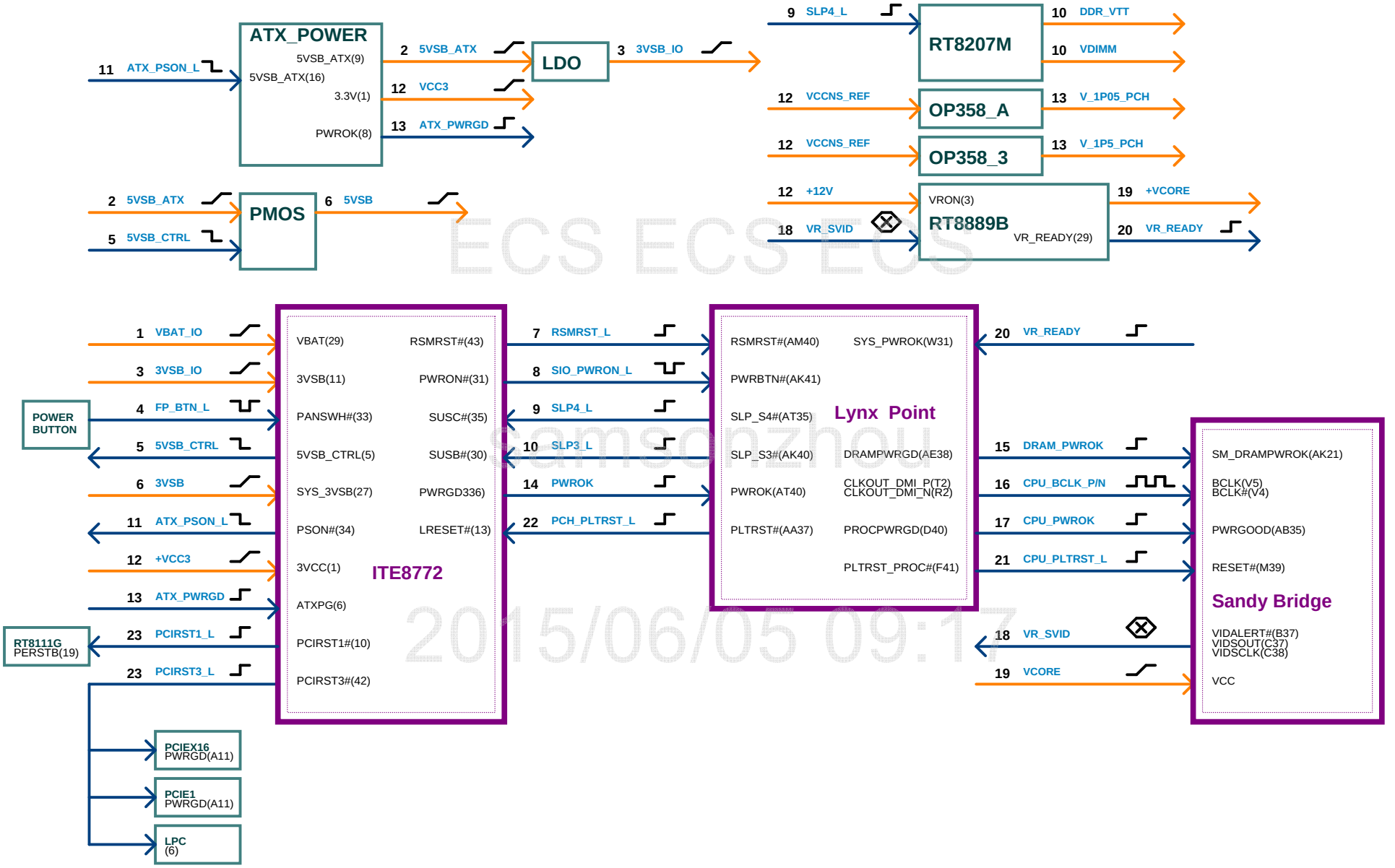

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Title: PWR Sequence/RST Diagram

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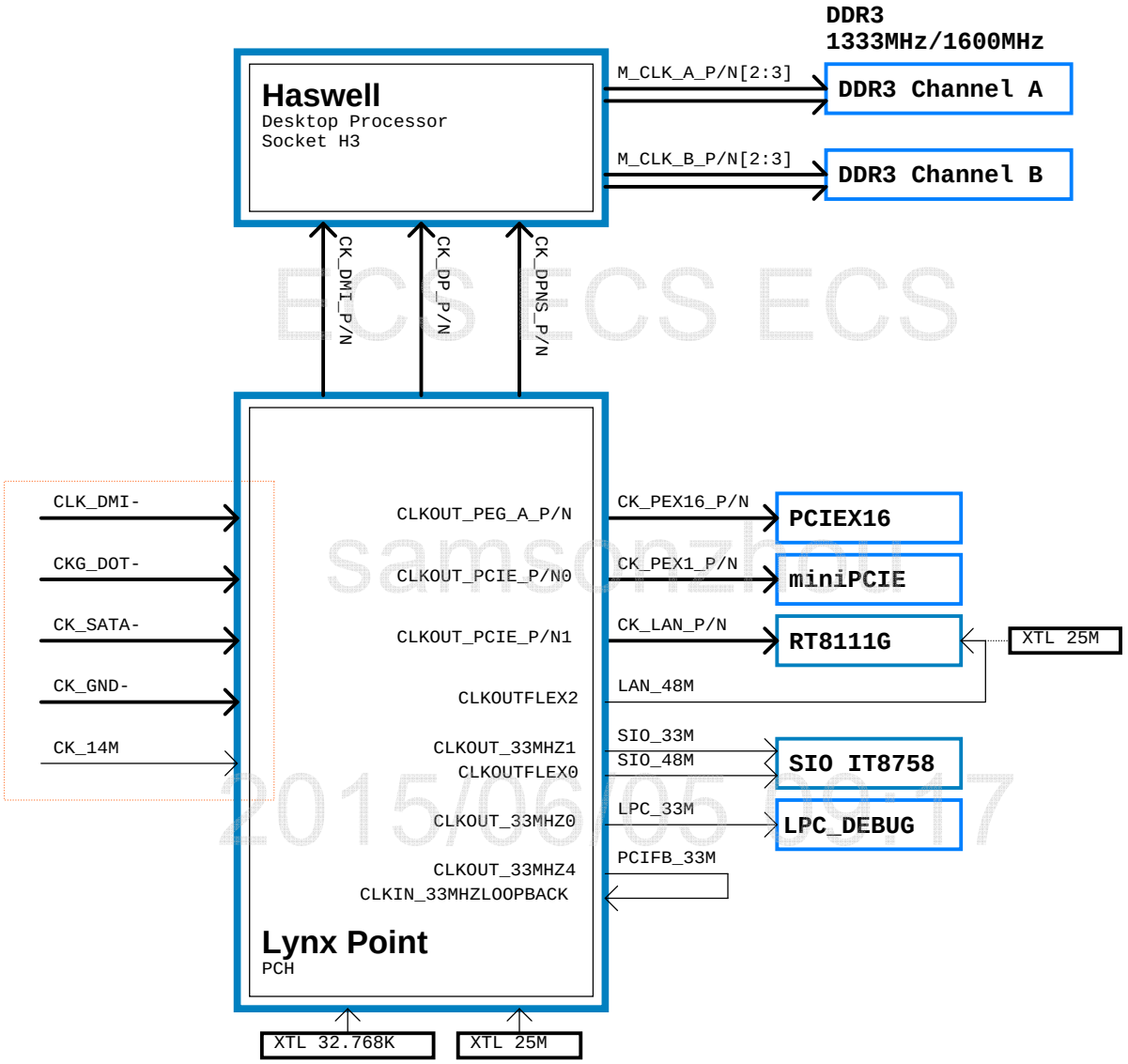

Elitegroup Computer Systems

Title: CLK Distribution

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