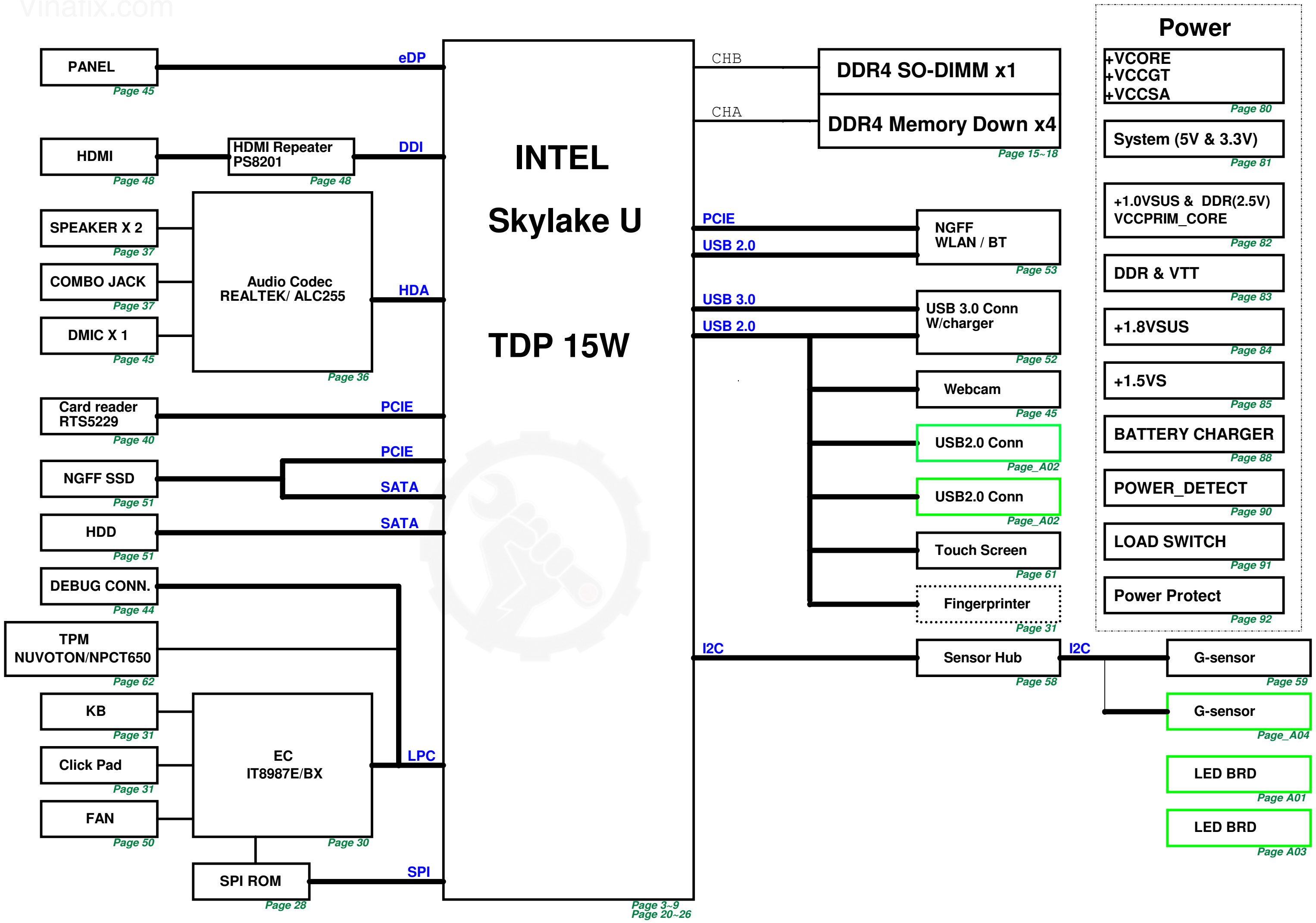
SYSTEM PAGE REF.

01. Block Diagram
02. GPIO Setting
03. CPU(1)_DDI/eDP
04. CPU(2)_DDR4
05. CPU(3)_+VCCCORE
06. CPU(4)_+VCCGT
07. CPU(5)_+VDDQ/IO/SA
08. CPU(6)_CPU GND
09. CPU(7)_CFG/RSVD
13. TYPE-C (CC)
14. TYPE-C (MUX + Redriver)
16. LPDDR3(1)_MEMORY DOWN
17. LPDDR3(2)_MEMORY DOWN
18. LPDDR3(3)_CA/DQ Voltage
20. PCH(1)_SPI/LPC
21. PCH(2)_ISH
22. PCH(3)_HDA/SDIO
23. PCH(4)_USB/PCIE/SATA
24. PCH(5)_CLK/RTC
25. PCH(6)_POWER MANAGEMENT
26. PCH(7)_POWER
28. PCH(9)_SPI/SMB
30. EC_IT8587/FX
31. EC_IT8587E/FX_KB/TP/KBBL
32. RST_Reset Circuit
36. ALC255_Combo Jack,SPK,DMIC
37. xxx AUDIO HP/MIC JACK
40. xxx CB_RTS5170_GR
44. Debug CONN
45. CRT(1)_eDP,CAMERA,TSN
48. HDMI OUT
50. THERMAL / FAN
51. NGFF PCIE/SATA SSD x2
52. USB 3.0/Sleep Charge IC
53. NGFF PCIE WLAN/BT
55. xxx CAMERA
56. xxx LED
57. Discharge
58. SHB_Sensor Hub
60. DC_DC/BAT CONN
62 TPM NPCT650
64. IO Board
65. ME_CONN / Skew Hole
68. BYPASS EC SEQUENCE
69. Power Switch
80_POWER_VCORE for U22
81_POWER_SYSTEM
82_POWER_+1.0VSUS
83_POWER_ DDR & VTT_UMA
84_POWER_ 1.8VSUS
85_POWER_XXX
86_POWER_XXX
87_POWER_XXX
88_POWER_CHARGER
89_POWER_AC_PD_WC Input
90_POWER_DETECT
91_POWER_LOAD SWITCH
92_POWER_PROTECT
93_POWER_SIGNAL
94_POWER_FLOWCHART
97. System History
A01. Power On Sequence
A02. Power On Timing
B01. LED Board/LED, Hall Sensor
B02. IO Board/CB, USB2, Key
B03. Sensor Board/G-SEN,DMIC

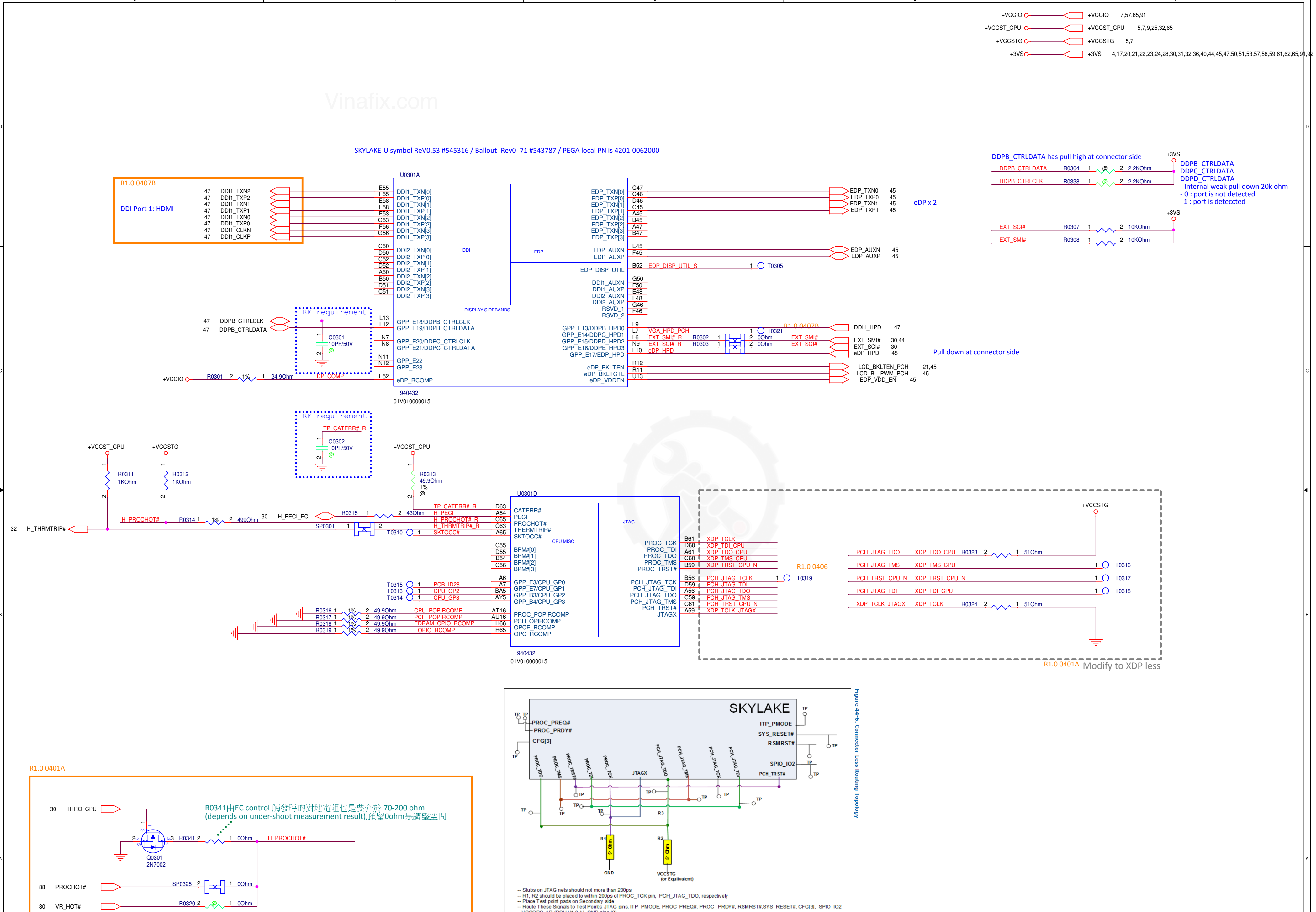
ST5DB for Skylake U Platform Block Diagram



Discharge Circuit (Page 57)	DC & BATT. Conn. (Page 60)
Reset Circuit (Page 32)	Skew Holes (Page 65)

<Variant Name>

PEGATRON	Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
	Engineer:		
Size C	STPDP Project Name		Rev 1.0
Date:	Monday, July 18, 2016	Sheet 2	of 110



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

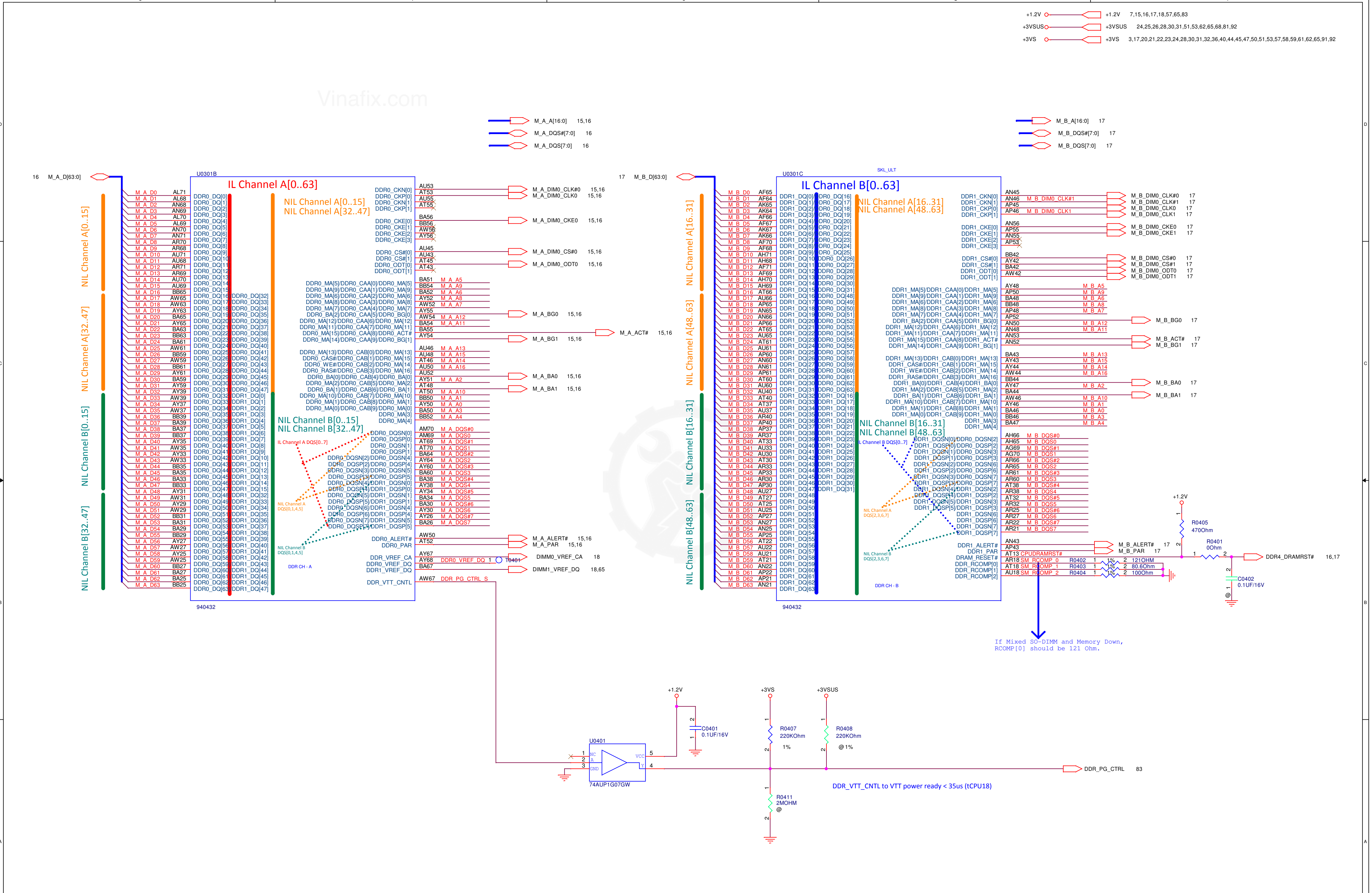
Title : CPU(1)_DDI/eDP

BG1/HW3

Engineer: Jack_Lee

Size	Project Name	Rev
C	ST5DB	1.0

Date: Monday, July 18, 2016 | Sheet 3 of 110



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

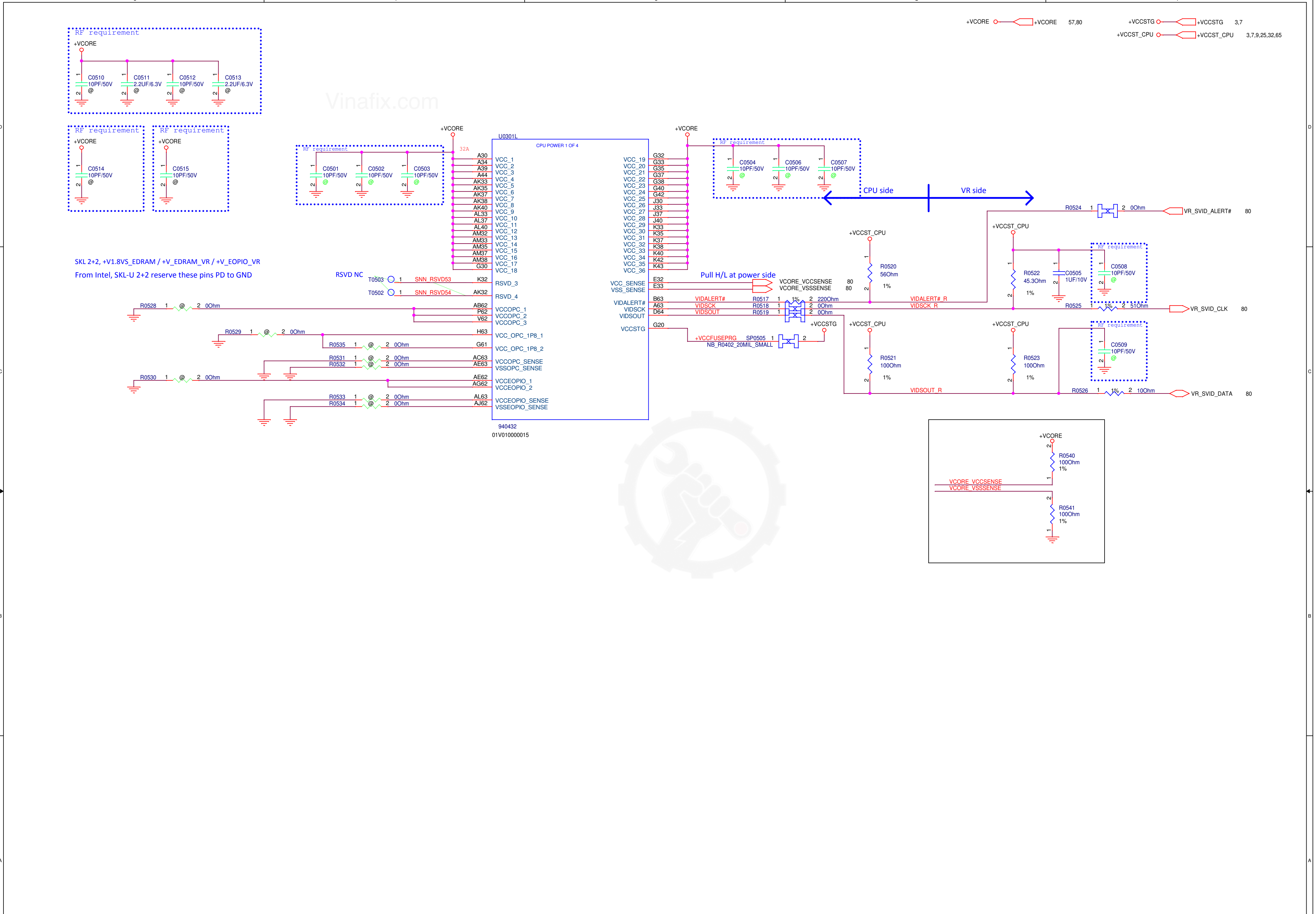
Title : CPU(2)_DDR3L

BG1/HW3

Engineer: Jack_Lee

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 4 of 110



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

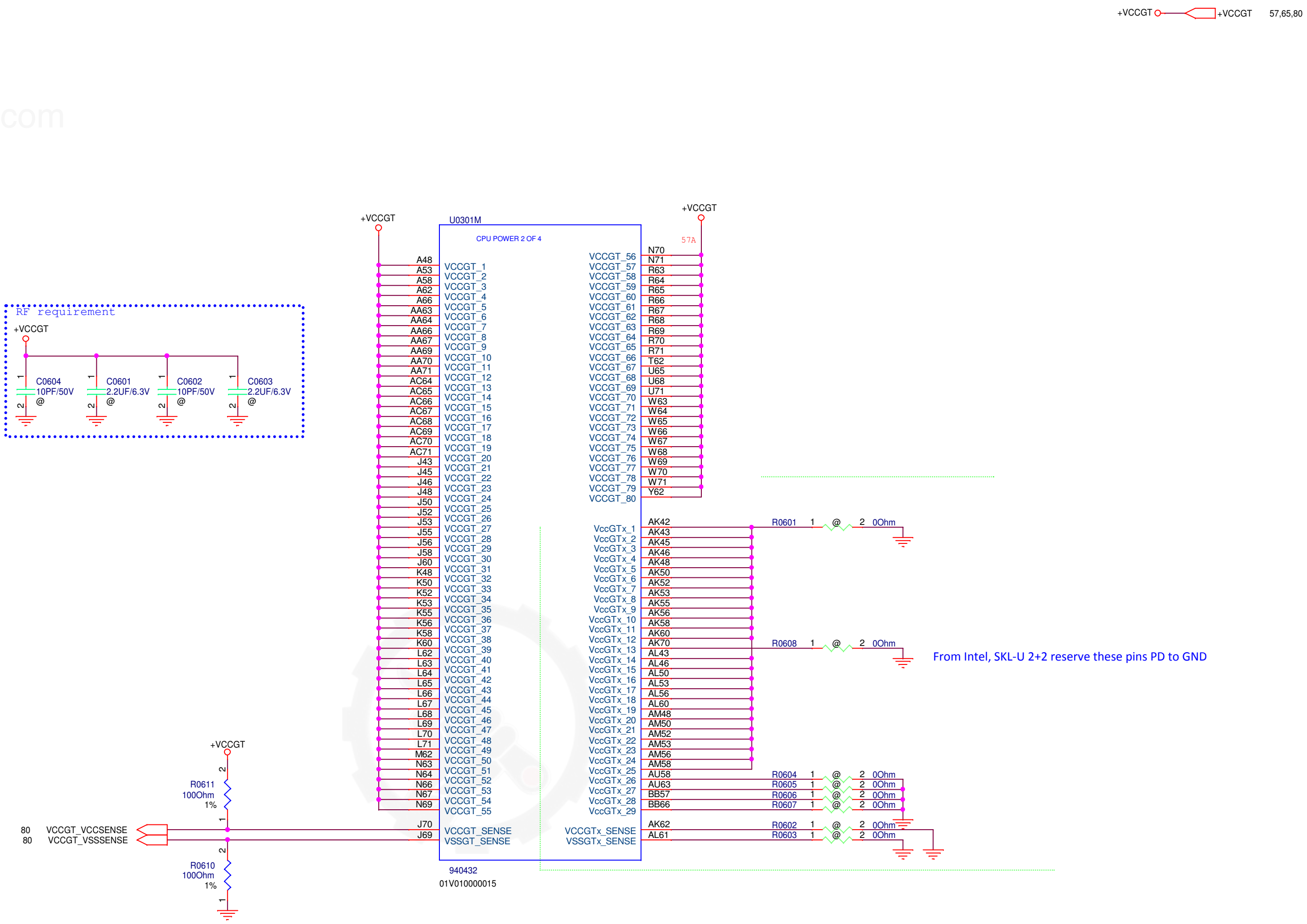
Title: CPU(3)_+VCCCORE

BG1/HW3

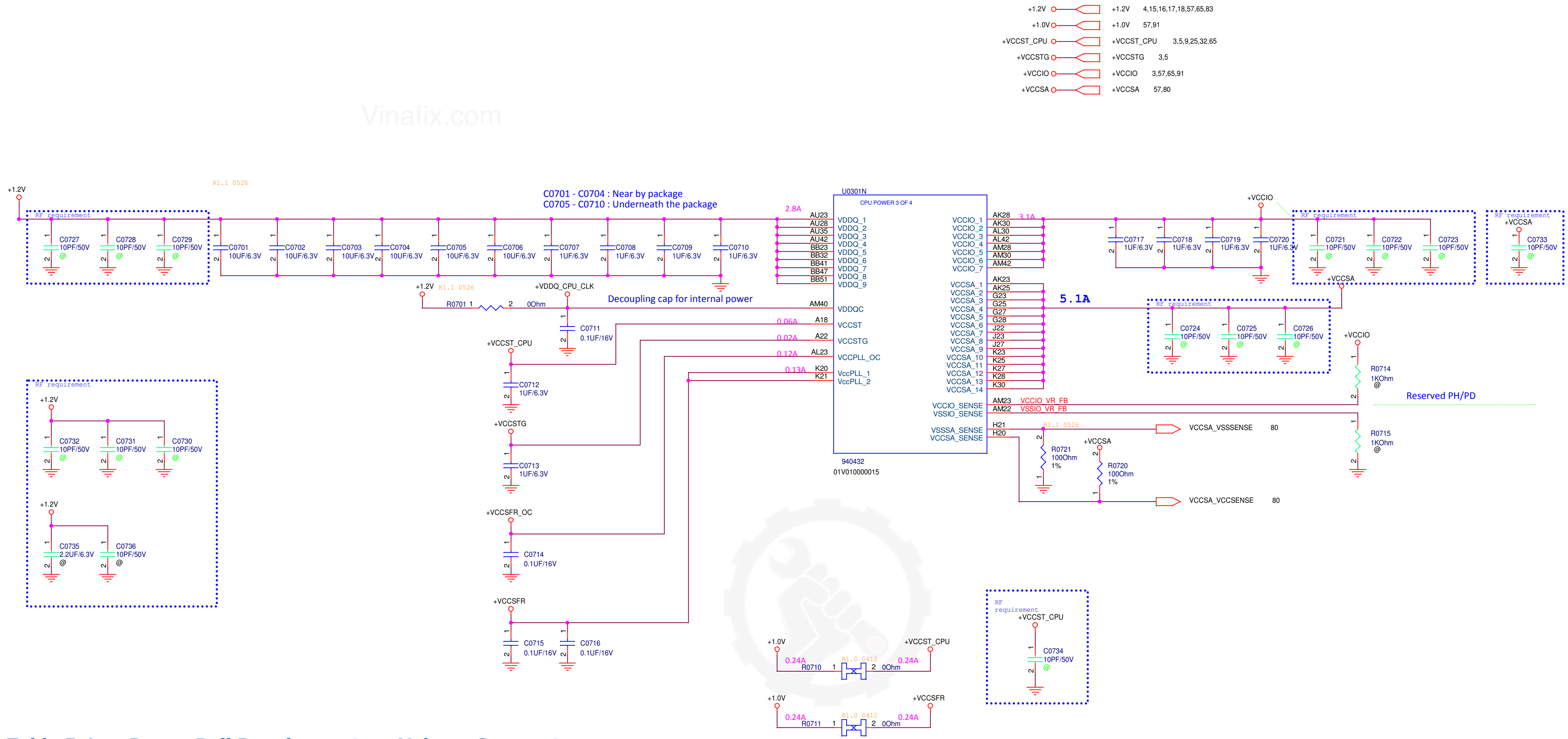
Engineer: Jack_Lee

Size	Project Name	Rev
C	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 5 of 110



PEGATRON	Title :	CPU(4)_+VCCGT
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3	Engineer:	Jack_Lee
Size: C	Project Name: ST5DB	Rev: 1.0
Date: Monday, July 18, 2016	Sheet 6 of 110	



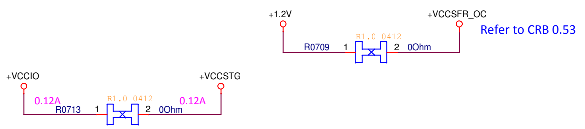
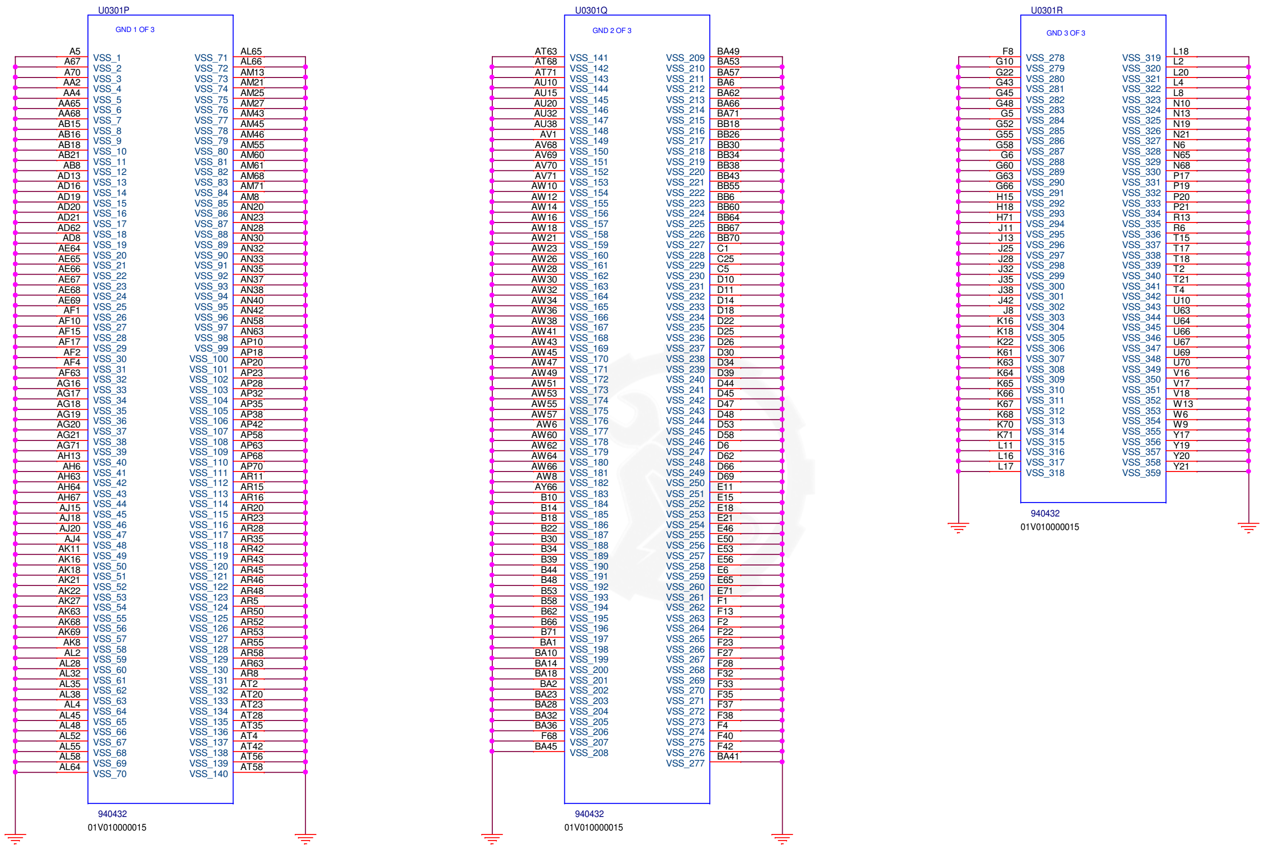


Table 5-1. Power Rail Requirements — Volume Segment — U-Line

Load switch (LS)	LS ENABLE	Load/Rail name	Imax (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc_{ST}	0.04
		$Vcc_{PLL}(Vcc_{SFR})$	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VccIO	3.0
		Vcc_{STG}	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu_04



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : CPU(6)_CPU GND

BG1/HW3

Engineer: Jack_Lee

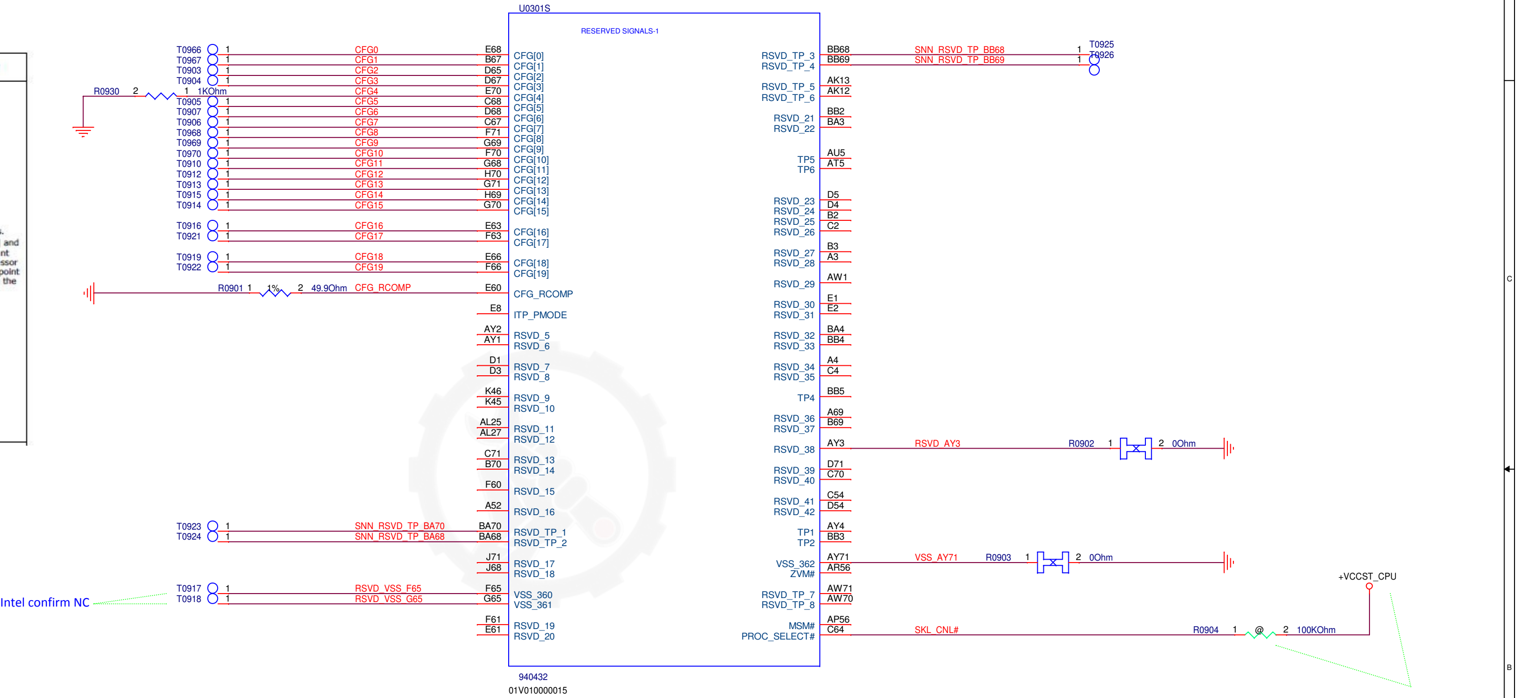
Size	Project Name	Rev
C	ST5DB	1.0

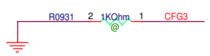
Date: Monday, July 18, 2016 Sheet 8 of 110

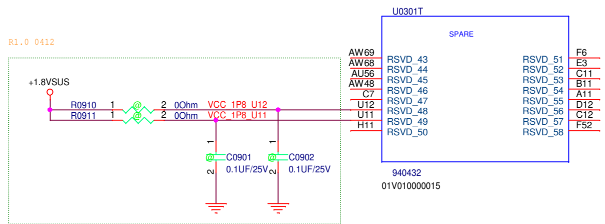
6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.







PDG 1.2
Placeholder only. Does not need to be stuffed.
Placement are required for future platform compatibility purpose only.

PEGATRON Title CPU(7)_CFG/RSVD
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3 Engineer: Jack_Lee
Size C | Project Name ST5DB | Rev 1.0
Date: Monday, July 18, 2016 Sheet 9 of 110

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

Project Name

Rev 1.0

Date: Monday, July 18, 2016 Sheet 10 of 110

<Variant Name>

PEGATRON Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

Size C	Project Name STB08	Rev 1.0
Date: Monday, July 18, 2016	Sheet 11 of 110	

<Variant Name>

PEGATRON **Title :** <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

Size	Project Name	Rev
C	STDP	1.0

Date: Monday, July 18, 2016 Sheet 12 of 110

Vinafix.com

<Variant Name>

PEGATRON **Title :**

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title>

Engineer:

Size C	Project Name STBDP	Rev 1.0
Date: Monday, July 18, 2016	Sheet 13 of 110	

<Variant Name>

PEGATRON **Title :**

PEGATRON PROPRIETARY AND CONFIDENTIAL

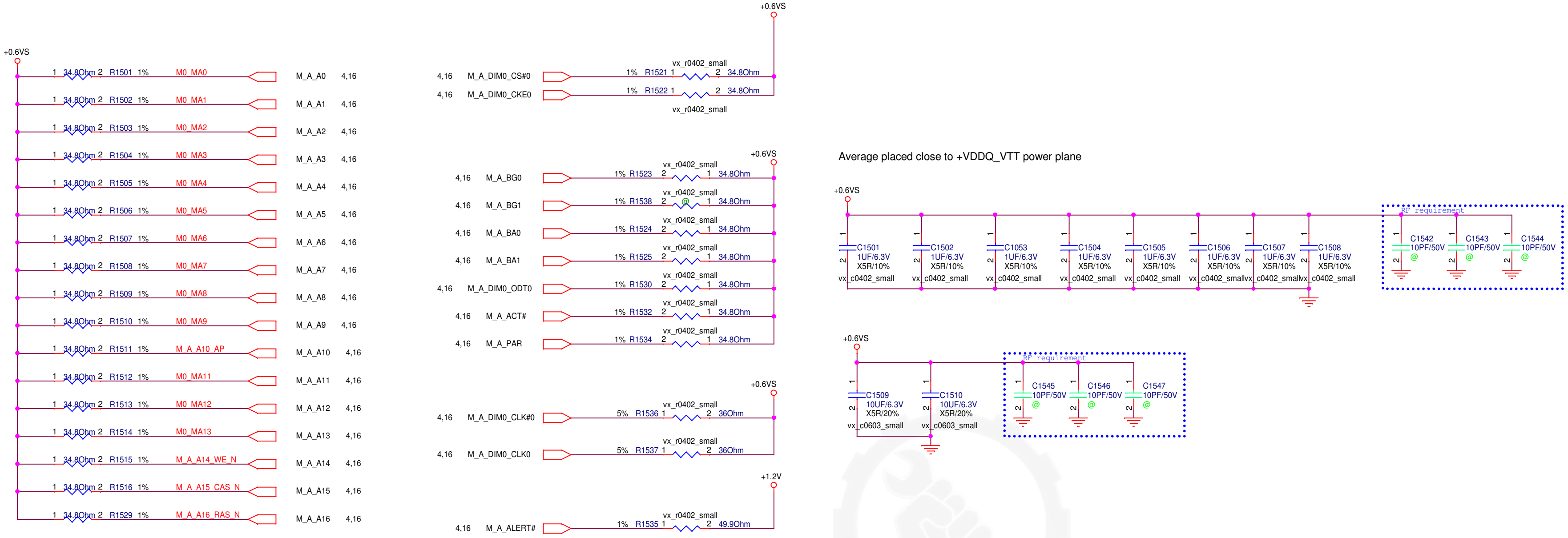
<Title>

Engineer:

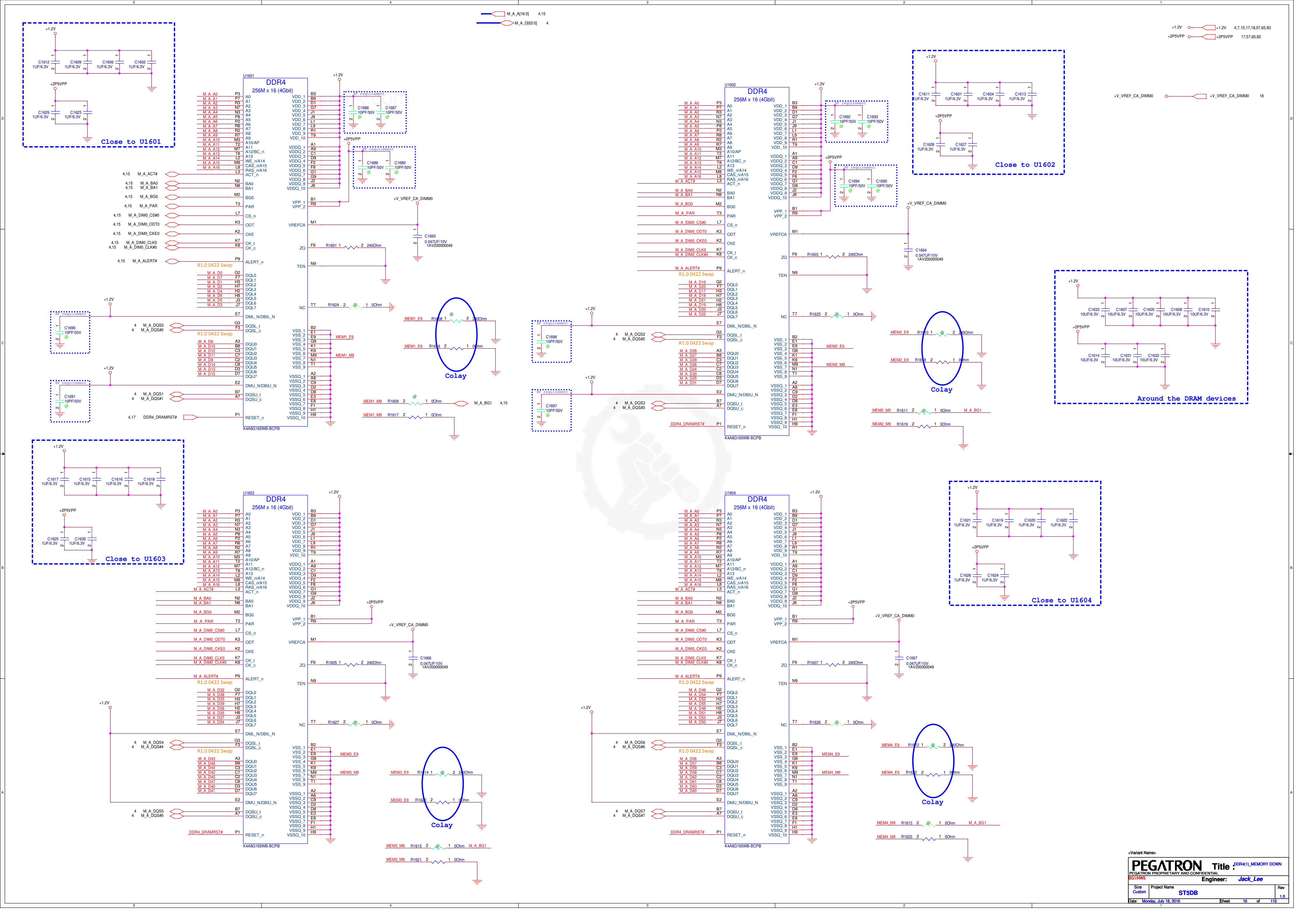
Size C	Project Name STBDP	Rev 1.0
Date: Monday, July 18, 2016	Sheet 14 of 110	

DDR4(0)_Termination

+0.6VS +0.6VS 17,57,83
+1.2V +1.2V 4,7,16,17,18,57,65,83



PEGATRON	Title : DDR4(1)_Termination		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3	Engineer: Jack_Lee		
Size C	Project Name ST5DB		Rev 1.0
Date: Monday, July 18, 2016	Sheet 15 of 110		



M_A_A[16:0]
M_A_D[63:0]
Close to U1601
Close to U1602
Close to U1603
Close to U1604
Around the DRAM devices
DDR4
256M x 16 (4Gbit)
U1601
U1602
U1603
U1604
K4A8G165WB-BCPB
RF requirement
R1.0 0422 Swap
Colay
+1.2V
+2P5VPP
+V_VREF_CA_DIMM0
DDR4_DRAMRST#
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(1)_MEMORY DOWN
Engineer: Jack_Lee
Project Name
ST5DB
Rev
1.0
Date: Monday, July 18, 2016
Sheet 16 of 110

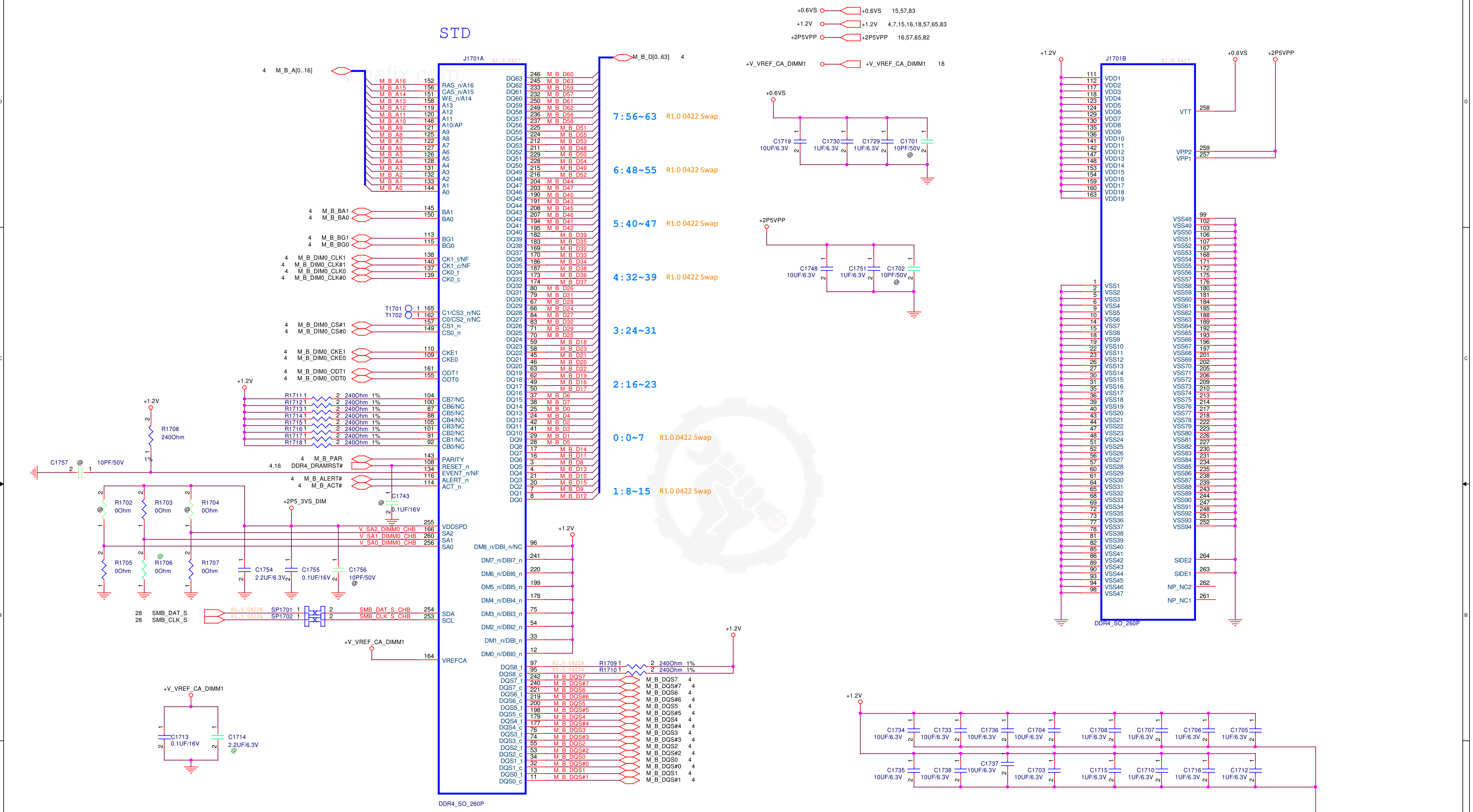
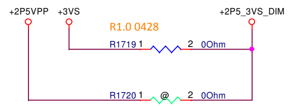


Table 4-52. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0805)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 2.2µF (0402)	

Notes:
1. Total quantity is referring to 2 channels.



<Variant Name>

PEGATRON Title : DDR4(1)_SO-DIMM

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Jack_Lee

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 17 of 110

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off

+1.2V +1.2V 4,7,15,16,17,57,65,83
+V_VREF_CA_DIMM0 +V_VREF_CA_DIMM0 16
+V_VREF_CA_DIMM1 +V_VREF_CA_DIMM1 17

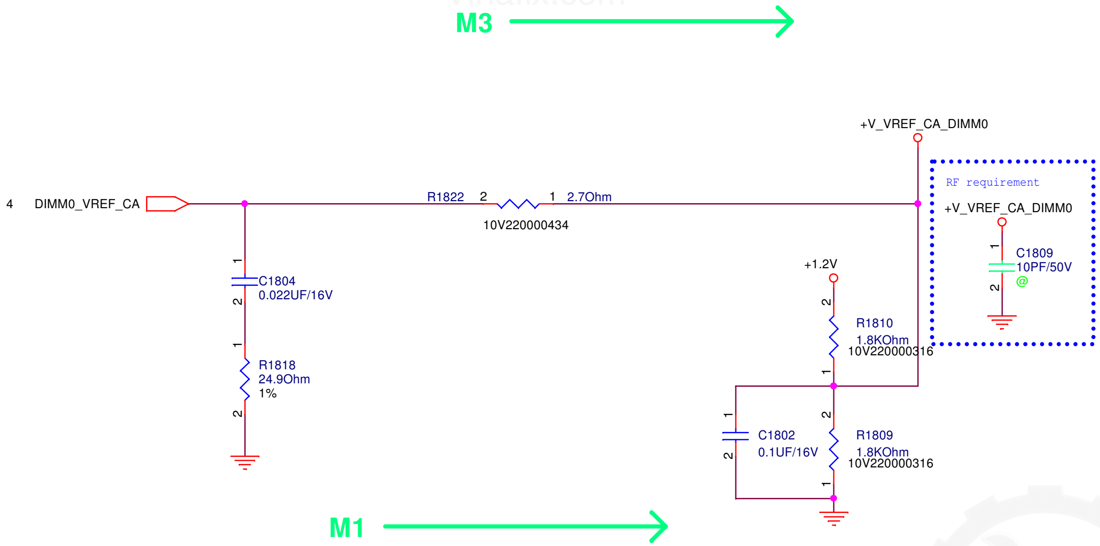
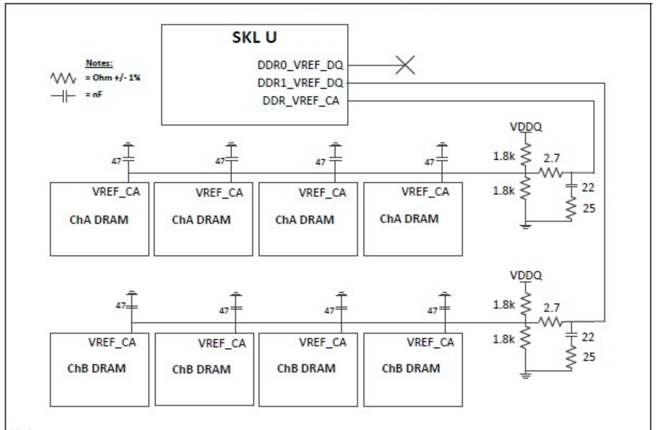


Figure 4-46. SKL U DDR4/-RS x16 Devices Memory Down V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

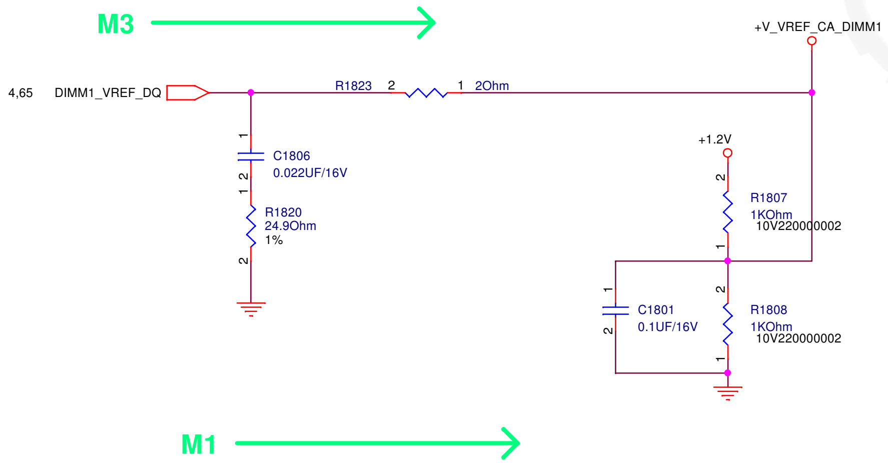
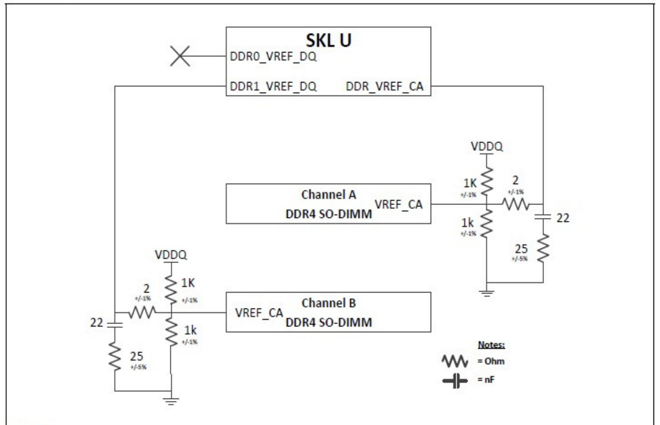
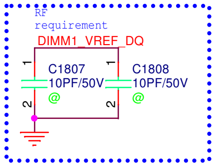


Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.



<Variant Name>

PEGATRON Title : DDR4(3)_CA/DQ Volta

Engineer: Jack_Lee

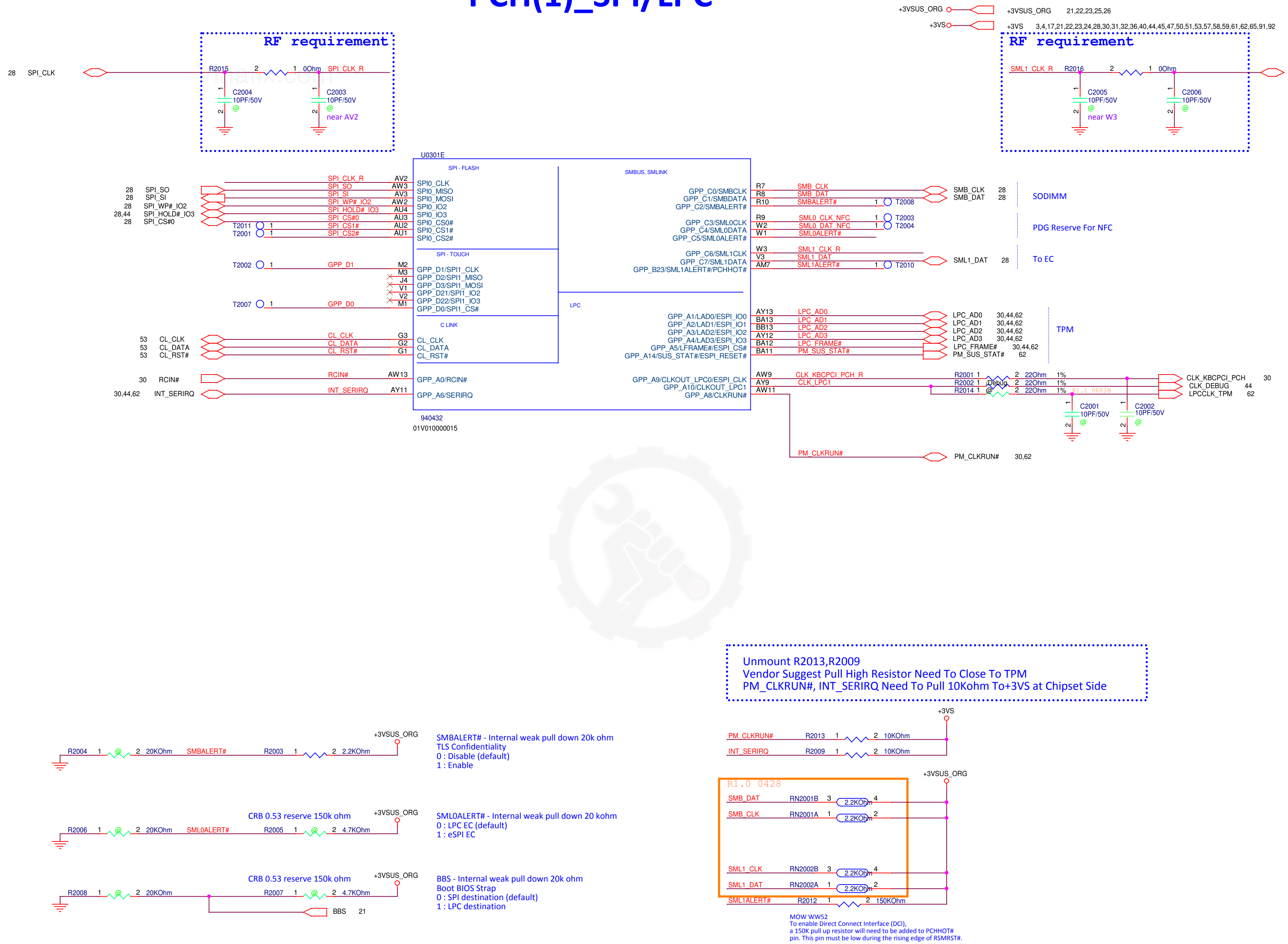
BG1/HW3

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 18 of 110

20

PCH(1)_SPI/LPC



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3

Title : PCH(1)_SPI/LPC

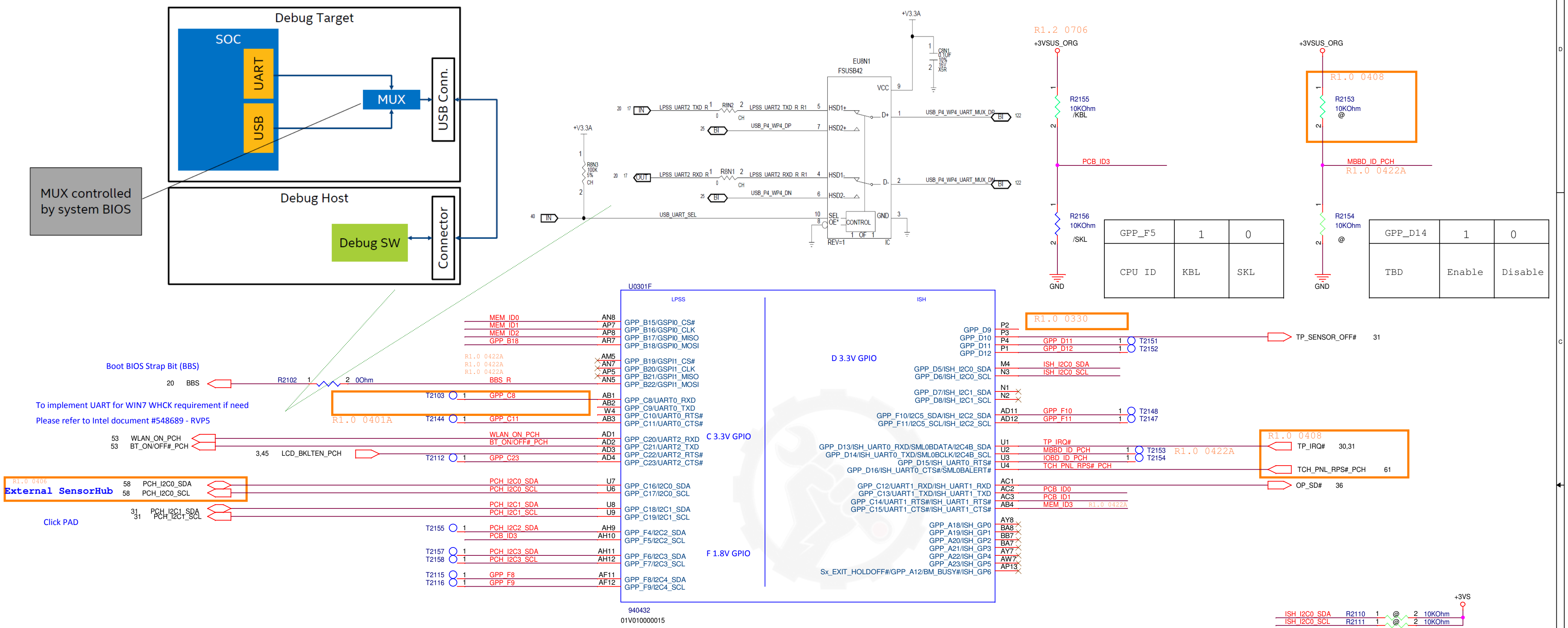
Engineer: Jack_Lee

Size	Project Name	Rev
C	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 20 of 110

Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required



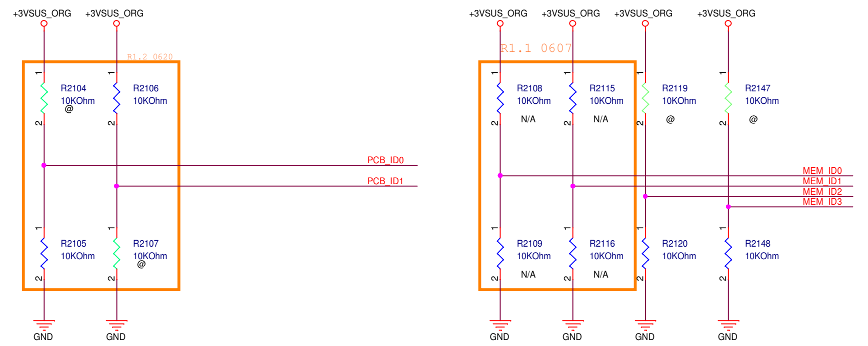
GPP_F5	1	0
CPU ID	KBL	SKL

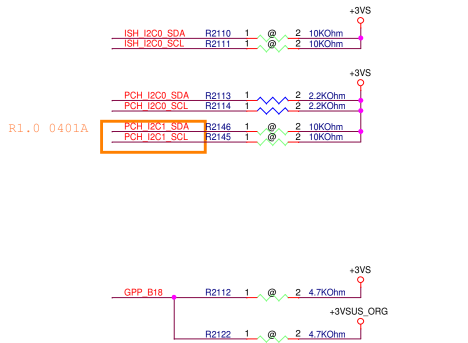
GPP_D14	1	0
TBD	Enable	Disable

Memory ID

	MEM_ID3 (GPP_C15)	MEM_ID2 (GPP_B17)	MEM_ID1 (GPP_B16)	MEM_ID0 (GPP_B15)	PEGA P/N
SAMSUNG K4A8G165WB-BCPB 2133MT 8Gb	0	0	0	0	0315-01HF0PB
SAMSUNG K4A8G165WB-BCRC 2400MT 8Gb	0	0	0	1	0315-01C80PB
MICRON MT40A512M16JY-083E:B 2400MT 8Gb	0	0	1	0	0315-01W90PB
SK HYNIX H5AN8G6NAFR-UHC 2400MT 8Gb	0	0	1	1	0315-01W60PB
	0	1	0	0	Reserved
	0	1	0	1	Reserved
	0	1	1	0	Reserved
	0	1	1	1	Reserved

R1.2 0629



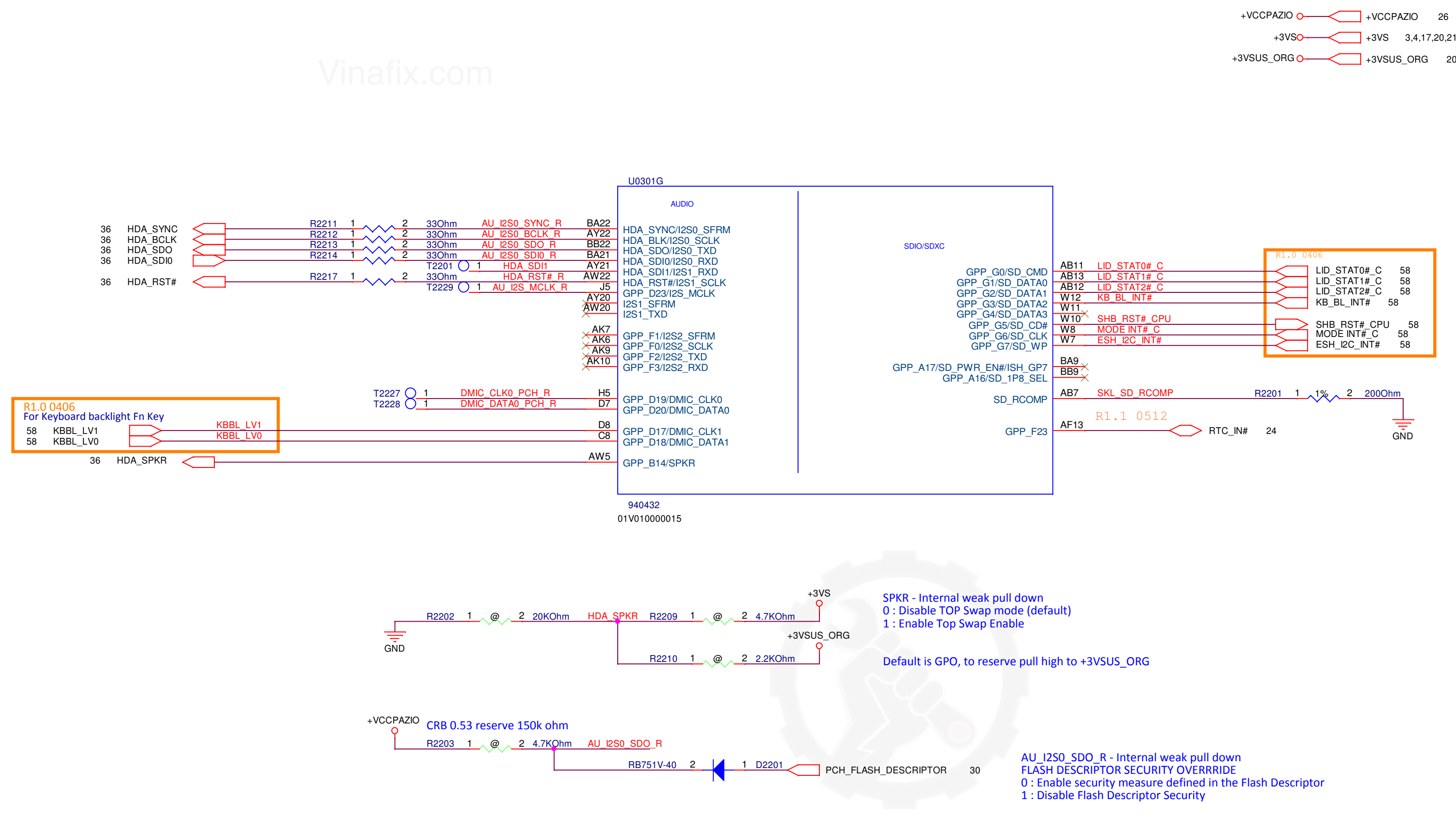


GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

Default is GPO, to reserve pull high to +3VSUS_ORG

MB Version ID

	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R1.0	0	0
R1.1	0	1
R1.2	1	0
R2.0	1	1



<Variant Name>

PEGATRON **Title : PCH(3)_HDA/SDIO**

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 **Engineer:** *Jack_Lee*

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 22 of 110

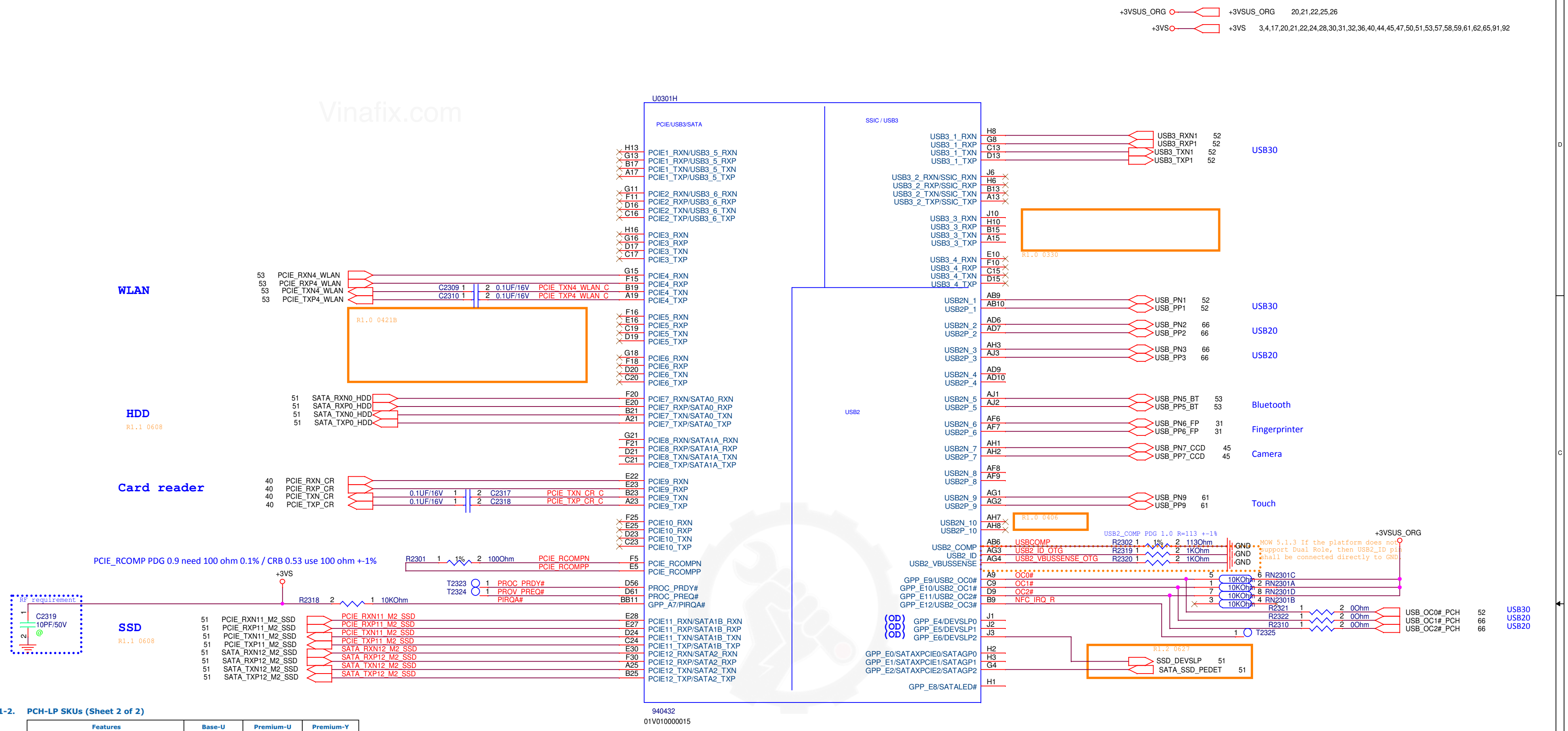


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U

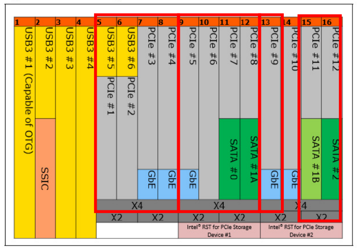
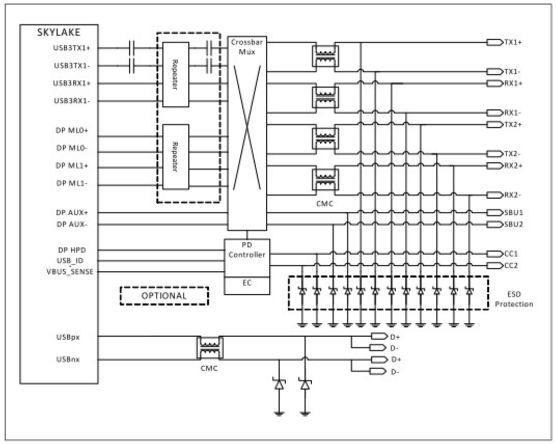


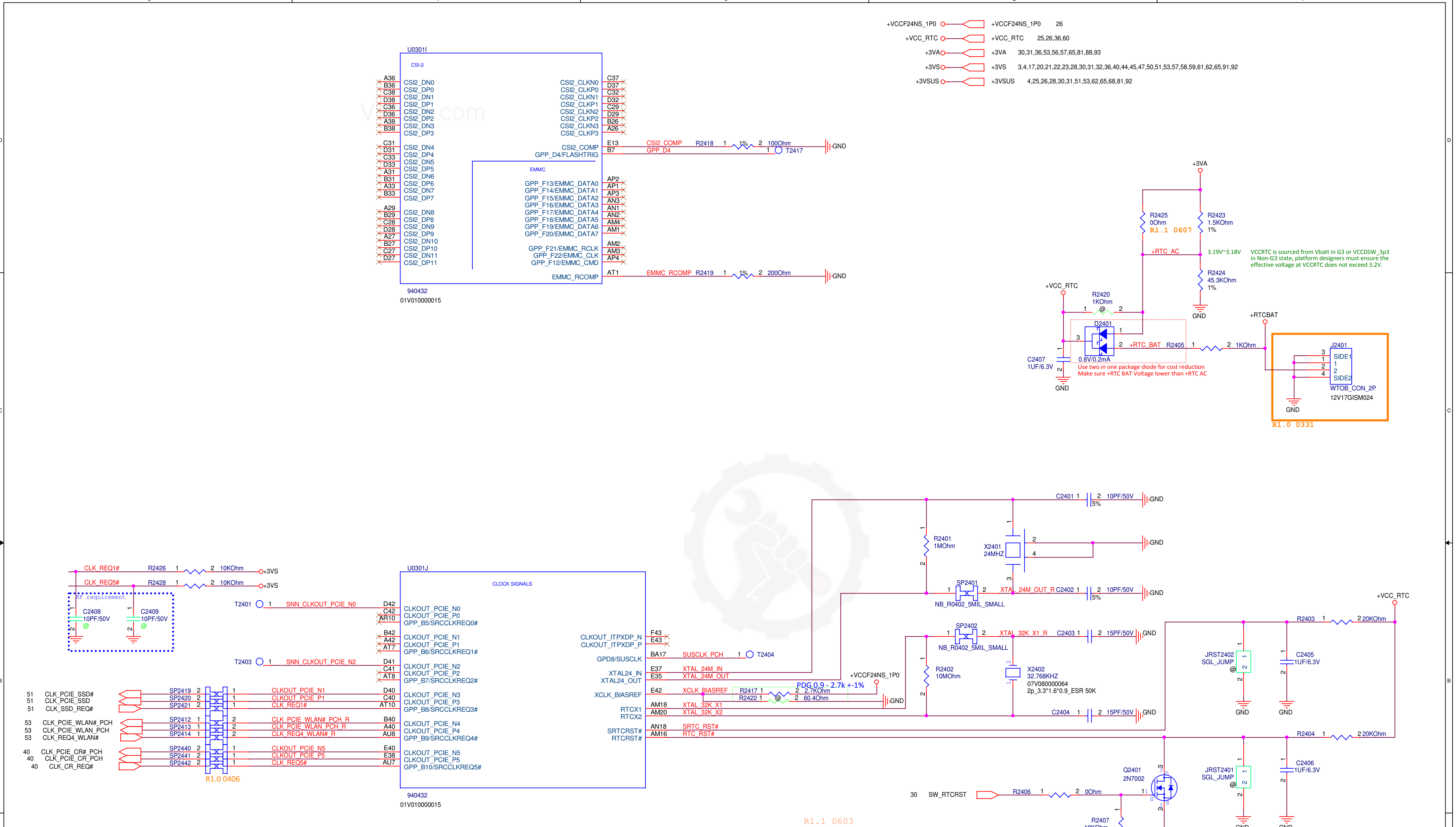
Figure 16-18.USB 3.0 Dual Role and DP x 2



Note: The figure above is a high level example implementation block; actual implementation on schematic may vary.

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: PCH(4)_USB/PCIE/SATA
BG1/HW3
Engineer: Jack_Lee
Size: C | Project Name: ST5DB | Rev: 1.0
Date: Monday, July 18, 2016 | Sheet 23 of 110



SRCCLKREQ#[5:0] (PDG v1.3 Page 835)
Any un-used, disabled, must be left as no connects at the PCH side on the platform.
Any used, enabled, should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail.

CLKOUT_PCIE_P/N[5:0] (PDG v1.3 Page420)
Any differential clock pair not being used must be left as no connect

2015.04.06 YenPin
Add CLOCK Buffer Schematic (CRB Page123)

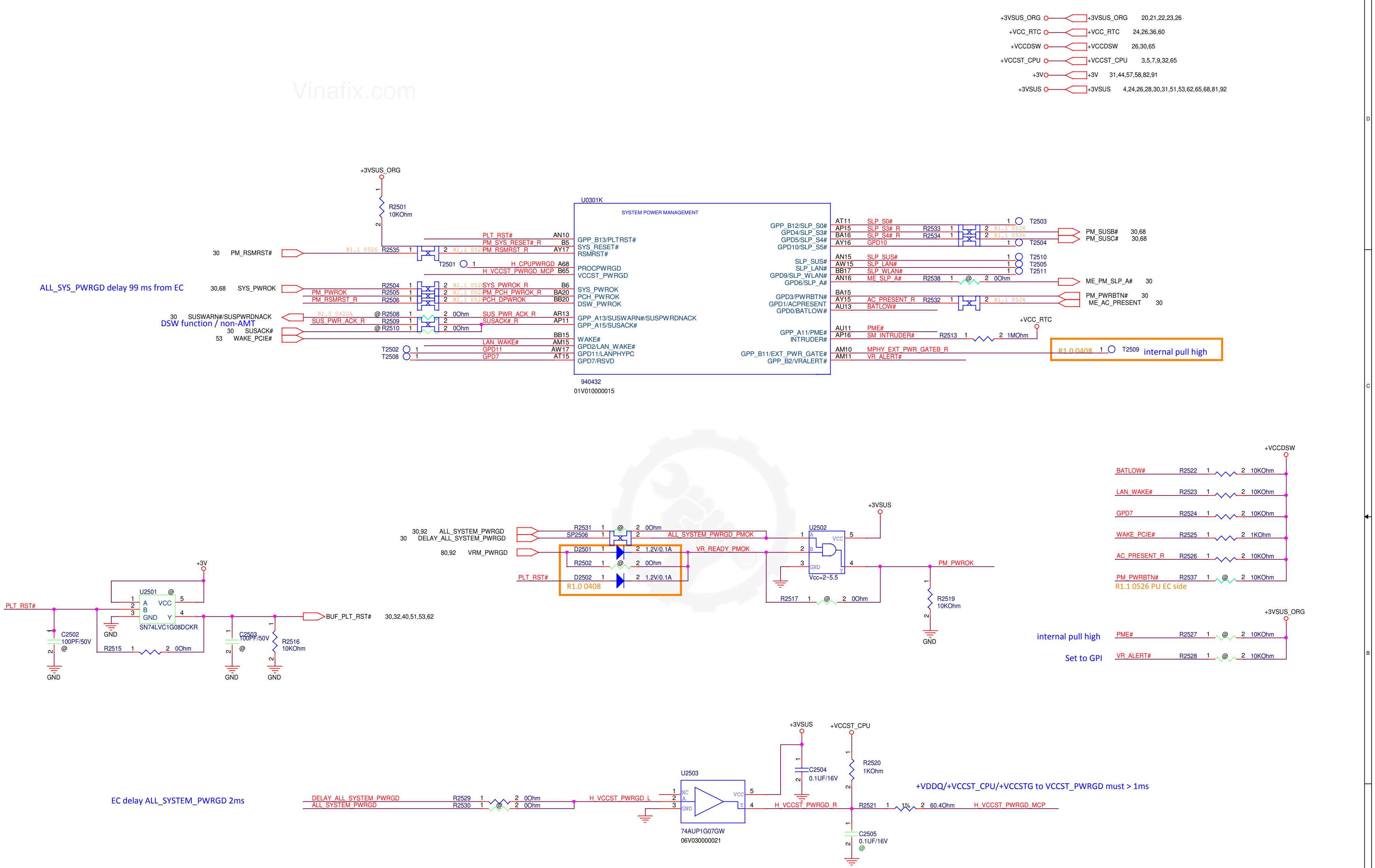
R2426~R2428 Close To U2401

SUSCLK is on the DSW well and is available earlier in the boot sequence.

Remove SUSCLK

<Variant Name>

PEGATRON Title PCH(5)_CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3
Engineer: Jack_Lee
Size C | Project Name ST5DB | Rev 1.0
Date: Monday, July 18, 2016 | Sheet 24 of 110



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title:	PCH(6)_POWER MANAGE	
BG1/HW3	Engineer:	Jack_Lee
Size C	Project Name ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 25	of 110

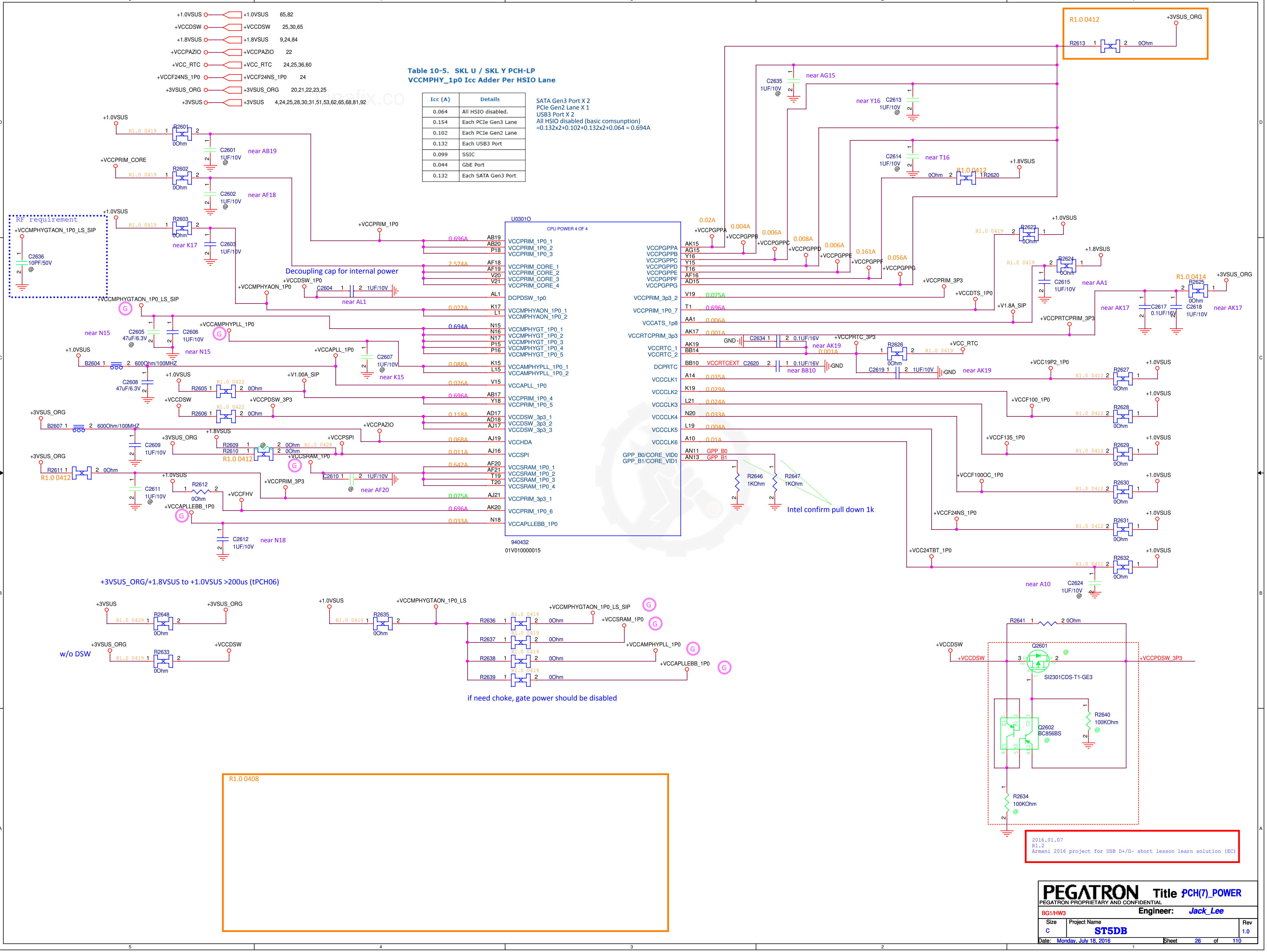


Table 10-5. SKL U / SKL Y PCH-LP VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

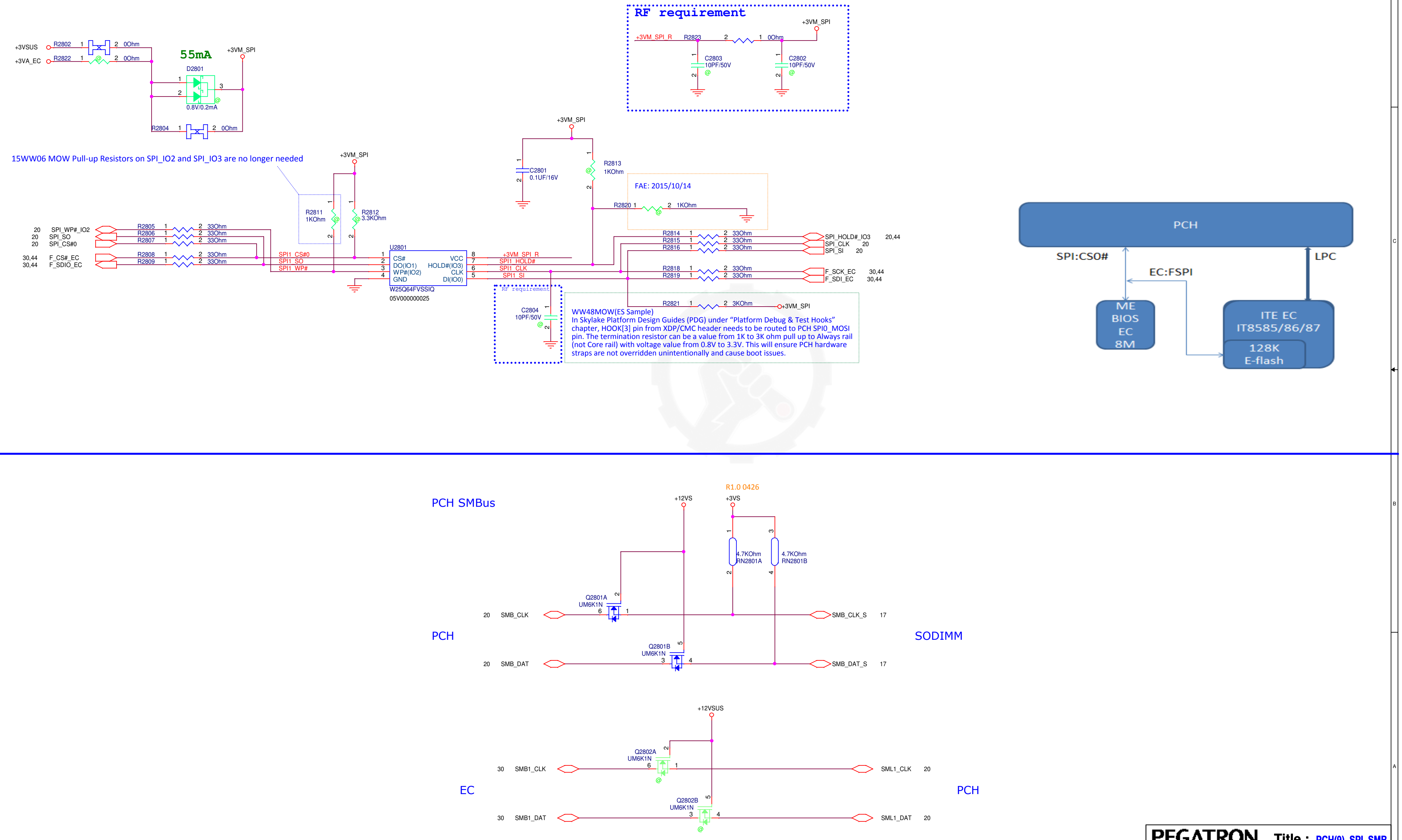
Title: PCH(7)_POWER
Engineer: Jack_Lee
BG1/HW3
Size: C
Project Name: ST5DB
Rev: 1.0
Date: Monday, July 18, 2016
Sheet 26 of 110

<Variant Name>

PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL <Title>	Title :		
	Engineer:		
Size C	STBDP Project Name		Rev 1.0
Date:	Monday, July 18, 2016	Sheet 27 of 110	

PCH(9)_SPI_SMB

+3VS — +3VS 3,4,17,20,21,22,23,24,30,31,32,36,40,44,45,47,50,51,53,57,58,59,61,62,65,91,92
+12VS — +12VS 31,48,57,91
+3VSUS — +3VSUS 4,24,25,26,30,31,51,53,62,65,68,81,92
+3VA_EC — +3VA_EC 30,32,44
+12VSUS — +12VSUS 81,91



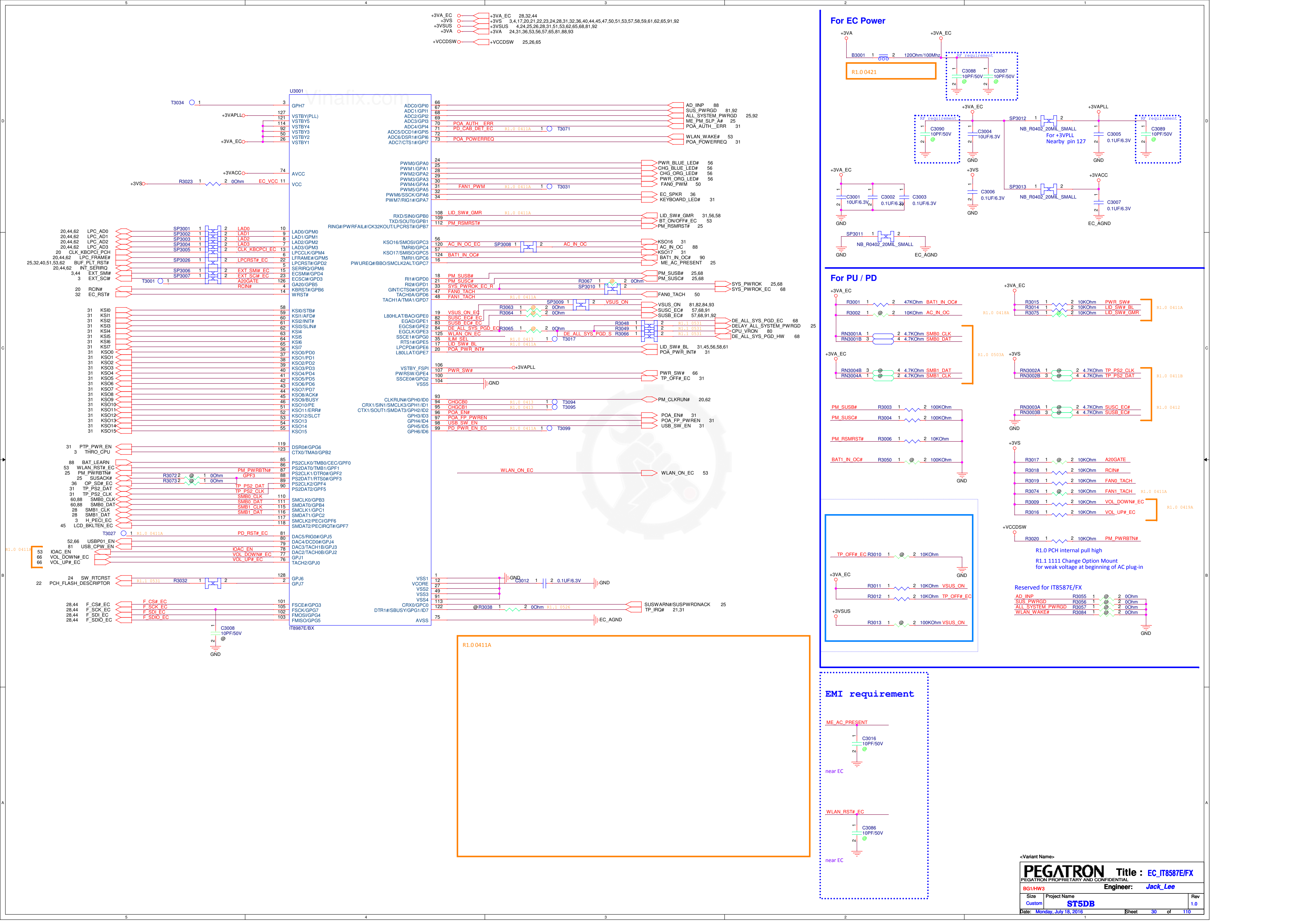
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PCH(9)_SPI_SMB
BG1/HW3
Engineer: Jack_Lee

Size	Project Name	Rev
C	ST5DB	1.0

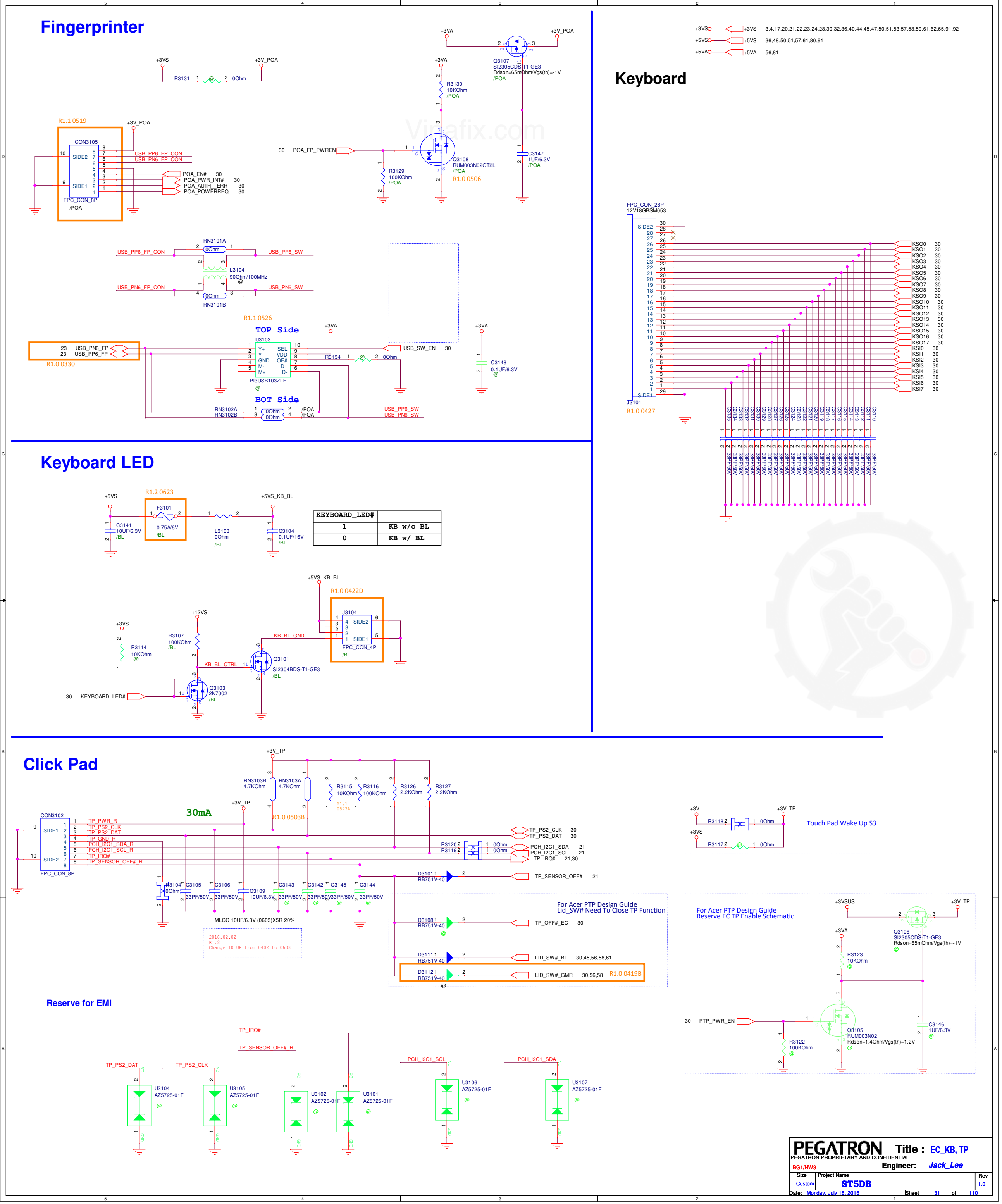
Date: Monday, July 18, 2016 Sheet 28 of 110

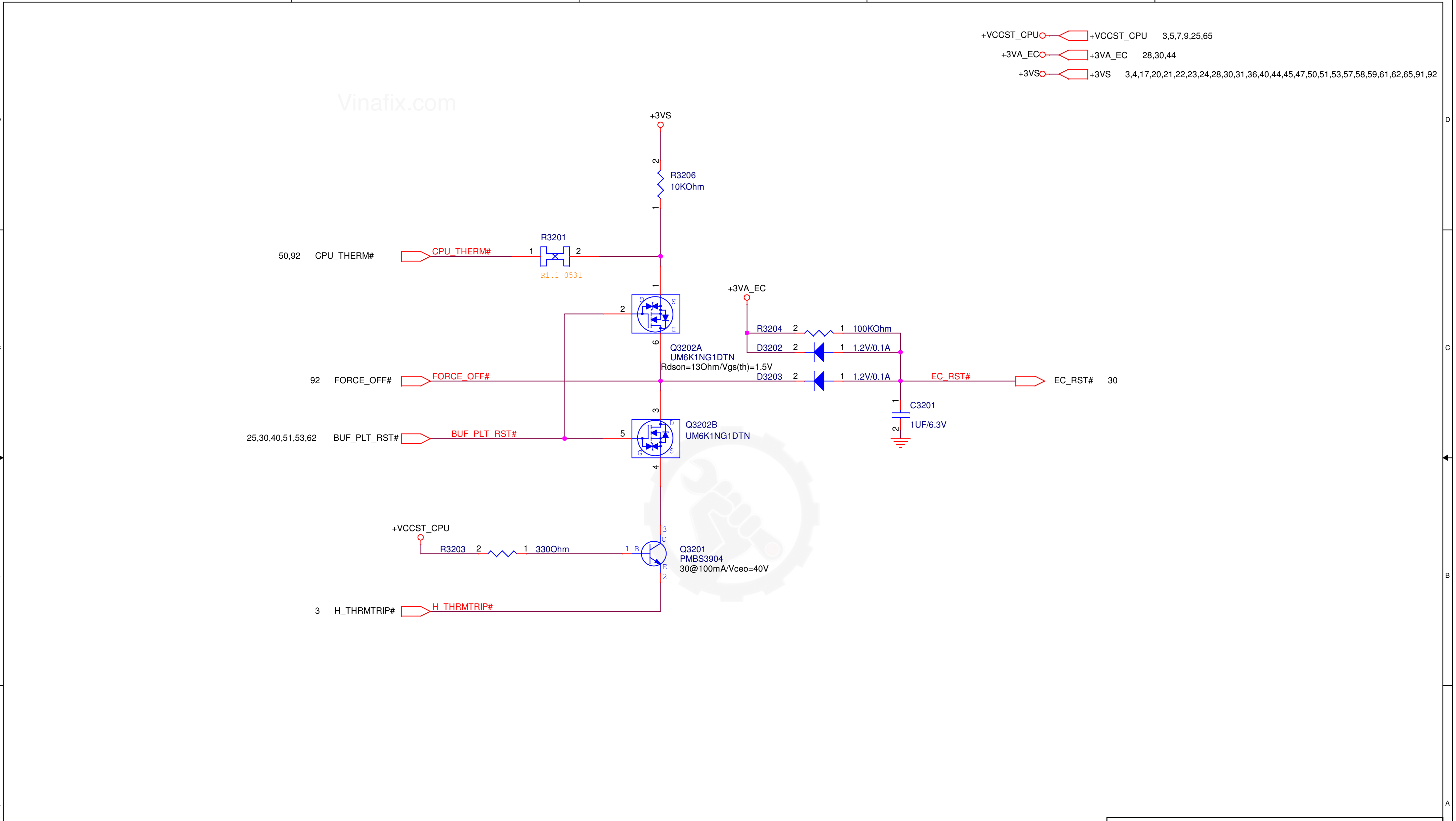
<Variant Name>

PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL	Title :	
<Title>	Engineer:	
Size C	Project Name ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 29 of 110	



U3001
IT8987E/BX
For EC Power
R1.0 0421
RF requirement
NB_R0402_20MIL_SMALL
For +3VPLL
Nearby pin 127
For PU / PD
R1.0 PCH internal pull high
R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in
Reserved for IT8587E/FX
R1.0 0411A
EMI requirement
near EC
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : EC_IT8587E/FX
BG1/HW3
Engineer: Jack_Lee
Size
Custom
Project Name
ST5DB
Rev
1.0
Date: Monday, July 18, 2016
Sheet 30 of 110


Fingerprinter
Keyboard
Keyboard LED
Click Pad
Reserve for EMI
TOP Side
BOT Side
KEYBOARD_LED#
1 KB w/o BL
0 KB w/ BL
30mA
Touch Pad Wake Up S3
For Acer PTP Design Guide
Lid_SW# Need To Close TP Function
For Acer PTP Design Guide
Reserve EC TP Enable Schematic
MLCC 10UF/6.3V (0603)X5R 20%
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : EC_KB, TP
Engineer: Jack_Lee
Size Custom
Project Name ST5DB
Rev 1.0
Date: Monday, July 18, 2016
Sheet 31 of 110



PEGATRON Title : RST_Reset Circuit

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Jack_Lee

Size	Project Name	Rev
B	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 32 of 110

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Title : Realtek RTL8111G

Engineer: Jack_Lee

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 33 of 110

PEGATRON	Title : RJ45		
BG1/HW3	Engineer: Jack_Lee		
Size	Project Name	ST5DB	Rev
Custom	P/N		1.0
Date: Monday, July 18, 2016		Sheet 34 of 110	

<Variant Name>

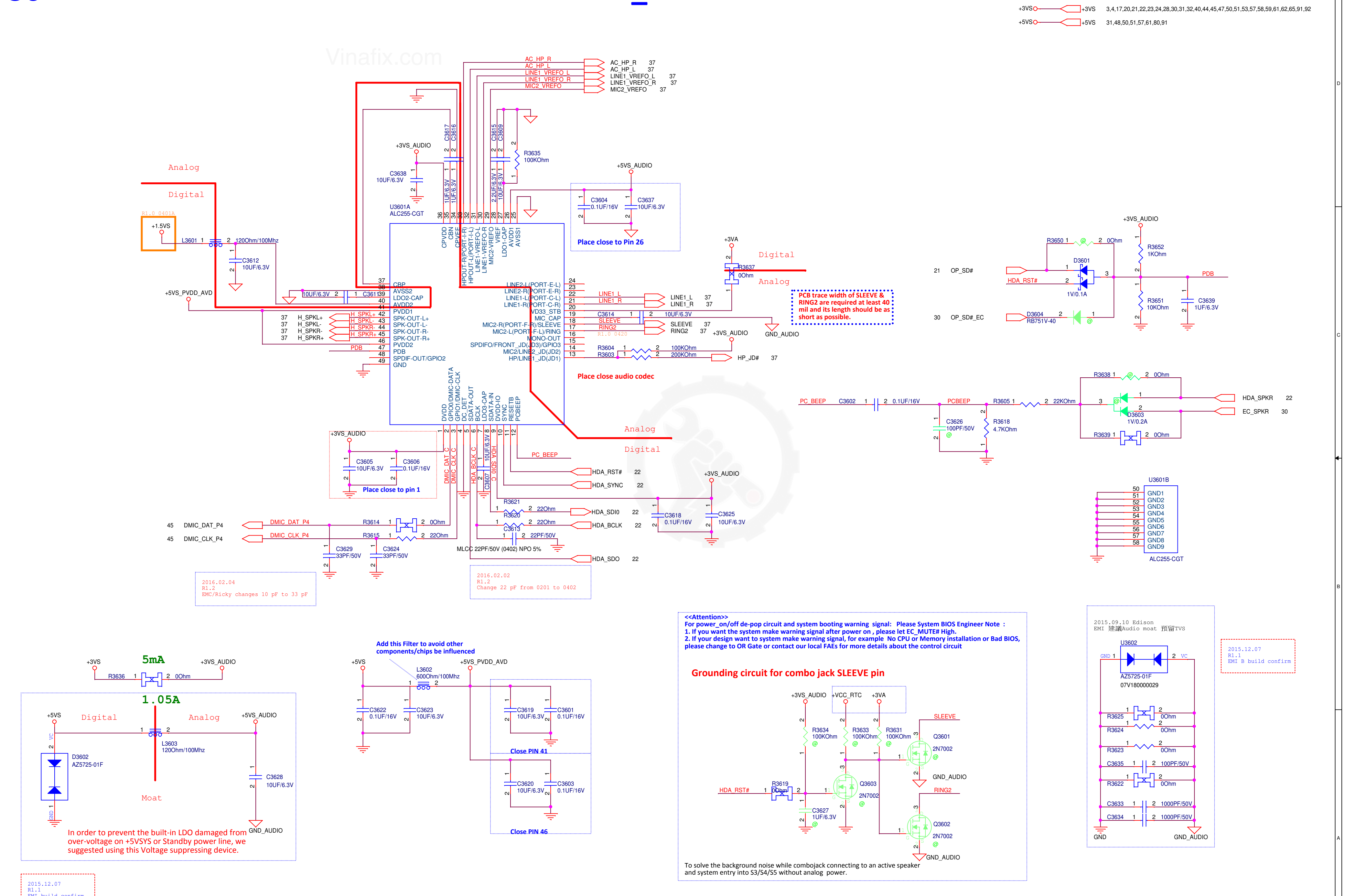
PEGATRON **Title :**

<Title> **Engineer:**

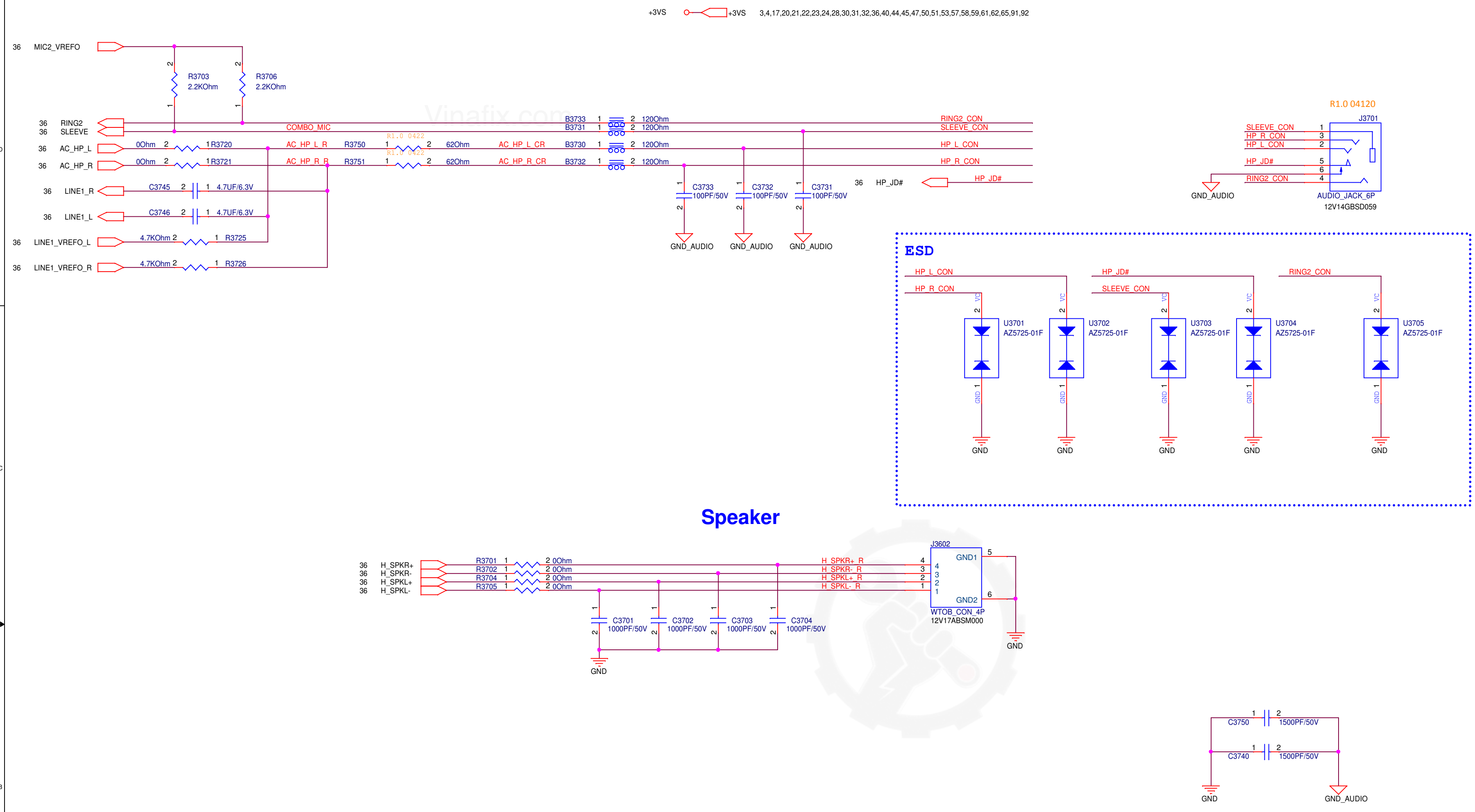
Size	Project Name	ST5DB	Rev
C			1.0

Date: Monday, July 18, 2016 Sheet 35 of 110

AUD_ALC255



PEGATRON	Title : AUD_ALC255
BG1/HW3	Engineer: Jack_Lee
Size C	Project Name ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 36 of 110



<Variant Name>

PEGATRON Title : COMBO_JACK

PEGATRON PROPRIETARY AND CONFIDENTIAL

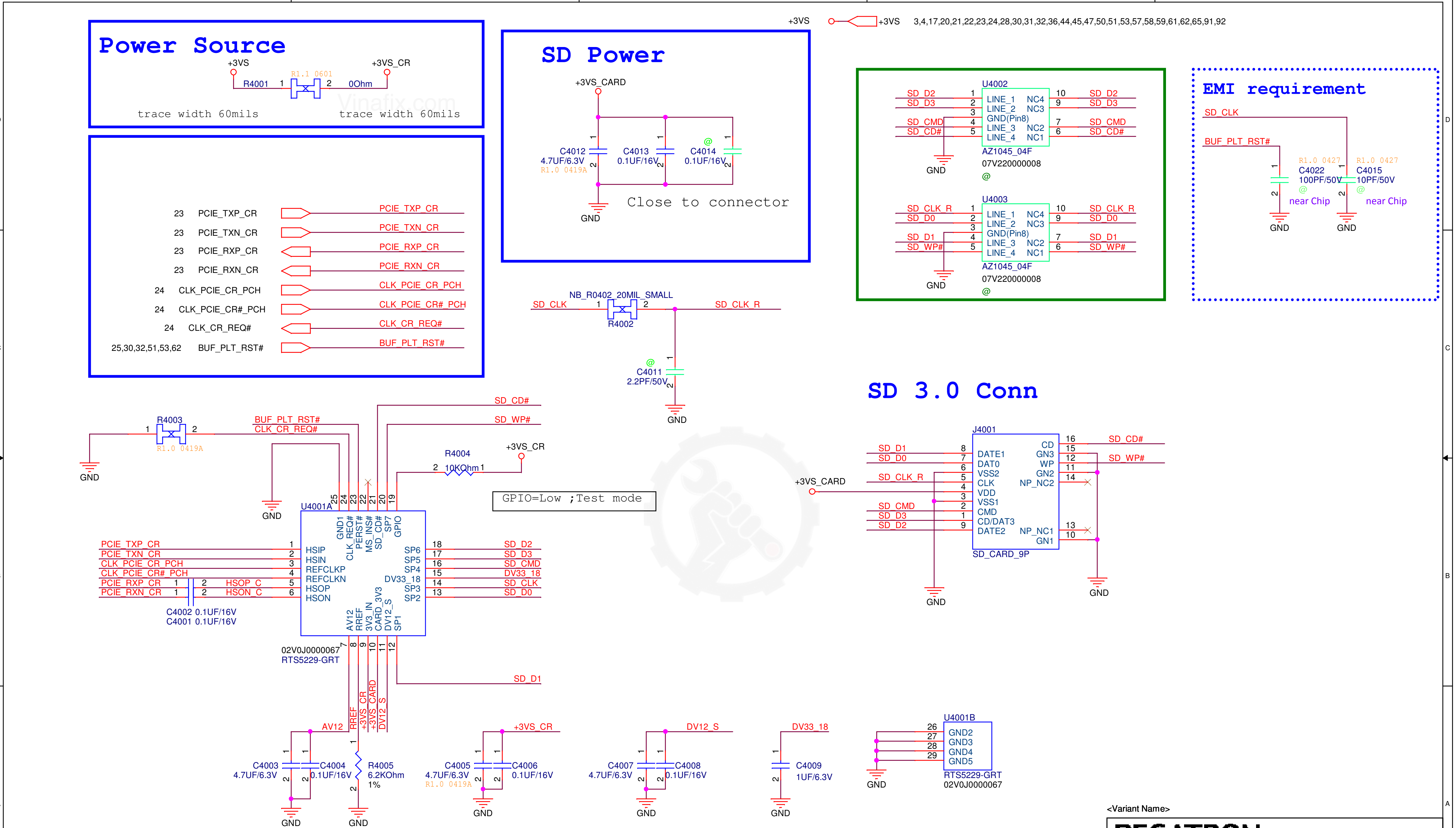
Engineer: Jack_Lee

Size: C | Project Name: ST5DB | Rev: 1.0

Date: Monday, July 18, 2016 | Sheet 37 of 110

<Variant Name>

PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL	Title :	
<Title>	Engineer:	
Size C	Project Name ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 38 of 110	



<Variant Name>

PEGATRON Title : RTS5229

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Jack_Lee

BG1/HW3

Size	Project Name	Rev
B	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 40 of 110

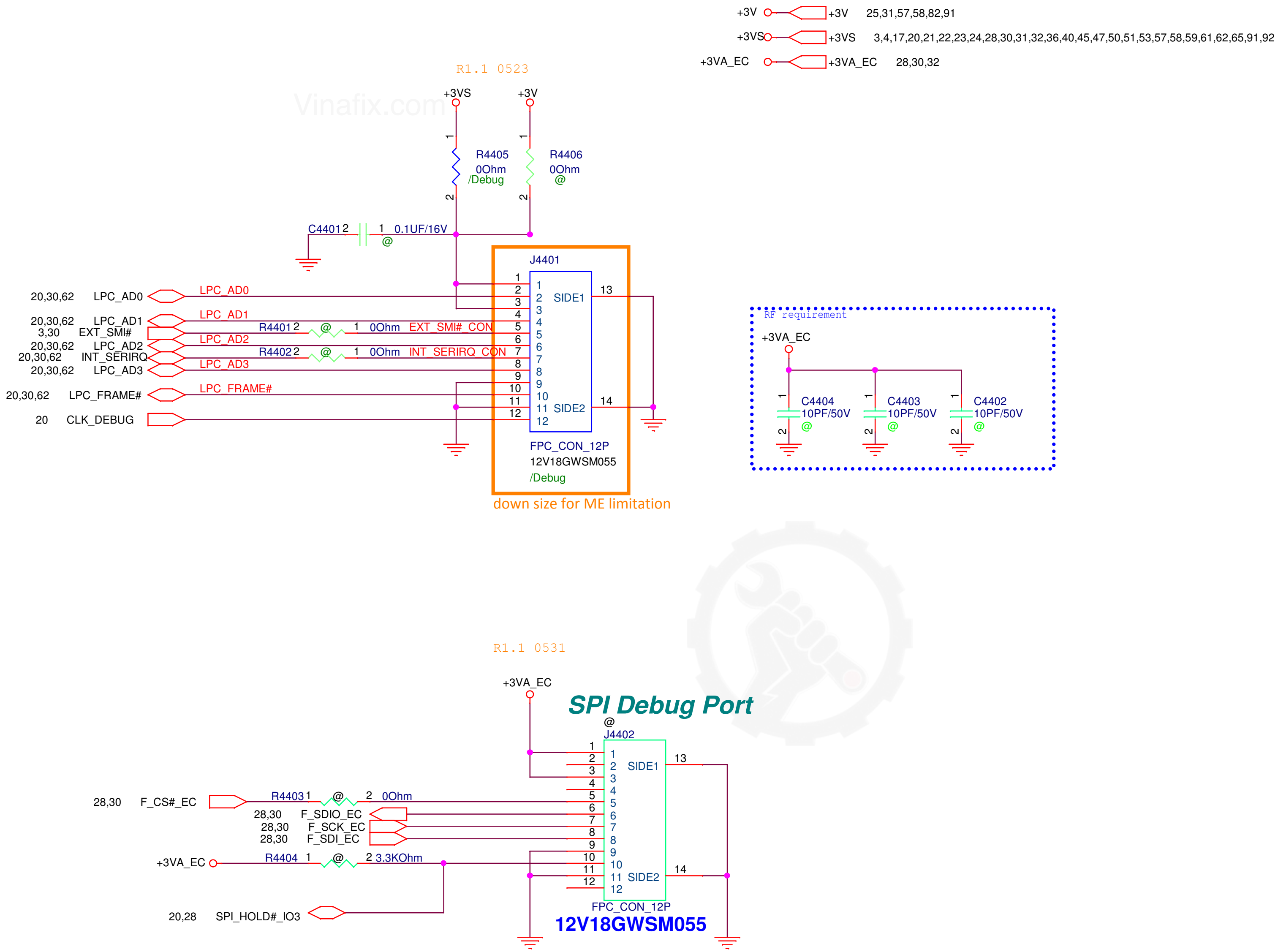
<Variant Name>

PEGATRON **Title :**

<Title> **Engineer:**

Size	Project Name	ST5DB	Rev
C			1.0

Date: Monday, July 18, 2016 Sheet 42 of 110



<Variant Name>

PEGATRON Title : BUG_Debug

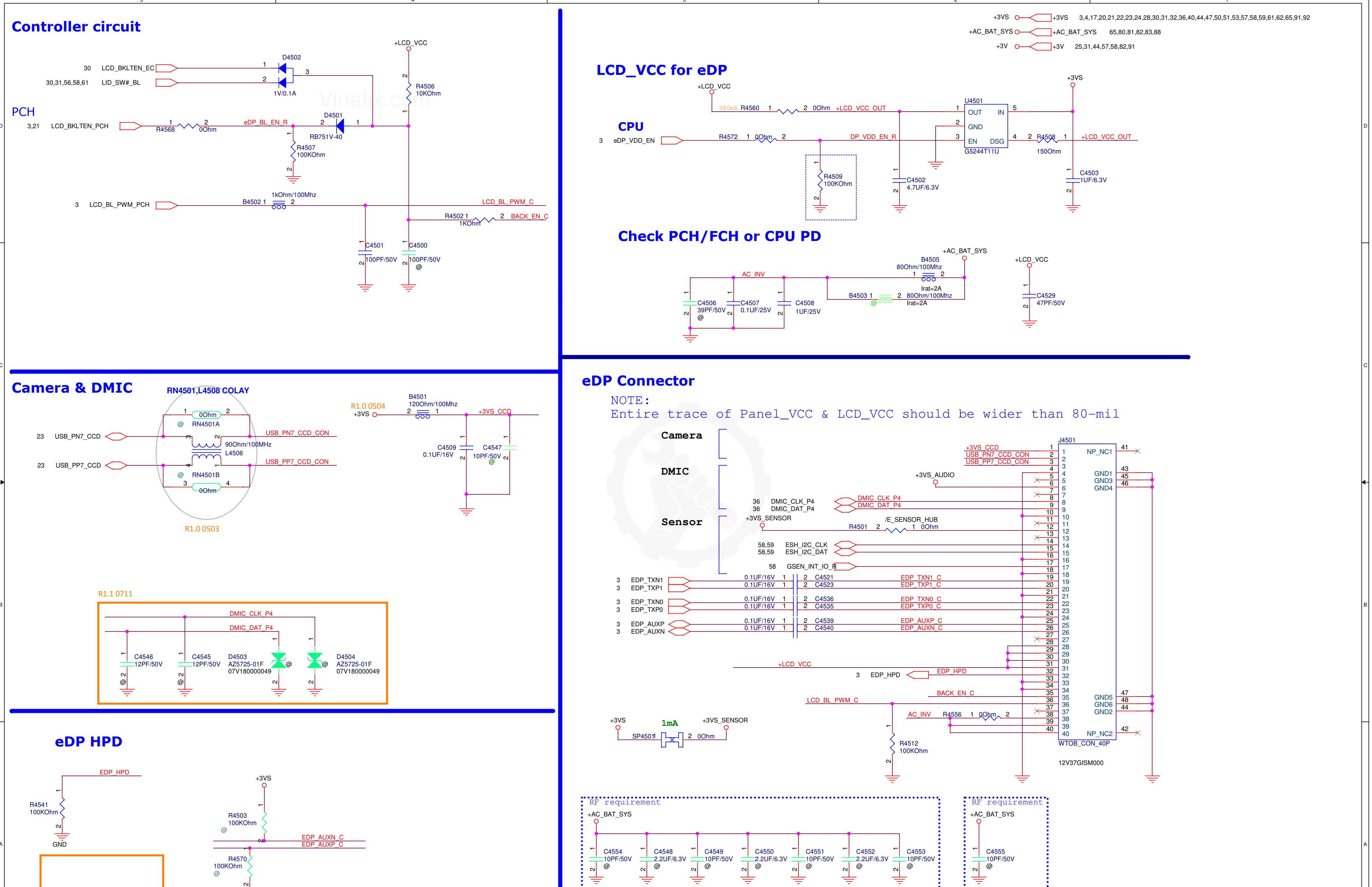
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Jack_Lee*

Size	Project Name	Rev
B		1.0

Date: Monday, July 18, 2016 Sheet 44 of 110



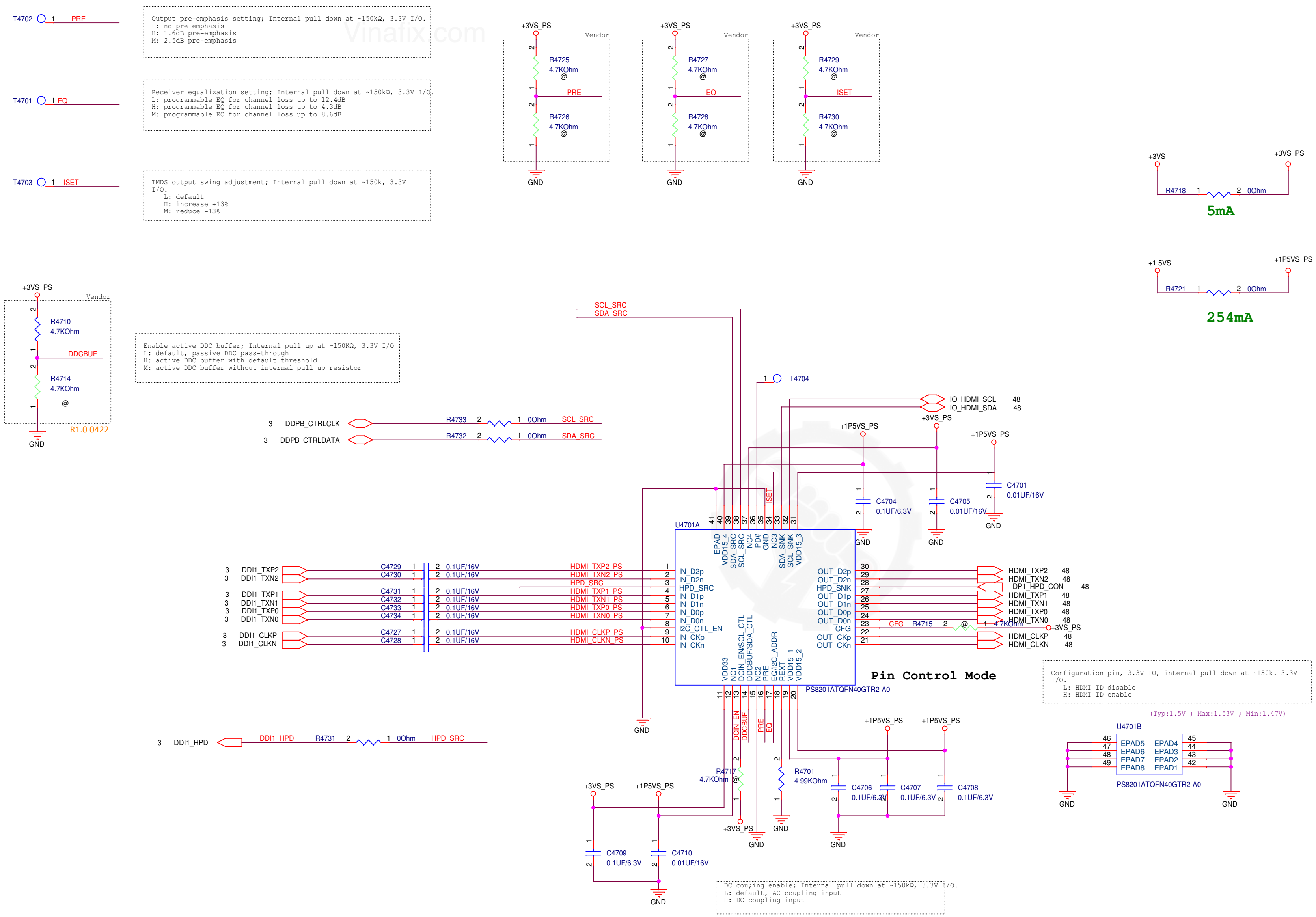
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title :	eDP Out
BG1/HW3	Engineer: Jack_Lee
Size	Custom
Project Name	ST5DB
Rev	1.0
Date:	Monday, July 18, 2016
Sheet	45 of 110

3D CAMERA & USB 3.0 Repeater

<Variant Name>

PEGATRON	3D CAMERA USB30_REPEATER_DMIC X2	Title :
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3	Engineer:	Jack_Lee
Size: Custom	Project Name: ST5DB	Rev: 1.0
Date: Monday, July 18, 2016	Sheet 46	of 110



PEGATRON Title : HDMI-4K2K

PEGATRON PROPRIETARY AND CONFIDENTIAL

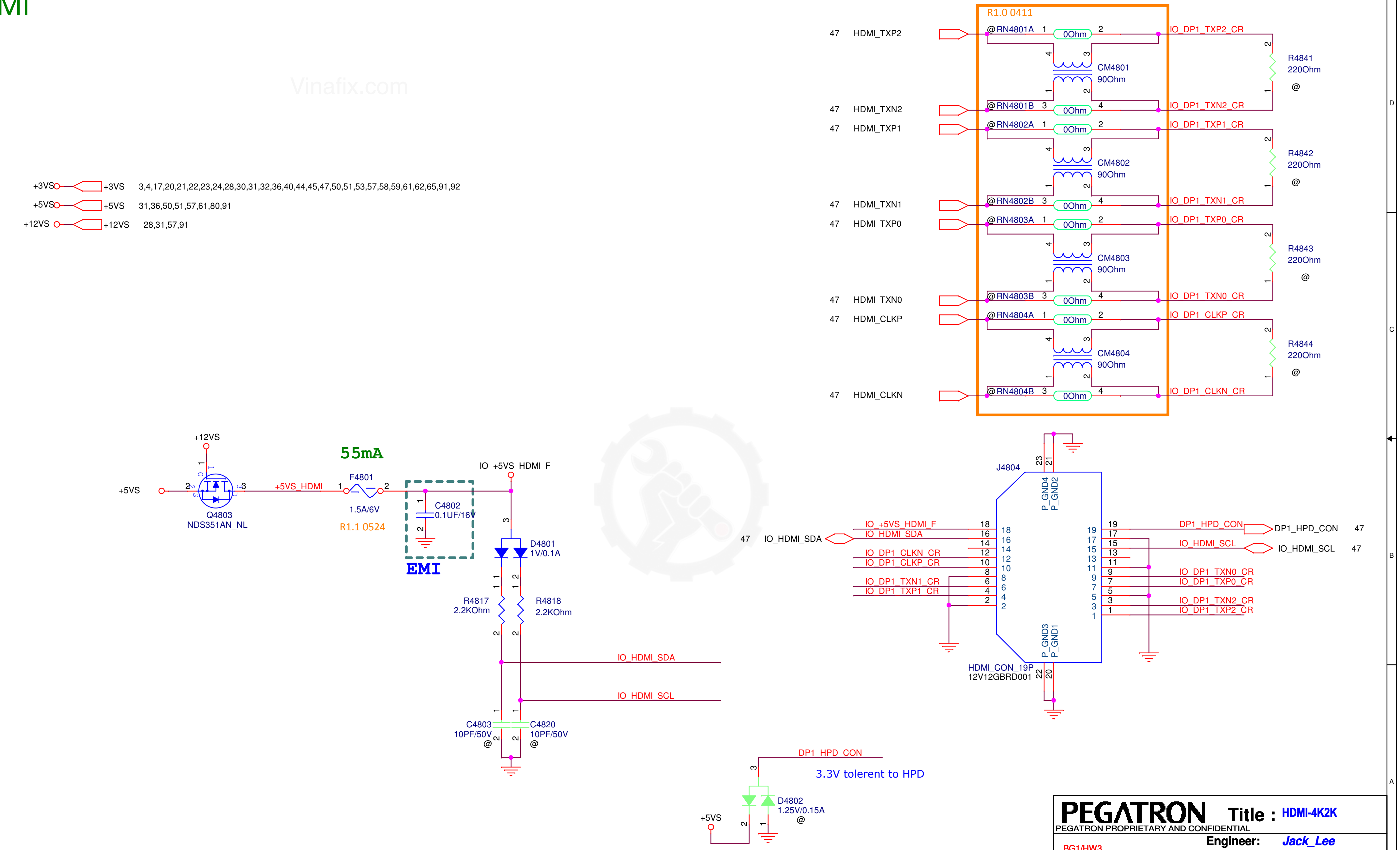
Engineer: Jack_Lee

BG1/HW3

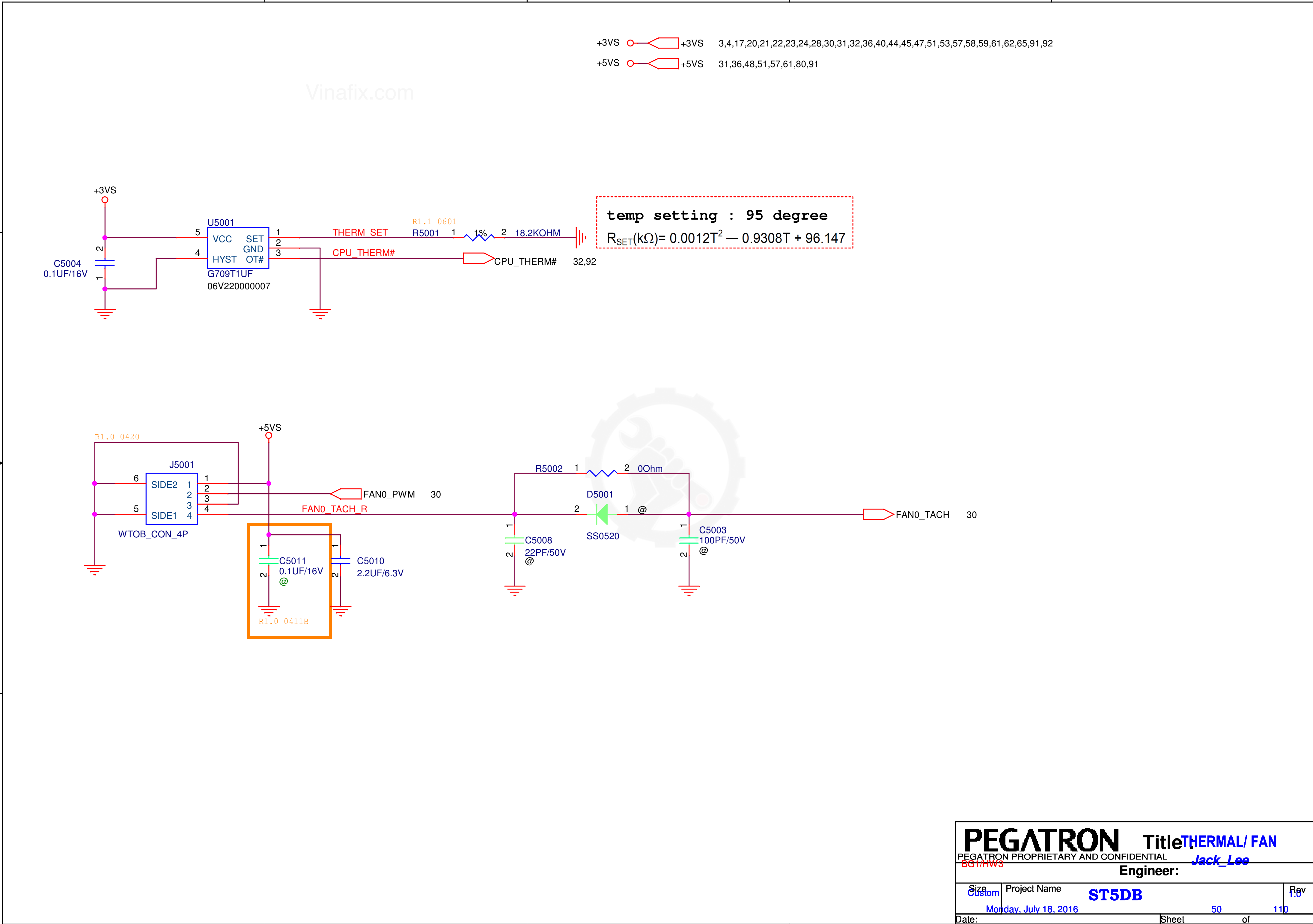
Size	Project Name	Rev
C	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 47 of 110

HDMI

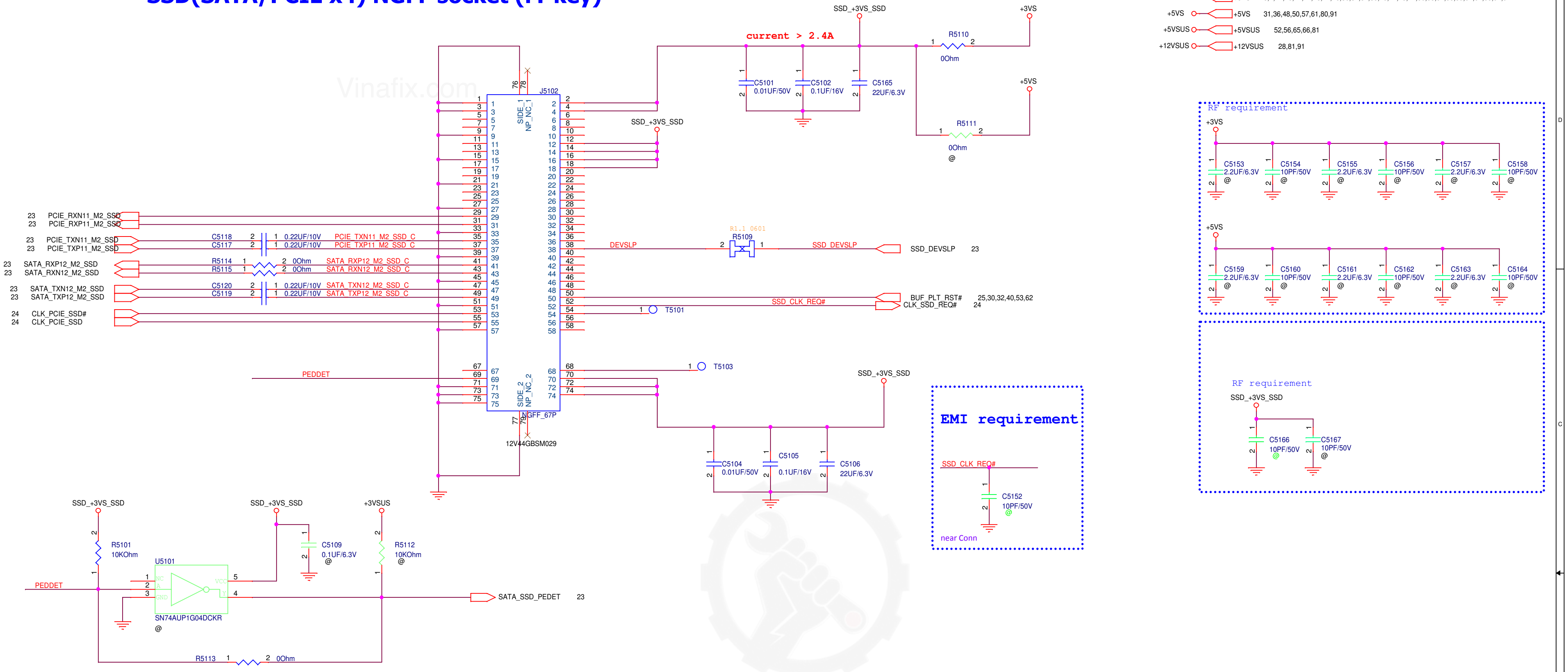


PEGATRON	Title : HDMI-4K2K
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Jack_Lee
BG1/HW3	
Size B	Project Name ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 48 of 110

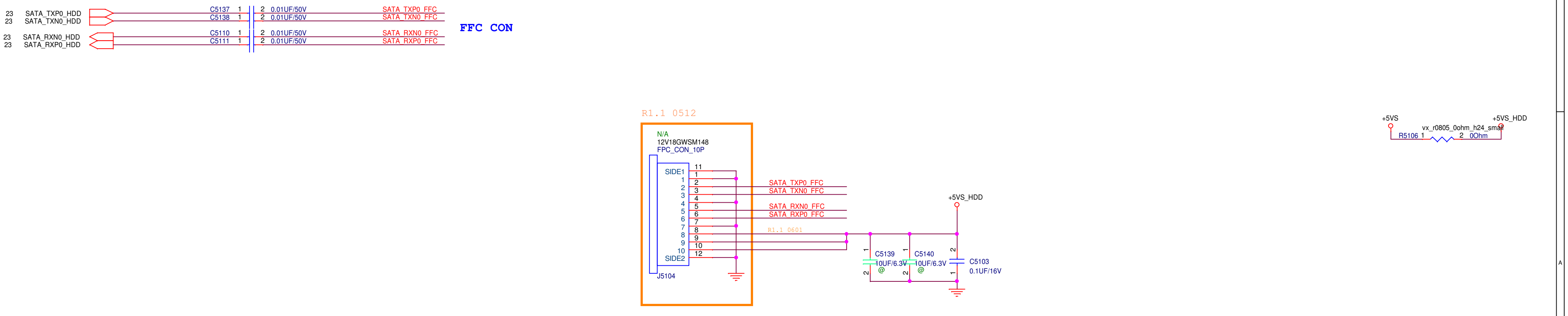


+3VS
+3VS
3,4,17,20,21,22,23,24,28,30,31,32,36,40,44,45,47,51,53,57,58,59,61,62,65,91,92
+5VS
+5VS
31,36,48,51,57,61,80,91
Vinafix.com
temp setting : 95 degree
$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$
+3VS
U5001
VCC
SET
GND
HYST
OT#
G709T1UF
06V220000007
C5004
0.1UF/16V
THERM_SET
CPU_THERM#
R1.1 0601
R5001
1%
18.2KOHM
CPU_THERM#
32,92
+5VS
R1.0 0420
J5001
SIDE2
SIDE1
WTOB_CON_4P
FAN0_PWM
30
FAN0_TACH_R
C5011
0.1UF/16V
@
C5010
2.2UF/6.3V
R1.0 0411B
R5002
0Ohm
D5001
SS0520
@
C5008
22PF/50V
@
C5003
100PF/50V
@
FAN0_TACH
30
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3
Title: THERMAL/ FAN
Engineer: Jack_Lee
Size
Custom
Project Name
ST5DB
Rev
1.0
Date: Monday, July 18, 2016
Sheet 50 of 110

SSD(SATA/PCIE x4) NGFF socket (M-key)



HDD Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : SATA HDD/ ODD

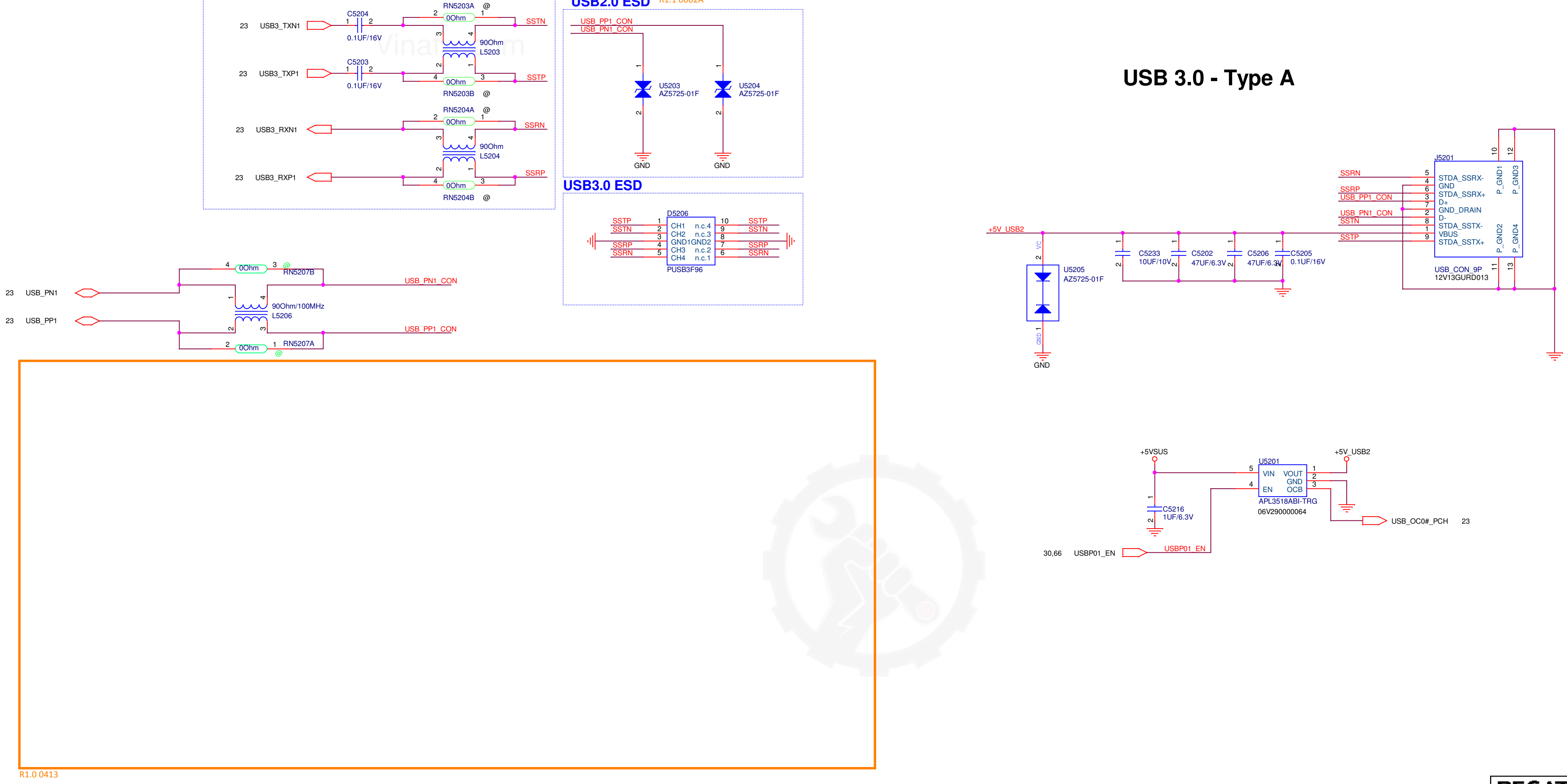
Engineer: Jay2 Liu

Size	Project Name	Rev
C	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 51 of 110

USB 3.0

USB3.0 Choke



PEGATRON Title : USB JACK

PEGATRON PROPRIETARY AND CONFIDENTIAL

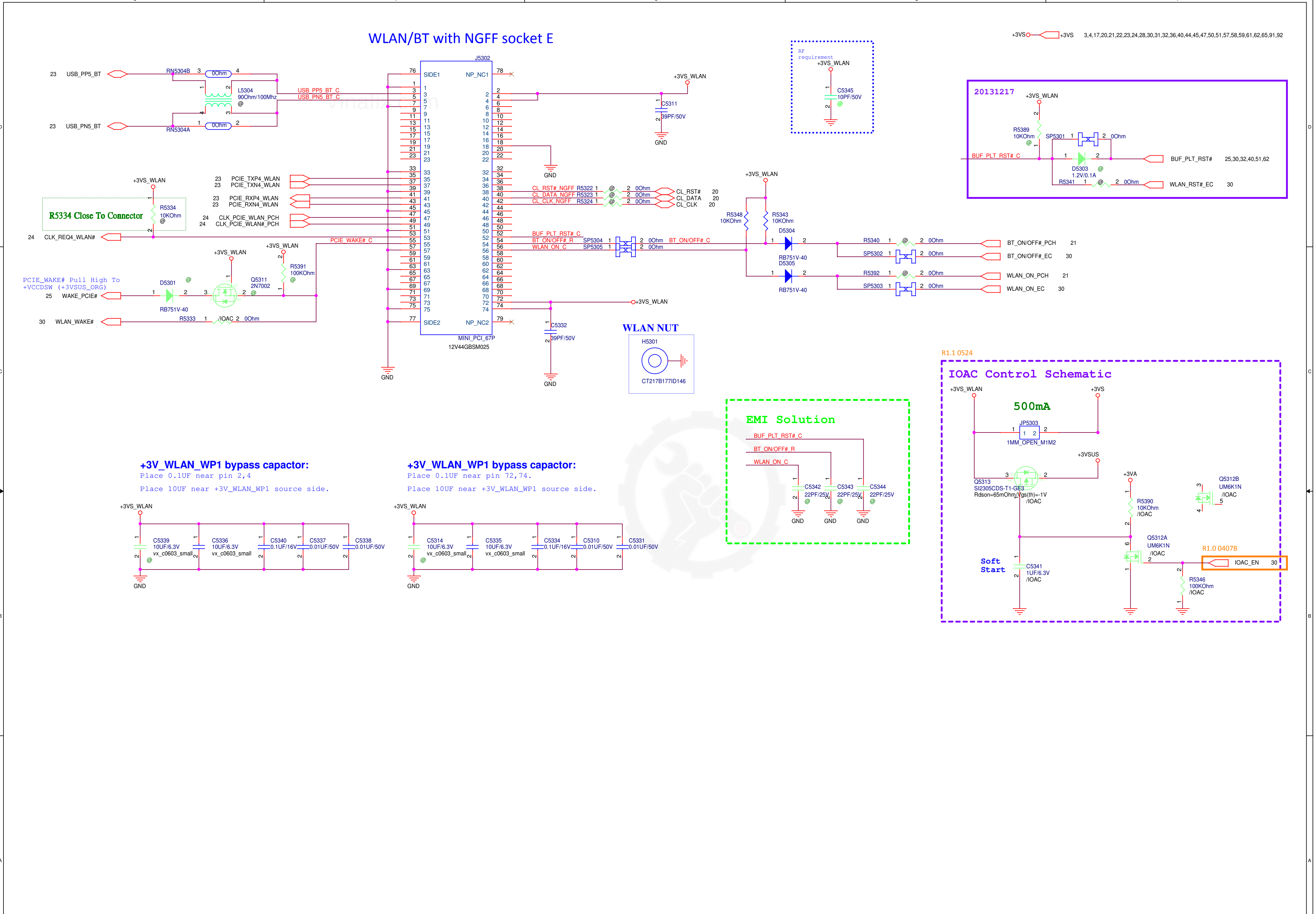
Engineer: Jack_Lee

BG1/HW3

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 52 of 110

WLAN/BT with NGFF socket E



PEGATRON	Title :	WLAN	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
	Engineer:	Jack_Lee	
BG1/HW3			
Size C	Project Name	ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 53	of 110	

5	4	3	2	1

D

C

B

A

PEGATRON Title : <Title>

BG1/HW3 Engineer: Jack_Lee

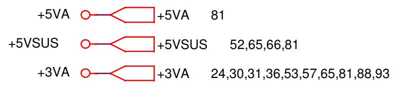
Size	Project Name	Rev
A	ST5DB	1.0

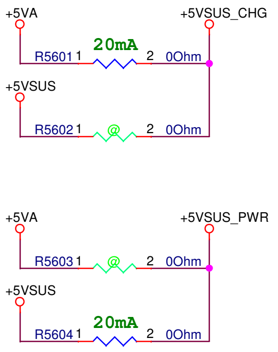
Date: Monday, July 18, 2016 Sheet 54 of 110

5	4	3	2	1

PEGATRON Title : <Title>
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3	Engineer: Jack_Lee	
Size A	Project Name ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 55 of 110	

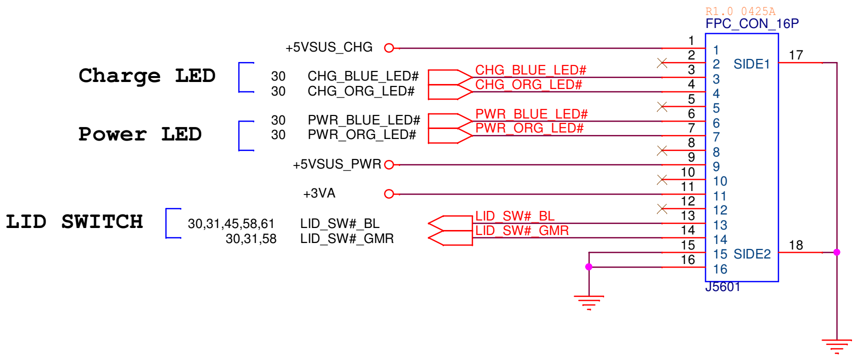




MB Connector Pin Define

	ST5DB
1	+5VSUS_CHG
2	NC
3	CHG_BLUE_LED#
4	CHG_ORG_LED#
5	NC
6	PWR_BLUE_LED#
7	PWR_ORG_LED#
8	NC
9	+5VSUS_PWR
10	NC
11	+3VA
12	NC
13	LID_SW#_BL
14	LID_SW#_GMR
15	GND
16	GND

LED Board Conn



PEGATRON

BG1/HW3

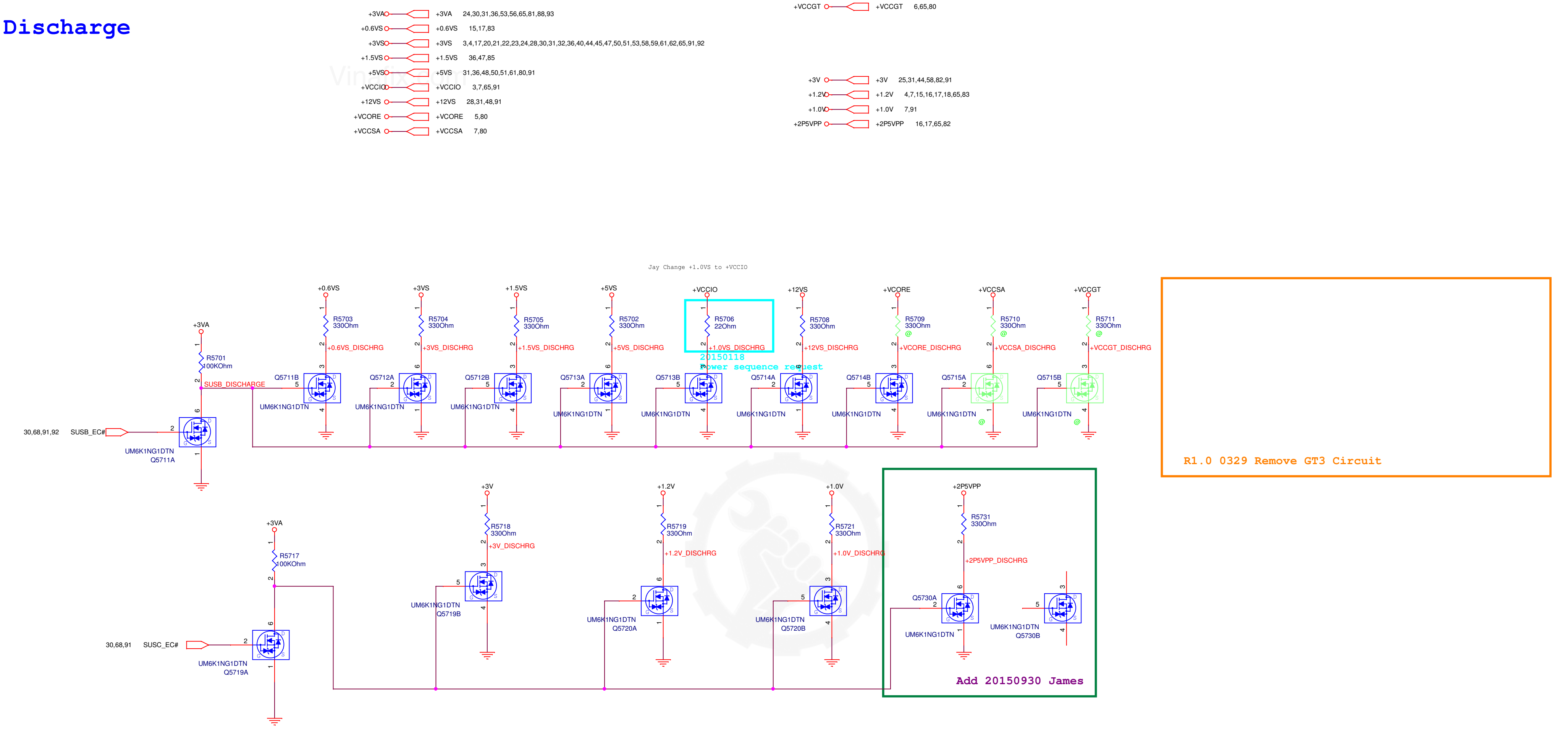
Title : LED

Engineer: Jack_Lee

Size	Project Name	Rev
B	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 56 of 110

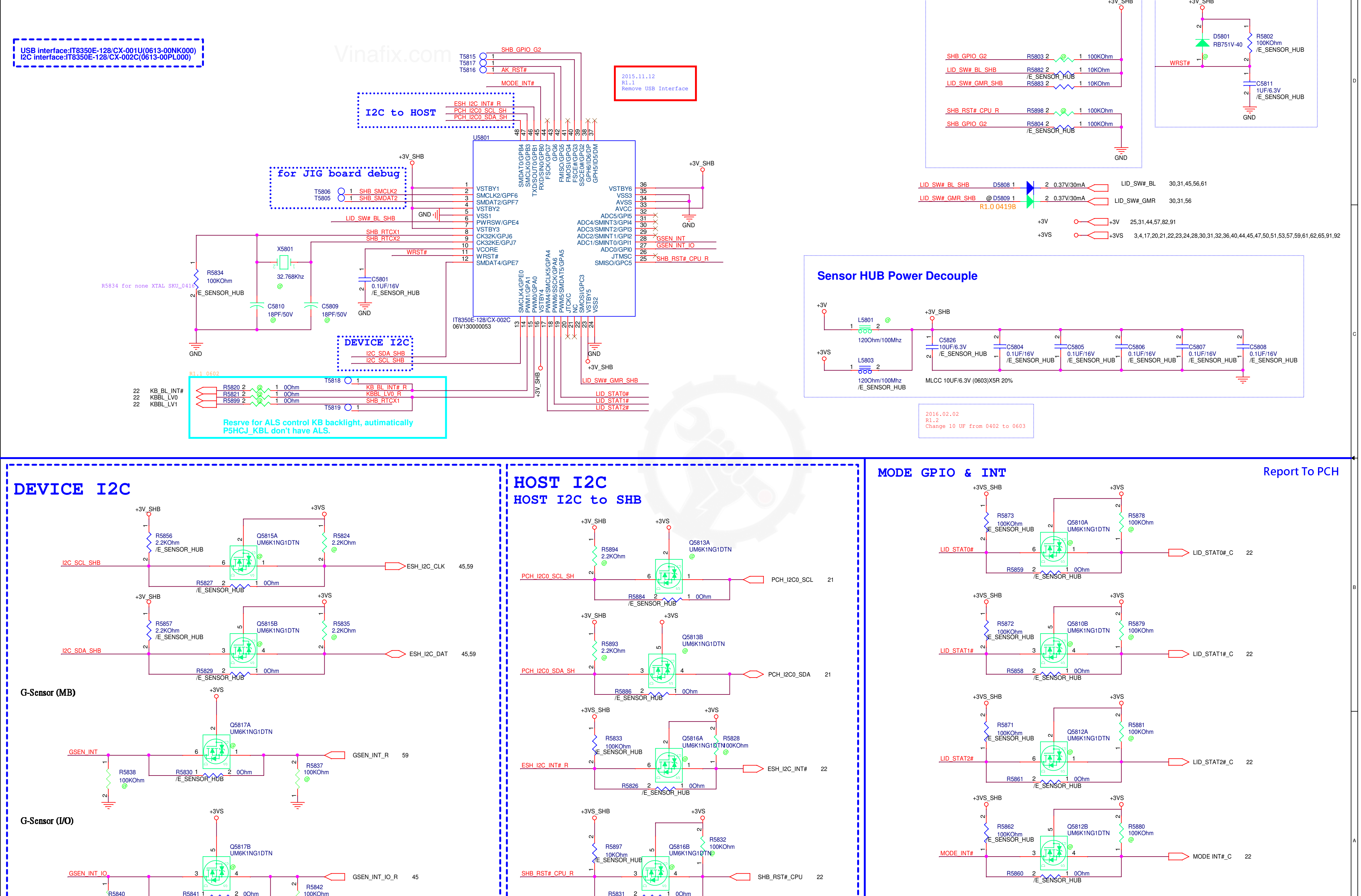
Discharge



PEGATRON	Title DSG_Discharge
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Jack_Lee
Size Custom	Project Name ST5DB, Rev 1.0
Date: Monday, July 18, 2016	Sheet 57 of 110

58

Sensor Hub



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3

Title : Sensor Hub

Engineer: Jack_Lee

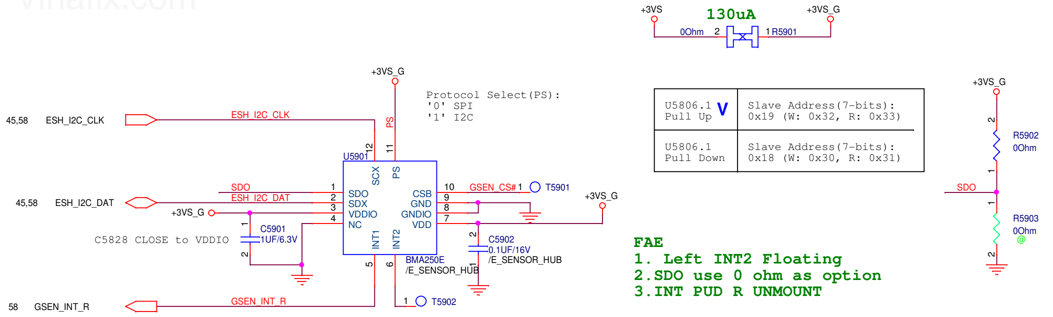
Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 58 of 110

59

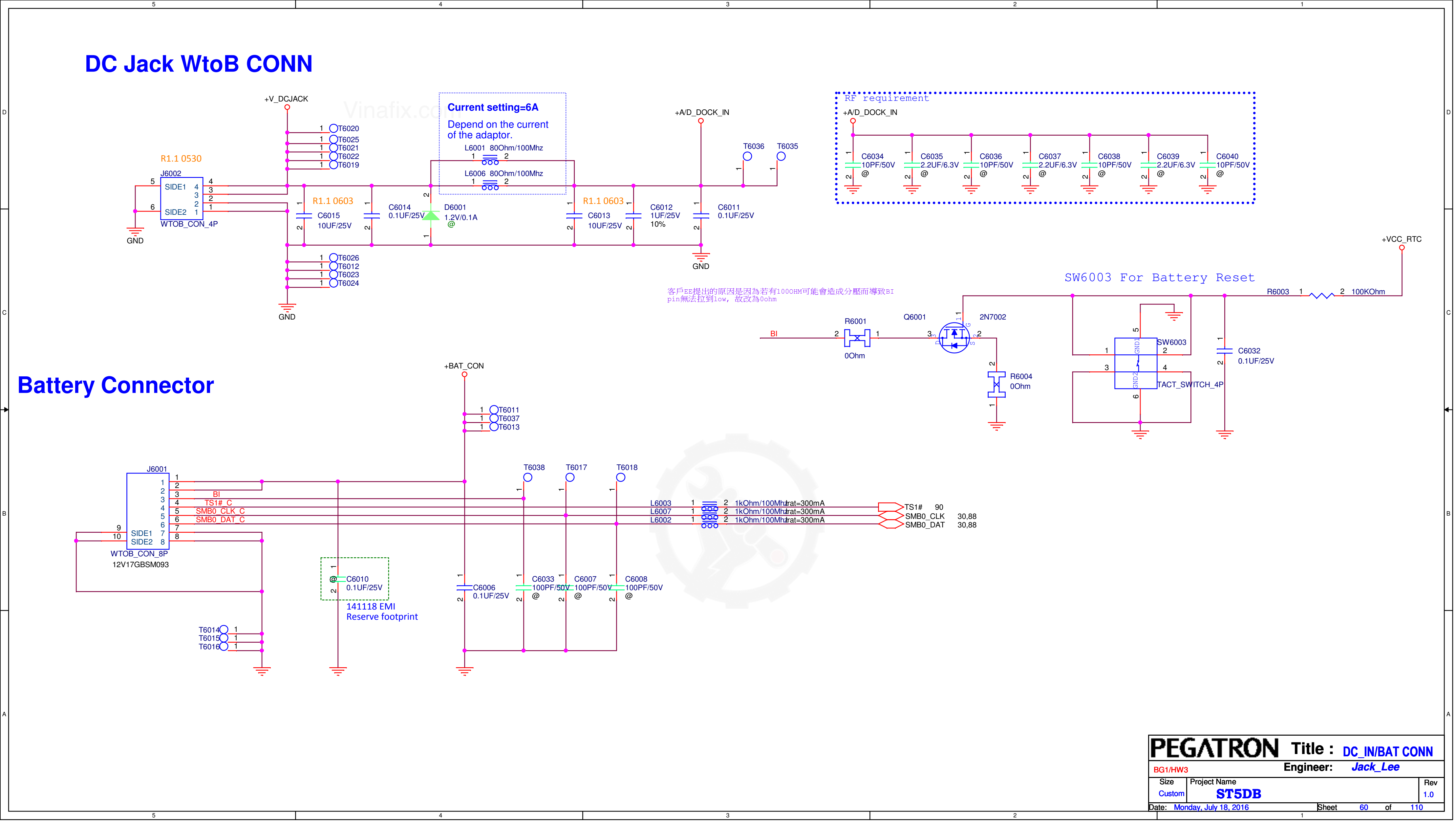
G Sensor

+3VS +3VS 3,4,17,20,21,22,23,24,28,30,31,32,36,40,44,45,47,50,51,53,57,58,61,62,65,91,92



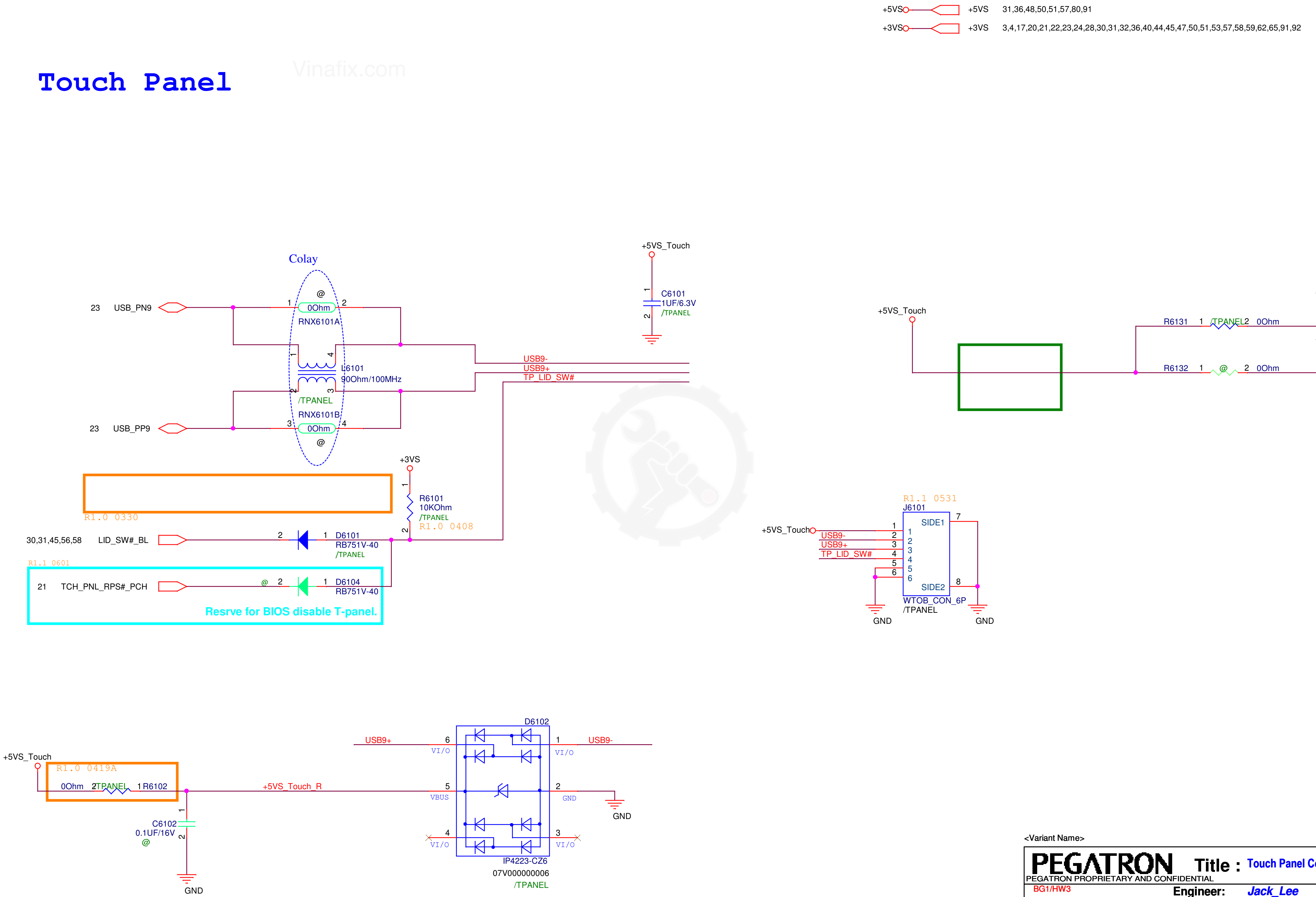
U5806.1 Pull Up V	Slave Address(7-bits): 0x19 (W: 0x32, R: 0x33)
U5806.1 Pull Down	Slave Address(7-bits): 0x18 (W: 0x30, R: 0x31)

FAE
1. Left INT2 Floating
2. SDO use 0 ohm as option
3. INT PUD R UNMOUNT



DC Jack WtoB CONN
+V_DCJACK
R1.1 0530
J6002
SIDE1
SIDE2
WTOB_CON_4P
GND
T6020
T6025
T6021
T6022
T6019
T6026
T6012
T6023
T6024
Current setting=6A
Depend on the current of the adaptor.
L6001 80Ohm/100Mhz
L6006 80Ohm/100Mhz
R1.1 0603
C6015 10UF/25V
C6014 0.1UF/25V
D6001 1.2V/0.1A
C6013 10UF/25V
C6012 1UF/25V 10%
C6011 0.1UF/25V
+A/D_DOCK_IN
T6036
T6035
RF requirement
C6034 10PF/50V
C6035 2.2UF/6.3V
C6036 10PF/50V
C6037 2.2UF/6.3V
C6038 10PF/50V
C6039 2.2UF/6.3V
C6040 10PF/50V
+VCC_RTC
SW6003 For Battery Reset
客戶EE提出的原因是因為若有100OHM可能會造成分壓而導致BI
pin無法拉到low, 故改為0ohm
R6003 100KOhm
BI
R6001 0Ohm
Q6001 2N7002
R6004 0Ohm
SW6003
TACT_SWITCH_4P
C6032 0.1UF/25V
Battery Connector
+BAT_CON
T6011
T6037
T6013
J6001
TS1#_C
SMB0_CLK_C
SMB0_DAT_C
WTOB_CON_8P
12V17GBSM093
T6038
T6017
T6018
L6003 1kOhm/100Mhz rat=300mA
L6007 1kOhm/100Mhz rat=300mA
L6002 1kOhm/100Mhz rat=300mA
TS1# 90
SMB0_CLK 30,88
SMB0_DAT 30,88
C6010 0.1UF/25V
141118 EMI
Reserve footprint
C6006 0.1UF/25V
C6033 100PF/50V
C6007 100PF/50V
C6008 100PF/50V
T6014
T6015
T6016
BG1/HW3
Title : DC_IN/BAT CONN
Engineer: Jack_Lee
Size Custom
Project Name ST5DB
Rev 1.0
Date: Monday, July 18, 2016
Sheet 60 of 110

Touch Panel



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

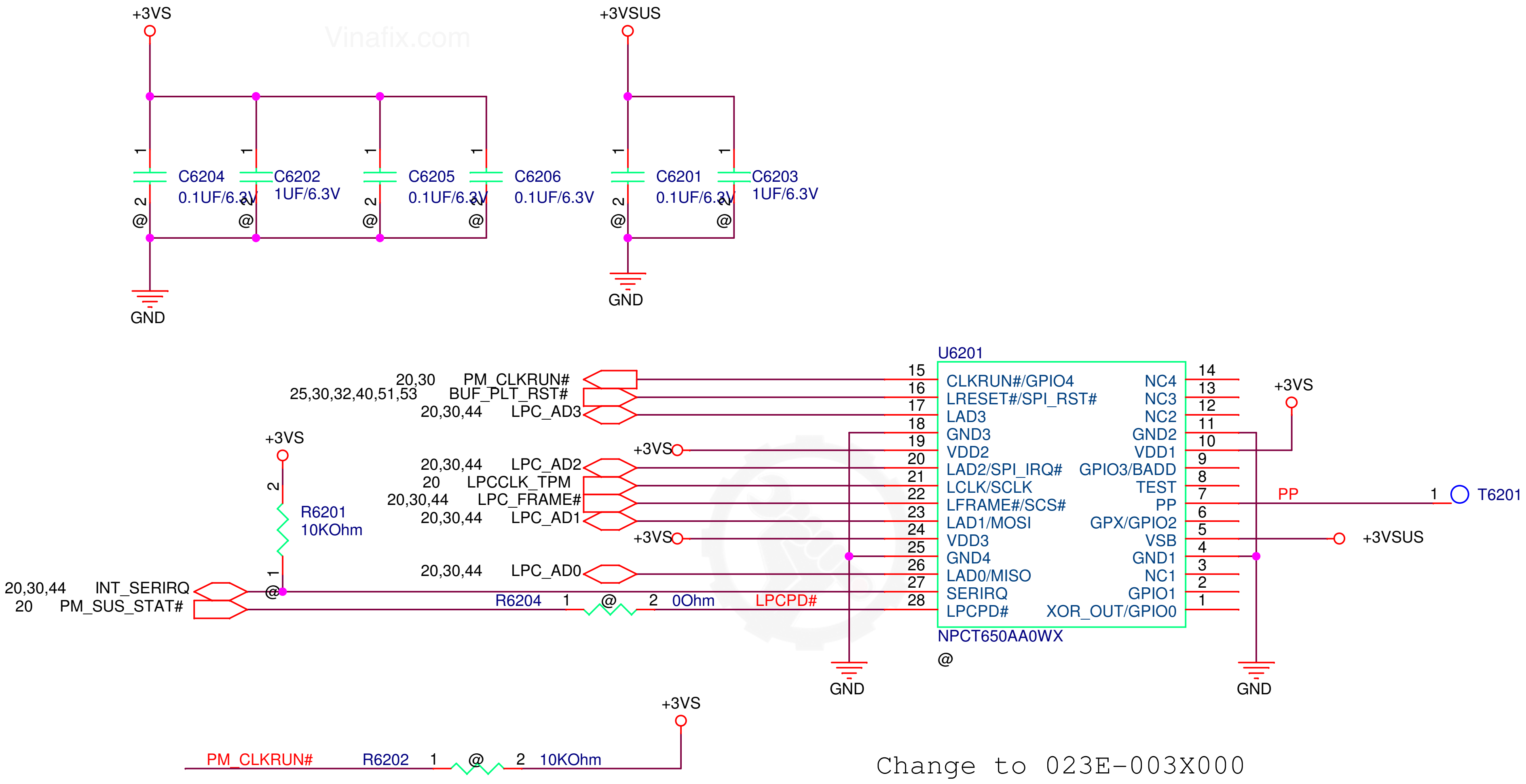
BG1/HW3

Title : Touch Panel Conn

Engineer: Jack_Lee

Size	Project Name	Rev
Custom		1.0

Date: Monday, July 18, 2016 Sheet 61 of 110



Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

PEGATRON **Title :** TPM CONN

BG1/HW3 **Engineer:** *Jack_Lee*

Size	Project Name	Rev
A	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 62 of 110

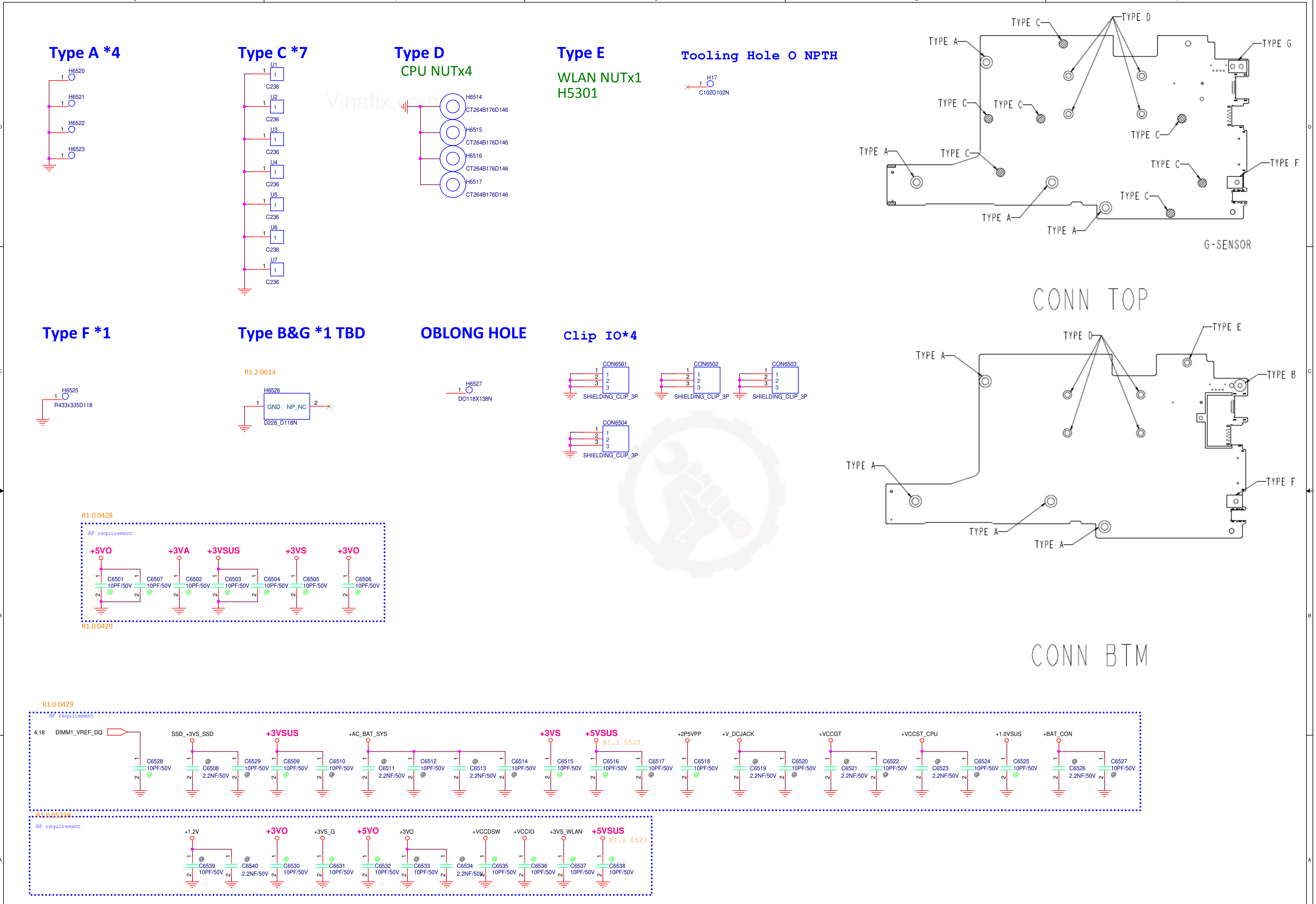
PEGATRON Title : <Title>

BG1/HW3

Engineer: *Jack_Lee*

Size	Project Name	Rev
A	**ST5DB**	1.0

Date: Monday, July 18, 2016 Sheet 63 of 110



<Variant Name>

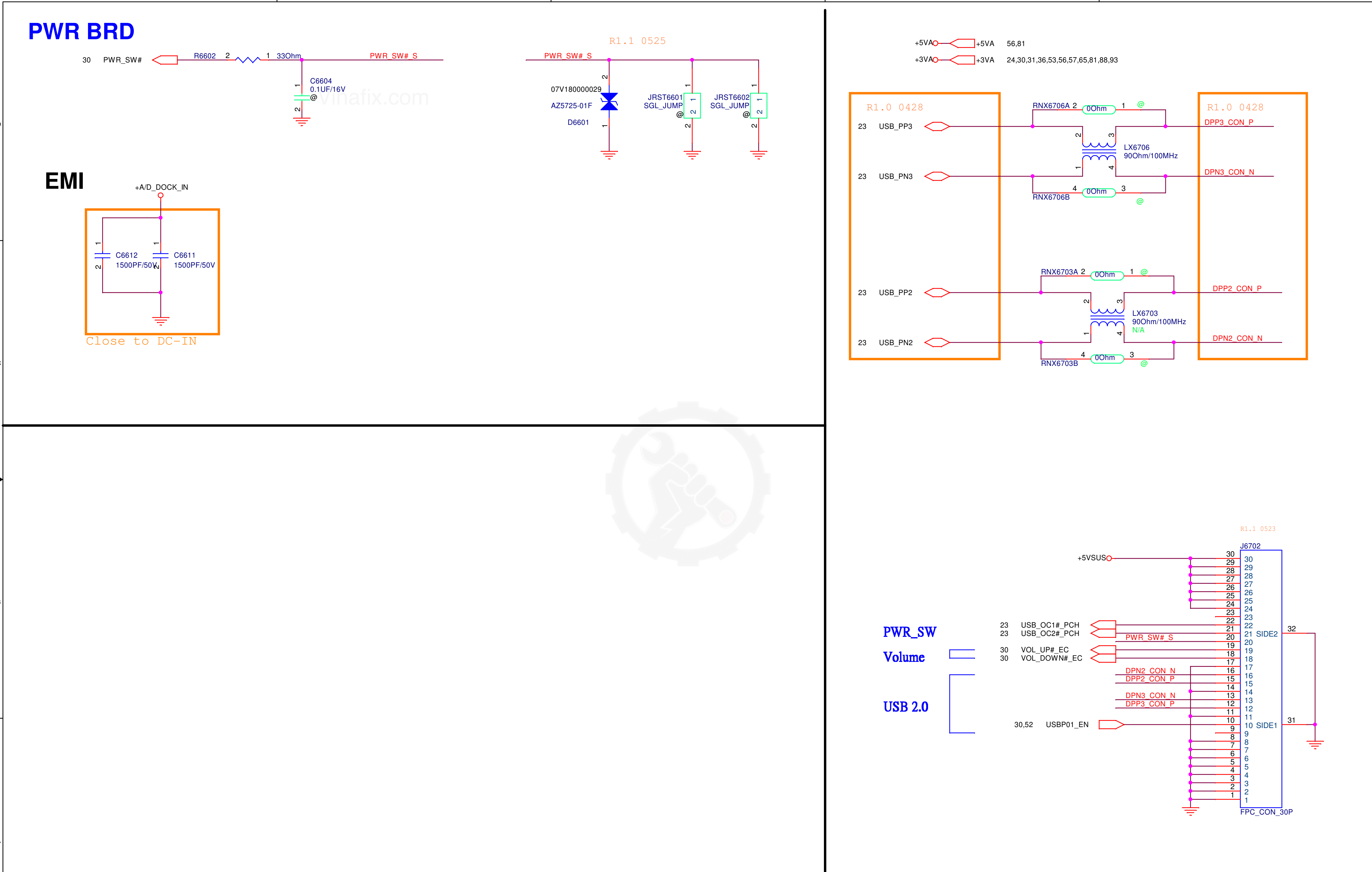
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: ME_CONN,Skew Hole

Engineer: Jack_Lee

Size	Project Name	Rev
C	ST5DB	1.0

Date: Monday, July 18, 2016 | Sheet 65 of 110



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Title: PWR BRD/ IO BRD

Engineer: Jack_Lee

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 66 of 110

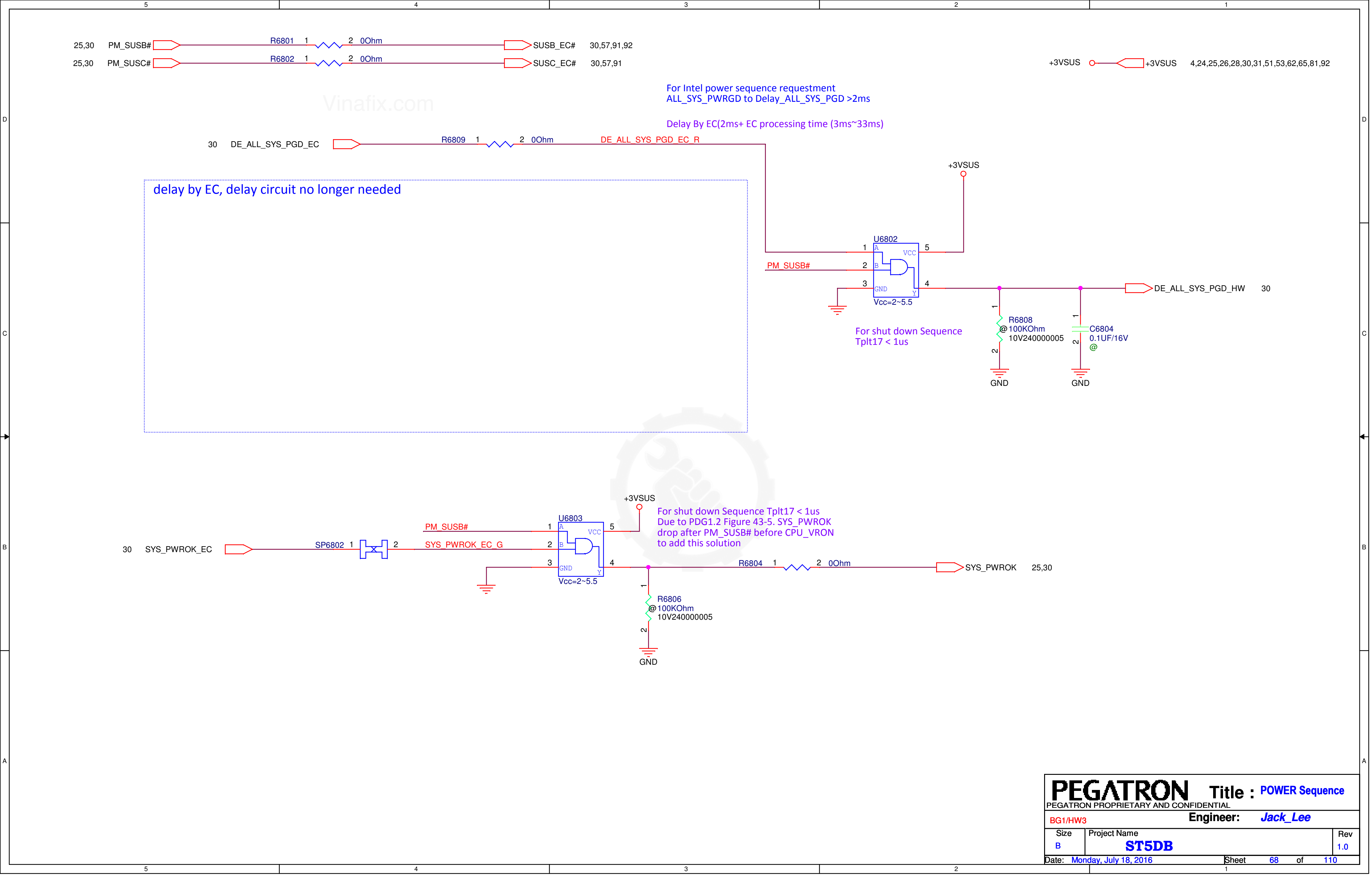
5 4 3 2 1

D C B A

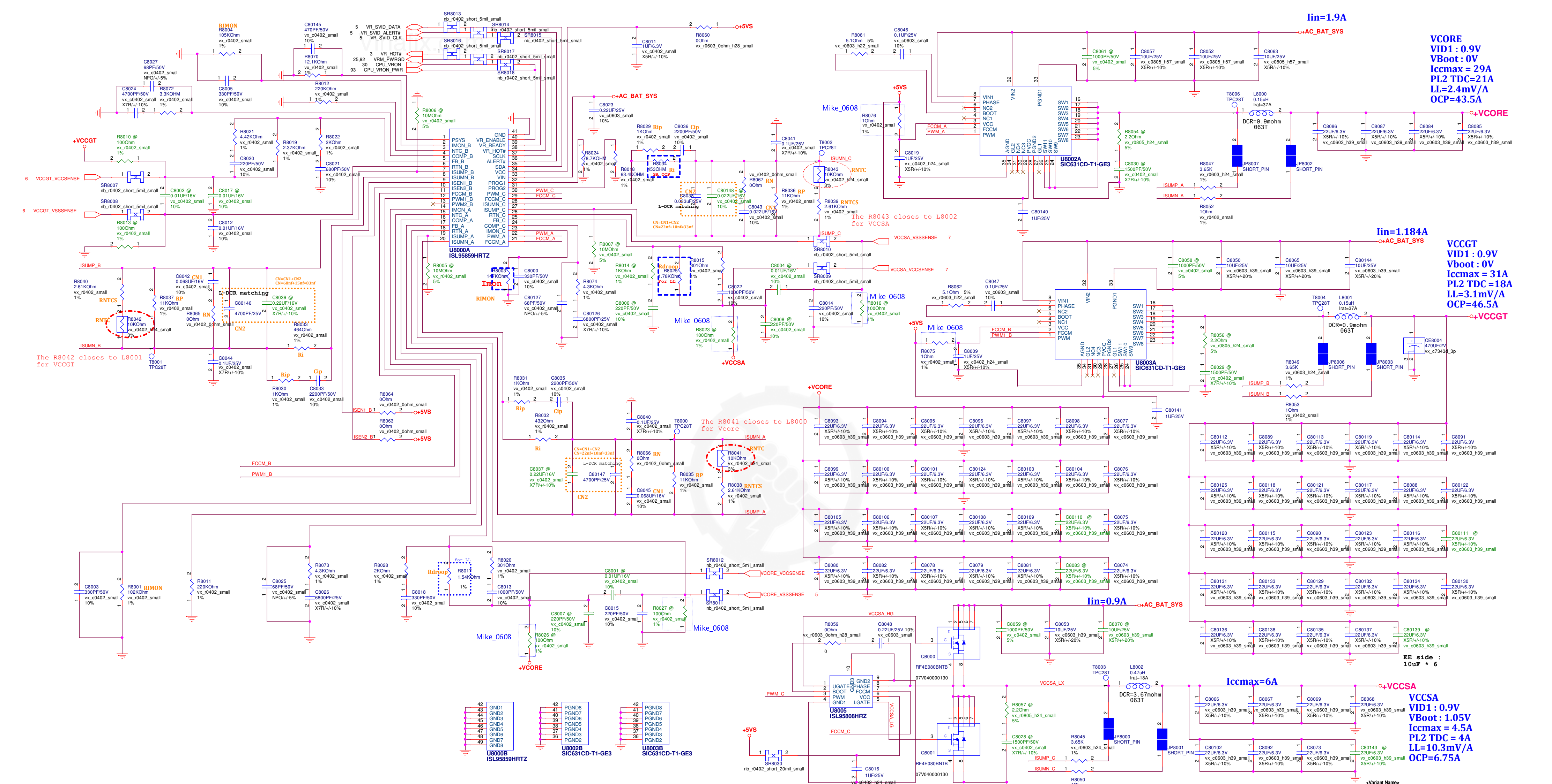
R1.1

J6702 co-lay J6703

PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : USB Repeter	
BG1/HW3	Engineer: Jack_Lee	
Size Custom	Project Name ST5DB	Rev 1.0
Date: Monday, July 18, 2016	Sheet 67 of 110	


25,30 PM_SUSB#
R6801 1 2 0Ohm
SUSB_EC# 30,57,91,92
25,30 PM_SUSC#
R6802 1 2 0Ohm
SUSC_EC# 30,57,91
+3VSUS
+3VSUS 4,24,25,26,28,30,31,51,53,62,65,81,92
For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms
Delay By EC(2ms+ EC processing time (3ms~33ms)
30 DE_ALL_SYS_PGD_EC
R6809 1 2 0Ohm
DE_ALL_SYS_PGD_EC_R
delay by EC, delay circuit no longer needed
+3VSUS
U6802
VCC
GND
Vcc=2~5.5
PM_SUSB#
DE_ALL_SYS_PGD_HW 30
R6808
@ 100KOhm
10V240000005
C6804
0.1UF/16V
@
For shut down Sequence
Tplt17 < 1us
GND
GND
+3VSUS
U6803
For shut down Sequence Tplt17 < 1us
Due to PDG1.2 Figure 43-5. SYS_PWROK
drop after PM_SUSB# before CPU_VRON
to add this solution
PM_SUSB#
30 SYS_PWROK_EC
SP6802
SYS_PWROK_EC_G
Vcc=2~5.5
R6804 1 2 0Ohm
SYS_PWROK 25,30
R6806
@ 100KOhm
10V240000005
GND
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER Sequence
BG1/HW3
Engineer: Jack_Lee
Size B
Project Name ST5DB
Rev 1.0
Date: Monday, July 18, 2016
Sheet 68 of 110

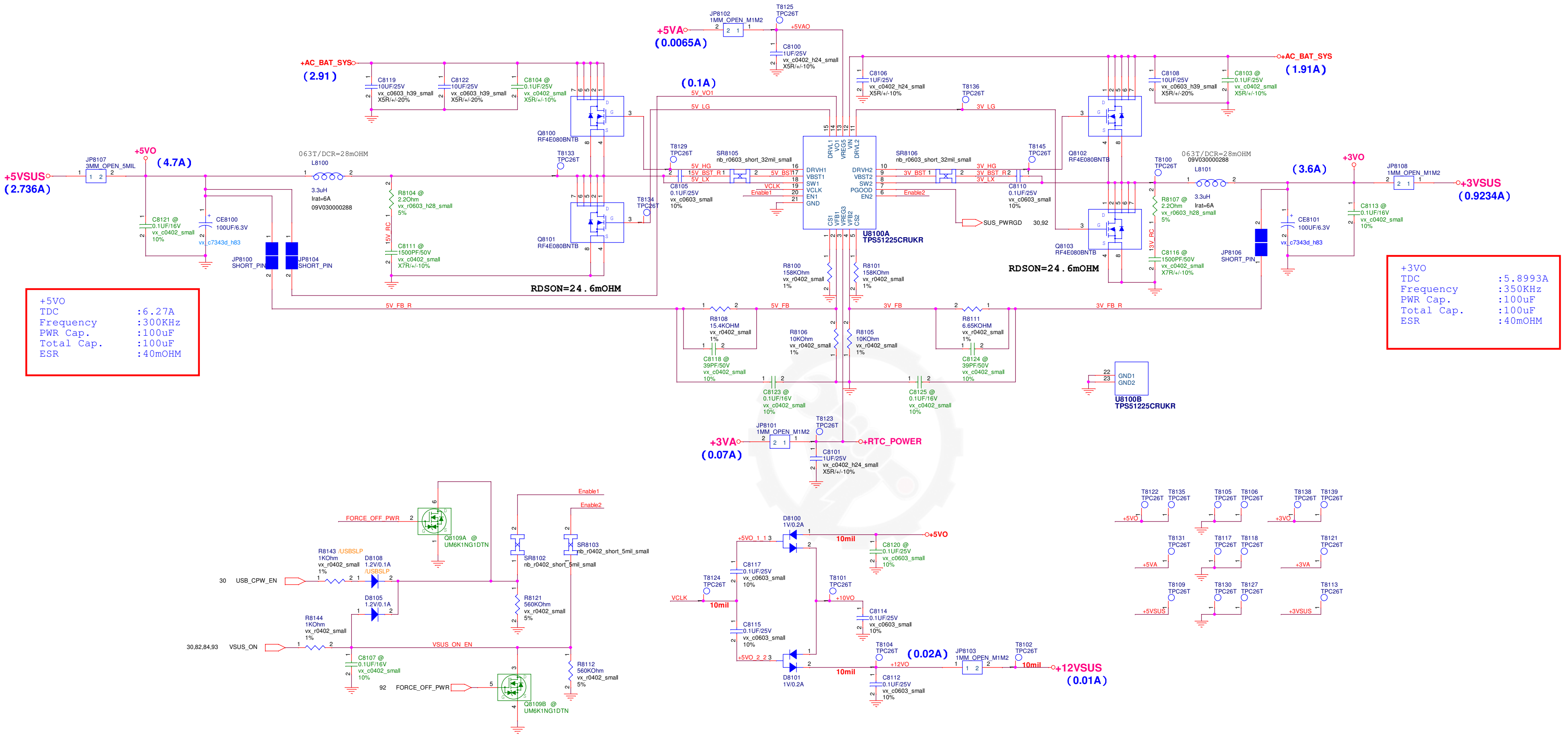
VCORE & VCCGT & VCCSA POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_VCORE
Engineer: Adams Lin
Size: Custom
Project Name: R15
Rev: 1.0
Date: Monday, July 18, 2016
Sheet 80 of 94

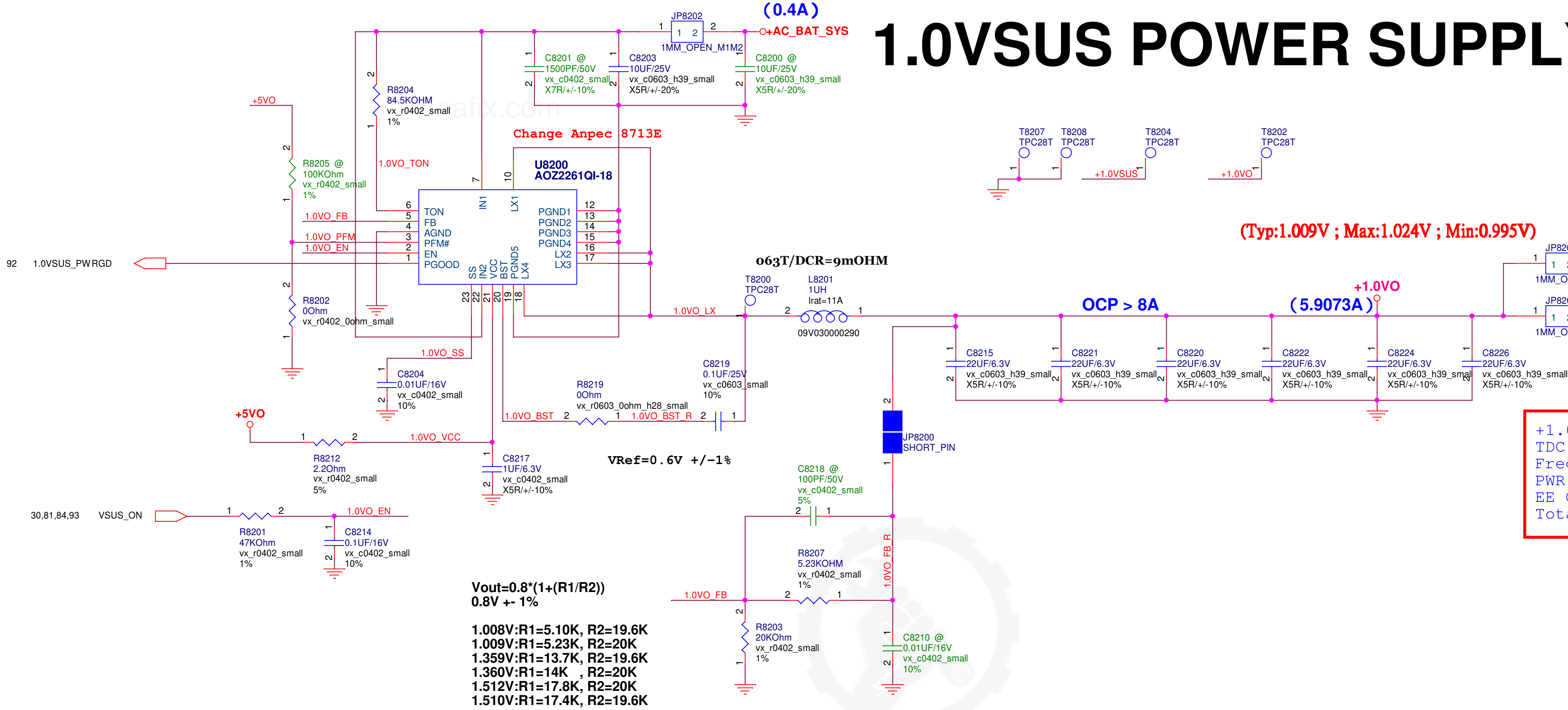
5VO & 3VO POWER SUPPLY



+5VO	
TDC	:6.27A
Frequency	:300KHz
PWR Cap.	:100uF
Total Cap.	:100uF
ESR	:40mOHM

+3VO	
TDC	:5.8993A
Frequency	:350KHz
PWR Cap.	:100uF
Total Cap.	:100uF
ESR	:40mOHM

1.0VSUS POWER SUPPLY

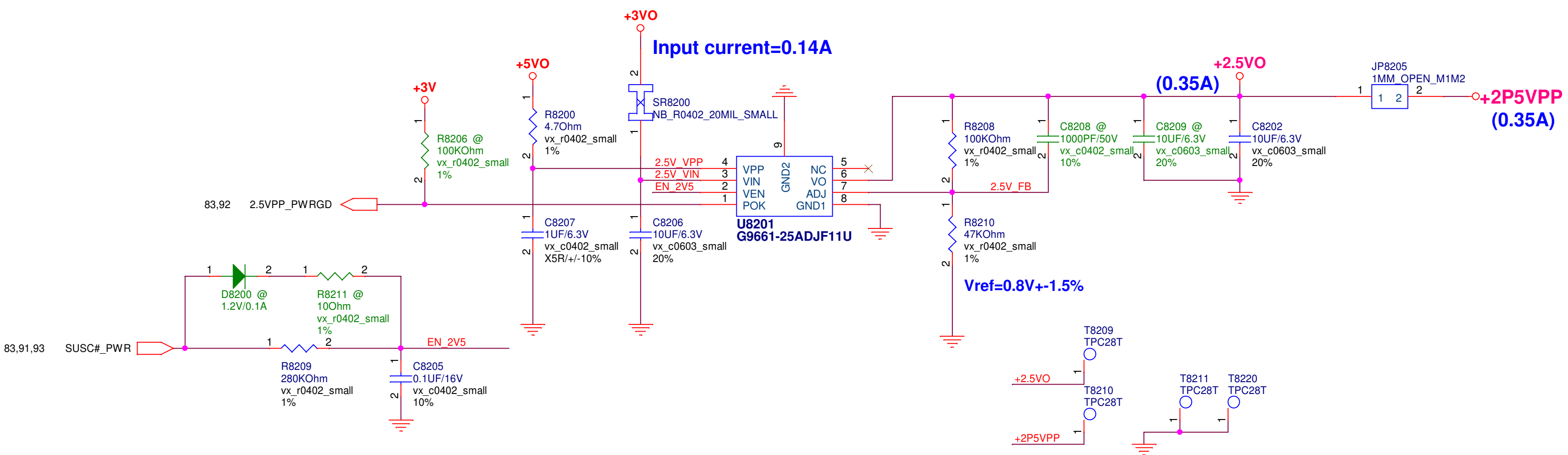


Vout=0.8*(1+(R1/R2))
0.8V +- 1%

1.008V:R1=5.10K, R2=19.6K
1.009V:R1=5.23K, R2=20K
1.359V:R1=13.7K, R2=19.6K
1.360V:R1=14K , R2=20K
1.512V:R1=17.8K, R2=20K
1.510V:R1=17.4K, R2=19.6K

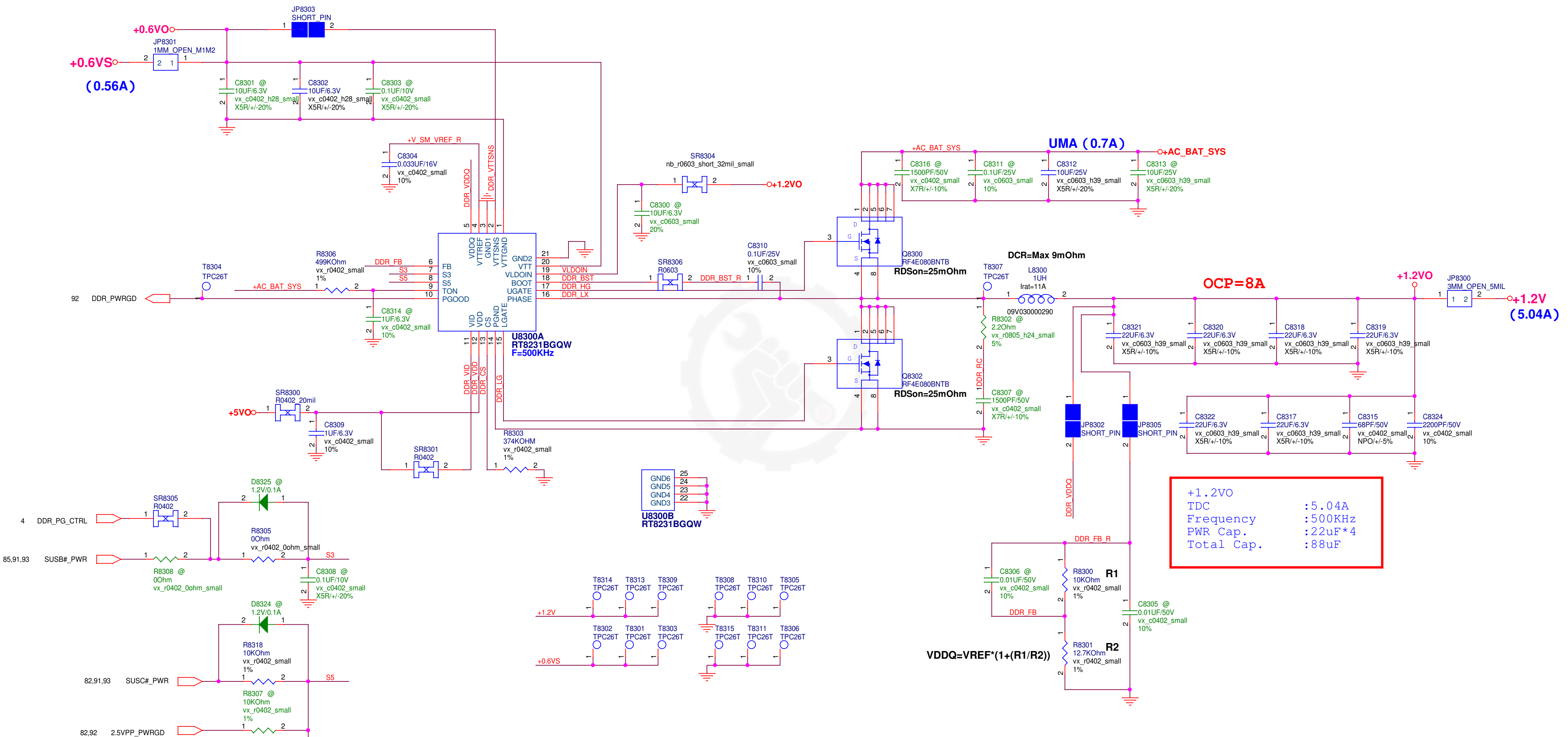
+1.0VO	
TDC	:5.9073A
Frequency	:519KHz
PWR Cap.	:132uF
EE Cap	:
Total Cap.	:132uF

2.5V POWER SUPPLY



+2.5VO	
TDC	:0.35A
OCP	:3A
PWR Cap.	:20uF
EE Cap.	:10uF
Total Cap.	:30uF

DDR & VTT POWER SUPPLY



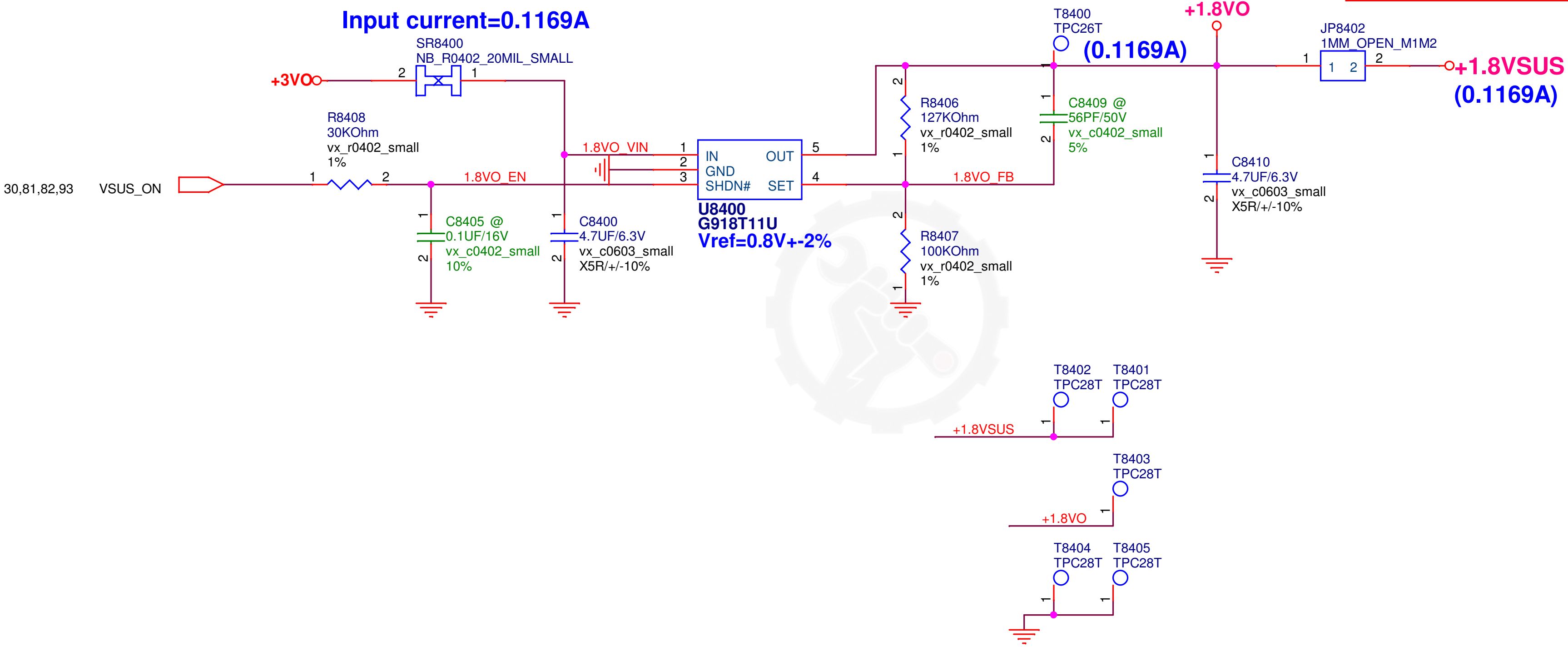
VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_DDR & VTT
Engineer: Adams Lin
BG1-POWER
Size: Custom
Project Name: R15
Rev: 1.0
Date: Monday, July 18, 2016
Sheet 83 of 94

1.8VSUS POWER SUPPLY

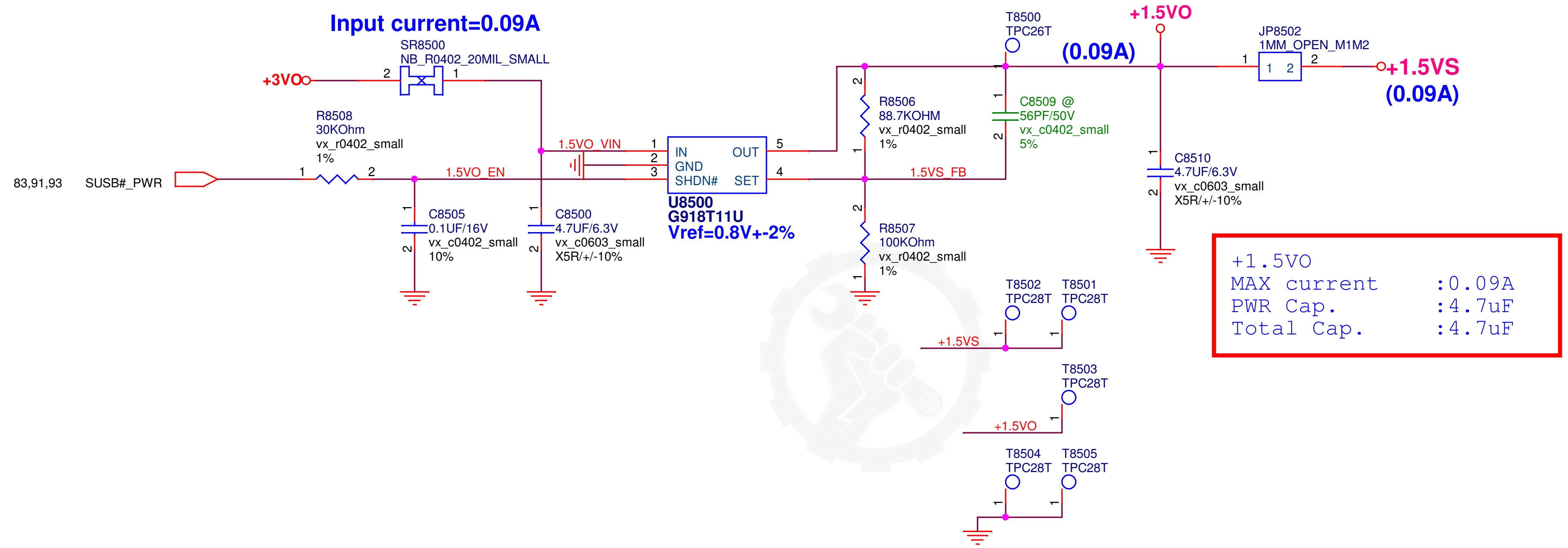
+1.8VO		
MAX current	:0.1169A	
PWR Cap.	:20uF	
Total Cap.	:20uF	



<Variant Name>

PEGATRON	Title : POWER_+1.8VSUS	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
	Engineer:	Adams Lin
Size: Custom	Project Name: R15	Rev: 1.0
Date: Monday, July 18, 2016	Sheet 84 of 94	

1.5VS POWER SUPPLY



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

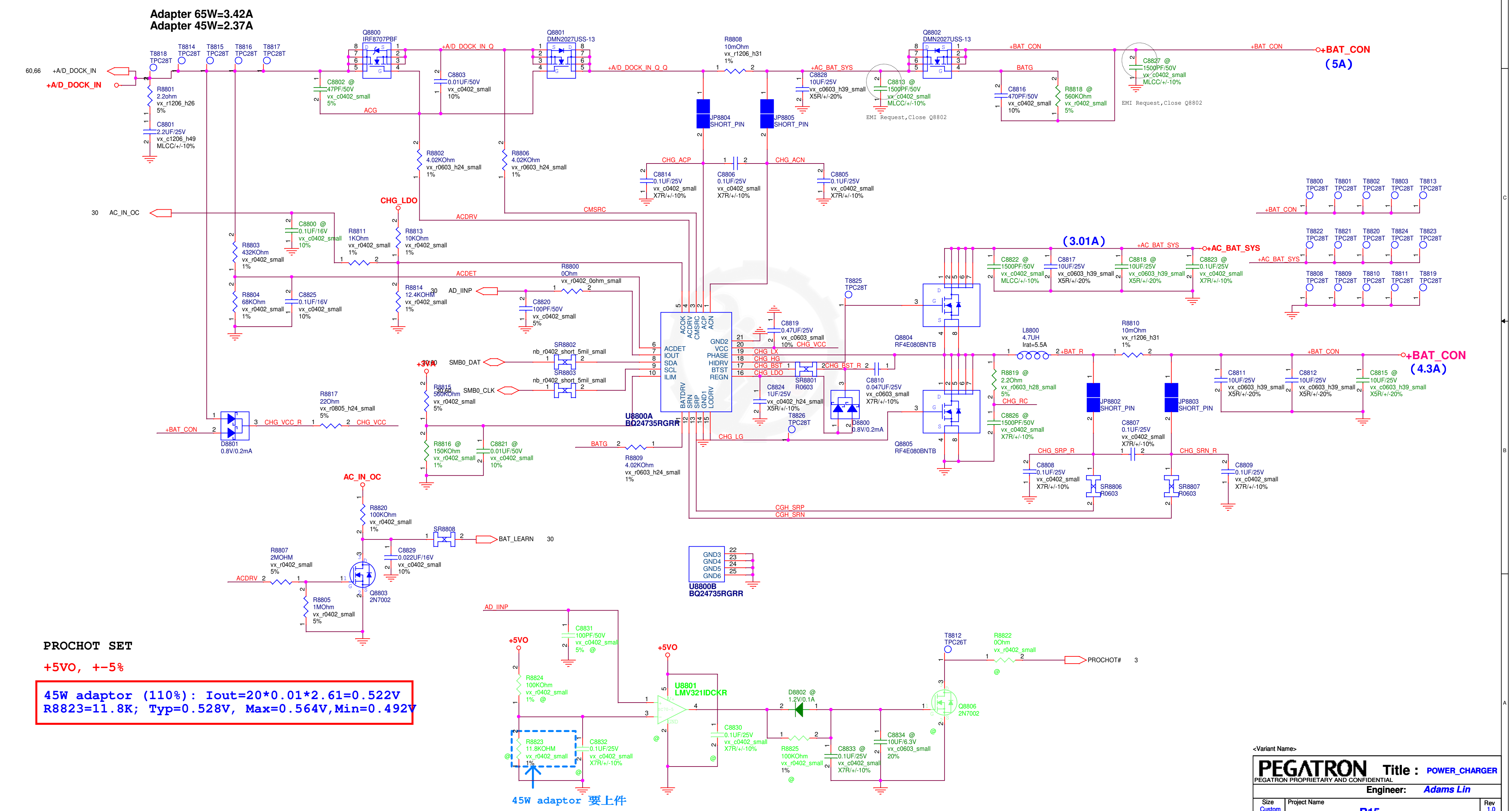
Title : POWER_+1.5VS

Engineer: Adams Lin

Size	Project Name	Rev
Custom	R15	1.0

Date: Monday, July 18, 2016 Sheet 85 of 94

BATTERY CHARGER



PROCHOT SET

+5VO, +-5%

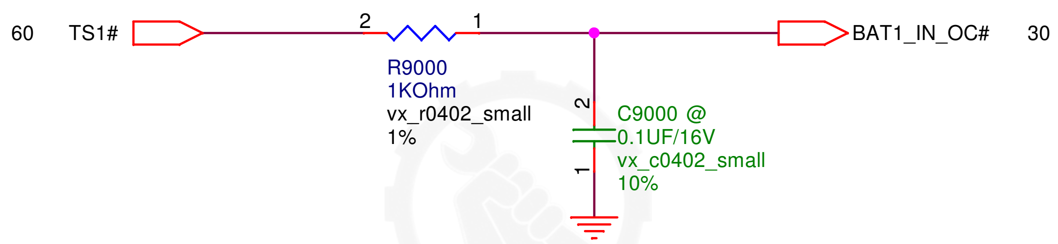
45W adaptor (110%): Iout=20*0.01*2.61=0.522V
R8823=11.8K; Typ=0.528V, Max=0.564V,Min=0.492V

PEGATRON Title : POWER_CHARGER
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin

Size	Project Name	Rev
Custom	R15	1.0

Date: Monday, July 18, 2016 Sheet 88 of 94

BATTERY IN DETECT



<Variant Name>

PEGATRON

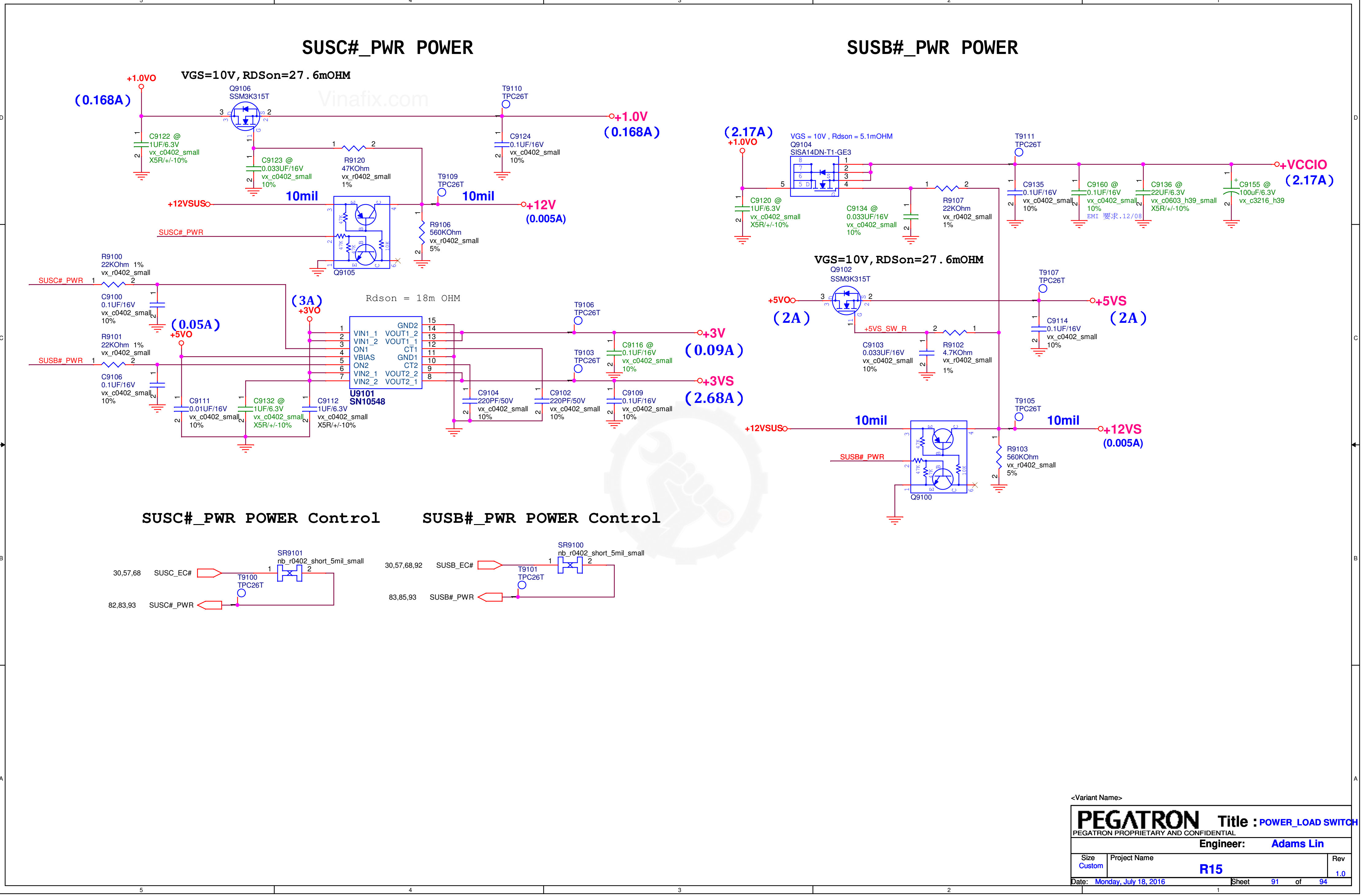
Title : POWER_DETECT

PEGATRON PROPRIETARY AND CONFIDENTIAL

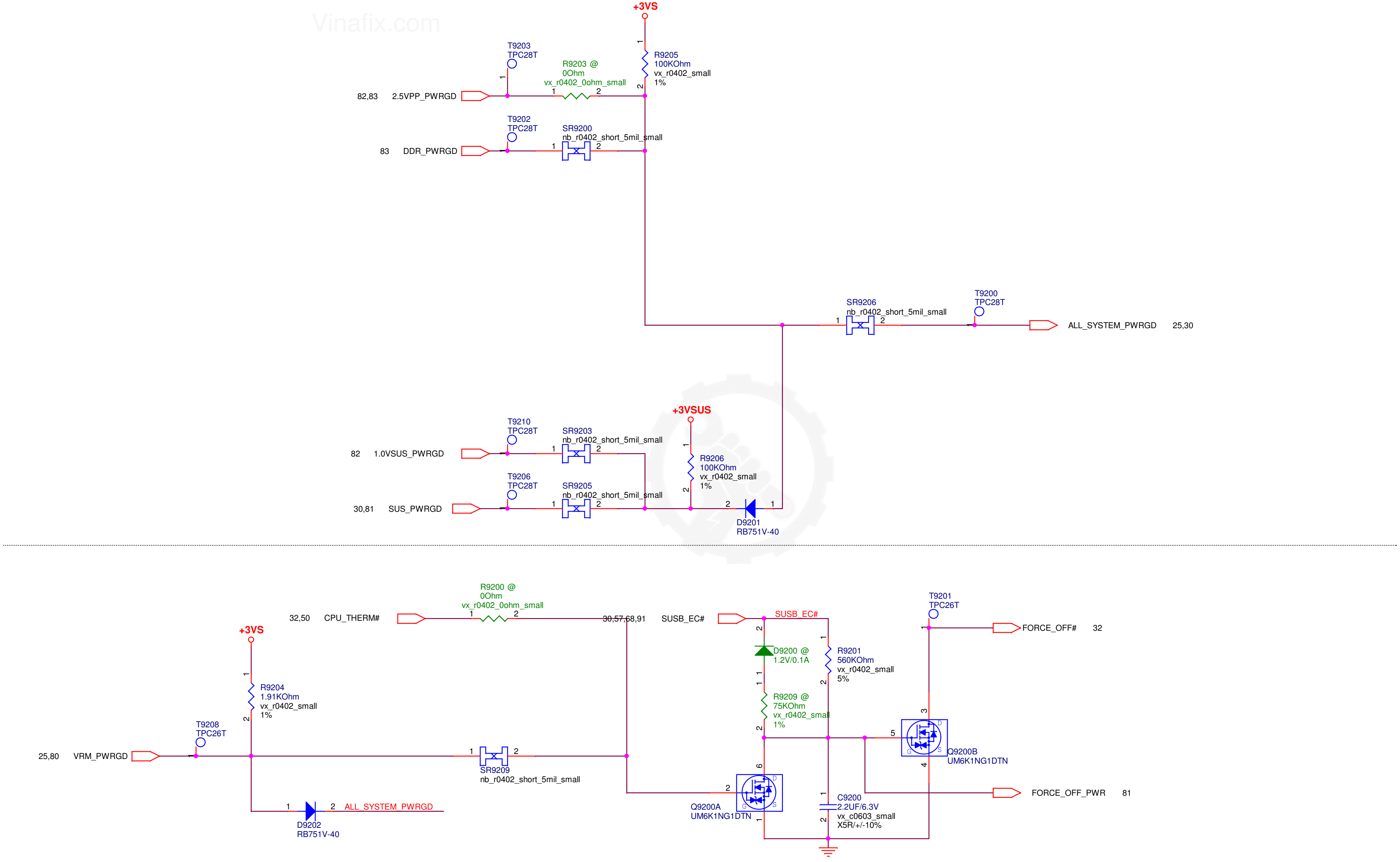
Engineer: Adams Lin

Size	Project Name	Rev
Custom	R15	1.0

Date: Monday, July 18, 2016 | Sheet 90 of 94


SUSC#_PWR POWER
SUSB#_PWR POWER
VGS=10V,RDSon=27.6mOHM
Q9106 SSM3K315T
T9110 TPC26T
+1.0VO
(0.168A)
+1.0V
(0.168A)
C9122 @ 1UF/6.3V vx_c0402_small X5R/+/-10%
C9123 @ 0.033UF/16V vx_c0402_small 10%
R9120 47KOhm vx_r0402_small 1%
C9124 0.1UF/16V vx_c0402_small 10%
T9109 TPC26T
10mil
+12VSUS
+12V
(0.005A)
SUSC#_PWR
R9106 560KOhm vx_r0402_small 5%
Q9105
R9100 22KOhm 1% vx_r0402_small
C9100 0.1UF/16V vx_c0402_small 10%
(0.05A)
+5VO
R9101 22KOhm 1% vx_r0402_small
SUSB#_PWR
C9106 0.1UF/16V vx_c0402_small 10%
(3A)
+3VO
Rdson = 18m OHM
U9101 SN10548
VIN1_1 VIN1_2 ON1 VBIAS ON2 VIN2_1 VIN2_2 GND2 VOUT1_2 VOUT1_1 CT1 GND1 CT2 VOUT2_2 VOUT2_1
T9106 TPC26T
+3V
(0.09A)
C9116 @ 0.1UF/16V vx_c0402_small 10%
T9103 TPC26T
+3VS
(2.68A)
C9111 0.01UF/16V vx_c0402_small 10%
C9132 @ 1UF/6.3V vx_c0402_small X5R/+/-10%
C9112 1UF/6.3V vx_c0402_small X5R/+/-10%
C9104 220PF/50V vx_c0402_small 10%
C9102 220PF/50V vx_c0402_small 10%
C9109 0.1UF/16V vx_c0402_small 10%
(2.17A)
+1.0VO
VGS = 10V , Rdson = 5.1mOHM
Q9104 SISA14DN-T1-GE3
T9111 TPC26T
+VCCIO
(2.17A)
C9120 @ 1UF/6.3V vx_c0402_small X5R/+/-10%
C9134 @ 0.033UF/16V vx_c0402_small 10%
R9107 22KOhm vx_r0402_small 1%
C9135 0.1UF/16V vx_c0402_small 10%
C9160 @ 0.1UF/16V vx_c0402_small 10%
EMI 要求.12/08
C9136 @ 22UF/6.3V vx_c0603_h39_small X5R/+/-10%
C9155 @ 100uF/6.3V vx_c3216_h39
VGS=10V,RDSon=27.6mOHM
Q9102 SSM3K315T
T9107 TPC26T
+5VO
(2A)
+5VS
(2A)
+5VS_SW_R
C9103 0.033UF/16V vx_c0402_small 10%
R9102 4.7KOhm vx_r0402_small 1%
C9114 0.1UF/16V vx_c0402_small 10%
T9105 TPC26T
+12VSUS
10mil
+12VS
(0.005A)
SUSB#_PWR
R9103 560KOhm vx_r0402_small 5%
Q9100
SUSC#_PWR POWER Control
SUSB#_PWR POWER Control
SR9101 nb_r0402_short_5mil_small
30,57,68 SUSC_EC#
T9100 TPC26T
82,83,93 SUSC#_PWR
SR9100 nb_r0402_short_5mil_small
30,57,68,92 SUSB_EC#
T9101 TPC26T
83,85,93 SUSB#_PWR
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_LOAD SWITCH
Engineer: Adams Lin
Size Custom
Project Name R15
Rev 1.0
Date: Monday, July 18, 2016
Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON **Title : POWER_PROTECT**

PEGATRON PROPRIETARY AND CONFIDENTIAL

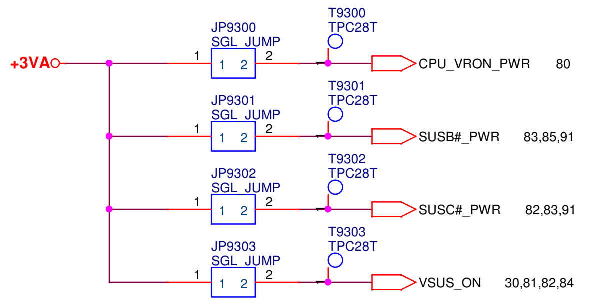
Engineer: **Adams Lin**

Size	Project Name	Rev
Custom	R15	1.0

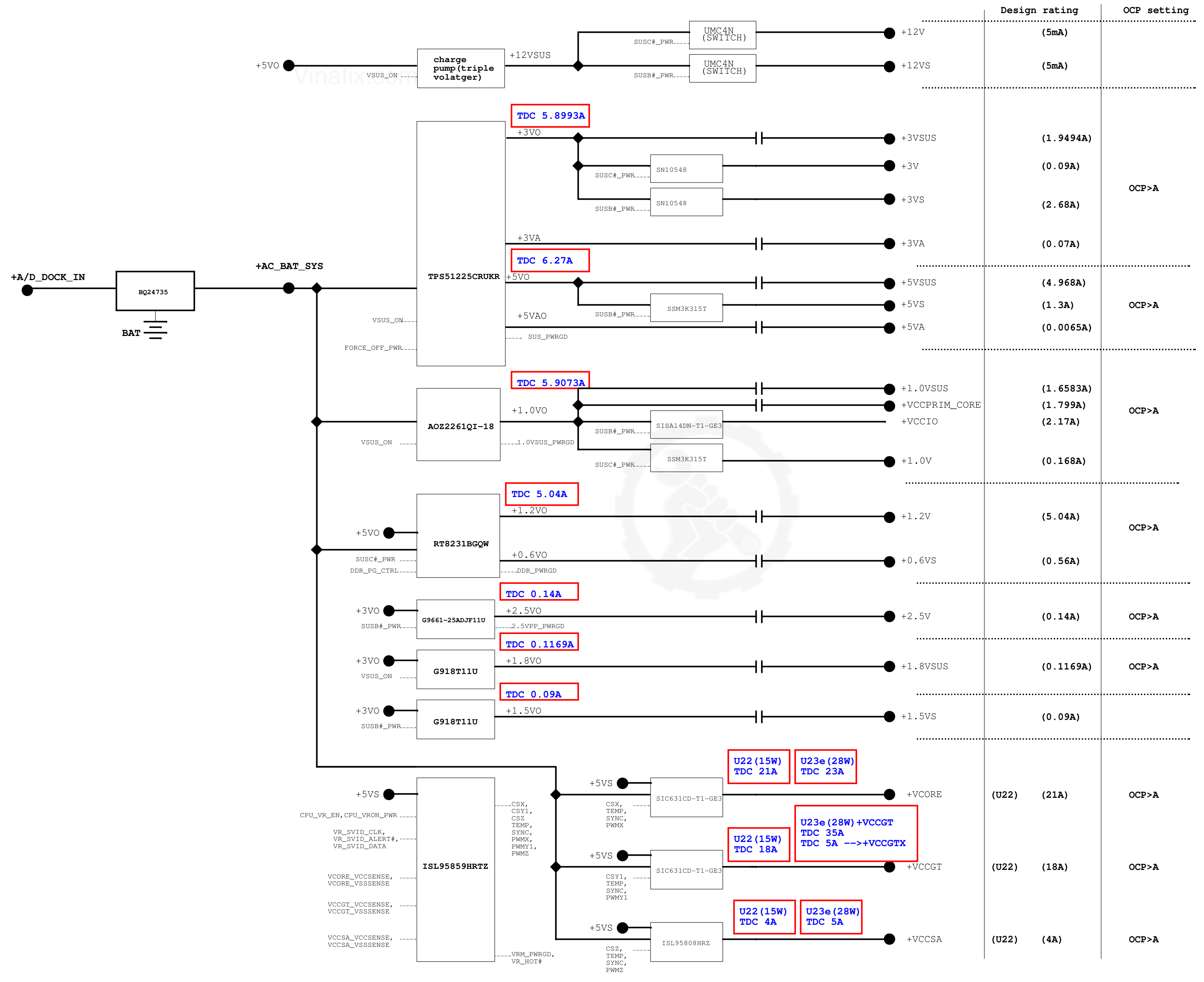
Date: Monday, July 18, 2016 Sheet 92 of 94

Net	Off-page	Sheets
+AC_BAT_SYS	+AC_BAT_SYS	45,65,80,81,82,83,88
+BAT_CON	+BAT_CON	60,65,88
+RTC_POWER	+RTC_POWER	81
+5VA	+5VA	56,81
+3VA	+3VA	24,30,31,36,53,56,57,65,81,88
+5VO	+5VO	65,81,82,83,88,91
+3VO	+3VO	65,81,82,84,85,91
+2.5VO	+2.5VO	82
+1.8VO	+1.8VO	84
+1.2VO	+1.2VO	83
+1.0VO	+1.0VO	82,91
+0.6VO	+0.6VO	83
+12VSUS	+12VSUS	28,81,91
+5VSUS	+5VSUS	52,56,65,66,81
+3VSUS	+3VSUS	4,24,25,26,28,30,31,51,53,62,65,68,81,92
+1.8VSUS	+1.8VSUS	9,24,26,84
+1.0VSUS	+1.0VSUS	26,65,82
+12V	+12V	91
+2P5VPP	+2P5VPP	16,17,57,65,82
+1.2V	+1.2V	4,7,15,16,17,18,57,65,83
+1.0V	+1.0V	7,57,91
+12VS	+12VS	28,31,48,57,91
+5VS	+5VS	31,36,48,50,51,57,61,80,91
+3VS	+3VS	3,4,17,20,21,22,23,24,28,30,31,32,36,40,44,45,47,50,51,53,57,58,59,61,62,65,91,92
+0.6VS	+0.6VS	15,17,57,83
+VCORE	+VCORE	5,57,80
+VCCGT	+VCCGT	6,57,65,80
+VCCSA	+VCCSA	7,57,80
+VCCIO	+VCCIO	3,7,57,65,91
+VCCPRIM_CORE	+VCCPRIM_CORE	26,82

FOR POWER TEST



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_SIGNAL
BG1-POWER
Engineer: Adams Lin
Size: B
Project Name: R15
Rev: 1.0
Date: Monday, July 18, 2016
Sheet 93 of 94



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER_FLOWCHART

Engineer: Adams Lin

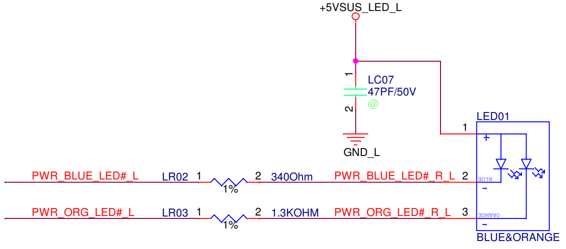
Size	Project Name	Rev
Custom	R15	1.0

Date: Monday, July 18, 2016 Sheet 94 of 94

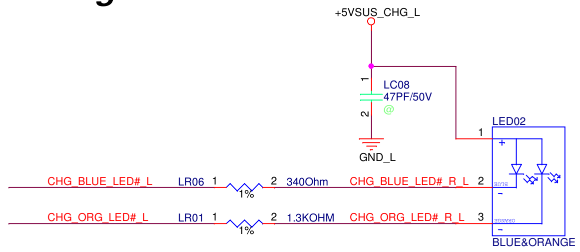
65

LED Board

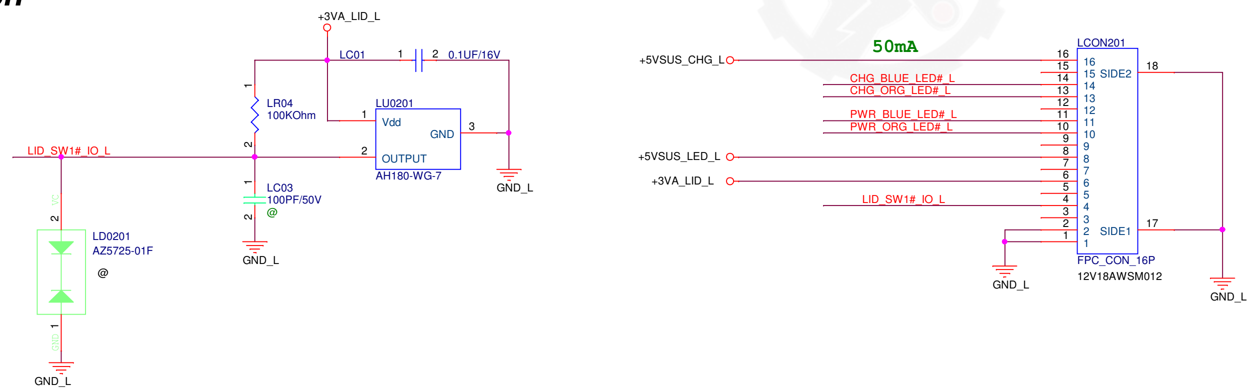
POWER LED

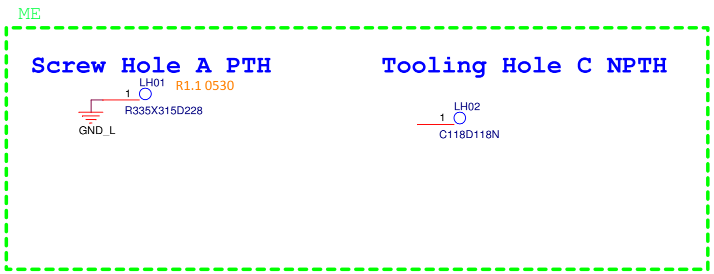


Charger LED



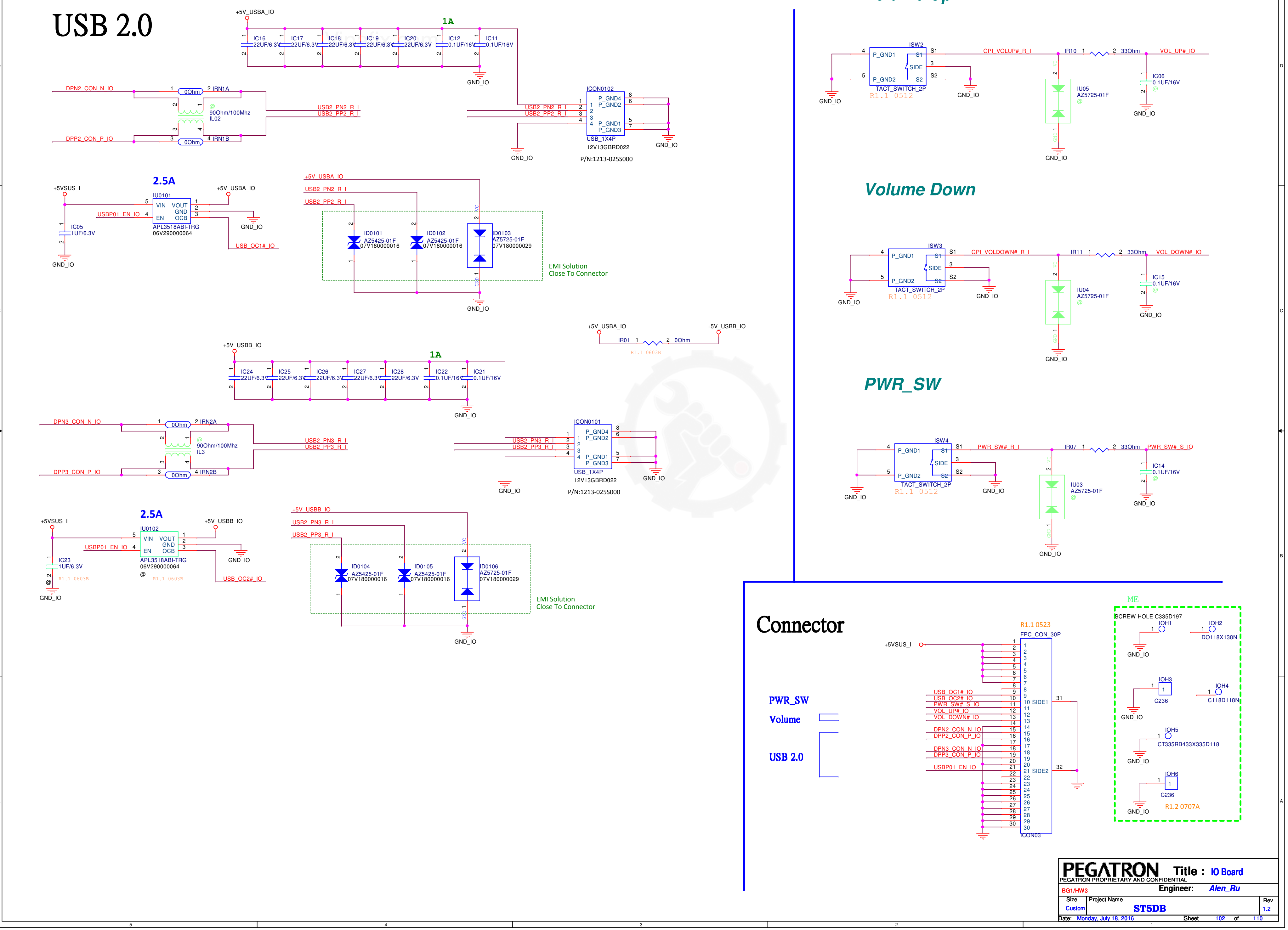
LID Switch

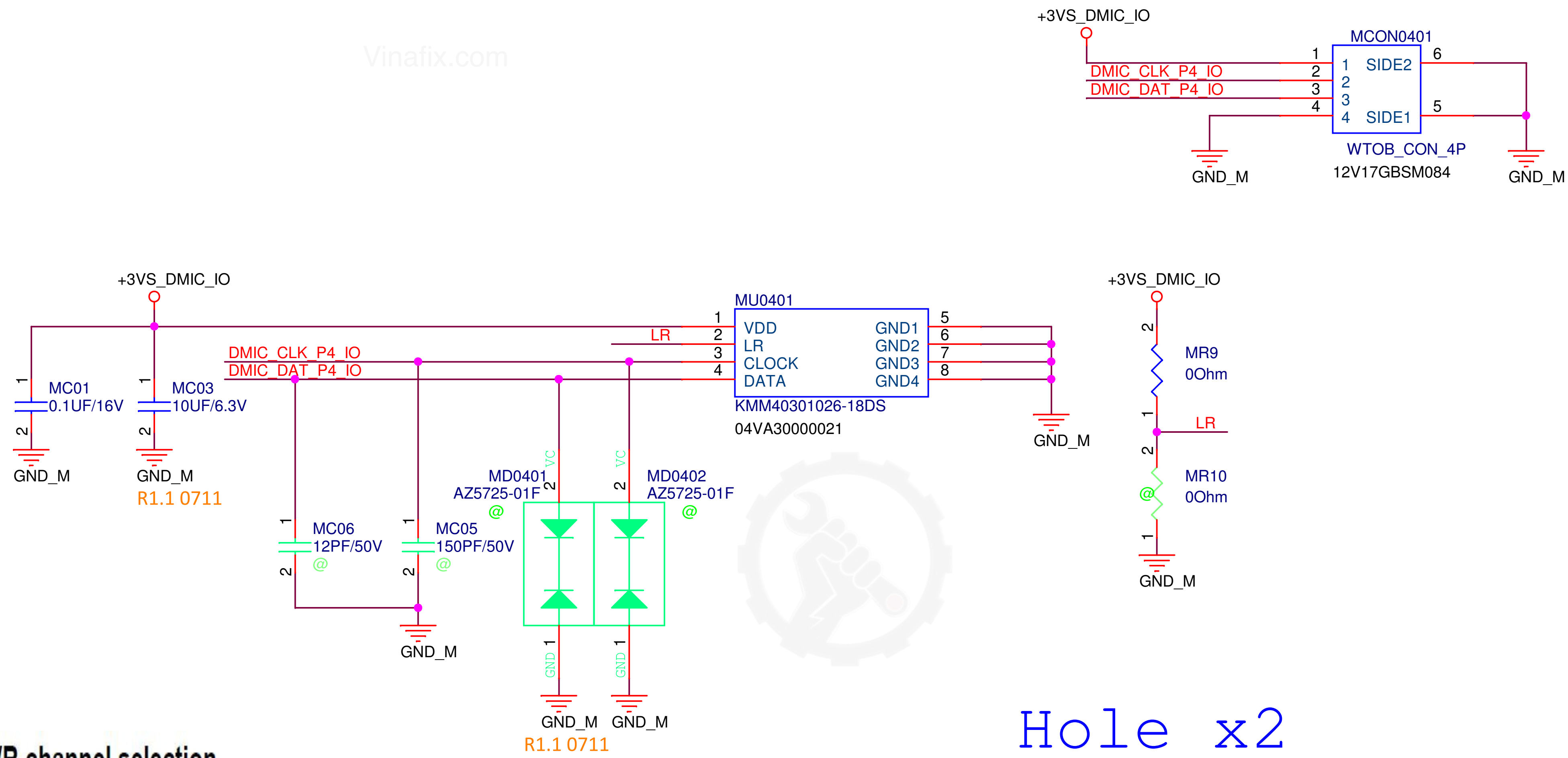




PEGATRON	Title : LED Board	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3	Engineer: Alen_Ru	
Size: Custom	Project Name: ST5DB	Rev: 1.2
Date: Monday, July 18, 2016	Sheet 101 of 110	

IO Board

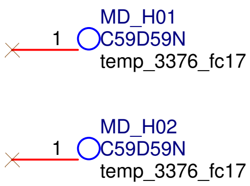

USB 2.0
Volume Up
Volume Down
PWR_SW
Connector
PWR_SW
Volume
USB 2.0
+5V_USBA_IO
1A
IC16 22UF/6.3V
IC17 22UF/6.3V
IC18 22UF/6.3V
IC19 22UF/6.3V
IC20 22UF/6.3V
IC12 0.1UF/16V
IC11 0.1UF/16V
GND_IO
DPN2_CON_N_IO
DPP2_CON_P_IO
IRN1A 0Ohm
IRN1B 0Ohm
90Ohm/100Mhz
IL02
USB2_PN2_R_I
USB2_PP2_R_I
ICON0102
P_GND4
P_GND2
P_GND1
P_GND3
USB_1X4P
12V13GBRD022
P/N:1213-025S000
2.5A
+5VSUS_I
IU0101
VIN
VOUT
GND
EN
OCB
APL3518ABI-TRG
06V290000064
USBP01_EN_IO
IC05 1UF/6.3V
USB_OC1#_IO
ID0101 AZ5425-01F 07V180000016
ID0102 AZ5425-01F 07V180000016
ID0103 AZ5725-01F 07V180000029
EMI Solution
Close To Connector
+5V_USBB_IO
IR01 0Ohm
IC24 22UF/6.3V
IC25 22UF/6.3V
IC26 22UF/6.3V
IC27 22UF/6.3V
IC28 22UF/6.3V
IC22 0.1UF/16V
IC21 0.1UF/16V
DPN3_CON_N_IO
DPP3_CON_P_IO
IRN2A 0Ohm
IRN2B 0Ohm
IL3
USB2_PN3_R_I
USB2_PP3_R_I
ICON0101
IU0102
IC23 1UF/6.3V
USB_OC2#_IO
ID0104 AZ5425-01F 07V180000016
ID0105 AZ5425-01F 07V180000016
ID0106 AZ5725-01F 07V180000029
ISW2
TACT_SWITCH_2P
R1.1 0512
GPI_VOLUP#_R_I
IR10 33Ohm
VOL_UP#_IO
IU05 AZ5725-01F
IC06 0.1UF/16V
ISW3
GPI_VOLDOWN#_R_I
IR11 33Ohm
VOL_DOWN#_IO
IU04 AZ5725-01F
IC15 0.1UF/16V
ISW4
PWR_SW#_R_I
IR07 33Ohm
PWR_SW#_S_IO
IU03 AZ5725-01F
IC14 0.1UF/16V
R1.1 0523
FPC_CON_30P
ICON03
SIDE1
SIDE2
ME
SCREW HOLE C335D197
IOH1
IOH2 DO118X138N
IOH3 C236
IOH4 C118D118N
IOH5 CT335RB433X335D118
IOH6 C236
R1.2 0707A
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : IO Board
BG1/HW3
Engineer: Alen_Ru
Size Custom
Project Name ST5DB
Rev 1.2
Date: Monday, July 18, 2016
Sheet 102 of 110



L/R channel selection

L/R	CLK Low	CLK high
GND	Date valid	High impedance
Vdd	High impedance	Date valid

Hole x2



<Variant Name>

PEGATRON

Title : MIC_IO

PEGATRON PROPRIETARY AND CONFIDENTIAL

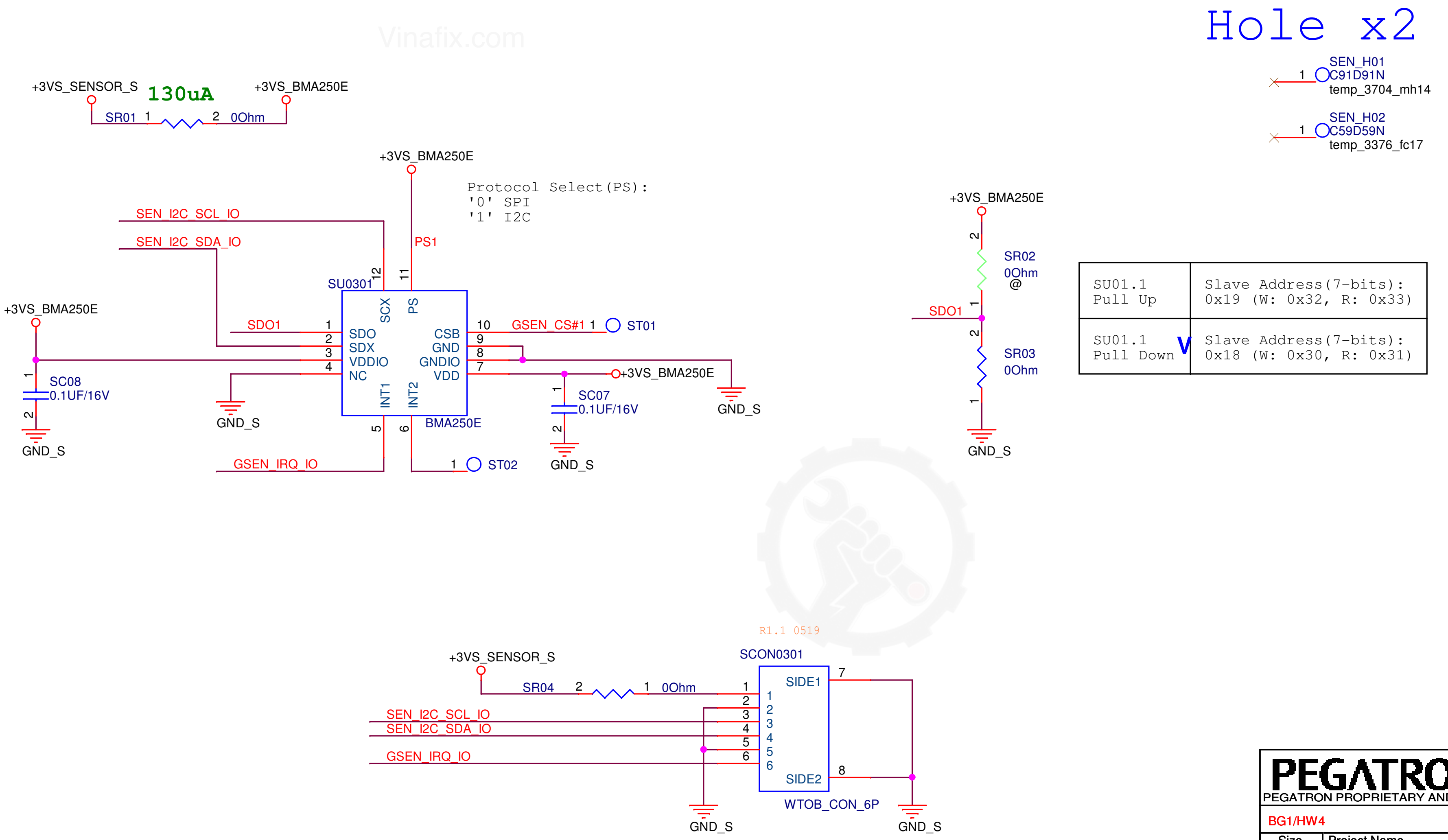
BG1/HW3

Engineer: Alen_Ru

Size	Project Name	Rev
A	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 103 of 110

G-Sensor



SU01.1 Pull Up	Slave Address(7-bits): 0x19 (W: 0x32, R: 0x33)
SU01.1 Pull Down V	Slave Address(7-bits): 0x18 (W: 0x30, R: 0x31)

PEGATRON Title : Sensor Board

BG1/HW4 Engineer: Alen_Ru

Size	Project Name	Rev
Custom	ST5DB	1.0

Date: Monday, July 18, 2016 Sheet 104 of 110