L-IG41M3 Rev:1.1

TABLE OF CONTENTS

Design guide:
649795_Intel_G31_Platform_Design_Guide_Rev1_0 for ICH7
367652_Intel_4_Series_Platform_Design_Guide_Rev2_3

Revision History

Rev	Data	Description
A	2009/03/14	
0.1	2009/05/08	Page04:add cpu heat sink fix HOLE via for lenovo request (edit cpu lib (add HOLE _GND pin 1~16)) Page15:VGA R/G/B signal rise/fall time fail solution and VGA leakage current issue solution Page22:F _USB1/F _USB2 change to 6*2 header for lenovo usb header spec change Page27:add serial resistors for PS/2 KB/MS (lenovo request) Page31:VRD11.1 signal measure solution Page07/Page20:RTC signal measure fail solution Page09/21:follow intel review result Page32/Page33:Reserve damping resistor at gate pin of MOSFET and negative feedback signal of OP
1.0	2009/07/01	page07:change PB12 footprint to 0603 for somkeless issue page25:update LAN Dual Color LED Schematic page26:IT8757 Update ATXPG circuit for 3V level page31:change R113/R112/R116=1R0 ,C98/C102/C106=4700pF for Low side MOS VDS over spec
	2009/07/28	page25:add bom table for lan EFUSE & EEPROM
1.1	2009/08/17	page25:update lan active LED control circuit

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Title: COVER PAGE		
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ICH7 GPIO Table

Name	Type	Voltage	Default	Functional	Function
GPIO6	I/O	+VCC3	GPI	GPI6	CLR_COMS
GPIO10	I/O	+3VSB	GPI	GPI10	LAN DSM function Detect
GPIO23	I/O	+VCC3	LDRQ1#	LDRQ1#	FRONT_AUD_DET
GPIO24	I/O	+3VSB	GPO	GPO24	CPU Variable SET
GPIO28	I/O	+3VSB	GPO	GPO28	
GPIO26	I/O	+3VSB	GPO	GPO26	USBPWR_FR
GPIO27	I/O	+3VSB	GPO	GPO27	USBPWR_RE
GPIO34	I/O	+VCC3	GPO	GPO34	LAN DSM function control
GPIO35	I/O	+VCC3	GPI	GPO35	Chassis ID 1
GPIO39	I/O	+VCC3	GPI	GPO39	Chassis ID 2
GPIO38	I/O	+VCC3	GPI	GPO38	COM1 detect
GPIO8	I/O	+3VSB	GPI	GPI8	COM header detect 0 with com header *1 without com header
GPIO9	I/O	+3VSB	GPI	GPI9	SPDIFOUT header detect 0 with spdifout header *1 without spdifout header

ITE8755 GPIO Table

Name	Type	Voltage	Default	Functional Description	Function
GP25	DIOD8	VCCH	GPO25	GPIO25	Y LED CONTROL
GP26	DIOD8	VCCH	GPO26	GPIO26	G LED CONTROL
GP12	DIOD8	+VCC	PCI Reset 1#	PCI Reset 1# / GPIO 12	WT_BEEP
GP14	DIOD8	+VCC	PECI Request	PECI Request /GPIO14	ICH_THRM_L
GP40	DIOD8	VCCH	3VSBSW#	3VSBSW# / GPIO 40	DIMM_5VDUAL CONTROL

G41 Strapping table

Name	Strapping
SDVO_CTRLDATA sample during reset	1 Enable the digital Port B 0 Disabled the digital Port B(DEFAULT INTERNAL PD)
DDPC_CTRLDATA sample during reset	1 Enable the digital Port C 0 Disabled the digital Port C(DEFAULT INTERNAL PD)
TCEN	TLS Confidentiality Enable(Transport Layer Security Straps) *0 = Disable TLS (DEFAULT) 1 = Enable TLS
ITPM	Integrated TPM Enable 0 = Enable Intel TPM *1 = Disable Intel TPM (DEFAULT)
EXP_SLR	PCI Express* Static Lane Reversal/Form Factor Selection *1 Normal operation (ATX) (DEFAULT) 0 (G)MCH PCI Express lane numbers are reversed (BTX)
EXP_SM	Concurrent PCI Express Port Enable *1 Both SDVO and PCI Express are operating simultaneously via the PCI Express port (DEFAULT) 0 Only SDVO or PCI Express is operational
TP_MF20 (DualX8_Enable)	2x8 PEG Port Bifurcation: *1 1x16 PCI Express Port Enabled(DEFAULT) 0 2x8 PCI Express Ports Enabled

ICH7 Strapping table

Name	Strapping
GPO25 internal pull-up	DMI AC/DC Coupling Selection(Sampled on Rising Edge of RSMRST#) 1 the DMI interface is strapped to operate in DC coupled mode *0 the DMI interface is strapped to operate in AC coupled mode(Default)
GNT5_L : GNT4_L internal pull-up	BOOT BIOS DESTINATION SELECTION(Sampled on rising edge of PWROK) *0 : 1 Flash Cycles Routed to SPI(Default) 1 : 0 Flash Cycles Routed to PCI 1 : 1 Flash Cycles Routed to LPC 0 : 0 Reserved
TP_SF21 (ICH PIN F21:TP3) internal pull-up	XOR Chain Entrance(Sampled on rising edge of PWROK): low enable (This signal should not be pulled low unless using XOR Chain testing.)
ICH_HDSDOUT :bit1 ICH_HDSYNC :bit0 internal pull-down	PCI Express Port Configuration (Sampled on rising edge of PWROK when TP3 is not pulled low at the rising edge of PWROK) 11 = 1 x4, Port 1 (x4) 10 = Reserved 01 = Reserved *00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1), Port 4 (x1)
ICH_INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable *1 Enable 0 Disabled
SPKR internal pull-down	No Reboot mode(ICH7 will disable the TCO Timer system reboot feature) 1 Enable (Sampled on rising edge of PWROK) *0 Disabled

Support HDMI audio table

*

	HDMI Disable	HDMI Enable
HDMIa(Page10)	X	V
HDMIb(Page10)	V	X
HDMIc(Page11)	X	V
HDMId(Page11)	V	X
HDMIe(Page20)	X	V
HDMIf(Page21)	+3VSB	+1P5_SB
HDMIg(Page21)	+VCC3	+ICH_1P5V
HDMIh(Page29)	+VCC3	+ICH_1P5V
HDMIi(Page33)	X	V

PCI ROUTING TABLE

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	18	F/G/H/E	REQ0	GNT0

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Title: GPIO/STRAP

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McCreary(Corporate) ,vPro
Eaglelake Q: Corporate Integrated Graphics

Boulder Creek(consumer) ,VIIV
* Eaglelake G: Consumer Integrated Graphics
Eaglelake P: Consumer Discrete Graphics

PCB	Total Thickness	Core Prepreg
BearLake	62 mil	50 mil
* EagleLake	59 mil	47 mil

PCB:244*224*1.5mm 4L
1080:50 ohm +/-15%(4 mil)

INTEL
LGA 775 pin
Intel P4 Processor Core 2 Duo & Core 2 Quad & Dual Core PAGE 4-6

FSB : 800MHz & Freq : 200MHz
FSB : 1066MHz & Freq : 266MHz
FSB : 1333MHz & Freq : 333MHz

BW : 10GB/s

VGA PAGE 15

HDMI PAGE 14/15

INTEL G41 GMCH PAGE 8-12

DDR3 :800/1066MHz

CHANNEL-A

DIMM1: DDR3 Socket 240P PAGE 16

CHANNEL-B

DIMM2: DDR3 Socket 240P PAGE 17

PCIEx16 PAGE 13

BW : 8G/s @Freq : 100MHz

BW : 2GB/s

INTEL ICH 7 PAGE 18-21

BW : 500MB/s @Freq : 100MHz

PCIE X1_1 PAGE 23

PCIE X1_2 PAGE 23

BW : 500MB/s @Freq : 100MHz

REALTEK 8102EL/8103EL 8111DL PAGE 25

USBLAN RJ45 PAGE 25

PS. USBLAN is RJ45+2 port USB conn

BW : 133MB/s @Freq : 33MHz

PCI Slot 120pin @ AD18 PAGE 24

USB1 2 ports
USB2 2 ports
USBLAN 2 ports
USB X2 2 ports
PAGE 22

BW : 480MB/s @Freq : 48MHz

USB 2.0

Line In
Line Out
Mic In
SPDIF OUT
PAGE 30

HD Audio Codec ALC662 PAGE 29

SPI ROM PAGE 23

ITE 8755 Super I/O 64pin PAGE 26

PS2 KB/MS PAGE 27

SATA1 7Pin
SATA2 7pin
SATA3 7Pin
SATA4 7pin
PAGE 19

SATA-II
BW : 3G/s

COM PAGE 27

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Title: **System Block Diagram**

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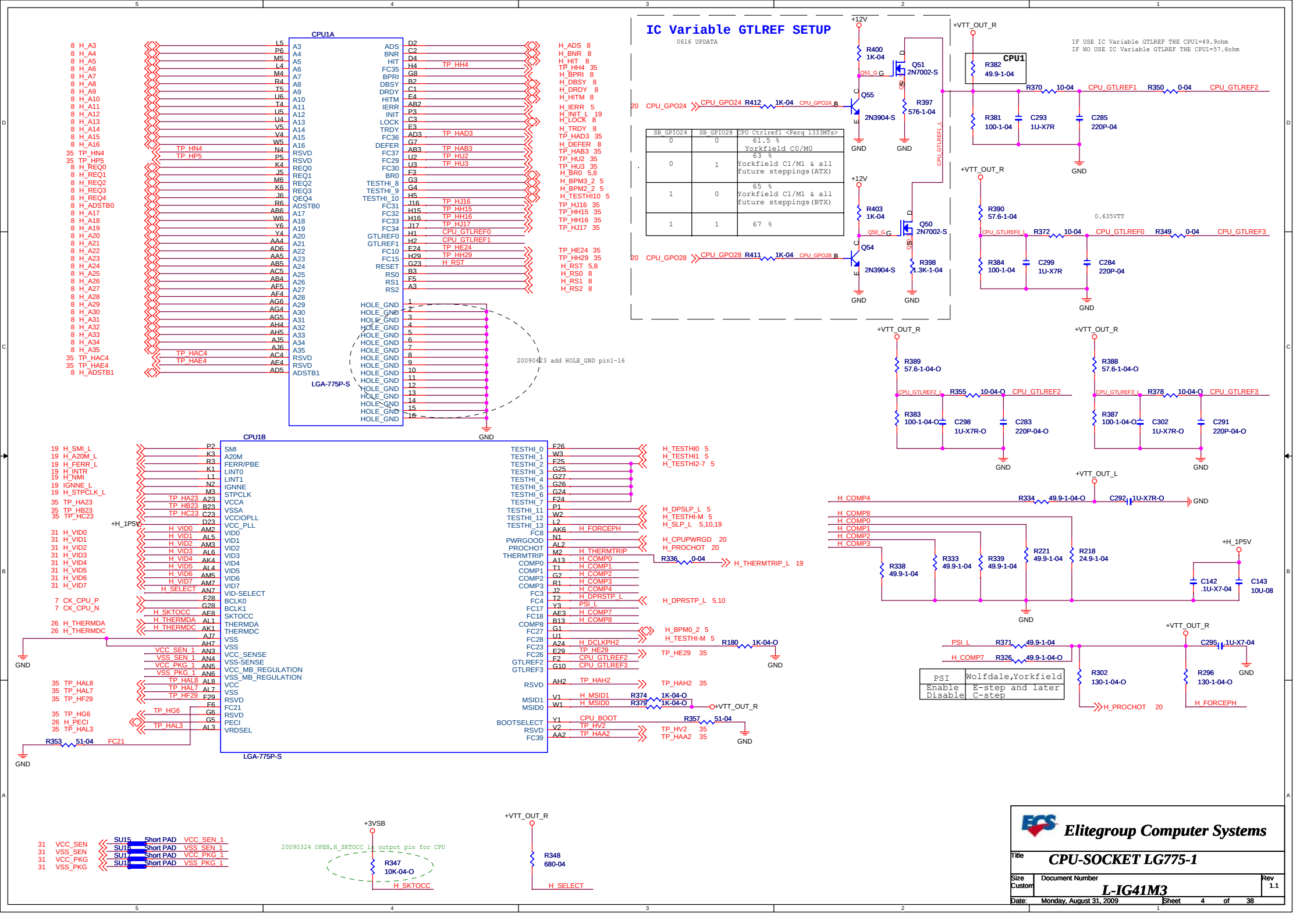
IC Variable GTLREF SETUP
0616 UPDATA
IF USE IC Variable GTLREF THE CPU1=49.9ohm
IF NO USE IC Variable GTLREF THE CPU1=57.6ohm
SB_GPIO24 | SB_GPIO28 | CPU Ctrlref1 <Ferq 1333MTs>
0 | 0 | 61.5 % Yorkfield C0/M0
0 | 1 | 63 % Yorkfield C1/M1 & all future steppings(ATX)
1 | 0 | 65 % Yorkfield C1/M1 & all future steppings(BTX)
1 | 1 | 67 %
CPU1A
LGA-775P-S
20090423 add HOLE_GND pin1~16
CPU1B
LGA-775P-S
PSI | Wolfdale,Yorkfield
Enable | E-step and later
Disable | C-step
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CPU-SOCKET LG775-1
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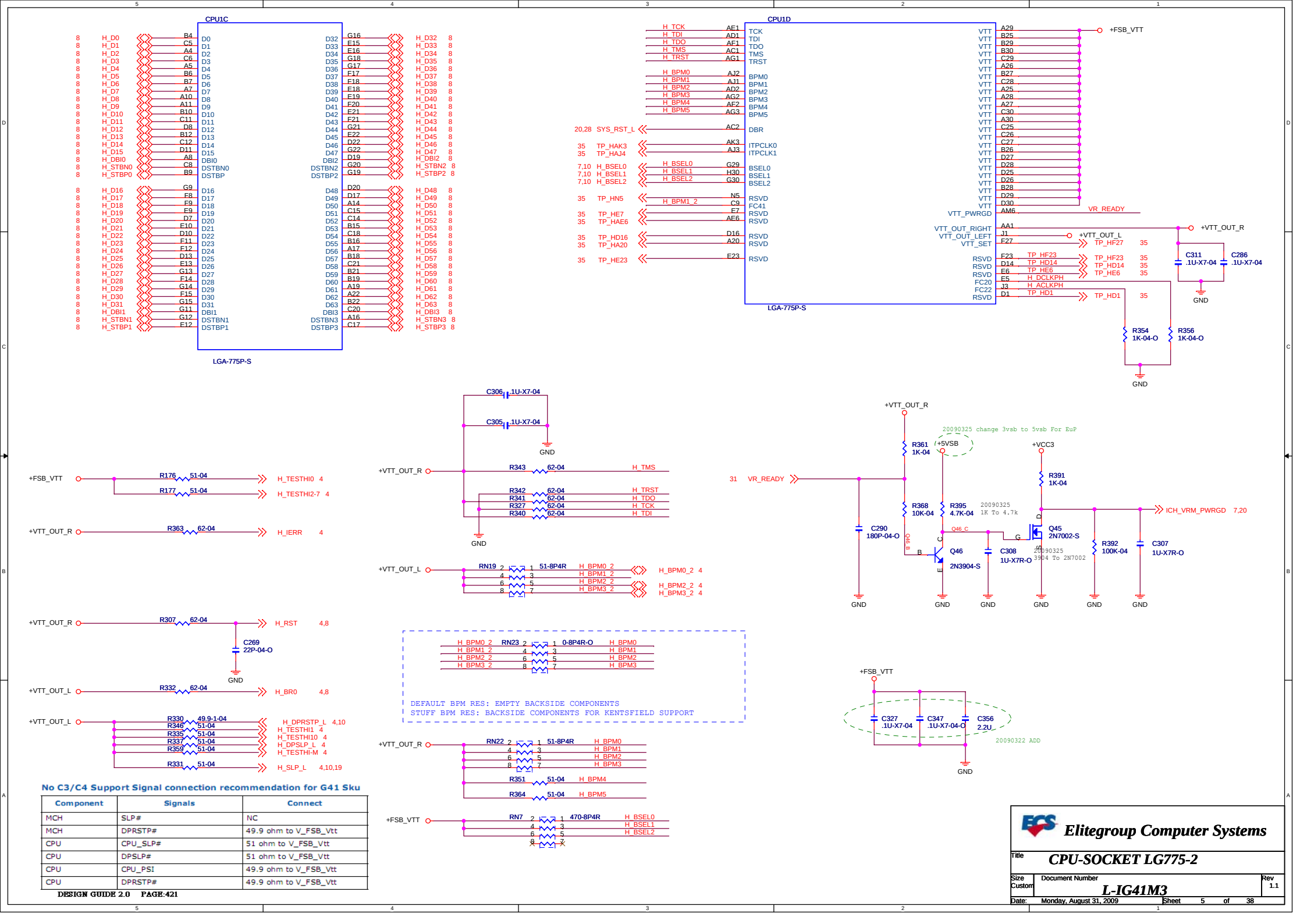

No C3/C4 Support Signal connection recommendation for G41 Sku

Component	Signals	Connect
MCH	SLP#	NC
MCH	DPRSTP#	49.9 ohm to V_FSB_Vtt
CPU	CPU_SLP#	51 ohm to V_FSB_Vtt
CPU	DPSLP#	51 ohm to V_FSB_Vtt
CPU	CPU_PSI	49.9 ohm to V_FSB_Vtt
CPU	DPRSTP#	49.9 ohm to V_FSB_Vtt

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Title: CPU-SOCKET LG775-2

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CPU

MCH(FSB)

MCH(PCIE)

MCH(VGA)

LAN

ICH(SATA)

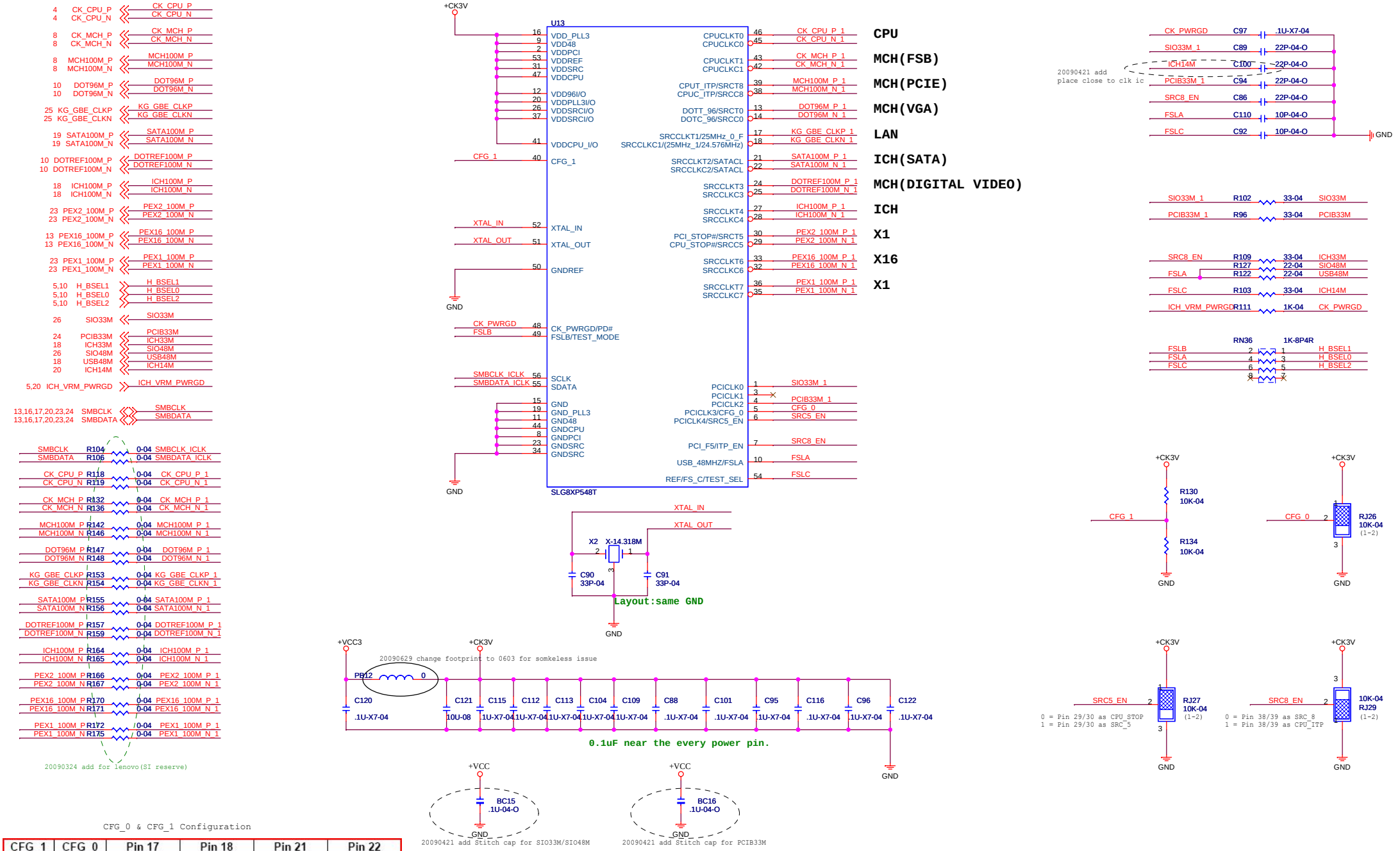
MCH(DIGITAL VIDEO)

ICH

X1

X16

X1



CFG_0 & CFG_1 Configuration

CFG_1	CFG_0	Pin 17	Pin 18	Pin 21	Pin 22
Low	Low	25MHz_0_F	25MHz_1	SRC_2	SRC_2#
Mid	Low	SRC_1	SRC_1#	SRC_2	SRC_2#
High	Low	25MHz_0_F	24.576MHz	SRC_2	SRC_2#
Low	High	25MHz_0_F	25MHz_1	SATA	SATA#
Mid	High	SRC_1	SRC_1#	SATA	SATA#
High	High	25MHz_0_F	24.576MHz	SATA	SATA#

Voltage Threshold for CFG_1 (tri-level input)

State	Min	Typical	Max
Low	0V	0.55V	0.9V
Mid	1.3V	1.65V	2.0V
High	2.4V	2.75V	VDD

Bit2 FSLC	Bit1 FSLB	Bit0 FSLA	CPU CLOCK (MHZ)	CPU FSB CLOCK
0	0	0	266.66	FSB 1066
0	0	1	133.33	
0	1	0	200.00	FSB 800
0	1	1	166.66	
1	0	0	333.33	FSB 1333
1	0	1	100.00	
1	1	0	400.00	

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Title: SLG8XP548T(CK505)

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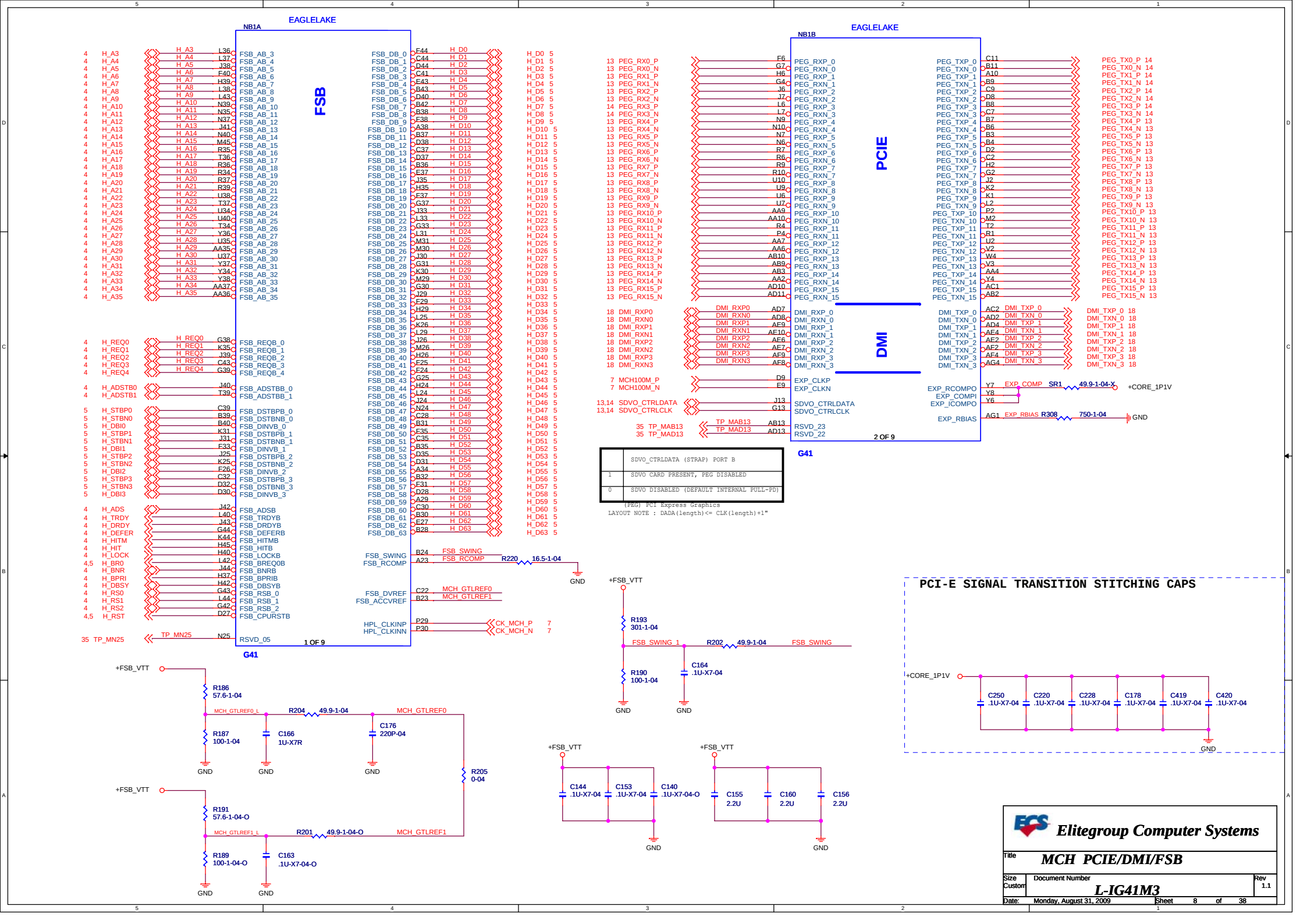
EAGLELAKE
NB1A
FSB
1 OF 9
G41
EAGLELAKE
NB1B
PCIE
DMI
2 OF 9
G41
SDVO_CTRLDATA (STRAP) PORT B
1 SDVO CARD PRESENT, PEG DISABLED
0 SDVO DISABLED (DEFAULT INTERNAL PULL-PD)
(PEG) PCI Express Graphics
LAYOUT NOTE : DADA(length)<= CLK(length)+1"
PCI-E SIGNAL TRANSITION STITCHING CAPS
+CORE_1P1V
C250 .1U-X7-04
C220 .1U-X7-04
C228 .1U-X7-04
C178 .1U-X7-04
C419 .1U-X7-04
C420 .1U-X7-04
GND
+FSB_VTT
R186 57.6-1-04
R187 100-1-04
C166 1U-X7R
C176 220P-04
R204 49.9-1-04
R205 0-04
R191 57.6-1-04-O
R189 100-1-04-O
C163 .1U-X7-04-O
R201 49.9-1-04-O
R193 301-1-04
R190 100-1-04
C164 .1U-X7-04
R202 49.9-1-04
C144 .1U-X7-04
C153 .1U-X7-04
C140 .1U-X7-04-O
C155 2.2U
C160 2.2U
C156 2.2U
R220 16.5-1-04
R308 750-1-04
SR1 49.9-1-04-X
Elitegroup Computer Systems
Title MCH PCIE/DMI/FSB
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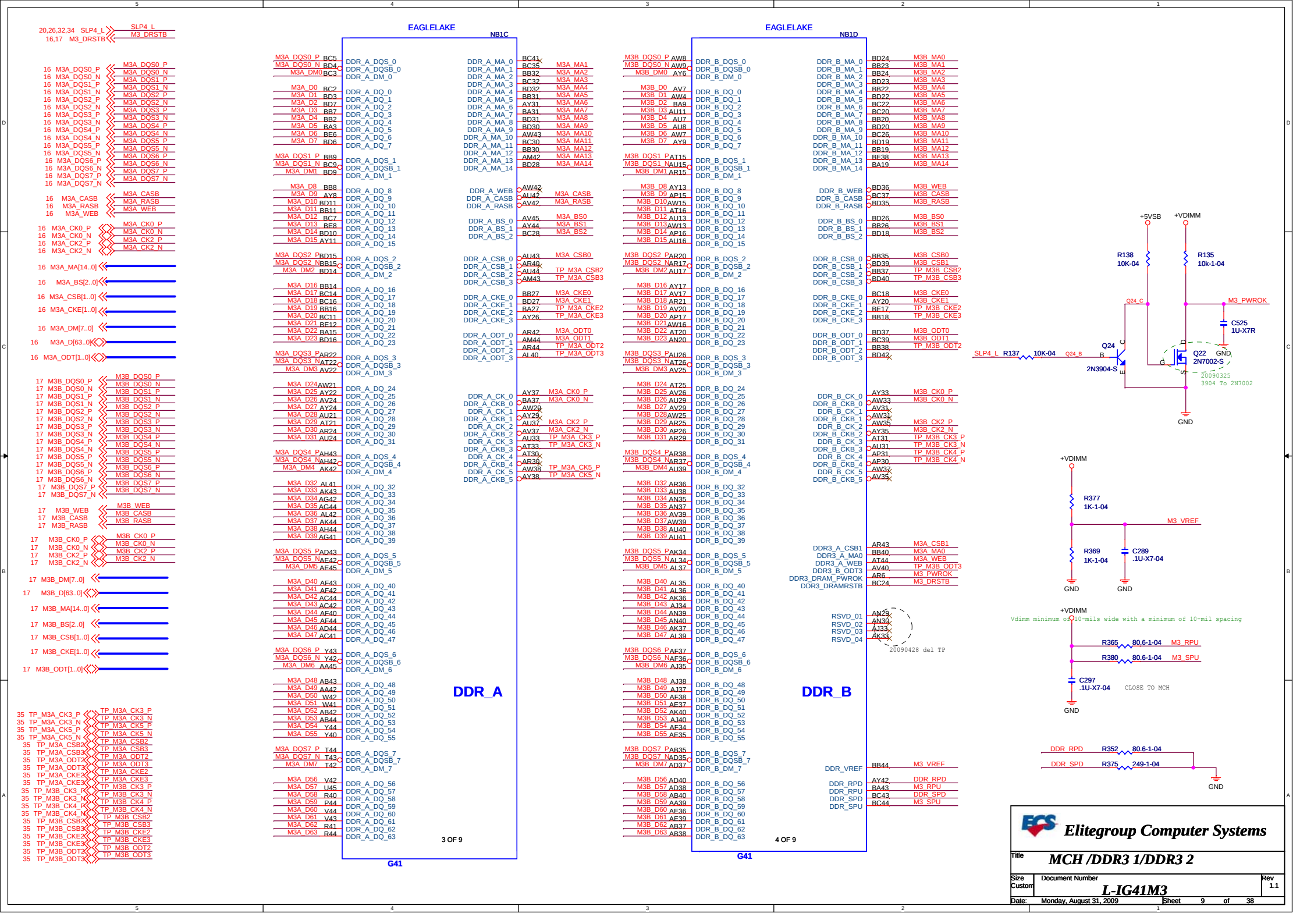

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Title	MCH /DDR3 1/DDR3 2	
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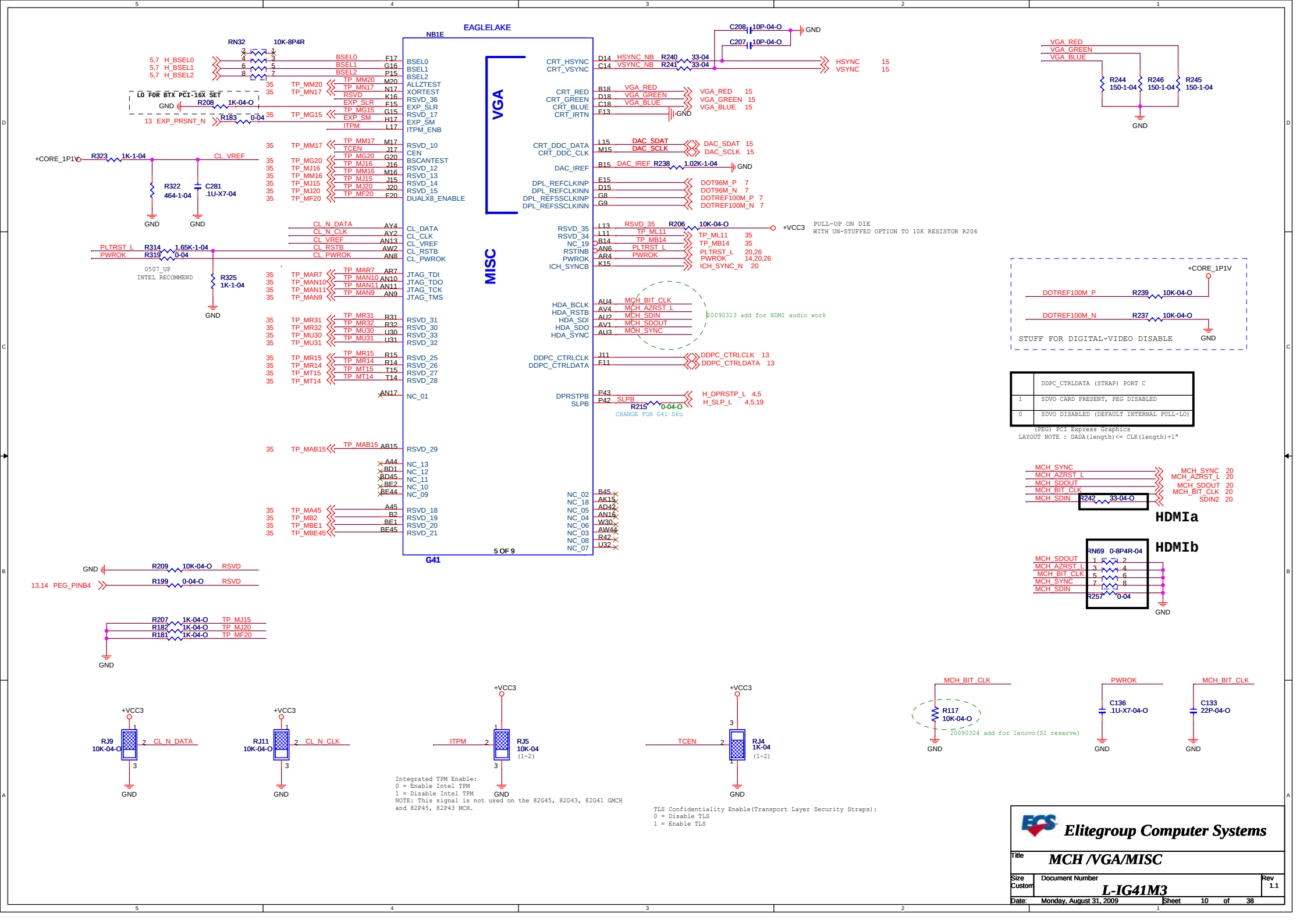
EAGLELAKE
NB1E
G41
5 OF 9
VGA
MISC
RN32 10K-8P4R
LO FOR BTX PCI-16X SET
R208 1K-04-O
R183 0-04
R323 1K-1-04
R322 464-1-04
C281 .1U-X7-04
R314 1.65K-1-04
R319 0-04
R325 1K-1-04
0507_UP
INTEL RECOMMEND
R209 10K-04-O RSVD
R199 0-04-O RSVD
R207 1K-04-O TP_MJ15
R182 1K-04-O TP_MJ20
R181 1K-04-O TP_MF20
C208 10P-04-O
C207 10P-04-O
R240 33-04
R241 33-04
R244 150-1-04
R246 150-1-04
R245 150-1-04
R238 1.02K-1-04
R206 10K-04-O
PULL-UP ON DIE
WITH UN-STUFFED OPTION TO 10K RESISTOR R206
R239 10K-04-O
R237 10K-04-O
STUFF FOR DIGITAL-VIDEO DISABLE
20090313 add for HDMI audio work
R215 0-04-O
CHANGE FOR G41 Sku
DDPC_CTRLDATA (STRAP) PORT C
1 SDVO CARD PRESENT, PEG DISABLED
0 SDVO DISABLED (DEFAULT INTERNAL PULL-LO)
(PEG) PCI Express Graphics
LAYOUT NOTE : DADA(length)<= CLK(length)+1"
R242 33-04-O
HDMIa
RN69 0-8P4R-04
R257 0-04
HDMIb
RJ9 10K-04-O
RJ11 10K-04-O
RJ5 10K-04
(1-2)
RJ4 1K-04
(1-2)
Integrated TPM Enable:
0 = Enable Intel TPM
1 = Disable Intel TPM
NOTE: This signal is not used on the 82G45, 82G43, 82G41 GMCH
and 82P45, 82P43 MCH.
TLS Confidentiality Enable(Transport Layer Security Straps):
0 = Disable TLS
1 = Enable TLS
R117 10K-04-O
20090324 add for lenovo(SI reserve)
C136 .1U-X7-04-O
C133 22P-04-O
Elitegroup Computer Systems
Title MCH /VGA/MISC
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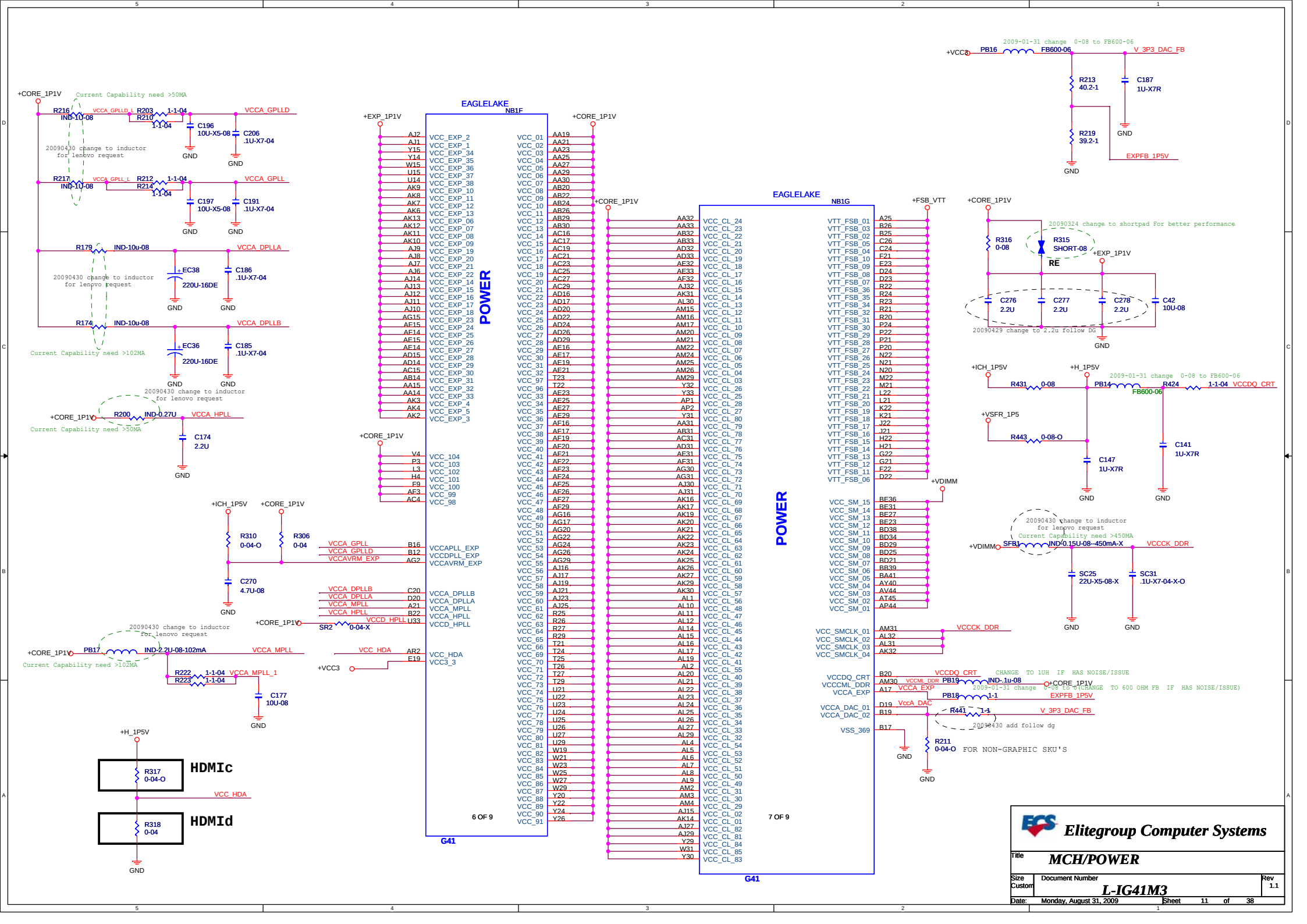
+CORE_1P1V
Current Capability need >50MA
R216 IND-1U-08
VCCA_GPLLD_L
R203 1-1-04
R210 1-1-04
VCCA_GPLLD
C196 10U-X5-08
C206 .1U-X7-04
GND
20090430 change to inductor for lenovo request
R217 IND-1U-08
VCCA_GPLL_L
R212 1-1-04
R214 1-1-04
VCCA_GPLL
C197 10U-X5-08
C191 .1U-X7-04
R179 IND-10u-08
VCCA_DPLLA
EC38 220U-16DE
C186 .1U-X7-04
R174 IND-10u-08
VCCA_DPLLB
Current Capability need >102MA
EC36 220U-16DE
C185 .1U-X7-04
R200 IND-0.27U
VCCA_HPLL
Current Capability need >50MA
C174 2.2U
+ICH_1P5V
R310 0-04-O
R306 0-04
C270 4.7U-08
VCCA_GPLL
VCCA_GPLLD
VCCAVRM_EXP
VCCAPLL_EXP
VCCDPLL_EXP
VCCAVRM_EXP
VCCA_DPLLB
VCCA_DPLLA
VCCA_MPLL
VCCA_HPLL
VCCD_HPLL
SR2 0-04-X
PB17 IND-2.2U-08-102mA
VCCA_MPLL
Current Capability need >102MA
R222 1-1-04
R223 1-1-04
VCCA_MPLL_1
C177 10U-08
+H_1P5V
R317 0-04-O
HDMIc
VCC_HDA
R318 0-04
HDMId
+EXP_1P1V
EAGLELAKE
NB1F
POWER
6 OF 9
G41
VCC_EXP_2
VCC_EXP_1
VCC_EXP_34
VCC_EXP_35
VCC_EXP_36
VCC_EXP_37
VCC_EXP_38
VCC_EXP_10
VCC_EXP_11
VCC_EXP_12
VCC_EXP_13
VCC_EXP_06
VCC_EXP_07
VCC_EXP_08
VCC_EXP_09
VCC_EXP_19
VCC_EXP_20
VCC_EXP_21
VCC_EXP_22
VCC_EXP_14
VCC_EXP_15
VCC_EXP_16
VCC_EXP_17
VCC_EXP_18
VCC_EXP_23
VCC_EXP_24
VCC_EXP_25
VCC_EXP_26
VCC_EXP_27
VCC_EXP_28
VCC_EXP_29
VCC_EXP_30
VCC_EXP_31
VCC_EXP_32
VCC_EXP_33
VCC_EXP_4
VCC_EXP_5
VCC_EXP_3
VCC_104
VCC_103
VCC_102
VCC_101
VCC_100
VCC_99
VCC_98
VCC_01
VCC_02
VCC_03
VCC_04
VCC_05
VCC_06
VCC_07
VCC_08
VCC_09
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_43
VCC_44
VCC_45
VCC_46
VCC_47
VCC_48
VCC_49
VCC_50
VCC_51
VCC_52
VCC_53
VCC_54
VCC_55
VCC_56
VCC_57
VCC_58
VCC_59
VCC_60
VCC_61
VCC_62
VCC_63
VCC_64
VCC_65
VCC_66
VCC_69
VCC_70
VCC_71
VCC_72
VCC_73
VCC_74
VCC_75
VCC_76
VCC_77
VCC_78
VCC_79
VCC_80
VCC_81
VCC_82
VCC_83
VCC_84
VCC_85
VCC_86
VCC_87
VCC_88
VCC_89
VCC_90
VCC_91
+CORE_1P1V
VCC_CL_24
VCC_CL_23
VCC_CL_22
VCC_CL_21
VCC_CL_20
VCC_CL_19
VCC_CL_18
VCC_CL_17
VCC_CL_16
VCC_CL_15
VCC_CL_14
VCC_CL_13
VCC_CL_12
VCC_CL_11
VCC_CL_10
VCC_CL_09
VCC_CL_08
VCC_CL_07
VCC_CL_06
VCC_CL_05
VCC_CL_04
VCC_CL_03
VCC_CL_26
VCC_CL_25
VCC_CL_28
VCC_CL_27
VCC_CL_80
VCC_CL_79
VCC_CL_78
VCC_CL_77
VCC_CL_76
VCC_CL_75
VCC_CL_74
VCC_CL_73
VCC_CL_72
VCC_CL_71
VCC_CL_70
VCC_CL_69
VCC_CL_68
VCC_CL_67
VCC_CL_66
VCC_CL_65
VCC_CL_64
VCC_CL_63
VCC_CL_62
VCC_CL_61
VCC_CL_60
VCC_CL_59
VCC_CL_58
VCC_CL_57
VCC_CL_56
VCC_CL_48
VCC_CL_47
VCC_CL_46
VCC_CL_45
VCC_CL_44
VCC_CL_43
VCC_CL_42
VCC_CL_41
VCC_CL_55
VCC_CL_40
VCC_CL_39
VCC_CL_38
VCC_CL_37
VCC_CL_36
VCC_CL_35
VCC_CL_34
VCC_CL_33
VCC_CL_32
VCC_CL_54
VCC_CL_53
VCC_CL_52
VCC_CL_51
VCC_CL_50
VCC_CL_49
VCC_CL_31
VCC_CL_30
VCC_CL_29
VCC_CL_02
VCC_CL_01
VCC_CL_82
VCC_CL_81
VCC_CL_84
VCC_CL_85
VCC_CL_83
+FSB_VTT
VTT_FSB_01
VTT_FSB_03
VTT_FSB_02
VTT_FSB_05
VTT_FSB_04
VTT_FSB_10
VTT_FSB_09
VTT_FSB_08
VTT_FSB_07
VTT_FSB_36
VTT_FSB_35
VTT_FSB_34
VTT_FSB_32
VTT_FSB_31
VTT_FSB_30
VTT_FSB_29
VTT_FSB_28
VTT_FSB_27
VTT_FSB_26
VTT_FSB_25
VTT_FSB_24
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VTT_FSB_22
VTT_FSB_21
VTT_FSB_20
VTT_FSB_19
VTT_FSB_18
VTT_FSB_17
VTT_FSB_16
VTT_FSB_15
VTT_FSB_14
VTT_FSB_13
VTT_FSB_12
VTT_FSB_11
VTT_FSB_06
+VDIMM
VCC_SM_15
VCC_SM_14
VCC_SM_13
VCC_SM_12
VCC_SM_11
VCC_SM_10
VCC_SM_09
VCC_SM_08
VCC_SM_07
VCC_SM_06
VCC_SM_05
VCC_SM_04
VCC_SM_03
VCC_SM_02
VCC_SM_01
VCC_SMCLK_01
VCC_SMCLK_02
VCC_SMCLK_03
VCC_SMCLK_04
VCCDQ_CRT
VCCCML_DDR
VCCA_EXP
VCCA_DAC_01
VCCA_DAC_02
VSS_369
7 OF 9
G41
+VCC3
PB16 FB600-06
2009-01-31 change 0-08 to FB600-06
V_3P3_DAC_FB
R213 40.2-1
C187 1U-X7R
R219 39.2-1
EXPFB_1P5V
20090324 change to shortpad For better performance
R316 0-08
R315 SHORT-08
RE
C276 2.2U
C277 2.2U
C278 2.2U
C42 10U-08
20090429 change to 2.2u follow DG
+ICH_1P5V
+H_1P5V
R431 0-08
PB14 FB600-06
R424 1-1-04
VCCDQ_CRT
+VSFR_1P5
R443 0-08-O
C147 1U-X7R
C141 1U-X7R
SFB1 IND-0.15U-08-450mA-X
VCCCK_DDR
SC25 22U-X5-08-X
SC31 .1U-X7-04-X-O
CHANGE TO 1UH IF HAS NOISE/ISSUE
PB19 IND-.1u-08
2009-01-31 change 0-08 to 0ICHANGE TO 600 OHM FB IF HAS NOISE/ISSUE)
PB18 1-1
EXPFB_1P5V
R441 1-1
V_3P3_DAC_FB
20090430 add follow dg
R211 0-04-O FOR NON-GRAPHIC SKU'S
Elitegroup Computer Systems
MCH/POWER
L-IG41M3
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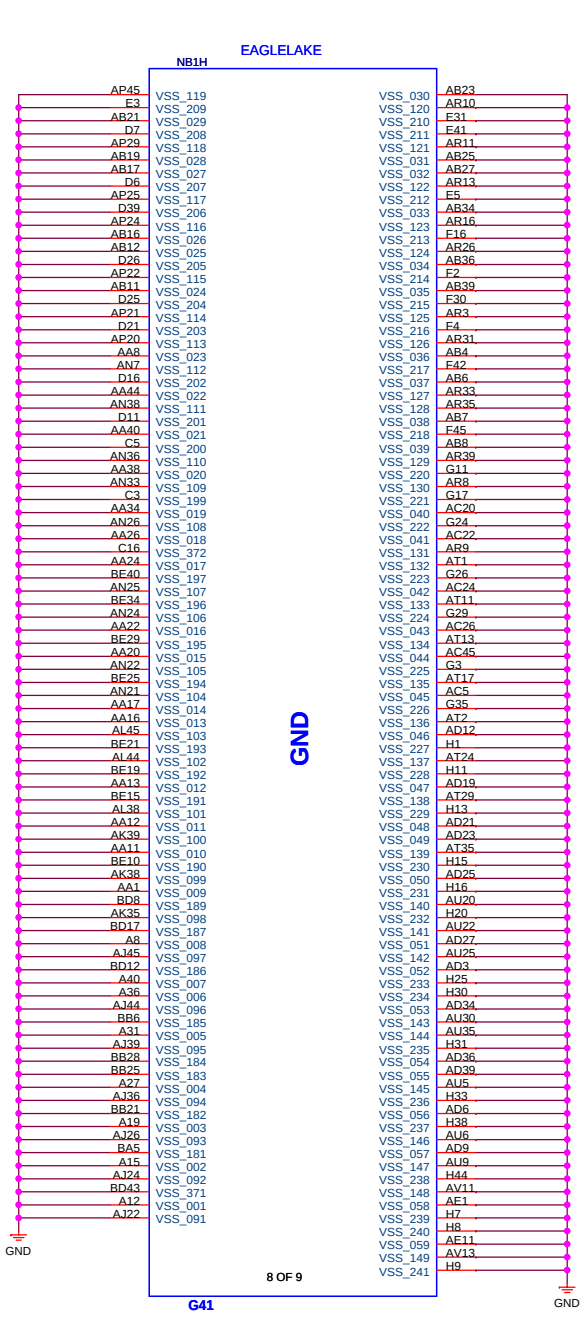
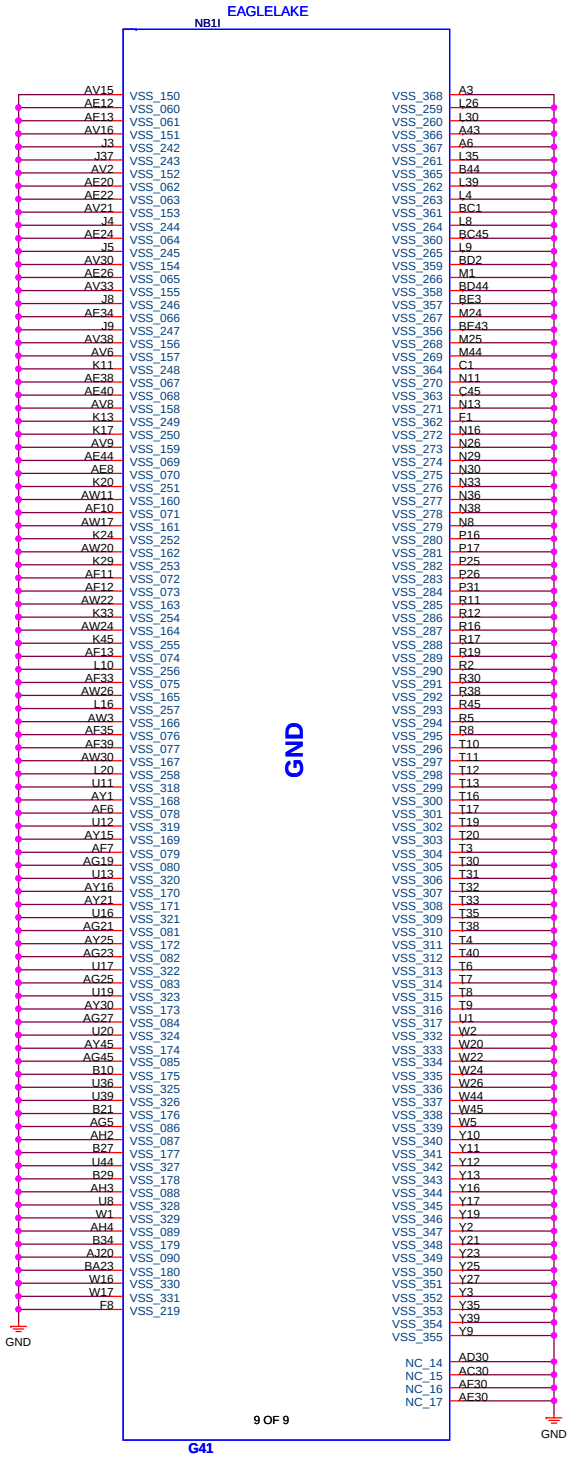
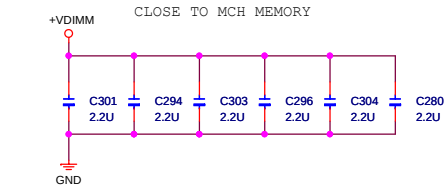
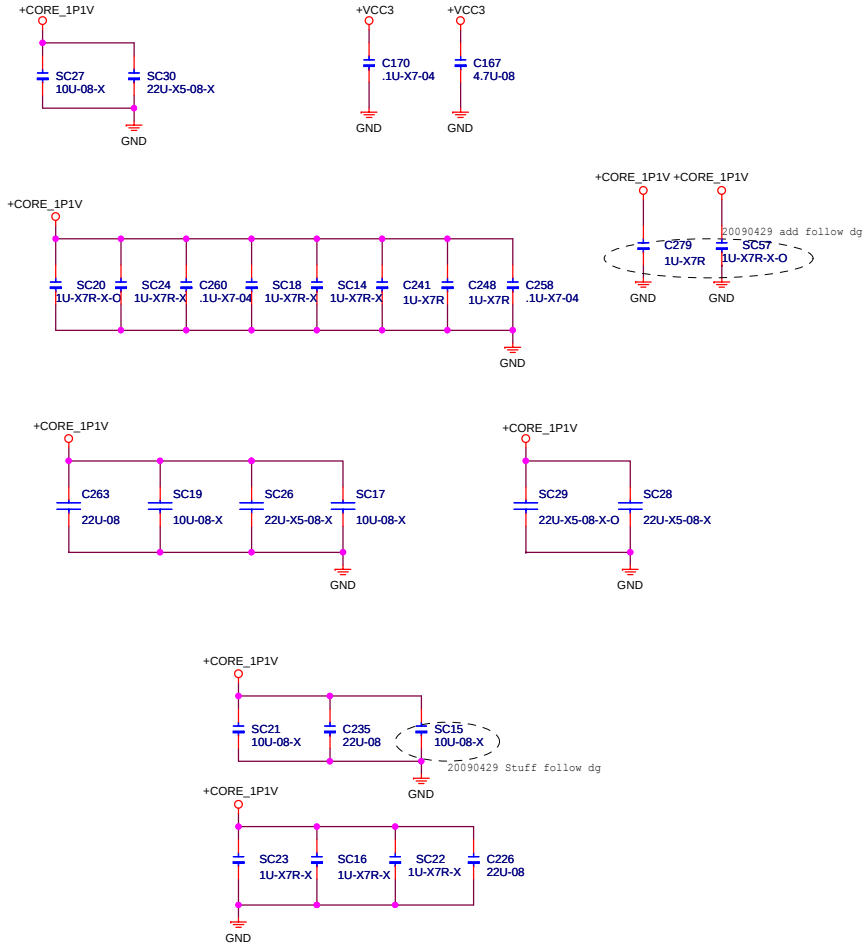






ME DECOUPLING



Elitegroup Computer Systems		
Title: MCH /GND		
Size: Custom	Document Number: L-IG41M3	Rev: 1.1
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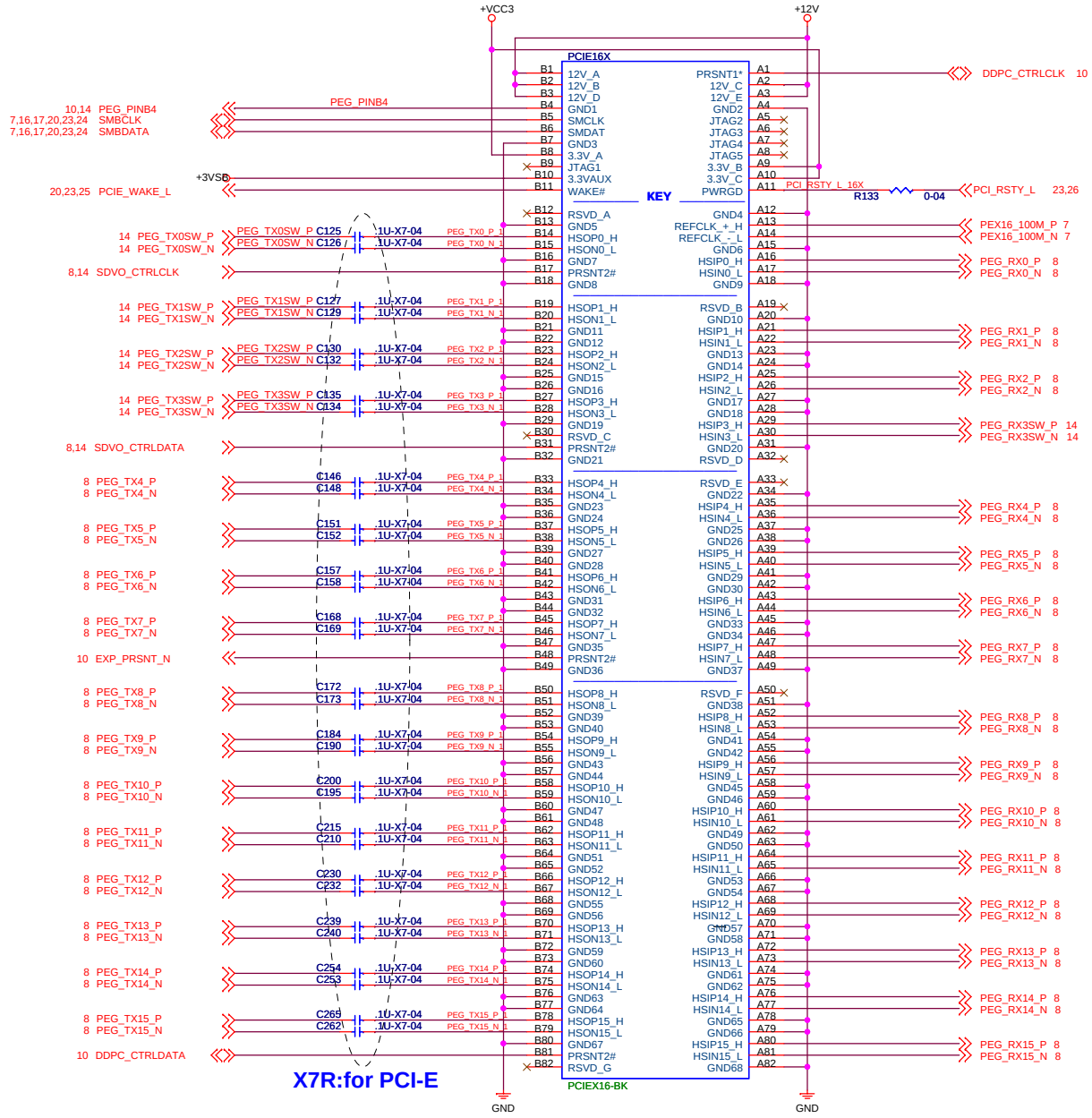
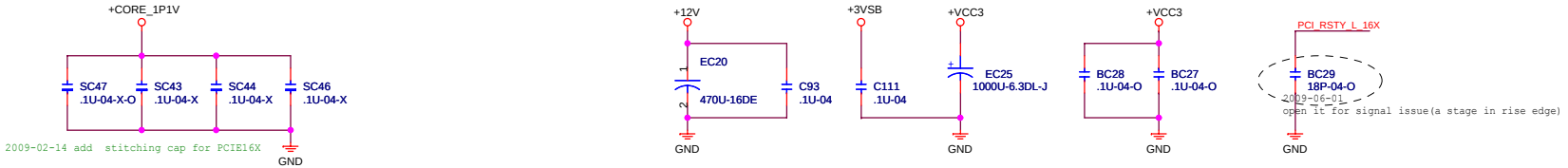


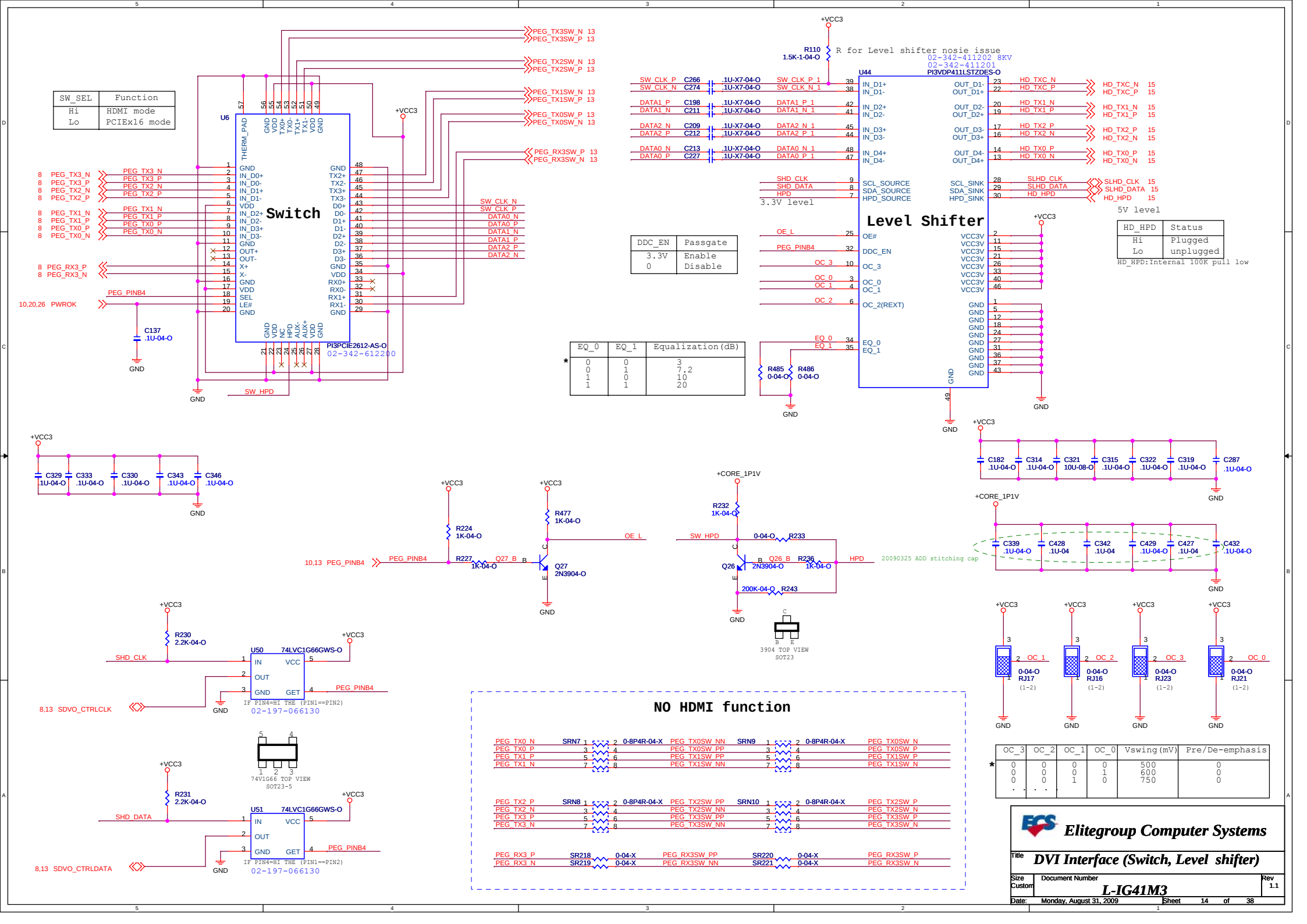


Elitegroup Computer Systems

Title: PCIE 16X

Size: Custom | Document Number: L-IG41M3 | Rev: 1.1

Date: Monday, August 31, 2009 | Sheet 13 of 38


SW_SEL | Function
Hi | HDMI mode
Lo | PCIEx16 mode
U6
Switch
PI3PCIE2612-AS-O
02-342-612200
SW_HPD
C137 .1U-04-O
PEG_PINB4
10,20,26 PWROK
R110 1.5K-1-04-O
R for Level shifter nosie issue
02-342-411202 8KV
02-342-411201
U44
PI3VDP411LSTZDES-O
Level Shifter
3.3V level
5V level
DDC_EN | Passgate
3.3V | Enable
0 | Disable
EQ_0 | EQ_1 | Equalization(dB)
0 | 0 | 3
0 | 1 | 7.2
1 | 0 | 10
1 | 1 | 20
HD_HPD | Status
Hi | Plugged
Lo | unplugged
HD_HPD:Internal 100K pull low
R224 1K-04-O
R227 1K-04-O
R477 1K-04-O
Q27 2N3904-O
R232 1K-04-O
R233 0-04-O
Q26 2N3904-O
R236 1K-04-O
R243 200K-04-O
HPD
20090325 ADD stitching cap
3904 TOP VIEW
SOT23
R230 2.2K-04-O
R231 2.2K-04-O
U50 74LVC1G66GWS-O
U51 74LVC1G66GWS-O
74V1G66 TOP VIEW
SOT23-5
IF PIN4=HI THE (PIN1==PIN2)
02-197-066130
8,13 SDVO_CTRLCLK
8,13 SDVO_CTRLDATA
NO HDMI function
SRN7 SRN8 SRN9 SRN10 0-8P4R-04-X
SR218 SR219 SR220 SR221 0-04-X
OC_3 | OC_2 | OC_1 | OC_0 | Vswing(mV) | Pre/De-emphasis
0 | 0 | 0 | 0 | 500 | 0
0 | 0 | 0 | 1 | 600 | 0
0 | 0 | 1 | 0 | 750 | 0
Elitegroup Computer Systems
Title
DVI Interface (Switch, Level shifter)
Size Custom
Document Number
L-IG41M3
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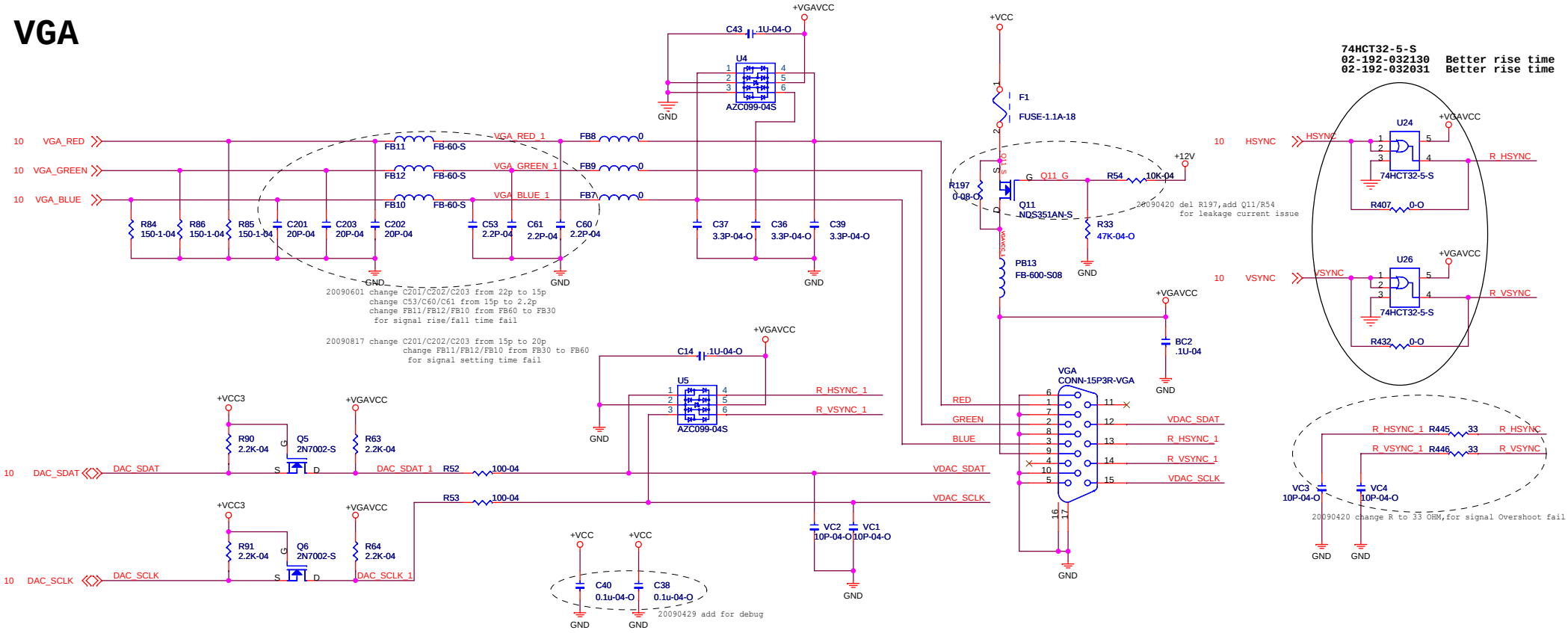
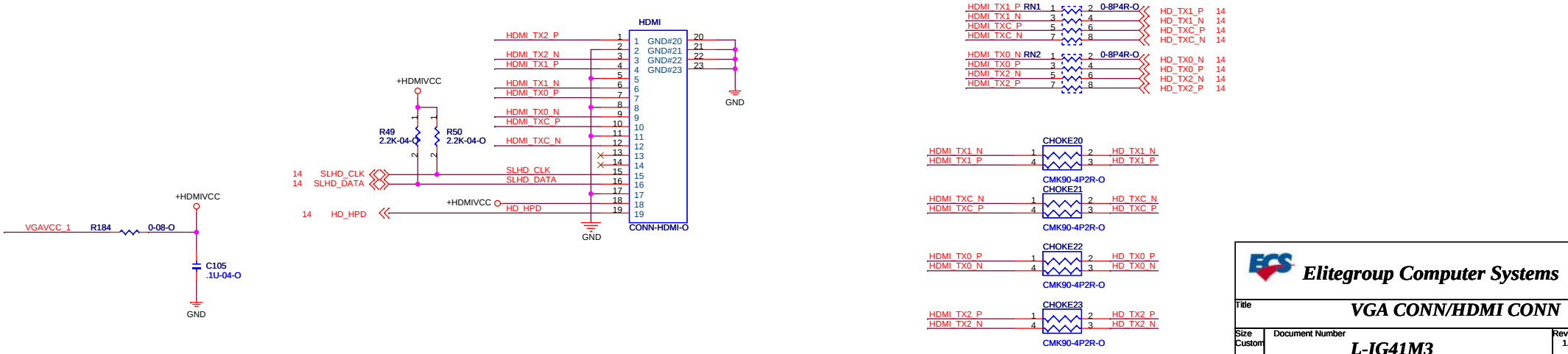
VGA



HDMI

20090313 ADD



Elitegroup Computer Systems			
Title	VGA CONN/HDMI CONN		
Size: Custom	Document Number: L-IG41M3		Rev: 1.1
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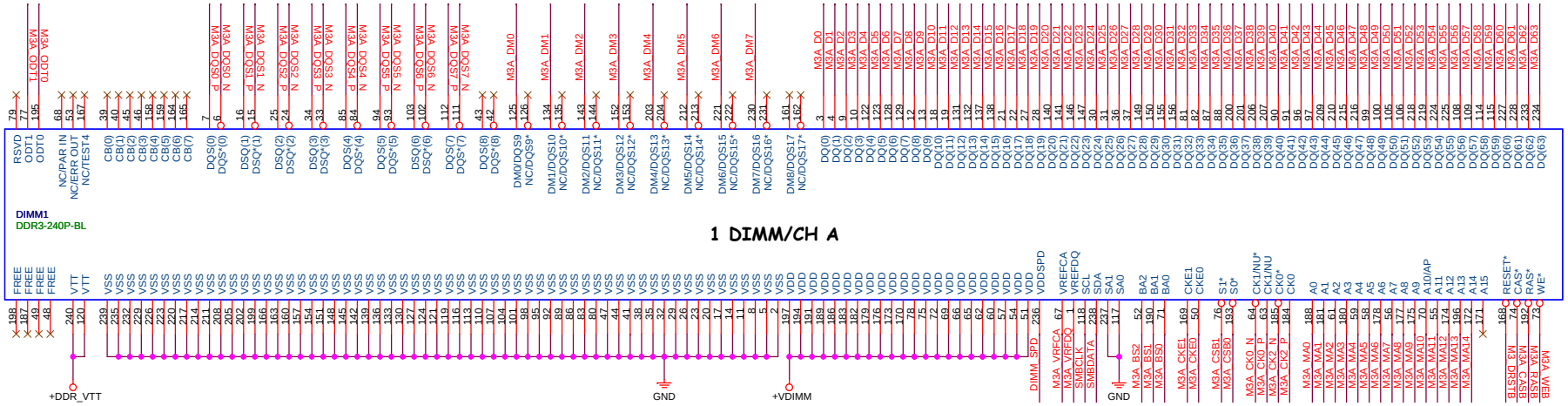


9 M3A_D[63..0]
9 M3A_DM[7..0]
9 M3A_MA[14..0]
9 M3A_BS[2..0]
9 M3A_CKE[1..0]
9 M3A_CSB[1..0]
9 M3A_ODT[1..0]

9 M3A_DQS7_N — M3A_DQS7_N
9 M3A_DQS7_P — M3A_DQS7_P
9 M3A_DQS6_N — M3A_DQS6_N
9 M3A_DQS6_P — M3A_DQS6_P
9 M3A_DQS5_N — M3A_DQS5_N
9 M3A_DQS5_P — M3A_DQS5_P
9 M3A_DQS4_N — M3A_DQS4_N
9 M3A_DQS4_P — M3A_DQS4_P
9 M3A_DQS3_N — M3A_DQS3_N
9 M3A_DQS3_P — M3A_DQS3_P
9 M3A_DQS2_N — M3A_DQS2_N
9 M3A_DQS2_P — M3A_DQS2_P
9 M3A_DQS1_N — M3A_DQS1_N
9 M3A_DQS1_P — M3A_DQS1_P
9 M3A_DQS0_N — M3A_DQS0_N
9 M3A_DQS0_P — M3A_DQS0_P

9 M3A_CK2_P — M3A_CK2_P
9 M3A_CK2_N — M3A_CK2_N
9 M3A_CK0_P — M3A_CK0_P
9 M3A_CK0_N — M3A_CK0_N

9 M3A_WEB — M3A_WEB
9 M3A_RASB — M3A_RASB
9 M3A_CASB — M3A_CASB
9,17 M3_DRSTB — M3_DRSTB

17 DIMM_SPD — DIMM_SPD

7,13,17,20,23,24 SMBCLK — SMBCLK
7,13,17,20,23,24 SMBDATA — SMBDATA

2009-01-27 :
Each DIMM must have 4 x 1.0 UF capacitors
placed as close to the DIMM power pins as possible

+VDIMM
BC62 1U
BC65 1U
BC67 1U
BC63 1U
EC52 470U-6.3DE
GND

2009-01-27 :
Each Dimm must have a set of 0.1UF & 4.7UF caps
placed as close to the DIMMs *V_SM_VTT pins as
possible

+DDR_VTT
BC66 4.7U-08
BC68 .1U-04
GND

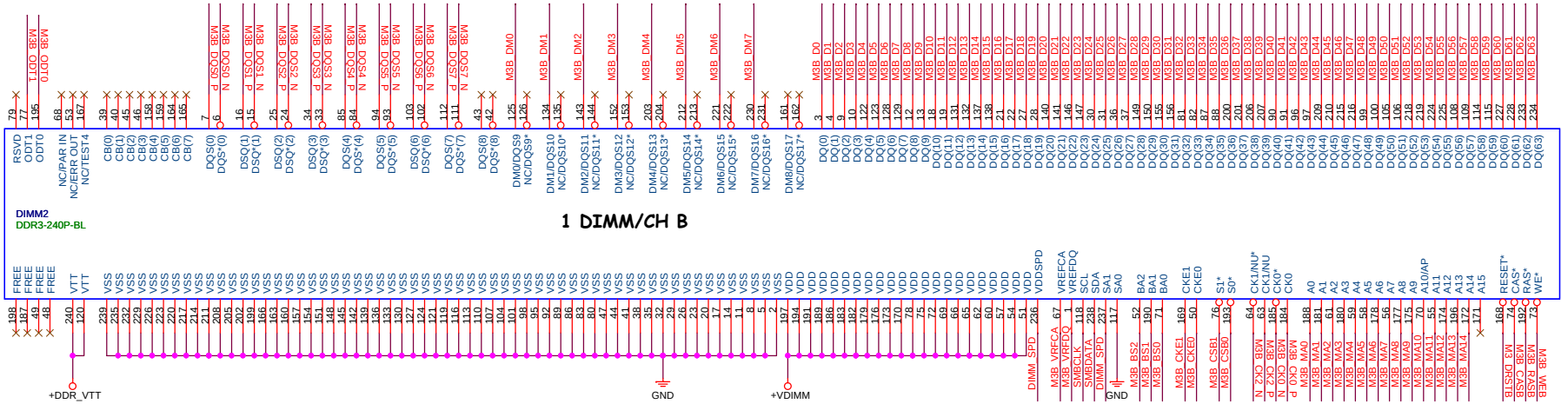
DIMM_SPD
C345 .1U-04
PLACE NEAR PIN 236 OF DIMM
GND

+VDIMM
R188 1K-1-04
C373 .1U-04-O
R192 1K-1-04
C159 10U-08
20090425 change to 10u for DC issue
M3A_VRFCA
GND GND GND

+VDIMM
R194 1K-1-04
C397 .1U-04-O
R195 1K-1-04
C165 .1U-04
M3A_VRFDQ
GND GND GND

Elitegroup Computer Systems

Title	240P DDR3, CHA	
Size: Custom	Document Number: L-IG41M3	Rev: 1.1
Date: Monday, August 31, 2009	Sheet 16 of 38	



9 M3B_ODT[1..0]
9 M3B_CSB[1..0]
9 M3B_CKE[1..0]
9 M3B_BS[2..0]
9 M3B_DM[7..0]
9 M3B_D[63..0]
9 M3B_MA[14..0]

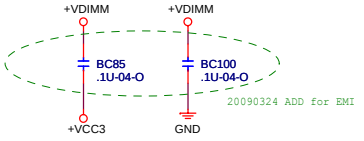
9 M3B_DQS7_N — M3B_DQS7_N
9 M3B_DQS7_P — M3B_DQS7_P
9 M3B_DQS6_N — M3B_DQS6_N
9 M3B_DQS6_P — M3B_DQS6_P
9 M3B_DQS5_N — M3B_DQS5_N
9 M3B_DQS5_P — M3B_DQS5_P
9 M3B_DQS4_N — M3B_DQS4_N
9 M3B_DQS4_P — M3B_DQS4_P
9 M3B_DQS3_N — M3B_DQS3_N
9 M3B_DQS3_P — M3B_DQS3_P
9 M3B_DQS2_N — M3B_DQS2_N
9 M3B_DQS2_P — M3B_DQS2_P
9 M3B_DQS1_N — M3B_DQS1_N
9 M3B_DQS1_P — M3B_DQS1_P
9 M3B_DQS0_N — M3B_DQS0_N
9 M3B_DQS0_P — M3B_DQS0_P

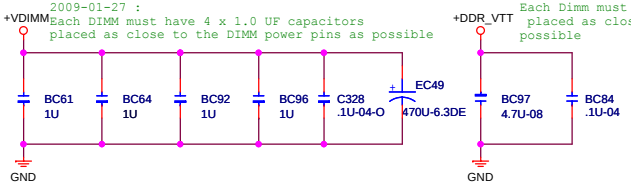
9 M3B_CK0_P — M3B_CK0_P
9 M3B_CK0_N — M3B_CK0_N
9 M3B_CK2_P — M3B_CK2_P
9 M3B_CK2_N — M3B_CK2_N

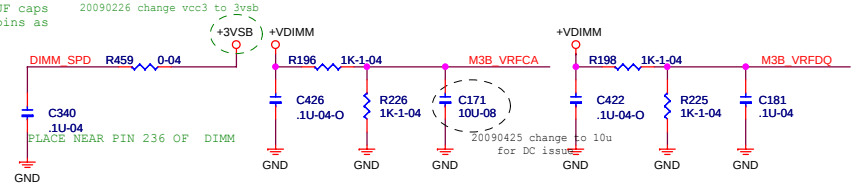
9 M3B_WEB — M3B_WEB
9 M3B_RASB — M3B_RASB
9 M3B_CASB — M3B_CASB
9,16 M3_DRSTB — M3_DRSTB

16 DIMM_SPD — DIMM_SPD

7,13,16,20,23,24 SMBCLK — SMBCLK
7,13,16,20,23,24 SMBDATA — SMBDATA







Elitegroup Computer Systems

Title	240P DDR3, CHB	
Size: Custom	Document Number: L-IG41M3	Rev: 1.1
Date: Monday, August 31, 2009	Sheet 17 of 38	

20090425 intel review
Place near ICH7
PDG chapter8 fig8-19

SB1A
NH82801GB-A1

X7R:for DMI

8 DMI_TXP_0 SC314 .1U-X7-04-X DMI_TXP0 V25
8 DMI_TXN_0 SC315 .1U-X7-04-X DMI_TXN0 V26
8 DMI_TXP_1 SC319 .1U-X7-04-X DMI_TXP1 Y25
8 DMI_TXN_1 SC321 .1U-X7-04-X DMI_TXN1 Y26
8 DMI_TXP_2 SC322 .1U-X7-04-X DMI_TXP2 AB25
8 DMI_TXN_2 SC326 .1U-X7-04-X DMI_TXN2 AB26
8 DMI_TXP_3 SC327 .1U-X7-04-X DMI_TXP3 AD24
8 DMI_TXN_3 SC328 .1U-X7-04-X DMI_TXN3 AD25

DMI_RXP0 U27 DMI_RX_P0 C352 .1U-X7-04 DMI_RXP0 8
DMI_RXN0 U28 DMI_RX_N0 C354 .1U-X7-04 DMI_RXN0 8
DMI_RXP1 W27 DMI_RX_P1 C451 .1U-X7-04 DMI_RXP1 8
DMI_RXN1 W28 DMI_RX_N1 C452 .1U-X7-04 DMI_RXN1 8
DMI_RXP2 AA27 DMI_RX_P2 C454 .1U-X7-04 DMI_RXP2 8
DMI_RXN2 AA28 DMI_RX_N2 C453 .1U-X7-04 DMI_RXN2 8
DMI_RXP3 AC27 DMI_RX_P3 C455 .1U-X7-04 DMI_RXP3 8
DMI_RXN3 AC28 DMI_RX_N3 C456 .1U-X7-04 DMI_RXN3 8

+FIL_1P5V R467 24.9-1-04 DMI_COMP C25 D25

DMI_ZCOMP
DMI_IRCOMP
DMI_CLKP AE27 ICH100M_P ICH100M_P 7
DMI_CLKN AE28 ICH100M_N ICH100M_N 7

PCIE_RXP4 M25 PCIE_RXP1 F25 GPP_RX3P GPP_RX3P 25
PCIE_RXN4 M26 PCIE_RXN1 F26 GPP_RX3N GPP_RX3N 25
PCIE_TXP4 L27 PCIE_TXP1 E27 PCIE_TXP1 C322 .1U-X7-04 GPP_TX3P GPP_TX3P 25
PCIE_TXN4 L28 PCIE_TXN1 E28 PCIE_TXN1 C351 .1U-X7-04 GPP_TX3N GPP_TX3N 25
REALTEK LAN

PCIE_RXP5 P25 PCIE_RXP2 H25 HS1_RX_P HS1_RX_P 23
PCIE_RXN5 P26 PCIE_RXN2 H26 HS1_RX_N HS1_RX_N 23
PCIE_TXP5 N27 PCIE_TXP2 G27 HS1_TX_P HS1_TX_P 23
PCIE_TXN5 N28 PCIE_TXN2 G28 HS1_TX_N HS1_TX_N 23
PCIE X1 slot

PCIE_RXP6 T24 PCIE_RXP3 K25 HS2_RX_P HS2_RX_P 23
PCIE_RXN6 T25 PCIE_RXN3 K26 HS2_RX_N HS2_RX_N 23
PCIE_TXP6 R27 PCIE_TXP3 J27 HS2_TX_P HS2_TX_P 23
PCIE_TXN6 R28 PCIE_TXN3 J28 HS2_TX_N HS2_TX_N 23
PCIE X1 slot

22 USB4_P USB4_P K2 USB_P4 USB_P0 F2 USB0_P USB0_P 22
22 USB4_N USB4_N K1 USB_N4 USB_N0 F1 USB0_N USB0_N 22
USB_OC4_R_N E5 #OC4 #OC0 D3 USB_OC0_R_N

22 USB5_P USB5_P L5 USB_P5 USB_P1 G3 USB1_P USB1_P 22
22 USB5_N USB5_N L4 USB_N5 USB_N1 G4 USB1_N USB1_N 22
USB_OC4_R_N C3 #OC5/*GPIO29 #OC1 C4 USB_OC0_R_N

22 USB6_P USB6_P M2 USB_P6 USB_P2 H2 USB2_P USB2_P 22
22 USB6_N USB6_N M1 USB_N6 USB_N2 H1 USB2_N USB2_N 22
USB_OC6_R_N A2 #OC6/*GPIO30 #OC2 D5 USB_OC2_R_N

22 USB7_P USB7_P N3 USB_P7 USB_P3 J3 USB3_P USB3_P 22
22 USB7_N USB7_N N4 USB_N7 USB_N3 J4 USB3_N USB3_N 22
USB_OC6_R_N B3 #OC7/*GPIO31 #OC3 D4 USB_OC2_R_N

22.6-1-04 R480 USBRBIAS_L D1 USBRBIAS CLK48 B2 USB48M USB48M 7
D2 #USBRBIAS
GND

Must routing a trace to 22.6ohm pad, Don't direct connect with USBRBIAS.(two trace must < 500 mils)

C56 10P-04-O
GND

SB1B
NH82801GB-A1

24 PAR PAR E10 PAR AD0 E18 AD0
24 DEVSEL_L DEVSEL_L A12 #DEVSEL AD1 C18 AD1
7 ICH33M ICH33M A9 PCICLK AD2 A16 AD2
24 PCIRST_L PCIRST_L B18 #PCIRST AD3 F18 AD3
24 IRDY_L IRDY_L A7 #IRDY AD4 E16 AD4
24 PME_L PME_L B19 #PME AD5 A18 AD5
24 SERR_L SERR_L B10 #SERR AD6 E17 AD6
24 STOP_L STOP_L F15 #STOP AD7 A17 AD7
24 PLOCK_L PLOCK_L E11 #PLOCK AD8 A15 AD8
24 TRDY_L TRDY_L F14 #TRDY AD9 C14 AD9
24 PERR_L PERR_L C9 #PERR AD10 E14 AD10
24 FRAME_L FRAME_L F16 #FRAME AD11 D14 AD11
AD12 B12 AD12
AD13 C13 AD13
24 GNT0_L GNT0_L E7 #GNT0 AD14 G15 AD14
GNT1_L D16 #GNT1 AD15 G13 AD15
GNT2_L D17 #GNT2 AD16 E12 AD16
GNT3_L F13 #GNT3 AD17 C11 AD17
GNT4_L A14 #GNT4/GPIO48 AD18 D11 AD18
GNT5_L D8 #GNT5/GPO17 AD19 A11 AD19
AD20 A10 AD20
24 REQ0_L REQ0_L D7 #REQ0 AD21 E11 AD21
REQ1_L C16 #REQ1 AD22 F10 AD22
REQ2_L C17 #REQ2 AD23 E9 AD23
REQ3_L F13 #REQ3 AD24 D9 AD24
REQ4_L A13 #REQ4/GPIO22 AD25 B9 AD25
REQ5_L C8 #REQ5/GPI1 AD26 A8 AD26
AD27 A6 AD27
INTA_L A3 #PIRQA AD28 C7 AD28
INTB_L B4 #PIRQB AD29 B6 AD29
INTC_L C5 #PIRQC AD30 E6 AD30
INTD_L B5 #PIRQD AD31 D6 AD31
24 INTE_L INTE_L G8 #PIRQE/**GPI2
24 INTF_L INTF_L F7 #PIRQF/**GPI3
24 INTG_L INTG_L F8 #PIRQG/**GPI4 C_#BE0 B15 C_BE_L0
24 INTH_L INTH_L G7 #PIRQH/**GPI5 C_#BE1 C12 C_BE_L1
C_#BE2 D12 C_BE_L2
C_#BE3 C15 C_BE_L3

N1 VSS VSS P3
N2 VSS VSS P4
N5 VSS VSS P12
N6 VSS VSS P13
N11 VSS VSS P14
N12 VSS VSS P15
N13 VSS VSS P16
N14 VSS VSS P17
N15 VSS VSS P24
N16 VSS VSS P27
N17 VSS VSS P28
N18 VSS VSS R1
N24 VSS VSS R11
N25 VSS VSS R12
N26 VSS VSS R13
GND GND

AD[31..0] AD[31..0] 24
C_BE_L[3..0] C_BE_L[3..0] 24

34 USB_OC0_R_N USB_OC0_R_N
34 USB_OC2_R_N USB_OC2_R_N
34 USB_OC4_R_N USB_OC4_R_N
34 USB_OC6_R_N USB_OC6_R_N
20090324 add for lenovo

+3VSB
RN67 10K-8P4R-04
USB_OC0_R_N 1 2
USB_OC2_R_N 3 4
USB_OC4_R_N 5 6
USB_OC6_R_N 7 8

+VCC3
GNT0_L R427 10K-04-O
GNT1_L R422 10K-04-O
GNT2_L R437 10K-04-O
GNT3_L R435 10K-04-O
ICH7 internal 20K pull-ups for GNT0-5

+VCC3
REQ0_L R491 10K-04
REQ1_L R492 10K-04
REQ5_L RN29 1 2 8.2K-8P4R
REQ3_L 3 4
REQ4_L 5 6
REQ2_L 7 8

+VCC3
INTA_L RN28 1 2 8.2K-8P4R
INTC_L 3 4
INTB_L 5 6
INTD_L 7 8
INTE_L RN31 1 2 8.2K-8P4R
INTF_L 3 4
INTG_L 5 6
INTH_L 7 8

+VCC3
GNT5_L 2
RJ15 1K-04 (2-3)
1 3
GND
+VCC3
GNT4_L 2
RJ10 1K-04-O (1-2)
1 3
GND

BOOT BIOS DESTINATION SELECTION		
GNT5_L	GNT4_L	BOOT BIOS DESTINATION
* 0	1	SPI
1	0	PCI
1	1	LPC
0	0	Reserved

*Default

ICH33M C323 10P-04-O
near ICH7
GND

+VCC3
for usb current return path
C369 1U-X7-04
+VCC

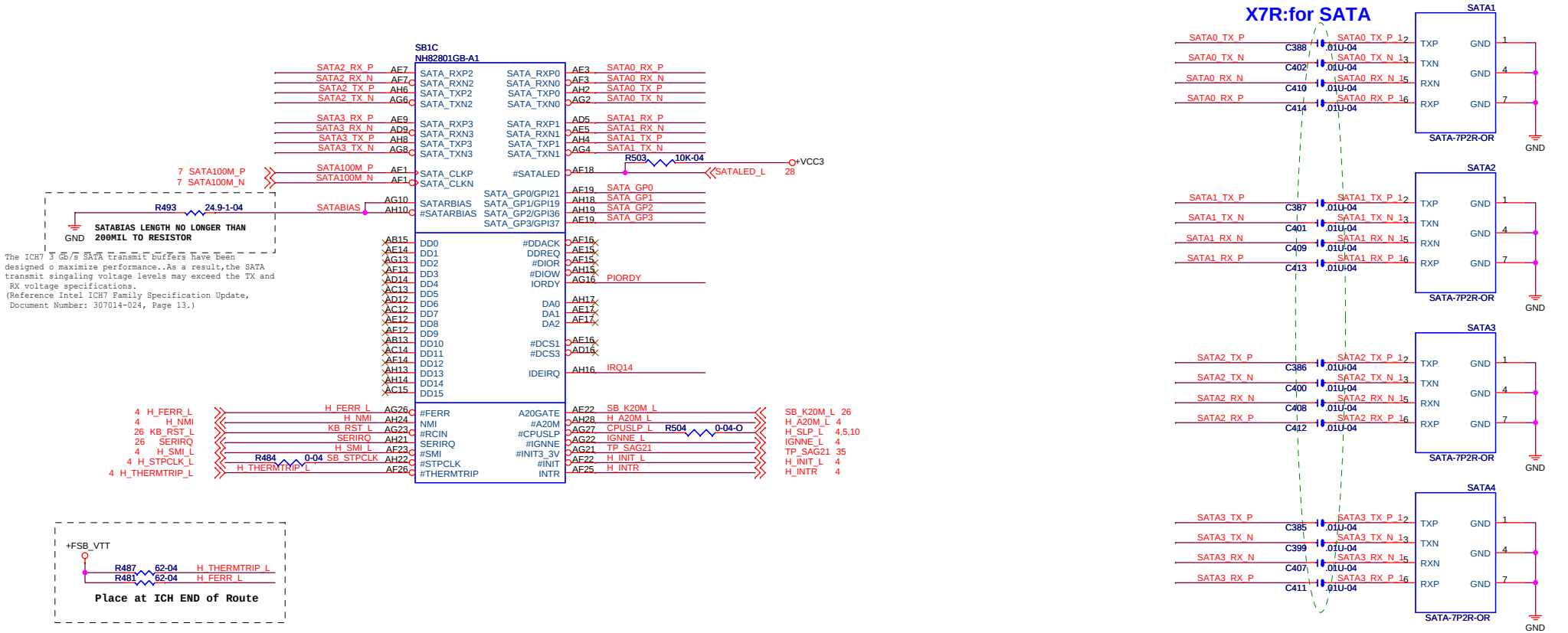
+VCC3
SC51 10P-04-X
SC38 10P-04-X
GND

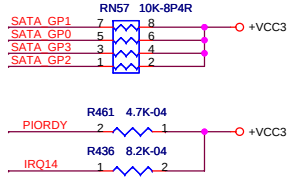
Elitegroup Computer Systems

Title: ICH7 PCI/PCI-E/USB

Size	Document Number	Rev
Custom	L-IG41M3	1.1

Date: Monday, August 31, 2009 Sheet 18 of 38





Elitegroup Computer Systems		
Title: ICH7 SATA		
Size: Custom	Document Number: L-IG41M3	Rev: 1.1
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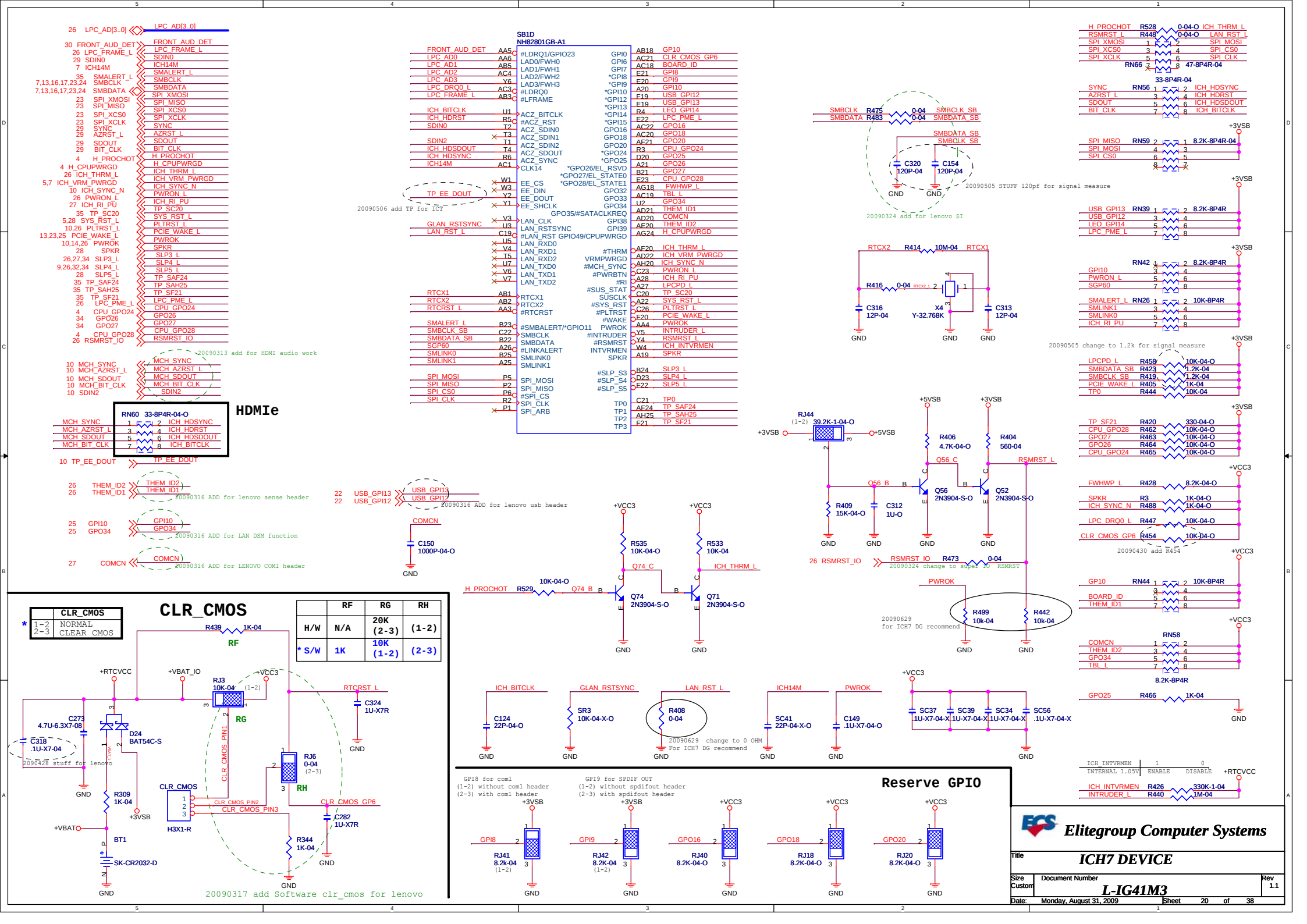
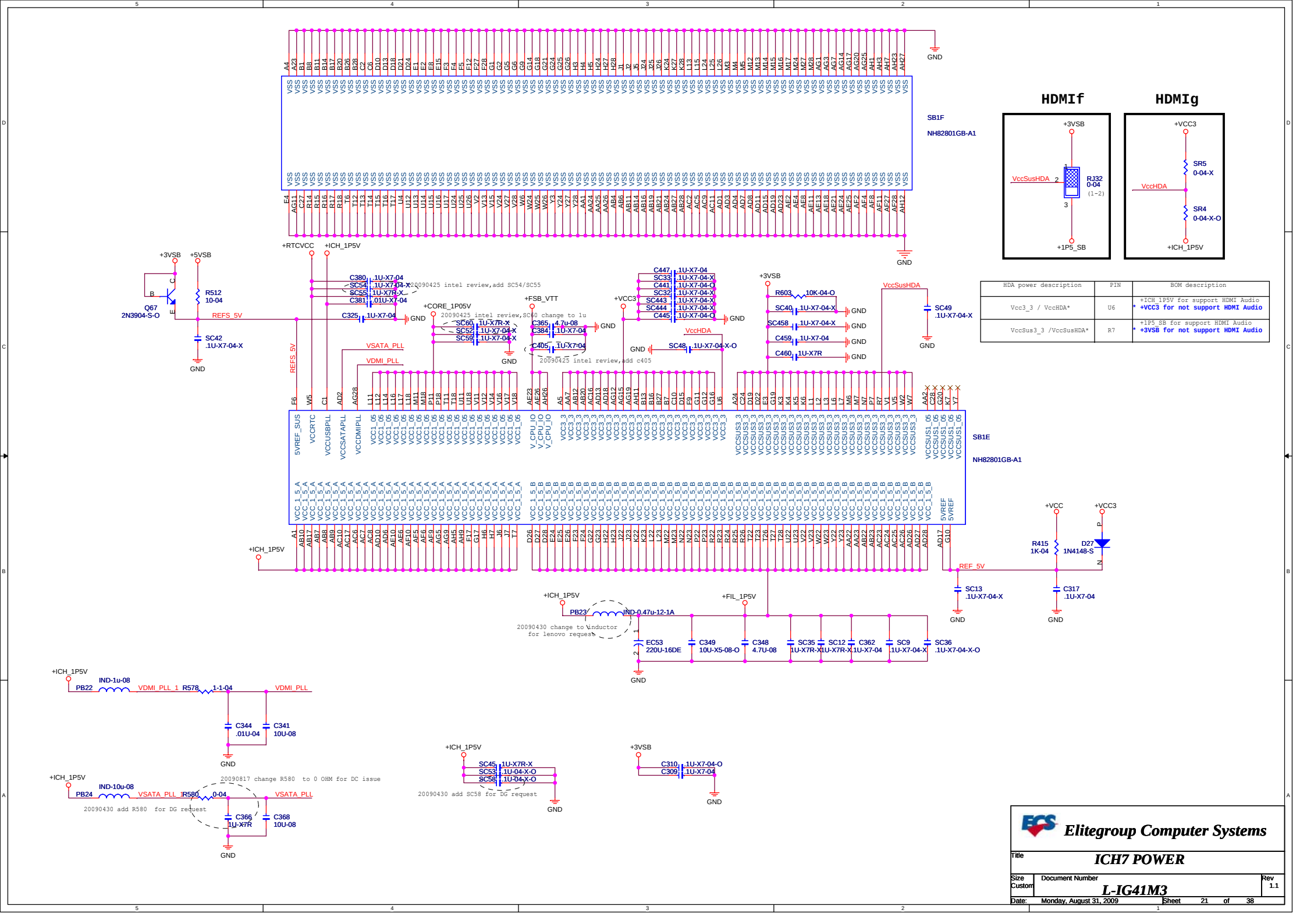

SB1D
NH82801GB-A1
HDMIe
CLR_CMOS
RF
RG
RH
Reserve GPIO
ICH7 DEVICE
Elitegroup Computer Systems
L-IG41M3
Monday, August 31, 2009
20090317 add Software clr_cmos for lenovo
20090324 add for lenovo SI
20090505 STUFF 120pf for signal measure
20090505 change to 1.2k for signal measure
20090313 add for HDMI audio work
20090316 ADD for lenovo sense header
20090316 ADD for LAN DSM function
20090316 ADD for LENOVO COM1 header
20090316 ADD for lenovo usb header
20090506 add TP for ICT
20090324 change to super IO RSMRST
20090629 change to 0 OHM For ICH7 DG recommend
20090430 add R454
20090428 stuff for lenovo


SB1F
NH82801GB-A1
SB1E
NH82801GB-A1
HDMIf
HDMIg
+3VSB
VccSusHDA
RJ32
0-04
(1-2)
+1P5_SB
+VCC3
SR5
0-04-X
VccHDA
SR4
0-04-X-O
+ICH_1P5V
HDA power description
PIN
BOM description
Vcc3_3 / VccHDA*
U6
+ICH_1P5V for support HDMI Audio
* +VCC3 for not support HDMI Audio
VccSus3_3 /VccSusHDA*
R7
+1P5_SB for support HDMI Audio
* +3VSB for not support HDMI Audio
Elitegroup Computer Systems
ICH7 POWER
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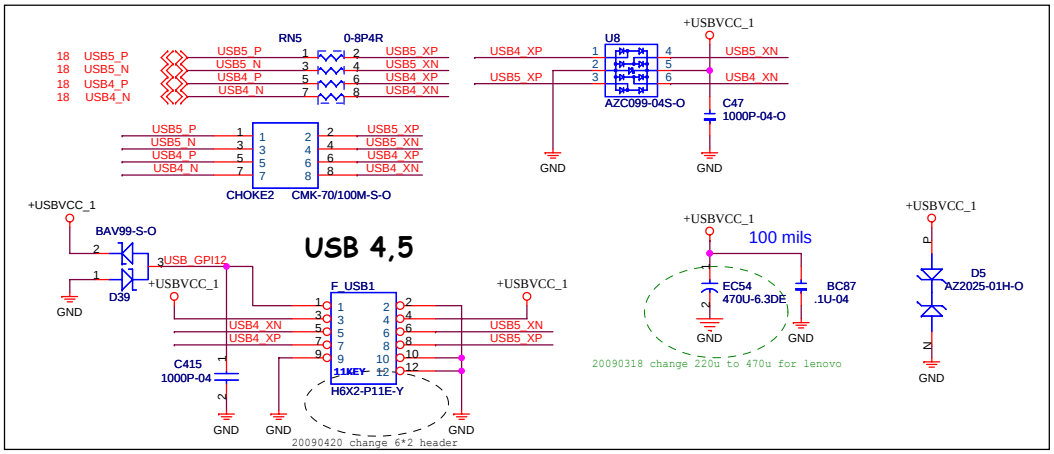
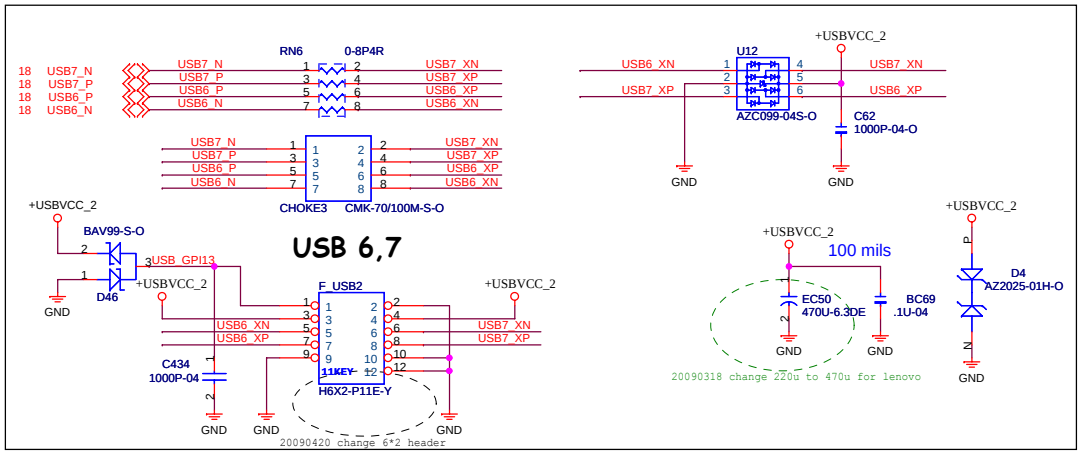
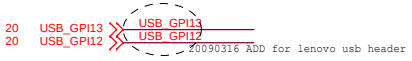
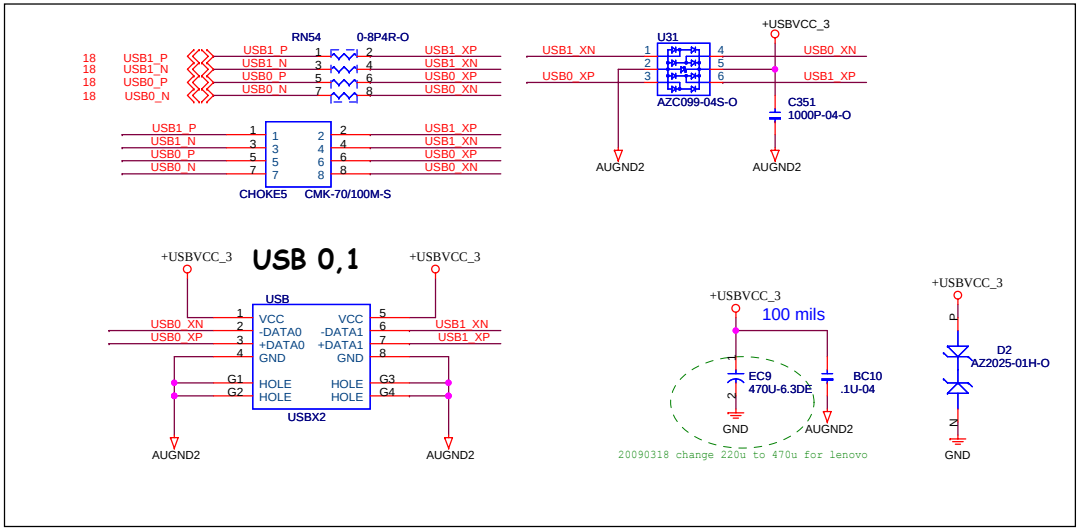
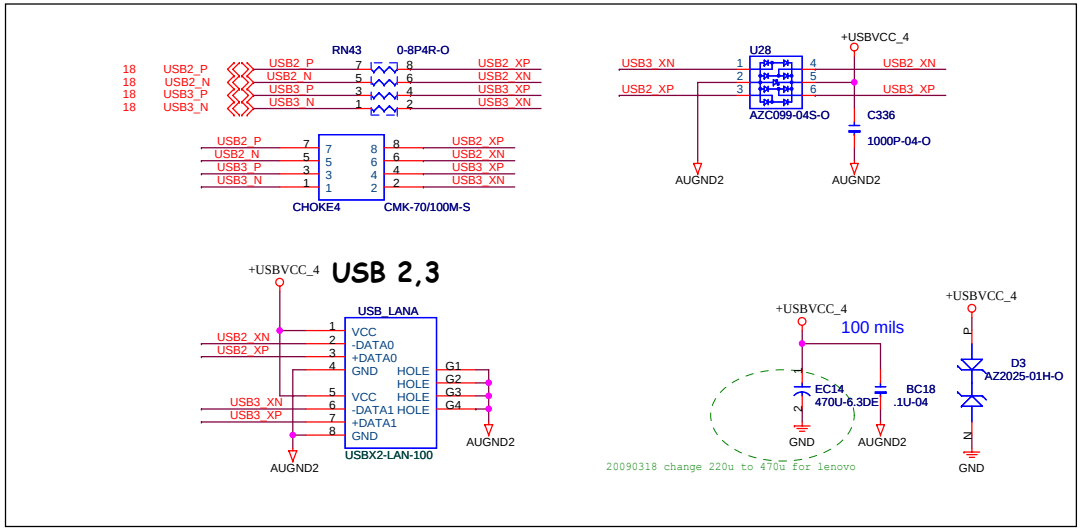


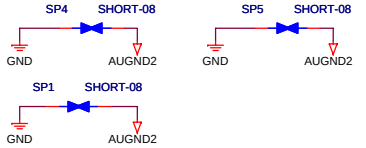


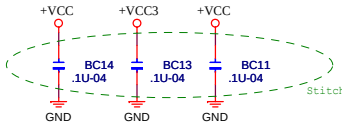


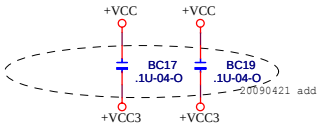
Lenovo request
F_USB1: UHCI HOST CONTROLLER 3#
F_USB2: UHCI HOST CONTROLLER 4#
REAR_USB: UHCI HOST CONTROLLER 1#、2#











Elitegroup Computer Systems

Title	USB	
Size: Custom	Document Number: L-IG41M3	Rev: 1.1
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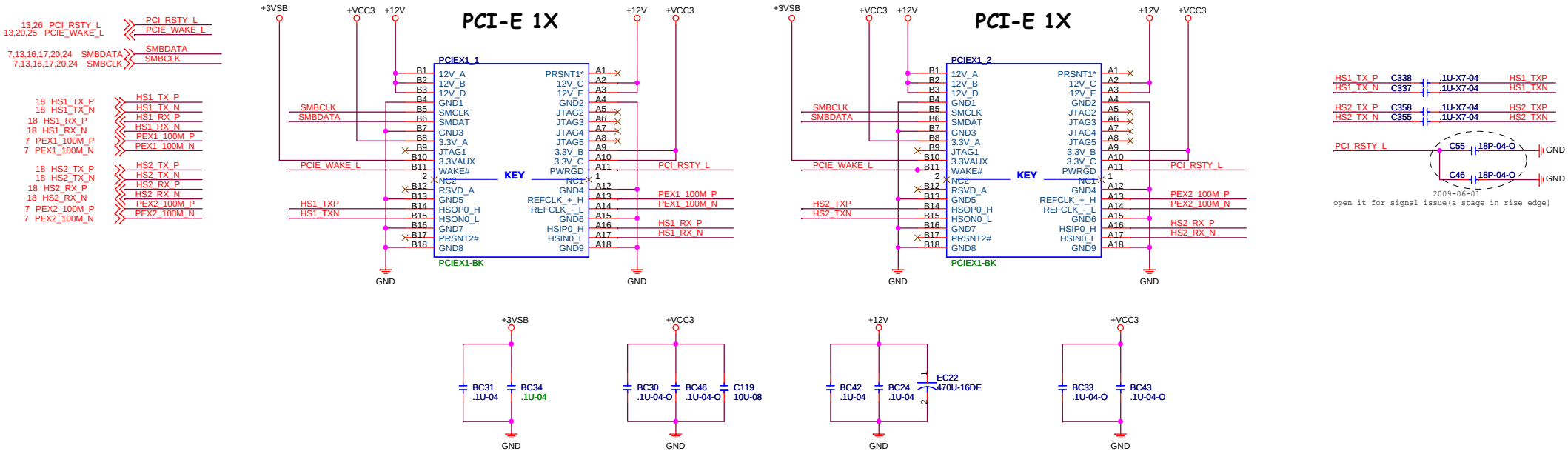

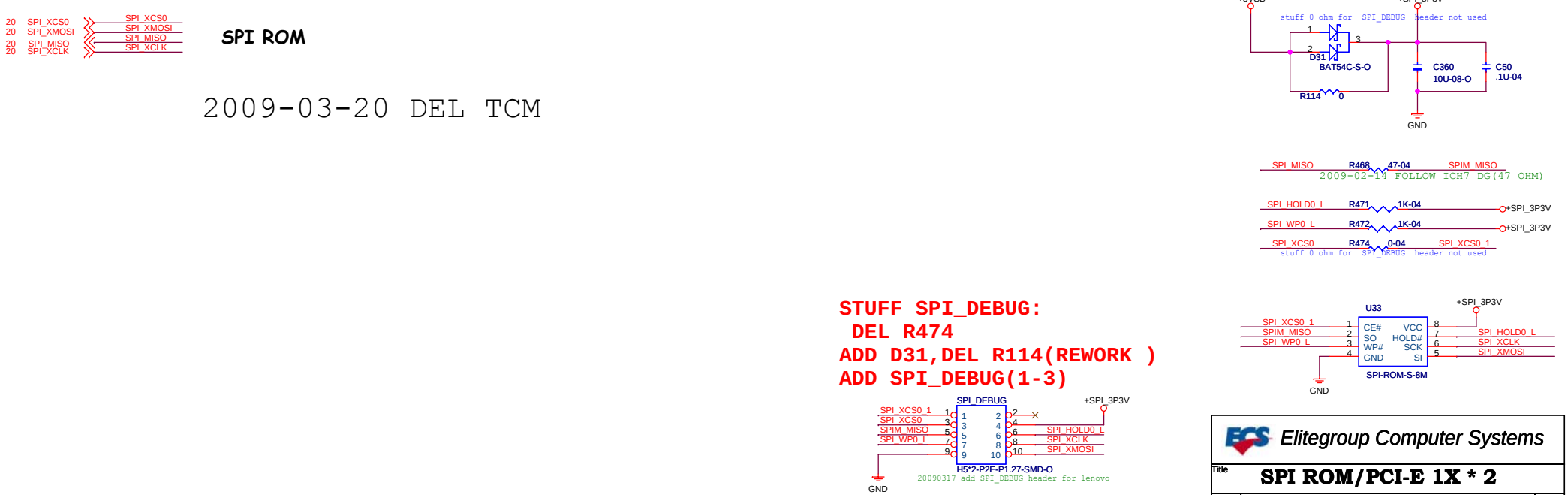

Elitegroup Computer Systems

Title	SPI ROM/PCI-E 1X * 2	
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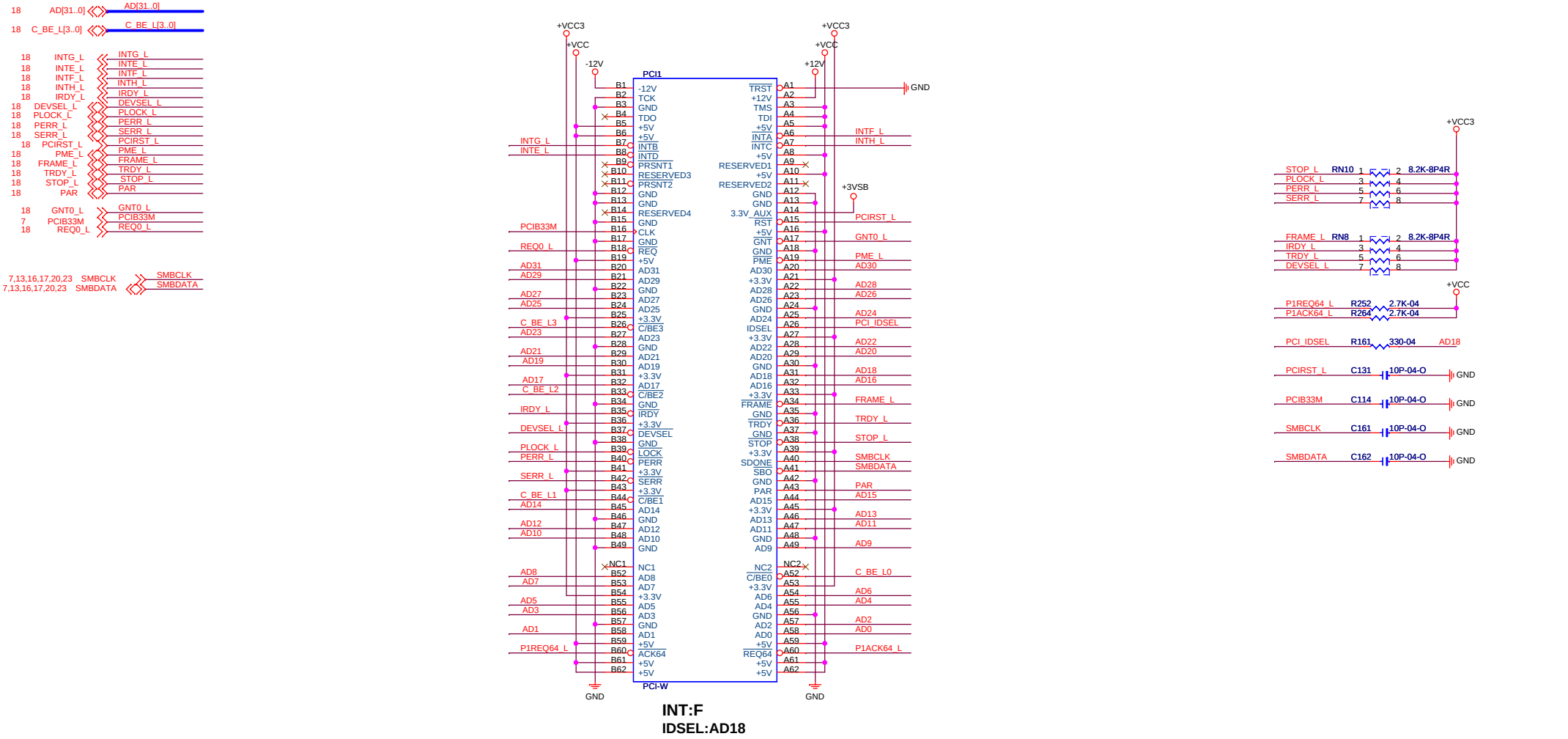

Elitegroup Computer Systems

Title: PCI

Size: Custom | Document Number: L-IG41M3 | Rev: 1.1

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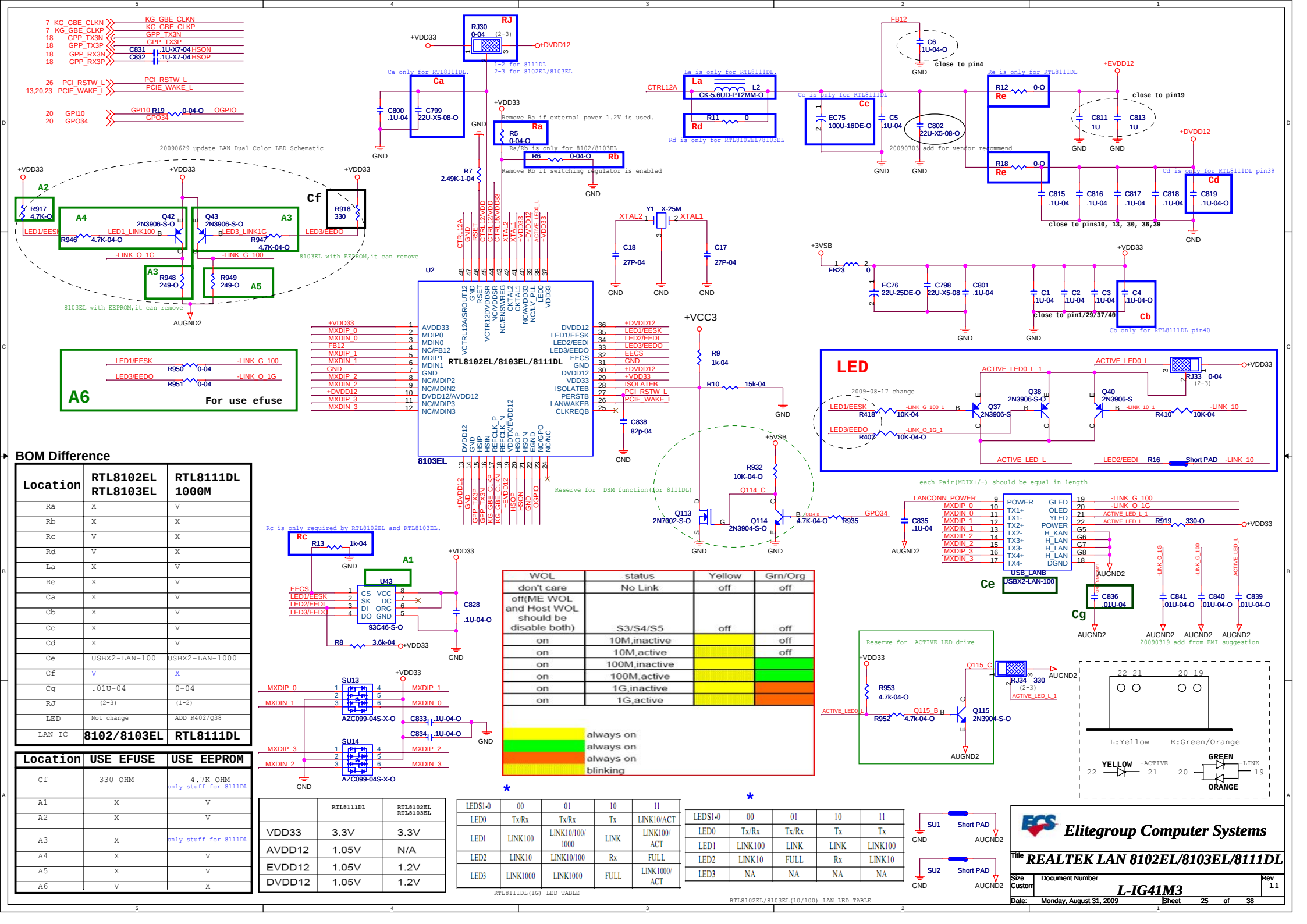

BOM Difference

Location	RTL8102EL RTL8103EL	RTL8111DL 1000M
Ra	X	V
Rb	X	X
Rc	V	X
Rd	V	X
La	X	V
Re	X	V
Ca	X	V
Cb	X	V
Cc	X	V
Cd	X	V
Ce	USBX2-LAN-100	USBX2-LAN-1000
Cf	V	X
Cg	.01U-04	0-04
RJ	(2-3)	(1-2)
LED	Not change	ADD R402/Q38
LAN IC	8102/8103EL	RTL8111DL

Location	USE EFUSE	USE EEPROM
Cf	330 OHM	4.7K OHM only stuff for 8111DL
A1	X	V
A2	X	V
A3	X	only stuff for 8111DL
A4	X	V
A5	X	V
A6	V	X

	RTL8111DL	RTL8102EL RTL8103EL
VDD33	3.3V	3.3V
AVDD12	1.05V	N/A
EVDD12	1.05V	1.2V
DVDD12	1.05V	1.2V

WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

always on
always on
always on
blinking

*

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ACT
LED1	LINK100	LINK10/100/1000	LINK	LINK100/ACT
LED2	LINK10	LINK10/100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000/ACT

RTL8111DL(1G) LED TABLE

*

LEDS1-0	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK	LINK	LINK100
LED2	LINK10	FULL	Rx	LINK10
LED3	NA	NA	NA	NA

RTL8102EL/8103EL(10/100) LAN LED TABLE

Elitegroup Computer Systems

Title: REALTEK LAN 8102EL/8103EL/8111DL

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If without use these pins, Please pull-up to VCC. Don't let it floating
1.Pin 52:VIN3/ATXPG
2.Pin 32:SUSB#
3.Pin 25/ Pin 58/ Pin 60/ Pin 62
4.Pin 10:RESETCON#

IT8755E
64-LQFP

SIO

RSMRST_IO

The RSMRST# signal of the IntelR ICH7 must transition from 20% signal level to 80% signal level and vice versa in 50 µs or less, and the falling edge must transition to 0.8 V or less before VccSus3_3 drops to 2.1V

ICH7 Integrates 20 k pull-up resistors for LPC signal

minimum trace width 12mils

20090324 add for lenovo(SI reserve)

20090421 change R to 150-04 for Signal measure

for ICH7 request

20090629 Update IT8757 ATXPG circuit for 3V level

20090421 LENOVO SUGGESTION

RN55 Stuff when COM1 not stuff

THEM_ID1	THEM_ID2	Chassic type
0	0	10L
0	1	13L
1	0	17L
★ 1	1	25L

BOM Difference

	IT8755 ★	IT8757
IO_1	V	X
IO_2	X	V
IO_3	V	X
IO_4	X	V
IO_5	(2-3)	(1-2)

VCCH_IO < 15mA
VCC_IO < 60mA
AVCC_IO < 60mA

Close to pin31 Close to pin2,15 Close to pin30 Close to pin56

Place it close to 8755 pin49

Elitegroup Computer Systems

Title: SIO:IT8755/8757

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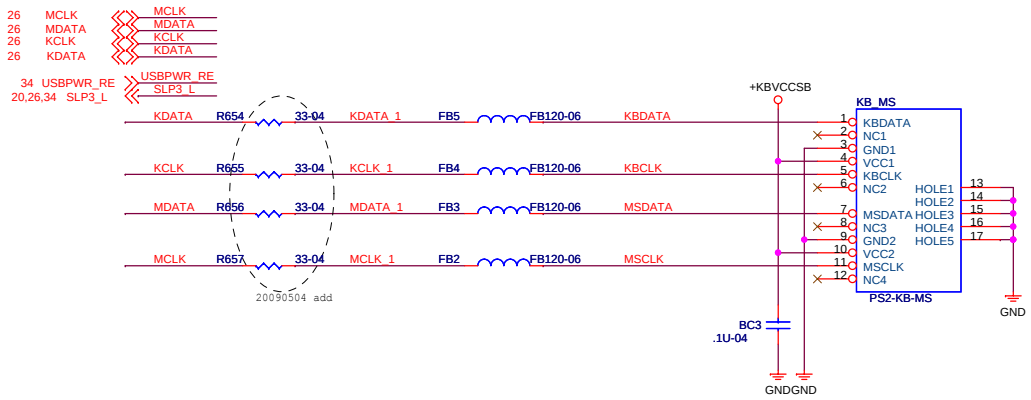
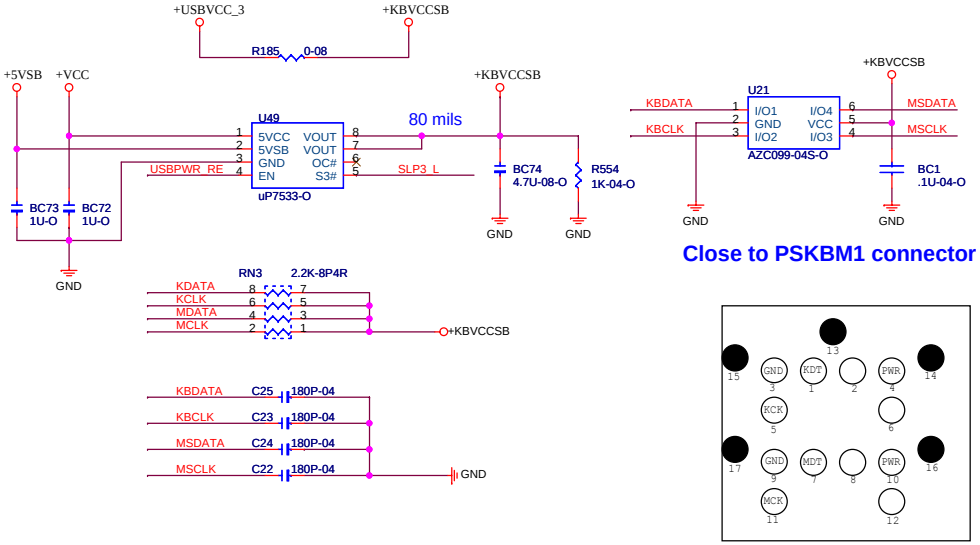
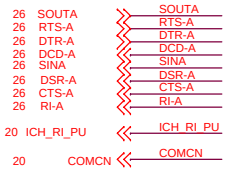
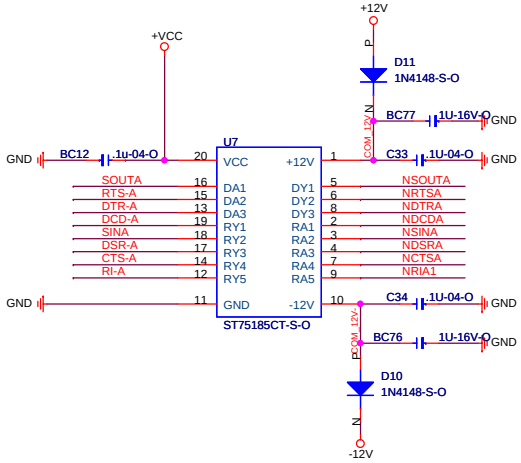
KEYBOARD & MOUSE

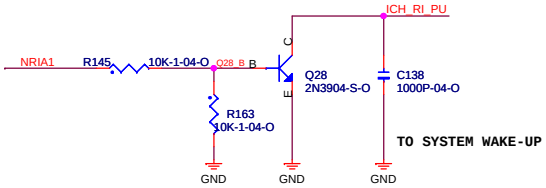


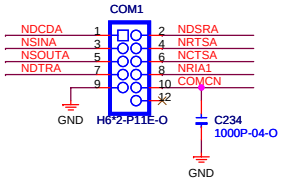


COM1

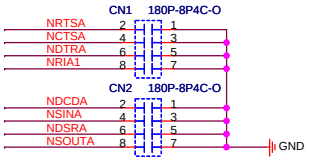








COM1 USE Header



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Title	PS2/COM	
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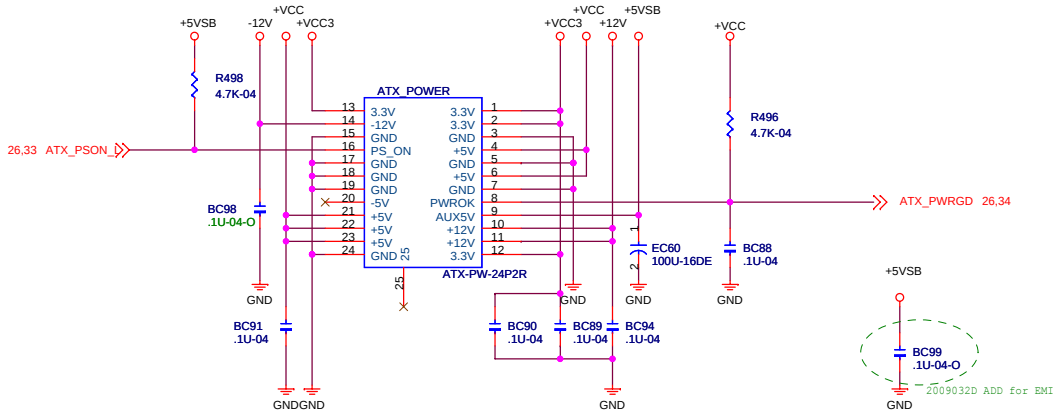
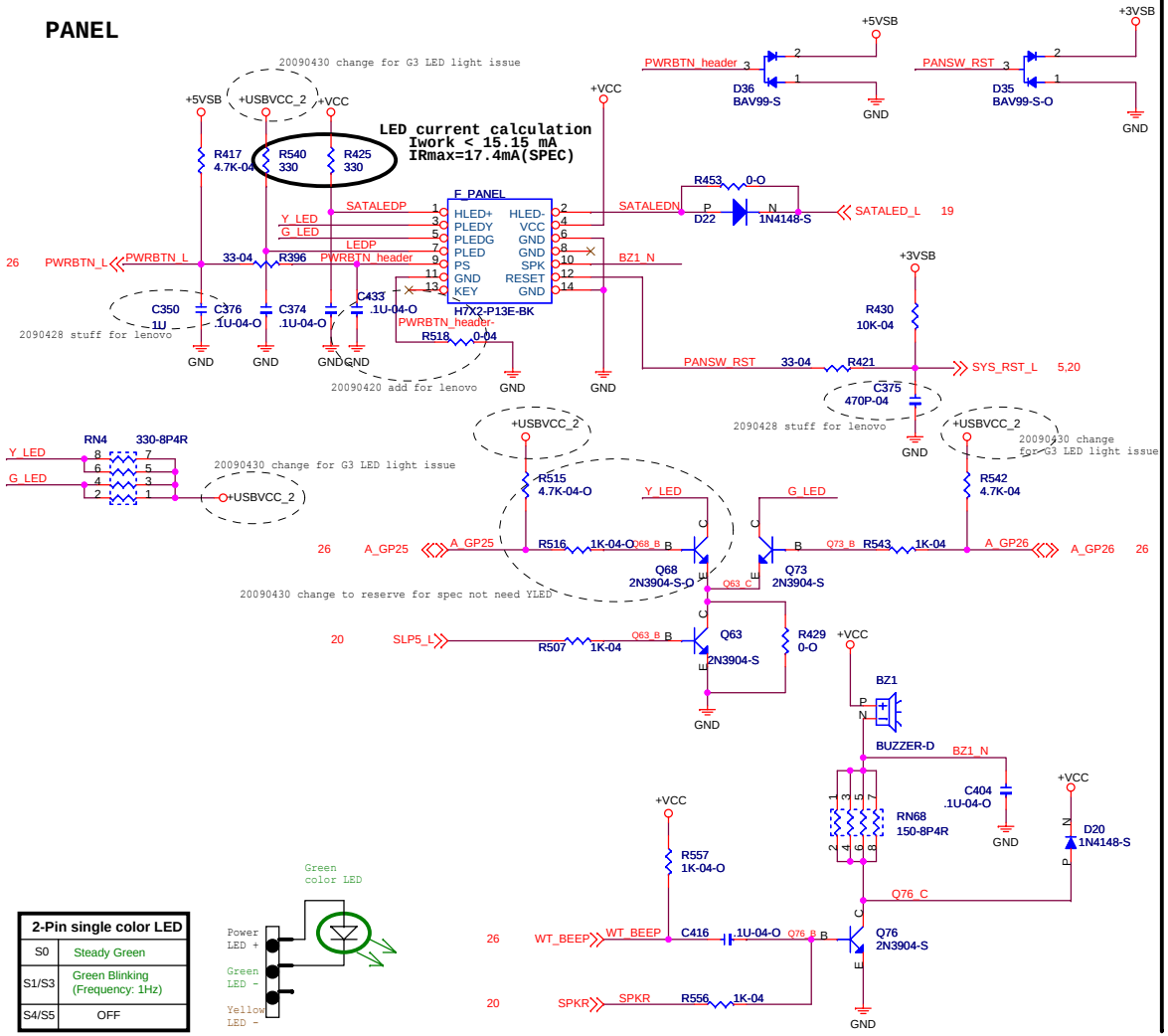
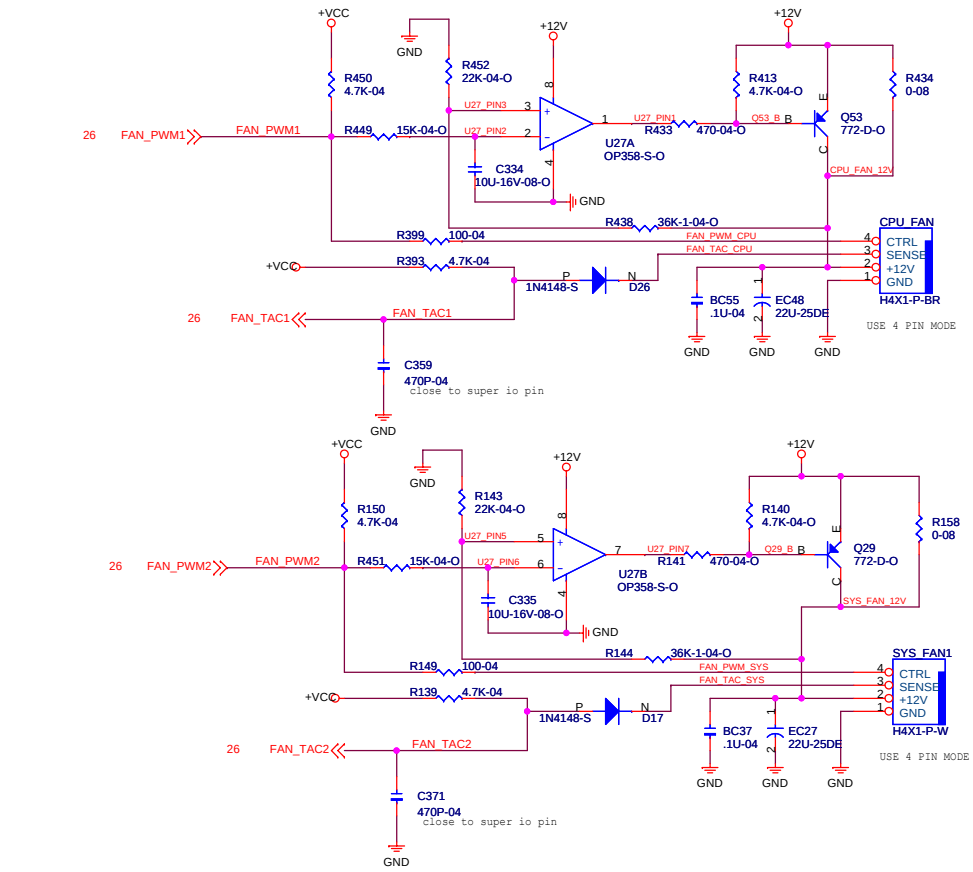


PANEL



2-Pin single color LED	
S0	Steady Green
S1/S3	Green Blinking (Frequency: 1Hz)
S4/S5	OFF

FAN



Title	PANEL & FAN
Size	Custom
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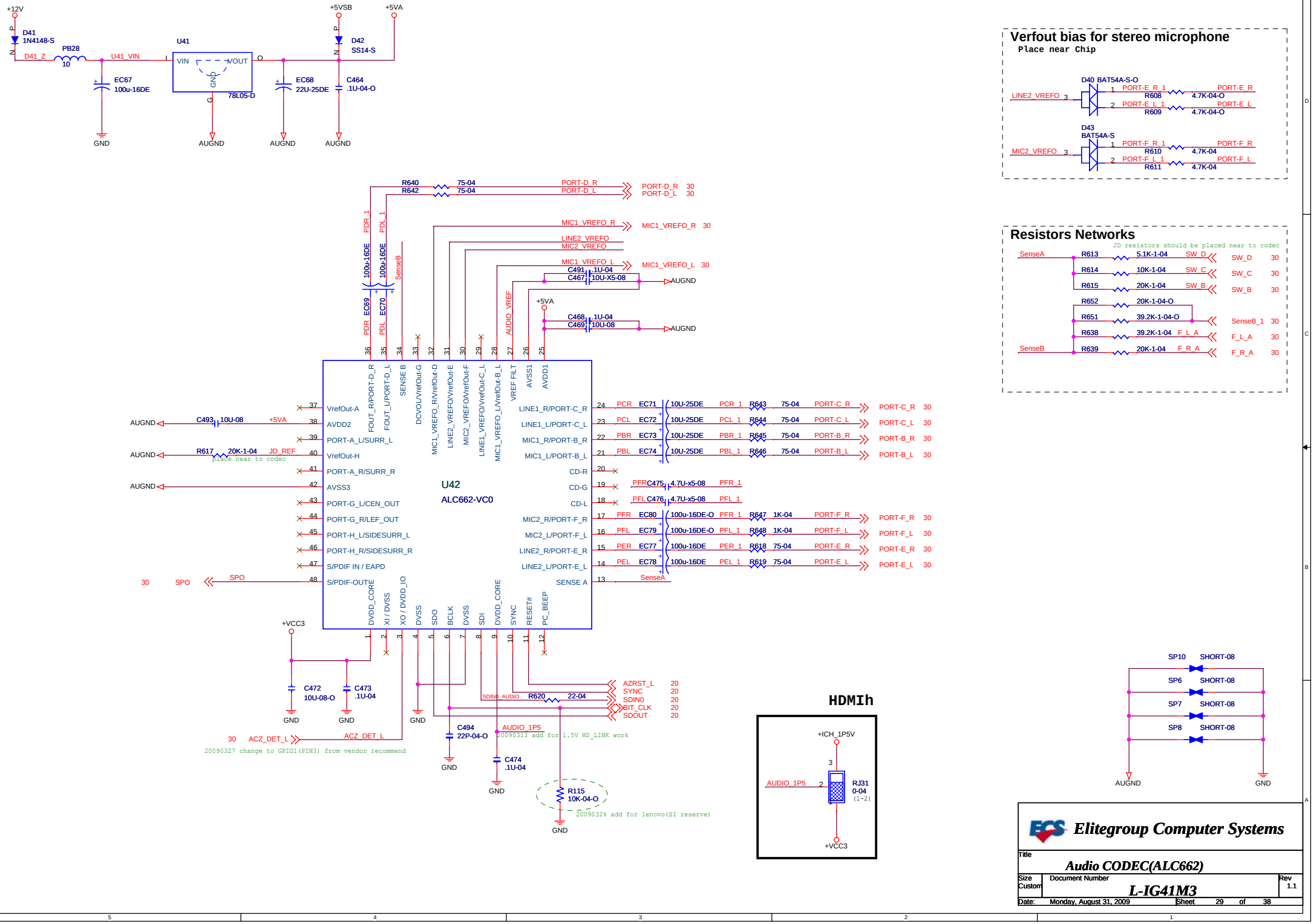
+12V
D41
1N4148-S
PB28
10
D41_Z
U41_VIN
U41
VIN
VOUT
GND
78L05-D
EC67
100u-16DE
EC68
22U-25DE
C464
.1U-04-O
+5VSB
+5VA
D42
SS14-S
GND
AUGND
AUGND
AUGND
Verfout bias for stereo microphone
Place near Chip
D40 BAT54A-S-O
LINE2_VREFO
PORT-E_R_1
PORT-E_L_1
R608
R609
4.7K-04-O
PORT-E_R
PORT-E_L
D43
BAT54A-S
MIC2_VREFO
PORT-F_R_1
PORT-F_L_1
R610
R611
4.7K-04
PORT-F_R
PORT-F_L
Resistors Networks
JD resistors should be placed near to codec
SenseA
R613
5.1K-1-04
SW_D
R614
10K-1-04
SW_C
R615
20K-1-04
SW_B
R652
20K-1-04-O
R651
39.2K-1-04-O
SenseB_1
R638
39.2K-1-04
F_L_A
SenseB
R639
20K-1-04
F_R_A
R640
R642
75-04
PORT-D_R
PORT-D_L
MIC1_VREFO_R
LINE2_VREFO
MIC2_VREFO
MIC1_VREFO_L
C491
C467
.1U-04
10U-X5-08
C468
C469
1U-04
10U-08
AUDIO_VREF
PDR
PDL
EC69
EC70
100u-16DE
SenseB
U42
ALC662-VC0
VrefOut-A
AVDD2
PORT-A_L/SURR_L
VrefOut-H
PORT-A_R/SURR_R
AVSS3
PORT-G_L/CEN_OUT
PORT-G_R/LEF_OUT
PORT-H_L/SIDESURR_L
PORT-H_R/SIDESURR_R
S/PDIF IN / EAPD
S/PDIF-OUT
C493
10U-08
+5VA
R617
20K-1-04
JD_REF
place near to codec
SPO
LINE1_R/PORT-C_R
LINE1_L/PORT-C_L
MIC1_R/PORT-B_R
MIC1_L/PORT-B_L
CD-R
CD-G
CD-L
MIC2_R/PORT-F_R
MIC2_L/PORT-F_L
LINE2_R/PORT-E_R
LINE2_L/PORT-E_L
SENSE A
PCR
PCL
PBR
PBL
PFR
PFL
PER
PEL
EC71
EC72
EC73
EC74
EC80
EC79
EC77
EC78
10U-25DE
100u-16DE-O
100u-16DE
PCR_1
PCL_1
PBR_1
PBL_1
PFR_1
PFL_1
PER_1
PEL_1
R643
R644
R645
R646
R647
R648
R618
R619
1K-04
PORT-C_R
PORT-C_L
PORT-B_R
PORT-B_L
PORT-F_R
PORT-F_L
PORT-E_R
PORT-E_L
C475
C476
4.7U-x5-08
SenseA
DVDD_CORE
XI / DVSS
XO / DVDD_IO
DVSS
SDO
BCLK
DVSS
SDI
DVDD_CORE
SYNC
RESET#
PC_BEEP
+VCC3
C472
10U-08-O
C473
.1U-04
AZRST_L
SYNC
SDIN0
BIT_CLK
SDOUT
SDIN0_AUDIO
R620
22-04
ACZ_DET_L
20090327 change to GPIO1(PIN3) from vendor recommend
C494
22P-04-O
AUDIO_1P5
20090313 add for 1.5V HD_LINK work
C474
.1U-04
R115
10K-04-O
20090324 add for lenovo(SI reserve)
HDMIh
+ICH_1P5V
AUDIO_1P5
RJ31
0-04
(1-2)
+VCC3
SP10
SP6
SP7
SP8
SHORT-08
AUGND
GND
Elitegroup Computer Systems
Title
Audio CODEC(ALC662)
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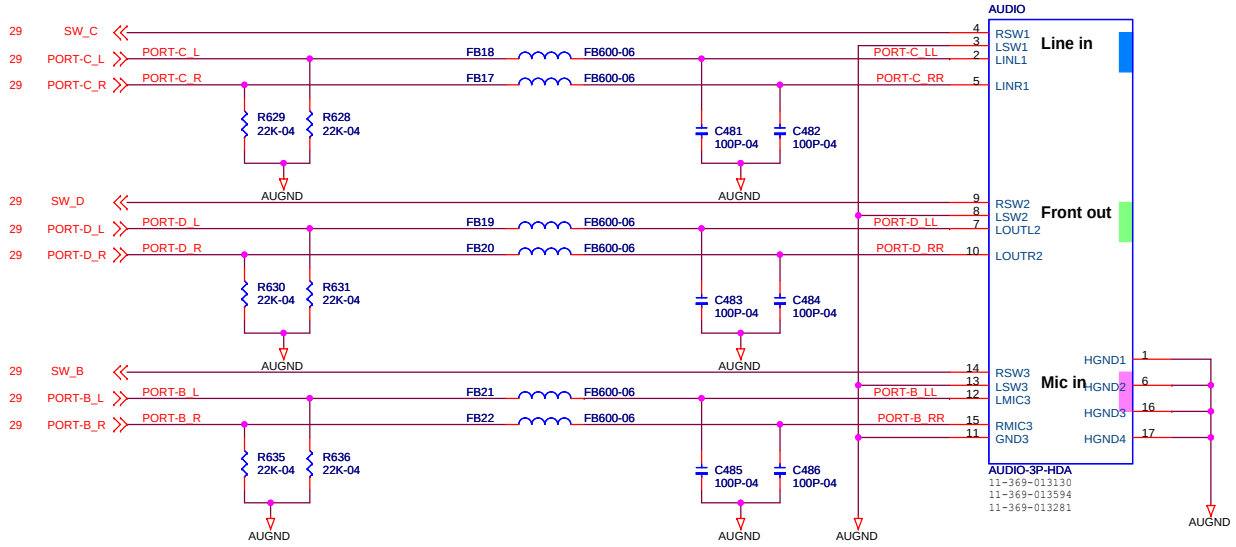

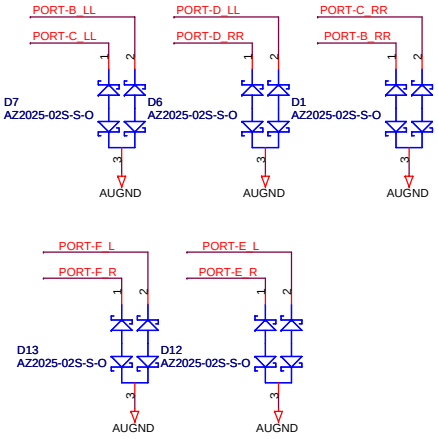

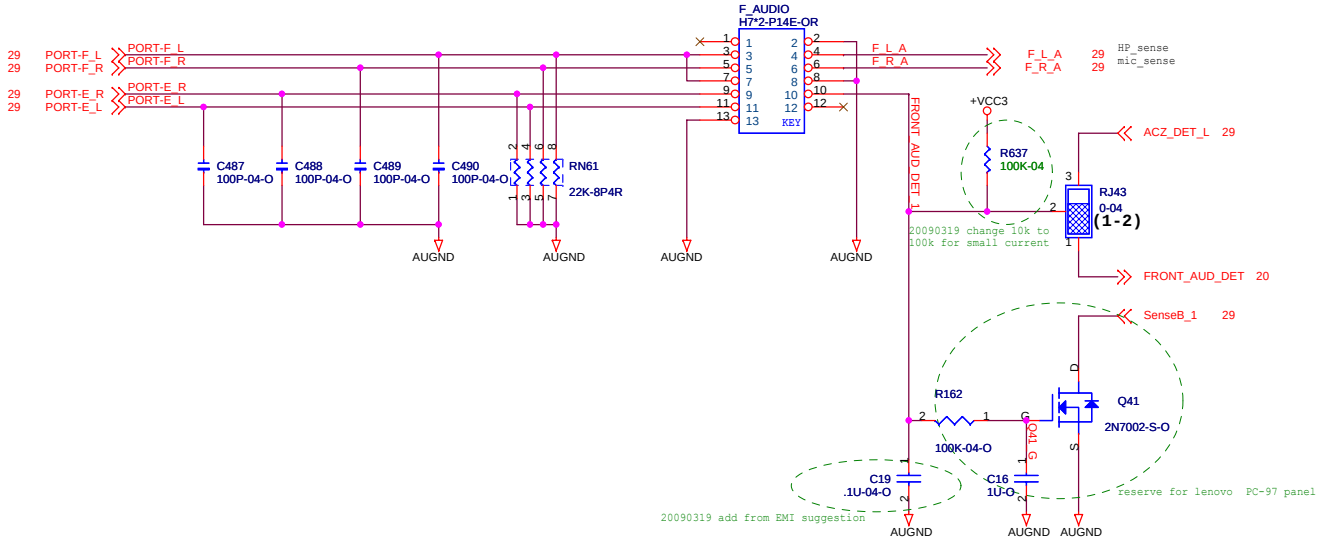

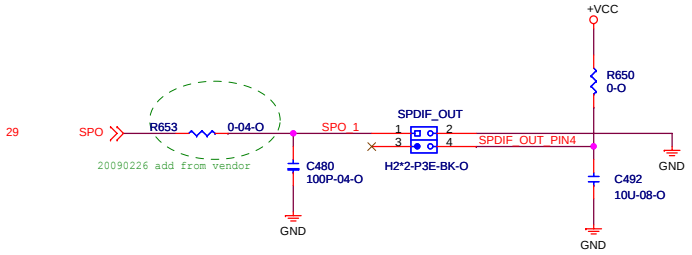

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Title	AUDIO Connecter	
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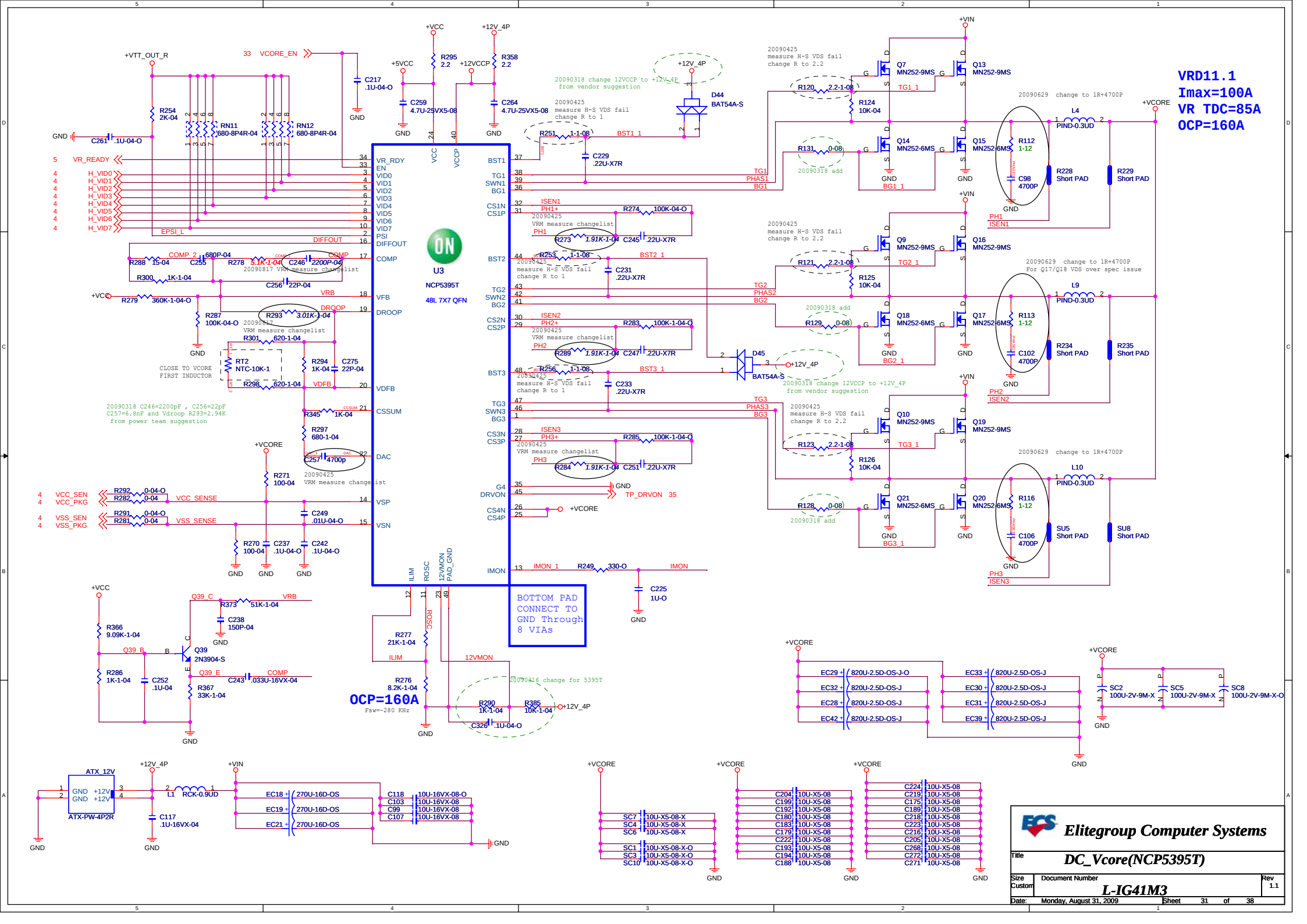
VRD11.1
Imax=100A
VR TDC=85A
OCP=160A
U3
NCP5395T
48L 7X7 QFN
BOTTOM PAD
CONNECT TO
GND Through
8 VIAs
OCP=160A
Fsw=~280 KHz
Elitegroup Computer Systems
DC_Vcore(NCP5395T)
L-IG41M3
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Total:VDIMM:~16A

VDIMM:3.6A/2DIMM
FSB_VTT:5.8A
ICH_1P5V:~2A
CORE_1P05V:1.31A
DDR_VTT:0.415A
MCH_VCC_SM:~2.2A

+5VSB, +VCC, +DIMM_5VDUAL, +DIMM_5VDUAL

R506 0-O
D34 BAT54C-S
D33 BAT54C-S
DIMM_PWM_VCC
BC95 1U-X7R
U35 RT8105GS-S
GND VCC BOOT UGATE PHASE COMP/OCSET FB LGATE
DIMM_boot_1
R534 0
BC93 .1U-X7R-04
D_TG
R525 0
D_TG_1
DIMM_PHASE
COMP_DDR
R526 16.5K-1-04
OC1
DDR_FB
D_BG
R532 0
D_BG_1
R600 43K-04-O
OC2
Iocset=(40uA*Rocset-0.4V)/Rdson(low side MOSFET)
Rocset=16.5K=R526
Rds(on)=7.3 mOHM ,OCP ~ 35.6A
R531 1K-04-O
DDR_FB_1
C379 4700P-04-O
ER18 887-1-04
Rup
R530 976-1-04
Rdown
+5VSB
R929 1K-04-O
Q112_C
SLP4_L
R930 4.7K-04-O
Q112_B
Q112 2N3904-S-O
Q111 2N3904-S-O
209-01-18 open it, Vdimm disabled by GP40 in S4/S5
If Q111 stuff,lock P/N:03-070-590431/03-070-904053
9,20,26,34 SLP4_L SLP4_L

L8 RCK-0.5UD 08-020-504042
COMP_DDR R527 24K-04-O
DIMM_5VDUAL_input
EC61 1000U-6.3DL-J-O
EC56 560U-6.3D-OS-J
MC6 10U-16VX-08
Q64 MN252-9MS
L7 PIND1.5UD-20A 08-413-155096
+VDIMM
Default 1.527 V
OCP ~ 35.6A
Vout=Vref*(1+Rup/Rdown)
UPI6109&RT9214 Vref=0.8
UPI6103N Vref=0.6
Q60 MN252-6MS
R469 2.2-08
DIMM_PHASE_1
C353 4700P-04
EC57 1000U-6.3DL-J
MC14 10U-08-O
EC62 1000U-6.3DL-J
D_TG_1
R933 10K-04
2009-02-05 add for Protect Q64

OC1	OC2	PWM IC
* STUFF	NC	RT9214
NC	STUFF	UPI 6109

NB CORE_1P1V(+/-5%):22A

+VCC, +12V, +VCC3

R247 2.2
R248 2.2-O
L5 RCK-0.5UD 08-020-504042
NB_CORE_PWM_VCC
NB_CORE_VIN
D21 BAT54C-S
EC41 560U-6.3D-OS-J
EC43 1000U-6.3DL-J-O
MC2 10U-16VX-08
MC1 10U-16VX-08-O
C221 1U-X7R
U22 RT8105GS-S
GND VCC BOOT UGATE PHASE COMP/OCSET FB LGATE
BC44 1U-X7R-04
NB_BOOT_1
R536 0
NB_TG
R255 2.2
NB_TG_1
Q32 MN252-9MS
NB_PHASE
COMP_NB_CORE
OC3
R268 17.4K-1-04
NB_BG
R250 0
NB_BG_1
Q34 MN252-6MS
Q33 MN252-6MS-O
R269 2.2-08
NB_PHASE_1
C236 4700P-04
NB_CORE_FB
Rds(on)=7.3 mOHM ,OCP ~40.5A
OC4 R601 27K-04-O
20090318 change to 1uH from vendor suggestion
L6 PIND-1.0UD
+CORE_1P1V
OCP ~ 40.5A
+ICH_1P5V
D23 BAT54C-S
For power sequence
R272 1K-04-O
NB_CORE_FB_2
C244 4700P-04-O
ER6 732-1-04
Rup1
Vout=Vref*(1+Rup1/Rdown1)
ER5 1.8K-1-04
Rdown1
NB_TG_1
R934 10K-04
2009-02-05 add for Protect Q32
EC47 1000U-6.3DL-O
EC46 820U-2.5D-OS-J
C288 22U-08
C267 .1U-X7-04

*

	G41(ICH7)	Other	G45/G43
MCH	1.1V+/-5%	1.1V+/-5%	**1.125V+/-2.5%**
ICH	**1.05V+/-5%**	1.1V+/-5%	1.1V+/-5%

OC3	OC4	PWM IC
* STUFF	NC	RT9214
NC	STUFF	UPI 6109

FSB_VTT(1.2V):5.8A

20090324 change 3vsb to 5vsb For EuP
2009-03-20 change core_1p1v to 3vsb
+CORE_1P1V +5VSB, +3VSB, +VREF25_FSB, +12V, +VDIMM

R160 10K-04
R168 4.7K-04
R169 17.5K-04-O
ER2 11K-1-04
VREF_1P2V
Q23 2N3904-S
Q25 2N7002-S
C139 1U
ER3 10K-1-04
C128 1U-O
U17B OP358-S
Q30_G_1
R560 0-04
Q30_G
R173 10K-04-O
Q30 MN252-20MS P2003BDG
Pd(max)=1.74W
EC34 220U-16DE
+FSB_VTT
FSB_VTT_FB
R566 0-04
D19 BAT54C-S
+ICH_1P5V
C145 .1U-04-O
20090420 add for lenovo
EC37 1000U-6.3DL-J
For power sequence
+ICH_1P5V must power up before +FSB_VTT or after +FSB_VTT within 0.7V
+FSB_VTT must power down before +ICH_1P5V or after +ICH_1P5V within 0.7V

DDR_VTT:1.2A

20090324 change 3vsb to 5vdual for EuP lot6 requirement.
+VDIMM, +DDR_VTT, +VDIMM, +DIMM_5VDUAL

ER12 10K-1-04
DDR_VTT_REF
U30 9173DPSP-S
VIN VCNTL GND REFEN VCNTL REFEN VCNTL VOUT VCNTL
ER13 10K-1-04
BC75 1U
EC59 470U-6.3DE
EC58 470U-6.3DE
BC86 .1U-04

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1085 3VSB:3A

ICH7 VccSus3_3:0.7A
LAN: 0.2A
PCI:0.375A
PCIE1X:0.375*2=0.75A
PCIE16X:0.375A

+5VSB → U36 ADJ1085-S (IN, OUT, ADJ) → +3VSB
Vout=1.25(Ra+Rb)/Ra
Minimum Load Current:Ilmin=10mA
Ra ER29 110-1-04
Rb ER30 180-1-04
EC63 100U-16DE-O, C837 .1U-04, EC64 100U-16DE

HDMIi

2009/03/13 add for VccSusHDA
R641 1.3k-1-04-O, Q92_B, Q92 PMBT2222A-S-O, C515 .1U-04-O, R649 2k-1-04-O, +1P5_SB
20090421 change R value for Vbe=0.52V

1P5SB:17MA

U38 02-348-179840 RT9179PB-O (VIN, VOUT, EN, GND, ADJ) 300MA
Vout=1.175(Ra+Rb)/Rb
Ra R564 27.4k-1-04-O, MC16 10U-08-O
Rb R565 100k-1-04-O
1P5_SB_ADJ
20090325 co-layout

3VSB PWM circuit for EuP lot6 requirement.

U37 UP6107-O (GND, VCC, BOOT, UGATE, PHASE, POK/EN, FB, LGATE)
3VSB_PWM_VCC, BC101 1U-X7R-O
D38 BAT54C-S-O, R517 2.2-O
3VSB_boot_1, R943 10K-04-O, 3VSB_TG_1
3VSB_boot, R551 2.2-O, BC102 1U-X7R-04-O
3VSB_TG, R561 0-O, 3VSB_TG_1
3VSB_PHASE
COMP_3VSB, R562 10K-04-O
3VSB_BG, R559 0-O, 3VSB_BG_1
3VSB_FB, R944 27K-04-O
Q2A FDS8984-O, Q2B FDS8984-O
FB24 FB120P-08-O
3VSB_5VSB_input
MC8 10U-08-O, MC9 10U-08-O, MC7 10U-08-O
L11 CK-4.0UD-O
MC15 10U-08-O, EC66 1000U-6.3DL-J-O
R489 2.2-08-O, C430 4700P-04-O, 3VSB_PHASE_1
ER21 2k-1-04-O, Rup
R558 1K-04-O, 3VSB_FB_1, C431 4700P-04-O
R563 630-1-04-O, Rdown
Vout=0.8*(1+Rup/Rdown)
20090325 co-layout

ICH_1P5V:~2A

(For USB/SATA/PCIE/DMI)

Pd(max)=36mW

R513 10K-04-O, R511 10K-04-O, Q65 2N3904-S-O, C378 1U-O
ER19 20K-1-04-O, 2009-03-20 ADD, ER16 10K-1-04-O, Q61 2N3904-S-O, ER14 16.2K-1-04-O, C363 1U-O
VREF_ICH_1P5V
U29B OP358-S
Q59_G_1, R567 0-04-O, Q59_G
R470 10K-04, Q59 MN252-9MS 2SK3918-2K-S
R568 0-04-O, ICH_1P5V_FB
C364 .1U-04-O, MC5 10U-08-O, EC55 680U-4VDL
20090420 add for lenovo
20090430 change to 680u 04-731-687436/04-731-687432

CORE_1P05V:1.31A

Pd(max)=0.59W

ER20 5.4K-1-04-O, 2009-03-20 ADD, ER17 3.48K-1-04
VREF_CL1P1V
U29A OP358-S
Q58_G_1, R569 0-04, Q58_G_G
R482 4.7K-04, Q58 P3055LDG-S
C367 1U, ER15 2.49K-1-04
CORE_1P05V_FB, R570 0-04
C361 .1U-04-O, MC4 10U-08-O, EC51 680U-4VDL
SB_CORE +CORE_1P05V
20090420 add for lenovo
20090430 change to 680u 04-731-687436/04-731-687432

VREF25:0.1A

+VREF25 R401 Short PAD +VREF25_FSB
C377 .1U-04-O
+VCC3 R510 220 GS431BWS Q69 431-S
20090319 change 5vsb to vcc3

+FSB_VTT R376 10K-04, +5VSB R394 10K-04, +FSB_VTT R386 1K-04
Q48_C, Q48_B, Q48 2N3904-S, C300 1U
Q47 2N7002-S 20090325 3904 To 2N7002
VCORE_EN → VCORE_EN 31
DELAY 10 ms

+VREF25_FSB, ER28 10K-1-04-O, ER27 15K-1-04-O, C448 1U-O
VSFR_1P5_REF, U17A OP358-S, VSFR_1P5_FB
Q79_G_1, R571 0-04-O, Q79_G_G, Q79 2N7002-S-O, R579 0-04-O
C449 .1U-04-O, MC12 10U-08-O
20090420 add for lenovo

+12V R519 100-2512-2W-O, Q120_D, Q120 2N7002-S-O
26,28 ATX_PSON → ATX_PSON_L
09/02/06 Dummy Load for Power

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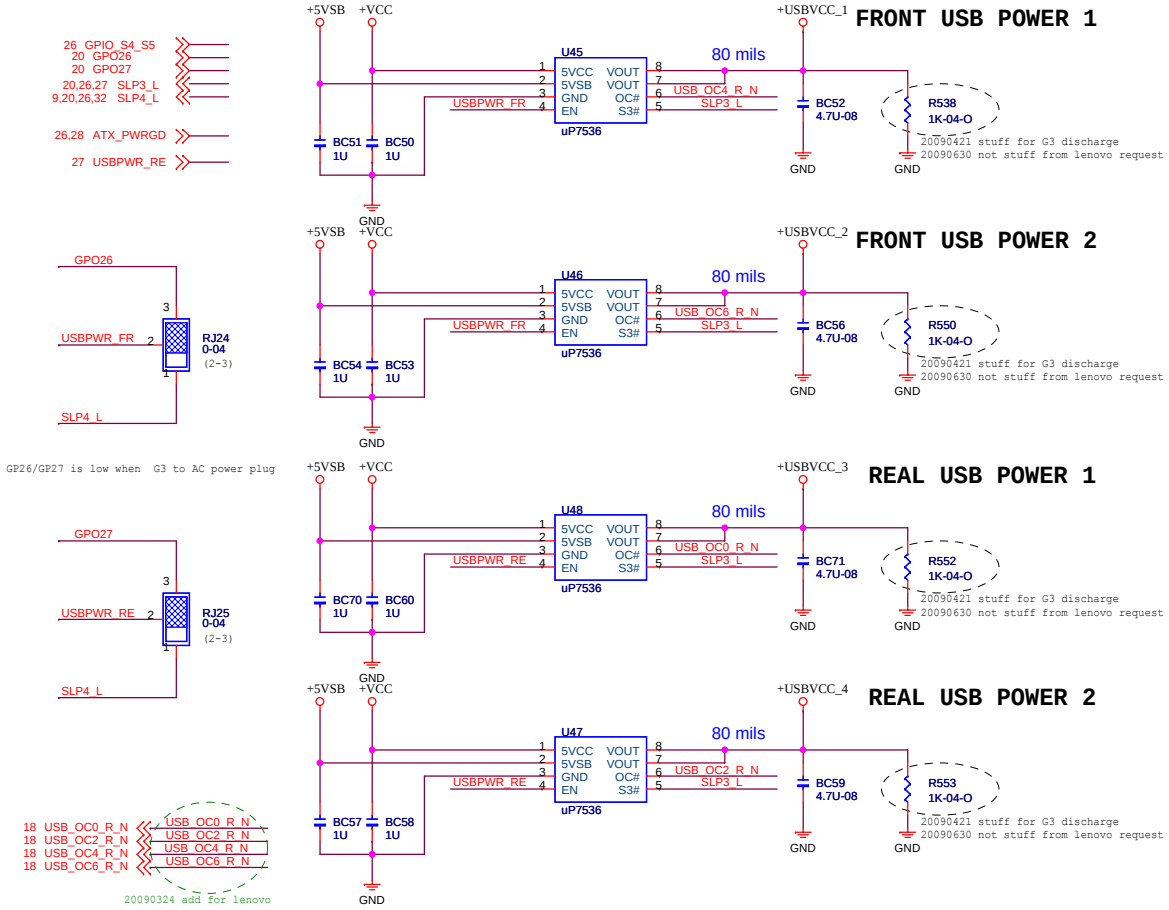

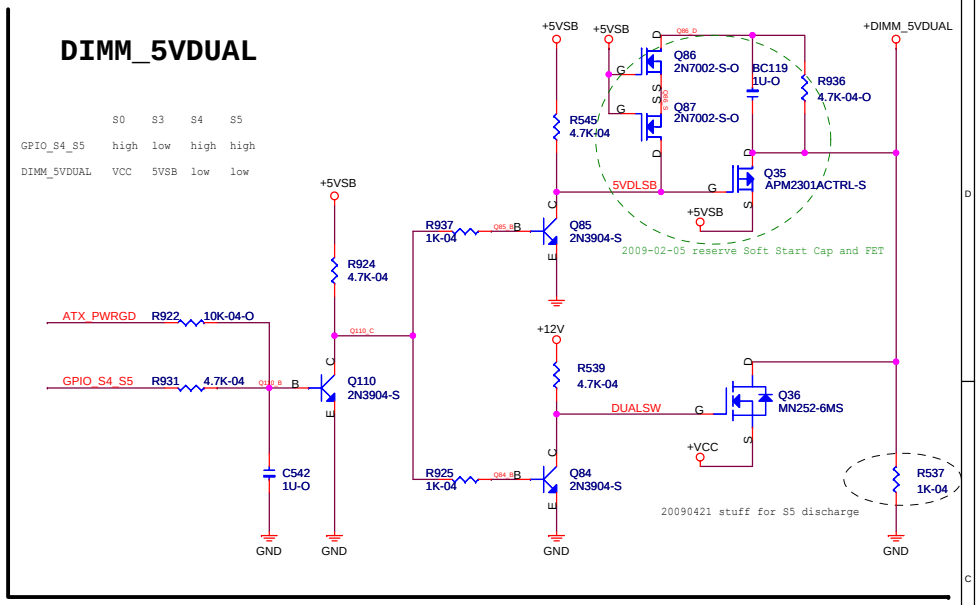

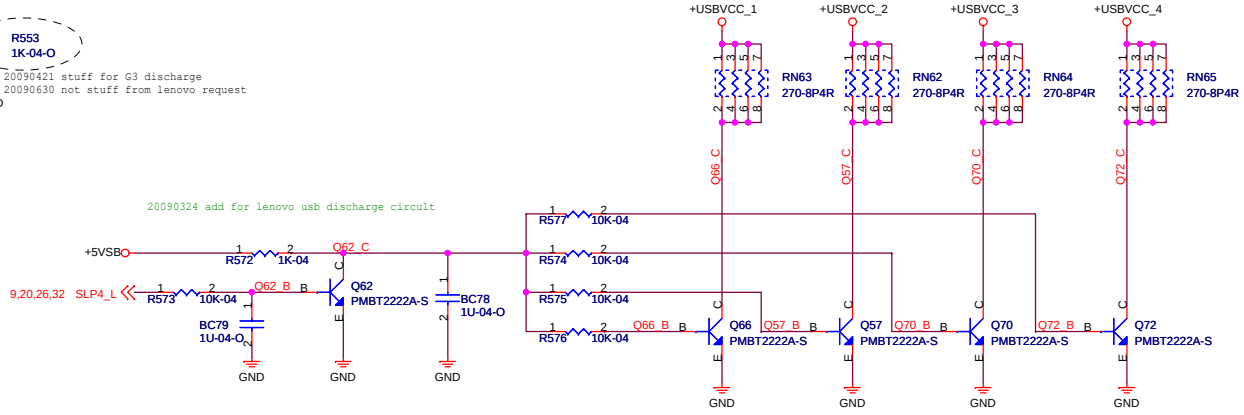

remove the PSI# errata circuit (G41 not support C3/C4)

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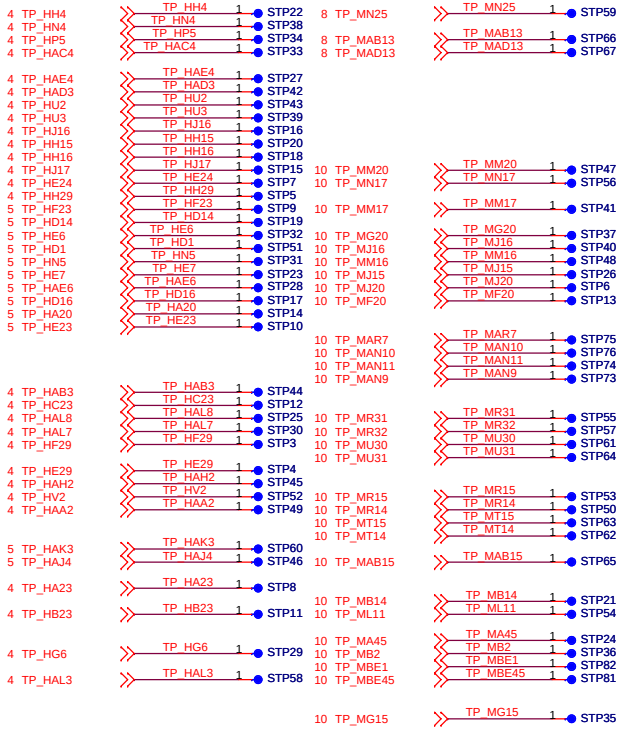

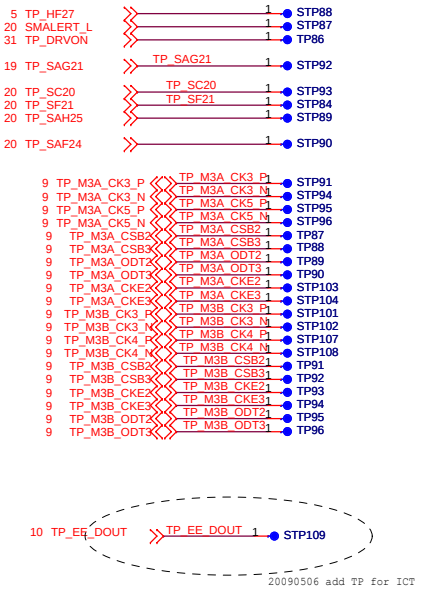

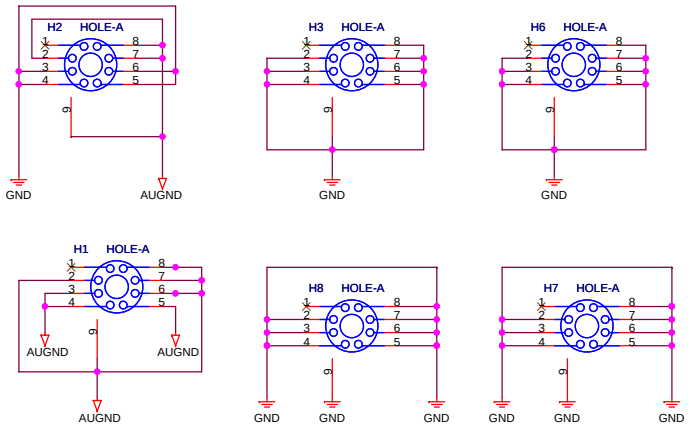

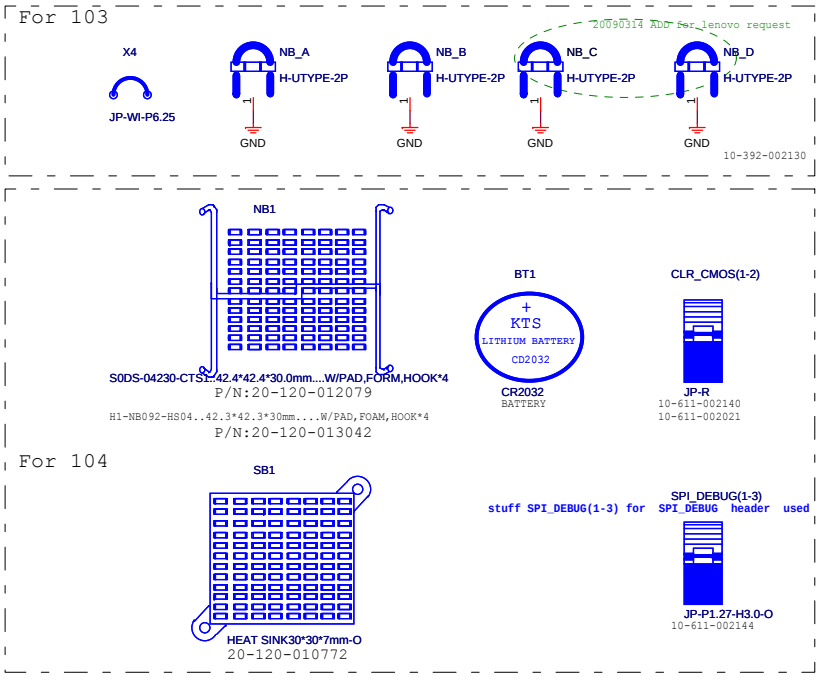

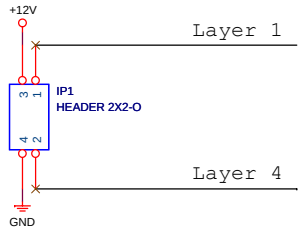

1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

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Title: TEST POINT & OTHER

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