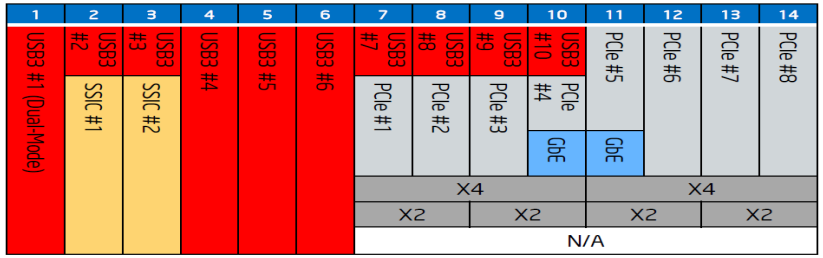
H11H4-AD2

V:1.1

ECS CONFIDENTIAL

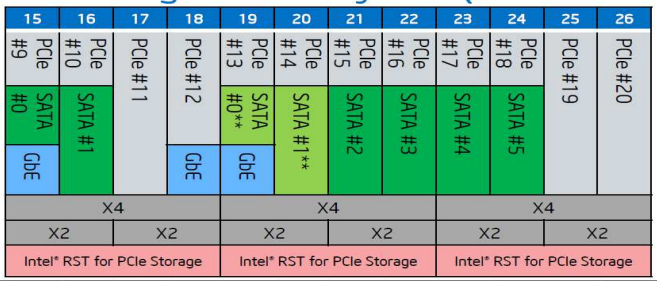
SCHEMATICS TABLE:

HSIO Lane Assignements by SKU (Lanes 1-14)



sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe /LAN	PCIe	PCIe	PCIe

HSIO Lane Assignements by SKU (Lanes 15-26)



Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
Q150	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3
Q170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

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Title	Cover Page
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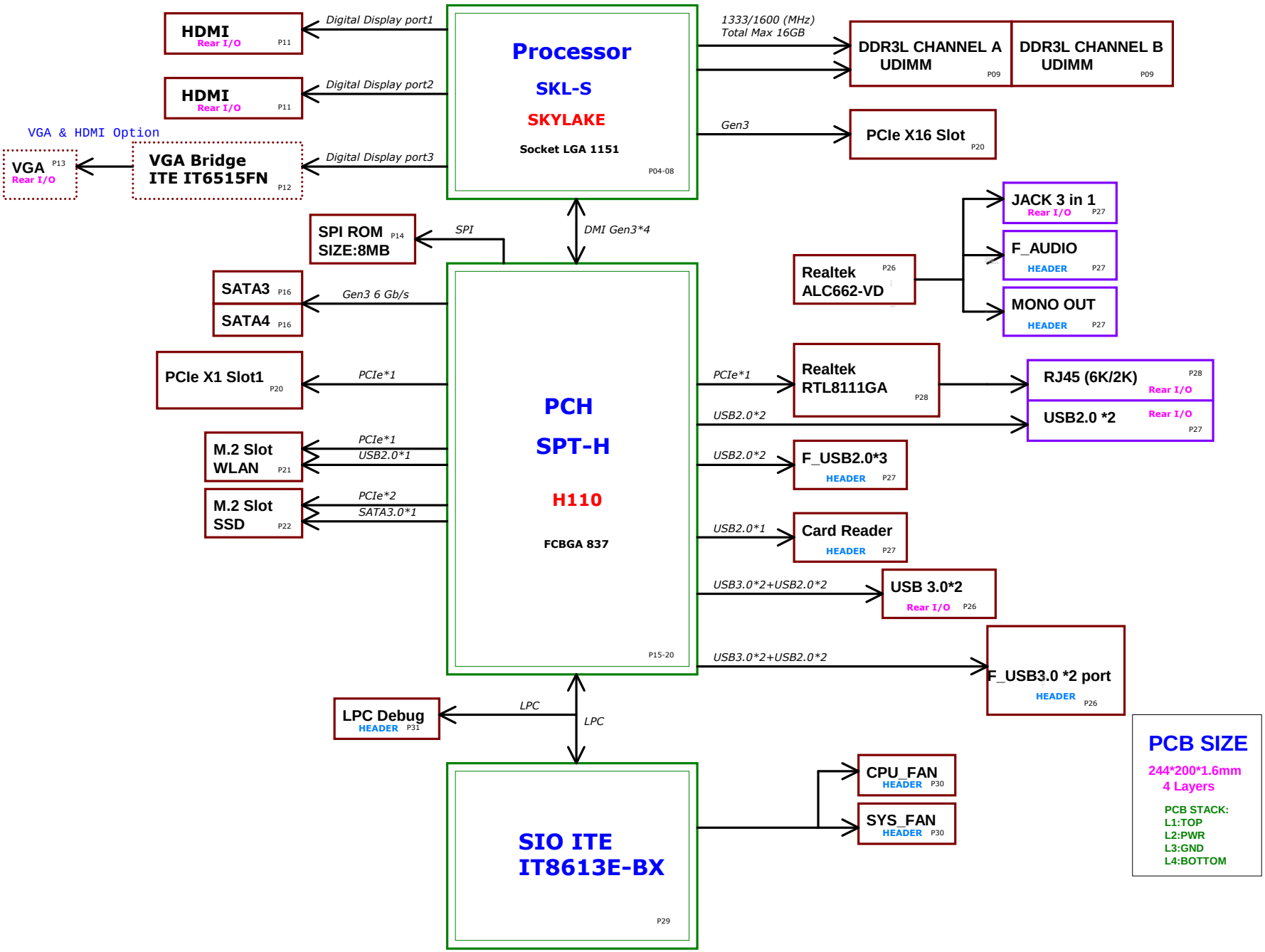
Skylake-S Desktop Platform



Elitegroup Computer Systems			
Title: Block Diagram			
Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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PCH-GPIO function

Data:2014/11/28

Pin Name	Power Well	Usage	Boot Set
GPP_F17	3VSB	LPC_PME_L	PME#
GPD10	ATX_3VSB	GPD10_DIS_ME	GPO
GPP_B13	N/A	PCH_PLTRST_L	PLTRST#
GPP_G16	3VSB	IOAC	GPO
GPP_G13	VCC3	HDPANEL_DETECT	GPI
GPP_E7	VCC3	THERMAL_SD	GPI
GPP_B3	3VSB	BT_DIS_L_R	GPO
GPP_H18	3VSB	GPP_H18	GPI
GPP_H17	3VSB	GPP_H17	GPI
GPP_H16	3VSB	GPP_H16	GPI
GPP_H15	3VSB	GPP_H15	For Acer Reserve
GPP_H14	3VSB	GPP_H14	For Acer Reserve
GPP_B14	+VCC3	PCH_SPKR	SPKR
GPP_A14	3VSB	LPCPD_L	SUS_STAT#
GPP_C6	3VSB	SML1_CLK	SML1CLK
GPP_C7	3VSB	SML1_DATA	SML1DATA
GPP_E8	VCC3	SATALED_L	SATALED#
GPP_E0	VCC3	SSD_DETECT_L	GPI
GPP_E4	VCC3	DEVSLP0	SATA_DEVSLP0
GPP_F22	VCC3	PCIEX16RST	GPO
GPP_F14	3VSB	H_SKTOCC_L	GPI
GPP_B17	3VSB	M.2_DIS_L_R	GPO
GPP_B6	VCC3	CLK_REQ1_M.2_WLAN_L	SRCCLKREQ1#
GPP_B8	VCC3	CLKREQ3_SSD_L	SRCCLKREQ3#

SIO-GPIO function

Data:2014/11/28

Pin Name	Power Well	Usage	Default SET
PCH_D0B/GP22	+ATX3VSB	Front Panel LED contral (SIO_LED1)	GPO
GP21	+ATX3VSB	Front Panel LED contral (SIO_LED0)	GPO
PCIRST1#/PCH_C0A/GP12	3VSB	SML1_CLK	PCH_C0A
VCORE_EN/GP42/ PCH_C0B/SUSWARN#	3VSB	SUSWARN_R	SUSWARN
DSR1#/GP45/PCH_D0A	3VSB	SML1_DATA	PCH_D0A
CTS1#/GP31/FAN_TAC5	VCC3	THERMAL_SD	GPO
VLDT_EN/SLP_SUS#/GP63	+ATX3VSB	SLPSUS_L	SLP_SUS#
SUSACK#/PWRGD1	3VSB	SUSACK_R	SUSACK#

Interrupt mapping

Data:2014/11/28

Function	INT# port	PCIe*1 port	Device
M.2(WLAN)	INTB#	Port 10	Wireless LAN
LAN	INTB#	Port 6	RTL8111GA
SATA	INTA#	NA	SATA3.0
M.2(SSD)	INTC#	Port 7	SSD
	INTB#	Port 8	
PCIeX1	INTA#	Port 5	PCIeX1

Strap Setting

Data:2014/11/28

Schematics Version History Table:

Data:2014/11/28

Rev.	Date	Page	Change list	Remark
B	20150121	7,38	C312,C301,C313,C302 ->Del:C39 .33U-10VX7-06 -> .22U-25VX7-06 R122 27.4K-1-04 -> 47.5K-1-04;R117 3.74K-1-04 ->4.99K-1-04 R111 56K-04 ->88.7K-1-04;C72 1200P-50VX7-04 -> 3300P-50VX7-04 C644 220P-50VX7-04 -> 330P-50VX7-04;R67 1K-1-04 -> 510-1-04	Vcore power solution.
	20150121	38,40	R165 11K-1-04 -> 15K-1-04; R175 7.5K-04 -> 36K-04 C175 1200P-50VX7-04 -> 560P-50VX7-04; R204 3.6K-04 -> 1K-04 C187 680P-50VX7-04->1800P-50VX7-04; R194 1K-04 -> 200-04 Del: SC35	VGT power solution.
	20150121	38,40	R196 3.3K-1-04 -> 4.99K-1-04; Del:SC22	VSA power solution.
	20150121	38	R165 11K-1-04 -> 15K-1-04; R175 7.5K-04 -> 36K-04 C175 1200P-50VX7-04 -> 560P-50VX7-04; R204 3.6K-04 -> 1K-04 C187 680P-50VX7-04->1800P-50VX7-04; R194 1K-04 -> 200-04	VCC leakage issue in sleep S3.
	20150121	38,41	R143 22K-04 -> unstuff; R323 unstuff -> 20K-04	VR_Ready sequence issue in Power on.
	20150121	41	R704 10K-04->4.99K-1-04; R693 4.7K-04->20K-1-04 R666 8.2K-04 -> 8.2K-1-04; R667 750-1-04 ->2.4K-1-04	VCCIO POWER Sequence isssue.
	20150121	41	L19 footprint CHOKE_1R5_SMD_2P change to CHOKE_PT5D45MM_SMD	NPI issue
	20150121	42	R398 unstuff->100K; R688 4.7K-> unstuff	VDIMM Power sequence issue
	20150121	42	L22,L23 BOM change from INC0809-1R0M-JY1W to INC0809-1R0M-JY1W	Power issue
	20150121	32	Add circuit for DPWROK & +ATX_3VSB power down sequence timing issue.	
	20150121	32	Add circuit for RSMRST & +V1P0A power down sequence timing issue.	
	20150121	11	Add C428,C398,C438 (22U-6V3X5-08)	VRFF DC noise.
	20150121	12	Add C47,C46,C31,C12 unstuff -> 470P-50VX7-04 Add reserve C56,C77,C95,C87	Solve DDC signal test fail.
	20150121	13,14,27 ,29,30	C14 unstuff -> 1U-6V3X5-04; C4 unstuff -> 4.7U-6V3X5-06 C14 · SC8 · SC7 · C3 · C468 · C629 · C122 · C284 · C120 · C97 · C117 unstuff -> .1U; C8 · C7 unstuff -> 27P-04; C51 unstuff -> 1U-6V3X5-04 C139~C146 unstuff -> 2.7P-04 L8 · L7 unstuff ->CMK-90-08-MUTI-TAITECH; C105,C118,C119Unstuff -> 470P-50VX7-04	EMI solution.
	20150121	26	U33 · U15 change from UP7556 to UP7537	Safety solution
	20150121	33	Q38 Pin change from LAN_LED0 to LAN_LED2.	Solve Front LAN LED issue
	20150121	33	C554 · C599 unstuff -> .1U-16VX7-04	Acer PUS AVLC request.
	20150121	39	Minimun Load circuit modify	
	20150121	21	Remove WLAN LED BOM	
	20150121	17,18	SC43,SC42 22P->15P; Add SR36 0-04 C588,C592 18P->15P; R662 22-04 -> 33-1-04 R722 22-04 -> 47.5-1-04	CLK solution
	20150121	15	R610 unstuff -> 1K-04 R597 1.2K-1-04 -> unstuff	MOW 04 Update
C	20150302	6	R273 22-04 ->20-04	Follow PDG
	20150302	12,14	C77 · C86 · C87 · C95 unstuff -> 10P-04;C16 unstuff -> 1000P-50VX7-04 C30 unstuff -> .1U-25VX5-04;	EMI solution.
	20150302	14	C8 · C7 unstuff -> 27P-04;R722 47.5-1-04 -> 56-1-04	SI solution.
	20150302	16,24	Add PCIeX16/X1 PRSNT# circuit	CLK Auto detect
	20150302	22	PCIe Port 7 · 8 Sawp for PCI Express Controller Lane Reversal	Follow PDG1.5 Update
	20150302	22	Remove LAN Power circuit.	By EuP test PASS
	20150302	37	Add C558,C645 10U	220W PSU noise solution
	20150310	7,38~42	Power cost down	
	20150302	43	R440 4.7K-04 -> unstuff for +3VSB leakage solution in EuP mode .	

Schematics Version History Table:

Data:2014/11/28

Rev.	Date	Page	Change list	Remark
1.0	20150518	13,14	VGA change to Reserve	
	20150518	12	C31,C12,C46,C47 unstuff -> 470P-50VX7-04	HDMI DDC sloution for SI test.
	20150518	15	R610 1K-04->unstuff;R597 unstuff -> 1.21K-1-04	For PCH QS pull-down 1.21K
	20150518	17,32	R662 33-1-04 -> 56-1-04;C613 unstuff -> 10P-04	24M CLK solution for SI test.
	20150518	32	Reserve RSMRST& Power down sequence circuit.	For tPCH21 power sequence pass.
	20150518	21	R357 unstuff ->10K-04;R432 unstuff->0-04 R426 unstuff->0-04	Auto control CLK
	20150518	15	ME test · SPI_Debug · LPC_Debug header change to Reserve.	MP request
	20150518	37	C598 unstuff ->.1U-16VX7-04;C531 unstuff->.22-16VX5-04 C596 unstuff ->.1U16VX7-04	EMC solution
	20150518	39	Z2,Z3 footprint change to short pad.	
	20150518	32	R639 change from 4.7k to 510 for tPCH16 of B BOM issue.	

Elitegroup Computer Systems

Title: GPIO FunctionINT# Mapping

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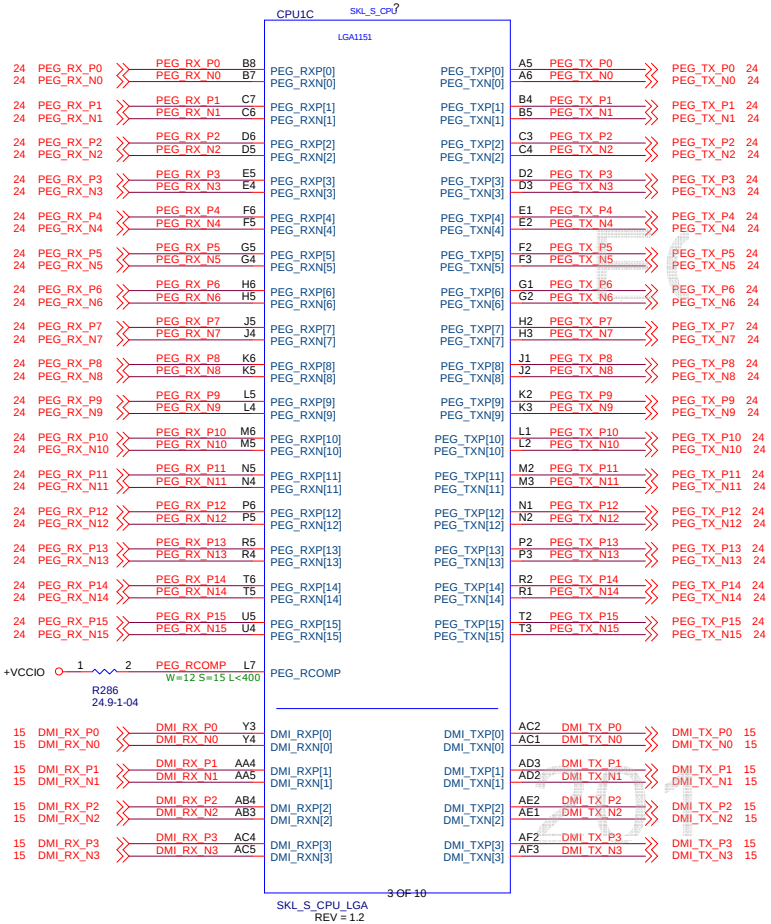

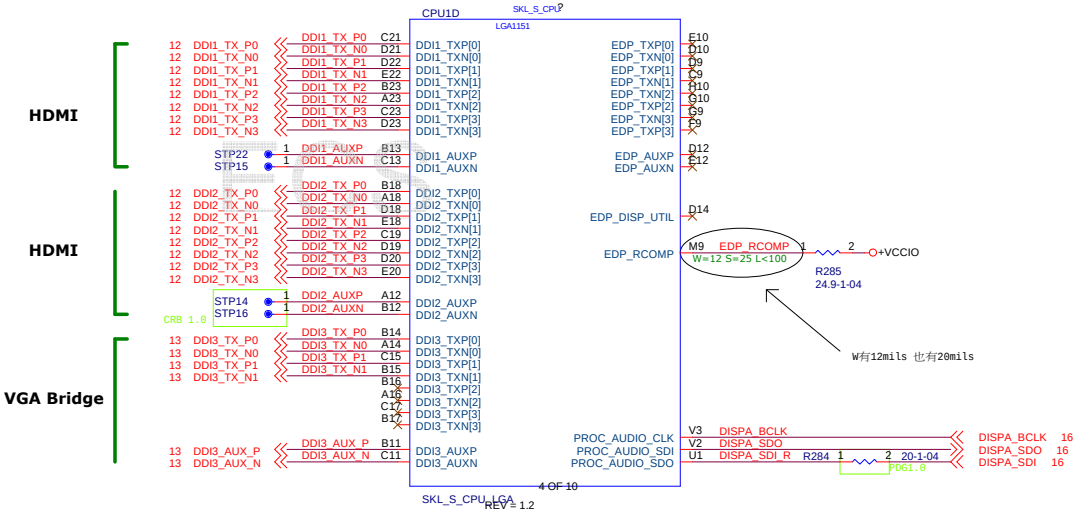

Elitegroup Computer Systems			
Title: CPU-PEG/DMI/DDI/EDP			
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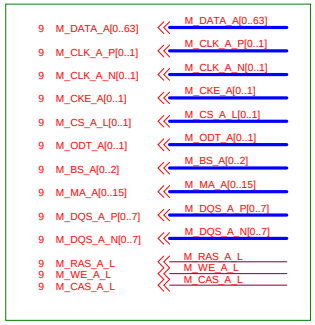
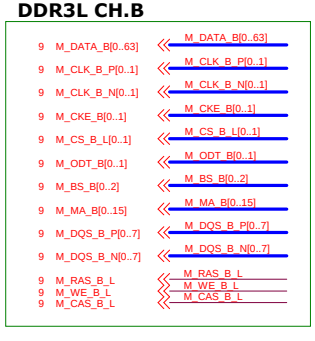
DDR3L CH.A

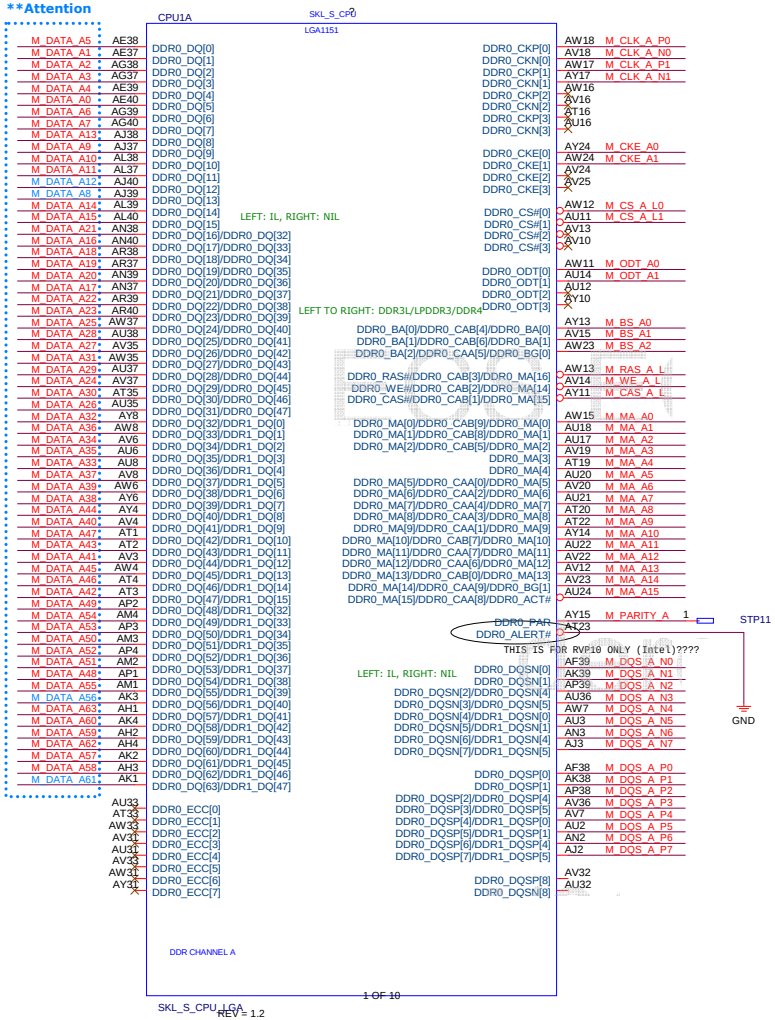


DDR3L CH.B



Follow DDR4 RVP8 CRB

**Attention



Follow DDR4 RVP8 CRB

**Attention

Elitegroup Computer Systems			
Title: DDR4			
Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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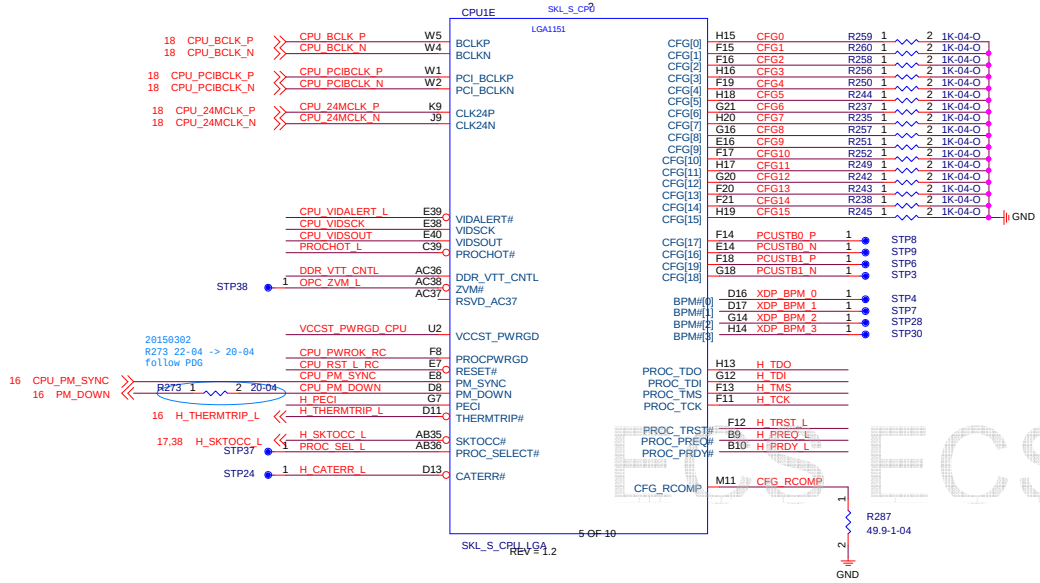
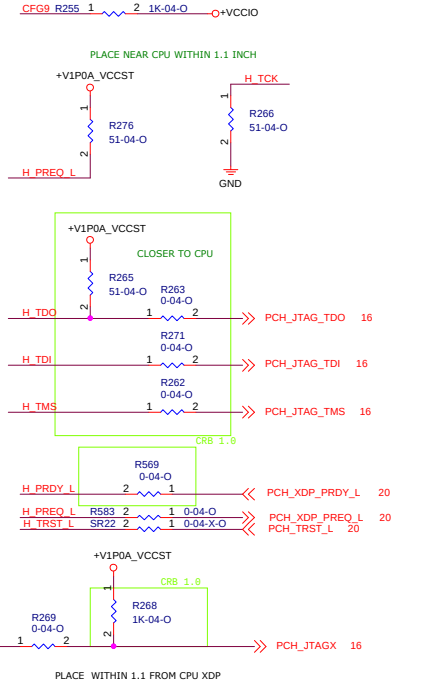
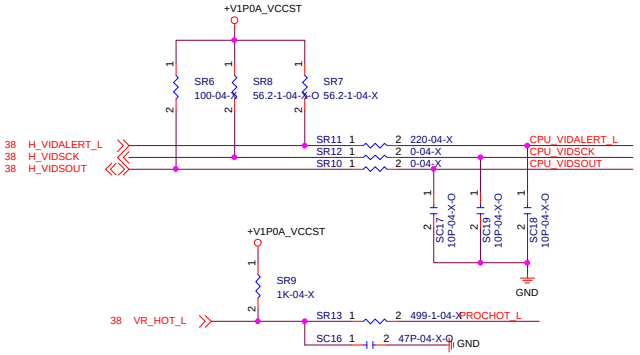


CFG[0:15] Configuration note

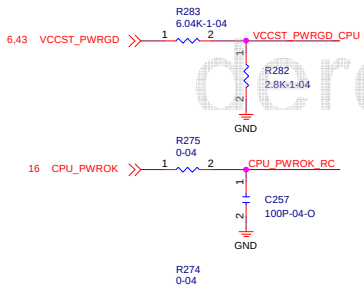
- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]:** Reserved configuration lane.
- **CFG[4]:** eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]:** PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]:** Reserved configuration lanes.



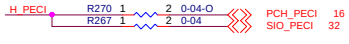
Asynchronous & Sideband Signal



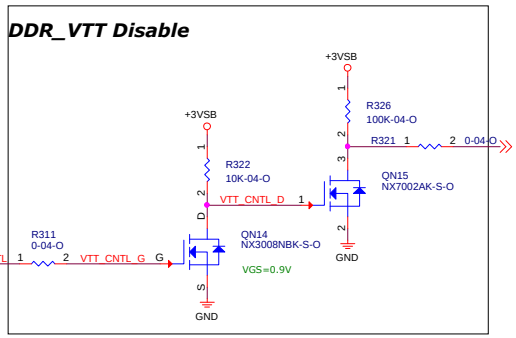
Processor Power Good



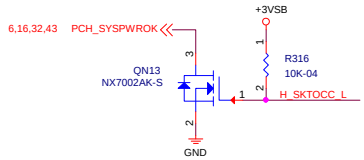
PECI



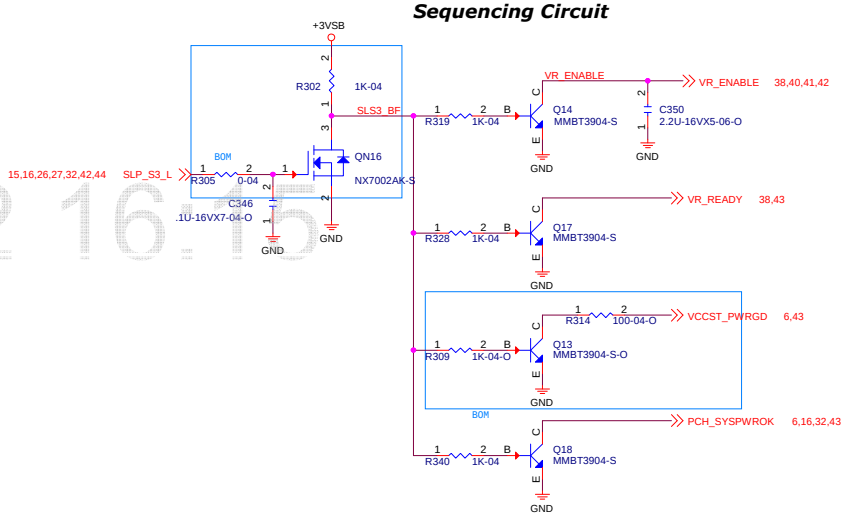
DDR_VTT Disable



SKTOCC#



Sequencing Circuit



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Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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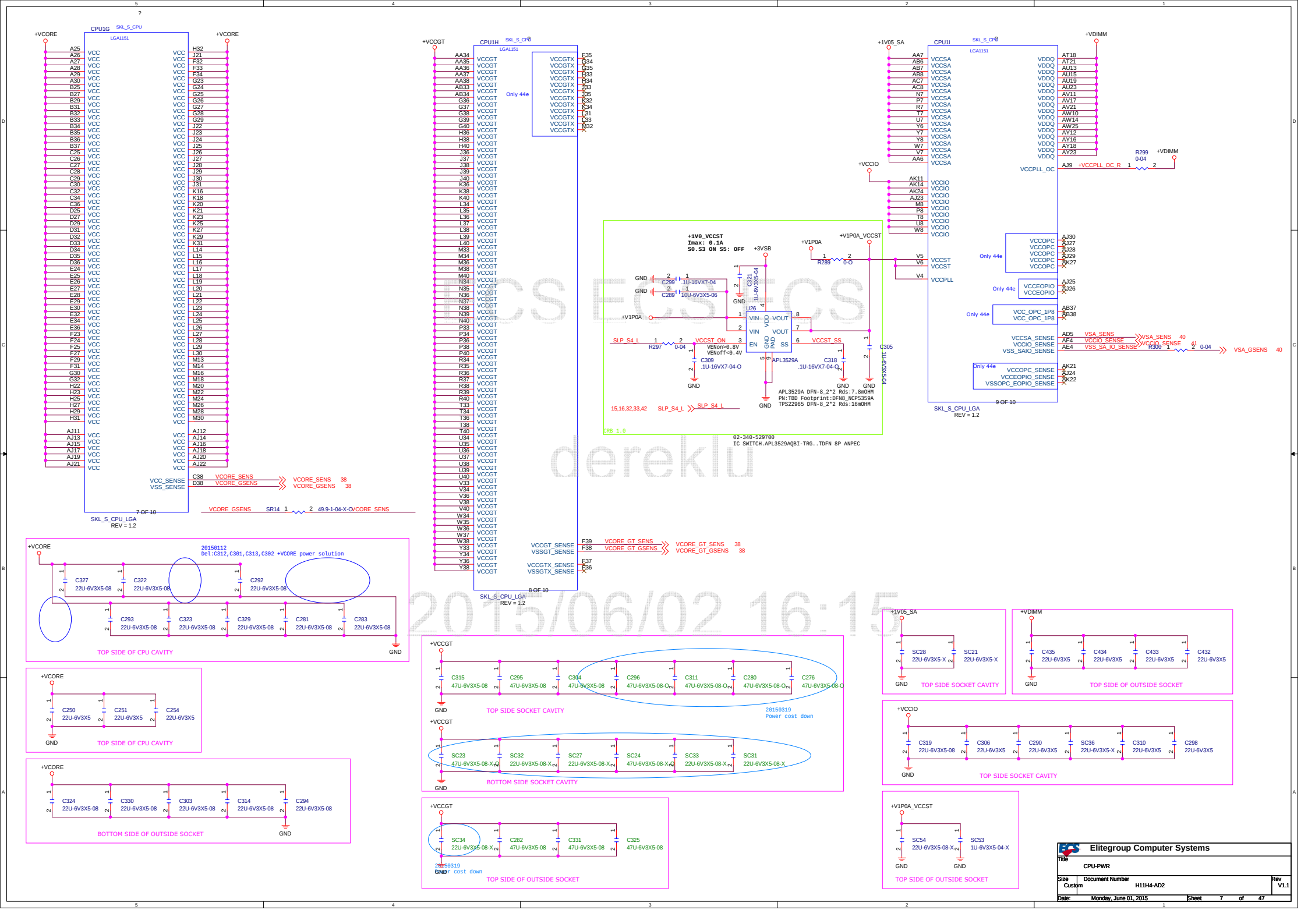
CPU1G
SKL_S_CPU
LGA1151
+VCORE
7 OF 10
SKL_S_CPU_LGA
REV = 1.2
VCC_SENSE
VSS_SENSE
VCORE_SENS
VCORE_GSENS
VCORE_SENS 38
VCORE_GSENS 38
VCORE_GSENS
SR14
49.9-1-04-X-O
VCORE_SENS
CPU1H
+VCCGT
Only 44e
8 OF 10
VCCGT_SENSE
VSSGT_SENSE
VCCGTX_SENSE
VSSGTX_SENSE
VCORE_GT_SENS
VCORE_GT_GSENS
VCORE_GT_SENS 38
VCORE_GT_GSENS 38
CPU1I
+1V05_SA
+VDIMM
VCCPLL_OC
+VCCPLL_OC_R
R299
0-04
+VCCIO
VCCOPC_SENSE
VCCEOPIO_SENSE
VSSOPC_EOPIO_SENSE
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VSA_SENS
VCCIO_SENSE
VSS_SA_IO_SENSE
VSA_SENS 40
VCCIO_SENSE 41
VSA_GSENS 40
9 OF 10
+1V0_VCCST
Imax: 0.1A
S0.S3 ON S5: OFF
+3VSB
+V1P0A
+V1P0A_VCCST
R289
0-O
C299
1U-16VX7-04
C289
10U-6V3X5-06
C321
1U-6V3X5-04
U26
APL3529A
VCCST_ON
VCCST_SS
SLP_S4_L
R297
0-04
C309
.1U-16VX7-04-O
C318
.1U-16VX7-04-O
C305
1U-6V3X5-04
VENon>0.8V
VENoff<0.4V
APL3529A DFN-8_2*2 Rds:7.8mOHM
PN:TBD Footprint:DFN8_NCP5359A
TPS22965 DFN-8_2*2 Rds:16mOHM
15,16,32,33,42
SLP_S4_L
CRB 1.0
02-340-529700
IC SWITCH.APL3529AQBI-TRG..TDFN 8P ANPEC
20150112
Del:C312,C301,C313,C302 +VCORE power solution
C327
22U-6V3X5-08
C322
22U-6V3X5-08
C292
22U-6V3X5-08
C293
22U-6V3X5-08
C323
22U-6V3X5-08
C329
22U-6V3X5-08
C281
22U-6V3X5-08
C283
22U-6V3X5-08
TOP SIDE OF CPU CAVITY
C250
22U-6V3X5
C251
22U-6V3X5
C254
22U-6V3X5
TOP SIDE OF CPU CAVITY
C324
22U-6V3X5-08
C330
22U-6V3X5-08
C303
22U-6V3X5-08
C314
22U-6V3X5-08
C294
22U-6V3X5-08
BOTTOM SIDE OF OUTSIDE SOCKET
C315
47U-6V3X5-08
C295
47U-6V3X5-08
C304
47U-6V3X5-08
C296
47U-6V3X5-08-O
C311
47U-6V3X5-08-O
C280
47U-6V3X5-08-O
C276
47U-6V3X5-08-O
TOP SIDE SOCKET CAVITY
20150319
Power cost down
SC23
47U-6V3X5-08-X-O
SC32
22U-6V3X5-08-X
SC27
22U-6V3X5-08-X
SC24
47U-6V3X5-08-X-O
SC33
22U-6V3X5-08-X
SC31
22U-6V3X5-08-X
BOTTOM SIDE SOCKET CAVITY
SC34
22U-6V3X5-08-X
C282
47U-6V3X5-08
C331
47U-6V3X5-08
C325
47U-6V3X5-08
TOP SIDE OF OUTSIDE SOCKET
SC28
22U-6V3X5-X
SC21
22U-6V3X5-X
TOP SIDE SOCKET CAVITY
C435
22U-6V3X5
C434
22U-6V3X5
C433
22U-6V3X5
C432
22U-6V3X5
TOP SIDE OF OUTSIDE SOCKET
C319
22U-6V3X5-08
C306
22U-6V3X5
C290
22U-6V3X5
SC36
22U-6V3X5-X
C310
22U-6V3X5
C298
22U-6V3X5
TOP SIDE SOCKET CAVITY
SC54
22U-6V3X5-08-X
SC53
1U-6V3X5-04-X
TOP SIDE OF OUTSIDE SOCKET
Elitegroup Computer Systems
Title
CPU-PWR
Size
Custom
Document Number
H11H4-AD2
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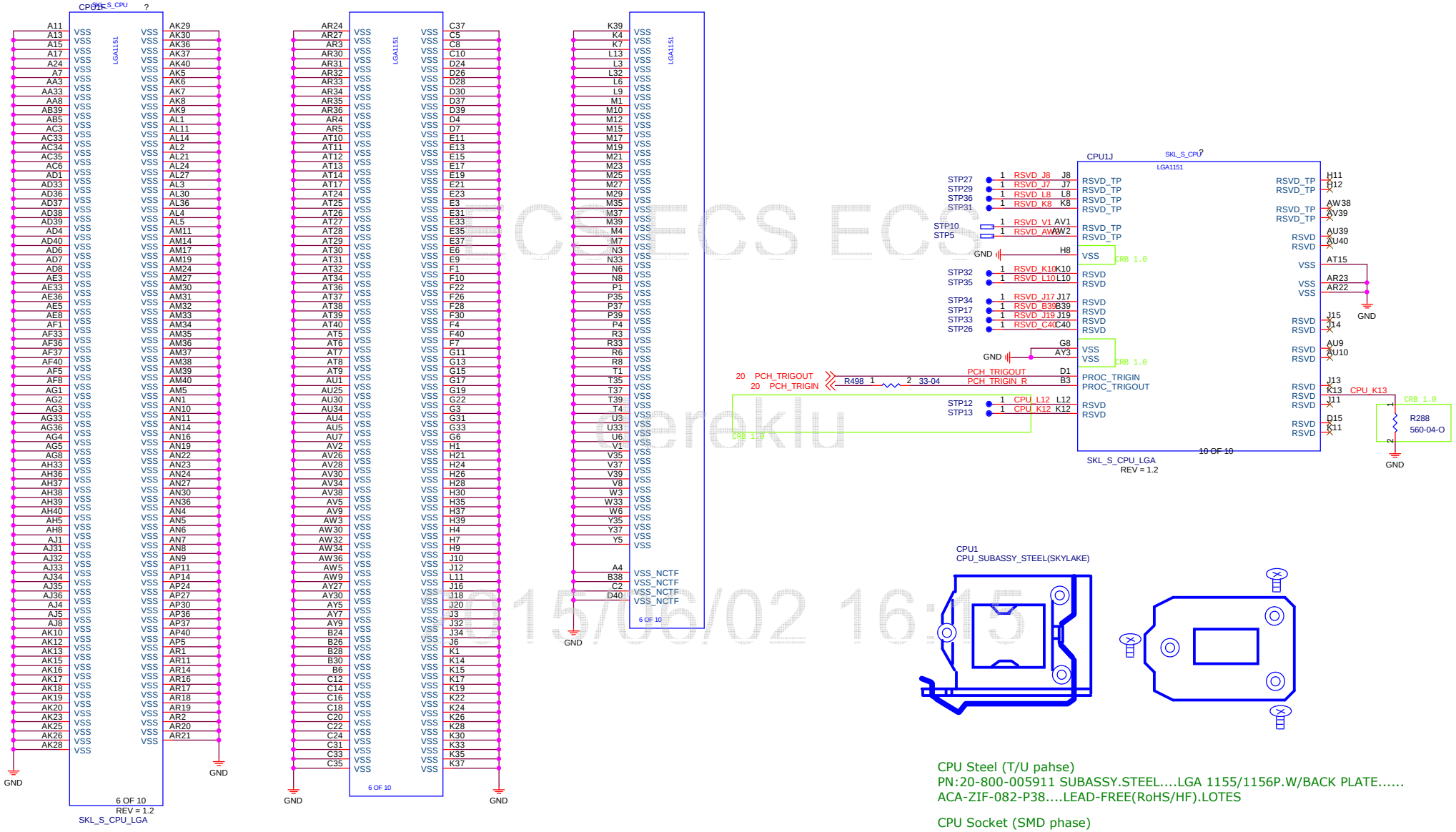
of
47



CPU Steel (T/U pahse)
PN:20-800-005911 SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....
ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES

CPU Socket (SMD phase)
PN:11-018-115133 SOCKET.CPU..LGA 1151P SMD..G/F...
BLACK.AZIF0049-P002C...HF.LEAD-FREE.LOTES

Elitegroup Computer Systems			
Title: CPU-GND			
Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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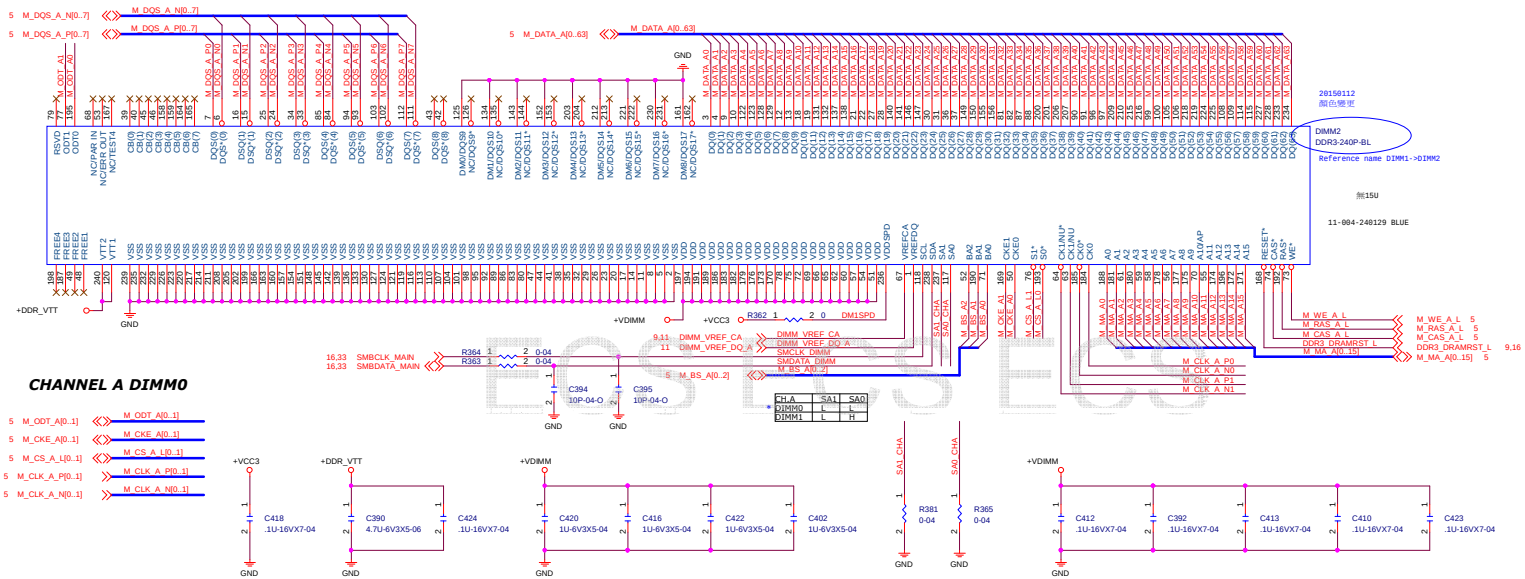
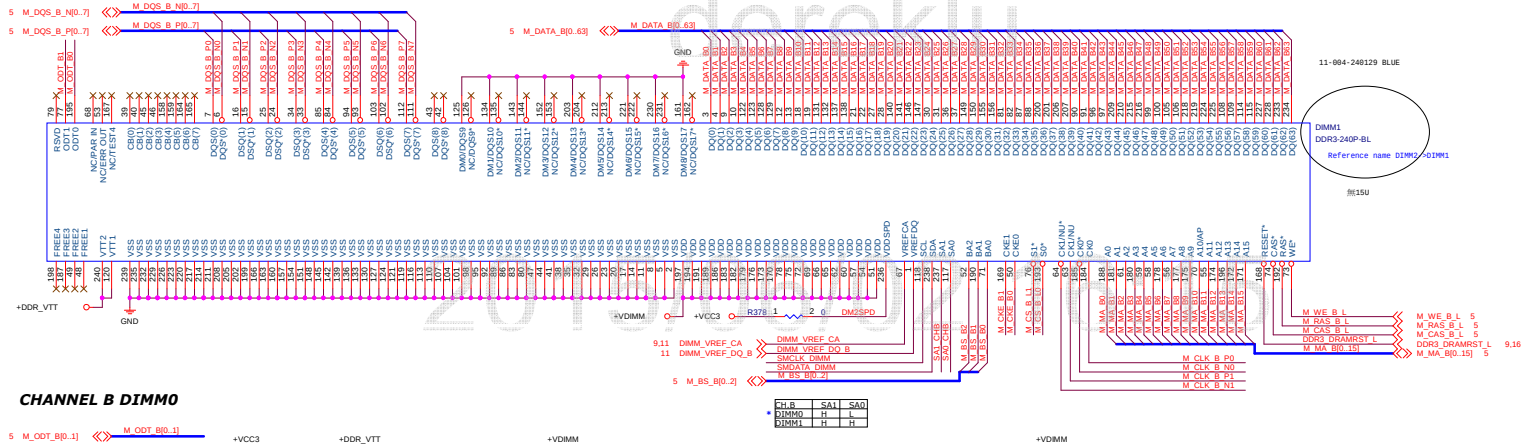
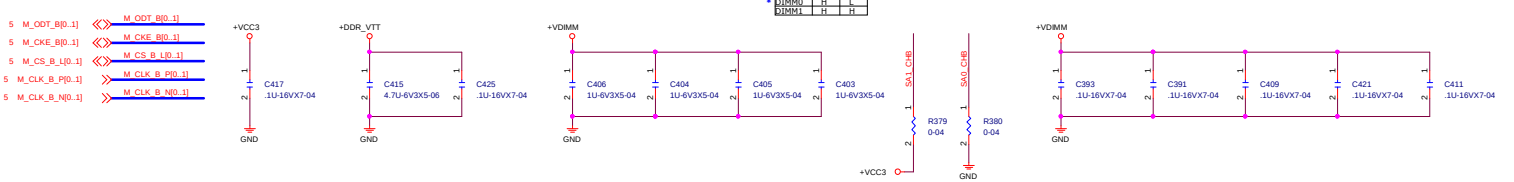


CHANNEL A DIMM0



CHANNEL B DIMM0



Elitegroup Computer Systems	
Title	DDR4-CHA
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Title: Reserve	
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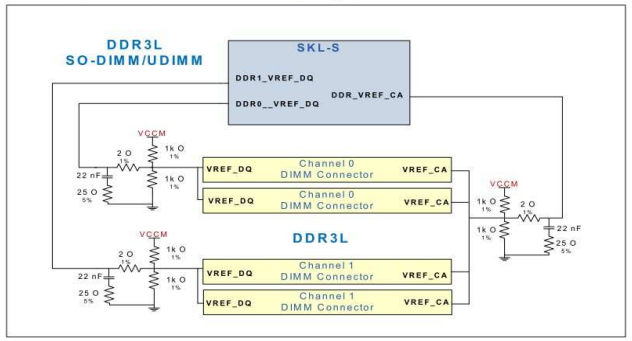
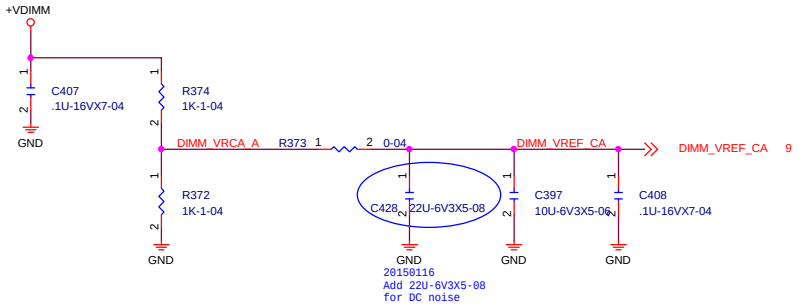
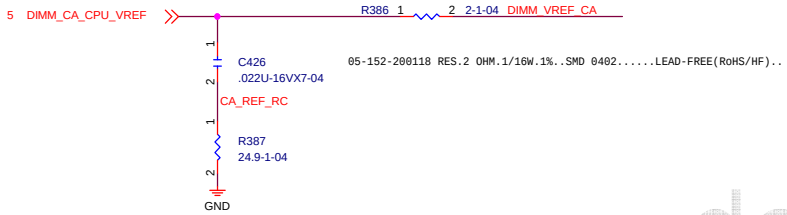
Figure 4-12. DDR3L SODIMM and UDIMM VREF Topologies

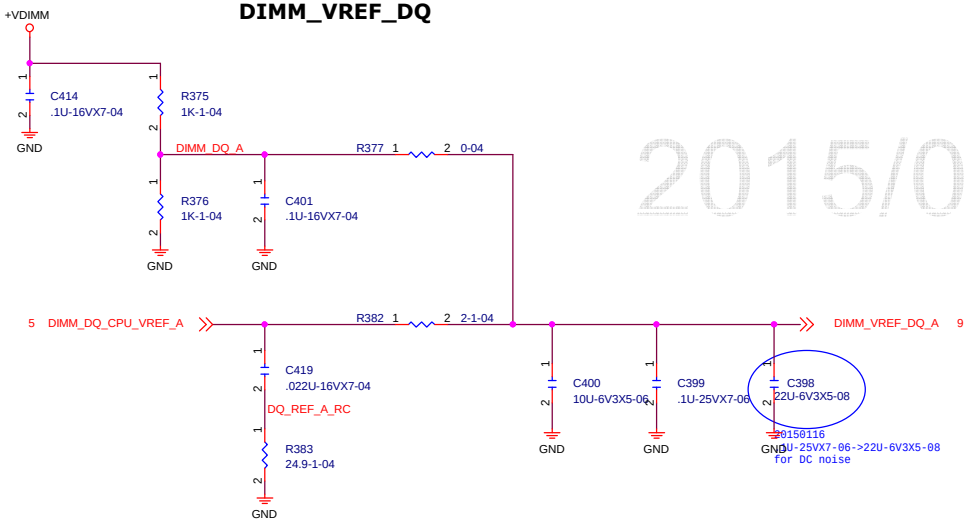


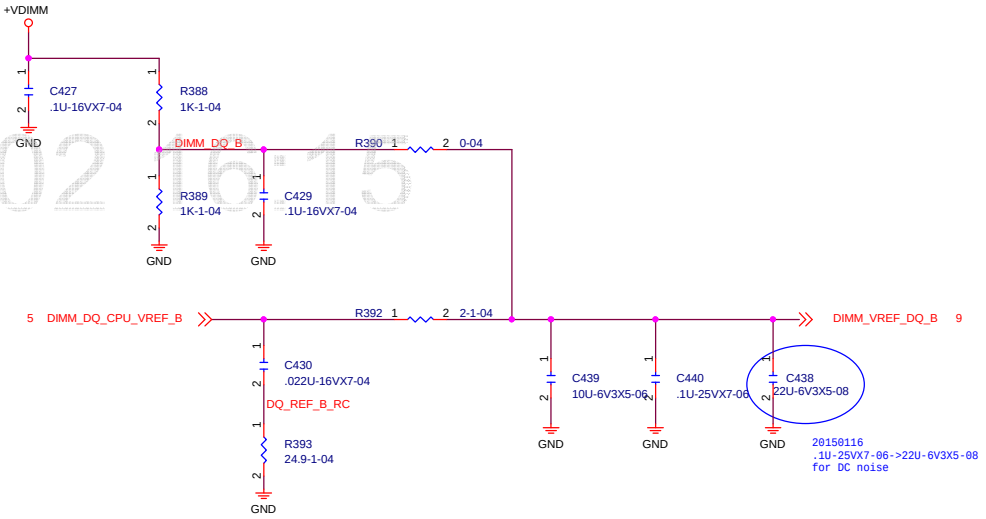


DIMM_VREF_CA



DIMM_VREF_DQ





Elitegroup Computer Systems		
Title: DDR3L-CHB		
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Port 2			
	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN

HDMI

HDMI的DDI_TX訊號,TX0和TX2必須交換1次

CRLS Support max data rate of 1.65 Gb/s

PN:10-083-019701
CONN.HDMI A-TYPE..19P 90D SMD
.....G/F..W/SCREW HOLE....1HD01911-51213...
HF.LEAD-FREE.HI-TOP

HDMI Connector Pin13:CEC
沒有使用必須空接(Floating)
避免HDCP 測試 FAIL

20150302
C87、C95 unstuff -> 10P-04
EMI solution

20150114
C31,C12,C46,C47 unstuff -> 470P-50VX7-04
for SI Issue

HDMI
(HDMI& VGA Option)

CRLS Support max data rate of 1.65 Gb/s

PN:10-083-019701
CONN.HDMI A-TYPE..19P 90D SMD
.....G/F..W/SCREW HOLE....1HD01911-51213...
HF.LEAD-FREE.HI-TOP

HDMI Connector Pin13:CEC
沒有使用必須空接(Floating)
避免HDCP 測試 FAIL

20150302
C77、C86 unstuff -> 10P-04
EMI solution

HDMI & VGA BOM Note
not floating

20150302
C16 unstuff -> 1000P-50VX7-04
EMI solution

Port 1			
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA

Elitegroup Computer Systems	
Title	HDMI*2
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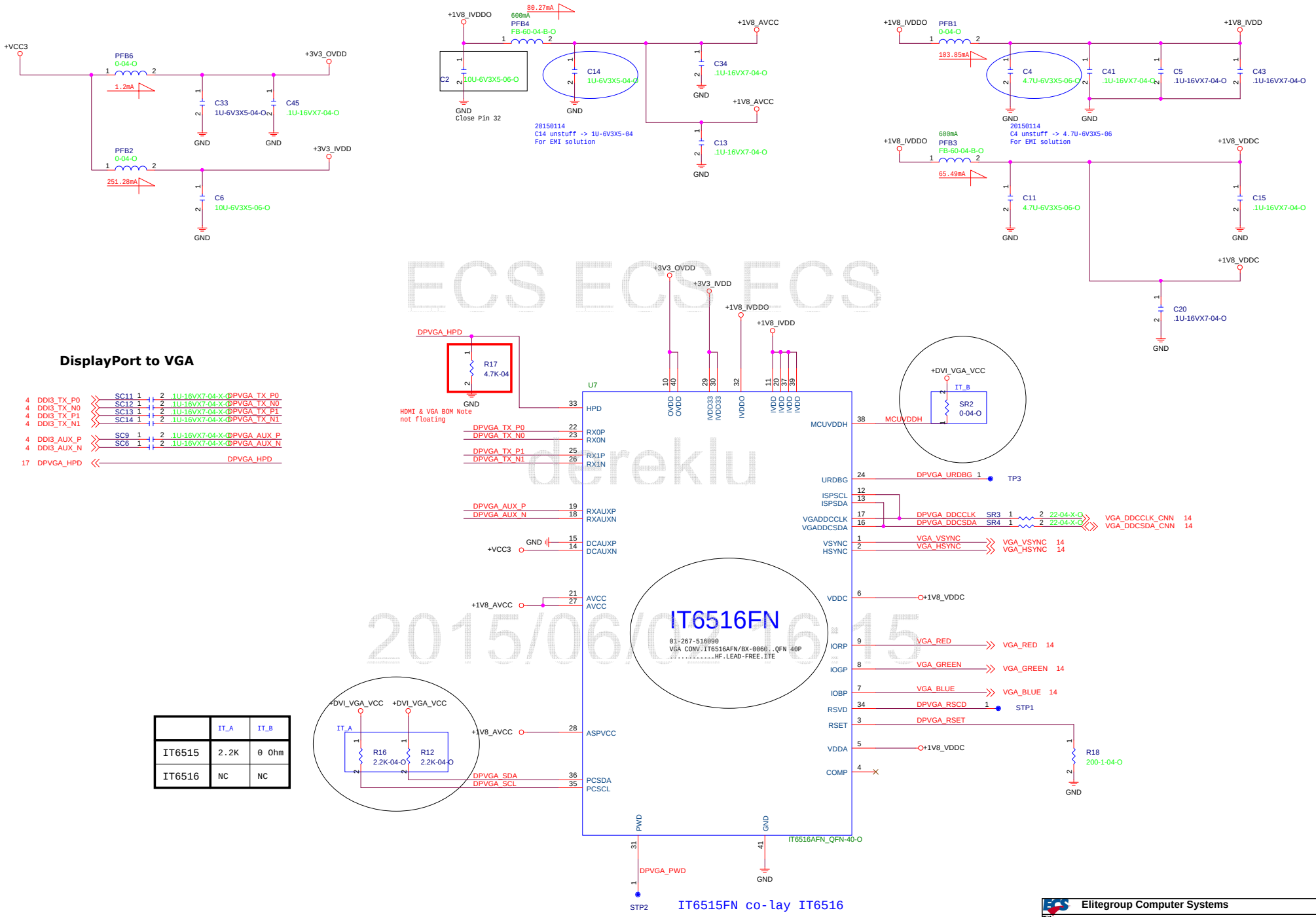

	IT_A	IT_B
IT6515	2.2K	0 Ohm
IT6516	NC	NC

Elitegroup Computer Systems		
Title: DP to VGA(IT6515)		
Size: Custom	Document Number: H11H4-AD2	Rev: V1.1
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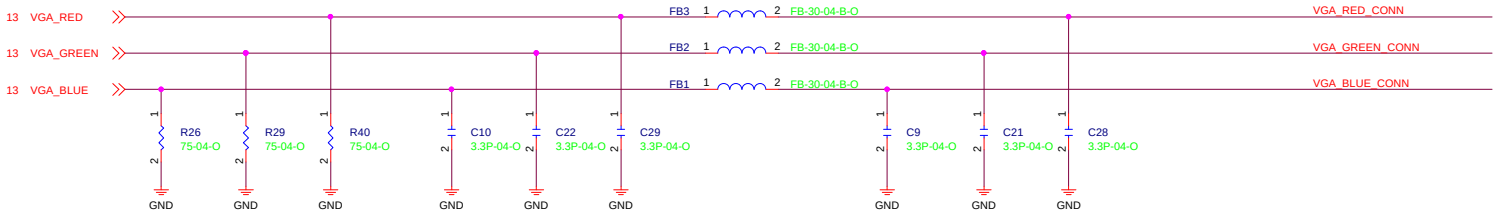
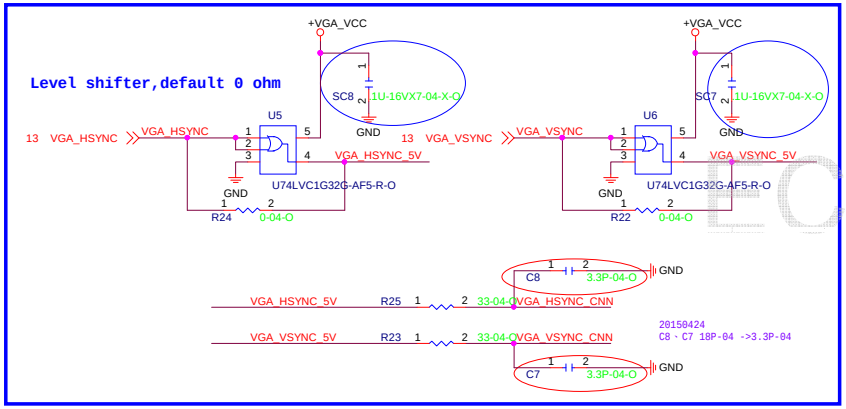
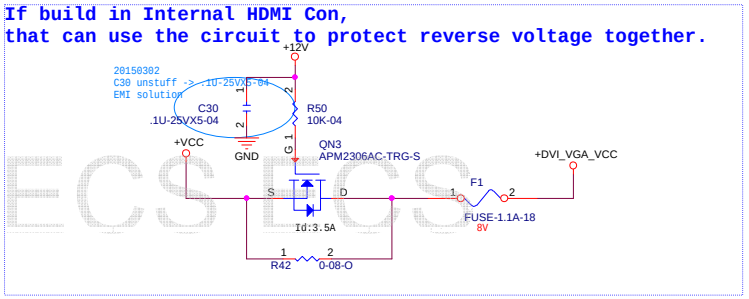
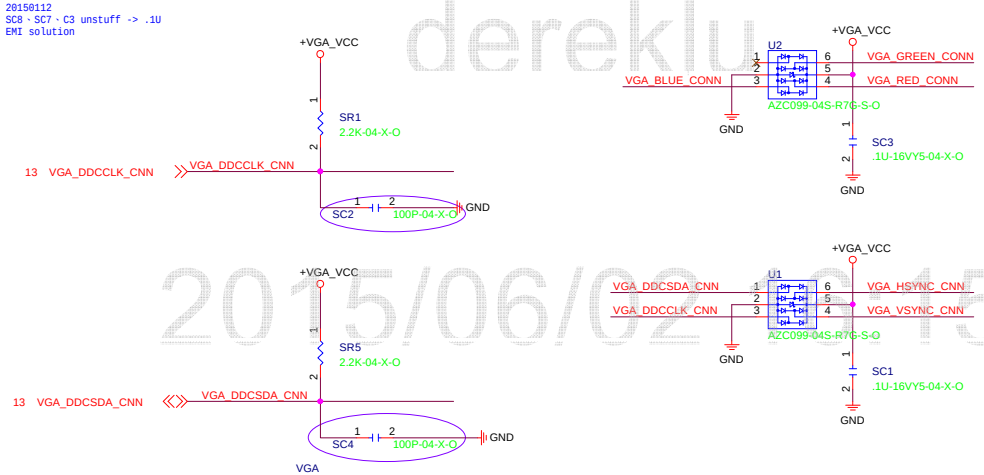
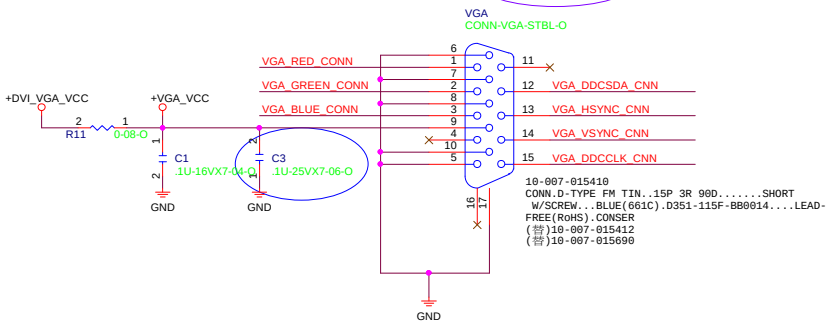
VGA (VGA & DP Option)











Elitegroup Computer Systems		
Title: VGA		
Size: Custom	Document Number: H11H4-AD2	Rev: V1.1
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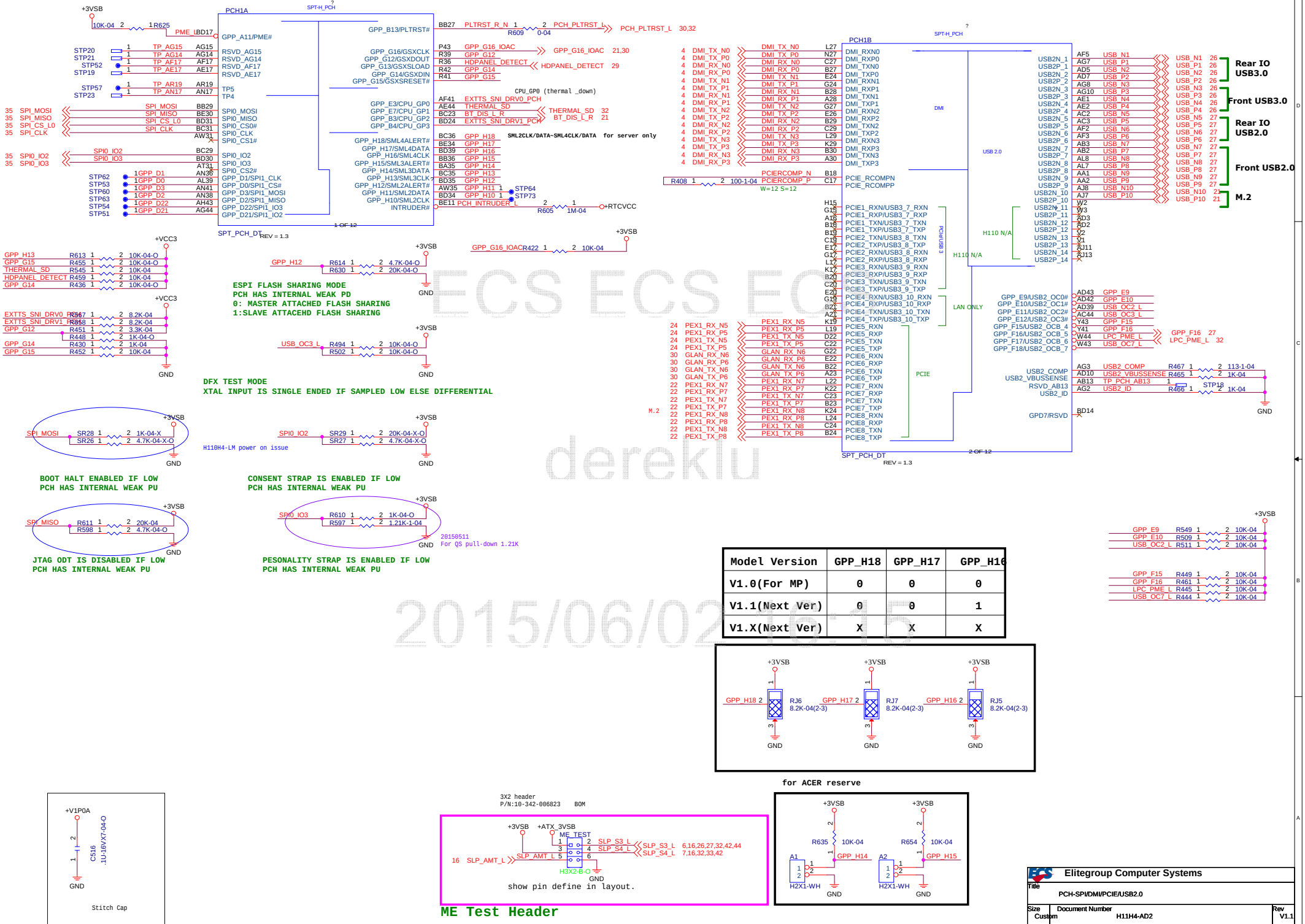
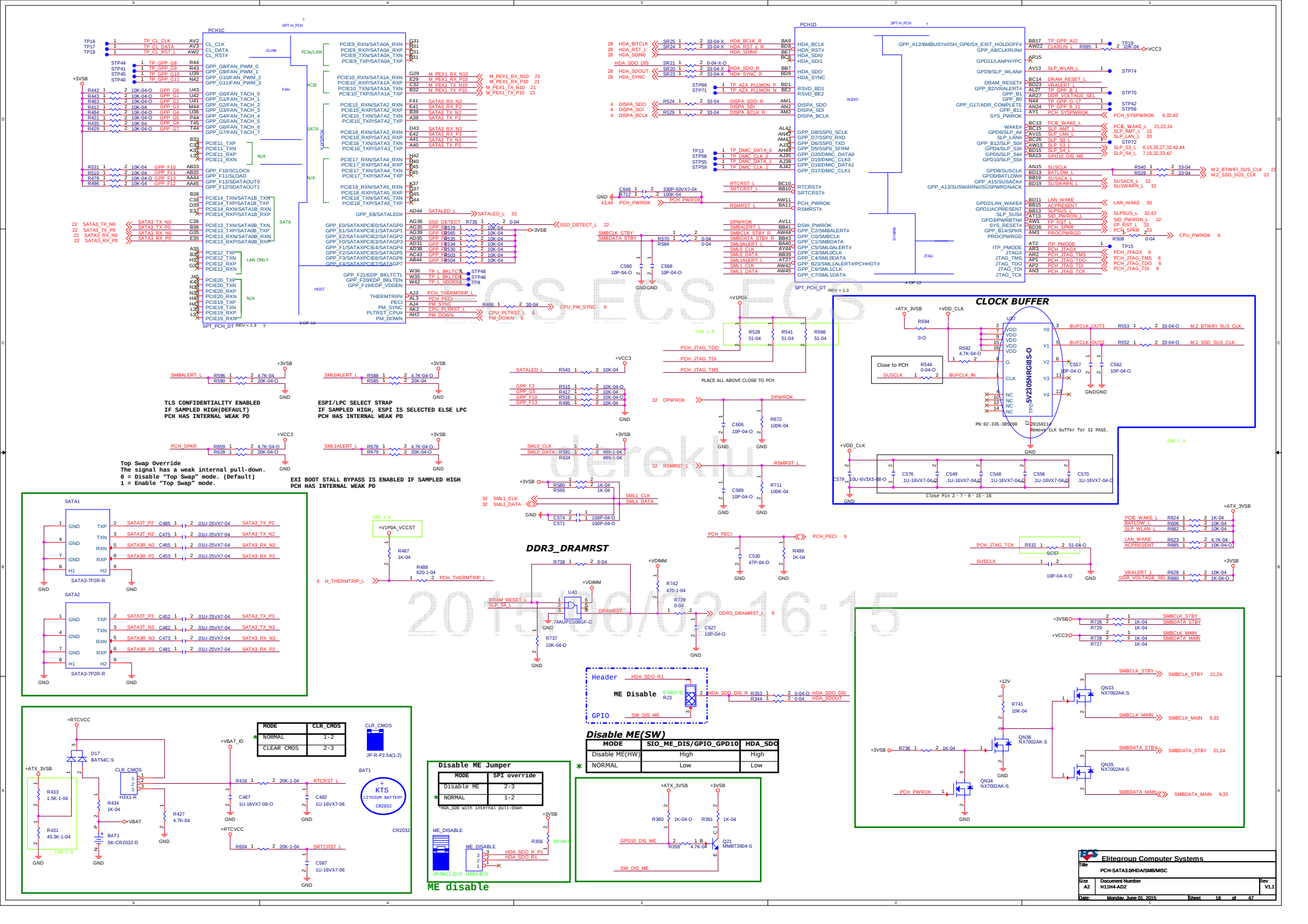
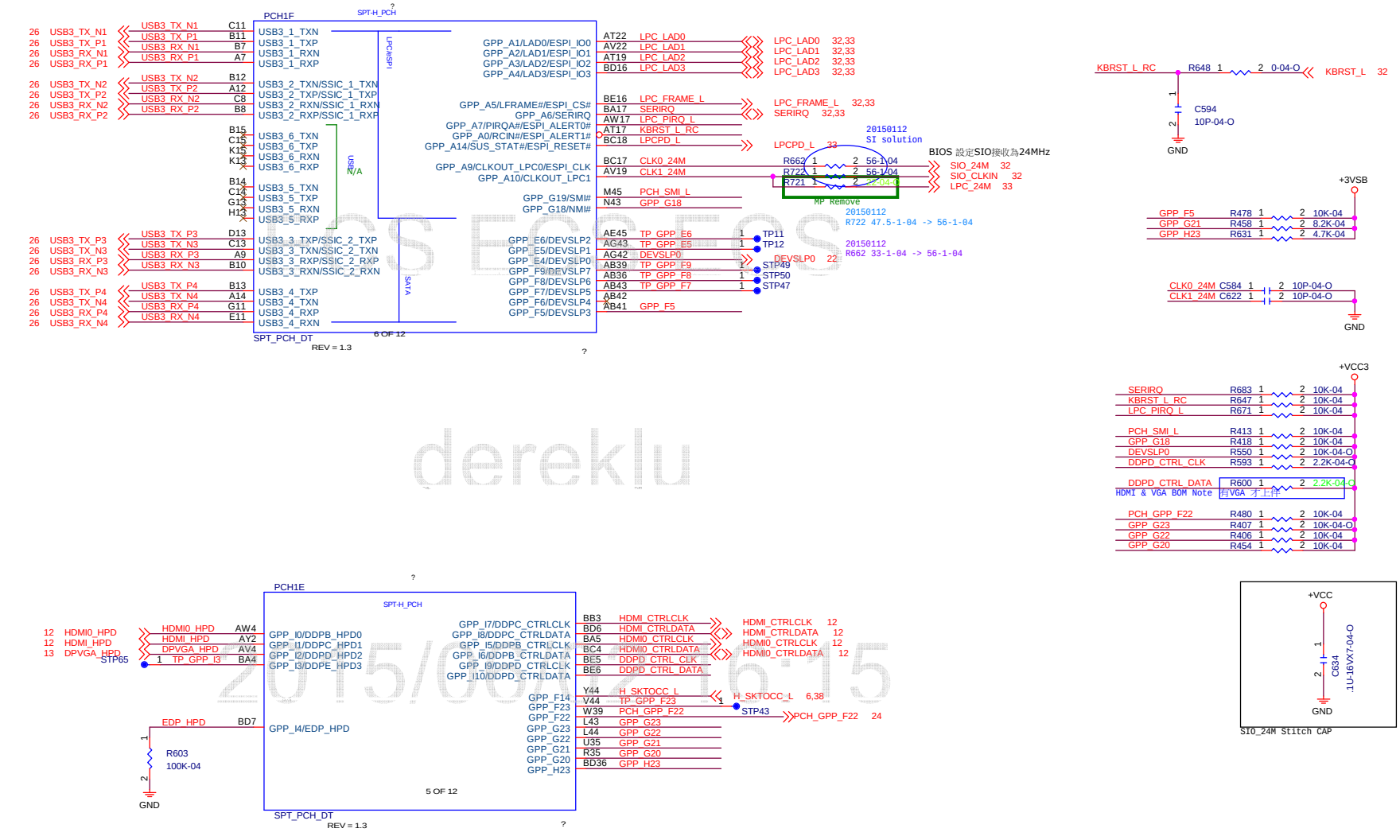


Model Version	GPP_H18	GPP_H17	GPP_H16
V1.0(For MP)	0	0	0
V1.1(Next Ver)	0	0	1
V1.X(Next Ver)	X	X	X


PCH1C
PCH1D
SPT-H_PCH
CLOCK BUFFER
5V2306NRGI8S-O
DDR3_DRAMRST
Disable ME(SW)
Disable ME Jumper
ME disable
TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH(DEFAULT)
PCH HAS INTERNAL WEAK PD
ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD
Top Swap Override
The signal has a weak internal pull-down.
0 = Disable “Top Swap” mode. (Default)
1 = Enable “Top Swap” mode.
EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD
PLACE ALL ABOVE CLOSE TO PCH
Close to PCH
Remove CLK buffer for SI PASS.
Header
ME Disable
GPIO
Elitegroup Computer Systems
PCH-SATA3.0/HDA/SMB/MISC



Elitegroup Computer Systems			
Title: PCH-USB3.0/LPC			
Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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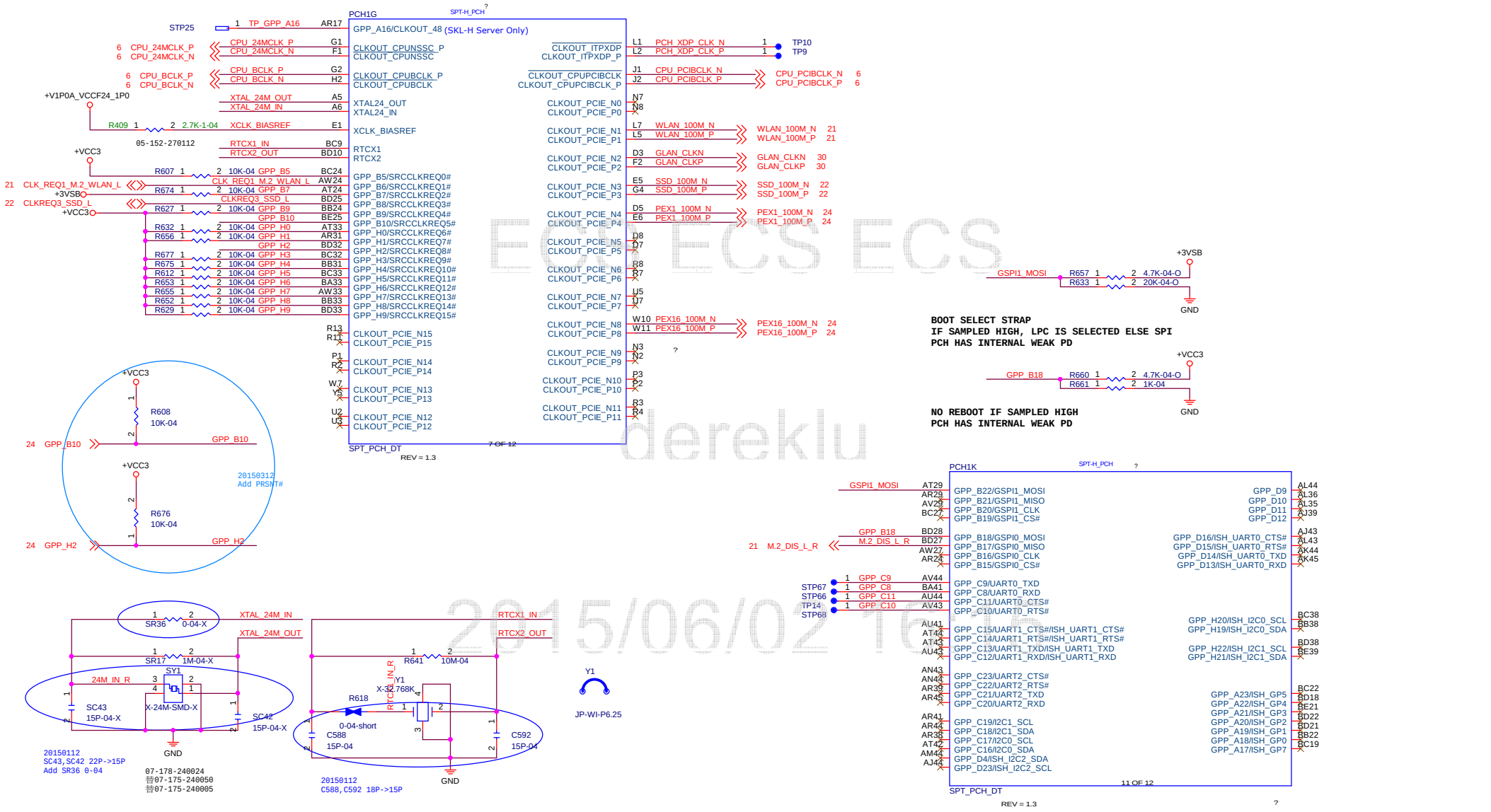

Elitegroup Computer Systems			
Title: PCH-CLK			
Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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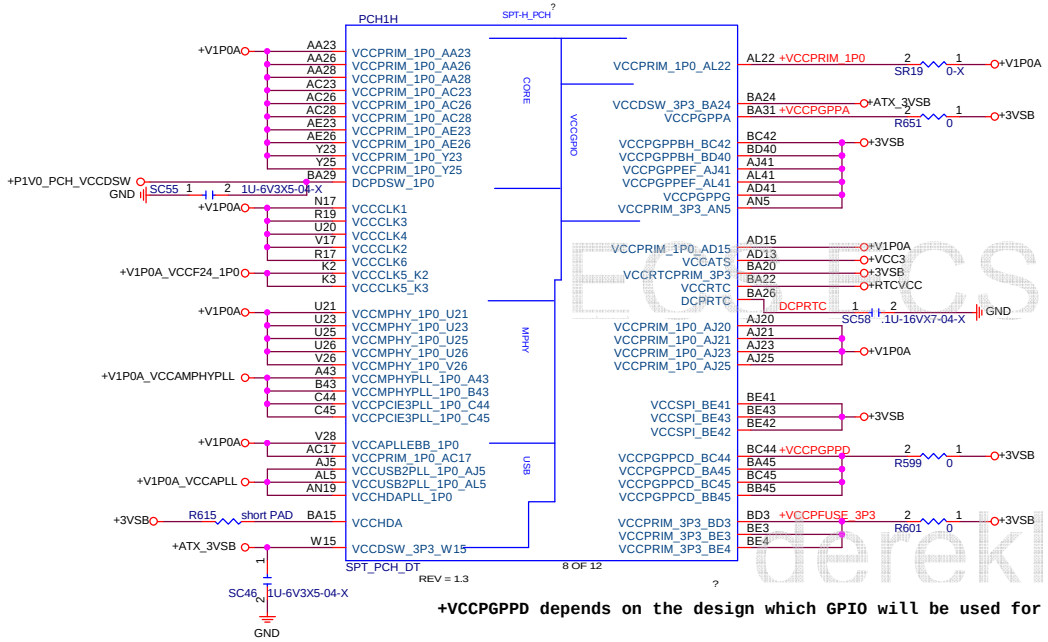
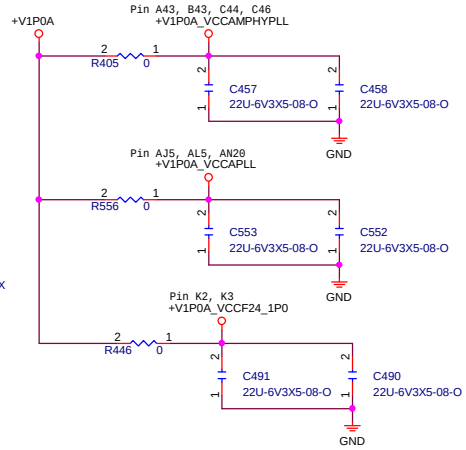
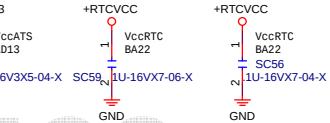
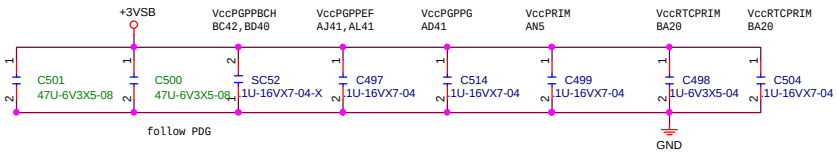
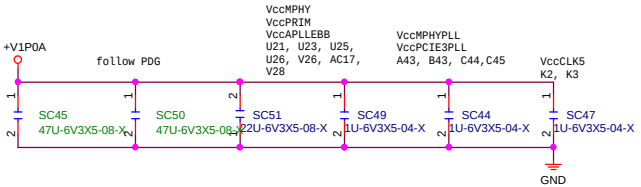


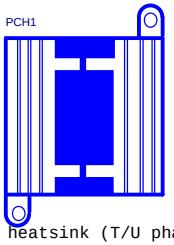








+VCCPGPPD depends on the design which GPIO will be used for 3.3V or 1.8V.



PCH heatsink (T/U phase)
P/N:20-120-012520
20-120-013505
20-120-013678

Elitegroup Computer Systems			
Title: PCH-PWR			
Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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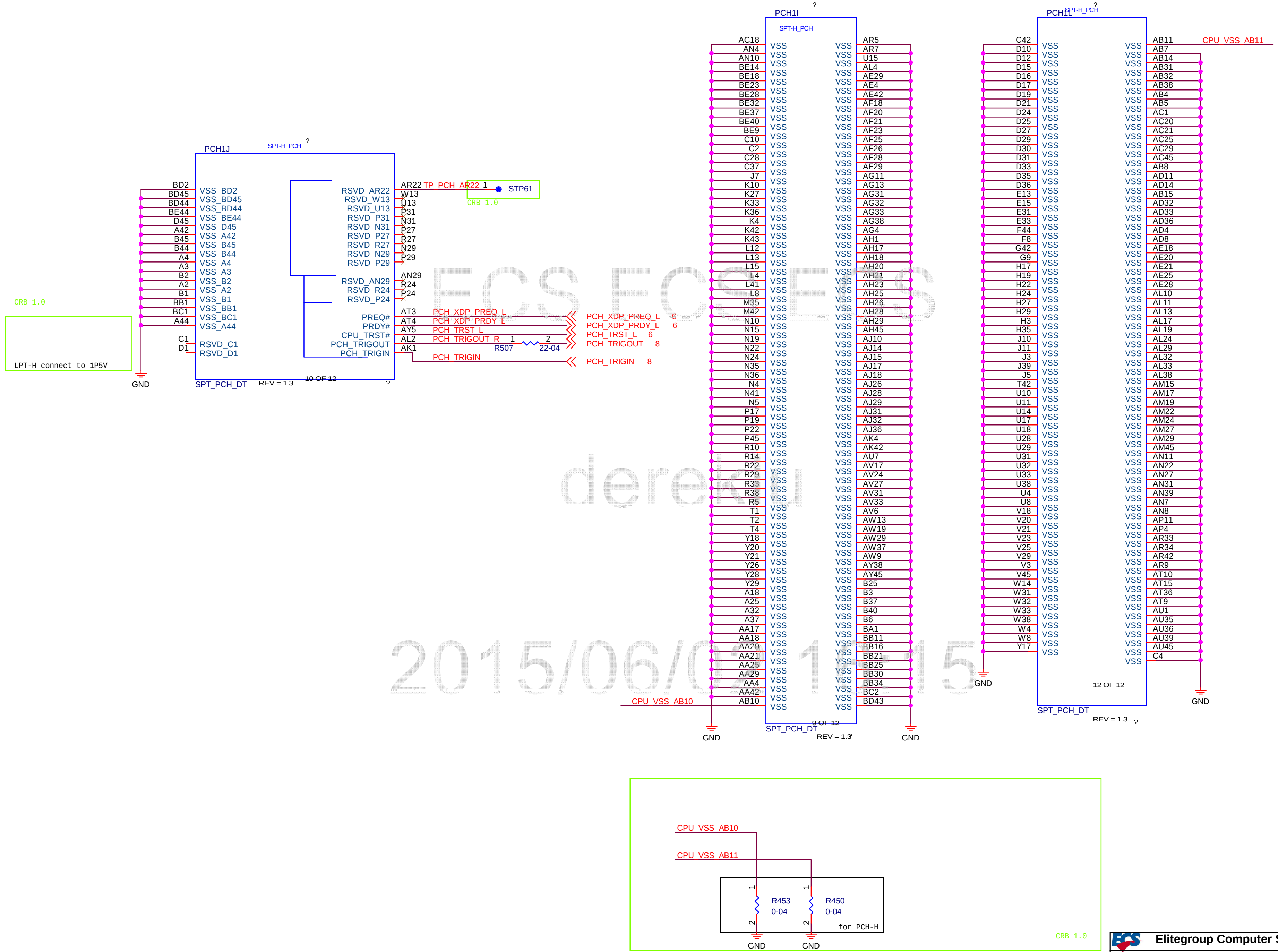

Elitegroup Computer Systems	
Title	PCH-GND
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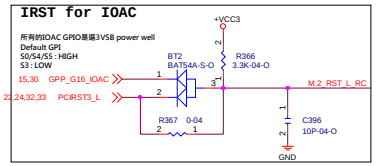
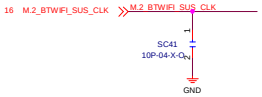
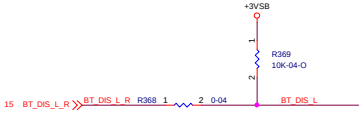
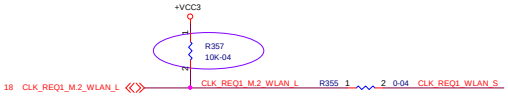
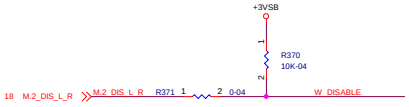
M.2 (NGFF)

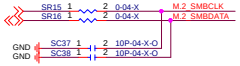


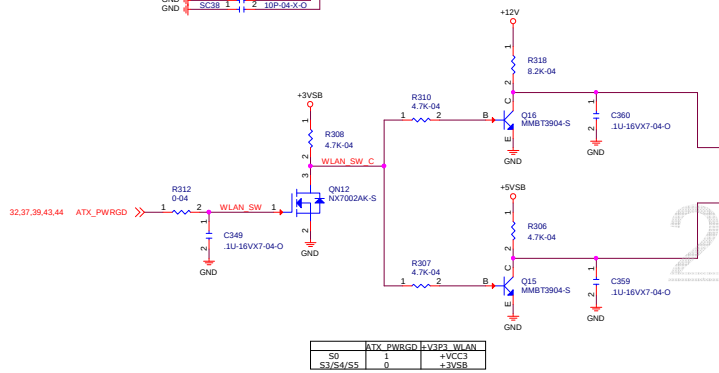




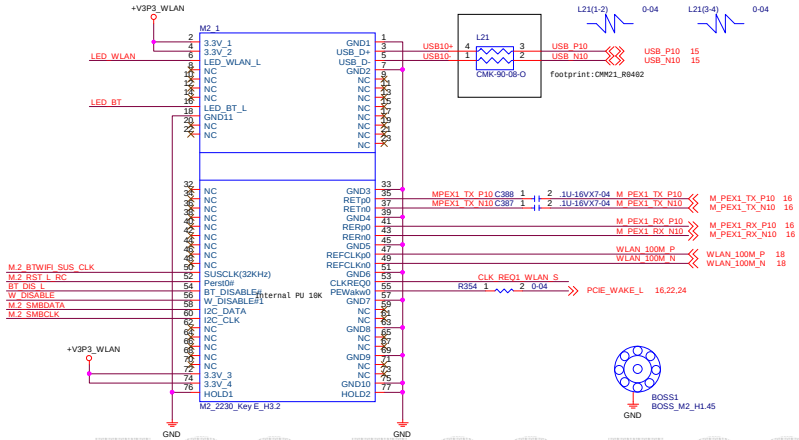


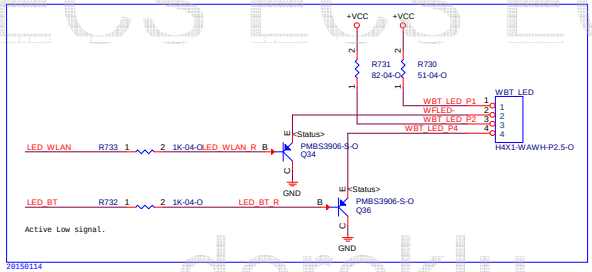


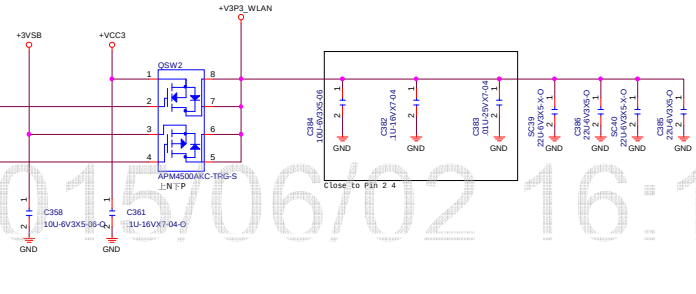




	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3VSB







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Title	M.2 Slot(WLAN
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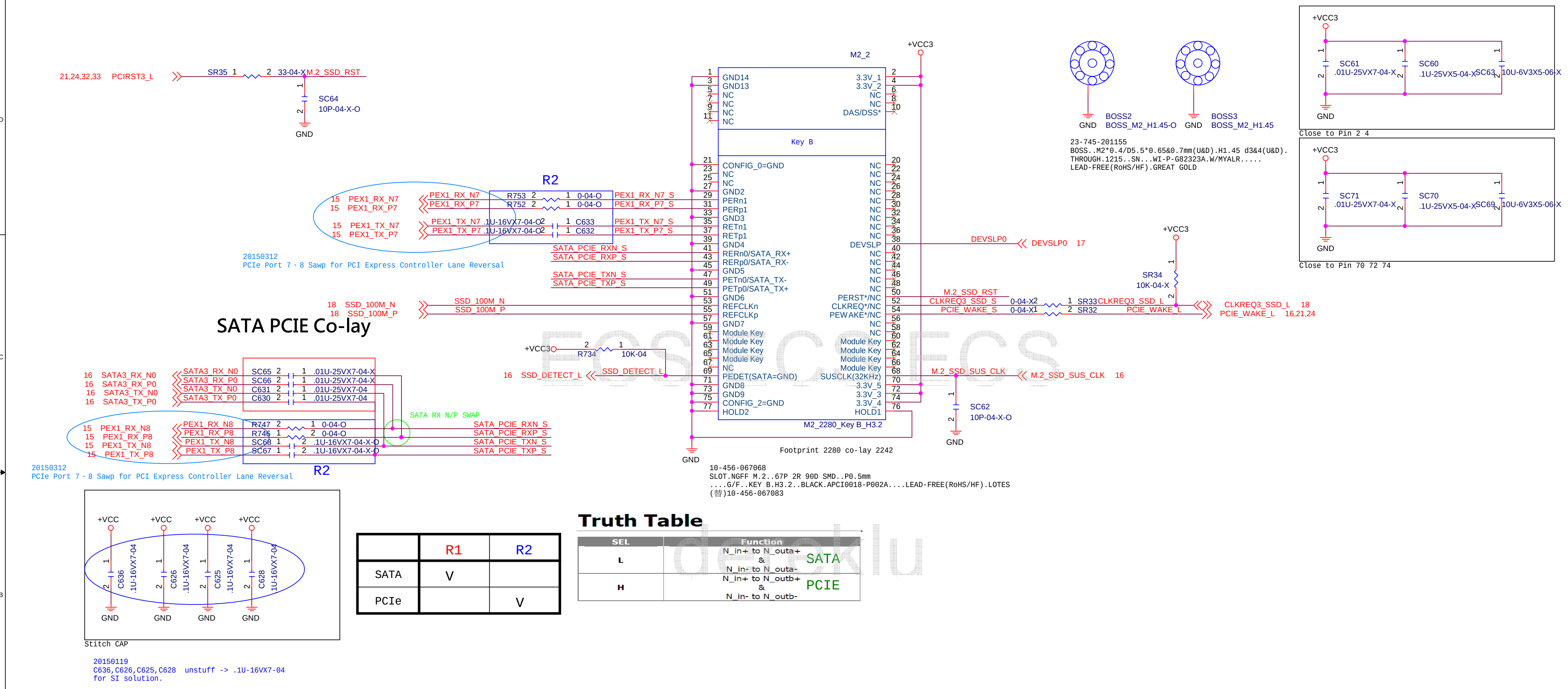

	R1	R2
SATA	V	
PCIe		V

Truth Table

SEL	Function	
L	N_in+ to N_outa+ & N_in- to N_outa-	SATA
H	N_in+ to N_outb+ & N_in- to N_outb-	PCIE

Elitegroup Computer Systems

Title: M.2 Slot(SSD)

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Title	Reserve	
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one slot support dual lan card,reserve

PCI-E X16 SLOT

PCI-E SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A

PCIE16X

PCIE16-GY

PCI-E X1 SLOT1

20150112
Silk screen PCIEX1_1->PCIEX1

PCIE1X

PCIE1X-W

close to PCIE*1

This cap should be placed close to slot power pin

	Ra	Rb	Rc
GPIO PEG Reset	X	V	V
NO GPIO PEG Reset	V	X	X

02-197-008133
IC TTL.74LVC1G08GW..SOT-353-1
....HF.LEAD-FREE(RoHS).NXP

Between PCI-E X16 Slot & PCI-E X1 Slot

This cap should be placed close to slot power pin

Elitegroup Computer Systems			
Title: PCI-E X16/X1 Slot			
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Elitegroup Computer Systems		
Title: Reserve		
Size: C	Document Number: H11H4-AD2	Rev: V1.1
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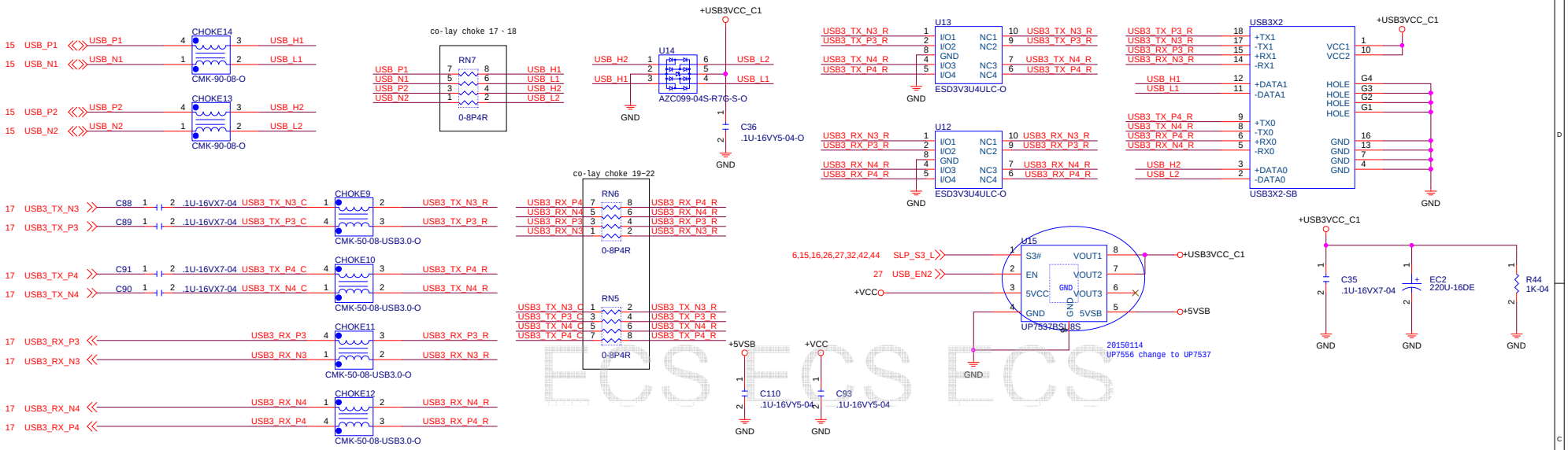
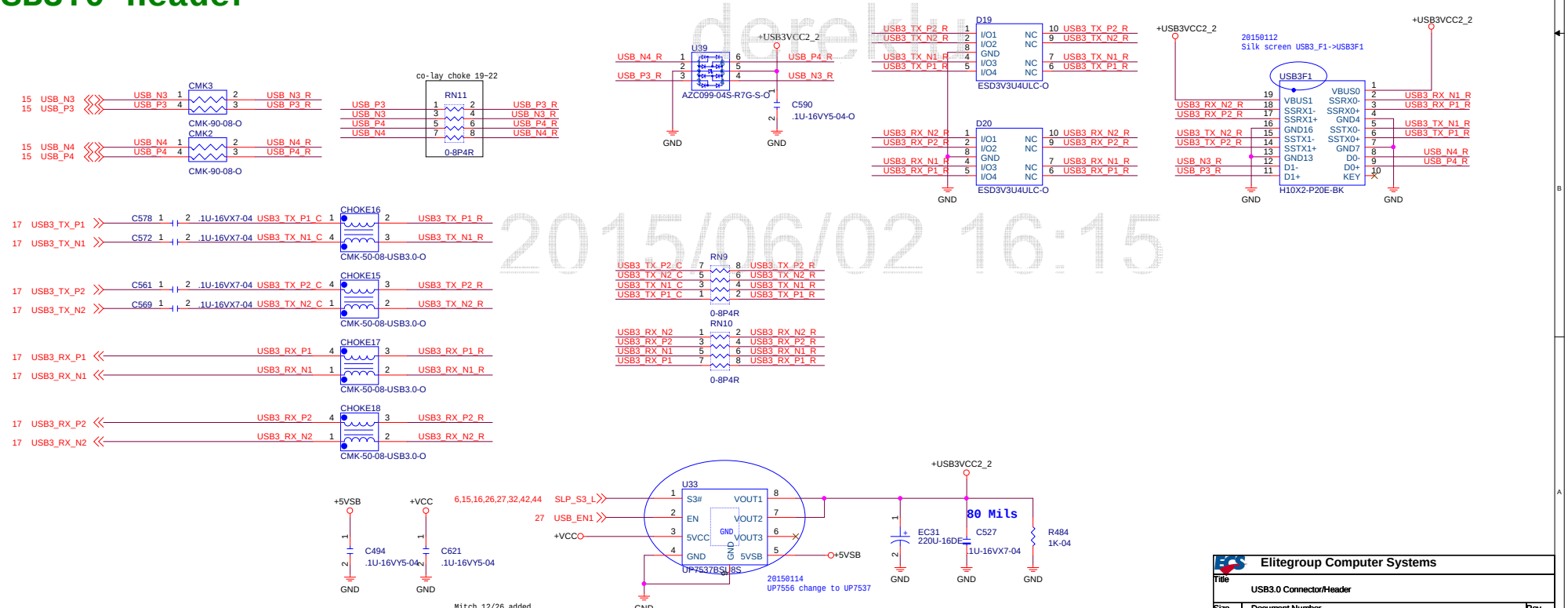
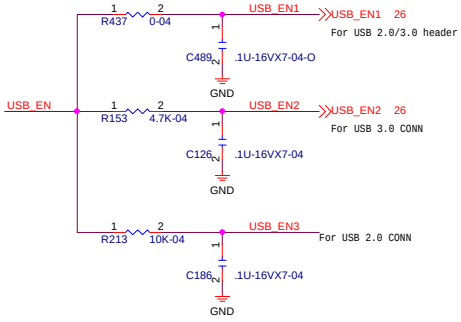


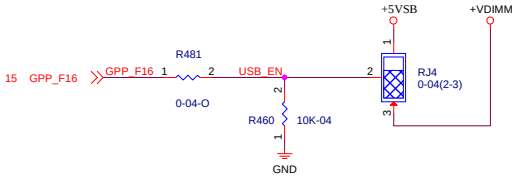
USB3.0 connecter

USB3.0 Header

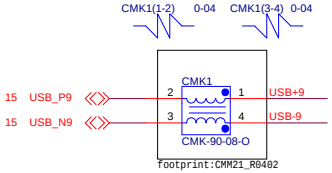


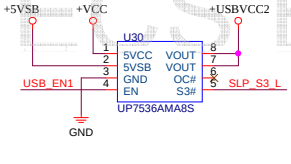
Elitegroup Computer Systems		
Title: USB3.0 Connector/Header		
Size: Custom	Document Number: H11H4-AD2	Rev: V1.1
Date: Monday, June 01, 2015	Sheet 26 of 47	

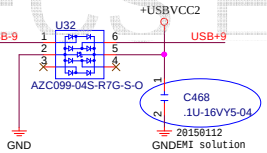


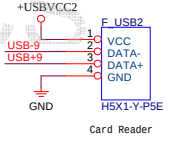


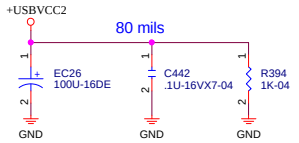
	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
*	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	



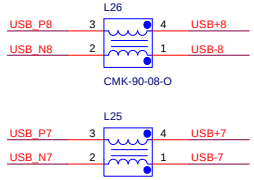


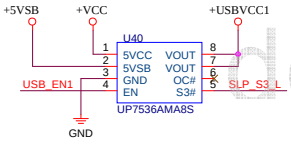


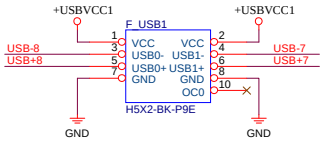


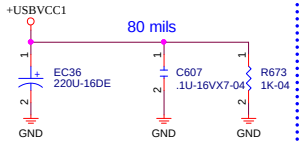


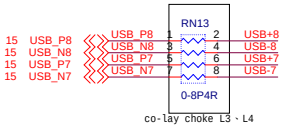
6,15,16,26,32,42,44 SLP_S3_L







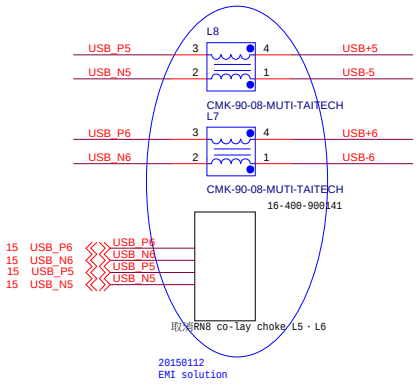


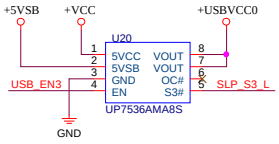


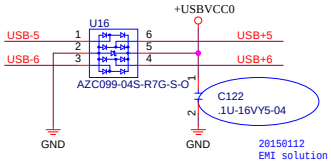
USB2.0 header

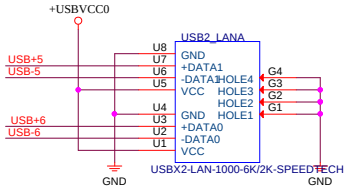
USB2.0 connecter

USB2.0 header reserve

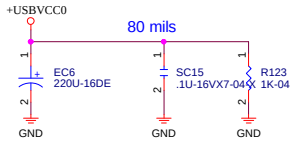








Lan + USB2.0



Elitegroup Computer Systems			
Title: USB2.0 Connector/Header			
Size: Custom	Document Number: H11H4-AD2		Rev: V1.1
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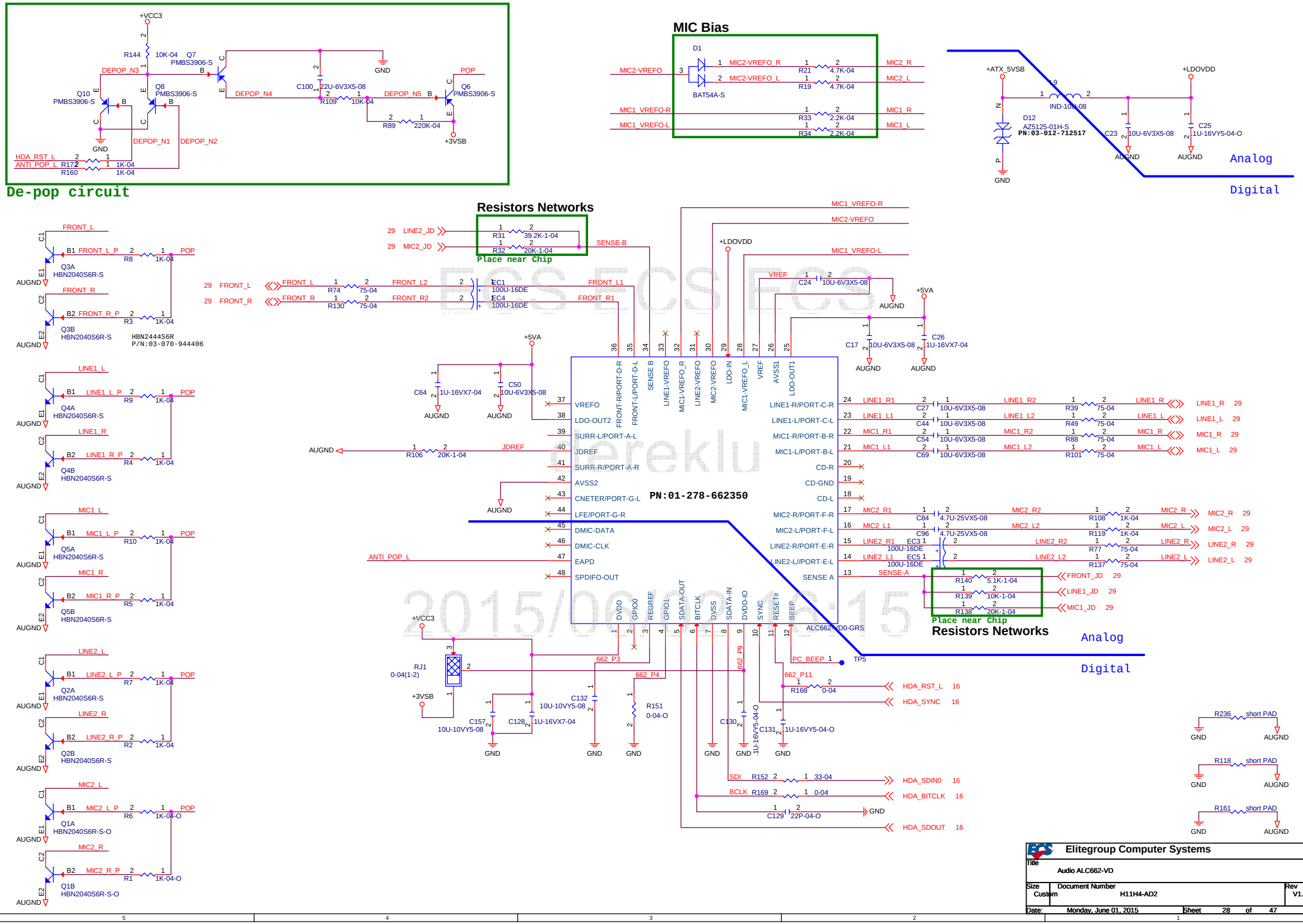
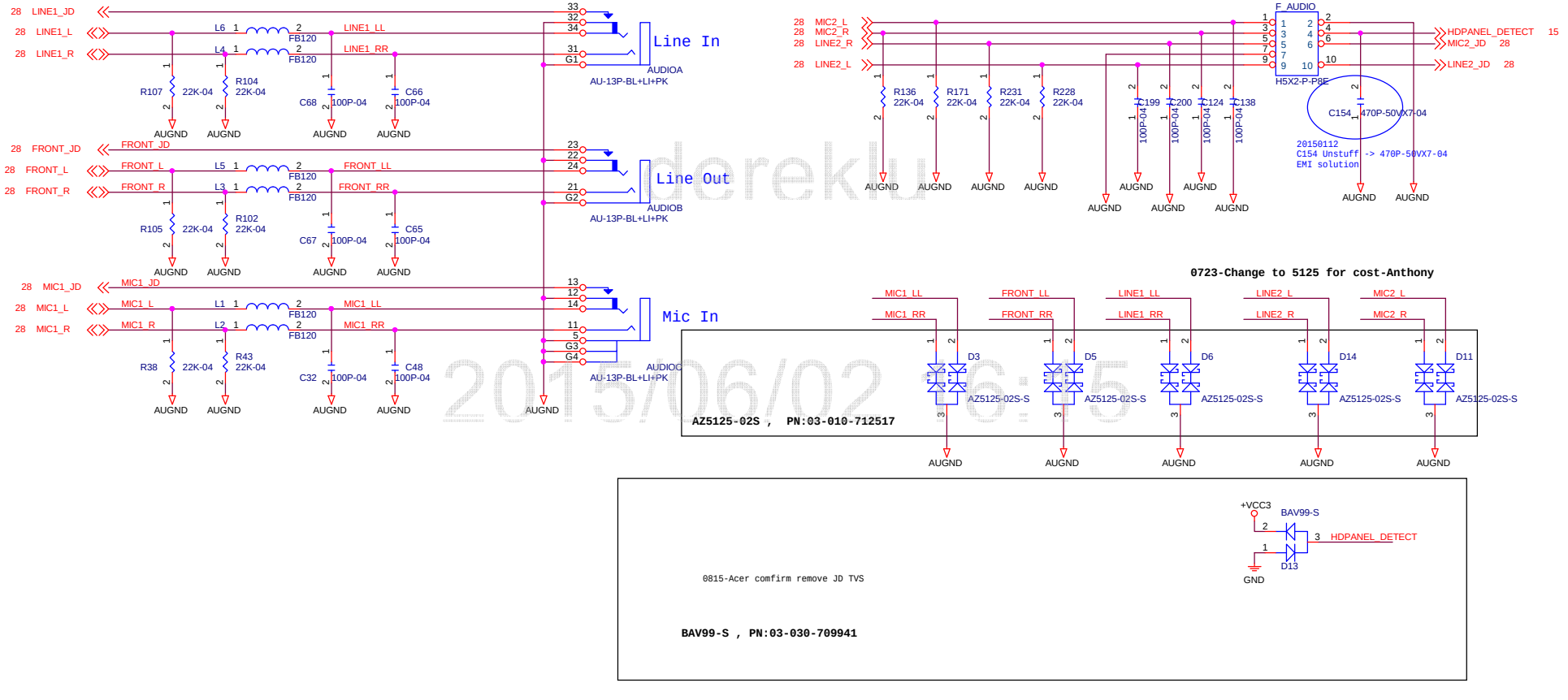

De-pop circuit
MIC Bias
Resistors Networks
Place near Chip
Analog
Digital
PN:01-278-662350
ALC662-VD0-GRS
Elitegroup Computer Systems
Audio ALC662-VD
H11H4-AD2
Monday, June 01, 2015



Elitegroup Computer Systems		
Title: Audio Jack/Header		
Size: Custom	Document Number: H11H4-AD2	Rev: V1.1
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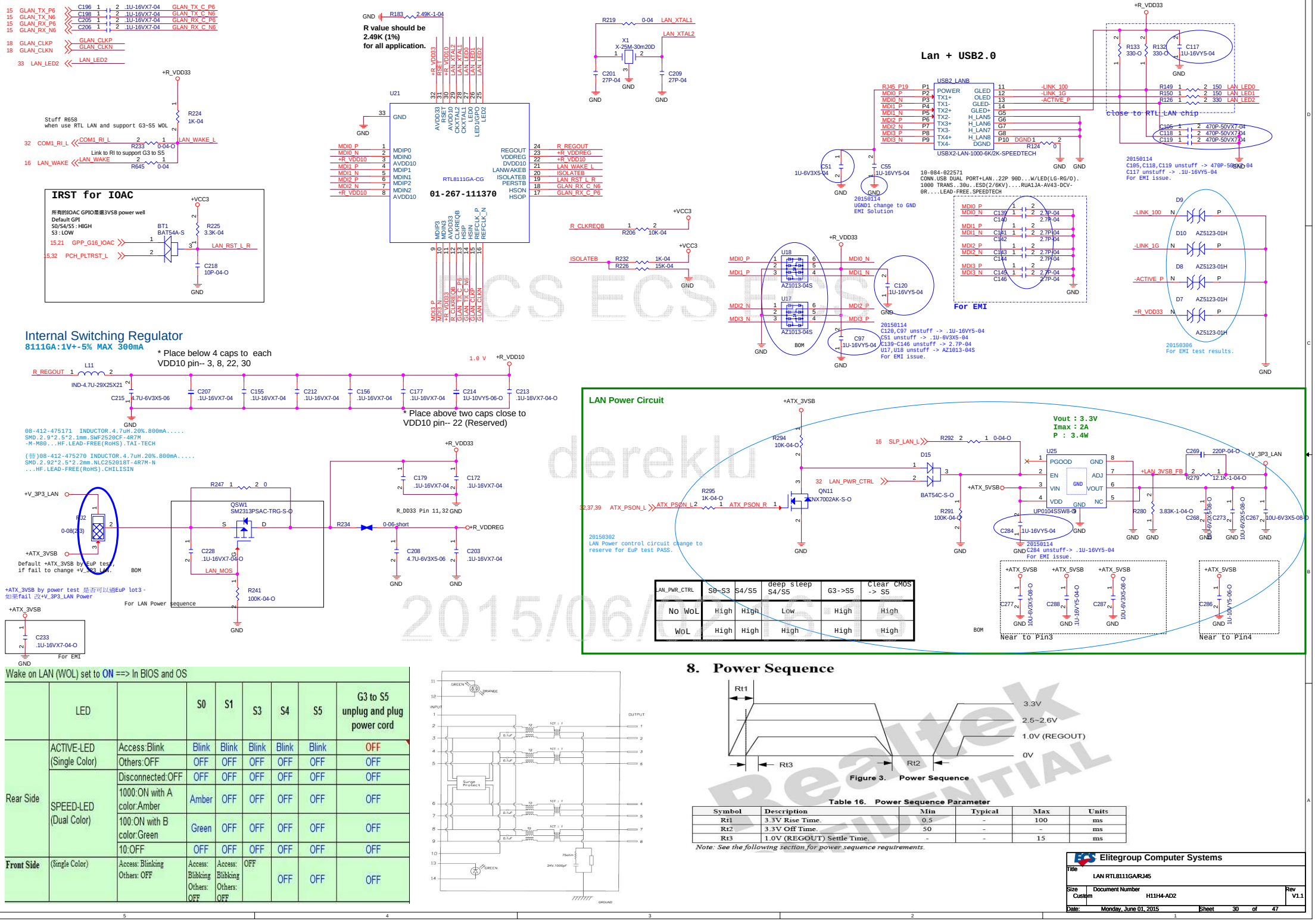

LAN_PWR_CTRL	S0~S3	S4/S5	deep sleep S4/S5	G3->S5	Clear CMOS -> S5
No WoL	High	High	Low	High	High
WoL	High	High	High	High	High

Wake on LAN (WOL) set to ON ==> In BIOS and OS

	LED		S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access:Blink	Blink	Blink	Blink	Blink	Blink	OFF
		Others:OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected:OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000:ON with A color:Amber	Amber	OFF	OFF	OFF	OFF	OFF
		100:ON with B color:Green	Green	OFF	OFF	OFF	OFF	OFF
		10:OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blibking Others: OFF	Access: Blibking Others: OFF	OFF	OFF	OFF	OFF

8. Power Sequence

Figure 3. Power Sequence

Table 16. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V Rise Time.	0.5	-	100	ms
Rt2	3.3V Off Time.	50	-	-	ms
Rt3	1.0V (REGOUT) Settle Time.	-	-	15	ms

Note: See the following section for power sequence requirements.

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Title	LAN RTL8111GA/RJ45
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Elitegroup Computer Systems		
Title: Reserve		
Size: Custom	Document Number: H11H4-AD2	Rev: V1.1
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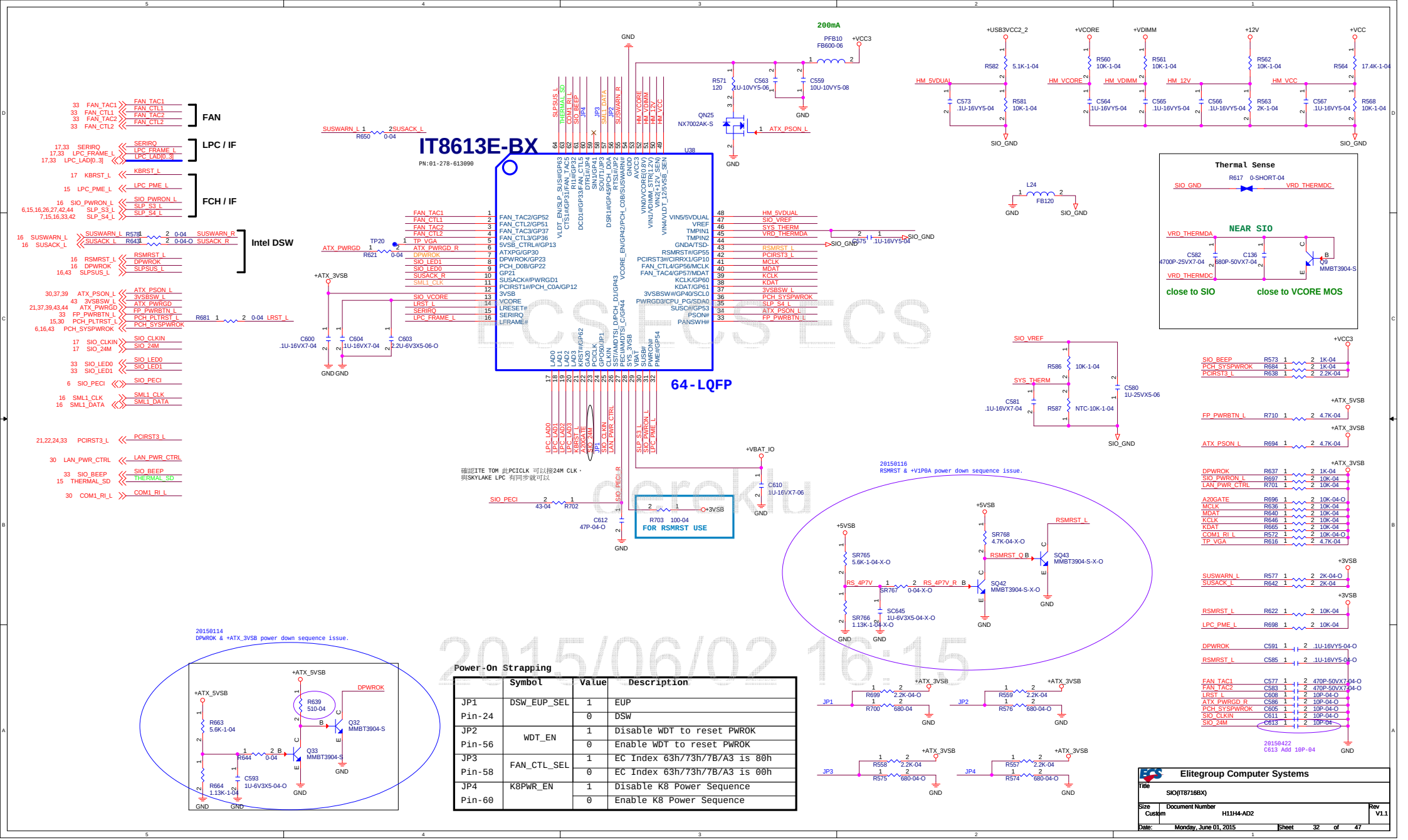
IT8613E-BX
PN:01-278-613090
64-LQFP
U38
200mA
FAN
LPC / IF
FCH / IF
Intel DSW
Thermal Sense
NEAR SIO
close to SIO
close to VCORE MOS
FOR RSMRST USE
20150116
RSMRST & +V1P0A power down sequence issue.
20150114
DPWROK & +ATX_3VSB power down sequence issue.
20150422
C613 Add 10P-04
Power-On Strapping
Symbol
Value
Description
JP1
DSW_EUP_SEL
1
EUP
Pin-24
0
DSW
JP2
WDT_EN
1
Disable WDT to reset PWROK
Pin-56
0
Enable WDT to reset PWROK
JP3
FAN_CTL_SEL
1
EC Index 63h/73h/7B/A3 is 80h
Pin-58
0
EC Index 63h/73h/7B/A3 is 00h
JP4
K8PWR_EN
1
Disable K8 Power Sequence
Pin-60
0
Enable K8 Power Sequence
Elitegroup Computer Systems
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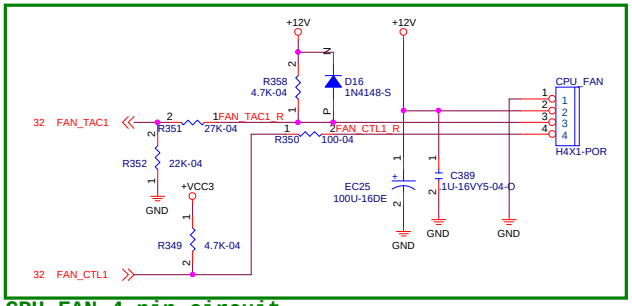
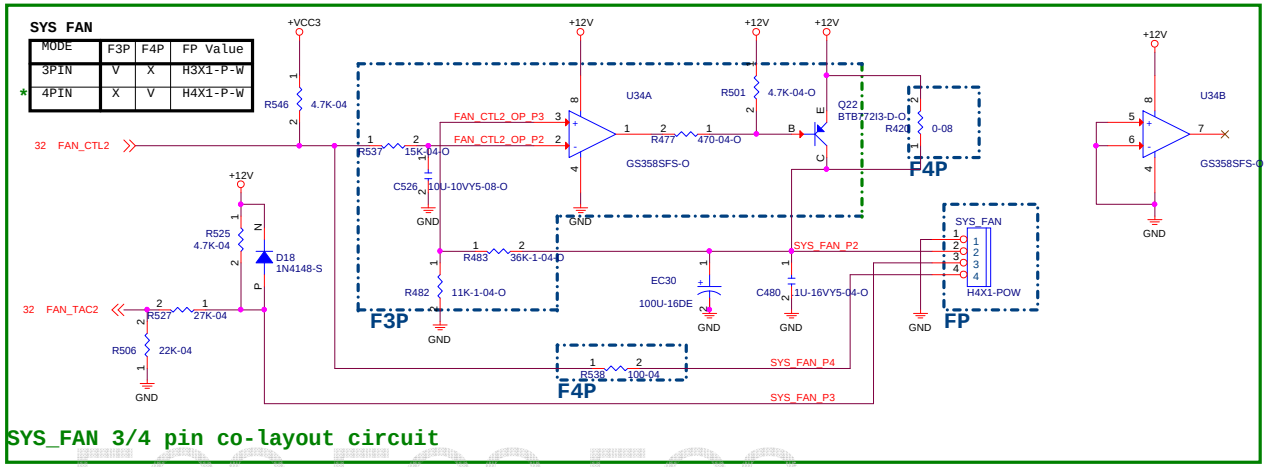
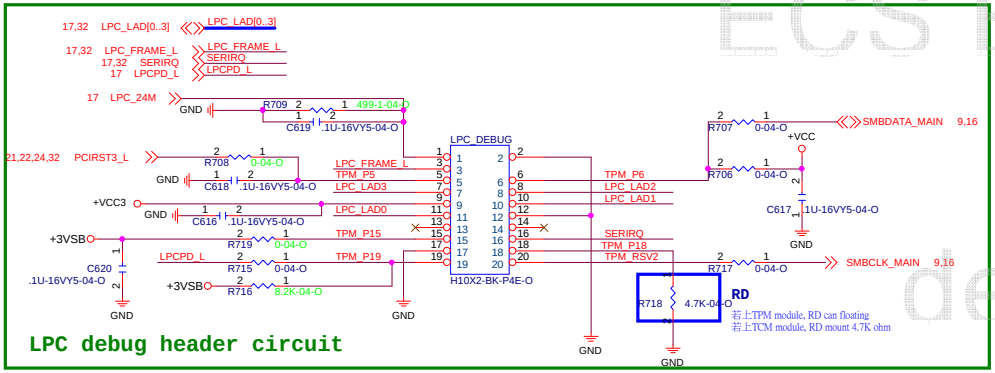


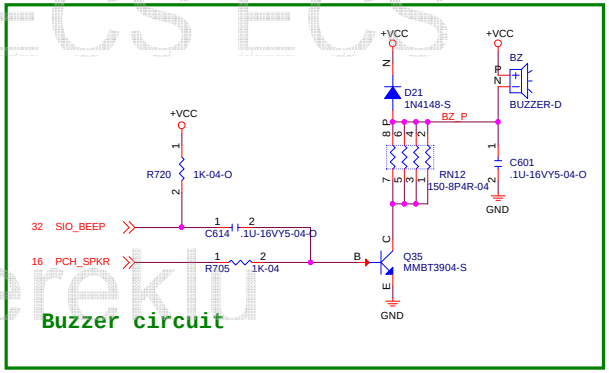
CPU_FAN 4 pin circuit



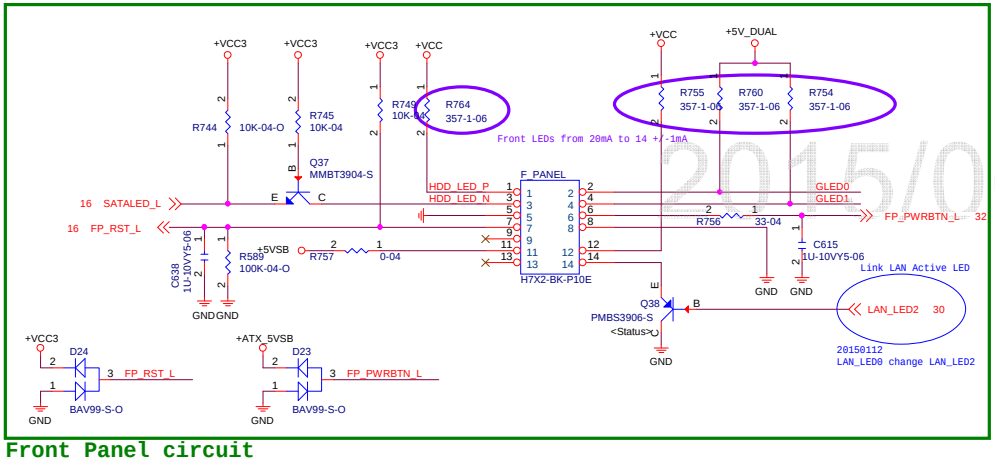
SYS_FAN 3/4 pin co-layout circuit



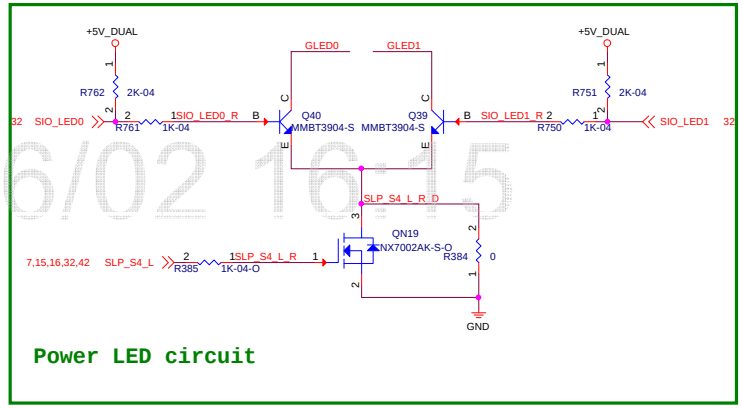
LPC debug header circuit



Buzzer circuit



Front Panel circuit



Power LED circuit

Elitegroup Computer Systems			
Title: FAN/Buzzer/PS2/Front Panel			
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Elitegroup Computer Systems

Title: Reserve

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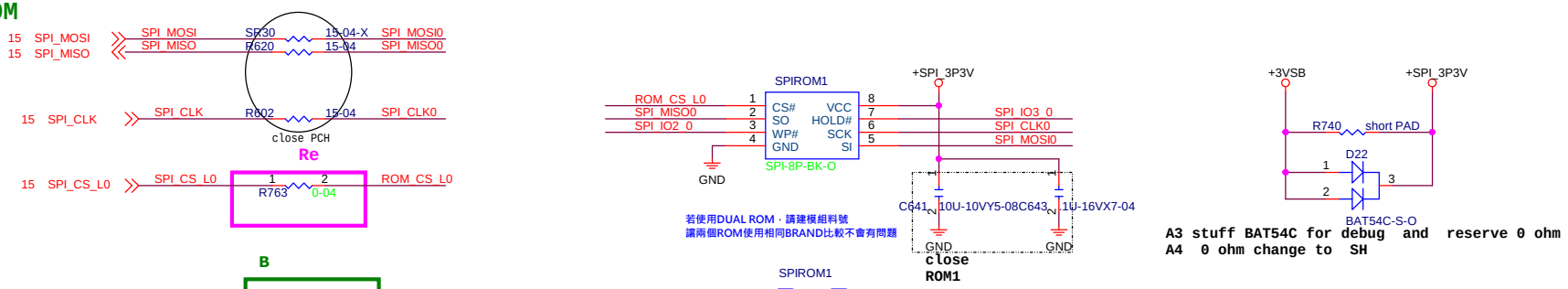
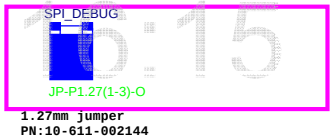
SPI ROM



SPI mode selection:

MODE	BIOS WP	A	B
* Standard/Dual	NA	10K	X
Quad	NA	1K	V

Note.Quad SPI not support WP



	Ra	Rd	Re
A3~A5	0	0	X
MP	X	X	0

BIOS WP

Title	SPI ROM		
Size B	Document Number H11H4-AD2		Rev V1.1
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Title: Reserv		
Size: B	Document Number: H11H4-AD2	Rev: V1.1
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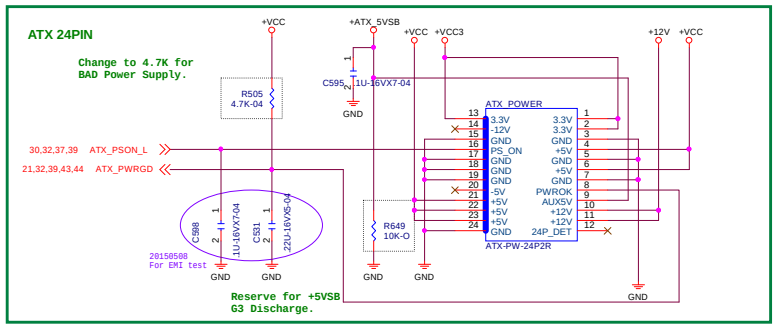
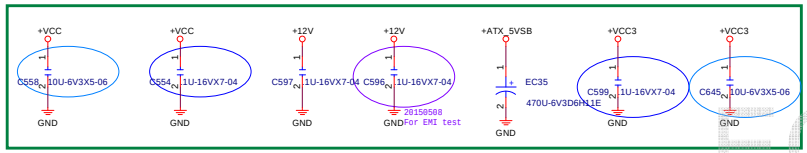
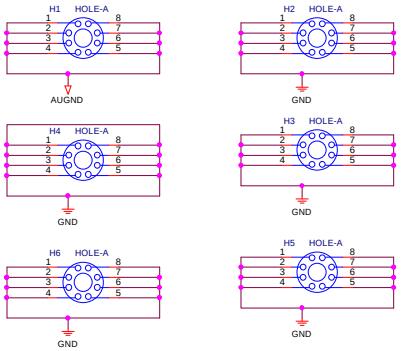
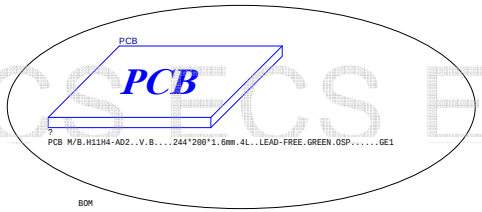
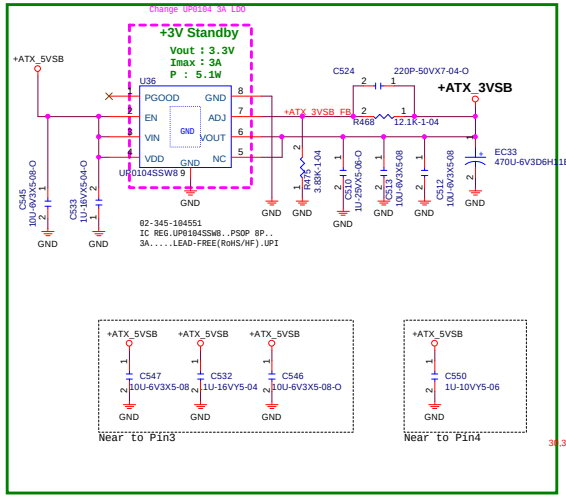


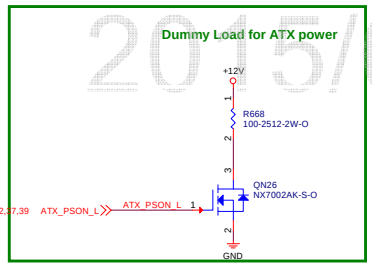




Derek Lu 9/12 Del VCC3 & VCC DC/DC switching







Elitegroup Computer Systems		
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Size: Custom	Document Number: H11H4-AD2	Rev: V1.1
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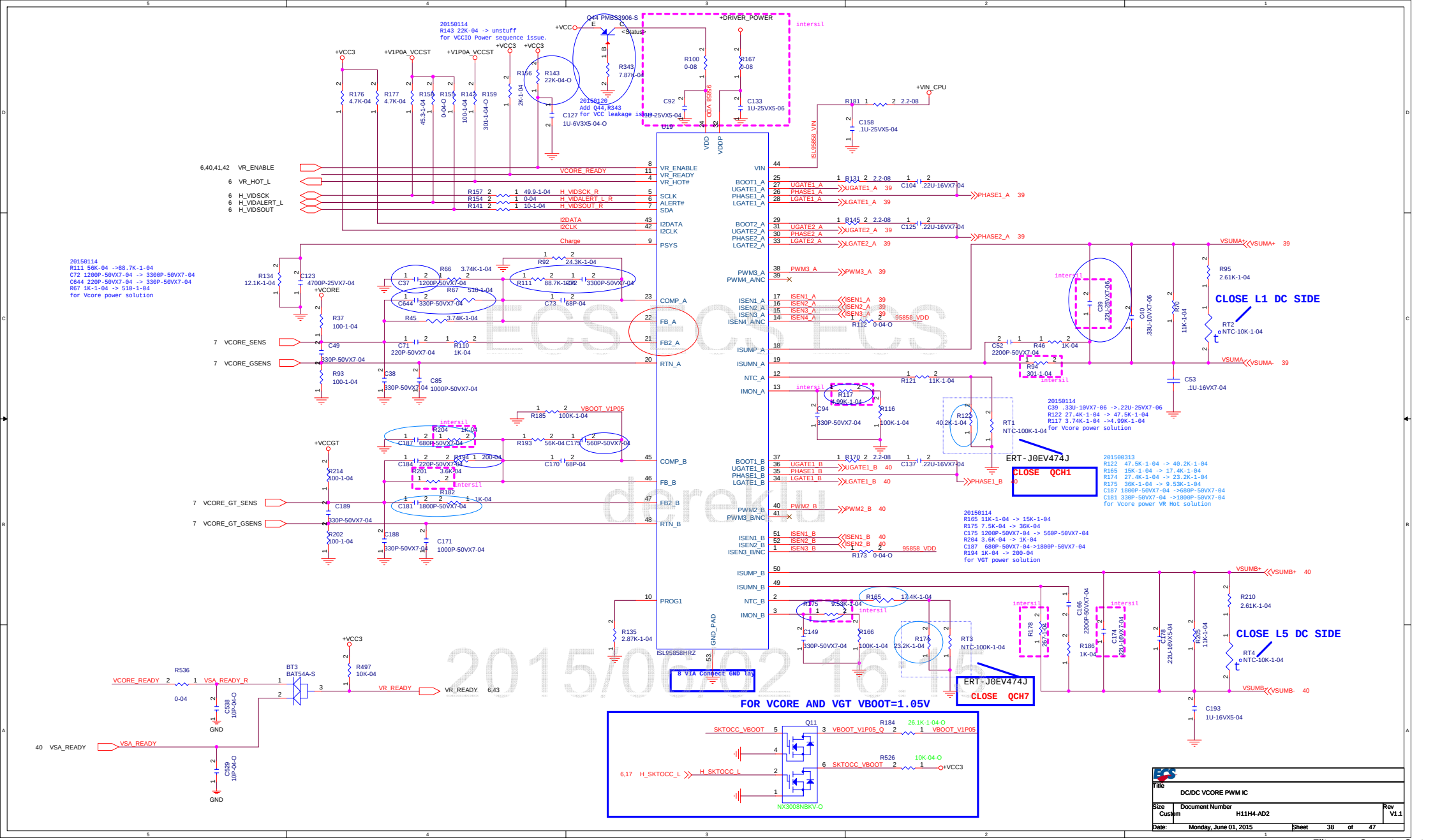

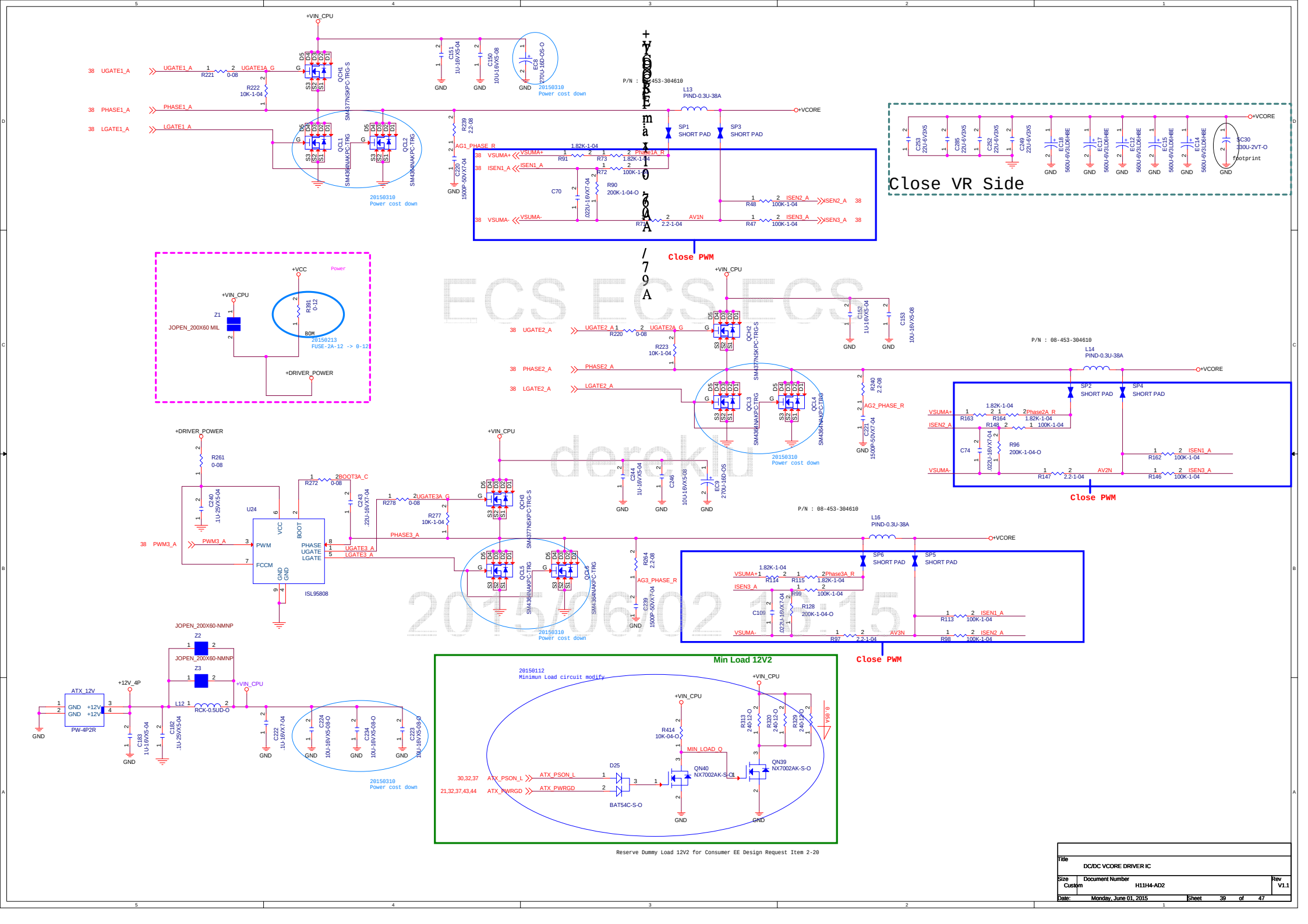
+VIN_CPU
38 UGATE1_A
UGATE1_A
UGATE1A_G
R221 0-08
R222 10K-1-04
QCH1 SM4377NSKPC-TRG-S
38 PHASE1_A
PHASE1_A
38 LGATE1_A
LGATE1_A
QCL1 SM4306NAKPC-TRG
QCL2 SM4306NAKPC-TRG
C151 1U-16VX5-04
C150 10U-16VX5-08
EC8 270U-16D-OS-O
GND
20150310 Power cost down
P/N : 08-453-304610
L13 PIND-0.3U-38A
+VCORE
SP1 SHORT PAD
SP3 SHORT PAD
R239 2.2-08
AG1_PHASE_R
C229 1500P-50VX7-04
VSUMA+
ISEN1_A
VSUMA-
R91 1.82K-1-04
R73 1.82K-1-04
R72 100K-1-04
R90 200K-1-04-O
C70 .022U-16VX7-04
R71 2.2-1-04
AV1N
R48 100K-1-04
R47 100K-1-04
ISEN2_A
ISEN3_A
38
Close PWM
C253 22U-6V3X5
C285 22U-6V3X5
C252 22U-6V3X5
C249 22U-6V3X5
EC18 560U-6V3LD6H8E
EC17 560U-6V3LD6H8E
EC12 560U-6V3LD6H8E
EC15 560U-6V3LD6H8E
EC14 560U-6V3LD6H8E
SC30 330U-2VT-O
footprint
Close VR Side
+VCC
Power
+VIN_CPU
Z1
JOPEN_200X60 MIL
BOM
R391 0-12
20150213 FUSE-2A-12 -> 0-12
+DRIVER_POWER
38 UGATE2_A
UGATE2_A
UGATE2A_G
R220 0-08
R223 10K-1-04
QCH2 SM4377NSKPC-TRG-S
38 PHASE2_A
PHASE2_A
38 LGATE2_A
LGATE2_A
QCL3 SM4306NAKPC-TRG
QCL4 SM4306NAKPC-TRG
C152 1U-16VX5-04
C153 10U-16VX5-08
P/N : 08-453-304610
L14 PIND-0.3U-38A
+VCORE
SP2 SHORT PAD
SP4 SHORT PAD
R240 2.2-08
AG2_PHASE_R
C221 1500P-50VX7-04
VSUMA+
ISEN2_A
VSUMA-
R163 1.82K-1-04
R164 1.82K-1-04
R148 100K-1-04
C74 .022U-16VX7-04
R96 200K-1-04-O
R147 2.2-1-04
AV2N
R162 100K-1-04
R146 100K-1-04
ISEN1_A
ISEN3_A
Close PWM
+DRIVER_POWER
R261 0-08
C240 .1U-25VX5-04
U24
VCC
BOOT
PWM
FCCM
PHASE
UGATE
LGATE
GND
ISL95808
38 PWM3_A
PWM3_A
R272 0-08
2BOOT3A_C
C243 .22U-16VX7-04
R278 0-08
2UGATE3A_G
R277 10K-1-04
PHASE3_A
UGATE3_A
LGATE3_A
QCH3 SM4377NSKPC-TRG-S
QCL5 SM4306NAKPC-TRG
QCL6 SM4306NAKPC-TRG
C244 1U-16VX5-04
C246 10U-16VX5-08
EC9 270U-16D-OS
P/N : 08-453-304610
L16 PIND-0.3U-38A
+VCORE
SP6 SHORT PAD
SP5 SHORT PAD
R264 2.2-08
AG3_PHASE_R
C229 1500P-50VX7-04
VSUMA+
ISEN3_A
VSUMA-
R114 1.82K-1-04
R115 1.82K-1-04
R98 100K-1-04
C109 .022U-16VX7-04
R128 200K-1-04-O
R97 2.2-1-04
AV3N
R113 100K-1-04
R98 100K-1-04
ISEN1_A
ISEN2_A
Close PWM
JOPEN_200X60-NMNP
Z2
JOPEN_200X60-NMNP
Z3
ATX_12V
GND
+12V
PW-4P2R
+12V_4P
+VIN_CPU
L12
RCK-0.5UD-O
C183 1U-16VX5-04
C182 .1U-25VX5-04
C222 1U-16VX7-04
C224 10U-16VX5-08-O
C234 10U-16VX5-08-O
C223 10U-16VX5-08-O
20150310 Power cost down
Min Load 12V2
20150112 Minimun Load circuit modify
+VIN_CPU
R414 10K-04-O
MIN_LOAD_O
30,32,37 ATX_PSON_L
21,32,37,43,44 ATX_PWRGD
D25 BAT54C-S-O
QN40 NX7002AK-S-O1
QN39 NX7002AK-S-O
R313 240-12-O
R320 240-12-O
R329 240-12-O
V5B_O
Reserve Dummy Load 12V2 for Consumer EE Design Request Item 2-20
Title
DC/DC VCORE DRIVER IC
Size Custom
Document Number H11H4-AD2
Rev V1.1
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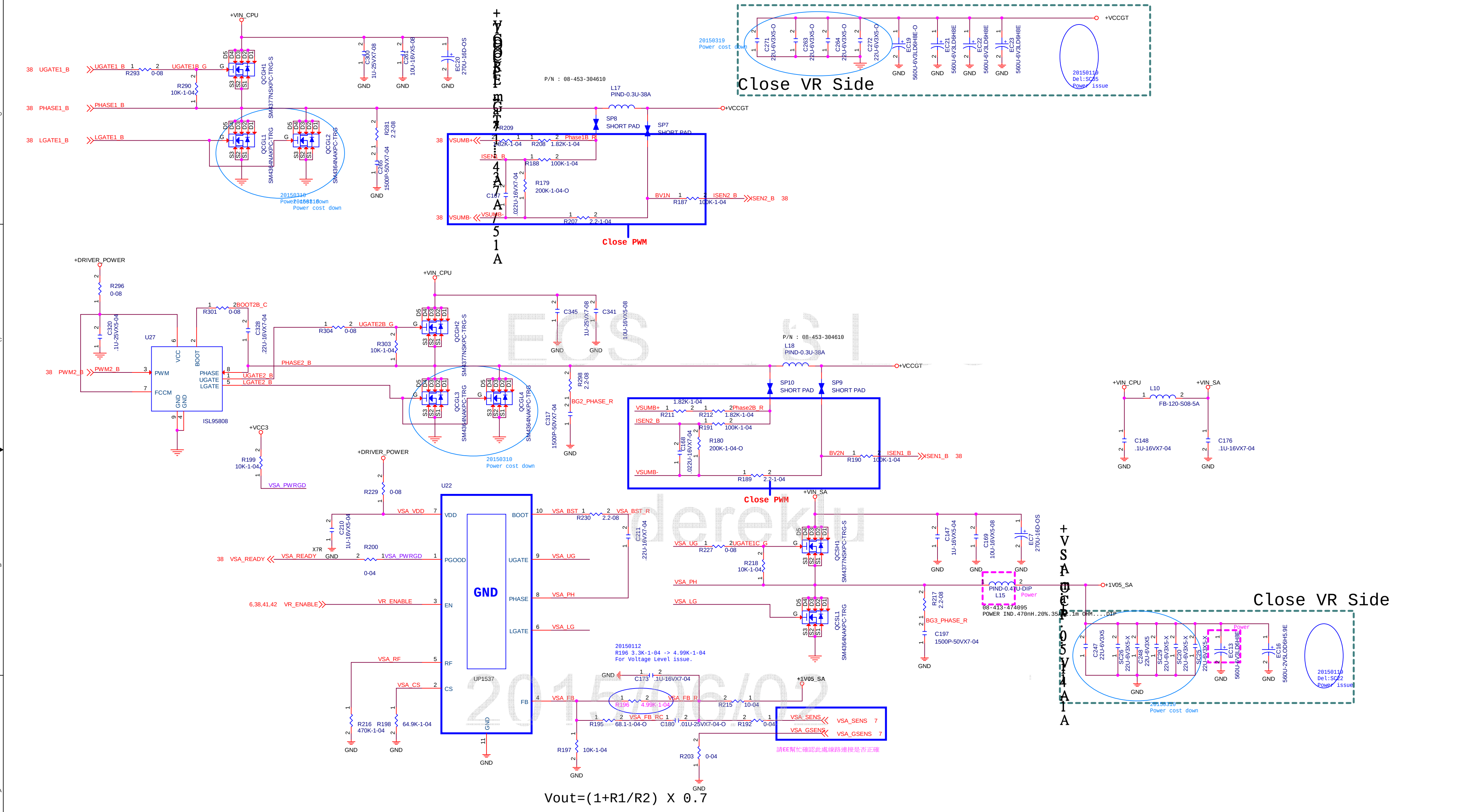

Vout=(1+R1/R2) X 0.7

VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

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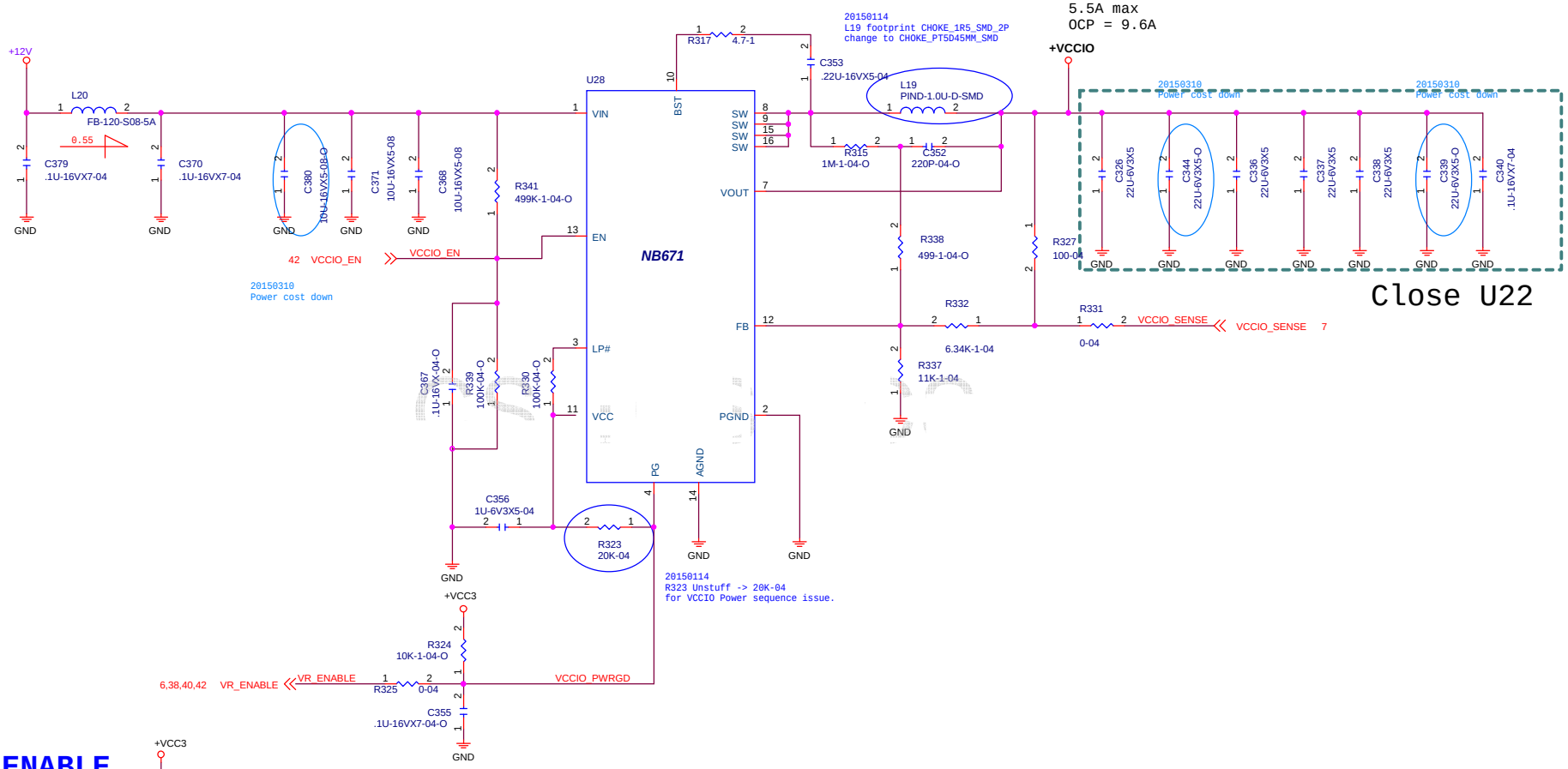
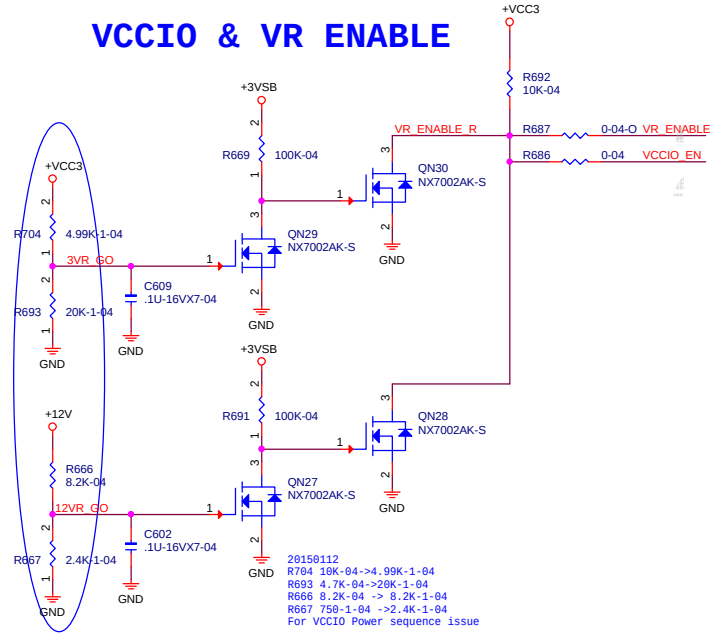


VCCIO & VR ENABLE



VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps

Vout=(1+R1/R2) X 0.6

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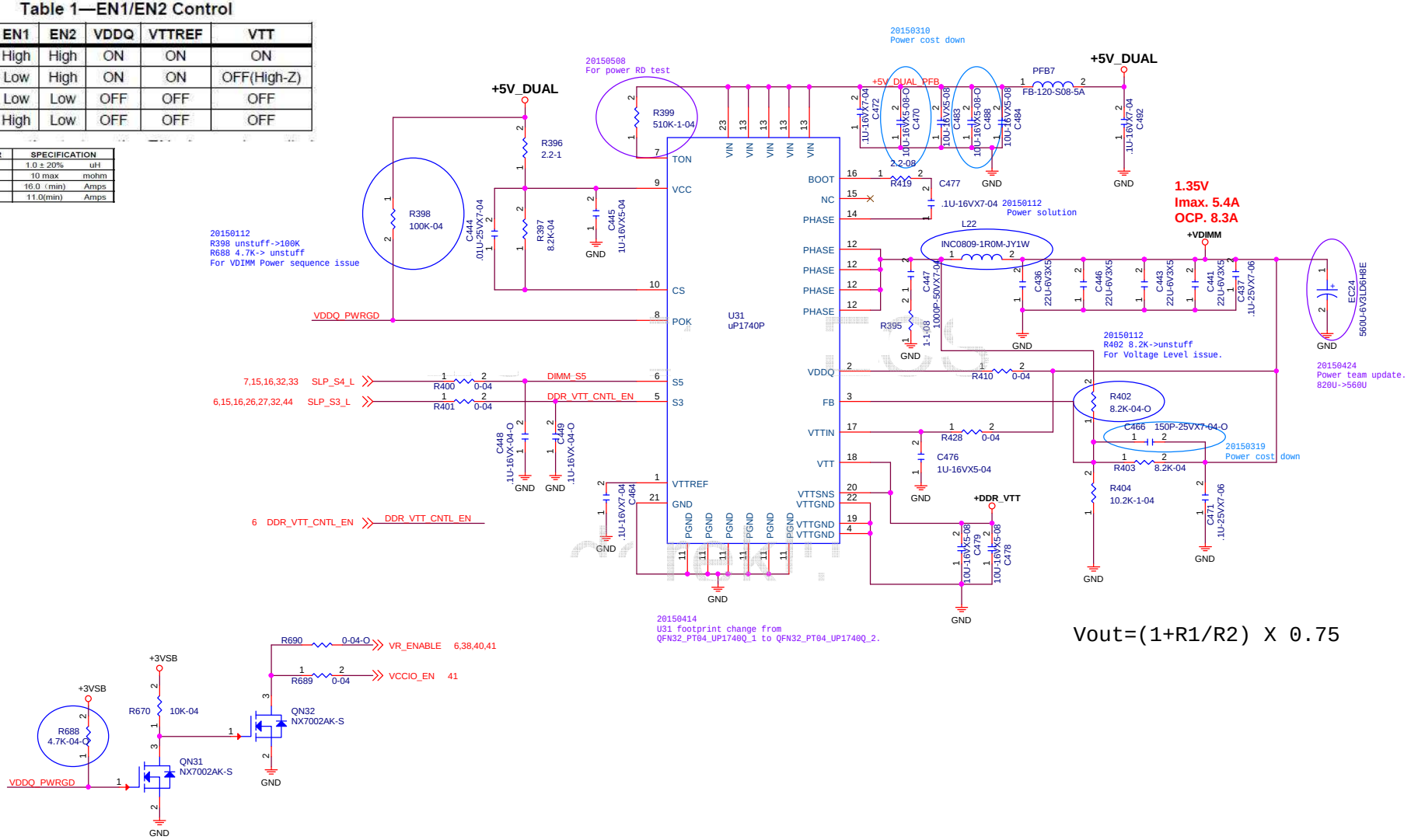
VDIMM

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

PARAMETER	SPECIFICATION	
L0	1.0 ± 20%	uH
DCR	10 max	mohm
I-sat	16.0 (min)	Amps
I rms	11.0(min)	Amps



Title	DC/DC VDIMM & DDRVTT		
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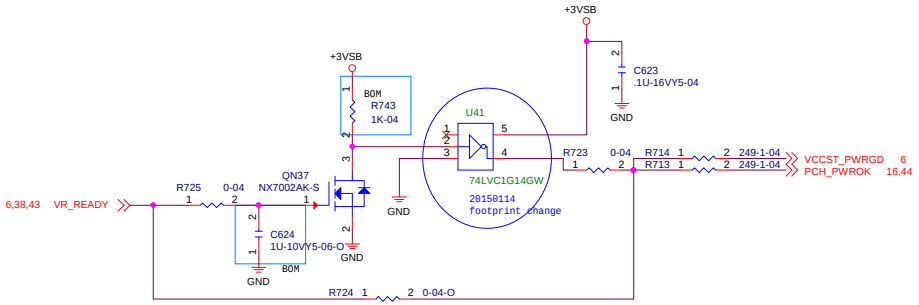
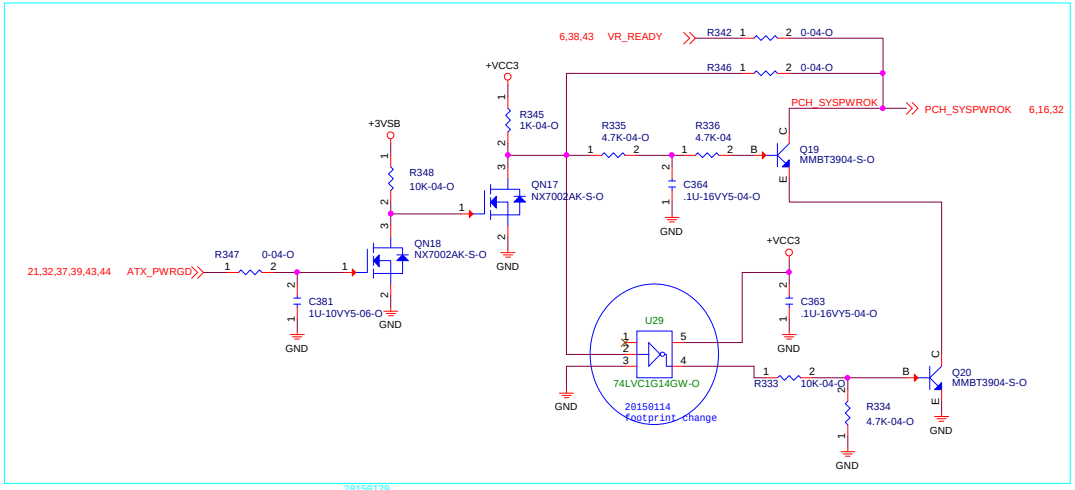
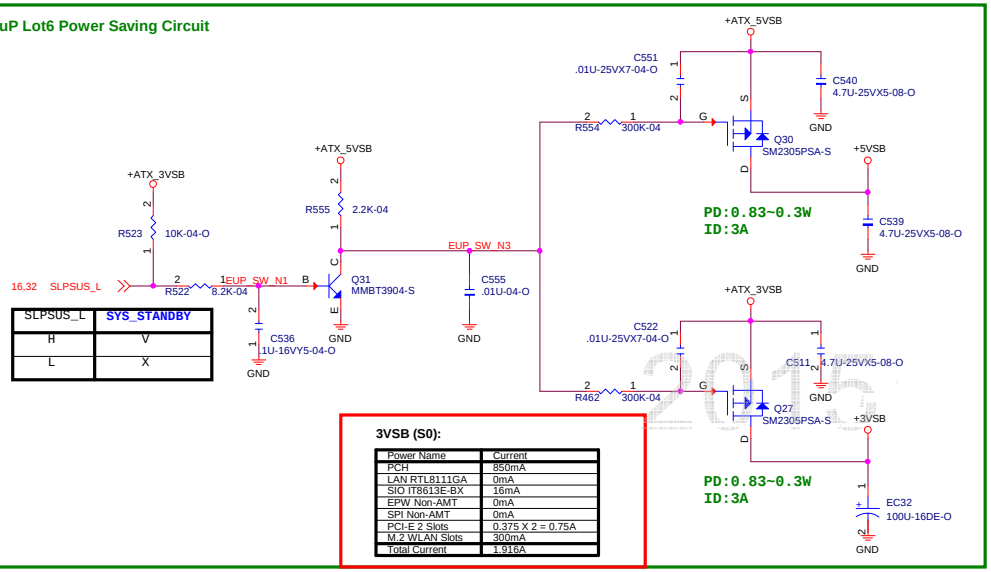
PCH & VCCST PWROK



SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS



EuP Lot6 Power Saving Circuit

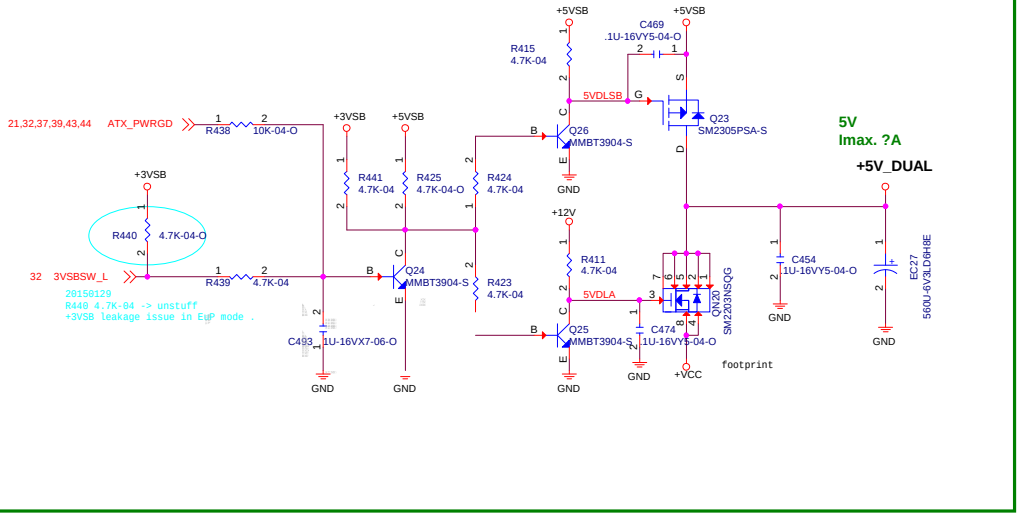


SLPSUS_L	SYS_STANDBY
H	V
L	X

3VSB (S0):

Power Name	Current
PCH	850mA
LAN RTL8111GA	0mA
SIO IT8613E-BX	16mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 2 Slots	0.375 X 2 = 0.75A
M.2 WLAN Slots	300mA
Total Current	1.916A

5VDUAL



Title	DC/DC DDRVPP & 5VDUAL		
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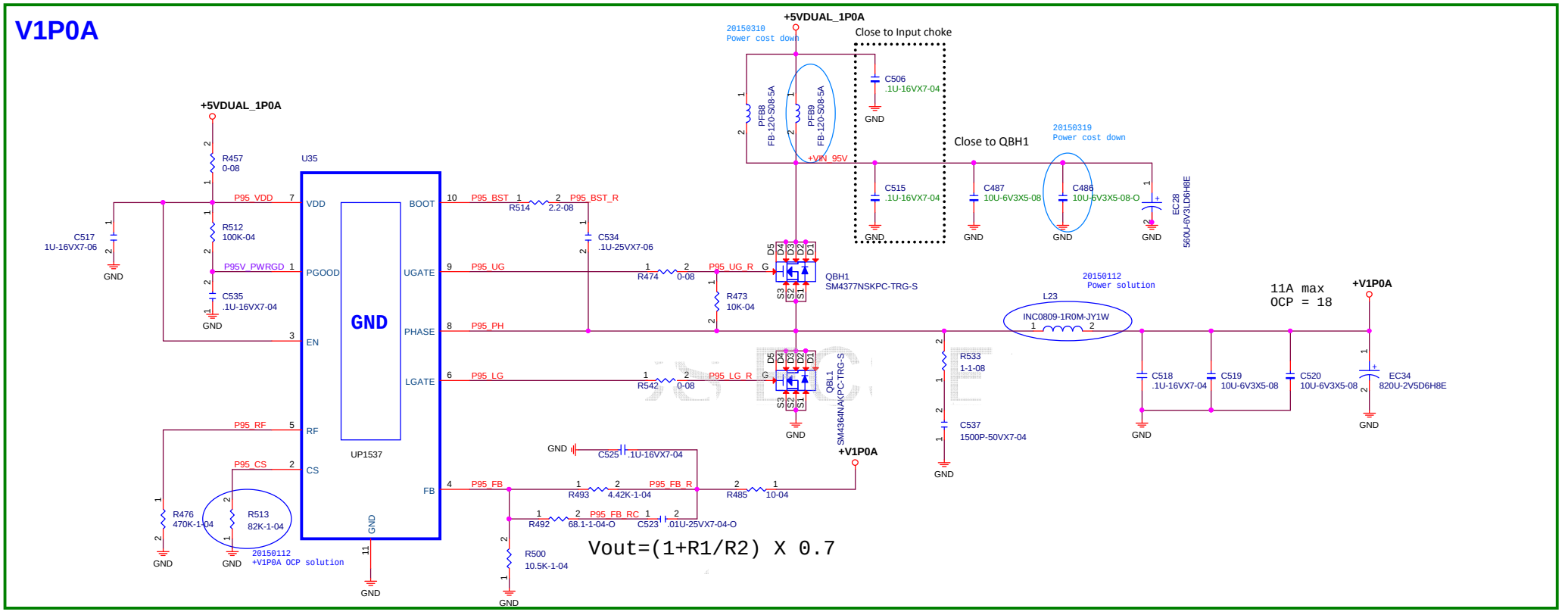
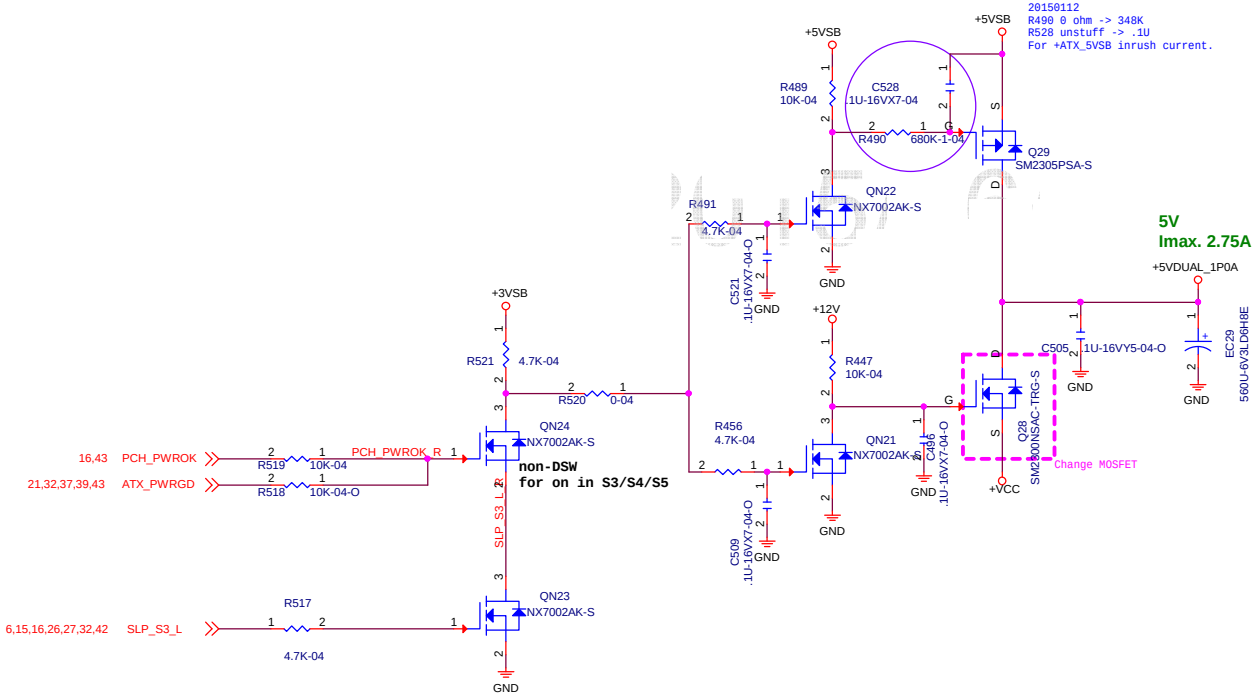
V1P0A





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5 SLP4_L

+1V0_VCCST

+1V35_DIMM

8.2 +VCC3

+0V95_VCCIO

PGOOD[10]

9

+1V05_SA

ISL95858HRZ

VRDY[11]

10

NGFF

(SSD)

NGFF

(For WLAN & BT module)

PCIe X16 Slot

PCIe X1 Slot_1

OnBoard LAN

LPC debug

13 PCH_PLTRST_L

SIO_PCIRST3_L

13

13 PCH_PLTRST_L

RSMRST# de-actives delay 75ms from SYS_3VSB

81 PCIRST3#

LRESET#[34]

3 FP_PWRBTN_L

POWER BUTTON

PANSHW#[33]

RSMRST#[82]

2 RSMRST_L

5 SLP3_L

Super I/O IT8613E-BX

SUSB#[68]

4 SIO_PWRBTN_L

PWRON#[69]

11 PWRGD3

Delay Logic 150ms

1 +3VSB

SYS_3VSB[12]

PWRGD3[75]

9 ATX_PWRGD

ATXPG[16]

VIN[2:3] [92],[93]

PSON#[73]

7

+VCC

+12V

6 PSON_L

ATX_24P 2 EN

+3VSB/5VSB

PLTRST#[BB27]

PCH_PWROK[AW11]

RSMRST#[BA11]

SLP_S3#[AW15]

PLTRST_CPU#[AK2]

PWRBTN#[AT13]

PCH-H

SYS_PWROK[AY1]

PROCPWRGD[AM3]

SLP_SUS

CPU_PLTRST_L

12 PROCPWRGD

RESET#[E7]

S-processor

PROCPWRGD

Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

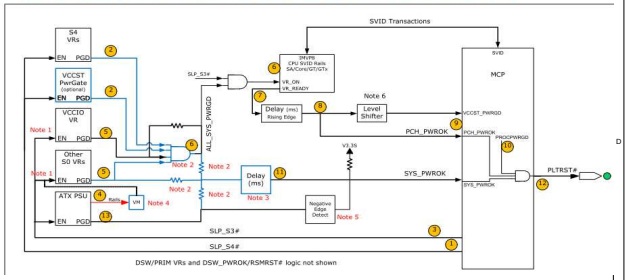
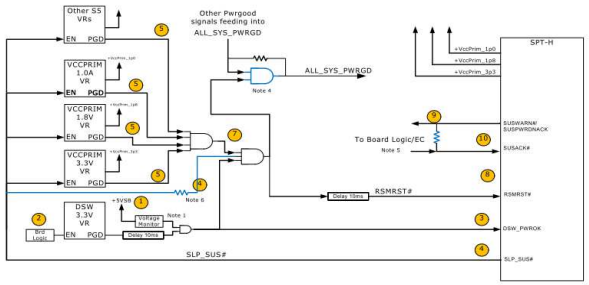


Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation



Title	Power Sequence		
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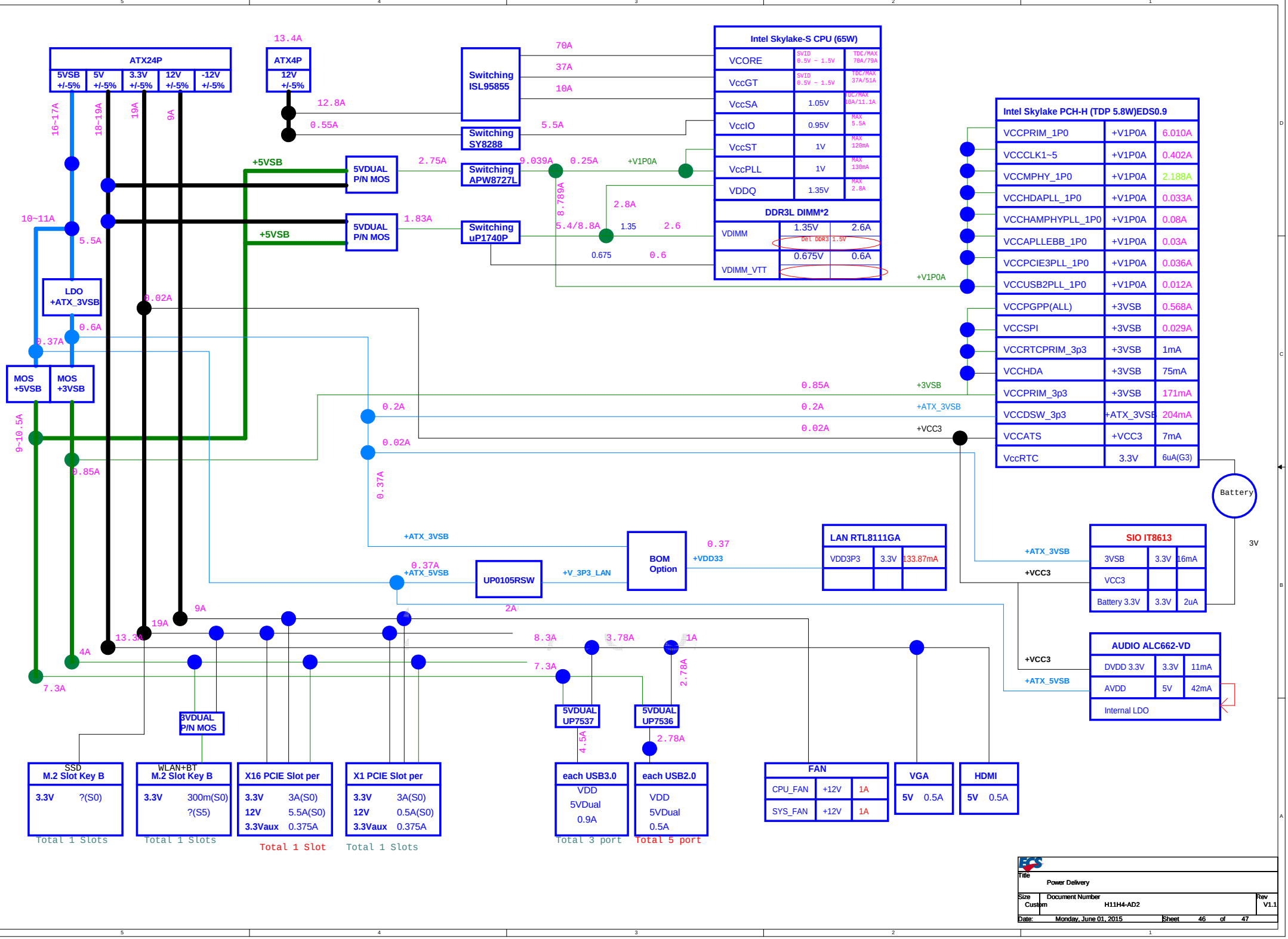
ATX24P
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
13.4A
12.8A
0.55A
16~17A
18~19A
19A
9A
10~11A
5.5A
Switching ISL95855
Switching SY8288
Switching APW8727L
Switching uP1740P
70A
37A
10A
5.5A
9.039A
0.25A
+V1P0A
8.789A
2.8A
5.4/8.8A
1.35
2.6
0.675
0.6
2.75A
1.83A
+5VSB
5VDUAL P/N MOS
5VDUAL P/N MOS
Intel Skylake-S CPU (65W)
VCORE
SVID 0.5V ~ 1.5V
TDC/MAX 70A/79A
VccGT
SVID 0.5V ~ 1.5V
TDC/MAX 37A/51A
VccSA
1.05V
TDC/MAX 10A/11.1A
VccIO
0.95V
MAX 5.5A
VccST
1V
MAX 120mA
VccPLL
1V
MAX 130mA
VDDQ
1.35V
MAX 2.8A
DDR3L DIMM*2
VDIMM
1.35V
2.6A
Del DDR3 1.5V
VDIMM_VTT
0.675V
0.6A
Intel Skylake PCH-H (TDP 5.8W)EDS0.9
VCCPRIM_1P0 +V1P0A 6.010A
VCCCLK1~5 +V1P0A 0.402A
VCCMPHY_1P0 +V1P0A 2.188A
VCCHDAPLL_1P0 +V1P0A 0.033A
VCCHAMPHYPLL_1P0 +V1P0A 0.08A
VCCAPLLEBB_1P0 +V1P0A 0.03A
VCCPCIE3PLL_1P0 +V1P0A 0.036A
VCCUSB2PLL_1P0 +V1P0A 0.012A
VCCPGPP(ALL) +3VSB 0.568A
VCCSPI +3VSB 0.029A
VCCRTCPRIM_3p3 +3VSB 1mA
VCCHDA +3VSB 75mA
VCCPRIM_3p3 +3VSB 171mA
VCCDSW_3p3 +ATX_3VSB 204mA
VCCATS +VCC3 7mA
VccRTC 3.3V 6uA(G3)
LDO +ATX_3VSB
0.02A
0.6A
0.37A
MOS +5VSB
MOS +3VSB
9~10.5A
0.85A
0.85A +3VSB
0.2A +ATX_3VSB
0.02A +VCC3
0.02A
0.37A
Battery
3V
+ATX_3VSB
0.37A
+ATX_5VSB
UP0105RSW
+V_3P3_LAN
BOM Option
0.37
+VDD33
LAN RTL8111GA
VDD3P3 3.3V 133.87mA
SIO IT8613
3VSB 3.3V 16mA
VCC3
Battery 3.3V 3.3V 2uA
+ATX_3VSB
+VCC3
AUDIO ALC662-VD
DVDD 3.3V 3.3V 11mA
AVDD 5V 42mA
Internal LDO
+VCC3
+ATX_5VSB
2A
9A
19A
13.3A
4A
7.3A
8.3A
3.78A
1A
7.3A
2.78A
3VDUAL P/N MOS
5VDUAL UP7537
5VDUAL UP7536
4.5A
2.78A
SSD
M.2 Slot Key B
3.3V ?(S0)
Total 1 Slots
WLAN+BT
M.2 Slot Key B
3.3V 300m(S0)
?(S5)
Total 1 Slots
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 1 Slots
each USB3.0
VDD
5VDual
0.9A
Total 3 port
each USB2.0
VDD
5VDual
0.5A
Total 5 port
FAN
CPU_FAN +12V 1A
SYS_FAN +12V 1A
VGA
5V 0.5A
HDMI
5V 0.5A
Title
Power Delivery
Size
Custom
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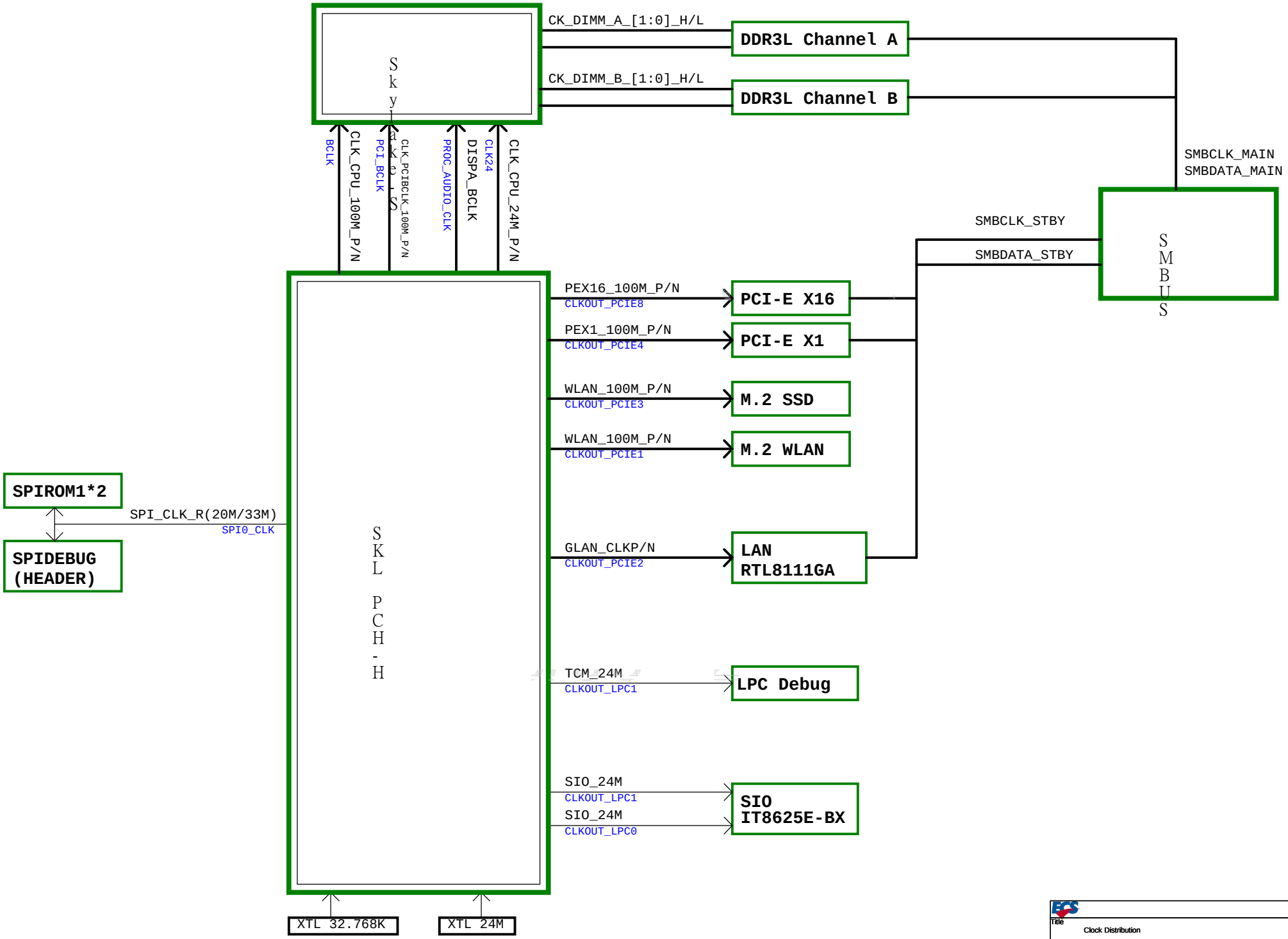

Title	Clock Distribution	
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