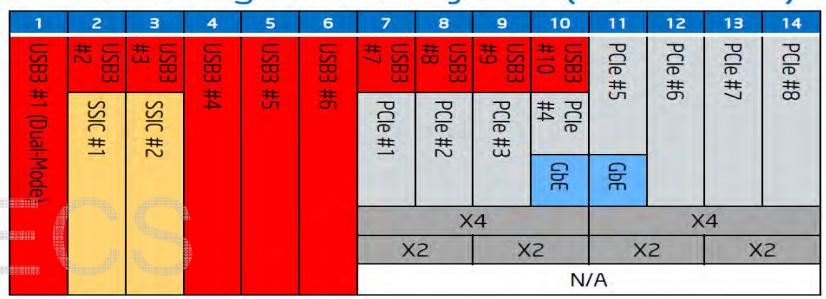
SKYLAKE-S V:1.0

ECS CONFIDENTIAL

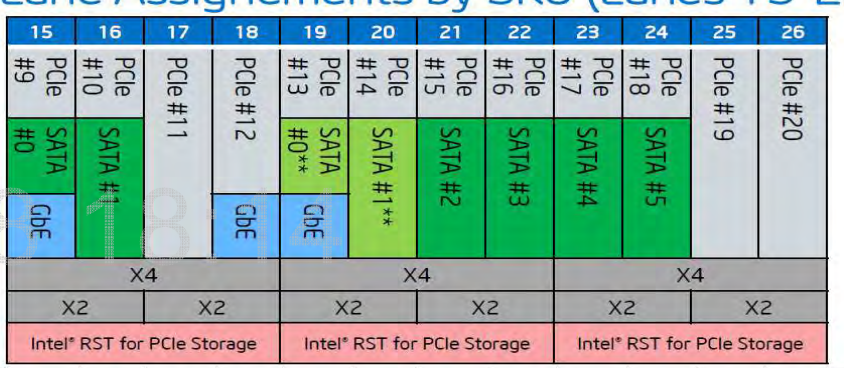
SCHEMATICS TABLE:

HSIO Lane Assignements by SKU (Lanes 1-14)



sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
Q150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe/ LAN	PCIe	PCIe	PCIe
Q170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe	USB3/ PCIe/ LAN	PCIe /LAN	PCIe	PCIe	PCIe

HSIO Lane Assignements by SKU (Lanes 15-26)

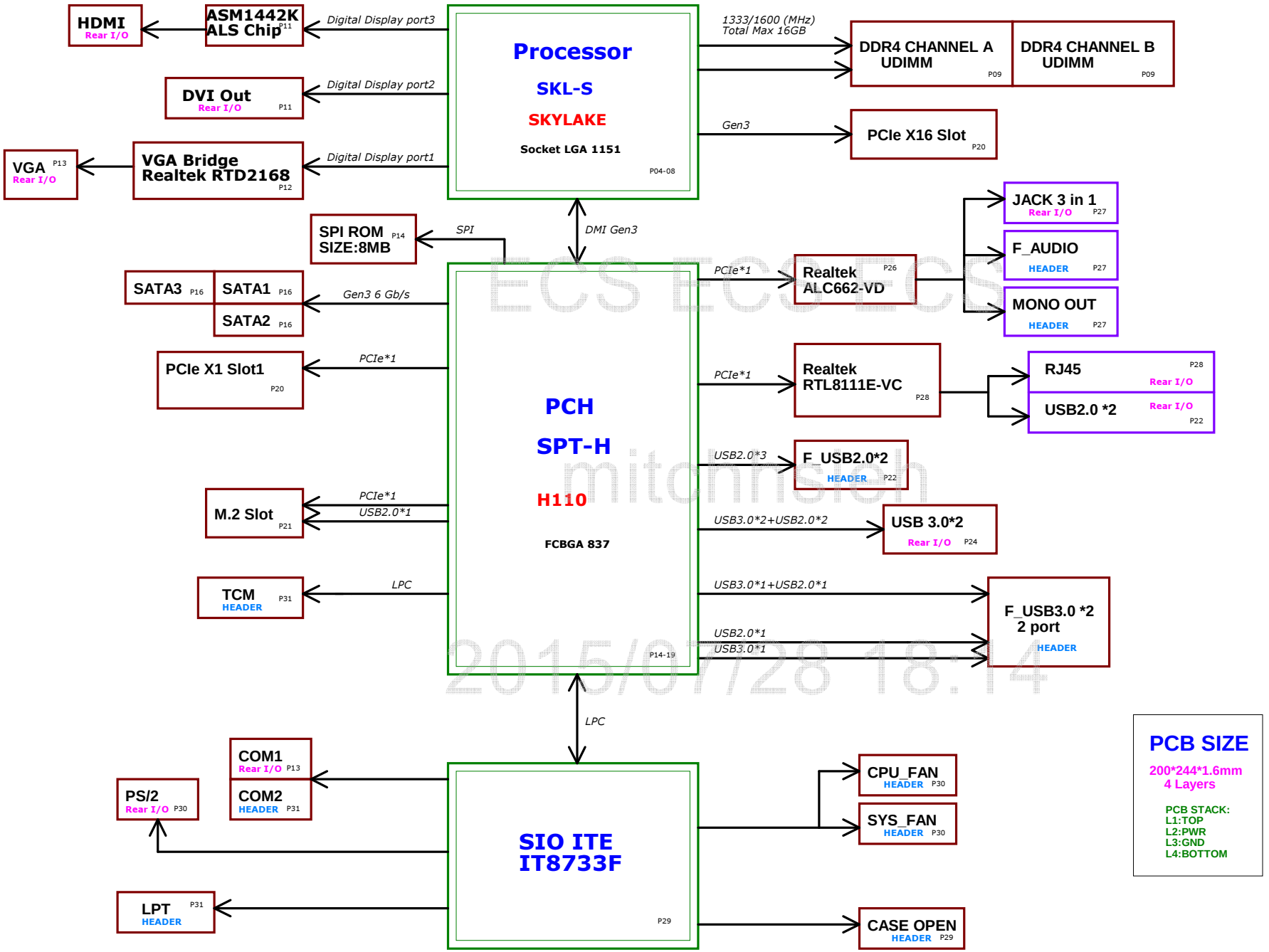


Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A	0
B150	PCIe/LAN SATA*	PCIe/ SATA*	PCIe	PCIe/ LAN	SATA* /LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A	0
Q150	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	SATA	SATA	SATA	SATA	N/A	N/A	0
H170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	SATA	SATA	PCIe	PCIe	2
Z170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3
Q170	PCIe/LAN SATA	PCIe/ SATA	PCIe	PCIe/ LAN	PCIe/LAN SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe/ SATA	PCIe	PCIe	3

Elitegroup Computer Systems

Title: Cover Page		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 1 of 46	

Skylake-S Desktop Platform



PCB SIZE

200*244*1.6mm
4 Layers

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

Elitegroup Computer Systems		
Title: Block Diagram		
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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPP_F17	3VSB	LPC_PME_L	PME# GPI
GPD10	ATX_3VSB	GPD10 (GPD10_DIS_ME)	GPD10 OUTPUT Low/Normal, High/ME disable
GPP_B13	N/A	PCH_PLTRST_L	PLTRST#
GPP_G16	N/A	GPP_G16	GPO S0/S3/S4/S5:High
GPP_G15	VCC3	GPP_G15 (TMP Header Sel)	GPI
GPP_G13	VCC3	HDPANEL_DETECT	GPI
GPP_E7	VCC3	THERMAL_SD	GPI
GPP_B3	VCC3	BT_DIS_L_R	GPO S0/S3/S4/S5:High
GPP_H18	3VSB	GPP_H18	GPI
GPP_H17	3VSB	GPP_H17	GPI
GPP_H16	3VSB	GPP_H16	GPI
GPP_H15	3VSB	GPP_H15	For Acer Reserve
GPP_H14	3VSB	GPP_H14	For Acer Reserve
GPP_B14	+VCC3	PCH_SPKR	SPKR
GPP_A14	3VSB	LPCPD_L	SUS_STAT#
GPP_C6	3VSB	SML1_CLK	SML1CLK
GPP_C7	3VSB	SML1_DATA	SML1DATA
GPP_E8	VCC3	SATALED_L	SATALED#
GPP_E9	3VSB	GPP_E9 (BIOS WP)	GPI INPUT Low/Normal, High/BIOS WP
GPP_E10	3VSB	GPP_E10 (SW BIOS WP)	GPO OUTPUT Low/BIOS WP, High/Normal
GPP_E0	VCC3	GPP_E0 (OBR)	GPI
GPP_E4	VCC3	GPP_E4	GPO S0/S3/S4/S5:High
GPP_F22	VCC3	PCH_GPP_F22 (PCIEX16RST)	GPO S0:High S3/S4/S5:Low
GPP_F16	3VSB	GPP_F16 (USB_EN)	GPO S0/S3:High S4/S5:Low
GPP_F14	3VSB	H_SKTOCC_L	GPI
GPP_B17	VCC3	M.2_DIS_L_R	GPO S0/S3/S4/S5:High
GPP_B6	VCC3	CLK_REQ1_M.2_WLAN_L	GPO
GPP_B8	VCC3	GPP_B8	GPI
GPD0	DSW	RLAN_PWR_EN	GPO
GPP_D4	3VSB	SIO_GP16(PC_health)	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP37	+DIMM_5VDUAL	SIO_LED1	FAN_TAC3(DI)
GP36	3VSB	THERMAL_SD	FAN_CTL3(DOD8)
GP35	+DIMM_5VDUAL	SIO_LED0	FAN_TAC4(DI)
GP34	3VSB	SUSWARN_L	SUSWARN#(DOD8)
GP33	3VSB	SUSACK_L	SUSACK#(DOD8)
GP32	ATX3VSB	DPWROK	DPWROK(DOD8)
GP30	VCC	ATX_PWRGD	ATXPG(DI)
GP14	3VSB	SML1_CLK	VCORE_EN(DOD8)
N/A	3VSB	SML1_DATA	PCH_D1
GP13	VCC3	PCH_SYSPWROK	PWROK1(DOD8)
GP12	N/A	PCIRST1_L	PCIRST1#(DO8)
GP11	N/A	PCIRST2_L	PCIRST2#(DO8)
GP44	3VSB	SIO_PWRON_L	PWRON#(DOD8)
GP54	3VSB	LPC_PME_L	PME#(DOD8)
GP43	ATX5VSB	FP_PWRBTN_L	PANSWH#(DI)
GP42	ATX3VSB	ATX_PSON_L	PSON#(DOD8)
GP53	N/A	SLP_S4_L	SUSC#(DI)
GP40	3VSB	3VSBSW_L	3VSBSW#(DO8)
GP10	N/A	PCIRST3_L	PCIRST3#(DO8)
GP55	3VSB	RSMRST_L	RSMRST3#(DOD8)
GP16	3VSB	SIO_GP16(PC_health)	5VSB_CTRL3#(DOD8)

CPU-Strap

Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	PCIE16X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP enable:	1 = Disabled.
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable “Top Swap” mode. (Default)
GSPI0_MOSI/GPP_B18	No Reboot	0 =Disable “No Reboot” mode
SMBALERT#/GPP_C2	TLS Confidentiality	1 =EnableIntel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit BBS	0=SPI
SML0ALERT#/GPP_C5	eSPI or LPC	0 =LPCIs selected for EC.
HDA_SDO	Flash Descriptor Security Override	This signal has a weak internal pull-down. 0 =Enable security measures defined in the Flash Descriptor. 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.

Elitegroup Computer Systems			
Title: GPIO Function & INT# Mapping			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
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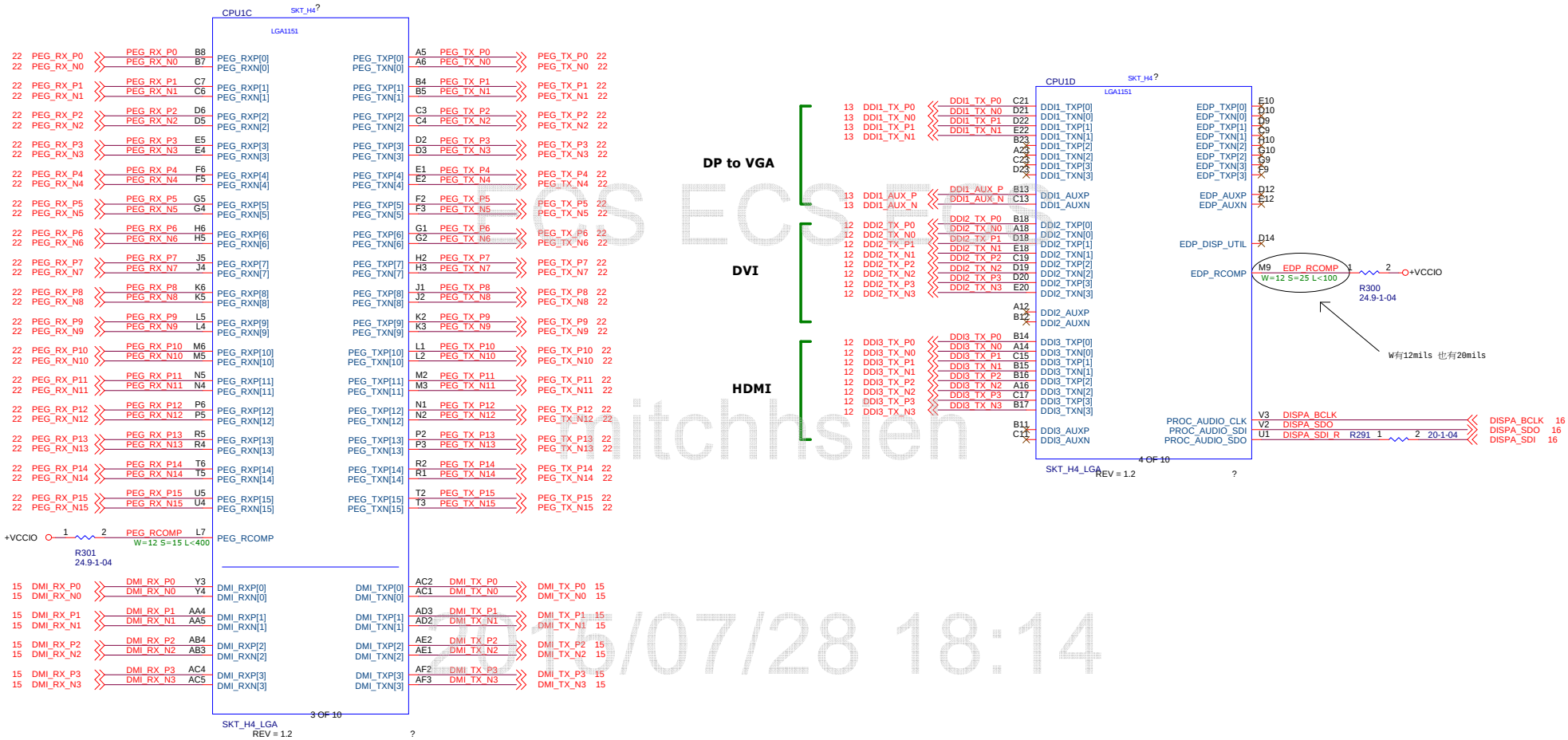
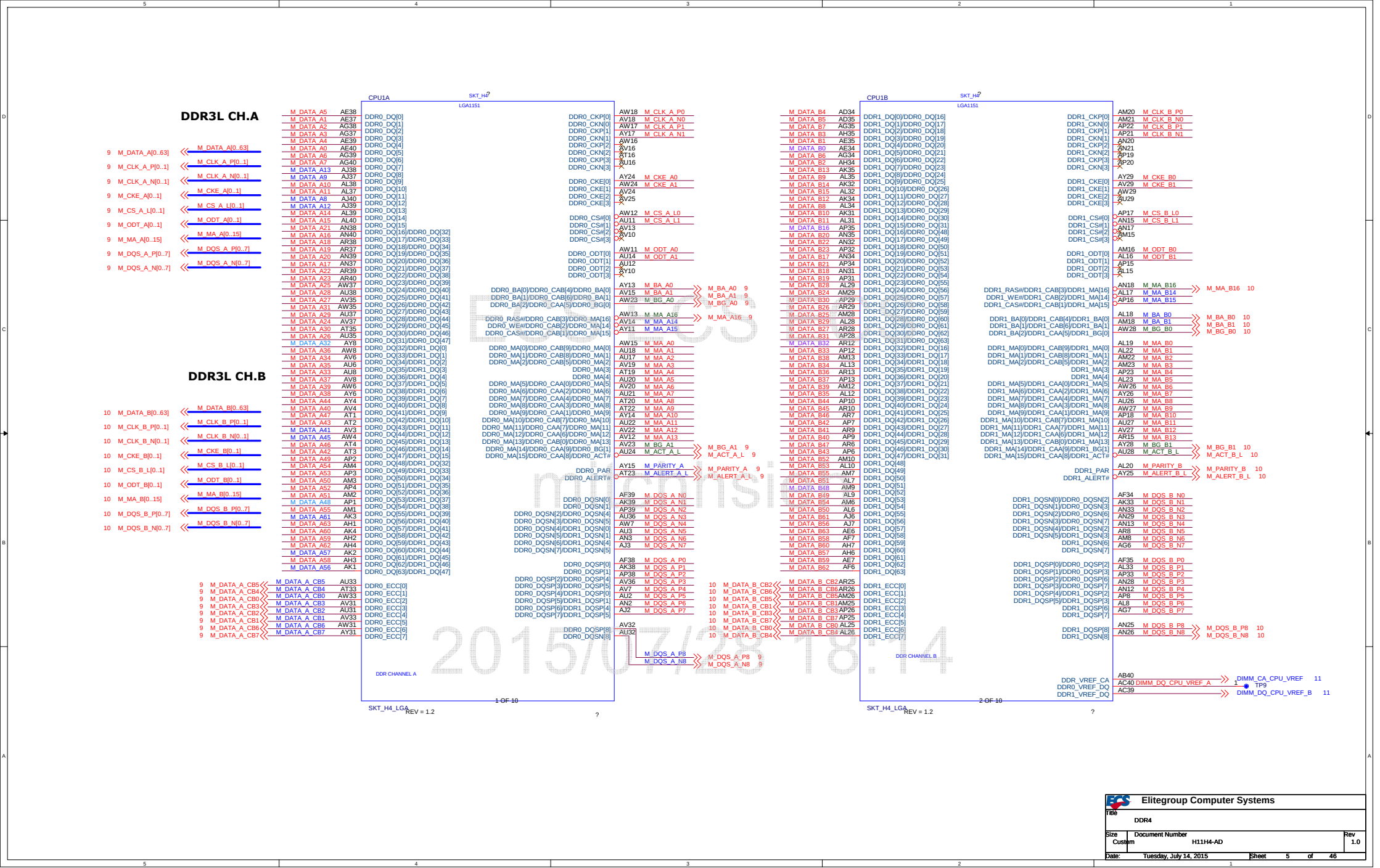


Elitegroup Computer Systems			
Title: CPU-PEG/DMI/DDI/EDP			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 4 of 46		



Company	Elitegroup Computer Systems
Title	DDR4
Size	Custom
Document Number	H11H4-AD
Rev	1.0
Date:	Tuesday, July 14, 2015
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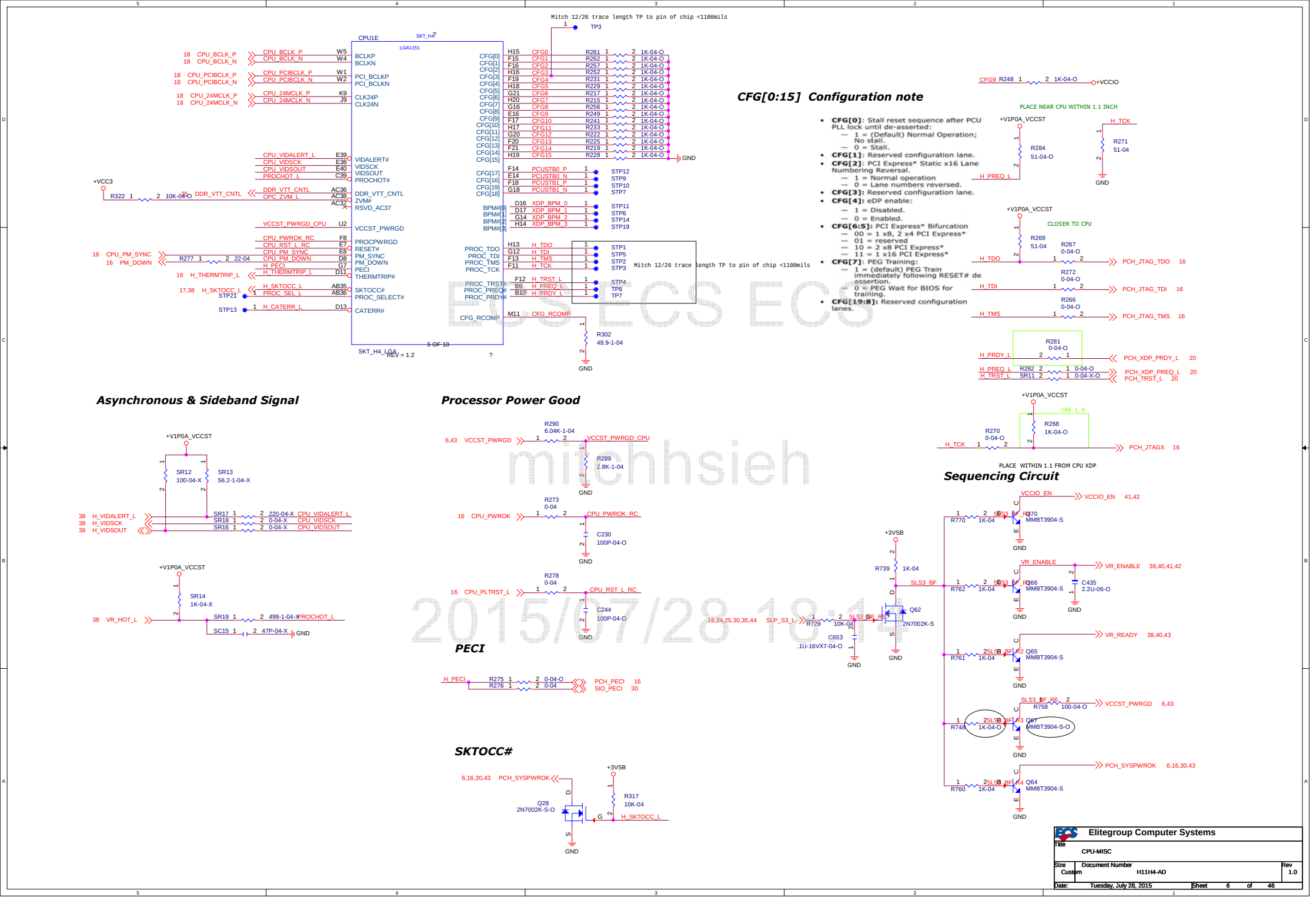
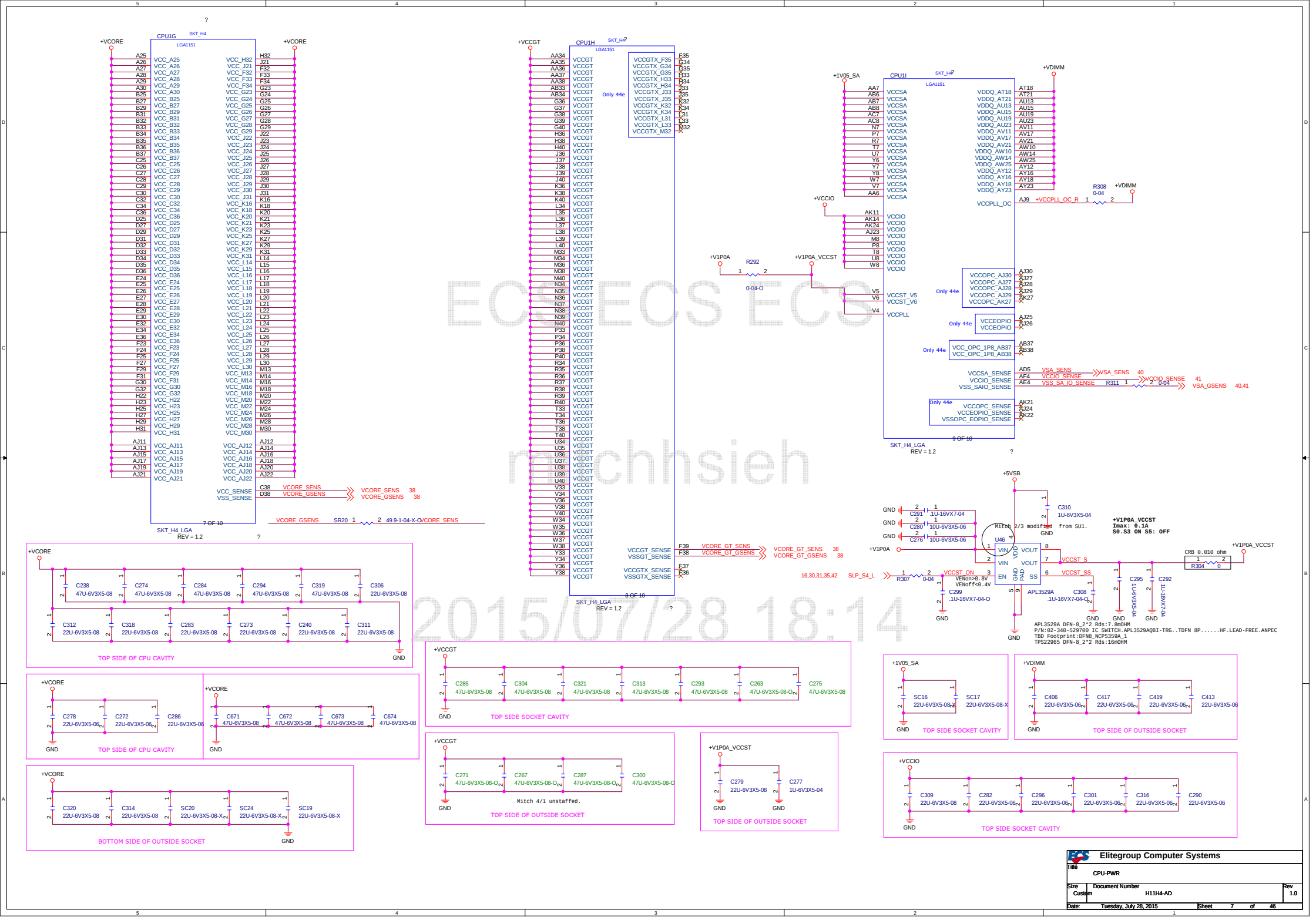

Mitch 12/26 trace length TP to pin of chip <1100mils
CPU1E
SKT_H4
LGA1151
CFG[0:15] Configuration note
Asynchronous & Sideband Signal
Processor Power Good
Sequencing Circuit
PECI
SKTOCC#
PLACE NEAR CPU WITHIN 1.1 INCH
CLOSER TO CPU
PLACE WITHIN 1.1 FROM CPU XDP
Elitegroup Computer Systems
CPU-MISC
H11H4-AD
Tuesday, July 28, 2015


CPU1G
SKT_H4
LGA1151
+VCORE
VCC_A25
VCC_A26
VCC_A27
VCC_A28
VCC_A29
VCC_A30
VCC_B25
VCC_B27
VCC_B29
VCC_B31
VCC_B32
VCC_B33
VCC_B34
VCC_B35
VCC_B36
VCC_B37
VCC_C25
VCC_C26
VCC_C27
VCC_C28
VCC_C29
VCC_C30
VCC_C32
VCC_C34
VCC_C36
VCC_D25
VCC_D27
VCC_D29
VCC_D31
VCC_D32
VCC_D33
VCC_D34
VCC_D35
VCC_D36
VCC_E24
VCC_E25
VCC_E26
VCC_E27
VCC_E28
VCC_E29
VCC_E30
VCC_E32
VCC_E34
VCC_E36
VCC_F23
VCC_F24
VCC_F25
VCC_F27
VCC_F29
VCC_F31
VCC_G30
VCC_G32
VCC_H22
VCC_H23
VCC_H25
VCC_H27
VCC_H29
VCC_H31
VCC_AJ11
VCC_AJ13
VCC_AJ15
VCC_AJ17
VCC_AJ19
VCC_AJ21
VCC_H32
VCC_J21
VCC_F32
VCC_F33
VCC_F34
VCC_G23
VCC_G24
VCC_G25
VCC_G26
VCC_G27
VCC_G28
VCC_G29
VCC_J22
VCC_J23
VCC_J24
VCC_J25
VCC_J26
VCC_J27
VCC_J28
VCC_J29
VCC_J30
VCC_J31
VCC_K16
VCC_K18
VCC_K20
VCC_K21
VCC_K23
VCC_K25
VCC_K27
VCC_K29
VCC_K31
VCC_L14
VCC_L15
VCC_L16
VCC_L17
VCC_L18
VCC_L19
VCC_L20
VCC_L21
VCC_L22
VCC_L23
VCC_L24
VCC_L25
VCC_L26
VCC_L27
VCC_L28
VCC_L29
VCC_L30
VCC_M13
VCC_M14
VCC_M16
VCC_M18
VCC_M20
VCC_M22
VCC_M24
VCC_M26
VCC_M28
VCC_M30
VCC_AJ12
VCC_AJ14
VCC_AJ16
VCC_AJ18
VCC_AJ20
VCC_AJ22
VCC_SENSE
VSS_SENSE
VCORE_SENS
VCORE_GSENS
VCORE_SENS 38
VCORE_GSENS 38
SR20
49.9-1-04-X-O
VCORE_SENS
7 OF 10
SKT_H4_LGA
REV = 1.2
CPU1H
+VCCGT
VCCGT
VCCGTX_F35
VCCGTX_G34
VCCGTX_G35
VCCGTX_H33
VCCGTX_H34
VCCGTX_J33
VCCGTX_J35
VCCGTX_K32
VCCGTX_K34
VCCGTX_L31
VCCGTX_L33
VCCGTX_M32
Only 44e
VCCGT_SENSE
VSSGT_SENSE
VCCGTX_SENSE
VSSGTX_SENSE
VCORE_GT_SENS
VCORE_GT_GSENS
VCORE_GT_SENS 38
VCORE_GT_GSENS 38
8 OF 10
CPU1I
+1V05_SA
VCCSA
VDDQ_AT18
VDDQ_AT21
VDDQ_AU13
VDDQ_AU15
VDDQ_AU19
VDDQ_AU23
VDDQ_AV11
VDDQ_AV17
VDDQ_AV21
VDDQ_AW10
VDDQ_AW14
VDDQ_AW25
VDDQ_AY12
VDDQ_AY16
VDDQ_AY18
VDDQ_AY23
VCCPLL_OC
+VDIMM
R308
0-04
+VCCPLL_OC_R
+VCCIO
VCCIO
VCCPC_AJ30
VCCPC_AJ27
VCCPC_AJ28
VCCPC_AJ29
VCCPC_AK27
VCCEOPIO
VCC_OPC_1P8_AB37
VCC_OPC_1P8_AB38
VCCSA_SENSE
VCCIO_SENSE
VSS_SAIO_SENSE
VSA_SENS
VCCIO_SENSE
VSS_SA_IO_SENSE
VSA_SENS 40
VCCIO_SENSE 41
VSA_GSENS 40,41
VCCPC_SENSE
VCCEOPIO_SENSE
VSSOPC_EOPIO_SENSE
9 OF 10
+V1P0A
R292
0-04-O
+V1P0A_VCCST
VCCST_V5
VCCST_V6
VCCPLL
+5VSB
U46
VIN
VOUT
EN
SS
GND
PAD
VCCST_ON
VENon>0.8V
VENoff<0.4V
VCCST_S
VCCST_SS
APL3529A
Mitch 2/3 modified from SU1.
+V1P0A_VCCST
Imax: 0.1A
S0.S3 ON S5: OFF
CRB 0.010 ohm
R304
R307
SLP_S4_L
16,30,31,35,42
APL3529A DFN-8_2*2 Rds:7.8mOHM
P/N:02-340-529700 IC SWITCH.APL3529AQBI-TRG..TDFN 8P.....HF.LEAD-FREE.ANPEC
TBD Footprint:DFN8_NCP5359A_1
TPS22965 DFN-8_2*2 Rds:16mOHM
TOP SIDE OF CPU CAVITY
TOP SIDE SOCKET CAVITY
TOP SIDE OF OUTSIDE SOCKET
BOTTOM SIDE OF OUTSIDE SOCKET
Mitch 4/1 unstaffed.
Elitegroup Computer Systems
CPU-PWR
H11H4-AD
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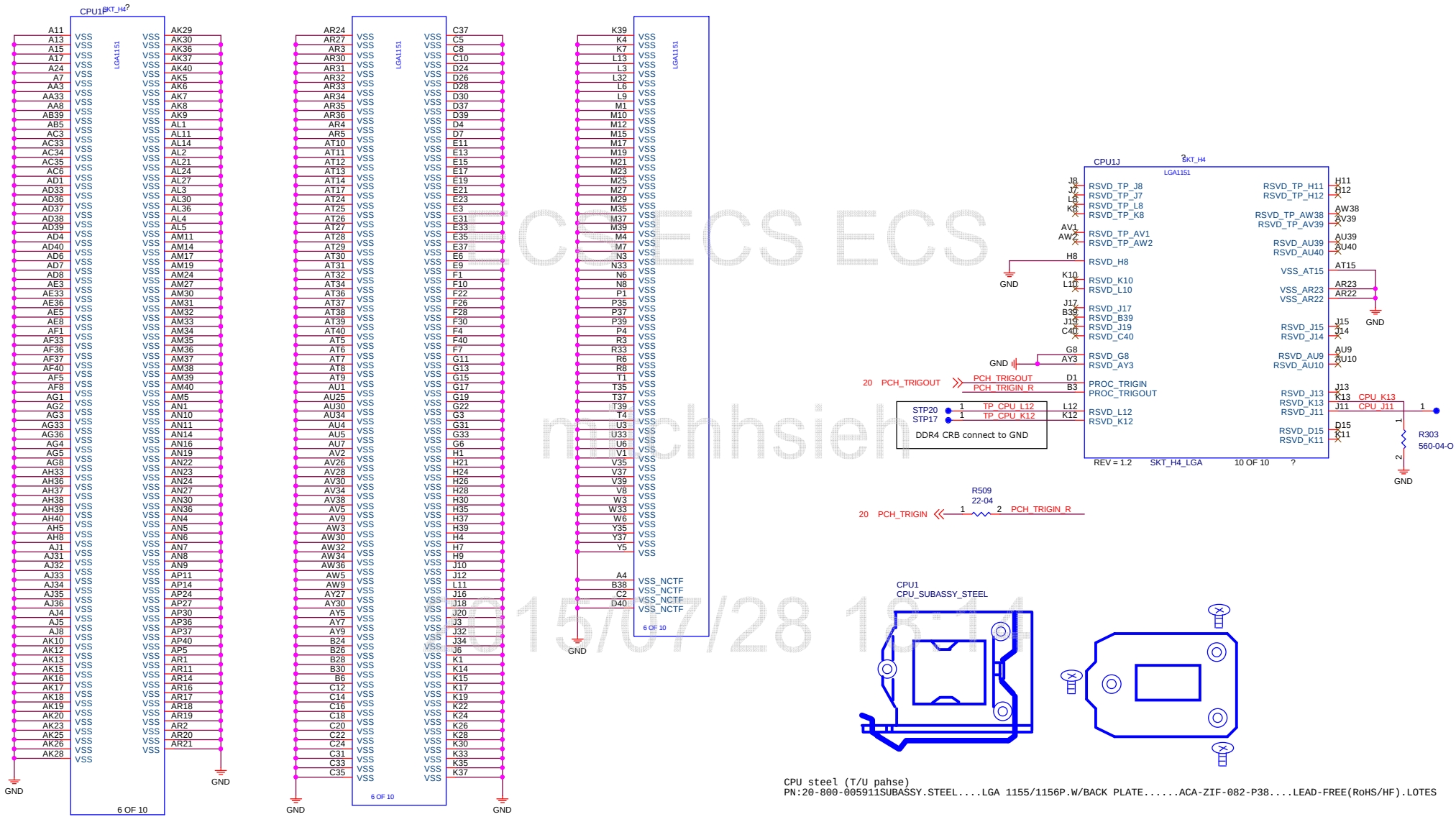
7
46
1.0



CPU steel (T/U pahse)
PN:20-800-005911SUBASSY.STEEL....LGA 1155/1156P.W/BACK PLATE.....ACA-ZIF-082-P38....LEAD-FREE(RoHS/HF).LOTES

Elitegroup Computer Systems		
Title: CPU-GND		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
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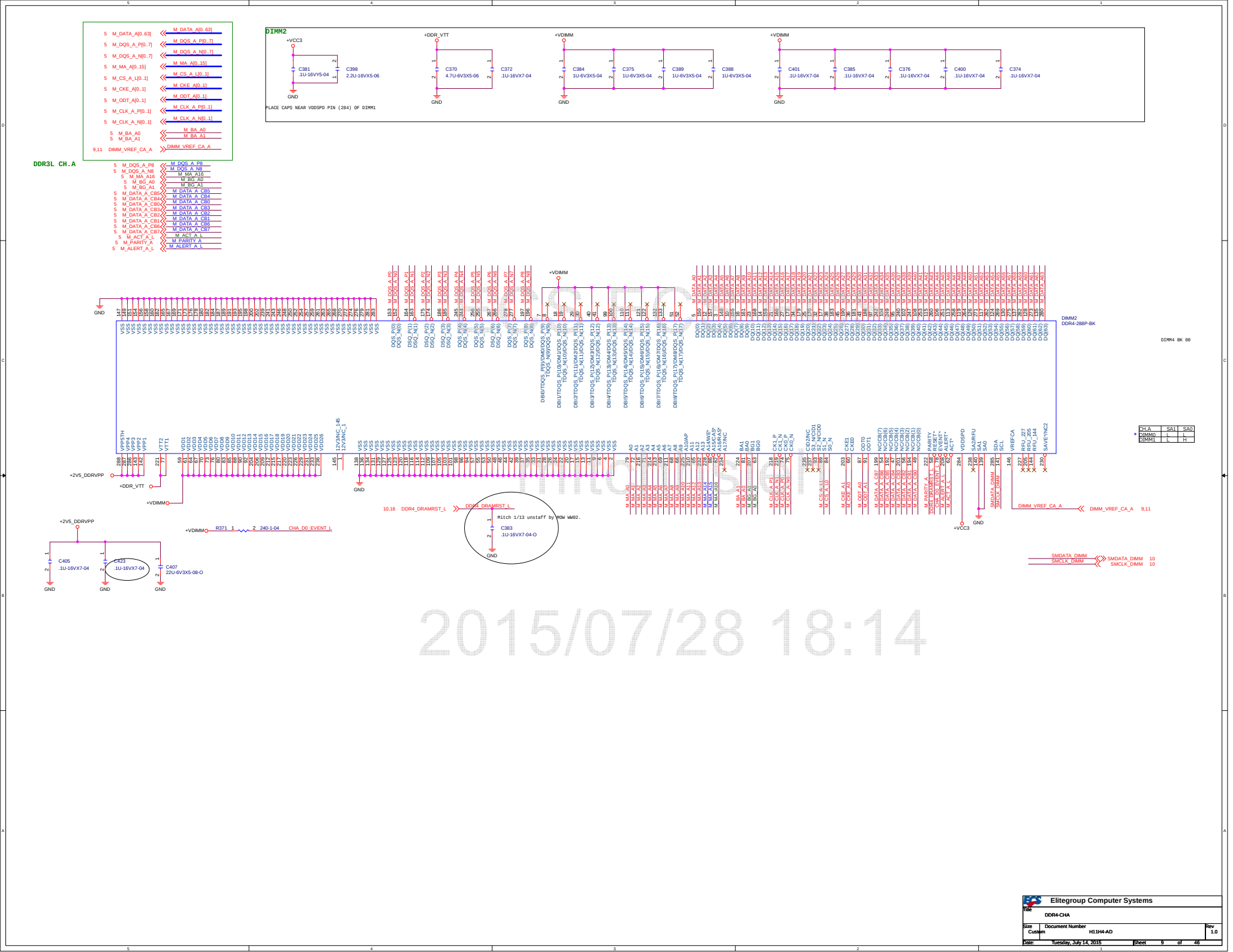
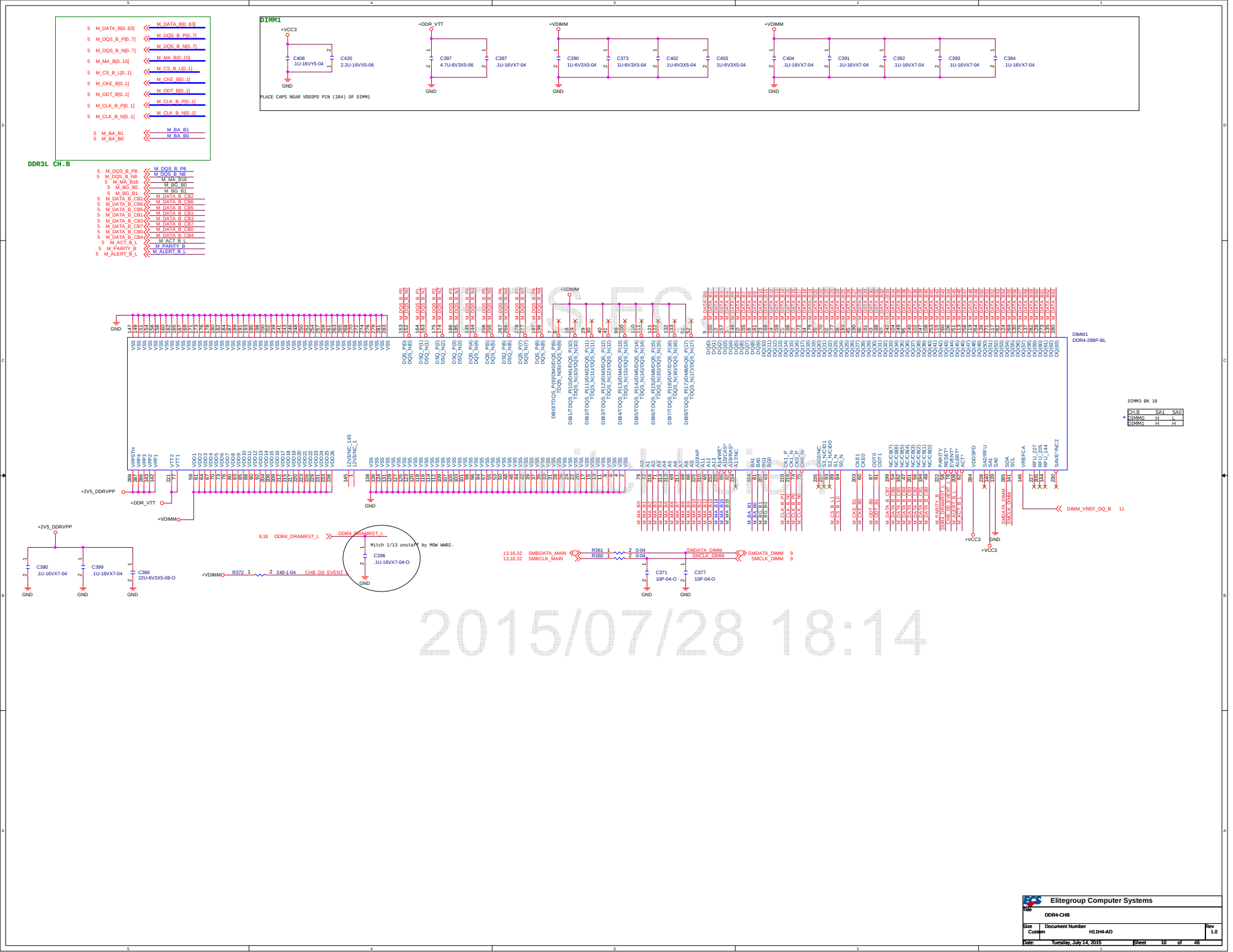

DIMM2
PLACE CAPS NEAR VDDSPD PIN (284) OF DIMM1
C381 .1U-16VY5-04
C398 2.2U-16VX5-06
C370 4.7U-6V3X5-06
C372 .1U-16VX7-04
C384 1U-6V3X5-04
C375 1U-6V3X5-04
C389 1U-6V3X5-04
C388 1U-6V3X5-04
C401 .1U-16VX7-04
C385 .1U-16VX7-04
C376 .1U-16VX7-04
C400 .1U-16VX7-04
C374 .1U-16VX7-04
DDR3L CH.A
DIMM2 DDR4-288P-BK
DIMM4 BK 00
C405 .1U-16VX7-04
C423 .1U-16VX7-04
C407 22U-6V3X5-08-O
R371 240-1-04 CHA_D0_EVENT_L
C383 .1U-16VX7-04-O
Mitch 1/13 unstaff by MOW WW82.
CH.A SA1 SA0
DIMM0 L L
DIMM1 L H
2015/07/28 18:14



Elitegroup Computer Systems	
Title	DDR4-CHB
Size: Custom	Document Number: H11H4-AD
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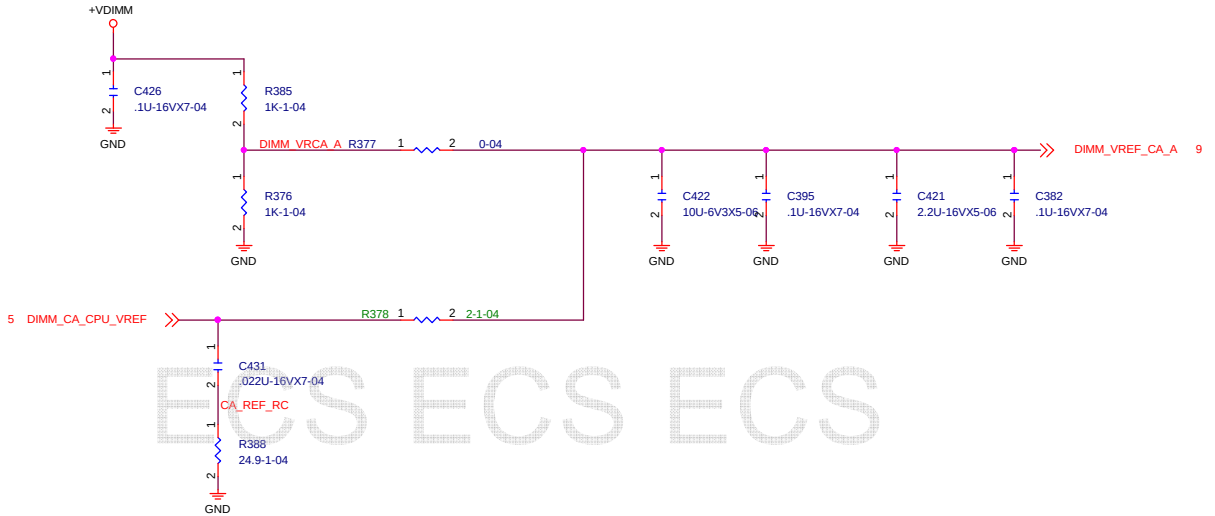
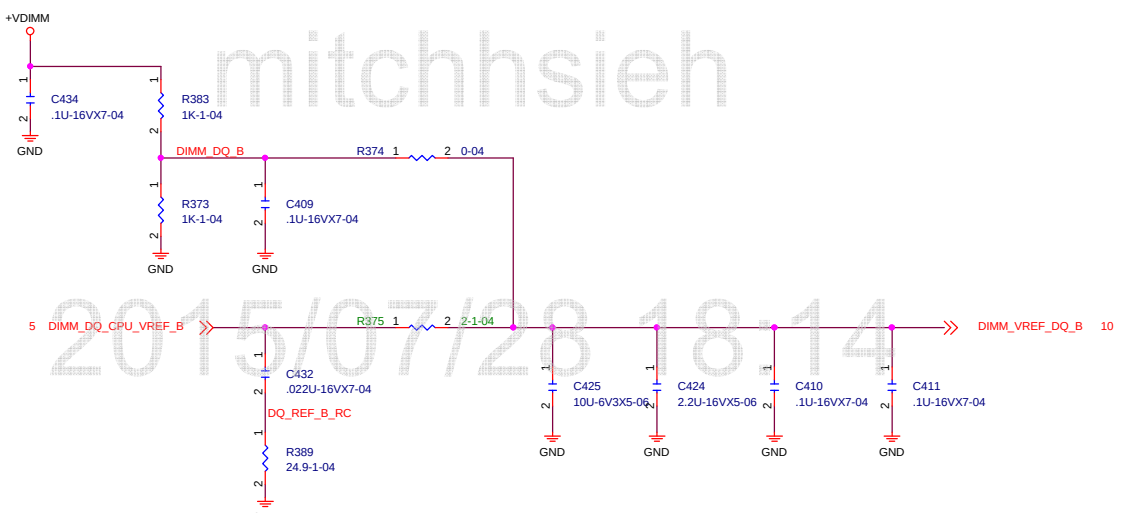
DIMM_VREF_CA



DIMM_VREF_DQ



Elitegroup Computer Systems		
Title: DDR3L-CHB		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
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Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN

HDMI

HDMI的DDI_TX組號,TX0和TX2必須交換1次

4	DDI3_TX_N3	C84 1	2 1U-16VX7-04-O	HDMI_CLK_N3	
4	DDI3_TX_P3	C83 1	2 1U-16VX7-04-O	HDMI_CLK_P3	
4	DDI3_TX_N2	C82 1	2 1U-16VX7-04-O	HDMI_TX_N0	
4	DDI3_TX_P2	C81 1	2 1U-16VX7-04-O	HDMI_TX_P0	
4	DDI3_TX_N1	C80 1	2 1U-16VX7-04-O	HDMI_TX_N1	
4	DDI3_TX_P1	C79 1	2 1U-16VX7-04-O	HDMI_TX_P1	
4	DDI3_TX_N0	C78 1	2 1U-16VX7-04-O	HDMI_TX_N2	
4	DDI3_TX_P0	C77 1	2 1U-16VX7-04-O	HDMI_TX_P2	

SDA, SCL對地電容，Default 先不要上件， 如 EMI 需求須上件， 請務必確認可以 Pass HDMI 的 Spec

HDMI Connector Pin13:CEC
沒有使用必須空接(Floating)
避免HDCP 測試 FAIL

HDMI-19P-O

CHOKE1 CMK-90-08-HDMI-O
CHOKE2 CMK-90-08-HDMI-O
CHOKE3 CMK-90-08-HDMI-O
CHOKE4 CMK-90-08-HDMI-O

RN1 0-8P4R-O
RN2 0-8P4R-O
Co-lay

SQ2 BAT54A-S-X-O
SQ1 2N7002K-S-X-O
Q13 2N7002K-S-O
Q14 2N7002K-S-O
Q15 2N7002K-S-O
Q16 2N7002K-S

U1 AZ1045-04F-S-O
U3 AZ1045-04F-S-O
U10 AZC099-04S-R7G-S-O

DVI

HDMI的DDI_TX組號,TX0和TX2必須交換1次

4	DDI2_TX_P0	C108 1	2 .1U-16VX7-04	DVI_TX_P2	
4	DDI2_TX_N0	C109 1	2 .1U-16VX7-04	DVI_TX_N2	
4	DDI2_TX_P1	C110 1	2 .1U-16VX7-04	DVI_TX_P1	
4	DDI2_TX_N1	C111 1	2 .1U-16VX7-04	DVI_TX_N1	
4	DDI2_TX_P2	C112 1	2 .1U-16VX7-04	DVI_TX_P0	
4	DDI2_TX_N2	C113 1	2 .1U-16VX7-04	DVI_TX_N0	
4	DDI2_TX_P3	C114 1	2 .1U-16VX7-04	DVI_CLK_P3	
4	DDI2_TX_N3	C115 1	2 .1U-16VX7-04	DVI_CLK_N3	

1. 16-400-900143 COMMON CHOKE.90 OHM..SMD 0805..HDMI2012F2SF-900T04,400mA...LEAD-FREE(RoHS).TAI-TECH
2. 16-400-900171 COMMON CHOKE.90 OHM.25%.SMD 0805..QTCW2012H-090-LF.300mA....LEAD-FREE(RoHS/HF).MAGIC

CHOKE11 CMK-90-08-HDMI
CHOKE12 CMK-90-08-HDMI
CHOKE13 CMK-90-08-HDMI
CHOKE14 CMK-90-08-HDMI
Mitch 4/15 VB staffed.

RN7 0-8P4R-O Mitch 4/15 VB unstaffed.
RN8 0-8P4R-O Mitch 4/15 VB unstaffed.

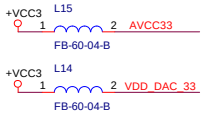
U7 AZ1045-04F-S-O
U8 AZ1045-04F-S-O
U2 AZC099-04S-R7G-S-O

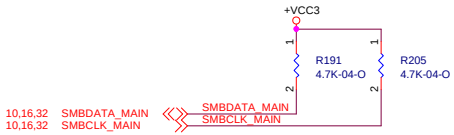
SQ3 BAT54A-S-X
Q11 2N7002K-S
Q10 2N7002K-S
Q7 2N7002K-S

DVI-24P-SH-HIT

Elitegroup Computer Systems			
Title: DP/HDMI			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 12 of 46		

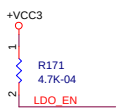
Power



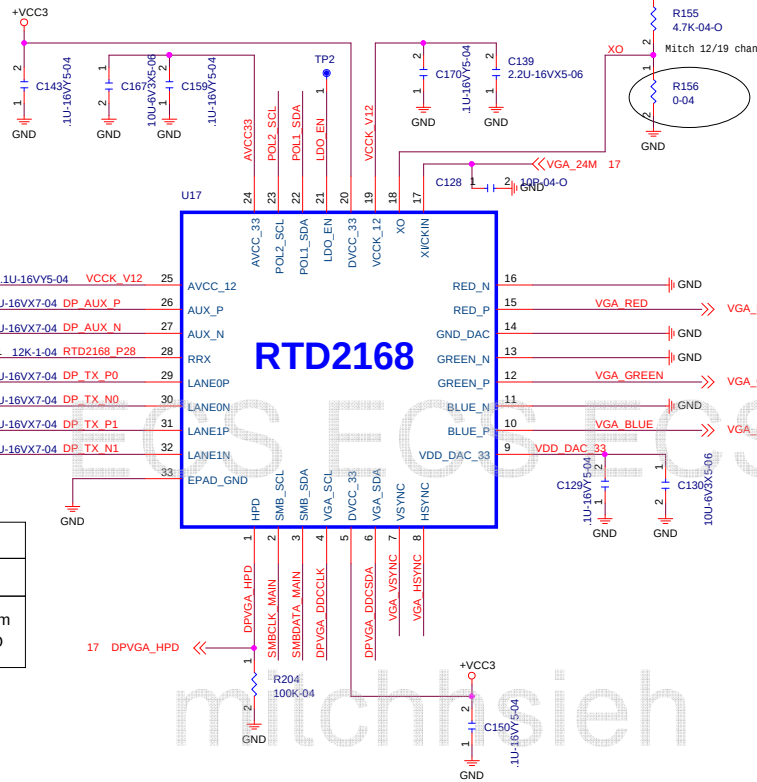


IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69



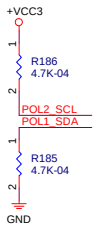
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

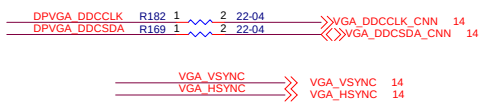


Note: When connected to non-EDID monitor,
XO Pin Pull Down : Disable RTD2168 embedded EDID, CPU handle.
XO Pin Pull High : Enable RTD2168 embedded EDID.

Mode Configure Table(Power On Latch)

to set PIN22 pull low, PIN23 pull high for Rom mode.





Elitegroup Computer Systems			
Title: DP to VGA(RTD2168)			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
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VGA

Part:BLM18BB220SN
P/N:16-105-220130 FB.22 OHM.25%...SMD 0402.BLM15BB220SN1D.300mA...HF.LEAD-FREE.MURATA
P/N:16-105-220140 FB.22 OHM.25%...SMD 0402.FCM1005MF-220T03.300mA...HF.LEAD-FREE.TAI-TECH

13 VGA_RED
13 VGA_GREEN
13 VGA_BLUE

FB1 FB2 FB3 FB-22-04-B

VGA_RED_CONN
VGA_GREEN_CONN
VGA_BLUE_CONN

R159 R158 R157 75-1-04
C101 C100 C99 2P-04
C70 C69 C68 2P-04
C76 C75 C74 10P-04-O

GND

Level shifter,default 0 ohm

+VGA_VCC

SC6 SC7 1U-16VX7-04-X-O

13 VGA_HSYNC → VGA_HSYNC → SU4 74LVC32-5-S-X-O → VGA_HSYNC_5V
13 VGA_VSYNC → VGA_VSYNC → SU3 74LVC32-5-S-X-O → VGA_VSYNC_5V

SR6 SR5 0-04-X

SC4 SC3 10P-04-X

VGA_HSYNC_5V → SR3 36-1-04-X → VGA_HSYNC_CNN
VGA_VSYNC_5V → SR2 36-1-04-X → VGA_VSYNC_CNN

If build in Internal DVI Con,
that can use the circuit to protect reverse voltage together.

+12V
C148 .1U-25VX5-04-O
R175 10K-04
+DVI_VGA_VCC_G
+VCC
Q20 P8503BMG-S
耐壓:8V
F4 FUSE-1.1A-18
+DVI_VGA_VCC
R194 0-08-O

U9 AZC099-04S-R7G-S-O
VGA_BLUE_CONN
VGA_RED_CONN
VGA_GREEN_CONN
C29 .1U-16VY5-04-O

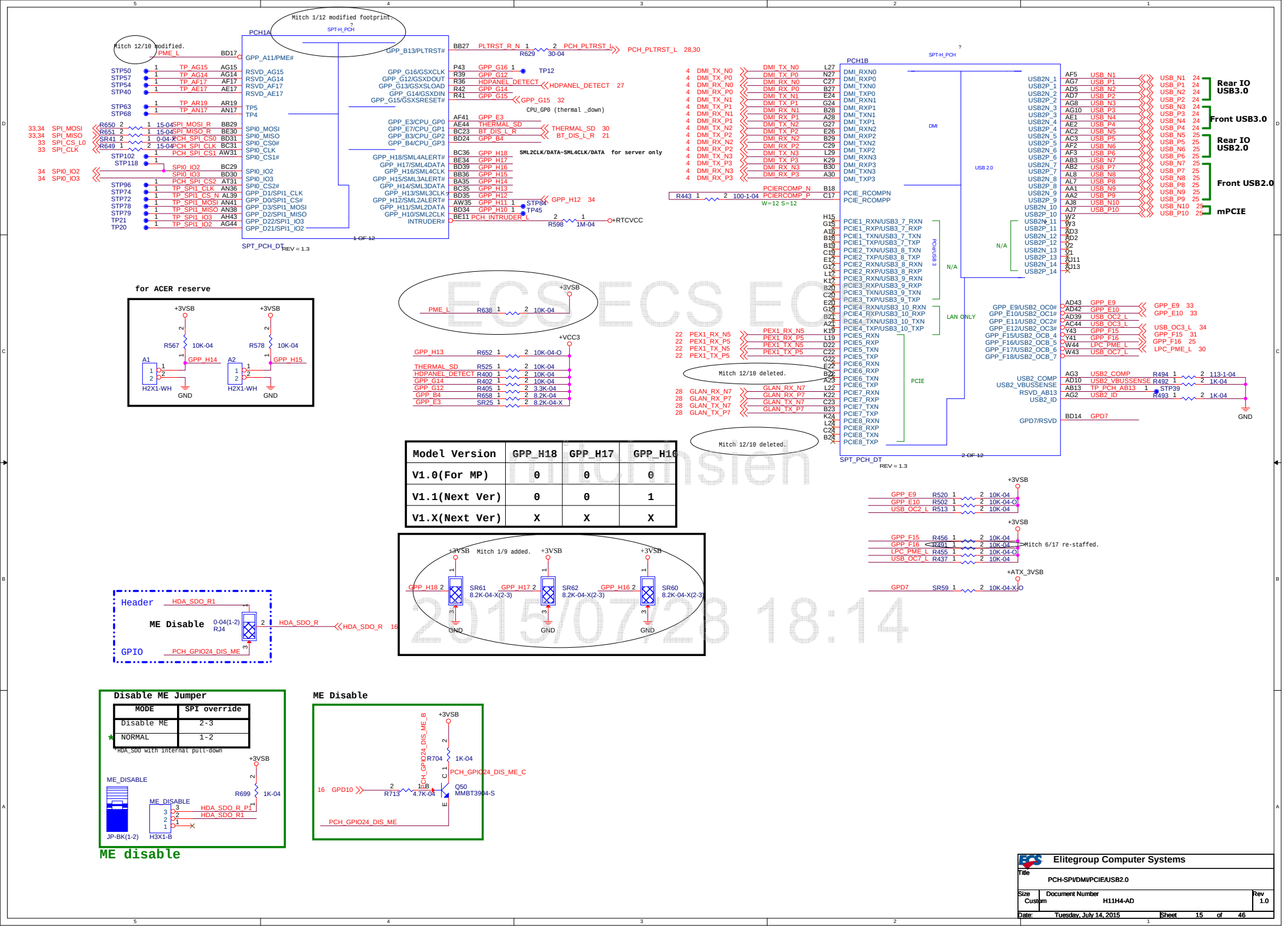
SR1 SR4 2.2K-04-X
13 VGA_DDCCLK_CNN → VGA_DDCCLK_CNN → SC2 100P-04-X-O
13 VGA_DDCSDA_CNN → VGA_DDCSDA_CNN → SC5 100P-04-X-O

SU2 AZC099-04S-R7G-S-X-O
VGA_DDCCLK_CNN
VGA_DDCSDA_CNN
VGA_HSYNC_CNN
VGA_VSYNC_CNN
SC1 .1U-16VY5-04-X-O

VGA CONN-15P3R-VGA
VGA_RED_CONN
VGA_GREEN_CONN
VGA_BLUE_CONN
VGA_DDCSDA_CNN
VGA_HSYNC_CNN
VGA_VSYNC_CNN
VGA_DDCCLK_CNN
G1 G2

+DVI_VGA_VCC
R210 0-08
C174 .1U-16VX7-04
C175 1U-16VX7-06-O

Elitegroup Computer Systems		
Title: VGA		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 28, 2015	Sheet 14 of 46	


Mitch 1/12 modified footprint.
Mitch 12/10 modified.
PCH1A
SPT-H_PCH
PME_L
GPP_A11/PME#
TP_AG15
TP_AG14
TP_AF17
TP_AE17
TP_AR19
TP_AN17
RSVD_AG15
RSVD_AG14
RSVD_AF17
RSVD_AE17
TP5
TP4
SPI_MOSI_R
SPI_MISO_R
SPI_CS0#
SPI_CLK
SPI_CS1#
SPI0_MOSI
SPI0_MISO
SPI0_CS0#
SPI0_CLK
SPI0_CS1#
SPI0_IO2
SPI0_IO3
PCH_SPI_CS2
TP_SPI1_CLK
TP_SPI1_CS_N
TP_SPI1_MOSI
TP_SPI1_MISO
TP_SPI1_IO3
TP_SPI1_IO2
SPI0_CS2#
GPP_D1/SPI1_CLK
GPP_D0/SPI1_CS#
GPP_D3/SPI1_MOSI
GPP_D2/SPI1_MISO
GPP_D22/SPI1_IO3
GPP_D21/SPI1_IO2
SPT_PCH_DT
REV = 1.3
1 OF 12
GPP_B13/PLTRST#
PLTRST_R_N
PCH_PLTRST_L
GPP_G16/GSXCLK
GPP_G12/GSXDOUT
GPP_G13/GSXSLOAD
GPP_G14/GSXDIN
GPP_G15/GSXSRESET#
GPP_G16
GPP_G12
HDPANEL_DETECT
GPP_G14
GPP_G15
CPU_GP0 (thermal _down)
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
GPP_E3
THERMAL_SD
BT_DIS_L_R
GPP_B4
SML2CLK/DATA~SML4CLK/DATA for server only
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML2ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
INTRUDER#
GPP_H18
GPP_H17
GPP_H16
GPP_H15
GPP_H14
GPP_H13
GPP_H12
GPP_H11
GPP_H10
PCH_INTRUDER_L
STP84
TP45
+RTCVCC
for ACER reserve
+3VSB
R567
10K-04
R578
GPP_H14
GPP_H15
H2X1-WH
GND
PME_L
R638
GPP_H13
R652
THERMAL_SD
R525
HDPANEL_DETECT
R400
GPP_G14
R402
GPP_G12
R405
GPP_B4
R658
GPP_E3
SR25
10K-04-O
10K-04
3.3K-04
8.2K-04
8.2K-04-X
+VCC3
PCH1B
SPT-H_PCH
DMI_TX_N0
DMI_TX_P0
DMI_RX_N0
DMI_RX_P0
DMI_TX_N1
DMI_TX_P1
DMI_RX_N1
DMI_RX_P1
DMI_TX_N2
DMI_TX_P2
DMI_RX_N2
DMI_RX_P2
DMI_TX_N3
DMI_TX_P3
DMI_RX_N3
DMI_RX_P3
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI
USB 2.0
PCIERCOMP_N
PCIERCOMP_P
PCIE_RCOMPN
PCIE_RCOMPP
R443
100-1-04
W=12 S=12
PCIE1_RXN/USB3_7_RXN
PCIE1_RXP/USB3_7_RXP
PCIE1_TXN/USB3_7_TXN
PCIE1_TXP/USB3_7_TXP
PCIE2_TXN/USB3_8_TXN
PCIE2_TXP/USB3_8_TXP
PCIE2_RXN/USB3_8_RXN
PCIE2_RXP/USB3_8_RXP
PCIE3_RXN/USB3_9_RXN
PCIE3_RXP/USB3_9_RXP
PCIE3_TXN/USB3_9_TXN
PCIE3_TXP/USB3_9_TXP
PCIE4_RXN/USB3_10_RXN
PCIE4_RXP/USB3_10_RXP
PCIE4_TXN/USB3_10_TXN
PCIE4_TXP/USB3_10_TXP
PCIE5_RXN
PCIE5_RXP
PCIE5_TXN
PCIE5_TXP
PCIE6_RXN
PCIE6_RXP
PCIE6_TXN
PCIE6_TXP
PCIE7_RXN
PCIE7_RXP
PCIE7_TXN
PCIE7_TXP
PCIE8_RXN
PCIE8_RXP
PCIE8_TXN
PCIE8_TXP
PCIE/USB3
PCIE
LAN ONLY
N/A
PEX1_RX_N5
PEX1_RX_P5
PEX1_TX_N5
PEX1_TX_P5
Mitch 12/10 deleted.
GLAN_RX_N7
GLAN_RX_P7
GLAN_TX_N7
GLAN_TX_P7
Mitch 12/10 deleted.
USB2_N_1
USB2_P_1
USB2_N_2
USB2_P_2
USB2_N_3
USB2_P_3
USB2_N_4
USB2_P_4
USB2_N_5
USB2_P_5
USB2_N_6
USB2_P_6
USB2_N_7
USB2_P_7
USB2_N_8
USB2_P_8
USB2_N_9
USB2_P_9
USB2_N_10
USB2_P_10
USB2_N_11
USB2_P_11
USB2_N_12
USB2_P_12
USB2_N_13
USB2_P_13
USB2_N_14
USB2_P_14
USB_N1
USB_P1
USB_N2
USB_P2
USB_N3
USB_P3
USB_N4
USB_P4
USB_N5
USB_P5
USB_N6
USB_P6
USB_N7
USB_P7
USB_N8
USB_P8
USB_N9
USB_P9
USB_N10
USB_P10
Rear IO USB3.0
Front USB3.0
Rear IO USB2.0
Front USB2.0
mPCIE
GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_F15/USB2_OCB_4
GPP_F16/USB2_OCB_5
GPP_F17/USB2_OCB_6
GPP_F18/USB2_OCB_7
GPP_E9
GPP_E10
GPP_F15
GPP_F16
USB_OC3_L
LPC_PME_L
USB_OC7_L
USB2_COMP
USB2_VBUSSENSE
RSVD_AB13
USB2_ID
GPD7/RSVD
GPD7
2 OF 12
SPT_PCH_DT
REV = 1.3
+3VSB
GPP_E9
GPP_E10
USB_OC2_L
R520
R502
R513
10K-04
10K-04-O
+3VSB
GPP_F15
GPP_F16
LPC_PME_L
USB_OC7_L
R456
R491
R455
R437
Mitch 6/17 re-staffed.
+ATX_3VSB
GPD7
SR59
10K-04-X-O
Model Version | GPP_H18 | GPP_H17 | GPP_H16
V1.0(For MP) | 0 | 0 | 0
V1.1(Next Ver) | 0 | 0 | 1
V1.X(Next Ver) | X | X | X
Mitch 1/9 added.
+3VSB
GPP_H18
GPP_H17
GPP_H16
SR61
SR62
SR60
8.2K-04-X(2-3)
GND
Header
HDA_SDO_R1
ME Disable
0-04(1-2)
RJ4
HDA_SDO_R
GPIO
PCH_GPIO24_DIS_ME
Disable ME Jumper
MODE
SPI override
Disable ME
2-3
NORMAL
1-2
*HDA_SDO with internal pull-down
ME_DISABLE
R699
1K-04
JP-BK(1-2)
H3X1-B
HDA_SDO_R_P1
HDA_SDO_R1
ME Disable
PCH_GPIO24_DIS_ME_B
R704
1K-04
PCH_GPIO24_DIS_ME_C
16 GPD10
R713
4.7K-04
Q50
MMBT3904-S
PCH_GPIO24_DIS_ME
ME disable
Elitegroup Computer Systems
PCH-SPI/DMI/PCIE/USB2.0
Size Custom
Document Number H11H4-AD
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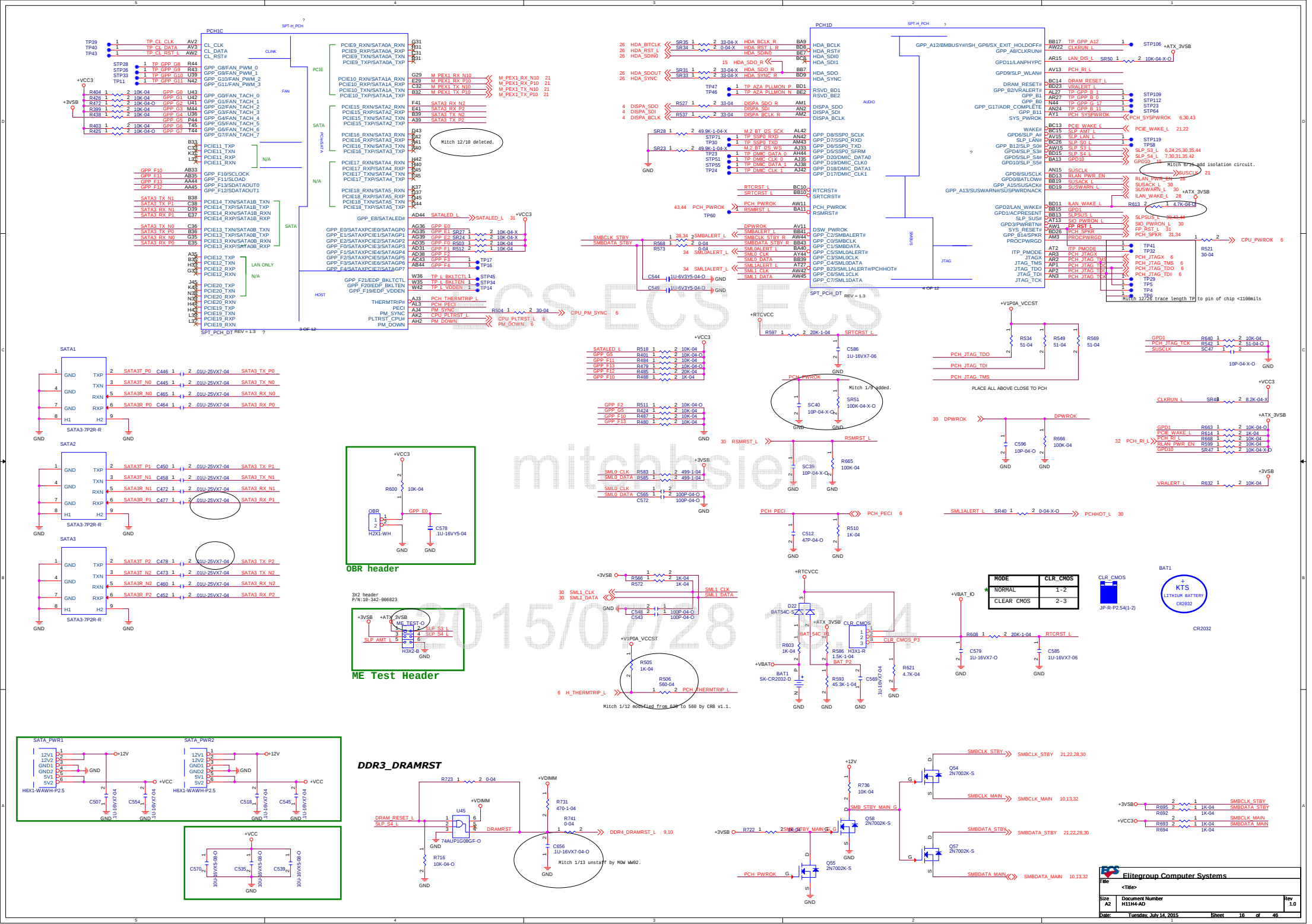
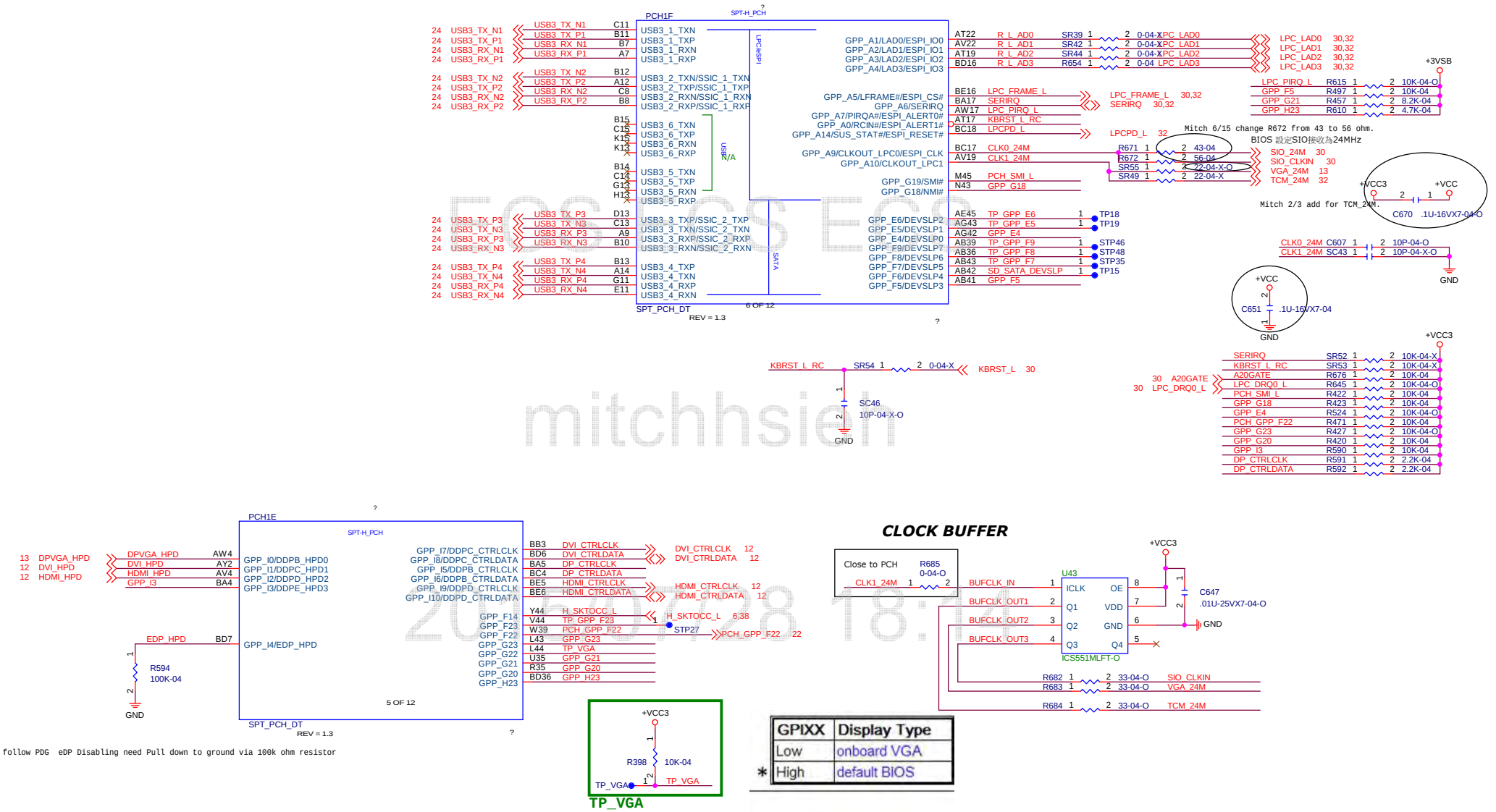

PCH1C
PCH1D
SATA1
SATA2
SATA3
SATA_PWR1
SATA_PWR2
OBR header
ME Test Header
DDR3_DRAMRST
MODE
CLR_CMOS
NORMAL
1-2
CLEAR CMOS
2-3
Elitegroup Computer Systems
H11H4-AD
Tuesday, July 14, 2015
mitchsien
2015/07/28 18:14



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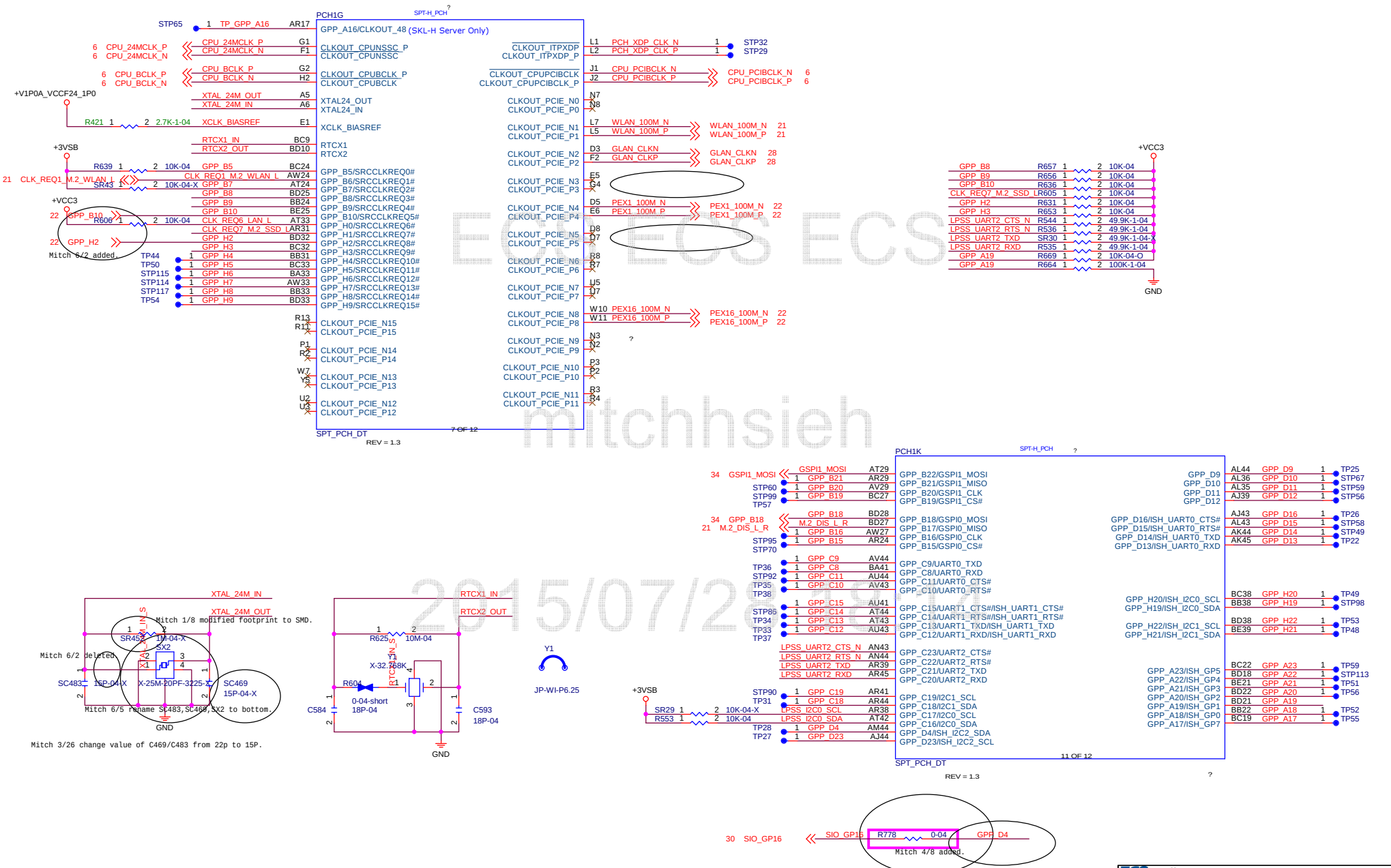
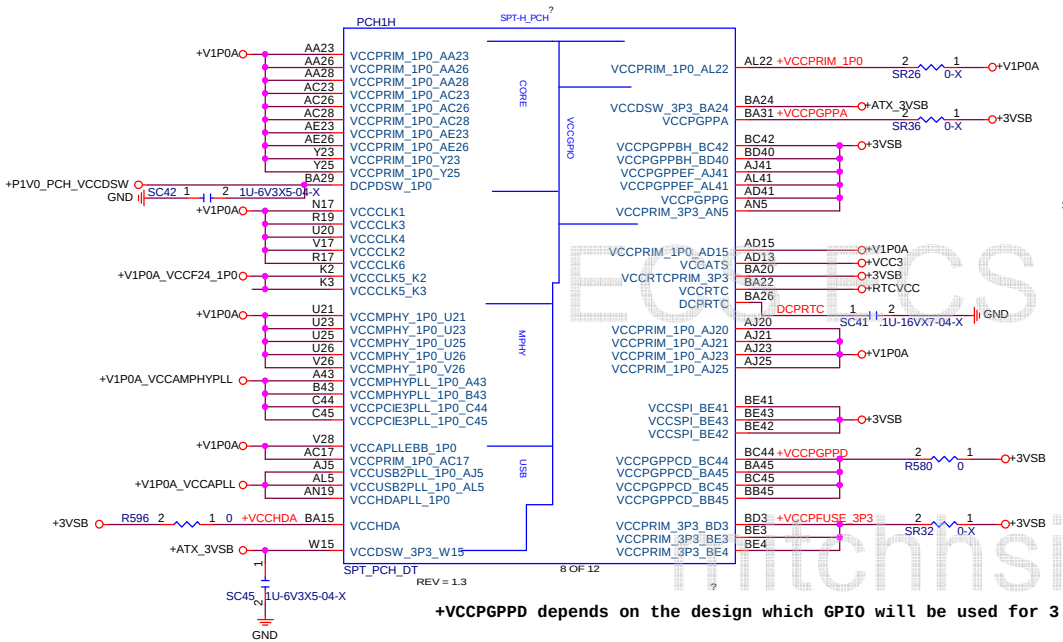
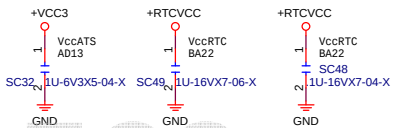
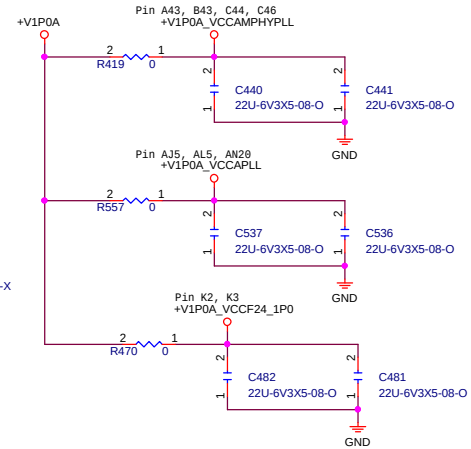
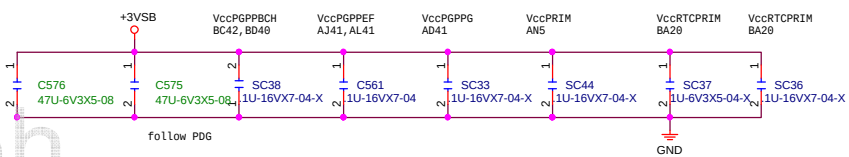
Size	Custom
Document Number	H11H4-AD
Rev	1.0
Date:	Tuesday, July 14, 2015
Sheet	17 of 46

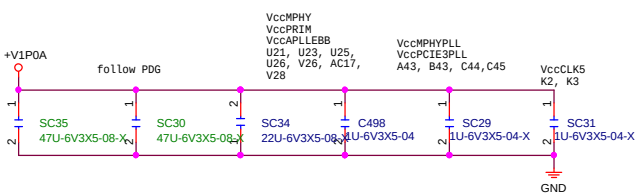

PCH1G
SPT-H_PCH
GPP_A16/CLKOUT_48 (SKL-H Server Only)
SPT_PCH_DT
REV = 1.3
7 OF 12
PCH1K
11 OF 12
Mitch 1/8 modified footprint to SMD.
Mitch 6/2 deleted.
Mitch 6/5 rename SC483,SC469,SX2 to bottom.
Mitch 3/26 change value of C469/C483 from 22p to 15P.
Mitch 6/2 added.
Mitch 4/8 added.
JP-WI-P6.25
Elitegroup Computer Systems
H11H4-AD
Tuesday, July 28, 2015



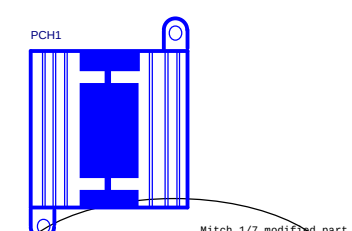








+VCCPGPPD depends on the design which GPIO will be used for 3.3V or 1.8V.



Mitch 1/7 modified part.

PCH heatsink (T/U phase)
P/N:20-120-012520
20-120-013505
20-120-013678

Elitegroup Computer Systems			
Title: PCH-PWR			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
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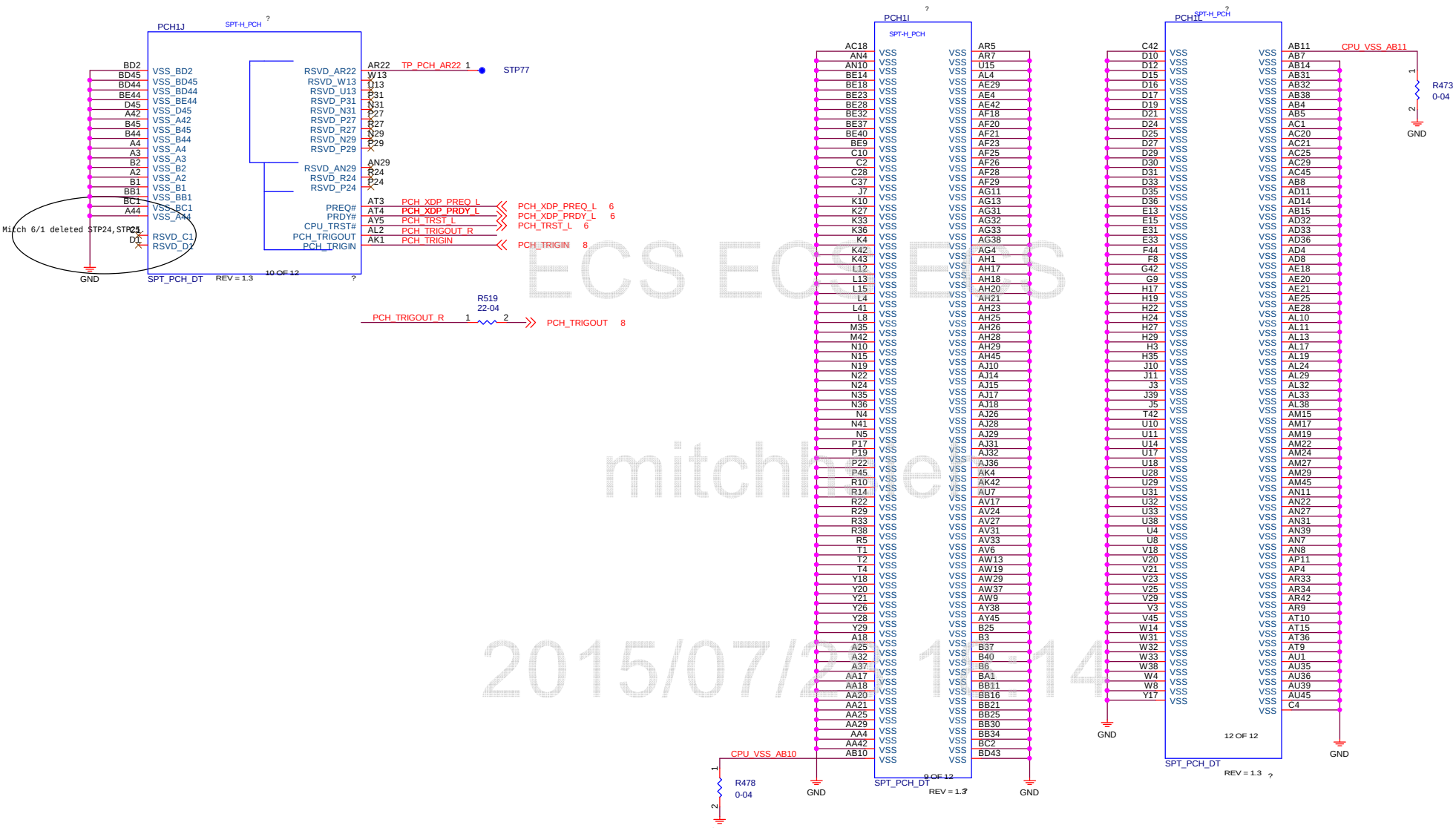

Elitegroup Computer Systems		
Title: PCH-GND		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
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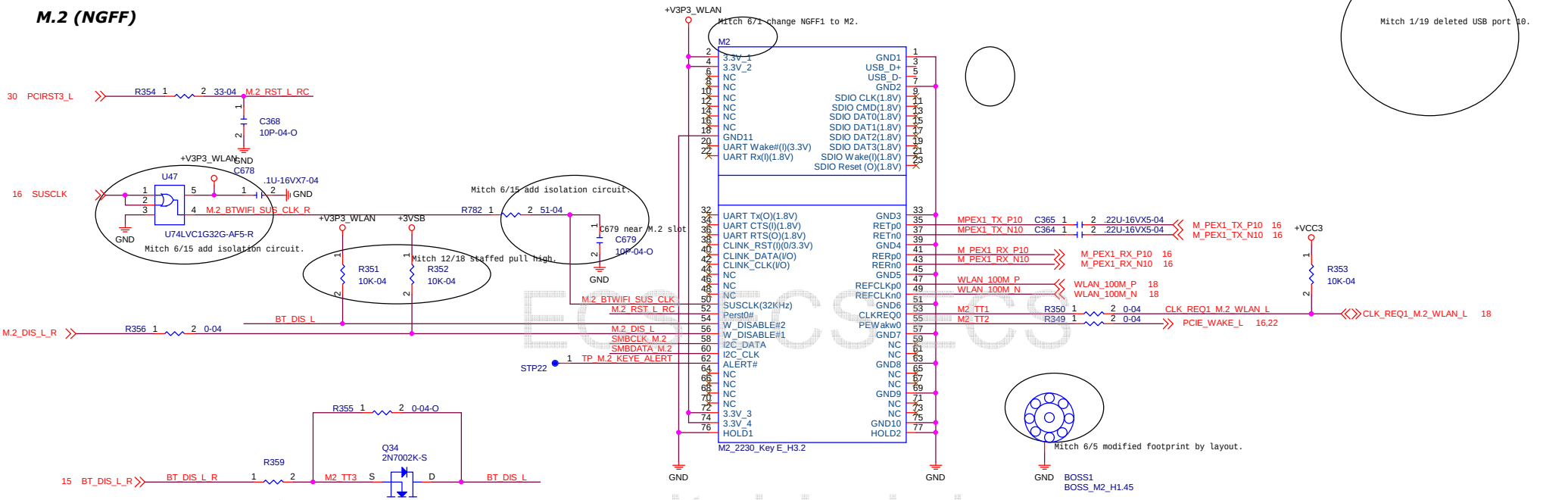
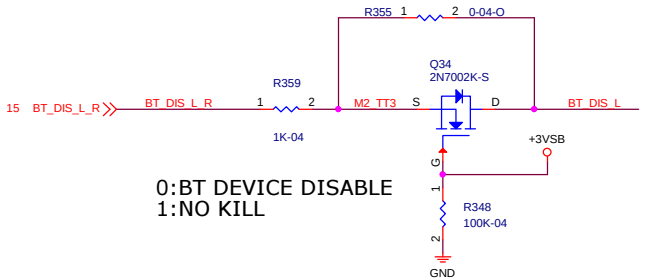
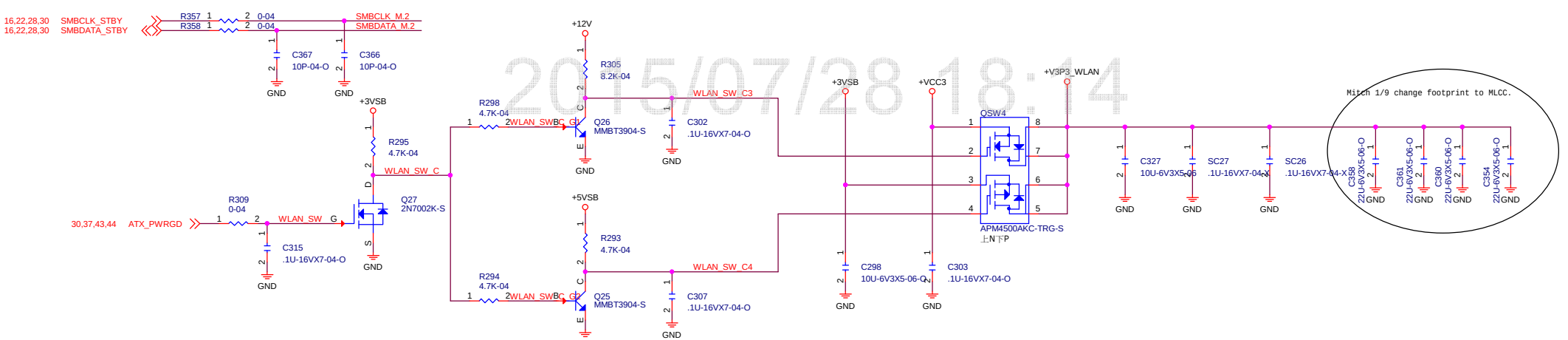
M.2 (NGFF)





Key	Power Rail	Voltage Tolerance	Current Consumption Limit Peak mA Max Avg @ 100 µs	Current Consumption Limit Normal mA Max Avg @ 1 s
E	3.3 V	± 5%	2000	



	ATX_PWRGD	+V3P3_WLAN
S0	1	+VCC3
S3/S4/S5	0	+3VSB

Title	M.2 Slot
Size	Custom
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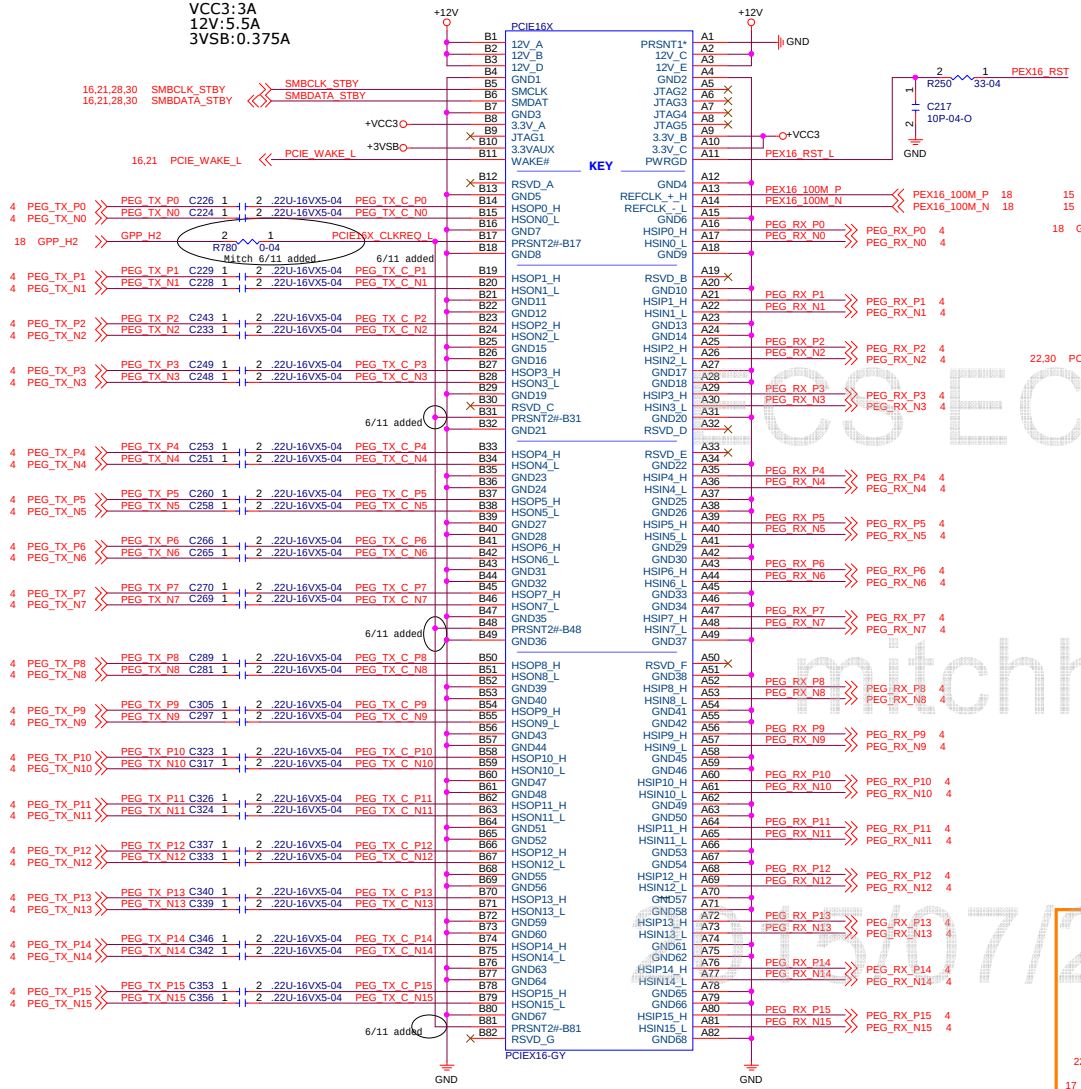
Elitegroup Computer Systems

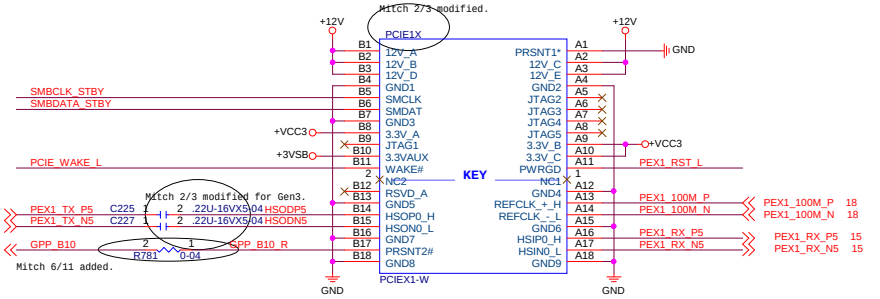
one slot support dual lan card,reserve

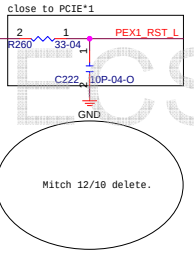
PCI-E X16 SLOT

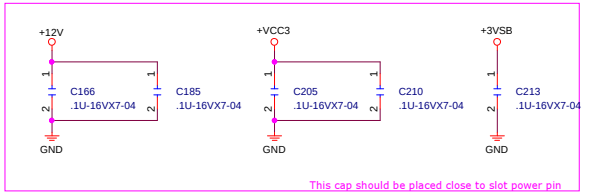
PCI-E SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A



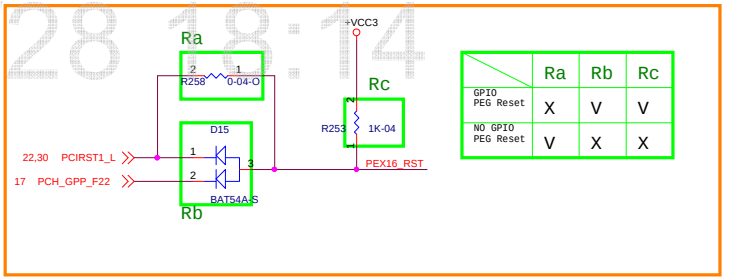
PCI-E X1 SLOT1

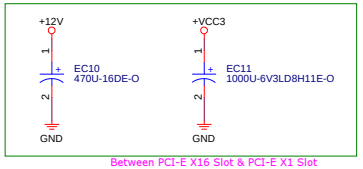


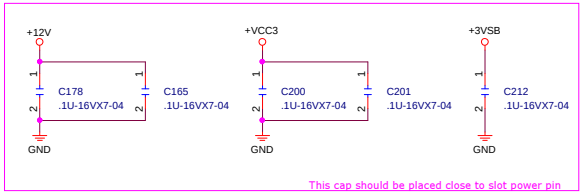




PCI-E X1 SLOT2







Elitegroup Computer Systems	
Title	PCI-E X16/X1
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ECS ECS ECS

mitchhsieh

2015/07/28 18:14

Title: HDMI		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
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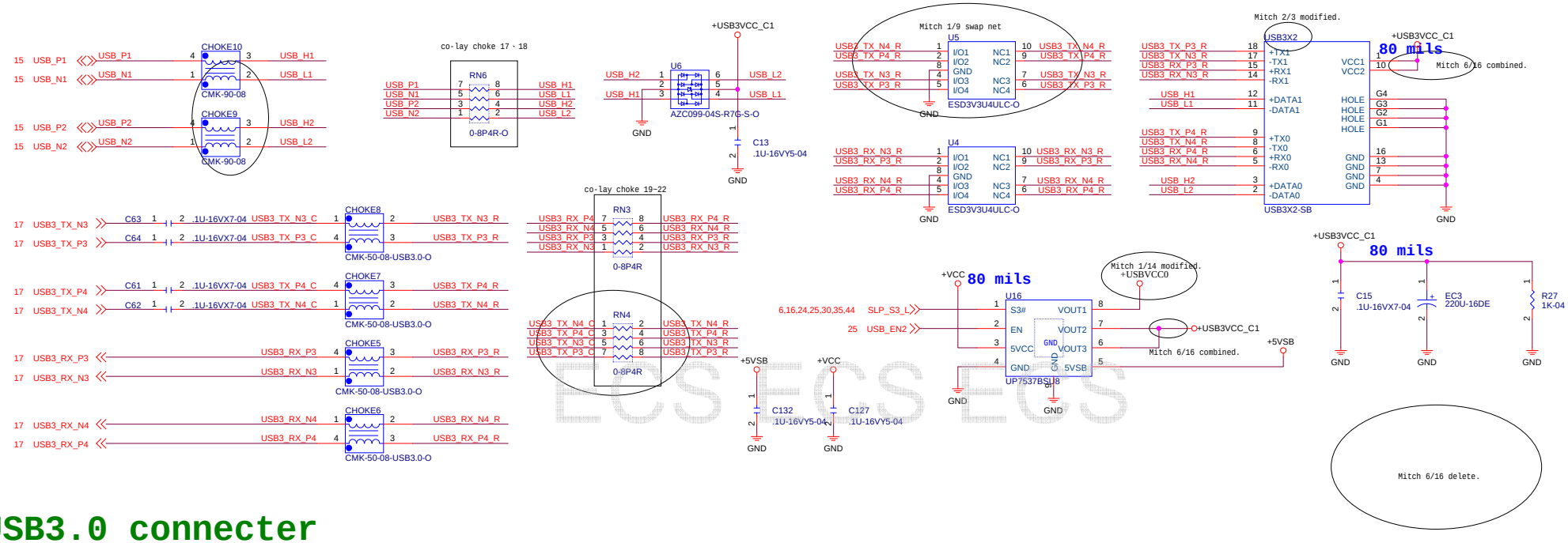
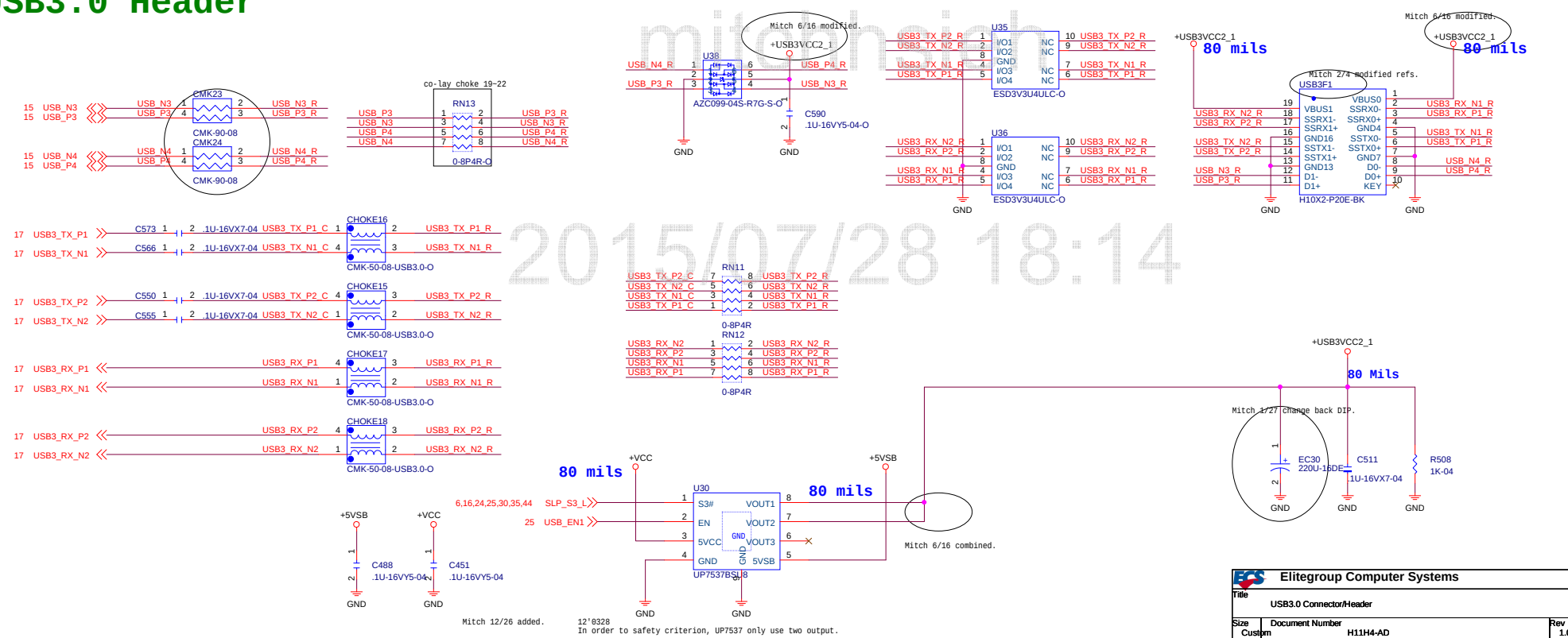


USB3.0 connecter

USB3.0 Header



Elitegroup Computer Systems		
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Size: Custom	Document Number: H11H4-AD	Rev: 1.0
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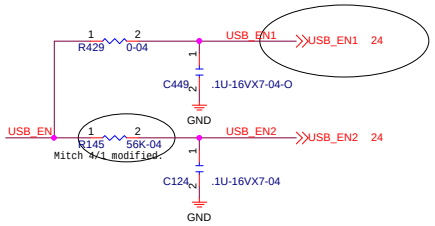
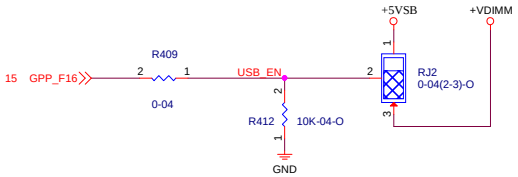
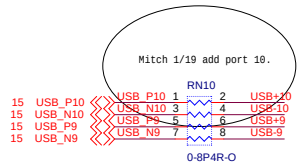
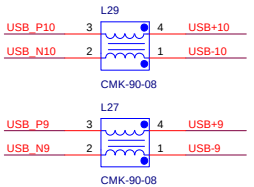
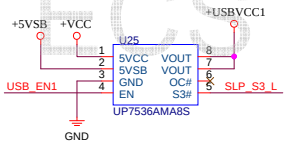


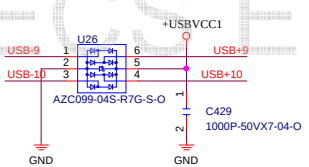


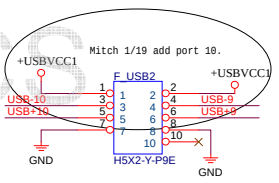
	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

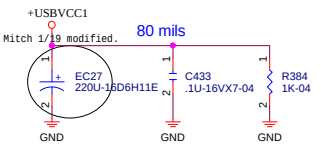


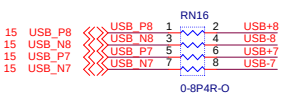


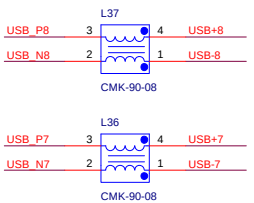


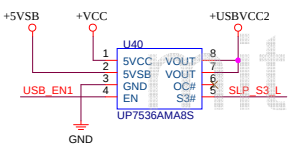


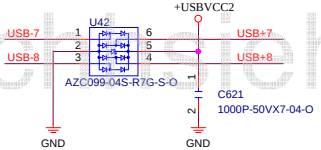


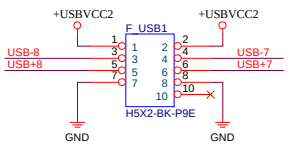


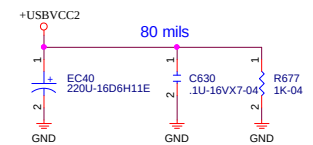






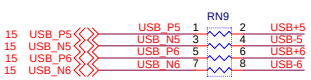


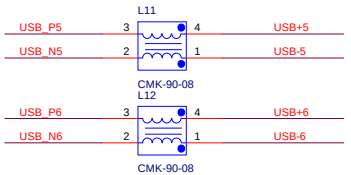


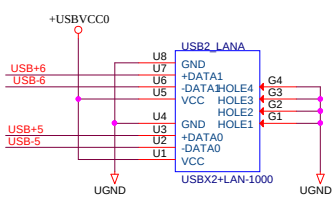


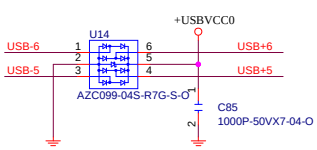
USB2.0 header

USB2.0 connecter

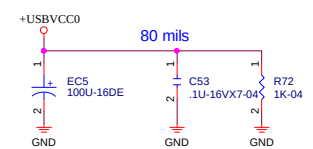




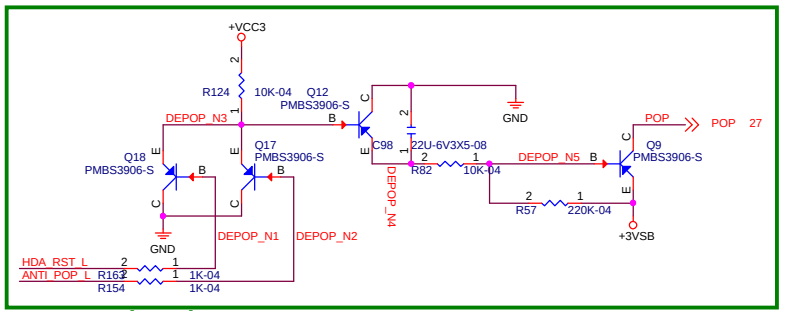




Lan + USB2.0

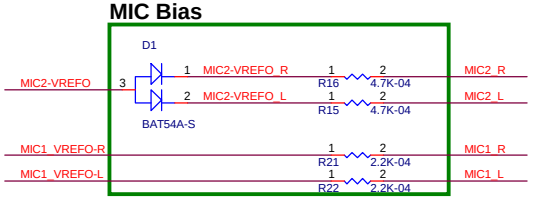


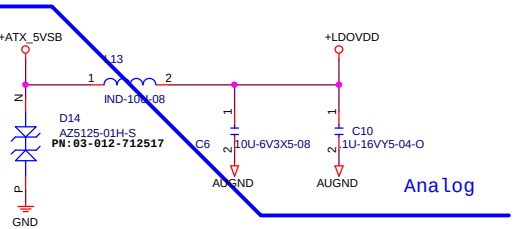
Elitegroup Computer Systems			
Title: USB2.0 Connector/Header			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 25 of 46		



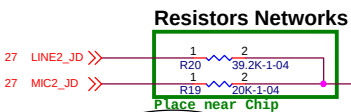
De-pop circuit

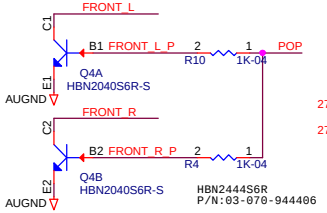
MIC Bias

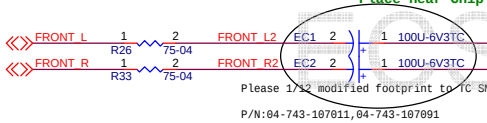


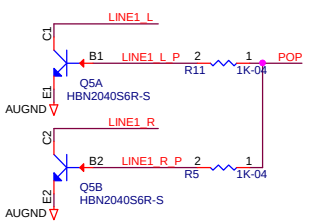


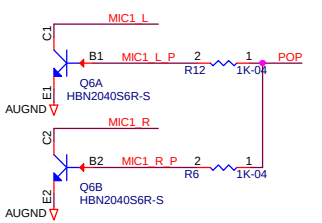
Resistors Networks

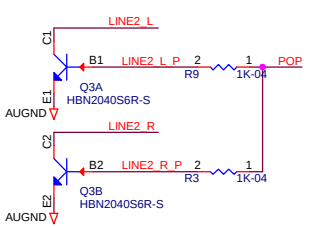


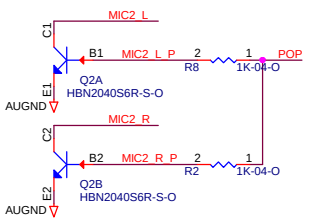


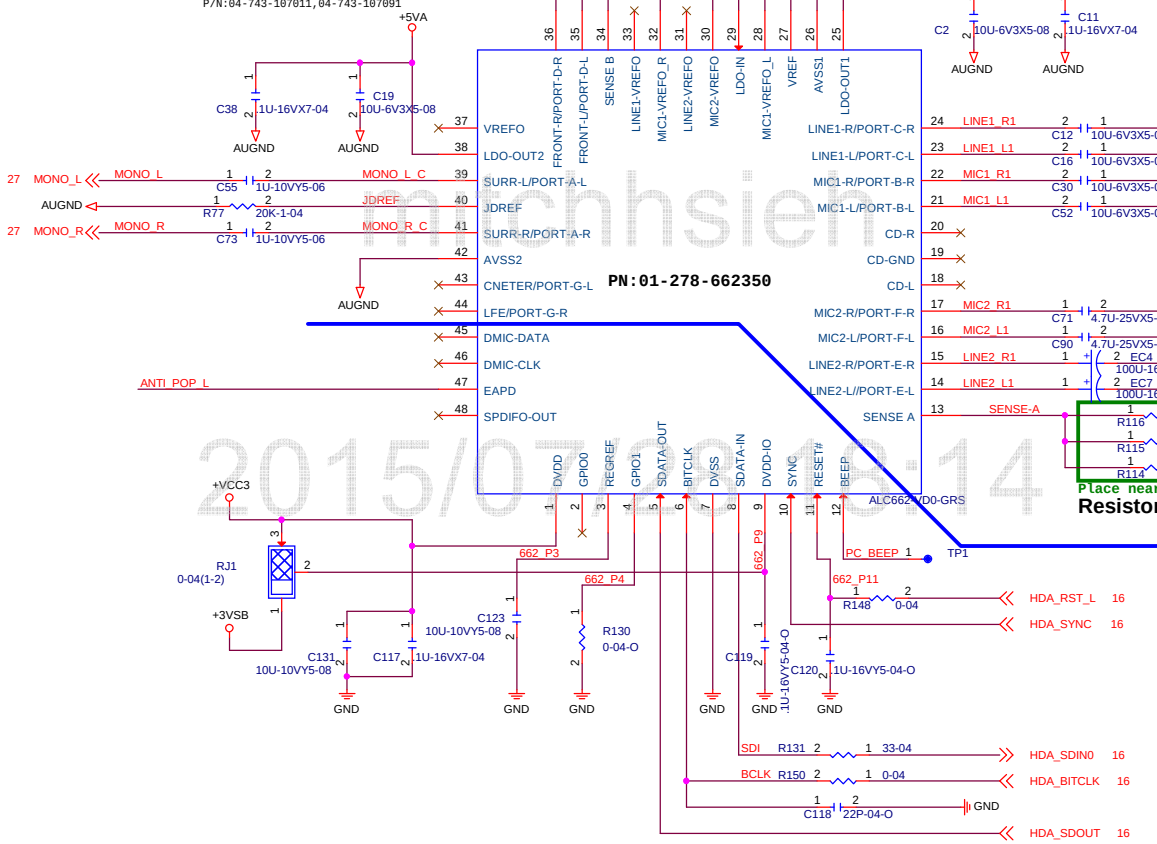


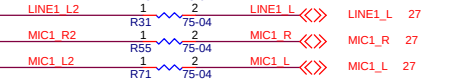


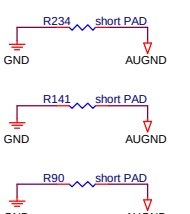












Elitegroup Computer Systems			
Title: Audio ALC662-VD			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
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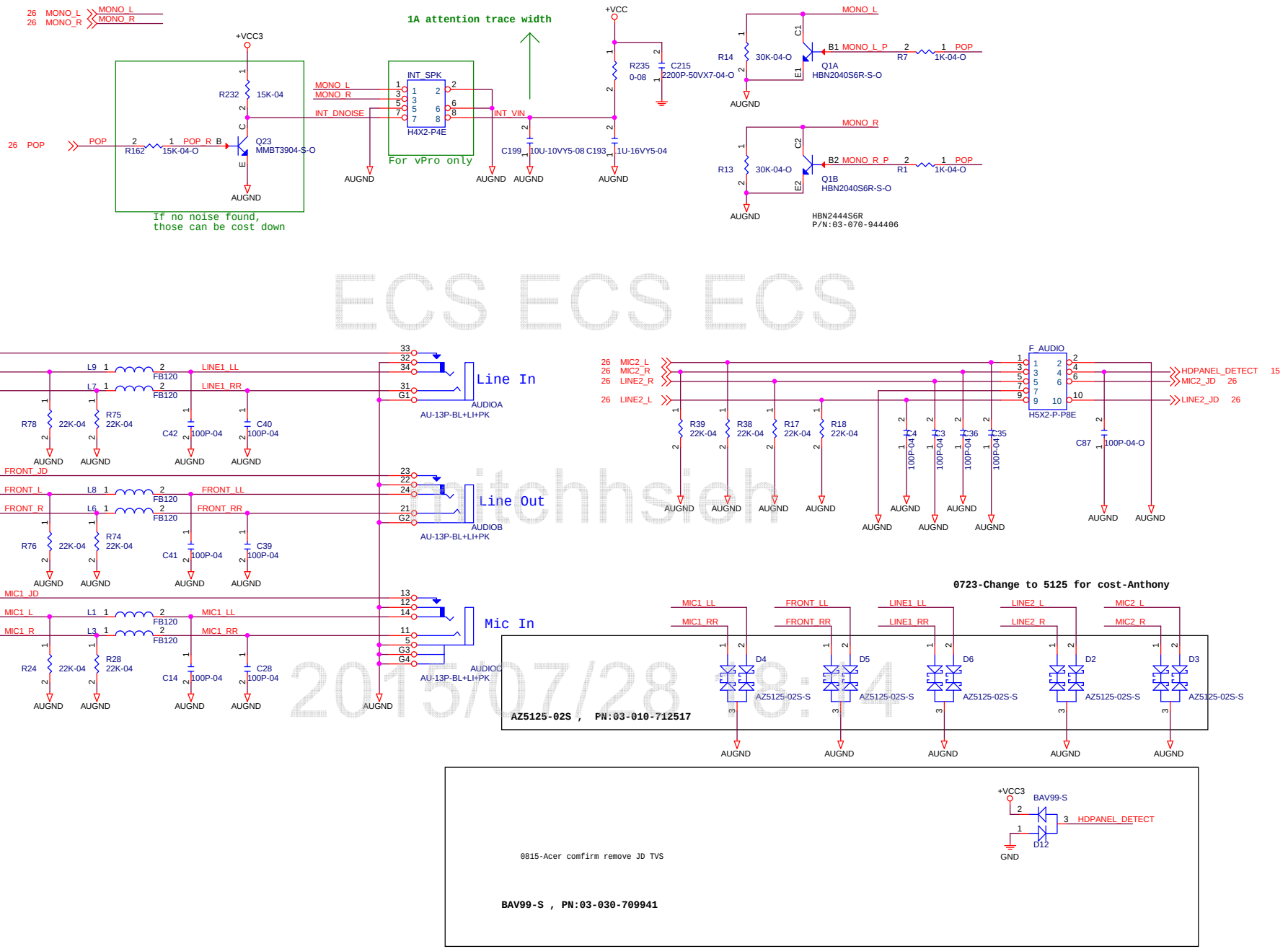

Elitegroup Computer Systems		
Title: Audio Jack/Header		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
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+V_3P3_LAN

177mA

R176 0-08-O

Q19 PA002FMG-S

C138 .1U-16VX7-04 +V_3P3_LAN_G1

R160 150K-1-04

GND

For RTL8111E

* Bellow CAP are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

+VDD33

70mA

SC8 SC10 SC11 SC14 SC9 SC13 .1U-16VX7-04-X

R239 0-06-short

AVDD33_REG

107mA

C207 4.7U-6V3X5-06

C202 .1U-16VX7-04

Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)

08-412-475171
INDUCTOR.4.7uH.20%.800mA.....SMD.2.9*2.5*2.1mm.SWF2520CF-4R7M-M-M80...HF.LEAD-FREE(RoHS).TAI-TECH

L18 IND-4.7U-SCD0403

REGOUT

REGOUT_R

R224 0-06-short

Pls. refer to 8111E Layout Guide for Lx, Cout1, Cout2 selection criteria.

C208 4.7U-6V3X5-06

C206 .1U-16VX7-04

Remove For Disable Switch Regulator (Accept External 1.05V Power Supply)

For RTL8111E

* Bellow CAPs are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

+VDD10

1.05V

C173 C147 C145 C149 C186 C204 C146 .1U-16VX7-04

R216 0-06-short

* Bellow CAPs are for EVD1D10 pins--21.

+EVDD10

1.05V

C188 1U-6V3X5-04

SC12 .1U-16VX7-04-X

R208 2.49k-1-04 RSET

R684 value should be 2.49K (1%) for all application.

U18

RTL8111E-VC-CG

More Detail Layout
Pls. Refer to Layout Guide

R259 0-04

R677 For Enable Switch Regulator.
R679 For Disable Switch Regulator.

R246 0-04-O

+VCC3

R237 1K-04

R227 15K-04

Mitch 1/13 modified recovery.

+VDD33

CLKREQB R206 10K-04

10K ohm close to Host side

Acer/FDR request:
1:default use e-FUSE;
2:only reserve External EEPROM;

e-Fuse pull low

R207 10K-04-O

Pull high in PCH

X_SMB_DATA R195 1K-04-O

X_SMB_CLK R196 1K-04-O

X_SMBALERT R214 1K-04

GND

+VDD33

EEPROM

EECS_SCL

LED1/EESK

EEDI_SDA

LED3/EEDO

CS SK DI DO VCC DC ORG GND

M93C66WMN6-O

C214 .1U-16VX7-04-O

93C46 P/N:01-530-046157
93C66 P/N:01-530-066020

Y3 X-25M

XTAL2

XTAL1

C169 33P-04

C189 33P-04

Mitch 3/26 change value of C169/C189 from 27p to 33P.

EECS_SCL R265 10K-04

EEDI_SDA R264 10K-04

GND

+ATX_3VSB R245 10K-04 WAKE_L

Stuff R
when use RTL LAN and support G3~S5 WOL

16 ILAN_WAKE_L ILAN_WAKE_L R238 0-04 WAKE_L

LED0 P2 Short PAD LAN_LED2_100M

EEDI_SDA R247 0-04-O Short PAD

LED1/EESK P1 LAN_LED1_1G

PERSTB R236 0-04 PCH_PLTRST_L 15,30

C203 10P-04-O

18 GLAN_CLKP

18 GLAN_CLKN

X_SMB_DATA R189 0-04 SMBDATA_STBY SMBDATA_STBY 16,21,22,30

X_SMB_CLK R190 0-04 SMBCLK_STBY SMBCLK_STBY 16,21,22,30

X_SMBALERT R218 0-04-O SMBALERT_L SMBALERT_L 16,34

15 GLAN_TX_P7 C172 .1U-16VX7-04 HSIP

15 GLAN_TX_N7 C176 .1U-16VX7-04 HSIN

15 GLAN_RX_P7 C197 .1U-16VX7-04 HSOP

15 GLAN_RX_N7 C198 .1U-16VX7-04 HSON

C122 1U-16VX7-06-O

C121 .1U-16VY5-04

UGND

USB2_LANB

CENTER_TAP MXDIP_0 MXDIN_0 MXDIP_1 MXDIN_1 MXDIP_2 MXDIN_2 MXDIP_3 MXDIN_3

POWER TX1+ TX1- TX2+ TX2- TX3+ TX3- TX4+ TX4- DGND

GLED OLED GLED- GLED+ H_LAN5 H_LAN6 H_LAN7 H_LAN8 DGND

LAN_LED1_1G LAN_C_POWER LAN_UGND

USBX2+LAN-1000

R120 0-04

Close to LAN side

Mitch 1/9 modified by Vendor.

R117 R108 R97 330-04-O

R128 150-04

R92 150-04

R109 330-04

LAN_LED2_100M

LAN_LED1_1G

LED3/EEDO

+VDD33

C95 C94 C93 C88 470P-50VX7-04-O

LED3/EEDO 31

LAN Power Circuit

+ATX_3VSB

R288 10K-04

ATX_PSON_L_D

16 RLAN_PWR_EN

D16 BAT54C-7-F-S

RLAN_PWR_EN_R

R286 200K-04

R296 1K-04

30,37 ATX_PSON_L

ATX_PSON_L_R

Q24 2N7002K-S

GND

LAN Power Circuit

Vout : 3.3V
Imax : 2A
P : 3.4W

U20 APL5933CKAI-TRGS

PGOOD EN VIN VDD GND ADJ VOUT NC

+LAN_3VSB_FB

R279 12.1K-1-04

R280 3.83K-1-04

C247 220P-04-O

+V_3P3_LAN

C245 C246 C250 10U-6V3X5-08

C256 1U-16VY5-04-O

LAN_PWR_CTRL	S0~S3	S4/S5	deep sleep S4/S5	G3->S5	Clear CMOS -> S5
No WOL	High	High	Low	High	High
WOL	High	High	High	High	High

+ATX_3VSB

C262 10U-6V3X5-08

C254 .1U-16VY5-04

C261 10U-6V3X5-08-O

Near to Pin3

C255 1U-16VY5-06

Near to Pin4

Mitch 1/13 modified recovery.

R32 R46 0

MXDIP_1 MXDIN_0 MXDIP_3 MXDIN_2

U12 U13 AZC099-04S-R7G-S-O

MXDIP_0 MXDIN_1 MXDIP_2 MXDIN_3

C91 C92 .1U-16VX7-04-O

D10 D11 D8 D9 AZ5125-01H-S-O

LAN_LED2_100M_R

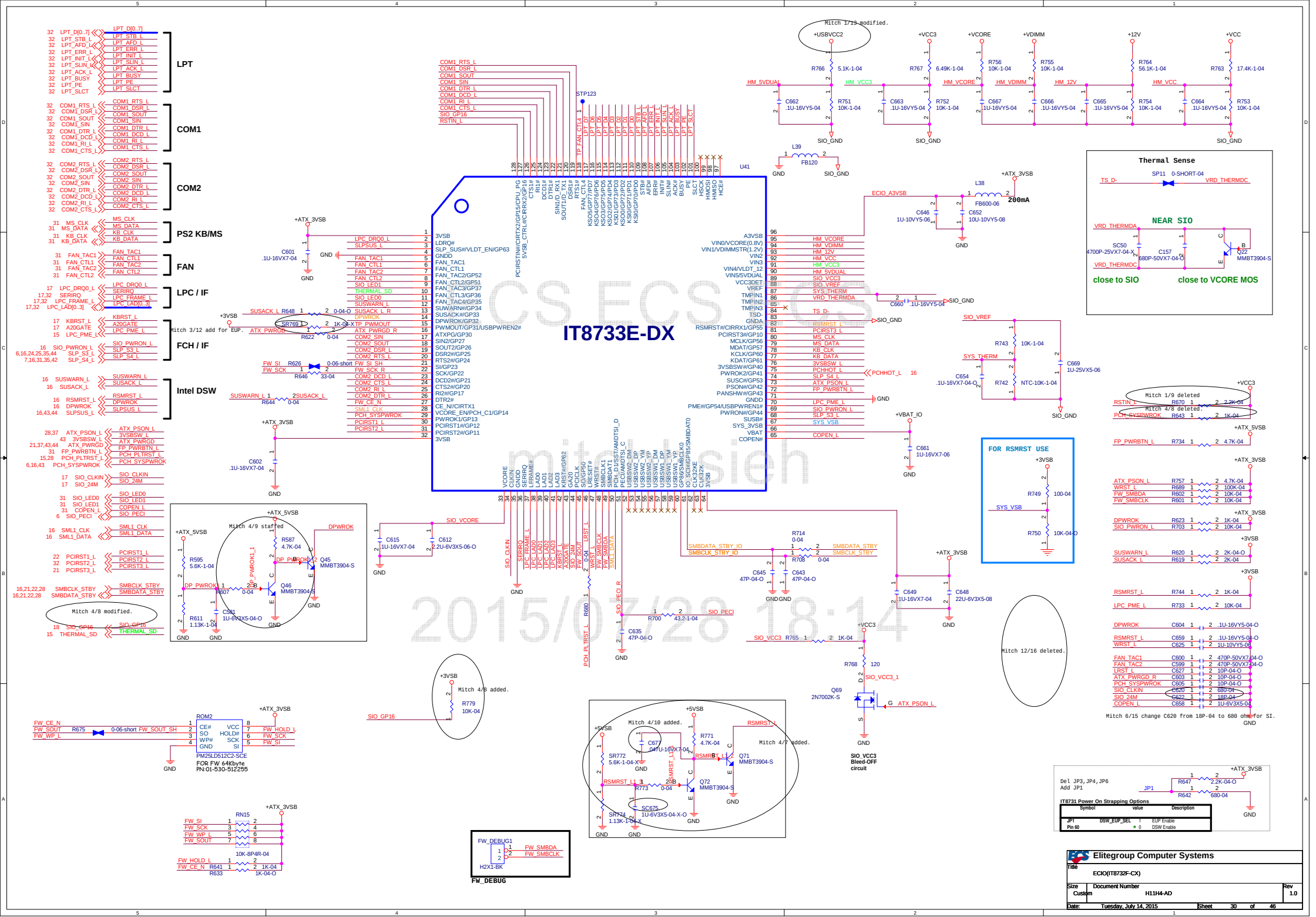
LAN_LED1_1G

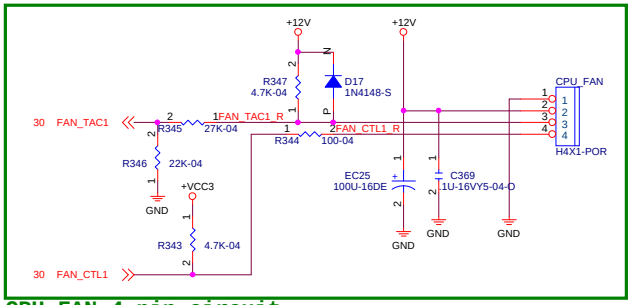
LED3/EEDO

LAN_C_POWER

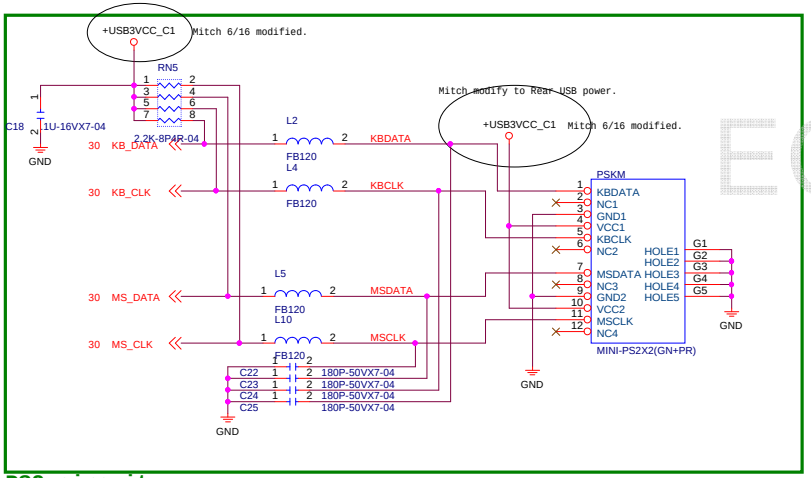
Elitegroup Computer Systems			
Title: LAN RTL8111GN			
Size: C	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 28 of 46		

Elitegroup Computer Systems		
Title: LAN I219LM		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 29 of 46	

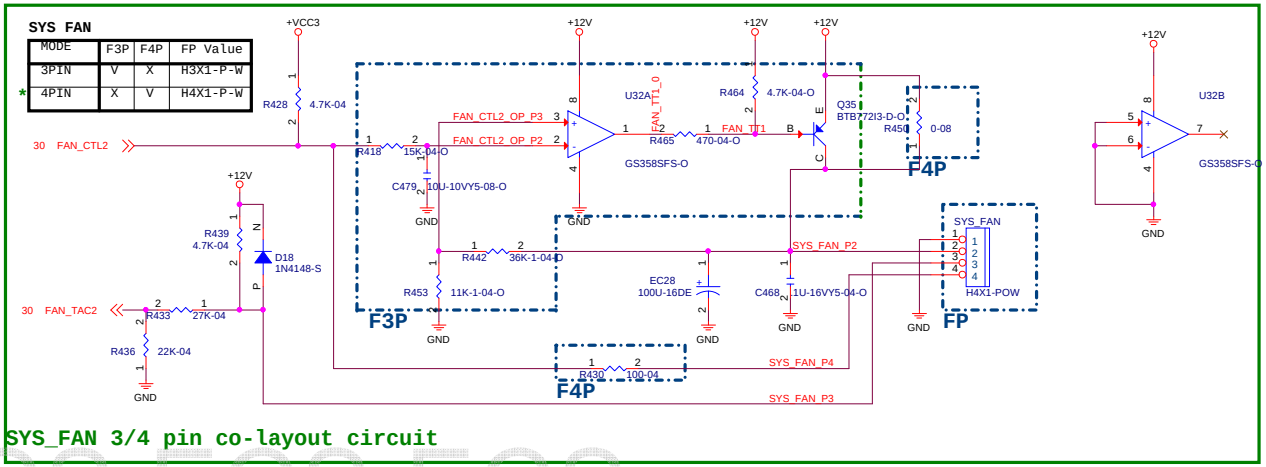

IT8733E-DX
LPT
COM1
COM2
PS2 KB/MS
FAN
LPC / IF
FCH / IF
Intel DSW
Mitch 1/19 modified.
Thermal Sense
NEAR SIO
close to SIO
close to VCORE MOS
FOR RSMRST USE
Mitch 3/12 add for EUP.
Mitch 4/9 staffed
Mitch 4/8 modified.
Mitch 4/8 added.
Mitch 4/10 added.
Mitch 4/7 added.
Mitch 1/9 deleted
Mitch 4/8 deleted.
Mitch 12/16 deleted.
Mitch 6/15 change C620 from 18P-04 to 680 ohm for SI.
FW_DEBUG
SIO_VCC3 Bleed-OFF circuit
IT8731 Power On Strapping Options
Elitegroup Computer Systems
ECIO(IT8732F-CX)
H11H4-AD
Tuesday, July 14, 2015
2015/07/28 18:14



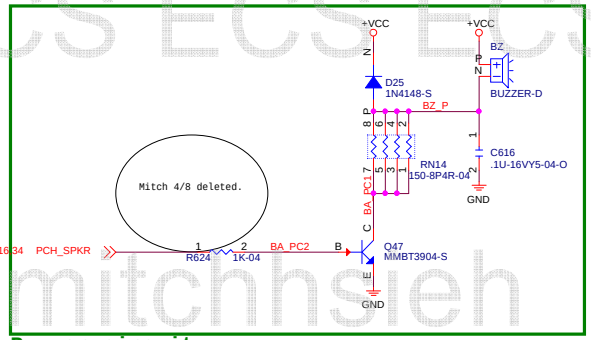
CPU_FAN 4 pin circuit



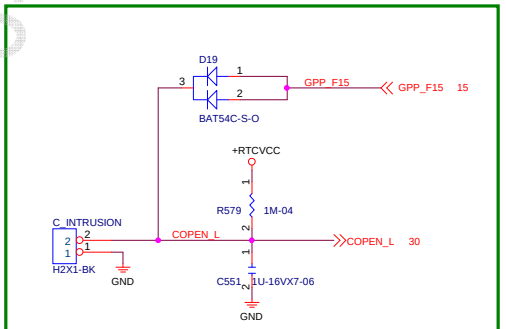
PS2 circuit



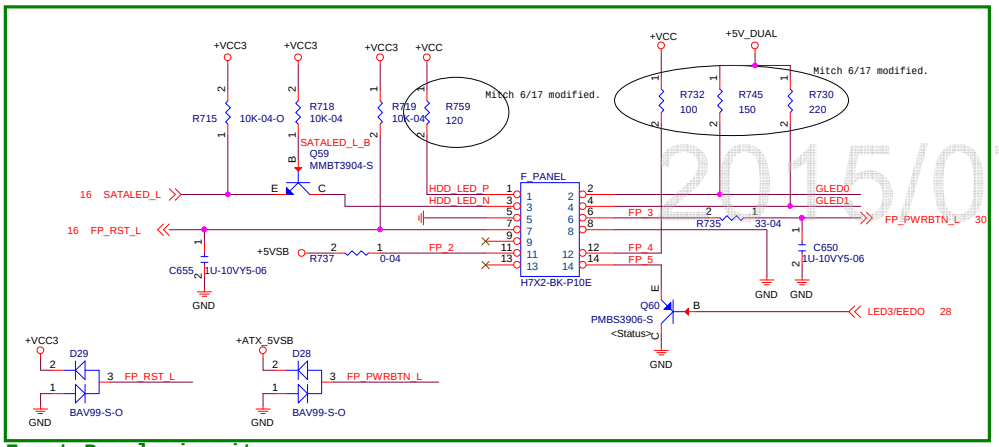
SYS_FAN 3/4 pin co-layout circuit



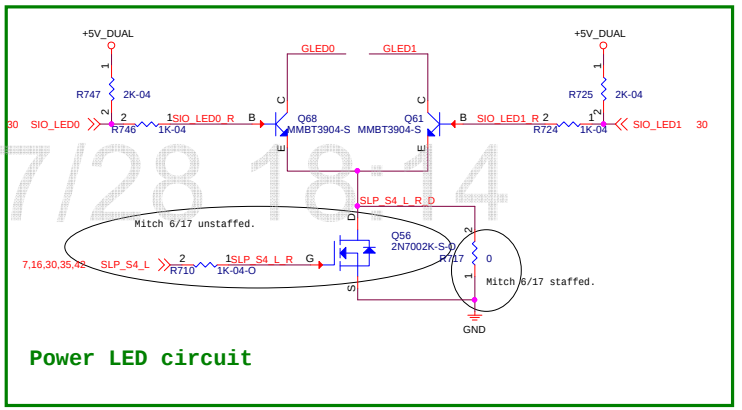
Buzzer circuit



Case open circuit

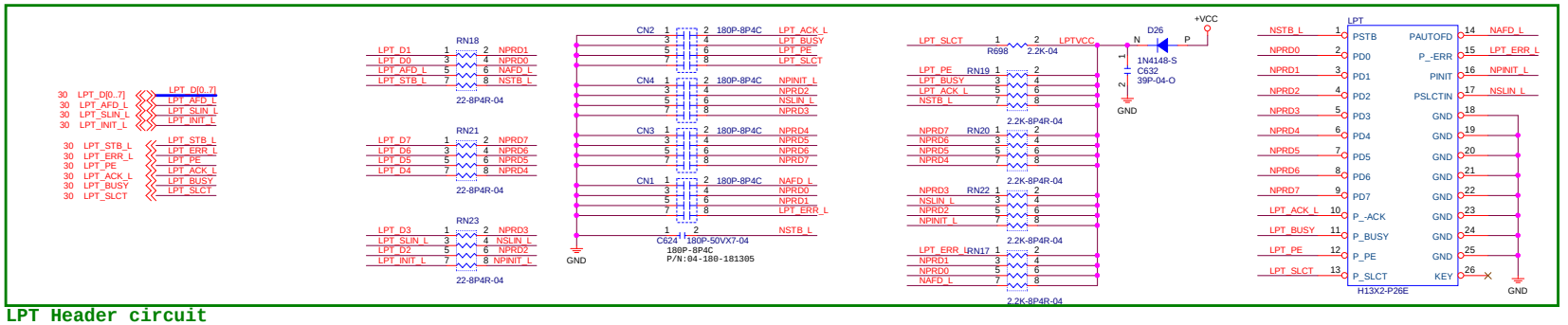


Front Panel circuit

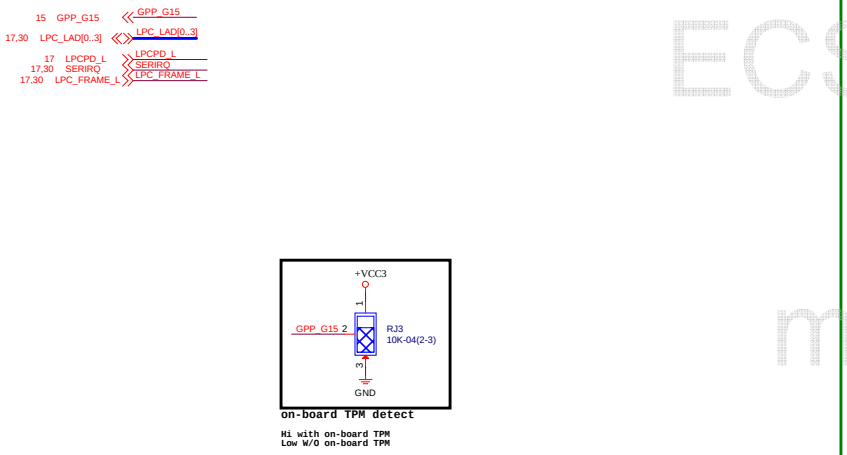


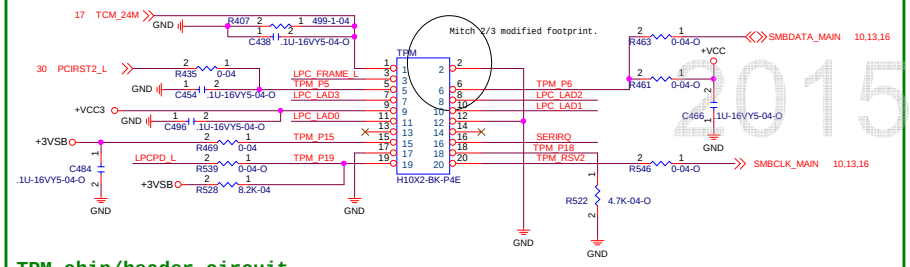
Power LED circuit

Elitegroup Computer Systems		
Title: FAN/Buzzer/PS2/Front Panel		
Size: Custom	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 31 of 46	

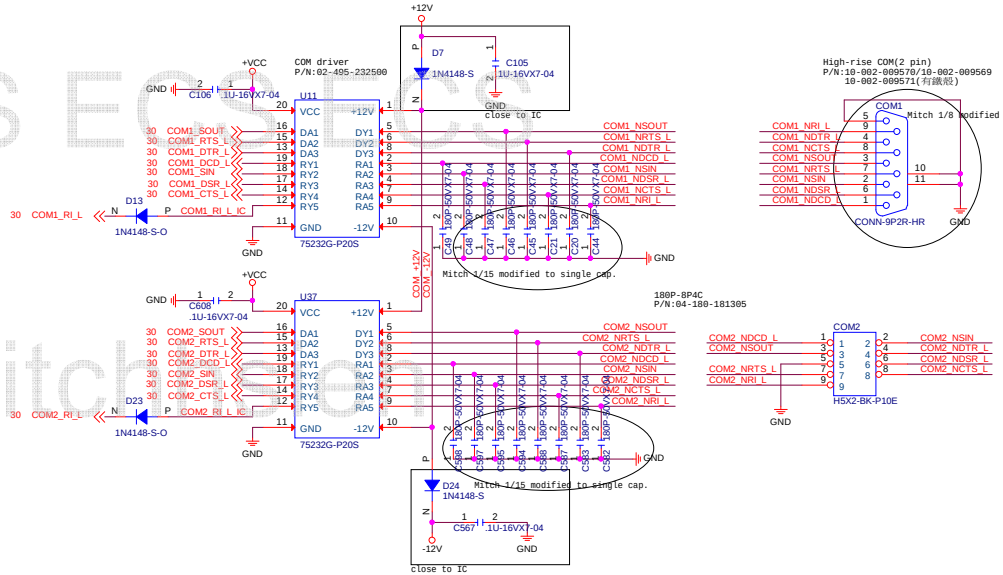


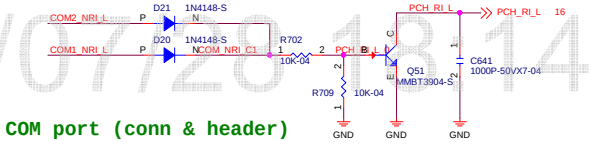
LPT Header circuit





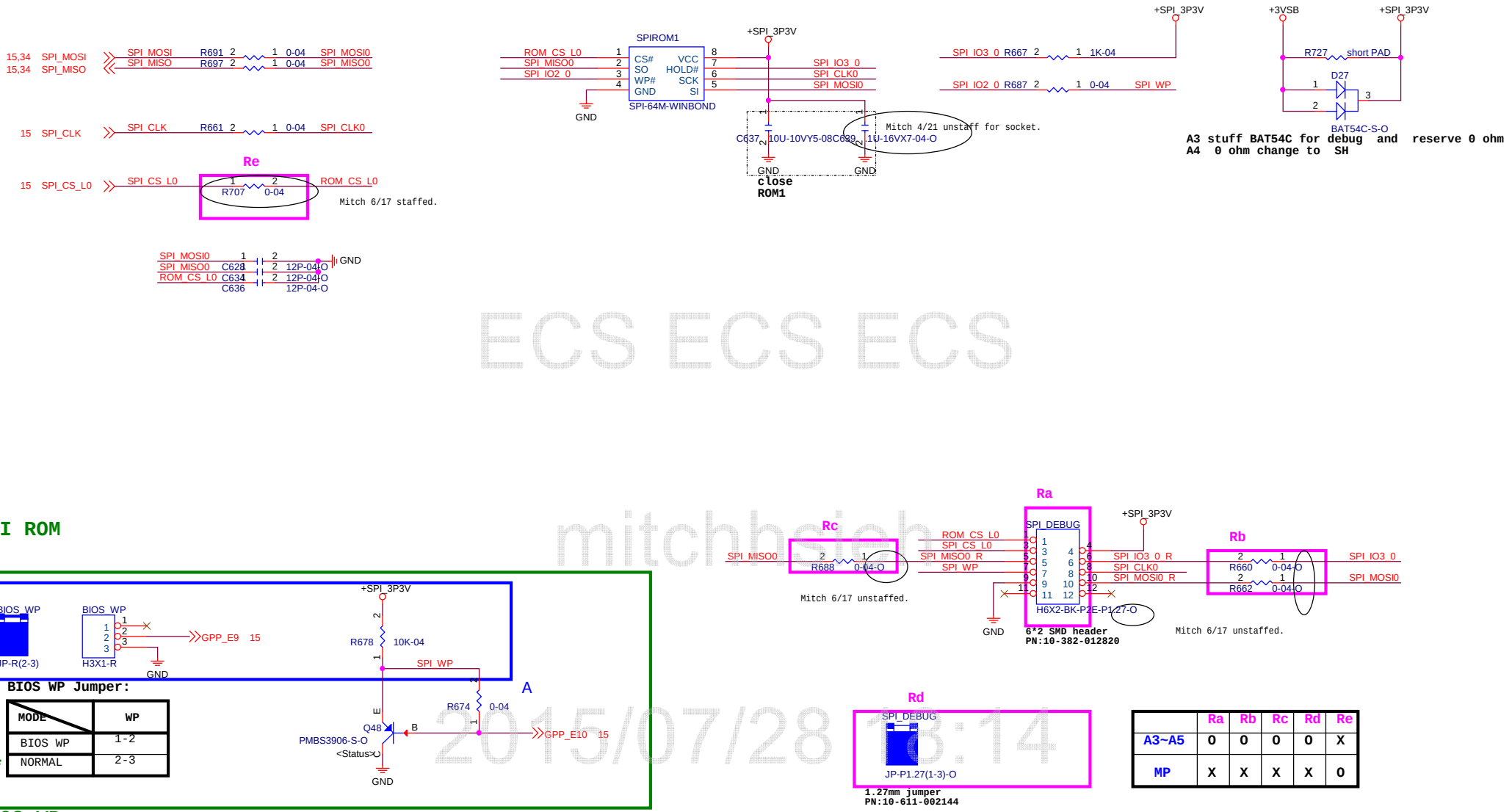
TPM chip/header circuit





COM port (conn & header)

Elitegroup Computer Systems			
Title: TPM/TCM/LPT/COM/Asset ID			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 32 of 46		



SPI ROM

BIOS WP

	Ra	Rb	Rc	Rd	Re
A3~A5	0	0	0	0	X
MP	X	X	X	X	0

Title: SPI ROM			
Size: B	Document Number: H11H4-AD		Rev: 1.0
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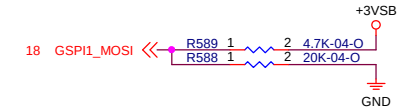
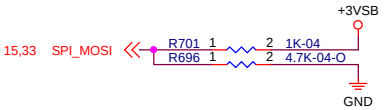
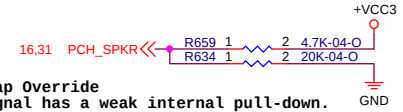


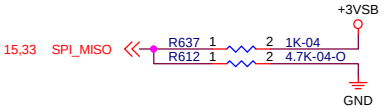
BOOT SELECT STRAP
IF SAMPLED HIGH, LPC IS SELECTED ELSE SPI
PCH HAS INTERNAL WEAK PD



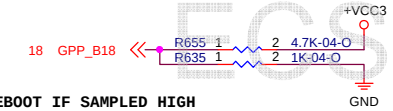
BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



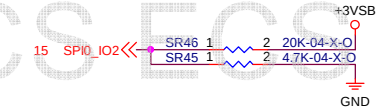
Top Swap Override
The signal has a weak internal pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.



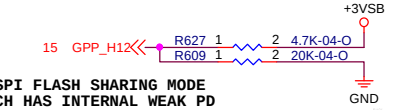
JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU



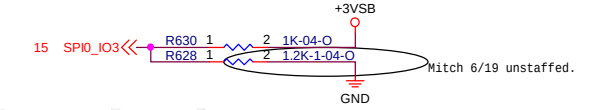
NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD



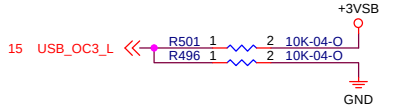
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



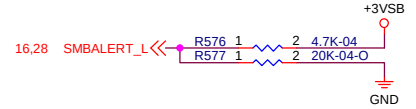
ESPI FLASH SHARING MODE
PCH HAS INTERNAL WEAK PD
0: MASTER ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING



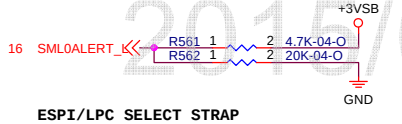
PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
(P.S. Pull down for pre ES1/ES1 only)



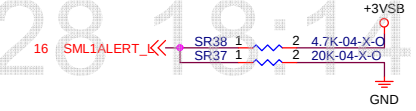
DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



TLS CONFIDENTIALITY ENABLED
IF SAMPLED HIGH(DEFAULT)
PCH HAS INTERNAL WEAK PD

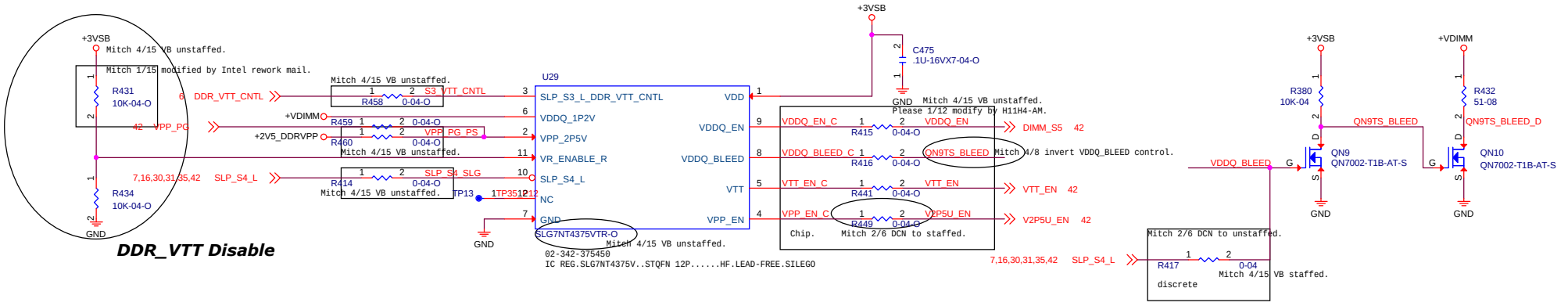


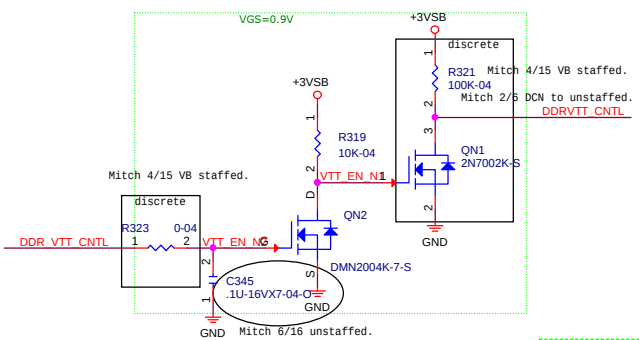
ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD

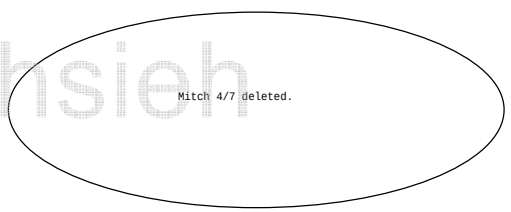


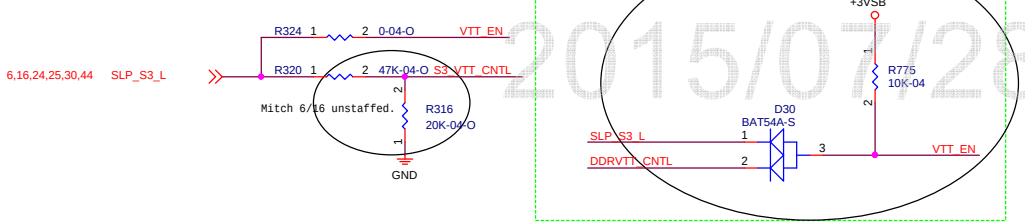
EXI BOOT STALL BYPASS IS ENABLED IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD

Title: Strap Pin		
Size: B	Document Number: H11H4-AD	Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 34 of 46	





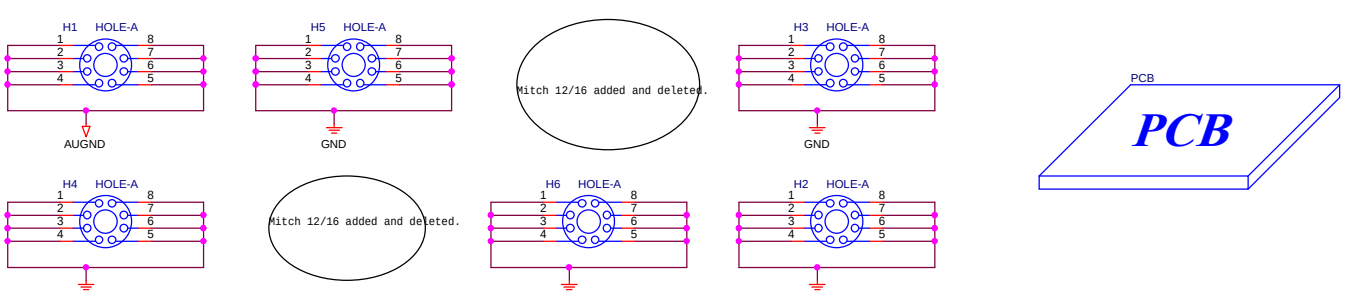




FUNCTION TABLE

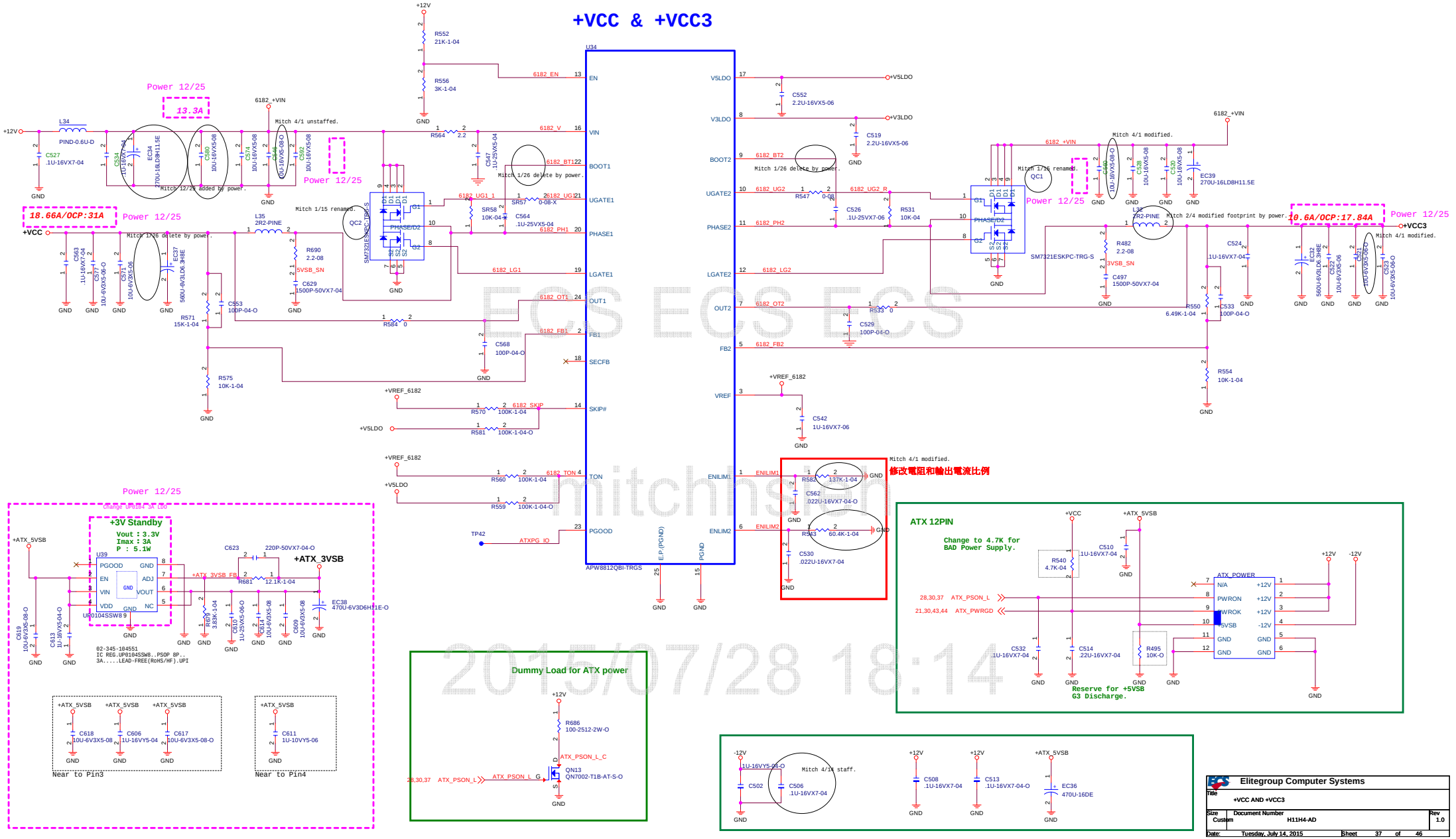
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Title	DP SWITCH		
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 35 of 46		

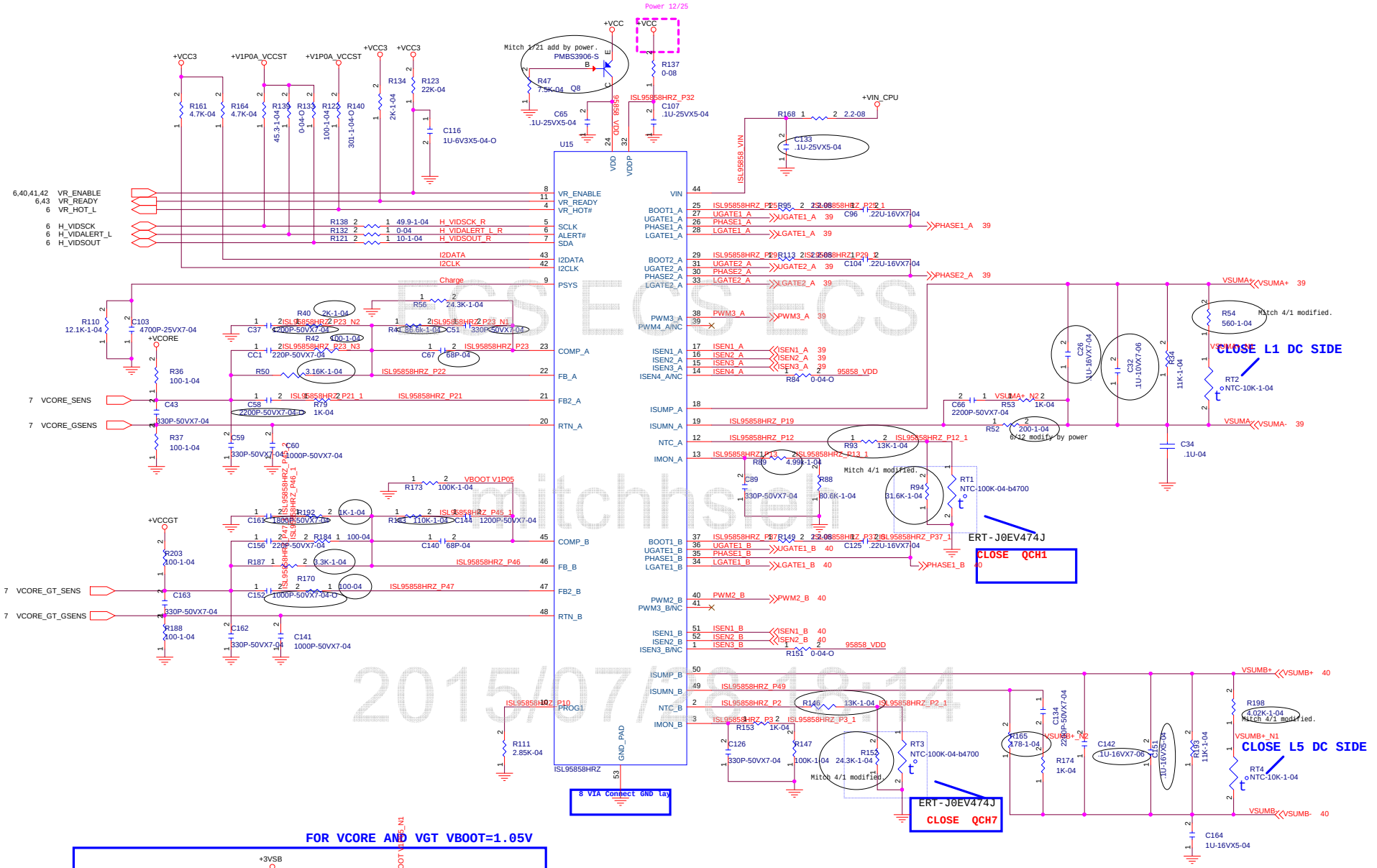


Elitegroup Computer Systems			
Title: XDP			
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 36 of 46		

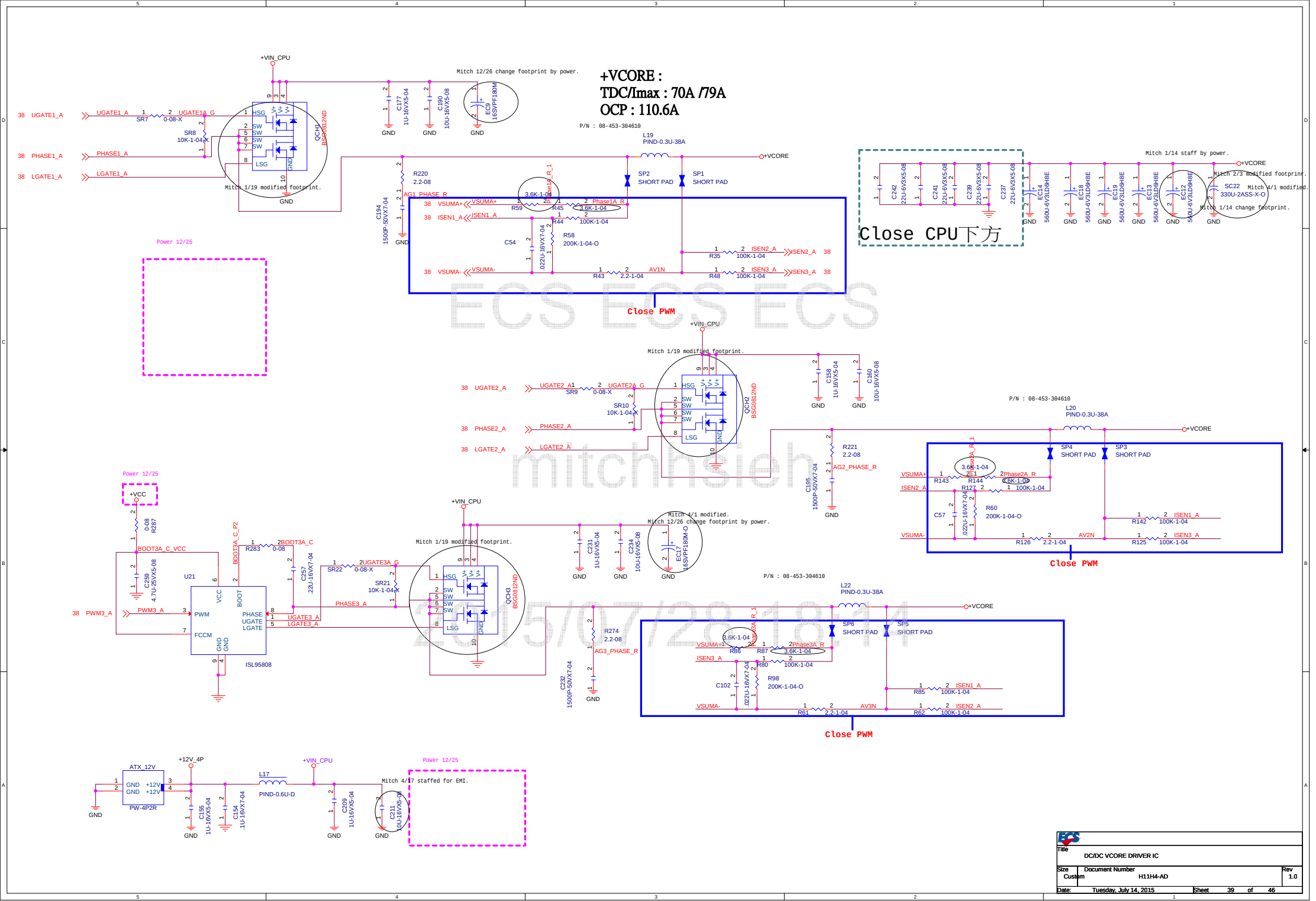
+VCC & +VCC3



Elitegroup Computer Systems	
Title	+VCC AND +VCC3
Size: Custom	Document Number: H11H4-AD
Rev	1.0
Date: Tuesday, July 14, 2015	Sheet 37 of 46



Company	Elitegroup Computer Systems
Title	DC/DC VCORE PWM IC
Size	Custom
Document Number	H11H4-AD
Rev	1.0
Date	Tuesday, July 14, 2015
Sheet	38 of 46


+VCORE :
TDC/Imax : 70A /79A
OCP : 110.6A
Close CPU下方
Close PWM
Close PWM
Close PWM
Power 12/25
Power 12/25
Mitch 12/26 change footprint by power.
Mitch 1/19 modified footprint.
Mitch 1/14 staff by power.
Mitch 2/3 modified footprint.
Mitch 1/14 change footprint.
Mitch 4/1 modified.
Mitch 4/17 staffed for EMI.
P/N : 08-453-304610
P/N : 08-453-304610
P/N : 08-453-304610
+VIN_CPU
+VCORE
+VCC
+12V_4P
ISL95808
PW-4P2R
ATX_12V
Title
DC/DC VCORE DRIVER IC
Size
Custom
Document Number
H11H4-AD
Rev
1.0
Date:
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39
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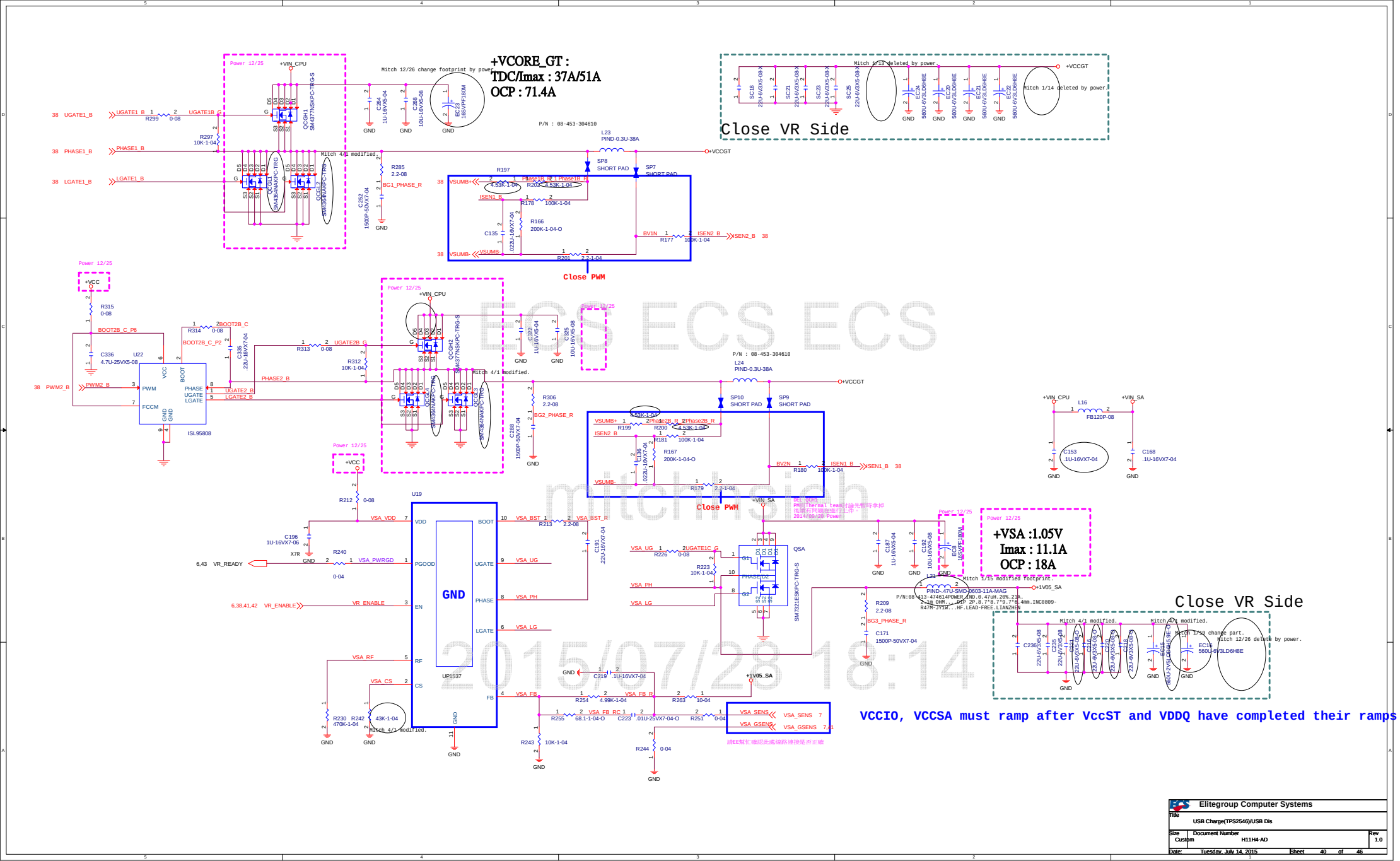
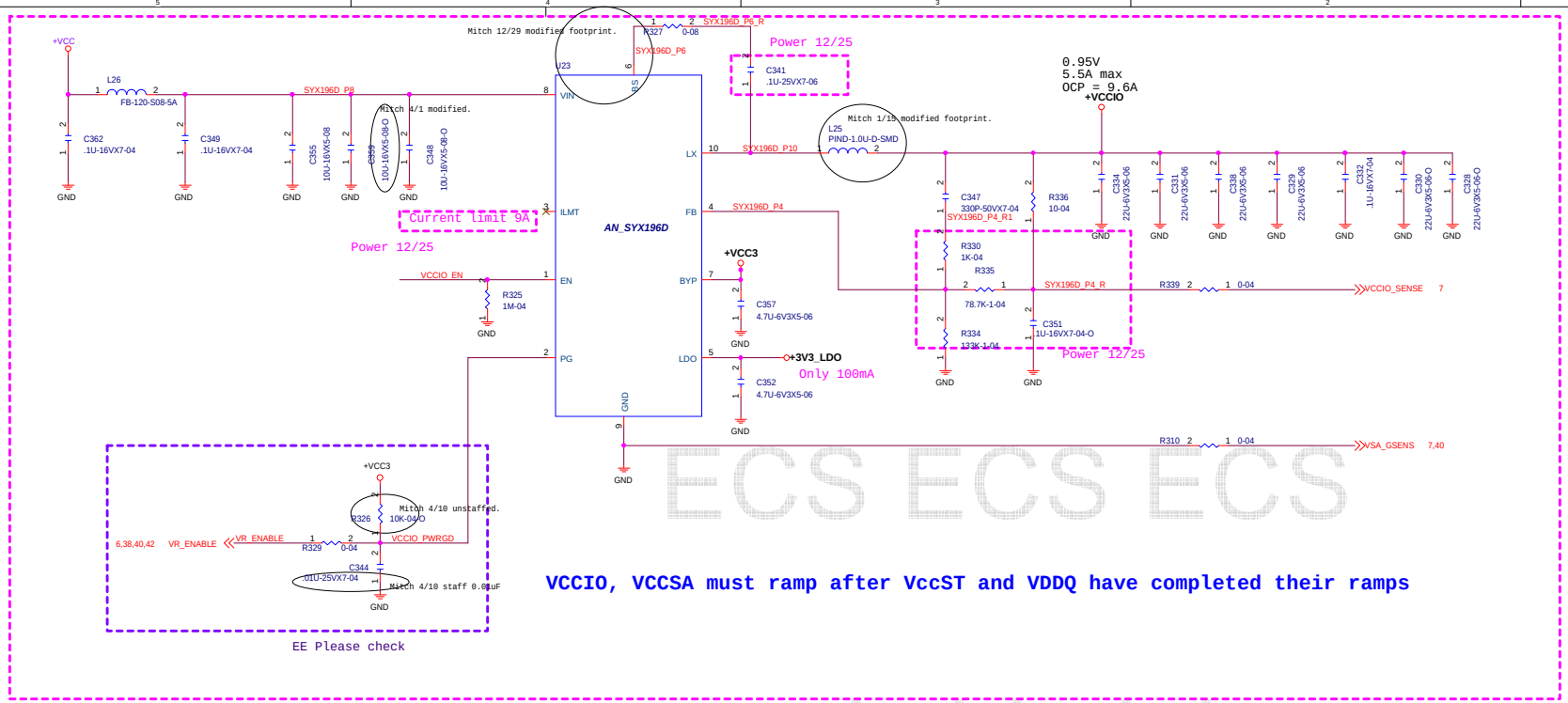
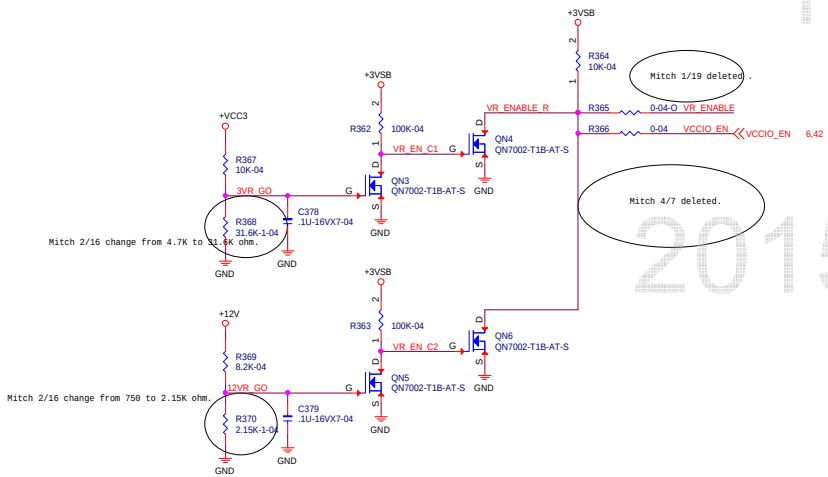
46


+VCORE_GT :
TDC/Imax : 37A/51A
OCP : 71.4A
Close VR Side
Close PWM
+VSA :1.05V
Imax : 11.1A
OCP : 18A
Close VR Side
VCCIO, VCCSA must ramp after VccST and VDDQ have completed their ramps
ISL95808
UP1537
SM7321ESKPC-TRG-S
SM4337NSKPC-TRG-S
SM4384NAKPC-TRG
Elitegroup Computer Systems
USB Charge(TPS2546)/USB Dis
H11H4-AD
Tuesday, July 14, 2015



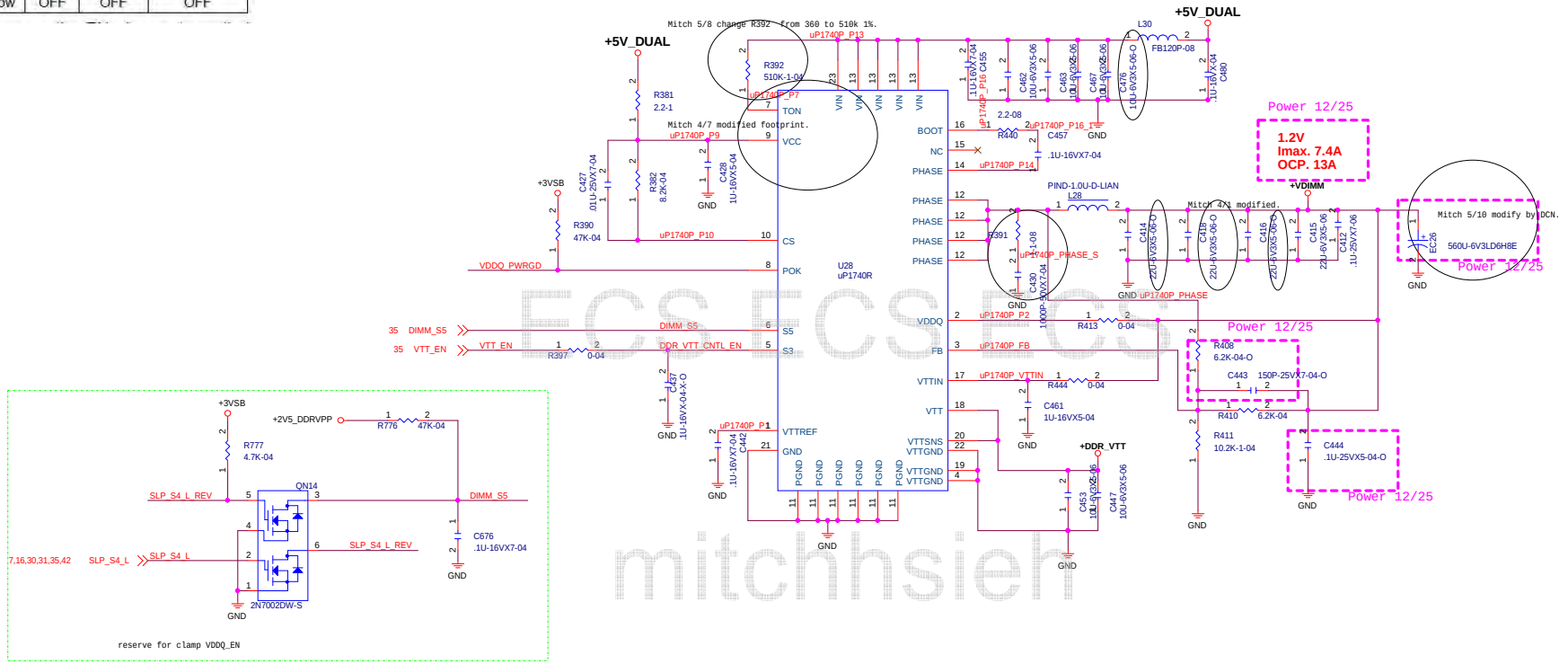


Title	DC/DC VCCIO		
Size C	Document Number H11H4-AD		Rev 1.0
Date: Tuesday, July 14, 2015	Sheet 41 of 46		

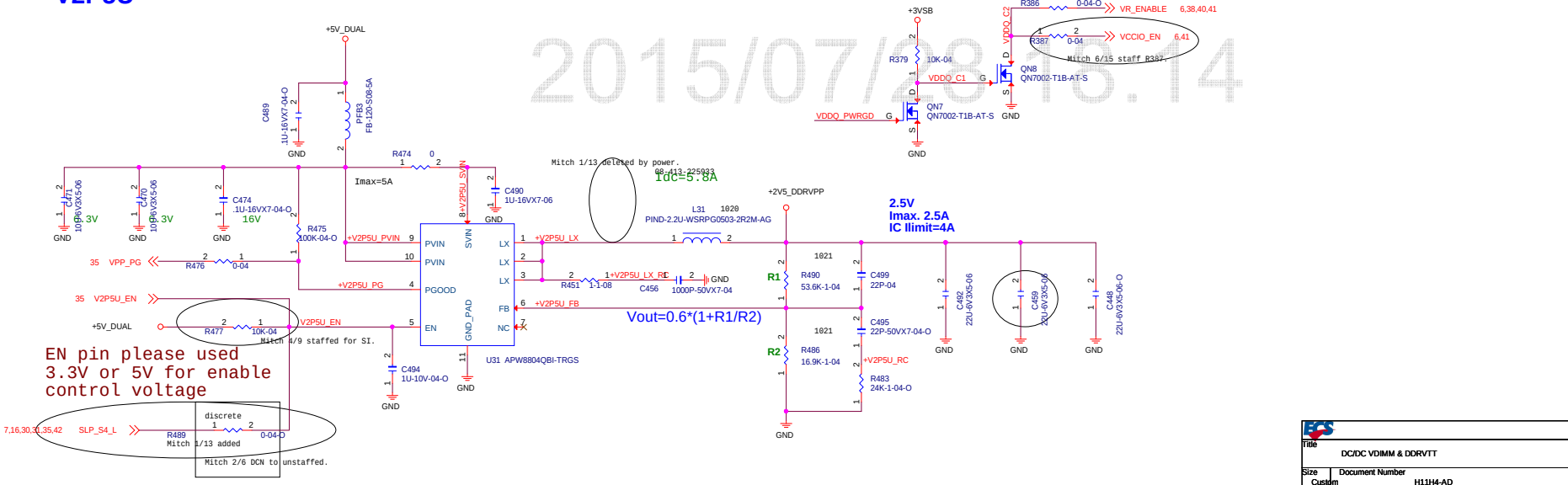
VDIMM

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

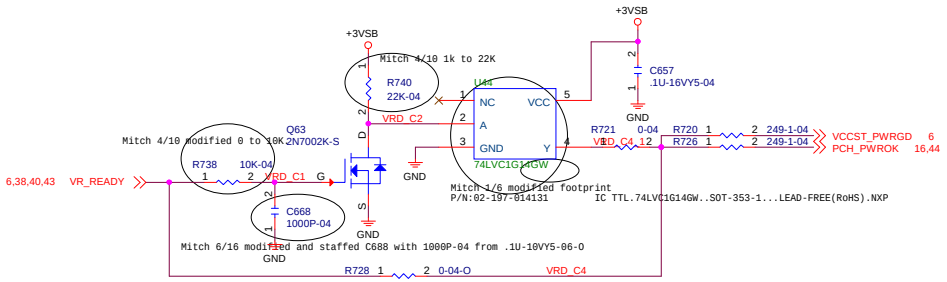


V2P5U

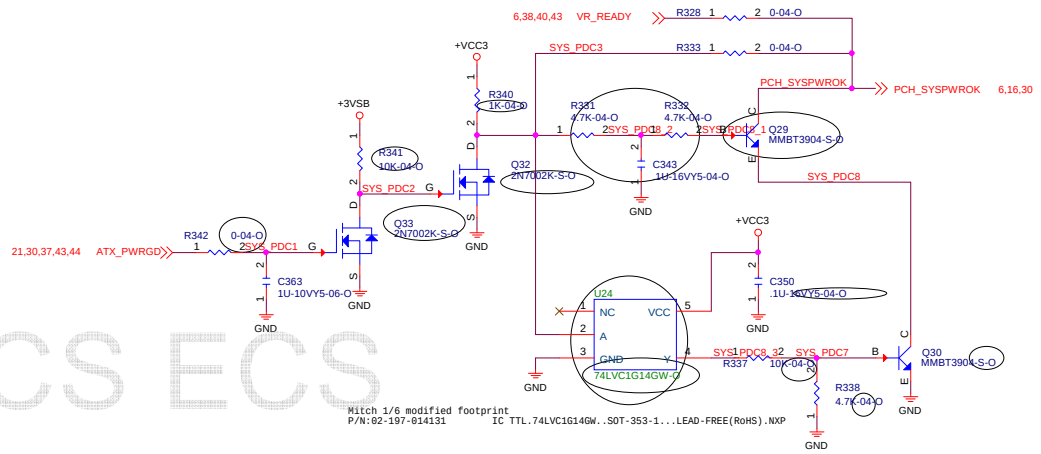


Title	DC/DC VDIMM & DDRVTT		
Size: Custom	Document Number: H11H4-AD		Rev: 1.0
Date: Tuesday, July 14, 2015	Sheet 42 of 46		

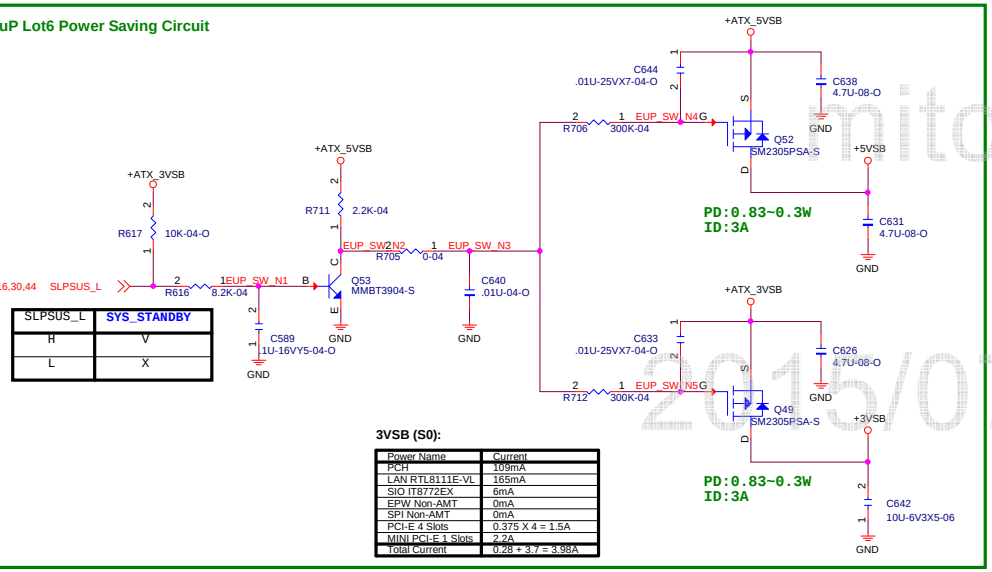
PCH & VCCST PWROK



SYS_PWROK SURPRISE POWER DOWN TRIGGERED BY PWRGD_PS



EuP Lot6 Power Saving Circuit

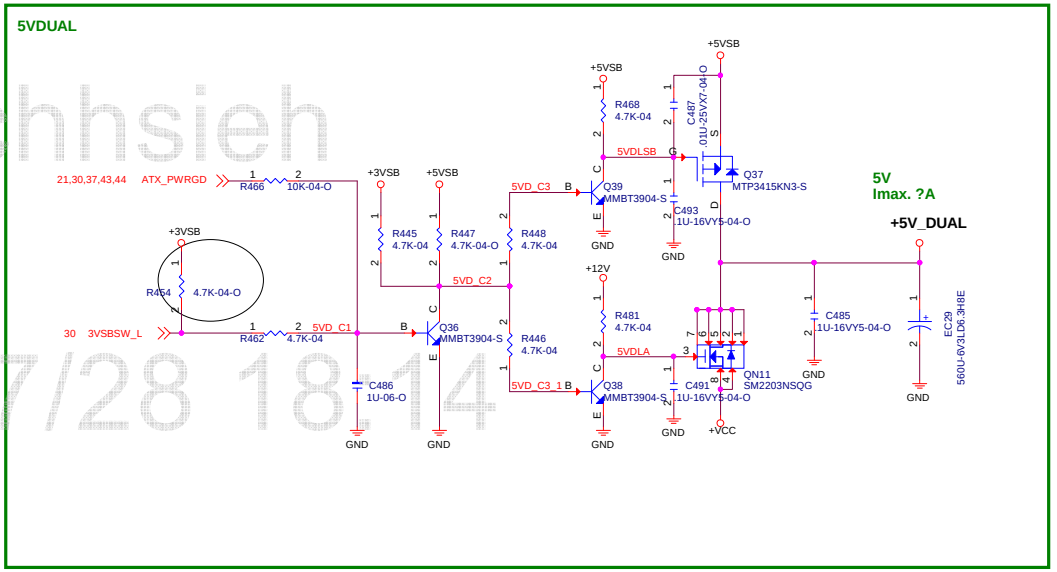


SLPSUS_L	SYS_STANDBY
H	V
L	X

3VSB (S0):

Power Name	Current
PCH	105mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	2.2A
Total Current	0.28 + 3.7 = 3.98A

5VDUAL



Title	DC/DC DDRVPP & 5VDUAL		
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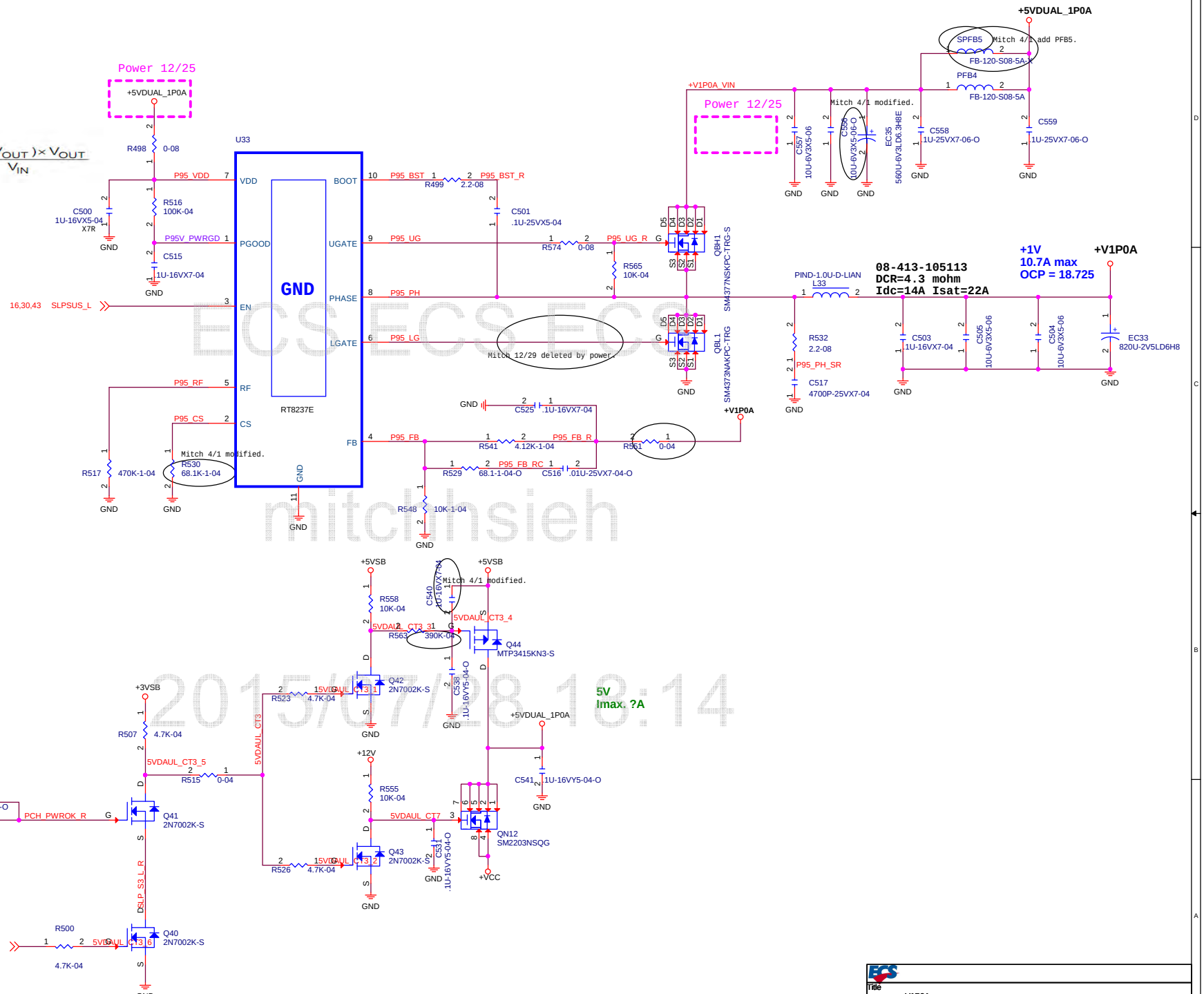
V1P0A

$$I_{LOAD\_OC} = \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{CS\_OC}}{8 \times R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$



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Size	Document Number		Rev
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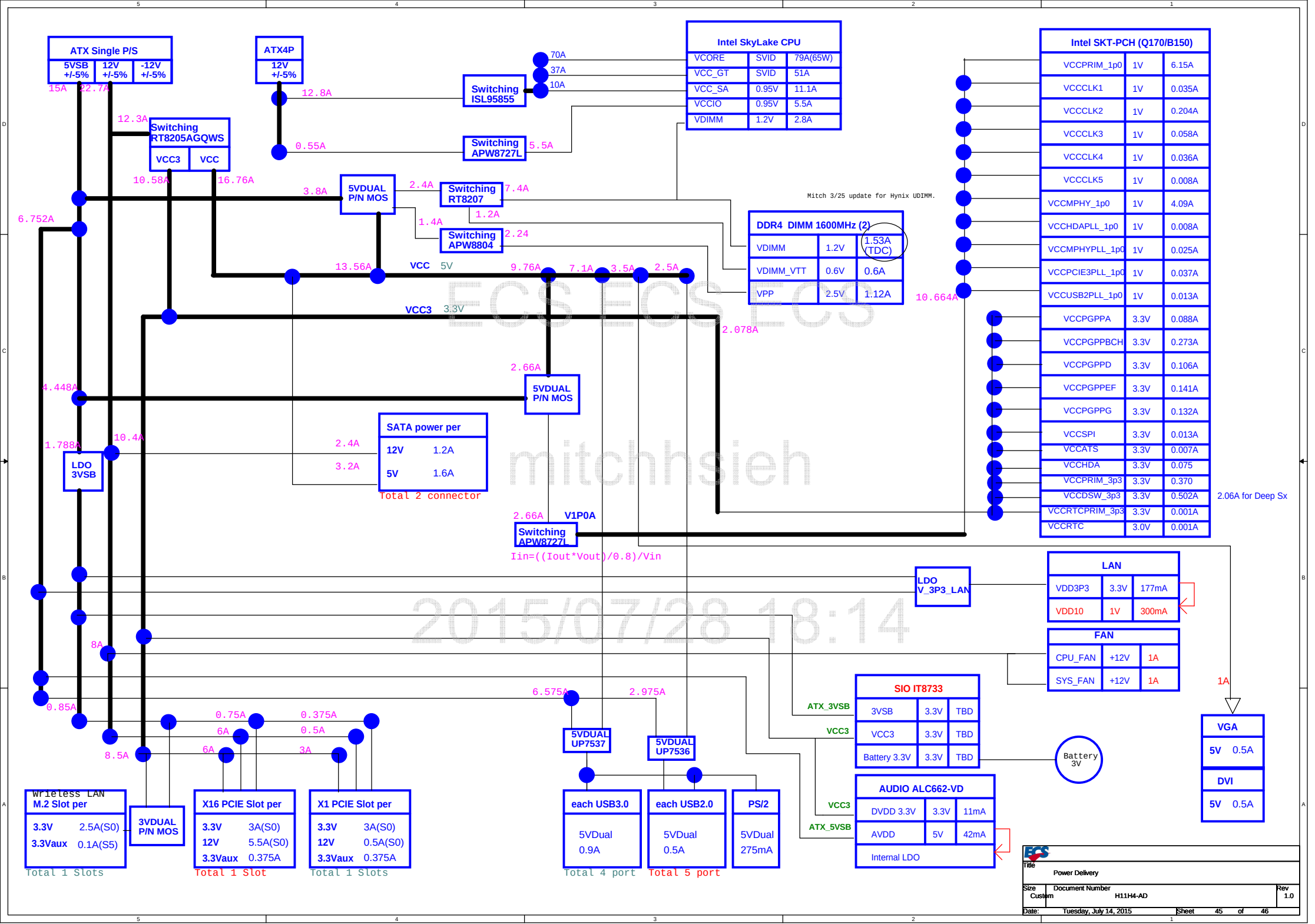
ATX Single P/S
5VSB +/-5%
12V +/-5%
-12V +/-5%
15A
22.7A
ATX4P
12V +/-5%
12.8A
0.55A
12.3A
Switching RT8205AGQWS
VCC3
VCC
10.58A
16.76A
Switching ISL95855
70A
37A
10A
Switching APW8727L
5.5A
Intel SkyLake CPU
VCORE SVID 79A(65W)
VCC_GT SVID 51A
VCC_SA 0.95V 11.1A
VCCIO 0.95V 5.5A
VDIMM 1.2V 2.8A
3.8A
5VDUAL P/N MOS
2.4A
Switching RT8207
7.4A
1.2A
1.4A
Switching APW8804
2.24
6.752A
13.56A
VCC 5V
9.76A
7.1A
3.5A
2.5A
Mitch 3/25 update for Hynix UDIMM.
DDR4 DIMM 1600MHz (2)
VDIMM 1.2V 1.53A (TDC)
VDIMM_VTT 0.6V 0.6A
VPP 2.5V 1.12A
Intel SKT-PCH (Q170/B150)
VCCPRIM_1p0 1V 6.15A
VCCCLK1 1V 0.035A
VCCCLK2 1V 0.204A
VCCCLK3 1V 0.058A
VCCCLK4 1V 0.036A
VCCCLK5 1V 0.008A
VCCMPHY_1p0 1V 4.09A
VCCHDAPLL_1p0 1V 0.008A
VCCMPHYPLL_1p0 1V 0.025A
VCCPCIE3PLL_1p0 1V 0.037A
VCCUSB2PLL_1p0 1V 0.013A
10.664A
VCCPGPPA 3.3V 0.088A
VCCPGPPBCH 3.3V 0.273A
VCCPGPPD 3.3V 0.106A
VCCPGPPEF 3.3V 0.141A
VCCPGPPG 3.3V 0.132A
VCCSPI 3.3V 0.013A
VCCATS 3.3V 0.007A
VCCHDA 3.3V 0.075
VCCPRIM_3p3 3.3V 0.370
VCCDSW_3p3 3.3V 0.502A
VCCRTCPRIM_3p3 3.3V 0.001A
VCCRTC 3.0V 0.001A
2.06A for Deep Sx
VCC3 3.3V
2.078A
2.66A
5VDUAL P/N MOS
4.448A
1.788A
10.4A
LDO 3VSB
2.4A
3.2A
SATA power per
12V 1.2A
5V 1.6A
Total 2 connector
2.66A
V1P0A
Switching APW8727L
Iin=((Iout*Vout)/0.8)/Vin
LDO V_3P3_LAN
LAN
VDD3P3 3.3V 177mA
VDD10 1V 300mA
FAN
CPU_FAN +12V 1A
SYS_FAN +12V 1A
1A
8A
0.85A
6.575A
2.975A
ATX_3VSB
VCC3
SIO IT8733
3VSB 3.3V TBD
VCC3 3.3V TBD
Battery 3.3V 3.3V TBD
Battery 3V
VGA
5V 0.5A
DVI
5V 0.5A
0.75A
6A
6A
0.375A
0.5A
3A
8.5A
5VDUAL UP7537
5VDUAL UP7536
AUDIO ALC662-VD
DVDD 3.3V 3.3V 11mA
AVDD 5V 42mA
Internal LDO
VCC3
ATX_5VSB
Wrieless LAN M.2 Slot per
3.3V 2.5A(S0)
3.3Vaux 0.1A(S5)
Total 1 Slots
3VDUAL P/N MOS
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 1 Slots
each USB3.0
5VDual 0.9A
Total 4 port
each USB2.0
5VDual 0.5A
Total 5 port
PS/2
5VDual 275mA
ECS ECS ECS
mitchhsieh
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Power Delivery
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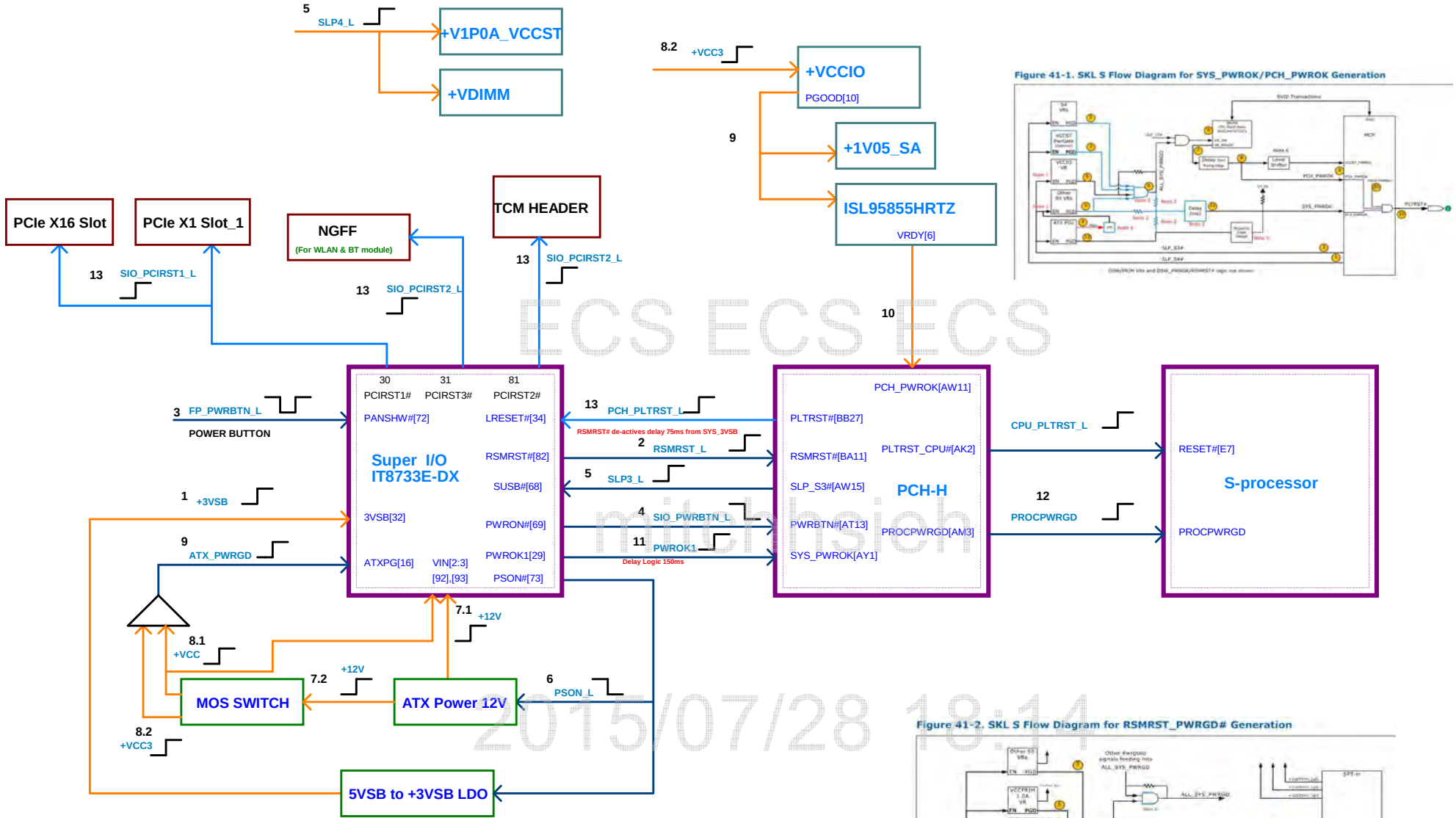
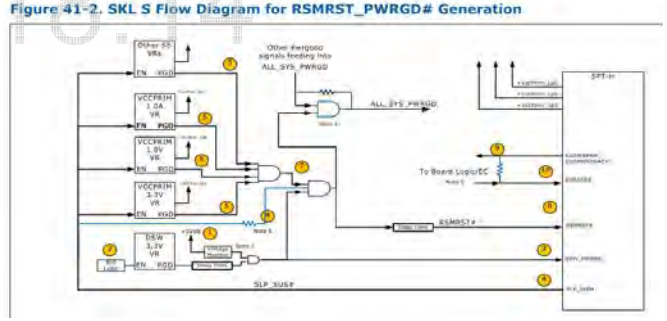


Figure 41-1. SKL S Flow Diagram for SYS_PWROK/PCH_PWROK Generation

Figure 41-2. SKL S Flow Diagram for RSMRST_PWRGD# Generation



Title	Power Sequence MAP		
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