COVER PAGE

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41	POWER_DELIVERY_1.2V_&_2.5V	1.0	
42	POWER_DELIVERY_LOADSWITCH	1.0	
43	POWER_DELIVERY_Backlight	1.0	
44	POWER_DELIVERY_CORE_&_NB	1.0	
45	V1P8GPU/V3P3GPU/V0P95GPU	1.0	
46	POWER_DELIVERY_V1P35GPU	1.0	
47	POWER_DELIVERY_VGA_CORE	1.0	
48	GPU_Weston_Pro_PCIE	1.0	
49	GPU_Weston_Pro_Main_MSIC	1.0	
50	GPU_Weston_Pro_TMDP	1.0	
51	GPU_Weston_Pro_DP_Power	1.0	
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53	GPU_Weston_Pro_MEMORY	1.0	
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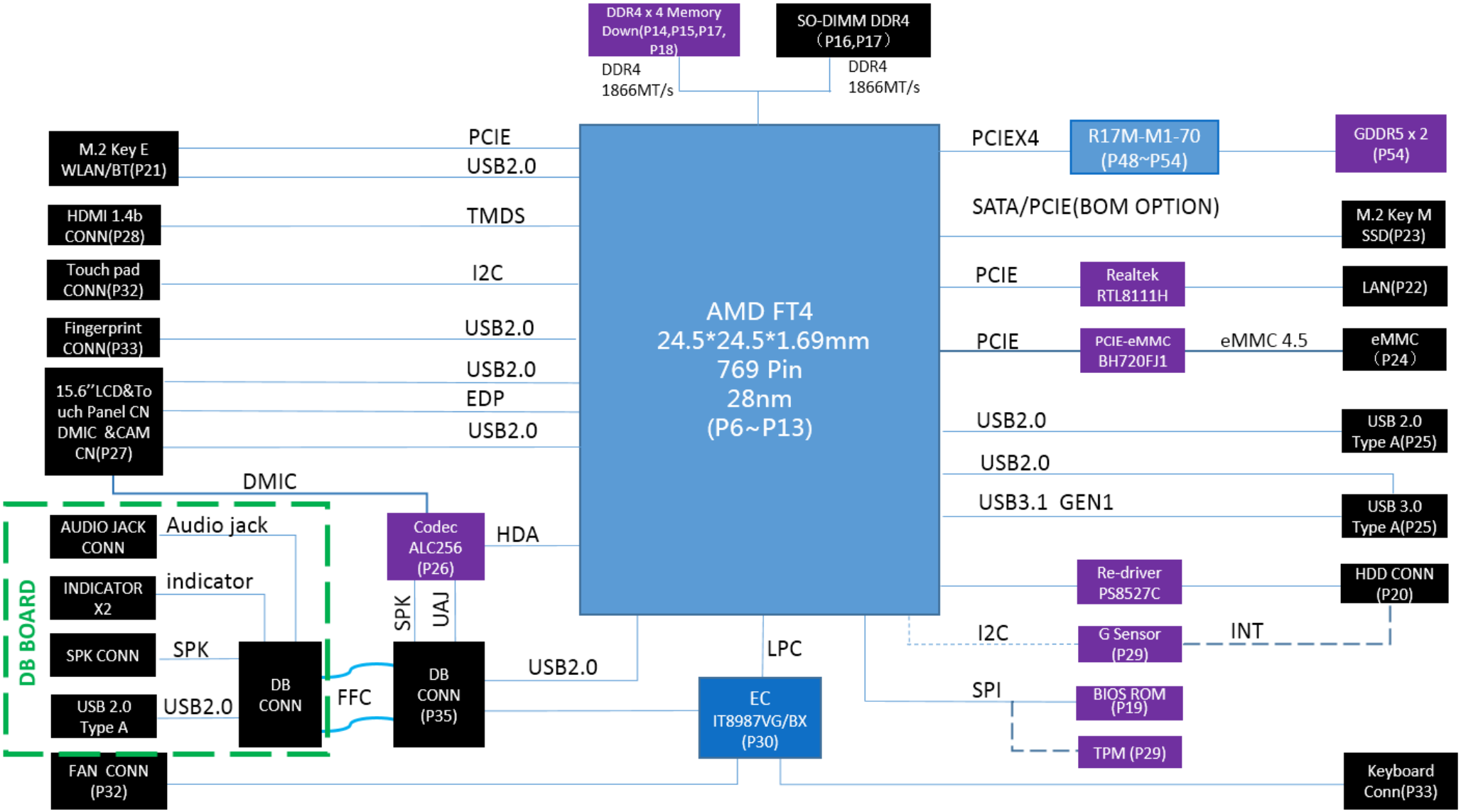
MB Block Diagram



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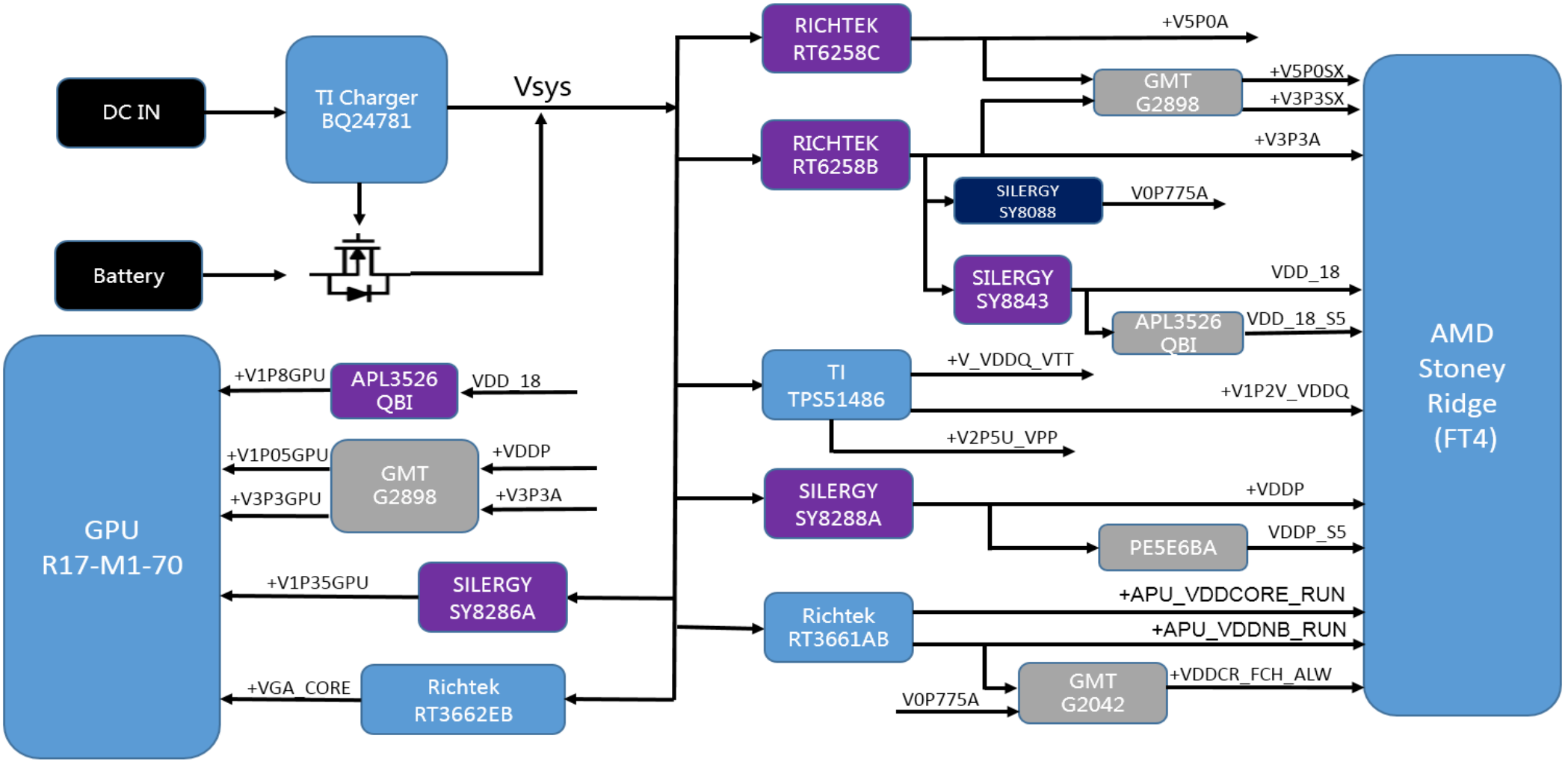
MB Power Map



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Power States(Adapter)

Signal	+VCCSP3_LDO_OUT	+V5P0A	+V3P3A	+V1P8A	+V0P95A	+V0P775A	+VDDCR_PCH_ALW	+V1P2V_VDDQ	+V5P0SX	+V3P3SX	+V1P8SX	+VDDP_S0	+V_VDDQ_VTT	+APU_VDDCORE_RUN	+APU_VDDNB_RUN	+V3P3GPU	+V1P8GPU	+V0P95GPU	+V1P35GPU	+VGA_CORE
S0(Full On)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5(SoftOff)	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Power States(Battery)

Signal	+VCCSP3_LDO_OUT	+V5P0A	+V3P3A	+V1P8A	+V0P95A	+V0P775A	+VDDCR_PCH_ALW	+V1P2V_VDDQ	+V5P0SX	+V3P3SX	+V1P8SX	+VDDP_S0	+V_VDDQ_VTT	+APU_VDDCORE_RUN	+APU_VDDNB_RUN	+V3P3GPU	+V1P8GPU	+V0P95GPU	+V1P35GPU	+VGA_CORE
S0(Full On)	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
S3(STM)	ON	ON	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5(SoftOff)	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

BOARD ID

BOARD_ID5 1--RU183 0--RU191	BOARD_ID4 1--RU182 0--RU190	BOARD_ID3 1--RU181 0--RU189	BOARD_ID2 1--RU180 0--RU188	BOARD_ID1 1--RU179 0--RU187	BOARD_ID0 1--RU178 0--RU186
1--DGPU 0--UMA	1--SATA SSD 0--PCIE SSD	RESERVE	MEMORY ID		

SMBUS/I2C Control Table

	SOURCE	GPU	BATT	IT8987E	SODIMM	Touch Pad	Thermal Sensor	APU	Charger	G-SENSOR Sensor
SM_BAT_CLK SM_BAT_DATA	IT8987E +V3P3A_EC	X	V		X	X	X	X	V	X
SM_THRM_SCL SM_THRM_SDA	IT8987E +V3P3SX_EC	V +V3P3GPU	X		X	X	V	V APU_SIC APU_SID +V1P8SX	X	X
APU_SMB_CLK APU_SMB_DATA	APU +V3P3SX	X	X	X	V	X	X		X	X
GSEN_I2C0_SCL GSEN_I2C0_SDA	APU +V1P8_GSENSOR	X	X	X	X	X	X		X	V
TOUCHPAD_I2C_CLK TOUCHPAD_I2C_SDA	APU +V3P3A_CP	X	X	X	X	V	X		X	X

PCIe/GFX Port

PCIE	Device
0	LAN
1	WLAN
2	eMMC
3	SSD
GFX	Device
0-3	DGPU

USB2.0 Port

Port	Device
0	Blue Tooth
1	DB USB2.0
2	Finger print
4	USB 3.0 Port
5	USB2.0
6	Touch Panel
7	Camera

SATA Port

Port	Device
0	HDD
1	SSD

USB3.0 Port

Port	Device
0	USB3.0 Type-A
1	NA

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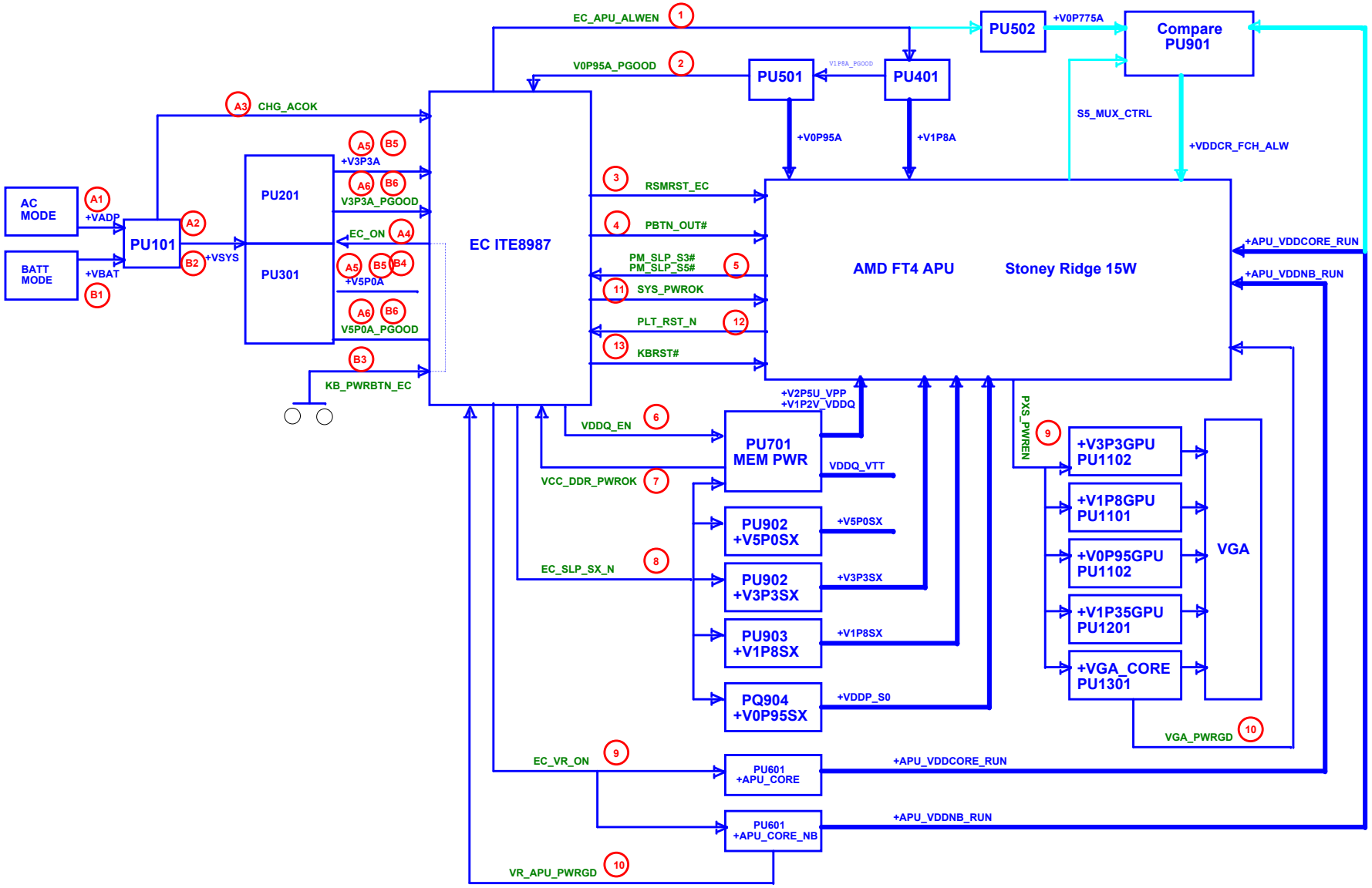

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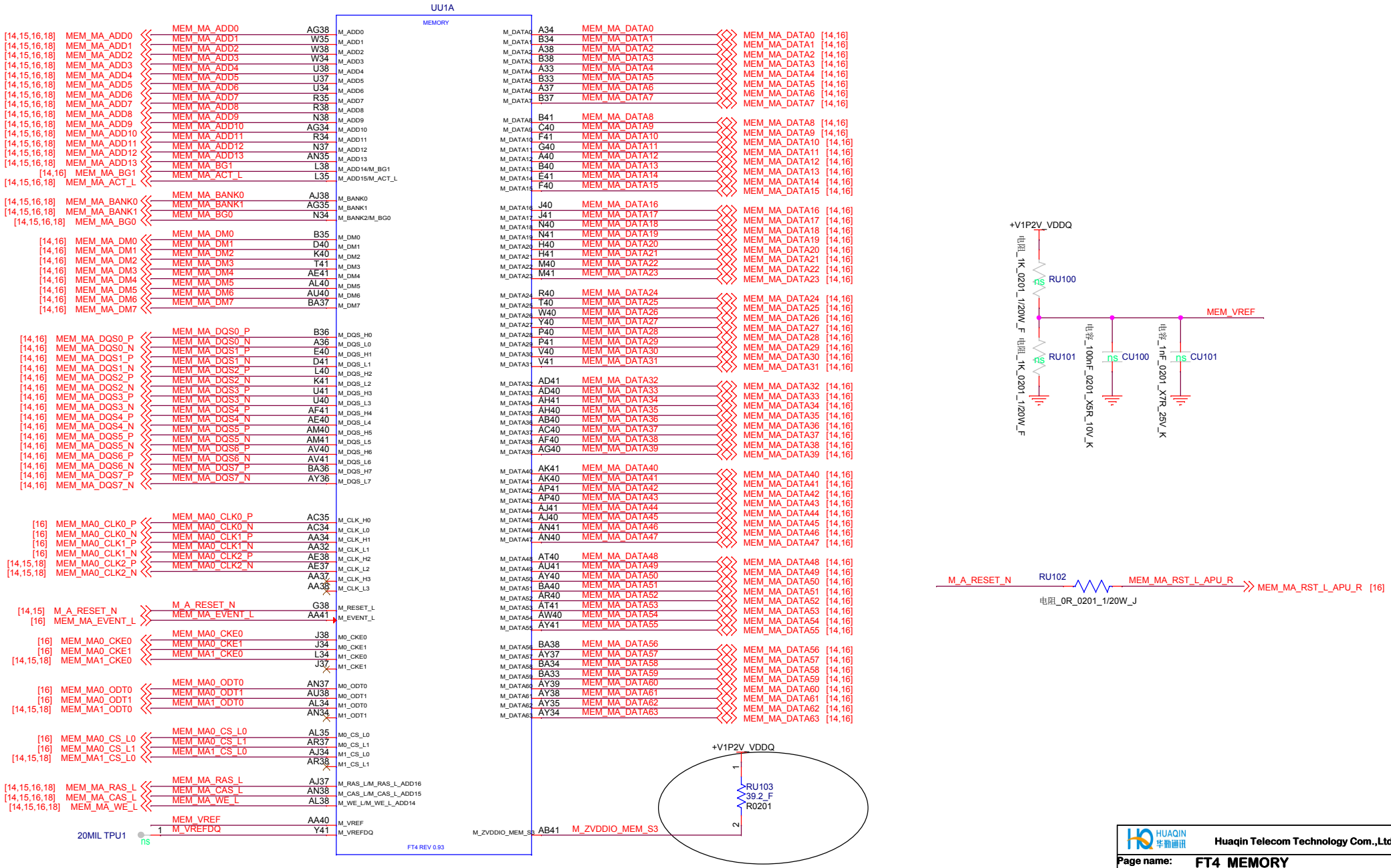
UU1A
MEMORY
FT4 REV 0.93
MEM_MA_ADD0 AG38
MEM_MA_ADD1 W35
MEM_MA_ADD2 W38
MEM_MA_ADD3 W34
MEM_MA_ADD4 U38
MEM_MA_ADD5 U37
MEM_MA_ADD6 U34
MEM_MA_ADD7 R35
MEM_MA_ADD8 R38
MEM_MA_ADD9 N38
MEM_MA_ADD10 AG34
MEM_MA_ADD11 R34
MEM_MA_ADD12 N37
MEM_MA_ADD13 AN35
MEM_MA_BG1 L38
MEM_MA_ACT_L L35
MEM_MA_BANK0 AJ38
MEM_MA_BANK1 AG35
MEM_MA_BG0 N34
MEM_MA_DM0 B35
MEM_MA_DM1 D40
MEM_MA_DM2 K40
MEM_MA_DM3 T41
MEM_MA_DM4 AE41
MEM_MA_DM5 AL40
MEM_MA_DM6 AU40
MEM_MA_DM7 BA37
MEM_MA_DQS0_P B36
MEM_MA_DQS0_N A36
MEM_MA_DQS1_P E40
MEM_MA_DQS1_N D41
MEM_MA_DQS2_P L40
MEM_MA_DQS2_N K41
MEM_MA_DQS3_P U41
MEM_MA_DQS3_N U40
MEM_MA_DQS4_P AF41
MEM_MA_DQS4_N AE40
MEM_MA_DQS5_P AM40
MEM_MA_DQS5_N AM41
MEM_MA_DQS6_P AV40
MEM_MA_DQS6_N AV41
MEM_MA_DQS7_P BA36
MEM_MA_DQS7_N AY36
MEM_MA0_CLK0_P AC35
MEM_MA0_CLK0_N AC34
MEM_MA0_CLK1_P AA34
MEM_MA0_CLK1_N AA32
MEM_MA0_CLK2_P AE38
MEM_MA0_CLK2_N AE37
M_A_RESET_N G38
MEM_MA_EVENT_L AA41
MEM_MA0_CKE0 J38
MEM_MA0_CKE1 J34
MEM_MA1_CKE0 L34
MEM_MA0_ODT0 AN37
MEM_MA0_ODT1 AU38
MEM_MA1_ODT0 AL34
MEM_MA0_CS_L0 AL35
MEM_MA0_CS_L1 AR37
MEM_MA1_CS_L0 AJ34
MEM_MA_RAS_L AJ37
MEM_MA_CAS_L AN38
MEM_MA_WE_L AL38
MEM_VREF AA40
MEM_VREFDQ Y41
20MIL TPU1
M_ZVDDIO_MEM_S3 AB41
M_ZVDDIO_MEM_S3
MEM_MA_DATA0 A34
MEM_MA_DATA1 B34
MEM_MA_DATA2 A38
MEM_MA_DATA3 B38
MEM_MA_DATA4 A33
MEM_MA_DATA5 B33
MEM_MA_DATA6 A37
MEM_MA_DATA7 B37
MEM_MA_DATA8 B41
MEM_MA_DATA9 C40
MEM_MA_DATA10 F41
MEM_MA_DATA11 G40
MEM_MA_DATA12 A40
MEM_MA_DATA13 B40
MEM_MA_DATA14 E41
MEM_MA_DATA15 F40
MEM_MA_DATA16 J40
MEM_MA_DATA17 J41
MEM_MA_DATA18 N40
MEM_MA_DATA19 N41
MEM_MA_DATA20 H40
MEM_MA_DATA21 H41
MEM_MA_DATA22 M40
MEM_MA_DATA23 M41
MEM_MA_DATA24 R40
MEM_MA_DATA25 T40
MEM_MA_DATA26 W40
MEM_MA_DATA27 Y40
MEM_MA_DATA28 P40
MEM_MA_DATA29 P41
MEM_MA_DATA30 V40
MEM_MA_DATA31 V41
MEM_MA_DATA32 AD41
MEM_MA_DATA33 AD40
MEM_MA_DATA34 AH41
MEM_MA_DATA35 AH40
MEM_MA_DATA36 AB40
MEM_MA_DATA37 AC40
MEM_MA_DATA38 AF40
MEM_MA_DATA39 AG40
MEM_MA_DATA40 AK41
MEM_MA_DATA41 AK40
MEM_MA_DATA42 AP41
MEM_MA_DATA43 AP40
MEM_MA_DATA44 AJ41
MEM_MA_DATA45 AJ40
MEM_MA_DATA46 AN41
MEM_MA_DATA47 AN40
MEM_MA_DATA48 AT40
MEM_MA_DATA49 AU41
MEM_MA_DATA50 AY40
MEM_MA_DATA51 BA40
MEM_MA_DATA52 AR40
MEM_MA_DATA53 AT41
MEM_MA_DATA54 AW40
MEM_MA_DATA55 AY41
MEM_MA_DATA56 BA38
MEM_MA_DATA57 AY37
MEM_MA_DATA58 BA34
MEM_MA_DATA59 BA33
MEM_MA_DATA60 AY39
MEM_MA_DATA61 AY38
MEM_MA_DATA62 AY35
MEM_MA_DATA63 AY34
+V1P2V_VDDQ
RU103
39.2_F
R0201
+V1P2V_VDDQ
电阻_1K_0201_1/20W_F
RU100
RU101
MEM_VREF
电容_100nF_0201_X5R_10V_K
CU100
电容_1nF_0201_X7R_25V_K
CU101
M_A_RESET_N
RU102
MEM_MA_RST_L_APU_R
电阻_0R_0201_1/20W_J
KC.91202.A4E
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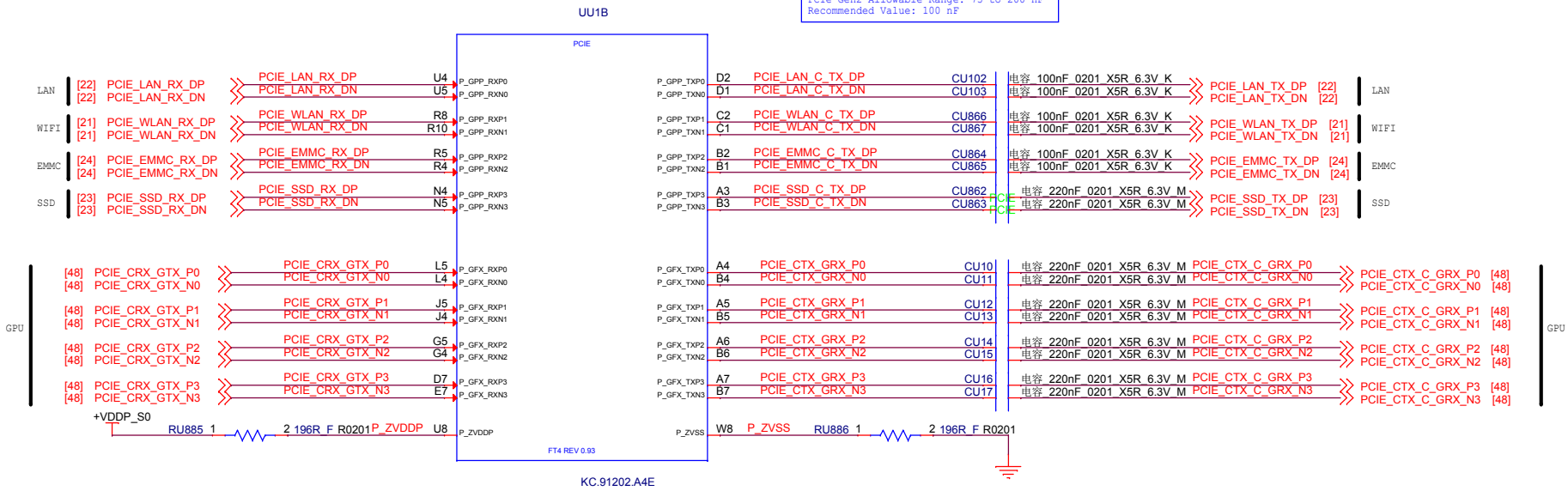
NOTE:
PCIe Gen3 Allowable Range: 176 to 265 nF
Recommended Value: 220 nF
PCIe Gen2 Allowable Range: 75 to 200 nF
Recommended Value: 100 nF



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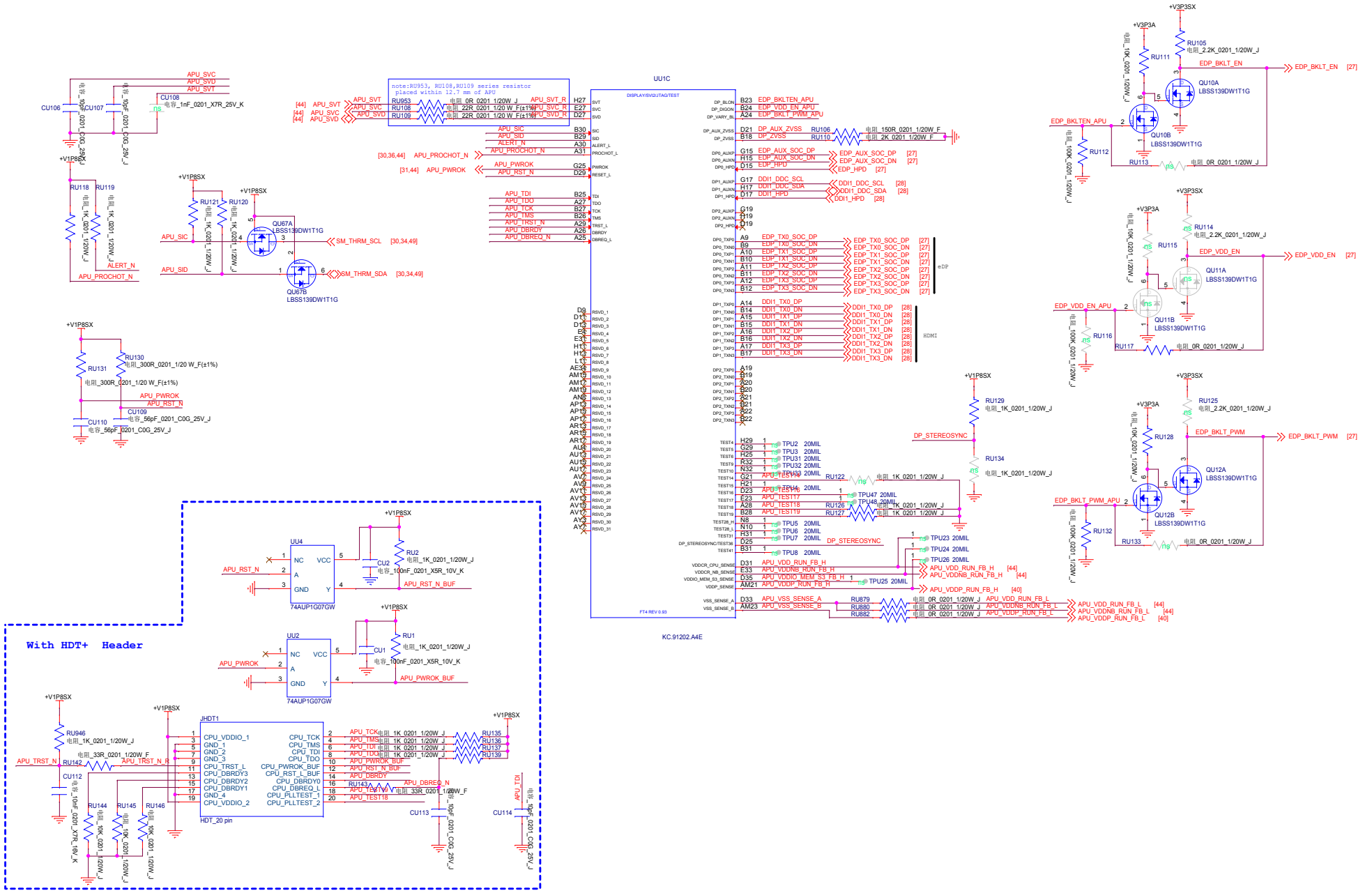
With HDT+ Header
UU1C
DISPLAY/SVI2/JTAG/TEST
note:RU953, RU108,RU109 series resistor placed within 12.7 mm of APU
APU_SVC
APU_SVD
APU_SVT
APU_PROCHOT_N
APU_PWROK
APU_RST_N
APU_SIC
APU_SID
APU_TDI
APU_TDO
APU_TCK
APU_TMS
APU_TRST_N
APU_DBRDY
APU_DBREQ_N
SM_THRM_SCL
SM_THRM_SDA
EDP_AUX_SOC_DP
EDP_AUX_SOC_DN
EDP_HPD
EDP_TX0_SOC_DP
EDP_TX0_SOC_DN
EDP_TX1_SOC_DP
EDP_TX1_SOC_DN
EDP_TX2_SOC_DP
EDP_TX2_SOC_DN
EDP_TX3_SOC_DP
EDP_TX3_SOC_DN
DDI1_DDC_SCL
DDI1_DDC_SDA
DDI1_HPD
DDI1_TX0_DP
DDI1_TX0_DN
DDI1_TX1_DP
DDI1_TX1_DN
DDI1_TX2_DP
DDI1_TX2_DN
DDI1_TX3_DP
DDI1_TX3_DN
EDP_BKLTEN_APU
EDP_VDD_EN_APU
EDP_BKLT_PWM_APU
DP_STEREOSYNC
APU_VDD_RUN_FB_H
APU_VDDNB_RUN_FB_H
APU_VDDP_RUN_FB_H
APU_VSS_SENSE_A
APU_VSS_SENSE_B
APU_VDD_RUN_FB_L
APU_VDDNB_RUN_FB_L
APU_VDDP_RUN_FB_L
JHDT1
HDT_20 pin
74AUP1G07GW
eDP
HDMI
KC.91202.A4E
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Page name: FT4_DISPLAY/SVI2/JTAG/TEST
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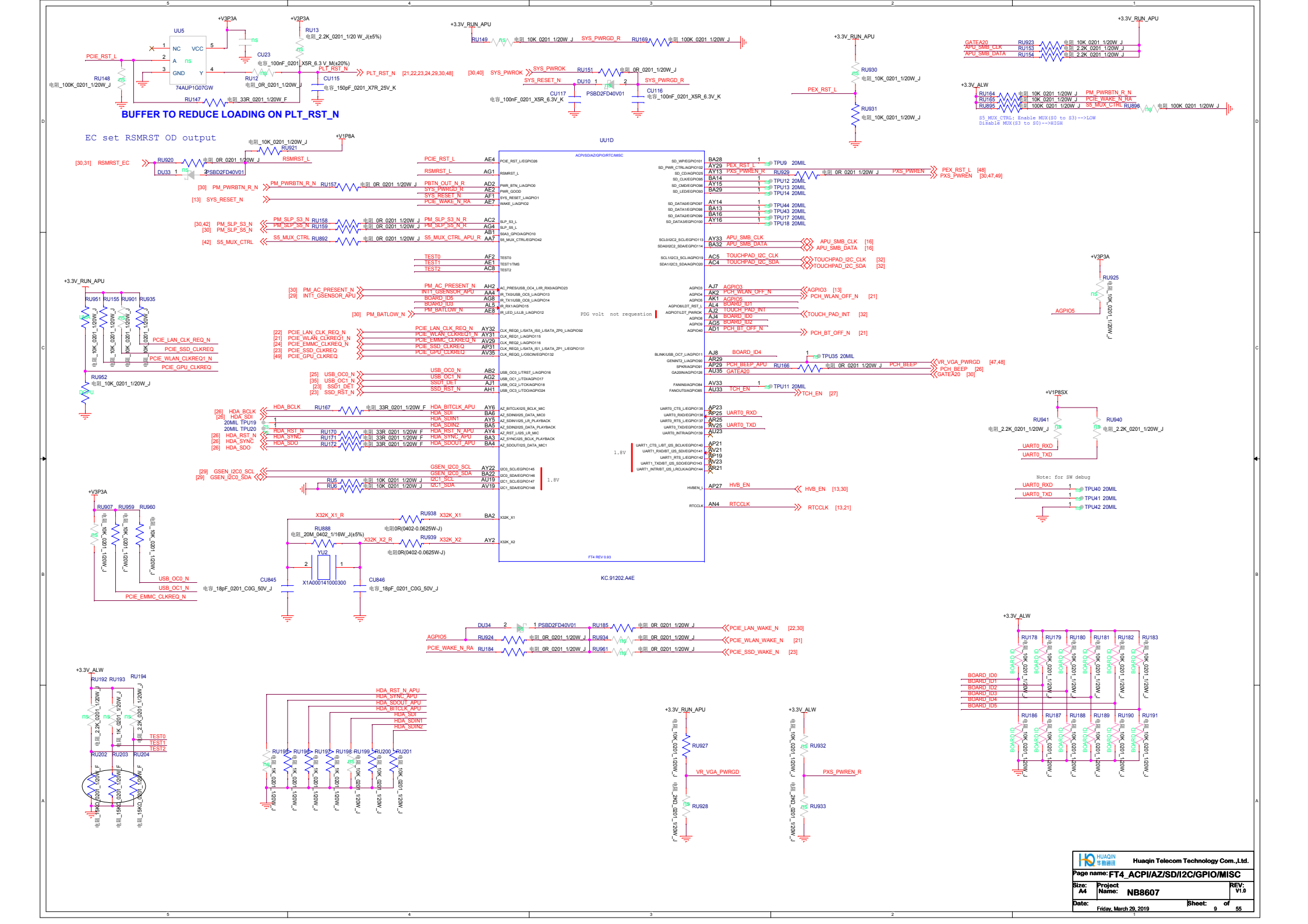
BUFFER TO REDUCE LOADING ON PLT_RST_N
EC set RSMRST OD output
UU1D
ACPI/SD/AZ/GPIO/RTC/MISC
FT4 REV 0.93
KC.91202.A4E
PDG volt not requestion
Note: for SW debug
S5_MUX_CTRL: Enable MUX(S0 to S3)-->LOW
Disable MUX(S3 to S0)-->HIGH
Huaqin Telecom Technology Com.,Ltd.
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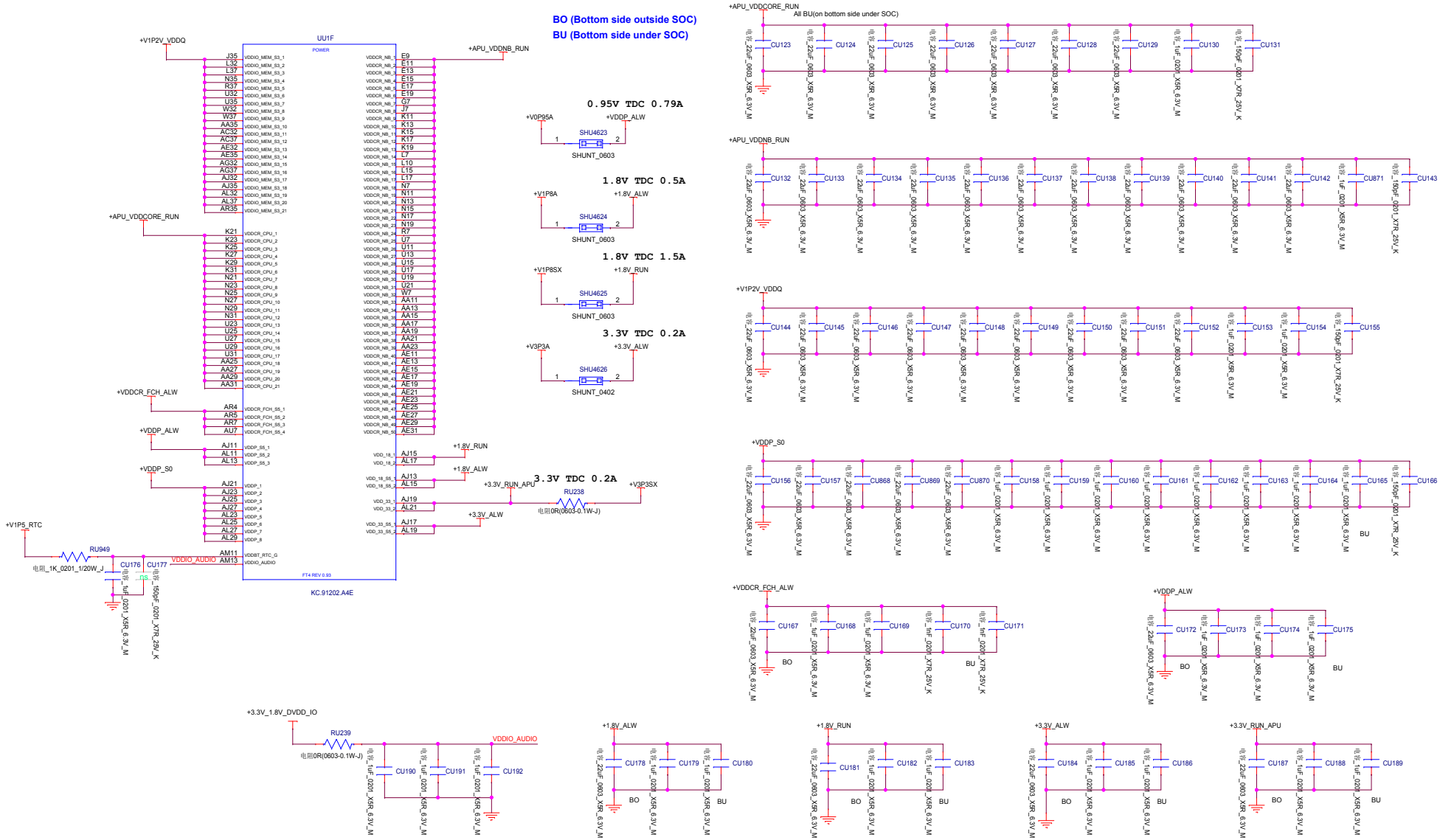

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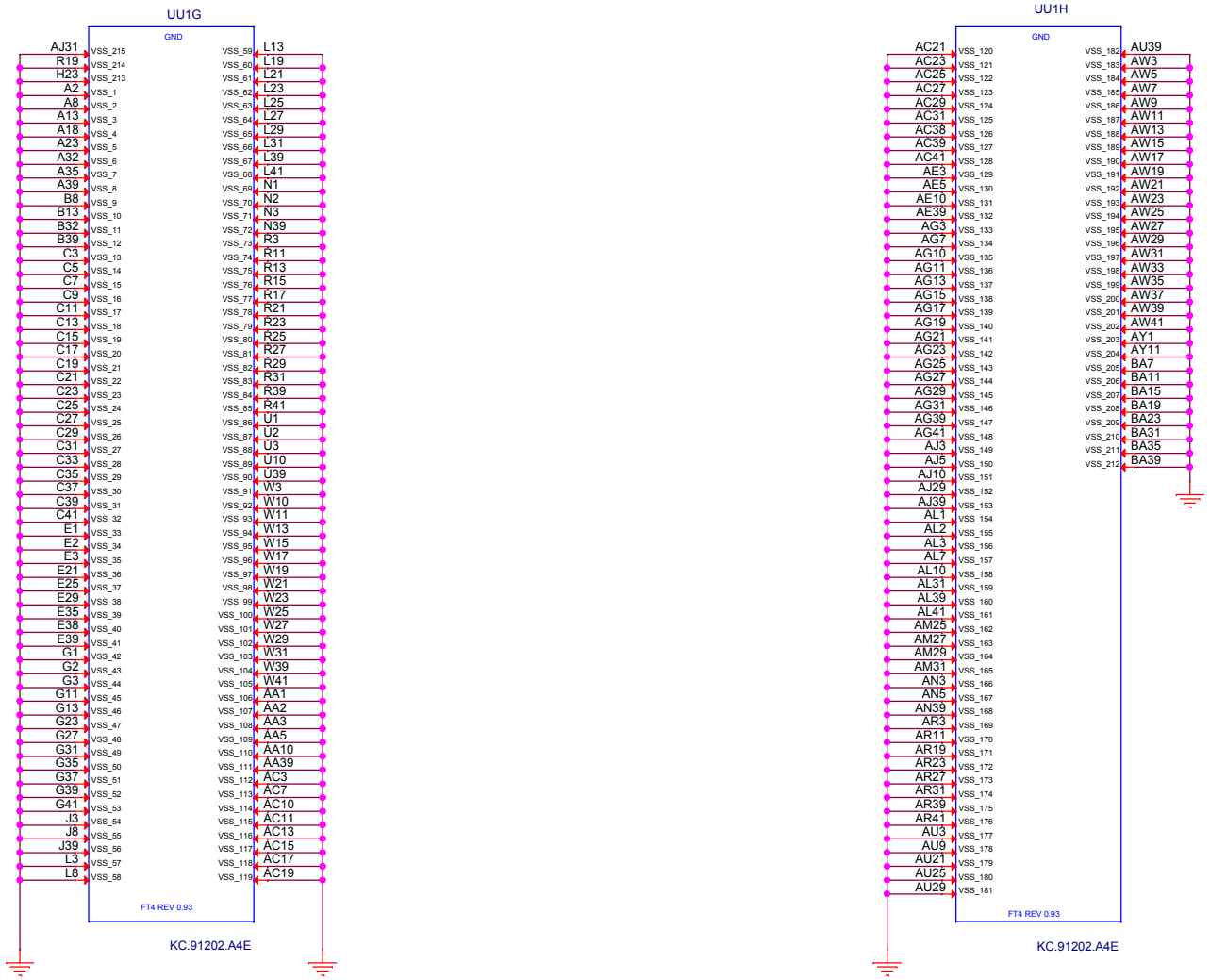

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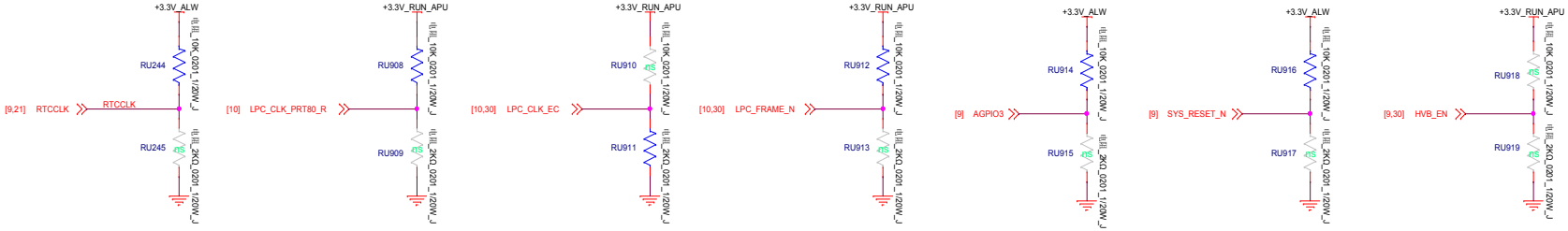

	LPC_CLK0 (LPC_CLK_EC)	LPC_CLK1 (LPC_CLK_PRT80_R)	LFRAME_L	AGPIO3 Int pull-up	RTC_CLK Int pull-up	SYS_RST# Int pull-up	HVB_EN
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	SPI ROM (DEFAULT)	Enhanced reset (for quicker S5 (DEFAULT)	Coin battery is on board. (DEFAULT)	normal reset mode (DEFAULT)	floating Disable HVB
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC ROM	Default to traditional reset logic	Coin battery is not on board.	short reset mode	connected to VSS Enable HVB

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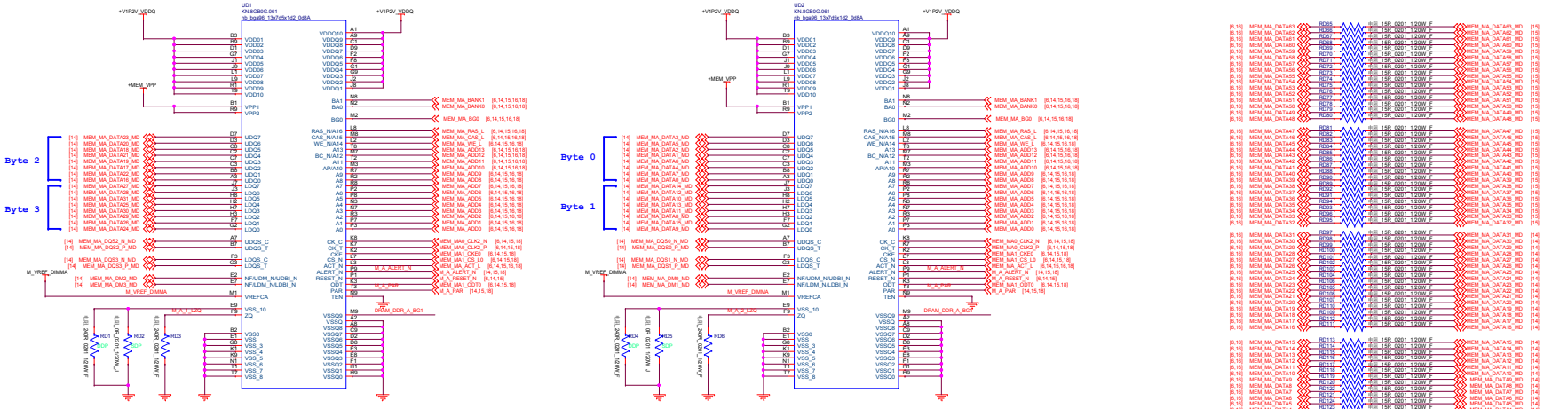
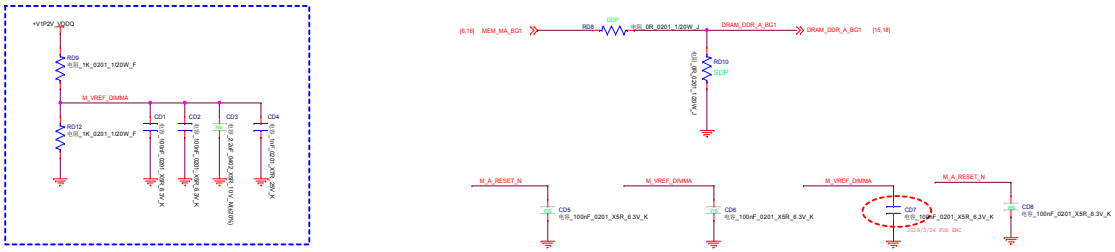


SDRAM REF GENERATION



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Page name:	DDR4 CH-A(DEVICE0)
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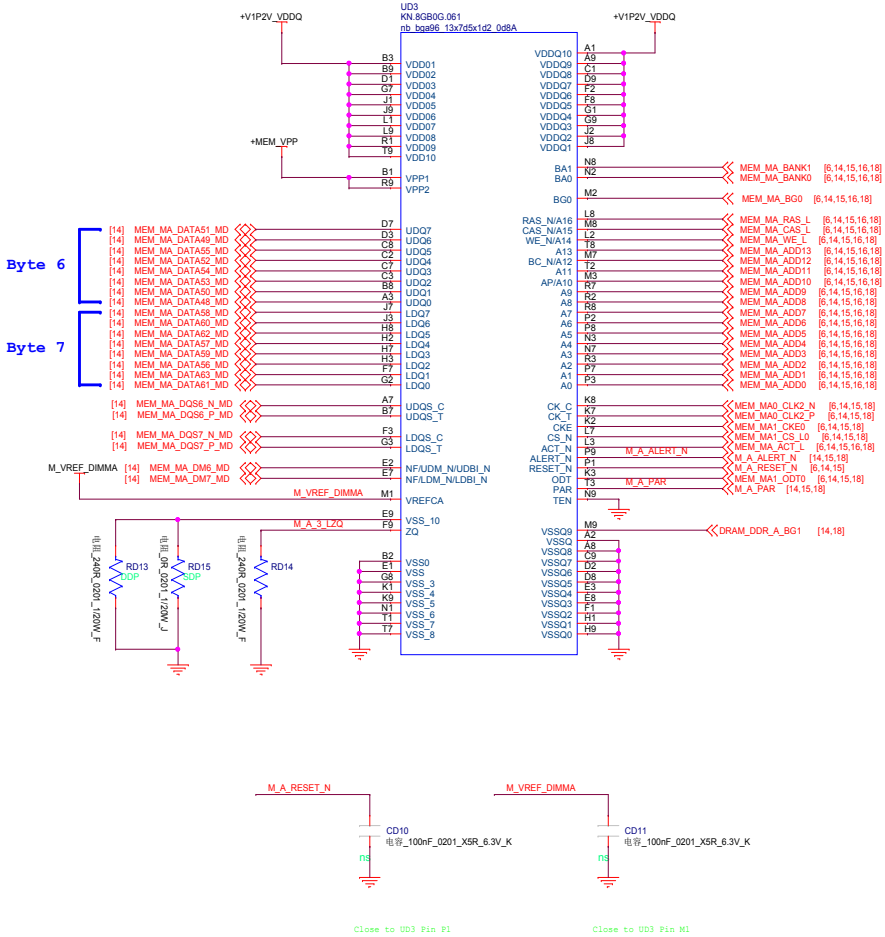

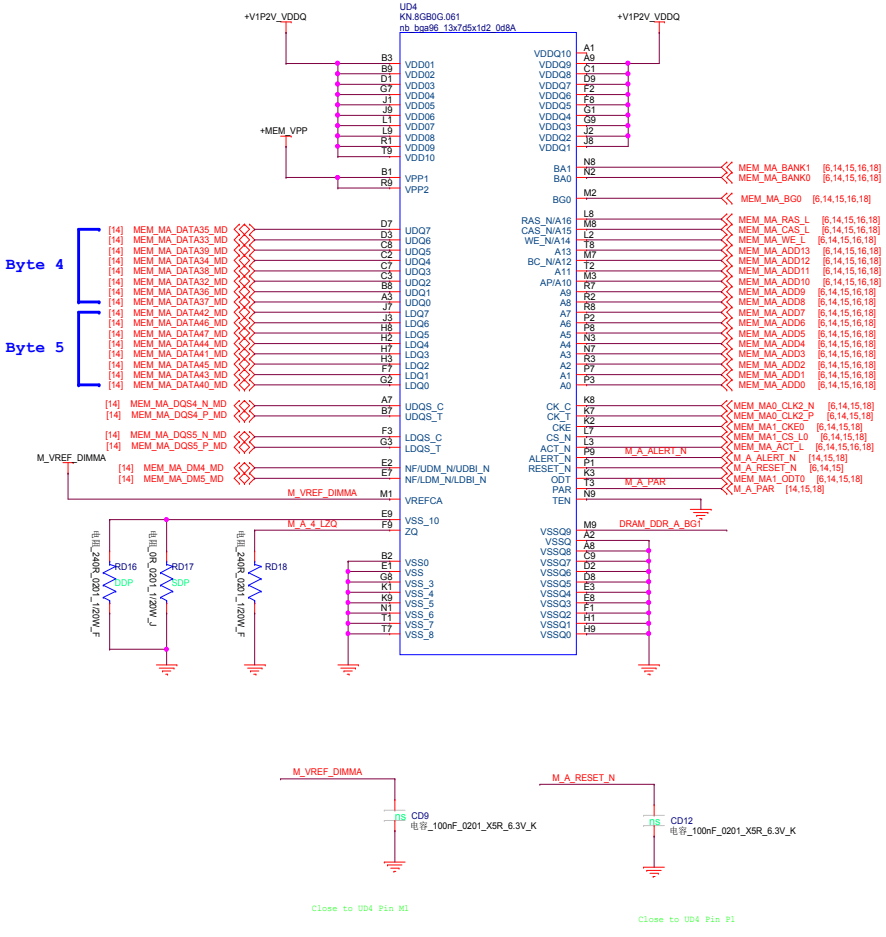

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Page name:	DDR4 CH-A(DEVICE0)	
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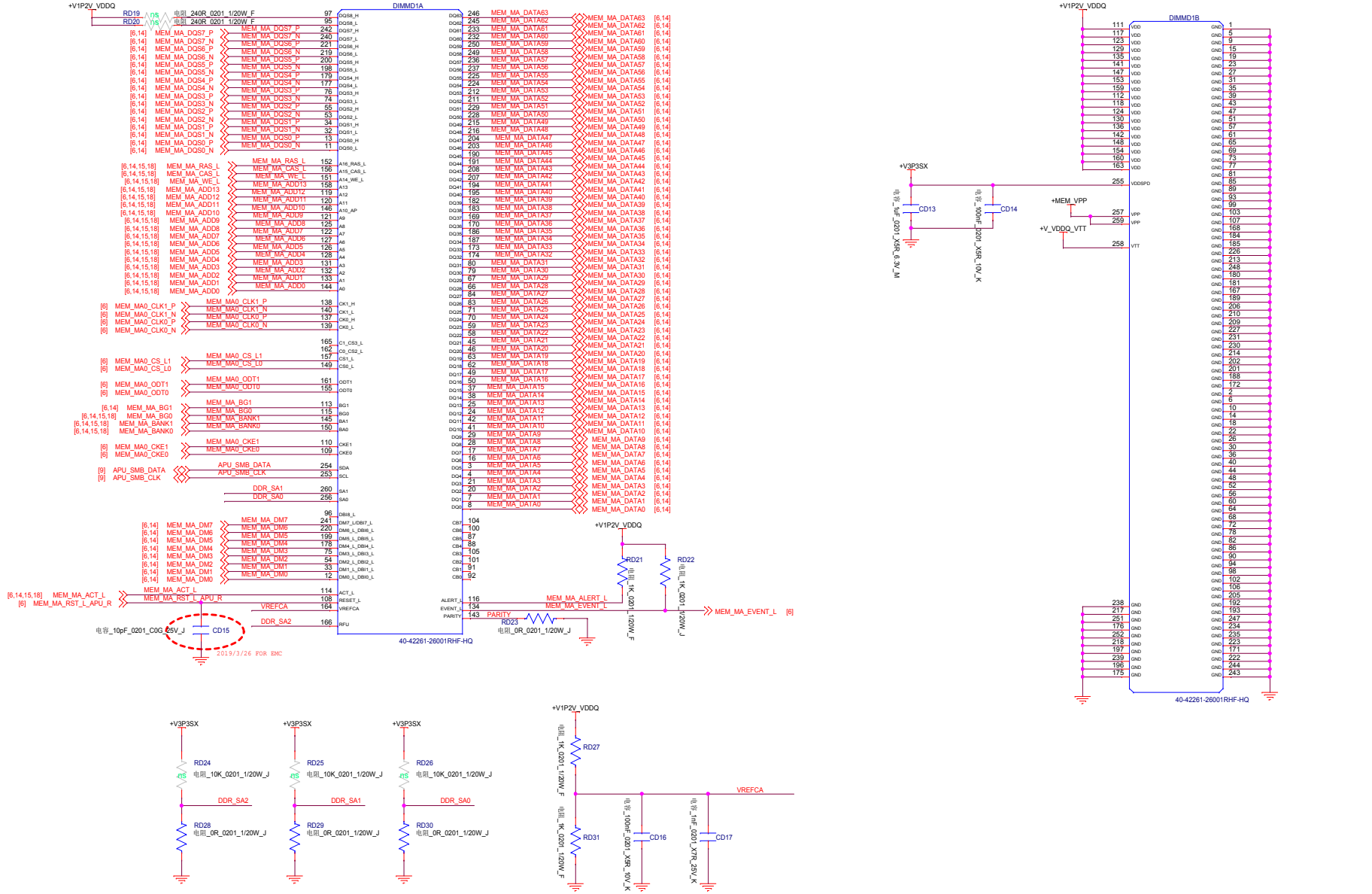

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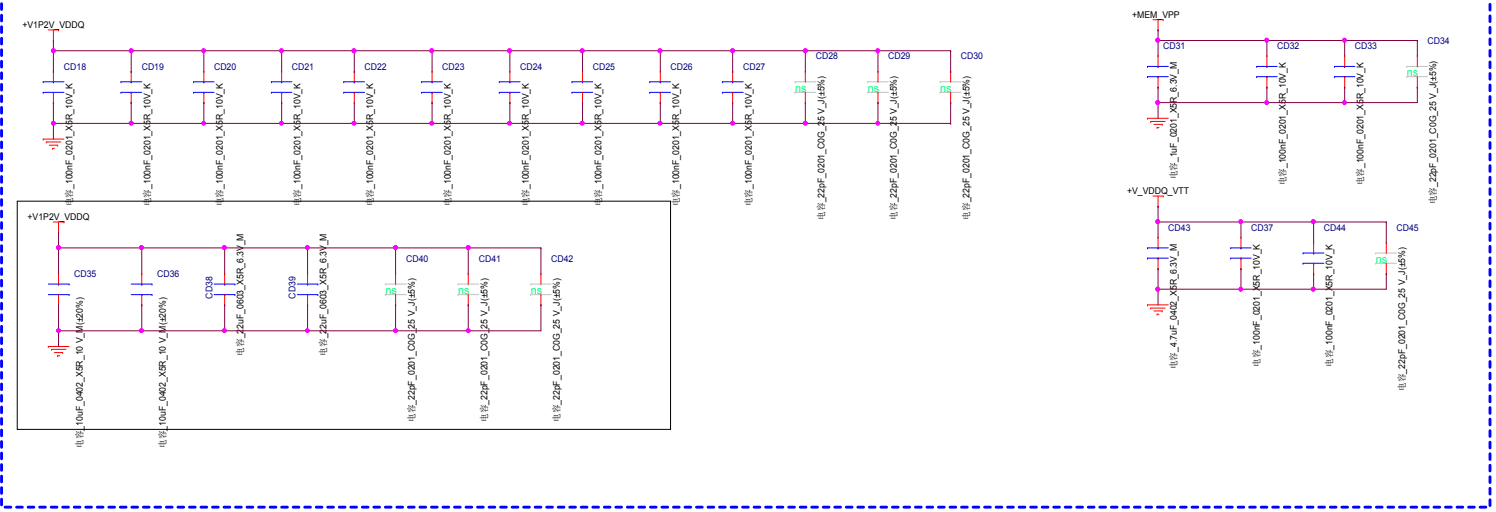
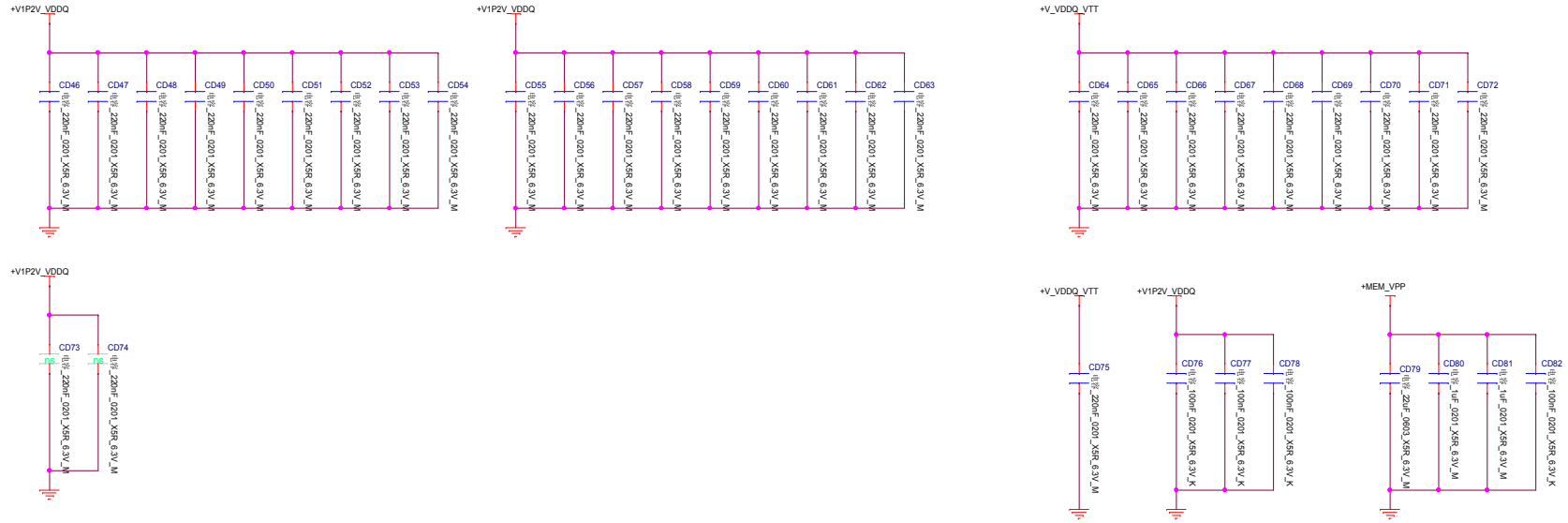
Layout Note: Place near SODIMM



DECOUPLING CAPACITORS FOR MEMORY DOWN



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Page name:	MEM_DECAPS	
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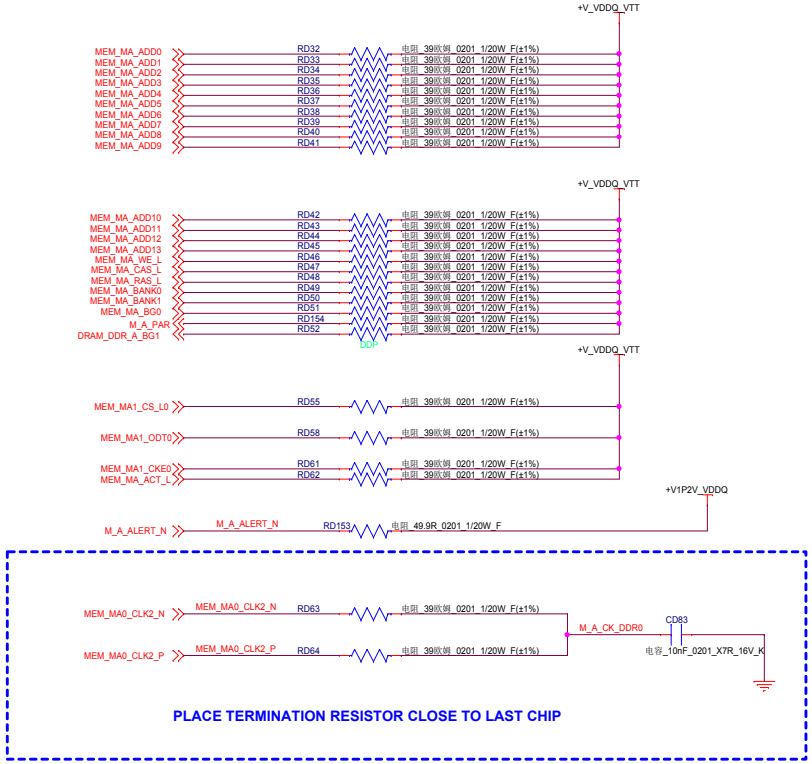
MEMORY TERMINATIONS FOR MEMORY DOWN



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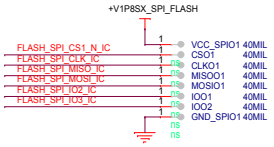
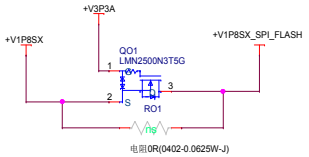
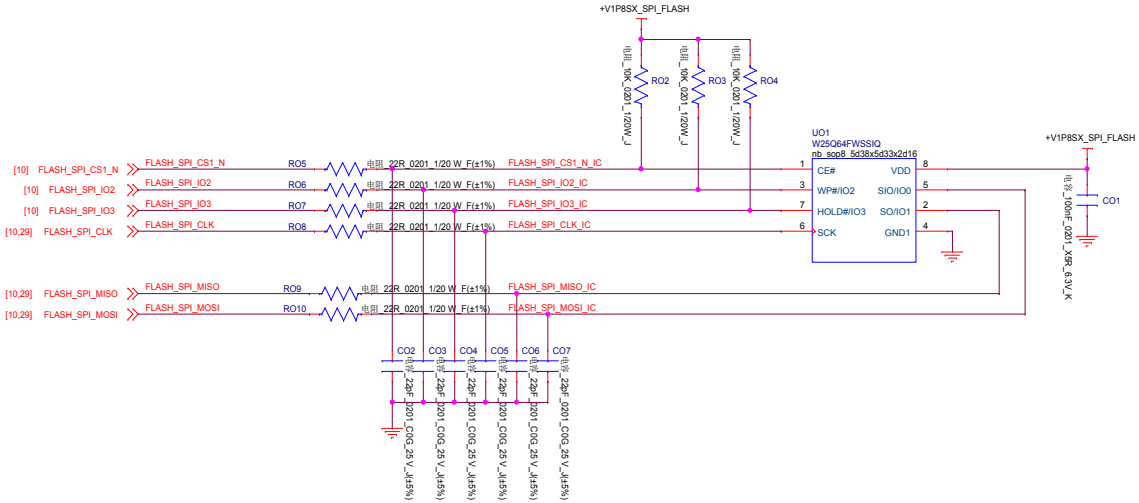
FOR product line







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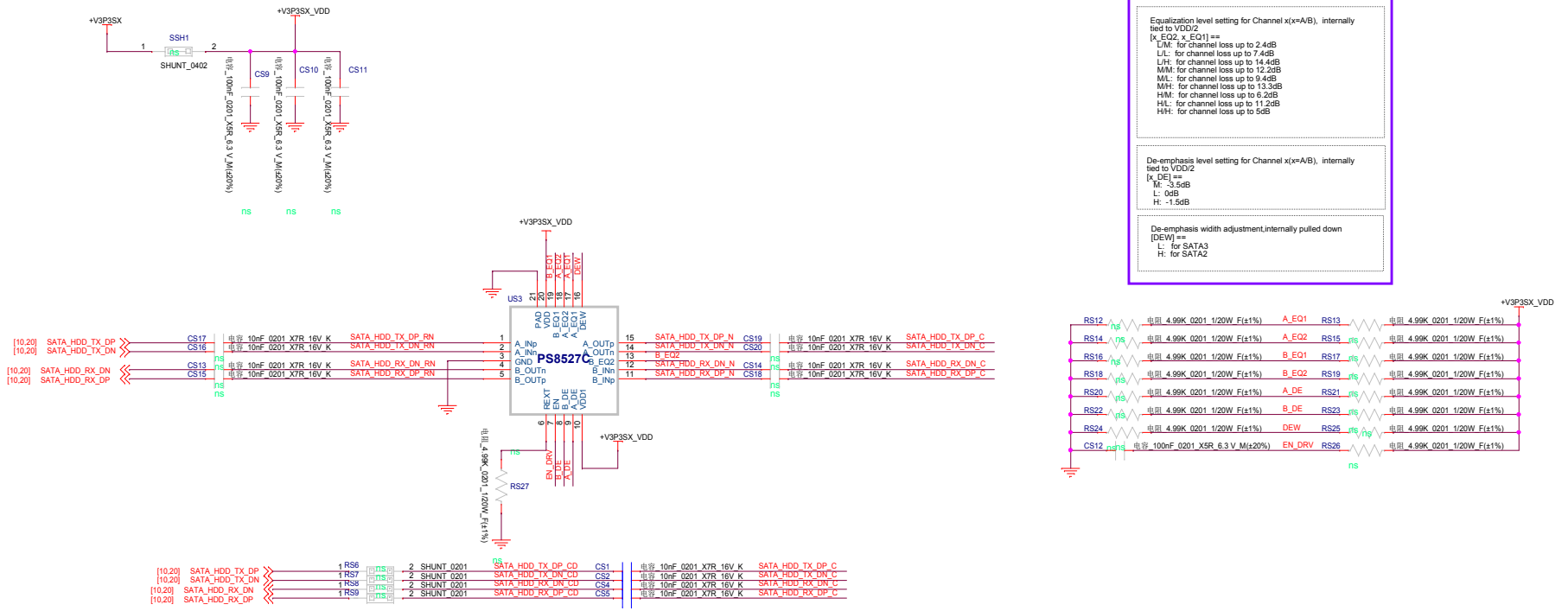
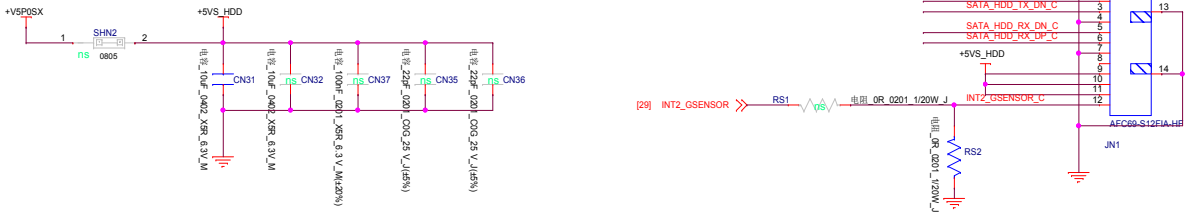
SATA Redriver IC



SATA HDD CONN



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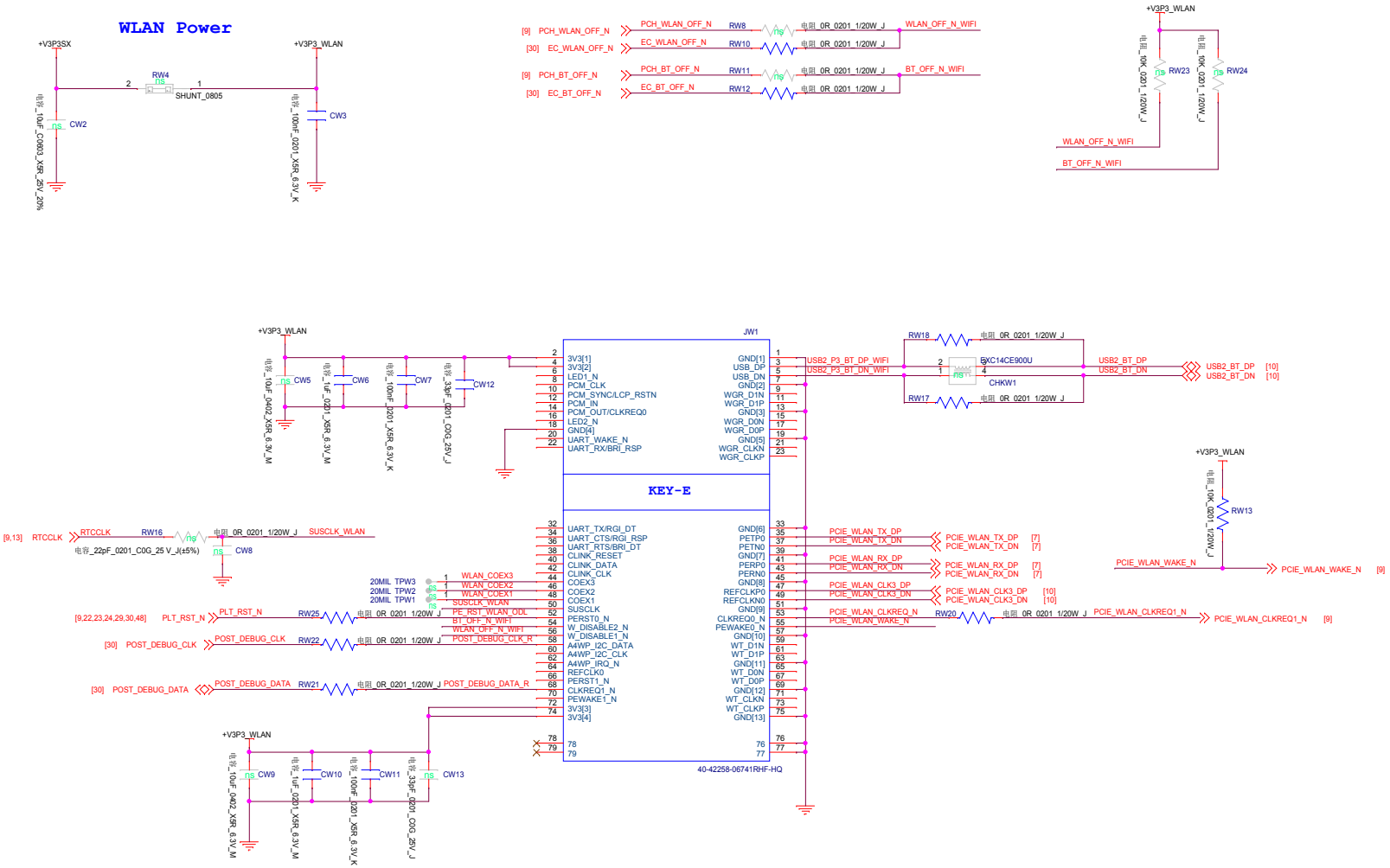
WLAN



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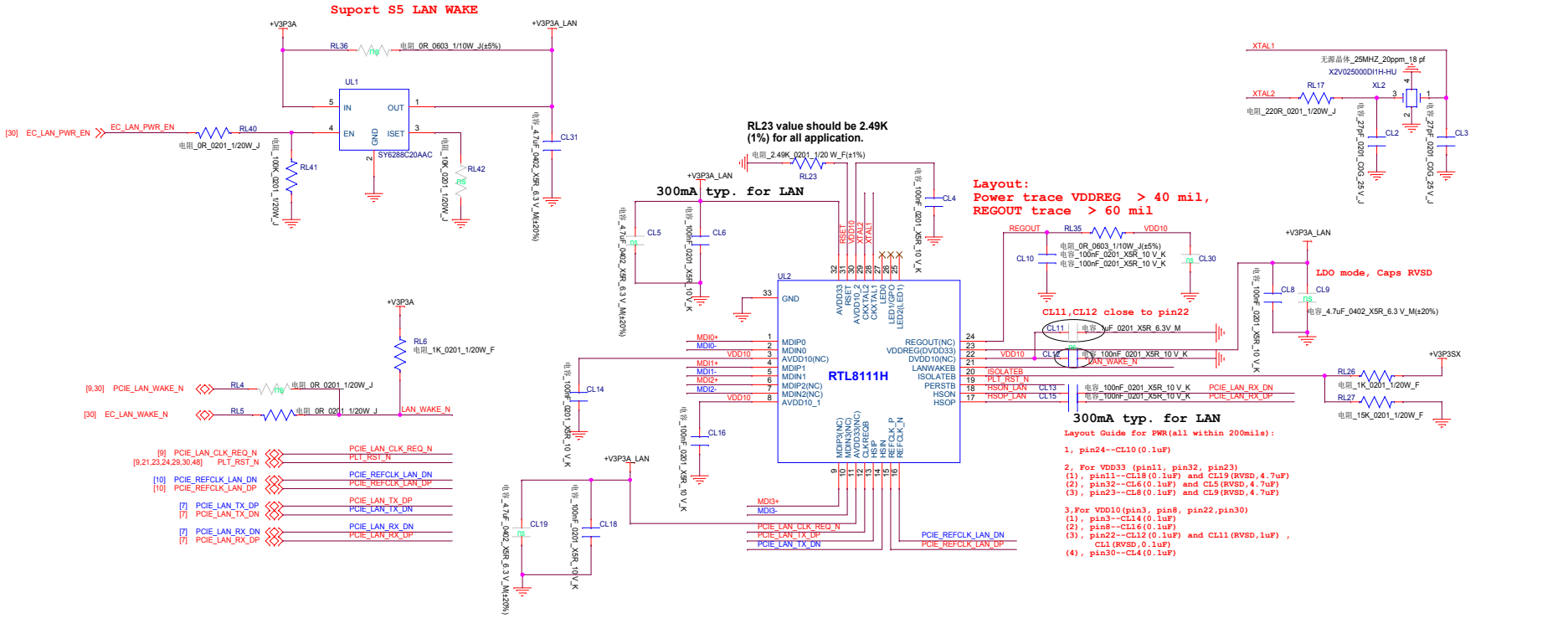
LAN IC RTL8111H



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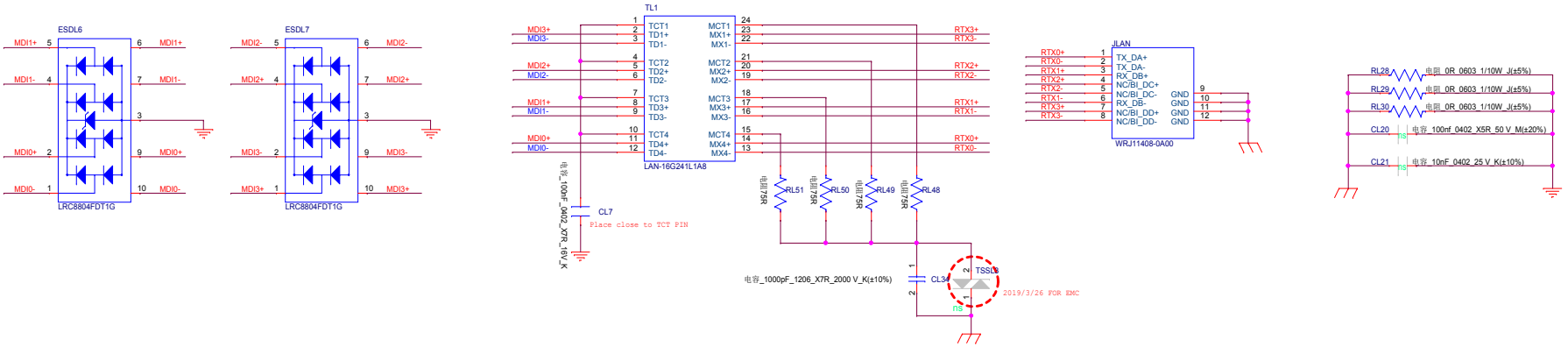

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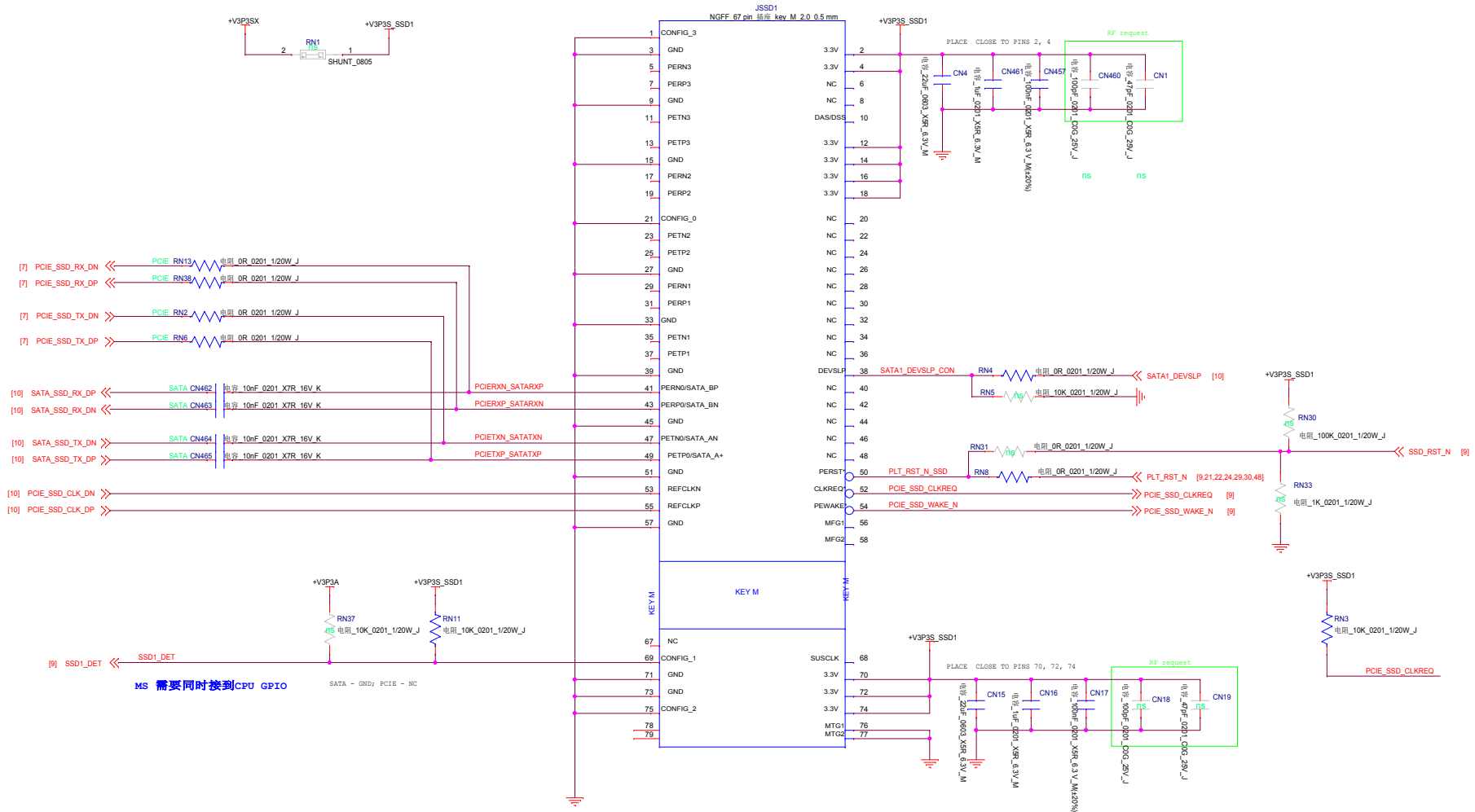
SSD CONN



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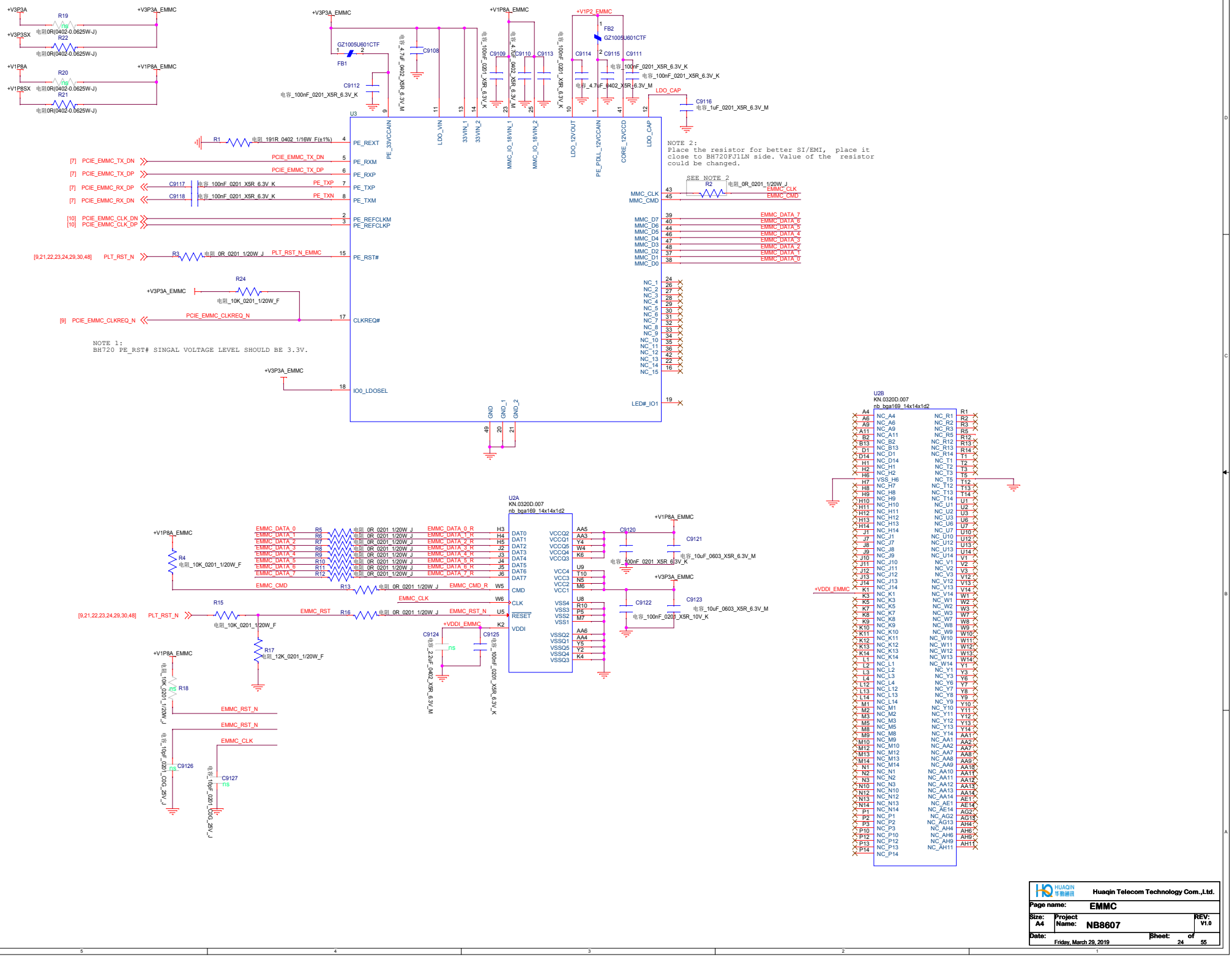

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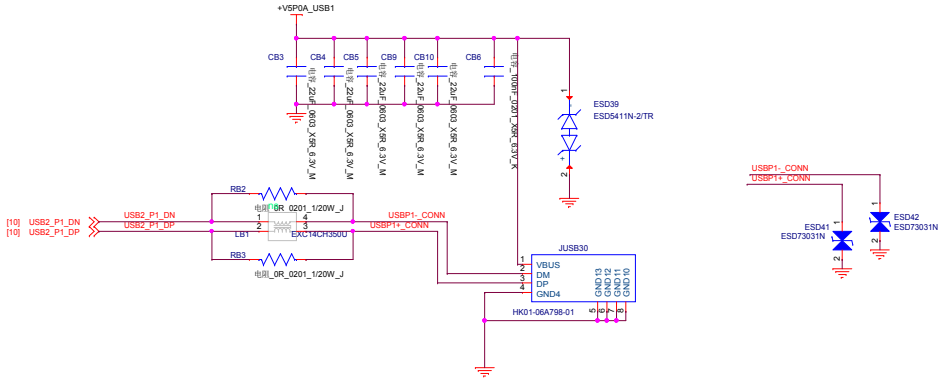
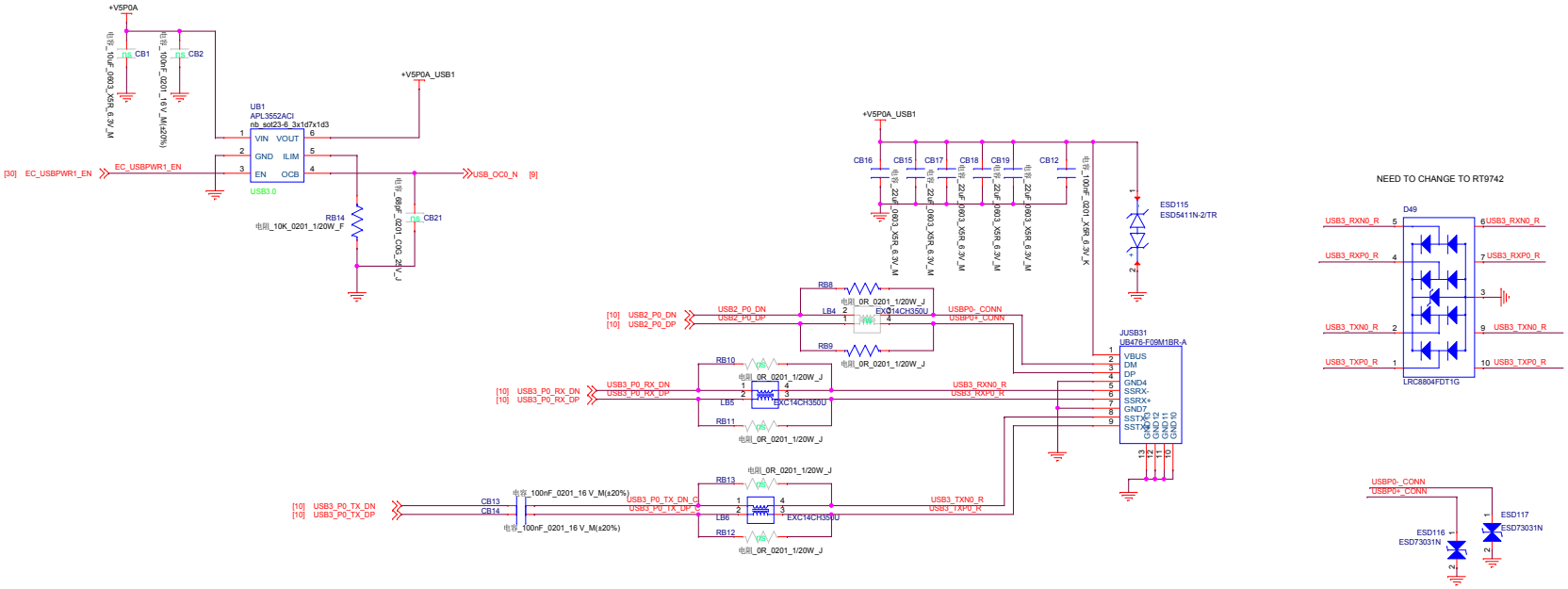
USB2.0 CONN



USB3.0 CONN



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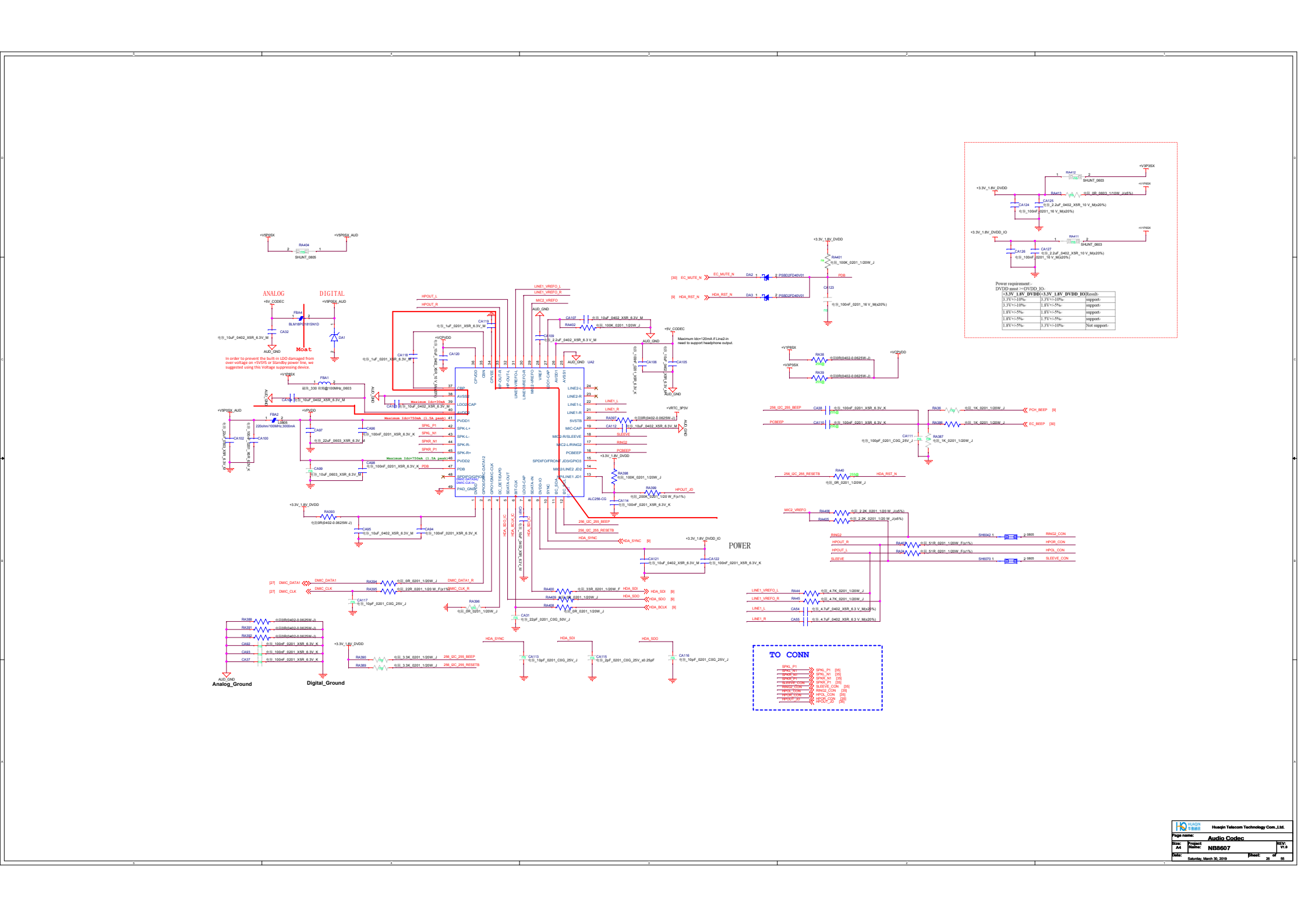
ANALOG
DIGITAL
POWER
Moat
In order to prevent the built-in LDO damaged from over-voltage on +5V/3V5 or Standby power line, we suggested using this Voltage suppressing device.
Maximum Idc=120mA if Line2-in need to support headphone output.
Analog_Ground
Digital_Ground
TO CONN
Power requirement:
DVDD must >=DVDD_IO.
+3.3V_1.8V_DVDD
+3.3V_1.8V_DVDD_IO
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Audio Codec
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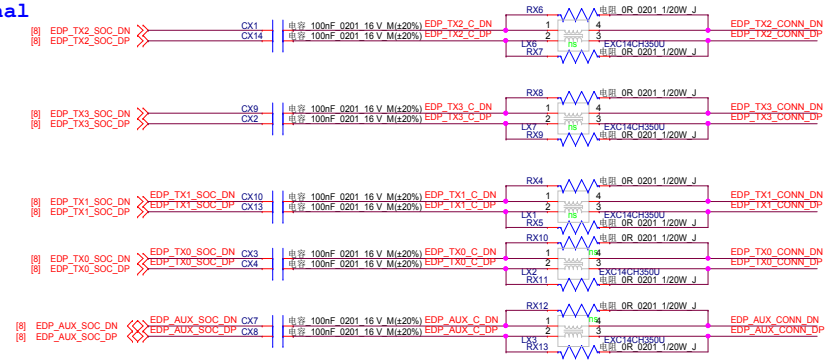
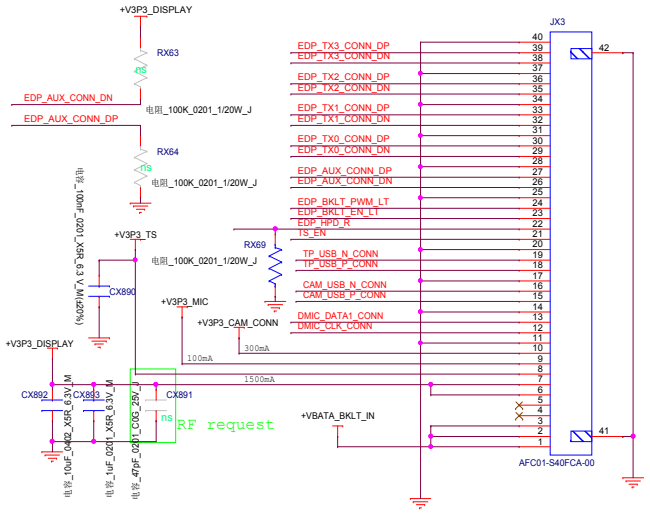
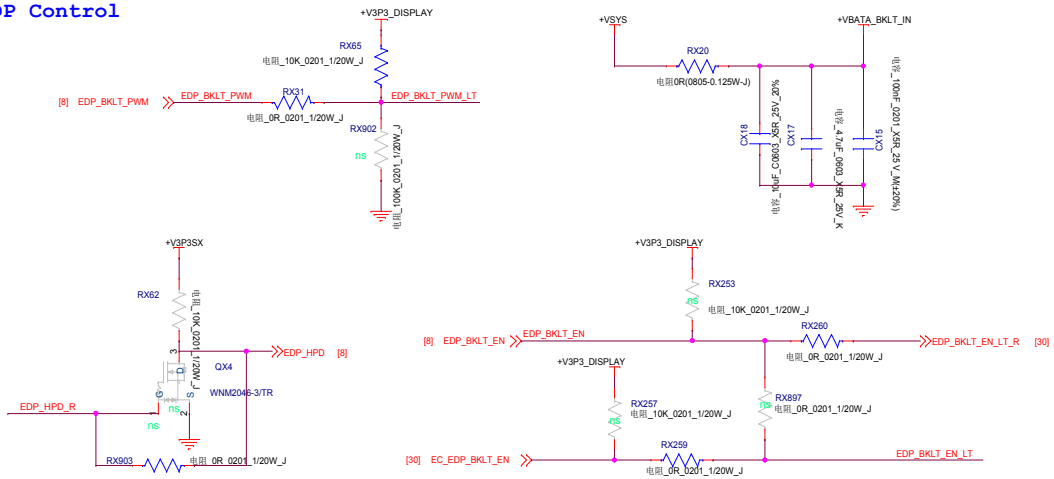
eDP Signal



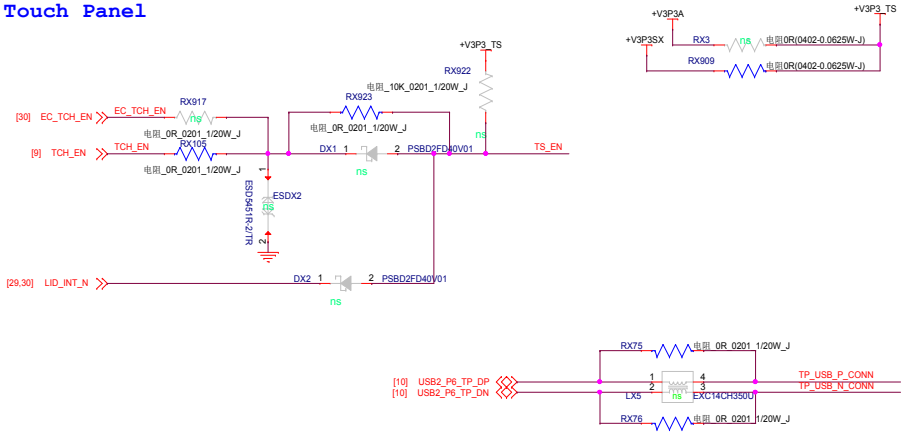
eDP & CAM & DMIC & Touch Panel CONN



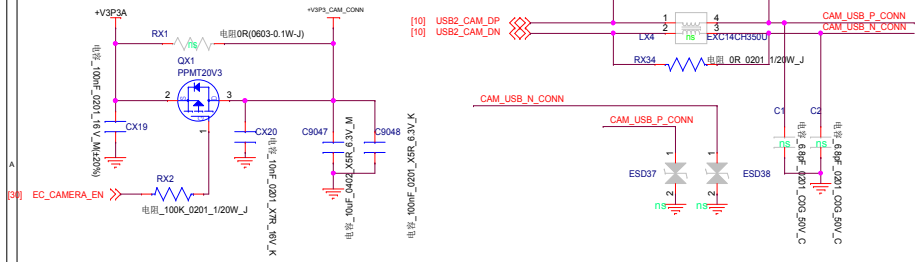
eDP Control



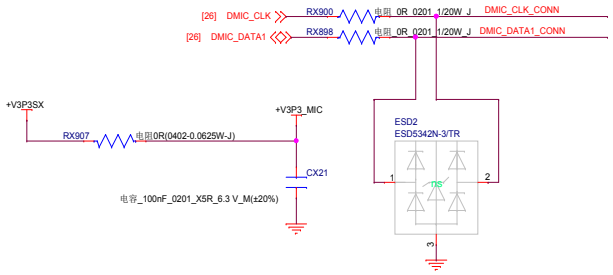
Touch Panel



CAM Power



MIC



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Page name:	EDP &CAM&MIC	
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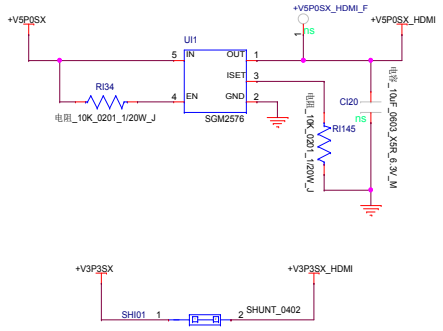
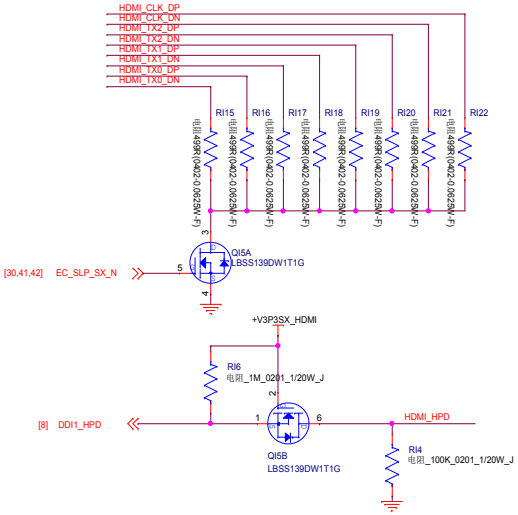
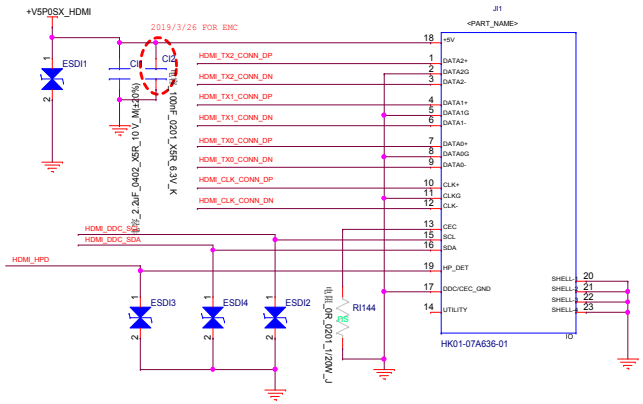
HDMI power

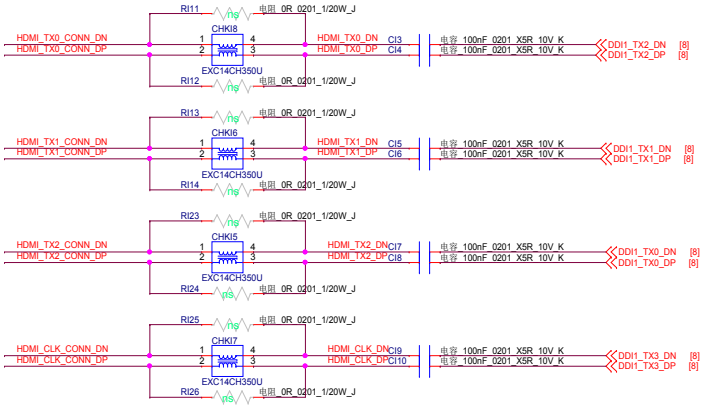




HDMI CONN



Signal



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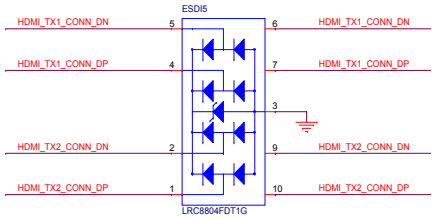

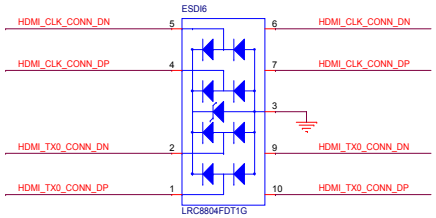

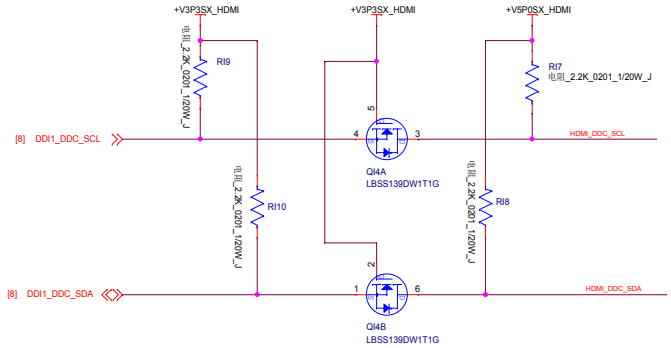

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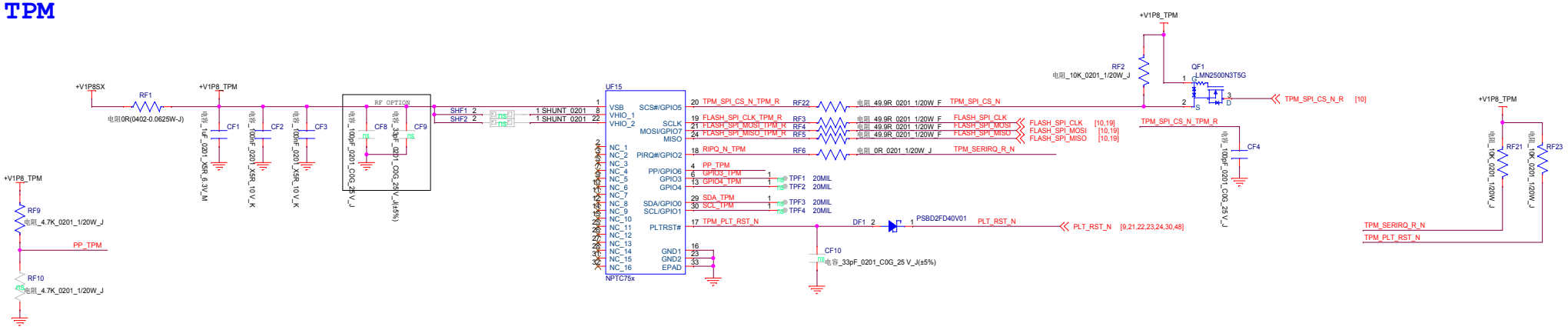
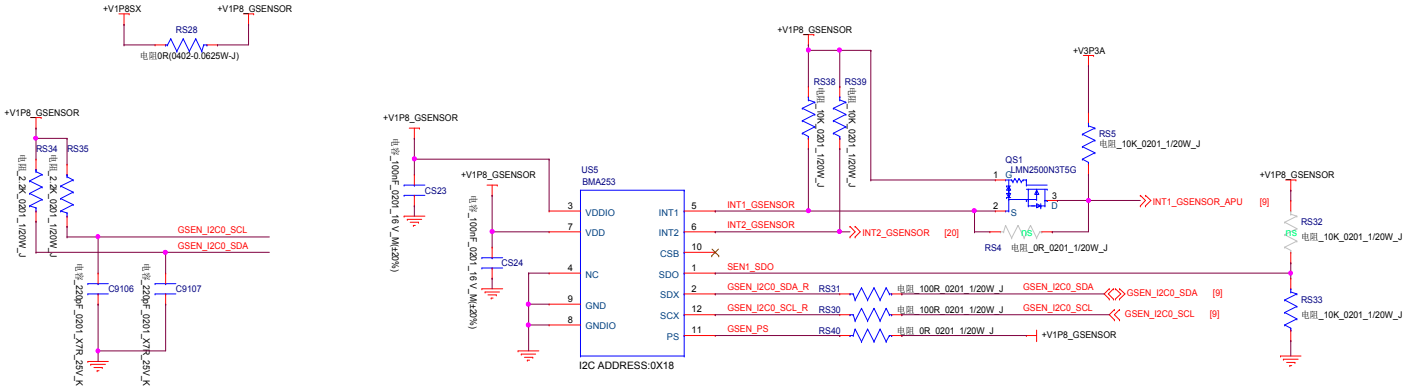
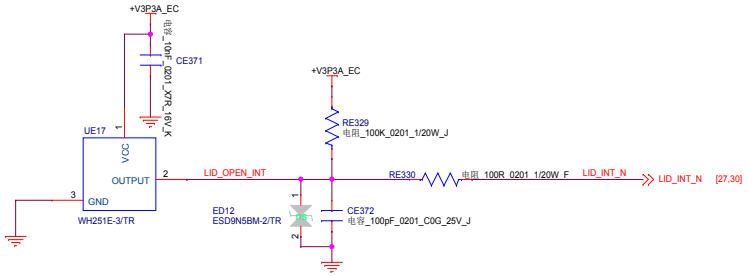
TPM



G-SENSOR



Hall-SENSOR



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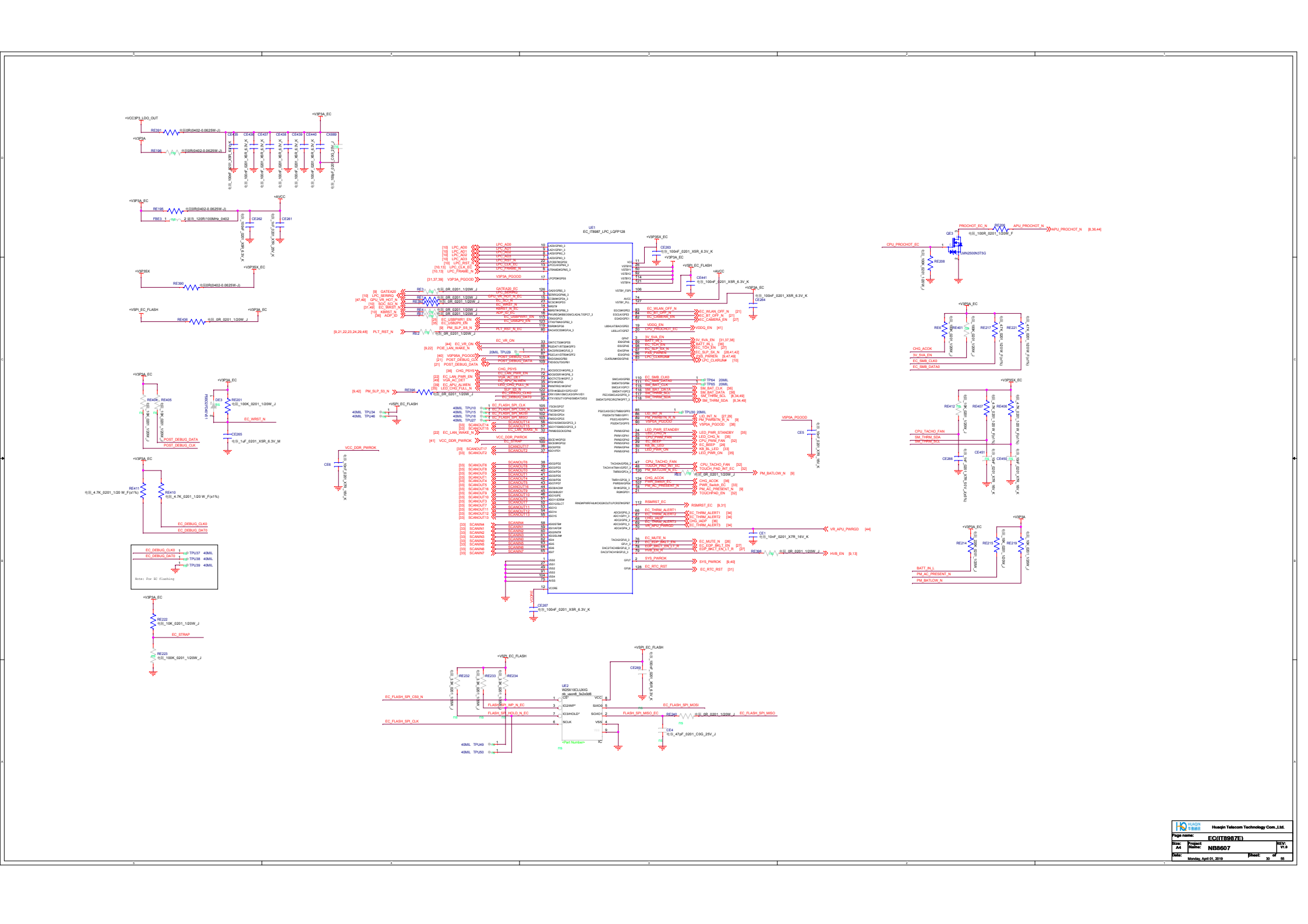

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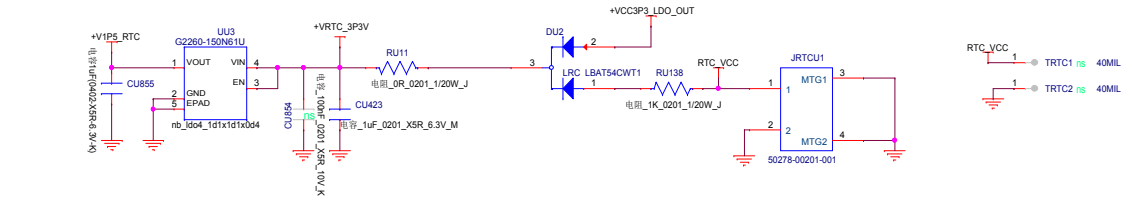

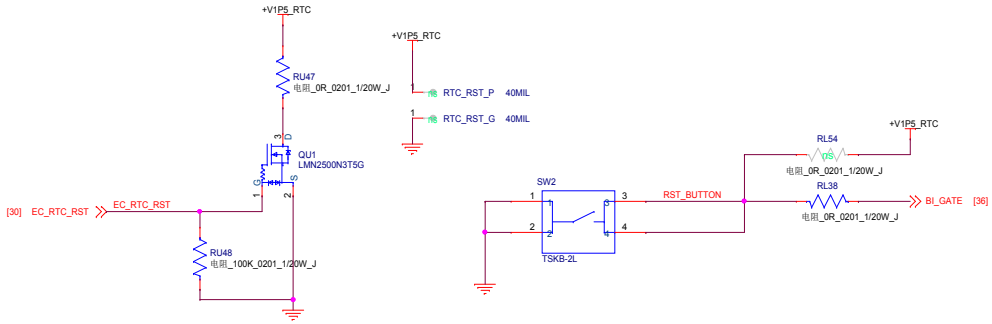

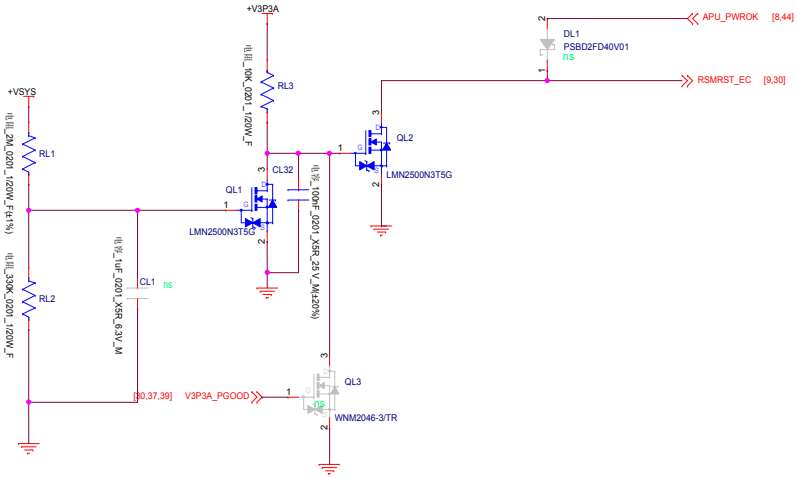

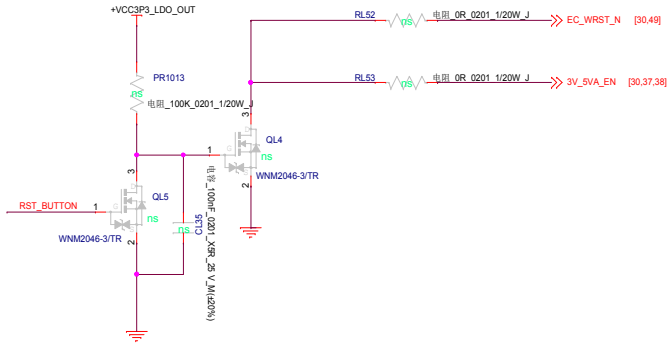

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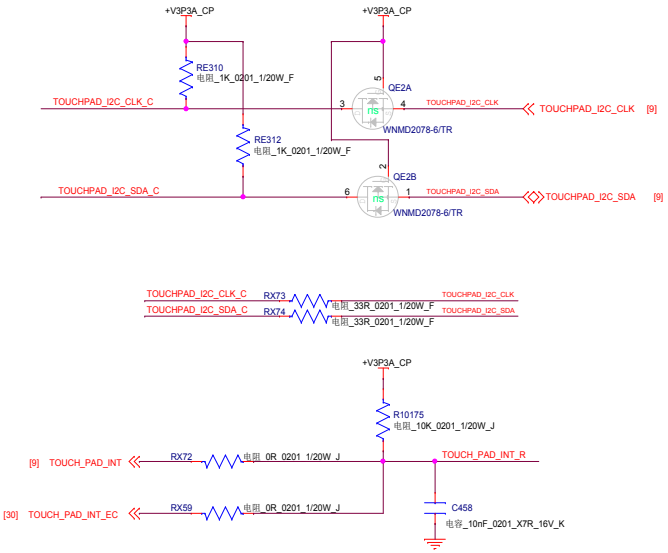
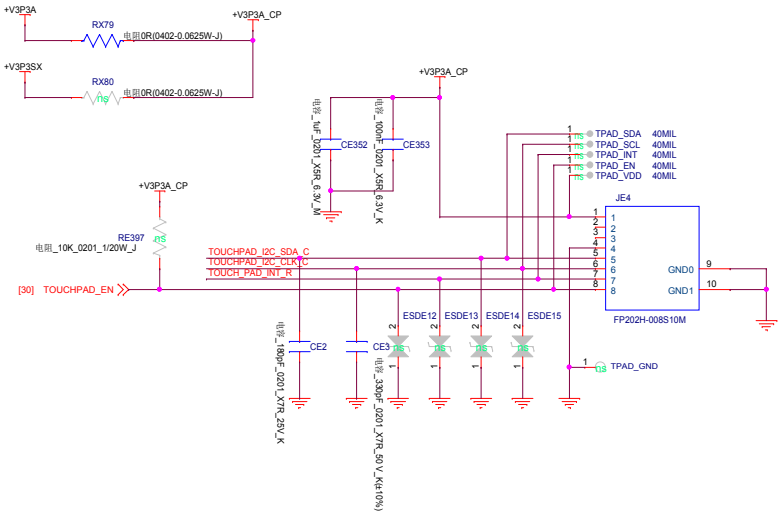
TOUCH PAD





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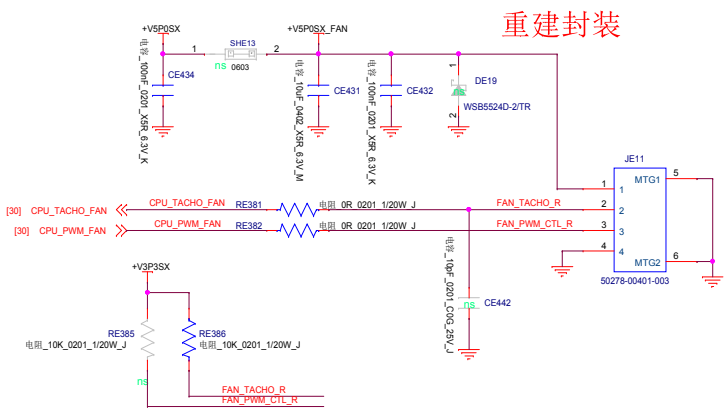

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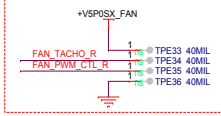

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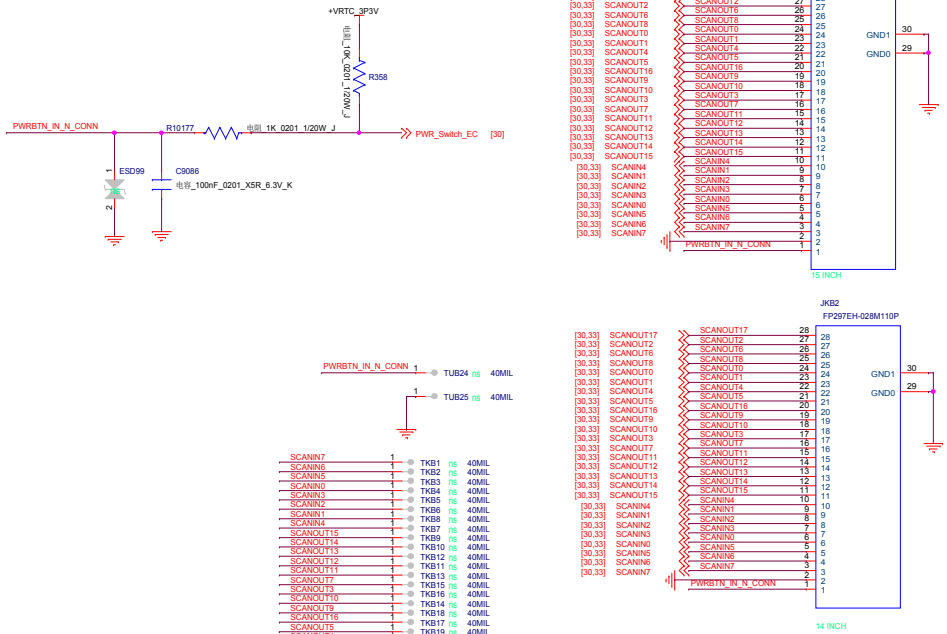
KB CONN



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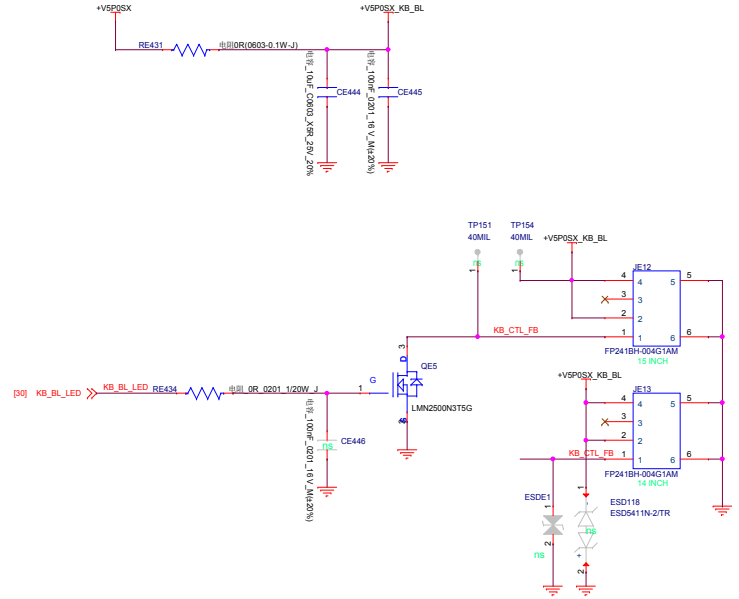

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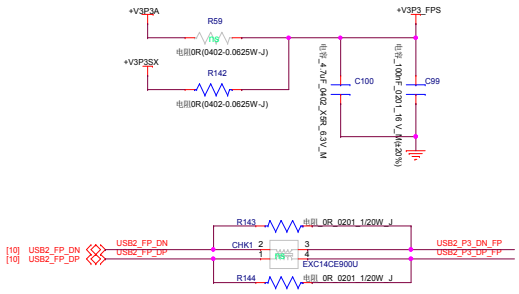

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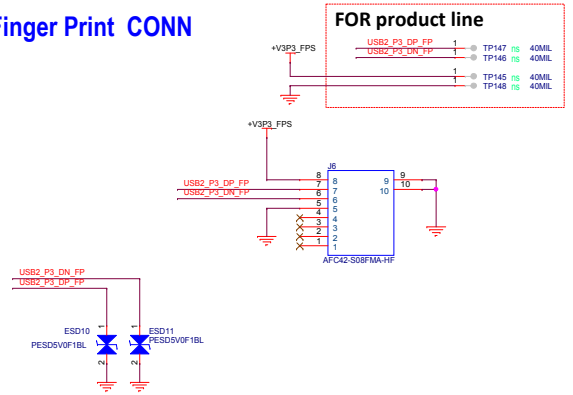

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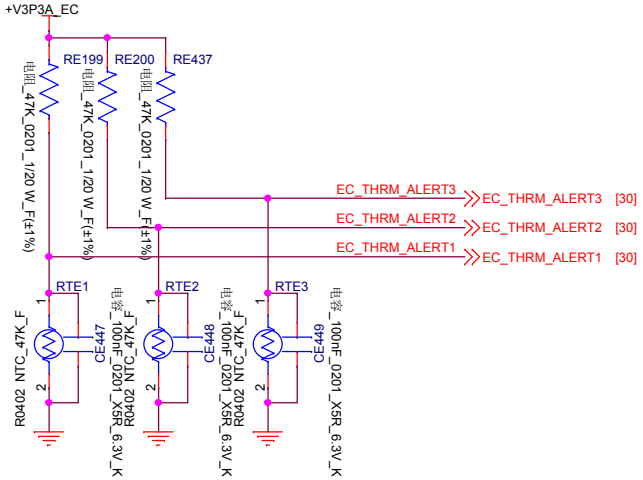
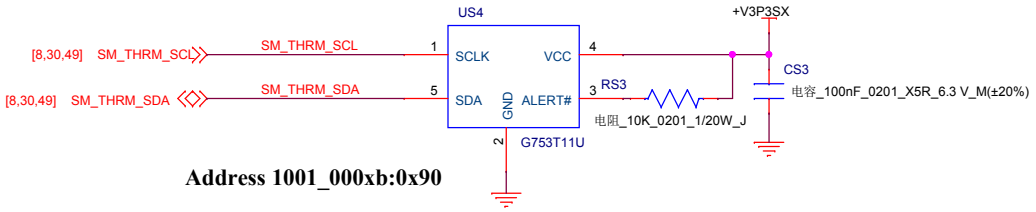
Thermal sensor





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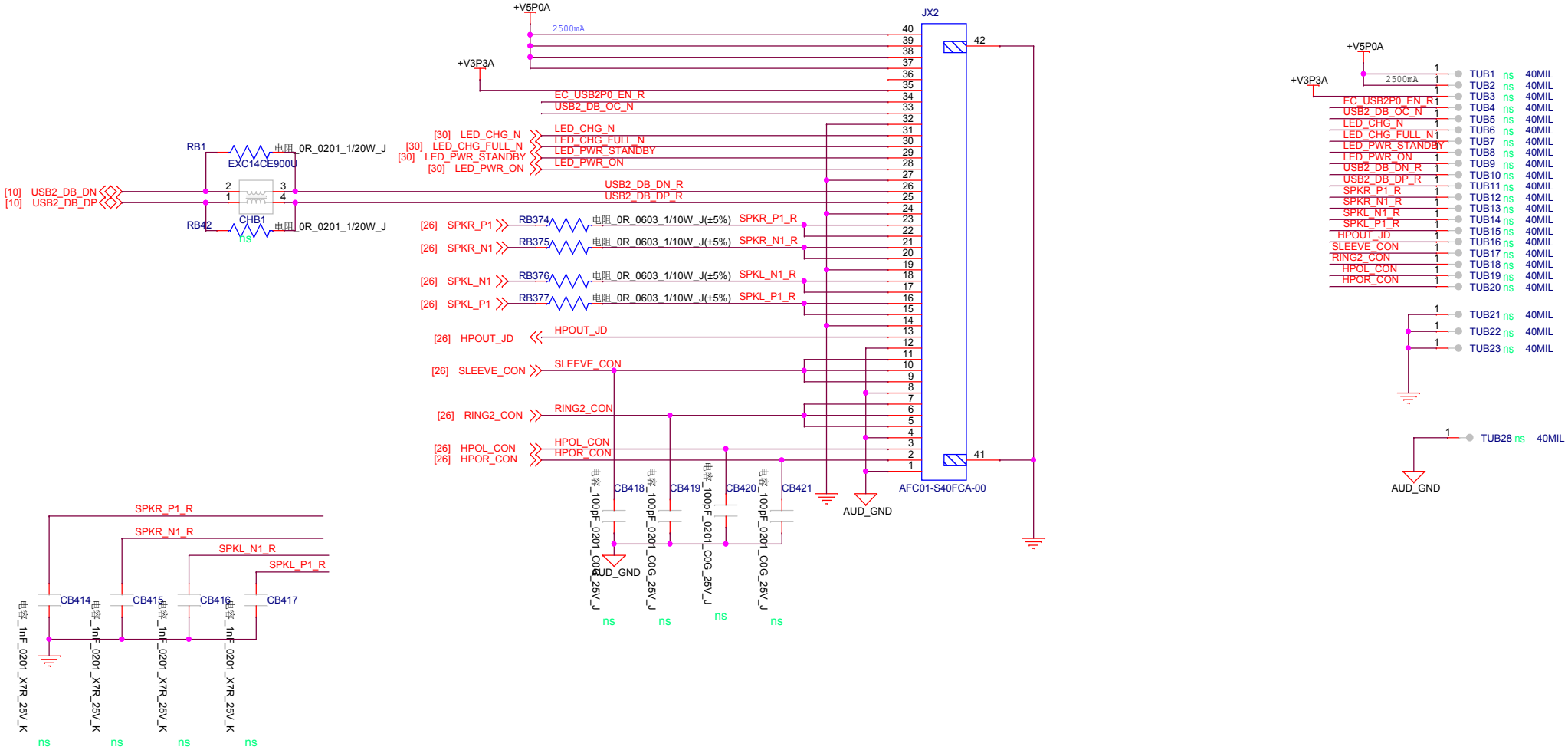
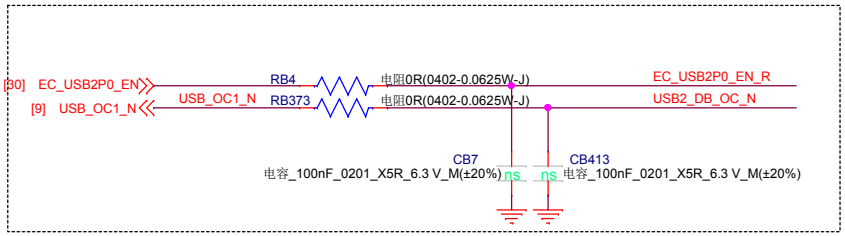
IO Board Conn





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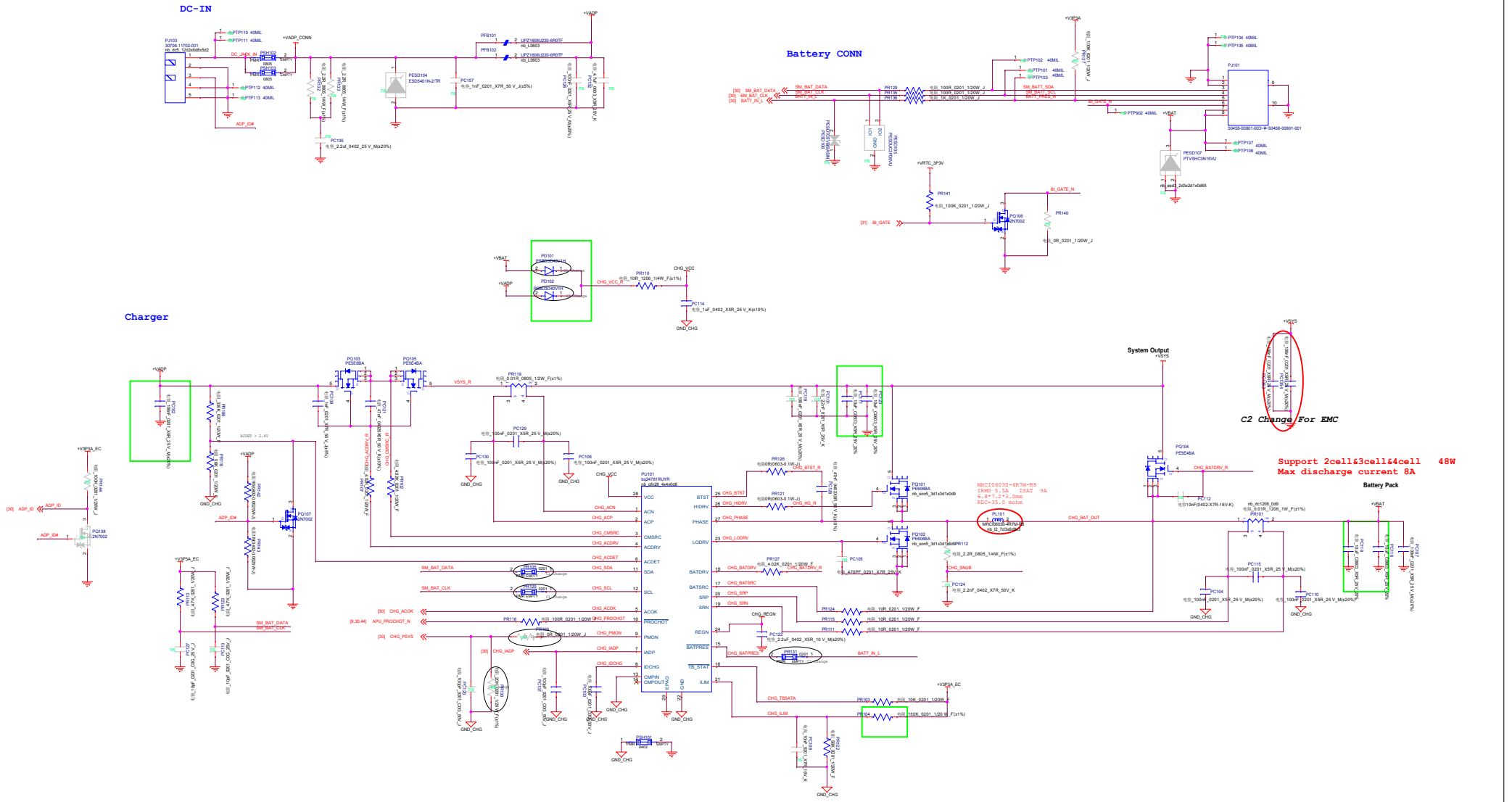
DC-IN
Battery CONN
Charger
System Output
Battery Pack
C2 Change For EMC
Support 2cell&3cell&4cell 48W
Max discharge current 8A
Huaqin Telecom Technology Com.,Ltd.
Page name: BATTERY CHARGER
Size: A4
Project Name: NB8607
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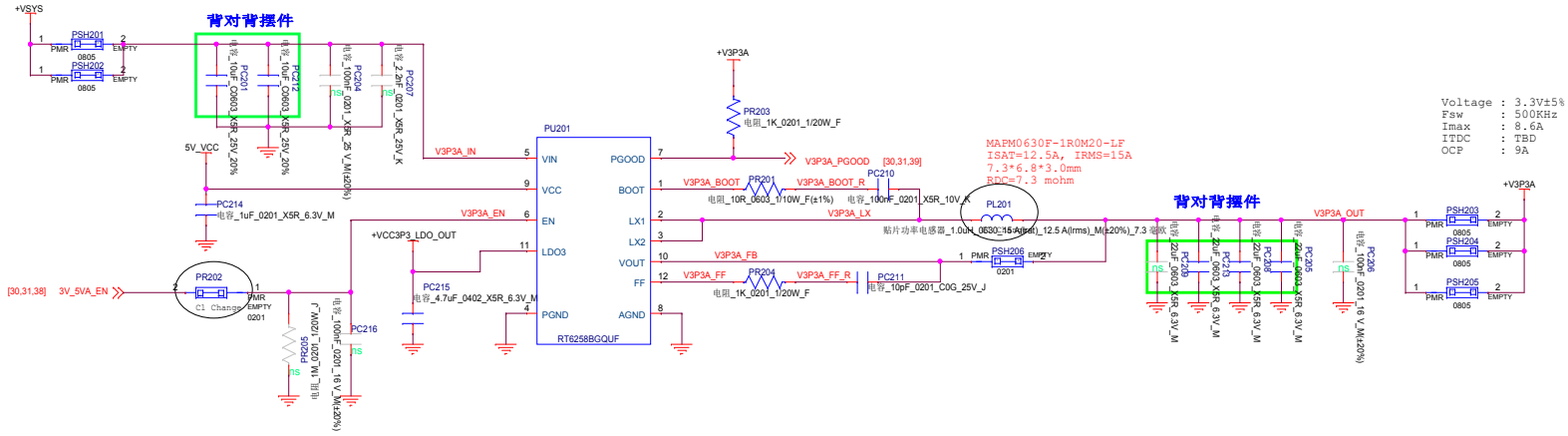
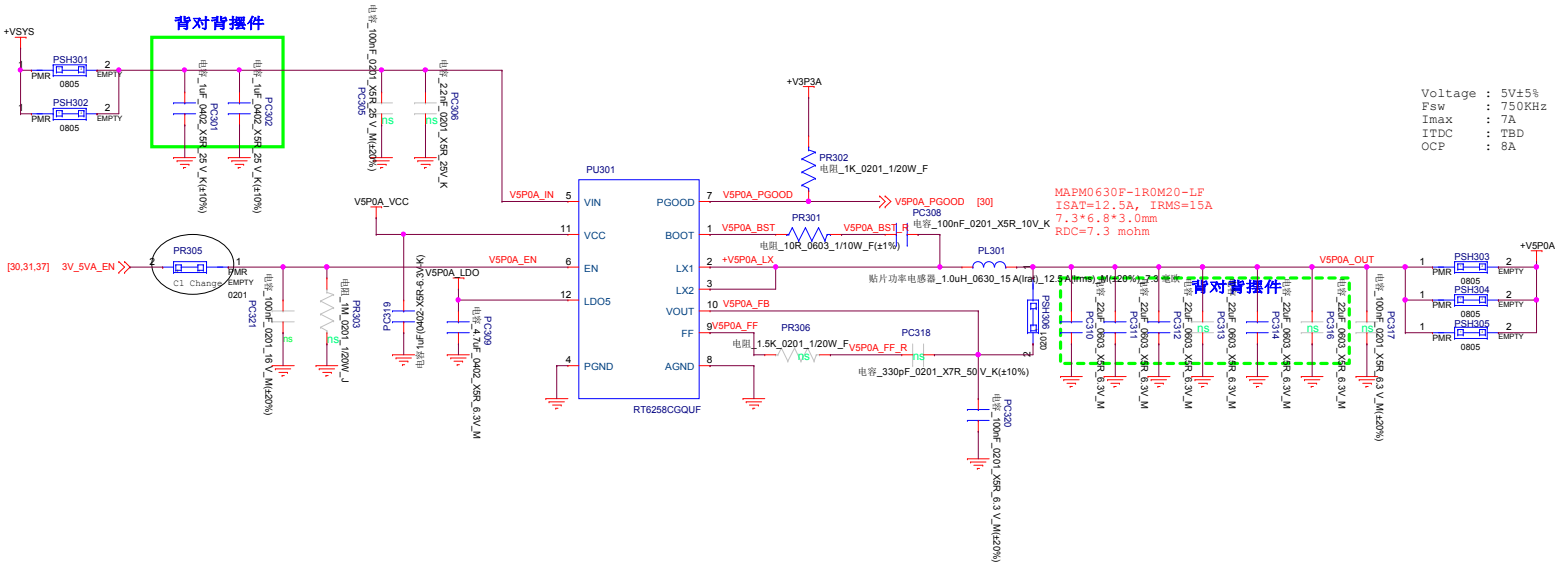
+V3P3A

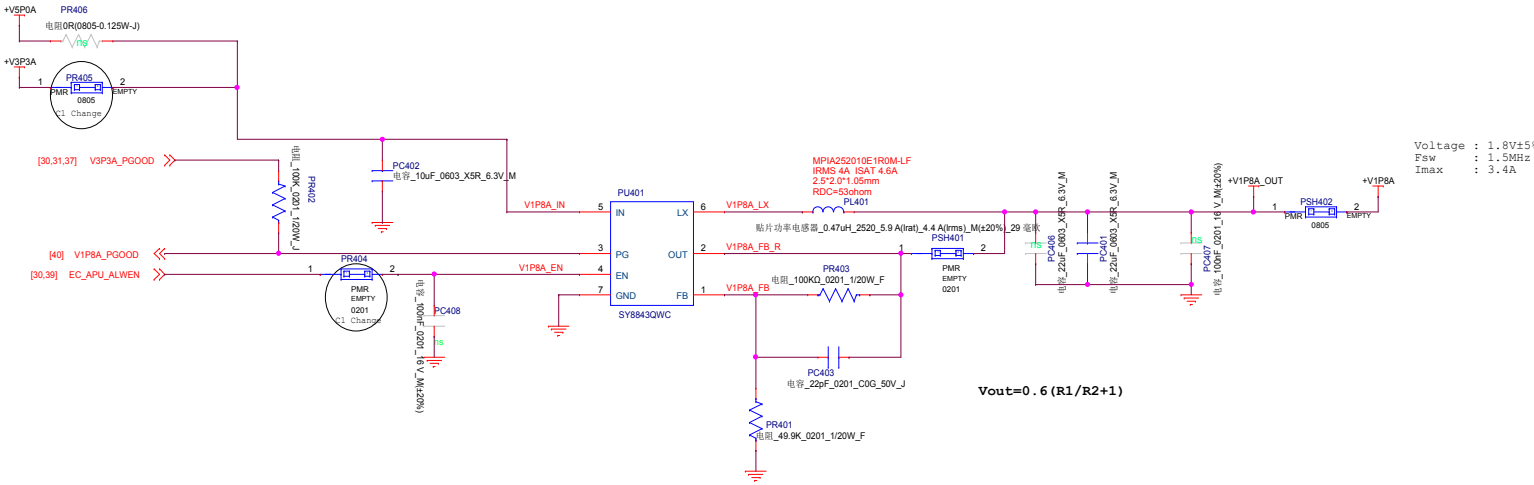


Huaqin Telecom Technology Com.,Ltd.			
Page name:	POWER DELIVERY 3.3V		
Size: A4	Project Name: NB8607		REV: V1.0
Date: Friday, March 29, 2019		Sheet: 37	of 55

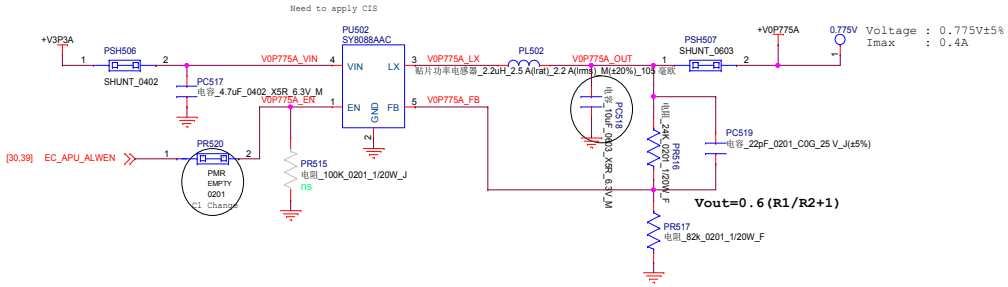


Huaqin Telecom Technology Com.,Ltd.			
Page name:	POWER DELIVERY 5V		
Size: A4	Project Name: NB8607		REV: V1.0
Date: Friday, March 29, 2019		Sheet: 38	of 55

+V1P8A

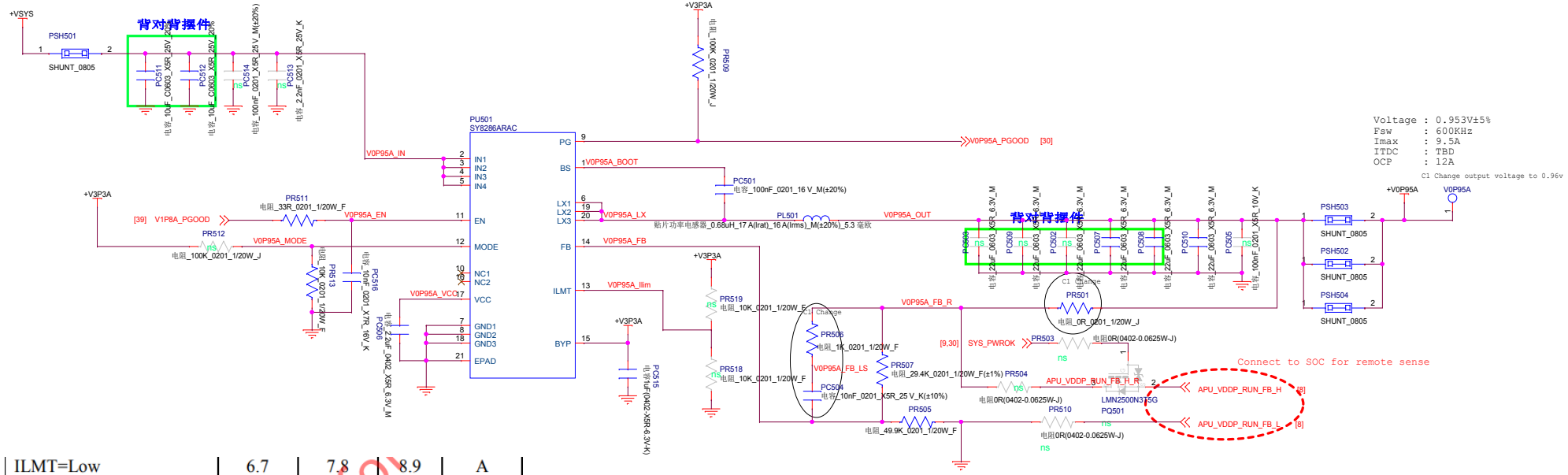


+V0P775A



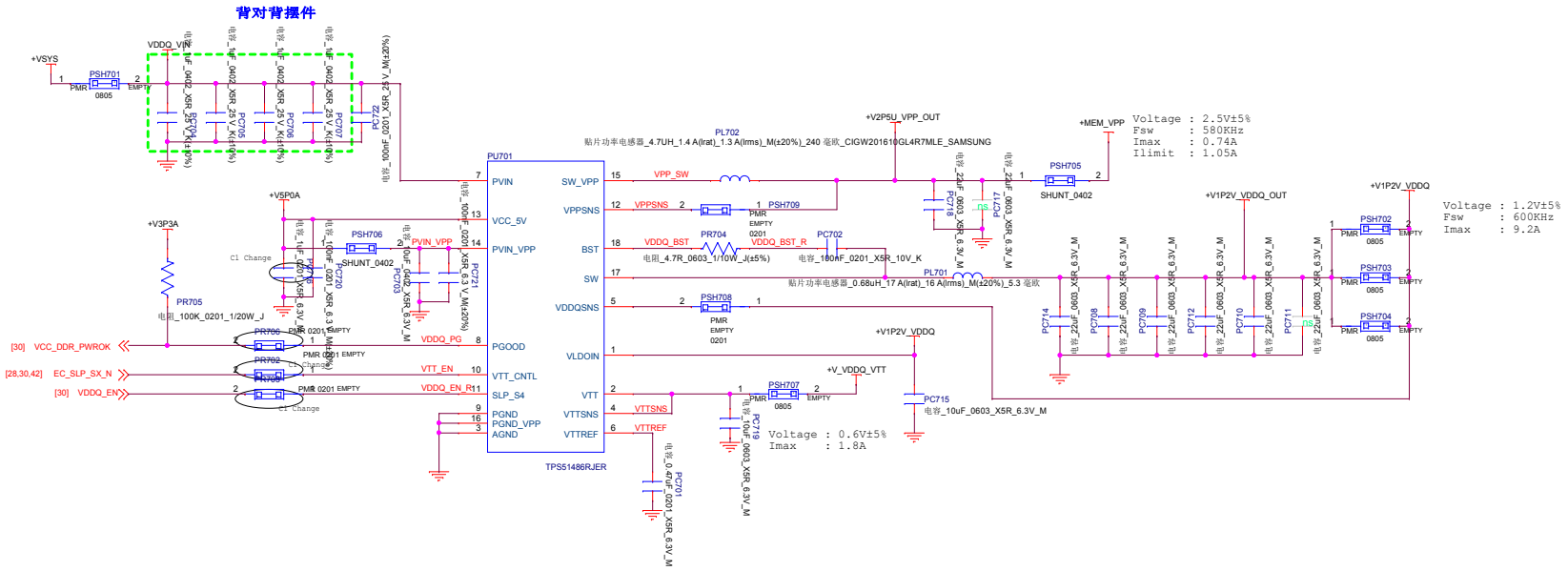
Huaqin Telecom Technology Com.,Ltd.		
Page name:	POWER DELIVERY 1.8V/0.775A	
Size: A4	Project Name: NB8607	REV: V1.0
Date: Friday, March 29, 2019	Sheet: 39 of 55	

+V0P95A

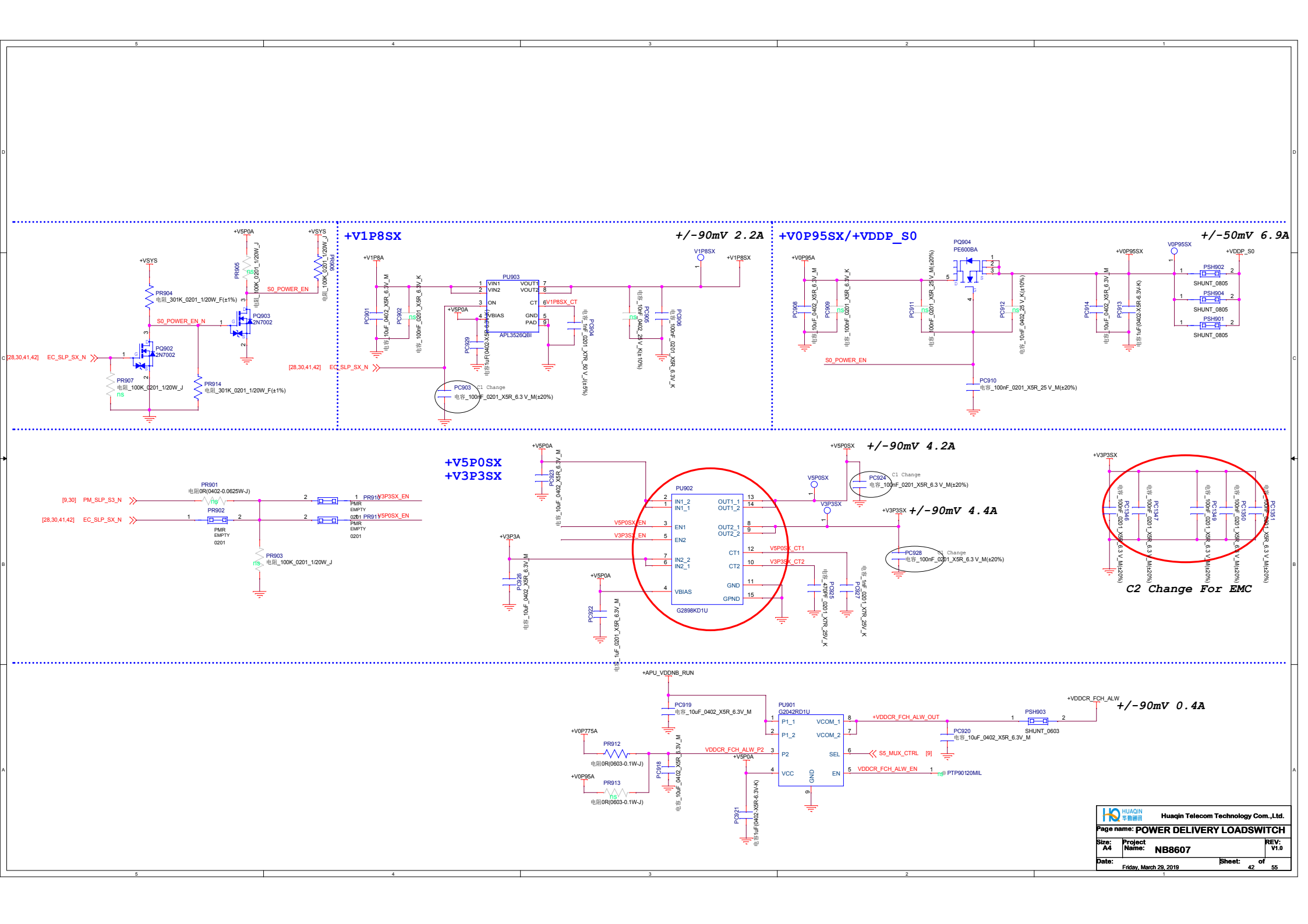


ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A

Huaqin Telecom Technology Com.,Ltd.		
Page name: POWER DELIVERY 0.95V		
Size: A4	Project Name: NB8607	REV: V1.0
Date: Friday, March 29, 2019	Sheet: 40 of 55	



Huaqin Telecom Technology Com.,Ltd.			
Page name: POWER DELIVERY 1.2V & 2.5V			
Size: A4	Project Name: NB8607		REV: V1.0
Date: Friday, March 29, 2019		Sheet: 41	of 55


+V1P8SX
+/-90mV 2.2A
+V0P95SX/+VDDP_S0
+/-50mV 6.9A
+V5P0SX
+V3P3SX
+/-90mV 4.2A
+/-90mV 4.4A
C2 Change For EMC
+/-90mV 0.4A
S0_POWER_EN
EC_SLP_SX_N
PM_SLP_S3_N
PU902
PU903
PU901
G2898KD1U
APL3526QBI
G2042RD1U
Huaqin Telecom Technology Com.,Ltd.
Page name: POWER DELIVERY LOADSWITCH
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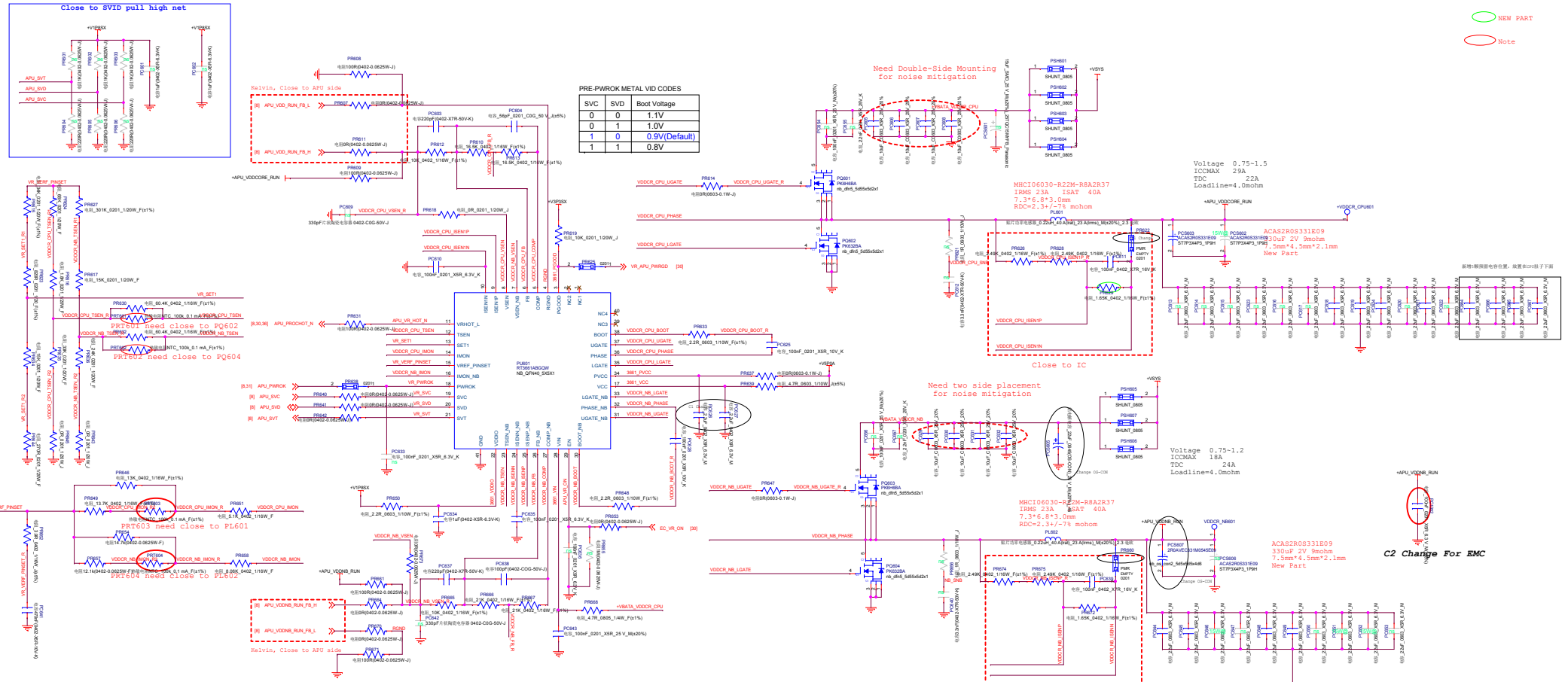
HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.
Page name:	POWER DELIVERY backlight
Size: A4	Project Name: NB8607
REV: V1.0	
Date: Friday, March 29, 2019	Sheet: 43 of 55



Supply [1]	Nominal Voltage (V) [2]	Condition	SYSTEM_CONFIGURATION 10 (25W)	9 (15W)	11 (10W)	12 (6W)
VDDCR_CPU	Variable (0.75–1.5) [13]	TDC [3]	24	22	18	11
		EDC	32	29	24	15
		Max Loadstep [4]	21	20	18	11
VDDCR_NB	Variable (0.75–1.2) [13]	TDC [3]	22	18	15	11
		EDC	29	24	20	15
		Max Loadstep [4]	19	16	13	10
VDDCR_FCH_S5	0.775 [11]	TDC	0.1			
	Variable [12]	TDC	0.4			

Husqin Telecom Technology Com.,Ltd.	
Page name:	CORE & NB
Size: A4	Project Name: NB8607
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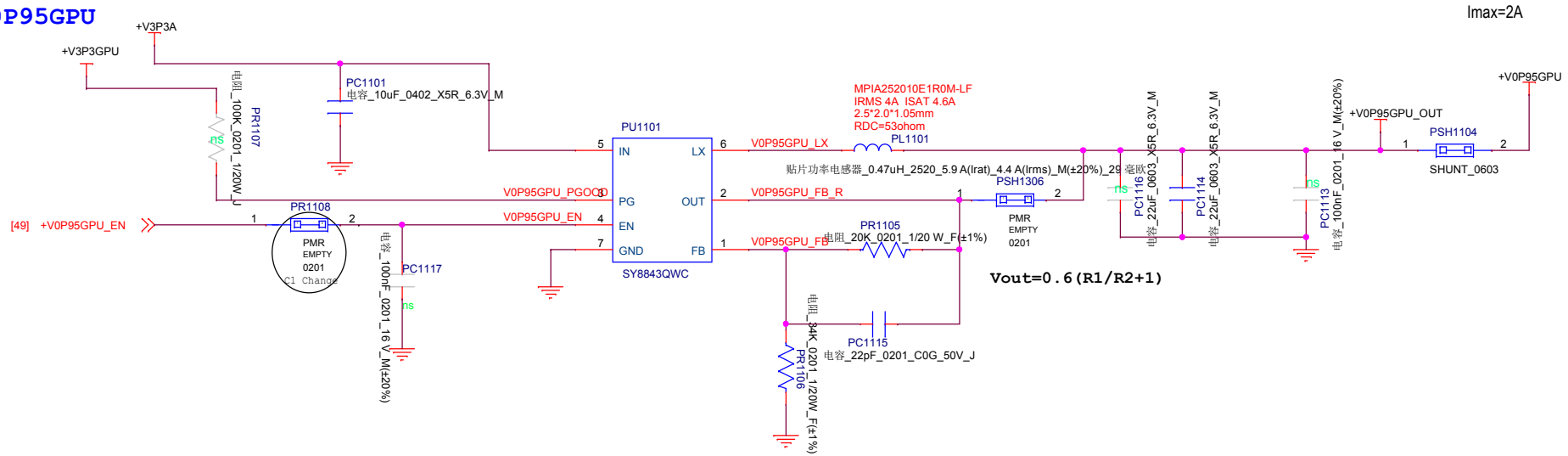
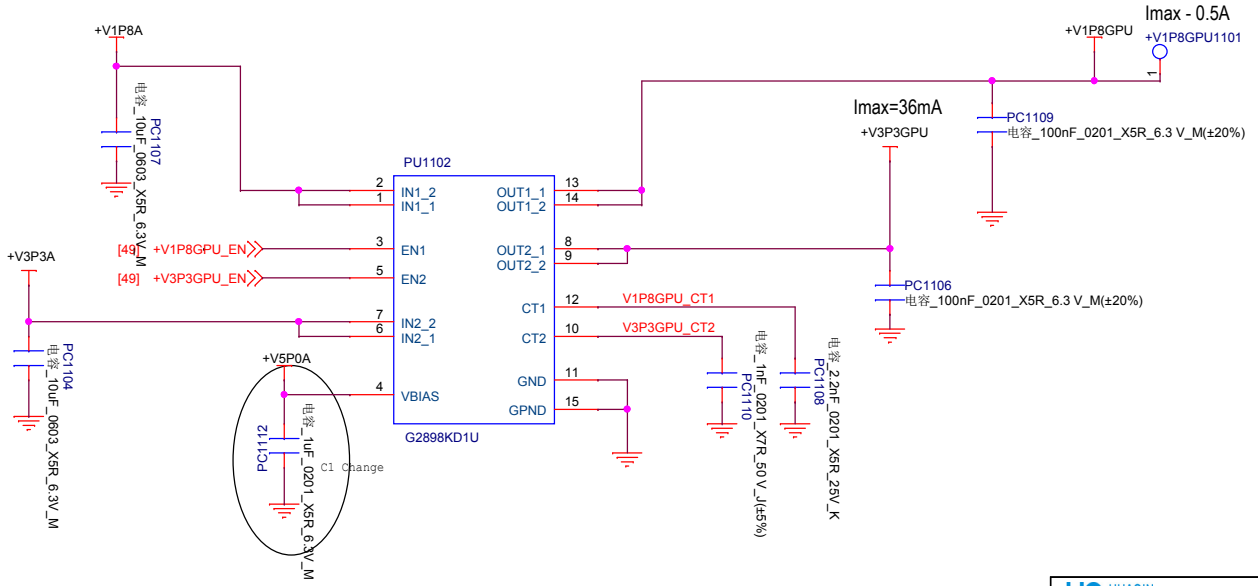
Date: Friday, March 29, 2019	Sheet: 44 of 55

+V0P95GPU



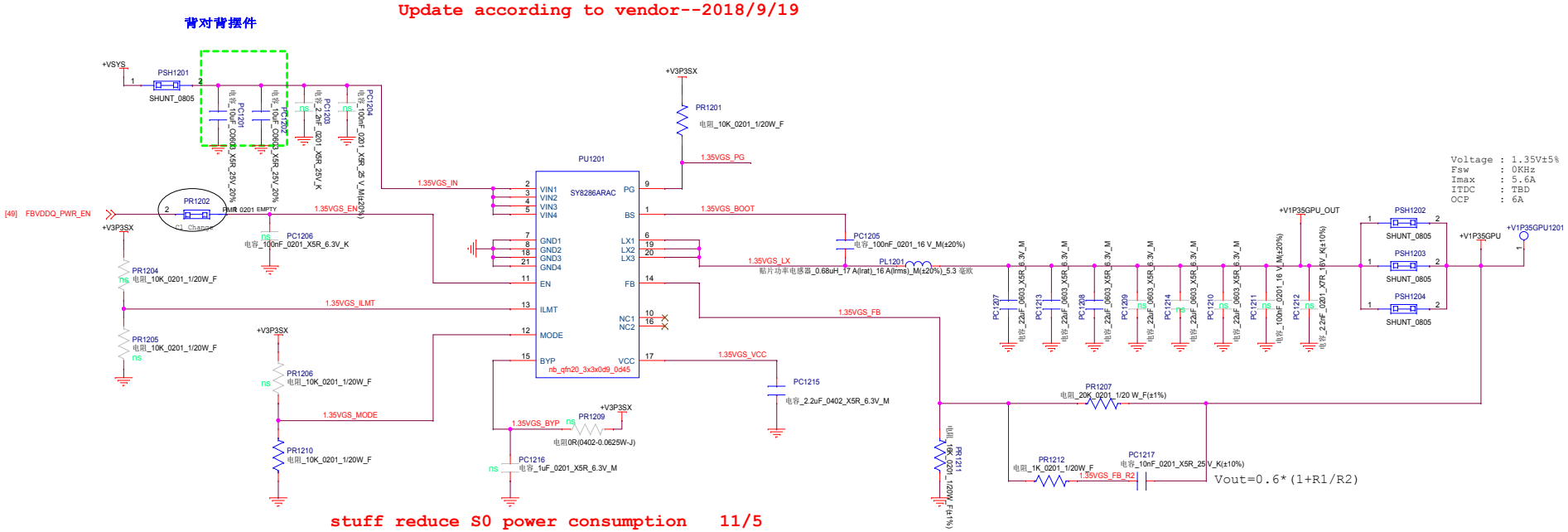
+V1P8GPU
+V3P3GPU



HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	GPU_LOADSWITCH	
Size: A4	Project Name: NB8607	REV: V1.0
Date: Tuesday, April 02, 2019	Sheet: 45 of 55	

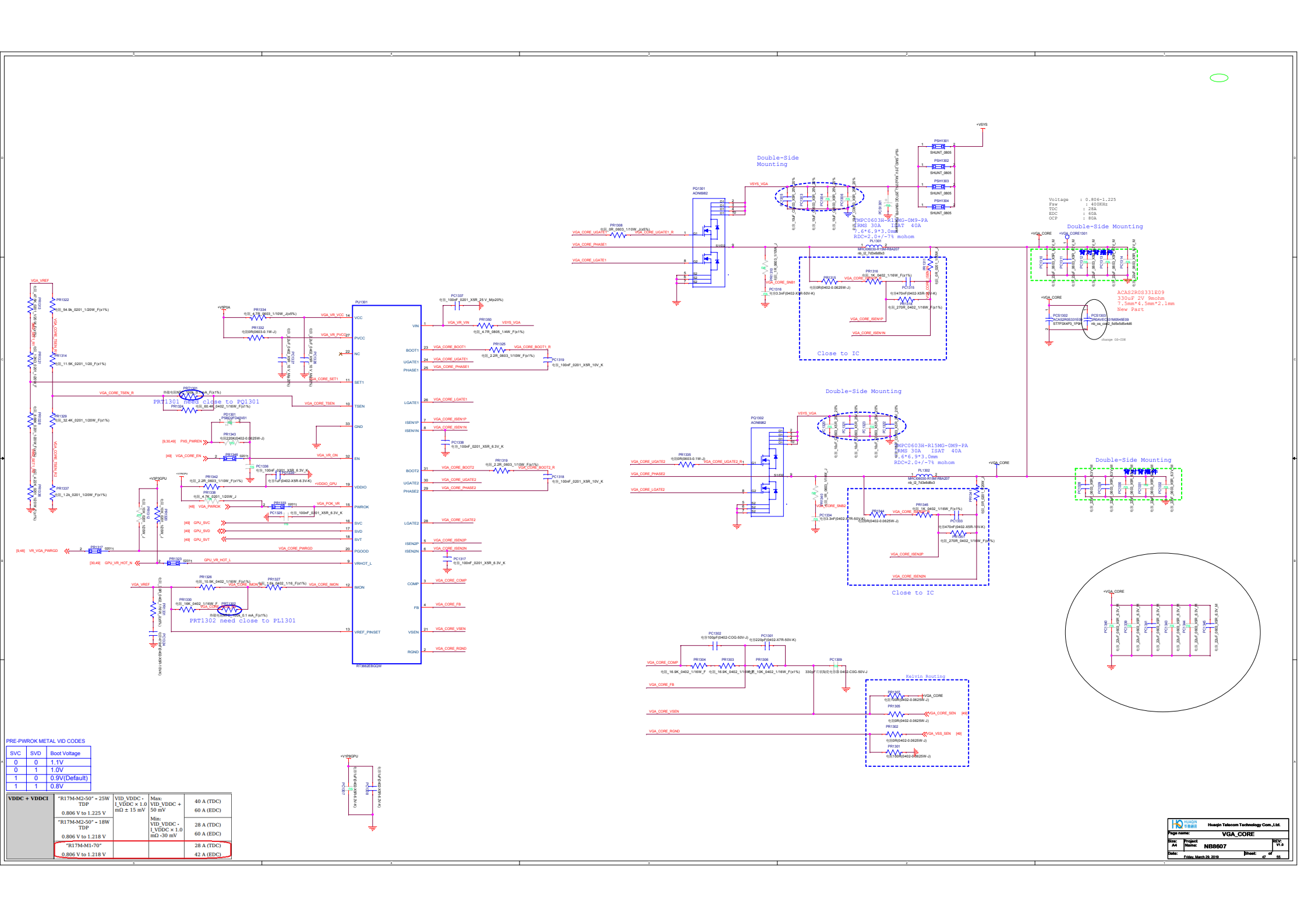
ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A

Update according to vendor--2018/9/19



stuff reduce S0 power consumption 11/5

HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.		
Page name:	V1P35GPU		
Size: A4	Project Name: NB8607	REV: V1.0	
Date: Friday, March 29, 2019	Sheet: 46 of 55		

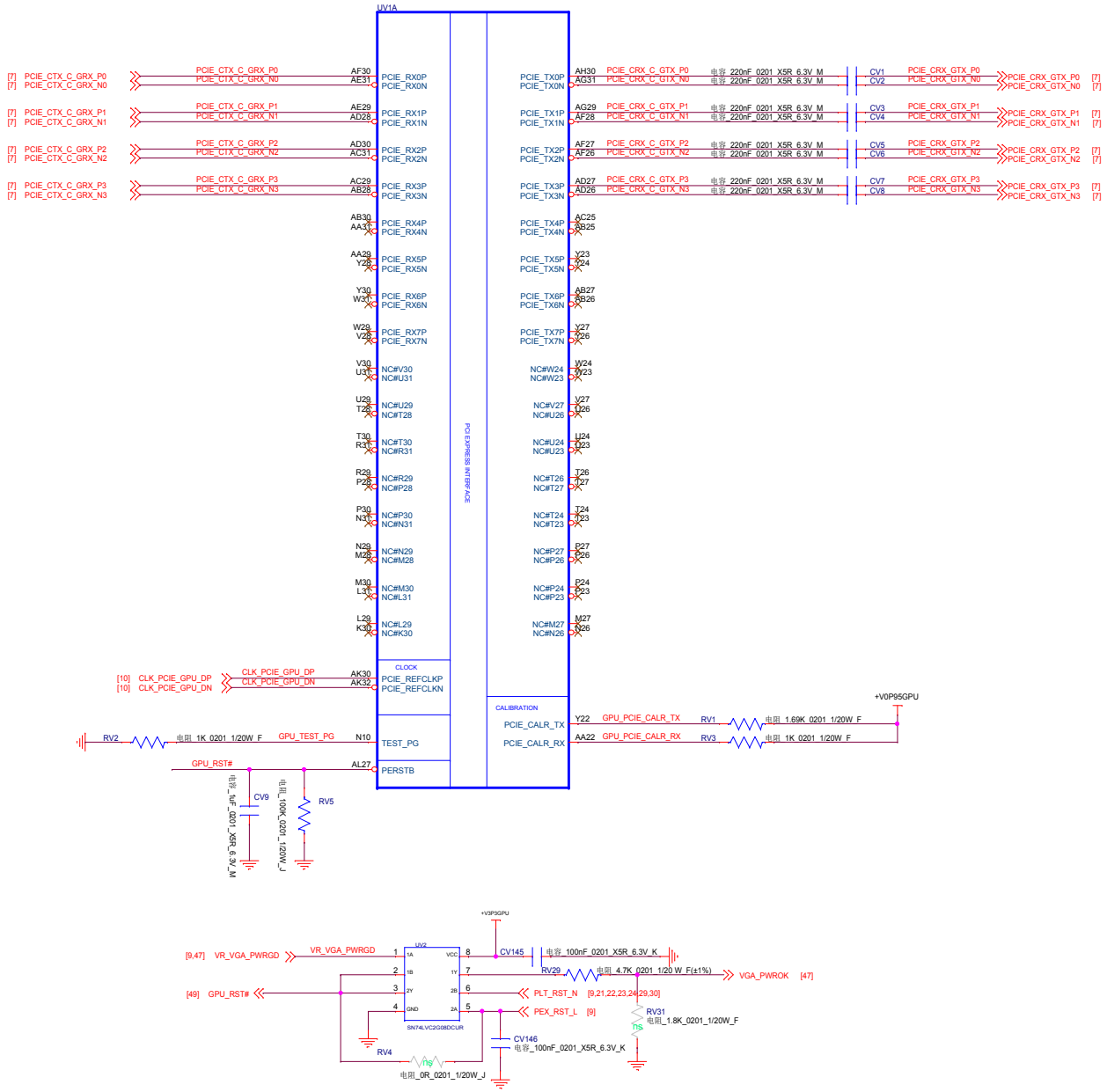


PRE-PWROK METAL VID CODES

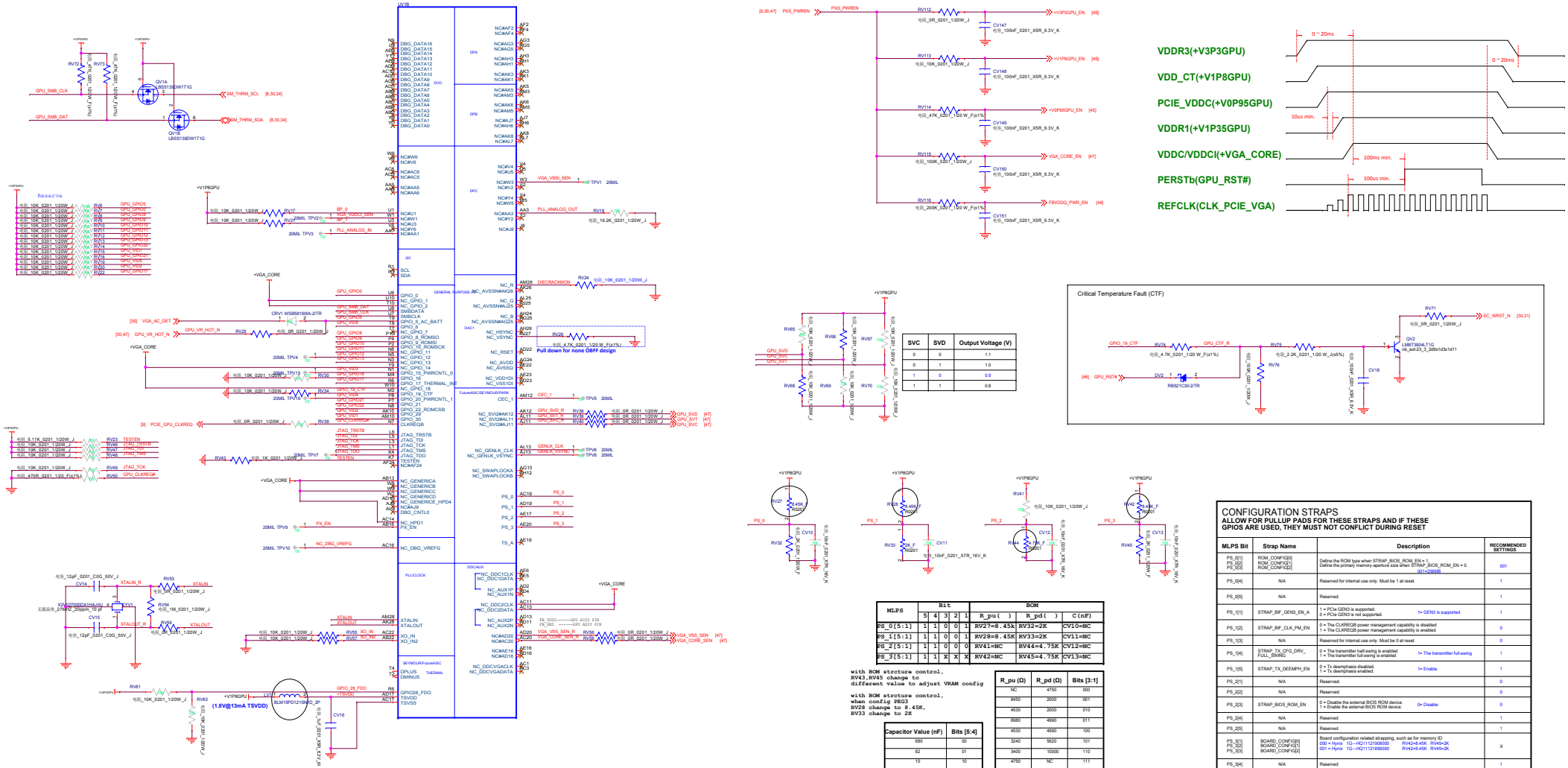
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

VDDC + VDDCI				
	"R17M-M2-50" - 25W TDP 0.806 V to 1.225 V	VID_VDDC - I_VDDC × 1.0 mΩ ± 15 mV	Max: VID_VDDC + 50 mV	40 A (TDC) 60 A (EDC)
	"R17M-M2-50" - 18W TDP 0.806 V to 1.218 V		Min: VID_VDDC - I_VDDC × 1.0 mΩ -30 mV	28 A (TDC) 60 A (EDC)
	"R17M-M1-70" 0.806 V to 1.218 V			28 A (TDC) 42 A (EDC)

Huaqin Telecom Technology Com.,Ltd.			
Page name:	VGA_CORE		
Size: A4	Project Name: NB8607		REV: V1.0
Date: Friday, March 29, 2019	Sheet: 47	of 55	



Huaqin Telecom Technology Com.,Ltd.	
Page name:	FT4_PCIE
Size: A4	Project Name: NB8607
REV: V1.0	
Date: Friday, March 29, 2019	Sheet: 48 of 55



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0.	001 001=256MB
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= GEN3 is supported	1
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled 1= The transmitter full-swing	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	1
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	0
PS_2[4]	N/A	Reserved	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 1G---HQ11121908000 RV42=8.45K RV45=2K 001 = Hynix 1G---HQ11121908000 RV42=8.45K RV45=2K	X
PS_3[4]	N/A	Reserved	1
PS_3[5]	N/A	Reserved	1

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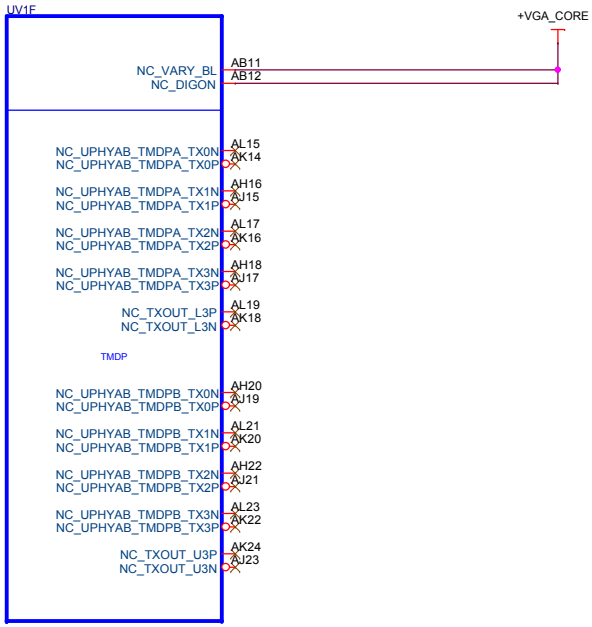
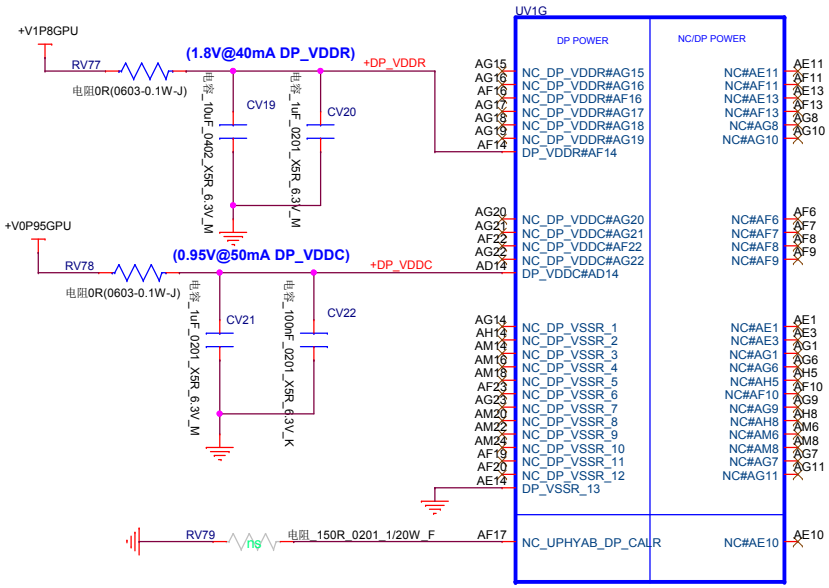
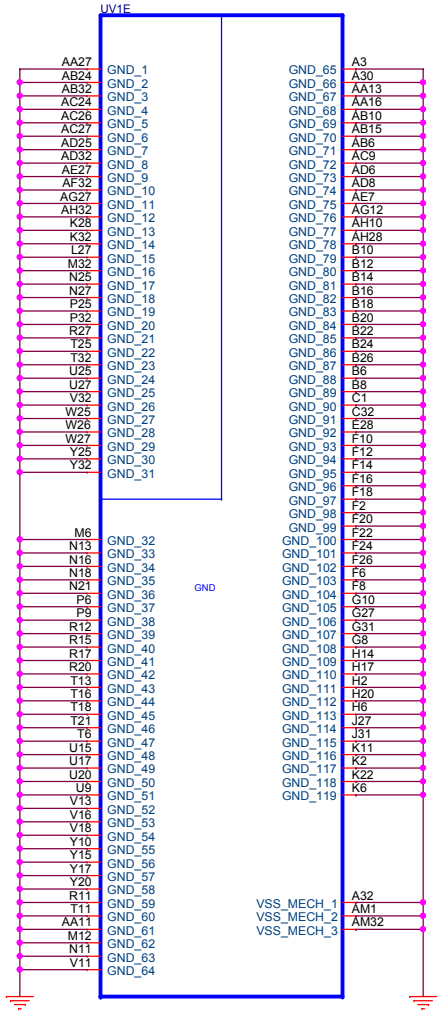
Page name:	FT4_PCIE
Size: A4	Project Name: N88607 REV: V1.0
Date: Sunday, March 31, 2019	Sheet: 49 of 55

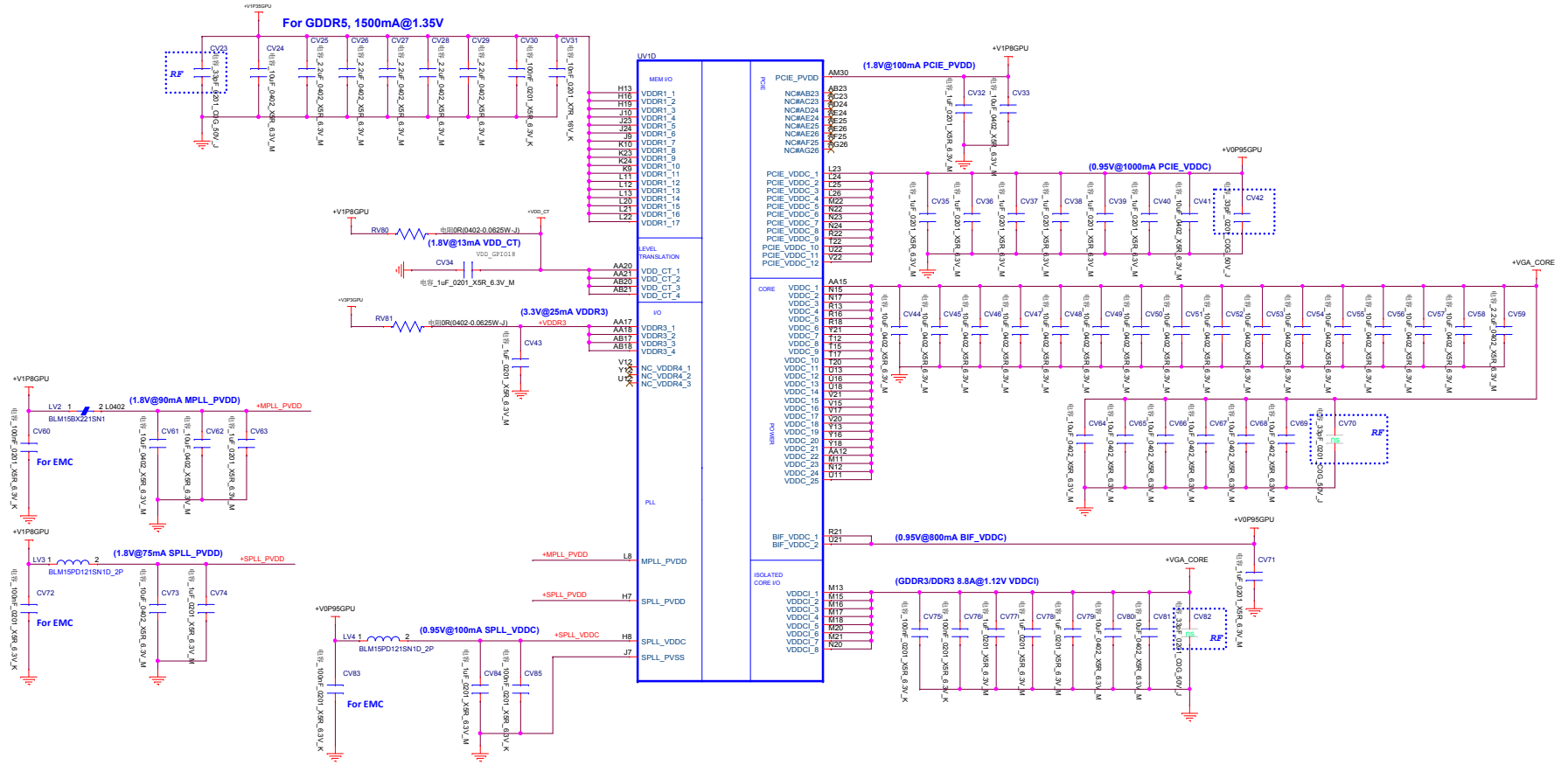


HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	FT4_PCIE	
Size: A4	Project Name: NB8607	REV: V1.0
Date: Friday, March 29, 2019	Sheet: 50 of 55	





HUAQIN 华勤通讯	Huaqin Telecom Technology Com.,Ltd.	
Page name:	FT4_PCIE	
Size: A4	Project Name: NB8607	REV: V1.0
Date: Friday, March 29, 2019	Sheet: 51 of 55	


For GDDR5, 1500mA@1.35V
UV1D
MEM I/O
LEVEL TRANSLATION
I/O
PLL
PCIE
CORE
PCI MEM
ISOLATED CORE I/O
PCIE_PVDD
(1.8V@100mA PCIE_PVDD)
(0.95V@1000mA PCIE_VDDC)
(1.8V@13mA VDD_CT)
(3.3V@25mA VDDR3)
(1.8V@90mA MPLL_PVDD)
(1.8V@75mA SPLL_PVDD)
(0.95V@100mA SPLL_VDDC)
(0.95V@800mA BIF_VDDC)
(GDDR3/DDR3 8.8A@1.12V VDDCI)
For EMC
RF
+VGA_CORE
Huaqin Telecom Technology Com.,Ltd.
Page name: FT4_PCIE
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Date: Friday, March 29, 2019
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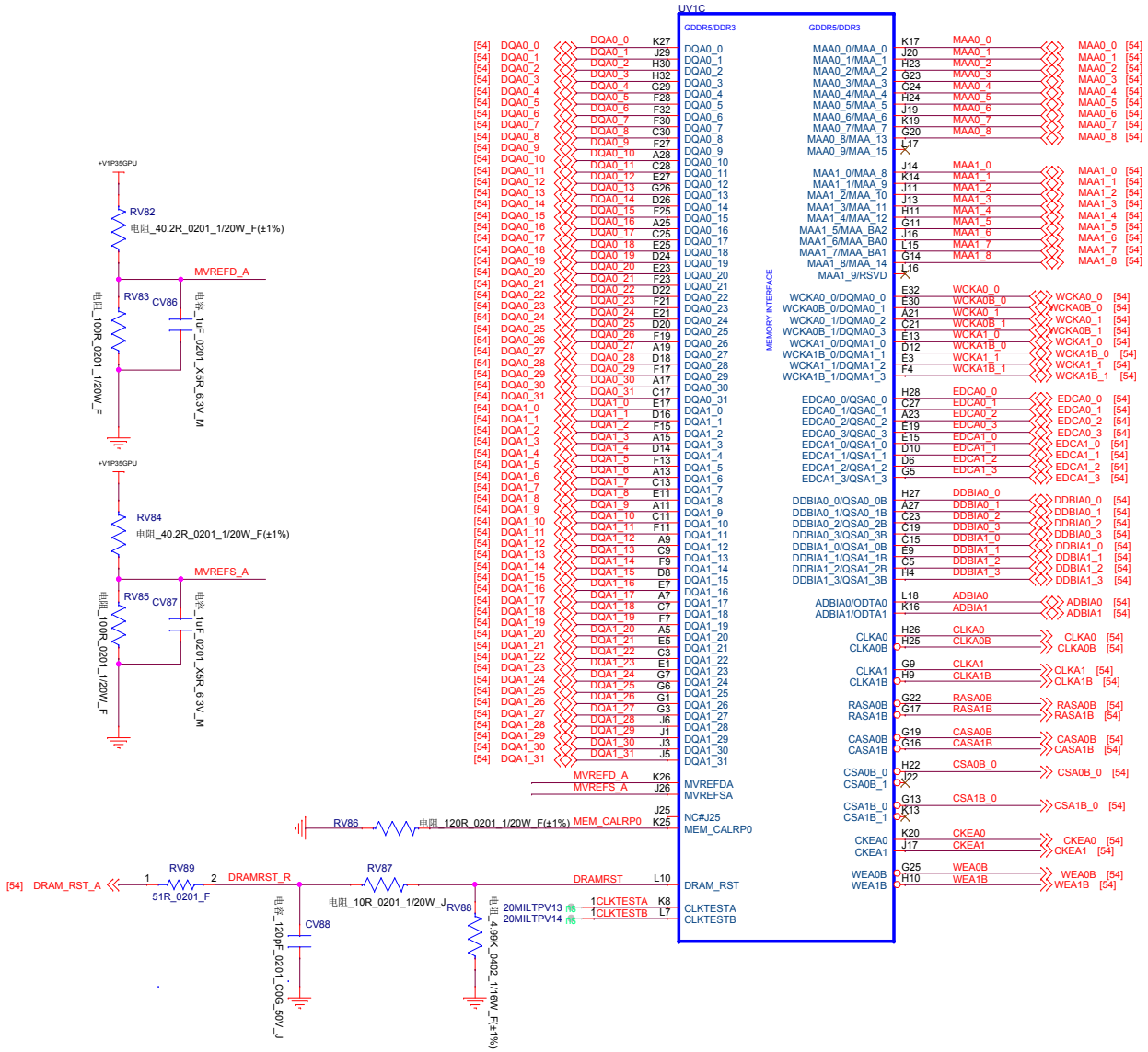
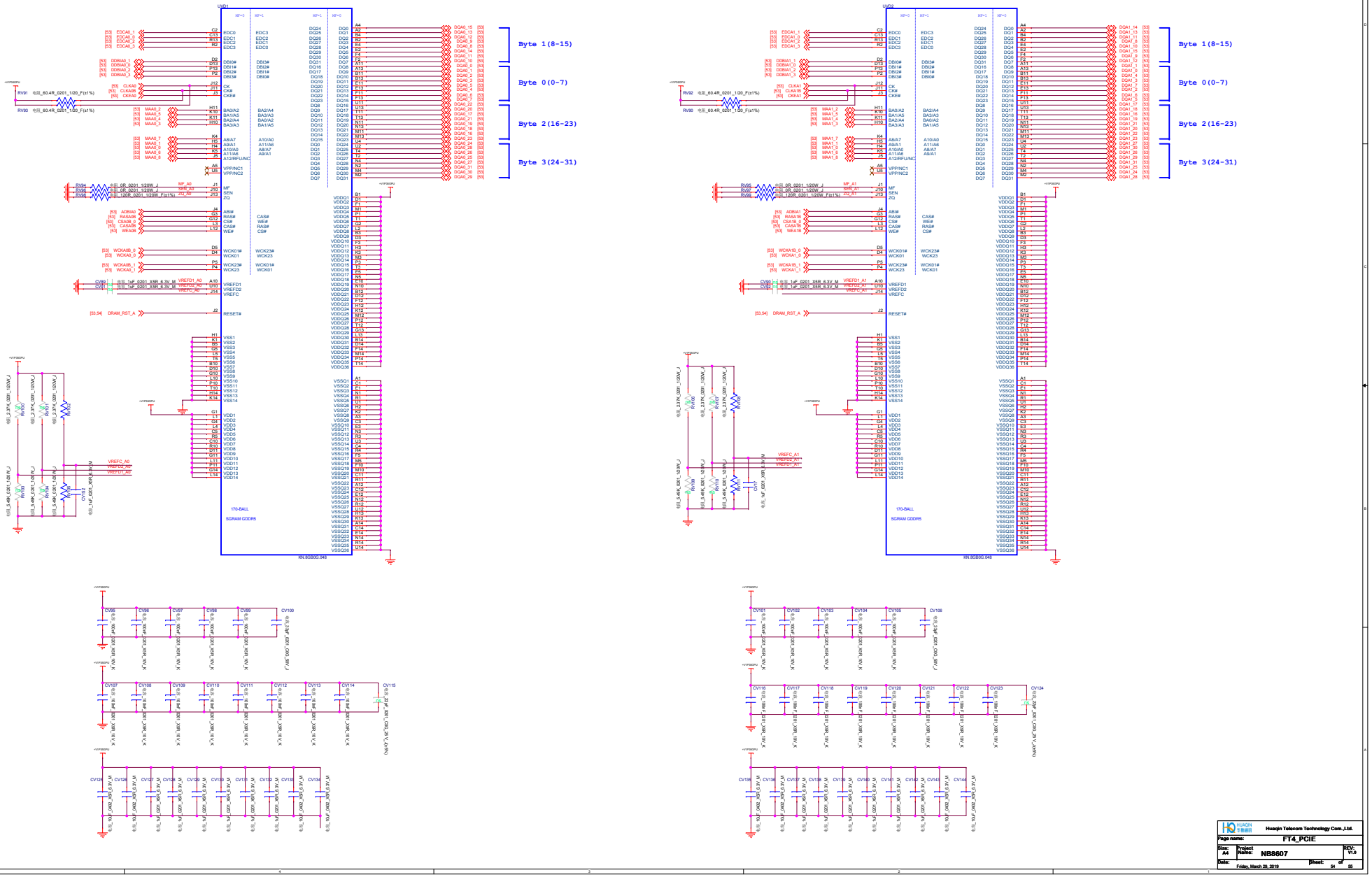


Huaqin Telecom Technology Com.,Ltd.	
Page name:	FT4_PCIE
Size: A4	Project Name: NB8607
REV: V1.0	
Date: Friday, March 29, 2019	Sheet: 53 of 55


UUD1
UUD2
Byte 1(8-15)
Byte 0(0-7)
Byte 2(16-23)
Byte 3(24-31)
170-BALL
SGRAM GDDR5
Husqin Telecom Technology Com.,Ltd.
Page name:
FT4_PCIE
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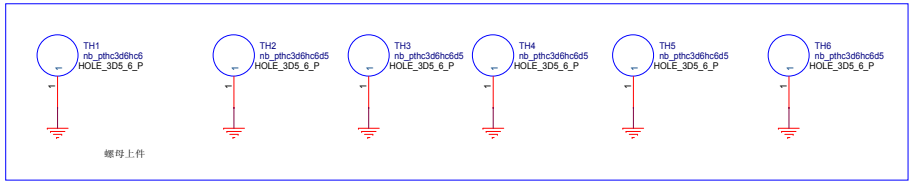

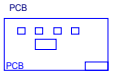

NB8607_主板PCB_V1_瀚宇博德

Huaqin Telecom Technology Com.,Ltd.		
Page name:	MEM_DECAPS	
Size: A4	Project Name: NB8607	REV: V1.0
Date: Monday, April 01, 2019	Sheet: 55 of 55	