GA-880GM-D2H

Revision : 1.32

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10	RS880 SYSTEM I/F STRAP
11	RS880 POWER & GND
12	RTM880-792
13	ATI SB710 PCIE/PCI/CPU/LPC
14	ATI SB710 ACPI/USB/GPIO/AUDIO
15	ATI SB710 SATA/SPI/IDE/HWM
16	ATI SB710 POWER & GND
17	PCI EXPRESS x16 ,x1
18	PCI SLOT 1, 2
19	REALTK RTL8111D/8101E
20	ALC888B
21	AUDIO JACK
22	IDE ,FDD ,HDMI ,DVI Connector
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9M-00

PAGE	TITLE
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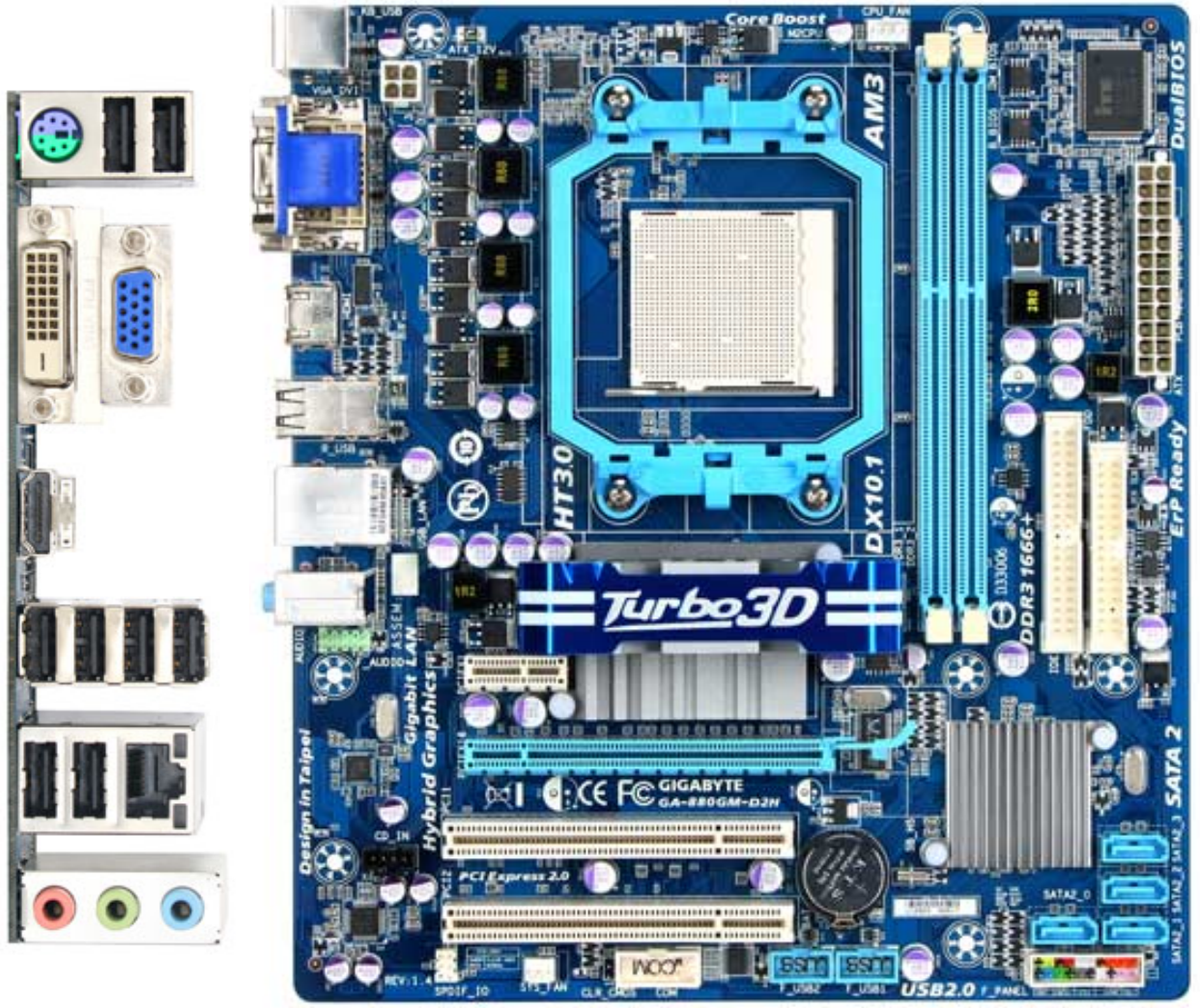
29	NB/SB POWER, VCC12HT, VDDA25 ,VCC12_Dual
30	DDRIII POWER, VCC18



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Title: COVER SHEET		
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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Model Name : GA-880GM-D2H

Component value change history

Version: 1.32

P-Code: U99020-0

Date	Change Item		Reason
2009.05.04	1.3A EVT BOM Release.	PCB: 1.3	Modify from MA78LM-S2 3.3 B Change RS880P
			Change to all OS CON CAP/ ADD HDMI connector.
2009.05.27	1.3B PVT BOM Release.	PCB: 1.31	Remove CBC1 SPDIF bypass / modify R2774 NB_VCC RES to 4.7K
			Add Q84 for HDMI/DVI Plug togeter No output issue
			BAT54A 改不指定料號 / C74 Remove (-LDTSTOP)
			IT8718 改銅製程 add SPI 8M Winbond 25Q80
2009.07.02	1.4A E BOM Release.	PCB: 1.4	Change ALC888B-VD2
2009.07.23	1.3F P BOM Release.	PCB: 1.32	SPI CS Pull up RES (R28, R33) 330ohm -> 220ohm CR6 0 ohm --> 75 ohm CR16 add 0 ohm
2009.08.05	1.3F P BOM Release.	PCB: 1.32	ECN : add NB_HS & SB_HS 2nd source

Circuit or PCB layout change for next version

Date	Version	Change Item
2010.05.05	1.3 Gerber out	Copy from MA78LM-S2H 3.3. Add DDR3 1666+ Change EC49 footprin to EC6D8MM-RH.
2010.05.26	1.31 Gerber out	Add DX10.1, Hybrid Crossfire.
2010.07.01	1.4 Gerber out	888B/888B-VD2 Colay
2010.07.01	1.32 Gerber out	Modify from 1.4 Fix SPDIF Crosstalk issue / AGND to DGND shortpad / MH2 AGND --> DGND for AP

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Title: BOM & PCB HISTORY

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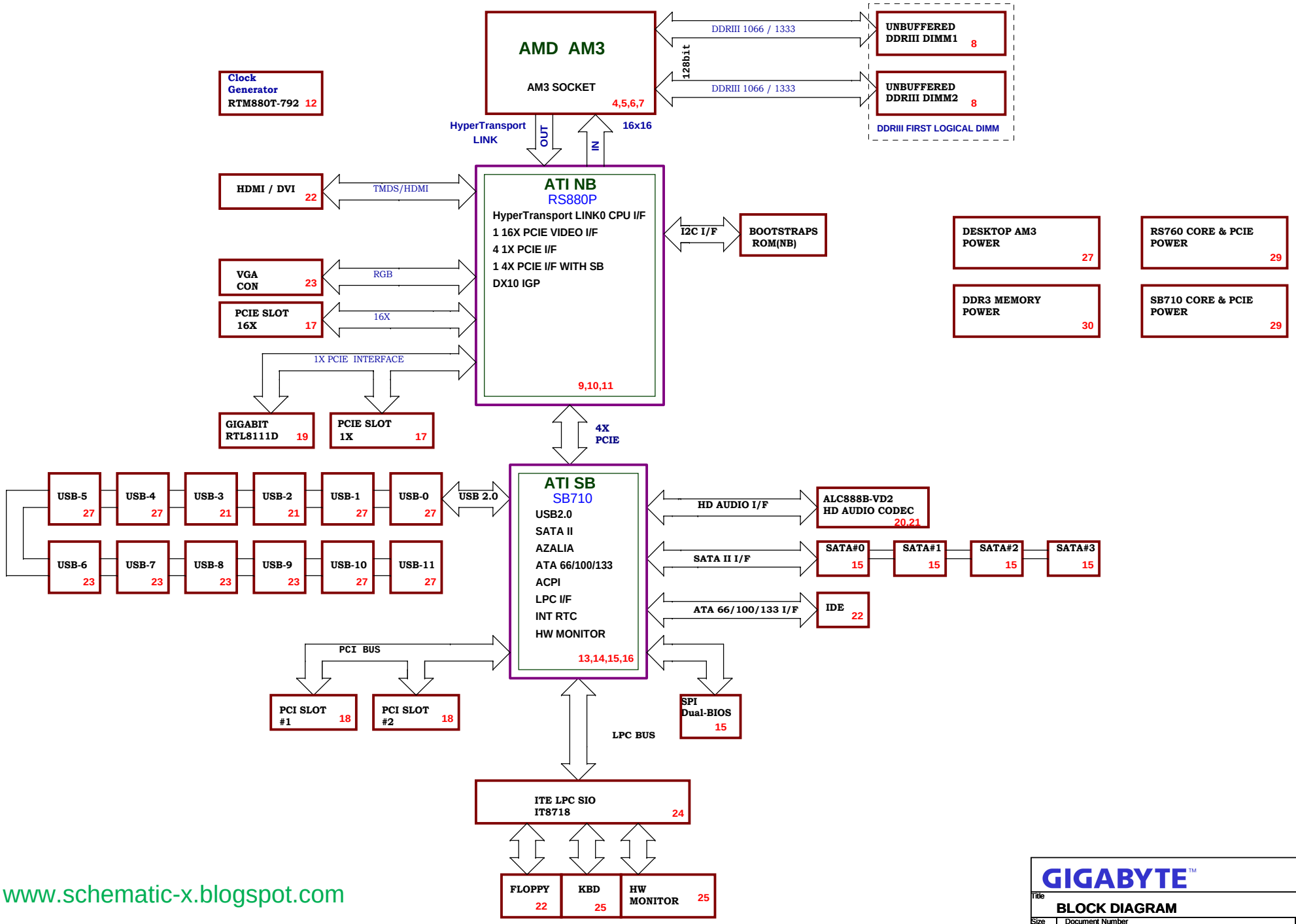
RS880 CUSTOMER DESKTOP REFERENCE DESIGN



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Title: BLOCK DIAGRAM		
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
Date: Friday, July 23, 2010	Sheet 3 of 30	

L0_CADIN_L[0..15] L0_CADIN_L[0..15] <9>

L0_CADIN_H[0..15] L0_CADIN_H[0..15] <9>

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <9>

L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <9>

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

<9> L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1	<9>
<9> L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1	<9>
<9> L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0	<9>
<9> L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0	<9>
<9> L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1	<9>
<9> L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1	<9>
<9> L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0	<9>
<9> L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0	<9>
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15		
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15		
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14		
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14		
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13		
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13		
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12		
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12		
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11		
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11		
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10		
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10		
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9		
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9		
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8		
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8		
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7		
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7		
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6		
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6		
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5		
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5		
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4		
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4		
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3		
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3		
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2		
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2		
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1		
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1		
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0		
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0		

CPU-SK/941AM3/S/15u

M2CPU

AM2RM/SC/BK/MB/[12KRC-04K812-11R_12KRC-04K812-12R]

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Title: CPU HYPER TRANSPORT		
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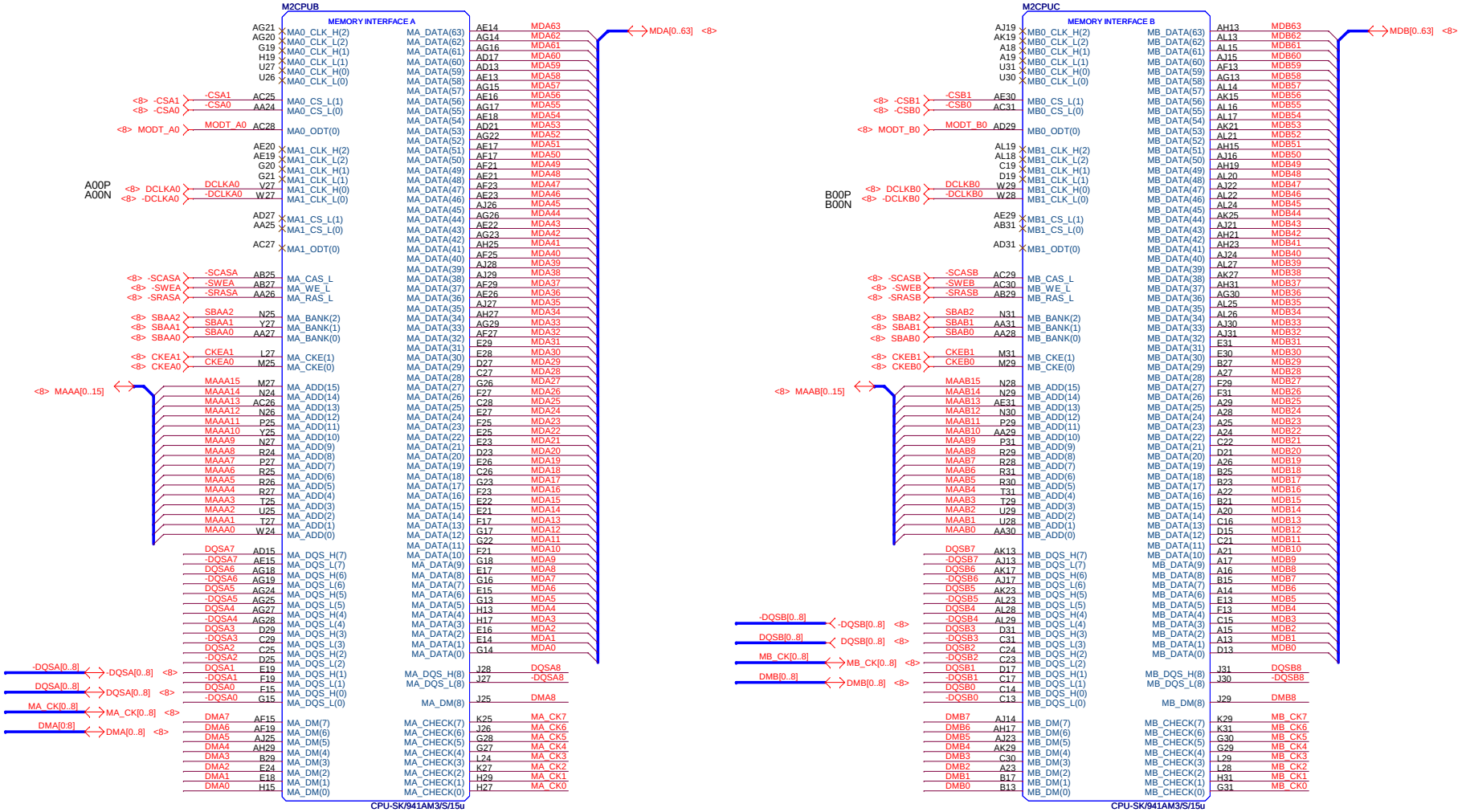

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Title	CPU DDRII MEMORY	
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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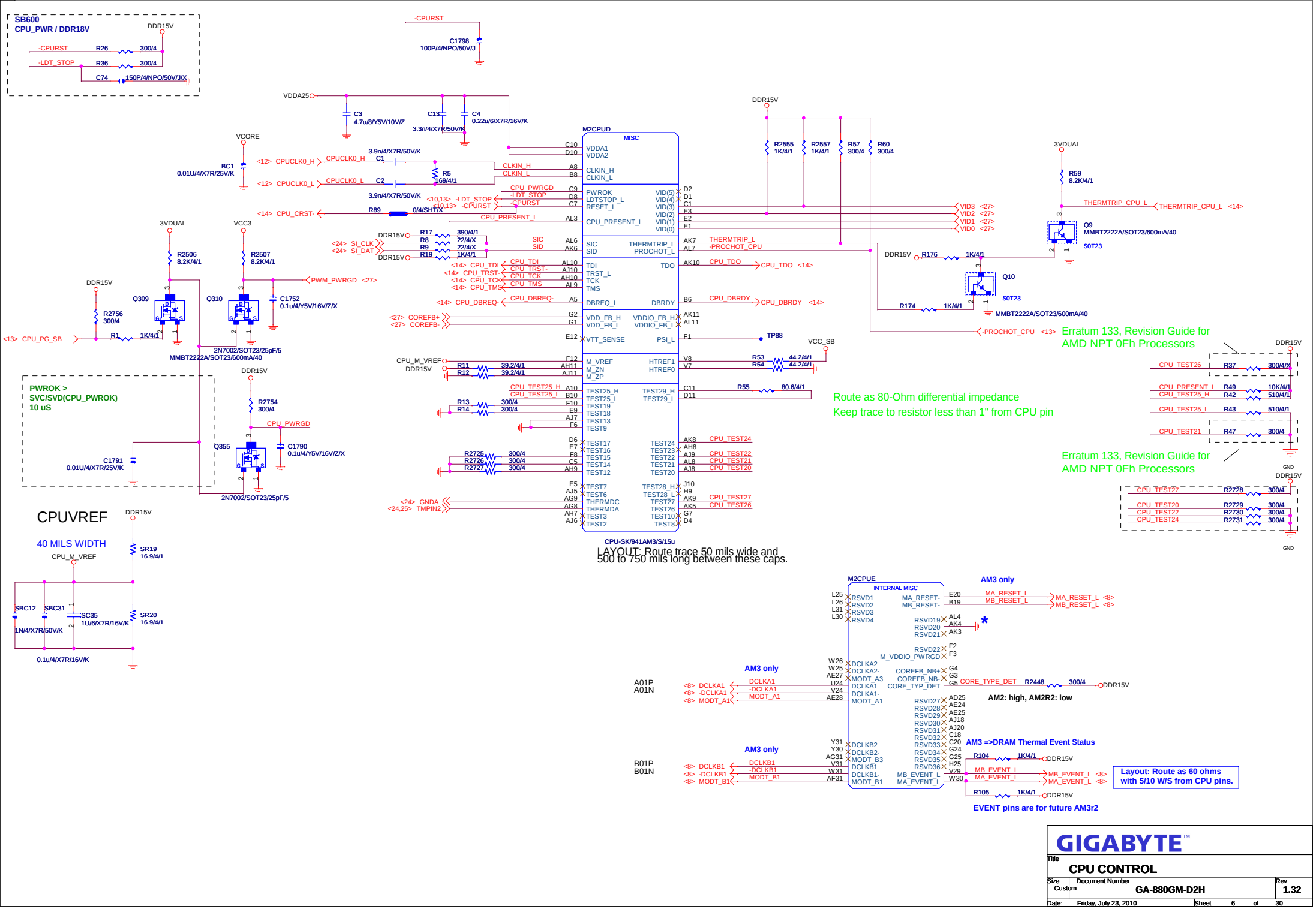

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Title	CPU CONTROL	
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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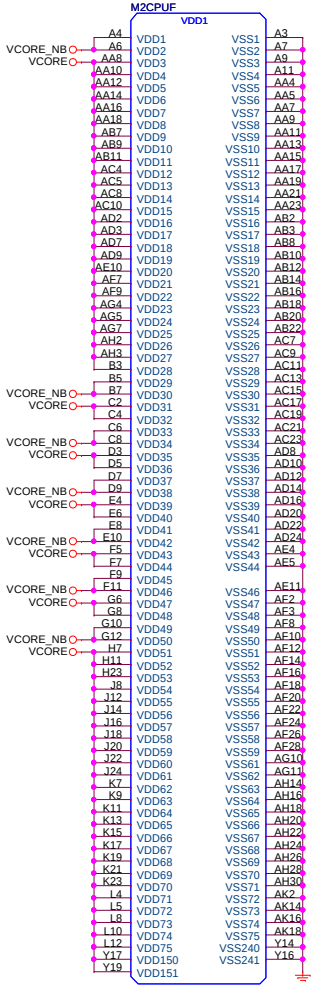
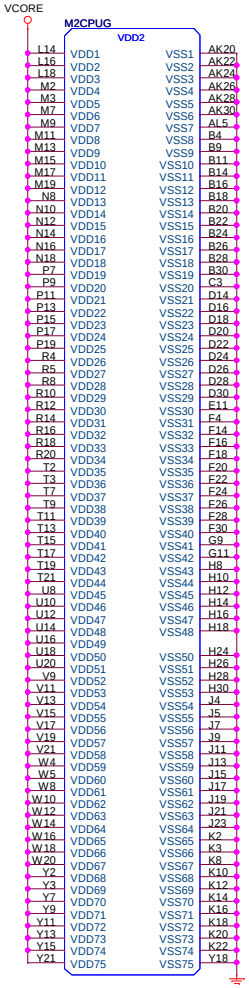
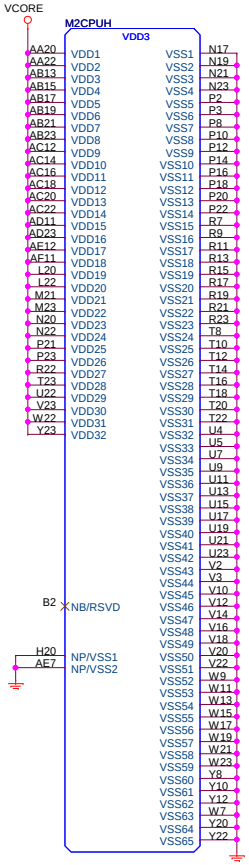
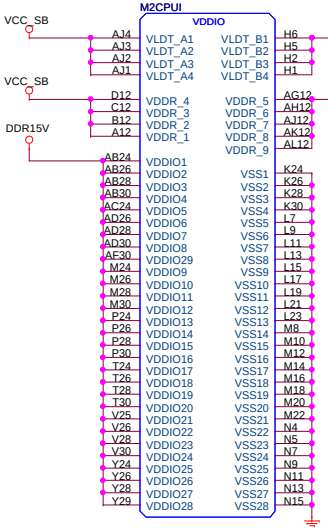
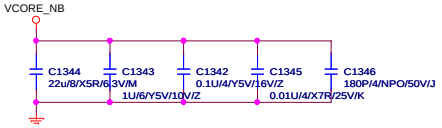
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

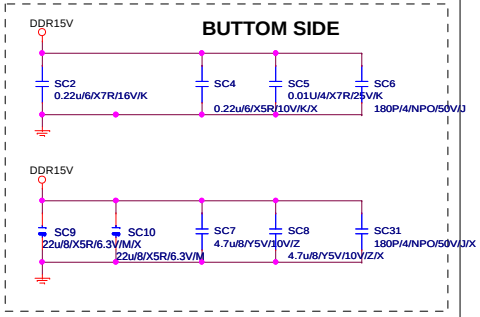


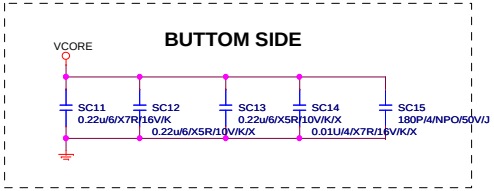


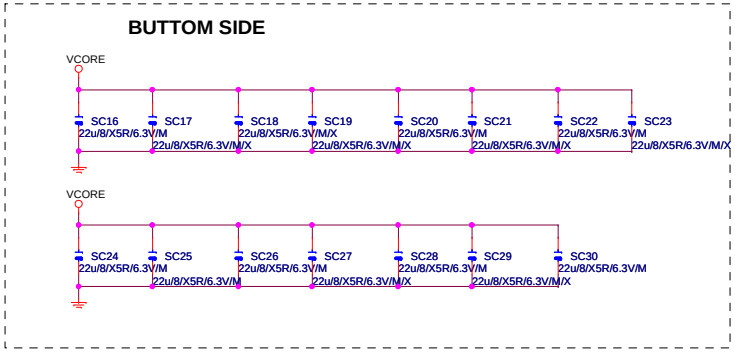


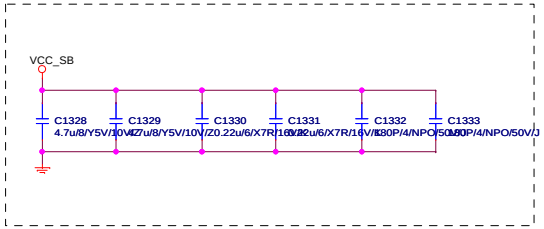


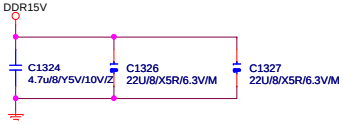


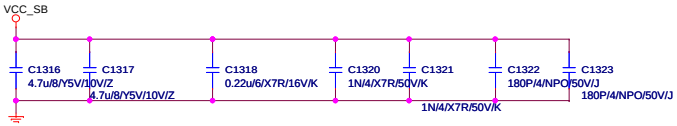


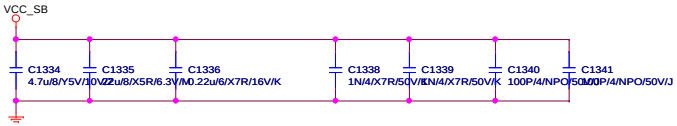


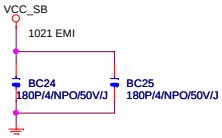












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Title: CPU POWER & GND		
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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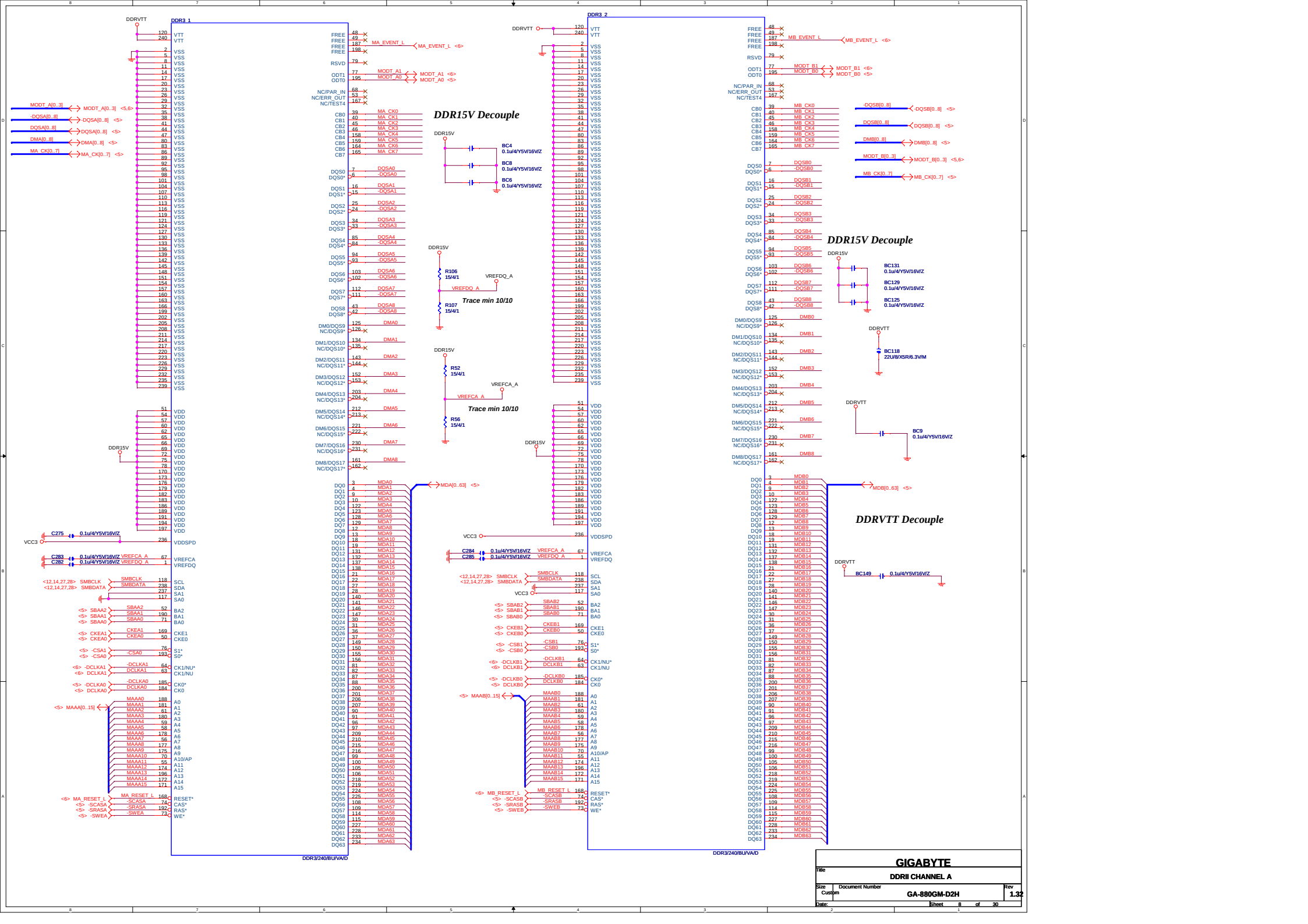

GIGABYTE			
Title: DDRII CHANNEL A			
Size: Custom	Document Number: GA-880GM-D2H		Rev: 1.32
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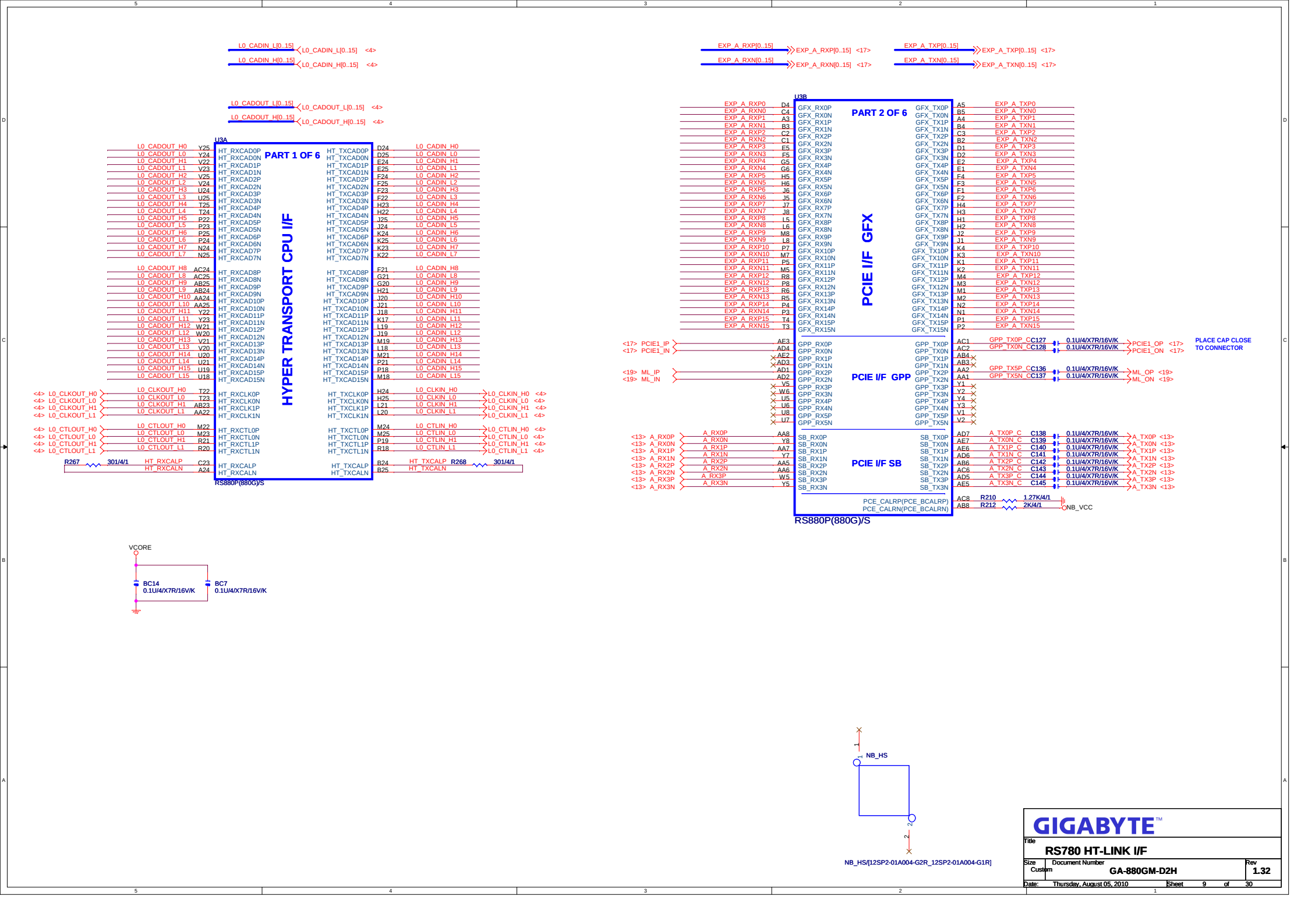
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L0_CADIN_H[0..15]
L0_CADIN_H[0..15] <4>
L0_CADOUT_L[0..15]
L0_CADOUT_L[0..15] <4>
L0_CADOUT_H[0..15]
L0_CADOUT_H[0..15] <4>
U3A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS880P(880G)/S
HT_RXCAD0P
HT_RXCAD0N
HT_RXCAD1P
HT_RXCAD1N
HT_RXCAD2P
HT_RXCAD2N
HT_RXCAD3P
HT_RXCAD3N
HT_RXCAD4P
HT_RXCAD4N
HT_RXCAD5P
HT_RXCAD5N
HT_RXCAD6P
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HT_RXCAD14P
HT_RXCAD14N
HT_RXCAD15P
HT_RXCAD15N
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HT_RXCLK1P
HT_RXCLK1N
HT_RXCTL0P
HT_RXCTL0N
HT_RXCTL1P
HT_RXCTL1N
HT_RXCALP
HT_RXCALN
HT_TXCAD0P
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HT_TXCAD1P
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HT_TXCAD2P
HT_TXCAD2N
HT_TXCAD3P
HT_TXCAD3N
HT_TXCAD4P
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HT_TXCAD10P
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HT_TXCLK1P
HT_TXCLK1N
HT_TXCTL0P
HT_TXCTL0N
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HT_TXCALP
HT_TXCALN
L0_CADOUT_H0 Y25
L0_CADOUT_L0 Y24
L0_CADOUT_H1 V22
L0_CADOUT_L1 V23
L0_CADOUT_H2 V25
L0_CADOUT_L2 V24
L0_CADOUT_H3 U24
L0_CADOUT_L3 U25
L0_CADOUT_H4 T25
L0_CADOUT_L4 T24
L0_CADOUT_H5 P22
L0_CADOUT_L5 P23
L0_CADOUT_H6 P25
L0_CADOUT_L6 P24
L0_CADOUT_H7 N24
L0_CADOUT_L7 N25
L0_CADOUT_H8 AC24
L0_CADOUT_L8 AC25
L0_CADOUT_H9 AB25
L0_CADOUT_L9 AB24
L0_CADOUT_H10 AA24
L0_CADOUT_L10 AA25
L0_CADOUT_H11 Y22
L0_CADOUT_L11 Y23
L0_CADOUT_H12 W21
L0_CADOUT_L12 W20
L0_CADOUT_H13 V21
L0_CADOUT_L13 V20
L0_CADOUT_H14 U20
L0_CADOUT_L14 U21
L0_CADOUT_H15 U19
L0_CADOUT_L15 U18
L0_CLKOUT_H0 T22
L0_CLKOUT_L0 T23
L0_CLKOUT_H1 AB23
L0_CLKOUT_L1 AA22
L0_CTLOUT_H0 M22
L0_CTLOUT_L0 M23
L0_CTLOUT_H1 R21
L0_CTLOUT_L1 R20
D24 L0_CADIN_H0
D25 L0_CADIN_L0
E24 L0_CADIN_H1
E25 L0_CADIN_L1
F24 L0_CADIN_H2
F25 L0_CADIN_L2
F23 L0_CADIN_H3
F22 L0_CADIN_L3
H23 L0_CADIN_H4
H22 L0_CADIN_L4
J25 L0_CADIN_H5
J24 L0_CADIN_L5
K24 L0_CADIN_H6
K25 L0_CADIN_L6
K23 L0_CADIN_H7
K22 L0_CADIN_L7
F21 L0_CADIN_H8
G21 L0_CADIN_L8
G20 L0_CADIN_H9
H21 L0_CADIN_L9
J20 L0_CADIN_H10
J21 L0_CADIN_L10
J18 L0_CADIN_H11
K17 L0_CADIN_L11
L19 L0_CADIN_H12
J19 L0_CADIN_L12
M19 L0_CADIN_H13
L18 L0_CADIN_L13
M21 L0_CADIN_H14
P21 L0_CADIN_L14
P18 L0_CADIN_H15
M18 L0_CADIN_L15
H24 L0_CLKIN_H0
H25 L0_CLKIN_L0
L21 L0_CLKIN_H1
L20 L0_CLKIN_L1
M24 L0_CTLIN_H0
M25 L0_CTLIN_L0
P19 L0_CTLIN_H1
R18 L0_CTLIN_L1
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B25 HT_TXCALN
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<4> L0_CTLOUT_L1
L0_CLKIN_H0 <4>
L0_CLKIN_L0 <4>
L0_CLKIN_H1 <4>
L0_CLKIN_L1 <4>
L0_CTLIN_H0 <4>
L0_CTLIN_L0 <4>
L0_CTLIN_H1 <4>
L0_CTLIN_L1 <4>
R267 301/4/1 HT_RXCALP
HT_RXCALN
R268 301/4/1 HT_TXCALP
HT_TXCALN
VCORE
BC14 0.1U/4/7R/16V/K
BC7 0.1U/4/7R/16V/K
EXP_A_RXP[0..15]
EXP_A_RXP[0..15] <17>
EXP_A_RXN[0..15]
EXP_A_RXN[0..15] <17>
EXP_A_TXP[0..15]
EXP_A_TXP[0..15] <17>
EXP_A_TXN[0..15]
EXP_A_TXN[0..15] <17>
U3B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS880P(880G)/S
GFX_RX0P
GFX_RX0N
GFX_RX1P
GFX_RX1N
GFX_RX2P
GFX_RX2N
GFX_RX3P
GFX_RX3N
GFX_RX4P
GFX_RX4N
GFX_RX5P
GFX_RX5N
GFX_RX6P
GFX_RX6N
GFX_RX7P
GFX_RX7N
GFX_RX8P
GFX_RX8N
GFX_RX9P
GFX_RX9N
GFX_RX10P
GFX_RX10N
GFX_RX11P
GFX_RX11N
GFX_RX12P
GFX_RX12N
GFX_RX13P
GFX_RX13N
GFX_RX14P
GFX_RX14N
GFX_RX15P
GFX_RX15N
GFX_TX0P
GFX_TX0N
GFX_TX1P
GFX_TX1N
GFX_TX2P
GFX_TX2N
GFX_TX3P
GFX_TX3N
GFX_TX4P
GFX_TX4N
GFX_TX5P
GFX_TX5N
GFX_TX6P
GFX_TX6N
GFX_TX7P
GFX_TX7N
GFX_TX8P
GFX_TX8N
GFX_TX9P
GFX_TX9N
GFX_TX10P
GFX_TX10N
GFX_TX11P
GFX_TX11N
GFX_TX12P
GFX_TX12N
GFX_TX13P
GFX_TX13N
GFX_TX14P
GFX_TX14N
GFX_TX15P
GFX_TX15N
GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N
GPP_RX4P
GPP_RX4N
GPP_RX5P
GPP_RX5N
GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N
GPP_TX4P
GPP_TX4N
GPP_TX5P
GPP_TX5N
SB_RX0P
SB_RX0N
SB_RX1P
SB_RX1N
SB_RX2P
SB_RX2N
SB_RX3P
SB_RX3N
SB_TX0P
SB_TX0N
SB_TX1P
SB_TX1N
SB_TX2P
SB_TX2N
SB_TX3P
SB_TX3N
EXP_A_RXP0 D4
EXP_A_RXN0 C4
EXP_A_RXP1 A3
EXP_A_RXN1 B3
EXP_A_RXP2 C2
EXP_A_RXN2 C1
EXP_A_RXP3 E5
EXP_A_RXN3 F5
EXP_A_RXP4 G5
EXP_A_RXN4 G6
EXP_A_RXP5 H5
EXP_A_RXN5 H6
EXP_A_RXP6 J6
EXP_A_RXN6 J5
EXP_A_RXP7 J7
EXP_A_RXN7 J8
EXP_A_RXP8 L5
EXP_A_RXN8 L6
EXP_A_RXP9 M8
EXP_A_RXN9 L8
EXP_A_RXP10 P7
EXP_A_RXN10 M7
EXP_A_RXP11 P5
EXP_A_RXN11 M5
EXP_A_RXP12 P8
EXP_A_RXN12 R8
EXP_A_RXP13 R6
EXP_A_RXN13 R5
EXP_A_RXP14 P4
EXP_A_RXN14 P3
EXP_A_RXP15 T4
EXP_A_RXN15 T3
A5 EXP_A_TXP0
B5 EXP_A_TXN0
A4 EXP_A_TXP1
B4 EXP_A_TXN1
C3 EXP_A_TXP2
B2 EXP_A_TXN2
D1 EXP_A_TXP3
D2 EXP_A_TXN3
E2 EXP_A_TXP4
E1 EXP_A_TXN4
F4 EXP_A_TXP5
F3 EXP_A_TXN5
F1 EXP_A_TXP6
F2 EXP_A_TXN6
H4 EXP_A_TXP7
H3 EXP_A_TXN7
H1 EXP_A_TXP8
H2 EXP_A_TXN8
J2 EXP_A_TXP9
J1 EXP_A_TXN9
K4 EXP_A_TXP10
K3 EXP_A_TXN10
K1 EXP_A_TXP11
K2 EXP_A_TXN11
M4 EXP_A_TXP12
M3 EXP_A_TXN12
M1 EXP_A_TXP13
M2 EXP_A_TXN13
N2 EXP_A_TXP14
N1 EXP_A_TXN14
P1 EXP_A_TXP15
P2 EXP_A_TXN15
<17> PCIE1_IP AE3
<17> PCIE1_IN AD4
AE2
AD3
<19> ML_IP AD1
<19> ML_IN AD2
V5
W6
U5
U6
U8
U7
AC1 GPP_TX0P_C C127 0.1U/4/X7R/16V/K PCIE1_OP <17>
AC2 GPP_TX0N_C C128 0.1U/4/X7R/16V/K PCIE1_ON <17>
AB4
AB3
AA2 GPP_TX5P_C C136 0.1U/4/X7R/16V/K ML_OP <19>
AA1 GPP_TX5N_C C137 0.1U/4/X7R/16V/K ML_ON <19>
Y1
Y2
Y4
Y3
V1
V2
PLACE CAP CLOSE TO CONNECTOR
<13> A_RX0P A_RX0P AA8
<13> A_RX0N A_RX0N Y8
<13> A_RX1P A_RX1P AA7
<13> A_RX1N A_RX1N Y7
<13> A_RX2P A_RX2P AA5
<13> A_RX2N A_RX2N AA6
A_RX3P A_RX3P W5
<13> A_RX3N A_RX3N Y5
AD7 A_TX0P_C C138 0.1U/4/X7R/16V/K A_TX0P <13>
AE7 A_TX0N_C C139 0.1U/4/X7R/16V/K A_TX0N <13>
AE6 A_TX1P_C C140 0.1U/4/X7R/16V/K A_TX1P <13>
AD6 A_TX1N_C C141 0.1U/4/X7R/16V/K A_TX1N <13>
AB6 A_TX2P_C C142 0.1U/4/X7R/16V/K A_TX2P <13>
AC6 A_TX2N_C C143 0.1U/4/X7R/16V/K A_TX2N <13>
AD5 A_TX3P_C C144 0.1U/4/X7R/16V/K A_TX3P <13>
AE5 A_TX3N_C C145 0.1U/4/X7R/16V/K A_TX3N <13>
PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)
AC8 R210 1.27K/4/1
AB8 R212 2K/4/1
NB_VCC
NB_HS
NB_HS/[12SP2-01A004-G2R_12SP2-01A004-G1R]
GIGABYTE
Title
RS780 HT-LINK I/F
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Rev 1.32
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RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

RS740_DFT_GPIO1 — R272 — 150/4/1

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

<23> DAC_VSYNC — R276 — 3K/4/1 — VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

<23> DAC_HSYNC — R285 — 3K/4/1 — VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

U3C — PART 3 OF 6 — RS880P(880G)/S

CRT/TVOUT: AVDD1(NC), AVDD2(NC), AVDDDI(NC), AVSSDI(NC), AVDDQ(NC), AVSSQ(NC), C_Pr(DFT_GPIO5), Y(DFT_GPIO2), COMP_Pb(DFT_GPIO4), RED(DFT_GPIO0), REDb(NC), GREEN(DFT_GPIO1), GREENb(NC), BLUE(DFT_GPIO3), BLUEb(NC), DAC_HSYNC(PWM_GPIO4), DAC_VSYNC(PWM_GPIO6), DAC_SDA(PCE_TCALRN), DAC_SCL(PCE_RCALRN), DAC_RSET(PWM_GPIO1)

PLL PWR LVTM: PLLVDD(NC), PLLVDD18(NC), PLLVSS(NC), VDDA18HTPLL, VDDA18PCIEPLL1, VDDA18PCIEPLL2

PM: SYSRESETb, POWERGOOD, LDTSTOPb, ALLOW_LDTSTOP

CLOCKs: HT_REFCLKP, HT_REFCLKN, REFCLK_P/OSCIN(OSCIN), REFCLK_N(PWM_GPIO3), GFX_REFCLKP, GFX_REFCLKN, GPP_REFCLKP, GPP_REFCLKN, GPPSB_REFCLKP(SB_REFCLKP), GPPSB_REFCLKN(SB_REFCLKN)

MIS.: I2C_DATA, I2C_CLK, DDC_DATA/AUX0P(NC), DDC_CLK/AUX0N(NC), AUX1P(NC), AUX1N(NC), STRP_DATA, RSVD, AUX_CAL(NC)

TXOUT_L0P(NC) … TXOUT_L3N(DBG_GPIO2) → TXD0+ … TXD2- <22>

TXOUT_U0P(NC) … TXOUT_U3N(NC) → TXD0+ R242 130/4/1/X TXD0-; TXD1+ R243 130/4/1/X TXD1-; TXD2+ R244 130/4/1/X TXD2-; TXC+ R245 130/4/1/X TXC-

TXCLK_LP(DBG_GPIO1) … TXCLK_UN(PCIE_RESET_GPIO1) → TXC+ <22>, TXC- <22>

VDDLTP18(NC), VSSLTP18(NC), VDDLT18_1(NC), VDDLT18_2(NC), VDDLT33_1(NC), VDDLT33_2(NC), VSSLT1(VSS) … VSSLT7(VSS), LVDS_DIGON(PCE_TCALRP), LVDS_BLON(PCE_RCALRP), LVDS_ENA_BL(PWM_GPIO2)

VCC18 — BC150 — BC151 — 1U/6/Y5V/10V/Z — 0.1U/4/Y5V/16V/Z

VDDLT18 — Q74 (P8503BMG/SOT23/450pF/85m) — +12V — R156 — 8.2K/4/1 — VCC18

BC145 — BC146 — 0.1U/4/Y5V/16V/Z — 1U/6/Y5V/10V/Z

TMDS_HPD(NC), HPD(NC) → TMDS_HPD <22>

TVCLKIN(PWM_GPIO5) → -SUS_STAT <14>

THERMALDIODE_P, THERMALDIODE_N, TESTMODE

TEST_EN — R279 — 1.8K/4/1

U3D — PAR 4 OF 6 — SBD_MEM/DVO_I/F — RS880P(880G)/S

MEM_A0(NC) … MEM_A13(NC), MEM_BA0(NC), MEM_BA1(NC), MEM_BA2(NC), MEM_RASb(NC), MEM_CASb(NC), MEM_WEb(NC), MEM_CSb(NC), MEM_CKE(NC), MEM_ODT(NC), MEM_CKP(NC), MEM_CKN(NC), MEM_COMPP(NC), MEM_COMPN(NC)

MEM_DQ0/DVO_VSYNC(NC) … MEM_DQ15/DVO_D11(NC), MEM_DQS0P/DVO_IDCKP(NC), MEM_DQS0N/DVO_IDCKN(NC), MEM_DQS1P(NC), MEM_DQS1N(NC), MEM_DM0(NC), MEM_DM1/DVO_D8(NC), IOPLLVDD18(NC), IOPLLVDD(NC), IOPLLVSS(NC), MEM_VREF(NC)

VCC18 — BC60 — 0.1u/4/Y5V/16V/Z; NB_VCC — BC61 — 0.1u/4/Y5V/16V/Z

SR1~SR3 PLACED WITHIN 1' OF NB: SR3 150/4/1, SR2 150/4/1, SR1 140/4/1

R159 150/4/1 — REFCLKN — R158 150/4/1

R265 — 8.2K/4/1 — STRP_DATA

RS740_DFT_GPIO1 — C8

SBC34 1U/6/Y5V/10V/Z; BC139; SBC29 1U/6/Y5V/10V/Z; SBC35 10U/8/X5R/6.3V/K; BC143 1U/6/Y5V/10V/Z; SBC36 1U/6/Y5V/10V/Z; SBC15 0.1u/4/Y5V/16V/Z; BC141 1U/6/Y5V/10V/Z

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Size	Custom
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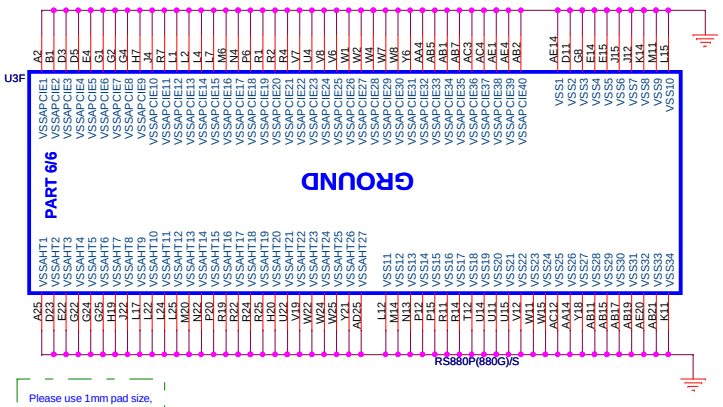
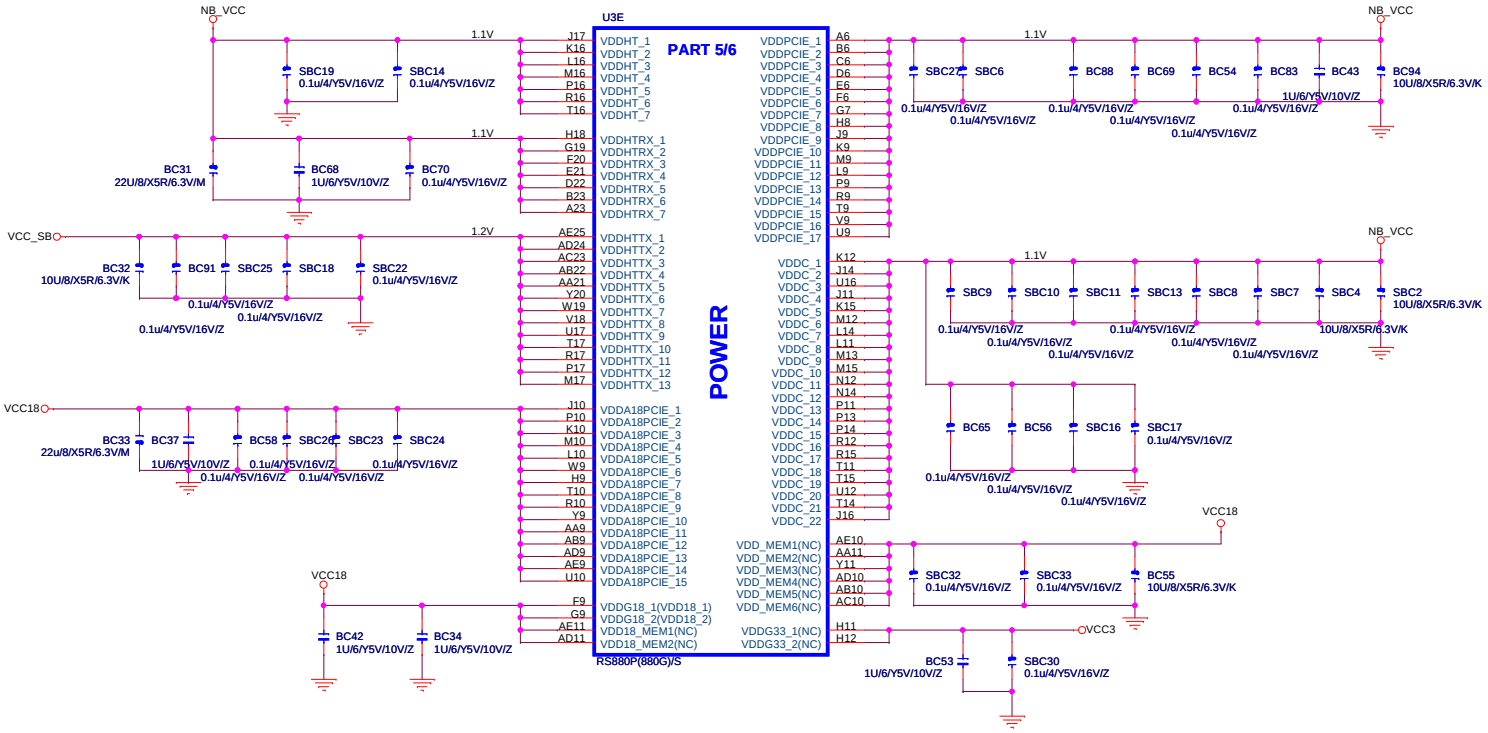
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



Please use 1mm pad size, place all ELT test pads on bottom side only



Title	RS780 POWER & GND	
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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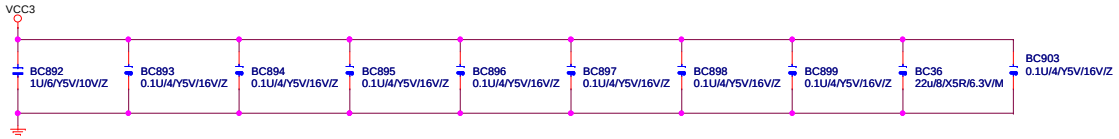


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

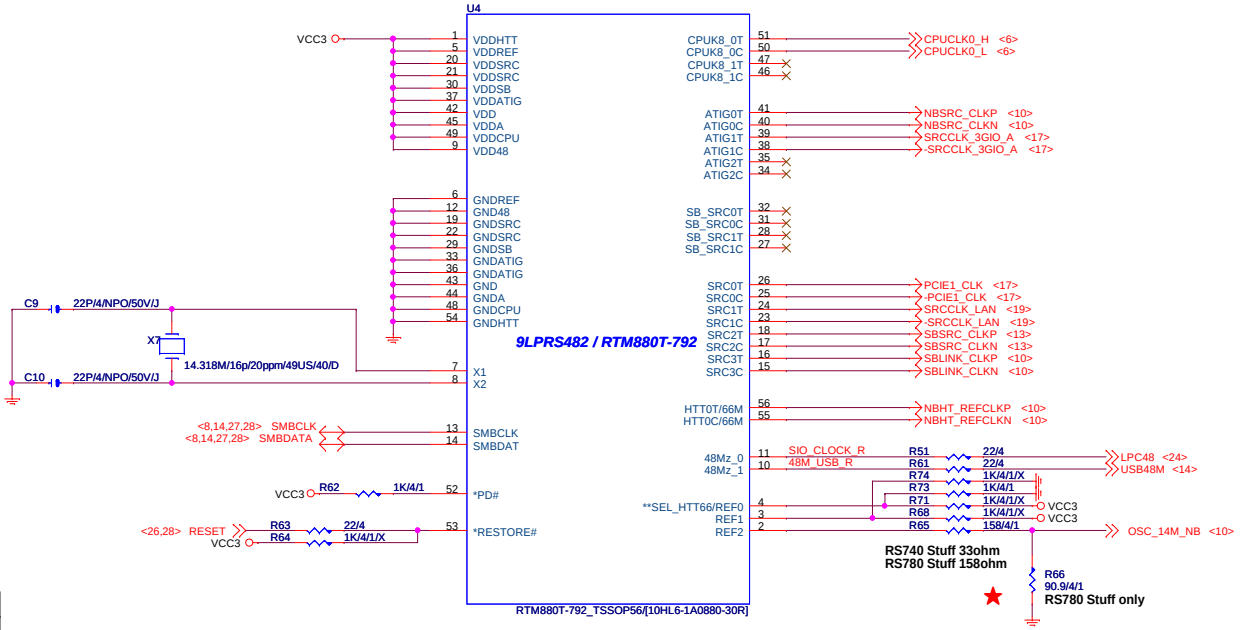
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

GIGABYTE™

Title: ICS9LPRS477		
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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030005-42R_12SP2-030005-41R_12SP2-030005-43R]

U2A

SB700 Part 1 of 5

PCI EXPRESS INTERFACE

PCI CLKS

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC XTAL

CPU

RTC

SB710/FCBGA528/A14/[10HB1-06B710-11R]

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

EMI 20071107

SHW/D0.64*5.08*6.74

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting
EC AOD-ACC

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

GIGABYTE™

Title: ATI SB710 PCIE/PCI/CPU/LPC

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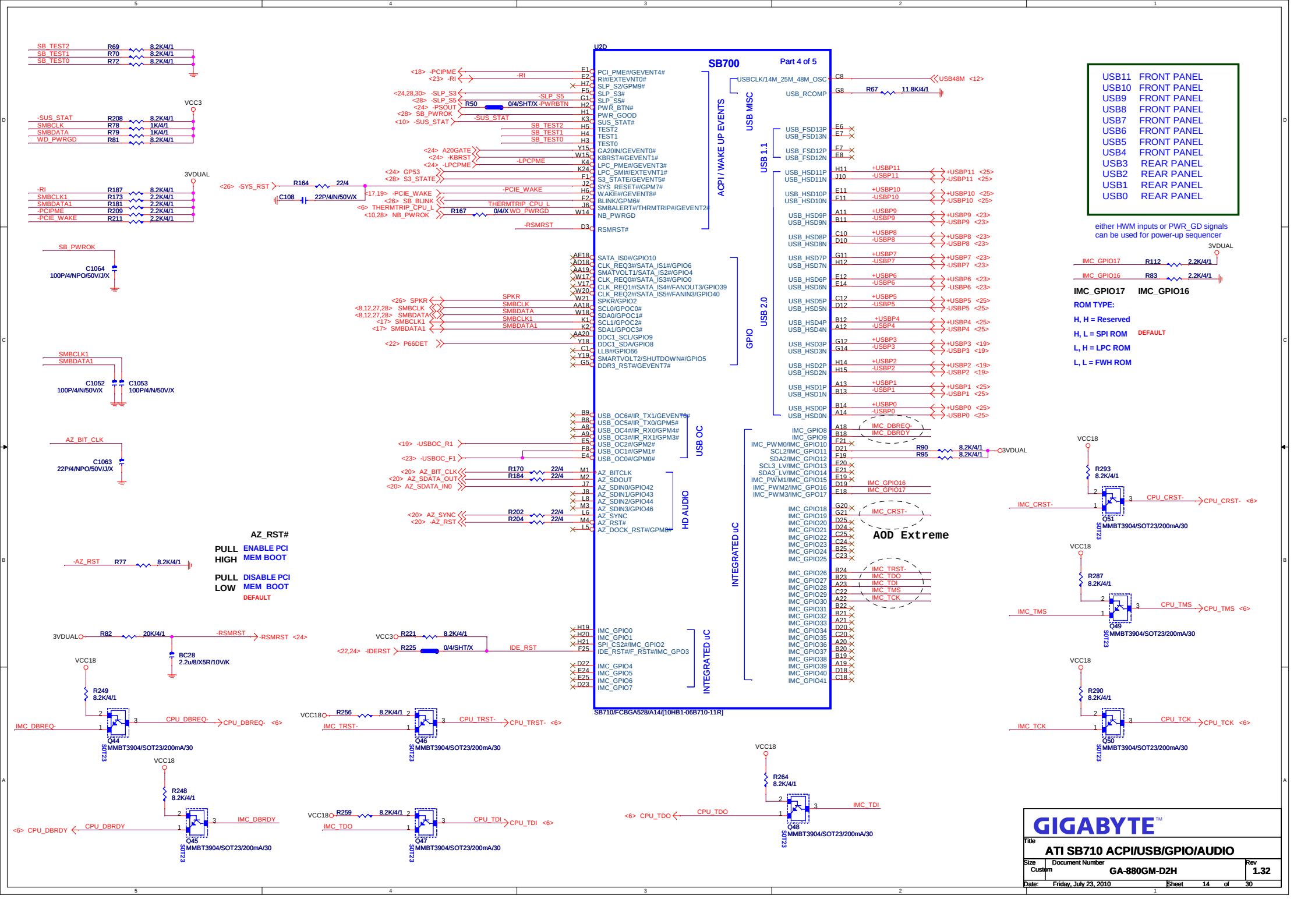
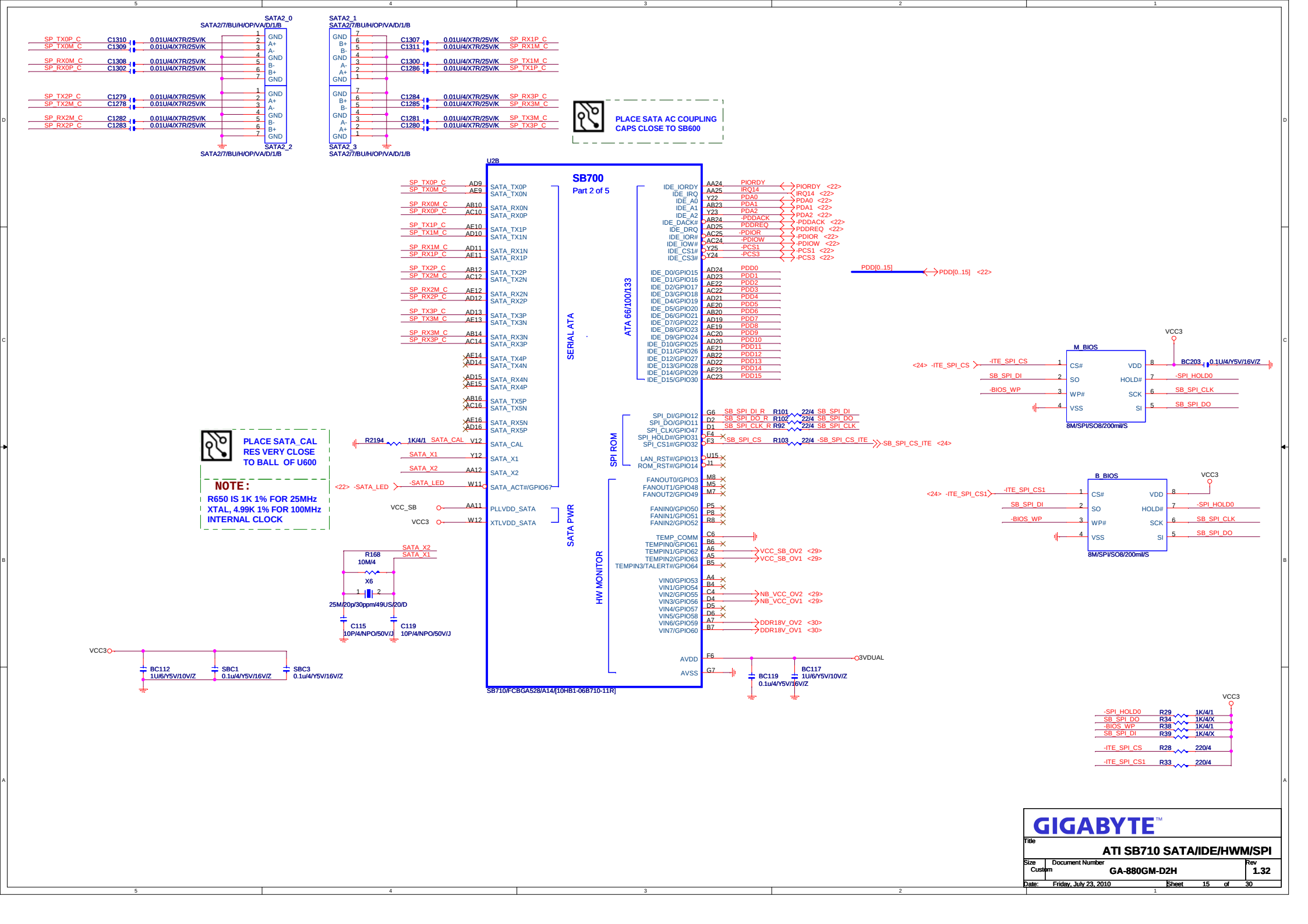

SB700
Part 4 of 5
U2D
SB710/FCBGA528/A14/[10HB1-06B710-11R]
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMATVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCLD/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
AOD Extreme
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals can be used for power-up sequencer
IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
AZ_RST#
PULL HIGH ENABLE PCI MEM BOOT
PULL LOW DISABLE PCI MEM BOOT DEFAULT
MMBT3904/SOT23/200mA/30
SOT23
GIGABYTE
Title
ATI SB710 ACPI/USB/GPIO/AUDIO
Size Custom
Document Number GA-880GM-D2H
Rev 1.32
Date: Friday, July 23, 2010
Sheet 14 of 30


SATA2_0
SATA2/7/BU/H/OP/VA/D/1/B
SATA2_1
SATA2/7/BU/H/OP/VA/D/1/B
SATA2_2
SATA2/7/BU/H/OP/VA/D/1/B
SATA2_3
SATA2/7/BU/H/OP/VA/D/1/B
PLACE SATA AC COUPLING CAPS CLOSE TO SB600
U2B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
SB710/FCBGA528/A14/{10HB1-06B710-11R}
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600
NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK
M_BIOS
8M/SPI/SO8/200mil/S
B_BIOS
8M/SPI/SO8/200mil/S
VCC3
3VDUAL
GIGABYTE
ATI SB710 SATA/IDE/HWM/SPI
GA-880GM-D2H
1.32
Friday, July 23, 2010
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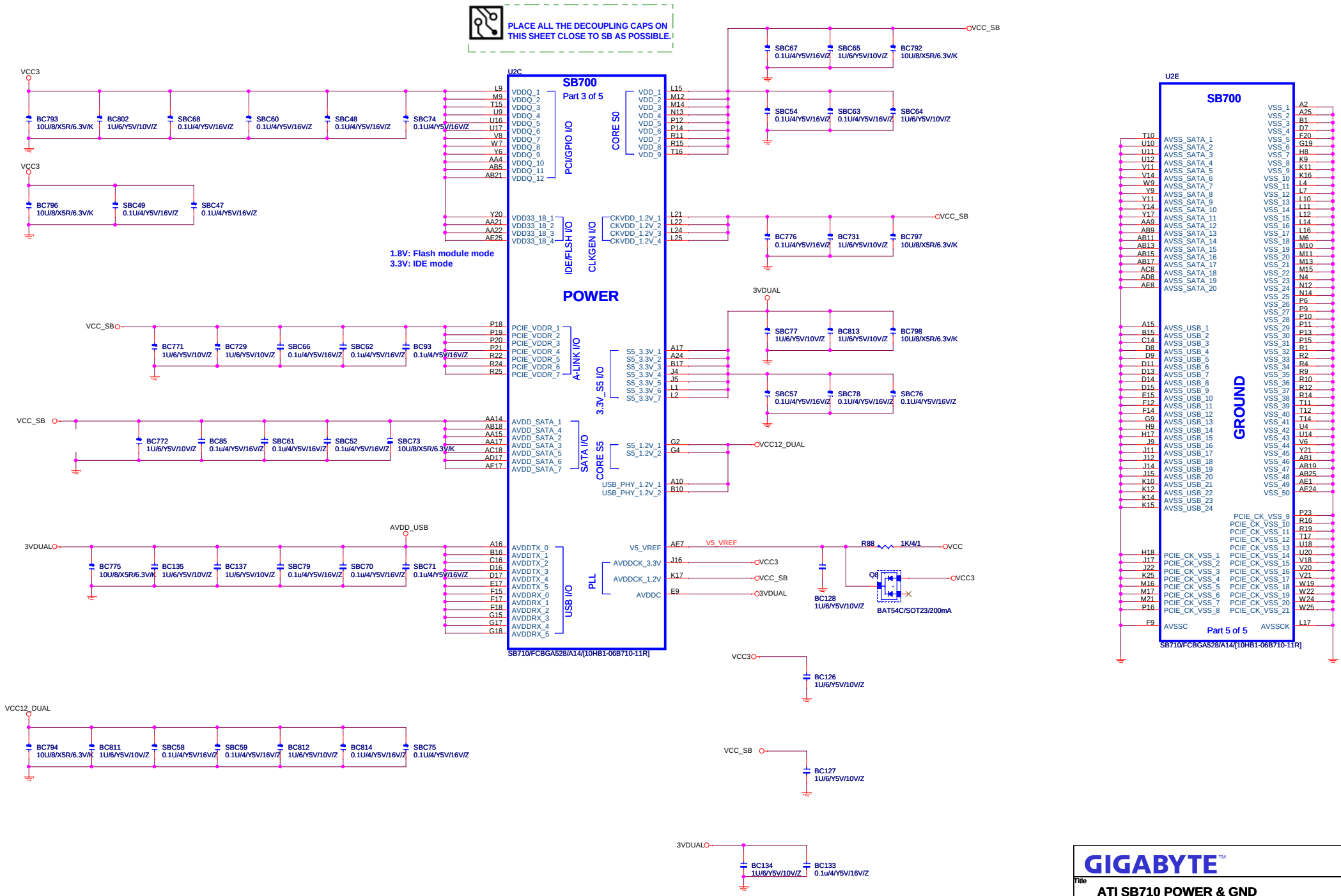
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
U2C
SB700
Part 3 of 5
POWER
1.8V: Flash module mode
3.3V: IDE mode
SB710/FCBGA528/A14/[10HB1-06B710-11R]
U2E
SB700
GROUND
Part 5 of 5
SB710/FCBGA528/A14/[10HB1-06B710-11R]
VCC3
VCC_SB
3VDUAL
VCC12_DUAL
AVDD_USB
V5_VREF
VCC
VCC3
VCC_SB
3VDUAL
BAT54C/SOT23/200mA
1K/4/1
GIGABYTE
ATI SB710 POWER & GND
GA-880GM-D2H
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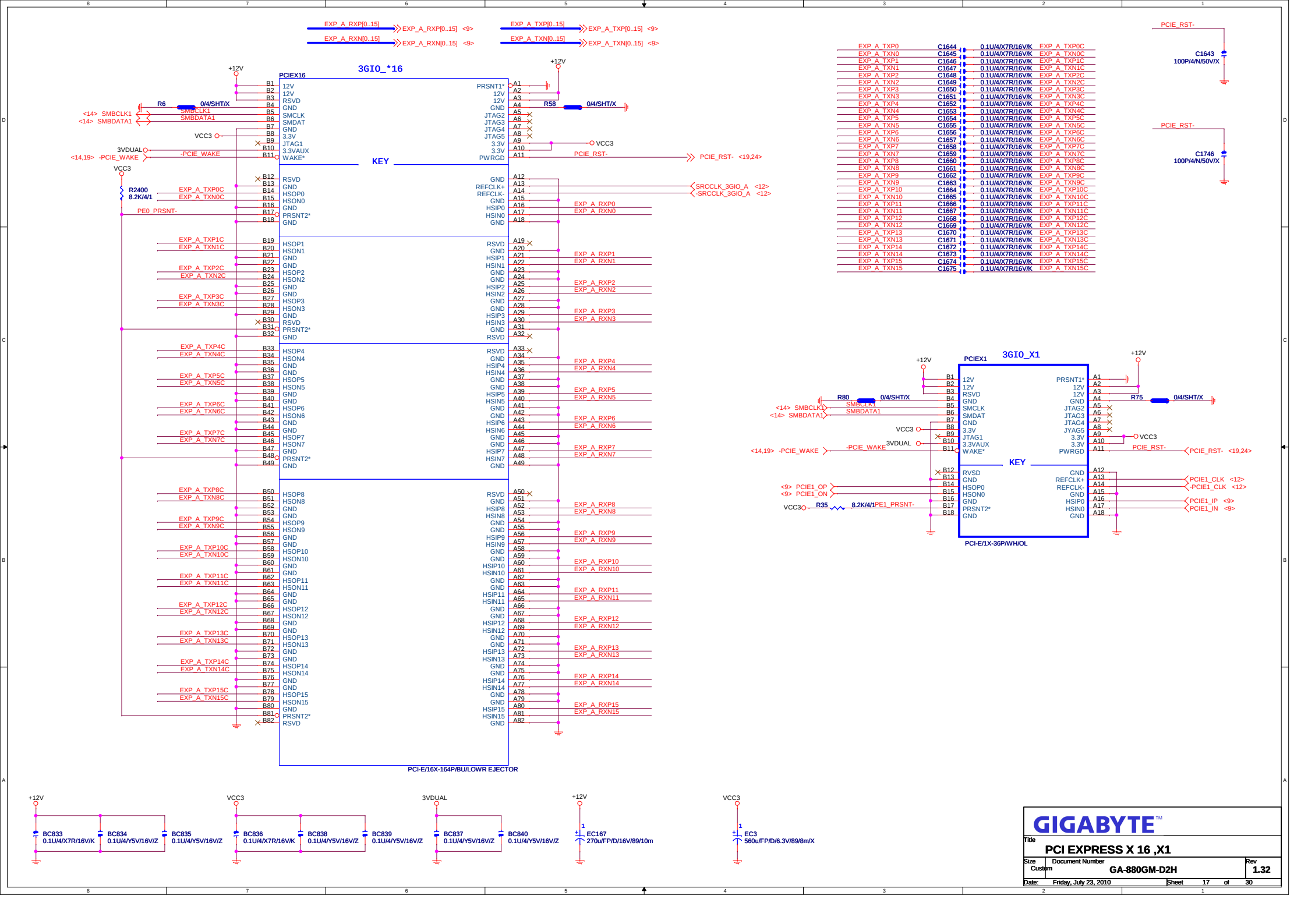
16
30



GIGABYTE™

Title	PCI EXPRESS X 16 ,X1
Size	Custom
Document Number	GA-880GM-D2H
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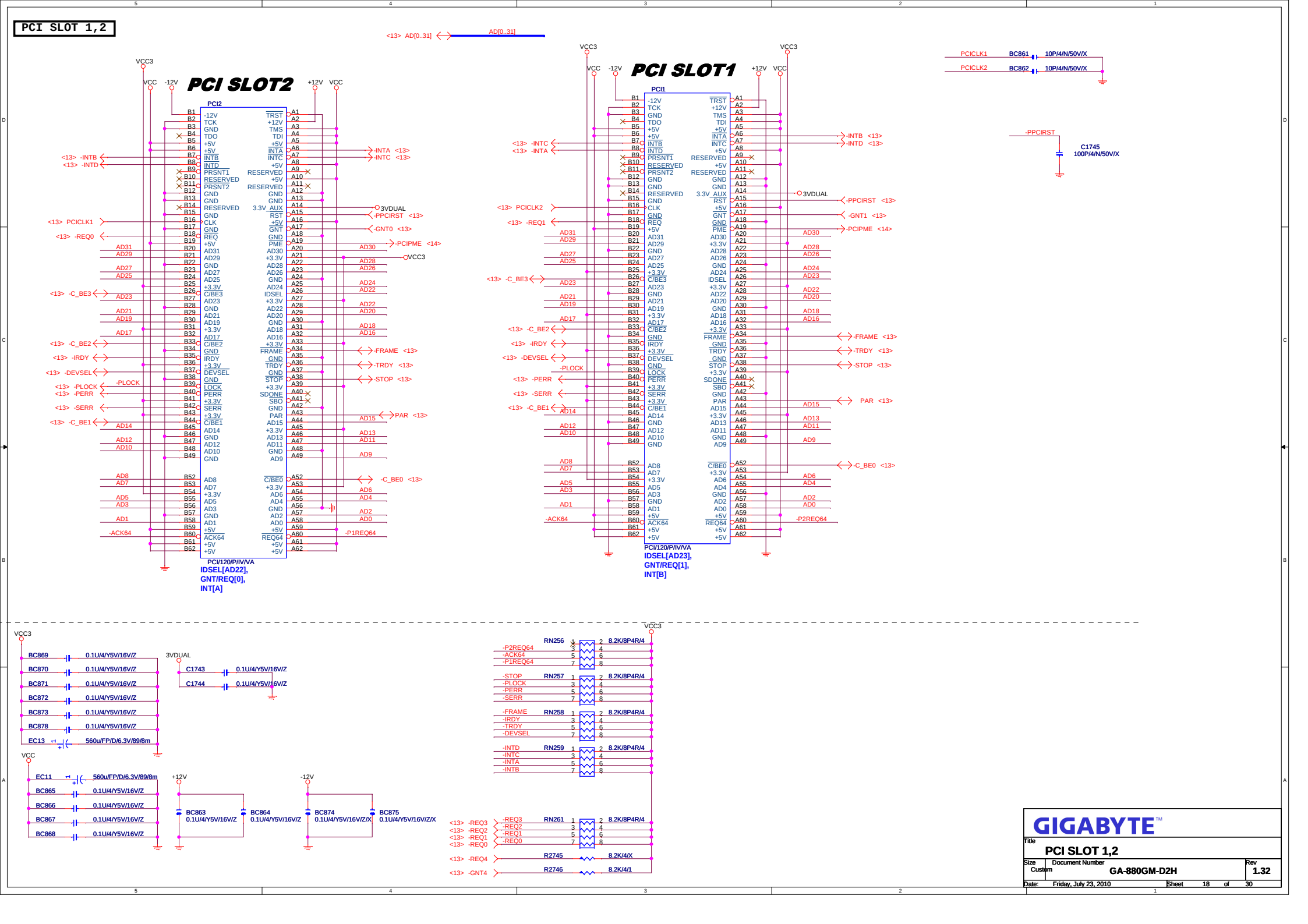
PCI SLOT 1,2



Title	PCI SLOT 1,2		
Size	Document Number		Rev
Custom	GA-880GM-D2H		1.32
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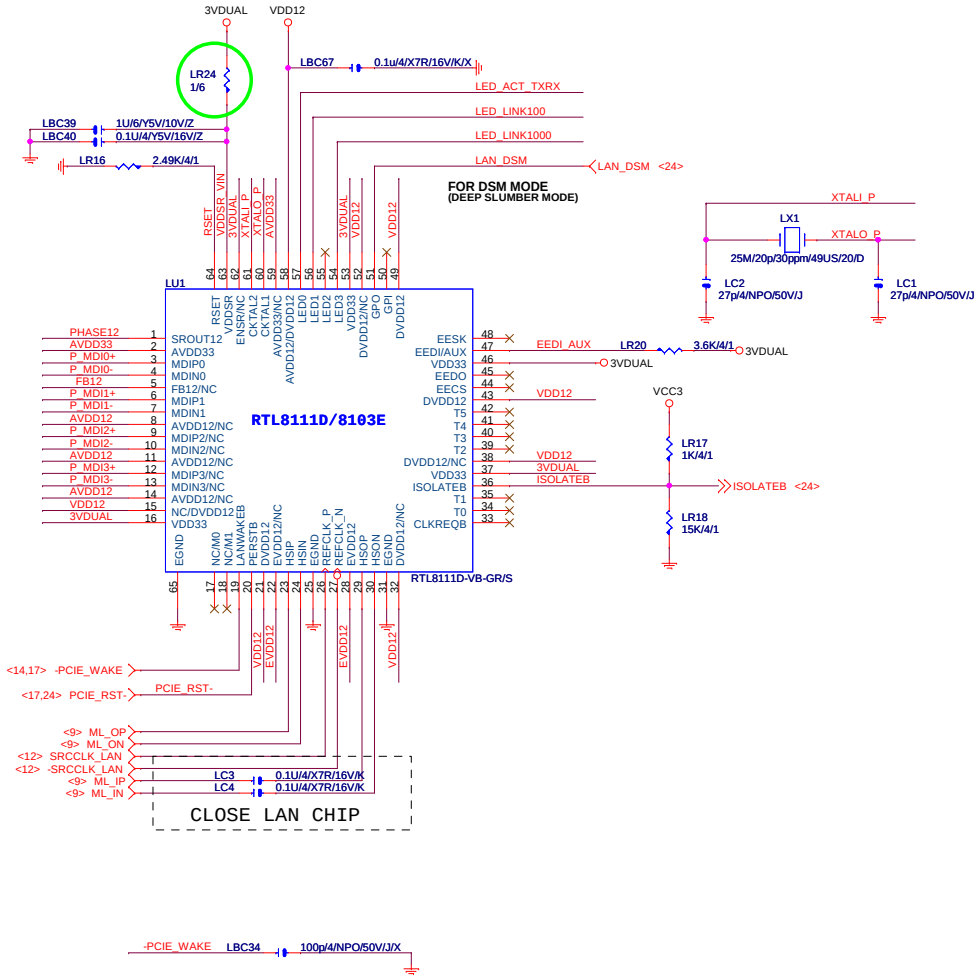
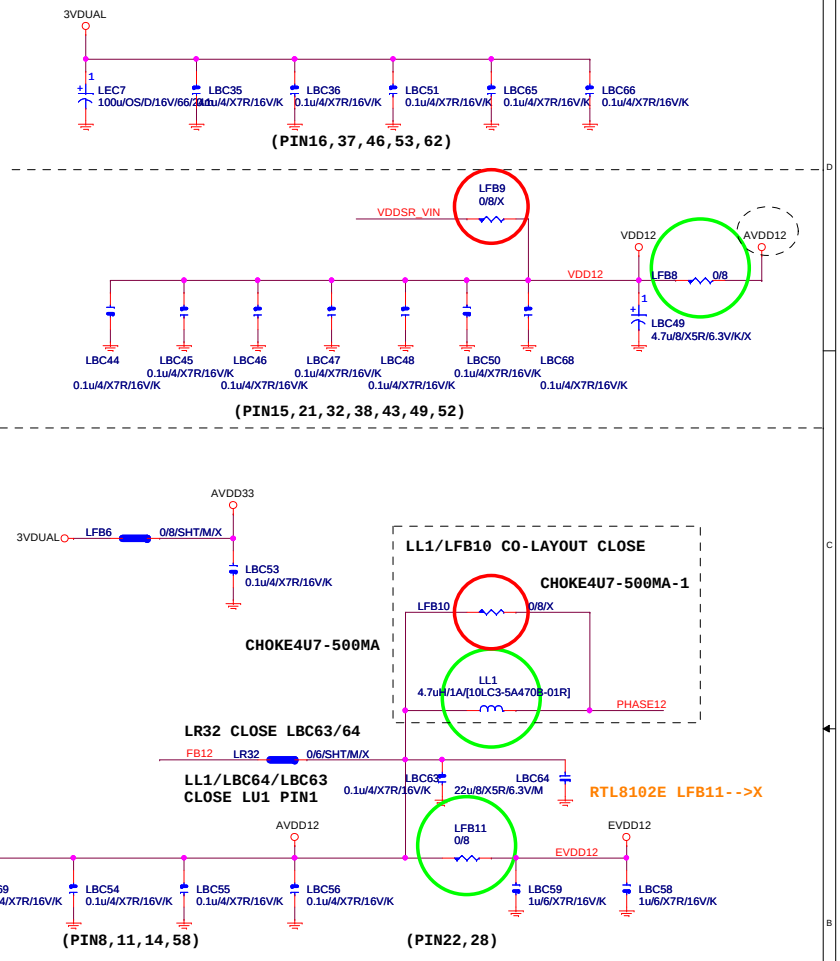
PCIE-1G LAN

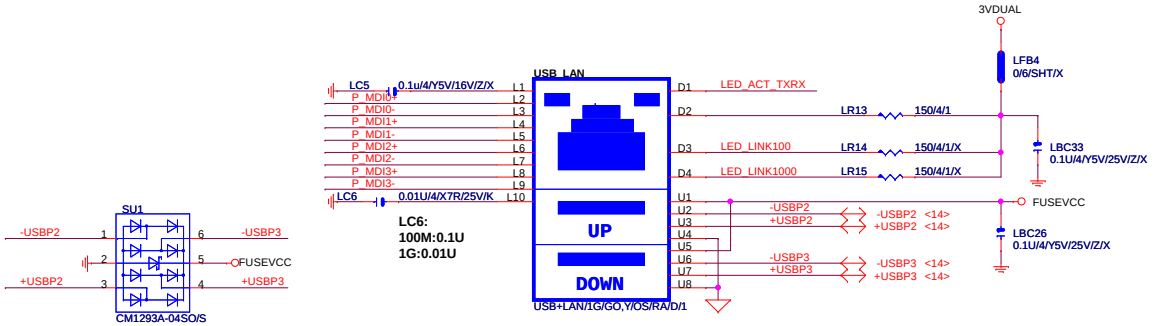


=>RTL8111D.
=>RTL8103E

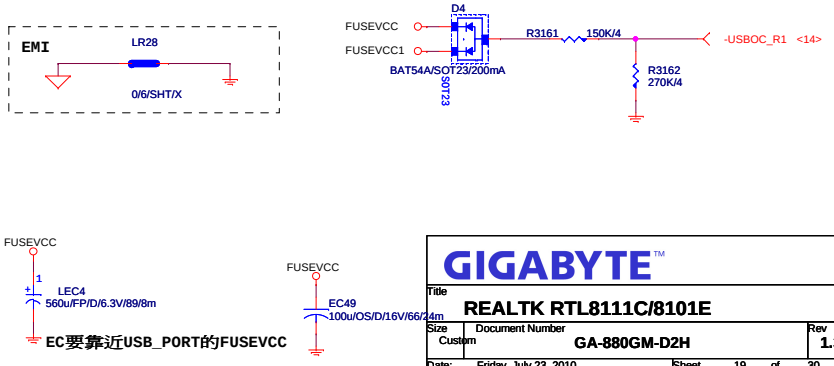


USB_LAN CONNECTOR

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1



USB_LAN



GIGABYTE™

Title	REALTK RTL8111C/8101E	
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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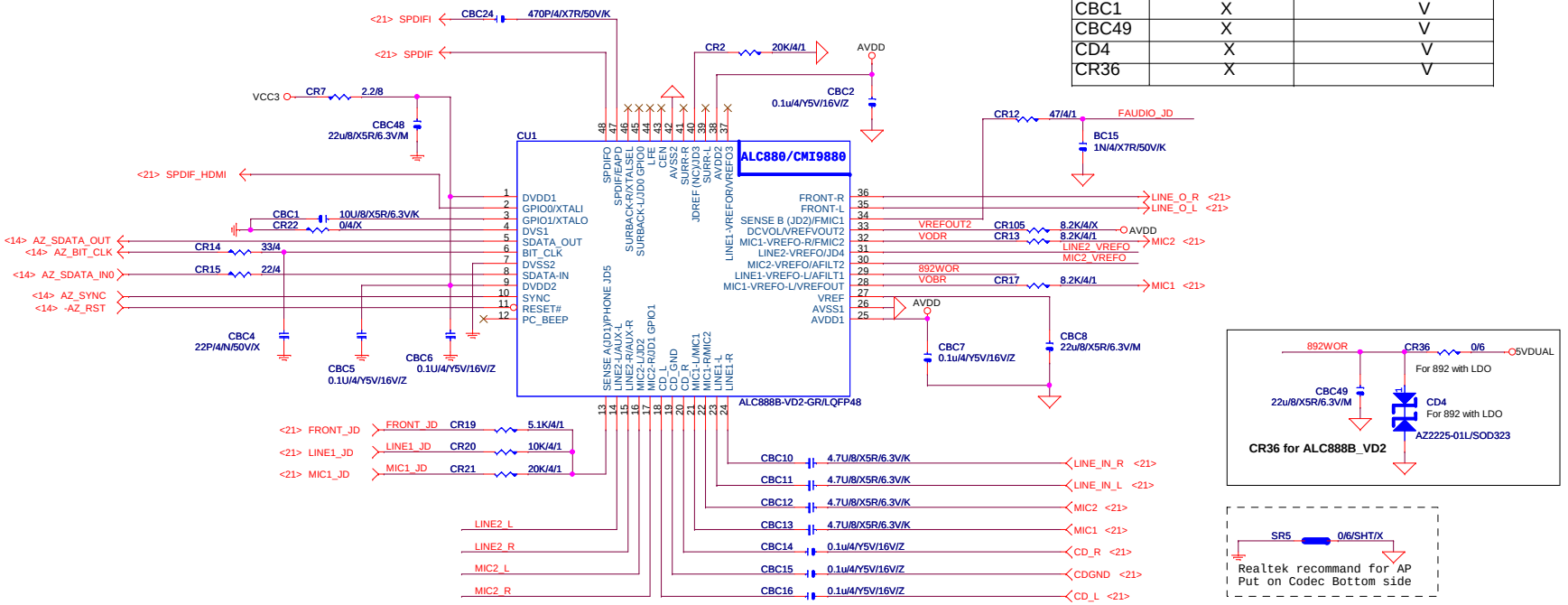
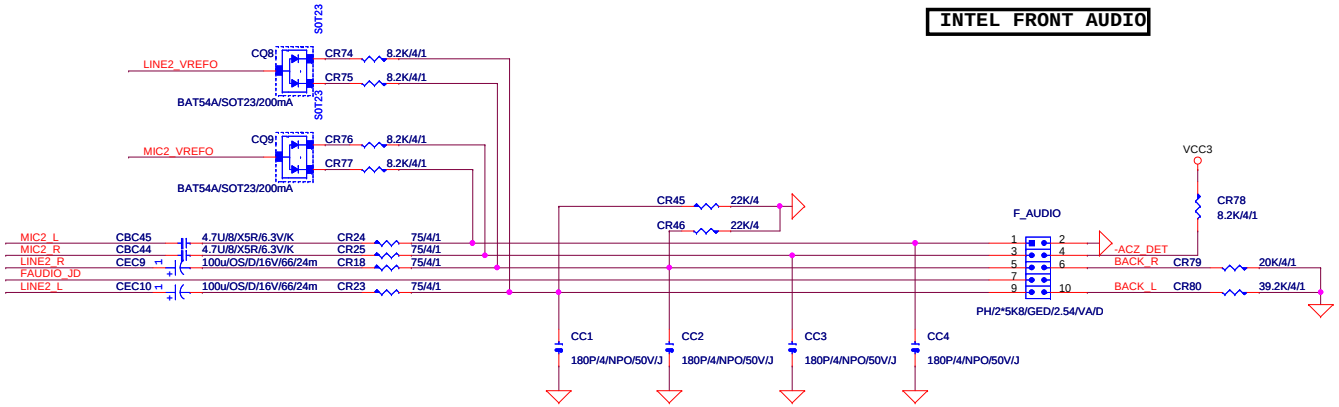
	ALC888B	ALC888B-VD2
CBC1	X	V
CBC49	X	V
CD4	X	V
CR36	X	V

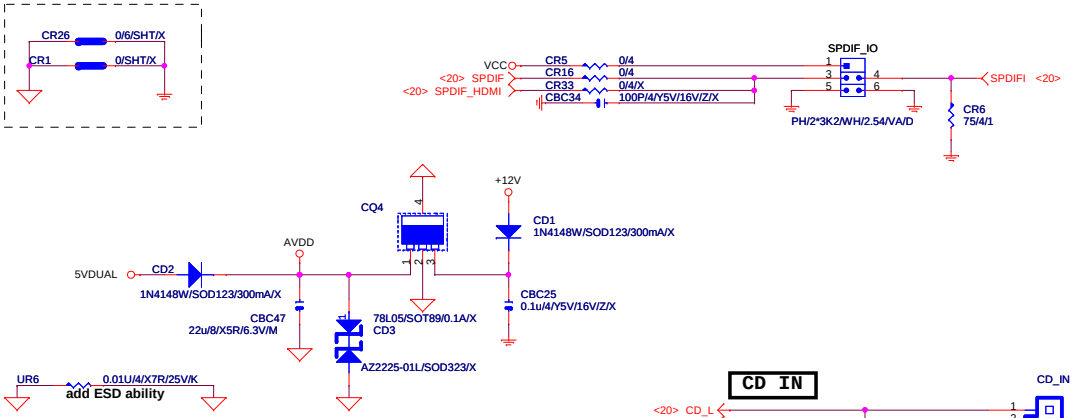


INTEL FRONT AUDIO

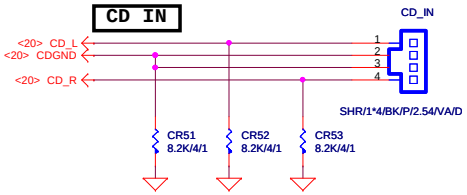


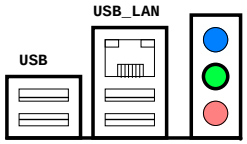
GIGABYTE™

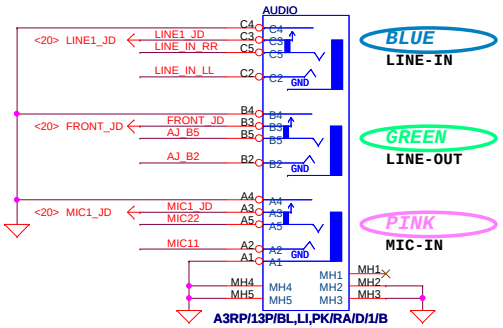
Title	ALC888B CODEC	
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
Date: Friday, July 23, 2010	Sheet 20 of 30	

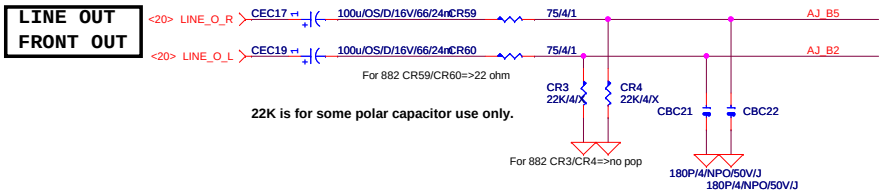


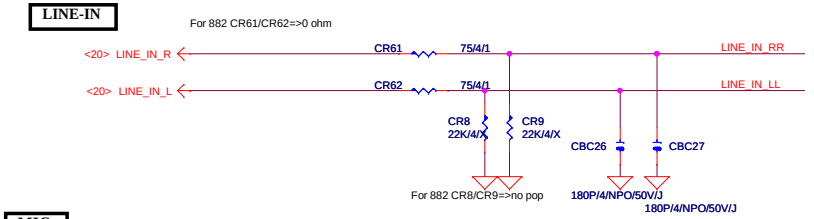
	ALC888B	ALC888B-VD2
CBC25	V	X
CBC47	V	V
CQ4	X	X
CD3	V	X
CD1 / CD2	V	X

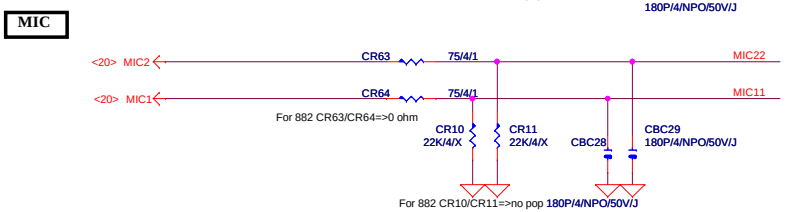












GIGABYTE™

Title	AUDIO JACK	
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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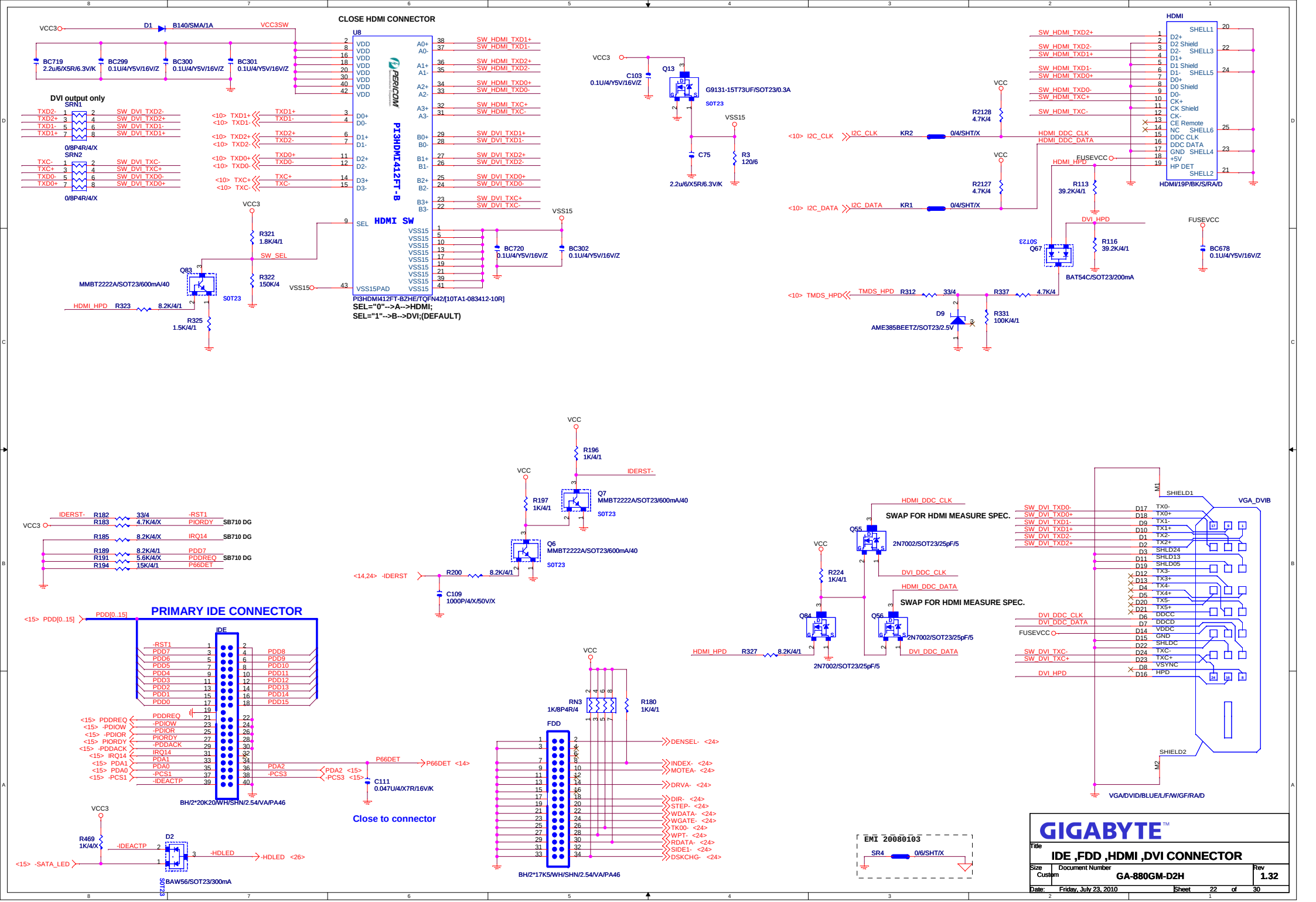
CLOSE HDMI CONNECTOR
U8
PI3HDMI412FT-B
HDMI SW
PI3HDMI412FT-BZHE/TQFN42/[10TA1-083412-10R]
SEL="0"-->A-->HDMI;
SEL="1"-->B-->DVI;(DEFAULT)
DVI output only
SRN1
SRN2
0/8P4R/4X
HDMI
HDMI/19P/BK/S/RA/D
MMBT2222A/SOT23/600mA/40
BAT54C/SOT23/200mA
AME385BEETZ/SOT23/2.5V
2N7002/SOT23/25pF/5
SWAP FOR HDMI MEASURE SPEC.
PRIMARY IDE CONNECTOR
IDE
BH/2*20K20/WH/SHN/2.54/VA/PA46
Close to connector
FDD
BH/2*17K5/WH/SHN/2.54/VA/PA46
BAW56/SOT23/300mA
VGA_DVIB
VGA/DVID/BLUE/L/F/W/GF/RA/D
EMI 20080103
GIGABYTE
IDE ,FDD ,HDMI ,DVI CONNECTOR
GA-880GM-D2H
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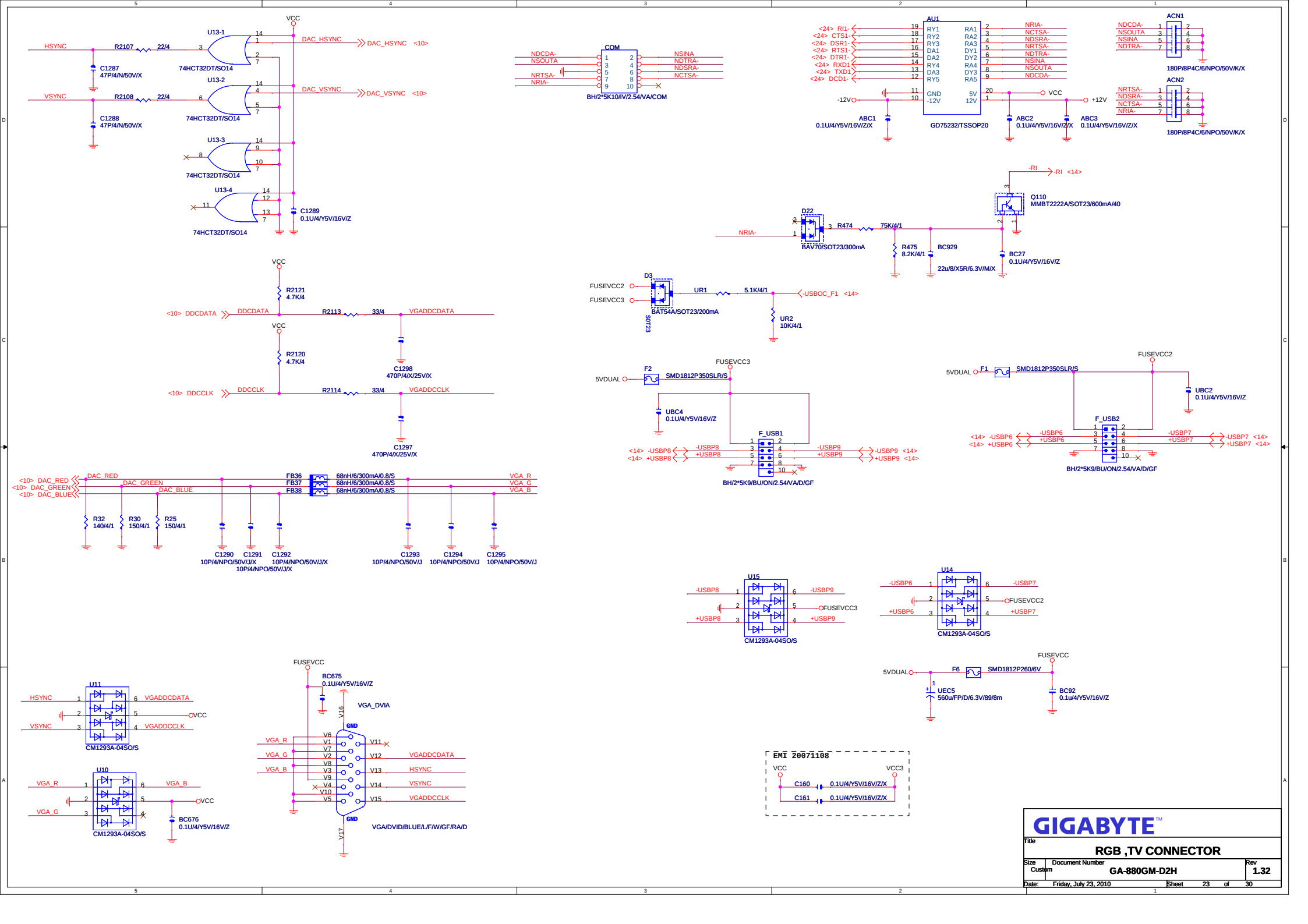

GIGABYTE™			
Title: RGB ,TV CONNECTOR			
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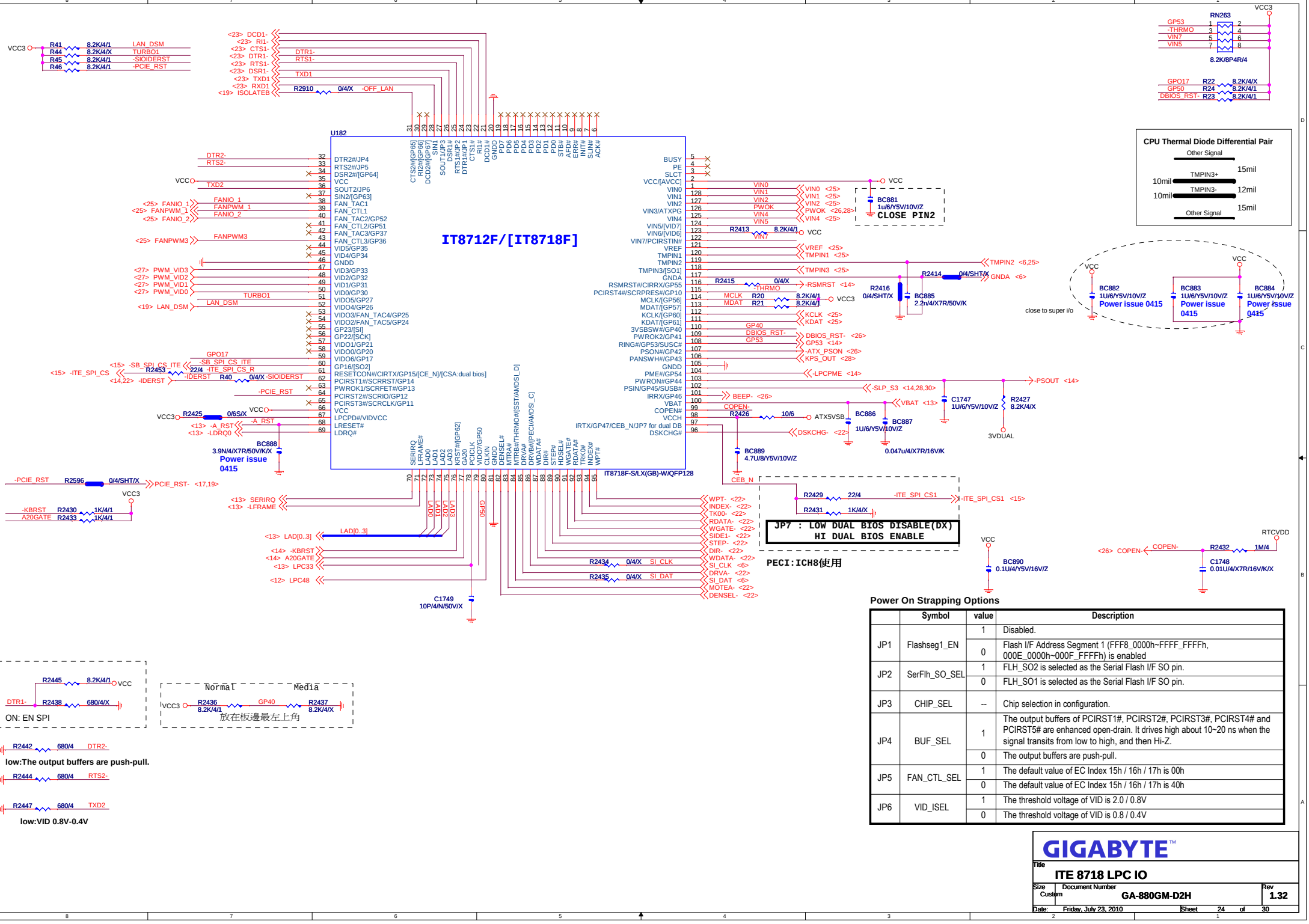

Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

GIGABYTE™

Title: ITE 8718 LPC IO

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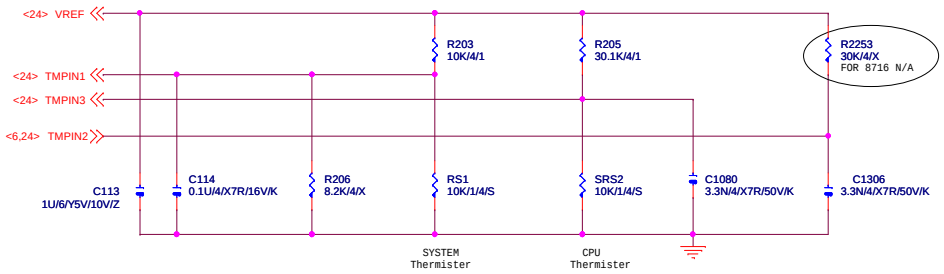
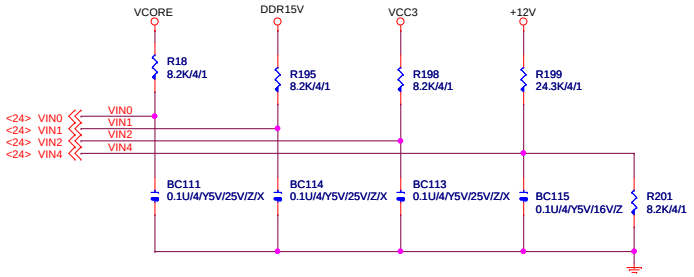
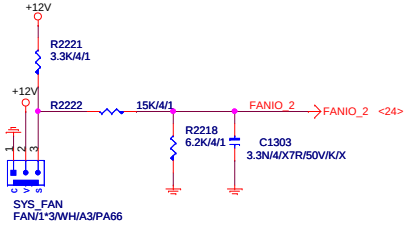
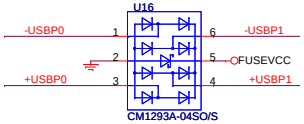
Hardware Monitor circuits



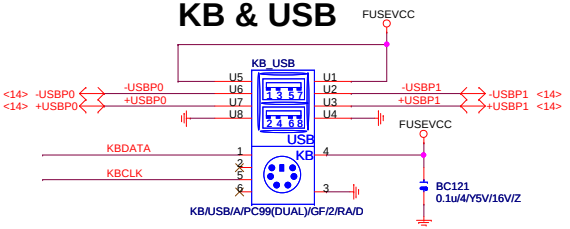


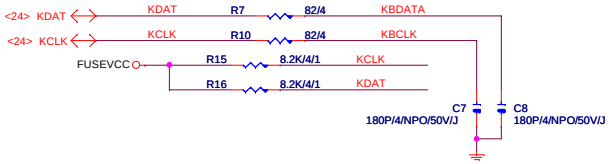
SYSTEM FAN



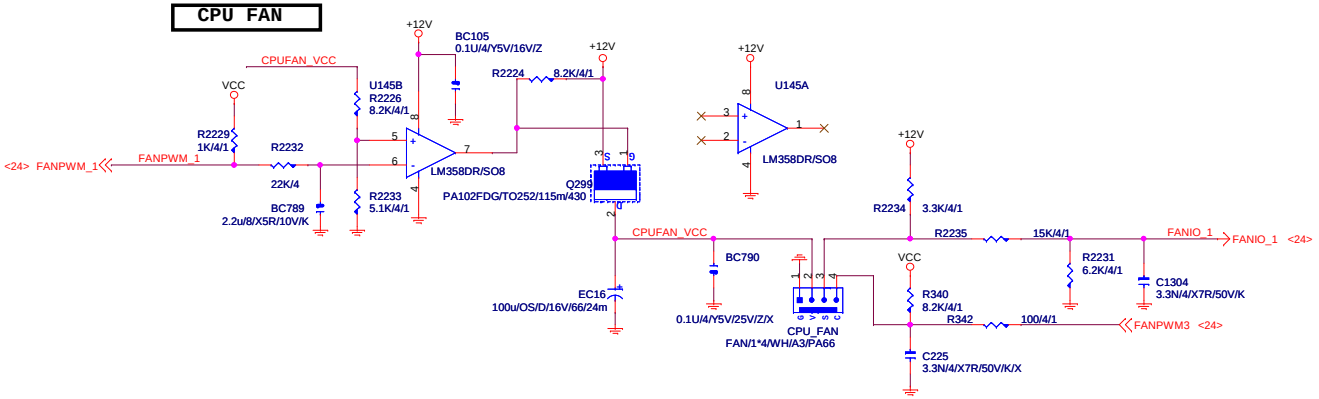


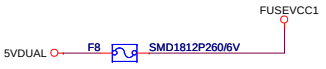
KB & USB

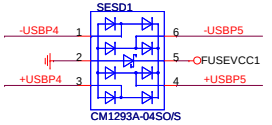


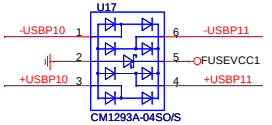


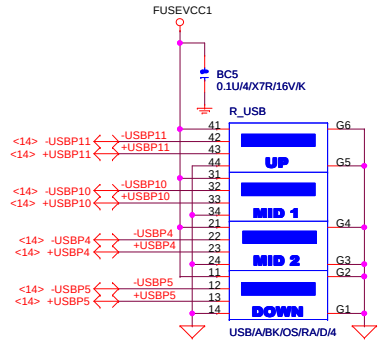
CPU FAN











GIGABYTE™

Title	FAN/HWMO ,KB/USB	
Size: Custom	Document Number: GA-880GM-D2H	Rev: 1.32
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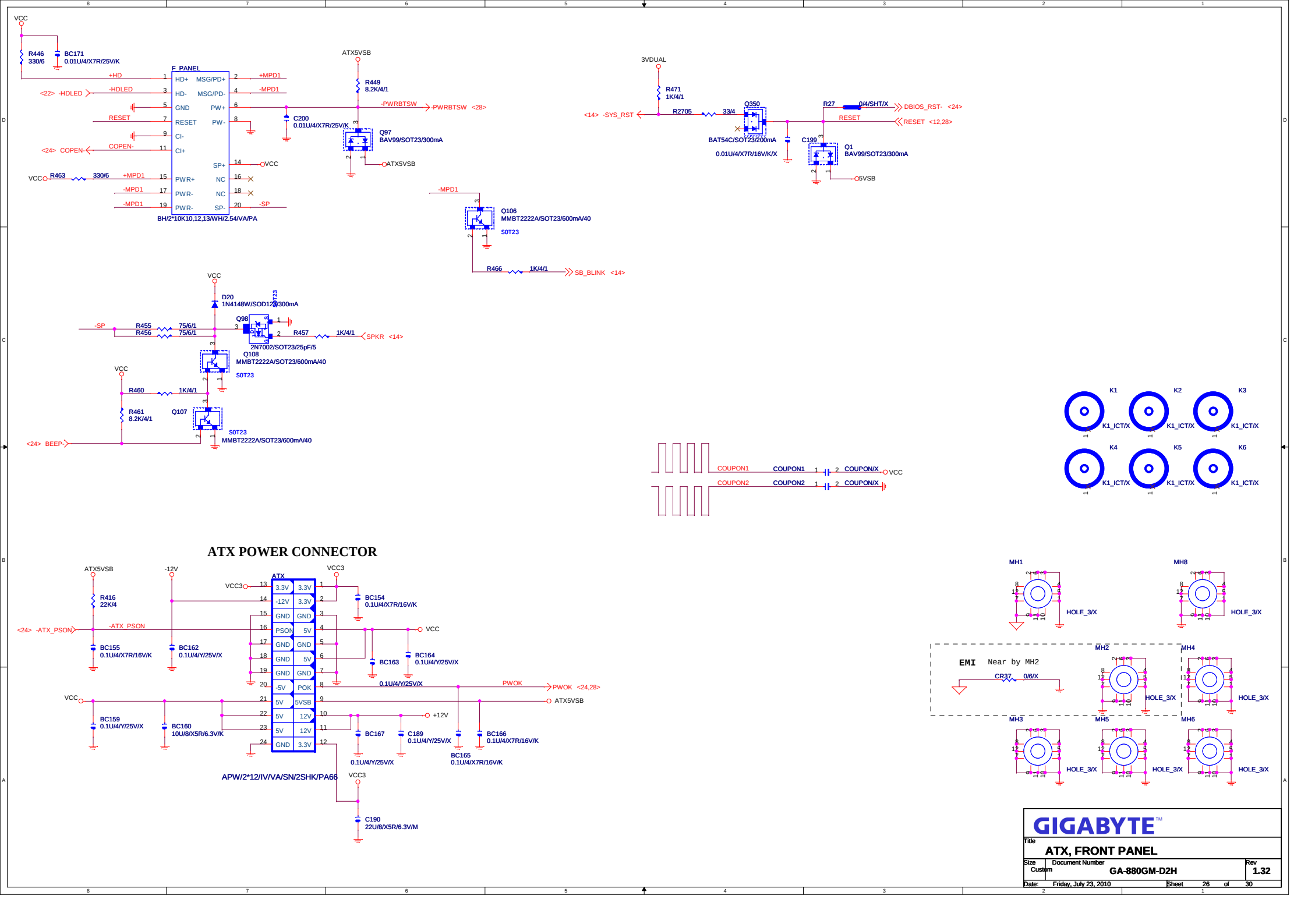
VCC
R446 330/6
BC171 0.01U/4/X7R/25V/K
F_PANEL
+HD
-HDLED
<22> -HDLED
RESET
COPEN-
<24> COPEN-
HD+
HD-
GND
RESET
CI-
CI+
PW+
PW-
SP+
PWR+
PWR-
PWR-
MSG/PD+
MSG/PD-
NC
NC
SP-
+MPD1
-MPD1
-SP
VCC
R463 330/6 +MPD1
-MPD1
-MPD1
BH/2*10K10,12,13/WH/2.54/VA/PA
ATX5VSB
R449 8.2K/4/1
-PWRBTSW
<28> -PWRBTSW
C200 0.01U/4/X7R/25V/K
Q97 BAV99/SOT23/300mA
ATX5VSB
3VDUAL
R471 1K/4/1
<14> -SYS_RST
R2705
33/4
Q350
BAT54C/SOT23/200mA
0.01U/4/X7R/16V/K/X
R27 0/4/SHT/X
DBIOS_RST- <24>
RESET
RESET <12,28>
C199
Q1 BAV99/SOT23/300mA
5VSB
-MPD1
Q106 MMBT2222A/SOT23/600mA/40
S0T23
R466 1K/4/1
SB_BLINK <14>
VCC
D20 1N4148W/SOD123/300mA
-SP
R455 75/6/1
R456 75/6/1
Q98
2N7002/SOT23/25pF/5
R457 1K/4/1
SPKR <14>
Q108 MMBT2222A/SOT23/600mA/40
S0T23
VCC
R460 1K/4/1
R461 8.2K/4/1
Q107
S0T23 MMBT2222A/SOT23/600mA/40
<24> BEEP-
K1
K2
K3
K1_ICT/X
K4
K5
K6
COUPON1
COUPON2
COUPON/X
VCC
ATX POWER CONNECTOR
ATX5VSB
-12V
VCC3
ATX
3.3V
-12V
GND
PSON
GND
GND
GND
-5V
5V
5V
5V
GND
5V
3.3V
GND
5V
GND
POK
5VSB
12V
12V
3.3V
R416 22K/4
<24> -ATX_PSON
-ATX_PSON
BC155 0.1U/4/X7R/16V/K
BC162 0.1U/4/Y/25V/X
BC154 0.1U/4/X7R/16V/K
BC163
BC164 0.1U/4/Y/25V/X
0.1U/4/Y/25V/X
PWOK
PWOK <24,28>
ATX5VSB
+12V
BC159 0.1U/4/Y/25V/X
BC160 10U/8/X5R/6.3V/K
BC167
0.1U/4/Y/25V/X
C189 0.1U/4/Y/25V/X
BC165 0.1U/4/X7R/16V/K
BC166 0.1U/4/X7R/16V/K
APW/2*12/IV/VA/SN/2SHK/PA66
C190 22U/8/X5R/6.3V/M
MH1
MH8
HOLE_3/X
EMI
Near by MH2
CR37 0/6/X
MH2
MH4
MH3
MH5
MH6
GIGABYTE
Title
ATX, FRONT PANEL
Size
Custom
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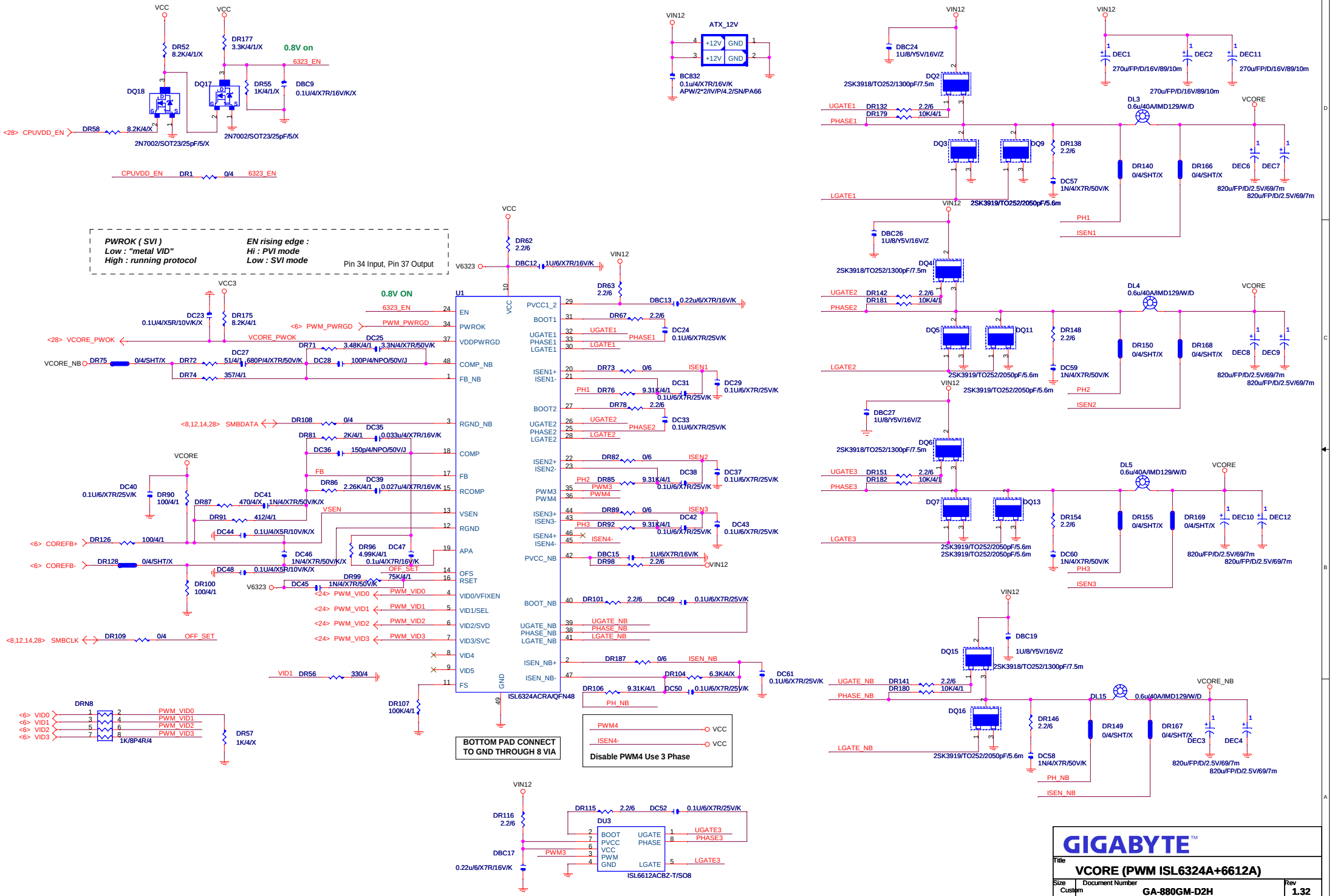
PWROK (SVI)
Low : "metal VID"
High : running protocol
EN rising edge :
Hi : PVI mode
Low : SVI mode
Pin 34 Input, Pin 37 Output
0.8V on
0.8V ON
ATX_12V
U1
ISL6324ACRA/QFN48
ISL6612ACBZ-T/SO8
2N7002/SOT23/25pF/5/X
2SK3918/TO252/1300pF/7.5m
2SK3919/TO252/2050pF/5.6m
BOTTOM PAD CONNECT TO GND THROUGH 8 VIA
Disable PWM4 Use 3 Phase
GIGABYTE
VCORE (PWM ISL6324A+6612A)
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Custom
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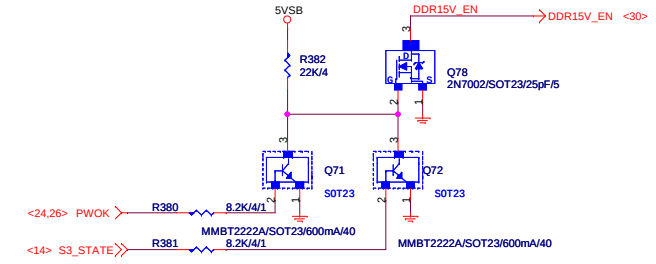
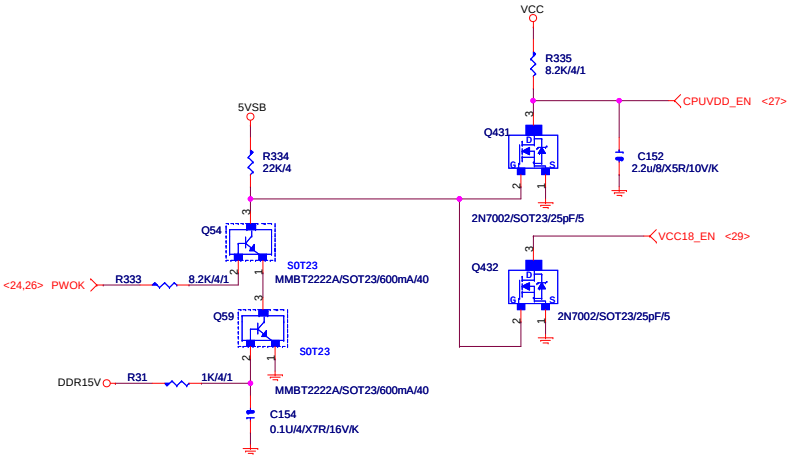
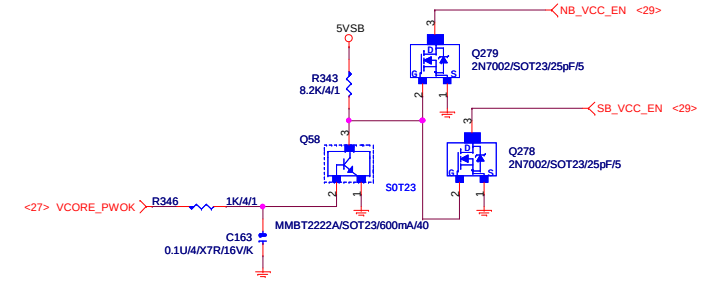
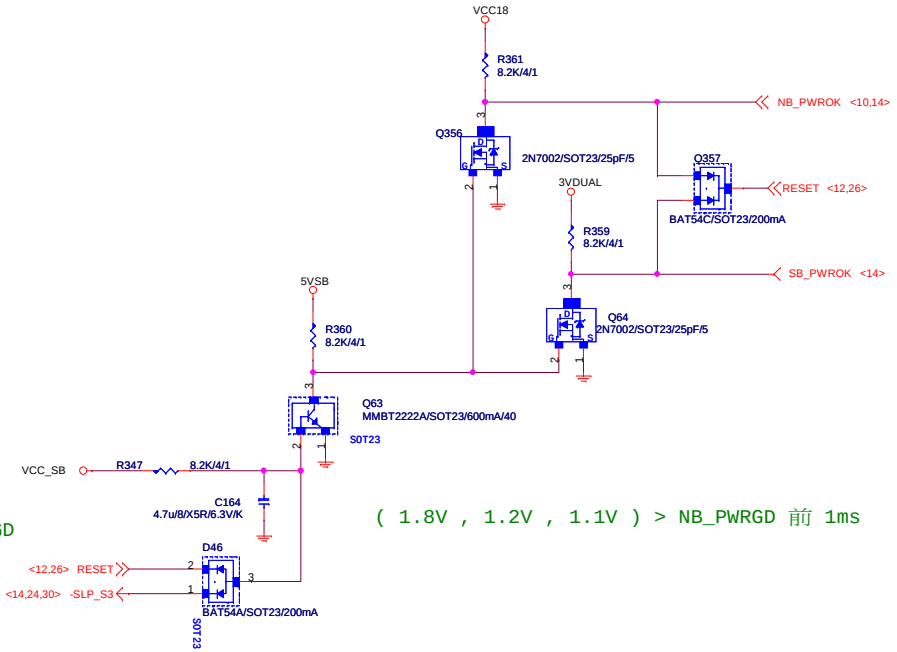


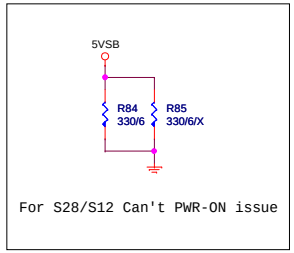




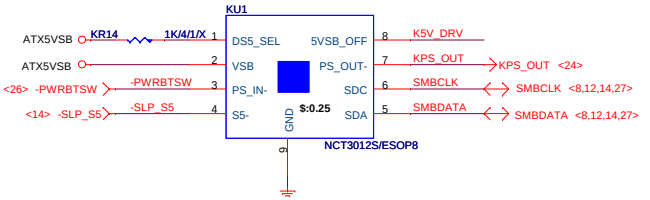
PWOK > NB_PWRGD / SB_PWRGD

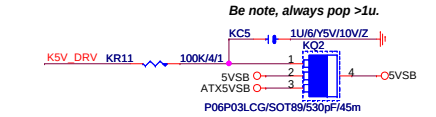


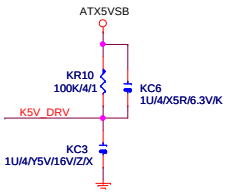
(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms



Function Selection. Strapped by VSB
Strapped to high :
DeepS5_Sel = 1:
System will enter the deep S5 state after 6 sec delays when AC power on.
Strapped to low : (Default)
DeepS5_Sel = 0:
System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.







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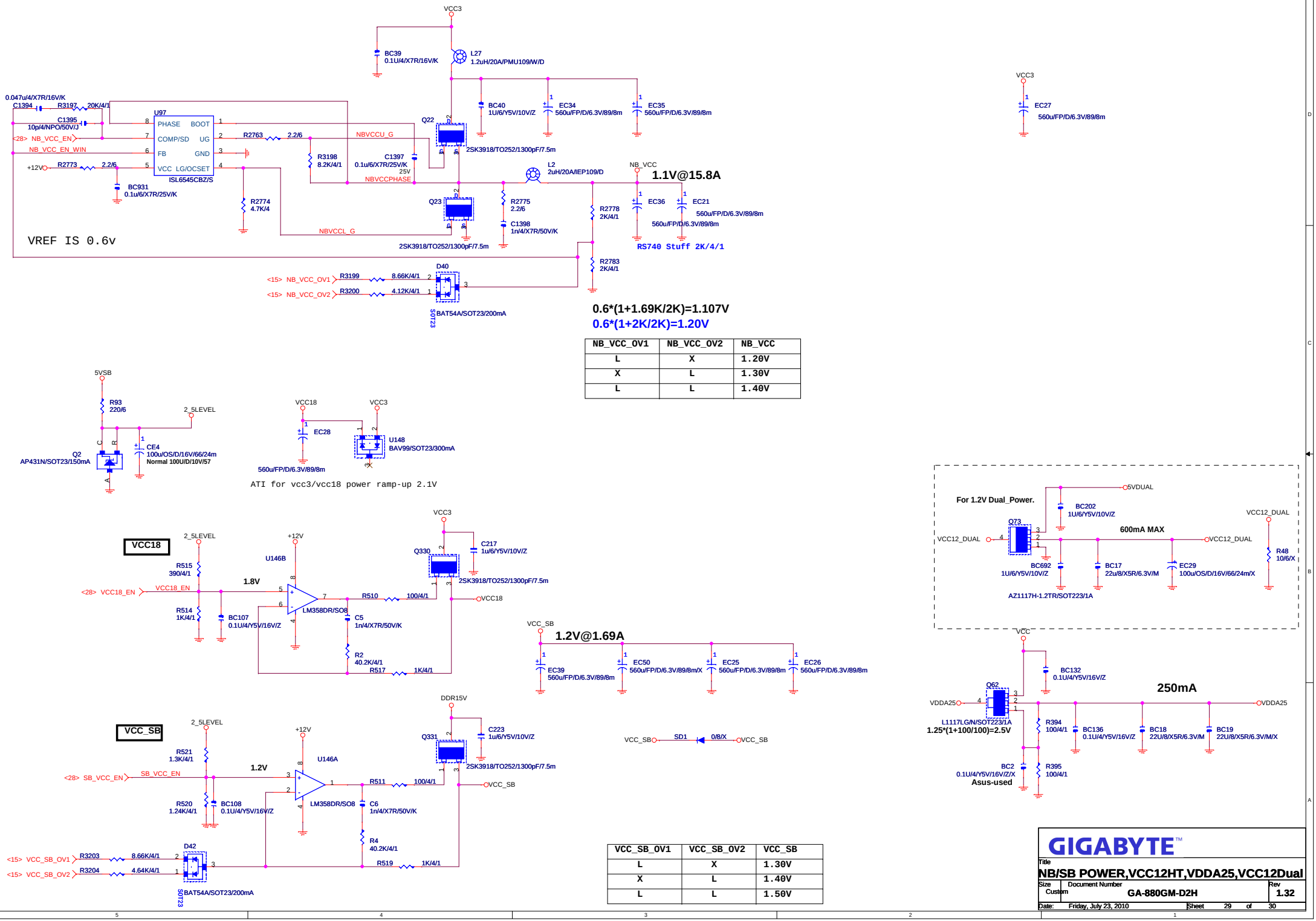

NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

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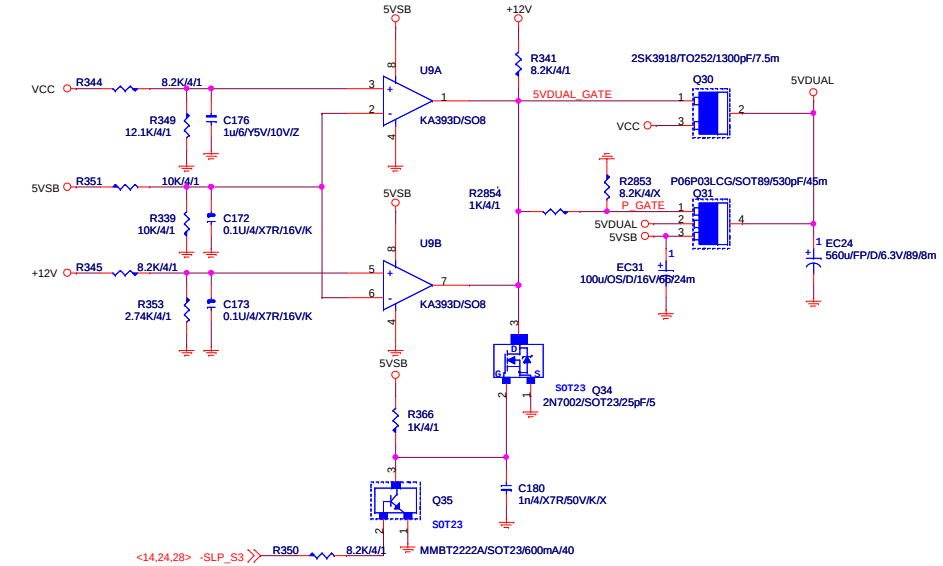
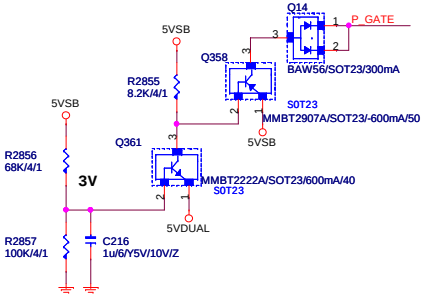
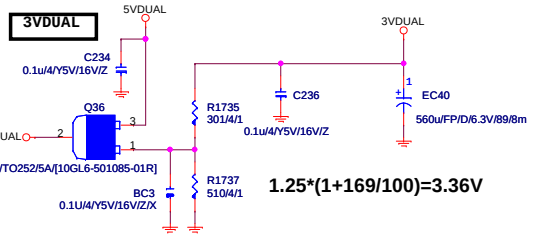
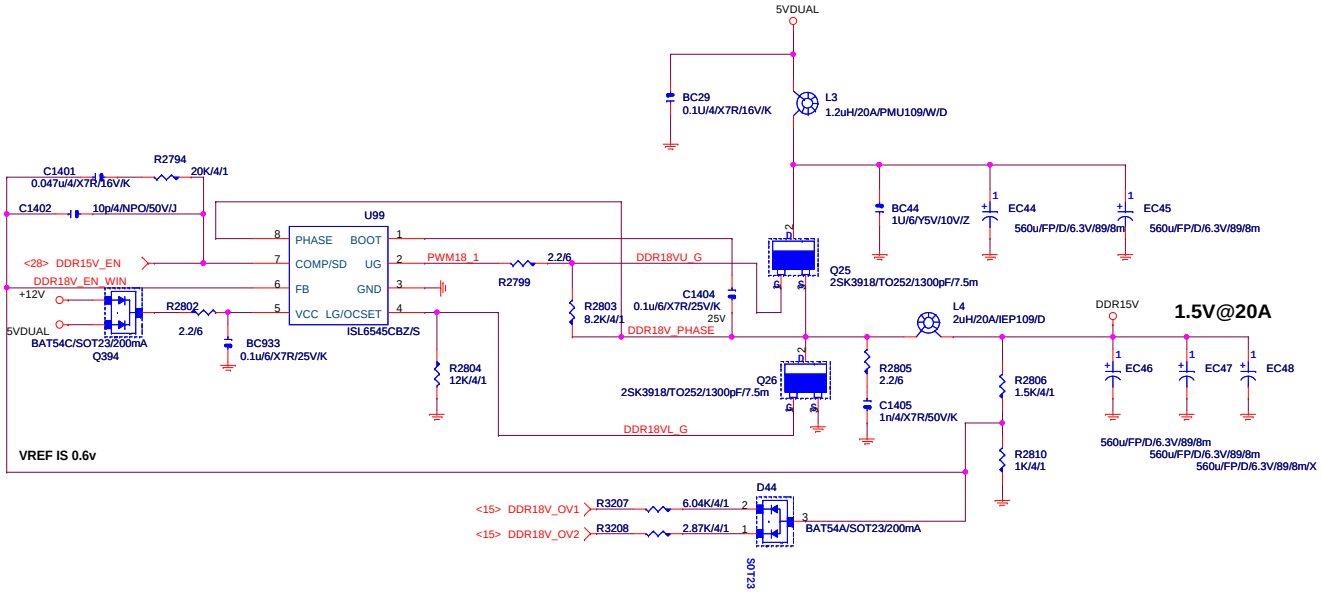
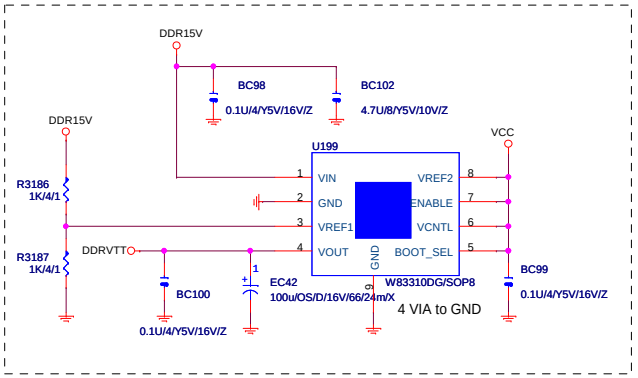
5VDUAL











0.6*(1+3K/1.43K)=1.859V

DDR18V_OV1	DDR18V_OV2	DDR18V
L	X	1.90V
X	L	2.00V
L	L	2.10V

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