MS-7364 Ver:0A

CPU:

Intel Prescott LGA775 -Mainstream CPU

System Chipset:

North Bridge : VIA P4M890
South Bridge : VIA VT8237R Plus

On Board Chipset:

LPC Super I/O -- W83627EHG
LAN(PHY) --- Realtek 8201CL
AC'97 Codec --Realtek ALC655
BIOS --SPI+LPC FLASH ROM

CLOCK Chip :

CLOCK Generator -- ICS9LPR700EGLFT

Main Memory:

DDRII * 1 +DDRI * 1

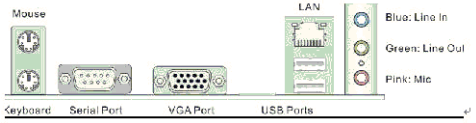
Expansion Slots:

PCI SLOT * 1

PWM:

VRM11 ST L6703 3Phase

Rear I/O
The same as follow picture

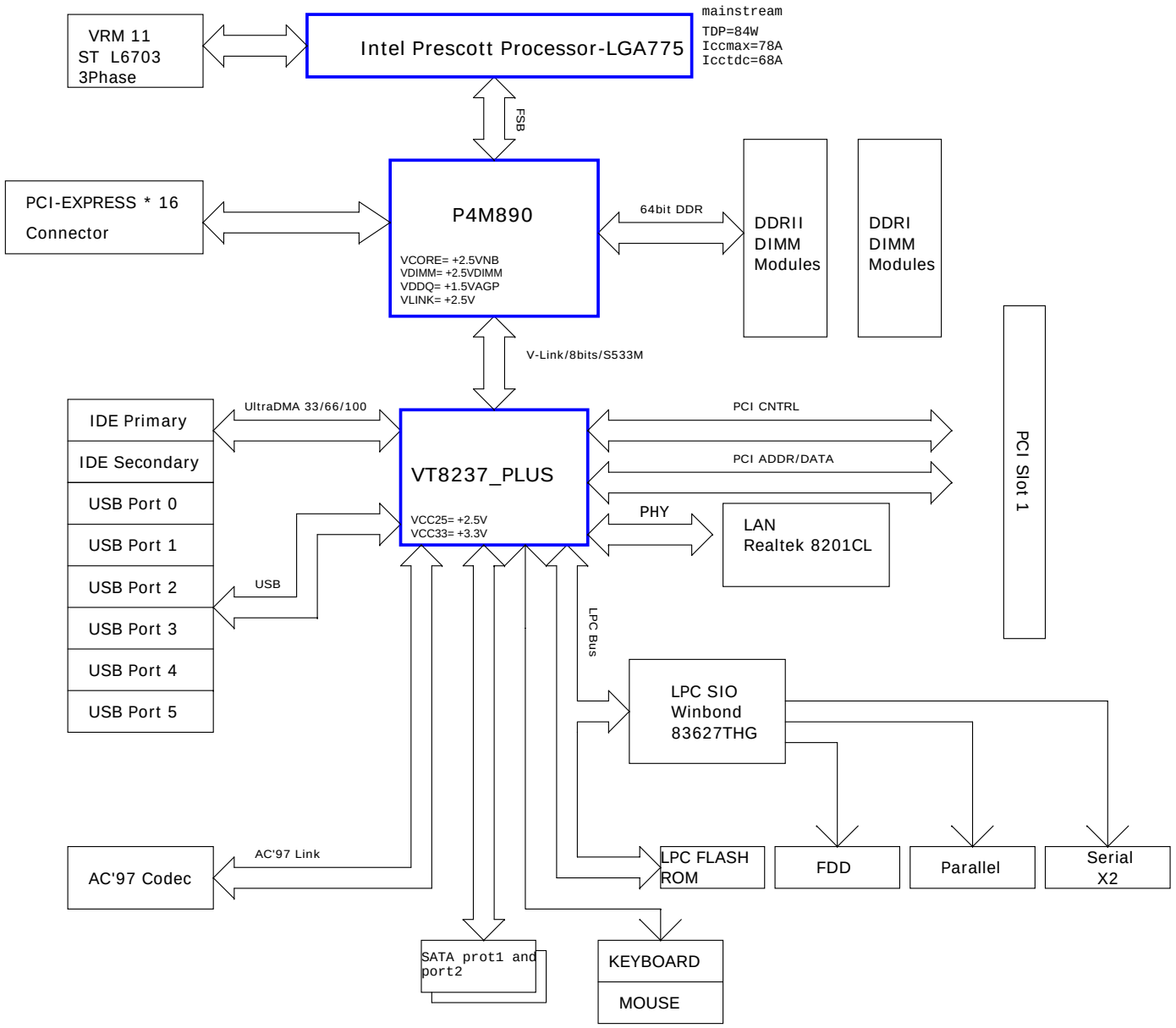


CHIPSET P4M890_Pro + VT8237R_PLUS

MSI MICRO-STAR INTL CO.,LTD.

Title: COVER SHEET		
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 1 of 31	

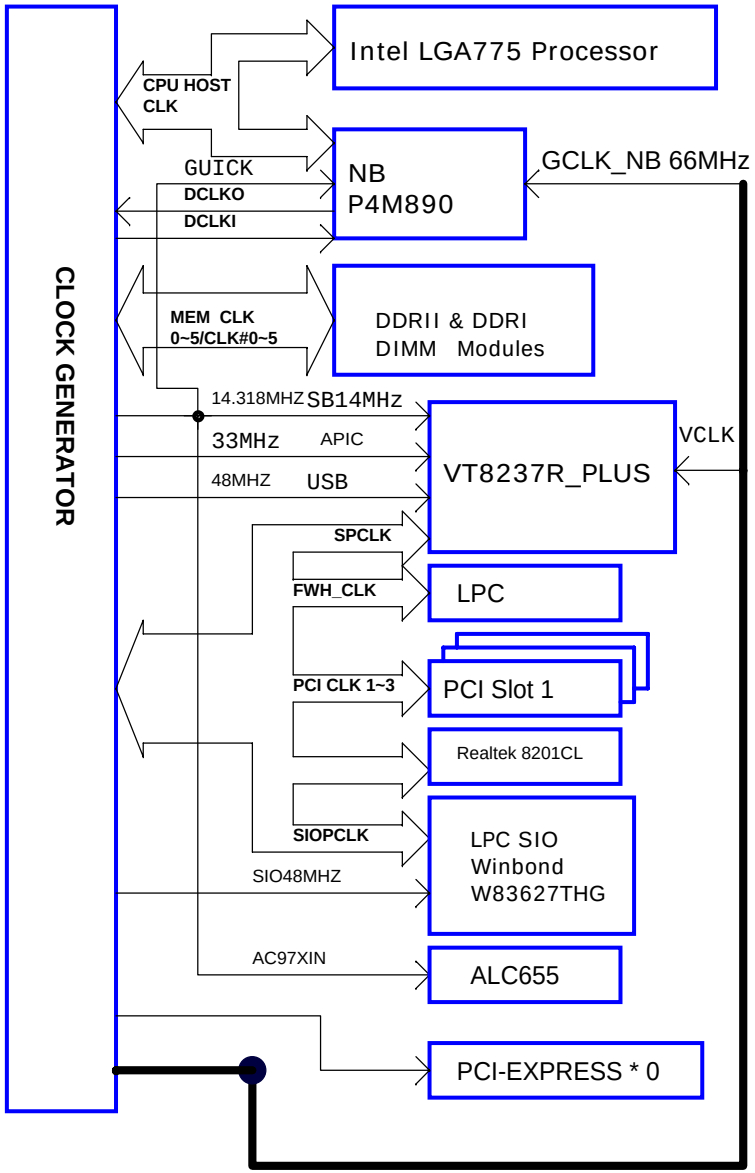
Block Diagram



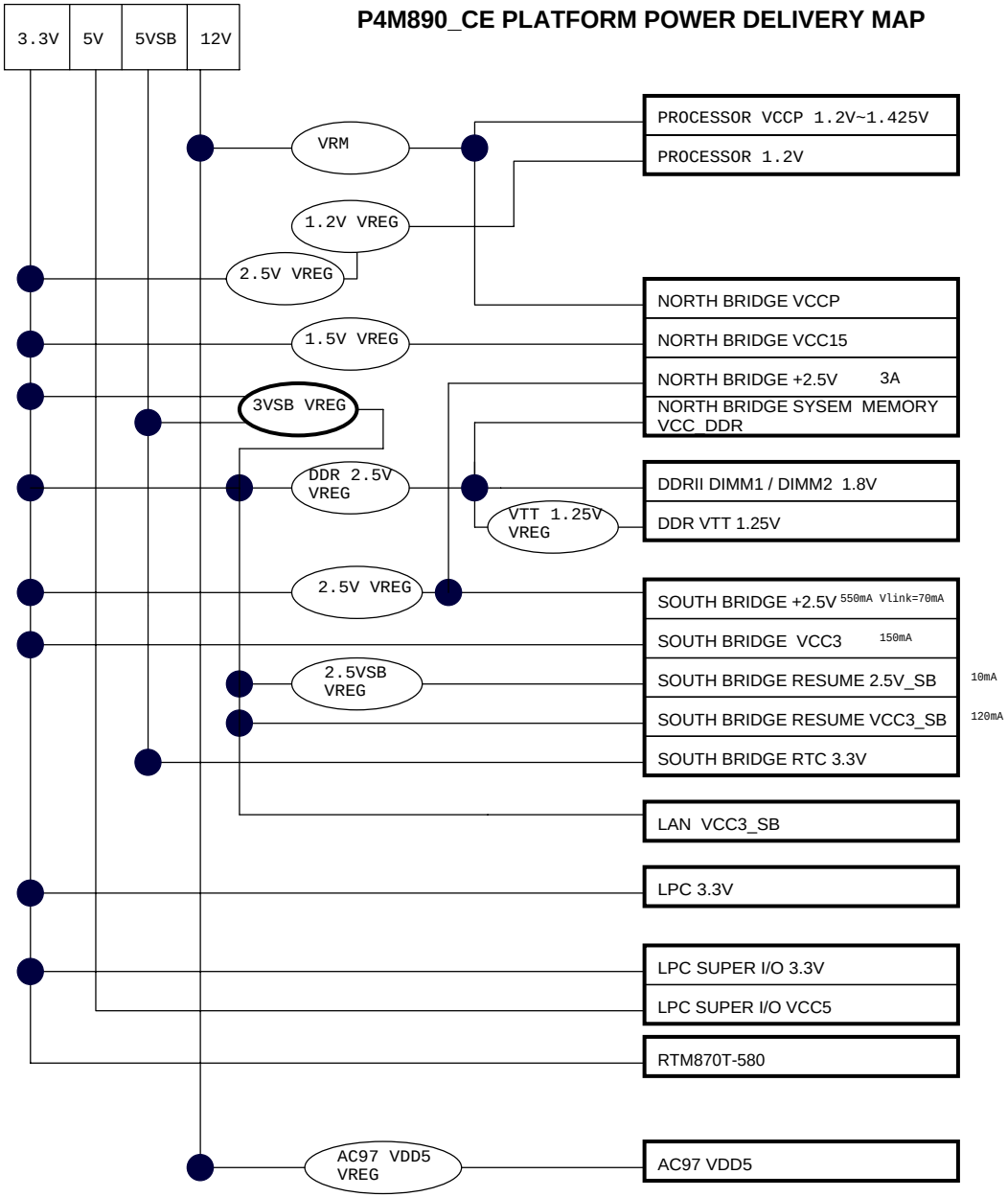
MSI MICRO-START INT'L CO.,LTD.

Title: BLOCK DIAGRAM		
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 2 of 31	

P4M890 PLATFORM CLOCK GENERATOR MAP



P4M890_CE PLATFORM POWER DELIVERY MAP



+12V : 0.1U 25V X 5
+12V_MOS: 4.7U 35V X 1
1U 16V X 2
1000U 16V X 4

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title: PWR And CLOCK Map		
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
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VT8237R_PLUS GPIO Function Define

PIN NAME	Default Function	Function define
GPO0 (VDDS)	GPO0	4.7K ohm Pull up to VCC3_SB
GPO1(VDDS)	GPO1	4.7K ohm Pull up to VCC3_SB
GPO2/SUSA# (VDDS)	SUSA#	4.7K ohm Pull up to VCC3_SB
GPO3/SUSST#(VDDS)	SUSST#	4.7K ohm Pull up to VCC3_SB
GPO4/SUSCLK(VDDS)	SUSCLK	4.7K ohm Pull up to VCC3_SB
GPO5/CPUSTP#	CPUSTP#	4.7K ohm Pull up to VCC3
GPO6/PCISTP#	PCISTP#	4.7K ohm Pull up to VCC3
GPO7/GNT5	GPO7	8.2K ohm Pull up to VCC3
GPO8/GPI8/VGATE	GPO8	2.7K ohm Pull up to VCC3
GPO9/UDPWREN	UDPWREN	NC
GPO10/GPI10/PICD0	GPO10	1K ohm Pull up to VCC3
GPO11/GPI11/PICD1	GPO11	1K ohm Pull up to VCC3
GPO12/GPI12/INTE#	GPO12	8.2K ohm Pull up to VCC3
GPO13/GPI13/INTF#	GPO13	8.2K ohm Pull up to VCC3
GPO14/GPI14/INTG#	GPO14	8.2K ohm Pull up to VCC3
GPO15/GPI15/INTH#	GPO15	8.2K ohm Pull up to VCC3
GPO20/GPI20 /ACSDIN2/PCS0#	GPI20/ACSDIN2	4.7K ohm Pull down
GPO21/GPI21/ACSDIN3 /PCS1#/SLPBTN#	GPI21/ACSDIN3	4.7K ohm Pull down
GPO22/GPI22/GHI#	GPI22	4.7K ohm Pull up to VCC3
GPO23/GPI23/DPSLP	GPI23	4.7K ohm Pull up to VCC3
GPO24/GPI24 /GPIOA	GPIOA	2.2K ohm Pull up to VCC3 SEL Vlink Manual mode
GPO25/GPI25 /GPIOB	GPIOB	2.2K ohm Pull down SEL IOQ Depth=8 Level
GPO26/GPI26/SMBDT2 (VDDS)	SMBDT2	2.7K ohm Pull up to VCC3_SB
GPO27/GPI27/SMBCK2 (VDDS)	SMBCK2	2.7K ohm Pull up to VCC3_SB
GPO28/GPI28/VIDSEL	GPO28 /VIDSEL	SATA_LED
GPO29/GPI29/VRDSLP	GPO29 /VRDSLP	4.7K ohm Pull down
GPO30/GPI30 /GPIOC	GPIOC	2.2K ohm Pull up to VCC3 SEL Host Clock=Auto mode
GPO31/GPI31 /GPIOD	GPIOD	2.2K ohm Pull down SEL GTL pull up=Enable

PIN NAME	Default Function	Function define
GPI0 (VBAT)	GPI0	1M ohm Pull up to VBAT
GPI1 (VSUS3)	GPI1	ATADET0=>Detect IDE1 ATA100/66
GPI2/EXTSMI# (VSUS3)	EXTSMI#	4.7K ohm Pull up to VCC3_SB
GPI3/RING# (VSUS3)	RING#	RING# 4.7K ohm Pull up to VCC3_SB
GPI4/LID# (VSUS3)	LID#	ATADET1=>Detect IDE2 ATA100/66
GPI5/BATLOW# (VDDS)	BATLOW#	4.7K ohm Pull up to VCC3_SB
GPI6/AGPBZ	AGPBZ	4.7K ohm Pull up to VCC3
GPI7/REQ5	GPI7	8.2K ohm Pull up to VCC3
GPI9/UDPWREN	UDPWR	10K ohm Pull down
GPI16/INTRUDER# (VBAT)	INTRUDER#	1M ohm Pull up to VBAT
GPI17/CPUMISS	CPUMISS	4.7K ohm Pull up to VCC3_SB
GPI18/AOLGP1/THRM#	THERM#	4.7K ohm Pull up to VCC3_SB
GPI19/APICCLK	APICCLK	APICCLK

USB

	Port	DATA +/-	OC#
Rear	USB1	USB1- USB1+ USB0- USB0+	OC#1 (OC#0~3)
	LAN_USB1	USB2- USB2+ USB3- USB3+	
Front	JUSB2	USB4- USB4+ USB6- USB6+	OC#4 (OC#4~7)
	JUSB1	USB5- USB5+ USB7- USB7+	

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLKA0/MDCLKA#0 DCLKA1/MDCLKA#1 DCLKA2/MDCLKA#2
DIMM 2	1010001B	DCLKA3/MDCLKA#3 DCLKA4/MDCLKA#4 DCLKA5/MDCLKA#5

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI slot 1-3
PCIRST#2	NB , Super I/O
PCIRST#3	LPC
HD_RST#	Primary, Scondary IDE

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	PIRQ#A PIRQ#D PIRQ#C PIRQ#B	PCIREQ#0 PCIGNT#0	AD19	PCI_CLK1	1
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PCIREQ#1 PCIGNT#1	AD20	PCI_CLK2	2
PCI Slot 3	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PCIREQ#2 PCIGNT#2	AD21	PCI_CLK3	5

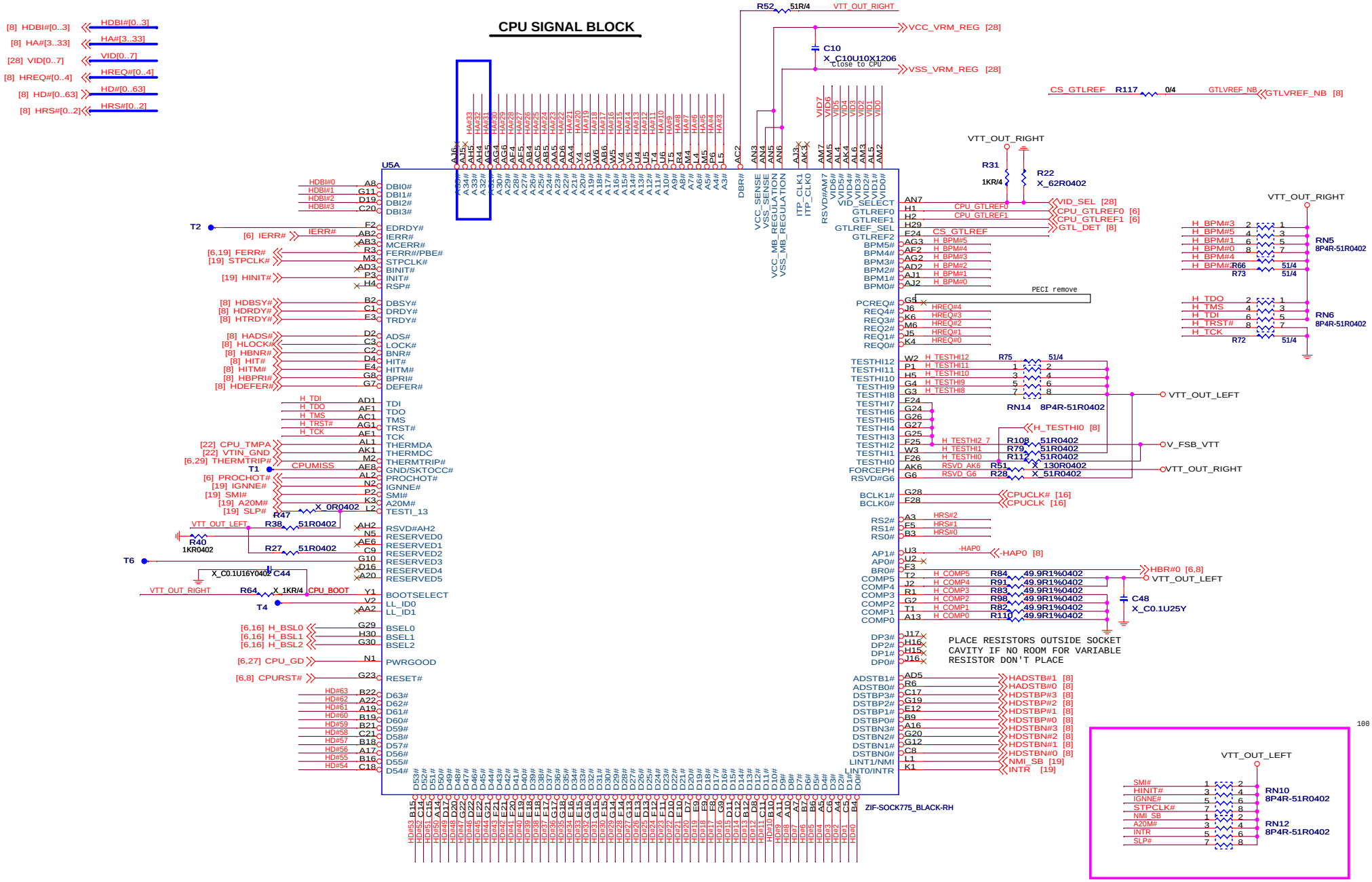
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: GPIO/MEMORY/PCI/HW STRPPING

Size: Custom | Document Number: MS-7364-V0A-0207-G | Rev: 3.1

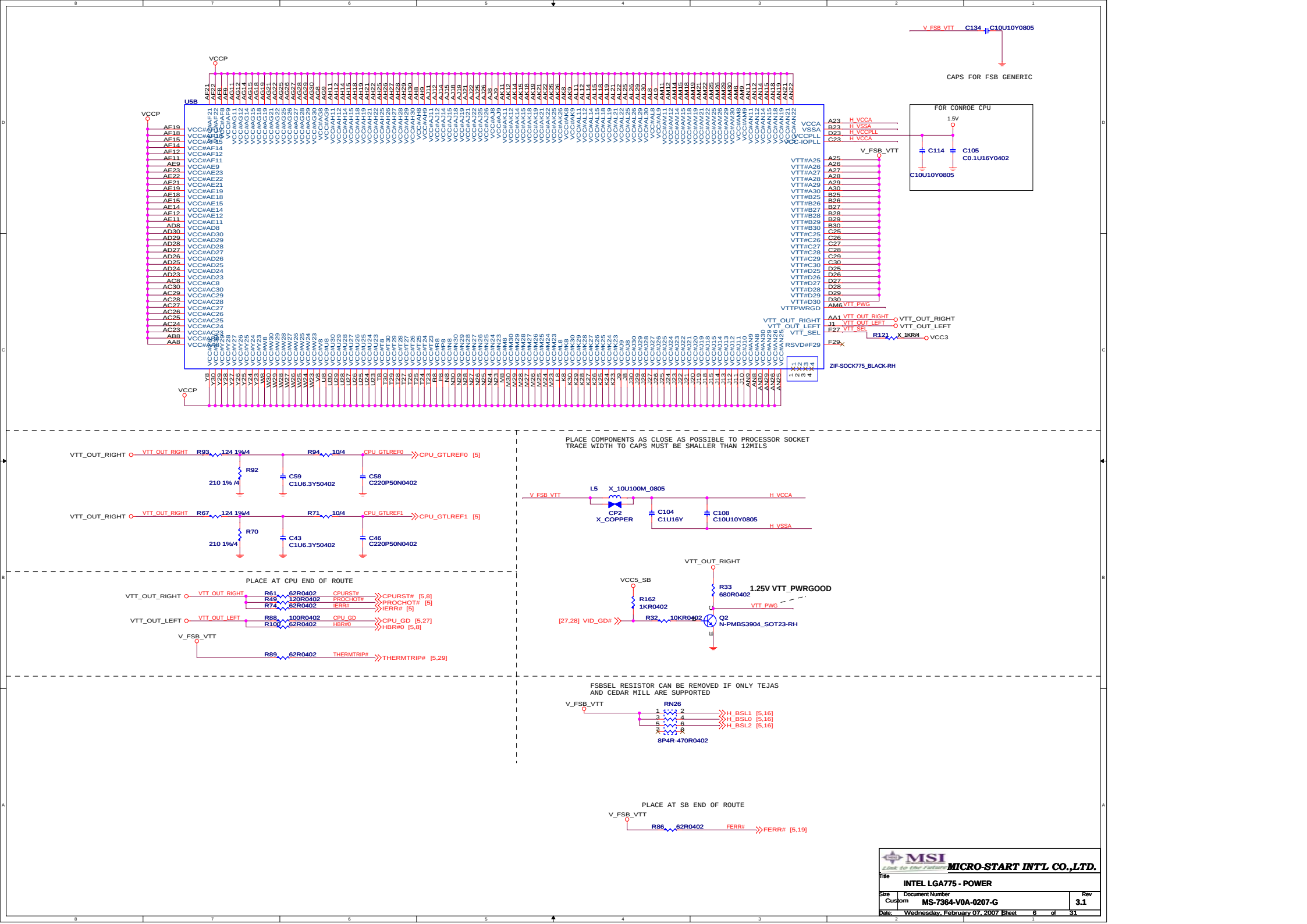
Date: Wednesday, February 07, 2007 | Sheet 4 of 31

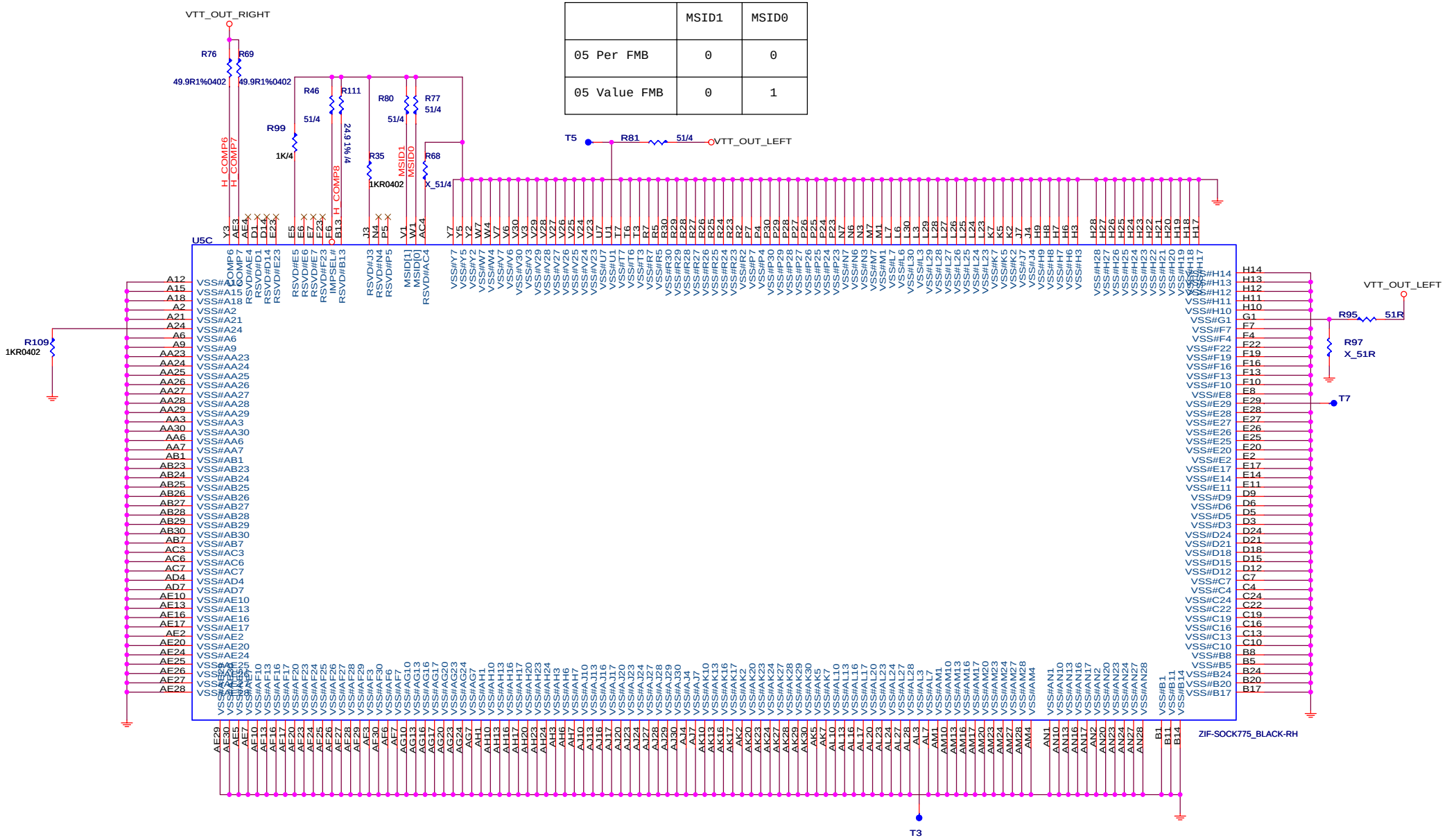
CPU SIGNAL BLOCK



MICRO-START INT'L CO.,LTD.

Title	INTEL LGA775 - SIGNALS	
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 5 of 31	

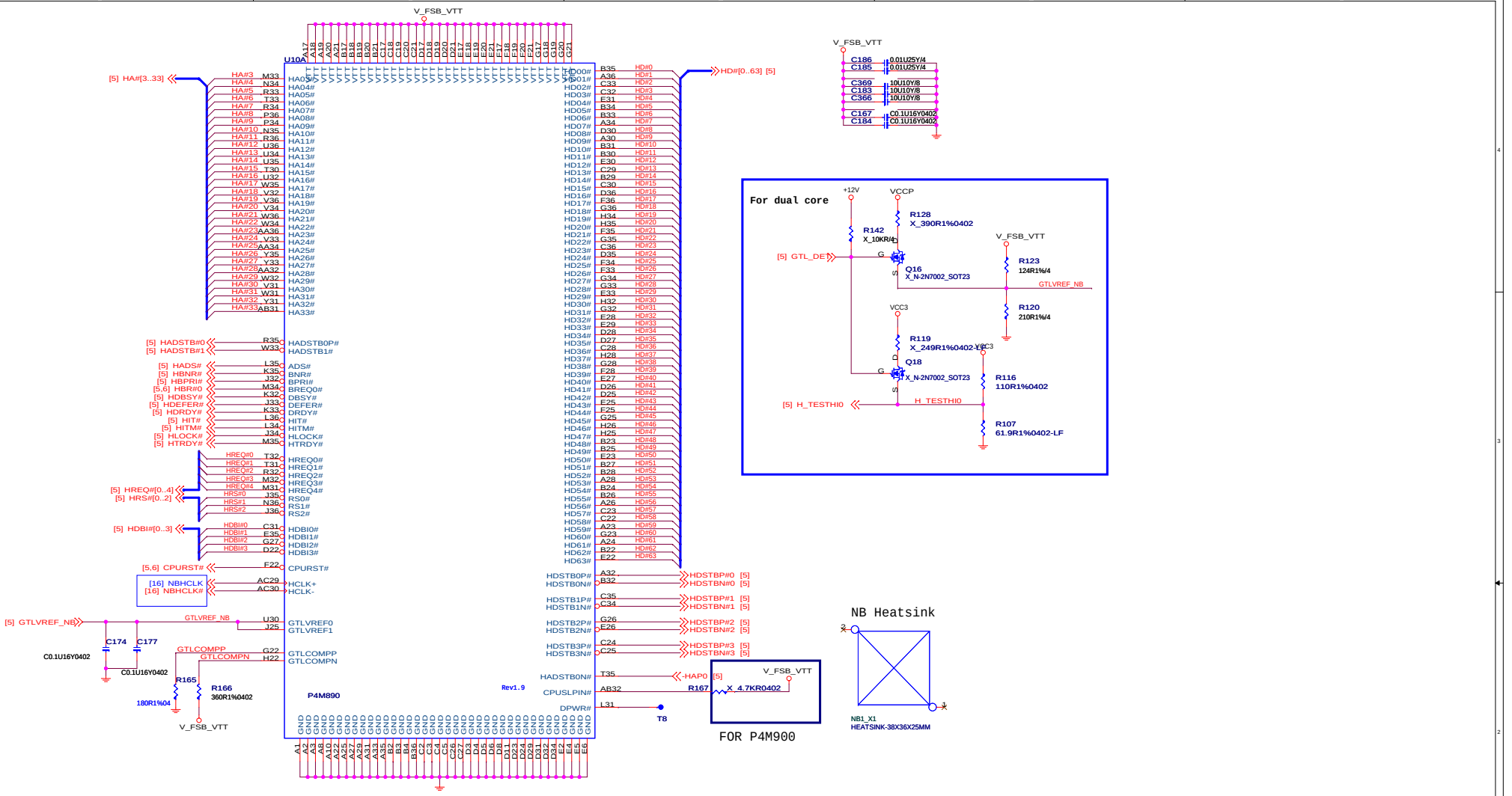

U5B
VCCP
VCCA
VSSA
VCCPLL
VCC-IOPLL
VTTPWRGD
RSVD#F29
ZIF-SOCK775_BLACK-RH
V_FSB_VTT
VTT_PWG
VTT_SEL
VTT_OUT_RIGHT
VTT_OUT_LEFT
H_VCCA
H_VSSA
H_VCCPLL
FOR CONROE CPU
1.5V
C114
C105
C0.1U16Y0402
C10U10Y0805
V_FSB_VTT C134 C10U10Y0805
CAPS FOR FSB GENERIC
VTT_OUT_RIGHT R93 124 1%/4 R94 10/4 CPU_GTLREF0 CPU_GTLREF0 [5]
R92 210 1% /4
C59 C1U6.3Y50402
C58 C220P50N0402
VTT_OUT_RIGHT R67 124 1%/4 R71 10/4 CPU_GTLREF1 CPU_GTLREF1 [5]
R70 210 1%/4
C43 C1U6.3Y50402
C46 C220P50N0402
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS
V_FSB_VTT L5 X_10U100M_0805 H_VCCA
CP2 X_COPPER
C104 C1U16Y
C108 C10U10Y0805
H_VSSA
PLACE AT CPU END OF ROUTE
VTT_OUT_RIGHT R61 62R0402 CPURST# CPURST# [5,8]
R49 120R0402 PROCHOT# PROCHOT# [5]
R74 62R0402 IERR# IERR# [5]
VTT_OUT_LEFT R88 100R0402 CPU_GD CPU_GD [5,27]
R100 62R0402 HBR#0 HBR#0 [5,8]
V_FSB_VTT
R89 62R0402 THERMTRIP# THERMTRIP# [5,29]
VTT_OUT_RIGHT
VCC5_SB
R33 680R0402 1.25V VTT_PWRGOOD
R162 1KR0402
[27,28] VID_GD#
R32 10KR0402 Q2 N-PMBS3904_SOT23-RH
VTT_PWG
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS
AND CEDAR MILL ARE SUPPORTED
V_FSB_VTT RN26
H_BSL1 [5,16]
H_BSL0 [5,16]
H_BSL2 [5,16]
8P4R-470R0402
PLACE AT SB END OF ROUTE
V_FSB_VTT
R86 62R0402 FERR# FERR# [5,19]
MSI MICRO-START INTL CO.,LTD.
Title
INTEL LGA775 - POWER
Size Custom
Document Number MS-7364-V0A-0207-G
Rev 3.1
Date: Wednesday, February 07, 2007 Sheet 6 of 31



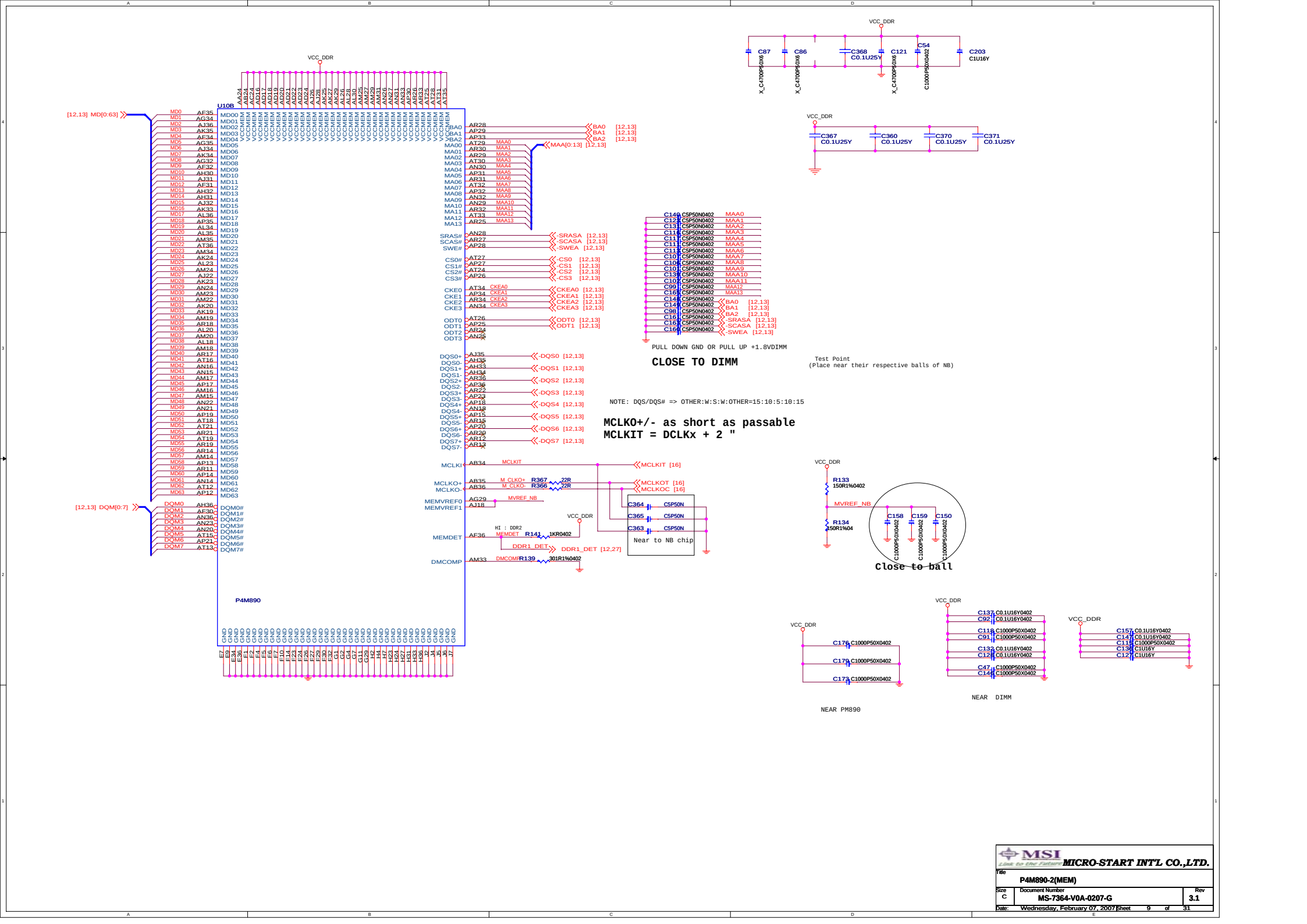
	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1

MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	INTEL LGA775 - GND	
Size A3	Document Number MS-7364-V0A-0207-G	Rev 3.1
Date: Wednesday, February 07, 2007	Sheet 7 of 31	

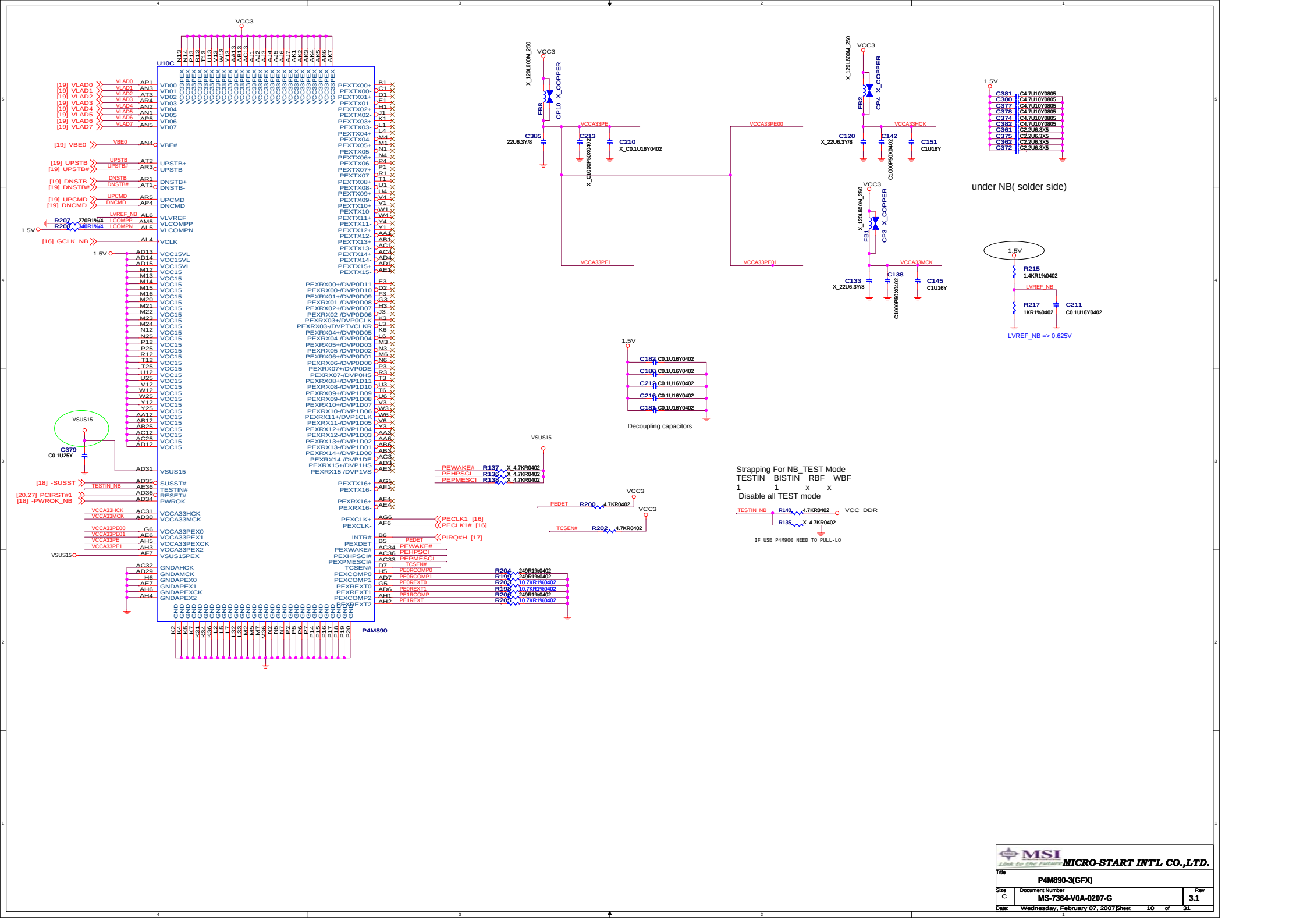


MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	P4M890-1 (HOST)		
Size C	Document Number MS-7364-V0A-0207-G		Rev 3.1
Date: Wednesday, February 07, 2007	Sheet 8	of	31



MICRO-START INT'L CO.,LTD.

Title	P4M890-2(MEM)	
Size C	Document Number MS-7364-V0A-0207-G	Rev 3.1
Date: Wednesday, February 07, 2007	Sheet 9 of 31	


U10C
P4M890
VCC3
1.5V
VSUS15
VCC33HCK
VCC33MCK
VCC33PE00
VCC33PE01
VCC33PE
VCC33PE1
VCCA33PE
VCCA33HCK
VCCA33MCK
under NB(solder side)
Decoupling capacitors
LVREF_NB => 0.625V
Strapping For NB_TEST Mode
TESTIN BISTIN RBF WBF
1 1 x x
Disable all TEST mode
IF USE P4M900 NEED TO PULL-LO
MICRO-STAR INT'L CO.,LTD.
P4M890-3(GFX)
MS-7364-V0A-0207-G
3.1
Wednesday, February 07, 2007
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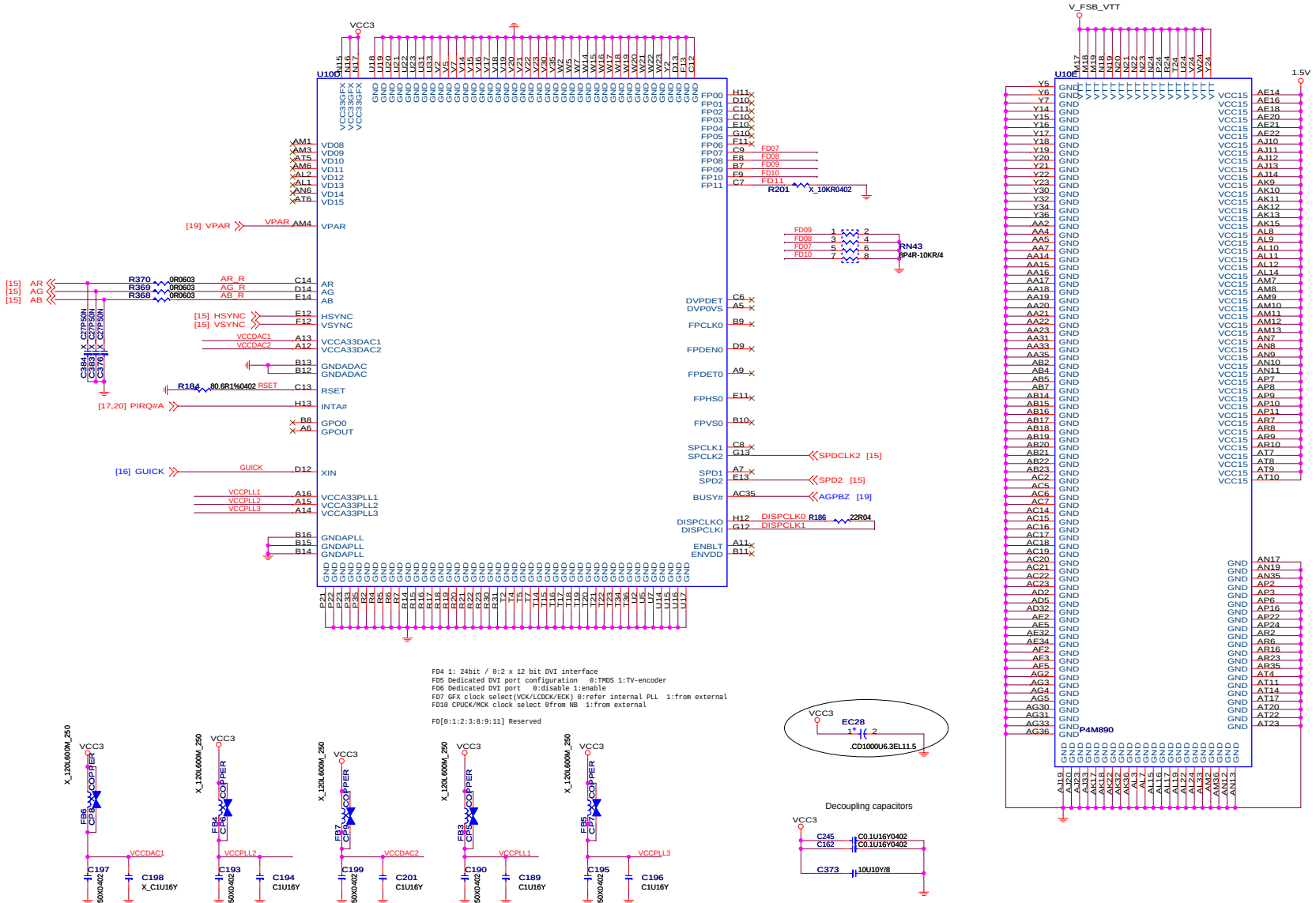
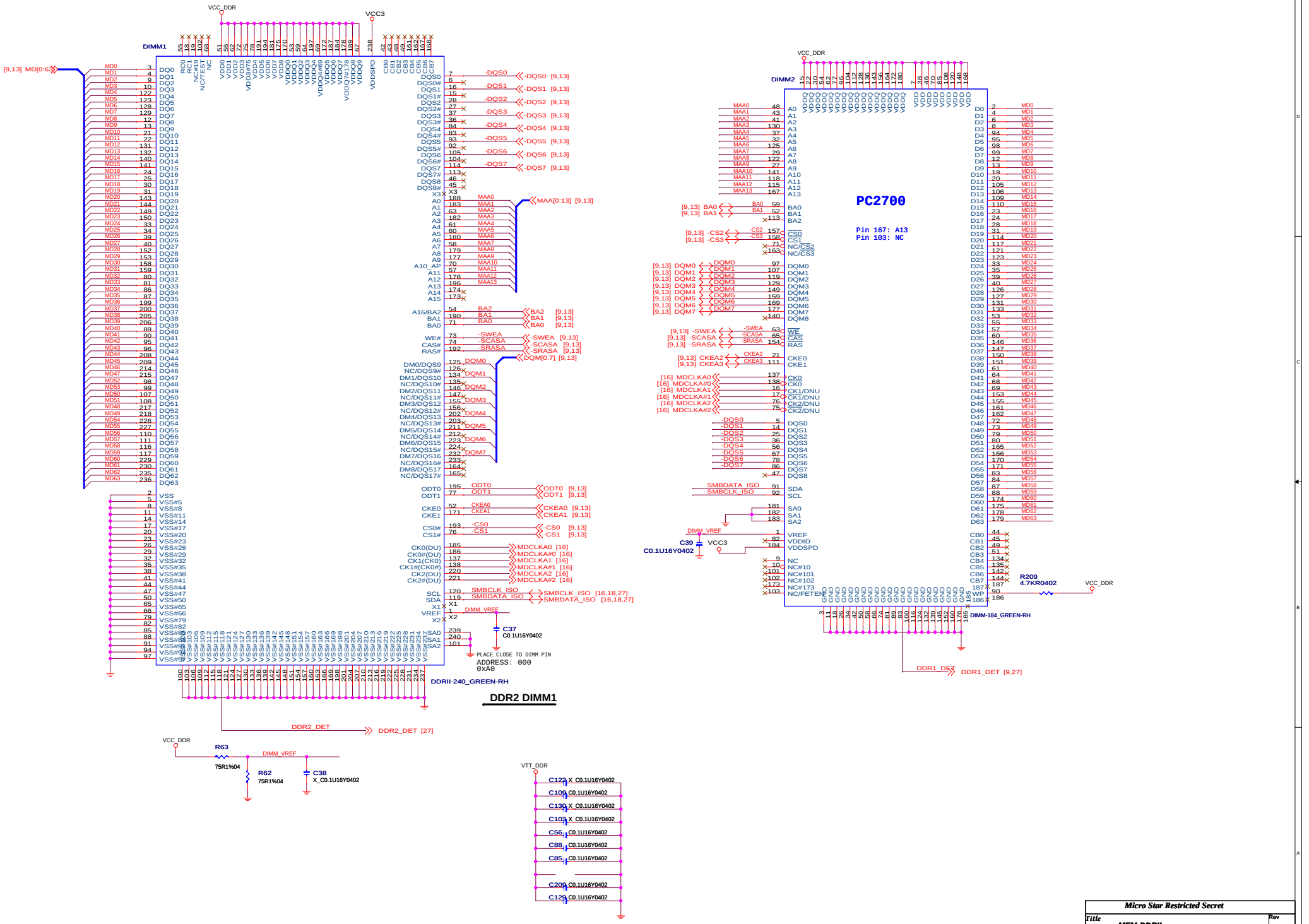


MSI MICRO-STAR INT'L CO.,LTD.

Title: P4M890-4(DISPLAY)

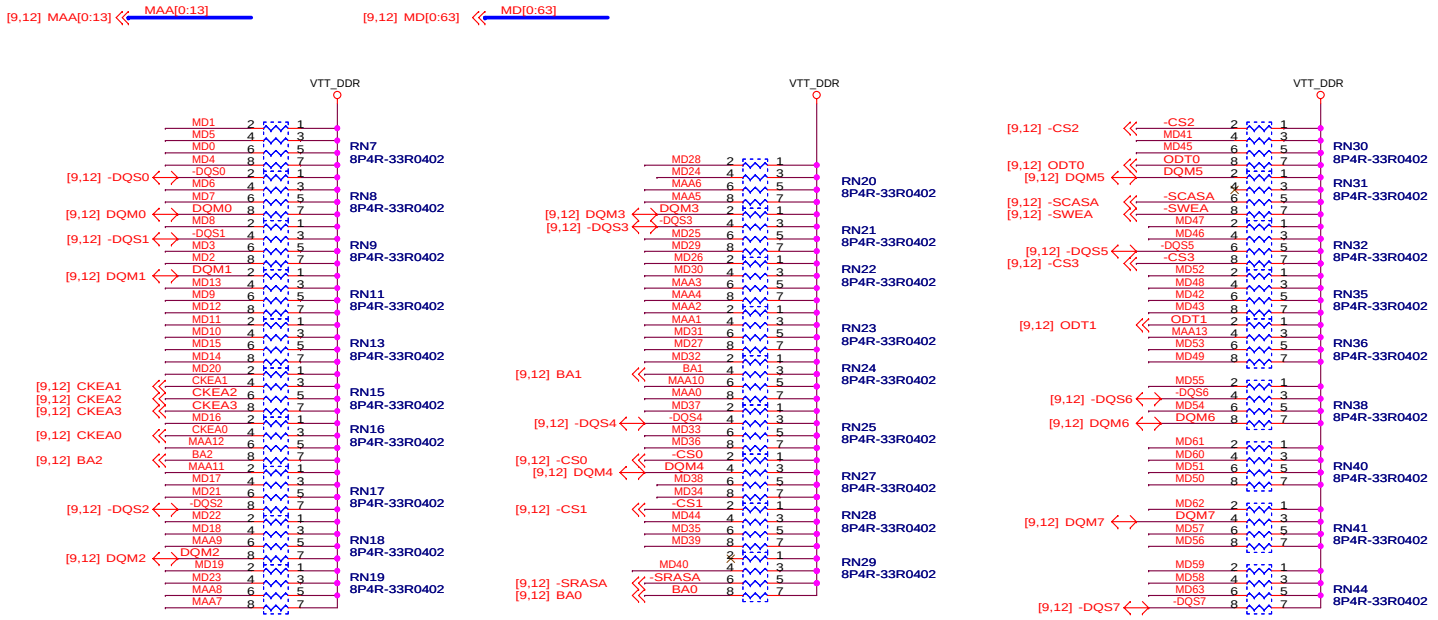
Size	Document Number	Rev
C	MS-7364-V0A-0207-G	3.1

Date: Wednesday, February 07, 2007 Sheet 11 of 31

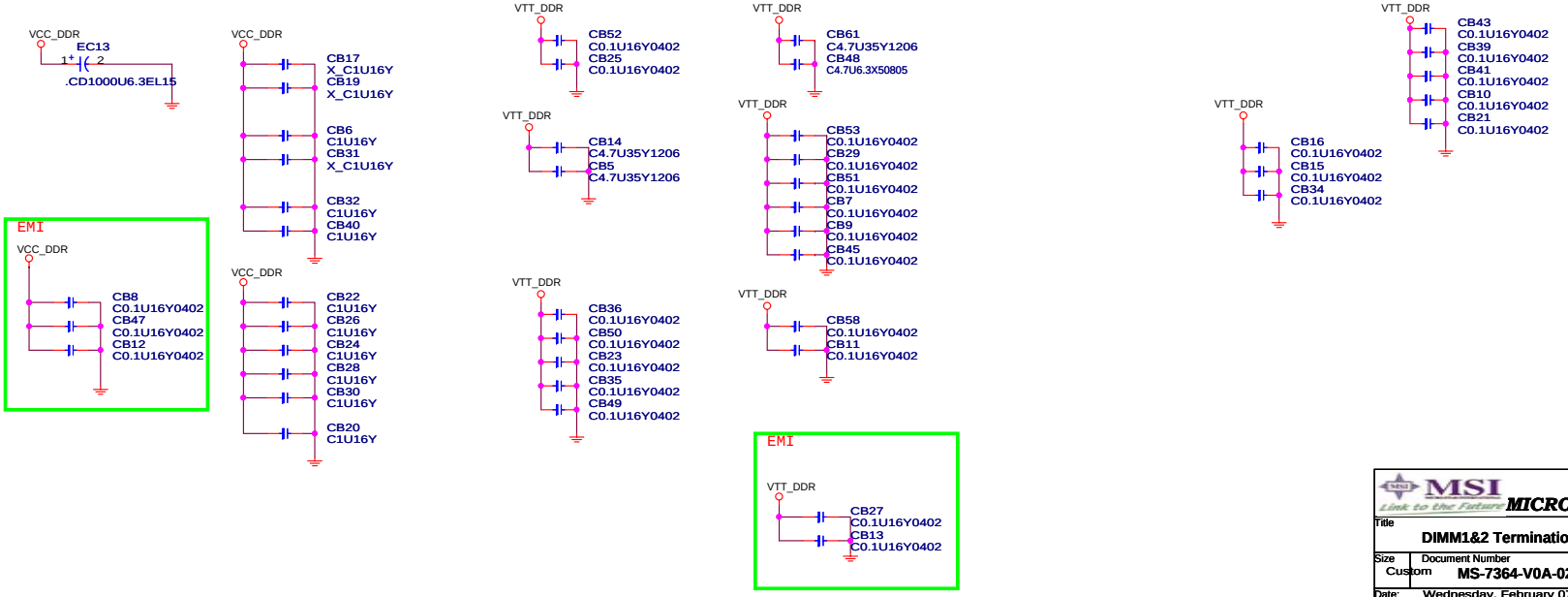


Micro Star Restricted Secret	
Title: MEM-DDRII	Rev: 3.1
Document Number: MS-7364-V0A-0207-G	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Wednesday, February 07, 2007
	Sheet 12 of 31

DIMM1 & 2 Terminations



V_SM_VTT DECOULPING CAPS



MICRO-START INT'L CO.,LTD.

Title: DIMM1&2 Terminations		
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
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12V ===> 5.5A for x16 slot ,75 Watt
3.3V===> 3A
3.3Vaux==>375mA

MICRO-START INT'L CO.,LTD.

Title	PCI-EXPRESS SLOT X16 & X1	
Size: C	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
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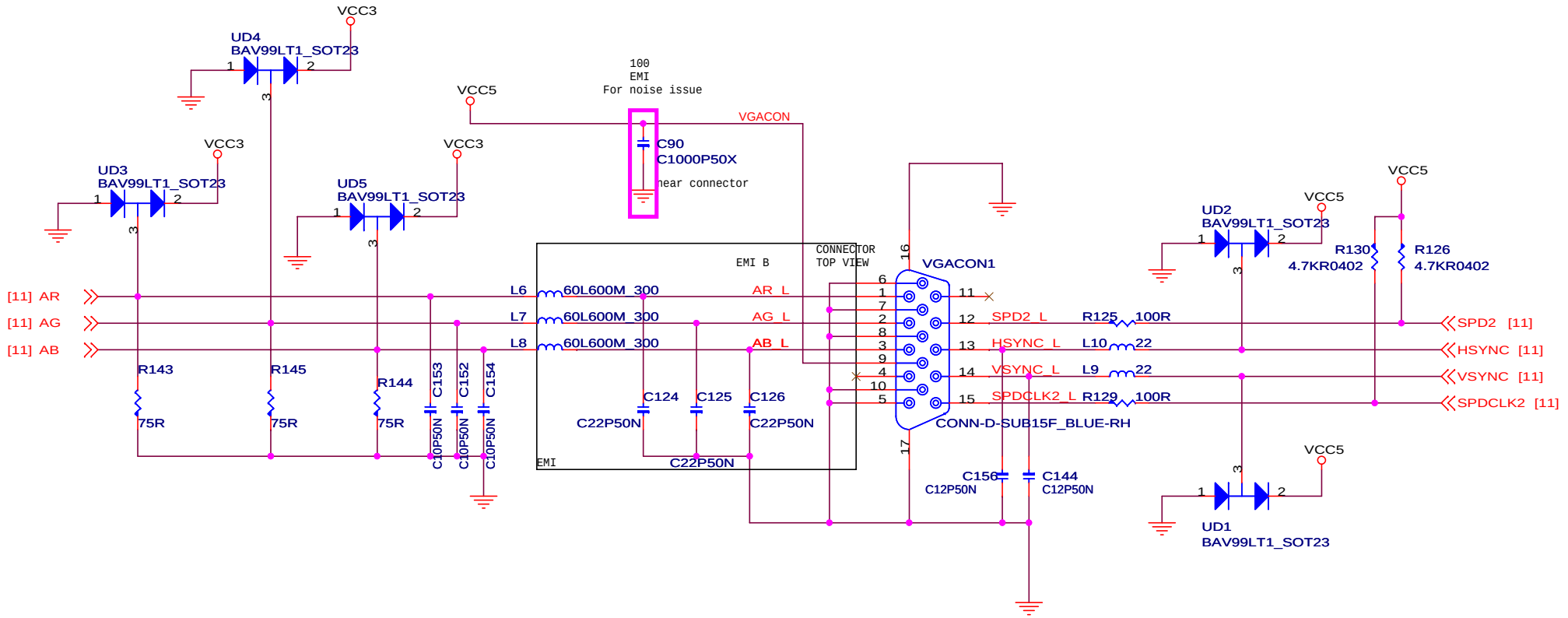
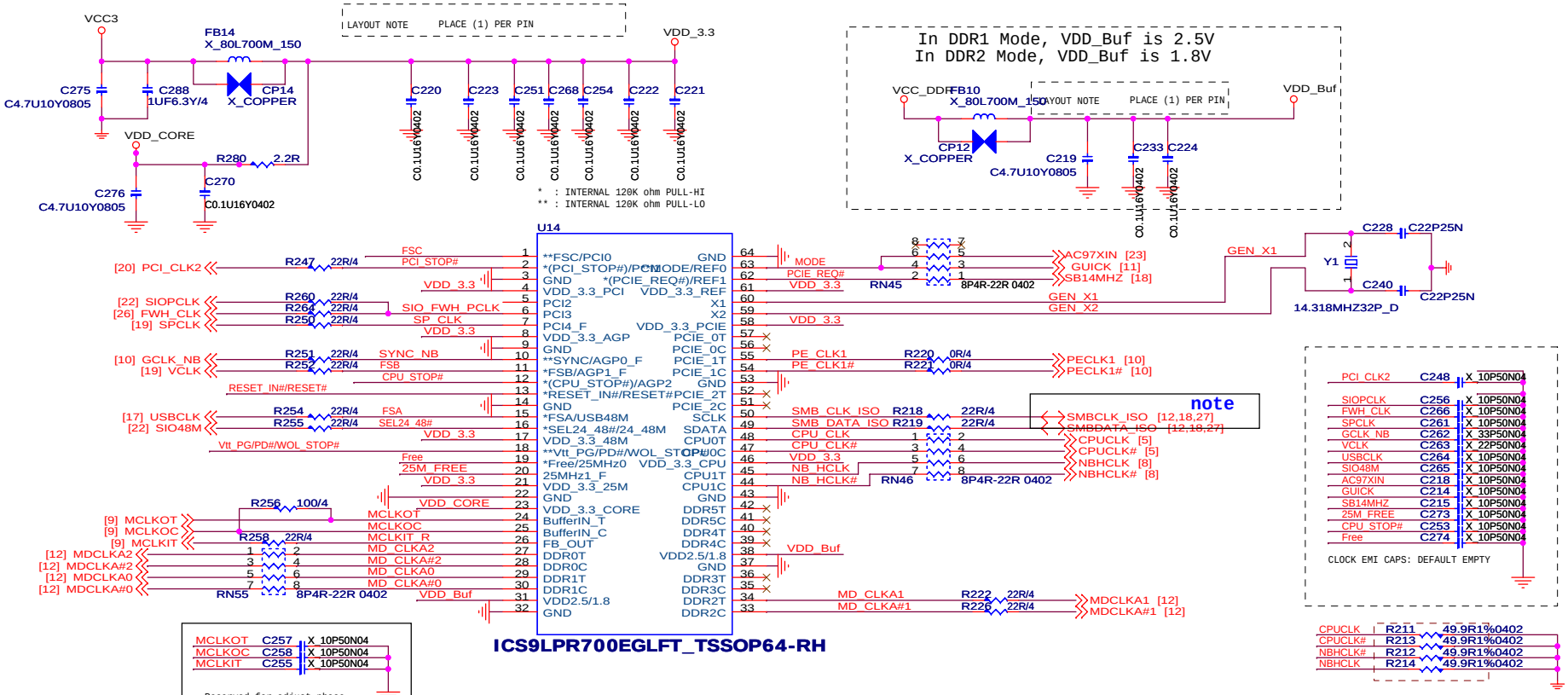
VGA CONNECTOR



MICRO-START INT'L CO.,LTD.

Link to the Future

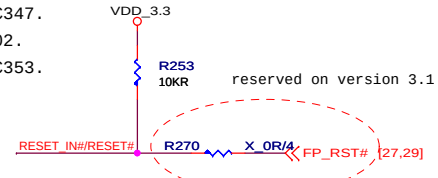
Title: VGA Connector		
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 15 of 31	

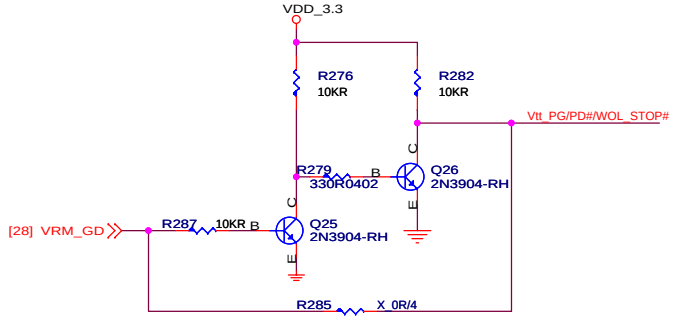


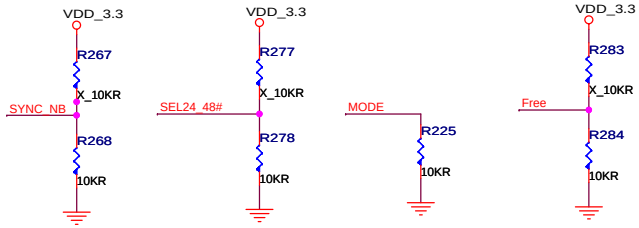
ICS9LPR700EGLFT_TSSOP64-RH

Modify clock skew issue.

1. R322 change to 0 ohm 0402.
2. Add a 22pf 0402 cap on C347.
3. R316 change to 33ohm 0402.
4. Add a 33pf 0402 cap on C353.







	1 (Pull High)	0 (Pull Low)
SYNC	PCIEX clocks are synchronous with CPU.	PCIEX clocks are asynchronous with CPU.
SEL24_48#	Pin16 = 24MHz	Pin16 = 48MHz
MODE	Notebook mode	Desktop mode
Free	25Mhz-0 is free running	25Mhz-0 is stoppable

Intel P4(775) Table

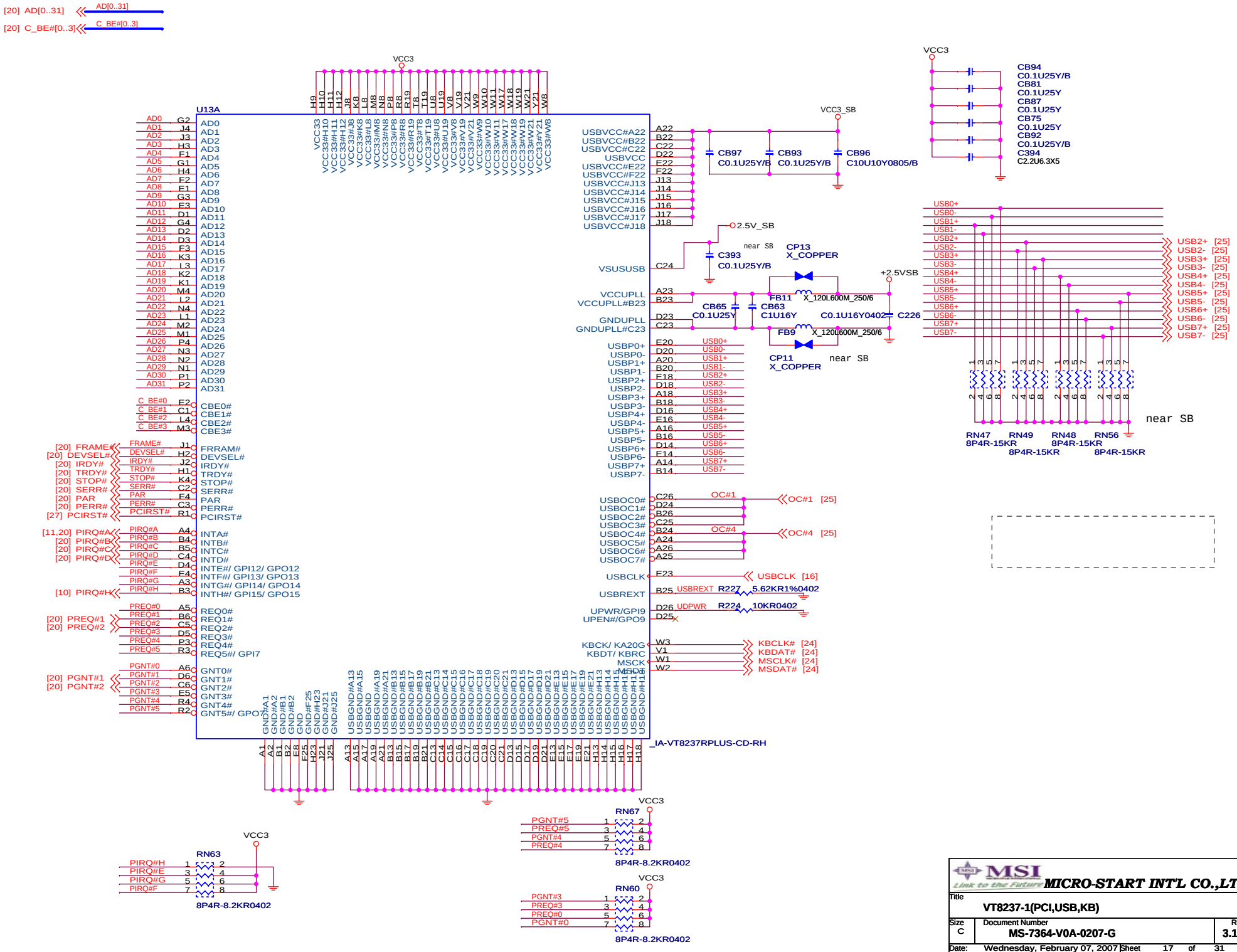
FS4	FS3	FS2	H_BSL1	H_BSL0	CPU
0	0	0	0	0	266
			0	1	133
			1	0	200
			1	1	166

MSI MICRO-START INT'L CO.,LTD.

Title: Clock Generator RTM870T-580

Size: Custom | Document Number: MS-7364-V0A-0207-G | Rev: 3.1

Date: Wednesday, February 07, 2007 | Sheet 16 of 31



MSI MICRO-START INT'L CO.,LTD.		
Title	VT8237-1(PCI,USB,KB)	
Size C	Document Number MS-7364-V0A-0207-G	Rev 3.1
Date: Wednesday, February 07, 2007	Sheet 17 of 31	

SB Pull up resistors

VT8237 strapping

Auto Reboot

RN77 8P4R-4.7KR0402
SUS_CLK
-EXTSMI
PEPMESCI_SB
-RING

RN76 8P4R-4.7KR0402
-SUSST
-THERM#
PME#
-BATLOW

RN81 8P4R-4.7KR0402
GPO1
-PWROK_NB
-PWRBTN
-SMBALT

GPO0 R329 4.7KR0402
-SUSA R332 4.7KR0402

ACSDO R311 4.7KR0402
0: Enable
1: Disable

LPC FWH Command

ACSYNC R303 4.7KR0402 (Try if not used) VCC3
R305 X_4.7KR0402
0: LPC FWH Enable
1: LPC FWH Disable

Use serial external LAN EEPROM

[29] SPKR — RN79 8P4R-4.7KR0402 (SPKR, SERIRQ, -CPUSTP, -PCISTP)
TPO R326 X_4.7KR0402

[19] MIIEEDI — R274 4.7KR0402, R265 X_4.7KR0402
1: Disable
0: Enable

External SATA PHY

ATADET, SMBCK2, SMBDATA_ISO, SMBCLK_ISO — RN80 8P4R-2.7KR0402 — VCC3_SB / VCC3
VBAT Issue: INTRUDER, GPI0 — R354 1MR0402, R350 1MR0402 — +3.3VBAT
PDDACK#_R R266 4.7KR0402 VCC3
0: Enable
1: Disable

SATA Master/Slave Mode

SDIN2, SDIN1, SDIN3 — RN72 8P4R-4.7KR0402
PDCS_#1 R259 10KR0402 VCC3
-LID R342 10KR0402
0: Master Slave mode
1: Master Master mode

NB Strapping Selection

RN62 8P4R-2.7KR0402: PD_A2, PD_A0, PD_A1
GPIOD R339 2.2KR0402
GPIOB R341 2.2KR0402
GPIOA R343 2.2KR0402
GPIOC R340 2.2KR0402
PDCS_#3 R257 2.2KR0402
R263 X_2.2KR0402

SW3 bit1

GPIOA	Vlink auto compensation
0	Auto mode
1	Manual mode

SW3 bit3

GPIOB	IOQ Depth
0	8 Level
1	1 Level

SW3 bit4

GPIOC	Host Clock
0	200Mhz
1	Auto Mode

SW3 bit2

GPIOD	GTL pullup
0	Enable
1	Disable

*"SPKR" => CPU Freq. Adjust Setting
1 - Disable (Default)
0 - Enable

U13B — VIA-VT8237RPLUS-CD-RH

[24] PDD[0..15] — PDD0..PDD15
[24] PDREQ, [24] PDDACK#_R, [24] PDIOR#_R, [24] PDIOW#_R, [24] PIORDY, [24] PDCS_#1, [24] PDCS_#3, [24] PD_A0, [24] PD_A1, [24] PD_A2, [24] IRQ14
[24] SDD7 — SDD7
[24] SD_REQ — SD_REQ
[24] SIORDY — SIORDY
[24] IRQ15 — IRQ15

C293 C0.1U25Y, R292 360R1%0402
STXP_1 C338 C0.01U25X/4 STXP1
STXN_1 C335 C0.01U25X/4 STXN1
SRXN_1 C315 C1200P50X/4 SRXN1
SRXP_1 C305 C1200P50X/4 SRXP1
near chipset device issue

+2.5VSB: C388 C0.1U25Y, C244, CM3
X_C4.7U10Y0805, X_C1U16Y — near chipset

C386 C1U16Y/B, C389 C1U16Y/B, CB72 C0.1U16Y0402, CB95 C1U16Y/B, CM1 C4.7U10Y0805

T1 BIT_CLK — BIT_CLK [23], SDIN0 [23]
U3 SDIN0, V2 SDIN1, U1 SDIN2, V3 SDIN3
T2 ACSYNC, U2 ACSDO, T3 ACRST — RN69 8P4R-33R0402 — SDOUT [23], -ACRST [23], SYNC [23]
W4 PME# — PME# [20,22]
V4 -BATLOW, Y1 PEPMESCI_SB, V2 -RING, Y3 -SUSST, Y4 THERM# — -SUSST [10], THERM# [22]
AA1 -EXTSMI, AB1 -SMBALT, AC1 -LID, AD2 -PWRBTN, AE1 -PWROK_NB — -PWROK_NB [10]
AB7 -CLKRUN, AC7 -CPUSTP, AD6 -PCISTP
AE1 INTRUDER
AB3 SUS_CLK
AC4 SMBCLK_ISO — SMBCLK_ISO [12,16,27]
AB2 SMBDATA_ISO — SMBDATA_ISO [12,16,27]
AC3 SMBCK2, AD1 ATADET — ATADET [24]
AA2 -SUSA, AD3 SLP_S3#, AF2 SLP_S5# — SLP_S3# [22,27,29], SLP_S5# [27]
AE2 GPI0, AC2 PEWAKE_SB#, AA3 GPO0, AE3 GPO1, AE5 GPIOA, AD5 GPIOB, AF5 GPIOC, AC6 GPIOD
GPI24 / GPO24 (GPIOA) / PCREQA / strap
GPI25 / GPO25 (GPIOB) / PCREQB / strap
GPI30 / GPO30 (GPIOC) / PCGNTA / strap
GPI31 / GPO31 (GPIOD) / PCGNTB / strap
AD9 SERIRQ — SERIRQ [22]
AF8 SPKR, AB8 SB14MHZ — SB14MHZ [16]
AF9 TPO, AE9 TEST
AC10 VDDA0, AB10 GNDA0, AD11 SREXT — C390 C1U16Y/B, R335 4.7KR1%0402
AE10 SXO, AE10 SXI
AE11 VCCA33 — VCC3, C304 X_C0.1U25Y
AE11 GNDA33
W5 GND#W5, V5 GND#V5, M16 GND#M16, N11 GND#N11, N12 GND#N12, N13 GND#N13, N14 GND#N14, N15 GND#N15, N16 GND#N16
W12 VCCATS, W13 VCCATS#W13, W14 VCCATS#W14, W15 VCCATS#W15, W16 VCCATS#W16
AC17 VCCAO#AC17, AC11 VCCAO, AB17 VCCAO#AB17, AB11 VCCAO#AB11
AB15 STX2+, AC15 STX2-, AE15 SRX2-, AE15 SRX2+
AB13 STX1+, AC13 STX1-, AE13 SRX1-, AE13 SRX1+
AC19 SDVREF, AB21 SDCOMP
AA4 AB4 AB5 AB6 T4 U4 — VCC3_SB2.5V_SB
J9 J10 J11 J12 K9 L9 L8 M9 M18 N9 N18 P9 P18 R9 R18 T9 T8 U9 U18 V9 V10 V11 V12 V13 V14 V15 V16 V18 — +2.5VSB
VCC25 VCC25#J10 VCC25#J11 VCC25#J12 VCC25#K9 VCC25#L9 VCC25#L18 VCC25#M9 VCC25#M18 VCC25#N9 VCC25#N18 VCC25#P9 VCC25#P18 VCC25#R9 VCC25#R18 VCC25#T9 VCC25#T18 VCC25#U9 VCC25#U18 VCC25#V9 VCC25#V10 VCC25#V11 VCC25#V12 VCC25#V13 VCC25#V14 VCC25#V15 VCC25#V16 VCC25#V17 VCC25#V18
VSUS33 VSUS33#AB4 VSUS33#AB5 VSUS33#AB6 VSUS25 VSUS25#U4
GNDATS GNDATS#AB14 GNDATS#AC14 GNDATS#AD12 GNDATS#AD13 GNDATS#AD14 GNDATS#AD15 GNDATS#AD16 GNDATS#AE12 GNDATS#AE14 GNDATS#AE16 GNDATS#AF12 GNDATS#AF14 GNDATS#AF16
GNDAS GNDAS#AC12 GNDAS#AB16 GNDAS#AB12
GND#F6 GND#F7 GND#J5 GND#K5 GND#P5 GND#R5 GND#C18 GND#C19 GND GND#L14 GND#L15 GND#L16 GND#A23 GND#B13 GND#A2 GND#B1 GND#M14 GND#M15 GND#K18
AB14 AC14 AD12 AD13 AD14 AD15 AE12 AE14 AE16 AE12 AE14 AE16 AC16 AC12 AB16 AB12 F6 F7 J5 K5 P5 R5 L11 L13 L14 L15 L16 M11 M12 M13 M14 M15 K18

VCC3_SB — PEWAKE_SB# R345 10K/4

SATA1 — CONN-SATA1P_ORANGE
STXP_1, STXN_1, SRXN_1, SRXP_1

[19] VGATE, [19,22] -LDRQ — RN78 8P4R-2.7KR0402 (VGATE, TEST, -CLKRUN, -LDRQ) — VCC3

SXO, SXI — Y3 25MHZ18P_D-4, C327 C16P50N, C321 C16P50N

-PWRBTN — R348 68R0402 — PWRBTN# [29]
C334 C0.1U25Y
VCC3 — C303 X_C0.1U25Y

Title	VT8237-2(IDE,STAT,GPIO)
Size	Custom
Document Number	MS-7364-V0A-0207-G
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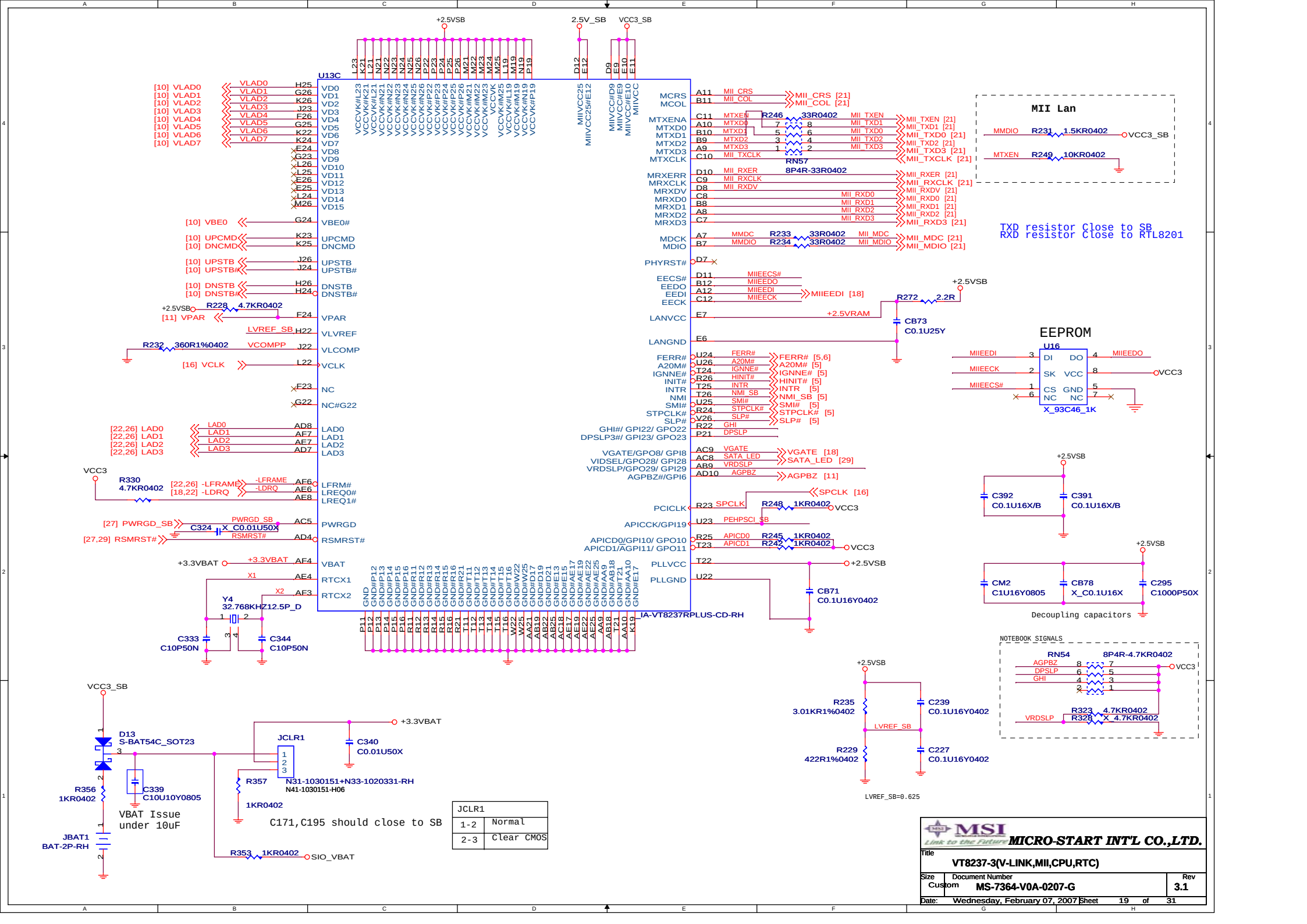
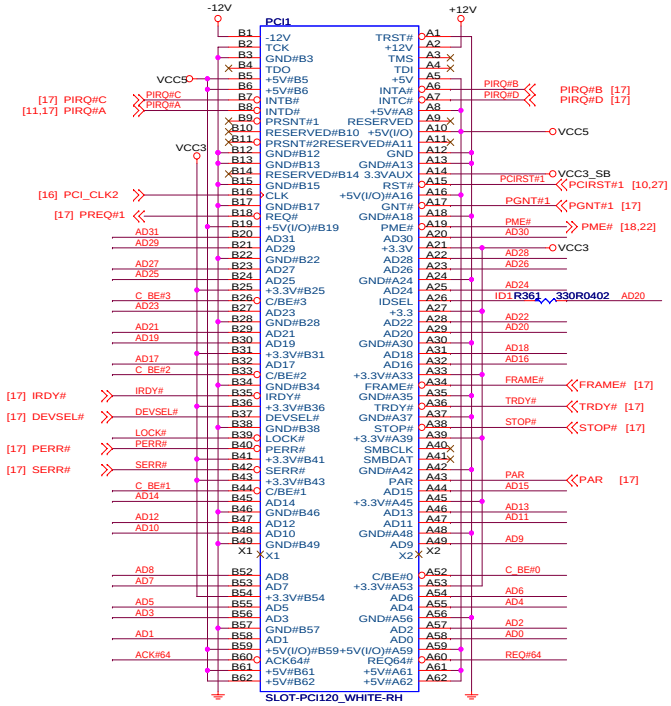
MSI MICRO-START INTL CO.,LTD.

1 - Enable


U13C
IA-VT8237RPLUS-CD-RH
+2.5VSB
2.5V_SB
VCC3_SB
MII Lan
MMDIO
MTXEN
R231 1.5KR0402
R249 10KR0402
VCC3_SB
TXD resistor Close to SB
RXD resistor Close to RTL8201
EEPROM
U16
X_93C46_1K
MIIEEDI
MIIEECK
MIIEECS#
MIIEEDO
VCC3
R272 2.2R
CB73
C0.1U25Y
+2.5VRAM
R228 4.7KR0402
VPAR
LVREF_SB
R232 360R1%0402
VCOMPP
VCLK
R330 4.7KR0402
-LFRAME
-LDRQ
PWRGD_SB
C324 X_C0.01U50X
RSMRST#
Y4
32.768KHZ12.5P_D
C333 C10P50N
C344 C10P50N
+3.3VBAT
C392 C0.1U16X/B
C391 C0.1U16X/B
CM2 C1U16Y0805
CB78 X_C0.1U16X
C295 C1000P50X
Decoupling capacitors
CB71 C0.1U16Y0402
R248 1KR0402
R245 1KR0402
R242 1KR0402
NOTEBOOK_SIGNALS
RN54 8P4R-4.7KR0402
R323 4.7KR0402
R328 X_4.7KR0402
R235 3.01KR1%0402
R229 422R1%0402
C239 C0.1U16Y0402
C227 C0.1U16Y0402
LVREF_SB=0.625
D13 S-BAT54C_SOT23
JBAT1 BAT-2P-RH
R356 1KR0402
C339 C10U10Y0805
VBAT Issue under 10uF
JCLR1
N31-1030151+N33-1020331-RH
N41-1030151-H06
R357 1KR0402
C340 C0.01U50X
R353 1KR0402
SIO_VBAT
C171,C195 should close to SB
JCLR1
1-2 Normal
2-3 Clear CMOS
MICRO-START INT'L CO.,LTD.
Title
VT8237-3(V-LINK,MII,CPU,RTC)
Size Custom
Document Number MS-7364-V0A-0207-G
Rev 3.1
Date: Wednesday, February 07, 2007
Sheet 19 of 31

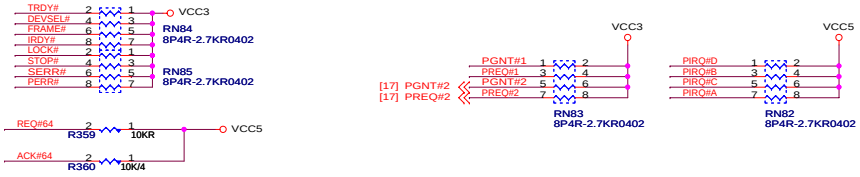
[17] AD[0..31] AD[0..31]
[17] C_BE#[0..3] C_BE#[0..3]

PCI SLOT 2

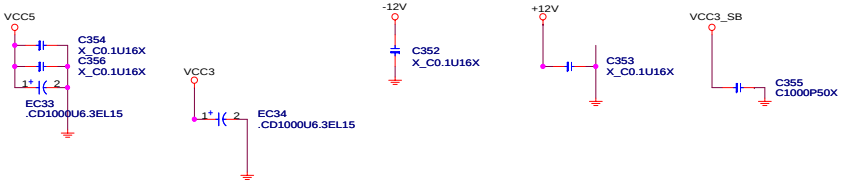


IDSEL = AD20
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS

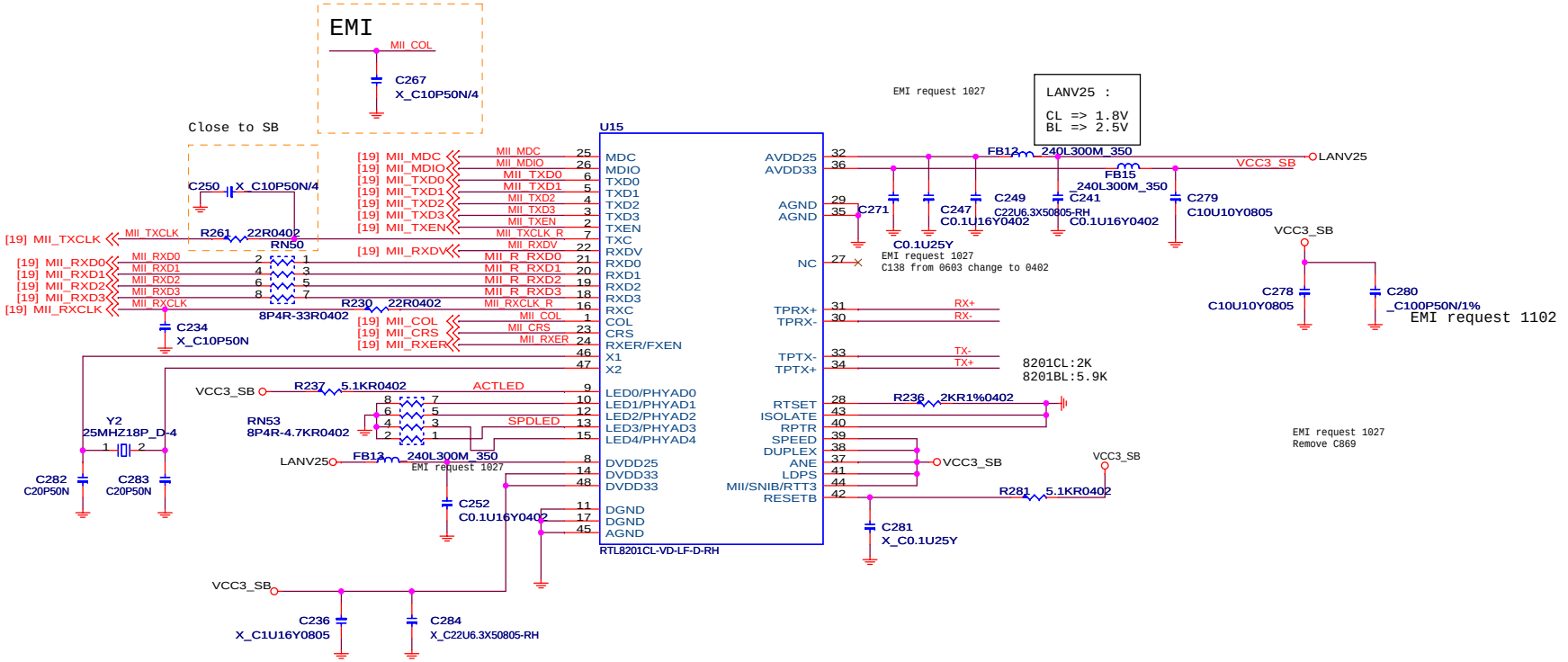


PCI SLOT DECOUPLING CAPACITORS



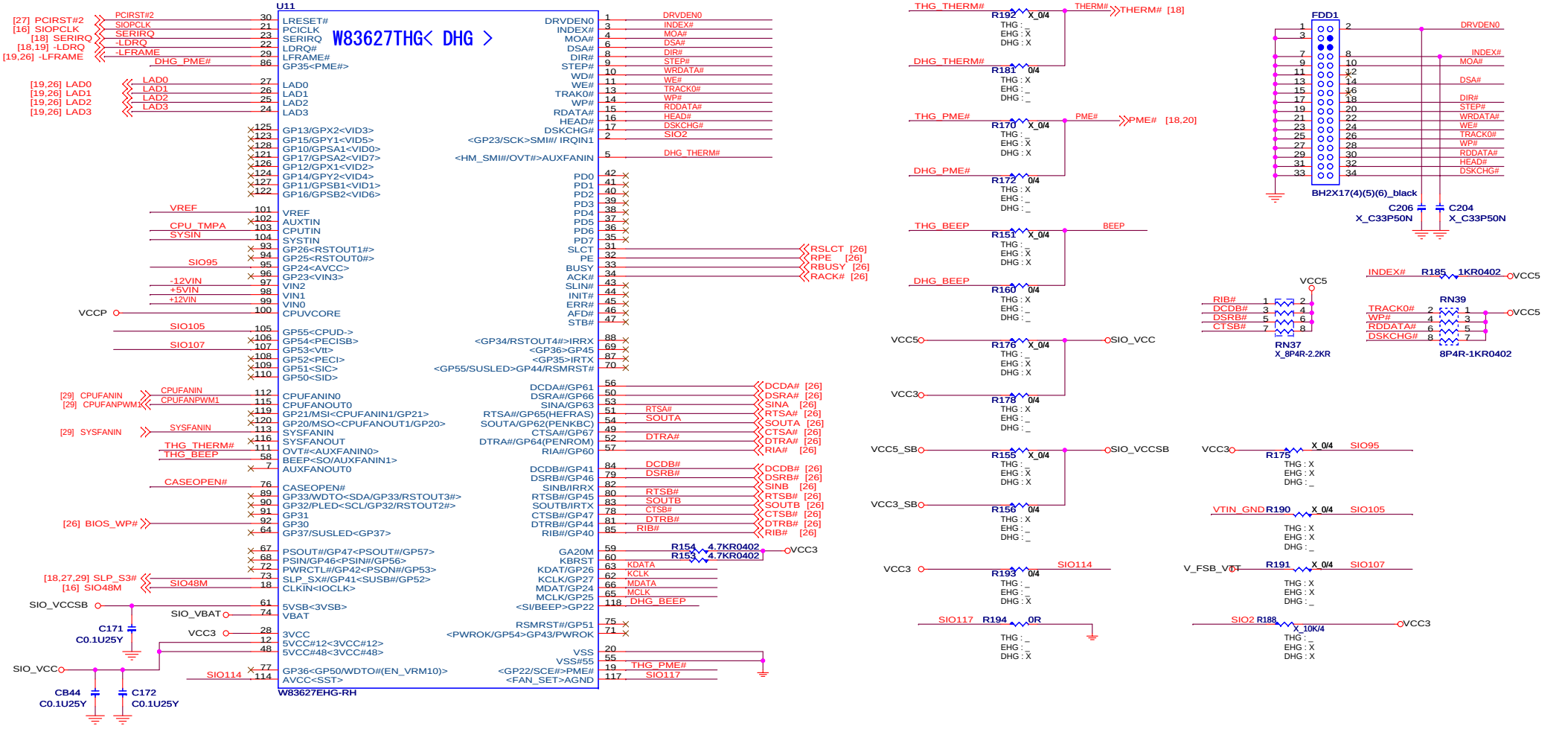
MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

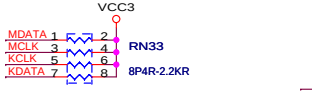
Title	PCI Slot 1 & 2 & 3	
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 20 of 31	

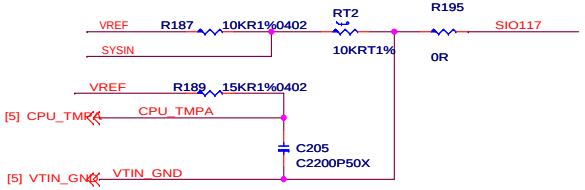


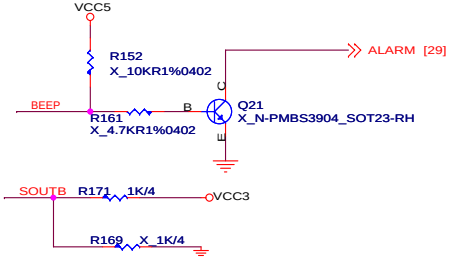
MICRO-START INT'L CO.,LTD.

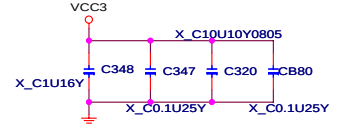
Title	Realtek 8201CL	
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 21 of 31	

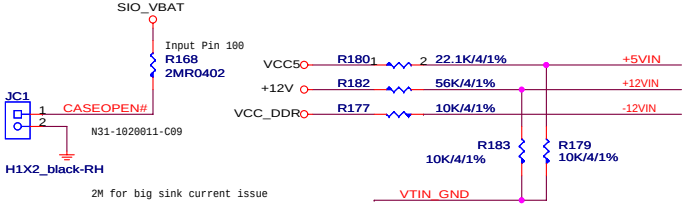












Chasiss Intrusion

Straps W83627DHG

SOUTB	L:1K R466	PWMOUT 50%	FOR CPUFANOUT 1
	H:1K R465	PWMOUT100%	

Straps W83627THG

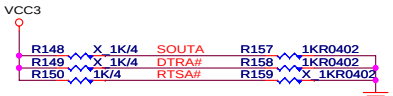
SOUTB	L:1K R466	24MHz	For CLKIN(pin 18)
	H:1K R465	48MHz	

FWH DECOUPLING CAPACITORS

Place Cap. as Close to FWH< 350 mil

Straps W83627THG

RTSA#	L: CFAD=2E *	H: CFAD=4E
SOUTA	L: KBC DISABLE *	H: KBC ENABLE
DTRA#	L: DISABLE Logical Device	H: ENABLE Logical Device *



Straps W83627DHG

RTSA#	L: CFAD=2E *	H: CFAD=4E
GP50	L: TTL LEVEL	H: VRM10 LEVEL
SOUTA	L: KBC DISABLE *	H: KBC ENABLE
DTRA#	L: DISABLE SPI *	H: ENABLE SPI

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: Super I/O & FAN 83627EHG

Size: Custom | Document Number: MS-7364-V0A-0207-G | Rev: 3.0

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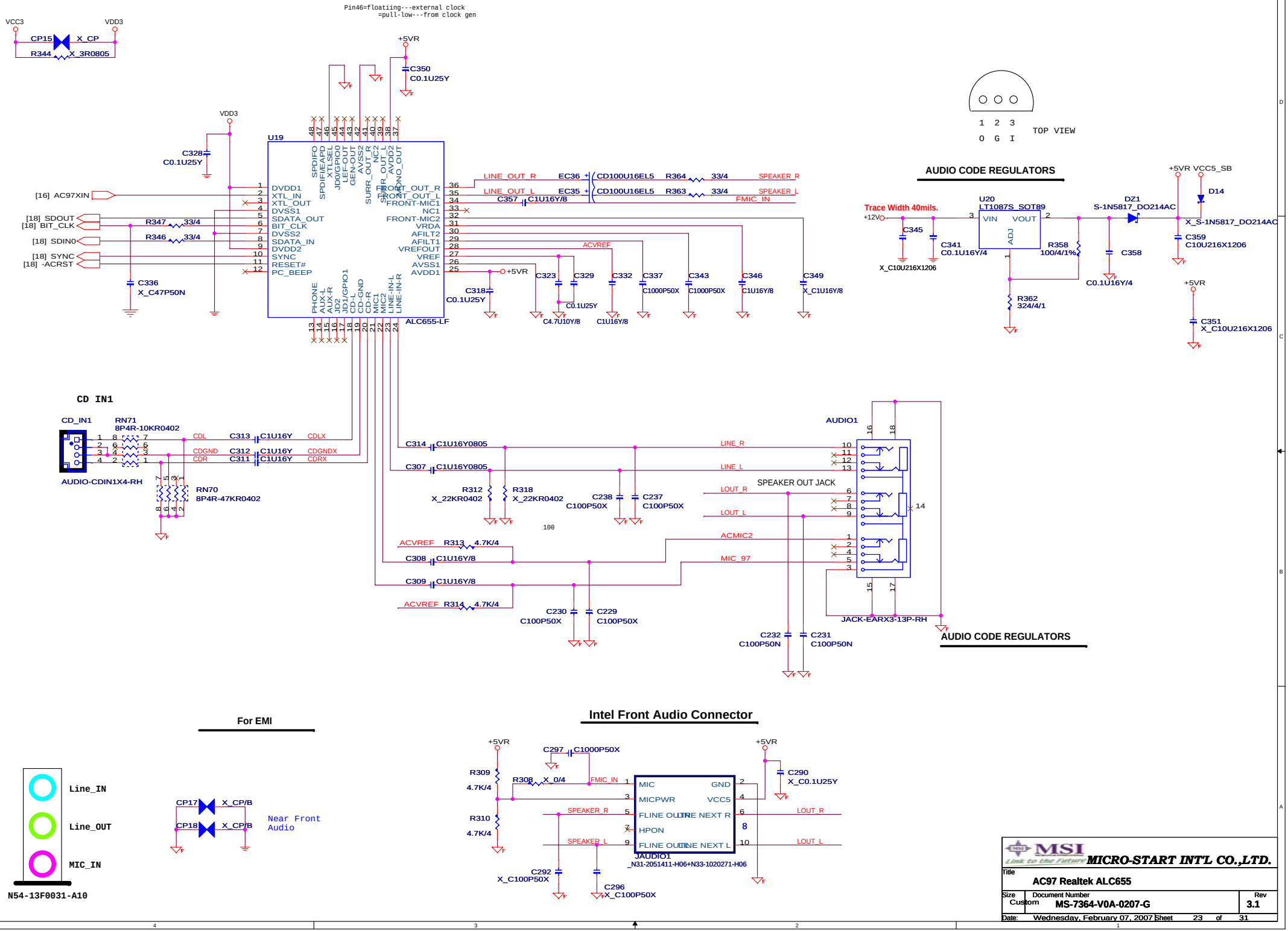


MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	AC97 Realtek ALC655	
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 23 of 31	

IDE1 AND IDE2

PRIMARY

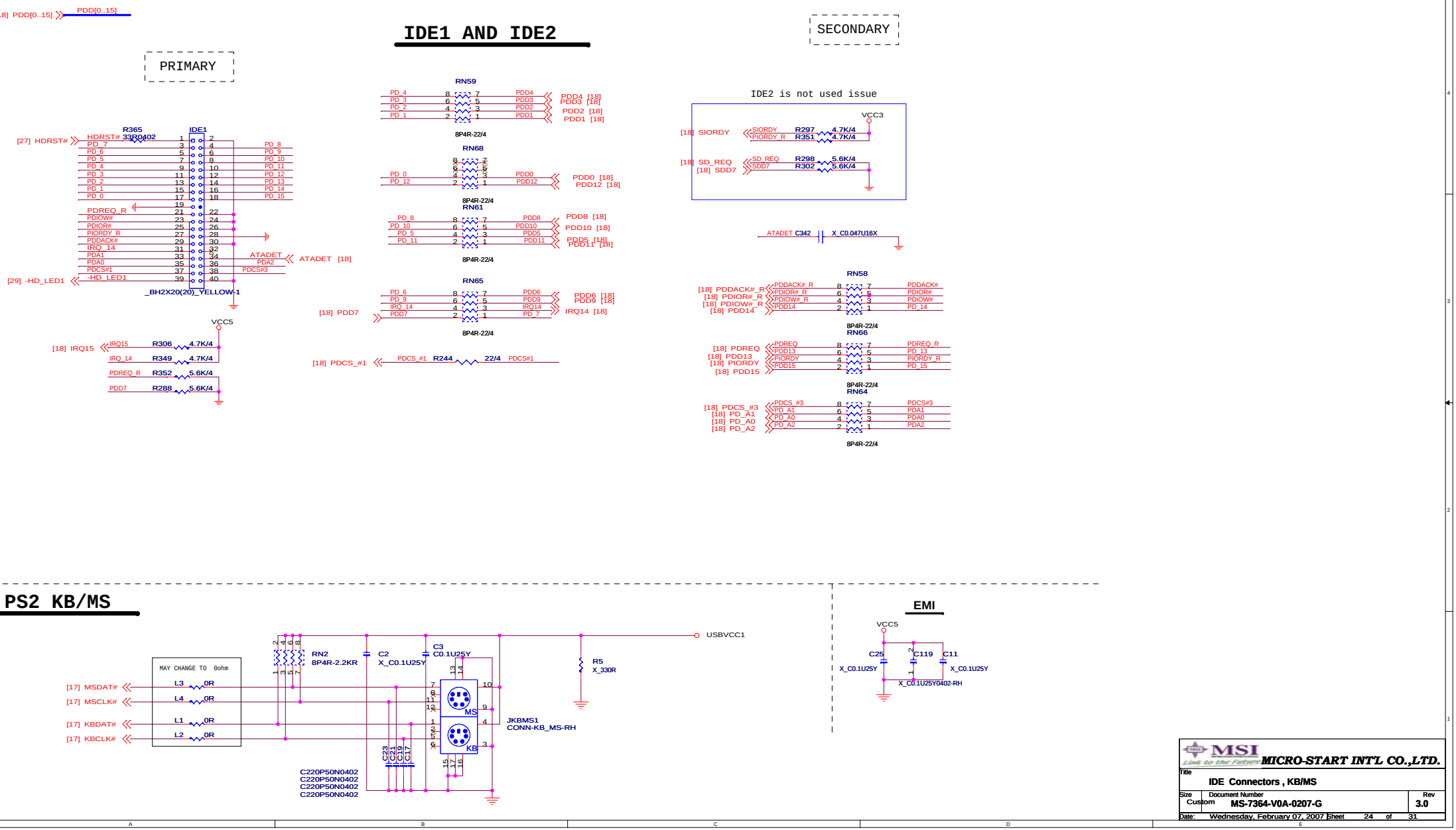
SECONDARY

[18] PDD[0..15] — PDD[0..15]

IDE2 is not used issue

PS2 KB/MS

EMI



MSI — MICRO-START INT'L CO.,LTD.		
Title: IDE Connectors , KB/MS		
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.0
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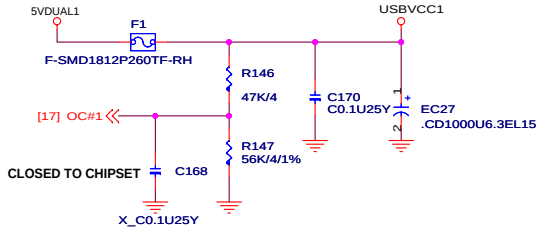
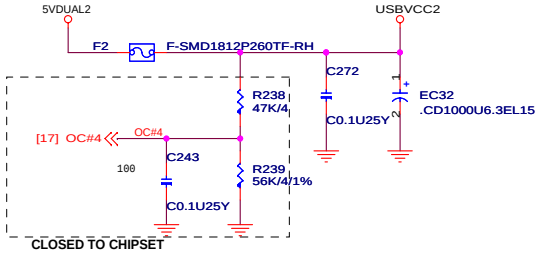
Rear USB Connectors

43mOHM X 2 A= 86mV

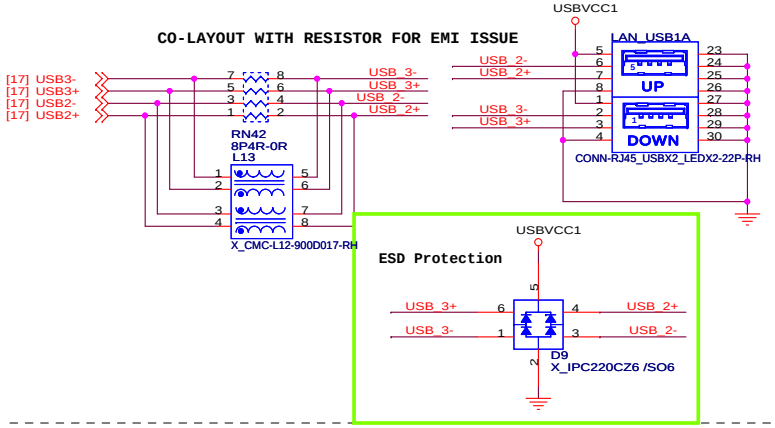


Front USB Connectors



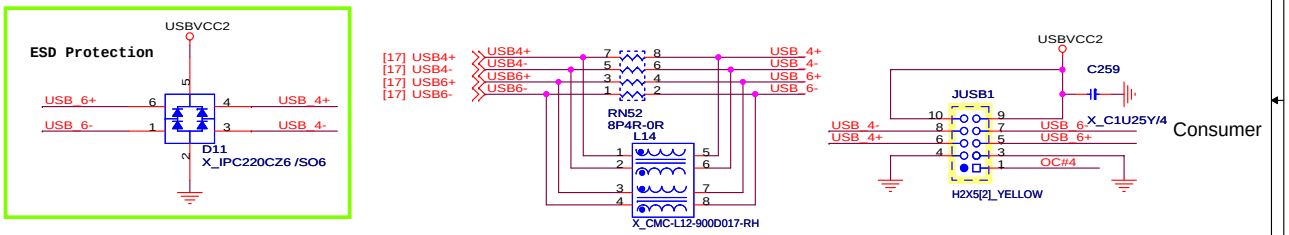
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

CO-LAYOUT WITH RESISTOR FOR EMI ISSUE

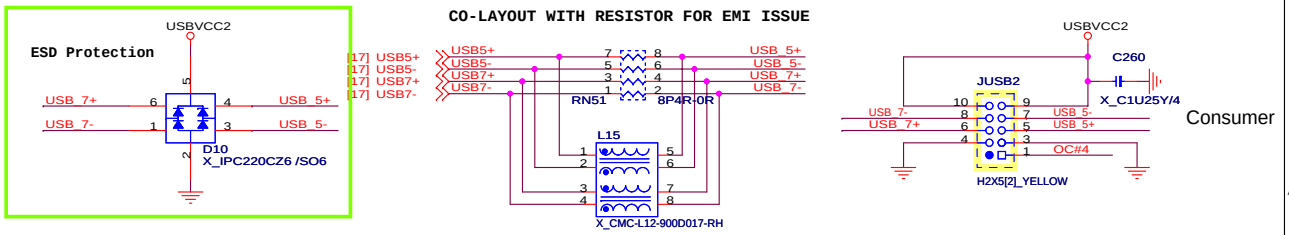


FRONT PANEL USB CONNECTOR FOR USB PORT 4,6

CO-LAYOUT WITH RESISTOR FOR EMI ISSUE



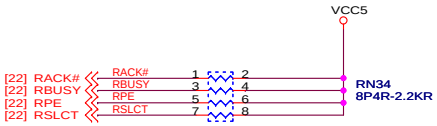
FRONT PANEL USB CONNECTOR FOR USB PORT 5,7



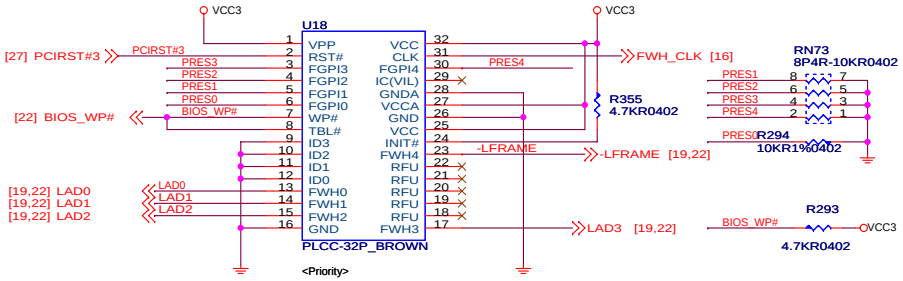
MICRO-START INT'L CO.,LTD.

Title: USB Connectors		
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 25 of 31	

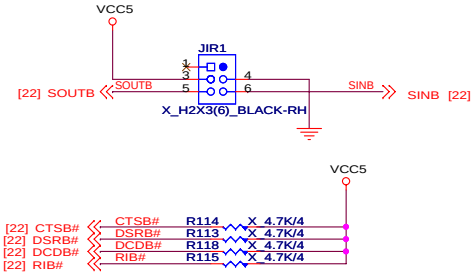
PRINTER PORT



Flash Rom

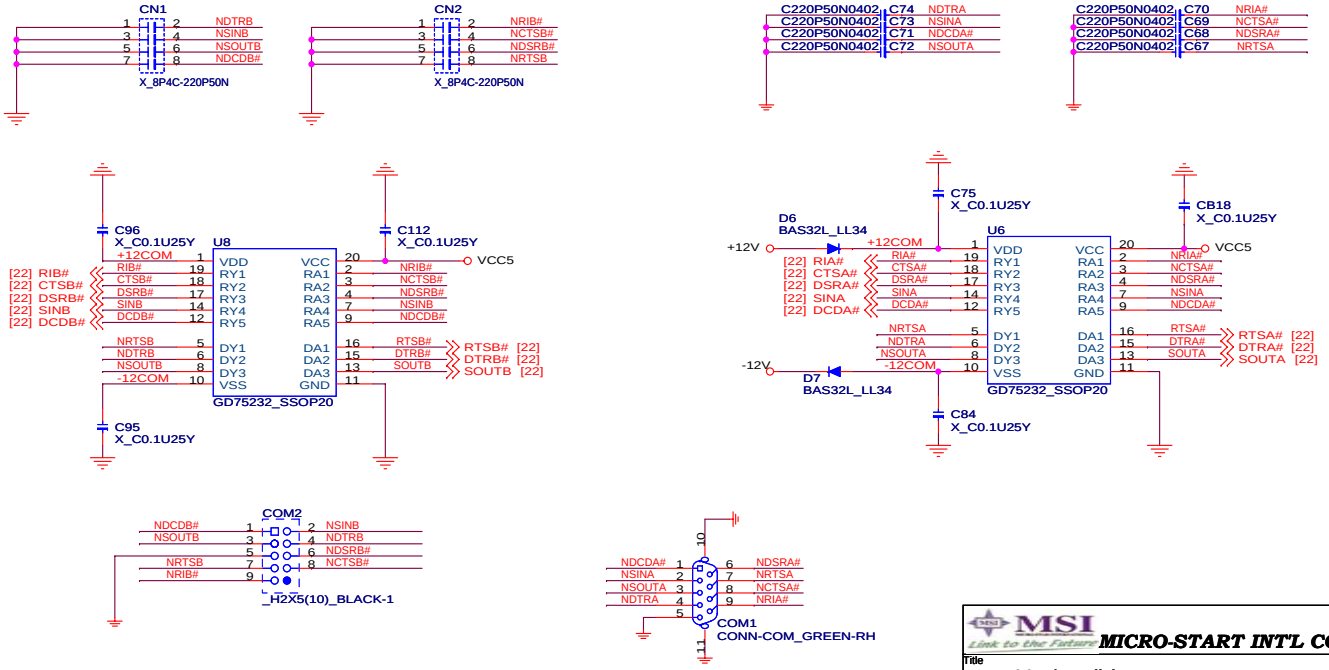


Intel Front IR Header



Notice: If system only get IR function but COMB. Those input pins need external pull up resistors incase transfer interrupt in IR.

SERIAL PORT 2



Title	COM / Parallel Port	
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.0
Date: Wednesday, February 07, 2007	Sheet 26 of 31	

MICRO-START INT'L CO.,LTD.

Gate Trace 8 mils
Sense Trace 8 mils

MOS	RDS(ON)	Vdss	Vgs	Id	Package	Qg
P07N03LV	25.0m	30V	20V	7A	SO-8	13
APM7313	28.0m	30V	20V	6A	SO-8	20
P3055LD	90.0m	25V	20V	12A	TO-252	20
P45N02LD	28.0m	25V	20V	45A	TO-252	30
P50N03LD	12.0m	27V	20V	50A	TO-252	50
NDS351	117m	30V	20V	2.5A	SOT-23	4
2N7002	7.5	60V	20V	115mA	SOT-23	
PHKD6N02LT	20.0m	20V	12V	6A	SO-8	20

3VSB MODE SELECT

3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM LINEAR OR PWM SELECT

For MS-7 + MS-8
Added For MS7 Ver:RAC

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

Connect to MS7_S3 for MS7 Ver:RAC

5V Dual Power

Rear USB ports

Front USB ports

NN-P2103HVG_SOP8-LF

Low RDS ON MOSFET

Rds(on)=0.02ohm Vgs=1V Id=7A

20mOHM X 2 A= 40mV
50mil 1inch 9.53mOHM

DDR TYPE DET

MS-7G-RBC-LF

8237
VCC3 should lead VCC2.5 by 1.5 ~ 2ms

close to MS7

WIDE TRACE

VTT
CPU Imax=3.5A
NB Imax=1.5A(Intel)

Rds(on)=0.054ohm@6V Vgs=0.6~1.5V Id=6A

Rds(on)=0.027ohm Vgs=1V Id=6A

2.5V_SB Power

DIMMx4=8A
NB I/O=4.1A
Stand-by=345mA
Vtt=2A
refer to Intel

1.5V

N-P45N02LDG_TO252-RH

+1.5VSUS

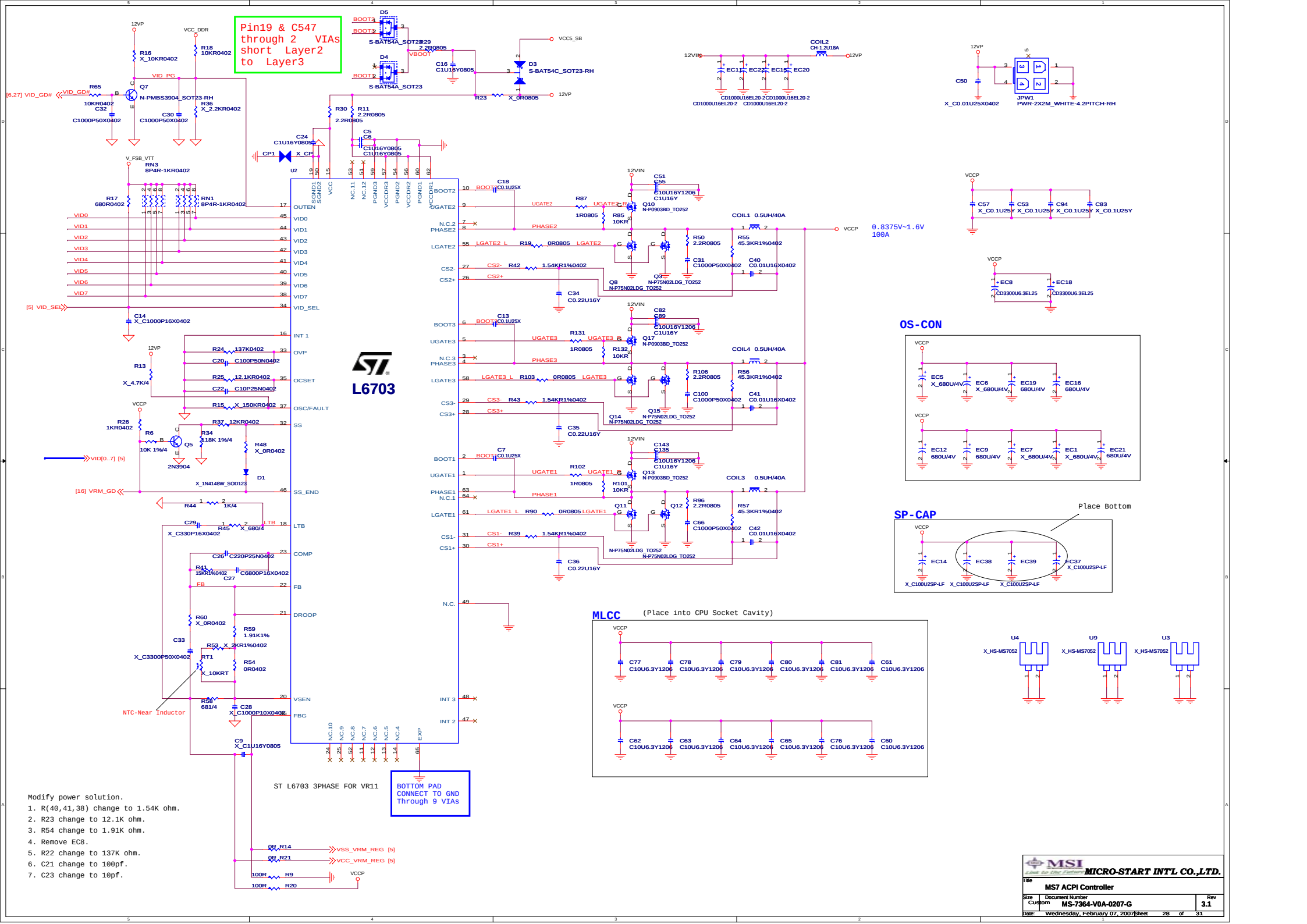
N-APM2306_SOT23

DDR VTT Power

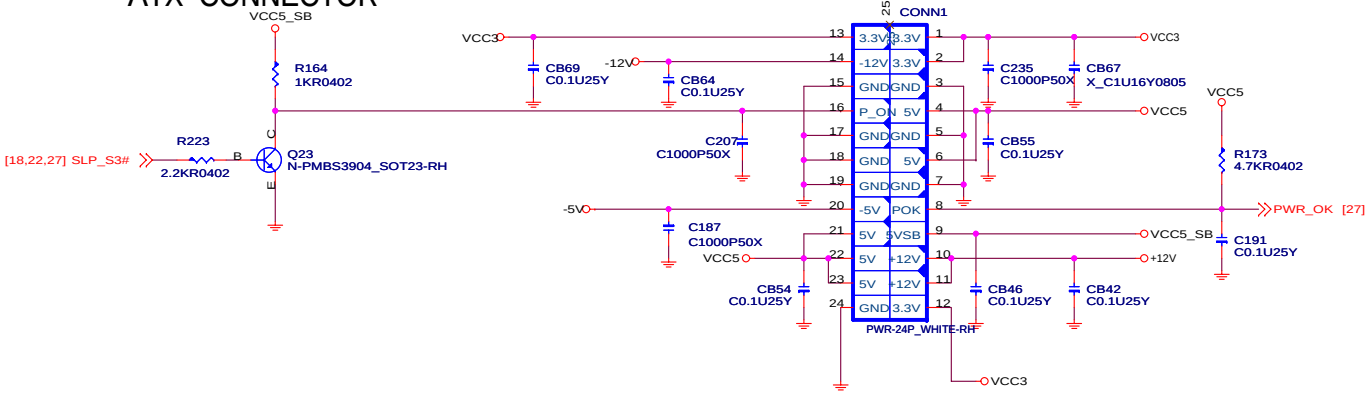
W83310DG_SOP8-RH

MICRO-START INT'L CO.,LTD.

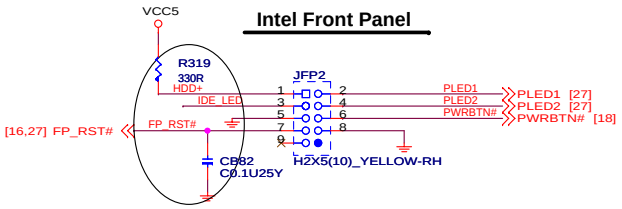
Title	MS7 ACPI Controller	
Size: Custom	Document Number: MS-7364-V0A-0207-G	Rev: 3.1
Date: Wednesday, February 07, 2007	Sheet 27 of 31	


Pin19 & C547 through 2 VIAs short Layer2 to Layer3
L6703
ST L6703 3PHASE FOR VR11
BOTTOM PAD CONNECT TO GND Through 9 VIAs
OS-CON
SP-CAP
Place Bottom
MLCC
(Place into CPU Socket Cavity)
0.8375V~1.6V 100A
NTC-Near Inductor
Modify power solution.
1. R(40,41,38) change to 1.54K ohm.
2. R23 change to 12.1K ohm.
3. R54 change to 1.91K ohm.
4. Remove EC8.
5. R22 change to 137K ohm.
6. C21 change to 100pf.
7. C23 change to 10pf.
MICRO-START INT'L CO.,LTD.
MS7 ACPI Controller
MS-7364-V0A-0207-G
3.1
Wednesday, February 07, 2007

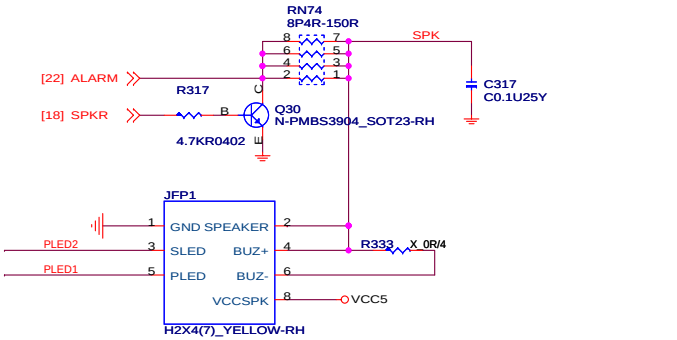
ATX CONNECTOR



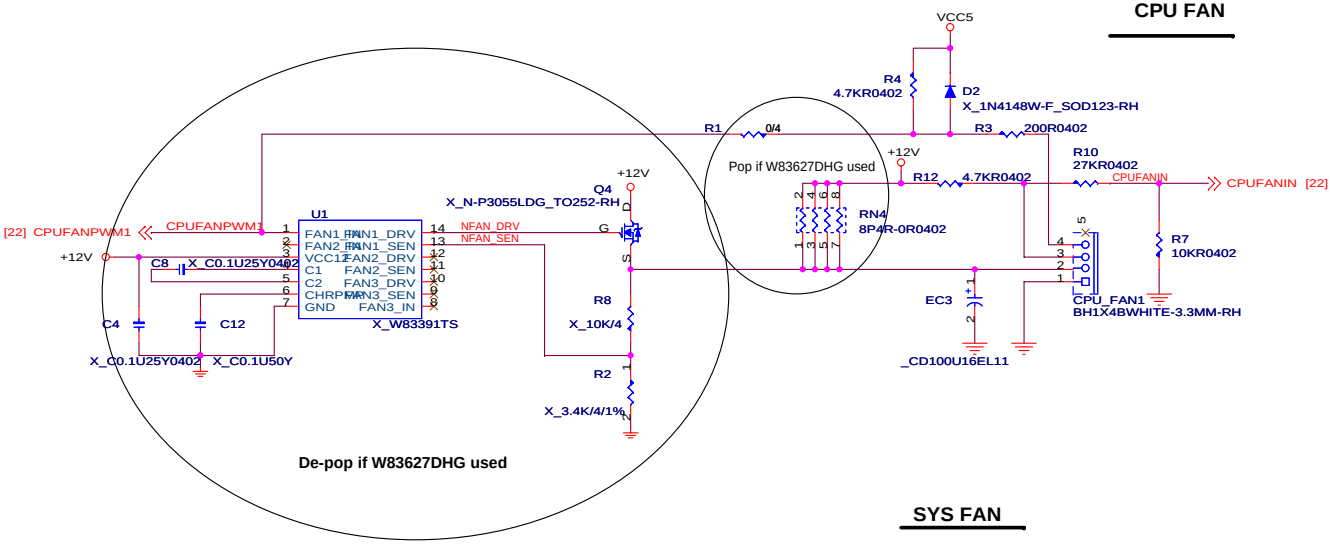
Intel Front Panel



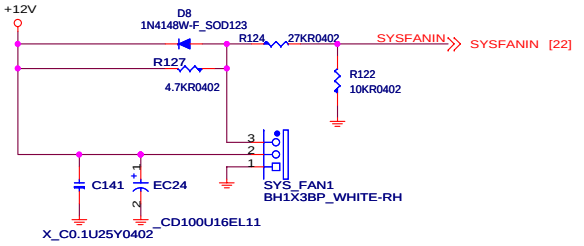
SPEAKER

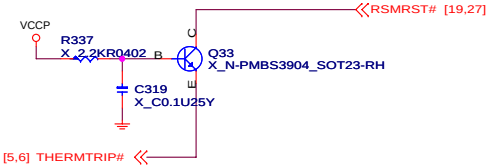


CPU FAN

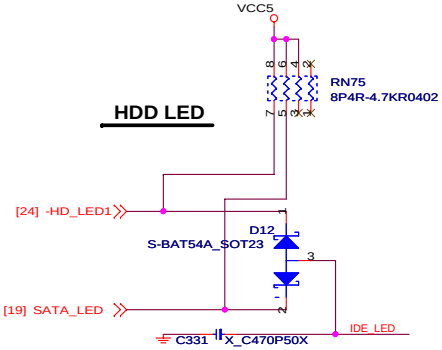


SYS FAN





HDD LED



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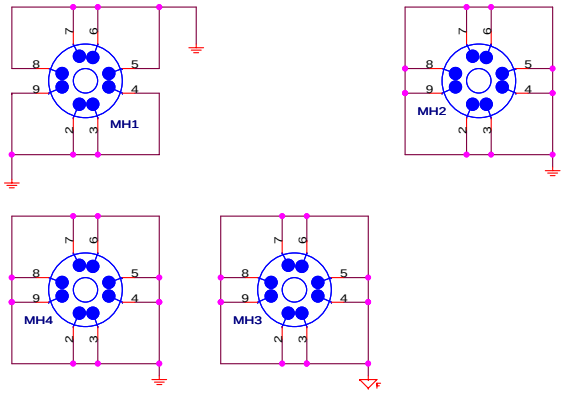
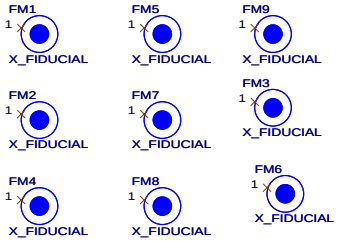
PCB OTHER COMPONENT

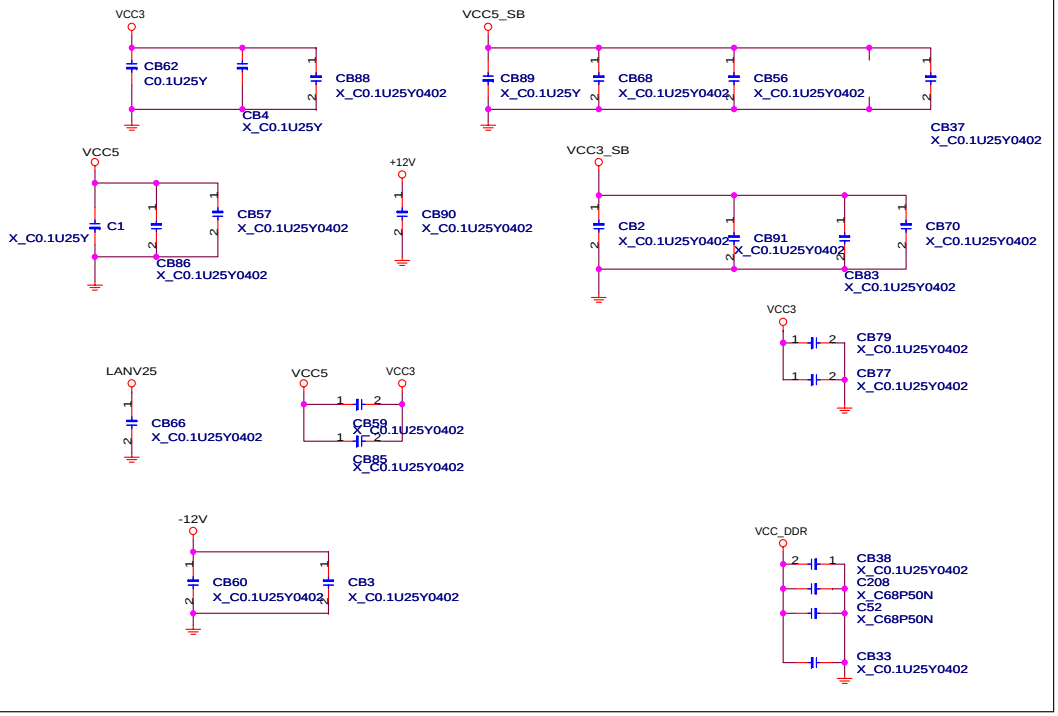


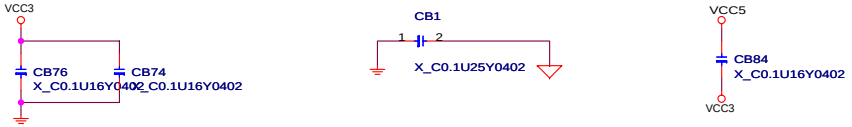
FIDUCIALS



EMI

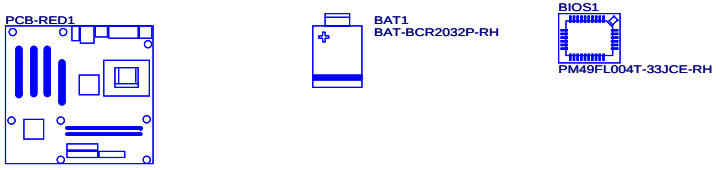
original EMI caps





Reserved EMI caps on 2006/10/31,from V3.0 to V3.1

Manual Part



P80-0725531-Y34,元茂
P80-0725531-D05,昆穎

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3.0 change to 3.1

Page12 :
1). Connect SMBUS to DDR & PCI-express slot.

Page14 :
1). Connect SMBUS to DDR & PCI-express slot.

Page16 :
1). R258 short, change net name "MCLKIT" to MCLKIT_R between R258 and clock generator.Change R258 to 0 ohm.
2). Reserve a 0 ohm resistor between "FP_RST#" and "RESET_IN#/RESET#".
3). Swap RN47 pin6 & pin8 (NBHCLK & NBHCLK#)
4). Uninstall R303 & 299,49.9 ohm pull-lo resistors are build in clock generator.
5). Swap net "H_BSL1" & "H_BSL2".
6). Change net name "SYNC" to SYNC_NB. Because the net name "SYNC" as same as AC'97 net "SYNC"

Page19 :
1). Reserved a EEPROM for LAN mac ID, reserved a pull-lo resistor on "MIIEEDI" to enable EEPROM.

Page22 :
1). Add case open function.
2). Modify SPI power to VCC3.
3). Modify RN26 power to VCC5.
4). Reserved a cap for VREF.
5). Uninstall SPI flash rom, use LPC flash rom to boot up system.

Page24 :
1). Swap IDE1 & IDE2 location.

Page29 :
1). Uninstall system fan control function.

Page30 :
1). Reserved EMI caps.

Page28 :
1). Add a cooper to connect digital GND and analog GND, place near C25.
2). Modify output choke's footprint to CHK_PMC109_R60M_M1 and change choke value to 0.5uH.
3). Uninstall one lo-side MosFET to keep 6*MosFET per phase.

2006/11/23 MS-7255 version3.1 ECN modify

Page22 :
1). Remove PLCC socket.
2). W83627DHC change to C version.

Page16 :
1). Modify clock skew issue.
2). Remove SMBUS damping resistors.

Page28 :
1). Modify power solution.

MSI Link to the Future MICRO-START INT'L CO.,LTD.

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