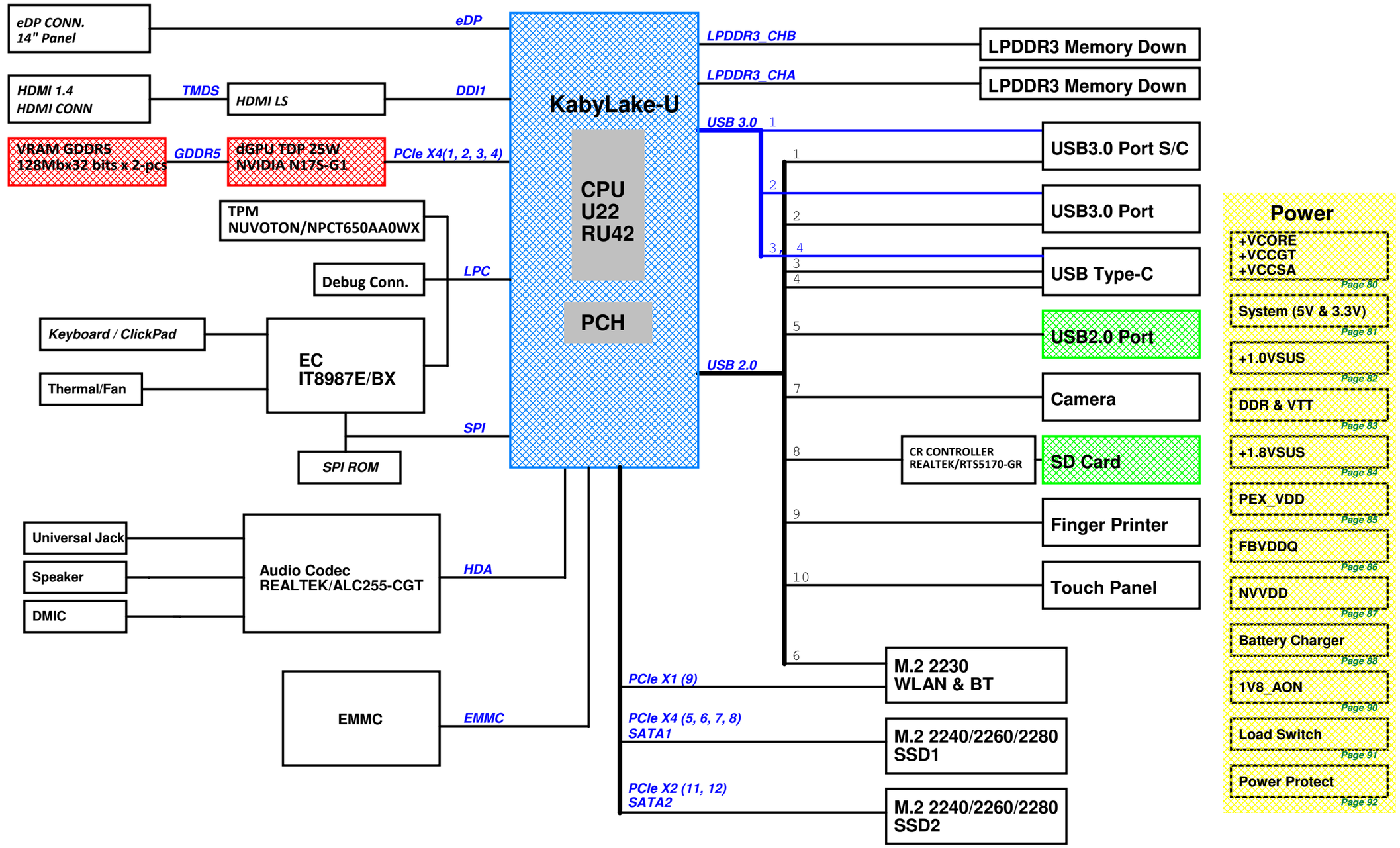
HE4EA Block Diagram



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD

Title : Block Diagram
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Wednesday, March 29, 2017 Sheet 1 of 94

Option

Optional	Remark
N/A	Mount
/@	Ummount
/Debug	Debug only
/EMI	Reserved EMI part
/UMA	Support UMA
/VGA	Support VGA
/SDP	Support SDP DRAM
/DDP	Support DDP DRAM
/U22	Support 2+2 CPU
/U42	Support 4+2 CPU
/14inch	Support 14"
/15inch	Support 15"
/TPM	Support TPM function
/IOAC	Support IOAC
/NON-IOAC	Not support IOAC
/PTP	Support PTP
/NON-PTP	Not support PTP
/SSD1	Support M.2 SSD1
/SSD2	Support M.2 SSD2
/EMMC	Support EMMC

PEGATRON Title : Option

BG1-HW RD Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Wednesday, March 29, 2017 Sheet 2 of 94

03

CPU(1)_DDI_eDP

+1.0V
+3VS
+VCCIO

+1.0V 5,7,9,25,32,57,91
+3VS 4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+VCCIO 5,7,9,57,91

DDI#1 DDPB_CTRLDATA
DDI#2 DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
 1 : port is detecctd

SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

DDI Port 1: HDMI

U0301A

48 HDMI_TXN2 — E55 DDI1_TXN[0]
48 HDMI_TXP2 — F55 DDI1_TXP[0]
48 HDMI_TXN1 — E58 DDI1_TXN[1]
48 HDMI_TXP1 — F58 DDI1_TXP[1]
48 HDMI_TXN0 — F53 DDI1_TXN[2]
48 HDMI_TXP0 — G53 DDI1_TXP[2]
48 HDMI_CLKN — F56 DDI1_TXN[3]
48 HDMI_CLKP — G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI

48 HDMI_SCL_PCH — DDPB_CTRLCLK L13 — GPP_E18/DDPB_CTRLCLK
48 HDMI_SDA_PCH — DDPB_CTRLDATA L12 — GPP_E19/DDPB_CTRLDATA

DDPC_CTRLCLK N7 — GPP_E20/DDPC_CTRLCLK
DDPC_CTRLDATA N8 — GPP_E21/DDPC_CTRLDATA

N11 GPP_E22
N12 GPP_E23

+VCCIO
R0301 2 1% 1 24.9Ohm DP_COMP E52 — eDP_RCOMP

DISPLAY SIDEBANDS

947859
0101-03860PB

EDP

EDP_TXN[0] C47 EDP_TXN0 → EDP_TXN0 45
EDP_TXP[0] C46 EDP_TXP0 → EDP_TXP0 45
EDP_TXN[1] D46 EDP_TXN1 → EDP_TXN1 45
EDP_TXP[1] C45 EDP_TXP1 → EDP_TXP1 45
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

E45 EDP_AUXN → EDP_AUXN 45
F45 EDP_AUXP → EDP_AUXP 45
EDP_AUXN
EDP_AUXP

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
RSVD_1 G46
RSVD_2 F46

GPP_E13/DDPB_HPD0 L9 DPB_HPD → DPB_HPD 48
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L6 EXT_SMI#_R — SP0302 1 2 0Ohm — EXT_SMI# → EXT_SMI# 30,44
GPP_E16/DDPE_HPD3 N9 EXT_SCI#_R — SP0303 1 2 0Ohm — EXT_SCI# → EXT_SCI# 30
GPP_E17/EDP_HPD L10 eDP_HPD → eDP_HPD 45

eDP_BKLTEN R12 LCD_BKLTEN_PCH → LCD_BKLTEN_PCH 21,45
eDP_BKLTCTL R11 LCD_BL_PWM_PCH → LCD_BL_PWM_PCH 45
eDP_VDDEN U13 EDP_VDD_EN → EDP_VDD_EN 45

DDPB_CTRLDATA
DDPB_CTRLCLK
both pull-up deleted, HDMI side pull-up

+3VS
DDPC_CTRLDATA R0305 1 @ 2 2.2KOhm
DDPC_CTRLCLK R0340 1 @ 2 2.2KOhm

+3VS
EXT_SCI# R0307 1 2 10KOhm
EXT_SMI# R0308 1 2 10KOhm

HDMI HPD

eDP HPD

+1.0V R0311 1KOhm
+VCCIO R0312 1KOhm 5%

141024 follow PDG V1.0 Table 10-4
Rpu = 1K ohm 5%
Rs = 500 ohm 5%

Closeer EC

+1.0V R0313 49.9Ohm 1% @

32 H_THRMTRIP#
H_PROCHOT# R0314 1 2 499Ohm 30 H_PECI_EC
R0315 1 2 43Ohm
SP0301 1 2 0Ohm @/SP
T0306 1 SKTOCC#
T0301 1

TP_CATERR#_R D63 CATERR#
H_PECI A54 PECI
H_PROCHOT#_R C65 PROCHOT#
H_THRMTRIP#_R C63 THERMTRIP#
SKTOCC# A65

CPU MISC

C55 BPM#[0]
D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

A6 GPP_E3/CPU_GP0
A7 GPP_E7/CPU_GP1
BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3

R0316 1 2 49.9Ohm CPU_POPIRCOMP AT16 PROC_POPIRCOMP
R0317 1 2 49.9Ohm PCH_POPIRCOMP AU16 PCH_OPIRCOMP
R0318 1 2 49.9Ohm EDRAM_OPIO_RCOMP H66 OPCE_RCOMP
R0319 1 2 49.9Ohm EOPIO_RCOMP H65 OPC_RCOMP

947859
0101-03860PB

JTAG

PROC_TCK B61 XDP_TCLK
PROC_TDI D60 XDP_TDI_CPU
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS_CPU
PROC_TRST# B59 XDP_TRST_CPU_N

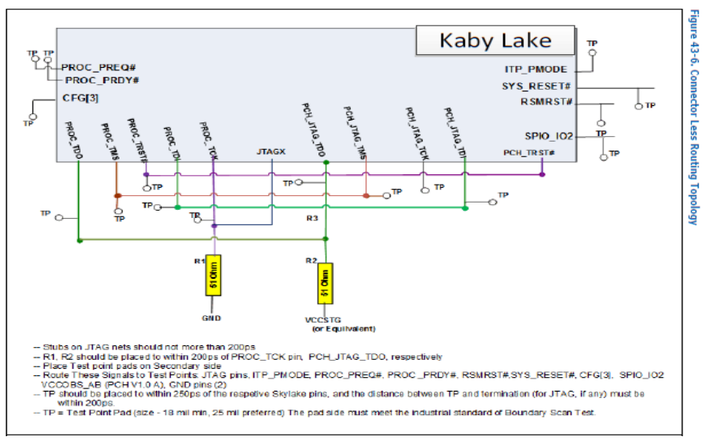
PCH_JTAG_TCK B56 PCH_JTAG_TCLK — 1 T0315
PCH_JTAG_TDI D59 XDP_TDI_CPU
PCH_JTAG_TDO A56 XDP_TDO_CPU
PCH_JTAG_TMS C59 XDP_TMS_CPU
PCH_TRST# C61 XDP_TRST_CPU_N
JTAGX A59 XDP_TCLK

+VCCIO
XDP_TDO_CPU R0323 2 1 51Ohm
XDP_TMS_CPU 1 T0319
XDP_TDI_CPU 1 T0318
XDP_TRST_CPU_N 1 T0317
XDP_TCLK R0324 2 1 51Ohm

30 THRO_CPU
R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result), 預留0ohm是調整空間

Q0301 2N7002
R0341 2 3 1 0Ohm
R0326 1 2 0Ohm H_PROCHOT#
C0301 0.1UF/16V
GND

88 PROCHOT#
SP0304 2 1 0Ohm @/SP
80 VR_HOT#
R0320 2 @ 1 0Ohm



– Stubs on JTAG nets should not more than 200ps
– R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
– Place Test point pads on Secondary side
– Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2
VCCOBS_AB (PCH V1.0 A), GND pins (2)
– TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
– TP = Test Point Pad (size - 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

Figure 43-6. Connector Less Routing Topology

PEGATRON Title : CPU(1)_DDI_eDP
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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Astrea used Non-Interleave

+1.2V
+3VS
+3VSUS
+12V

+1.2V 7,16,17,18,57,83
+3VS 3,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+3VSUS 20,21,22,23,24,25,26,28,30,31,41,51,53,62,74,81,92
+12V 57,91

16 M_A_D[63:0]
M_A_DQS#[7:0] 16
M_A_DQS[7:0] 16

17 M_B_D[63:0]
M_B_DQS#[7:0] 17
M_B_DQS[7:0] 17

U0301B

IL Channel A[0..63]
NIL Channel A[0..15]
NIL Channel A[32..47]
NIL Channel B[0..15]
NIL Channel B[32..47]

M_A_D0	AL71	DDR0_DQ[0]	DDR1_DQ[32]	AU53	DDR0_CKN[0]
M_A_D1	AL68	DDR0_DQ[1]	DDR1_DQ[33]	AT53	DDR0_CKP[0]
M_A_D2	AN68	DDR0_DQ[2]	DDR1_DQ[34]	AU55	DDR0_CKN[1]
M_A_D3	AN69	DDR0_DQ[3]	DDR1_DQ[35]	AT55	DDR0_CKP[1]
M_A_D4	AL70	DDR0_DQ[4]	DDR1_DQ[36]		
M_A_D5	AL69	DDR0_DQ[5]	DDR1_DQ[37]	BA56	DDR0_CKE[0]
M_A_D6	AN70	DDR0_DQ[6]	DDR1_DQ[38]	BB56	DDR0_CKE[1]
M_A_D7	AN71	DDR0_DQ[7]	DDR1_DQ[39]	AW56	DDR0_CKE[2]
M_A_D8	AR70	DDR0_DQ[8]	DDR1_DQ[40]	AY56	DDR0_CKE[3]
M_A_D9	AR68	DDR0_DQ[9]	DDR1_DQ[41]		
M_A_D10	AU71	DDR0_DQ[10]	DDR1_DQ[42]	AU45	DDR0_CS#[0]
M_A_D11	AU68	DDR0_DQ[11]	DDR1_DQ[43]	AU43	DDR0_CS#[1]
M_A_D12	AR71	DDR0_DQ[12]	DDR1_DQ[44]	AT45	DDR0_ODT[0]
M_A_D13	AR69	DDR0_DQ[13]	DDR1_DQ[45]	AT43	DDR0_ODT[1]
M_A_D14	AU70	DDR0_DQ[14]	DDR1_DQ[46]		
M_A_D15	AU69	DDR0_DQ[15]	DDR1_DQ[47]		
M_A_D32	BB65	DDR0_DQ[16]	DDR0_DQ[32]	BA51	M_A_CAA0
M_A_D33	AW65	DDR0_DQ[17]	DDR0_DQ[33]	BB54	M_A_CAA1
M_A_D34	AW63	DDR0_DQ[18]	DDR0_DQ[34]	BA52	M_A_CAA2
M_A_D35	AY63	DDR0_DQ[19]	DDR0_DQ[35]	AY52	M_A_CAA3
M_A_D36	BA65	DDR0_DQ[20]	DDR0_DQ[36]	AW52	M_A_CAA4
M_A_D37	AY65	DDR0_DQ[21]	DDR0_DQ[37]	AY55	M_A_CAA5
M_A_D38	BA63	DDR0_DQ[22]	DDR0_DQ[38]	AW54	M_A_CAA6
M_A_D39	BB63	DDR0_DQ[23]	DDR0_DQ[39]	BA54	M_A_CAA7
M_A_D40	BA61	DDR0_DQ[24]	DDR0_DQ[40]	BA55	M_A_CAA8
M_A_D41	AW61	DDR0_DQ[25]	DDR0_DQ[41]	AY54	M_A_CAA9
M_A_D42	BB59	DDR0_DQ[26]	DDR0_DQ[42]		
M_A_D43	AW59	DDR0_DQ[27]	DDR0_DQ[43]	AU46	M_A_CAB0
M_A_D44	BB61	DDR0_DQ[28]	DDR0_DQ[44]	AU48	M_A_CAB1
M_A_D45	AY61	DDR0_DQ[29]	DDR0_DQ[45]	AT46	M_A_CAB2
M_A_D46	BA59	DDR0_DQ[30]	DDR0_DQ[46]	AU50	M_A_CAB3
M_A_D47	AY59	DDR0_DQ[31]	DDR0_DQ[47]	AU52	M_A_CAB4
M_B_D0	AY39	DDR1_DQ[0]	DDR1_DQ[32]	AY51	M_A_CAB5
M_B_D1	AW39	DDR1_DQ[1]	DDR1_DQ[33]	AT48	M_A_CAB6
M_B_D2	AY37	DDR1_DQ[2]	DDR1_DQ[34]	AT50	M_A_CAB7
M_B_D3	AW37	DDR1_DQ[3]	DDR1_DQ[35]	BB50	M_A_CAB8
M_B_D4	BB39	DDR1_DQ[4]	DDR1_DQ[36]	AY50	M_A_CAB9
M_B_D5	BA39	DDR1_DQ[5]	DDR1_DQ[37]	BA50	
M_B_D6	BA37	DDR1_DQ[6]	DDR1_DQ[38]	BB52	
M_B_D7	BB37	DDR1_DQ[7]	DDR1_DQ[39]		
M_B_D8	AY35	DDR1_DQ[8]	DDR1_DQ[40]	AM70	M_A_DQS#0
M_B_D9	AW35	DDR1_DQ[9]	DDR1_DQ[41]	AM69	M_A_DQS0
M_B_D10	AY33	DDR1_DQ[10]	DDR1_DQ[42]	AT69	M_A_DQS#1
M_B_D11	AW33	DDR1_DQ[11]	DDR1_DQ[43]	AT70	M_A_DQS1
M_B_D12	BB35	DDR1_DQ[12]	DDR1_DQ[44]	BA64	M_A_DQS#4
M_B_D13	BA35	DDR1_DQ[13]	DDR1_DQ[45]	AY64	M_A_DQS4
M_B_D14	BA33	DDR1_DQ[14]	DDR1_DQ[46]	AY60	M_A_DQS#5
M_B_D15	BB33	DDR1_DQ[15]	DDR1_DQ[47]	BA60	M_A_DQS5
M_B_D32	AY31	DDR1_DQ[32]	DDR0_DQ[48]	BB38	M_B_DQS#0
M_B_D33	AW31	DDR1_DQ[33]	DDR0_DQ[49]	AY38	M_B_DQS0
M_B_D34	AY29	DDR1_DQ[34]	DDR0_DQ[50]	AY34	M_B_DQS#1
M_B_D35	AW29	DDR1_DQ[35]	DDR0_DQ[51]	BA34	M_B_DQS1
M_B_D36	BB31	DDR1_DQ[36]	DDR0_DQ[52]	BA30	M_B_DQS#4
M_B_D37	BA31	DDR1_DQ[37]	DDR0_DQ[53]	AY30	M_B_DQS4
M_B_D38	BA29	DDR1_DQ[38]	DDR0_DQ[54]	AY26	M_B_DQS#5
M_B_D39	BB29	DDR1_DQ[39]	DDR0_DQ[55]	BA26	M_B_DQS5
M_B_D40	AY27	DDR1_DQ[40]	DDR0_DQ[56]		
M_B_D41	AW27	DDR1_DQ[41]	DDR0_DQ[57]	AW50	DDR0_ALERT#
M_B_D42	AY25	DDR1_DQ[42]	DDR0_DQ[58]	AT52	DDR0_PAR
M_B_D43	AW25	DDR1_DQ[43]	DDR0_DQ[59]		
M_B_D44	BB27	DDR1_DQ[44]	DDR0_DQ[60]	AY67	DDR_VREF_CA
M_B_D45	BA27	DDR1_DQ[45]	DDR0_DQ[61]	AY68	DDR0_VREF_DQ
M_B_D46	BA25	DDR1_DQ[46]	DDR0_DQ[62]	BA67	DDR1_VREF_DQ
M_B_D47	BB25	DDR1_DQ[47]	DDR0_DQ[63]		DDR_VTT_CNTL
				AW67	DDR_PG_CTRL_S

M_A_DIM0_CLK#0 16
M_A_DIM0_CLK0 16
M_A_DIM0_CLK#1 16
M_A_DIM0_CLK1 16
M_A_DIM0_CKE0 16
M_A_DIM0_CKE1 16
M_A_DIM0_CKE2 16
M_A_DIM0_CKE3 16
M_A_DIM0_CS#0 16
M_A_DIM0_CS#1 16
M_A_DIM0_ODT0 16
M_A_CAA[9:0] 16
M_A_CAB[9:0] 16
DIMM_VREF_CA 18
DIMM0_VREF_DQ 18
DIMM1_VREF_DQ 18

DDR0_DQSN[0] DDR0_DQSP[0] DDR0_DQSN[1] DDR0_DQSP[1] DDR0_DQSN[2] DDR0_DQSP[2] DDR0_DQSN[3] DDR0_DQSP[3] DDR0_DQSN[4] DDR0_DQSP[4] DDR0_DQSN[5] DDR0_DQSP[5] DDR0_DQSN[6] DDR0_DQSP[6] DDR0_DQSN[7] DDR0_DQSP[7]

IL Channel A DQS[0..7]
NIL Channel A DQS[0,1,4,5]
NIL Channel B DQS[0,1,4,5]
DDR CH - A

RVP LPDDR3 floating. DDR3L GND PDG short to GND.

947859

U0301C

SKL_ULT

IL Channel B[0..63]
NIL Channel A[16..31]
NIL Channel A[48..63]
NIL Channel B[16..31]
NIL Channel B[48..63]

M_A_D16	AF65	DDR1_DQ[0]	DDR0_DQ[16]	AN45	DDR1_CKN[0]
M_A_D17	AF64	DDR1_DQ[1]	DDR0_DQ[17]	AN46	DDR1_CKN[1]
M_A_D18	AK65	DDR1_DQ[2]	DDR0_DQ[18]	AP45	DDR1_CKP[0]
M_A_D19	AK64	DDR1_DQ[3]	DDR0_DQ[19]	AP46	DDR1_CKP[1]
M_A_D20	AF66	DDR1_DQ[4]	DDR0_DQ[20]		
M_A_D21	AF67	DDR1_DQ[5]	DDR0_DQ[21]	AN56	DDR1_CKE[0]
M_A_D22	AK67	DDR1_DQ[6]	DDR0_DQ[22]	AP55	DDR1_CKE[1]
M_A_D23	AK66	DDR1_DQ[7]	DDR0_DQ[23]	AN55	DDR1_CKE[2]
M_A_D24	AF70	DDR1_DQ[8]	DDR0_DQ[24]	AP53	DDR1_CKE[3]
M_A_D25	AF68	DDR1_DQ[9]	DDR0_DQ[25]		
M_A_D26	AH71	DDR1_DQ[10]	DDR0_DQ[26]	BB42	DDR1_CS#[0]
M_A_D27	AH68	DDR1_DQ[11]	DDR0_DQ[27]	AY42	DDR1_CS#[1]
M_A_D28	AF71	DDR1_DQ[12]	DDR0_DQ[28]	BA42	DDR1_ODT[0]
M_A_D29	AF69	DDR1_DQ[13]	DDR0_DQ[29]	AW42	DDR1_ODT[1]
M_A_D30	AH70	DDR1_DQ[14]	DDR0_DQ[30]		
M_A_D31	AH69	DDR1_DQ[15]	DDR0_DQ[31]	AY48	DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
M_A_D48	AT66	DDR1_DQ[16]	DDR0_DQ[48]	AP50	DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
M_A_D49	AU66	DDR1_DQ[17]	DDR0_DQ[49]	BA48	DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
M_A_D50	AP65	DDR1_DQ[18]	DDR0_DQ[50]	BB48	DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
M_A_D51	AN65	DDR1_DQ[19]	DDR0_DQ[51]	AP48	DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
M_A_D52	AN66	DDR1_DQ[20]	DDR0_DQ[52]	AP52	DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]
M_A_D53	AP66	DDR1_DQ[21]	DDR0_DQ[53]	AN50	DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
M_A_D54	AT65	DDR1_DQ[22]	DDR0_DQ[54]	AN48	DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
M_A_D55	AU65	DDR1_DQ[23]	DDR0_DQ[55]	AN53	DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#
M_A_D56	AT61	DDR1_DQ[24]	DDR0_DQ[56]	AN52	DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]
M_A_D57	AU61	DDR1_DQ[25]	DDR0_DQ[57]		
M_A_D58	AP60	DDR1_DQ[26]	DDR0_DQ[58]	BA43	DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
M_A_D59	AN60	DDR1_DQ[27]	DDR0_DQ[59]	AY43	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]
M_A_D60	AN61	DDR1_DQ[28]	DDR0_DQ[60]	AY44	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
M_A_D61	AP61	DDR1_DQ[29]	DDR0_DQ[61]	AW44	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
M_A_D62	AT60	DDR1_DQ[30]	DDR0_DQ[62]	BB44	DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
M_A_D63	AU60	DDR1_DQ[31]	DDR0_DQ[63]	AY47	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
M_B_D16	AU40	DDR1_DQ[32]	DDR1_DQ[16]	BA44	DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
M_B_D17	AT40	DDR1_DQ[33]	DDR1_DQ[17]	AW46	DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
M_B_D18	AT37	DDR1_DQ[34]	DDR1_DQ[18]	AY46	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
M_B_D19	AU37	DDR1_DQ[35]	DDR1_DQ[19]	BA46	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
M_B_D20	AR40	DDR1_DQ[36]	DDR1_DQ[20]	BB46	DDR1_MA[3]
M_B_D21	AP40	DDR1_DQ[37]	DDR1_DQ[21]	BB47	DDR1_MA[4]
M_B_D22	AP37	DDR1_DQ[38]	DDR1_DQ[22]		
M_B_D23	AR37	DDR1_DQ[39]	DDR1_DQ[23]	AH66	DDR1_DQSN[0]/DDR0_DQSN[2]
M_B_D24	AT33	DDR1_DQ[40]	DDR1_DQ[24]	AH65	DDR1_DQSP[0]/DDR0_DQSP[2]
M_B_D25	AU33	DDR1_DQ[41]	DDR1_DQ[25]	AG69	DDR1_DQSN[1]/DDR0_DQSN[3]
M_B_D26	AU30	DDR1_DQ[42]	DDR1_DQ[26]	AG70	DDR1_DQSP[1]/DDR0_DQSP[3]
M_B_D27	AT30	DDR1_DQ[43]	DDR1_DQ[27]	AR66	DDR1_DQSN[2]/DDR0_DQSN[6]
M_B_D28	AR33	DDR1_DQ[44]	DDR1_DQ[28]	AR65	DDR1_DQSP[2]/DDR0_DQSP[6]
M_B_D29	AP33	DDR1_DQ[45]	DDR1_DQ[29]	AR61	DDR1_DQSN[3]/DDR0_DQSN[7]
M_B_D30	AR30	DDR1_DQ[46]	DDR1_DQ[30]	AR60	DDR1_DQSP[3]/DDR0_DQSP[7]
M_B_D31	AP30	DDR1_DQ[47]	DDR1_DQ[31]	AT38	DDR1_DQSN[4]/DDR1_DQSN[2]
M_B_D48	AU27	DDR1_DQ[48]		AR38	DDR1_DQSP[4]/DDR1_DQSP[2]
M_B_D49	AT27	DDR1_DQ[49]		AT32	DDR1_DQSN[5]/DDR1_DQSN[3]
M_B_D50	AT25	DDR1_DQ[50]		AR32	DDR1_DQSP[5]/DDR1_DQSP[3]
M_B_D51	AU25	DDR1_DQ[51]		AR25	DDR1_DQSN[6]
M_B_D52	AP27	DDR1_DQ[52]		AR27	DDR1_DQSP[6]
M_B_D53	AN27	DDR1_DQ[53]		AR22	DDR1_DQSN[7]
M_B_D54	AN25	DDR1_DQ[54]		AR21	DDR1_DQSP[7]
M_B_D55	AP25	DDR1_DQ[55]			
M_B_D56	AT22	DDR1_DQ[56]		AN43	DDR1_ALERT#
M_B_D57	AU22	DDR1_DQ[57]		AP43	DDR1_PAR
M_B_D58	AU21	DDR1_DQ[58]		AT13	DRAM_RESET#
M_B_D59	AT21	DDR1_DQ[59]		AR18	SM_RCOMP_0 R0402 1 1% 2 200Ohm
M_B_D60	AN22	DDR1_DQ[60]		AT18	SM_RCOMP_1 R0403 1 1% 2 80.6Ohm
M_B_D61	AP22	DDR1_DQ[61]		AU18	SM_RCOMP_2 R0404 1 1% 2 162Ohm
M_B_D62	AP21	DDR1_DQ[62]			
M_B_D63	AN21	DDR1_DQ[63]			

M_B_DIM0_CLK#0 17
M_B_DIM0_CLK#1 17
M_B_DIM0_CLK0 17
M_B_DIM0_CLK1 17
M_B_DIM0_CKE0 17
M_B_DIM0_CKE1 17
M_B_DIM0_CKE2 17
M_B_DIM0_CKE3 17
M_B_DIM0_CS#0 17
M_B_DIM0_CS#1 17
M_B_DIM0_ODT0 17
M_B_CAA[9:0] 17
M_B_CAB[9:0] 17

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]

NIL Channel B[16..31]
NIL Channel B[48..63]
IL Channel B DQS[0..7]
NIL Channel A DQS[2,3,6,7]
NIL Channel B DQS[2,3,6,7]
DDR CH - B

RVP LPDDR3 floating. DDR3L GND PDG short to GND.

Controls reset to the memory subsystems, and is used on DDR3L, DDR4 (not applicable to LPDDR3).

DRAM_RESET#1 T0401

DDR1_DQSN[0] DDR1_DQSP[0] DDR1_DQSN[1] DDR1_DQSP[1] DDR1_DQSN[2] DDR1_DQSP[2] DDR1_DQSN[3] DDR1_DQSP[3] DDR1_DQSN[4] DDR1_DQSP[4] DDR1_DQSN[5] DDR1_DQSP[5] DDR1_DQSN[6] DDR1_DQSP[6] DDR1_DQSN[7] DDR1_DQSP[7]

947859

Symbol U0301 B

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1		
BYTE 2		ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 3		
BYTE 4		ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 5		
BYTE 6		ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 7		

+1.2V
+3VS
+3VSUS

C0401 0.1UF/16V
R0405 1KOhm
R0407 220KOhm @
R0411 2MOHM @

U0401 74AUP1G07GW
NC A GND VCC Y

DDR_PG_CTRL 83
DDR_VTT_CNTL to VTT power ready < 35us (tCPU18)

+12V
R0431 100KOhm @
Q0405 2N7002 @
R0430 330Ohm @
Q0403 PMBS3904 @

For cost down!!
unmount:U0401, C0401
mount: R0430,Q0403,Q0405,R0431

Symbol U0301 C

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		
BYTE 2		ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 3		
BYTE 4		ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 5		
BYTE 6		ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 7		

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Title : CPU(2)_LPDDR3
BG1/HW7
Engineer: Kai_Shen
Size C | Project Name HE4EA | Rev 1.0
Date: Friday, April 07, 2017 Sheet 4 of 94

05

CPU(3)_+VCCCORE

+1.0V
+VCORE
+VCCIO

+1.0V 3,7,9,25,32,57,91
+VCORE 6,80
+VCCIO 3,7,9,57,91

+VCORE

C0509 1UF/6.3V @
C0510 1UF/6.3V @
C0514 1UF/6.3V @
C0515 1UF/6.3V @
C0518 1UF/6.3V @
C0519 1UF/6.3V @
C0520 1UF/6.3V @
C0516 1UF/6.3V @
C0517 1UF/6.3V @
C0532 1UF/6.3V @
C0533 1UF/6.3V @
C0534 1UF/6.3V @
C0531 1UF/6.3V @
C0535 1UF/6.3V @
C0536 1UF/6.3V @
C0539 1UF/6.3V @
C0540 1UF/6.3V @
C0537 1UF/6.3V @
C0538 1UF/6.3V @
C0542 1UF/6.3V @
C0543 1UF/6.3V @
C0545 47UF/6.3V @
C0546 47UF/6.3V @
C0548 47UF/6.3V @
C0549 47UF/6.3V @

+VCORE

U0301L

CPU POWER 1 OF 4

A30	VCC_1	VCC_19	G32
A34	VCC_2	VCC_20	G33
A39	VCC_3	VCC_21	G35
A44	VCC_4	VCC_22	G37
AK33	VCC_5	VCC_23	G38
AK35	VCC_6	VCC_24	G40
AK37	VCC_7	VCC_25	G42
AK38	VCC_8	VCC_26	J30
AK40	VCC_9	VCC_27	J33
AL33	VCC_10	VCC_28	J37
AL37	VCC_11	VCC_29	J40
AL40	VCC_12	VCC_30	K33
AM32	VCC_13	VCC_31	K35
AM33	VCC_14	VCC_32	K37
AM35	VCC_15	VCC_33	K38
AM37	VCC_16	VCC_34	K40
AM38	VCC_17	VCC_35	K42
G30	VCC_18	VCC_36	K43
K32	RSVD_3	VCC_SENSE	E32
AK32	RSVD_4	VSS_SENSE	E33
AB62	VCCOPC_1	VIDALERT#	B63
P62	VCCOPC_2	VIDSCK	A63
V62	VCCOPC_3	VIDSOUT	D64
H63	VCC_OPC_1P8_1	VCCSTG	G20
G61	VCC_OPC_1P8_2		
AC63	VCCOPC_SENSE		
AE63	VSSOPC_SENSE		
AE62	VCCEOPIO_1		
AG62	VCCEOPIO_2		
AL63	VCCEOPIO_SENSE		
AJ62	VSSEOPIO_SENSE		

947859
0101-03860PB

+VCORE

Pull H/L near CPU side

R0536 1 1% 2 100Ohm +VCORE
VCORE_VCCSENSE 80
VCORE_VSSSENSE 80
R0537 1 1% 2 100Ohm

VIDALERT# R0517 1 1% 2 220Ohm
VIDSCK R0518 1 1% 2 0Ohm
VIDSOUT R0519 1 1% 2 0Ohm

+VCCIO

CPU side | VR side

2016.03.18
R0524,R0522,R0525,R0523,R0526 and C0505 close to U8000

+1.0V
R0520 56Ohm 1%
VIDALERT#_R
VIDSCK_R

R0524 1 2 0Ohm VR_SVID_ALERT# 80

+1.0V
R0522 45.3Ohm 1%
C0505 0.1UF/16V

R0525 1 1% 2 51Ohm VR_SVID_CLK 80

+1.0V
R0521 100Ohm 1%
VIDSOUT_R

+1.0V
R0523 100Ohm 1%

R0526 1 1% 2 10Ohm VR_SVID_DATA 80

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BG1-HW3 RD

Title: CPU(3)_+VCCCORE
Engineer: Kai_Shen

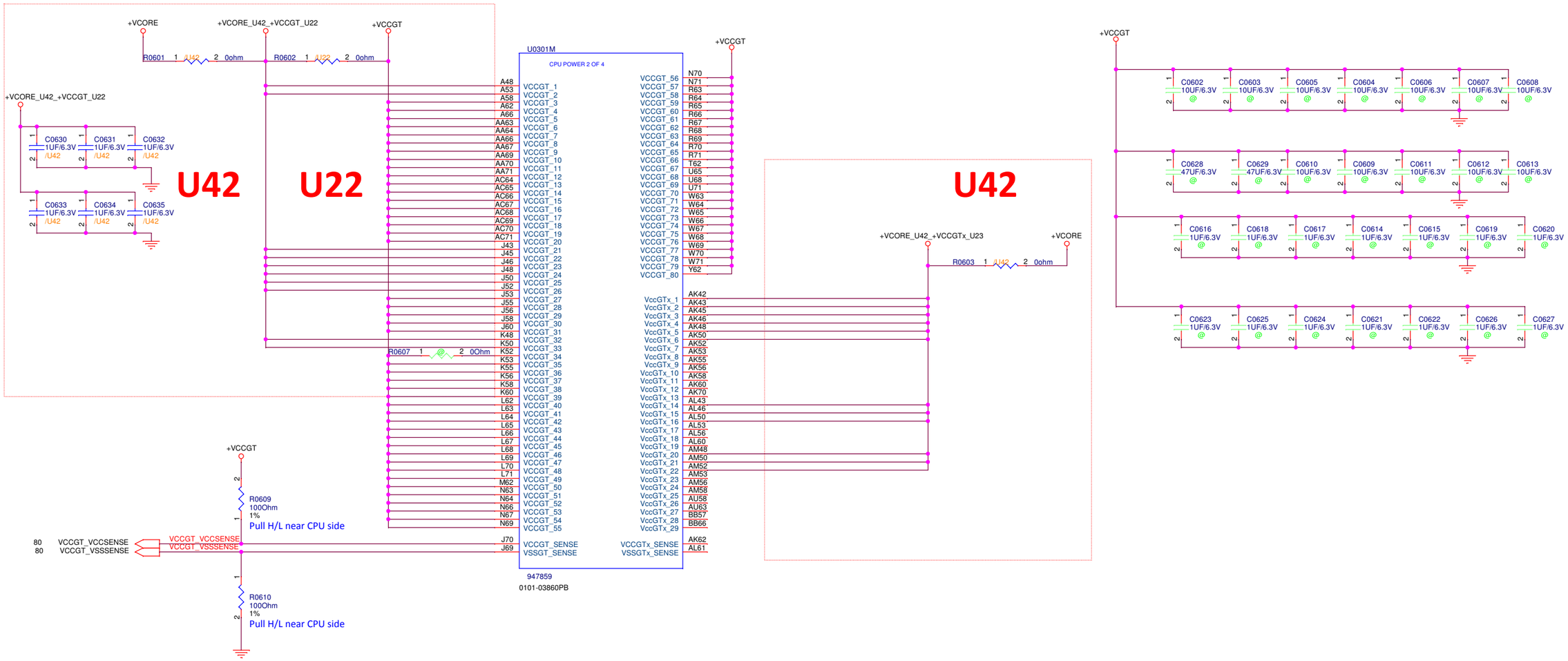
Size	Project Name	Rev
C	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 5 of 94

06 CPU(4)_+VCCGT

+VCORE
+VCCGT

+VCORE 5,80
+VCCGT 80



Ball #	Ball Names R-U42		Ball #	Ball Names U22		X[um]	Y[um]	R-U42/U22 common baord guidelines
C7	XTAL24_OUT		C7	NC		16791.178	-10013.696	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN		E3	NC		19013.678	-9039.86	connect to R-U42 XTAL24_IN
E35	NC		E35	XTAL24_OUT		280.416	-8591.296	connect to U22 XTAL24_OUT
E37	NC		E37	XTAL24_IN		-633.984	-8591.296	connect to U22 XTAL24_IN
AK42	VCCCORE		AK42	VccGTx		-3377.184	4009.136	
AK43	VCCCORE		AK43	VccGTx		-4291.584	4009.136	
AK45	VCCCORE		AK45	VccGTx		-5205.984	4009.136	
AK46	VCCCORE		AK46	VccGTx		-6120.384	4009.136	
AK48	VCCCORE		AK48	VccGTx		-7034.784	4009.136	
AK50	VCCCORE		AK50	VccGTx		-7949.184	4009.136	connect to VccGTx/VCCCORE
AL43	VCCCORE		AL43	VccGTx		-3834.384	4473.956	power plane island
AL46	VCCCORE		AL46	VccGTx		-5663.184	4473.956	
AL50	VCCCORE		AL50	VccGTx		-7491.984	4473.956	
AM48	VCCCORE		AM48	VccGTx		-7034.784	4946.396	
AM50	VCCCORE		AM50	VccGTx		-7949.184	4946.396	
AM52	VCCCORE		AM52	VccGTx		-8863.584	4946.396	
J43	VCCCORE		J43	VCCGT		-4748.784	-6826.504	
J45	VCCCORE		J45	VCCGT		-5663.184	-6826.504	
J46	VCCCORE		J46	VCCGT		-6577.584	-6826.504	
J48	VCCCORE		J48	VCCGT		-7491.984	-6826.504	
J50	VCCCORE		J50	VCCGT		-8406.384	-6826.504	connect to VccGT/VCCCORE
J52	VCCCORE		J52	VCCGT		-9320.784	-6826.504	power plane island
K48	VCCCORE		K48	VCCGT		-7034.784	-6361.684	
K50	VCCCORE		K50	VCCGT		-7949.184	-6361.684	
A48	VCCCORE		A48	VCCGT		-7313.422	-10989.056	
A53	VCCCORE		A53	VCCGT		-9791.446	-10989.056	
AK52	RSVD		AK52	VccGTx		-8863.584	4009.136	Not Connected
K52	RSVD		K52	VCCGT		-8863.584	-6361.684	Not Connected

PEGATRON Title : CPU(4)_+VCCGT
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD
Engineer: Kai_Shen
Size C | Project Name HE4EA | Rev 1.0
Date: Friday, April 07, 2017 Sheet 6 of 94

07

CPU(5)_+VDDQ/IO/SA

+1.0V
+1.2V
+VCCIO
+VCCSA

+1.0V 3,5,9,25,32,57,91
+1.2V 4,16,17,18,57,83
+VCCIO 3,5,9,57,91
+VCCSA 80

+1.2V
JP0701 @/SP
JP0702 @/SP
3MM_OPEN_5MIL
3MM_OPEN_5MIL

+VDDQ_CPU
C0701 10UF/6.3V
C0702 10UF/6.3V
C0703 10UF/6.3V
C0704 10UF/6.3V
C0705 10UF/6.3V
C0706 10UF/6.3V
C0707 1UF/6.3V
C0708 1UF/6.3V
C0709 1UF/6.3V
C0710 1UF/6.3V

C0701 - C0704 : Near by package
C0705 - C0710 : Underneath the package

2.8A

U0301N
CPU POWER 3 OF 4

AU23 VDDQ_1
AU28 VDDQ_2
AU35 VDDQ_3
AU42 VDDQ_4
BB23 VDDQ_5
BB32 VDDQ_6
BB41 VDDQ_7
BB47 VDDQ_8
BB51 VDDQ_9

+VDDQ_CPU
SP0701 1 2 0Ohm @/SP
+VDDQ_CPU_CLK
AM40 VDDQC
Decoupling cap for internal power

C0711 10UF/6.3V
1AV200000074
vx_c0402_h28_small

A18 VCCST
A22 VCCSTG
0.1A AL23 VCCPLL_OC
K20 VccPLL_1
K21 VccPLL_2

+VCCST_CPU
C0712 1UF/6.3V
+VCCSTG
C0713 1UF/6.3V
+VCCSFR_OC
C0714 1UF/6.3V
+VCCSFR
C0715 0.1UF/16V
C0716 0.1UF/16V

947859
0101-03860PB

AK28 VCCIO_1
AK30 VCCIO_2
AL30 VCCIO_3
AL42 VCCIO_4
AM28 VCCIO_5
AM30 VCCIO_6
AM42 VCCIO_7

+VCCIO
C0717 1UF/6.3V
C0718 1UF/6.3V
C0719 1UF/6.3V
C0720 1UF/6.3V

AK23 VCCSA_1
AK25 VCCSA_2
G23 VCCSA_3
G25 VCCSA_4
G27 VCCSA_5
G28 VCCSA_6
J22 VCCSA_7
J23 VCCSA_8
J27 VCCSA_9
K23 VCCSA_10
K25 VCCSA_11
K27 VCCSA_12
K28 VCCSA_13
K30 VCCSA_14

4.5A
+VCCSA

AM23 VCCIO_SENSE
AM22 VSSIO_SENSE
VCCIO_VR_FB
VSSIO_VR_FB

+VCCIO
R0714 1KOhm @
R0715 1KOhm @
Reserved PH/PD

H21 VSSSA_SENSE
H20 VCCSA_SENSE
VCCSA_VSSSENSE 80
VCCSA_VCCSENSE 80

+VCCSA
C0731 10UF/6.3V @
C0732 10UF/6.3V @
C0734 10UF/6.3V @
C0733 10UF/6.3V @
C0735 10UF/6.3V @
C0736 10UF/6.3V @
C0737 10UF/6.3V @
C0743 47UF/6.3V @
C0744 47UF/6.3V @
C0738 10UF/6.3V @
C0739 10UF/6.3V @
C0740 10UF/6.3V @
C0741 10UF/6.3V @
C0742 10UF/6.3V @

+VCCSA
R0720 100Ohm 1%
VCCSA_VCCSENSE
VCCSA_VSSSENSE
R0721 100Ohm 1%

+1.0V
+VCCST_CPU
0.24A R0710 1 2 0Ohm 0.24A
RES 0 OHM 1/10W (0603) JUMP

+1.0V
+VCCSFR
0.24A R0711 1 2 0Ohm 0.24A
RES 0 OHM 1/10W (0603) JUMP

+1.2V
+VCCSFR_OC
R0709 1 2 0Ohm
RES 0 OHM 1/10W (0603) JUMP
Refer to CRB 0.53

+VCCIO
+VCCSTG
0.12A R0713 1 2 0Ohm 0.12A
RES 0 OHM 1/10W (0603) JUMP

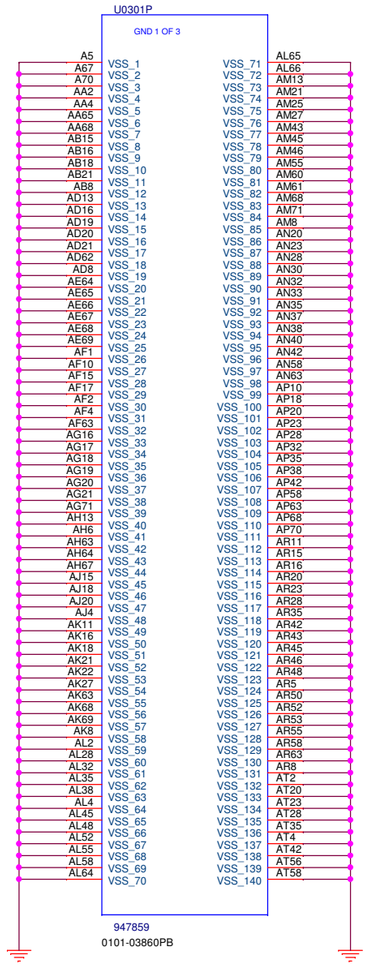
Title: CPU(5)_+VDDQ/IO/SA
BG1-HW3 RD
Engineer: Kai_Shen

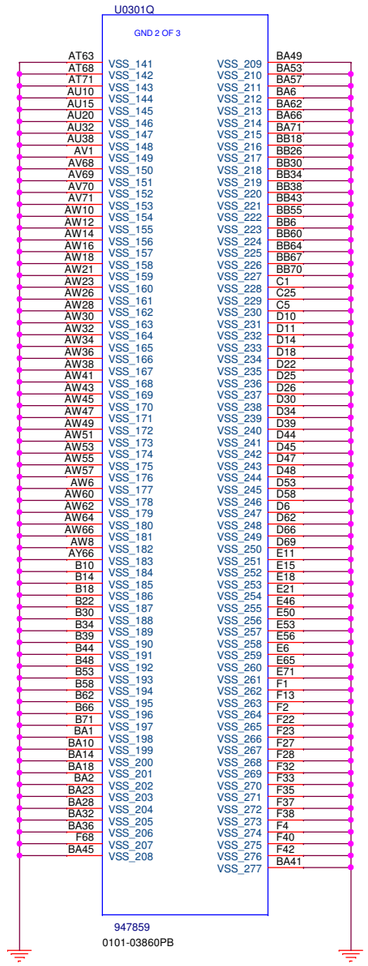
Size	Project Name	Rev
C	HE4EA	1.0

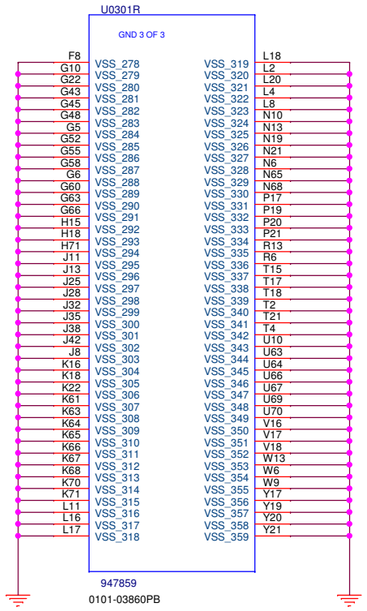
Date: Friday, April 07, 2017 Sheet 7 of 94

08

CPU(6)_CPU GND







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Title : CPU(6)_CPU GND

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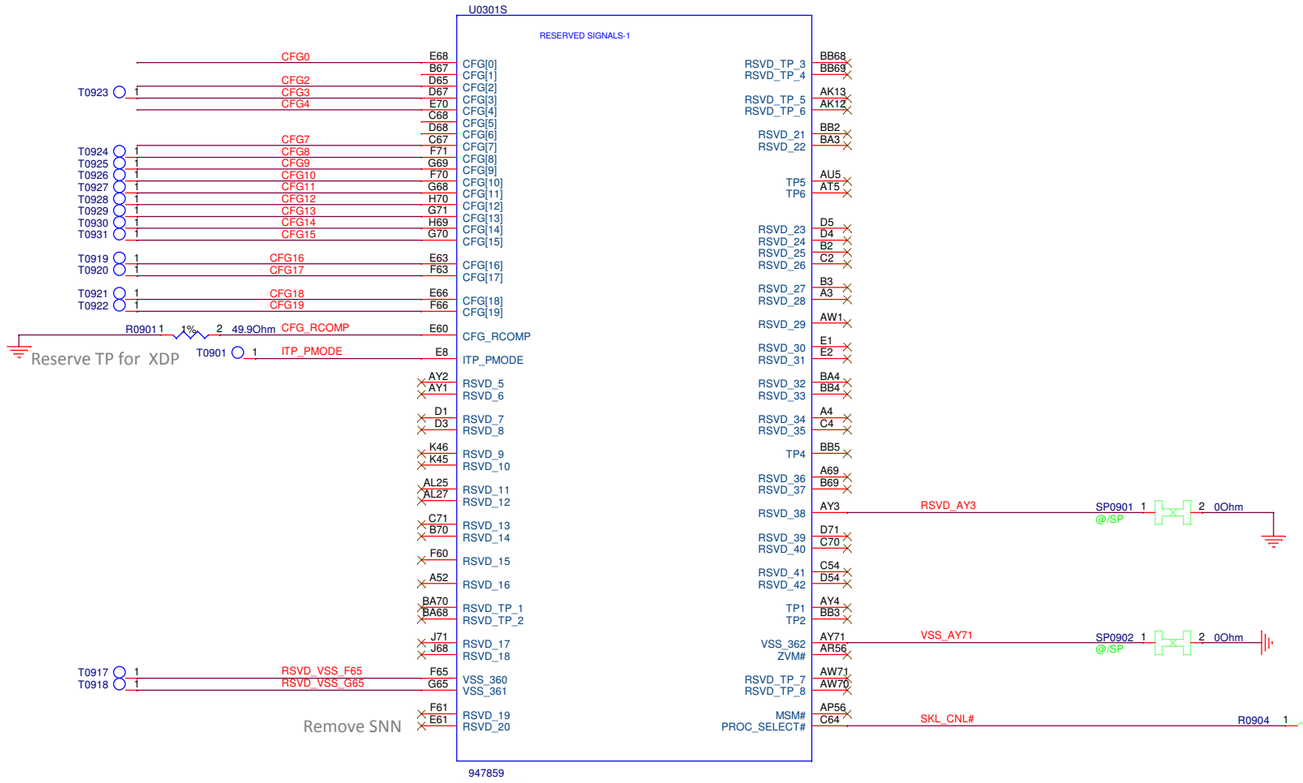
BG1-HW RD

Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Wednesday, March 29, 2017 Sheet 8 of 94

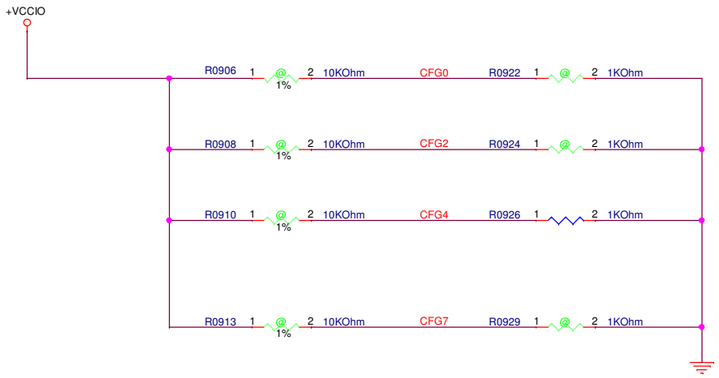
09 CPU(7)_CFG/RSVD



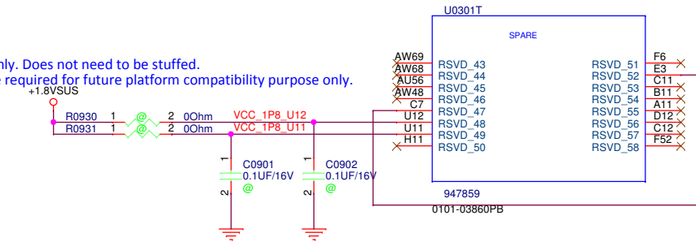
+1.0V, +1.8VSUS, +VCCIO

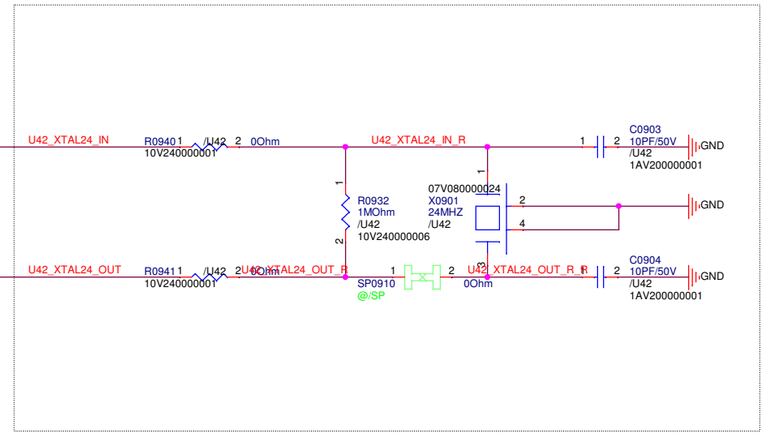
+1.0V	+1.0V	3,5,7,25,32,57,91
+1.8VSUS	+1.8VSUS	24,26,84
+VCCIO	+VCCIO	3,5,7,57,91

MOW WW48
1. Ball C64 which is PROC_SELECT# needs to be pulled to VCCST for Cannonlake support via 100K ohm resistor and with no resistor populated (floating pin) for Skylake.



PDG 1.2
Placeholder only. Does not need to be stuffed.
Placement are required for future platform compatibility purpose only.





Name	P5HCJ_KBL	Description
CFG0	1	1 = (Default) Normal Operation; No stall 0 = Stall
CFG1	1	Reserved configuration lane
CFG2	1	PCI Express* Static x16 Lane Numbering Reversal 1 = Normal operation 0 = Lane numbers reversed
CFG3	1	Reserved configuration lane
CFG4	0	CFG[4]: eDP* enable: 1 = Disabled. 0 = Enabled
CFG5 CFG6	1	CFG[6:5]: PCI Express* Bifurcation 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
CFG7	1	CFG[7]: PEG Training: 1 = (default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.
CFG[19:8]	1	Reserved configuration lane

The CFG signals have a default value of '1' if not terminated on the board.

*All processor lines.
CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them

From EDS_Intel_CPU(Kabylake.UY)_Vol1_559100_Rev0p91 Page.123

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BG1-HW RD

Title: CPU(7)_CFG/RSVD
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Wednesday, March 29, 2017 Sheet 9 of 94

PEGATRON

Title : Block Diagram

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BG1-HW RD

Engineer: Kai_Shen

Size	Project Name	Rev
A	HE4EA	1.0

Date: Wednesday, March 29, 2017 Sheet 10 of 94

Title	<Title>			
Size A	Document Number HE4EA			Rev 1.0
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Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 12 of 94

Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 13 of 94

Title	<Title>			
Size A	Document Number HE4EA			Rev 1.0
Date:	Wednesday, March 29, 2017	Sheet	14 of 94	

Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
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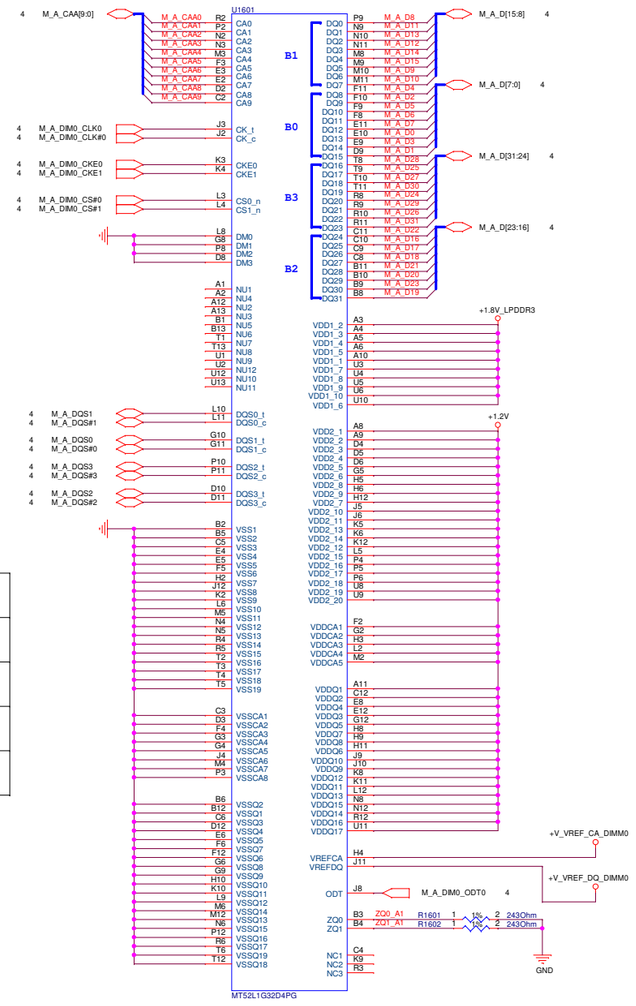
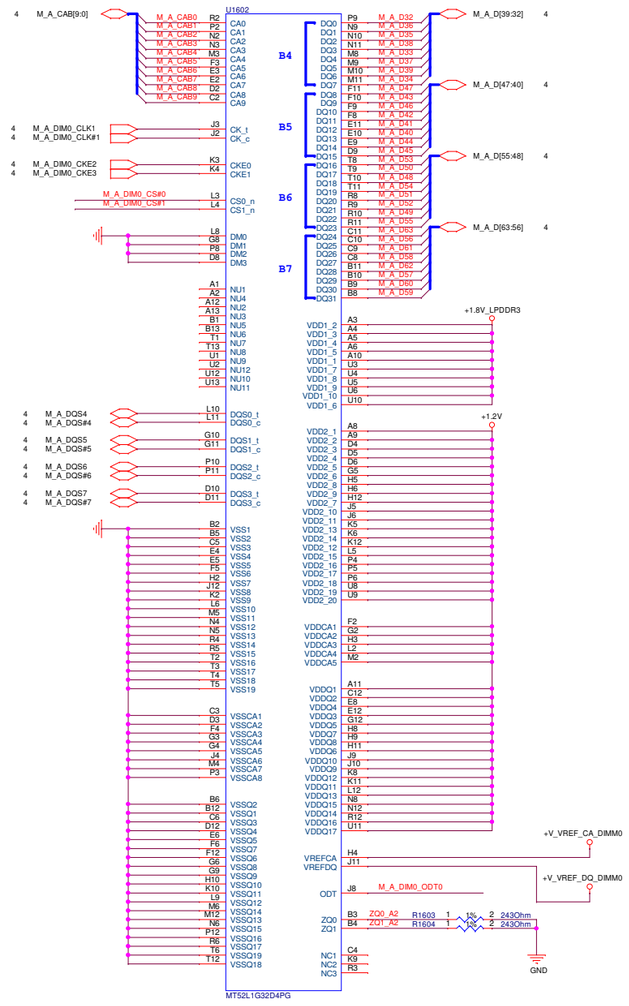
LPDDR3 SOURCE

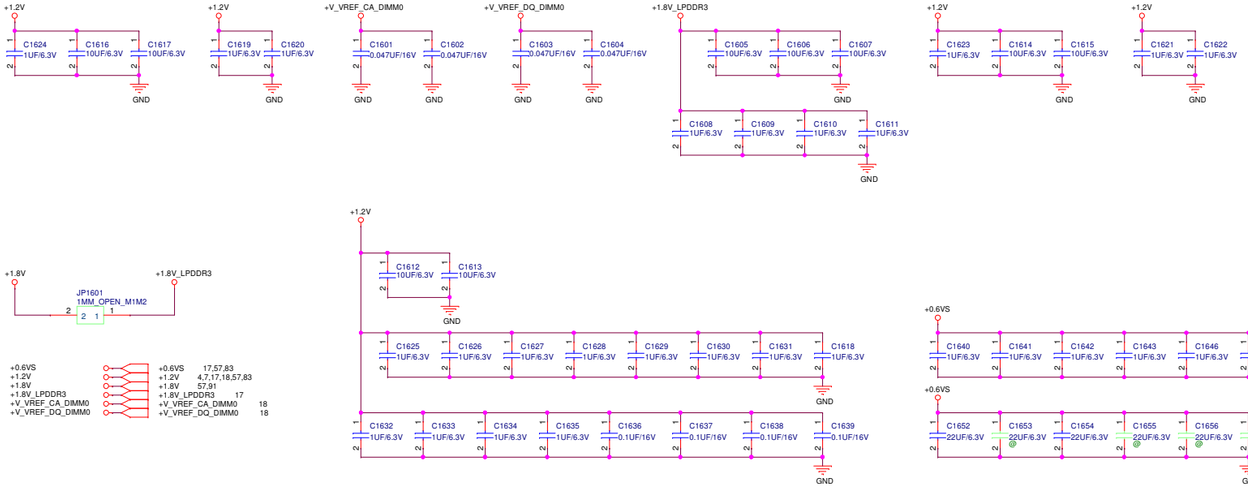
0315-01M9000	LPDDR3 8Gb	Samsung	K4E8E324EB-EGCF	11.0x11.5x0.90mm
0315-01MT000	LPDDR3 16Gb	Samsung	K4E6E304EB-EGCF	11.0x11.5x0.9mm
0315-01E10DE	LPDDR3 8Gb	SKHYNIX	H9CCNNN8GTMLAR-NUD	11.0x11.5x1.00mm
0315-01DP0DE	LPDDR3 16Gb	SKHYNIX	H9CCNNNBJTMLAR-NUD	11.0x11.5x1.00mm
0315-01GR000	LPDDR3 8Gb	SKHYNIX	H9CCNNN8JTBLAR-NUD	11.0x11.5x1.00mm

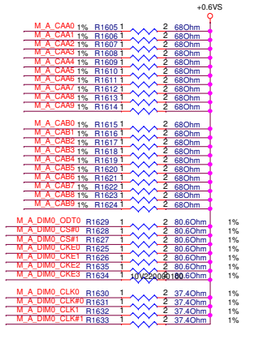
LPDDR3 Channel A



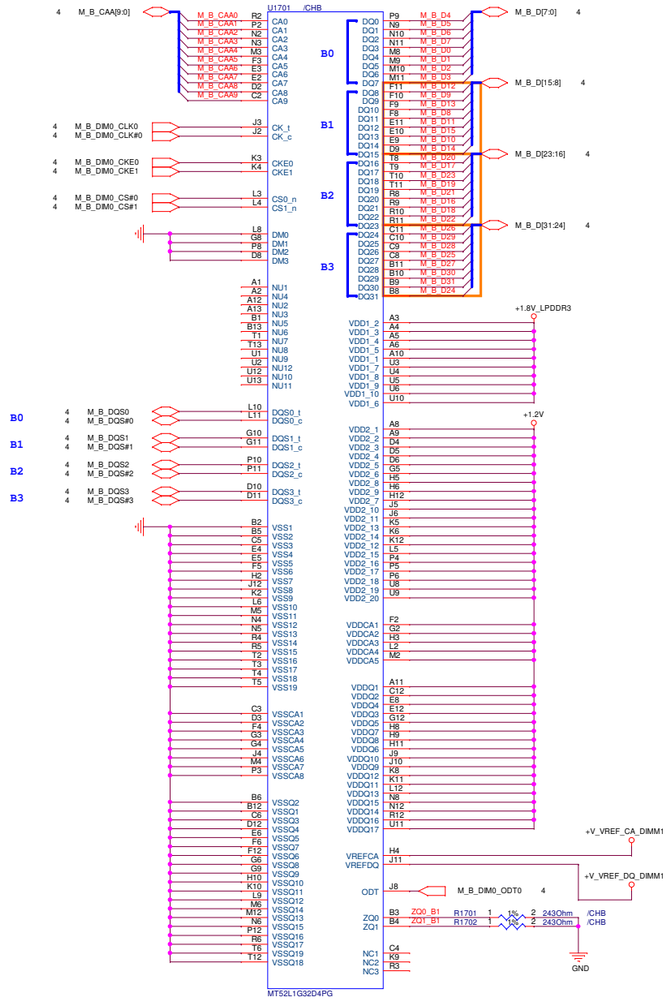


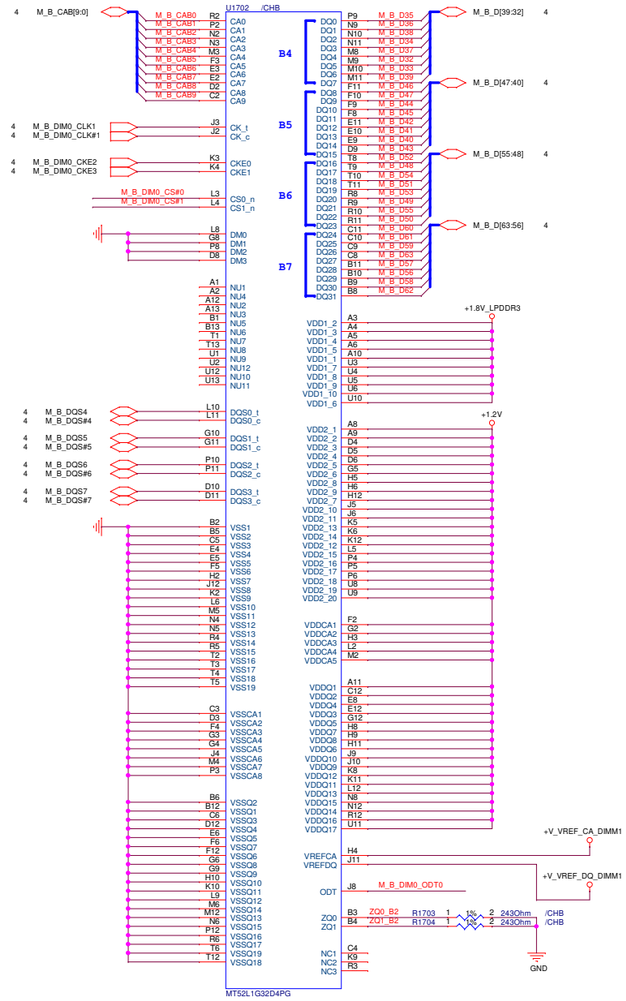
LPDDR3 1600 32Gb
MICRON/EDFB232A1MA-GD-F-D
12.5mm x 11.5mm



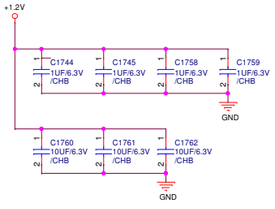


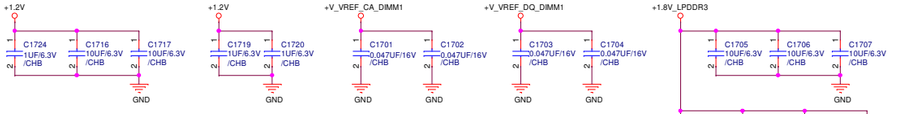
LPDDR3 Channel B

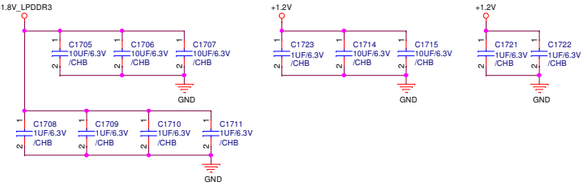


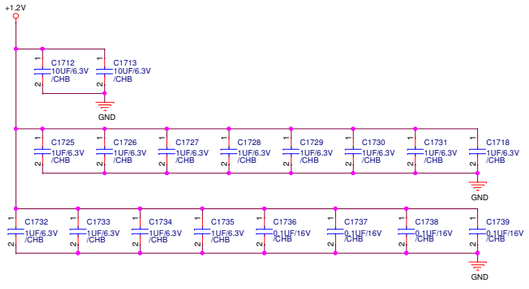


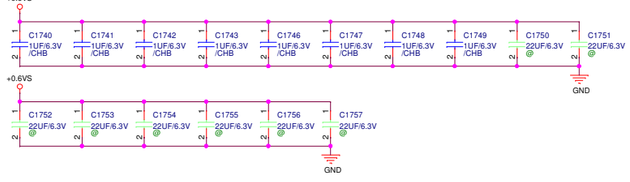
LPDDR3 1600 32Gb
MICRON/EDFB232A1MA-GD-F-D
12.5mm x 11.5mm

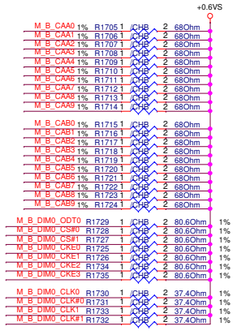












+0.6VS 16,57,83
+1.2V 4,7,16,18,57,83
+1.8V_LPDDR3 16
+V_VREF_CA_DIMM1 18
+V_VREF_DQ_DIMM1 18

<Variant Name>

PEGATRON Title : DDR3(2)_SO-DIMM1
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Kai_Shen
3G1AW7
Size: Custom | Project Name: HE4EA | Rev: 1.0
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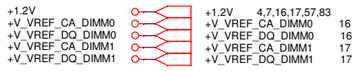
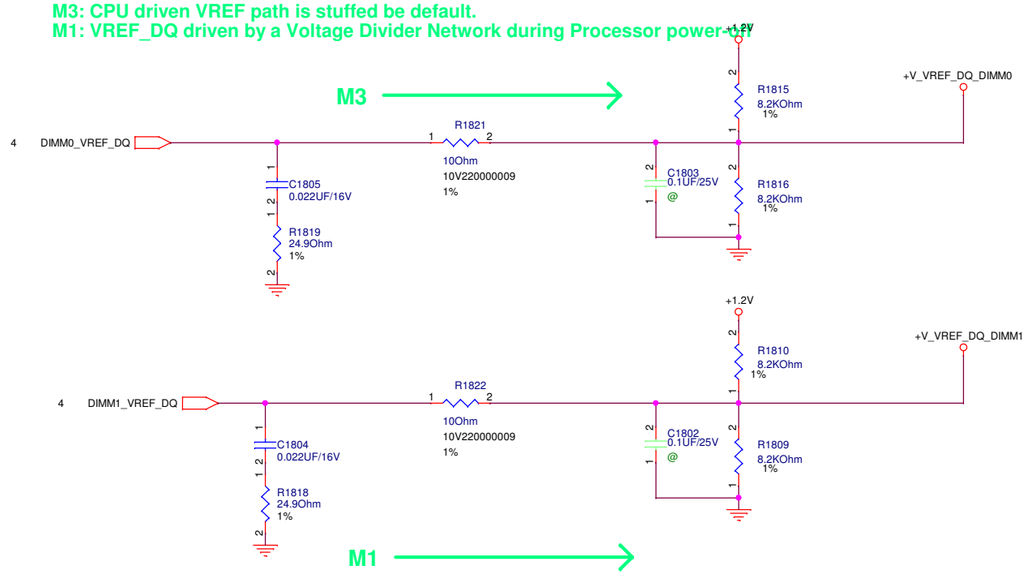
18 LPDDR3(3)_CA/DQ Voltage



M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



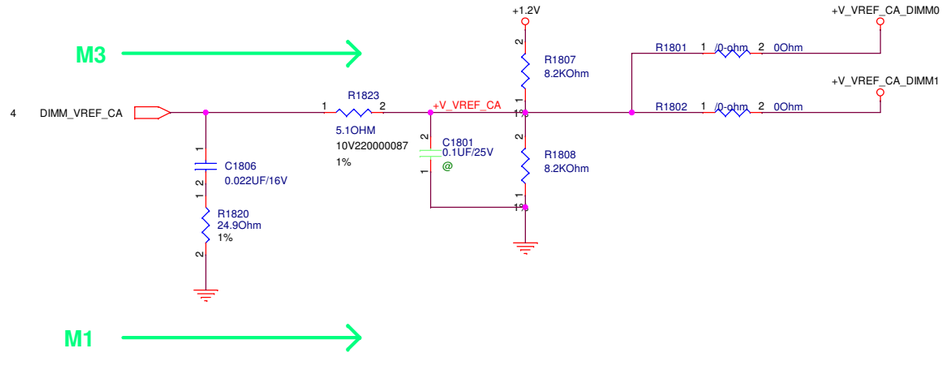
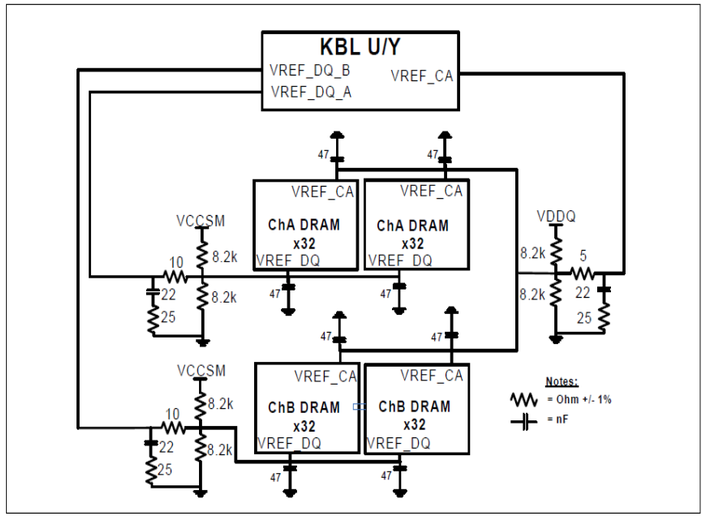


Figure 4-52. KBL U and KBL Y LPDDR3 x32 Memory Down V_{REF-DQ} and V_{REF-CA} Overview



561280_KBL UY PDG Rev1_0

47nF on Page 16&17

<Variant Name>

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Title: DDR3(3)_CA/DQ Voltage

Engineer: Kai_Shen

BG1/HW7

Size	Project Name	Rev
C	HE4EA	1.0

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Title	<Title>
Size: A	Document Number: HE4EA
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PCH(1)_SPI/LPC

+3VS
+3VSUS

+3VS 3,4,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+3VSUS 4,21,22,23,24,25,26,28,30,31,41,51,53,62,74,81,92

RF requirement

SPI_CLK — C2003 0.1UF/16V @ — near AV2

RF requirement

SML1_CLK — C2004 0.1UF/16V @ — near W3

U0301E

SPI - FLASH

28 SPI_CLK	SPI_CLK	AV2	SPI0_CLK
28 SPI_SO	SPI_SO	AW3	SPI0_MISO
28 SPI_SI	SPI_SI	AV3	SPI0_MOSI
28 SPI_WP#_IO2	SPI_WP#_IO2	AW2	SPI0_IO2
28 SPI_HOLD#_IO3	SPI_HOLD#_IO3	AU4	SPI0_IO3
28 SPI_CS#0	SPI_CS#0	AU3	SPI0_CS0#
T2011 1	SPI_CS1#	AU2	SPI0_CS1#
T2001 1	SPI_CS2#	AU1	SPI0_CS2#

SPI - TOUCH

T2002 1	GPP_D1	M2	GPP_D1/SPI1_CLK
		M3	GPP_D2/SPI1_MISO
		J4	GPP_D3/SPI1_MOSI
		V1	GPP_D21/SPI1_IO2
		V2	GPP_D22/SPI1_IO3
T2007 1	GPP_D0	M1	GPP_D0/SPI1_CS#

C LINK

53 CL_CLK	CL_CLK	G3	CL_CLK
53 CL_DATA	CL_DATA	G2	CL_DATA
53 CL_RST#	CL_RST#	G1	CL_RST#

30 RCIN#	RCIN#	AW13	GPP_A0/RCIN#
30,44,62 INT_SERIRQ	INT_SERIRQ	AY11	GPP_A6/SERIRQ

947859
0101-03860PB

SMBUS, SMLINK

GPP_C0/SMBCLK	R7	SMB_CLK	
GPP_C1/SMBDATA	R8	SMB_DAT	
GPP_C2/SMBALERT#	R10	SMBALERT#	1 T2008
GPP_C3/SML0CLK	R9	SML0_CLK_NFC	1 T2003
GPP_C4/SML0DATA	W2	SML0_DAT_NFC	1 T2004
GPP_C5/SML0ALERT#	W1	SML0ALERT#	
GPP_C6/SML1CLK	W3	SML1_CLK	SML1_CLK 28
GPP_C7/SML1DATA	V3	SML1_DAT	SML1_DAT 28 To EC
GPP_B23/SML1ALERT#/PCHHOT#	AM7	SML1ALERT#	1 T2010

LPC

GPP_A1/LAD0/ESPI_IO0	AY13	LPC_AD0	LPC_AD0 30,44,62
GPP_A2/LAD1/ESPI_IO1	BA13	LPC_AD1	LPC_AD1 30,44,62
GPP_A3/LAD2/ESPI_IO2	BB13	LPC_AD2	LPC_AD2 30,44,62
GPP_A4/LAD3/ESPI_IO3	AY12	LPC_AD3	LPC_AD3 30,44,62
GPP_A5/LFRAME#/ESPI_CS#	BA12	LPC_FRAME#	LPC_FRAME# 30,44,62
GPP_A14/SUS_STAT#/ESPI_RESET#	BA11	PM_SUS_STAT#	PM_SUS_STAT# 62

TPM
EC
DEBUG

GPP_A9/CLKOUT_LPC0/ESPI_CLK	AW9	CLK_KBCPCI_PCH_R	R20011 2 22Ohm 1% — CLK_KBCPCI_PCH 30
GPP_A10/CLKOUT_LPC1	AY9	CLK_LPC1	R20021 Debug 2 22Ohm 1% — CLK_DEBUG 44
GPP_A8/CLKRUN#	AW11		R20141 @ PM 2 22Ohm 1% — LPCCLK_TPM 62

C2001 10PF/50V @ — C2002 10PF/50V @

PM_CLKRUN# — PM_CLKRUN# 30,62

Unmount R2013,R2009
Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

+3VS
PM_CLKRUN# R2013 1 2 10KOhm
INT_SERIRQ R2009 1 2 10KOhm

+3VSUS
SMB_CLK RN2001A 1 2.2KOhm 2 @
SMB_DAT RN2001B 3 2.2KOhm 4 @
SML1_DAT RN2002B 3 2.2KOhm 4
SML1_CLK RN2002A 1 2.2KOhm 2
SML1ALERT# R2012 1 2 150KOhm

+3VSUS
R2004 1 @ 2 20KOhm SMBALERT# R2003 1 @ 2 2.2KOhm

SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable

CRB 0.53 reserve 150k ohm

+3VSUS
R2006 1 @ 2 20KOhm SML0ALERT# R2005 1 @ 2 4.7KOhm

SML0ALERT# - Internal weak pull down 20 kohm
0 : LPC EC (default)
1 : eSPI EC

CRB 0.53 reserve 150k ohm

+3VSUS
R2008 1 @ 2 20KOhm R2007 1 @ 2 4.7KOhm
BBS 21

BBS - Internal weak pull down 20k ohm
Boot BIOS Strap
0 : SPI destination (default)
1 : LPC destination

MOW WW52
To enable Direct Connect Interface (DCI),
a 150K pull up resistor will need to be added to PCHHOT#
pin. This pin must be low during the rising edge of RSMRST#.

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BG1-HW RD

Title : PCH(1)_SPI/LPC
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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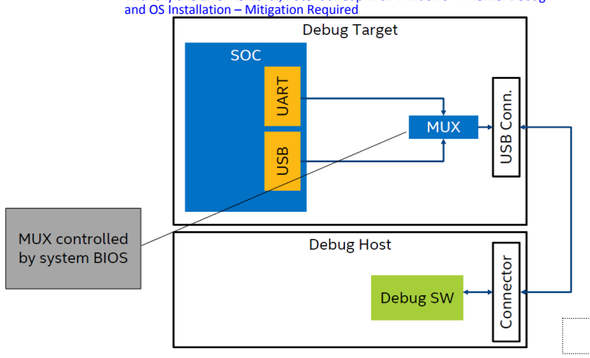
PCH(2)_ISH

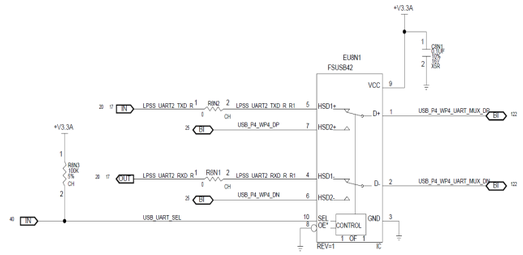
Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

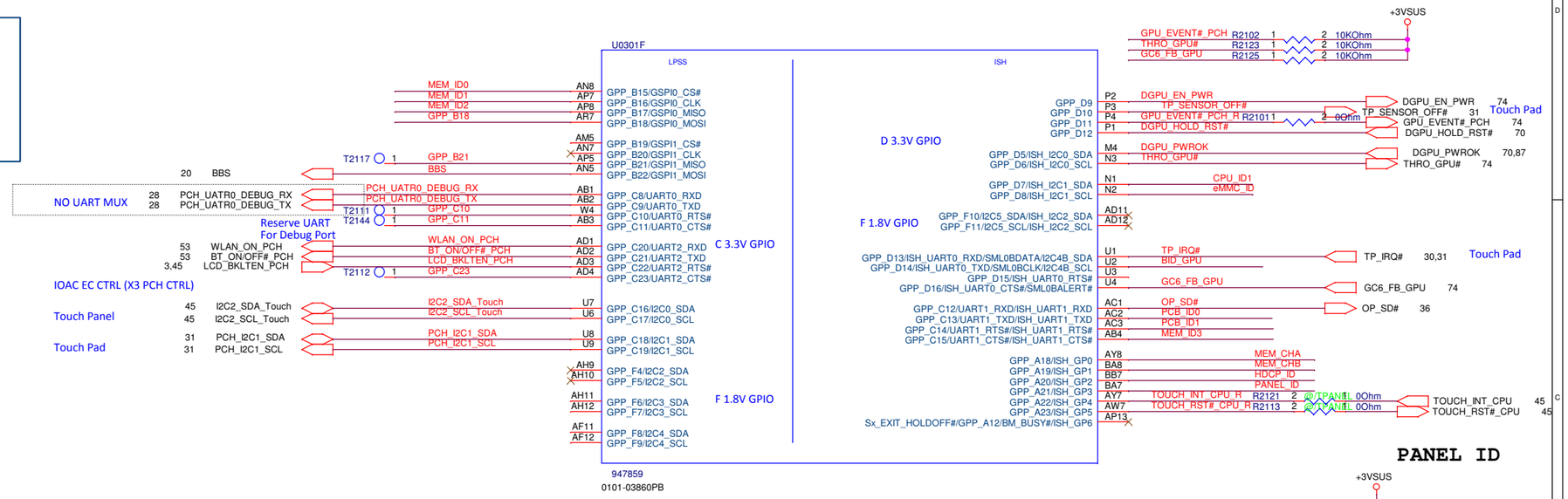
With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required

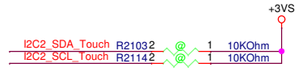


To implement UART for WIN7 WHCK requirement if need

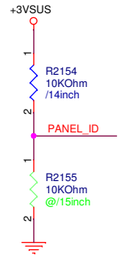
Please refer to Intel document #548689 - RVP5





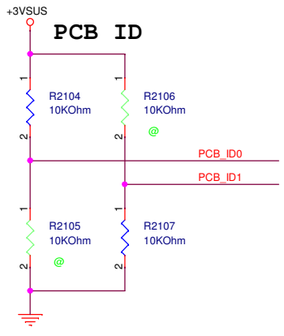


Function ID

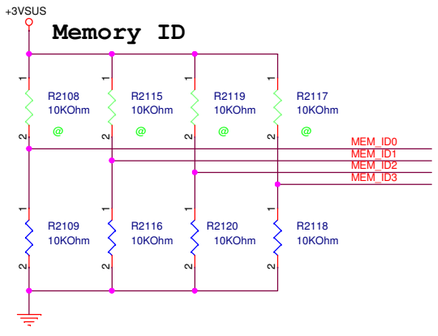


PANEL ID

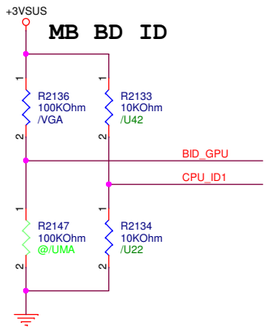
PCB ID



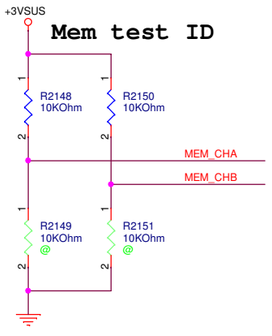
Memory ID



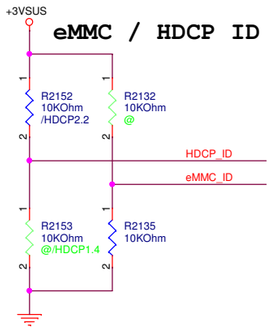
MB BD ID

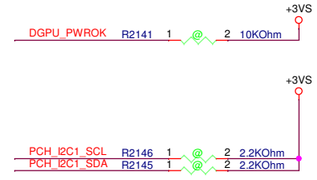


Mem test ID

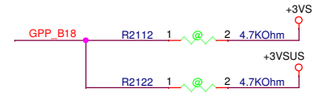


eMMC / HDCP ID





Change To 2.2Kohm PU side
Default PU +3V For S3 Resume by TP side



GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

Default is GPO, to reserve pull high to +3VSUS_ORG

	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R10	0	0
R11	0	1
R12	1	0
R20	1	1

		MEM_ID3 (GPP_C15)	MEM_ID2 (GPP_B17)	MEM_ID1 (GPP_B16)	MEM_ID0 (GPP_B15)
0	MICRON / 8Gb / 0315-01NJ0PB T52L256M32D1PF-107WT:B	0	0	0	0
1	MICRON / 16Gb / 0315-01N10PB MT52L512M32D2PF-107WT:B	0	0	0	1
2	MICRON / 32Gb / 0315-01N20PB MT52L1G32D4PG-107WT:B	0	0	1	0
3	KINGSTONE / 8Gb / 0315-025A0PB KB26AAEL3E08G	0	0	1	1
4	KINGSTONE / 16Gb / 0315-025E0PB KB26AAEL3E16G	0	1	0	0
5	SKHynix / 8Gb / 0315-01YQ0PB H9CCNNN8GTALAR-NUD	0	1	0	1
6	SKHynix / 16Gb / 0315-01Y00PB H9CCNNNBJTALAR-NUD	0	1	1	0
7		0	1	1	1

	BID_GPU
UMA	0
DIS	1

	CPU_ID1
U22	0
U42	1

	CHA	CHB
GPP_A18(0)	Disable	
GPP_A18(1)	Enable	
GPP_A19(0)		Disable
GPP_A19(1)		Enable

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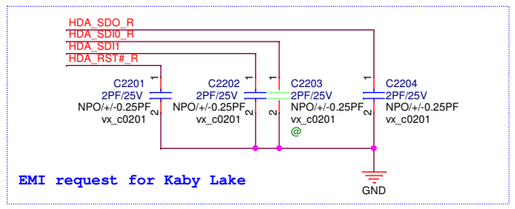
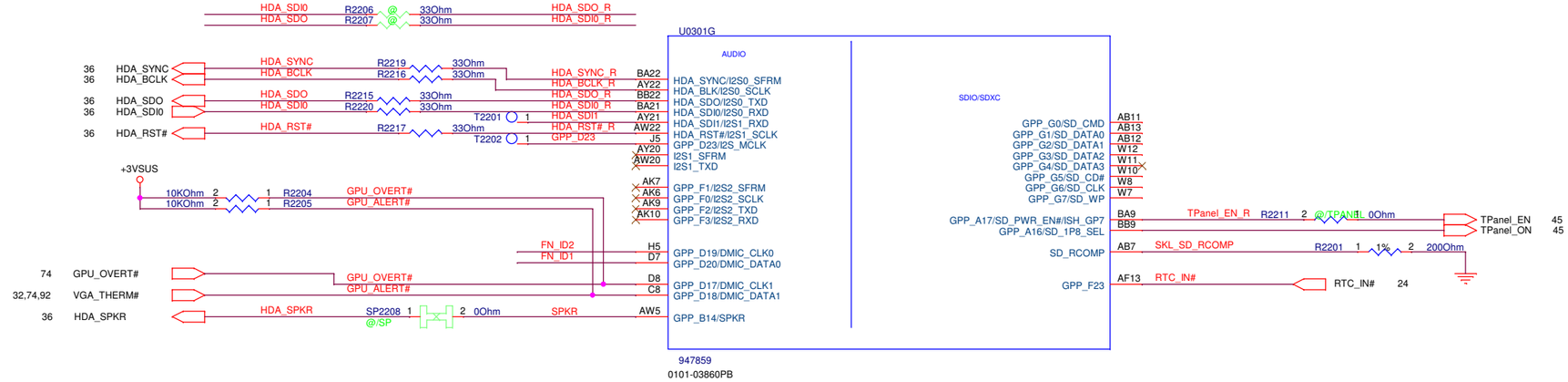
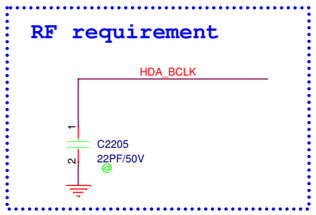
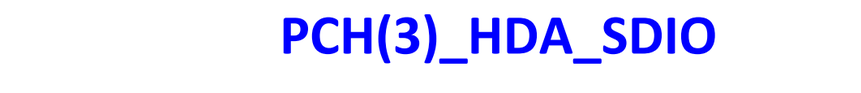
PCH(3)_HDA_SDIO



Recommended Routing : Stripline < 2"
Alternative Routing : Microstrip <1" (less noise-reduction)



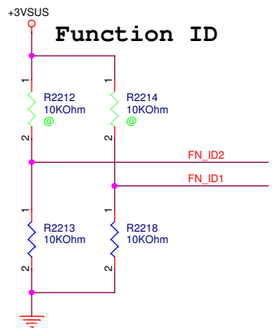




SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG

HDA_SDO - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRRIDE
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security



* The signal has a weak internal Pull-down.

Name	P5HCJ_KBL	Description
GPP_B14	0	0 = Disable “Top Swap” mode. (Default) 1 = Enable “Top Swap” mode.
GPP_B18	0	0 = Disable “No Reboot” mode. (Default) 1 = Enable “No Reboot” mode
GPP_B22	0	0 = SPI (Default) 1 = LPC
GPP_C5	0	0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.
HDA_SDO	0	0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override).
GPP_C2	0	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
GPP_E19	0	0 = Port B is not detected. (Default) 1 = Port B is detected.
GPP_E21	0	0 = Port C is not detected. (Default) 1 = Port C is detected.

From EDS_Intel_PCH(Skylake.UY_Kabylake.UY)_Vol1_545659_Rev2p0 Page.55-57

PEGATRON Title : PCH(3)_HDA/SDIO
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BG1-HW RD
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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PCH(4)_USB/PCIE/SATA

+3VS 3,4,20,21,22,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+3VSUS 4,20,21,22,24,25,26,28,30,31,41,51,53,62,74,81,92

U0301H

PCIE/USB3/SATA

PCIE x 4 -dGPU

70 PEX_TXX0* → PEX_TXX0* H13
70 PEX_TXX0 → PEX_TXX0 G13
70 PEX_RX0* → PEX_RX0* /NGAC2304 1 2 0.22UF/10V PEX_RX0*_C B17
70 PEX_RX0 → PEX_RX0 /NGAC2303 1 2 0.22UF/10V PEX_RX0_C A17
PCIE1_RXN/USB3_5_RXN
PCIE1_RXP/USB3_5_RXP
PCIE1_TXN/USB3_5_TXN
PCIE1_TXP/USB3_5_TXP

70 PEX_TXX1* → PEX_TXX1* G11
70 PEX_TXX1 → PEX_TXX1 F11
70 PEX_RX1* → PEX_RX1* /NGAC2310 1 2 0.22UF/10V PEX_RX1*_C D16
70 PEX_RX1 → PEX_RX1 /NGAC2309 1 2 0.22UF/10V PEX_RX1_C C16
PCIE2_RXN/USB3_6_RXN
PCIE2_RXP/USB3_6_RXP
PCIE2_TXN/USB3_6_TXN
PCIE2_TXP/USB3_6_TXP

70 PEX_TXX2* → PEX_TXX2* H16
70 PEX_TXX2 → PEX_TXX2 G16
70 PEX_RX2* → PEX_RX2* /NGAC2308 1 2 0.22UF/10V PEX_RX2*_C D17
70 PEX_RX2 → PEX_RX2 /NGAC2307 1 2 0.22UF/10V PEX_RX2_C C17
PCIE3_RXN
PCIE3_RXP
PCIE3_TXN
PCIE3_TXP

70 PEX_TXX3* → PEX_TXX3* G15
70 PEX_TXX3 → PEX_TXX3 F15
70 PEX_RX3* → PEX_RX3* /NGAC2306 1 2 0.22UF/10V PEX_RX3*_C B19
70 PEX_RX3 → PEX_RX3 /NGAC2305 1 2 0.22UF/10V PEX_RX3_C A19
PCIE4_RXN
PCIE4_RXP
PCIE4_TXN
PCIE4_TXP

M.2 SATA/PCIE x 4 -SSD

51 PCIE_RXN5 → PCIE_RXN5 F16
51 PCIE_RXP5 → PCIE_RXP5 E16
51 PCIE_TXN5 → PCIE_TXN5 C19
51 PCIE_TXP5 → PCIE_TXP5 D19
PCIE5_RXN
PCIE5_RXP
PCIE5_TXN
PCIE5_TXP

51 PCIE_RXN6 → PCIE_RXN6 G18
51 PCIE_RXP6 → PCIE_RXP6 F18
51 PCIE_TXN6 → PCIE_TXN6 D20
51 PCIE_TXP6 → PCIE_TXP6 C20
PCIE6_RXN
PCIE6_RXP
PCIE6_TXN
PCIE6_TXP

51 PCIE_RXN7 → PCIE_RXN7 F20
51 PCIE_RXP7 → PCIE_RXP7 E20
51 PCIE_TXN7 → PCIE_TXN7 B21
51 PCIE_TXP7 → PCIE_TXP7 A21
PCIE7_RXN/SATA0_RXN
PCIE7_RXP/SATA0_RXP
PCIE7_TXN/SATA0_TXN
PCIE7_TXP/SATA0_TXP

51 SATA_RXN8 → SATA_RXN8 G21
51 SATA_RXP8 → SATA_RXP8 F21
51 SATA_TXN8 → SATA_TXN8 D21
51 SATA_TXP8 → SATA_TXP8 C21
PCIE8_RXN/SATA1A_RXN
PCIE8_RXP/SATA1A_RXP
PCIE8_TXN/SATA1A_TXN
PCIE8_TXP/SATA1A_TXP

WLAN

53 PCIE_RXN_WLAN → E22
53 PCIE_RXP_WLAN → E23
53 PCIE_TXN_WLAN → 0.1UF/16V 1 2 C2322 PCIE_TXN_WLAN_C B23
53 PCIE_TXP_WLAN → 0.1UF/16V 1 2 C2323 PCIE_TXP_WLAN_C A23
PCIE9_RXN
PCIE9_RXP
PCIE9_TXN
PCIE9_TXP

F25
E25
D23
C23
PCIE10_RXN
PCIE10_RXP
PCIE10_TXN
PCIE10_TXP

PCIE_RCOMP PDG 0.9 need 100 ohm 0.1% / CRB 0.53 use 100 ohm +-1%

R2301 1 1% 2 100Ohm PCIE_RCOMPN F5
PCIE_RCOMPP E5
PCIE_RCOMPN
PCIE_RCOMPP

Reserve TP for XDP

T2323 1 PROC_PRDY# D56
T2324 1 PROV_PREQ# D61
PIRQA# BB11
PROC_PRDY#
PROC_PREQ#
GPP_A7/PIRQA#

M.2 SATA/PCIE x 2 -SSD

56 PCIE_RXN11_M2_SSD → PCIE_RXN11_M2_SSD E28
56 PCIE_RXP11_M2_SSD → PCIE_RXP11_M2_SSD E27
56 PCIE_TXN11_M2_SSD → PCIE_TXN11_M2_SSD D24
56 PCIE_TXP11_M2_SSD → PCIE_TXP11_M2_SSD C24
56 SATA_RXN12_M2_SSD → SATA_RXN12_M2_SSD E30
56 SATA_RXP12_M2_SSD → SATA_RXP12_M2_SSD F30
56 SATA_TXN12_M2_SSD → SATA_TXN12_M2_SSD A25
56 SATA_TXP12_M2_SSD → SATA_TXP12_M2_SSD B25
PCIE11_RXN/SATA1B_RXN
PCIE11_RXP/SATA1B_RXP
PCIE11_TXN/SATA1B_TXN
PCIE11_TXP/SATA1B_TXP
PCIE12_RXN/SATA2_RXN
PCIE12_RXP/SATA2_RXP
PCIE12_TXN/SATA2_TXN
PCIE12_TXP/SATA2_TXP

If SATA driver need change port,
Also must change reltaed "DEVSLP and SATAXPCIE" pin

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SSIC / USB3

USB3_1_RXN H8 USB3_RXN1 → USB3_RXN1 52
USB3_1_RXP G8 USB3_RXP1 → USB3_RXP1 52
USB3_1_TXN C13 USB3_TXN1 → USB3_TXN1 52
USB3_1_TXP D13 USB3_TXP1 → USB3_TXP1 52
USB3.0 S/C

USB3_2_RXN/SSIC_RXN J6 USB3_RXN2 → USB3_RXN2 52
USB3_2_RXP/SSIC_RXP H6 USB3_RXP2 → USB3_RXP2 52
USB3_2_TXN/SSIC_TXN B13 USB3_TXN2 → USB3_TXN2 52
USB3_2_TXP/SSIC_TXP A13 USB3_TXP2 → USB3_TXP2 52
USB3.0

USB3_3_RXN J10 USB3_RXN3 → USB3_RXN3 41
USB3_3_RXP H10 USB3_RXP3 → USB3_RXP3 41
USB3_3_TXN B15 USB3_TXN3 → USB3_TXN3 41
USB3_3_TXP A15 USB3_TXP3 → USB3_TXP3 41
USB3.0 Type C

USB3_4_RXN E10 USB3_RXN4 → USB3_RXN4 41
USB3_4_RXP F10 USB3_RXP4 → USB3_RXP4 41
USB3_4_TXN C15 USB3_TXN4 → USB3_TXN4 41
USB3_4_TXP D15 USB3_TXP4 → USB3_TXP4 41
USB3.0 Type C

USB2

USB2N_1 AB9 → USB_PN1_30 52
USB2P_1 AB10 → USB_PP1_30 52
USB3.0 S/C

USB2N_2 AD6 → USB_PN2_30 52
USB2P_2 AD7 → USB_PP2_30 52
USB3.0

USB2N_3 AH3 → USB_PN3_TYPEC 41
USB2P_3 AJ3 → USB_PP3_TYPEC 41
USB3.0 Type C

USB2N_4 AD9 → USB_PN4_TYPEC 41
USB2P_4 AD10 → USB_PP4_TYPEC 41
USB3.0 Type C

USB2N_5 AJ1 → USB_PN5_20 64
USB2P_5 AJ2 → USB_PP5_20 64
USB20 (IO BD)

USB2N_6 AF6 → USB_PN6_BT 53
USB2P_6 AF7 → USB_PP6_BT 53
Bluetooth

USB2N_7 AH1 → USB_PN7_CCD 45
USB2P_7 AH2 → USB_PP7_CCD 45
Camera (EDP CONN)

USB2N_8 AF8 → USB_PN8_CR 64
USB2P_8 AF9 → USB_PP8_CR 64
Card reader (IO BD)

USB2N_9 AG1 → USB_PN9_FP 69
USB2P_9 AG2 → USB_PP9_FP 69
FingerPrinter

USB2N_10 AH7 → USB_PN10_TP 45
USB2P_10 AH8 → USB_PP10_TP 45

USB2_COMP AB6 USBCOMP → R23021 1% 2 113Ohm
USB2_ID AG3 USB2_ID_OTG → R23191 2 1KOhm
USB2_VBUSSENSE AG4 USB2_VBUSSENSE_OTG → R23201 2 1KOhm
USB2_COMP PDG 1.0 R=113 +-1%

GPP_E9/USB2_OC0# A9 OC0# @/SP SP2301 1 2 0Ohm → USB_OC0#_PCH 52
GPP_E10/USB2_OC1# C9 OC1# @/SP SP2302 1 2 0Ohm → USB_OC1#_PCH 52
GPP_E11/USB2_OC2# D9 OC2# @/SP SP2303 1 2 0Ohm → USB_OC2#_PCH 64
GPP_E12/USB2_OC3# B9 OC3# @/SP SP2304 1 2 0Ohm → USB_OC3#_PCH 41
USB30 with USB Chager
USB30
USB20(IO BD)
Type C

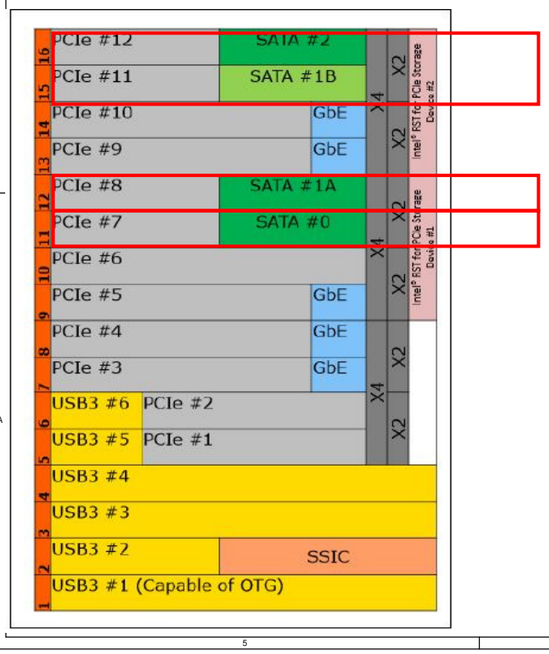
(OD) GPP_E4/DEVSLP0 J1 1 T2326
(OD) GPP_E5/DEVSLP1 J2 SATA_DEVSLP1 → SATA_DEVSLP1 51
(OD) GPP_E6/DEVSLP2 J3 SATA_DEVSLP2 → SATA_DEVSLP2 51
SATA SSD1
SATA SSD2

GPP_E0/SATAXPCIE0/SATAGP0 H2 1 T2325
GPP_E1/SATAXPCIE1/SATAGP1 H3 SATA_SSD1_PEDET → SATA_SSD1_PEDET 51
GPP_E2/SATAXPCIE2/SATAGP2 G4 SATA_SSD2_PEDET → SATA_SSD2_PEDET 51

GPP_E8/SATALED# H1 SATA_LED#

+3VSUS
OC3# 10KOhm 3 4 RN2301B
OC2# 10KOhm 7 8 RN2301D
OC1# 10KOhm 1 2 RN2301A
OC0# 10KOhm 5 6 RN2301C

+3VS
SATA_LED# R2304 1 2 10KOhm
PIRQA# R2318 1 2 10KOhm



Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

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BG1-HW RD

Title : PCH(4)_USB/PCIE/SATA
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 23 of 94

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PCH(5)_CLK

+1.8VSUS
+3VS
+3VSUS
+VCC_RTC

+1.8VSUS 9,26,84
+3VS 3,4,20,21,22,23,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+3VSUS 4,20,21,22,23,25,26,28,30,31,41,51,53,62,74,81,92
+VCC_RTC 25,26,36,60

U0301I
CSI-2

A36	CSI2_DN0	CSI2_CLKN0	C37		
B36	CSI2_DP0	CSI2_CLKP0	D37		
C38	CSI2_DN1	CSI2_CLKN1	C32		
D38	CSI2_DP1	CSI2_CLKP1	D32		
C36	CSI2_DN2	CSI2_CLKN2	C29		
D36	CSI2_DP2	CSI2_CLKP2	D29		
A38	CSI2_DN3	CSI2_CLKN3	B26		
B38	CSI2_DP3	CSI2_CLKP3	A26		
C31	CSI2_DN4	CSI2_COMP	E13	CSI2_COMP	R2418 100Ohm
D31	CSI2_DP4	GPP_D4/FLASHTRIG	B7	GPP_D4 1 T2417	RES 100 OHM 1/16W (0402) 1%
C33	CSI2_DN5				
D33	CSI2_DP5	EMMC			
A31	CSI2_DN6				
B31	CSI2_DP6	GPP_F13/EMMC_DATA0	AP2	eMMC_D0	49
A33	CSI2_DN7	GPP_F14/EMMC_DATA1	AP1	eMMC_D1	49
B33	CSI2_DP7	GPP_F15/EMMC_DATA2	AP3	eMMC_D2	49
		GPP_F16/EMMC_DATA3	AN3	eMMC_D3	49
A29	CSI2_DN8	GPP_F17/EMMC_DATA4	AN1	eMMC_D4	49
B29	CSI2_DP8	GPP_F18/EMMC_DATA5	AN2	eMMC_D5	49
C28	CSI2_DN9	GPP_F19/EMMC_DATA6	AM4	eMMC_D6	49
D28	CSI2_DP9	GPP_F20/EMMC_DATA7	AM1	eMMC_D7	49
A27	CSI2_DN10	GPP_F21/EMMC_RCLK	AM2	eMMC_RCLK	49
B27	CSI2_DP10	GPP_F22/EMMC_CLK	AM3	eMMC_CLK	49
C27	CSI2_DN11	GPP_F12/EMMC_CMD	AP4	eMMC_CMD	49
D27	CSI2_DP11	EMMC_RCOMP	AT1	EMMC_RCOMP	R2419 200Ohm
					RES 200 OHM 1/16W (0402) 1%

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GND

VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V.

+1.8VSUS
R2412 100KOhm 1% @
RTC_IN# 22
+RTCBAT
Q2402 2N7002 @
R2409 10MOhm @
+3VA
R2425 0Ohm @
R2423 1.5KOhm 1%
+RTC_AC
R2424 45.3KOhm 1%
+VCC_RTC
R2420 1KOhm @
D2401 RB751V-40 0.37V/30mA
D2402 RB751V-40 0.37V/30mA
+RTC_BAT
R2405 1 2 1KOhm
C2407 1UF/6.3V
CON2401
SIDE2
SIDE1
WtoB_CON_2P
12V17GISM030
P/N:1217-0105000
GND

U0301J
CLOCK SIGNALS

CLKOUT_PCIE_P/N[5:0] (PDG v1.3 Page420)
Any differential clock pair not being used must be left as no connect

51	CLK_PCIE_SSD1#	CLK_PCIE_SSD1#	@/SP	SP2405	CLK_PCIE_SSD1#_PCH_R	B42	CLKOUT_PCIE_N0
51	CLK_PCIE_SSD1	CLK_PCIE_SSD1	@/SP	SP2406	CLK_PCIE_SSD1_PCH_R	A42	CLKOUT_PCIE_P0
51	CLK_REQ1_SSD1#	CLK_REQ1_SSD1#	@/SP	SP2407	CLK_REQ1_SSD1#_R	AT7	GPP_B5/SRCCLKREQ0#
51	CLK_PCIE_SSD2#	CLK_PCIE_SSD2#	@/SP	SP2408	CLK_PCIE_SSD2#_PCH_R	D41	CLKOUT_PCIE_N1
51	CLK_PCIE_SSD2	CLK_PCIE_SSD2	@/SP	SP2409	CLK_PCIE_SSD2_PCH_R	C41	CLKOUT_PCIE_P1
51	CLK_REQ2_SSD2#	CLK_REQ2_SSD2#	@/SP	SP2410	CLK_REQ2_SSD2#_R	AT8	GPP_B6/SRCCLKREQ1#
70	PEX_REFCLK*	PEX_REFCLK*	@/SP	SP2415	PEX_REFCLK*_R	D40	CLKOUT_PCIE_N2
70	PEX_REFCLK	PEX_REFCLK	@/SP	SP2416	PEX_REFCLK_R	C40	CLKOUT_PCIE_P2
70	CLK_REQ3_PEG#	CLK_REQ3_PEG#	@/SP	SP2417	CLK_REQ3_PEG#_R	AT10	GPP_B7/SRCCLKREQ2#
53	CLK_PCIE_WLAN#_PCH	CLK_PCIE_WLAN#_PCH	@/SP	SP2412	CLK_PCIE_WLAN#_PCH_R	B40	CLKOUT_PCIE_N3
53	CLK_PCIE_WLAN_PCH	CLK_PCIE_WLAN_PCH	@/SP	SP2413	CLK_PCIE_WLAN_PCH_R	A40	CLKOUT_PCIE_P3
53	CLK_REQ4_WLAN#	CLK_REQ4_WLAN#	@/SP	SP2414	CLK_REQ4_WLAN#_R	AU8	GPP_B8/SRCCLKREQ3#
						E40	CLKOUT_PCIE_N4
						E38	CLKOUT_PCIE_P4
						AU7	GPP_B9/SRCCLKREQ4#
							CLKOUT_PCIE_N5
							CLKOUT_PCIE_P5
							GPP_B10/SRCCLKREQ5#

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CLKOUT_ITPXDP_N	F43		
CLKOUT_ITPXDP_P	E43		
GPD8/SUSCLK	BA17	SUSCLK_PCH	1 T2418
XTAL24_IN	E37	XTAL_24M_IN	
XTAL24_OUT	E35	XTAL_24M_OUT	
XCLK_BIASREF	E42	XCLK_BIASREF	R2417 1 0.5% 2 2.71Kohm +VCCF24NS_1P0
RTCX1	AM18	XTAL_32K_X1	
RTCX2	AM20	XTAL_32K_X2	
SRTCRST#	AN18	SRTC_RST#	
RTCRST#	AM16	RTC_RST#	

+VCC_RTC
R2403 1 2 20KOhm
JRST2402 SGL_JUMP @/SP
C2405 1UF/6.3V
R2455 1 2 0Ohm
R2404 1 2 20KOhm
Q2401 2N7002
JRST2401 SGL_JUMP @/SP
C2406 1UF/6.3V
C2409 0.1UF/16V @
30 SW_RTCRST
SP2403 1 @/SP 2 0Ohm
R2407 10KOhm
GND

CLK_REQ4_WLAN#_R — R2429 10KOhm +3VSUS; R2408 @ 10KOhm +3VS; R2411 @ 10KOhm GND
CLK_REQ3_PEG#_R — R2421 @ 10KOhm +3VSUS; R2410 @ 10KOhm +3VS; R2413 @ 10KOhm GND
CLK_REQ2_SSD2#_R — R2414 10KOhm +3VS; R2416 @ 10KOhm GND
CLK_REQ1_SSD1#_R — R2430 10KOhm +3VS; R2431 @ 10KOhm GND

SRCCLKREQ#[5:0] (PDG v1.3 Page 835)
Any un-used, disabled, must be left as no connects at the PCH side on the platform.
Any used, enabled, should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail.

24MHz signal 需包GND

Ball E37 XTAL_24M_IN — R2432 /U22 0Ohm
Ball E35 XTAL_24M_OUT — R2433 /U22 0Ohm
XTAL_24M_OUT_R_R — R2401 2 /U22 11MOhm
SP2401 0Ohm @/SP
X2401 24MHZ /U22
XTAL_24M_OUT_R
C2402 10PF/50V /U22
C2401 10PF/50V /U22
GND

XTAL_32K_X1
XTAL_32K_X2
R2402 10MOhm
SP2402 0Ohm @/SP
X2402 32.768KHZ 07V080000075 +/-20ppm/9PF
XTAL_32K_X1_R
C2404 7PF/50V
C2403 7PF/50V
GND

PEGATRON Title PCH(5)_CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD Engineer: Kai_Shen
Size C | Project Name HE4EA | Rev 1.0
Date: Friday, April 07, 2017 Sheet 24 of 94

N/A

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PCH(6)_POWER MANAGE

+1.0V +1.0V 3,5,7,9,32,57,91
+3V +3V 31,45,57,91
+3VSUS +3VSUS 4,20,21,22,23,24,26,28,30,31,41,51,53,62,74,81,92
+VCC_RTC +VCC_RTC 24,26,36,60

In Table 42-1 of PDG (#561280, Rev1p0)
PROCPWRGD is PCH to CPU, but KBL-U don't has this pin at CPU side.
we assume it's conted in MCP package.
So follow CRB to reserve TP only.

U0301K
SYSTEM POWER MANAGEMENT

PLT_RST# → AN10 GPP_B13/PLTRST#
PM_SYS_RESET#_R B5 SYS_RESET#
30 PM_RSMRST# → SP2501 @/SP → PM_RSMRST_R AY17 RSMRST#
T2501 H_CPUPWRGD_TP → R2503 @ 1KOhm → H_CPUPWRGD A68 PROCPWRGD
VCCST_PWRGD_CPU B65 VCCST_PWRGD
ALL_SYS_PWRGD delay 99 ms from EC
30 SYS_PWROK_PCH → SYS_PWROK_PCH B6 SYS_PWROK
PCH_PWROK_PCH BA20 PCH_PWROK
PM_RSMRST_R @/SP SP2502 0Ohm → PCH_DPWROK BB20 DSW_PWROK
DSW function / non-AMT
T2513 SUS_PWR_ACK_R → R2506 0-ohm 0Ohm → SUS_PWR_ACK_R AR13
T2512 SUSACK# → R2510 @ 0Ohm → SUSACK#_R AP11 GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
53 WAKE_PCIE# → BB15 WAKE#
T2511 LAN_WAKE# AM15 GPD2/LAN_WAKE#
T2502 GPD11 AW17 GPD11/LANPHYPC
T2508 GPD7 AT15 GPD7/RSVD

GPP_B12/SLP_S0# AT11 SLP_S0# → T2503
GPD4/SLP_S3# AP15 PM_SUSB#
GPD5/SLP_S4# BA16 PM_SUSC#
GPD10/SLP_S5# AY16 GPD10 → T2504
SLP_SUS# AN15 SLP_SUS# → T2510 If Deep Sx is not implemented on the platform, this signal may be left as no connect
SLP_LAN# AW15 SLP_LAN# → T2505
GPD9/SLP_WLAN# BB17 SLP_WLAN# → T2506
GPD6/SLP_A# AN16 ME_PM_SLP_M#_PCH → T2507
BA15
GPD3/PWRBTN# AY15 AC_PRESENT_R SP2505 @/SP 0Ohm → PM_PWRBTN# 30
GPD1/ACPRESENT AU13 BATLOW# → ME_AC_PRESENT 30
GPD0/BATLOW#
GPP_A11/PME# AU11 PME#
INTRUDER# AP16 SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# AM10 MPHY_EXT_PWR_GATEB_R → T2509 internal pull high
GPP_B2/VRALERT# AM11 VR_ALERT#

947859
0101-03860PB

PCH_PWROK logic

30,92 ALL_SYSTEM_PWRGD → R2531 @ 0Ohm
30 DELAY_ALL_SYSTEM_PWRGD → R2507 0-ohm 0Ohm → ALL_SYSTEM_PWRGD_PMOK
74,80,92 VRM_PWRGD → D2501 RB751V-40 → VR_READY_PMOK
PLT_RST# → D2502 RB751V-40

+3VSUS
U2502 (A, B, GND, VCC, Y) Vcc=2~5.5
PM_PWROK R2505 0Ohm → PCH_PWROK_PCH
C2516 0.1UF/16V @ → GND
R2517 @ 0Ohm
R2554 100KOhm N/A → GND
R2519 10KOhm → GND

30 DE_ALL_SYS_PGD_EC → SP2507 @/SP → DE_ALL_SYS_PGD_EC_R
PM_SUSB#
U2504 (A, B, GND, VCC, Y) Vcc=2~5.5
+3VSUS
For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms
Delay By EC(2ms+ EC processing time (3ms~33ms)
DE_ALL_SYS_PGD_HW 30
For shut down Sequence
Tplt17 < 1us
R2545 @100KOhm 10V240000005
C2540 0.1UF/16V @ → GND

SLP_S3# and SLP_S4# logic

PM_SUSB# → R2502 0Ohm → PM_SUSB# 30
30,57,74,91,92 SUSB_EC#
PM_SUSC# → R2504 0Ohm → PM_SUSC# 30
30,57,91 SUSC_EC#

+3VSUS
BATLOW# R2522 10KOhm
LAN_WAKE# R2523 10KOhm
GPD7 R2524 10KOhm
WAKE_PCIE# R2525 1KOhm
AC_PRESENT_R R2526 10KOhm

SYS_PWROK logic

+3V
U2501 @ (A, B, GND, VCC, Y) SN74LVC1G08DCKR
PLT_RST# → C2502 100PF/50V @ → GND
R2515 0-ohm 0Ohm
C2541 0.1UF/16V @ → GND
C2503 100PF/50V @ → GND
R2516 10KOhm → GND
BUF_PLT_RST# 30,32,49,51,53,62,70

30 SYS_PWROK_EC → R2508 0-ohm 0Ohm
PM_SUSB#
U2505 (A, B, GND, VCC, Y) Vcc=2~5.5
+3VSUS
SYS_PWROK_AND → R2509 0-ohm 0Ohm → SYS_PWROK_PCH
R2547 @100KOhm 10V240000005 → GND

+VCC_RTC
SM_INTRUDER# R25131 1MOhm
+3VSUS
internal pull high
PME# R2527 @ 10KOhm
Set to GPI
VR_ALERT# R2528 @ 10KOhm
PM_SYS_RESET#_R R2501 N/A 10KOhm

VCCST_PWRGD logic

+3VSUS
U2503 (NC, A, GND, VCC, Y) 74AUP1G07GW 06V030000021
C2504 0.1UF/16V → GND
+1.0V
R2520 1KOhm
DELAY_ALL_SYSTEM_PWRGD → R2511 0-ohm 0Ohm → H_VCCST_PWRGD_L
ALL_SYSTEM_PWRGD → R2530 @ 0Ohm
VCCST_PWRGD_CPU_R R2553 0Ohm
R2521 1% 60.4Ohm → VCCST_PWRGD_CPU
C2505 @ 0.1UF/16V → GND
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms

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Title : PCH(6)_POWER MANAGE
BG1-HW RD
Engineer: Kai_Shen
Size C | Project Name HE4EA | Rev 1.0
Date: Friday, April 07, 2017 | Sheet 25 of 94

26 PCH(7)_POWER

Table 10-5. SKL U / SKL Y PCH-LP
VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

PCIe Gen3 Lane X10
USB3 Port X3
All HSIO disabled (basic comsunption)
=0.154x10+0.132x3+0.064
=2 A

+1.0VSUS
+1.8VSUS
+3VSUS
+VCCPRIM_CORE
+1.0VSUS 82
+1.8VSUS 9,24,84
+3VSUS 4,20,21,22,23,24,25,28,30,31,41,51,53,62,74,81,92
+VCCPRIM_CORE 82

+1.0VSUS 4A
+VCCMPHYGTAON_1P0_LS_SIP 2A
+VCCSRAM_1P0
+VCCAMPHYPLL_1P0
+VCCAPLLEBB_1P0
S1V080500001 S1V040200001 0Ohm
0.642A 0.088A 0.033A
C2628 0.1UF/16V GND

+1.0VSUS_ORG
C2601 1UF/6.3V vx_c0402_small near AB19
+VCCPRIM_CORE
C2602 1UF/6.3V vx_c0402_small near AF18
+1.0VSUS_ORG
C2603 1UF/6.3V vx_c0402_small near K17
+VCCMPHYGTAON_1P0_LS_SIP 2A
C2605 47UF/6.3V @ near N15
C2606 1UF/6.3V near N15
+VCCAMPHYPLL_1P0
C2607 1UF/6.3V vx_c0402_small near K15
+3VSUS_ORG
C2611 1UF/6.3V vx_c0402_small near V19
+VCCAPLLEBB_1P0
C2612 1UF/6.3V near N18

U0301O
CPU POWER 4 OF 4

0.696A	AB19	VCCPRIM_1P0_1	
	AB20	VCCPRIM_1P0_2	
	P18	VCCPRIM_1P0_3	
2.574A	AF18	VCCPRIM_CORE_1	
	AF19	VCCPRIM_CORE_2	
	V20	VCCPRIM_CORE_3	
	V21	VCCPRIM_CORE_4	
	AL1	DCPDSW_1p0	
0.022A	K17	VCCMPHYAON_1P0_1	
	L1	VCCMPHYAON_1P0_2	
	N15	VCCMPHYGT_1P0_1	
	N16	VCCMPHYGT_1P0_2	
	N17	VCCMPHYGT_1P0_3	
	P15	VCCMPHYGT_1P0_4	
	P16	VCCMPHYGT_1P0_5	
0.088A	K15	VCCAMPHYPLL_1P0_1	
	L15	VCCAMPHYPLL_1P0_2	
+VCCAPLL_1P0_SOC 0.026A	V15	VCCAPLL_1P0	
0.696A	AB17	VCCPRIM_1P0_4	
	Y18	VCCPRIM_1P0_5	
0.118A	AD17	VCCDSW_3p3_1	
	AD18	VCCDSW_3p3_2	
	AJ17	VCCDSW_3p3_3	
+VCCPAZIO_SOC 0.068A	AJ19	VCCHDA	
0.011A	AJ16	VCCSPI	
0.642A	AF20	VCCSRAM_1P0_1	
	AF21	VCCSRAM_1P0_2	
	T19	VCCSRAM_1P0_3	
	T20	VCCSRAM_1P0_4	
0.075A	AJ21	VCCPRIM_3p3_1	
0.696A	AK20	VCCPRIM_1P0_6	
0.033A	N18	VCCAPLLEBB_1P0	

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Decoupling cap for internal power
+VCCDSW_1P0 C2604 1UF/6.3V near AL1
+VCCSRAM_1P0 C2610 1UF/6.3V vx_c0402_small near AF20
+1.0VSUS_ORG R2648 0Ohm C2644 0.1UF/16V
+VCCDSW_3P3
+1.0VSUS_ORG R2649 0Ohm C2645 0.1UF/16V

	AK15	VCCPGPPA	0.002A
	AG15	VCCPGPPB	0.004A
	Y16	VCCPGPPC	0.006A
	Y15	VCCPGPPD	0.008A
	T16	VCCPGPPE	0.006A
	AF16	VCCPGPPF	0.161A
	AD15	VCCPGPPG	0.0041A
	V19	VCCPRIM_3p3_2	0.075A
	T1	VCCPRIM_1P0_7	0.696A
	AA1	VCCATS_1p8	0.006A
	AK17	VCCRTCPRIM_3p3	0.001A
	AK19	VCCRTC_1	
	BB14	VCCRTC_2	
	BB10	DCPRTC	
	A14	VCCCLK1	0.035A
	K19	VCCCLK2	0.029A
	L21	VCCCLK3	0.024A
	N20	VCCCLK4	0.033A
	L19	VCCCLK5	0.004A
	A10	VCCCLK6	0.0039A
	AN11	GPP_B0/CORE_VID0	
	AN13	GPP_B1/CORE_VID1	

R2650 0Ohm C2646 @ 0.1UF/16V
R2651 0Ohm C2647 @ 0.1UF/16V
GND C2634 1UF/6.3V near AK19
VCCRTCEXT C2620 1UF/6.3V near BB10
C2619 1UF/6.3V near AK19
R2646 1KOhm R2647 1KOhm
Intel confirm pull down 1k

+3VSUS_ORG
vx_c0402_small C2635 near AG15
vx_c0402_small C2613 near Y16
vx_c0402_small C2614 near T16
+1.8VSUS_ORG
+1.0VSUS_ORG
+V1.8A_SIP
SP2605 0Ohm @/SP S1V040200001
C2615 1UF/6.3V near AA1
+3VSUS_ORG
C2625 1UF/6.3V near AK17
C2617 1UF/6.3V near AK17
C2618 1UF/6.3V near AK17
+VCC_RTC
+VCC19P2_1P0 SP2606 0Ohm @/SP S1V040200001 +1.0VSUS_ORG
+VCCF100_1P0 SP2607 0Ohm @/SP S1V040200001 +1.0VSUS_ORG
+VCCF135_1P0 SP2608 0Ohm @/SP S1V040200001 +1.0VSUS_ORG
+VCCF100OC_1P0 SP2609 0Ohm @/SP S1V040200001 +1.0VSUS_ORG
+VCCF24NS_1P0 SP2610 0Ohm @/SP S1V040200001 +1.0VSUS_ORG
+VCC24TBT_1P0 SP2611 0Ohm @/SP S1V040200001 +1.0VSUS_ORG
near A10
C2624 1UF/6.3V vx_c0402_small

+1.0VSUS R26041 0Ohm +VCCAPLL_1P0
C2608 47uF/6.3V @ C2636 0.1UF/16V
09V010000096 B2601 75OHM
C2640 2PF/25V NPO/+/-0.25PF vx_c0201 C2641 2PF/25V NPO/+/-0.25PF vx_c0201
+VCCAPLL_1P0_SOC near V15
GND

+3VSUS SP2602 @/SP 0Ohm S1V040200001 +VCCPAZIO
C2609 1UF/10V @ C2637 0.1UF/16V
09V010000096 B2602 75OHM
C2642 2PF/25V NPO/+/-0.25PF vx_c0201 C2643 2PF/25V NPO/+/-0.25PF vx_c0201
+VCCPAZIO_SOC near AJ19
GND

EMI request for Kaby Lake
Recommended Routing : Stripline < 2"
Alternative Routing : Microstrip <1"
(less noise-reduction)

+3VSUS SP2601 @/SP 0Ohm 0.5A S1V040200001 +3VSUS_ORG
+1.0VSUS SP2603 @/SP 0Ohm 1A S1V060300001 +1.0VSUS_ORG
+1.8VSUS SP2604 @/SP 0Ohm 0.5A S1V040200001 +1.8VSUS_ORG

+3VSUS R26361 @ 0Ohm +VCCPDSW_3P3
Q2601 PJA3411
Q2602 BC856BS
R2635 100KOhm
R2634 100KOhm

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BG1-HW RD
Title PCH(7)_POWER
Engineer: Kai_Shen
Size C | Project Name HE4EA | Rev 1.0
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PCH(9)_SPI_SMB

+3VSUS
+3VA
+12VSUS

+3VSUS 4,20,21,22,23,24,25,26,30,31,41,51,53,62,74,81,92
+3VA 24,30,31,36,53,57,67,81,88,93
+12VSUS 49,81,91

55mA

+3VSUS — R2802 1 — 2 0Ohm — +3VM_SPI
+3VA — R2830 1 — 2 0Ohm — +3VM_SPI

15WW06 MOW Pull-up Resistors on SPI_IO2 and SPI_IO3 are no longer needed

+3VM_SPI

R2811 1KOhm
R2812 3.3KOhm

C2801 0.1UF/16V
R2813 1KOhm

FAE: 2015/10/14

R2820 1 — 2 1KOhm

20	SPI_WP#_IO2	R2805 1 — 2 33Ohm	SPI1_CS#0	U2801 CS# / VCC 8
20	SPI_SO	R2806 1 — 2 33Ohm	SPI1_SO	DO(IO1) / HOLD#(IO3) 7
20	SPI_CS#0	R2807 1 — 2 33Ohm	SPI1_WP#	WP#(IO2) / CLK 6
30	F_CS#_EC	R2808 1 — 2 33Ohm		GND / DI(IO0) 5
30	F_SDIO_EC	R2809 1 — 2 33Ohm		1 2 3 4

W25Q64FVSSIQ
05V000000025

SPI1_HOLD#
SPI1_CLK
SPI1_SI

R2814 1 — 2 33Ohm — SPI_HOLD#_IO3 20
R2815 1 — 2 33Ohm — SPI_CLK 20
R2816 1 — 2 33Ohm — SPI_SI 20
R2818 1 — 2 33Ohm — F_SCK_EC 30
R2819 1 — 2 33Ohm — F_SDI_EC 30
R2821 1 — 2 3KOhm — +3VM_SPI

WW48MOW(ES Sample)
In Skylake Platform Design Guides (PDG) under “Platform Debug & Test Hooks” chapter, HOOK[3] pin from XDP/CMC header needs to be routed to PCH SPI0_MOSI pin. The termination resistor can be a value from 1K to 3K ohm pull up to Always rail (not Core rail) with voltage value from 0.8V to 3.3V. This will ensure PCH hardware straps are not overridden unintentionally and cause boot issues.

+3VM_SPI

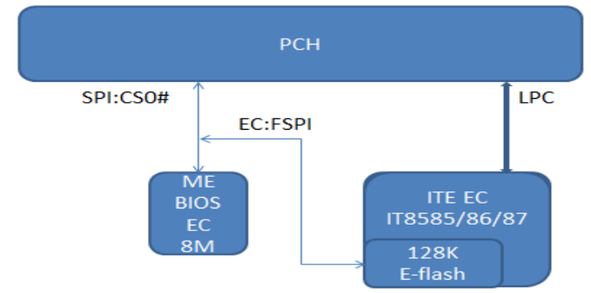
/Debug
CON2810

21	PCH_UATR0_DEBUG_TX	PCH_UATR0_DEBUG_TX	SPI_CS#0 R2850 2 /Debug 1 0Ohm	SIDE1 13
21	PCH_UATR0_DEBUG_RX	PCH_UATR0_DEBUG_RX	SPI_SO R2851 2 /Debug 1 0Ohm	
			SPI_CLK R2852 2 /Debug 1 0Ohm	
			SPI_SI R2853 2 /Debug 1 0Ohm	
		SPI_HOLD#_IO3		SIDE2 14

FPC_CON_12P

12V18GWSM055

SPI ROM size		
T-pad function	P/N	Size
NON-POA *	05V000000025	8M
POA	05V000000031	16M



PCH SMBus

+12VSUS

30,74	SMB1_CLK	Q2802A UM6K1NG1DTN Rdson=13Ohm/Vgs(th)=1.5V N/A		SML1_CLK 20
30,74	SMB1_DAT	Q2802B UM6K1NG1DTN N/A		SML1_DAT 20

EC

GPU

PCH

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BG1-HW RD

Title : PCH(9)_SPI_SMB

Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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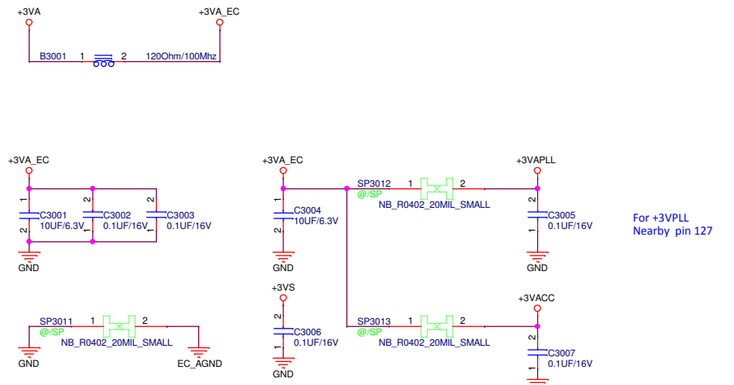
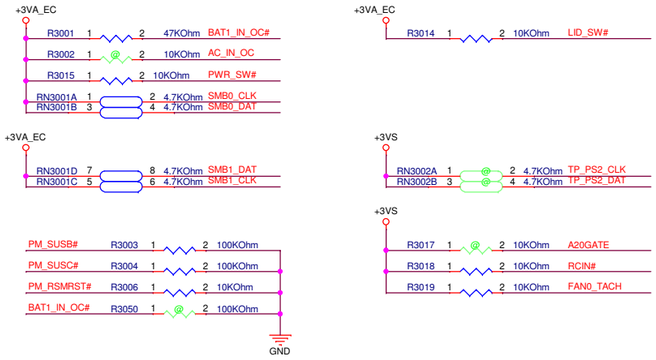
For EC Power



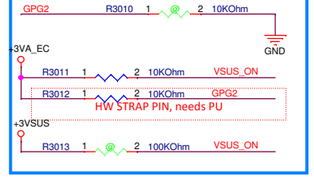
For PU / PD



R1.0 PCH internal pull high

R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in

141112 Remove Pull-D 10K to F_SDI_EC
(F Version problem has be solved)



Reserved for IT8587E/FX

AD_IINP	R3055	1	2 0Ohm
SUS_PWRGD	R3056	1	2 0Ohm
ALL_SYSTEM_PWRGD	R3057	1	2 0Ohm
GPI6	R3060	1	2 0Ohm

GND

31 KB_TP

Keyboard Backlight

+3V 25,45,57,91
+3VS 3,4,20,21,22,23,24,30,32,36,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+3VA 24,28,30,36,53,57,67,81,88,93
+5VS 36,45,48,50,57,69,80,87,91
+12VS 57,91

N/A
CON3101
12V18ABSM034
FPC_CON_28P

KSI7 KSI6 KSI5 KSI4 KSI3 KSI2 KSI1 KSI0
KSO15 KSO14 KSO13 KSO12 KSO11 KSO10 KSO9 KSO8 KSO7 KSO6 KSO5 KSO4 KSO3 KSO2 KSO1 KSO0

R3149 33Ohm 10V240000018
D3105 AZ5725-01F 07V180000049 /EMI
C3102 0.1UF/16V
@/SP JRST3101 SGL_JUMP
@/SP JRST3102 SGL_JUMP
PWR_SW# 30

KSI7 33PF/50V C3130
KSI6 33PF/50V C3131
KSI5 33PF/50V C3132
KSI4 33PF/50V C3133
KSI3 33PF/50V C3134
KSI2 33PF/50V C3135
KSI1 33PF/50V C3136
KSI0 33PF/50V C3137

KSO17 33PF/50V C3138
KSO16 33PF/50V C3139
KSO15 33PF/50V C3140
KSO14 33PF/50V C3141
KSO13 33PF/50V C3142
KSO12 33PF/50V C3143
KSO11 33PF/50V C3144
KSO10 33PF/50V C3145
KSO9 33PF/50V C3146
KSO8 33PF/50V C3147
KSO7 33PF/50V C3148
KSO6 33PF/50V C3149
KSO5 33PF/50V C3150
KSO4 33PF/50V C3151
KSO3 33PF/50V C3152
KSO2 33PF/50V C3153
KSO1 33PF/50V C3154
KSO0 33PF/50V C3155

+5VS
R31021 /14inch 0Ohm C3120 @ 0.1UF/16V
R31011 /14inch 340Ohm 1%
CAP_LED# 30
RN3115A 0Ohm @/15inch KSO17
RN3115B 0Ohm @/15inch KSO16
KSO17 30
KSO16 30

Close CON3101

KEYBOARD_LED#	
1	KB w/o BL
0	KB w/ BL

30 KEYBOARD_LED#
+3VA R3114 10KOhm @
+12VS R3107 100KOhm
KB_BL_CTRL
Q3101 SSM3K315T
Q3104 2N7002 Rdson=7.5Ohm/Vgs(th)=2.5V
+5VS_KB_BL
CON3104 FPC_CON_4P 12V18GWSM146 /14inch
KB_BL_GND

+5VS_KB_BL trace >20mils

+5VS F3101 0.75A/6V 07V120000025 +5VS_KB_BL
C3104 10UF/6.3V MLCC 10UF/6.3V (0603)X5R 20%
C3101 0.1UF/16V

KB_BL_GND
+5VS_KB_BL
D3106 AZ5725-01F 07V180000049 /EMI
D3104 AZ5725-01F 07V180000049 /EMI

Click Pad

CON3103 FPC_CON_8P
+3V_TP
TP_PS2_CLK
TP_PS2_DAT
TP_GND_R
PCH_I2C1_SDA_R
PCH_I2C1_SCL_R
TP_IRQ#
TP_SENSOR_OFF#_R

30mA

RN3101A 4.7KOhm N/A
RN3101B 4.7KOhm N/A
R3115 10KOhm
R3116 100KOhm
R3126 2.2KOhm
R3127 5.1KOhm

TP_PS2_CLK 30
TP_PS2_DAT 30
@/SP SP3103 0Ohm
@/SP SP3102 0Ohm
PCH_I2C1_SDA 21
PCH_I2C1_SCL 21
TP_IRQ# 21,30
D3101 RB751V-40
TP_SENSOR_OFF# 21

SP3101 0Ohm @/SP
C3105 33PF/50V
C3106 33PF/50V
C3109 0.1UF/16V
C3115 1UF/6.3V @
C3110 33PF/50V @
C3111 33PF/50V @
C3112 33PF/50V @
C3113 33PF/50V @

For Acer PTP Design Guide
Lid_SW# Need To Close TP Function

D3108 RB751V-40 @/PTP TP_OFF#_EC
TP_OFF#_EC 30
D3111 RB751V-40
LID_SW# 30,45,67

@ D3102 PUSB3F96 07V220000032 For working voltage 5v use
TP_PS2_CLK TP_PS2_DAT PCH_I2C1_SDA PCH_I2C1_SCL

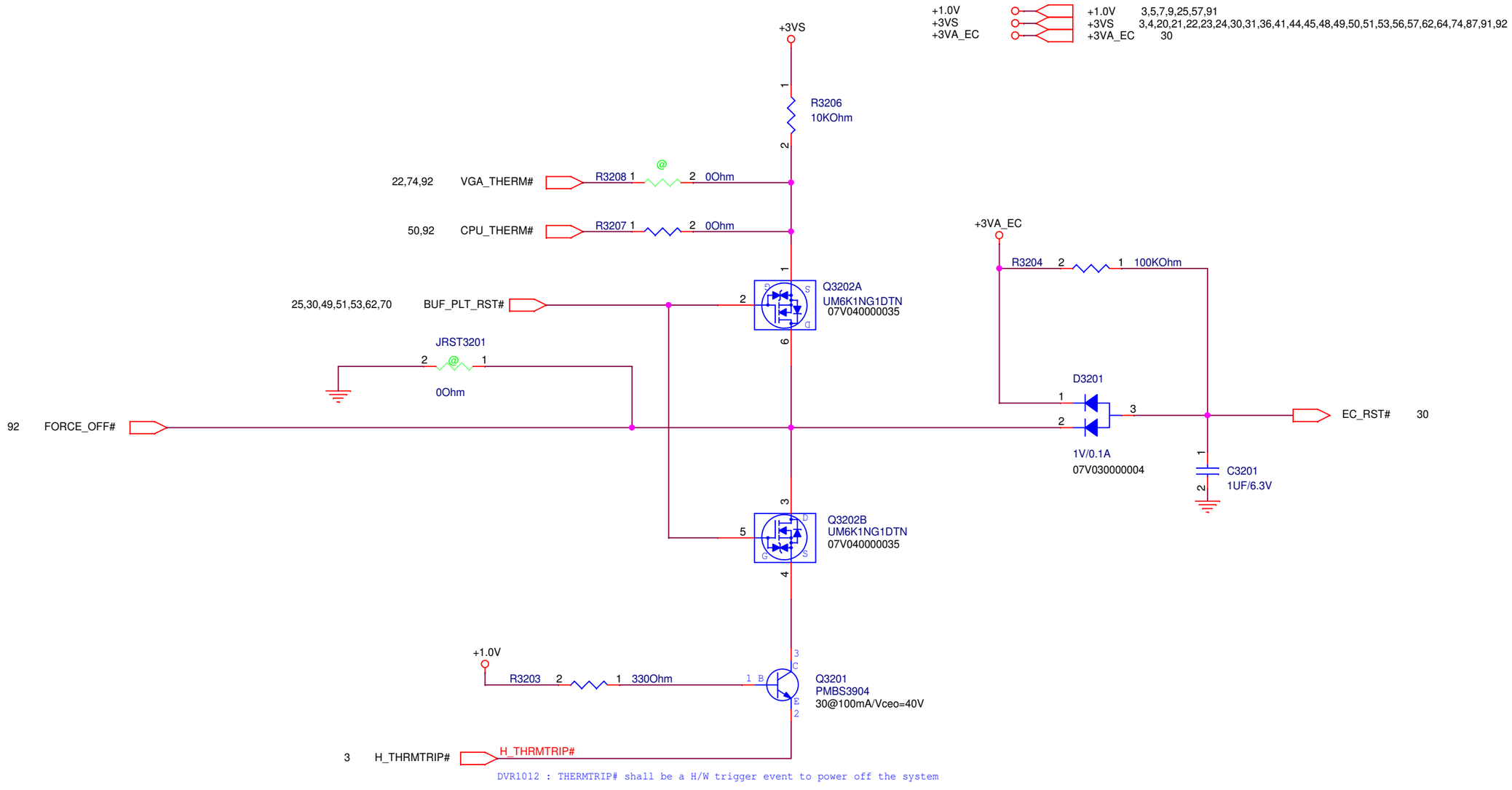
@ D3103 PUSB3F96 07V220000032 For working voltage 5v use
TP_IRQ# TP_SENSOR_OFF#_R

Touch Pad Wake Up S3
+3V +3V_TP
/NON-PTP R31182 0Ohm
+3VS R31172 @ 0Ohm

For Acer PTP Design Guide
Reserve EC TP Enable Schematic
+3VSUS Q3106 PJA3411 +3V_TP @/PTP
+3VA R3123 10KOhm @/PTP
30 PTP_PWR_EN
Q3105 2N7002 @/PTP
R3122 100KOhm @/PTP
C3114 1UF/6.3V @/PTP

PEGATRON	Title :	KB_TP	
BG1-HW RD	Engineer:	Kai_Shen	
Size: C	Project Name: HE4EA		Rev: 1.0
Date: Friday, April 07, 2017	Sheet 31 of 94		

32 RST_Reset Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

BG1-HW RD

Engineer: Kai_Shen

Size	Project Name	Rev
B	HE4EA	1.0

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Size A	Document Number HE4EA			Rev 1.0
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Title	<Title>			
Size A	Document Number HE4EA			Rev 1.0
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AUD_ALC255

+1.8VS
+3VS
+3VA
+5VS
+VCC_RTC

+1.8VS 49,57,91
+3VS 3,4,20,21,22,23,24,30,31,32,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+3VA 24,28,30,31,53,57,67,81,88,93
+5VS 31,45,48,50,57,69,80,87,91
+VCC_RTC 24,25,26,60

AC_HP_R 37
AC_HP_L 37
LINE1_VREFO_L 37
LINE1_VREFO_R 37
MIC2_VREFO 37

Analog
Digital

+1.8VS
L3603 /EMI 300Ohm/100Mhz
R3601 1 @ 2 0Ohm
C3612 10UF/6.3V
GND_AUDIO

+5VS_PVDD_AVD
10UF/6.3V C3611
GND_AUDIO

+3VS_AUDIO
C3638 10UF/6.3V
C3617 1UF/6.3V
C3616 1UF/6.3V

U3601A
ALC255-CGT

CPVDD 36
CBN 35
CPVEE 34
HPOUT-R(PORT-I-R) 33
HPOUT-L(PORT-I-L) 32
LINE1-VREFO-R 31
MIC2-VREFO 30
VREF 29
LDO1-CAP 28
AVDD1 27
AVSS1 26
25

+5VS_AUDIO
C3604 0.1UF/16V
C3637 10UF/6.3V
GND_AUDIO
Place close to Pin 26

R3635 100KOhm
C3609 10UF/6.3V
GND_AUDIO

C3615 2.2UF/6.3V
GND_AUDIO

+3VA
R3637 0Ohm

Digital
Analog

PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

+3VS_AUDIO
R3650 1 @ 2 0Ohm
D3601
HDA_RST# 2
1V/0.1A
21 OP_SD#
T3601 1
OP_SD#_EC 2
D3604 1.2V/0.1A
R3652 1KOhm
R3651 10KOhm
PDB
C3639 1UF/6.3V

CBP 37
AVSS2 38
LDO2-CAP 39
AVDD2 40
PVDD1 41
SPK-OUT-L+ 42
SPK-OUT-L- 43
SPK-OUT-R- 44
SPK-OUT-R+ 45
PVDD2 46
PDB 47
SPDIF-OUT/GPIO2 48
GND 49

37 H_SPKL+ H_SPKL+ 42
37 H_SPKL- H_SPKL- 43
37 H_SPKR- H_SPKR- 44
37 H_SPKR+ H_SPKR+ 45

LINE2-L(PORT-E-L) 24
LINE2-R(PORT-E-R) 23
LINE1-L(PORT-C-L) 22 LINE1_L
LINE1-R(PORT-C-R) 21 LINE1_R
VD33_STB 20
MIC_CAP 19 C3614 10UF/6.3V
MIC2-R(PORT-F-R)/SLEEVE 18 SLEEVE
MIC2-L(PORT-F-L)/RING 17 RING2
MONO-OUT 16
SPDIFO/FRONT_JD(JD3)/GPIO3 15
MIC2/LINE2_JD(JD2) 14 R3604 100KOhm
HP/LINE1_JD(JD1) 13 R3603 200KOhm

LINE1_L 37
LINE1_R 37
SLEEVE 37
RING2 37
+3VS_AUDIO
GND_AUDIO
HP_JD# 37

Place close audio codec

DVDD 1
GPIO0/DMIC-DATA 2
GPIO1/DMIC-CLK 3
DC_DET 4
SDATA-OUT 5
BCLK 6
LDO3-CAP 7
SDATA-IN 8
DVDD-IO 9
SYNC 10
RESETB 11
PCBEEP 12

Analog
Digital

+3VS_AUDIO
02V0J0000076
C3605 10UF/6.3V
C3606 0.1UF/16V
Place close to pin 1

DMIC_DAT_C
DMIC_CLK_C
HDA_BCLK_C
C3607 10UF/6.3V
Q_SDO_V0H

PC_BEEP
HDA_RST# 22
HDA_SYNC 22
HDA_SDI0 22
HDA_BCLK 22
HDA_SDO 22

R3621 2 22Ohm
R3620 2 22Ohm
C3613 1 2 22PF/50V

+3VS_AUDIO
C3618 0.1UF/16V
C3625 10UF/6.3V

45 DMIC_DAT_P4
45 DMIC_CLK_P4
SP3601 1 @/SP 2 0Ohm
R3615 1 2 22Ohm
C3629 33PF/50V @
C3624 33PF/50V

PC_BEEP
C3602 1 2 0.1UF/16V
PCBEEP
R3605 1 2 22KOhm
C3626 100PF/50V @
R3618 4.7KOhm

R3638 1 @ 2 0Ohm
D3603 1V/0.2A
HDA_SPKR 22
EC_SPKR 30
SP3603 1 @/SP 2 0Ohm

U3601B
50 GND1
51 GND2
52 GND3
53 GND4
54 GND5
55 GND6
56 GND7
57 GND8
58 GND9
ALC255-CGT
02V0J0000076

+3VS
5mA
+3VS_AUDIO
R3636 1 2 0Ohm
C3641 100PF/50V /EMI
C3640 10PF/50V @/EMI

1.05A
+5VS
Digital
L3604 /EMI 300Ohm/100Mhz
Analog
+5VS_AUDIO
R3602 1 @ 2 0Ohm
D3602 AZ5725-01F /EMI
Moat
C3628 10UF/6.3V
GND_AUDIO

In order to prevent the built-in LDO damaged from over-voltage on +5VSYS or Standby power line, we suggested using this Voltage suppressing device.

Add this Filter to avoid other components/chips be influenced

+5VS
L3602 600Ohm/100Mhz
+5VS_PVDD_AVD
C3622 0.1UF/16V
C3623 10UF/6.3V
C3619 10UF/6.3V
C3601 0.1UF/16V
Close PIN 41
C3620 10UF/6.3V
C3603 0.1UF/16V
Close PIN 46

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

Grounding circuit for combo jack SLEEVE pin

+3VS_AUDIO +VCC_RTC +3VA
R3634 100KOhm @
R3633 100KOhm @
R3631 100KOhm @
SLEEVE
Q3601 2N7002 @
GND_AUDIO
HDA_RST#
SP3602 0Ohm @/SP
Q3603 2N7002 @
RING2
C3627 1UF/6.3V @
Q3602 2N7002 @
GND_AUDIO

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

D3605 @/EMI
AZ5725-01F
07V180000029
R3622 1 @/EMI 2 0Ohm
R3623 1 /EMI 2 0Ohm
R3624 1 @/EMI 2 0Ohm
R3625 1 @/EMI 2 0Ohm
C3633 1 2 1000PF/50V /EMI
C3635 1 2 100PF/50V @/EMI
C3634 1 2 1000PF/50V @/EMI
GND
GND_AUDIO

PEGATRON Title : AUD_ALC255
BG1-HW RD Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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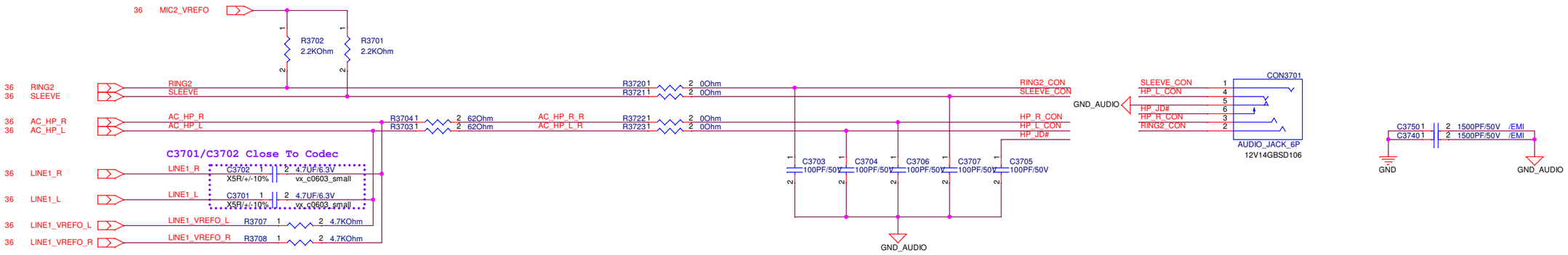
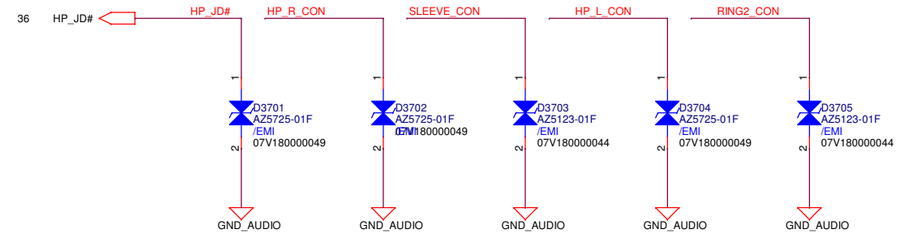
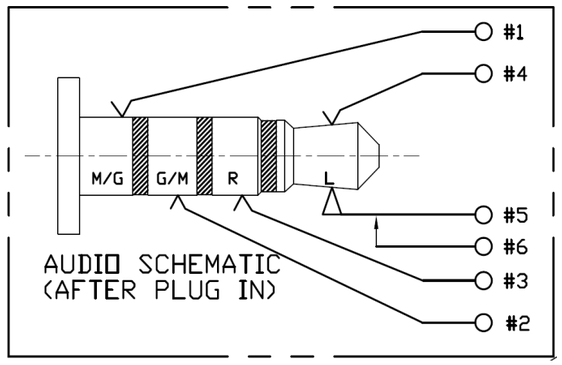
AUD_HP/SPK

Universal Audio Jack

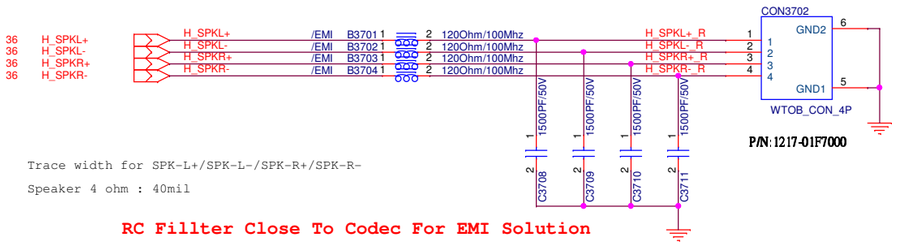


Close to CON3701





Internal Speaker



PEGATRON	Title : AUD_HP/DMIC/SPK		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RD	Engineer: Kai_Shen		
Size: C	Project Name: HE4EA		Rev: 1.0
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Rev: 1.0	
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Rev: 1.0	
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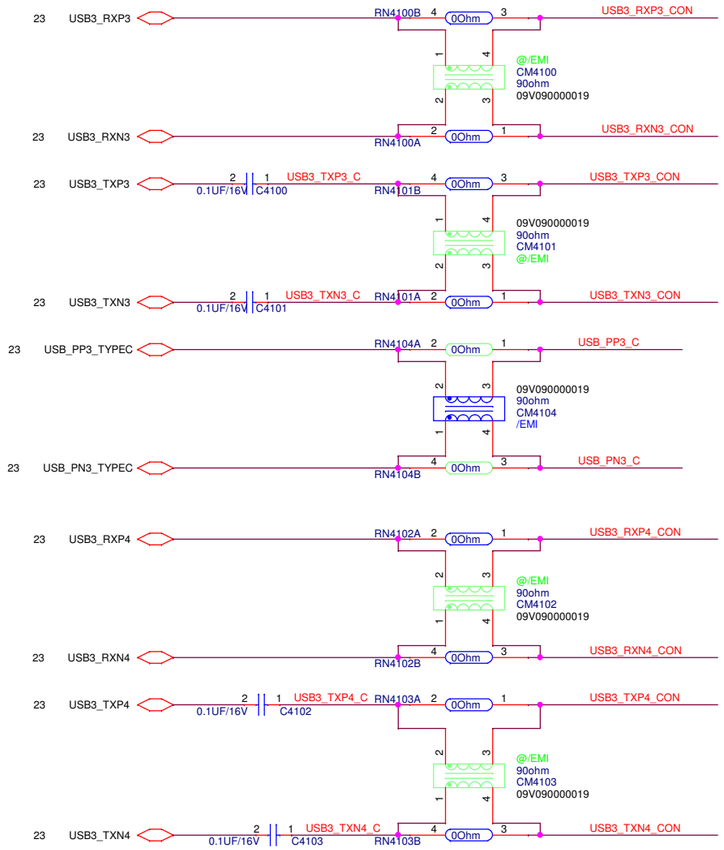
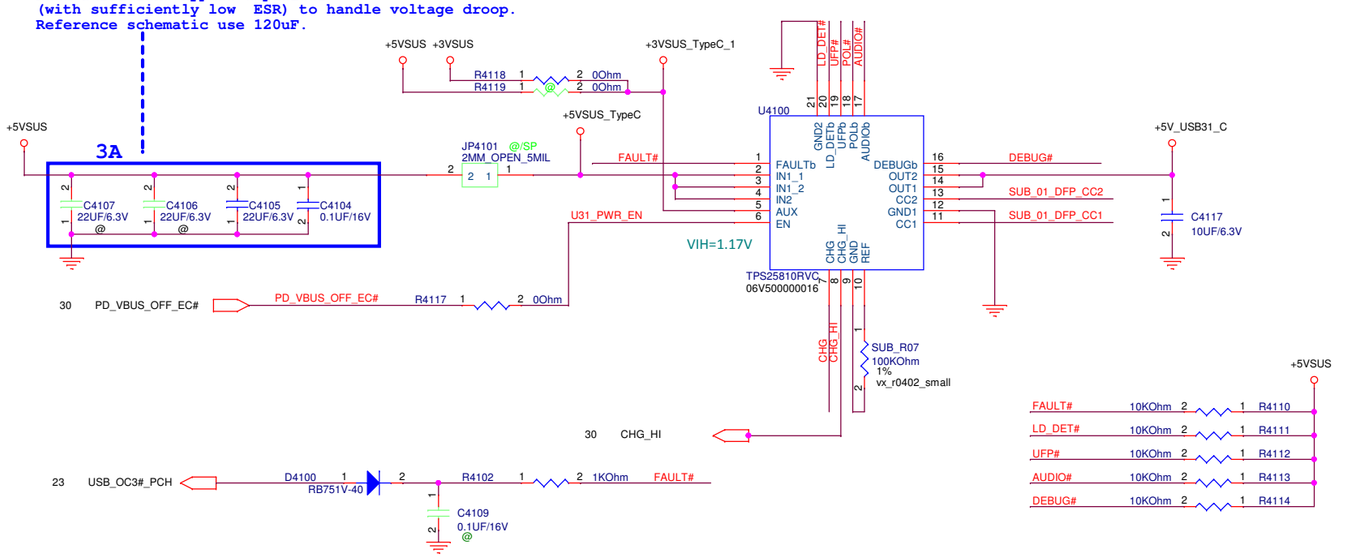
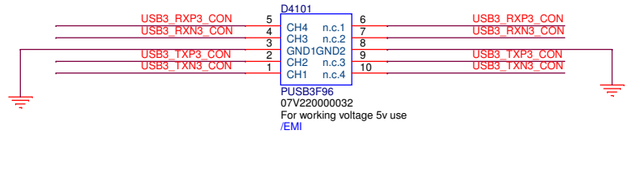
USB3.1 Type C TPS25810

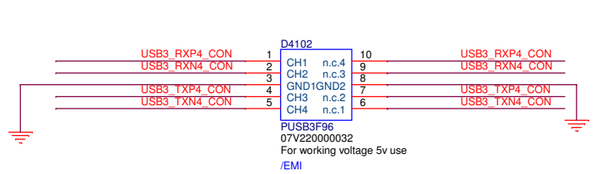


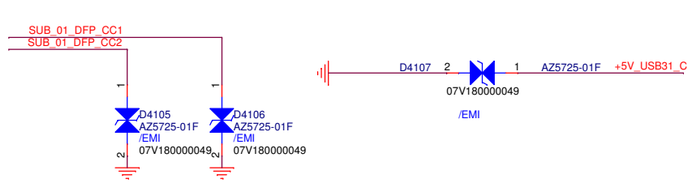
Need sufficient bypass capacitor
(with sufficiently low ESR) to handle voltage droop.
Reference schematic use 120uF.

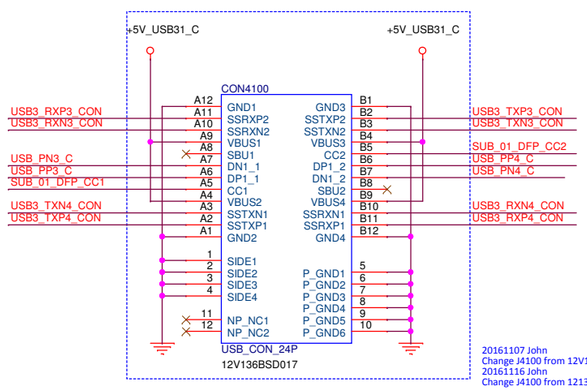


FAULTb pin is an open drain output that assert (active low) when device OUT current exceeds its programmed value and/or over temperature threshold is cressed.



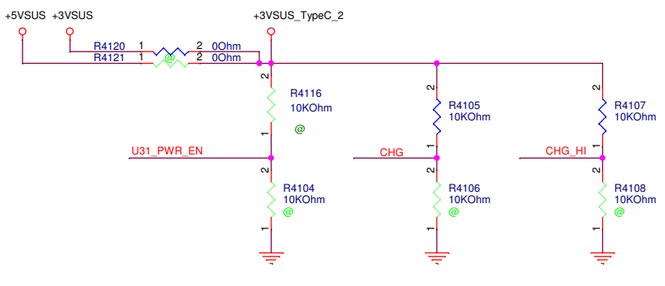






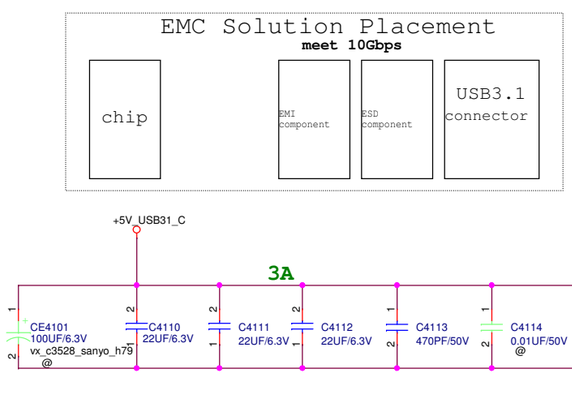
20161107 John
Change J4100 from 12V136BSD015 to 1213-02DG000
20161116 John
Change J4100 from 1213-02DG000 to 12V136BSD017

12V136BSD017



SMT-MS

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1



USB3 Connector(Diff. Z = 85 ohm)

PEGATRON	Title : USB3.1 TPS25810	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1-NB4	Engineer: Kai_Shen	
Size: Custom	Project Name: HE4EA	Rev: 1.0
Date: Friday, April 07, 2017	Sheet 41 of 94	

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Size A	Document Number HE4EA			Rev 1.0
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Size: A	Document Number: HE4EA
Rev: 1.0	
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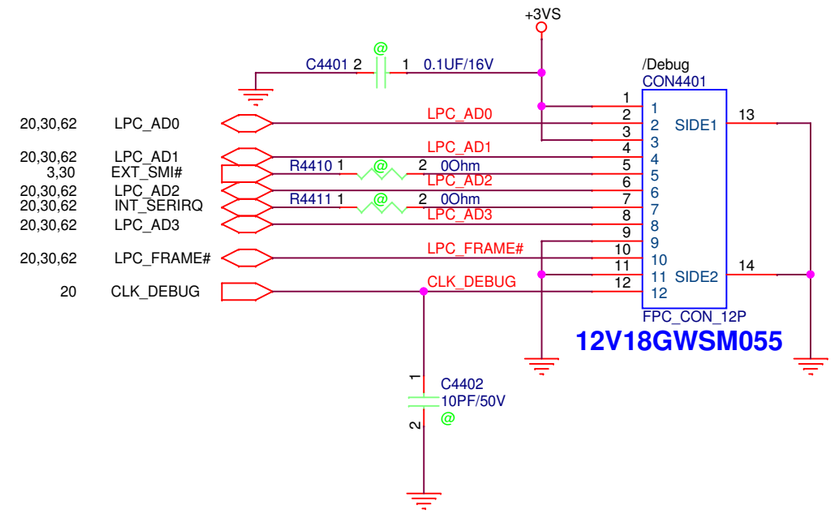
DEBUG CONN

+3VS  +3VS 3,4,20,21,22,23,24,30,31,32,36,41,45,48,49,50,51,53,56



PEGATRON PROPRIETARY AND CONFIDENTIAL

PEGATRON **Title : DEBUG CONN.**

BG1-HW RD **Engineer: *Kai_Shen***

Size	Project Name	Rev
B	**HE4EA**	1.0

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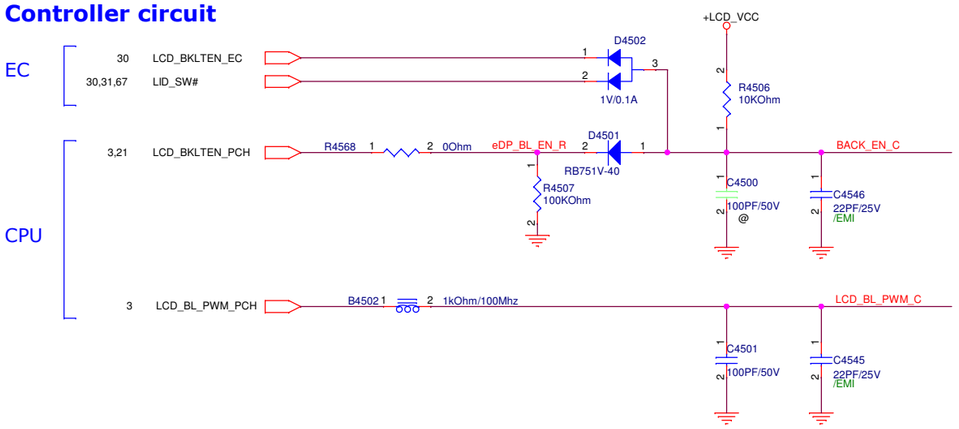
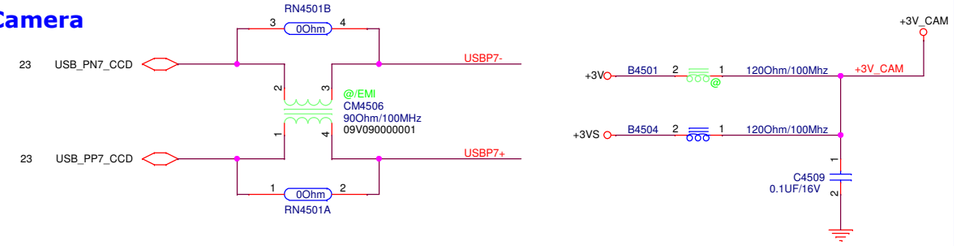
Controller circuit

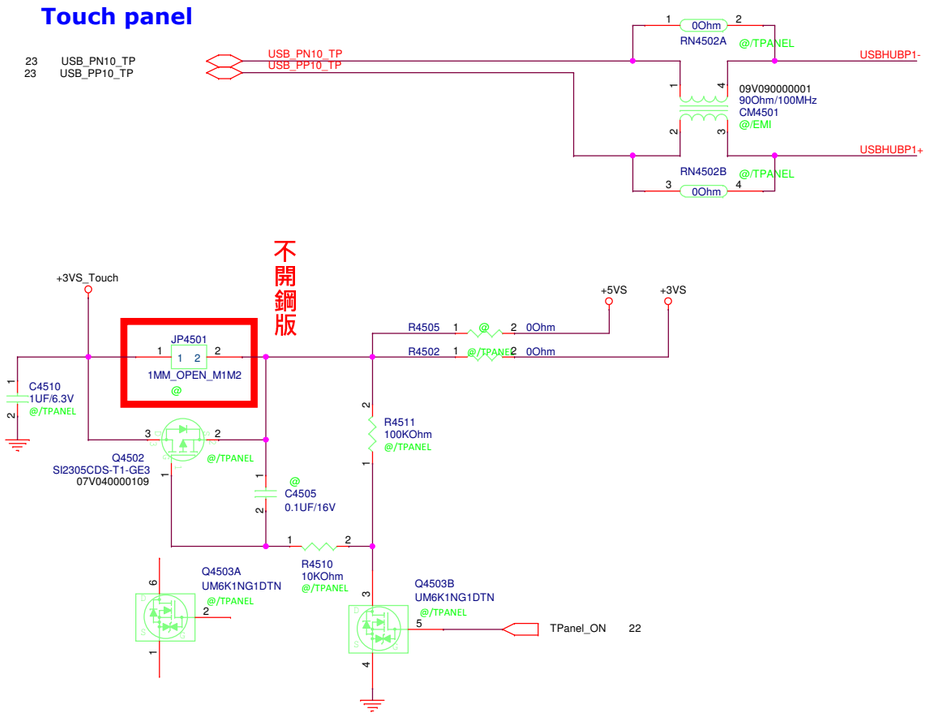


Camera

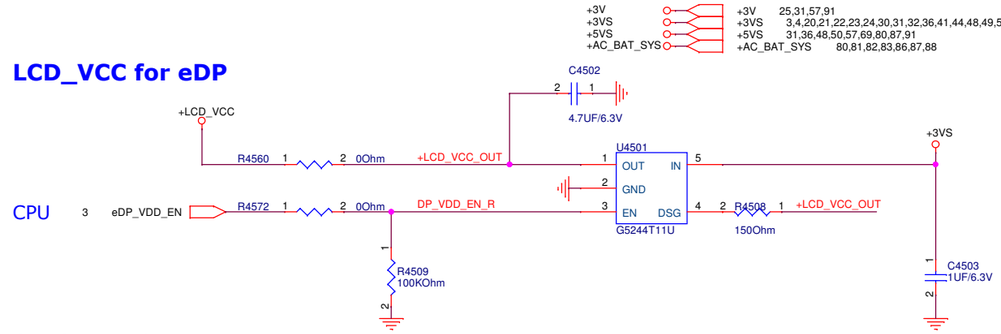


eDP HPD

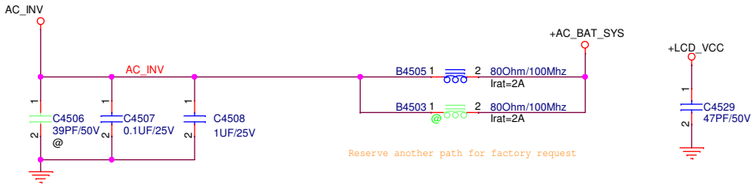
Touch panel



LCD_VCC for eDP

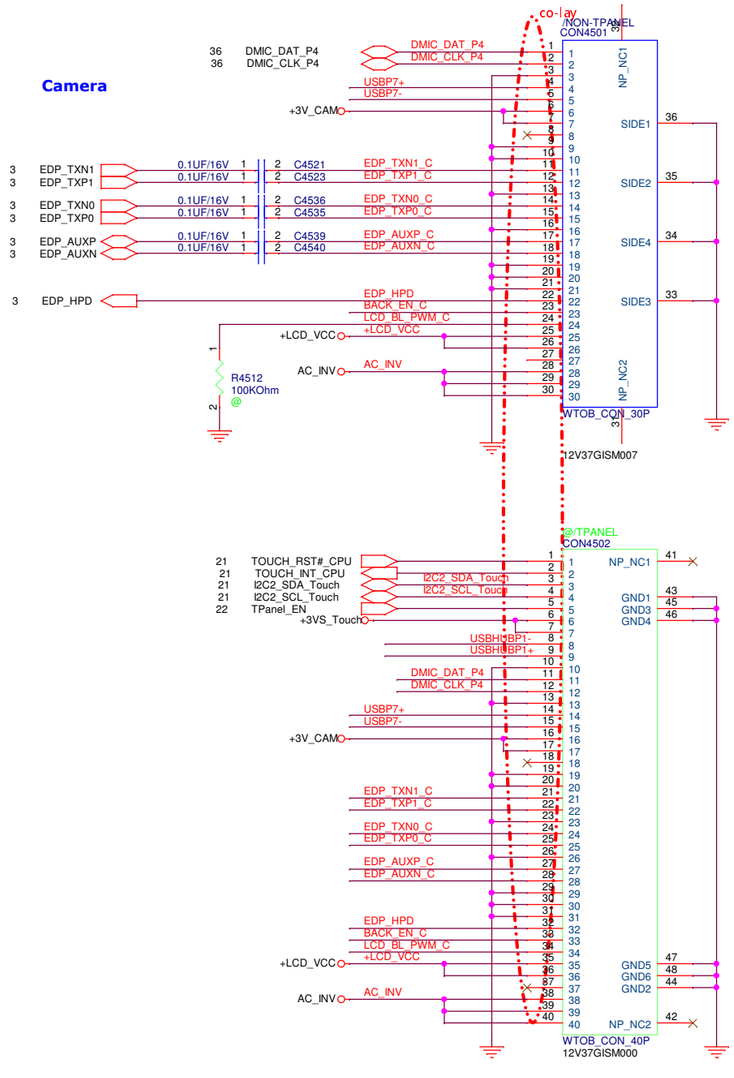


Check PCH/FCH or CPU PD



eDP Connector

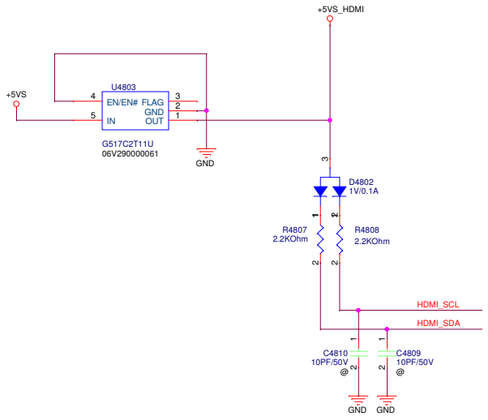
NOTE:
Entire trace of Panel_VCC & LCD_VCC should be wider than 80-mil

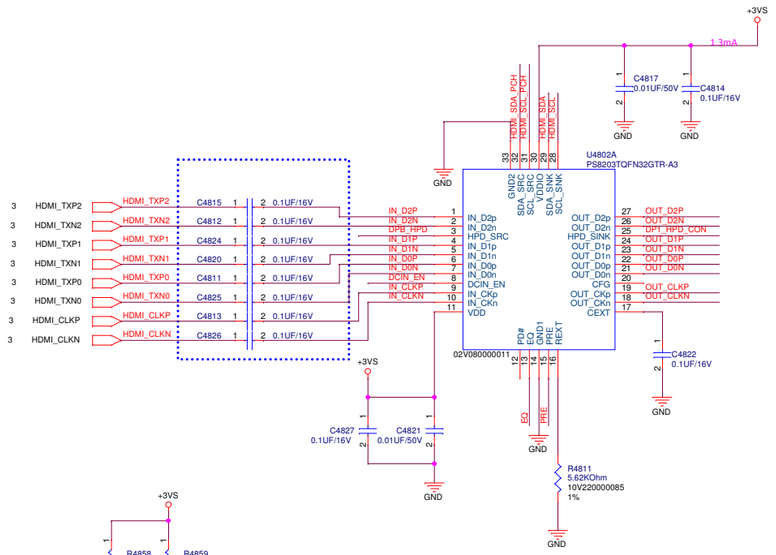


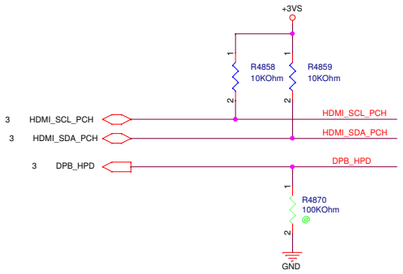
Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 46 of 94

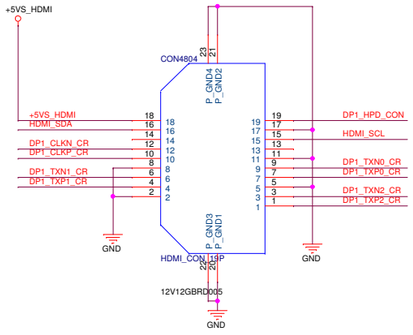
Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 47 of 94

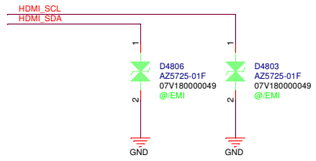
48 HDMI

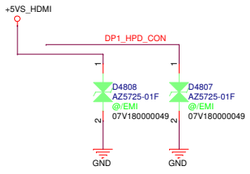


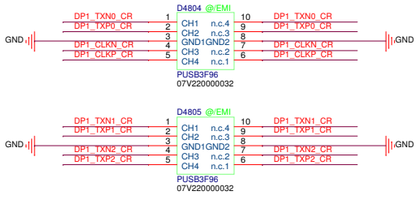








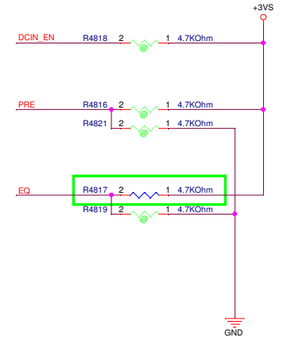


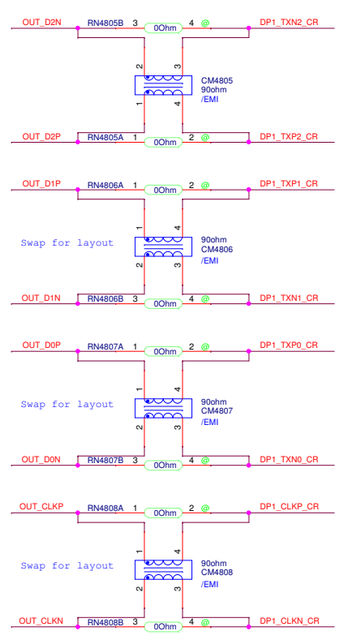



```
Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
   L: no pre-emphasis
   H: 2.5dB pre-emphasis
```

```
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
   L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
   H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
   M: programmable EQ for channel loss up to 8.6dB @ 3Gbps
```

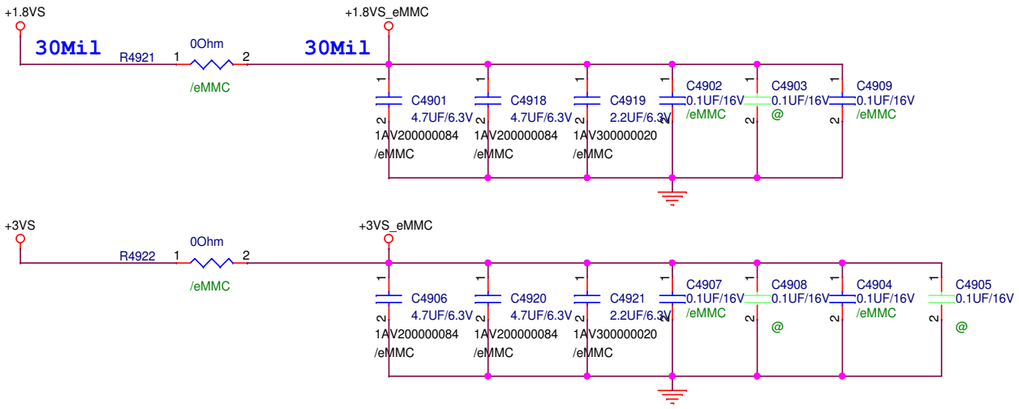
```
DC cou;ing enable; Internal pull down at ~150kΩ, 3.3V I/O.
   L: default, AC coupling input
   H: DC coupling input
```





+3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,49,50,51,53,56,57,62,64,74,87,91,92
+5VS 31,36,45,50,57,69,80,87,91

<Variant Name>
PEGATRON Title : HDMI-4K2K
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD Engineer: Kai_Shen
Size Custom | Project Name HE4EA | Rev 1.0
Date: Friday, April 07, 2017 | Sheet 48 of 94



+1.8VS
+3VS
+12VSUS

+1.8VS 36,57,91
+3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,50,51,53,56,57,62,64,74,87,91,92
+12VSUS 28,81,91

U4901B

A1	NC_1	NC_54	H12
A10	NC_2	NC_55	H13
A11	NC_3	NC_56	H14
A12	NC_4	NC_57	H2
A13	NC_5	NC_58	H3
A14	NC_6	NC_59	J1
A2	NC_7	NC_60	J12
A8	NC_8	NC_61	J13
A9	NC_9	NC_62	J14
B1	NC_10	NC_63	J2
B10	NC_11	NC_64	J3
B11	NC_12	NC_65	K1
B12	NC_13	NC_66	K12
B13	NC_14	NC_67	K13
B14	NC_15	NC_68	K14
B7	NC_16	NC_69	K2
B8	NC_17	NC_70	K3
B9	NC_18	NC_71	L1
C1	NC_19	NC_72	L12
C10	NC_20	NC_73	L13
C11	NC_21	NC_74	L14
C12	NC_22	NC_75	L2
C13	NC_23	NC_76	L3
C14	NC_24	NC_77	M1
C3	NC_25	NC_78	M10
C7	NC_27	NC_79	M11
C8	NC_28	NC_80	M12
C9	NC_29	NC_81	M13
D1	NC_30	NC_82	M14
D12	NC_31	NC_83	M2
D13	NC_32	NC_84	M3
D14	NC_33	NC_85	M7
D2	NC_34	NC_86	M8
D3	NC_35	NC_87	M9
E1	NC_36	NC_88	N1
E12	NC_37	NC_89	N10
E13	NC_38	NC_90	N11
E14	NC_39	NC_91	N12
E2	NC_40	NC_92	N13
E3	NC_41	NC_93	N14
F1	NC_42	NC_94	N3
F12	NC_43	NC_95	N6
F13	NC_44	NC_96	N7
F14	NC_45	NC_97	N8
F2	NC_46	NC_98	N9
F3	NC_47	NC_99	P1
G1	NC_48	NC_100	P11
G12	NC_49	NC_101	P12
G13	NC_50	NC_102	P13
G14	NC_51	NC_103	P14
G2	NC_52	NC_104	P2
H1	NC_53	NC_105	P8
		NC_106	P9

THGBMGG9T4LBAIR
05V000000095
/eMMC

24 eMMC_CLK
C4911 22PF/50V @

24 eMMC_CMD
24 eMMC_D0
24 eMMC_D1
24 eMMC_D2
24 eMMC_D3
24 eMMC_D4
24 eMMC_D5
24 eMMC_D6
24 eMMC_D7

R4902 1 /eMMC 2 0Ohm eMMC_CLK_R M6
R4901 1 /eMMC 2 0Ohm eMMC_CMD_R M5
R4903 1 /eMMC 2 0Ohm eMMC_D0_R A3
R4904 1 /eMMC 2 0Ohm eMMC_D1_R A4
R4905 1 /eMMC 2 0Ohm eMMC_D2_R A5
R4906 1 /eMMC 2 0Ohm eMMC_D3_R B2
R4907 1 /eMMC 2 0Ohm eMMC_D4_R B3
R4908 1 /eMMC 2 0Ohm eMMC_D5_R B4
R4909 1 /eMMC 2 0Ohm eMMC_D6_R B5
R4910 1 /eMMC 2 0Ohm eMMC_D7_R B6

@ TPC28T T4901 1
@ TPC28T T4902 1
@ TPC28T T4903 1
@ TPC28T T4904 1

24 eMMC_RCLK
R4920 1 /eMMC 2 0Ohm eMMC_RCLK_R

U4901A

CLK	M6	NC/index	D4
CMD	M5		
DAT0	A3	VssQ_1	C4
DAT1	A4	VssQ_2	N2
DAT2	A5	VssQ_3	N5
DAT3	B2	VssQ_4	P4
DAT4	B3	VssQ_5	P6
DAT5	B4	VccQ_5	P5
DAT6	B5	VccQ_4	P3
DAT7	B6	VccQ_3	N4
		VccQ_2	M4
Vss_1	A6	VccQ_1	C6
RFU_1	A7	VDDi	C2
NC_26	C5		
VSF_1	E10	Vss_2	E7
RFU_2	E5	Vss_3	G5
RFU_3	E8	Vss_4	H10
VSF_2	E9	Vss_6	K8
VSF_3	F10		
RFU_4	G10	Vcc_4	K9
RFU_5	G3	Vcc_3	J10
DS	H5	Vcc_2	F5
Vss_5	J5	Vcc_1	E6
RFU_6	K10		
RFU_7	K6	RST_n	K5
RFU_8	K7		
RFU_9	P10		
RFU_10	P7		

THGBMGG9T4LBAIR
05V000000095
/eMMC

+1.8VS_eMMC
0.1UF/6.3V 1 2 C4915
/eMMC_SAN
1UF/6.3V 1 2 C4910
@/eMMC_HY
+3VS_eMMC
EMMC_RST

+12VSUS
+1.8VS_eMMC
R4933 100KOhm /eMMC
R4934 10KOhm /eMMC
R4911 1 /eMMC 2 0Ohm EMMC_RST
Q4902B UM6K1NG1DTN /eMMC
Q4902A UM6K1NG1DTN /eMMC
C4913 0.1UF/16V @
25,30,32,51,53,62,70 BUF_PLT_RST#

+1.8VS_eMMC
eMMC_D0 R4923 1 /eMMC 2 20KOhm
eMMC_D1 R4924 1 /eMMC 2 20KOhm
eMMC_D2 R4925 1 /eMMC 2 20KOhm
eMMC_D3 R4926 1 /eMMC 2 20KOhm
eMMC_D4 R4927 1 /eMMC 2 20KOhm
eMMC_D5 R4928 1 /eMMC 2 20KOhm
eMMC_D6 R4929 1 /eMMC 2 20KOhm
eMMC_D7 R4930 1 /eMMC 2 20KOhm
eMMC_CMD R4932 1 /eMMC 2 20KOhm
eMMC_CLK R4936 1 /eMMC 2 20KOhm
eMMC_RCLK R4937 1 /eMMC 2 20KOhm

<Variant Name>

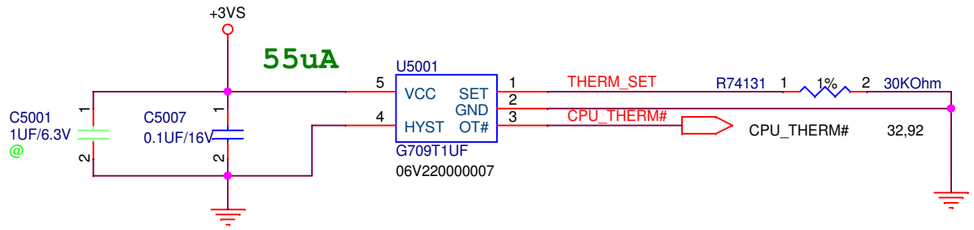
PEGATRON Title : eMMC
BG1-HW3 RD Engineer: Kai_Shen
Size: Custom | Project Name: HE4EA | Rev: 1.0
Date: Friday, April 07, 2017 Sheet 49 of 94

50 Thermal_Fan

G709 Thermal Sensor

+3VS
+5VS

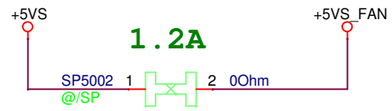
+3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,51,53,56,57,62,64,74,87,91,92
+5VS 31,36,45,48,57,69,80,87,91

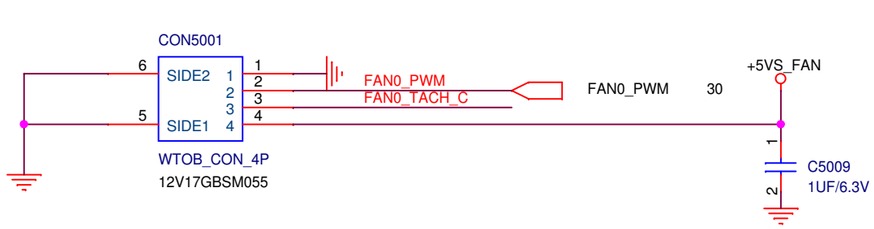


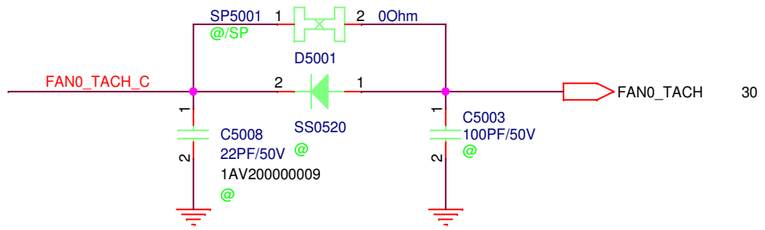
temp setting : 80 degree

RSET(kΩ)= 0.0012T2 – 0.9308T + 96.147

PWM FAN







PEGATRON Title : Thermal_Fan

BG1-HW RD Engineer: Kai_Shen

Size	Project Name	Rev
B	HE4EA	1.0

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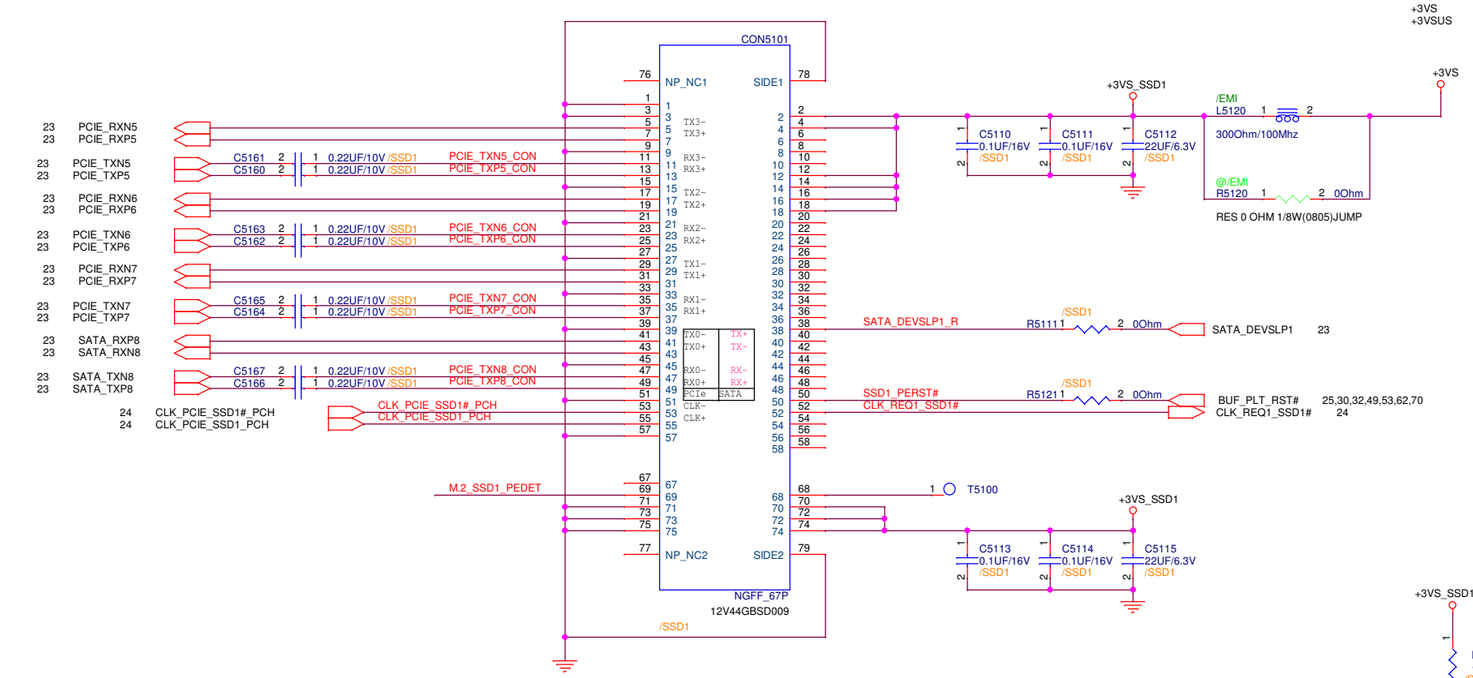
51

SSD1



+3VS
+3VSUS

+3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,53,56,57,62,64,74,87,91,92
+3VSUS 4,20,21,22,23,24,25,26,28,30,31,41,53,62,74,81,92

SSD type detection		
Interface	**Device side**	**PCH side**
PCIe	Hi-z	H
SATA	L	L
NO SSD	Hi-z	H

PCIe_M.2_Electromechanical_Spec_Rev_0.9-3_07312013_RS_Clean

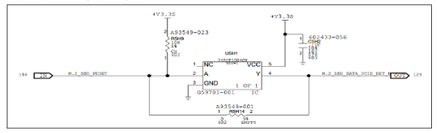
Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes					
CONFIG_0 (Pin 21)	**CONFIG_1 (Pin 69)**	**CONFIG_2 (Pin 75)**	**CONFIG_3 (Pin 1)**	**Module Type and Main Host Interface[1]**	**Port Configuration[2]**
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

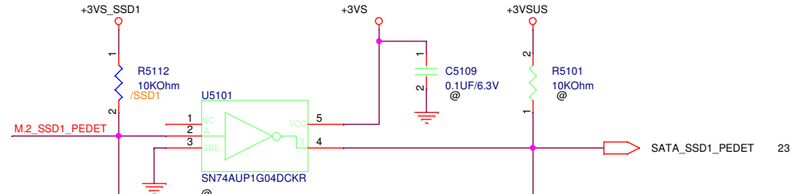
36.3.2.3 PEDET Guidelines

PEDET is the interface detect used by PCH to determine the communication protocol that the M.2 card uses; PCIe* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

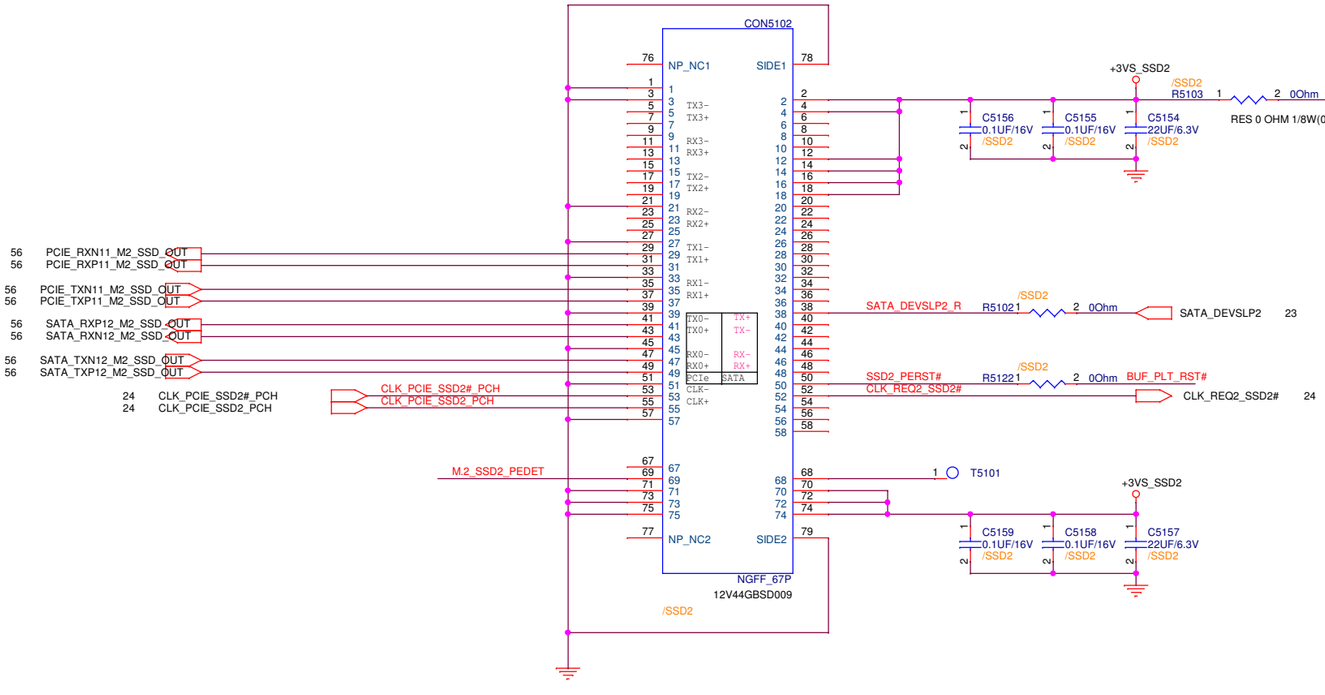
Figure 36-6. PEDET Circuitry Example

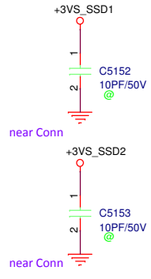


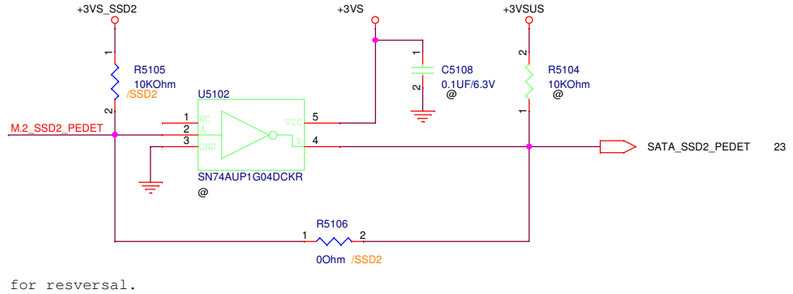
For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the M.2 device.



SSD2







Reserve for resversal.
If BIOS can set resversal, unmount these parts.

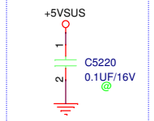
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: SATA SSD_HDD
BG1-HW3 RD
Engineer: Kai_Shen

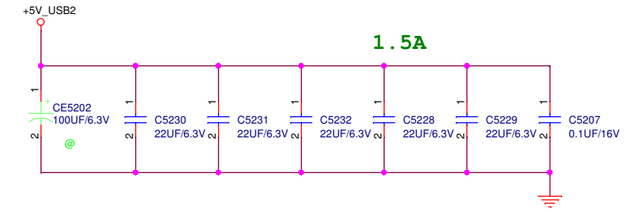
Size	Project Name	Rev
C	HE4EA	1.0

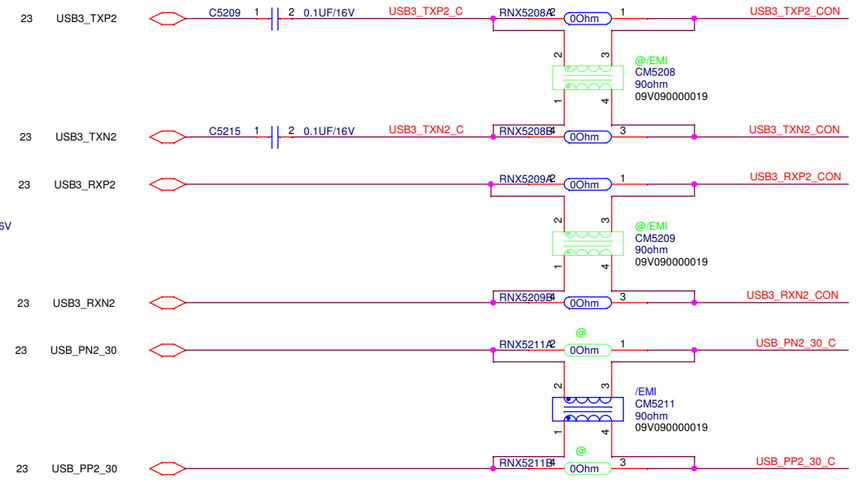
Date: Friday, April 07, 2017 Sheet 51 of 94

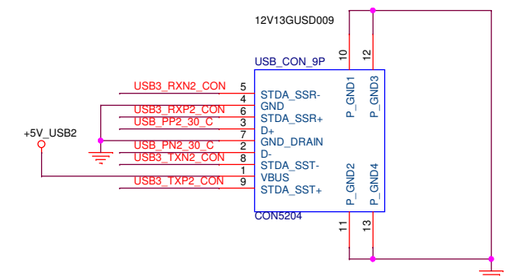
52 USB3.0

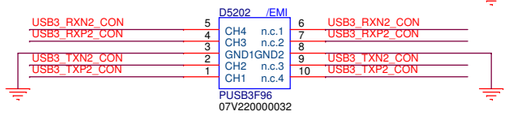
EMI 2016/03/17



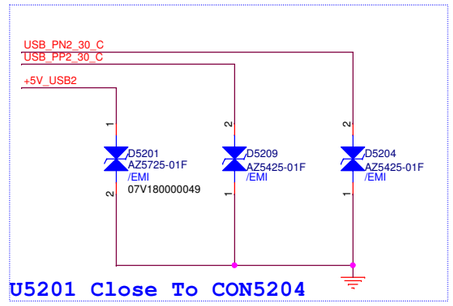








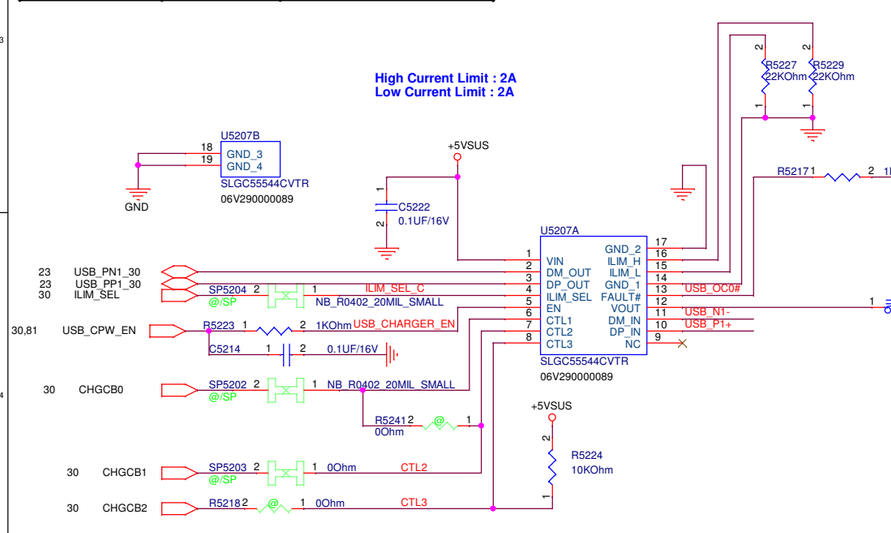
PLACE ESD Diodes near USB Connector

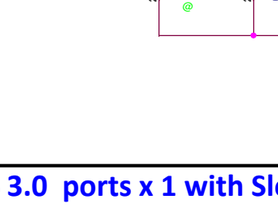


USB 3.0 ports x 1 with Sleep & Charge Left_Down

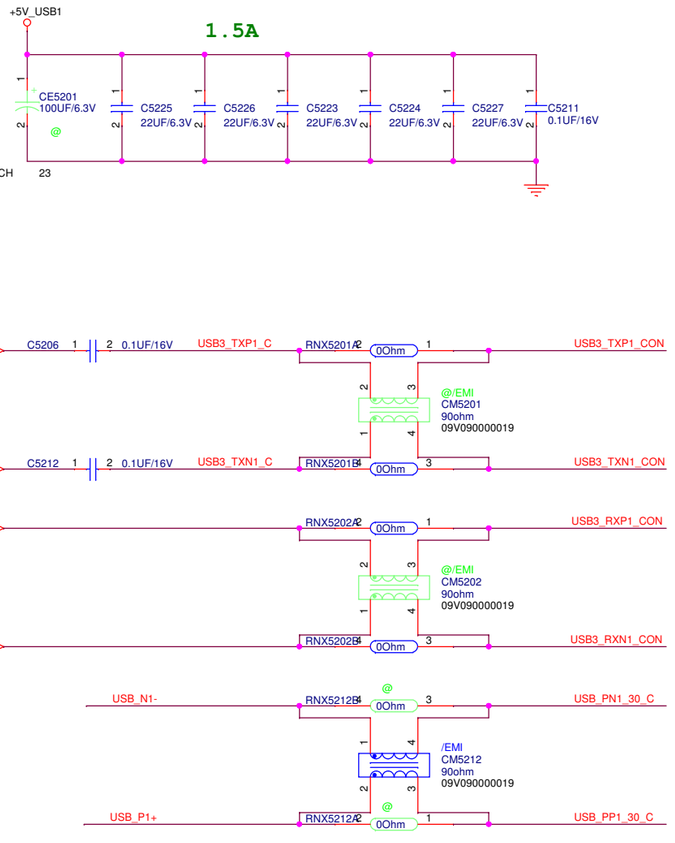
Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)

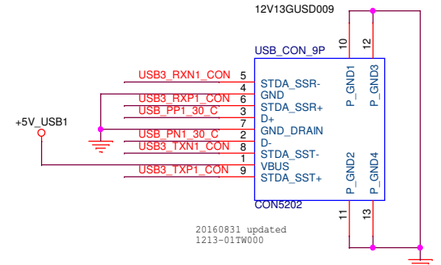
High Current Limit : 2A
Low Current Limit : 2A



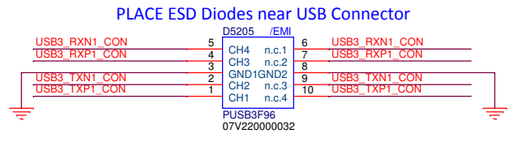


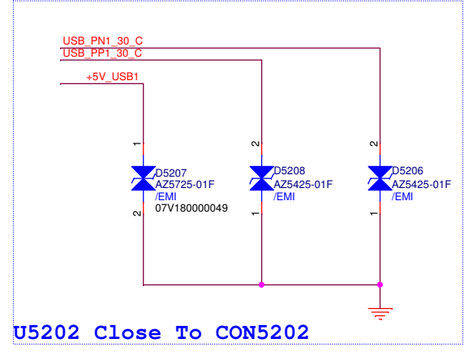
System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO





PLACE ESD Diodes near USB Connector





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

Title: USB3.0_Charge IC
Engineer: Kai_Shen

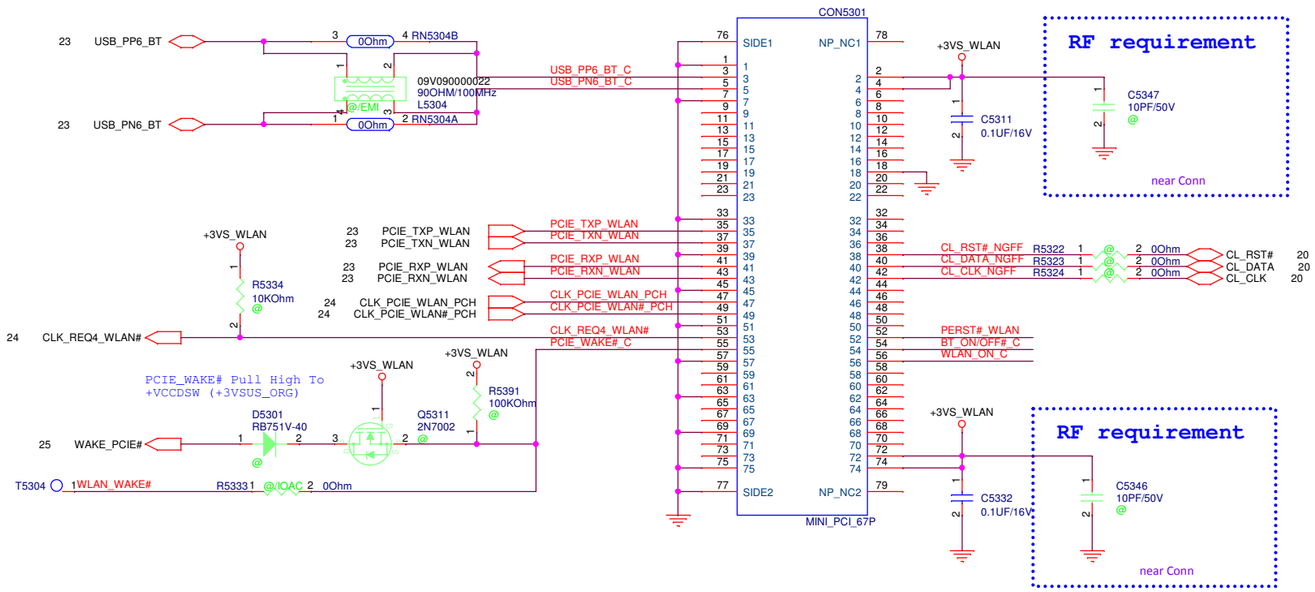
Size	Project Name	Rev
C	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 52 of 94

53 PCIE_WLAN_BT

+3VS
+3VSUS
+3VA

+3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,56,57,62,64,74,87,91,92
+3VSUS 4,20,21,22,23,24,25,26,28,30,31,41,51,62,74,81,92
+3VA 24,28,30,31,36,57,67,81,88,93

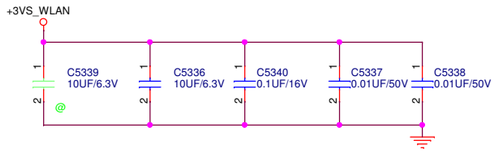


WLAN/BT with NGFF socket E

+3V_WLAN_WP1 bypass capactor:

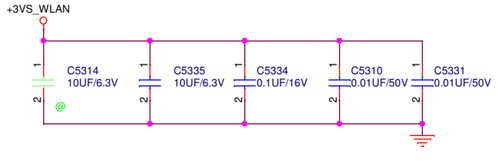
Place 0.1UF near pin 2,4

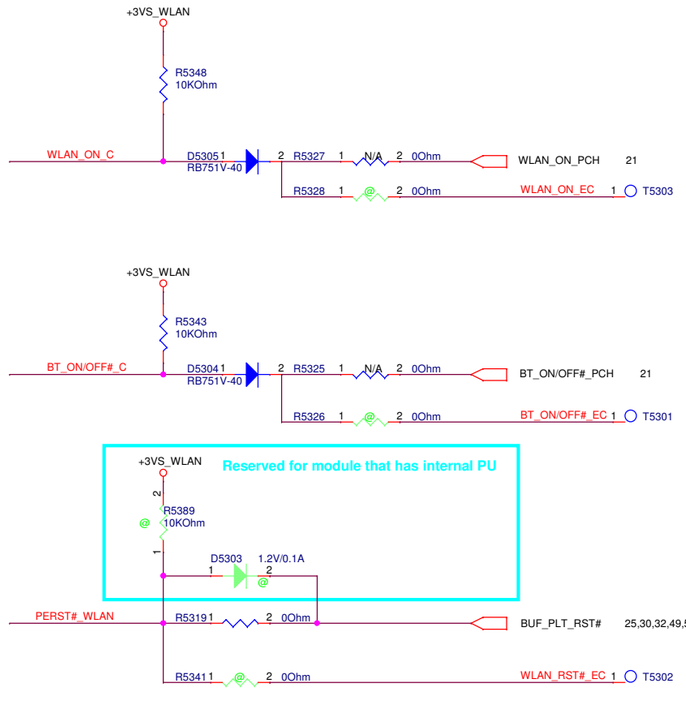
Place 10UF near +3V_WLAN_WP1 source side.

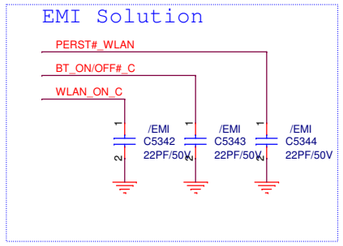


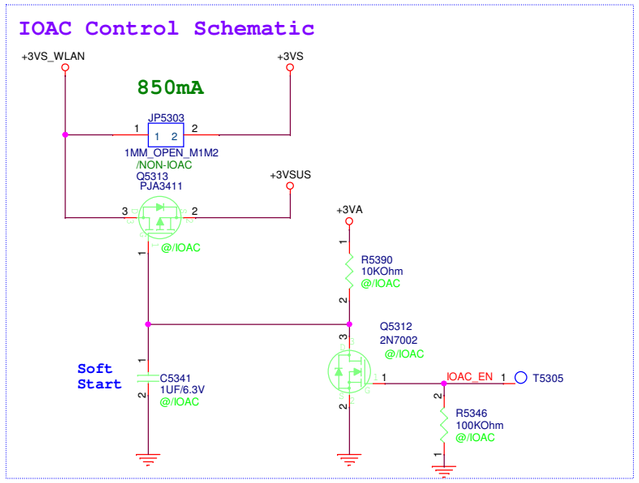
Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.









PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD

Title : PCIE_WLAN_BT
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 53 of 94

Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 54 of 94

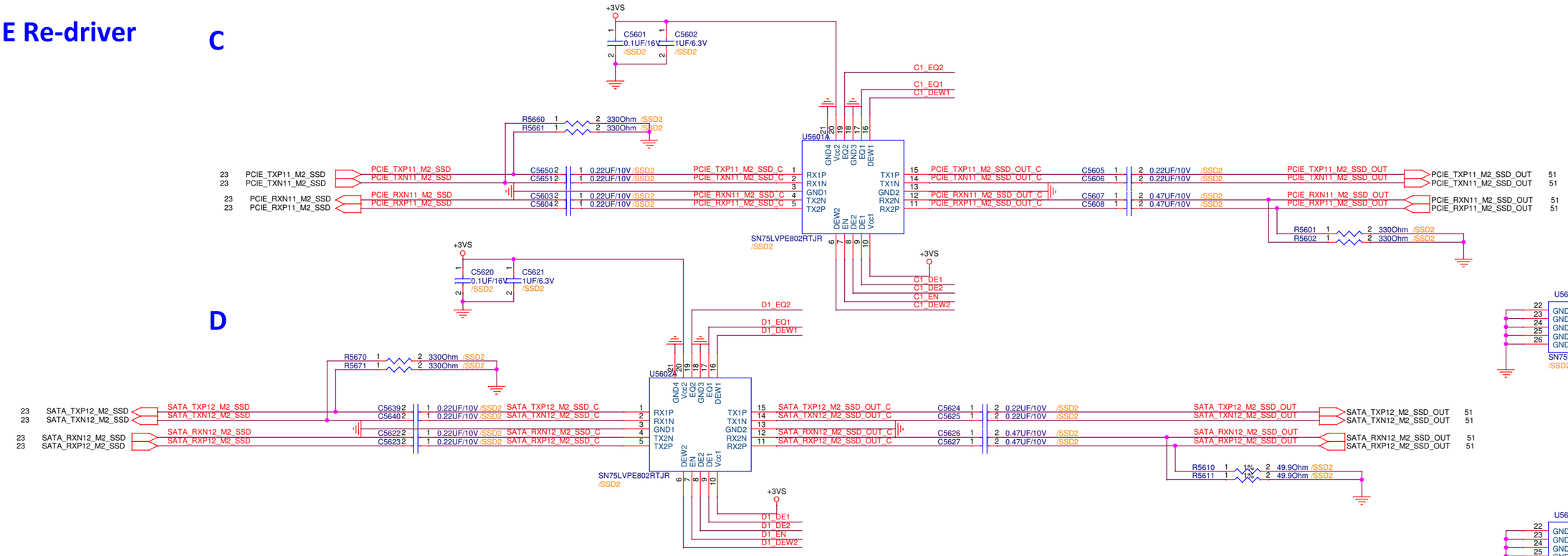
Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 55 of 94

+3VS +3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,5

PCIE Re-driver

C

D

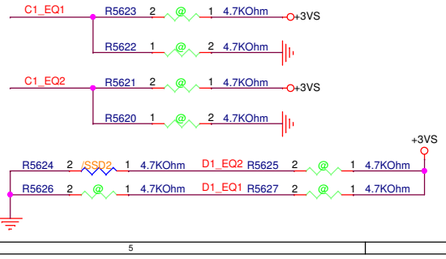


!!-R5602 Using TI's new source, imported by PN substitution, R12 should use right way to import when VX and symbol application is done

Equalizer control

EQ1 / EQ2	Channel 1 / Channel 2
NC	0 dB (Default)
H	7 dB
L	14 dB

Internally biased to VCC / 2 with >200-Ωk pullup or ulldown.
When 3-state pins are left as NC, board leakage at the pin pad must be <1 µA; otherwise, drive to VCC / 2 to assert mid-level



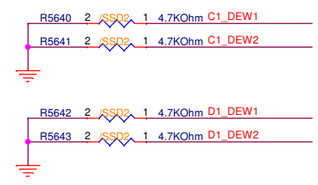
De-Emphasis setting

DE1 / DE2	Channel 1 / Channel 2
NC	-4 dB (Default)
H	0 dB
L	-2 dB

Internally biased to VCC / 2 with >200-Ωk pullup or ulldown.
When 3-state pins are left as NC, board leakage at the pin pad must be <1 µA; otherwise, drive to VCC / 2 to assert mid-level

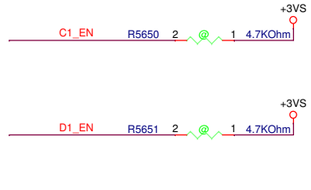
De-Emphasis width control

DEW1 or DEW2	Channel 1	Channel 2
H	De-emphasis plse duration, Long (Default)	
L	De-emphasis plse duration, Sfort	



Device enable

EN	Device
H	Device enabled (Default)
L	Device in standby mode



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

Title: SATA SSD_HDD
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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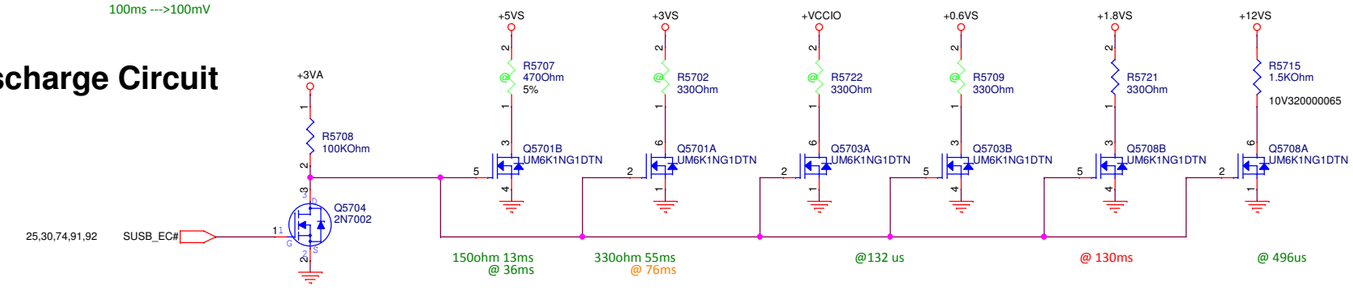
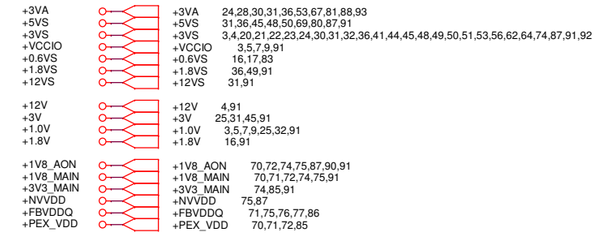
DISCHARGE

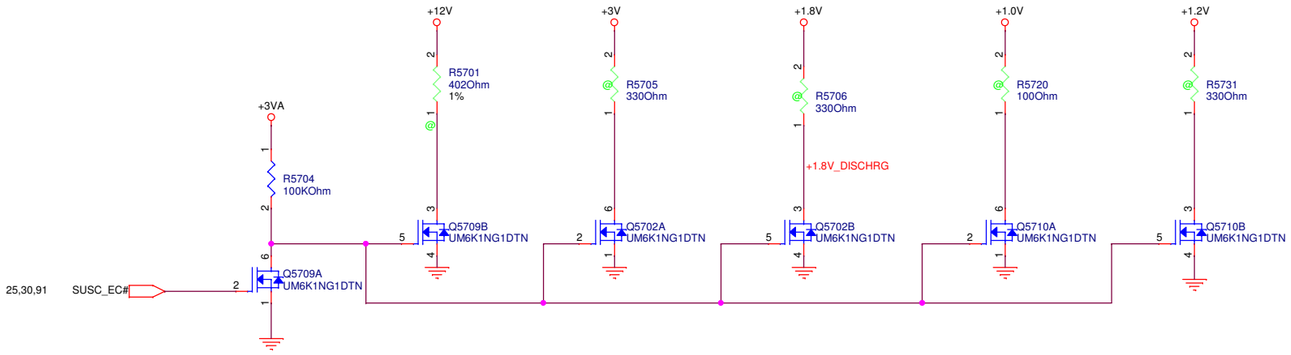
0402 1/16W min. resister
5V 400 OHM
3V 144 OHM
12V 2304 OHN

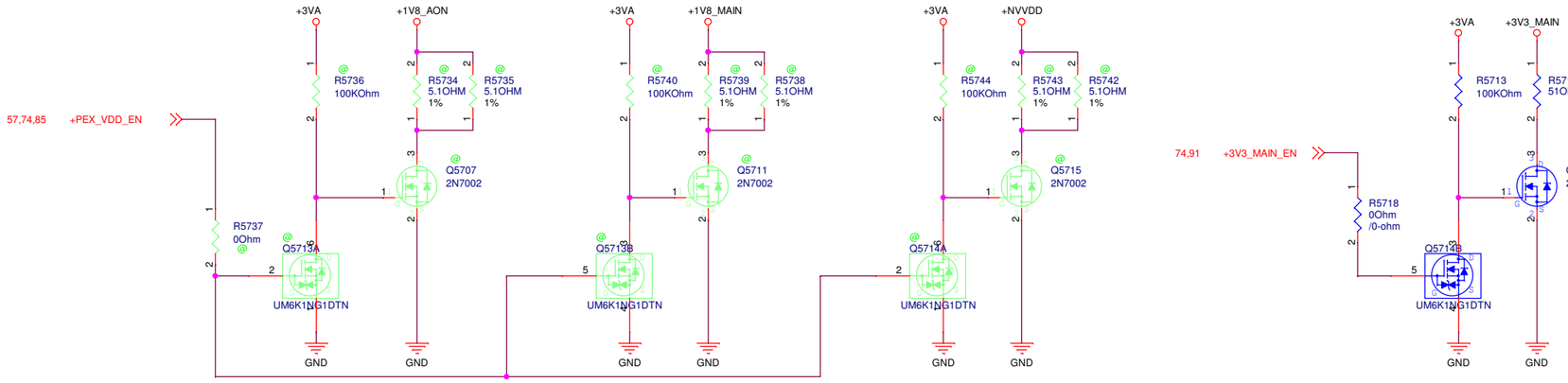
100ms --->100mV

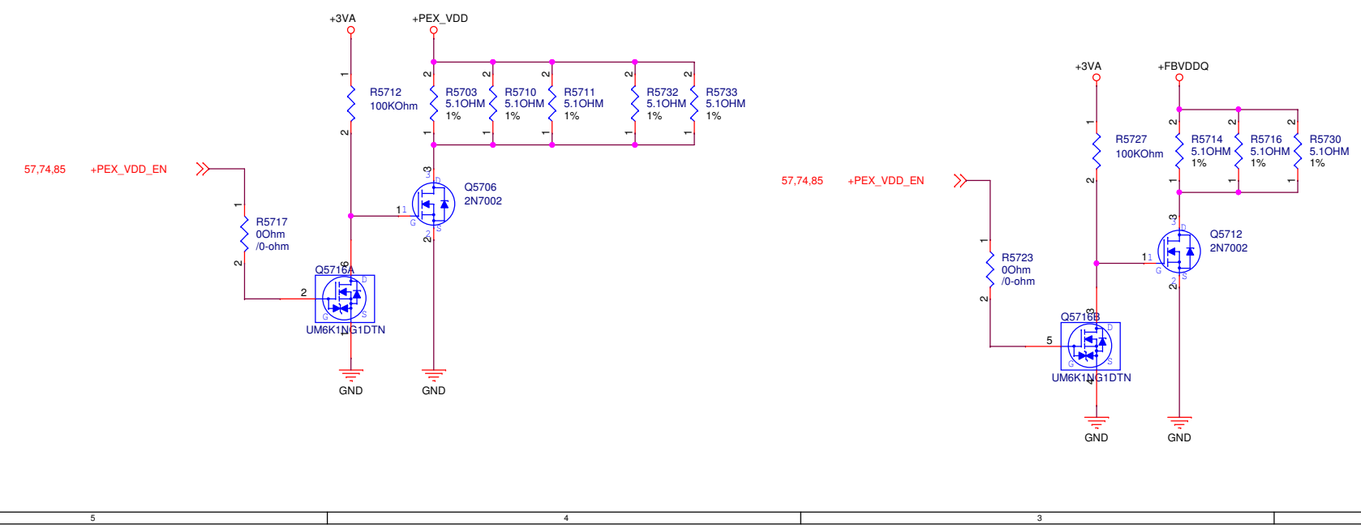
Discharge Circuit











PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW RD

Title : DISCHARGE
Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 58 of 94

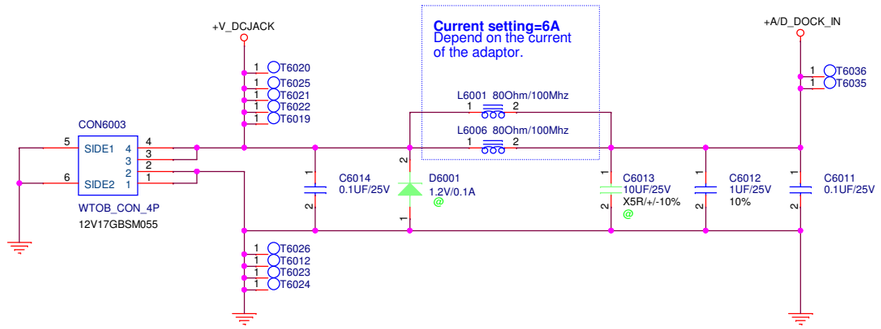
Title	<Title>
Size: A	Document Number: HE4EA
Rev: 1.0	
Date: Wednesday, March 29, 2017	Sheet 59 of 94

60 DC_BAT_CONN

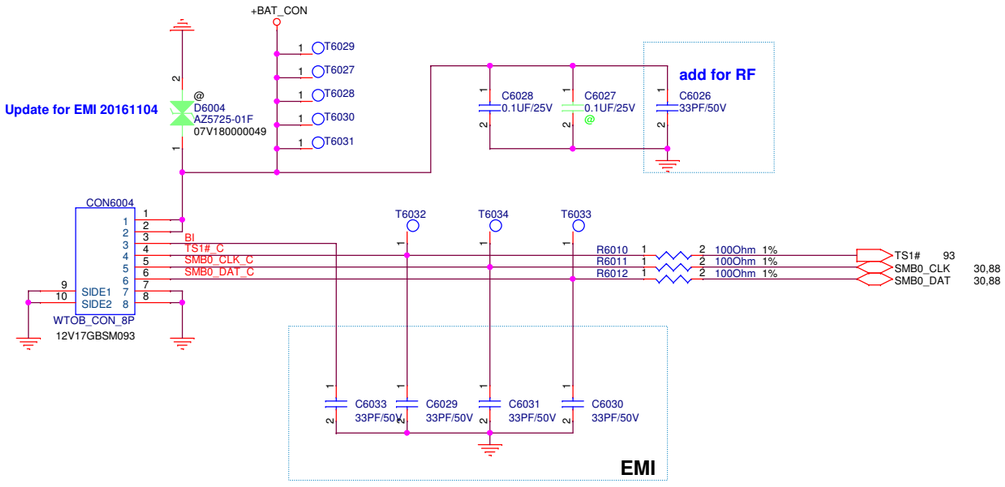
+A/D_DOCK_IN
+BAT_CON
+VCC_RTC

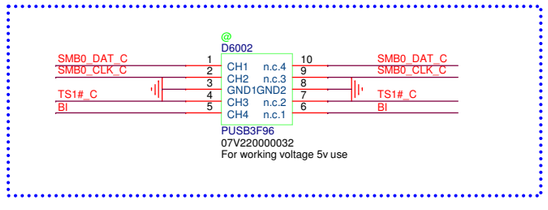
+A/D_DOCK_IN 88
+BAT_CON 88
+VCC_RTC 24,25,26,36

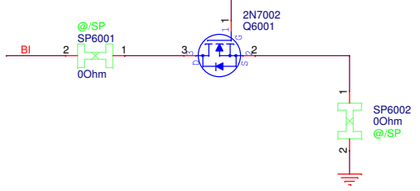
DC Jack WTB CONN

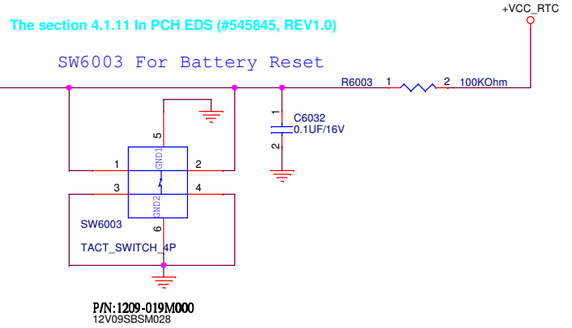


Battery Connector









PEGATRON Title : DC_BAT_CONN
BG1-HW RD Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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Title	<Title>	
Size: A	Document Number: HE4EA	Rev: 1.0
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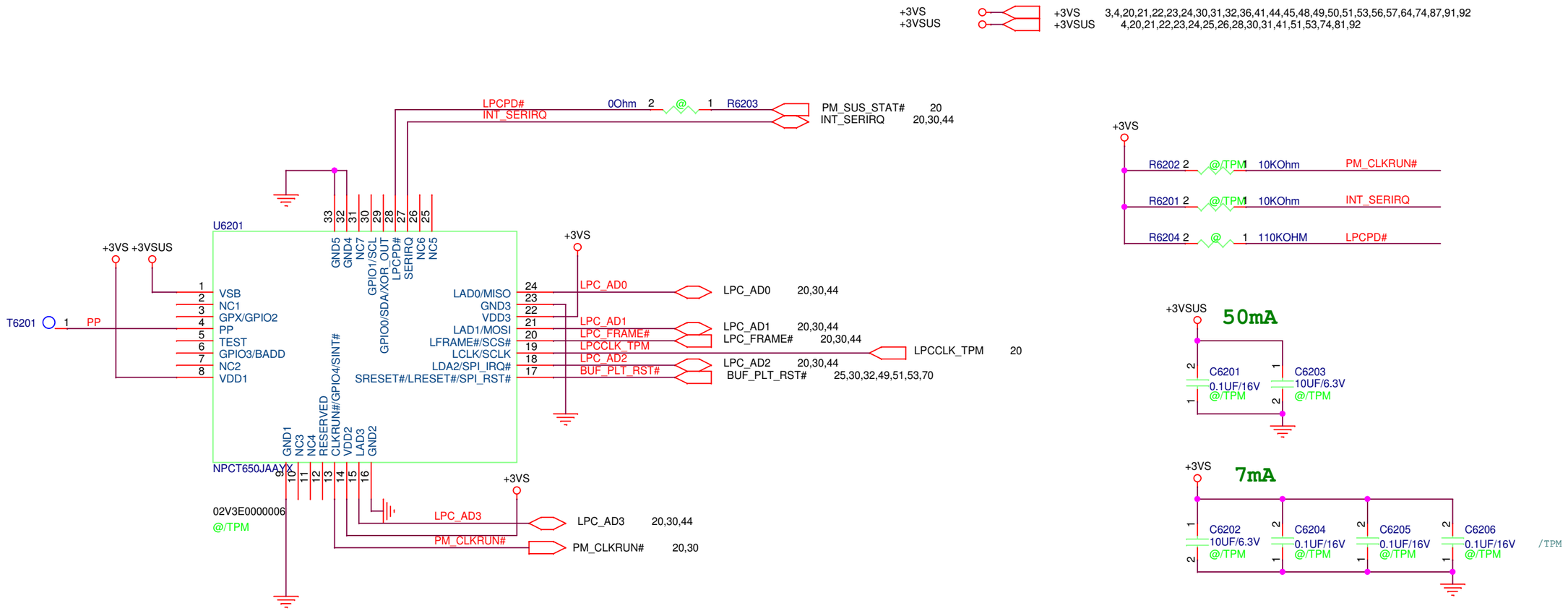
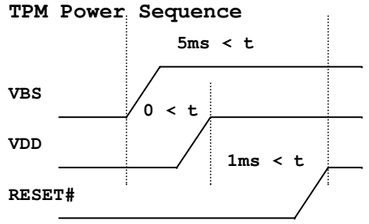
TPM NPCT650



TPM VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

TPM Power Sequence



NOTE: RESET# is LRESET#, SPI_RST# or SRESET#.

NOTE:
1) For TPM 1.2:
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
2) For TPM 2.0:
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
4) RESET# must be asserted for at least 5 msec after VSB power-up.
5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

PEGATRON	Title : TPM NPCT650	
BG1-HW RD	Engineer: Kai_Shen	
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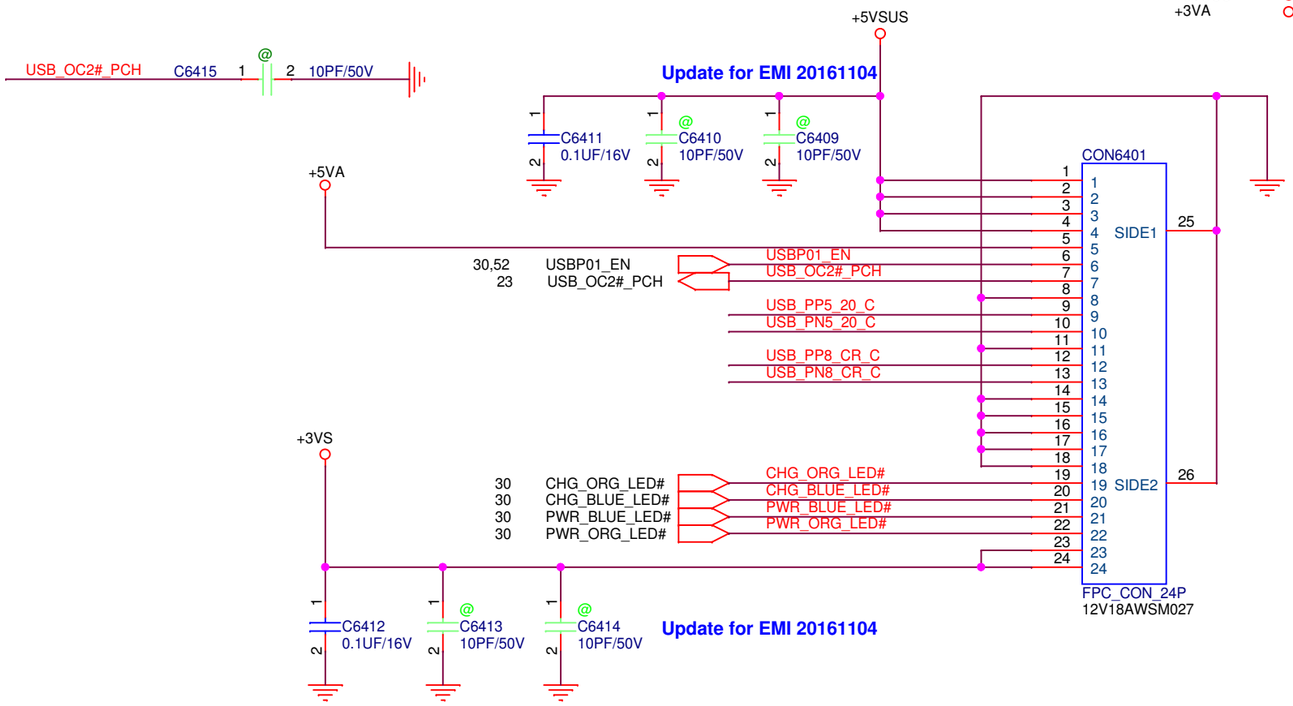
64 DB CONN

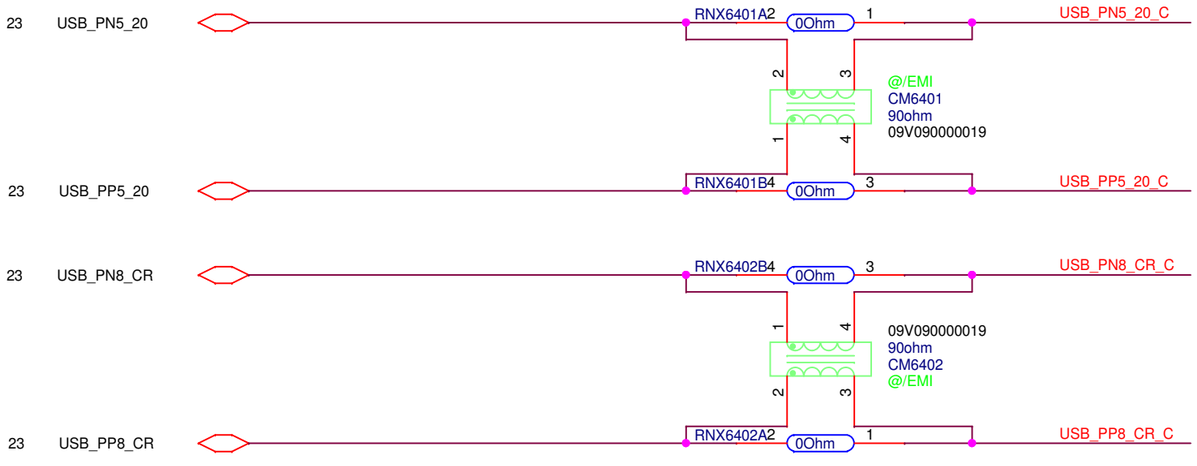
+3VS
+5VSUS
+3VA

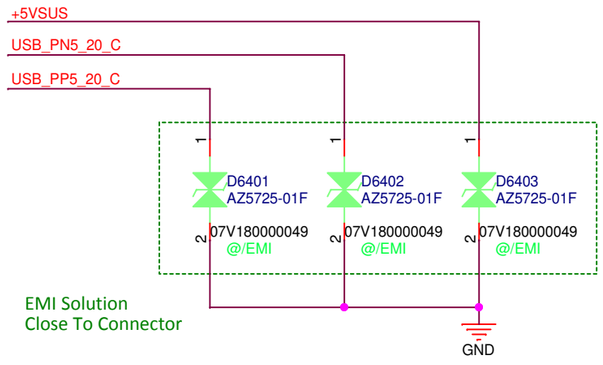
+3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,74,87,91,92
+5VSUS 41,52,81
+3VA 24,28,30,31,36,53,57,67,81,88,93



DB Connector Pin Define(MB Side)

1		+5VSUS
2		+5VSUS
3		+5VSUS
4		+5VSUS
5		+5VA
6		USB_EN
7		USB_OC
8	GND_IO	
9		USB_PP1_20
10		USB_PN1_20
11	GND_IO	
12		USB_PP2_20
13		USB_PN2_20
14	GND_IO	
15	GND_IO	
16	GND_IO	
17	GND_IO	
18	GND_IO	
19		CHG_ORG_LED#
20		CHG_BLUE_LED#
21		PWR_BLUE_LED#
22		PWR_ORG_LED#
23		+3VS
24		+3VS





PEGATRON Title : IO Board
BG1-HW3 RD Engineer: Kai_Shen

Size	Project Name	Rev
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Title <Title>		
Size A	Document Number HE4EA	Rev 1.0
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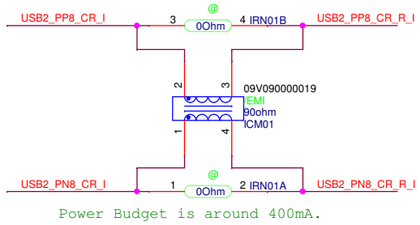
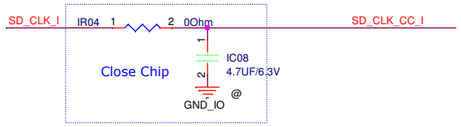
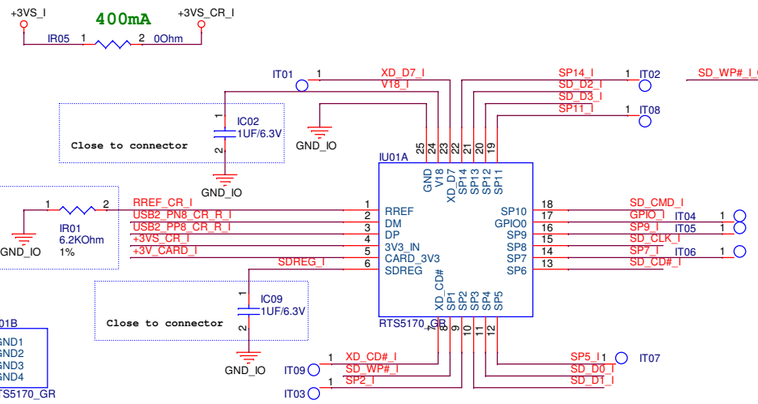
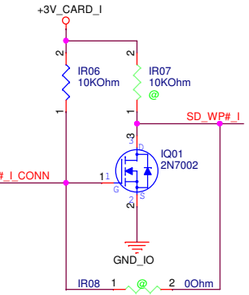
66 IO Board

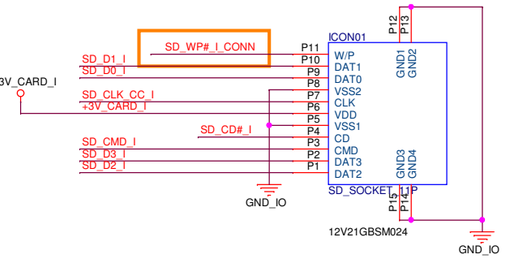
Card Reader

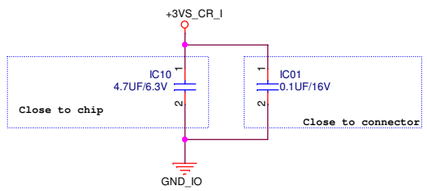


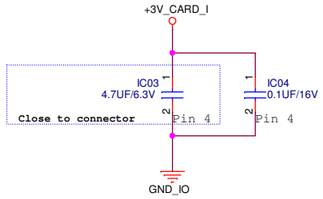


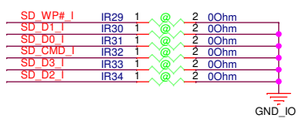


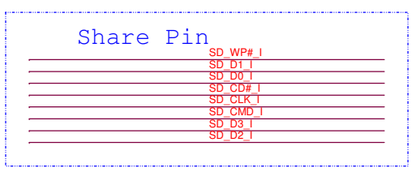




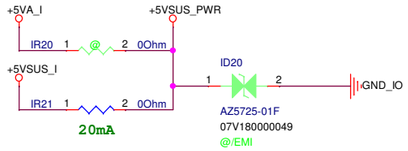




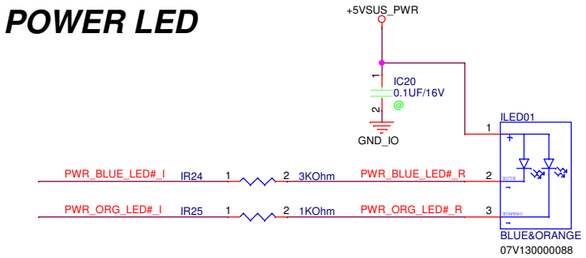




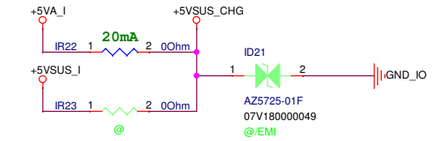
POWER LED



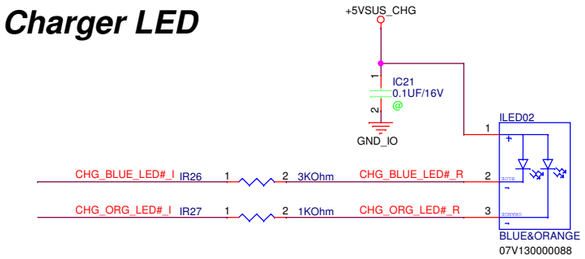
POWER LED

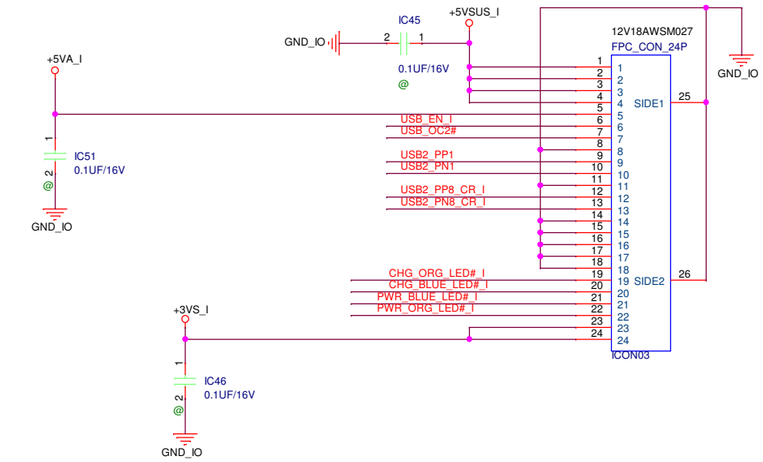


Charger LED

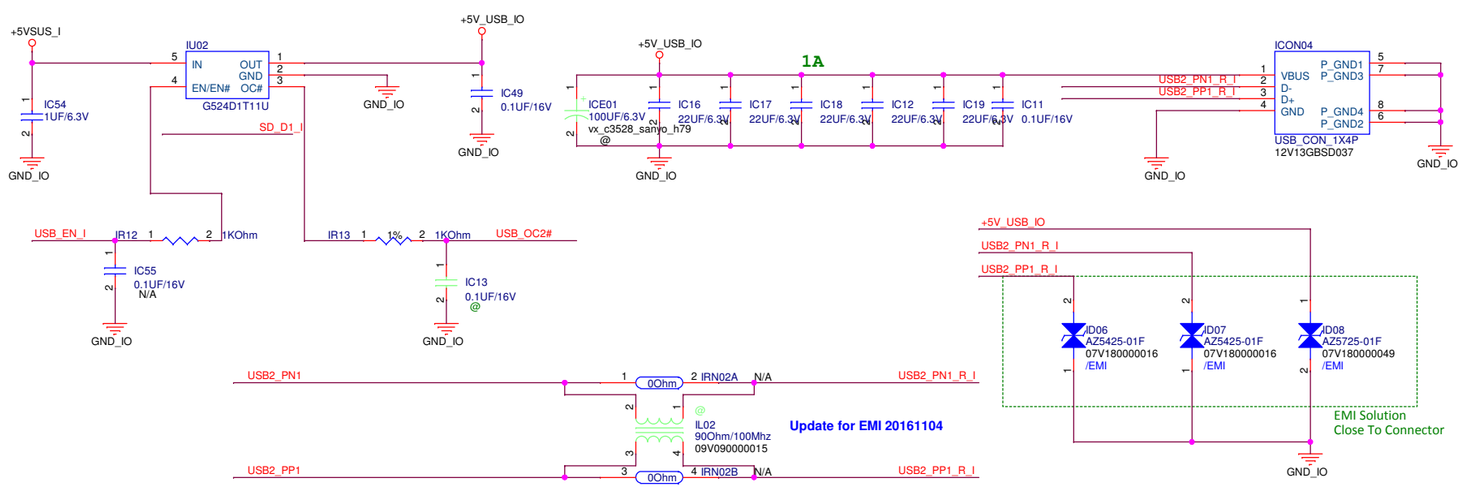


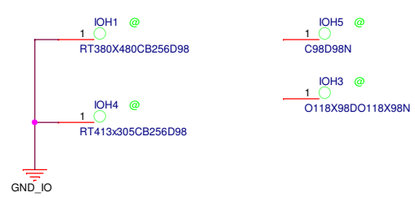
Charger LED





USB 2.0





1213-017L000

PEGATRON Title : IO Board

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Kai_Shen

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C	HE4EA	1.0

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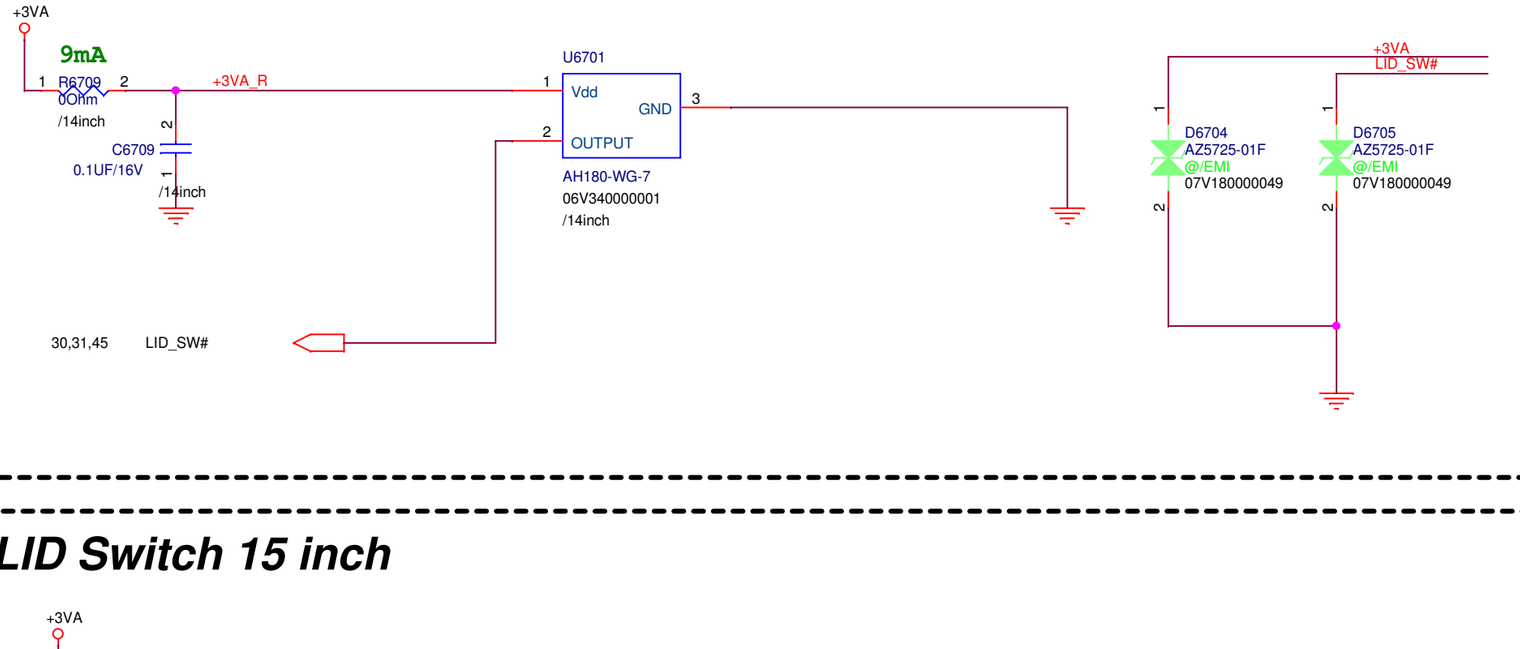
+3VA +3VA 24,28,30,31,36,53,57,81,88,93

LID Switch 14 inch



LID Switch 15 inch

PEGATRON Title : Sensor Board

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RD Engineer: Kai_Shen

Size	Project Name	Rev
B	HE4EA	1.0

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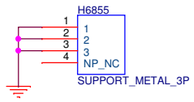
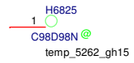
68 ME Hole

靠近M.2 CONN

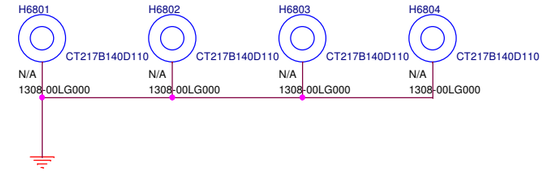


鎖IOPORT SHIELDING螺絲孔

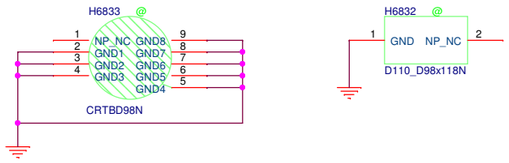
2.5X3.0 橢圓孔



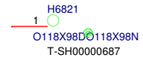
CPU NUT



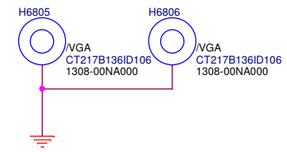
Main shielding 定位孔



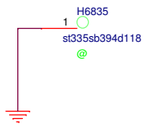
2.5 圓孔



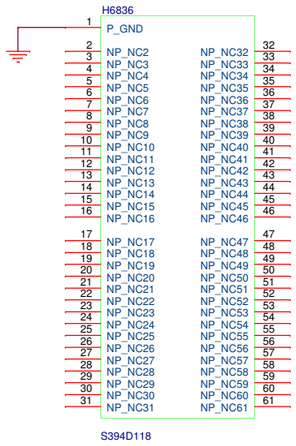
GPU NUT



Audio Jack下孔

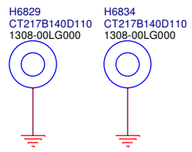


斷熱孔

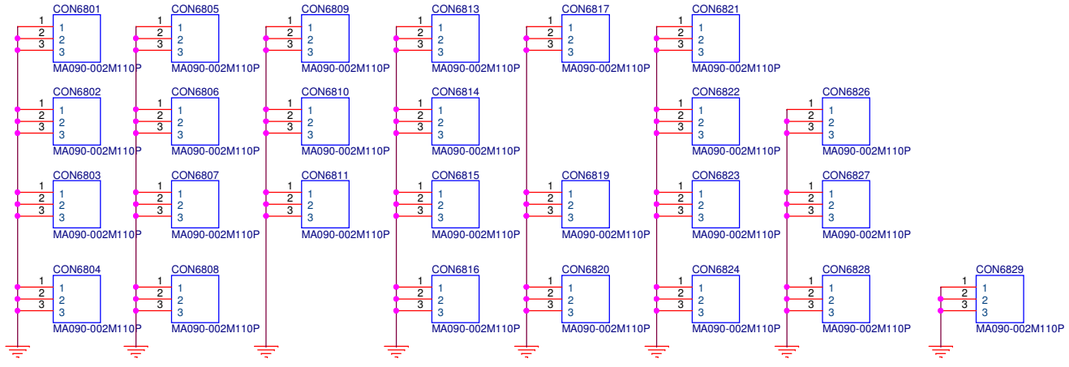


主板PTH孔

Main Shielding NUT



Clip



PEGATRON Title : ME Hole

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW RD

Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

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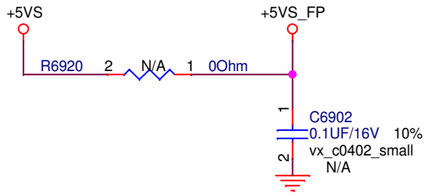
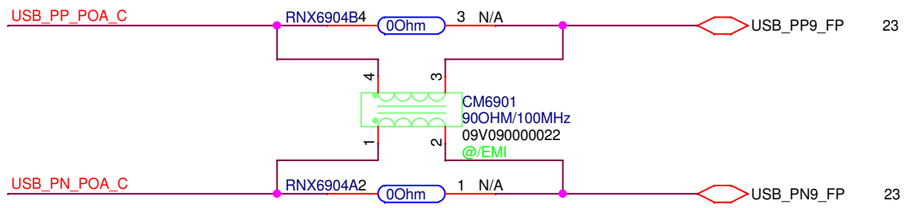
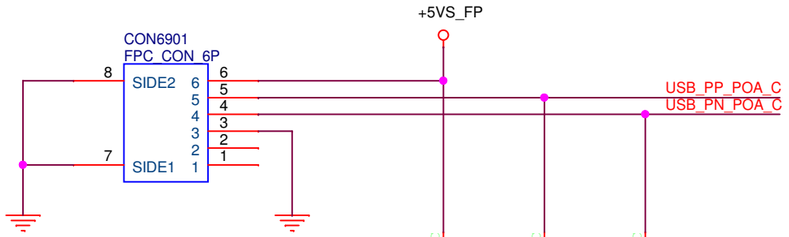
69 Finger printer

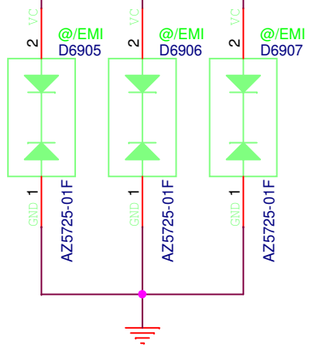
Close to CON6901







Pin	Definition
1	+FP_VCC
2	USBP
3	USBN
4	GND
5	NC
6	NC



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : Finger printer
BG1-HW3 RD
Engineer: Kai_Shen

Size	Project Name	Rev
B	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 69 of 94

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VGA_PCIE

+1V8_AON, +1V8_MAIN, +PEX_VDD

+1V8_AON	+1V8_AON	57,72,74,75,87,90,91
+1V8_MAIN	+1V8_MAIN	57,71,72,74,75,91
+PEX_VDD	+PEX_VDD	57,71,72,85

+1V8_MAIN

21,87 DGPU_PWROK — R7011 2 1 0Ohm, R7010 2 1 0Ohm

24 CLK_REQ3_PEG# — U7004A UM6K1NG1DTN

U7004B UM6K1NG1DTN

+1V8_AON

R7005 10KOhm

74 PEX_RST# — PEX_RST# — AC7 PEX_RST_N

PEX_CLKREQ* — AC6 PEX_CLKREQ_N

24 PEX_REFCLK, 24 PEX_REFCLK* — AE8 PEX_REFCLK, AD8 PEX_REFCLK_N

23 PEX_TXX0	PEX_TXX0	C7006 1 2 0.22UF/10V	PEX_TX0	AC9	PEX_TX0
23 PEX_TXX0*	PEX_TXX0*	C7001 1 2 0.22UF/10V	PEX_TX0*	AB9	PEX_TX0_N
23 PEX_RX0	PEX_RX0			AG6	PEX_RX0
23 PEX_RX0*	PEX_RX0*			AG7	PEX_RX0_N
23 PEX_TXX1	PEX_TXX1	C7007 1 2 0.22UF/10V	PEX_TX1	AB10	PEX_TX1
23 PEX_TXX1*	PEX_TXX1*	C7002 1 2 0.22UF/10V	PEX_TX1*	AC10	PEX_TX1_N
23 PEX_RX1	PEX_RX1			AF7	PEX_RX1
23 PEX_RX1*	PEX_RX1*			AE7	PEX_RX1_N
23 PEX_TXX2	PEX_TXX2	C7008 1 2 0.22UF/10V	PEX_TX2	AD11	PEX_TX2
23 PEX_TXX2*	PEX_TXX2*	C7003 1 2 0.22UF/10V	PEX_TX2*	AC11	PEX_TX2_N
23 PEX_RX2	PEX_RX2			AE9	PEX_RX2
23 PEX_RX2*	PEX_RX2*			AF9	PEX_RX2_N
23 PEX_TXX3	PEX_TXX3	C7009 1 2 0.22UF/10V	PEX_TX3	AC12	PEX_TX3
23 PEX_TXX3*	PEX_TXX3*	C7004 1 2 0.22UF/10V	PEX_TX3*	AB12	PEX_TX3_N
23 PEX_RX3	PEX_RX3			AG9	PEX_RX3
23 PEX_RX3*	PEX_RX3*			AG10	PEX_RX3_N

AB13 PEX_TX4, AC13 PEX_TX4_N

AF10 PEX_RX4, AE10 PEX_RX4_N

AD14 PEX_TX5, AC14 PEX_TX5_N

AE12 PEX_RX5, AF12 PEX_RX5_N

AC15 PEX_TX6, AB15 PEX_TX6_N

AG12 PEX_RX6, AG13 PEX_RX6_N

AB16 PEX_TX7, AC16 PEX_TX7_N

AF13 PEX_RX7, AE13 PEX_RX7_N

AD17 PEX_TX8, AC17 PEX_TX8_N

AE15 PEX_RX8, AF15 PEX_RX8_N

AC18 PEX_TX9, AB18 PEX_TX9_N

AG15 PEX_RX9, AG16 PEX_RX9_N

AB19 PEX_TX10, AC19 PEX_TX10_N

AF16 PEX_RX10, AE16 PEX_RX10_N

AD20 PEX_TX11, AC20 PEX_TX11_N

AE18 PEX_RX11, AF18 PEX_RX11_N

AC21 PEX_TX12, AB21 PEX_TX12_N

AG18 PEX_RX12, AG19 PEX_RX12_N

AD23 PEX_TX13, AE23 PEX_TX13_N

AF19 PEX_RX13, AE19 PEX_RX13_N

AF24 PEX_TX14, AE24 PEX_TX14_N

AE21 PEX_RX14, AF21 PEX_RX14_N

AG24 PEX_TX15, AG25 PEX_TX15_N

AG21 PEX_RX15, AG22 PEX_RX15_N

U7001A — N17S-G1 /VGA 02V0A0001N00

AB6 NC_3

VDD_SENSE — F2 — NVVDD_VDD_SENSE 87

GND_SENSE — F1 — NVVDD_VSS_SENSE 87

NC_11 AF22 — GM108_PEX_PLL_CLK_OUT* R7002 1 @ 2 200Ohm — AF22 GM108_PEX_PLL_CLK_OUT — NC_7

NC_1 AA14 — PEX_PLLVDD — NC_2 AA15

NVJTAG_SEL — AD9 NVJTAG_SEL — R7004 1 2 10KOhm

PEX_TERMP — AF25 PEX_TERMP — R7003 1 2 2.49KOhm 1%

PEX_DVDD_1 AA22, PEX_DVDD_2 AB23, PEX_DVDD_3 AC24, PEX_DVDD_4 AD25, PEX_DVDD_5 AE26, PEX_DVDD_6 AE27

PEX_HVDD_1 AA10, PEX_HVDD_2 AA12, PEX_HVDD_3 AA13, PEX_HVDD_4 AA16, PEX_HVDD_5 AA18, PEX_HVDD_6 AA19, PEX_HVDD_7 AA20, PEX_HVDD_8 AA21, PEX_HVDD_9 AB22, PEX_HVDD_10 AC23, PEX_HVDD_11 AD24, PEX_HVDD_12 AE25, PEX_HVDD_13 AF26, PEX_HVDD_14 AF27

PEX_PLL_HVDD_1 AA8, PEX_PLL_HVDD_2 AA9

NC_4 AB8

Place under GPU

1uFx(1+1), 4.7uFx(1)

C7011 1UF/6.3V /VGA, C7025 1UF/6.3V /VGA, C7012 4.7UF/10V @

1uFx4

PEX_HVDD

C7016 1UF/6.3V /VGA, C7017 1UF/6.3V /VGA, C7018 1UF/6.3V /VGA, C7019 1UF/6.3V /VGA

0.1uFx1

PEX_PLL_HVDD

C7026 0.1UF/25V /VGA

Place near GPU

4.7uFx2, 10uFx2, 22uFx1

C7013 4.7UF/10V /VGA, C7014 4.7UF/10V /VGA, C7015 10UF/6.3V /VGA, C7005 10UF/6.3V /VGA, C7010 22UF/6.3V /VGA

4.7uFx2, 10uFx2, 22uFx1

C7020 4.7UF/10V /VGA, C7021 4.7UF/10V /VGA, C7022 10UF/6.3V /VGA, C7024 10UF/6.3V /VGA, C7023 22UF/6.3V /VGA

+PEX_VDD +1V8_MAIN

R7015 0Ohm @

R7001 0Ohm

Place under GPU

0.1uFx(1)

C7027 0.1UF/25V @

Place near GPU

1uFx(1), 4.7uFx(1)

C7029 1UF/10V @, C7030 4.7UF/10V @

R7016 1 @ 2 0Ohm

+PEX_VDD

C7028 1UF/10V @

+1V8_AON

21 DGPU_HOLD_RST# — DGPU_HOLD_RST# — R7012 2 1 0Ohm — BUF_PLT_RST# 25,30,32,49,51,53,62

U7003 /VGA SN74LVC1G08DCKR

R7009 10KOhm @

PEX_RST#_R — R7014 2 @ 1 0Ohm — SYS_PEX_RST_MON*

R7017 2 /VGA 110KOhm — D7002 1V/0.1A

R7008 10KOhm @

R7013 0Ohm /VGA

+1V8_AON

74 GPU_PEX_RST_HOLD* — GPU_PEX_RST_HOLD*

74 SYS_PEX_RST_MON* — SYS_PEX_RST_MON*

U7002 @ SN74LVC1G08DCKR

R7007 10KOhm @

PEX_RST#

R7006 100KOhm

D7001 @ 1V/0.1A

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Engineer: Kai_Shen

PEGATRON Title : VGA_PCIE

Size	Project Name	Rev
C	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 70 of 94

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VGA_FRAME BUFFER_GDDR5

U7001B

76	FBA_D<0>	FBA_D<0>	E18	FBA_D0	
76	FBA_D<1>	FBA_D<1>	F18	FBA_D1	
76	FBA_D<2>	FBA_D<2>	E16	FBA_D2	
76	FBA_D<3>	FBA_D<3>	F17	FBA_D3	
76	FBA_D<4>	FBA_D<4>	D20	FBA_D4	
76	FBA_D<5>	FBA_D<5>	D21	FBA_D5	
76	FBA_D<6>	FBA_D<6>	F20	FBA_D6	
76	FBA_D<7>	FBA_D<7>	E21	FBA_D7	
76	FBA_D<8>	FBA_D<8>	E15	FBA_D8	
76	FBA_D<9>	FBA_D<9>	D15	FBA_D9	
76	FBA_D<10>	FBA_D<10>	F15	FBA_D10	
76	FBA_D<11>	FBA_D<11>	F13	FBA_D11	
76	FBA_D<12>	FBA_D<12>	C13	FBA_D12	
76	FBA_D<13>	FBA_D<13>	B13	FBA_D13	
76	FBA_D<14>	FBA_D<14>	E13	FBA_D14	
76	FBA_D<15>	FBA_D<15>	D13	FBA_D15	
76	FBA_D<16>	FBA_D<16>	B15	FBA_D16	
76	FBA_D<17>	FBA_D<17>	C16	FBA_D17	
76	FBA_D<18>	FBA_D<18>	A13	FBA_D18	
76	FBA_D<19>	FBA_D<19>	A15	FBA_D19	
76	FBA_D<20>	FBA_D<20>	B18	FBA_D20	
76	FBA_D<21>	FBA_D<21>	A18	FBA_D21	
76	FBA_D<22>	FBA_D<22>	A19	FBA_D22	
76	FBA_D<23>	FBA_D<23>	C19	FBA_D23	
76	FBA_D<24>	FBA_D<24>	B24	FBA_D24	
76	FBA_D<25>	FBA_D<25>	C23	FBA_D25	
76	FBA_D<26>	FBA_D<26>	A25	FBA_D26	
76	FBA_D<27>	FBA_D<27>	A24	FBA_D27	
76	FBA_D<28>	FBA_D<28>	A21	FBA_D28	
76	FBA_D<29>	FBA_D<29>	B21	FBA_D29	
76	FBA_D<30>	FBA_D<30>	C20	FBA_D30	
76	FBA_D<31>	FBA_D<31>	C21	FBA_D31	
77	FBA_D<32>	FBA_D<32>	R22	FBA_D32	
77	FBA_D<33>	FBA_D<33>	R24	FBA_D33	
77	FBA_D<34>	FBA_D<34>	T22	FBA_D34	
77	FBA_D<35>	FBA_D<35>	R23	FBA_D35	
77	FBA_D<36>	FBA_D<36>	N25	FBA_D36	
77	FBA_D<37>	FBA_D<37>	N26	FBA_D37	
77	FBA_D<38>	FBA_D<38>	N23	FBA_D38	
77	FBA_D<39>	FBA_D<39>	N24	FBA_D39	
77	FBA_D<40>	FBA_D<40>	V23	FBA_D40	
77	FBA_D<41>	FBA_D<41>	V22	FBA_D41	
77	FBA_D<42>	FBA_D<42>	T23	FBA_D42	
77	FBA_D<43>	FBA_D<43>	U22	FBA_D43	
77	FBA_D<44>	FBA_D<44>	Y24	FBA_D44	
77	FBA_D<45>	FBA_D<45>	AA24	FBA_D45	
77	FBA_D<46>	FBA_D<46>	Y22	FBA_D46	
77	FBA_D<47>	FBA_D<47>	AA23	FBA_D47	
77	FBA_D<48>	FBA_D<48>	AD27	FBA_D48	
77	FBA_D<49>	FBA_D<49>	AB25	FBA_D49	
77	FBA_D<50>	FBA_D<50>	AD26	FBA_D50	
77	FBA_D<51>	FBA_D<51>	AC25	FBA_D51	
77	FBA_D<52>	FBA_D<52>	AA27	FBA_D52	
77	FBA_D<53>	FBA_D<53>	AA26	FBA_D53	
77	FBA_D<54>	FBA_D<54>	W26	FBA_D54	
77	FBA_D<55>	FBA_D<55>	Y25	FBA_D55	
77	FBA_D<56>	FBA_D<56>	R26	FBA_D56	
77	FBA_D<57>	FBA_D<57>	T25	FBA_D57	
77	FBA_D<58>	FBA_D<58>	N27	FBA_D58	
77	FBA_D<59>	FBA_D<59>	R27	FBA_D59	
77	FBA_D<60>	FBA_D<60>	V26	FBA_D60	
77	FBA_D<61>	FBA_D<61>	V27	FBA_D61	
77	FBA_D<62>	FBA_D<62>	W27	FBA_D62	
77	FBA_D<63>	FBA_D<63>	W25	FBA_D63	

GNDS_SENSE F3

35 mA

+FBVDDQ +1V8_MAIN +PEX_VDD — +FBVDDQ 57,75,76,77,86 / +1V8_MAIN 57,70,72,74,75,91 / +PEX_VDD 57,70,72,85

NVIDIA Design Guide
DG-07875-001_v08 P.154
Table 9.5

DQ[31:0]	DQ[63:32]	Mapping
CMD0	CMD16	CS#
CMD1	CMD17	A2_BA0
CMD2	CMD18	A3_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE#
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI#
CMD9	CMD25	A12_RFU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS#
CMD13	CMD29	RST#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

+FBVDDQ

FBA_CMD<14> R7106 2 1 10KOhm 5%
FBA_CMD<30> R7105 2 1 10KOhm 5%
FBA_CMD<13> R7107 2 1 10KOhm 5%
FBA_CMD<29> R7108 2 1 10KOhm 5%

FBA_CMD0	C27	FBA_CMD<0>	FBA_CMD<0>	76	
FBA_CMD1	C26	FBA_CMD<1>	FBA_CMD<1>	76	
FBA_CMD2	E24	FBA_CMD<2>	FBA_CMD<2>	76	
FBA_CMD3	F24	FBA_CMD<3>	FBA_CMD<3>	76	
FBA_CMD4	D27	FBA_CMD<4>	FBA_CMD<4>	76	
FBA_CMD5	D26	FBA_CMD<5>	FBA_CMD<5>	76	
FBA_CMD6	F25	FBA_CMD<6>	FBA_CMD<6>	76	
FBA_CMD7	F26	FBA_CMD<7>	FBA_CMD<7>	76	
FBA_CMD8	F23	FBA_CMD<8>	FBA_CMD<8>	76	
FBA_CMD9	G22	FBA_CMD<9>	FBA_CMD<9>	76	
FBA_CMD10	G23	FBA_CMD<10>	FBA_CMD<10>	76	
FBA_CMD11	G24	FBA_CMD<11>	FBA_CMD<11>	76	
FBA_CMD12	F27	FBA_CMD<12>	FBA_CMD<12>	76	
FBA_CMD13	G25	FBA_CMD<13>	FBA_CMD<13>	76	
FBA_CMD14	G27	FBA_CMD<14>	FBA_CMD<14>	76	
FBA_CMD15	G26	FBA_CMD<15>	FBA_CMD<15>	76	
FBA_CMD16	M24	FBA_CMD<16>	FBA_CMD<16>	77	
FBA_CMD17	M23	FBA_CMD<17>	FBA_CMD<17>	77	
FBA_CMD18	K24	FBA_CMD<18>	FBA_CMD<18>	77	
FBA_CMD19	K23	FBA_CMD<19>	FBA_CMD<19>	77	
FBA_CMD20	M27	FBA_CMD<20>	FBA_CMD<20>	77	
FBA_CMD21	M26	FBA_CMD<21>	FBA_CMD<21>	77	
FBA_CMD22	M25	FBA_CMD<22>	FBA_CMD<22>	77	
FBA_CMD23	K26	FBA_CMD<23>	FBA_CMD<23>	77	
FBA_CMD24	K22	FBA_CMD<24>	FBA_CMD<24>	77	
FBA_CMD25	J23	FBA_CMD<25>	FBA_CMD<25>	77	
FBA_CMD26	J25	FBA_CMD<26>	FBA_CMD<26>	77	
FBA_CMD27	J24	FBA_CMD<27>	FBA_CMD<27>	77	
FBA_CMD28	K27	FBA_CMD<28>	FBA_CMD<28>	77	
FBA_CMD29	K25	FBA_CMD<29>	FBA_CMD<29>	77	
FBA_CMD30	J27	FBA_CMD<30>	FBA_CMD<30>	77	
FBA_CMD31	J26	FBA_CMD<31>	FBA_CMD<31>	77	

T7102 TP_28T @

For test/Debug only
SNN_FBA_CMD<32> — B19 FBA_CMD32 — +FBVDDQ

FBA_CMD34 FBA_CMD34 — F22 — R7101 1 @ 2 60.4Ohm 1%
FBA_CMD35 FBA_CMD35 — J22 — R7102 1 @ 2 60.4Ohm 1%

FBA_CLK0	D24	FBA_CLK0	76
FBA_CLK0_N	D25	FBA_CLK0*	76
FBA_CLK1	N22	FBA_CLK1	77
FBA_CLK1_N	M22	FBA_CLK1*	77

	F19	FBA_DQS_RN0	
	C14	FBA_DQS_RN1	
	A16	FBA_DQS_RN2	
	A22	FBA_DQS_RN3	
	P25	FBA_DQS_RN4	
	W22	FBA_DQS_RN5	
	AB27	FBA_DQS_RN6	
	T27	FBA_DQS_RN7	

FBA_WCK01	D18	FBA_WCK01	76
FBA_WCK01_N	C18	FBA_WCK01*	76
FBA_WCK23	D17	FBA_WCK23	76
FBA_WCK23_N	D16	FBA_WCK23*	76
FBA_WCK45	T24	FBA_WCK45	77
FBA_WCK45_N	U24	FBA_WCK45*	77
FBA_WCK67	V24	FBA_WCK67	77
FBA_WCK67_N	V25	FBA_WCK67*	77

0.1uFx(1+1) Place under GPU — 0.1uFx2 Place under GPU — 22uFx1, beadx(3-1) Place near GPU

FB_PLL_AVDD_1 F16
FB_PLL_AVDD_2 P22 — +FB_PLL_AVDD
FB_REFPLL_AVDD H22 — +FB_REFPLL_AVDD_GPU

C7104 0.1UF/25V /VGA — C7103 0.1UF/25V @
C7101 0.1UF/25V /VGA — C7105 0.1UF/25V /VGA

R7110 1 2 0Ohm
R7109 1 2 0Ohm

+FB_PLVDD — C7102 22UF/6.3V /VGA

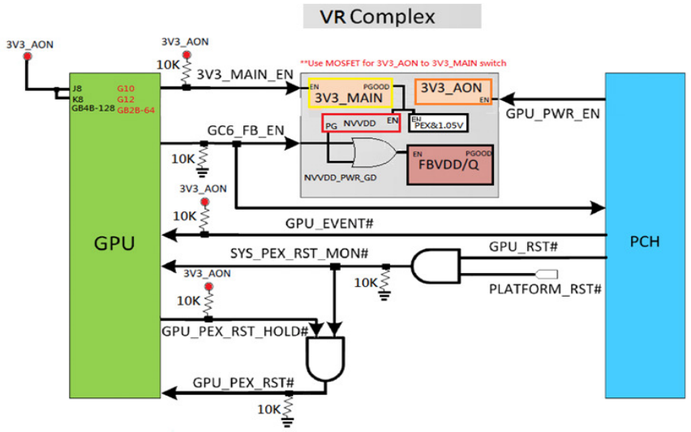
B7101 1 2 30Ohm/100Mhz vx_l0603_small
B7102 1 @ 2 30Ohm/100Mhz vx_l0603_small

+1V8_MAIN +PEX_VDD

T7101
1 FB_VREF D23 FB_VREF

N17S-G1
/VGA
02V0A0001N00

VR Complex



GC6 2.0 High-level Signal Connections

PEGATRON	Title :	VGA_FRAME BUFFER
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1-NB4	Engineer:	Kai_Shen
Size: C	Project Name: HE4EA	Rev: 1.0
Date: Friday, April 07, 2017	Sheet 71 of 94	

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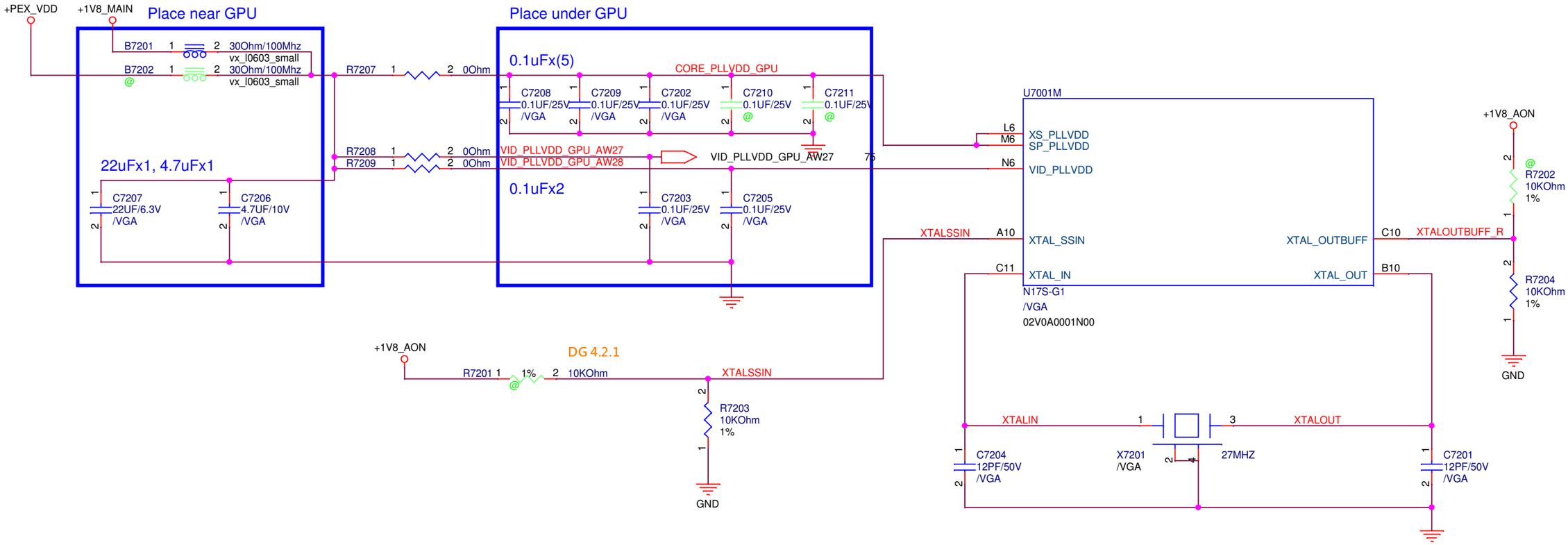
VGA_XTAL

+1V8_AON
+1V8_MAIN
+PEX_VDD

+1V8_AON 57,70,74,75,87,90,91
+1V8_MAIN 57,70,71,74,75,91
+PEX_VDD 57,70,71,85



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : VGA_XTAL

BG1-NB4

Engineer: Kai_Shen

Size	Project Name	Rev
B	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 72 of 94

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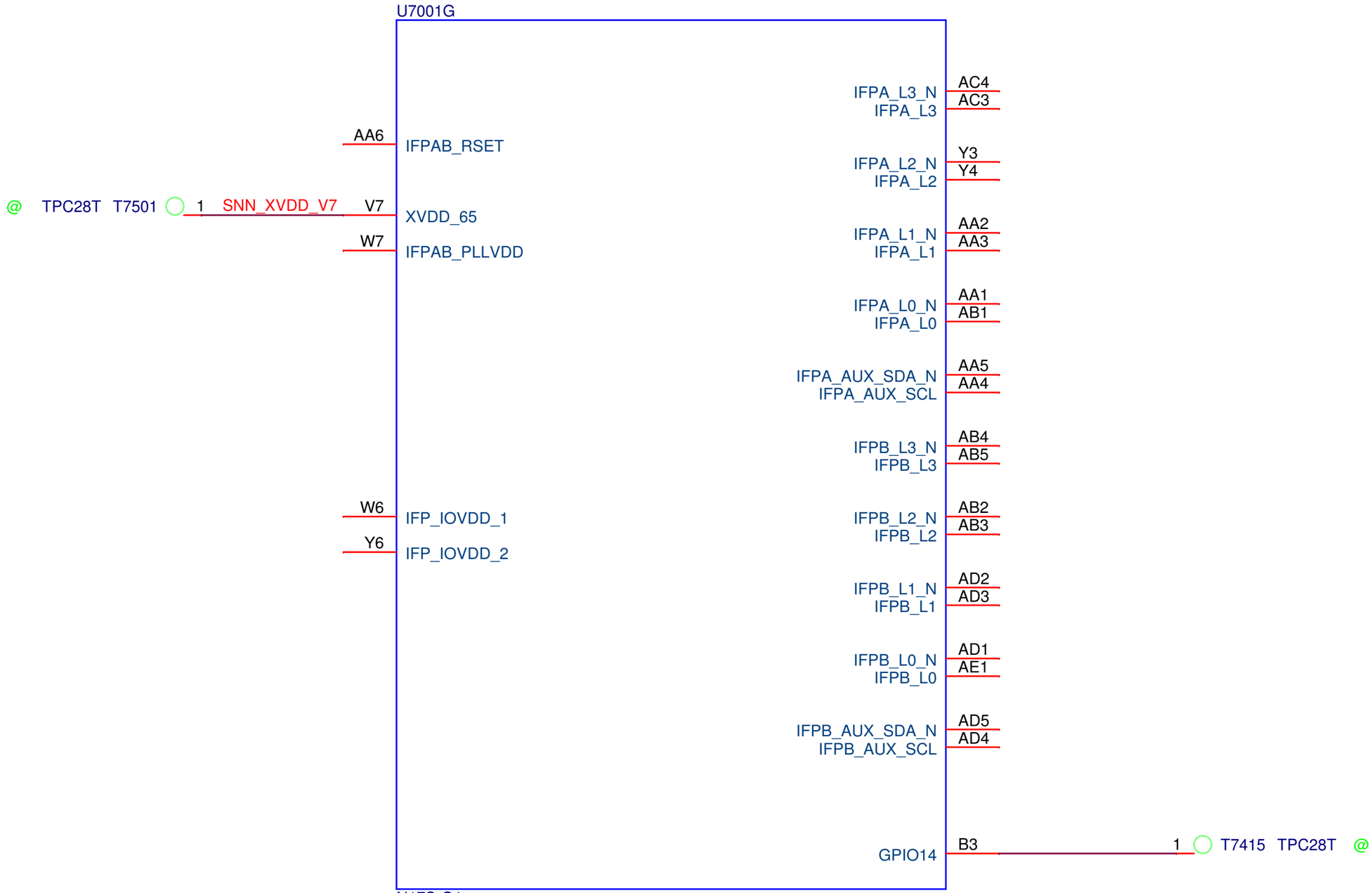
VGA_DISPLAY



PEGATRON Title : VGA_DISPLAY

PEGATRON PROPRIETARY AND CONFIDENTIAL

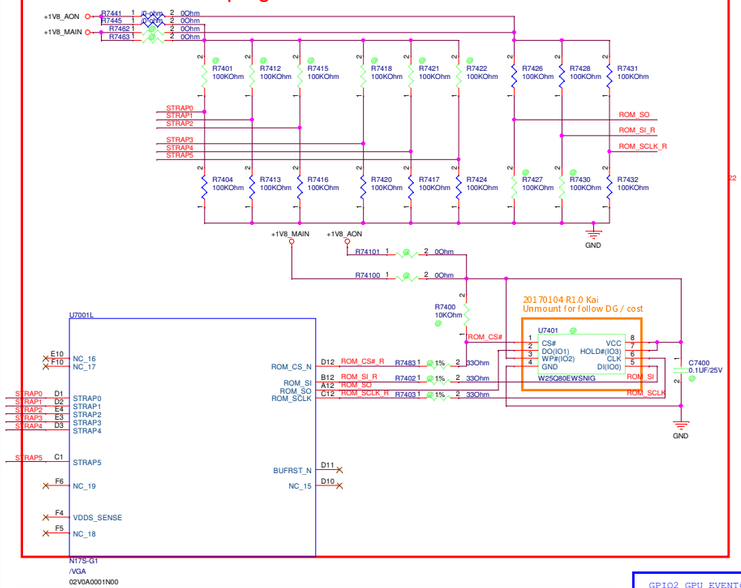
BG1-NB4

Engineer: *Kai_Shen*

Size	Project Name	Rev
A	**HE4EA**	1.0

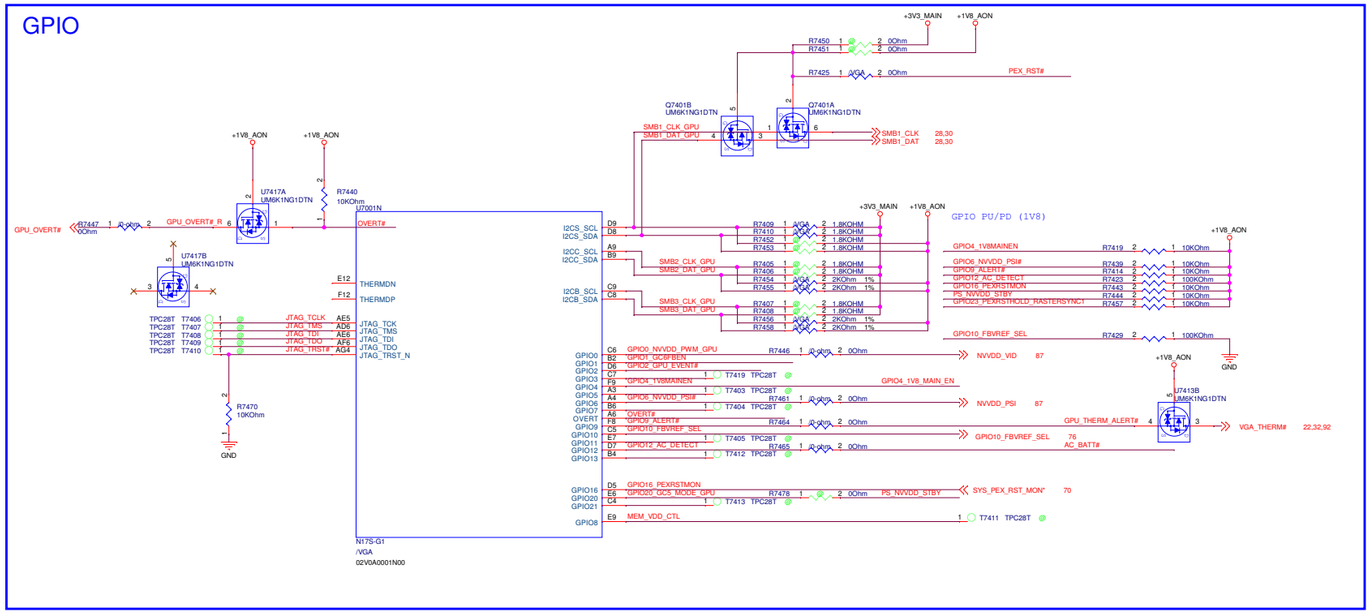
Date: Friday, April 07, 2017 Sheet 73 of 94

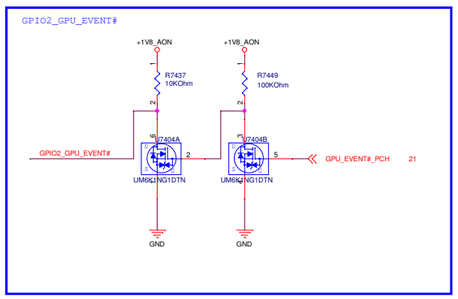
VBIOS ROM / Straping

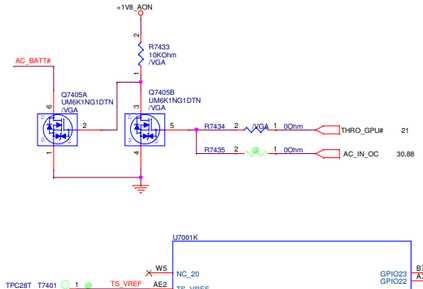


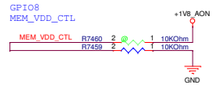
STRAP2	STRAP1	STRAP0	STRAP configure	Memory Density	Manufacturer Part Number	PEGA P/N
L (R7416)	L (R7413)	L (R7404)	0x0	8Gb	SAMSUNG/K4G80325FB-HC28	0315-01JG0PB
L (R7416)	L (R7413)	H (R7401)	0x1	8Gb	MICRON/MT51J256M32HF-70:A	0315-01LN0PB
L (R7416)	H (R7412)	L (R7404)	0x2	8Gb	SK HYNIX/H5GC8H24MJR-R0C	0315-01SB0PB
H (R7415)	H (R7412)	L (R7404)	0x6	4Gb	SK HYNIX/H5GC4H24AJR-R0C	0315-01HR0PB
H (R7415)	H (R7412)	H (R7401)	0x7	4Gb	MICRON/EDW4032BABG-70-F	0315-025D0PB
L (R7416)	L (R7413)	M (R7401 & R7404)	0x8	4Gb	SAMSUNG/K4G41325FE-HC28	0315-01Q90PB

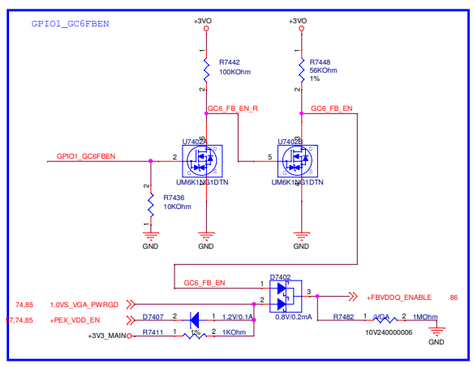
GPIO

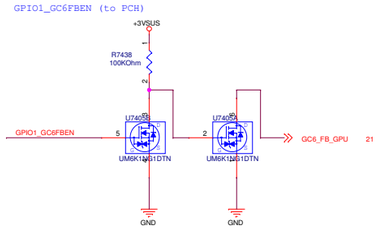


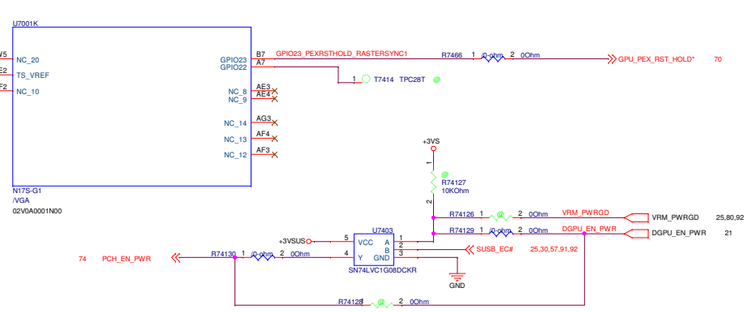




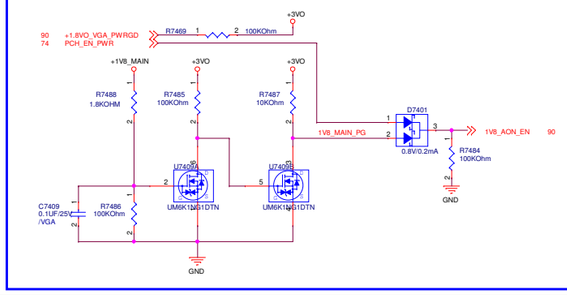




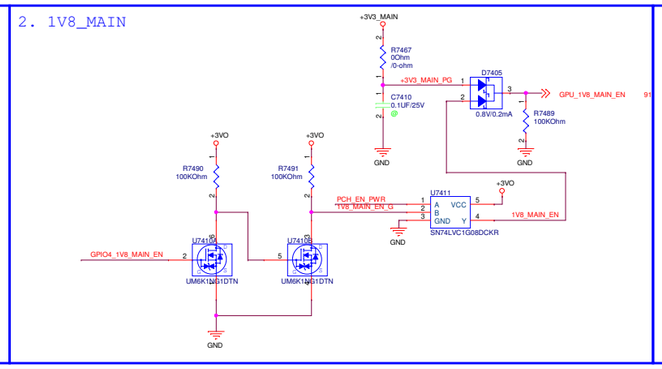




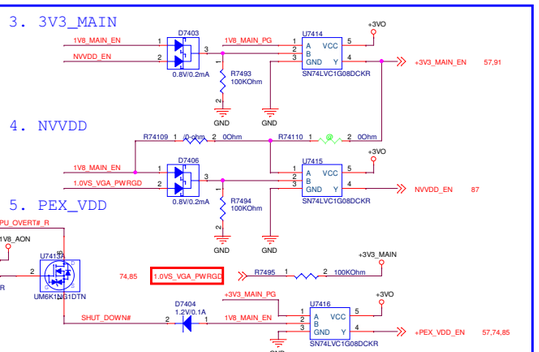
1.1V8_AON



2. 1V8_MAIN



3. 3V3_MAIN



4. NVVDD

5. PEX_VDD

PEGATRON DT-MB RESTRICTED SECRET
<Variant Name>

PEGATRON Title : NVIDIA MISC/GPIO
Pegatron Corp. Engineer: Kai_Shen

Size	Project Name	Rev
D	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 74 of 94

75

VGA_Power_GND

+1V8_AON
+1V8_MAIN
+NVVDD
+FBVDDQ

+1V8_AON 57,70,72,74,87,90,91
+1V8_MAIN 57,70,71,72,74,91
+NVVDD 57,87
+FBVDDQ 57,71,76,77,86

+FBVDDQ
Place under GPU
1uFx8, 10uFx2
C7516 1UF/6.3V /VGA
C7517 1UF/6.3V /VGA
C7518 1UF/6.3V /VGA
C7519 1UF/6.3V /VGA
C7520 1UF/6.3V /VGA
C7521 1UF/6.3V /VGA
C7522 1UF/6.3V /VGA
C7523 1UF/6.3V /VGA
C7501 10UF/6.3V /VGA
C7514 10UF/6.3V /VGA
GND
Place near GPU
10uFx1, 22uFx3
C7502 10UF/6.3V /VGA
C7503 22UF/6.3V /VGA
C7515 22UF/6.3V /VGA
C7524 22UF/6.3V /VGA
C7525 22UF/6.3V
C7526 22UF/6.3V
GND

+NVVDD
Place under GPU
1uFx3, 10uFx(8)
C7527 1UF/6.3V /VGA
C7528 1UF/6.3V /VGA
C7529 1UF/6.3V /VGA
C7532 10UF/6.3V
C7533 10UF/6.3V
C7534 10UF/6.3V
C7535 10UF/6.3V
C7536 10UF/6.3V
C7537 10UF/6.3V
C7530 10UF/6.3V
C7531 10UF/6.3V
GND
Place under GPU
4.7uFx(8)
C7556 4.7UF/10V /VGA
C7557 4.7UF/10V /VGA
C7558 4.7UF/10V /VGA
C7559 4.7UF/10V /VGA
GND
Place near GPU
4.7uFx4, 10uFx4, 22uFx3
C7541 4.7UF/10V /VGA
C7542 4.7UF/10V /VGA
C7543 4.7UF/10V /VGA
C7544 4.7UF/10V /VGA
C7545 10UF/6.3V /VGA
C7546 10UF/6.3V /VGA
C7547 10UF/6.3V /VGA
C7548 10UF/6.3V /VGA
C7538 22UF/6.3V /VGA
C7539 22UF/6.3V /VGA
C7540 22UF/6.3V /VGA
C7560 4.7UF/10V /VGA
C7561 4.7UF/10V /VGA
C7562 4.7UF/10V /VGA
C7563 4.7UF/10V /VGA
GND
Place near GPU
330uFx(1+1), 22uFx(5)
C7505 330UF/2V /VGA vx_c7343d_h83
C7549 22UF/6.3V
C7551 22UF/6.3V
C7552 22UF/6.3V
C7553 22UF/6.3V
C7550 22UF/6.3V
Place under VRAM
10uFx2
C7554 10UF/6.3V /VGA
C7555 10UF/6.3V /VGA
GND

VID_PLLVDD_GPU_AW27 72

U7001F
GND_1 GND_6 GND_7 GND_8 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24 GND_25 GND_26 GND_4 GND_27 GND_28 GND_29 GND_30 GND_31 GND_32 GND_33 GND_34 GND_35 GND_36 GND_5 GND_37 GND_38 GND_39 GND_40 GND_41 GND_42 GND_43 GND_44 GND_45 GND_46 GND_47 GND_48 GND_49 GND_50 GND_51 GND_52 GND_53 GND_54 GND_55 GND_56 GND_57 GND_58 GND_59 GND_60 GND_61 GND_62 GND_63 GND_64 GND_65 GND_66 GND_67 GND_68 GND_69 GND_70 GND_71 GND_72
GND_73 GND_74 GND_75 GND_76 GND_77 GND_78 GND_79 GND_80 GND_81 GND_82 GND_83 GND_84 GND_85 GND_86 GND_87 GND_88 GND_89 GND_90 GND_91 GND_92 GND_93 GND_94 GND_95 GND_96 GND_97 GND_98 GND_99 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114
GND_3 GND_9
N17S-G1 /VGA 02V0A0001N00
GND

+NVVDD
26A
U7001E
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDDS_1 VDD_6 VDD_7 VDDS_2 VDD_8 VDD_9 VDDS_3 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14 VDD_15 VDDS_4 VDDS_5 VDD_16 VDDS_6 VDDS_7 VDD_17 VDD_18 VDD_19 VDD_20 VDD_21 VDD_22 VDDS_8 VDD_23 VDD_24 VDDS_9 VDD_25 VDD_26 VDDS_10 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31
N17S-G1 /VGA 02V0A0001N00

+FBVDDQ
1.4A
U7001D
FBVDDQ_1 FBVDDQ_2 FBVDDQ_3 FBVDDQ_4 FBVDDQ_5 FBVDDQ_6 FBVDDQ_7 FBVDDQ_8 FBVDDQ_9 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26 FBVDDQ_27
FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18
FB_CAL_PD_VDDQ D22 +FBCAL_VDDQ R7503 1 2 40.2Ohm 1%
FB_CAL_PU_GND C24 +FBCAL_GND R7502 1 2 40.2Ohm 1%
FB_CAL_TERM_GND B25 +FBCAL_TERM R7501 1 2 60.4Ohm 1%
+FBVDDQ
GND
N17S-G1 /VGA 02V0A0001N00

+NVVDD
U7001C
NC_5 NC_6
GPCPLL_AVDD
XVDD_63 XVDD_64
XVDD_1 XVDD_2 XVDD_3 XVDD_4 XVDD_5 XVDD_6 XVDD_7
XVDD_59 XVDD_60
XVDD_66 XVDD_67 XVDD_68 XVDD_69
VDD18_1 VDD18_2 1V8_AON_1 1V8_AON_2
+1V8_MAIN +1V8_AON
N17S-G1 /VGA 02V0A0001N00

+1V8_MAIN
+1V8_AON
Place near GPU
Place under GPU
4.7UFx1, 1UFx1, 0.1UFx2
C7508 4.7UF/10V /VGA
C7507 1UF/6.3V /VGA
C7513 0.1UF/25V /VGA
C7506 0.1UF/25V /VGA
C7511 4.7UF/10V /VGA
C7512 1UF/6.3V /VGA
C7509 0.1UF/25V /VGA
C7510 0.1UF/25V /VGA
GND

+NVVDD
U7001H
XVDD_54
XVDD_32 XVDD_38
XVDD_41
XVDD_37 XVDD_36 XVDD_35 XVDD_34 XVDD_44 XVDD_43 XVDD_42 XVDD_49 XVDD_51 XVDD_50
GPIO15
T7416 TPC28T
N17S-G1 /VGA 02V0A0001N00

+NVVDD
U7001I
XVDD_58
XVDD_55
XVDD_48
XVDD_47
XVDD_40 XVDD_39 XVDD_46 XVDD_45 XVDD_53 XVDD_52 XVDD_57 XVDD_56 XVDD_62 XVDD_61
GPIO17
T7417 TPC28T
N17S-G1 /VGA 02V0A0001N00

+NVVDD
U7001J
XVDD_17
XVDD_24
XVDD_23
XVDD_10
XVDD_16
XVDD_13 XVDD_12 XVDD_11 XVDD_18 XVDD_20 XVDD_19 XVDD_29 XVDD_28 XVDD_27 XVDD_33 XVDD_9 XVDD_8 XVDD_15 XVDD_14 XVDD_22 XVDD_21 XVDD_26 XVDD_25 XVDD_31 XVDD_30
GPIO18
T7418 TPC28T
GPIO19
GPIO19_STEREO_OUT_SRV_HEAD
T7402 TPC28T
N17S-G1 /VGA 02V0A0001N00

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : VGA_Power
BG1-NB4
Engineer: Kai_Shen
Size D
Project Name HE4EA
Rev 1.0
Date: Friday, April 07, 2017
Sheet 75 of 94

VGA_FBA_GDDR5_32-bit_01

+FBVDDQ +FBVDDQ 57,71,75,77,86

Non-Mirrored / Mirred

U7600

71	FBA_D<31>	FBA_D<31>	M2	DQ31/DQ7	3	VDDQ_1	B1
71	FBA_D<30>	FBA_D<30>	M4	DQ30/DQ6		VDDQ_21	B3
71	FBA_D<29>	FBA_D<29>	N2	DQ29/DQ5		VDDQ_29	B12
71	FBA_D<28>	FBA_D<28>	N4	DQ28/DQ4		VDDQ_15	B14
71	FBA_D<27>	FBA_D<27>	T2	DQ27/DQ3		VDDQ_2	D1
71	FBA_D<26>	FBA_D<26>	T4	DQ26/DQ2		VDDQ_22	D3
71	FBA_D<25>	FBA_D<25>	U2	DQ25/DQ1		VDDQ_30	D12
71	FBA_D<24>	FBA_D<24>	U4	DQ24/DQ0		VDDQ_16	D14
71	FBA_D<23>	FBA_D<23>	M13	DQ23/DQ15	2	VDDQ_13	E5
71	FBA_D<22>	FBA_D<22>	M11	DQ22/DQ14		VDDQ_7	E10
71	FBA_D<21>	FBA_D<21>	N13	DQ21/DQ13		VDDQ_3	F1
71	FBA_D<20>	FBA_D<20>	N11	DQ20/DQ12		VDDQ_23	F3
71	FBA_D<19>	FBA_D<19>	T13	DQ19/DQ11		VDDQ_31	F12
71	FBA_D<18>	FBA_D<18>	T11	DQ18/DQ10		VDDQ_17	F14
71	FBA_D<17>	FBA_D<17>	U13	DQ17/DQ9		VDDQ_9	G2
71	FBA_D<16>	FBA_D<16>	U11	DQ16/DQ8		VDDQ_11	G13
71	FBA_D<15>	FBA_D<15>	F13	DQ15/DQ23	1	VDDQ_24	H3
71	FBA_D<14>	FBA_D<14>	F11	DQ14/DQ22		VDDQ_32	H12
71	FBA_D<13>	FBA_D<13>	E13	DQ13/DQ21		VDDQ_25	K3
71	FBA_D<12>	FBA_D<12>	E11	DQ12/DQ20		VDDQ_33	K12
71	FBA_D<11>	FBA_D<11>	B13	DQ11/DQ19		VDDQ_10	L2
71	FBA_D<10>	FBA_D<10>	B11	DQ10/DQ18		VDDQ_12	L13
71	FBA_D<9>	FBA_D<9>	A13	DQ9/DQ17		VDDQ_4	M1
71	FBA_D<8>	FBA_D<8>	A11	DQ8/DQ16		VDDQ_26	M3
71	FBA_D<7>	FBA_D<7>	F2	DQ7/DQ31	0	VDDQ_34	M12
71	FBA_D<6>	FBA_D<6>	F4	DQ6/DQ30		VDDQ_18	M14
71	FBA_D<5>	FBA_D<5>	E2	DQ5/DQ29		VDDQ_14	N5
71	FBA_D<4>	FBA_D<4>	E4	DQ4/DQ28		VDDQ_8	N10
71	FBA_D<3>	FBA_D<3>	B2	DQ3/DQ27		VDDQ_5	P1
71	FBA_D<2>	FBA_D<2>	B4	DQ2/DQ26		VDDQ_27	P3
71	FBA_D<1>	FBA_D<1>	A2	DQ1/DQ25		VDDQ_35	P12
71	FBA_D<0>	FBA_D<0>	A4	DQ0/DQ24		VDDQ_19	P14
						VDDQ_6	T1
						VDDQ_28	T3
						VDDQ_36	T12
						VDDQ_20	T14
71	FBA_CMD<9>	FBA_CMD<9>	J5				C5
71	FBA_CMD<6>	FBA_CMD<6>	K4	A12/A13		VDD_14	C10
71	FBA_CMD<7>	FBA_CMD<7>	K5	A8/A7/A10/A0		VDD_3	D11
71	FBA_CMD<4>	FBA_CMD<4>	K10	A11/A6/A9/A1		VDD_5	G1
71	FBA_CMD<3>	FBA_CMD<3>	K11	BA1/A5/BA3/A3		VDD_1	G4
71	FBA_CMD<1>	FBA_CMD<1>	H10	BA2/A4/BA0/A2		VDD_9	G11
71	FBA_CMD<2>	FBA_CMD<2>	H11	BA3/A3/BA1/A5		VDD_6	G14
71	FBA_CMD<11>	FBA_CMD<11>	H5	BA0/A2/BA2/A4		VDD_12	L1
71	FBA_CMD<10>	FBA_CMD<10>	H4	A9/A1/A11/A6		VDD_2	L4
				A10/A0/A8/A7		VDD_10	L11
						VDD_7	L14
71	FBA_WCK01	FBA_WCK01	D4			VDD_13	P11
71	FBA_WCK01*	FBA_WCK01*	D5	WCK01/WCK23		VDD_8	R5
				WCK01#/WCK23#		VDD_11	R10
71	FBA_WCK23	FBA_WCK23	P4			VDD_4	
71	FBA_WCK23*	FBA_WCK23*	P5	WCK23/WCK01			A1
				WCK23#/WCK01#		VSSQ_1	A3
71	FBA_EDC<3>	FBA_EDC<3>	R2			VSSQ_25	A12
71	FBA_EDC<2>	FBA_EDC<2>	R13	EDC3/EDC0		VSSQ_31	A14
71	FBA_EDC<1>	FBA_EDC<1>	C13	EDC2/EDC1		VSSQ_18	C1
71	FBA_EDC<0>	FBA_EDC<0>	C2	EDC1/EDC2		VSSQ_2	C3
				EDC0/EDC3		VSSQ_26	C4
71	FBA_DBI<3>	FBA_DBI<3>	P2			VSSQ_24	C11
71	FBA_DBI<2>	FBA_DBI<2>	P13	DBI3#/DBI0#		VSSQ_11	C12
71	FBA_DBI<1>	FBA_DBI<1>	D13	DBI2#/DBI1#		VSSQ_32	C14
71	FBA_DBI<0>	FBA_DBI<0>	D2	DBI1#/DBI2#		VSSQ_19	E1
				DBI0#/DBI3#		VSSQ_3	E3
						VSSQ_27	E12
71	FBA_CMD<12>	FBA_CMD<12>	G3			VSSQ_33	E14
71	FBA_CMD<15>	FBA_CMD<15>	L3	RAS#/CAS#		VSSQ_20	F5
				CAS#/RAS#		VSSQ_16	F10
71	FBA_CMD<14>	FBA_CMD<14>	J3			VSSQ_7	H2
	R76011 1% 2 40.2Ohm	FBA_CLK0*	J11	CKE#		VSSQ_9	H13
	R76021 1% 2 40.2Ohm	FBA_CLK0	J12	CK#		VSSQ_14	K2
71	FBA_CLK0*			CK		VSSQ_10	K13
71	FBA_CLK0					VSSQ_15	M5
71	FBA_CMD<0>	FBA_CMD<0>	G12			VSSQ_17	M10
71	FBA_CMD<5>	FBA_CMD<5>	L12	CS#/WE#		VSSQ_8	N1
				WE#/CS#		VSSQ_4	N3
						VSSQ_28	N12
	R7610 1 1% 2 121OHM	FBA_ZQ_1B	J13			VSSQ_34	N14
			J10	ZQ		VSSQ_21	R1
				SEN		VSSQ_5	R3
71	FBA_CMD<13>	FBA_CMD<13>	J2			VSSQ_29	R4
	R7608 1%	1KOhm	J1	RESET#		VSSQ_13	R11
				MF		VSSQ_12	R12
				[PD] Non-Mirrored		VSSQ_35	R14
						VSSQ_22	U1
			A5			VSSQ_6	U3
			U5	NC_2		VSSQ_30	U12
				NC_1		VSSQ_36	U14
						VSSQ_23	
							B5
			A10			VSS_14	B10
			U10	VREFD_1		VSS_3	D10
				VREFD_2		VSS_4	G5
						VSS_9	G10
						VSS_5	H1
						VSS_1	H14
			J14			VSS_12	K1
				VREFC		VSS_2	K14
						VSS_13	L5
			J4			VSS_10	L10
				ABI#		VSS_6	P10
						VSS_7	T5
						VSS_11	T10
						VSS_8	

K4G80325FB-HC03
03V150000095

+FBVDDQ

22uFx3, 1uFx(10+8), 10uFx4
Place under VRAM

C7632 22UF/6.3V /VGA
C7633 22UF/6.3V /VGA
C7634 22UF/6.3V /VGA
C7615 1UF/6.3V /VGA
C7617 1UF/6.3V /VGA
C7618 1UF/6.3V /VGA
C7619 1UF/6.3V /VGA
C7620 1UF/6.3V /VGA
C7621 1UF/6.3V /VGA
C7622 1UF/6.3V /VGA
C7623 1UF/6.3V /VGA
C7624 1UF/6.3V /VGA
C7625 1UF/6.3V /VGA
C7604 1UF/6.3V /VGA
C7603 1UF/6.3V /VGA
C7606 1UF/6.3V /VGA
C7605 1UF/6.3V /VGA
C7609 1UF/6.3V /VGA
C7607 1UF/6.3V /VGA
C7608 1UF/6.3V /VGA
C7610 1UF/6.3V /VGA
C7626 10UF/6.3V /VGA
C7616 10UF/6.3V /VGA
C7627 10UF/6.3V /VGA
C7628 10UF/6.3V /VGA

10uFx2, 22uFx(2+3)
Place near VRAM

C7629 10UF/6.3V /VGA
C7630 10UF/6.3V /VGA
C7612 22UF/6.3V /VGA
C7631 22UF/6.3V /VGA
C7602 22UF/6.3V /VGA
C7635 22UF/6.3V /VGA
C7636 22UF/6.3V /VGA

C7601 10NF/25V X7R/+/-5%

+FBVDDQ

R7609 549Ohm 1% @
R7603 549Ohm 1%

77 FBA_VREFD — FBA_VREFD
R7604 1.33KOhm 1% @
C7613 820PF/50V X7R/+/-10% @

77 FBA_VREFC — FBA_VREFC
R7605 931OHM 1% @
R7606 931OHM 1%
R7607 1.33KOhm 1%
C7614 820PF/50V X7R/+/-10%

FBA_VREF_Q

74 GPIO10_FBVREF_SEL — Q7601A UM6K1NG1DTN — 71 FBA_CMD<8>

Q7601B UM6K1NG1DTN

+FBVDDQ

C7637 10PF/50V /EMI 1AV200000001
C7638 22PF/50V /EMI 1AV200000009
C7639 22PF/50V /EMI 1AV200000009
C7640 22PF/50V /EMI 1AV200000009
C7641 22PF/50V /EMI 1AV200000009
C7642 22PF/50V /EMI 1AV200000009
C7643 22PF/50V /EMI 1AV200000009
C7644 47PF/50V /EMI 1AV200000015
C7645 47PF/50V /EMI 1AV200000015
C7646 47PF/50V /EMI 1AV200000015
C7647 47PF/50V /EMI 1AV200000015

PEGATRON Title : VGA_FBA_GDDR5
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 76 of 94

77

VGA_FBA_GDDR5_32-bit_02

+FBVDDQ +FBVDDQ 57,71,75,76,86

Non-Mirrored / Mirred

U7700

71	FBA_D<39>	FBA_D<39>	M2	DQ31/DQ7	4	VDDQ_1	B1
71	FBA_D<38>	FBA_D<38>	M4	DQ30/DQ6		VDDQ_21	B3
71	FBA_D<37>	FBA_D<37>	N2	DQ29/DQ5		VDDQ_29	B12
71	FBA_D<36>	FBA_D<36>	N4	DQ28/DQ4		VDDQ_15	B14
71	FBA_D<35>	FBA_D<35>	T2	DQ27/DQ3		VDDQ_2	D1
71	FBA_D<34>	FBA_D<34>	T4	DQ26/DQ2		VDDQ_22	D3
71	FBA_D<33>	FBA_D<33>	U2	DQ25/DQ1		VDDQ_30	D12
71	FBA_D<32>	FBA_D<32>	U4	DQ24/DQ0		VDDQ_16	D14
71	FBA_D<47>	FBA_D<47>	M13	DQ23/DQ15	5	VDDQ_13	E5
71	FBA_D<46>	FBA_D<46>	M11	DQ22/DQ14		VDDQ_7	E10
71	FBA_D<45>	FBA_D<45>	N13	DQ21/DQ13		VDDQ_3	F1
71	FBA_D<44>	FBA_D<44>	N11	DQ20/DQ12		VDDQ_23	F3
71	FBA_D<43>	FBA_D<43>	T13	DQ19/DQ11		VDDQ_31	F12
71	FBA_D<42>	FBA_D<42>	T11	DQ18/DQ10		VDDQ_17	F14
71	FBA_D<41>	FBA_D<41>	U13	DQ17/DQ9		VDDQ_9	G2
71	FBA_D<40>	FBA_D<40>	U11	DQ16/DQ8		VDDQ_11	G13
71	FBA_D<55>	FBA_D<55>	F13	DQ15/DQ23	6	VDDQ_24	H3
71	FBA_D<54>	FBA_D<54>	F11	DQ14/DQ22		VDDQ_32	H12
71	FBA_D<53>	FBA_D<53>	E13	DQ13/DQ21		VDDQ_25	K3
71	FBA_D<52>	FBA_D<52>	E11	DQ12/DQ20		VDDQ_33	K12
71	FBA_D<51>	FBA_D<51>	B13	DQ11/DQ19		VDDQ_10	L2
71	FBA_D<50>	FBA_D<50>	B11	DQ10/DQ18		VDDQ_12	L13
71	FBA_D<49>	FBA_D<49>	A13	DQ9/DQ17		VDDQ_4	M1
71	FBA_D<48>	FBA_D<48>	A11	DQ8/DQ16		VDDQ_26	M3
71	FBA_D<63>	FBA_D<63>	F2	DQ7/DQ31	7	VDDQ_34	M12
71	FBA_D<62>	FBA_D<62>	F4	DQ6/DQ30		VDDQ_18	M14
71	FBA_D<61>	FBA_D<61>	E2	DQ5/DQ29		VDDQ_14	N5
71	FBA_D<60>	FBA_D<60>	E4	DQ4/DQ28		VDDQ_8	N10
71	FBA_D<59>	FBA_D<59>	B2	DQ3/DQ27		VDDQ_5	P1
71	FBA_D<58>	FBA_D<58>	B4	DQ2/DQ26		VDDQ_27	P3
71	FBA_D<57>	FBA_D<57>	A2	DQ1/DQ25		VDDQ_35	P12
71	FBA_D<56>	FBA_D<56>	A4	DQ0/DQ24		VDDQ_19	P14
						VDDQ_6	T1
						VDDQ_28	T3
						VDDQ_36	T12
						VDDQ_20	T14
71	FBA_CMD<25>	FBA_CMD<25>	J5				C5
71	FBA_CMD<26>	FBA_CMD<26>	K4	A12/A13		VDD_14	C10
71	FBA_CMD<27>	FBA_CMD<27>	K5	A8/A7/A10/A0		VDD_3	D11
71	FBA_CMD<17>	FBA_CMD<17>	K10	A11/A6/A9/A1		VDD_5	G1
71	FBA_CMD<18>	FBA_CMD<18>	K11	BA1/A5/BA3/A3		VDD_1	G4
71	FBA_CMD<20>	FBA_CMD<20>	H10	BA2/A4/BA0/A2		VDD_9	G11
71	FBA_CMD<19>	FBA_CMD<19>	H11	BA3/A3/BA1/A5		VDD_6	G14
71	FBA_CMD<23>	FBA_CMD<23>	H5	BA0/A2/BA2/A4		VDD_12	L1
71	FBA_CMD<22>	FBA_CMD<22>	H4	A9/A1/A11/A6		VDD_2	L4
				A10/A0/A8/A7		VDD_10	L11
						VDD_7	L14
71	FBA_WCK67	FBA_WCK67	D4			VDD_13	P11
71	FBA_WCK67*	FBA_WCK67*	D5	WCK01/WCK23		VDD_8	R5
				WCK01#/WCK23#		VDD_11	R10
						VDD_4	
71	FBA_WCK45	FBA_WCK45	P4	WCK23/WCK01			A1
71	FBA_WCK45*	FBA_WCK45*	P5	WCK23#/WCK01#		VSSQ_1	A3
71	FBA_EDC<4>	FBA_EDC<4>	R2			VSSQ_25	A12
71	FBA_EDC<5>	FBA_EDC<5>	R13	EDC3/EDC0		VSSQ_31	A14
71	FBA_EDC<6>	FBA_EDC<6>	C13	EDC2/EDC1		VSSQ_18	C1
71	FBA_EDC<7>	FBA_EDC<7>	C2	EDC1/EDC2		VSSQ_2	C3
				EDC0/EDC3		VSSQ_26	C4
71	FBA_DBI<4>	FBA_DBI<4>	P2			VSSQ_24	C11
71	FBA_DBI<5>	FBA_DBI<5>	P13	DBI3#/DBI0#		VSSQ_11	C12
71	FBA_DBI<6>	FBA_DBI<6>	D13	DBI2#/DBI1#		VSSQ_32	C14
71	FBA_DBI<7>	FBA_DBI<7>	D2	DBI1#/DBI2#		VSSQ_19	E1
				DBI0#/DBI3#		VSSQ_3	E3
						VSSQ_27	E12
71	FBA_CMD<31>	FBA_CMD<31>	G3			VSSQ_33	E14
71	FBA_CMD<28>	FBA_CMD<28>	L3	RAS#/CAS#		VSSQ_20	F5
				CAS#/RAS#		VSSQ_16	F10
71	FBA_CMD<30>	FBA_CMD<30>	J3			VSSQ_7	H2
		FBA_CLK1*	J11	CKE#		VSSQ_9	H13
		FBA_CLK1	J12	CK#		VSSQ_14	K2
				CK		VSSQ_10	K13
71	FBA_CLK1*					VSSQ_15	M5
71	FBA_CLK1					VSSQ_17	M10
71	FBA_CMD<21>	FBA_CMD<21>	G12			VSSQ_8	N1
71	FBA_CMD<16>	FBA_CMD<16>	L12	CS#/WE#		VSSQ_4	N3
				WE#/CS#		VSSQ_28	N12
						VSSQ_34	N14
		FBA_ZQ_2B	J13	ZQ		VSSQ_21	R1
			J10	SEN		VSSQ_5	R3
						VSSQ_29	R4
71	FBA_CMD<29>	FBA_CMD<29>	J2			VSSQ_13	R11
			J1	RESET#		VSSQ_12	R12
				MF		VSSQ_35	R14
				[PH] Mirrored		VSSQ_22	U1
						VSSQ_6	U3
			A5			VSSQ_30	U12
			U5	NC_2		VSSQ_36	U14
				NC_1		VSSQ_23	
76	FBA_VREFD	FBA_VREFD	A10				B5
			U10	VREFD_1		VSS_14	B10
				VREFD_2		VSS_3	D10
						VSS_4	G5
			J14	VREFC		VSS_9	G10
76	FBA_VREFC	FBA_VREFC				VSS_5	H1
			J4	ABI#		VSS_1	H14
						VSS_12	K1
						VSS_2	K14
						VSS_13	L5
						VSS_10	L10
						VSS_6	P10
						VSS_7	T5
						VSS_11	T10
						VSS_8	

K4G80325FB-HC03
03V150000095

R7701 1 1% 2 40.2Ohm
R7702 1 1% 2 40.2Ohm
R7710 1 1% 2 121OHM
+FBVDDQ R7708 1% 1KOhm

C7701 10NF/25V X7R/+/-5%
C7713 820PF/50V X7R/+/-10% @
C7714 820PF/50V X7R/+/-10%

+FBVDDQ

22uFx3, 1uFx(10+8), 10uFx4
Place under VRAM

C7732 22UF/6.3V /VGA
C7733 22UF/6.3V /VGA
C7734 22UF/6.3V /VGA
C7715 1UF/6.3V /VGA
C7717 1UF/6.3V /VGA
C7718 1UF/6.3V /VGA
C7719 1UF/6.3V /VGA
C7720 1UF/6.3V /VGA
C7721 1UF/6.3V /VGA
C7722 1UF/6.3V /VGA
C7723 1UF/6.3V /VGA
C7724 1UF/6.3V /VGA
C7725 1UF/6.3V /VGA
C7704 1UF/6.3V /VGA
C7703 1UF/6.3V /VGA
C7706 1UF/6.3V /VGA
C7705 1UF/6.3V /VGA
C7709 1UF/6.3V /VGA
C7707 1UF/6.3V /VGA
C7708 1UF/6.3V /VGA
C7710 1UF/6.3V /VGA
C7726 10UF/6.3V /VGA
C7716 10UF/6.3V /VGA
C7727 10UF/6.3V /VGA
C7728 10UF/6.3V /VGA

10uFx2, 22uFx(2+3)
Place near VRAM

C7729 10UF/6.3V /VGA
C7730 10UF/6.3V /VGA
C7712 22UF/6.3V /VGA
C7731 22UF/6.3V /VGA
C7702 22UF/6.3V /VGA
C7735 22UF/6.3V /VGA
C7736 22UF/6.3V /VGA

PEGATRON Title : VGA_FBA_GDDR5
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: Kai_Shen

Size	Project Name	Rev
C	HE4EA	1.0

Date: Friday, April 07, 2017 Sheet 77 of 94

78 N/A

PEGATRON	Title : N/A		
BG1-HW RD	Engineer: *Kai_Shen*		
Size: A	Project Name: **HE4EA**		Rev: 1.0
Date: Wednesday, March 29, 2017	Sheet 78 of 94		

79 N/A

PEGATRON	Title : N/A	
BG1-HW RD	Engineer: *Kai_Shen*	
Size: A	Project Name: HE4EA	Rev: 1.0
Date: Wednesday, March 29, 2017	Sheet 79 of 94	

VCORE & VCCGT & VCCSA POWER SUPPLY

5 VR_SVID_DATA
5 VR_SVID_ALERT#
5 VR_SVID_CLK
3 VR_HOT#
25,74,92 VRM_PWRGD
30 CPU_VRON
93 CPU_VRON_PWR

SR8016 SR8017 SR8018

RIMON R8004 91KOhm vx_r0402_small 1%
C8145 470PF/50V vx_c0402_small 10%
R8070 12.1KOhm 1% vx_r0402_small
C8025 330PF/50V vx_c0402_small 10%
R8091 @ 220KOhm 1% vx_r0402_small
R8090 @ 13KOhm 1% vx_r0402_small
R8012 220KOhm 1%
C8024 8200PF/16V vx_c0402_small X7R/+/-10%
R8072 4.3KOhm 1% vx_r0402_small

R8021 499Ohm 1% vx_r0402_small
R8019 1.74KOhm 1% vx_r0402_small
R8022 2KOhm 1% vx_r0402_small
C8020 1000PF/50V vx_c0402_small 10%
C8021 330PF/50V vx_c0402_small 10%

+VCORE
5 VCORE_VCCSENSE
5 VCORE_VSSSENSE
R8010 @ 100Ohm vx_r0402_small
nb_r0402_short_5mil_small
SR8008 nb_r0402_short_5mil_small
SR8007
R8013 @ 100Ohm vx_r0402_small
C8002 @ 0.01UF/16V vx_c0402_small 10%
C8017 @ 0.01UF/16V vx_c0402_small 10%
C8012 0.01UF/16V vx_c0402_small 10%

ISUMP_B
RNTCS R8040 4.7KOhm vx_r0402_small 1%
RP R8037 11KOhm vx_r0402_small 1%
RNTC R8042 10KOHM vx_r0402_h24_small 5%
The R8042 closes to L8000 for +VCORE
SR8004 nb_r0402_short_5mil_small
ISUMN_B
T8001 TPC22T
CN1 C8042 0.027UF/25V vx_c0402_small X7R/+/-10%
CN2 C8046 0.047UF/25V vx_c0402_small X7R/+/-10%
C8044 0.1UF/25V vx_c0402_small X7R/+/-10%
C8039 @ 0.22UF/16V vx_c0402_small X7R/+/-10%
Ri R8033 442Ohm vx_r0402_small 1%
Rip R8030 2.49KOhm vx_r0402_small 1%
Cip C8033 2200PF/50V vx_c0402_small 10%
C80133 /U42 0.022UF/16V vx_c0402_small 10%
C80134 /U42 0.022UF/16V vx_c0402_small 10%

R8063 /U22 0Ohm vx_r0402_0ohm_small
R8064 /U22 0Ohm vx_r0402_0ohm_small
ISEN2_B
ISEN1_B
+5VS

SR8001 nb_r0603_short_32mil_small
C8011 1UF/6.3V vx_c0402_small X5R/+/-10%
C8023 0.22UF/25V vx_c0603_small X7R/+/-10%
+5VS
+AC_BAT_SYS

U8000A ISL95859AHRTZ
PSYS IMON_B NTC_B COMP_B FB_B RTN_B ISUMP_B ISUMN_B ISEN1_B ISEN2_B
FCCM_B PWM1_B PWM2_B IMON_A NTC_A FB_A RTN_A ISUMP_A ISUMN_A
GND VR_ENABLE VR_READY SCLK SDATA ALERT# VCC PRODI PROGB
PWM_C FCCM_C ISUMN_C ISUMP_C RTN_C FB_C COMP_C IMON_C PWM_A FCCM_A
PWM_C FCCM_C

R8018 9.31KOhm vx_r0402_small 1%
R8024 100KOhm vx_r0402_small 1%

Rip R8029 1KOhm vx_r0402_small 1%
Cip C8036 2.2NF/50V vx_c0402_small X5R/+/-10%
Ri R8034 422Ohm vx_r0402_small 1%
CN2 C8038 4700PF/50V vx_c0402_small X7R/+/-10%
C80148 @ 6800PF/25V vx_c0402_small X7R/+/-10%
CN1 C8043 0.068UF/25V vx_c0402_small X5R/+/-10%

C8041 0.1UF/25V vx_c0402_small X7R/+/-10%
T8002 TPC22T
ISUMN_C
SR8019 nb_r0402_short_5mil_small
RN
R8043 10KOHM vx_r0402_h24_small
RNTC
R8036 RP 11KOhm vx_r0402_small 1%
RNTCS R8039 4.7KOhm vx_r0402_small 1%
The R8043 closes to L8002 for VCCSA
ISUMP_C
SR8010 nb_r0402_short_5mil_small
VCCSA_VSSSENSE 7
SR8009 nb_r0402_short_5mil_small
VCCSA_VCCSENSE 7

RIMON R8003 95.3KOhm vx_r0402_small 1%
C8000 330PF/50V vx_c0402_small 10%
R8014 1KOhm vx_r0402_small 1%
Rdroop R8025 1.74KOhm vx_r0402_small 1%
R8015 301Ohm vx_r0402_small 1%
C8022 1000PF/50V vx_c0402_small 10%
C8006 220PF/50V vx_c0402_small 10%
C80127 18PF/50V vx_c0402_small 5%
R8074 4.3OHM vx_r0402_small 1%
C80126 6800PF/25V vx_c0402_small X7R/+/-10%
C8004 @ 0.01UF/16V vx_c0402_small 10%
C8008 @ 220PF/50V vx_c0402_small 10%
C8014 220PF/50V vx_c0402_small 10%
R8016 @ 100Ohm vx_r0402_small 1%
R8023 @ 100Ohm vx_r0402_small 1%
+VCCSA

Rip R8031 1KOhm vx_r0402_small 1%
Cip C8035 2200PF/50V vx_c0402_small 10%
Ri R8032 422Ohm vx_r0402_small 1%

C8040 0.1UF/25V vx_c0402_small X7R/+/-10%
T8000 TPC22T
ISUMN_A
SR8006 nb_r0402_short_5mil_small
RN
R8041 10KOHM vx_r0402_h24_small
RNTC
RNTCS R8038 4.7KOhm vx_r0402_small 1%
The R8041 closes to L8001 for +VCCGT
CN2 C8037 @ 0.22UF/16V vx_c0402_small X7R/+/-10%
C80147 0.047UF/25V vx_c0402_small X7R/+/-10%
CN1 C8045 0.027UF/25V vx_c0402_small X7R/+/-10%
RP R8035 11KOhm vx_r0402_small 1%
ISUMP_A

FCCM_B
PWM1_B
PWM2_B

R8020 301Ohm vx_r0402_small 1%
C8013 1200PF/50V vx_c0402_small X7R/+/-10%
R8028 2KOhm vx_r0402_small 1%
Rdroop R8017 2.15KOhm vx_r0402_small 1%
C8018 1000PF/50V vx_c0402_small 10%
SR8012 VCCGT_VCCSENSE 6
SR8011 VCCGT_VSSSENSE 6
C8001 @ 0.01UF/16V vx_c0402_small 10%
C8007 @ 220PF/50V vx_c0402_small 10%
C8015 220PF/50V vx_c0402_small 10%
R8027 @ 100Ohm vx_r0402_small 1%
R8026 @ 100Ohm vx_r0402_small 1%
+VCCGT

R8003 102KOhm vx_r0402_small 1%
R8001 102KOhm vx_r0402_small 1%
C8003 330PF/50V vx_c0402_small 10%
R8011 220KOhm vx_r0402_small 1%
R8081 @ 13KOhm vx_r0402_small 1%
R8084 @ 220KOhm vx_r0402_small 1%
C8025 22PF/50V vx_c0402_small 5%
C8026 6800PF/25V vx_c0402_small X7R/+/-10%
R8073 2.74KOhm vx_r0402_small 1%

U8000B ISL95859AHRTZ
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8
PGND8 PGND7 PGND6 PGND5 PGND4 PGND3 PGND2 PGND1
U8002B SIC634CD-T1-GE3
U8003B SIC634CD-T1-GE3
U8006B /U42 SIC634CD-T1-GE3

Iin=0.73A

VCCSA_HG
SR8000 nb_r0603_short_32mil_small
VCCSA_BST_R 2
C8048 0.22UF/25V vx_c0603_small X7R/+/-10%
C8059 @ 1000PF/50V vx_c0402_small 5%
C8053 10UF/25V vx_c0603_h39_small X5R/+/-20%
Q8000 PMPB20EN
VCCSA_BST
PWM_C
U8005 ISL95808HRZ
UGATE BOOT PWM GND1 PHASE FCCM VCC LGATE GND2
VCCSA_LG
Q8001 PMPB20EN
FCCM_C
+5VS
C8016 4.7UF/10V vx_c0402_h26_small X5R/+/-10%
VCCSA_LX
T8003 TPC22T 0.47uH Irat=18A
DCR=3.67mohm
063T
JP8000 SHORT_PIN
JP8001 SHORT_PIN
L8002
R8057 @ 2.2Ohm vx_r0805_h24_small 5%
VCCSA_RC
C8028 @ 1500PF/50V vx_c0402_small X7R/+/-10%
R8045 3.65KOHM vx_r0402_small 1%
ISUMP_C
ISUMN_C
VCCSA_LX_S
VCCSA_S
R8050 1Ohm vx_r0402_small 1%
C80139 /U42 22UF/6.3V X5R/+/-10% vx_c0603_h39_small
C80051 22UF/6.3V X5R/+/-10% vx_c0603_h39_small
C8031 22UF/6.3V X5R/+/-10% vx_c0603_h39_small
C8032 22UF/6.3V X5R/+/-10% vx_c0603_h39_small
C8049 22UF/6.3V X5R/+/-10% vx_c0603_h39_small
C8034 22UF/6.3V X5R/+/-10% vx_c0603_h39_small
C8010 22UF/6.3V X5R/+/-10% vx_c0603_h39_small
+VCCSA

U22
VCCSA
VID1 : 0.9V
VBoot : 1.05V
Iccmax = 4.5A
PL2 TDC = 4A
LL=10.3mV/A
Output Cap.
22uF/6.3V*6pcs

U42
VCCSA
VID1 : 0.9V
VBoot : 1.05V
Iccmax = 5A
LL=10.3mV/A
Output Cap.
22uF/6.3V*7pcs

Iin=2.25A

R8062 2.2Ohm vx_r0603_h28_small 1%
C8047 0.22UF/25V vx_c0603_small 10%
VCCGT_BST_R 2
VCCGT_BST
+5VS
R8076 1Ohm vx_r0402_small 1%
FCCM_A
PWM_A
U8003A SIC634CD-T1-GE3
VIN1 PHASE NC2 BOOT NC1 VCC FCCM PWM
AGND GL2 NC4 PVCC PGND2 GL1 SW10 SW9
VIN2 PGND1
SW1 SW2 SW3 SW4 SW5 SW6 SW7 SW8
C8009 1UF/25V vx_c0402_h24_small X5R/+/-10%
C8140 1UF/25V vx_c0402_h24_small X5R/+/-10%
C8058 @ 1000PF/50V vx_c0402_small 5%
C8050 10UF/25V vx_c0603_h39_small X5R/+/-20%
C8065 10UF/25V vx_c0603_h39_small X5R/+/-20%
C80144 10UF/25V vx_c0603_h39_small X5R/+/-20%
AC_BAT_SYS
VCCGT_LX
T8004 TPC28T
L8001 0.15uH Irat=37A
DCR=0.9mohm
063T
+VCCGT
R8056 @ 2.2Ohm vx_r0805_h24_small 5%
VCCGT_RC
C8029 @ 1500PF/50V vx_c0402_small X7R/+/-10%
JP8006 SHORT_PIN
JP8003 SHORT_PIN
CE8002 470uF/2V vx_c7343d_apaq_t03
R8049 3.65K vx_r0603_h24_small 1%
ISUMP_A
VCCGT_LX_S
ISUMN_A
VCCGT_S
R8053 1Ohm vx_r0402_small 1%

C8062 C80102 C80106 C8068 C80112 C8089 C80113 C80119 C80114 C8055 C8091 C8090
C8064 C8056 C8060 C8067 C80125 C80118 @ C80121 C80117 @ C8087 C8092 C80105 C8084
C8086 C8085 C8083 C8066 C8073 C8074
22UF/6.3V X5R/+/-20% vx_c0603_h39_small

U22
VCCGT
VID1 : 0.9V
Vboot : 0V
Iccmax = 21A
PL2 TDC =18A
LL=3.1mV/A
Output Cap.
22uF/6.3V*28pcs
470uF/2V*1pcs

U42
VCCGT
VID1 : 0.9V
Vboot : 0V
Iccmax = 28A
PL2 TDC =12A
LL=3.1mV/A
Output Cap.
22uF/6.3V*28pcs
470uF/2V*1pcs

Iin=2.625A

R8006 /U42 2.2Ohm vx_r0603_h28_small 1%
C80153 /U42 0.22UF/25V vx_c0603_small 10%
VCORE2_BST_R 2
VCORE2_BST
+5VS
R8051 /U42 1Ohm vx_r0402_small 1%
FCCM_B
PWM2_B
U8006A /U42 SIC634CD-T1-GE3
C80142 /U42 1UF/25V vx_c0402_h24_small X5R/+/-10%
C80132 /U42 1UF/25V vx_c0402_h24_small X5R/+/-10%
C80153(5) /U42 1000PF/50V vx_c0402_small 5%
C80141 /U42 10UF/25V vx_c0603_h39_small X5R/+/-20%
C80143 /U42 10UF/25V vx_c0603_h39_small X5R/+/-20%
AC_BAT_SYS
VCORE2_LX
T8007 TPC28T
L8003 /U42 0.15uH Irat=37A
DCR=0.9mohm
063T
+VCORE
R8092 @ 2.2Ohm vx_r0805_h24_small 5%
VCORE2_RC
C80154 @ 1500PF/50V vx_c0402_small X7R/+/-10%
JP8009 SHORT_PIN
JP8008 SHORT_PIN
CE8000 /U42 470uF/2V vx_c7343d_apaq_t03
R8007 /U42 3.65K vx_r0603_h24_small 1%
ISUMP_B
R8008 /U42 100KOhm vx_r0402_small 1%
ISEN2_B
VCORE2_LX_S
ISUMN_B
VCORE2_S
R8002 /U42 1Ohm vx_r0402_small 1%

C80110 C80109 C80107 C80093 C80094 C80095 C80096 C80097 C80098 C80081
C80116 C80123 C80128 C8099 C80100 C80101 C80124 C80103 C80104 C80080
C80111 C80108 C8079 C8078 C8082 C80149 C80150 C8071 C8072 C8069
22UF/6.3V X5R/+/-20% vx_c0603_h39_small

U22
VCORE
VID1 : 0.9V
VBoot : 0V
Imcmax = 29A
PL2 TDC=21A
LL=2.4mV/A
Output Cap.
22uF/6.3V*30pcs

U42
VCORE
VID1 : 0.9V
VBoot : 0V
Iccmax = 64A
PL2 TDC=42A
LL=2.4mV/A
Output Cap.
22uF/6.3V*30pcs
470uF/2V*2pcs

Iin=2.625A

R8061 2.2Ohm vx_r0603_h28_small 1%
C8046 0.22UF/25V vx_c0603_small 10%
VCORE1_BST_R 2
VCORE1_BST
+5VS
R8009 1Ohm vx_r0402_small 1%
FCCM_B
PWM1_B
U8002A SIC634CD-T1-GE3
C8019 1UF/25V vx_c0402_h24_small X5R/+/-10%
C80131 1UF/25V vx_c0402_h24_small X5R/+/-10%
C8061 @ 1000PF/50V vx_c0402_small 5%
C8057 10UF/25V vx_c0603_h39_small X5R/+/-20%
C8052 10UF/25V vx_c0603_h39_small X5R/+/-20%
C8063 10UF/25V vx_c0603_h39_small X5R/+/-20%
AC_BAT_SYS
VCORE1_LX
T8006 TPC28T
L8000 0.15uH Irat=37A
DCR=0.9mohm
063T
+VCORE
R8054 @ 2.2Ohm vx_r0805_h24_small 5%
VCORE1_RC
C8030 @ 1500PF/50V vx_c0402_small X7R/+/-10%
JP8007 SHORT_PIN
JP8002 SHORT_PIN
CE8008 /U42 470uF/2V vx_c7343d_apaq_t03
R8047 3.65K vx_r0603_h24_small 1%
ISUMP_B
R8005 /U42 100KOhm vx_r0402_small 1%
ISEN1_B
VCORE1_LX_S
ISUMN_B
VCORE1_S
R8052 1Ohm vx_r0402_small 1%

C80110 C80109 C80107 C80093 C80094 C80095 C80096 C80097 C80098 C80081
C80116 C80123 C80128 C8099 C80100 C80101 C80124 C80103 C80104 C80080
C80111 C80108 C8079 C8078 C8082 C80149 C80150 C8071 C8072 C8069
22UF/6.3V X5R/+/-20% vx_c0603_h39_small

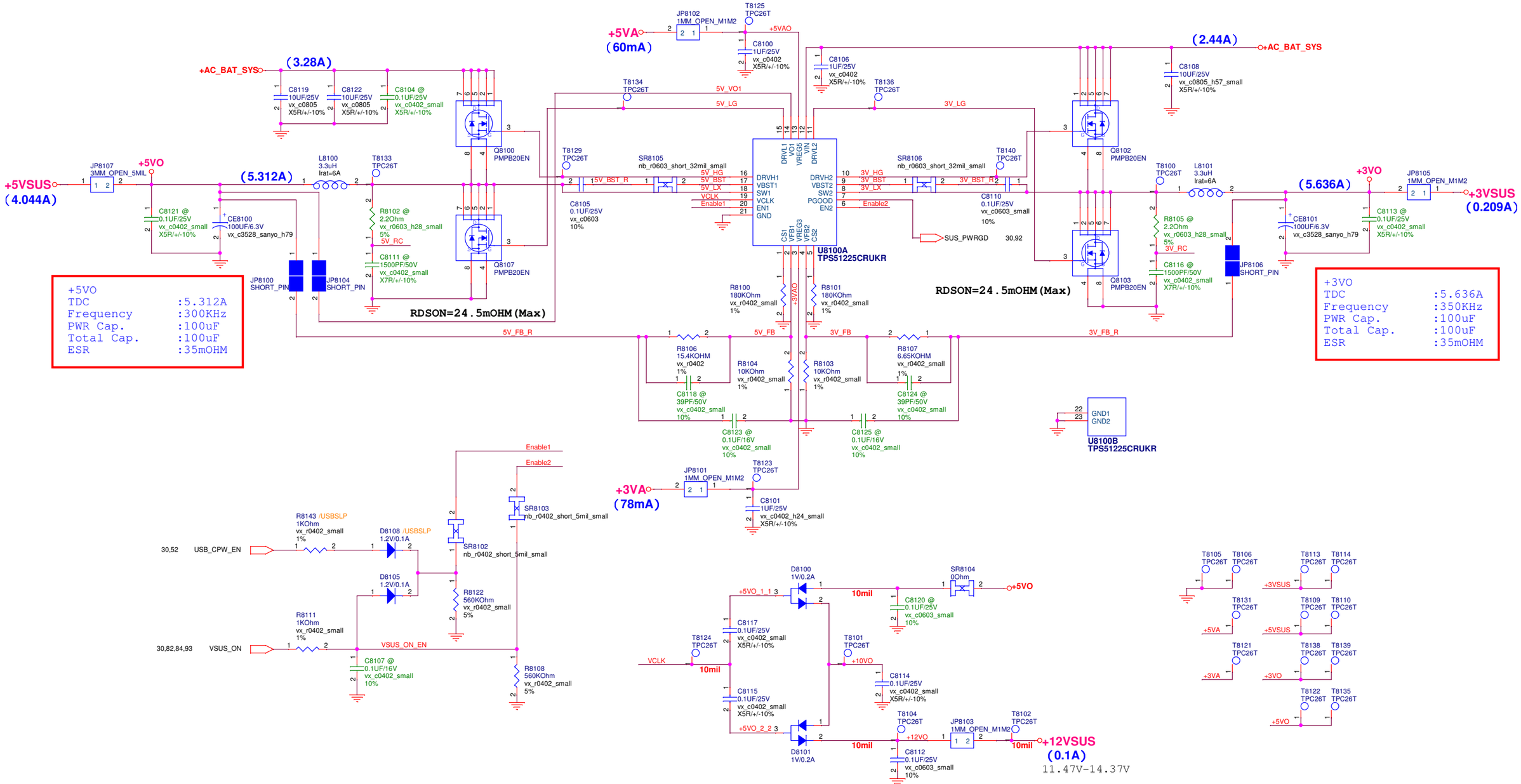
U22
VCORE
VID1 : 0.9V
VBoot : 0V
Iccmax = 29A
PL2 TDC=21A
LL=2.4mV/A
Output Cap.
22uF/6.3V*30pcs

U42
VCORE
VID1 : 0.9V
VBoot : 0V
Iccmax = 64A
PL2 TDC=42A
LL=2.4mV/A
Output Cap.
22uF/6.3V*30pcs
470uF/2V*2pcs

<Variant Name>

PEGATRON Title : POWER_VCORE
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin
Size Custom | Project Name HE4EA | Rev 1.1
Date: Wednesday, March 29, 2017 | Sheet 80 of 94

5VO & 3VO POWER SUPPLY



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

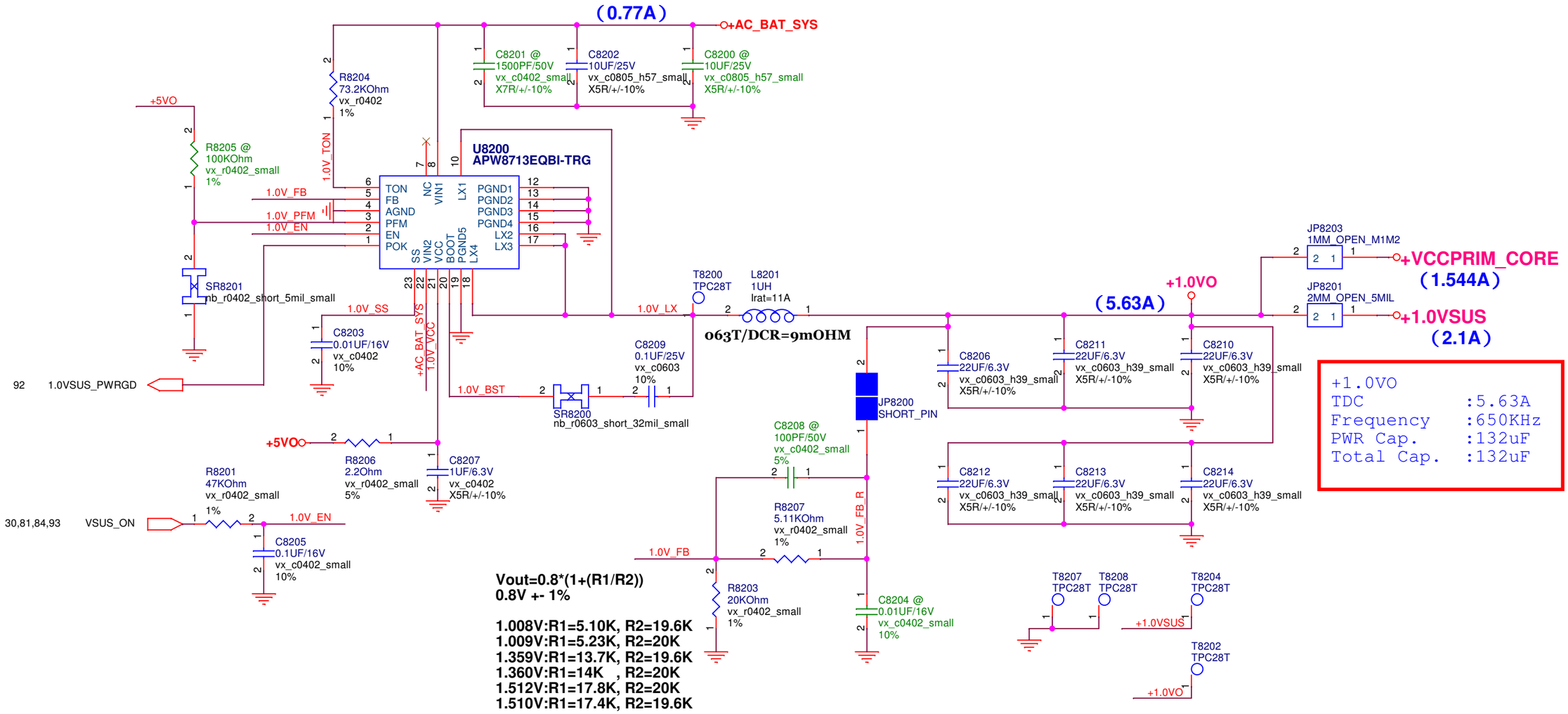
Title : POWER_SYSTEM

Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 81 of 94

+1.0VSUS POWER SUPPLY



+1.0VO
TDC :5.63A
Frequency :650KHz
PWR Cap. :132uF
Total Cap. :132uF

Vout=0.8*(1+(R1/R2))
0.8V +- 1%

1.008V:R1=5.10K, R2=19.6K
1.009V:R1=5.23K, R2=20K
1.359V:R1=13.7K, R2=19.6K
1.360V:R1=14K , R2=20K
1.512V:R1=17.8K, R2=20K
1.510V:R1=17.4K, R2=19.6K

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

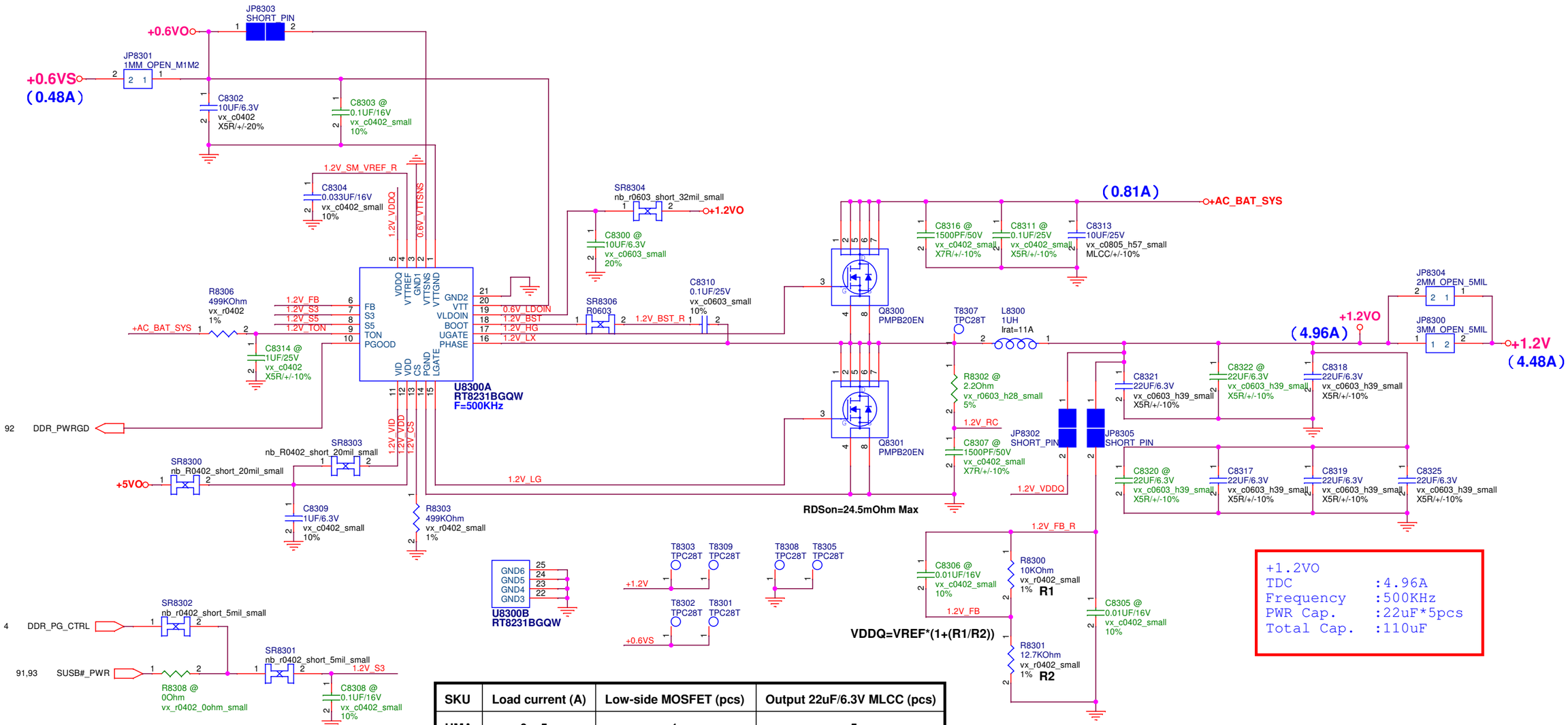
Title : P82_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 82 of 94

DDR & VTT POWER SUPPLY



SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

VID	Reference Voltage (V)
High	0.675
Low	0.75

```
+1.2VO
TDC          :4.96A
Frequency    :500KHz
PWR Cap.     :22uF*5pcs
Total Cap.   :110uF
```

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

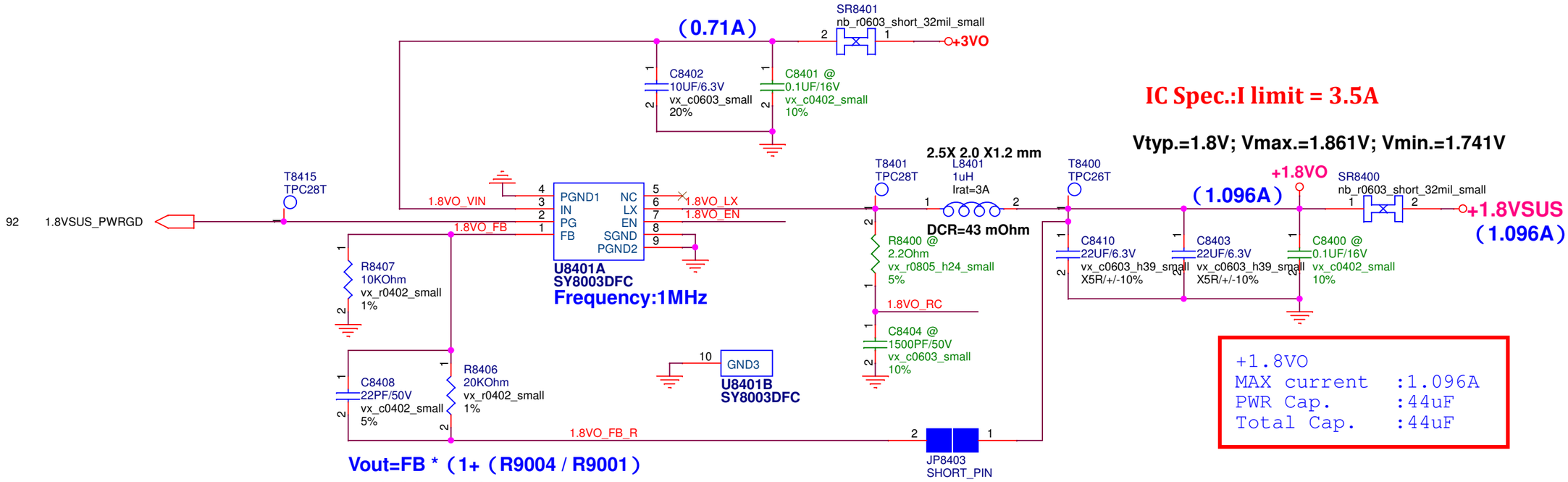
Title : POWER_DDR & VTT

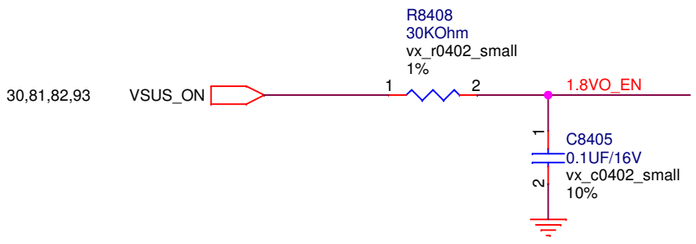
Engineer: Adams Lin

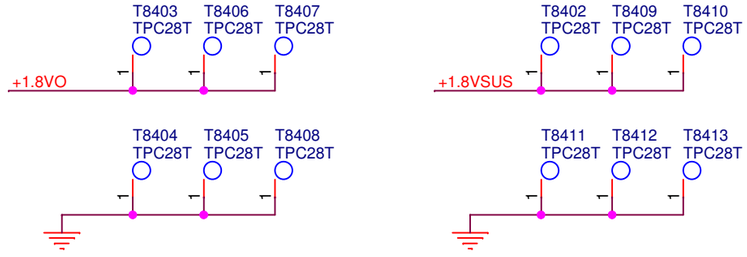
Size	Project Name	Rev
Custom	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 83 of 94

1.8VSUS POWER SUPPLY







<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

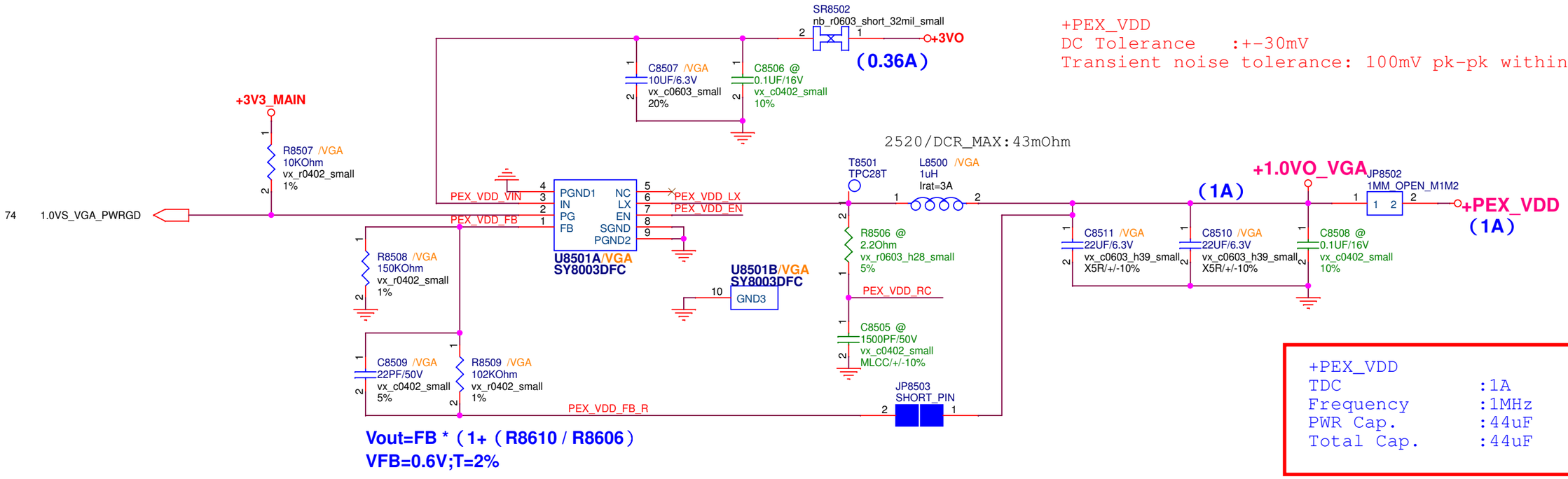
Title : POWER_1.8VSUS

Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

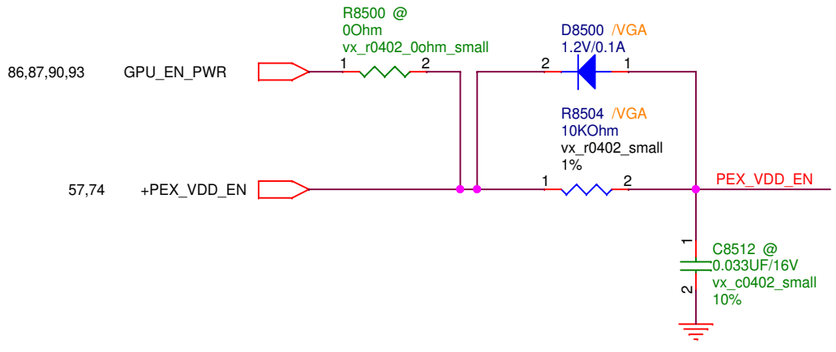
Date: Wednesday, March 29, 2017 Sheet 84 of 94

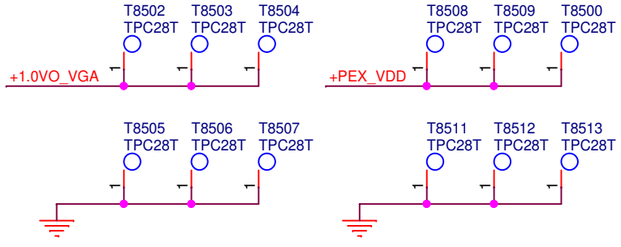
PEX_VDD POWER SUPPLY



+PEX_VDD
DC Tolerance :+-30mV
Transient noise tolerance: 100mV pk-pk within 20MHz BW

+PEX_VDD	
TDC	:1A
Frequency	:1MHz
PWR Cap.	:44uF
Total Cap.	:44uF





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

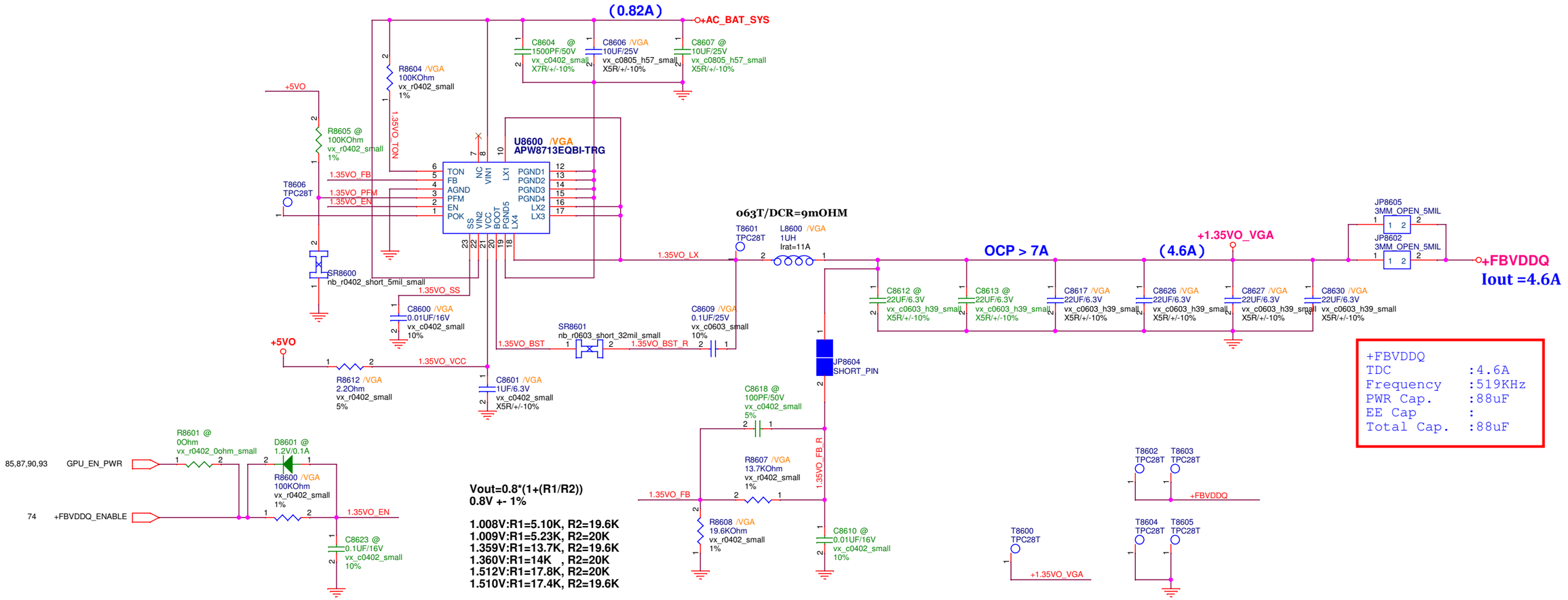
Title : POWER_PEX_VDD

Engineer: Adams Lin

Size	Project Name	Rev
B	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 85 of 94

FBVDDQ POWER SUPPLY



+FBVDDQ
TDC :4.6A
Frequency :519KHz
PWR Cap. :88uF
EE Cap :
Total Cap. :88uF

Vout=0.8*(1+(R1/R2))
0.8V +- 1%

1.008V:R1=5.10K, R2=19.6K
1.009V:R1=5.23K, R2=20K
1.359V:R1=13.7K, R2=19.6K
1.360V:R1=14K , R2=20K
1.512V:R1=17.8K, R2=20K
1.510V:R1=17.4K, R2=19.6K

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_FBVDDQ
Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 86 of 94

VGA_CORE POWER SUPPLY

	N17S_G1
R8723	6.19K
R8721	20.5K
R8716	4.32K
R8715	16.5K
R8717	309
C8720	4.7nF
Vstep	6.25mV
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V

VGA_PSI#	VO_action
~ 0.4V	1 Phase DEM
0.7 ~ 0.88V	1 Phase FCCM
1.08 ~ 1.35V	2 Phase FCCM
1.6V ~	2 Phase FCCM

+VGA_VCORE(Package type:N17VS-G1)
DC Tolerance :+-20mV

Overshoot/undershoot
Transient noise tolerance: -10% ~ +20% within 20MHz BW
High frequency noise: 400mV pk-pk within 1GHz BW

VID:0.6V ~ 1.2V
Number of programmable Volt: 96 levels
Programmable volt steps: 6.25mV
Settling Time: < 100us for rising, no restriction on falling

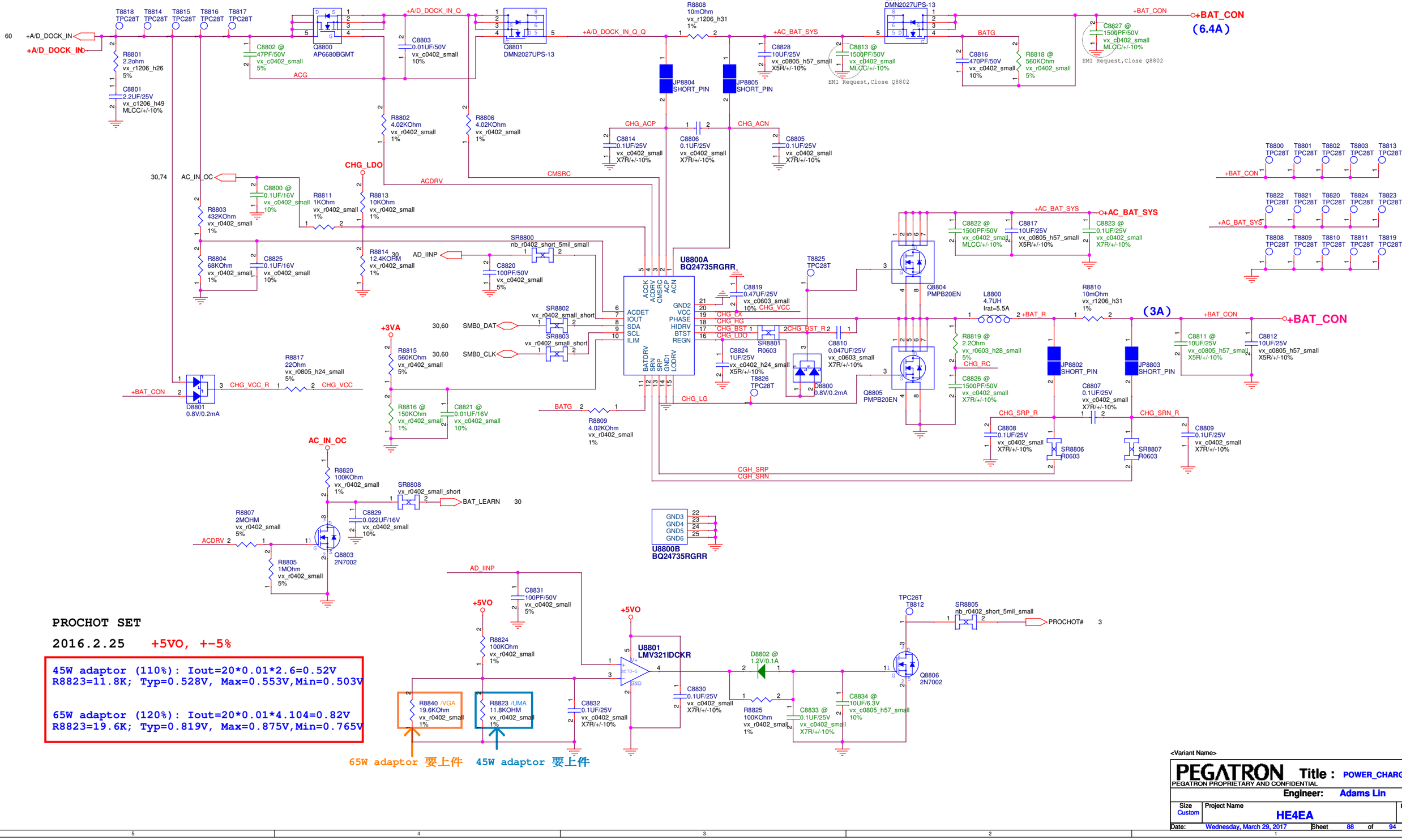
+NVVDD (2 Phase)
TDC :27.9A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

2 PHASE 25W
N17S-G1
TDC=27.9A
OCP:62A

<Variant Name>

PEGATRON Title : POWER_VGA
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Adams Lin
Size: Custom | Project Name: HE4EA | Rev: 1.1
Date: Wednesday, March 29, 2017 | Sheet 87 of 94

BATTERY CHARGER



PROCHOT SET

2016.2.25 **+5VO, +-5%**

45W adaptor (110%): Iout=20*0.01*2.6=0.52V
R8823=11.8K; Typ=0.528V, Max=0.553V,Min=0.503V

65W adaptor (120%): Iout=20*0.01*4.104=0.82V
R8823=19.6K; Typ=0.819V, Max=0.875V,Min=0.765V

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_CHARGER

Engineer: Adams Lin

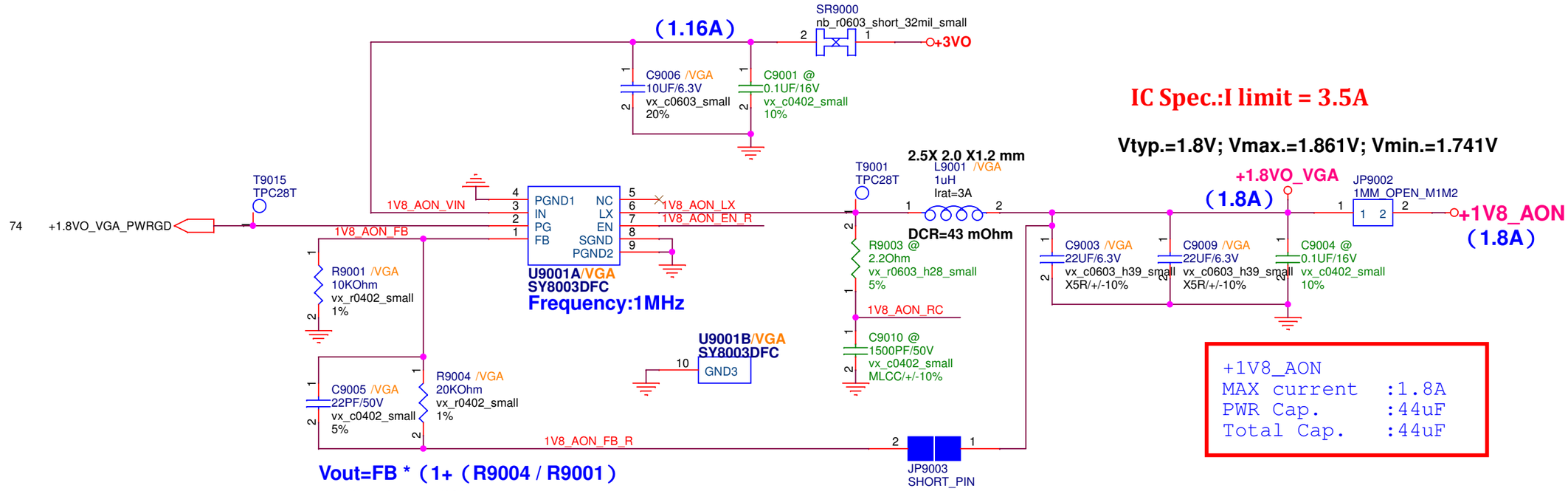
Size	Project Name	Rev
Custom	HE4EA	1.1

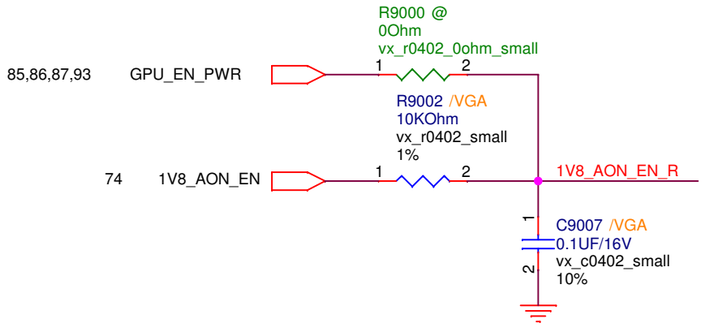
Date: Wednesday, March 29, 2017 Sheet 88 of 94

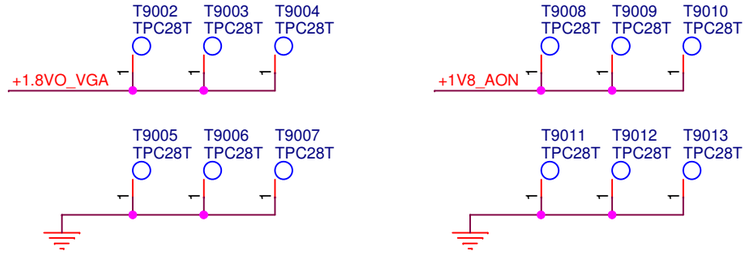
89 N/A

PEGATRON	Title : N/A	
BG1-HW RD	Engineer: *Kai_Shen*	
Size: A	Project Name: HE4EA	Rev: 1.0
Date: Wednesday, March 29, 2017	Sheet 89 of 94	

1V8_AON POWER SUPPLY







<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

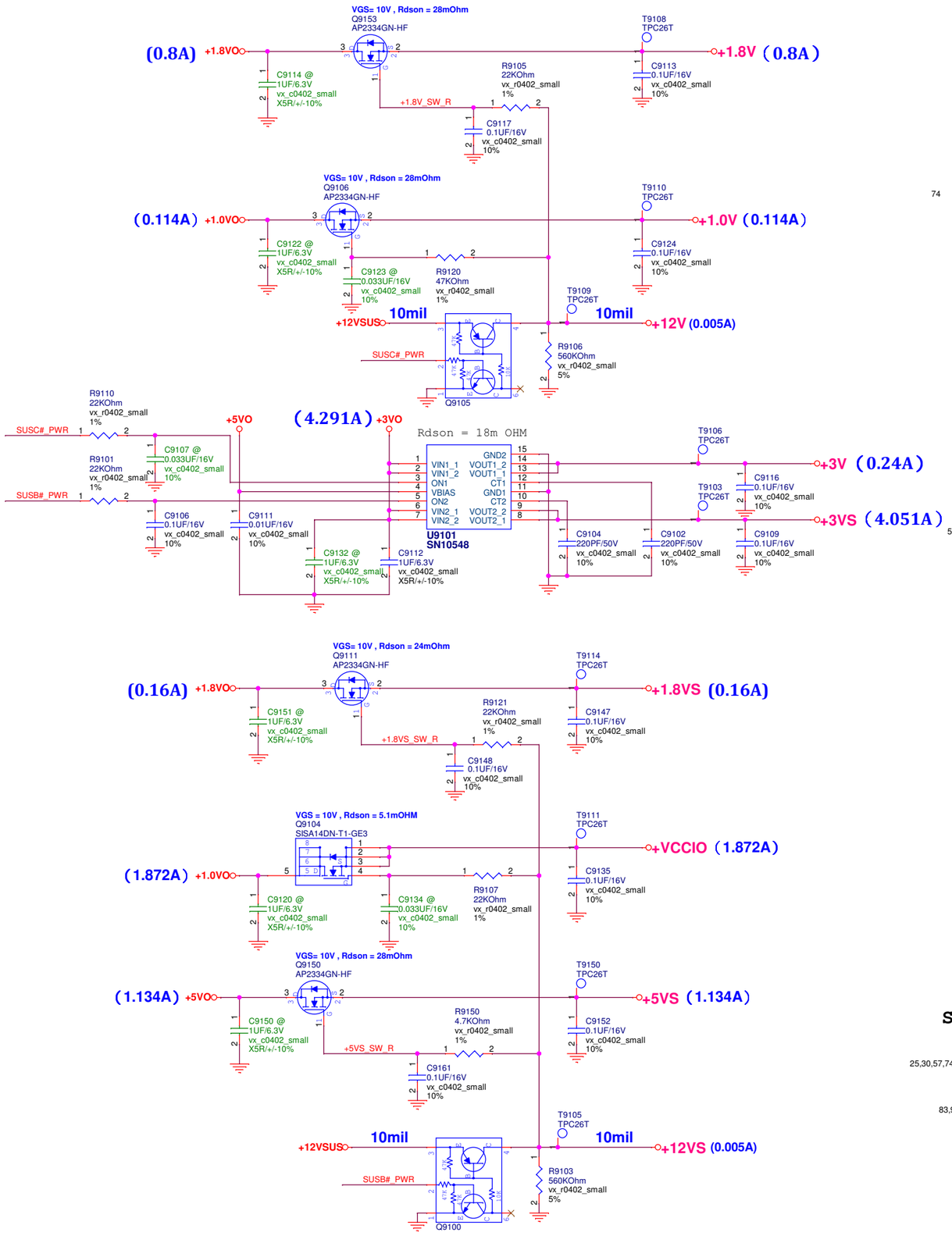
Title : +1V8_AON

Engineer: Adams Lin

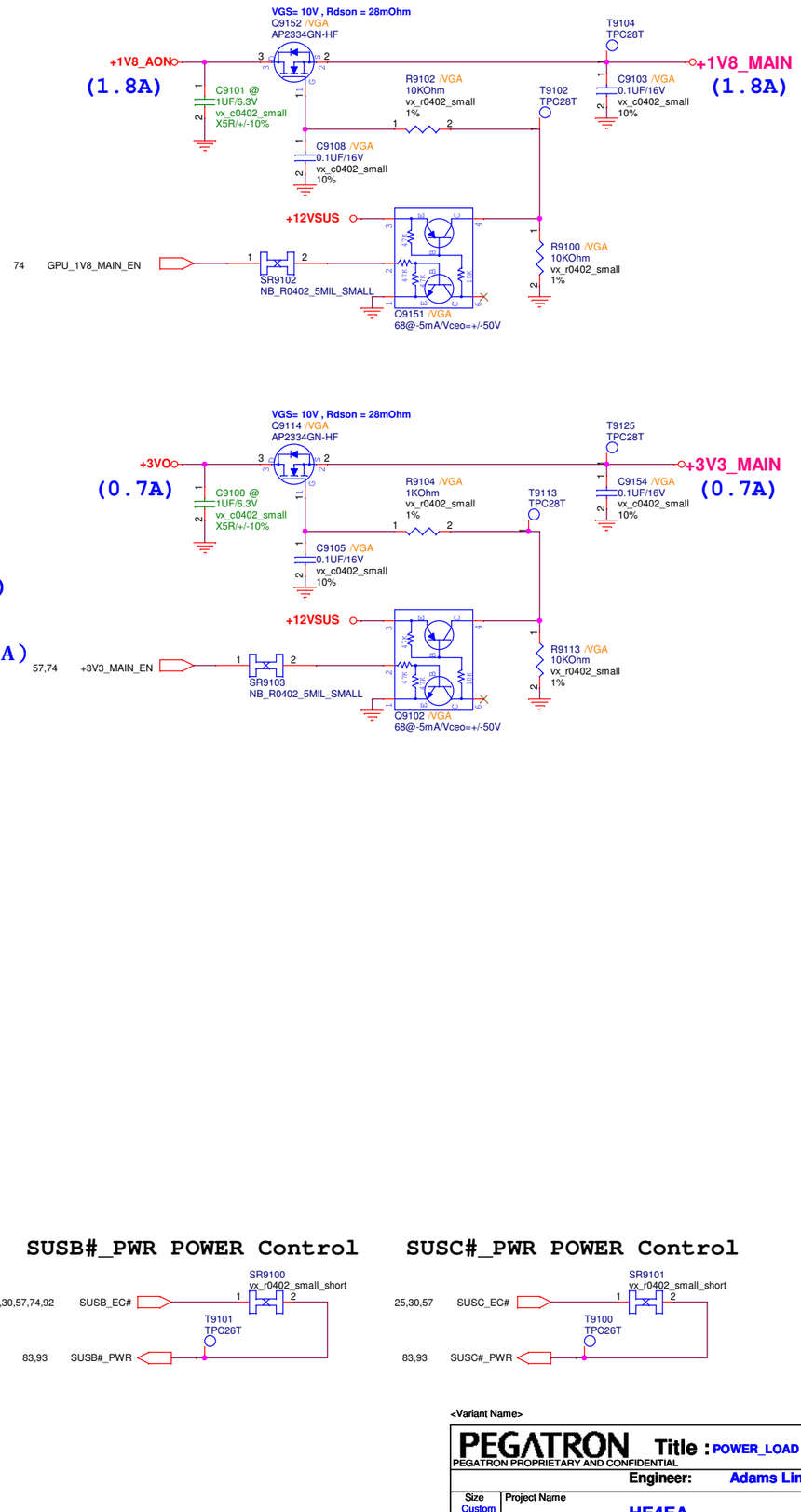
Size	Project Name	Rev
Custom	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 90 of 94

SUSB#_PWR POWER
SUSC#_PWR POWER



DSC_VGA_PWR POWER



SUSB#_PWR POWER Control

SUSC#_PWR POWER Control

<Variant Name>

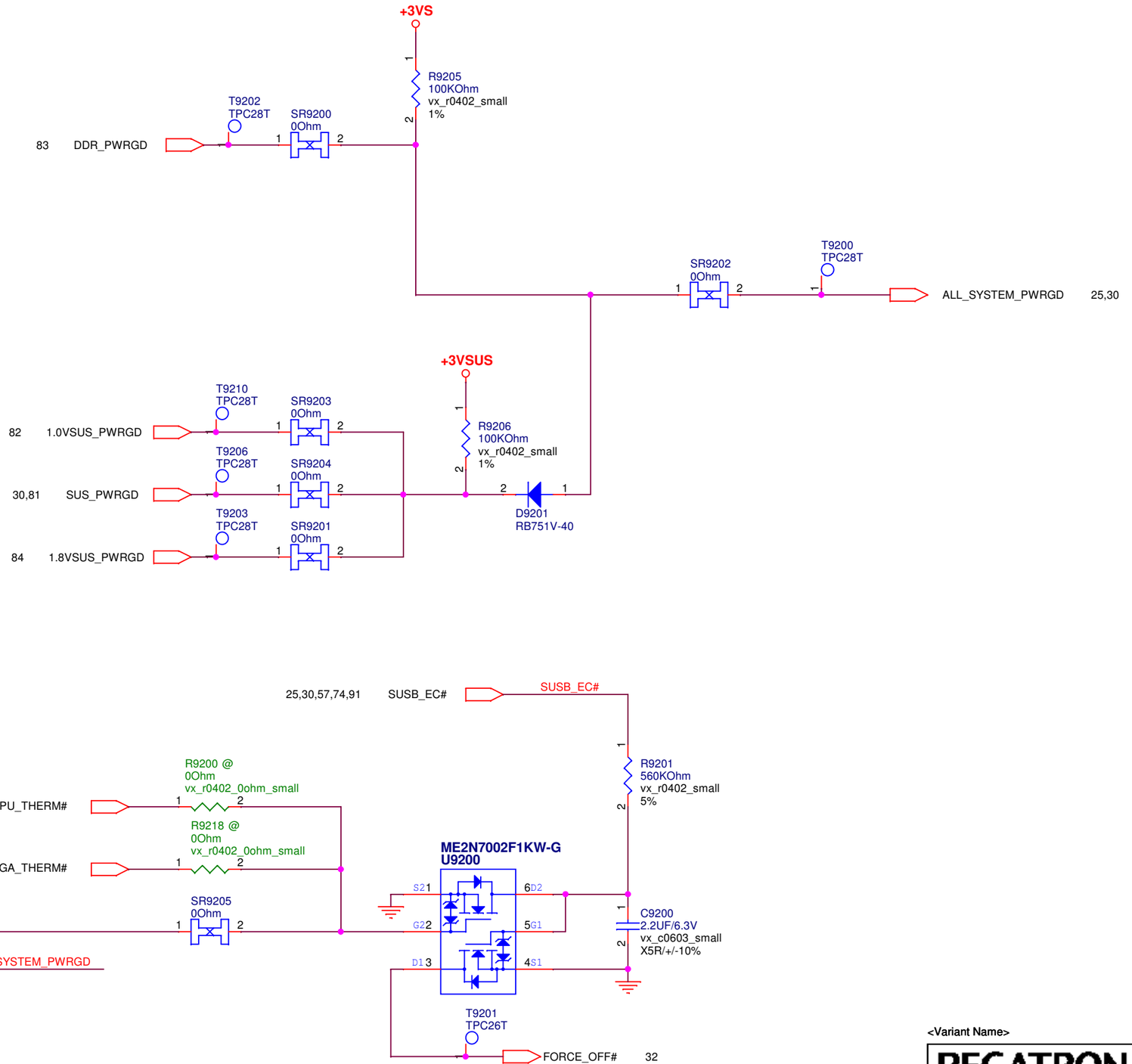
PEGATRON Title : POWER_LOAD SWITCH

Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

Date: Wednesday, March 29, 2017 Sheet 92 of 94

+A/D_DOCK_IN — +A/D_DOCK_IN 60,88
+BAT_CON — +BAT_CON 60,88
+AC_BAT_SYS — +AC_BAT_SYS 45,80,81,82,83,86,87,88

+5VA — +5VA 64,81
+3VA — +3VA 24,28,30,31,36,53,57,67,81,88

+5VO — +5VO 81,82,83,86,88,91
+3VO — +3VO 74,81,84,85,90,91
+1.8VO — +1.8VO 84,91
+1.8VO_VGA — +1.8VO_VGA 90
+1.35VO_VGA — +1.35VO_VGA 86
+1.2VO — +1.2VO 83
+1.0VO — +1.0VO 82,91
+1.0VO_VGA — +1.0VO_VGA 85
+0.6VO — +0.6VO 83

+12VSUS — +12VSUS 28,49,81,91
+5VSUS — +5VSUS 41,52,64,81
+3VSUS — +3VSUS 4,20,21,22,23,24,25,26,28,30,31,41,51,53,62,74,81,92
+1.8VSUS — +1.8VSUS 9,24,26,84
+1.0VSUS — +1.0VSUS 26,82

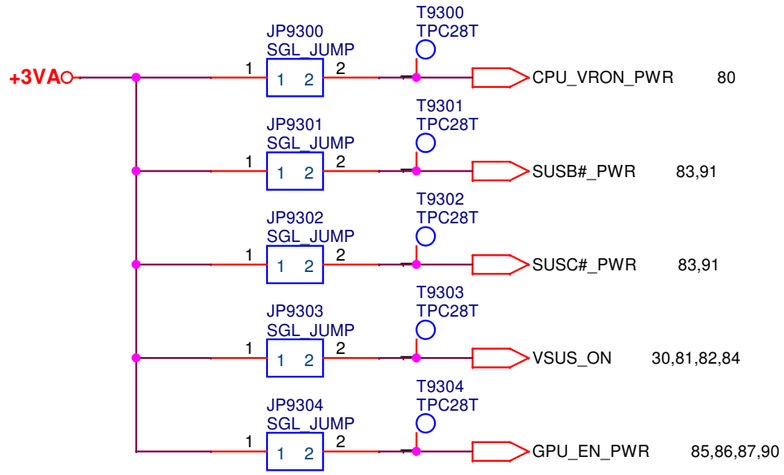
+12V — +12V 4,57,91
+3V — +3V 25,31,45,57,91
+1.8V — +1.8V 16,57,91
+1.2V — +1.2V 4,7,16,17,18,57,83
+1.0V — +1.0V 3,5,7,9,25,32,57,91

+12VS — +12VS 31,57,91
+5VS — +5VS 31,36,45,48,50,57,69,80,87,91
+3VS — +3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,74,87,91,92
+1.8VS — +1.8VS 36,49,57,91
+0.6VS — +0.6VS 16,17,57,83

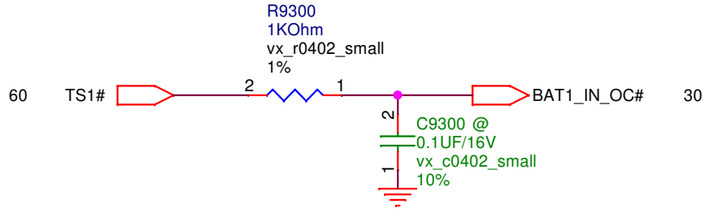
+VCCPRIM_CORE — +VCCPRIM_CORE 26,82
+VCCIO — +VCCIO 3,5,7,9,57,91
+VCCSA — +VCCSA 7,80
+VCCGT — +VCCGT 6,80
+VCORE — +VCORE 5,6,80

+3V3_MAIN — +3V3_MAIN 57,74,85,91
+1V8_AON — +1V8_AON 57,70,72,74,75,87,90,91
+1V8_MAIN — +1V8_MAIN 57,70,71,72,74,75,91
+FBVDDQ — +FBVDDQ 57,71,75,76,77,86
+PEX_VDD — +PEX_VDD 57,70,71,72,85
+NVVDD — +NVVDD 57,75,87

FOR POWER TEST



BATTERY IN DETECT



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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SIGNAL
Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

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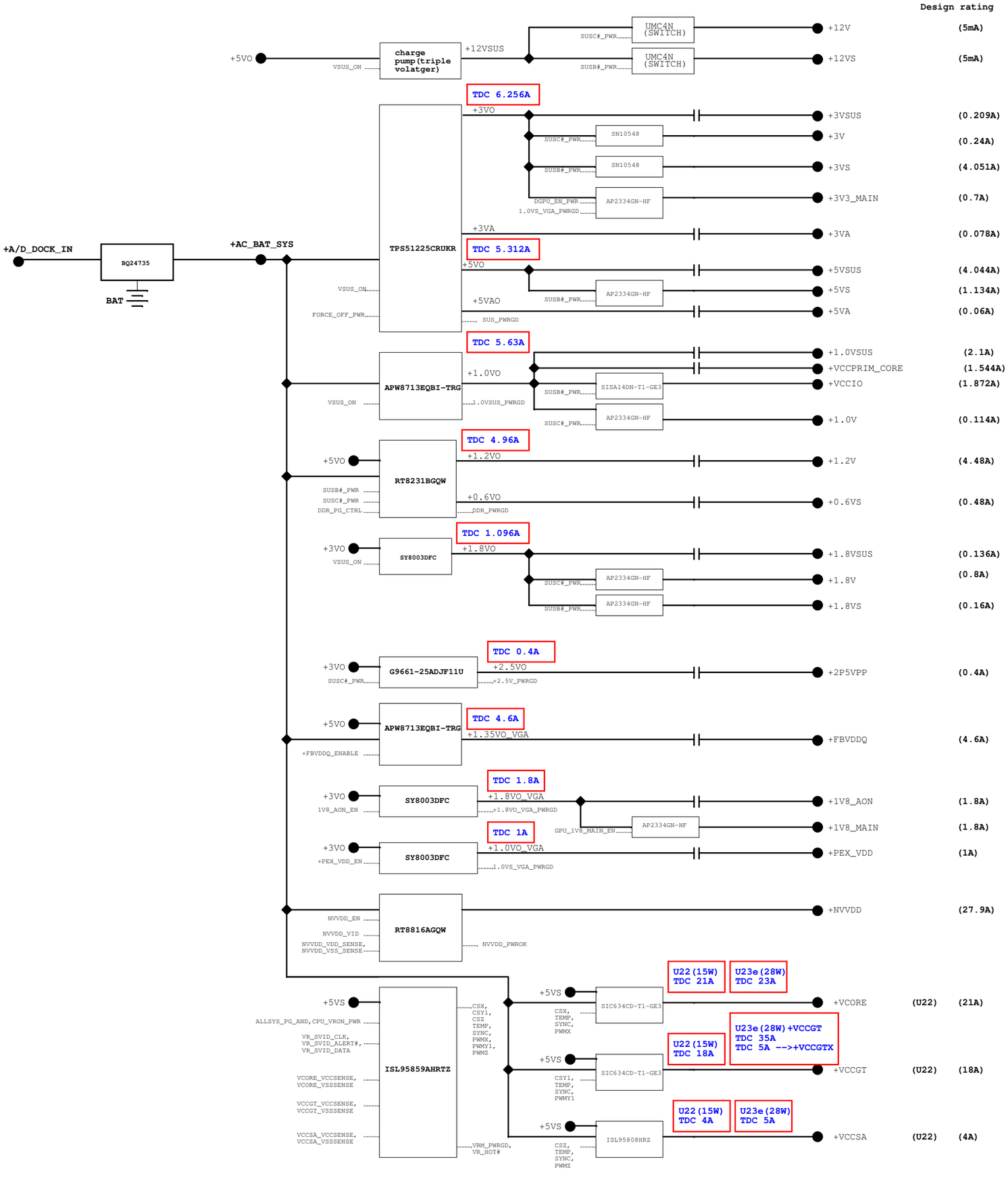

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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER_FLOWCHART

Engineer: Adams Lin

Size	Project Name	Rev
Custom	HE4EA	1.1

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