
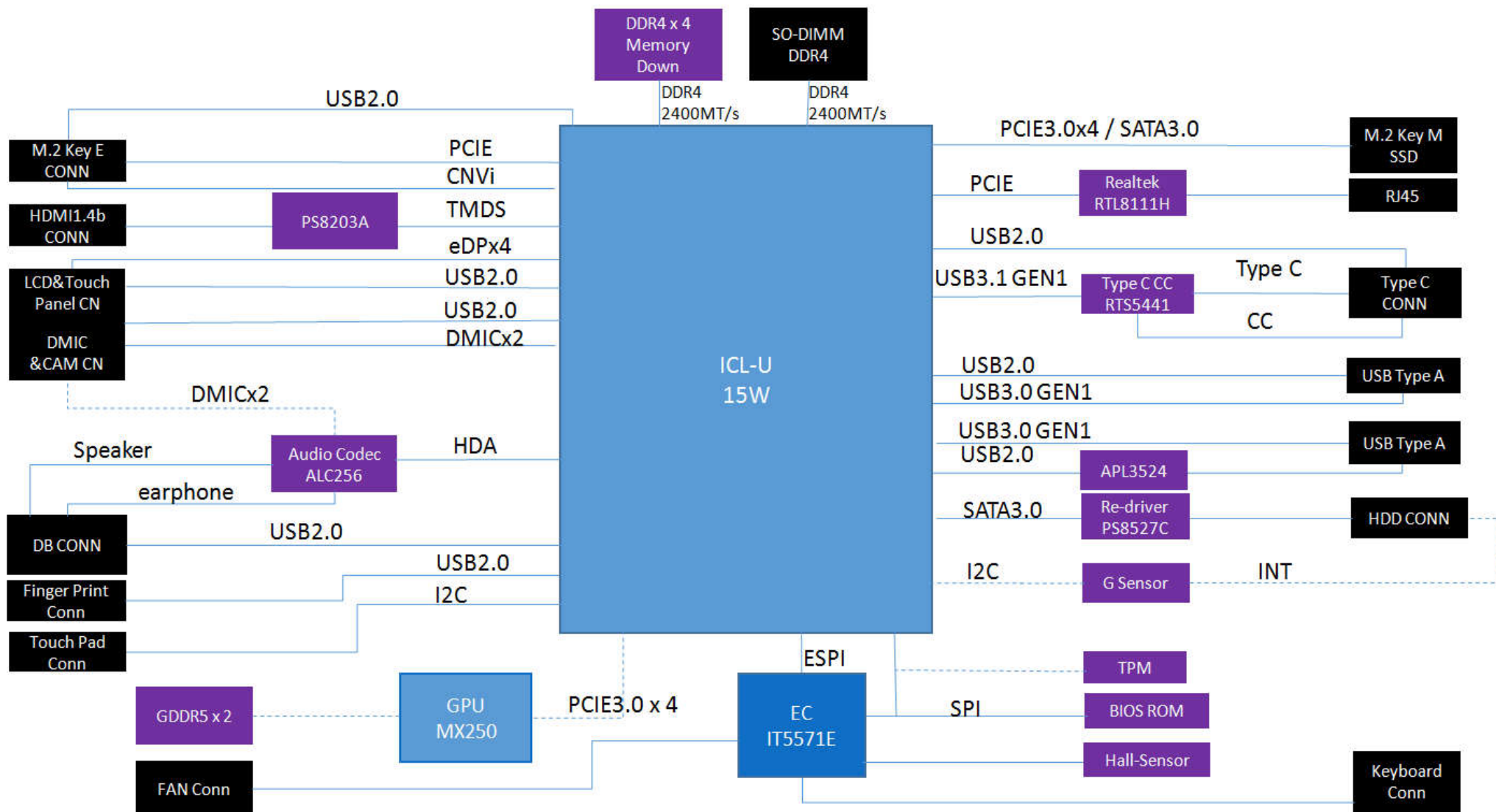


HuaQin Confidential

Aspire5_NB2593_M/B Schematics Document Intel Whiskey Lake U-Processor with DDR4 REV1.0 2019-11-12

| | | | | |
|----------|-------------|---|-----------------------------|-----------|
| Author | Albert Zhou |  Huaqin Telecom Technology Com.,Ltd. | | |
| Reviewer | Albert Zhou | Page name: Cover page | | |
| Approver | Lobo_Fan | Size: A4 | Project Name: NB2593 | REV: V1.0 |
| | | Date: Wednesday, December 25, 2019 | Sheet: 1 | of 72 |



MEM ID

| HW_ID0 | HW_ID1 | HW_ID2 | Description | Total |
|--------|--------|--------|---------------------------------------|-------|
| 0 | 0 | 0 | 4x Micron 8Gbx16 MT40A512M16TB-062E:J | 4GB |
| 1 | 0 | 0 | 4x Micron 8Gbx16 MT40A512M16LY-075:E | 4GB |
| 0 | 1 | 0 | 4x Hynix 8Gbx16 H5AN8G6NCJR-VKC | 4GB |
| 1 | 1 | 0 | NA | NA |
| 0 | 0 | 1 | 4x 16Gb(reserve) | 8GB |
| 1 | 0 | 1 | 4x 16Gb(reserve) | 8GB |
| 0 | 1 | 1 | 4x 16Gb(reserve) | 8GB |

GPU ID

| HW_ID3 | HW_ID4 | Description |
|--------|--------|-------------|
| 0 | 0 | UMA |
| 1 | 0 | N17-G5 |
| 0 | 1 | N17-G1 |
| 1 | 1 | N17-G2 |
| | | |
| | | |

G-sensor ID

| HW_ID5 | Description |
|--------|-------------------|
| 0 | no g-sensor |
| 1 | G-sensor on board |

FP ID

| HW_ID6 | Description |
|--------|-------------|
| 0 | no FP |
| 1 | FP on board |

TPM and fTPM ID

| HW_ID7 | Description |
|--------|-------------|
| 0 | fTPM |
| 1 | TPM |

| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | |
| C | | | | | |
| B | | | | | |
| A | | | | | |

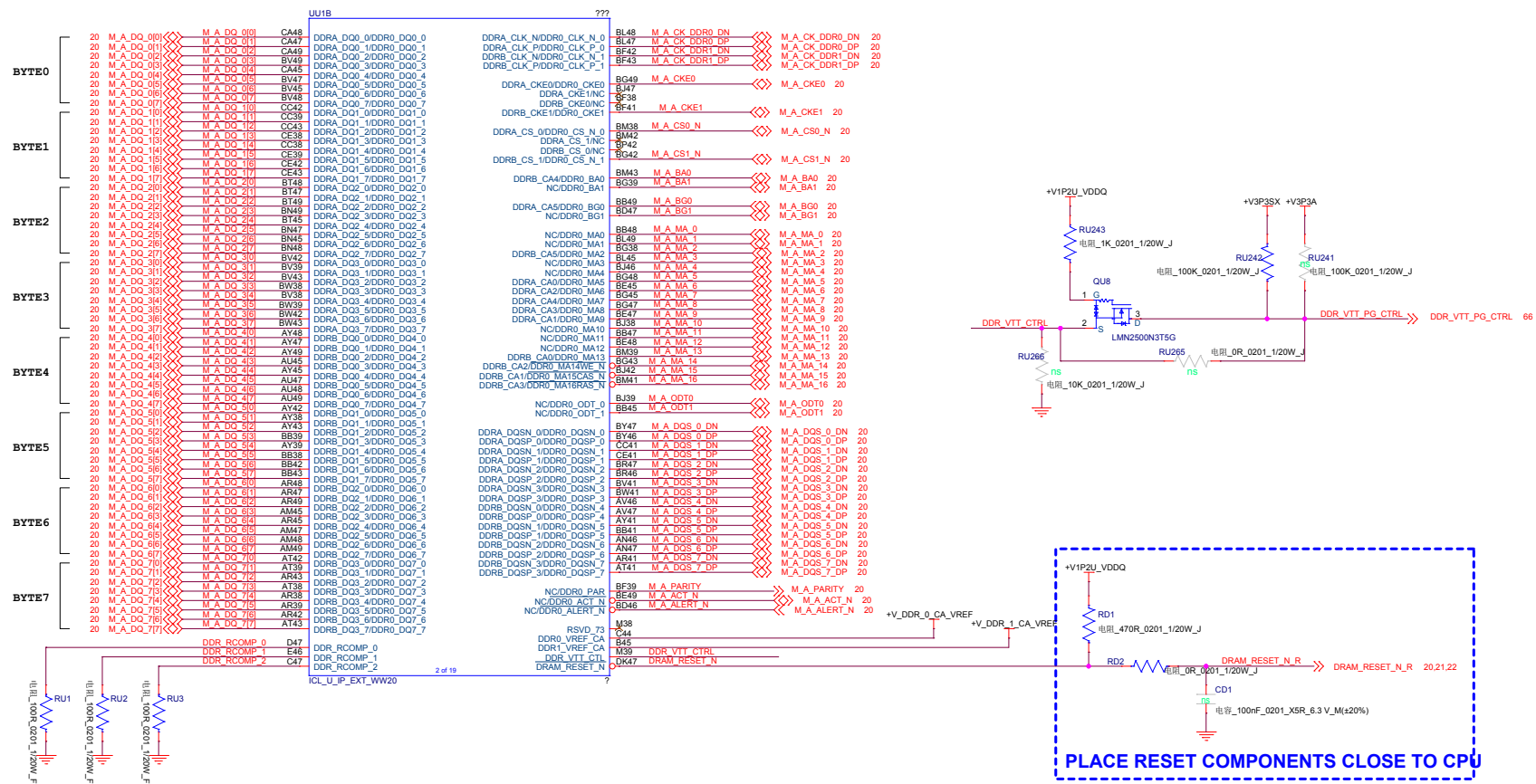


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|------------------------------------|----------------------|-----------|
| Page name: Blank | | |
| Size: A4 | Project Name: NB2593 | REV: V1.0 |
| Date: Wednesday, December 25, 2019 | Sheet: 4 | of 72 |

CHA



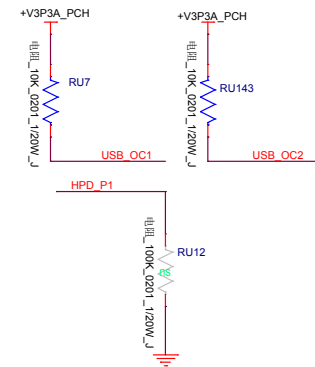
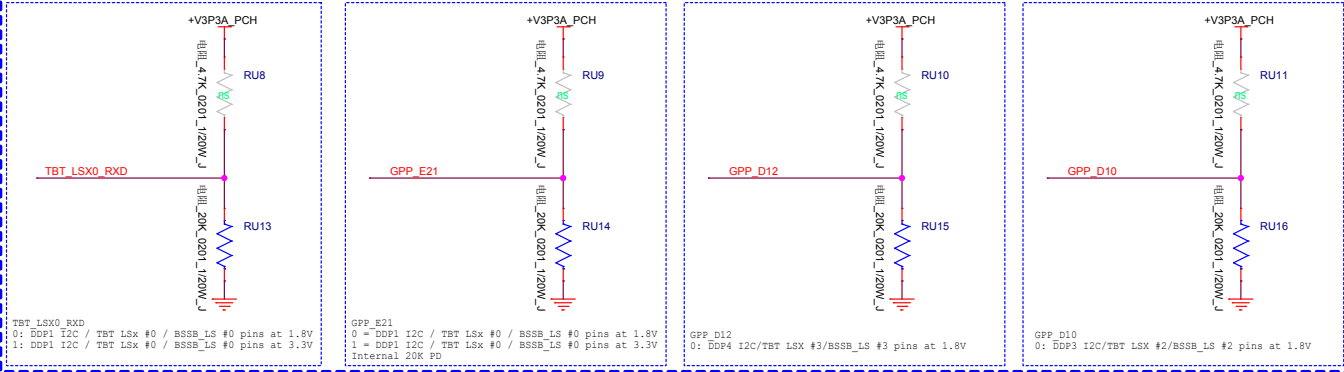
| | | | UU1C | ??? | | | |
|--------|----|-------------|-------------|------|-----------------------|-------------------------|-----------------------------|
| BYTE0 | 21 | M_B_DQ_0[0] | M_B_DQ_0[0] | AK48 | DDRC_DQ0_0/DDR1_DQ0_0 | DDRC_CLK_N/DDR1_CLK_N_0 | Y48 M_B_CK_DDR0_DN |
| | 21 | M_B_DQ_0[1] | M_B_DQ_0[1] | AK45 | DDRC_DQ0_1/DDR1_DQ0_1 | DDRC_CLK_P/DDR1_CLK_P_0 | Y47 M_B_CK_DDR0_DP |
| | 21 | M_B_DQ_0[2] | M_B_DQ_0[2] | AG47 | DDRC_DQ0_2/DDR1_DQ0_2 | DDRD_CLK_N/DDR1_CLK_N_1 | M43 M_B_CK_DDR0_DP 21,22,24 |
| | 21 | M_B_DQ_0[3] | M_B_DQ_0[3] | AK47 | DDRC_DQ0_3/DDR1_DQ0_3 | DDRD_CLK_P/DDR1_CLK_P_1 | M42 |
| BYTE1 | 21 | M_B_DQ_0[4] | M_B_DQ_0[4] | AG45 | DDRC_DQ0_4/DDR1_DQ0_4 | DDRC_CKE0/DDR1_CKE0 | U45 M_B_CKE0 |
| | 21 | M_B_DQ_0[5] | M_B_DQ_0[5] | AG48 | DDRC_DQ0_5/DDR1_DQ0_5 | DDRC_CKE1/NC | U46 M_B_CKE0 21,22,24 |
| | 21 | M_B_DQ_0[6] | M_B_DQ_0[6] | AG49 | DDRC_DQ0_6/DDR1_DQ0_6 | DDRD_CKE0/NC | M41 |
| | 21 | M_B_DQ_0[7] | M_B_DQ_0[7] | AJ38 | DDRC_DQ0_7/DDR1_DQ0_7 | DDRD_CKE1/DDR1_CKE1 | P43 |
| BYTE2 | 21 | M_B_DQ_1[0] | M_B_DQ_1[0] | AL39 | DDRC_DQ1_0/DDR1_DQ1_0 | DDRC_CS_0/DDR1_CS_N_0 | V42 M_B_CS0_N |
| | 21 | M_B_DQ_1[1] | M_B_DQ_1[1] | AJ39 | DDRC_DQ1_1/DDR1_DQ1_1 | DDRC_CS_1/NC | V39 M_B_CS0_N 21,22,24 |
| | 21 | M_B_DQ_1[2] | M_B_DQ_1[2] | AL43 | DDRC_DQ1_2/DDR1_DQ1_2 | DDRD_CS_0/NC | V39 |
| | 21 | M_B_DQ_1[3] | M_B_DQ_1[3] | AL38 | DDRC_DQ1_3/DDR1_DQ1_3 | DDRD_CS_1/DDR1_CS_N_1 | V39 |
| BYTE3 | 21 | M_B_DQ_1[4] | M_B_DQ_1[4] | AJ42 | DDRC_DQ1_4/DDR1_DQ1_4 | DDRD_CS_1/DDR1_CS_N_1 | T38 M_B_BA0 |
| | 21 | M_B_DQ_1[5] | M_B_DQ_1[5] | AL42 | DDRC_DQ1_5/DDR1_DQ1_5 | DDRD_CS_1/DDR1_CS_N_1 | T42 M_B_BA1 |
| | 21 | M_B_DQ_1[6] | M_B_DQ_1[6] | AJ43 | DDRC_DQ1_6/DDR1_DQ1_6 | DDRD_CA4/DDR1_BA0 | R45 M_B_BG0 |
| | 21 | M_B_DQ_1[7] | M_B_DQ_1[7] | AB49 | DDRC_DQ1_7/DDR1_DQ1_7 | NC/DDR1_BA1 | N47 M_B_BG1 |
| BYTE4 | 21 | M_B_DQ_2[0] | M_B_DQ_2[0] | AB48 | DDRC_DQ2_0/DDR1_DQ2_0 | NC/DDR1_MA0 | P42 M_B_MA_0 |
| | 21 | M_B_DQ_2[1] | M_B_DQ_2[1] | AE49 | DDRC_DQ2_1/DDR1_DQ2_1 | NC/DDR1_MA1 | Y49 M_B_MA_1 |
| | 21 | M_B_DQ_2[2] | M_B_DQ_2[2] | AE47 | DDRC_DQ2_2/DDR1_DQ2_2 | DDRD_CA5/DDR1_MA2 | U48 M_B_MA_2 |
| | 21 | M_B_DQ_2[3] | M_B_DQ_2[3] | AE48 | DDRC_DQ2_3/DDR1_DQ2_3 | NC/DDR1_MA3 | Y45 M_B_MA_3 |
| BYTE5 | 21 | M_B_DQ_2[4] | M_B_DQ_2[4] | AE48 | DDRC_DQ2_4/DDR1_DQ2_4 | NC/DDR1_MA4 | U47 M_B_MA_4 |
| | 21 | M_B_DQ_2[5] | M_B_DQ_2[5] | AB47 | DDRC_DQ2_5/DDR1_DQ2_5 | NC/DDR1_MA5 | R49 M_B_MA_5 |
| | 21 | M_B_DQ_2[6] | M_B_DQ_2[6] | AB45 | DDRC_DQ2_6/DDR1_DQ2_6 | DDRC_CA0/DDR1_MA5 | U49 M_B_MA_6 |
| | 21 | M_B_DQ_2[7] | M_B_DQ_2[7] | AE45 | DDRC_DQ2_7/DDR1_DQ2_7 | DDRC_CA2/DDR1_MA6 | M47 M_B_MA_7 |
| BYTE6 | 21 | M_B_DQ_3[0] | M_B_DQ_3[0] | AD38 | DDRC_DQ3_0/DDR1_DQ3_0 | DDRC_CA4/DDR1_MA7 | M45 M_B_MA_8 |
| | 21 | M_B_DQ_3[1] | M_B_DQ_3[1] | AD39 | DDRC_DQ3_1/DDR1_DQ3_1 | DDRC_CA3/DDR1_MA8 | R47 M_B_MA_9 |
| | 21 | M_B_DQ_3[2] | M_B_DQ_3[2] | AE39 | DDRC_DQ3_2/DDR1_DQ3_2 | DDRC_CA1/DDR1_MA9 | P39 M_B_MA_10 |
| | 21 | M_B_DQ_3[3] | M_B_DQ_3[3] | AE43 | DDRC_DQ3_3/DDR1_DQ3_3 | NC/DDR1_MA10 | N46 M_B_MA_11 |
| BYTE7 | 21 | M_B_DQ_3[4] | M_B_DQ_3[4] | AD43 | DDRC_DQ3_4/DDR1_DQ3_4 | NC/DDR1_MA11 | R48 M_B_MA_12 |
| | 21 | M_B_DQ_3[5] | M_B_DQ_3[5] | AD42 | DDRC_DQ3_5/DDR1_DQ3_5 | DDRD_CA0/DDR1_MA12 | Y41 M_B_MA_13 |
| | 21 | M_B_DQ_3[6] | M_B_DQ_3[6] | AD42 | DDRC_DQ3_6/DDR1_DQ3_6 | DDRD_CA2/DDR1_MA14WE_N | V41 M_B_MA_14 |
| | 21 | M_B_DQ_3[7] | M_B_DQ_3[7] | AE42 | DDRC_DQ3_7/DDR1_DQ3_7 | DDRD_CA1/DDR1_MA15CAS_N | Y42 M_B_MA_15 |
| BYTE8 | 22 | M_B_DQ_4[0] | M_B_DQ_4[0] | J48 | DDRD_DQ0_0/DDR1_DQ4_0 | DDRD_CA3/DDR1_MA16RAS_N | V47 M_B_MA_16 |
| | 22 | M_B_DQ_4[1] | M_B_DQ_4[1] | J45 | DDRD_DQ0_1/DDR1_DQ4_1 | NC/DDR1_ODT_0 | V43 M_B_ODT0 |
| | 22 | M_B_DQ_4[2] | M_B_DQ_4[2] | J49 | DDRD_DQ0_2/DDR1_DQ4_2 | NC/DDR1_ODT_1 | V38 M_B_ODT0 21,22,24 |
| | 22 | M_B_DQ_4[3] | M_B_DQ_4[3] | G47 | DDRD_DQ0_3/DDR1_DQ4_3 | DDRC_DQSN_0/DDR1_DQSN_0 | AH46 M_B_DQS_0_DN |
| BYTE9 | 22 | M_B_DQ_4[4] | M_B_DQ_4[4] | G45 | DDRD_DQ0_4/DDR1_DQ4_4 | DDRC_DQSP_0/DDR1_DQSP_0 | AH47 M_B_DQS_0_DP |
| | 22 | M_B_DQ_4[5] | M_B_DQ_4[5] | G48 | DDRD_DQ0_5/DDR1_DQ4_5 | DDRC_DQSN_1/DDR1_DQSN_1 | AJ41 M_B_DQS_1_DN |
| | 22 | M_B_DQ_4[6] | M_B_DQ_4[6] | E48 | DDRD_DQ0_6/DDR1_DQ4_6 | DDRC_DQSP_1/DDR1_DQSP_1 | AL41 M_B_DQS_1_DP |
| | 22 | M_B_DQ_4[7] | M_B_DQ_4[7] | J38 | DDRD_DQ0_7/DDR1_DQ4_7 | DDRC_DQSN_2/DDR1_DQSN_2 | AC47 M_B_DQS_2_DN |
| BYTE10 | 22 | M_B_DQ_5[0] | M_B_DQ_5[0] | G39 | DDRD_DQ1_0/DDR1_DQ5_0 | DDRC_DQSP_2/DDR1_DQSP_2 | AC46 M_B_DQS_2_DP |
| | 22 | M_B_DQ_5[1] | M_B_DQ_5[1] | G38 | DDRD_DQ1_1/DDR1_DQ5_1 | DDRC_DQSN_3/DDR1_DQSN_3 | AE41 M_B_DQS_3_DN |
| | 22 | M_B_DQ_5[2] | M_B_DQ_5[2] | G42 | DDRD_DQ1_2/DDR1_DQ5_2 | DDRD_DQSP_0/DDR1_DQSN_4 | AD41 M_B_DQS_3_DP |
| | 22 | M_B_DQ_5[3] | M_B_DQ_5[3] | J39 | DDRD_DQ1_3/DDR1_DQ5_3 | DDRD_DQSP_1/DDR1_DQSP_4 | H47 M_B_DQS_4_DN |
| BYTE11 | 22 | M_B_DQ_5[4] | M_B_DQ_5[4] | J42 | DDRD_DQ1_4/DDR1_DQ5_4 | DDRD_DQSP_2/DDR1_DQSP_5 | H46 M_B_DQS_4_DP |
| | 22 | M_B_DQ_5[5] | M_B_DQ_5[5] | G43 | DDRD_DQ1_5/DDR1_DQ5_5 | DDRD_DQSN_1/DDR1_DQSN_5 | G41 M_B_DQS_5_DN |
| | 22 | M_B_DQ_5[6] | M_B_DQ_5[6] | J43 | DDRD_DQ1_6/DDR1_DQ5_6 | DDRD_DQSP_1/DDR1_DQSP_5 | J41 M_B_DQS_5_DP |
| | 22 | M_B_DQ_5[7] | M_B_DQ_5[7] | B43 | DDRD_DQ1_7/DDR1_DQ5_7 | DDRD_DQSN_2/DDR1_DQSN_6 | C42 M_B_DQS_6_DN |
| BYTE12 | 22 | M_B_DQ_6[0] | M_B_DQ_6[0] | D43 | DDRD_DQ2_0/DDR1_DQ6_0 | DDRD_DQSP_2/DDR1_DQSP_6 | D42 M_B_DQS_6_DP |
| | 22 | M_B_DQ_6[1] | M_B_DQ_6[1] | D43 | DDRD_DQ2_1/DDR1_DQ6_1 | DDRD_DQSN_3/DDR1_DQSN_7 | D36 M_B_DQS_7_DN |
| | 22 | M_B_DQ_6[2] | M_B_DQ_6[2] | C40 | DDRD_DQ2_2/DDR1_DQ6_2 | DDRD_DQSP_3/DDR1_DQSP_7 | C36 M_B_DQS_7_DP |
| | 22 | M_B_DQ_6[3] | M_B_DQ_6[3] | C43 | DDRD_DQ2_3/DDR1_DQ6_3 | NC/DDR1_PAR | P38 M_B_PARITY |
| BYTE13 | 22 | M_B_DQ_6[4] | M_B_DQ_6[4] | D40 | DDRD_DQ2_4/DDR1_DQ6_4 | NC/DDR1_ACT_N | M48 M_B_ACT_N |
| | 22 | M_B_DQ_6[5] | M_B_DQ_6[5] | B40 | DDRD_DQ2_5/DDR1_DQ6_5 | NC/DDR1_ALERT_N | M49 M_B_ALERT_N |
| | 22 | M_B_DQ_6[6] | M_B_DQ_6[6] | B40 | DDRD_DQ2_6/DDR1_DQ6_6 | | |
| | 22 | M_B_DQ_6[7] | M_B_DQ_6[7] | A40 | DDRD_DQ2_7/DDR1_DQ6_7 | | |
| BYTE14 | 22 | M_B_DQ_7[0] | M_B_DQ_7[0] | B35 | DDRD_DQ3_0/DDR1_DQ7_0 | | |
| | 22 | M_B_DQ_7[1] | M_B_DQ_7[1] | D35 | DDRD_DQ3_1/DDR1_DQ7_1 | | |
| | 22 | M_B_DQ_7[2] | M_B_DQ_7[2] | A35 | DDRD_DQ3_2/DDR1_DQ7_2 | | |
| | 22 | M_B_DQ_7[3] | M_B_DQ_7[3] | D38 | DDRD_DQ3_3/DDR1_DQ7_3 | | |
| BYTE15 | 22 | M_B_DQ_7[4] | M_B_DQ_7[4] | C35 | DDRD_DQ3_4/DDR1_DQ7_4 | | |
| | 22 | M_B_DQ_7[5] | M_B_DQ_7[5] | C38 | DDRD_DQ3_5/DDR1_DQ7_5 | | |
| | 22 | M_B_DQ_7[6] | M_B_DQ_7[6] | B38 | DDRD_DQ3_6/DDR1_DQ7_6 | | |
| | 22 | M_B_DQ_7[7] | M_B_DQ_7[7] | A38 | DDRD_DQ3_7/DDR1_DQ7_7 | | |

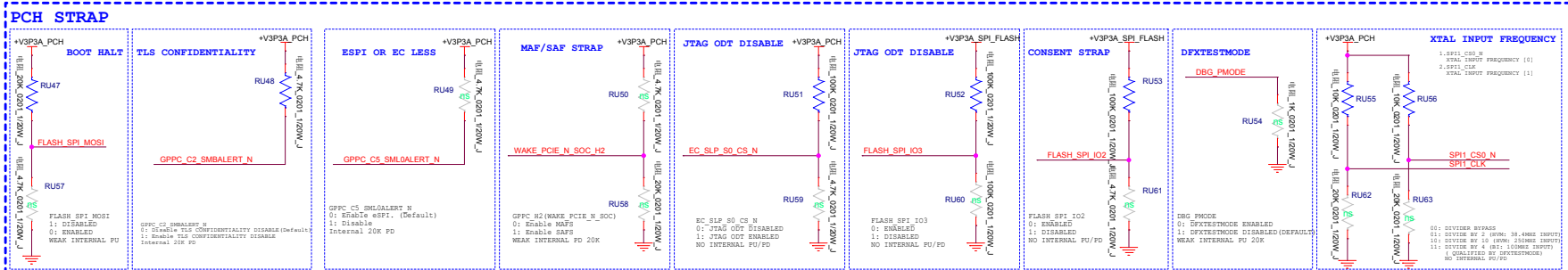
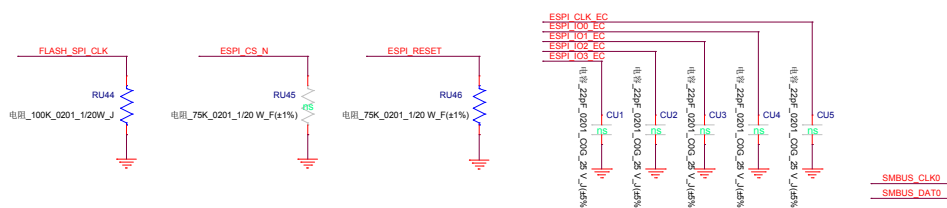
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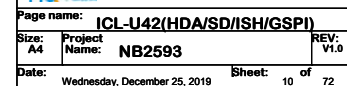
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PCH STRAP---VCCIO CONFIGURATION







GPU

LAN

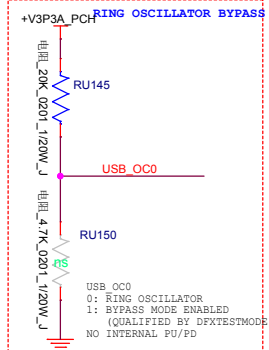
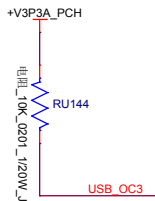
WLAN

HDD

fix WiFI Yellow mark
20191013

SSD1

PCH STRAP



U01H

777

ICL_U_IP_EXT_WW20

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USB_ID

USB_VBUSSENSE

USB2_COMP

RSDV_BSCAN

USB3.0 TypeA 1 AUO

USB3.0 Type-A 2

Type-C

NA

USB3.0 Type-A 1 AUO

USB3.0 Type-A 2

Finger Print

DB USB2.0 Type-A

Type-C

Camera

Touch Panel

NA

NA

BT

GPU



Huaqin Telecom Technology Com.,Ltd.

Page name: ICL-U42(USB/PCIE)

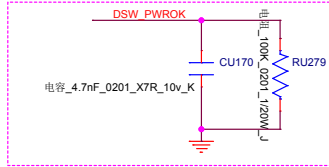
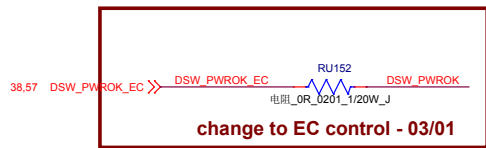
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Project Name: NB2593

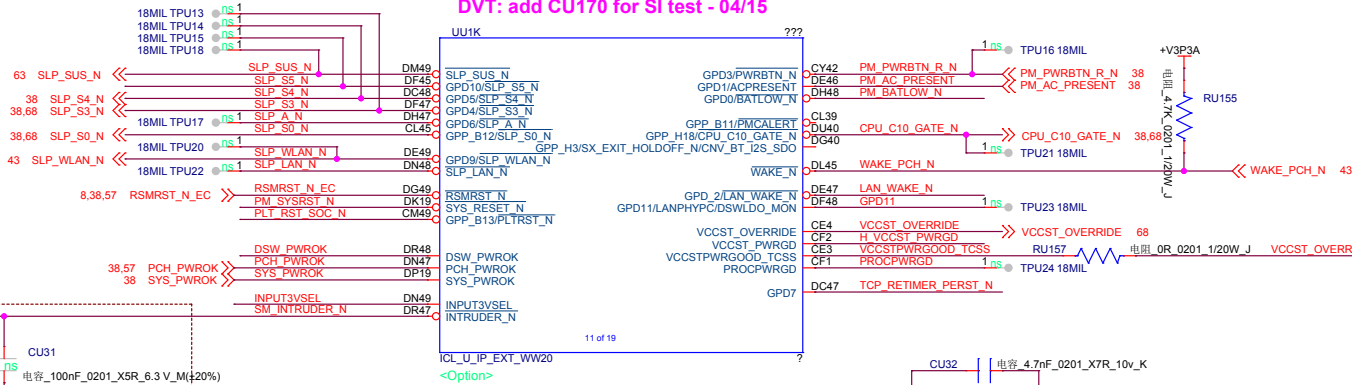
REV: V1.0

Date: Wednesday, December 25, 2019

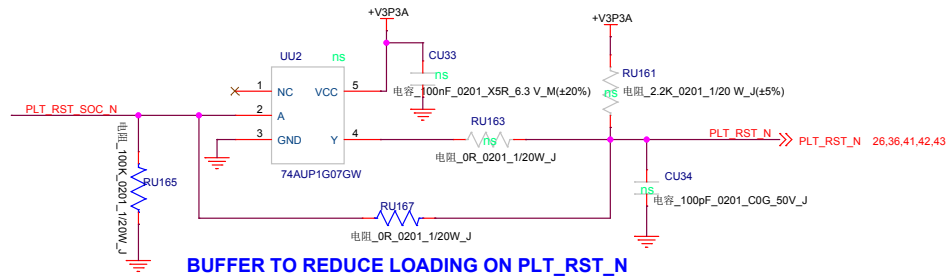
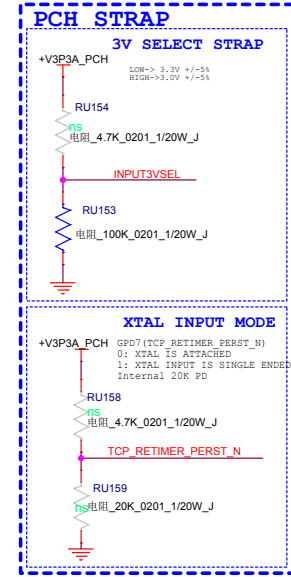
Sheet: 11 of 72



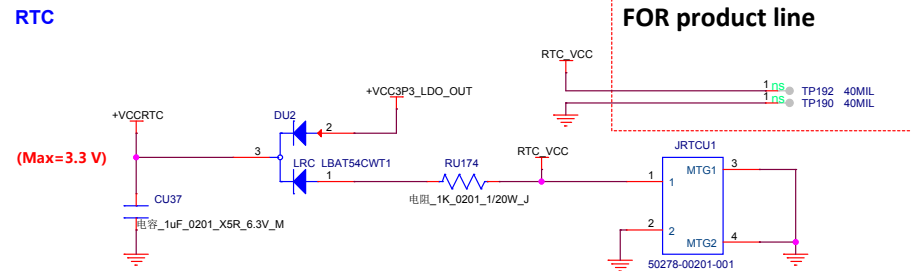
DVT: add CU170 for SI test - 04/15

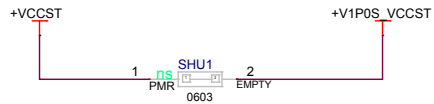
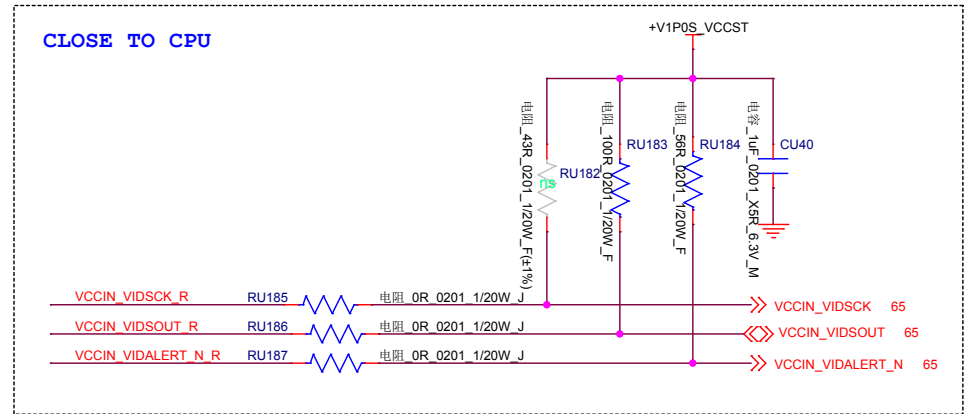
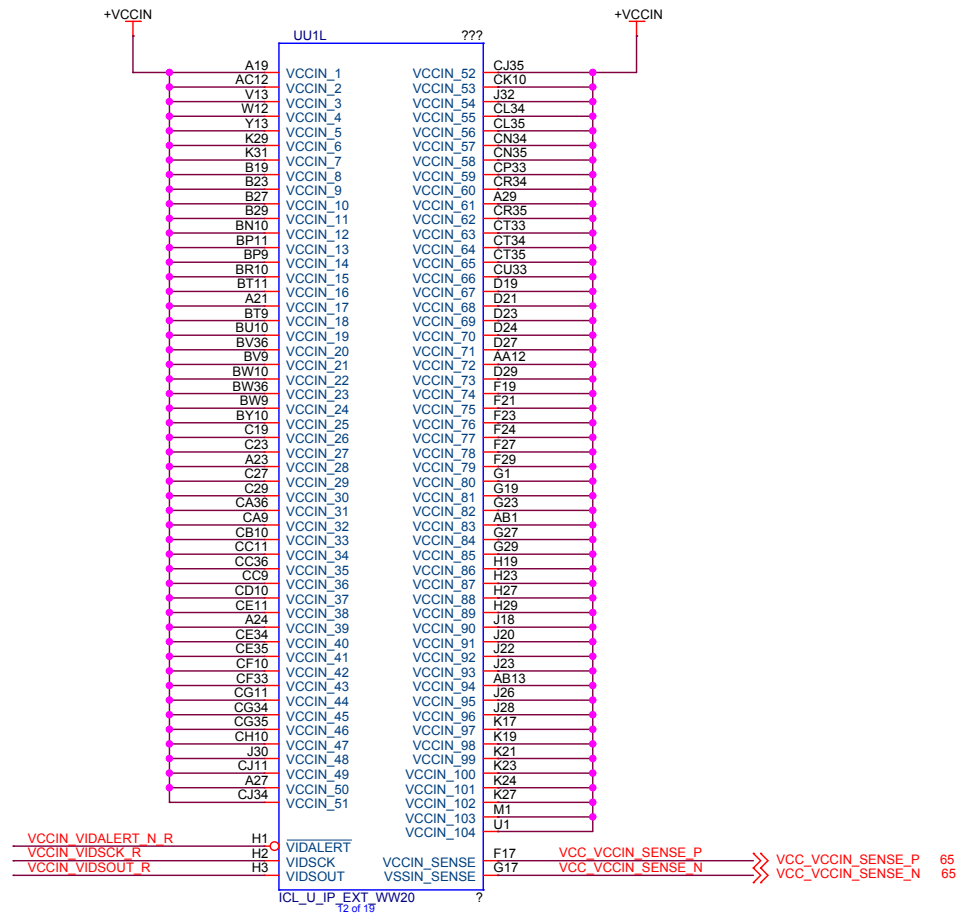


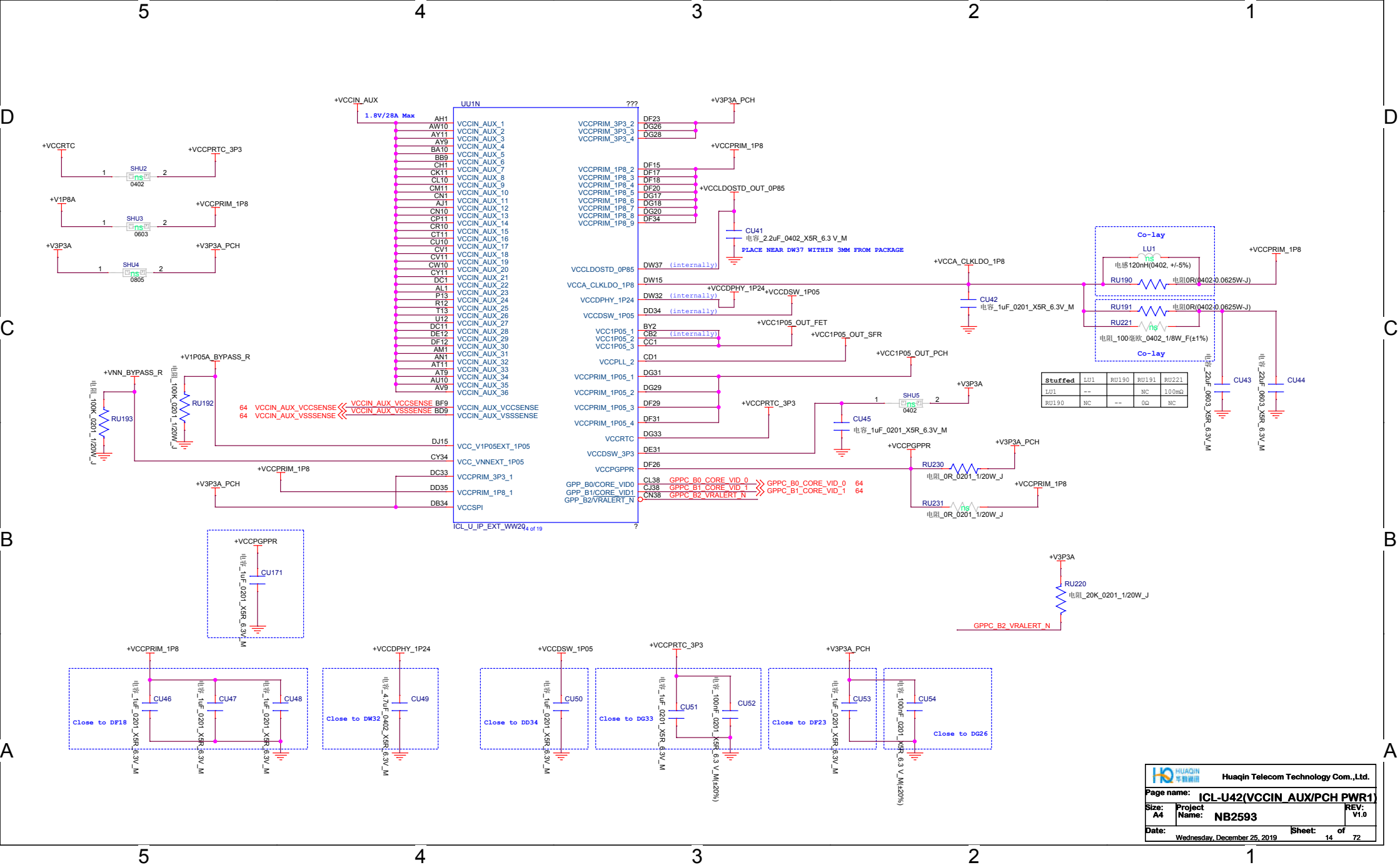
BY DEFAULT 3.3V FLASH SUPPORT.
FOR 1.8V FLASH OPERATION UNSTUFF CH23

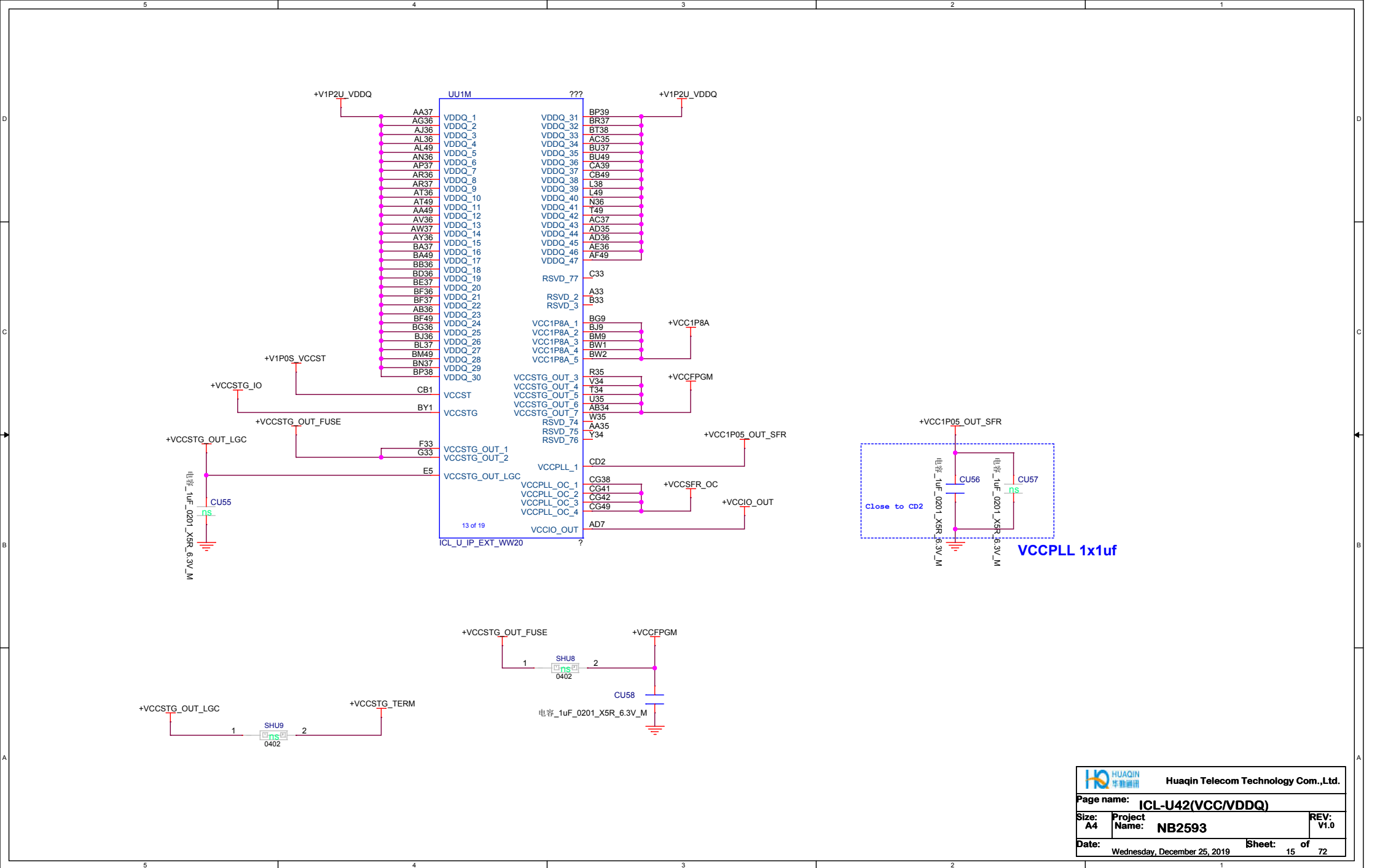


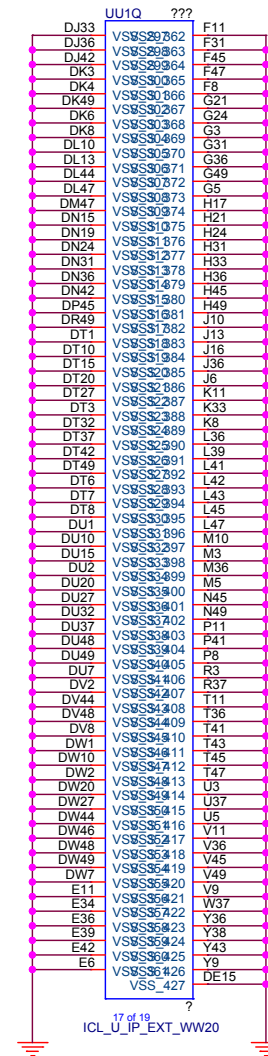
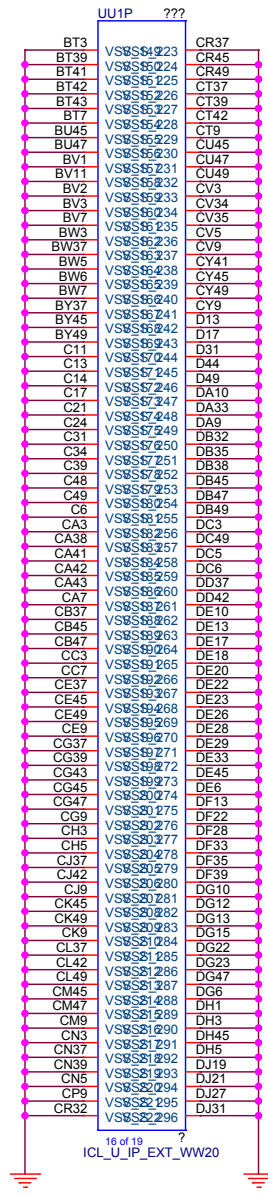
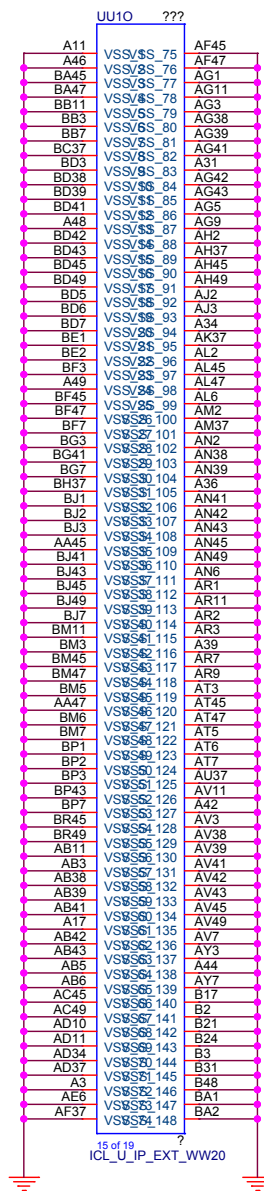
RTC

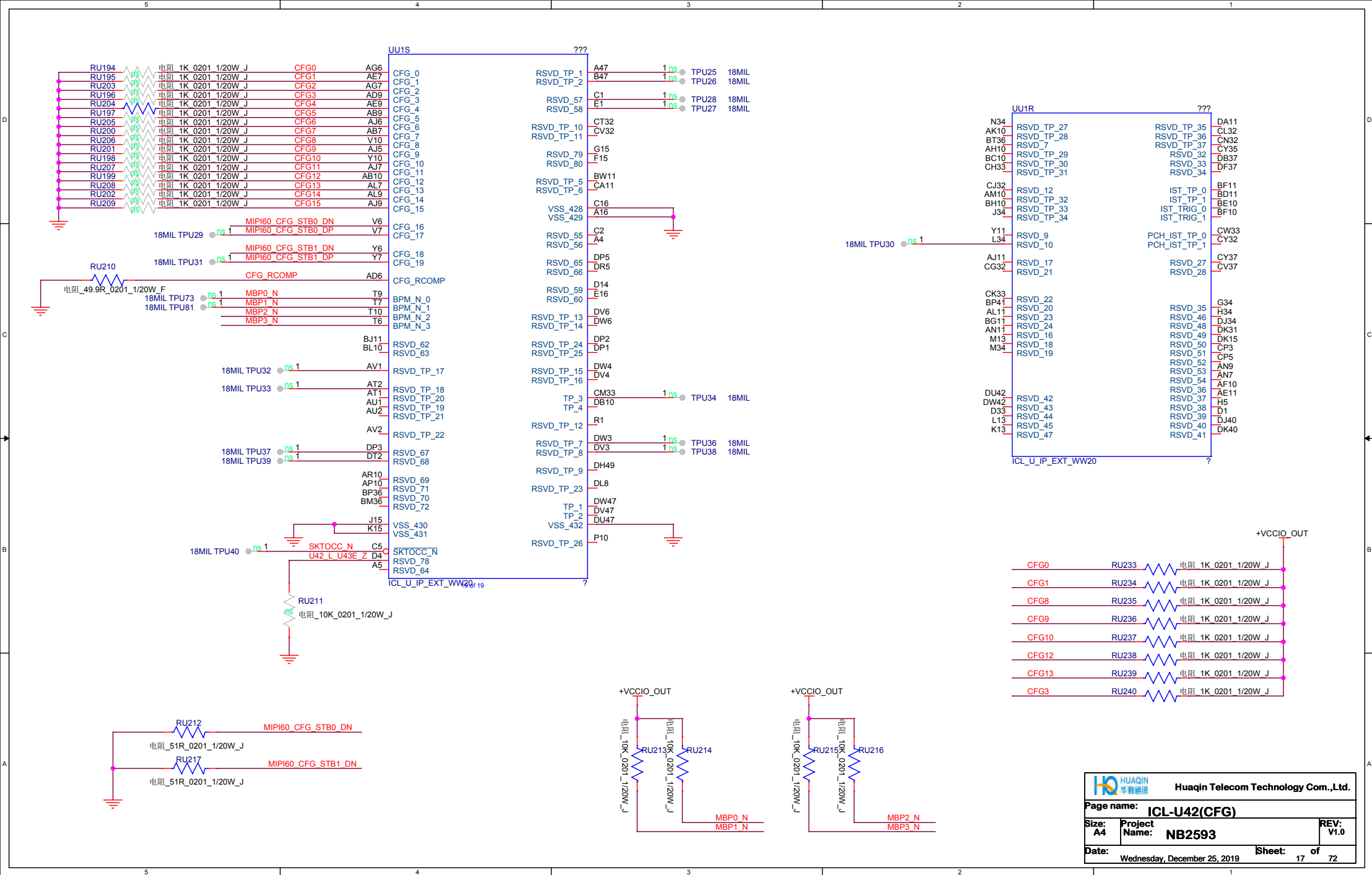


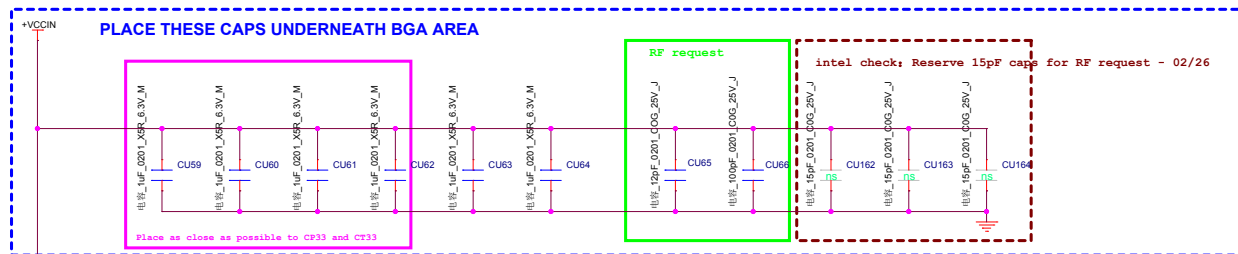






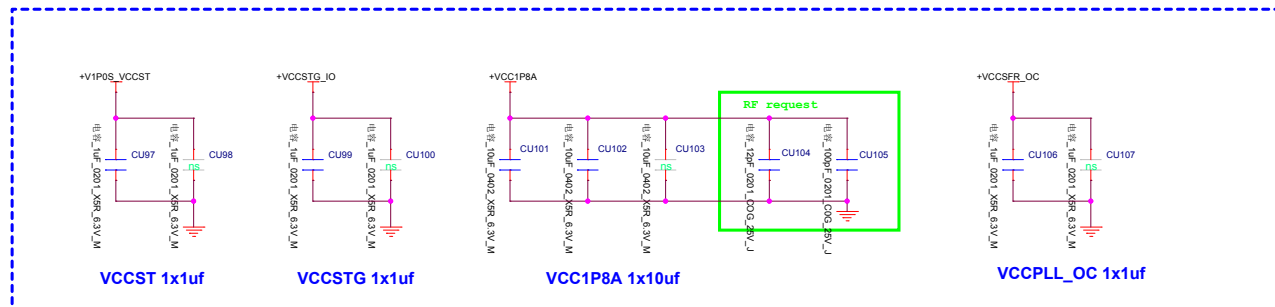
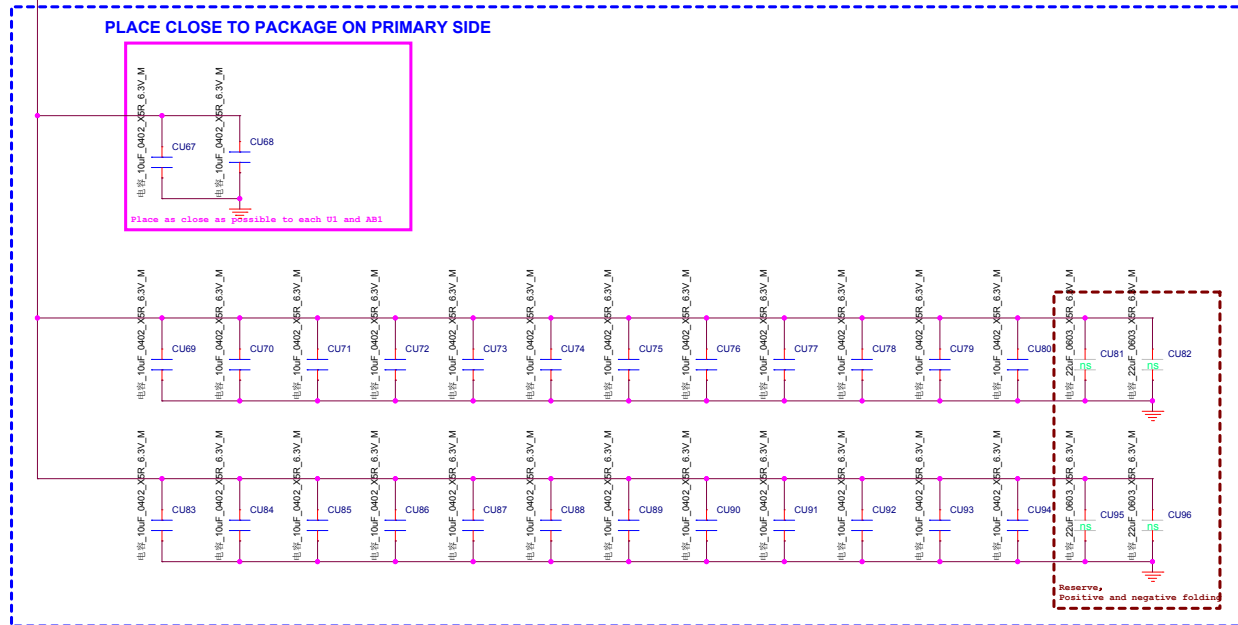


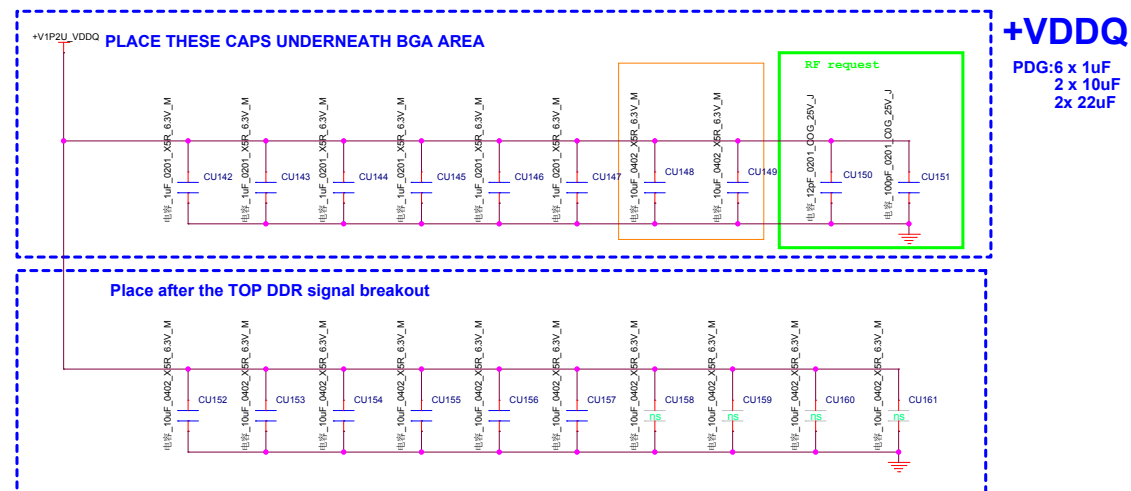
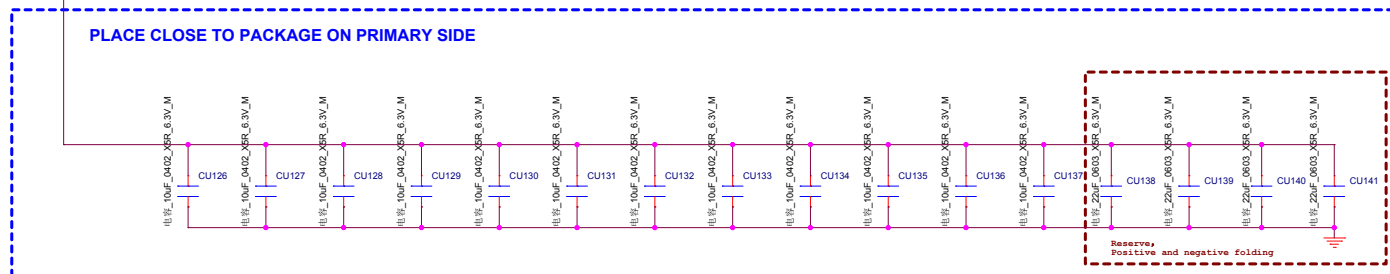
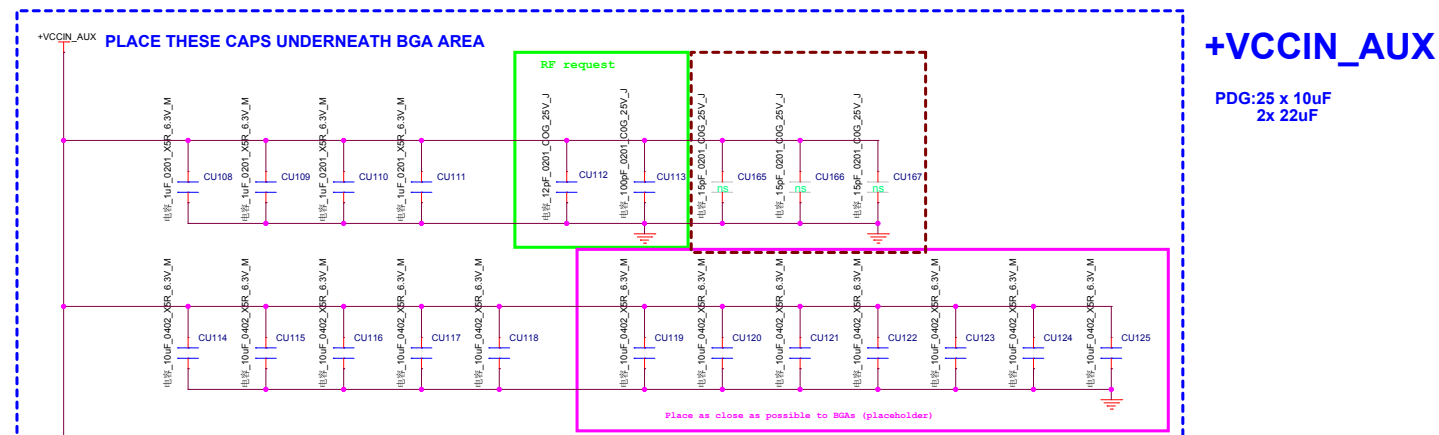




+VCCIN

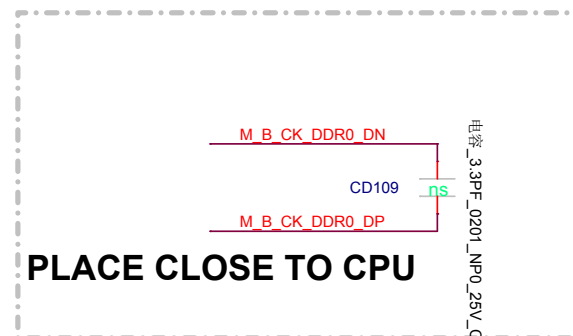
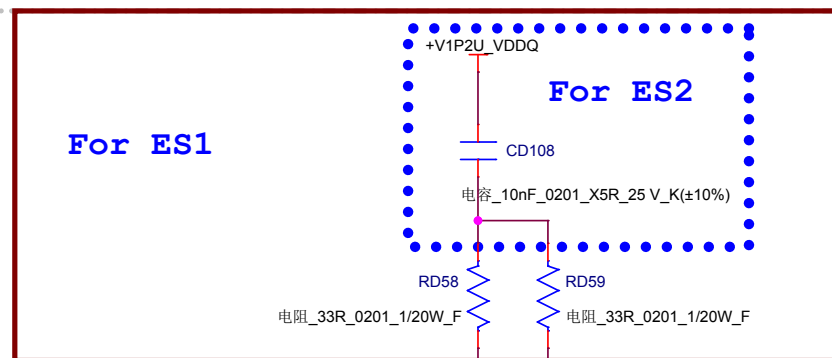
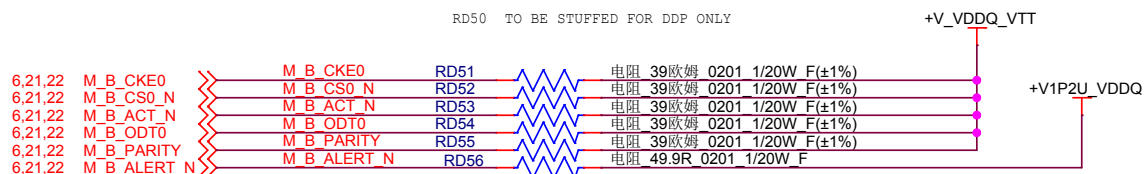
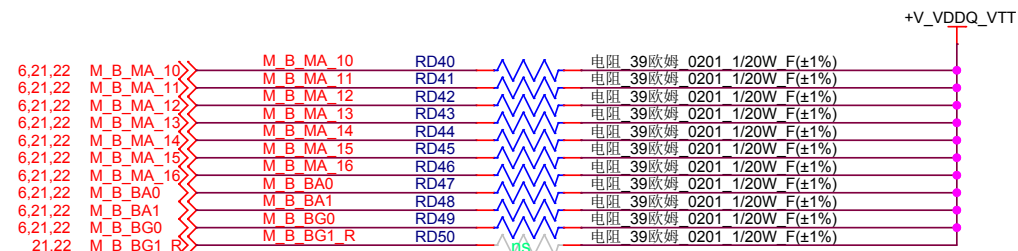
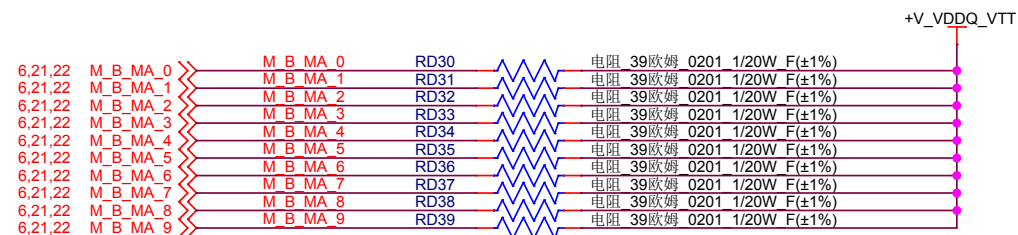
PDG:4 x 1uF
2 x 10uF
10x 22uF
3x 47uF





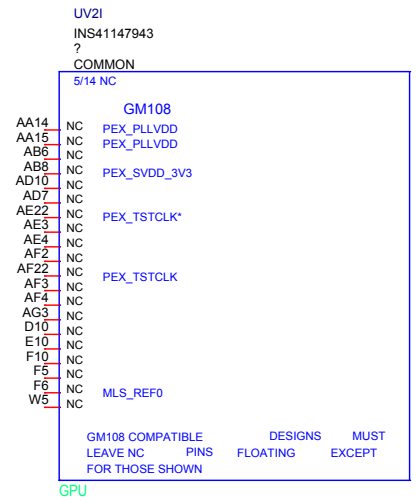
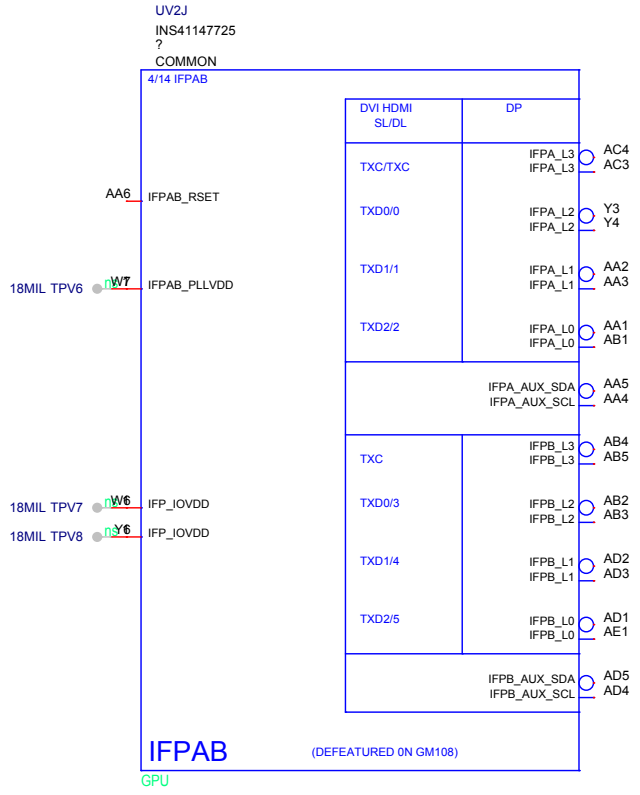
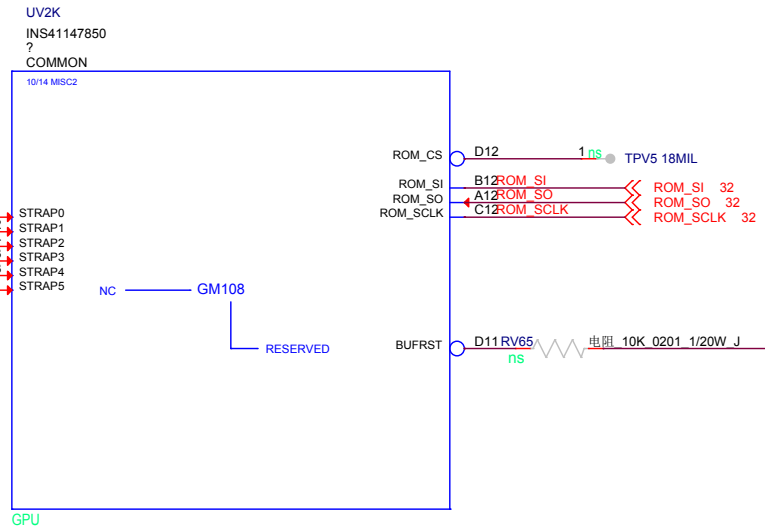
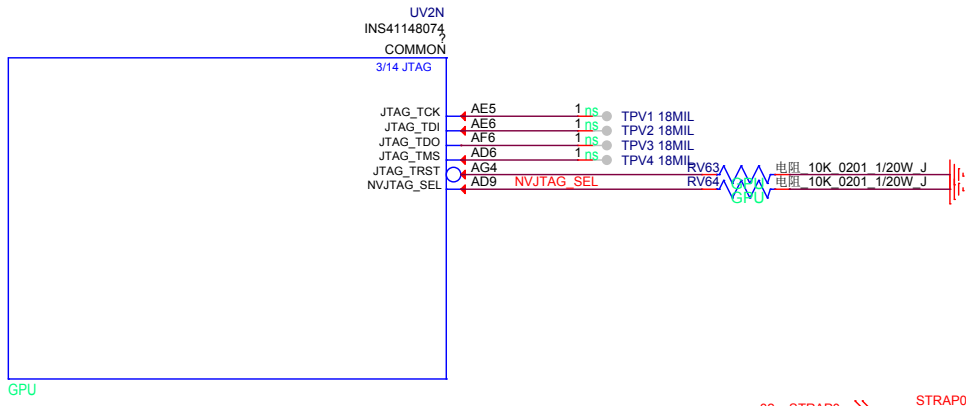
MEMORY TERMINATIONS

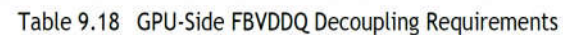
CHANNEL B MD



PLACE CLOSE TO CPU

PLACE TERMINATION RESISTOR CLOSE TO LAST CHIP



+V1P8A TO +V1P8_AON

Move to Power Page 2018/06/07

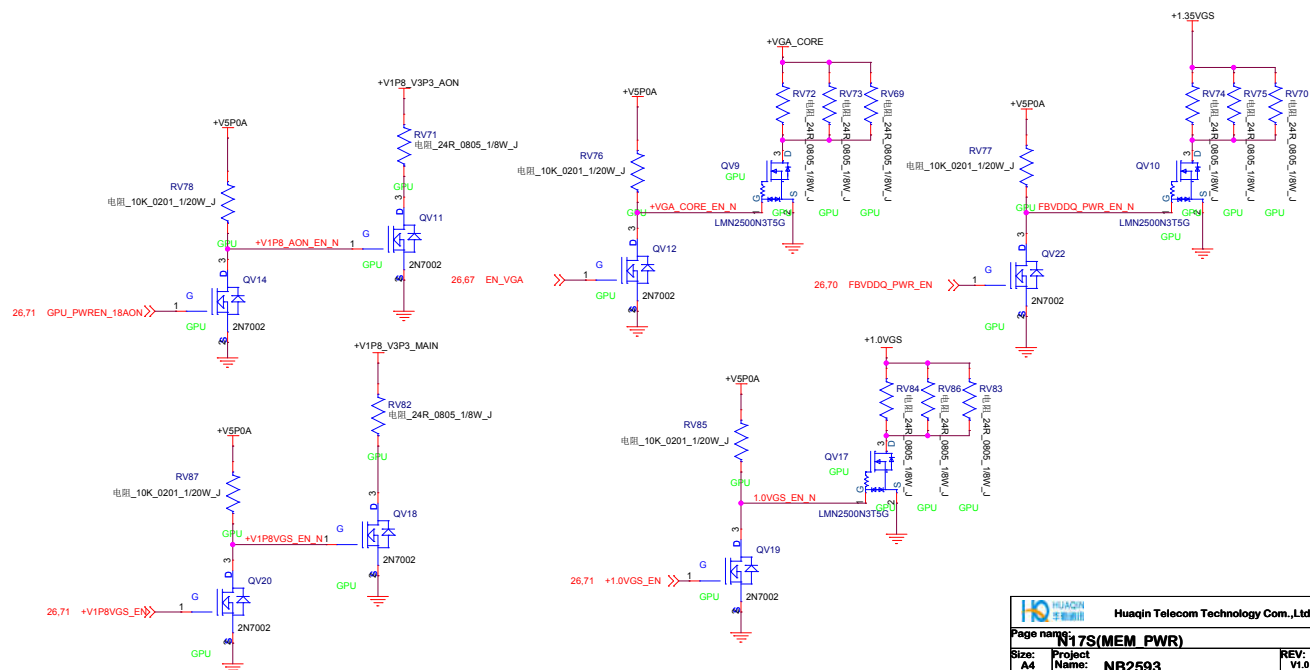


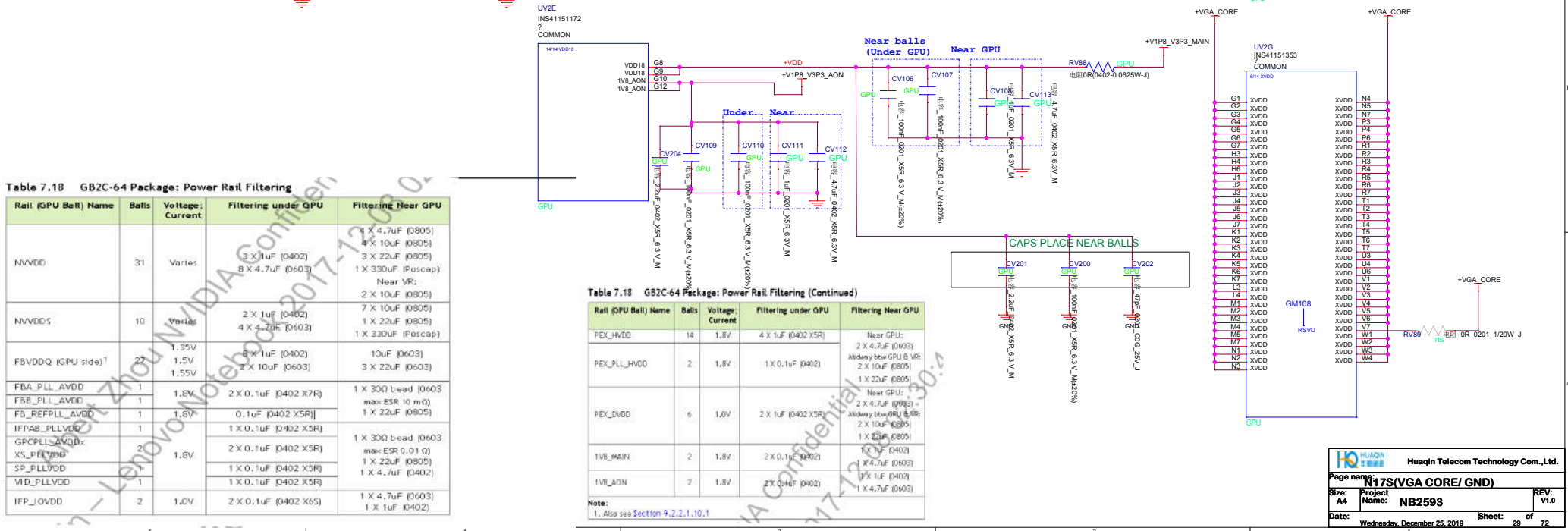
Table 7.18 GB2C-64 Package: Power Rail Filtering

| Rail (GPU Ball) Name | Balls | Voltage: Current | Filtering under GPU | Filtering Near GPU |
|--------------------------------|-------|------------------------|------------------------------------|--|
| NVVDD | 31 | Varies | 3 X 1uF (0402) 8 X 4.7uF (0603) | 1 X 4.7uF (0805) 4 X 10uF (0805) 3 X 22uF (0805) 1 X 330uF (Pocap) Near VR: 2 X 10uF (0805) |
| NVVDD_S | 10 | Varies | 2 X 1uF (0402) 4 X 4.7uF (0603) | 7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Pocap) |
| FBVDDQ (GPU side) ¹ | 27 | 1.35V 1.5V 1.55V | 8 X 1uF (0402) 2 X 10uF (0603) | 10uF (0603) 3 X 22uF (0603) |
| FBA_PLL_AVDD | 1 | 1.8V | 2 X 0.1uF (0402 X7R) | 1 X 300 bead (0603 max ESR 10 mΩ) |
| FBB_PLL_AVDD | 1 | 1.8V | 0.1uF (0402 X5R) | 1 X 22uF (0805) |
| FB_REFPLL_AVDD | 1 | 1.8V | 1 X 0.1uF (0402 X5R) | 1 X 22uF (0805) |
| IFPAB_PLLVDD | 1 | 1.8V | 1 X 0.1uF (0402 X5R) | 1 X 22uF (0805) |
| GPCPLL_AVDD | 2 | 1.8V | 2 X 0.1uF (0402 X5R) | 1 X 300 bead (0603 max ESR 0.01 Ω) |
| XS_PLLVDD | 1 | 1.8V | 1 X 0.1uF (0402 X5R) | 1 X 22uF (0805) |
| SP_PLLVDD | 1 | 1.8V | 1 X 0.1uF (0402 X5R) | 1 X 4.7uF (0402) |
| WD_PLLVDD | 1 | 1.8V | 1 X 0.1uF (0402 X5R) | 1 X 4.7uF (0402) |
| IFP_OVDD | 2 | 1.0V | 2 X 0.1uF (0402 X6S) | 1 X 4.7uF (0402) 1 X 1uF (0402) |

Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)

| Rail (GPU Ball) Name | Balls | Voltage: Current | Filtering under GPU | Filtering Near GPU |
|----------------------|-------|------------------|---------------------|---|
| PEX_HVDD | 14 | 1.8V | 4 X 1uF (0402 X5R) | Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805) |
| PEX_HVDD | 2 | 1.8V | 1 X 0.1uF (0402) | Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805) |
| PEX_DVDD | 6 | 1.0V | 2 X 1uF (0402 X5R) | Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805) |
| 1V8_MAIN | 2 | 1.8V | 2 X 0.1uF (0402) | 1 X 1uF (0402) 1 X 4.7uF (0603) |
| 1V8_AON | 2 | 1.8V | 2 X 0.1uF (0402) | 1 X 1uF (0402) 1 X 4.7uF (0603) |

Note:
1. Also see Section 9.2.2.1.10.1



Memory - Lower 32 bits

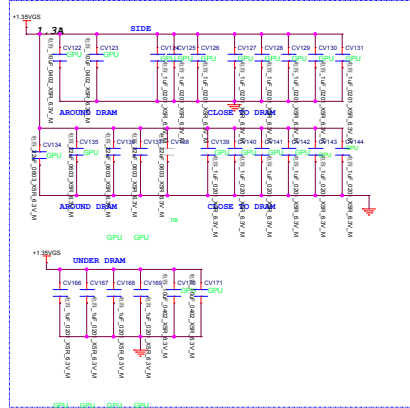
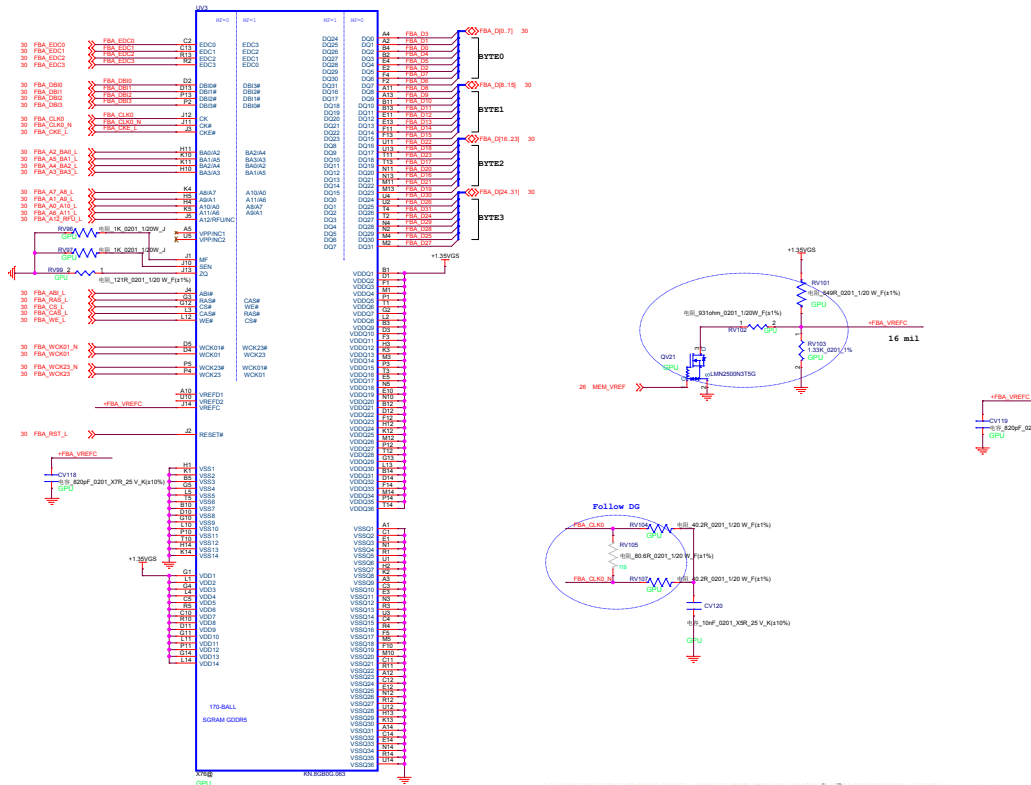
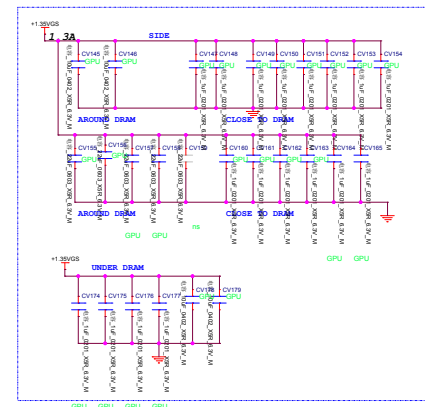
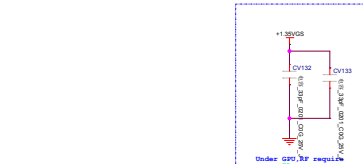
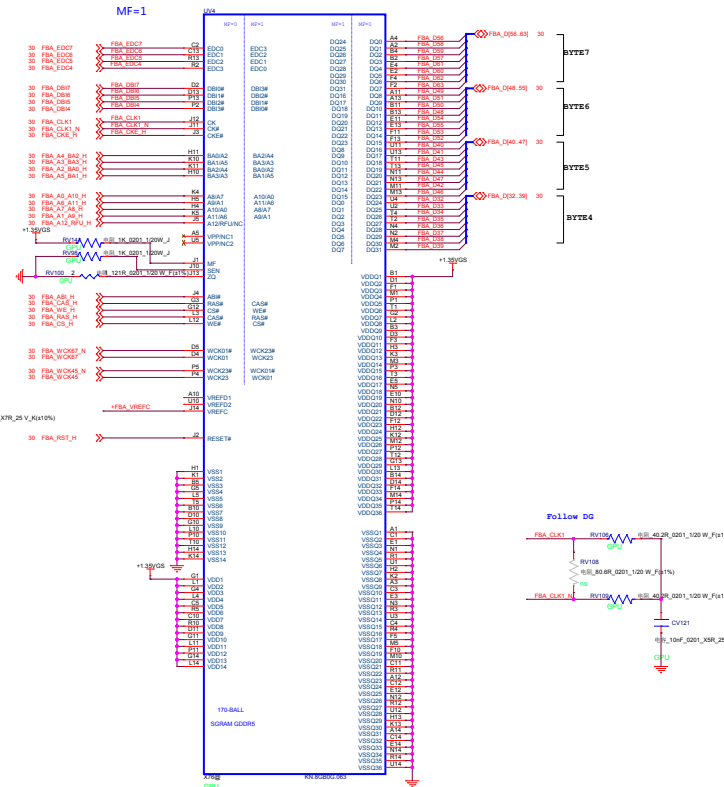
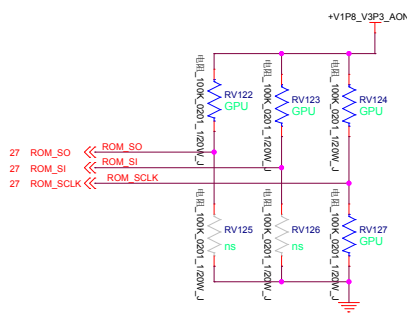
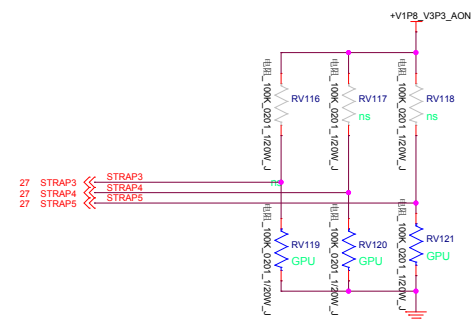
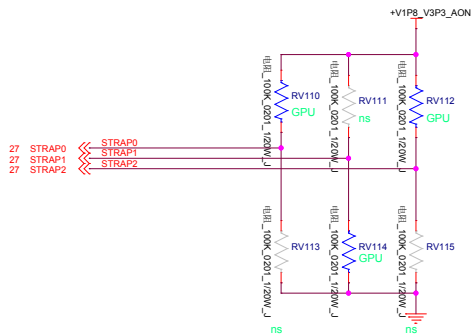


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

| Decoupling Capacitors | | Recommended Quantity and Placement (per DRAM device) | |
|-----------------------------------|-------------|--|--|
| Capacitance | Type [Size] | Quantity | Placement (by DRAM Interface Mode) |
| Combined FBVDD-FBVDDQ Rail | | | |
| 1.0 μ F | X65 [0402] | 10 | For x32 DRAM: Under the DRAM FBVDD or FBVDDQ ball. For x16 DRAM in a "clamshell" PCB configuration: As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor. |
| 10 μ F | X65 [0603] | 4 | |
| 1.0 μ F | X65 [0402] | 8 additional | For x32 DRAM: Choose x32 interface to activate FBVDDQ PCB signal. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDDQ ball via if possible. See Figure 9-23 for an example. |
| 10 μ F | X65 [0603] | 2 | Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor. |
| 22 μ F | X65 [0603] | 5 | For 4-GHz WGL (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor. |

Memory - Upper 32 bits





For N17

| GPU | Vendor | Manufacturer | Strap | Strap2 | Strap1 | Strap0 |
|------------|---------|--------------------|-------|--------|--------|--------|
| N17S-G1 | Samsung | K4G80325FB-HC25 | 0x0 | L | L | L |
| | | MT51J256M32HF-70:A | 0x1 | L | L | H |
| | Hynix | H5GC8H24MJR-ROC | 0x2 | L | H | L |
| | | MT51J256M32HF-70:B | 0x4 | H | L | L |
| N17S_G0/G2 | Hynix | H5GC8H24AJR-ROC | 0x5 | H | L | H |
| | Micron | MT51J256M32HF-80:B | 0x9 | L | M | L |
| | | H5GC8H24AJR-R2C | 0xA | L | M | H |

N17S_G0/G2 follow N17S_G1 with NV confirm

| PN | MPN | STRAP | Vendor |
|--------------|--------------------|-------|---------|
| HQ1121854000 | MT51J256M32HF-70:B | 0x4 | Micron |
| HQ1121852000 | H5GC8H24AJR-ROC | 0x5 | Hynix |
| HQ1121870000 | K4G80325FB-HC25 | 0x0 | Samsung |

| Physical Strapping pin | Power Rail | RAM_CFG[3] | RAM_CFG[0x02] | RAM_CFG[1] | RAM_CFG[0x00] |
|------------------------|------------|------------|---------------|------------|---------------|
| STRAP0 | | L | | | L |
| STRAP1 | | H | | | L |
| STRAP2 | | L | | | L |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

| SMBUS | ALT | ADDR |
|-------|-----|------------------------|
| 0 | | 0x9E (Default) |
| 1 | | 0x9C (Multi-GPU usage) |

| DEVID | SEL |
|-------|-----------|
| 0 | (Default) |
| 1 | |

| PCIE | CFG |
|------|-----------|
| 0 | (Default) |
| 1 | |

| VGA | DEVICE |
|-----|-----------------------------|
| 0 | 3D Device (Class Code 302h) |
| 1 | VGA Device (Default) |

| Physical Strapping pin | Power Rail | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
|------------------------|------------|--------------|--------------|--------------|--------------|
| ROM_SCLK | M | Disable | Disable | Disable | Disable |
| ROM_SI | H | | | | |
| ROM_SO | H | | | | |

Table 5.3 RAMCFG

| Strap Pins <small>(see Note)</small> | | | RAMCFG Setting Number |
|--------------------------------------|--------|--------|--|
| STRAP2 | STRAP1 | STRAP0 | (see Memory RVL for memory configs corresponding to these numbers) |
| L | L | L | 0 (0x0000) |
| L | L | H | 1 (0x0001) |
| L | H | L | 2 (0x0002) |
| L | H | H | 3 (0x0003) |
| H | L | L | 4 (0x0004) |
| H | L | H | 5 (0x0005) |
| H | H | L | 6 (0x0006) |
| H | H | H | 7 (0x0007) |
| L | L | M | 8 (0x0008) |
| L | M | L | 9 (0x0009) |
| L | M | H | 10 (0x000A) |
| L | H | M | 11 (0x000B) |
| M | L | L | 12 (0x000C) |
| M | L | H | 13 (0x000D) |

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

| Memory Density | Allowed Memory Configuration | FBVDD/Q | Vendor | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert | Qual Plan | Status |
|----------------|------------------------------|---------|--------|--------------------------|--------------|-------|--------------------|-----------------|-----------|------------------|
| 8 Gb | 256Mx32 | 1.35V | Micron | MT51J256M32HF-80:B | B-die | 0x9 | 8 Gbps | N/A | Full | Production ready |
| | 512Mx16 | | Hynix | H5GC8H24AJR-R2C | A-die | 0xA | 8 Gbps | N/A | Full | Production ready |

Notes:

- For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
- N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | |
| C | | | | | |
| B | | | | | |
| A | | | | | |



HUAQIN
华勤通信

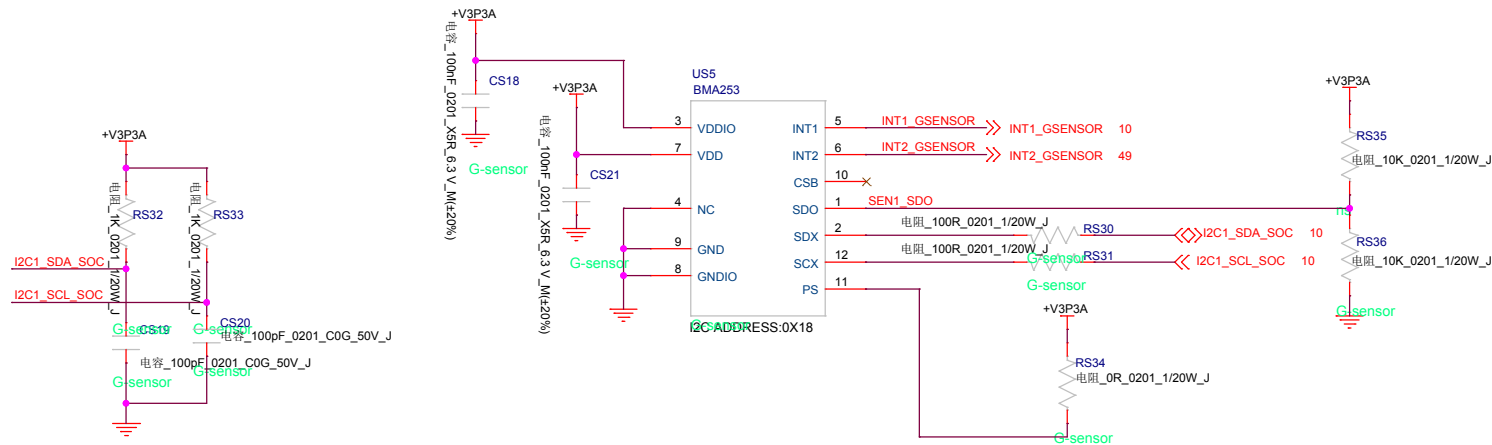
Huaqin Telecom Technology Com.,Ltd.

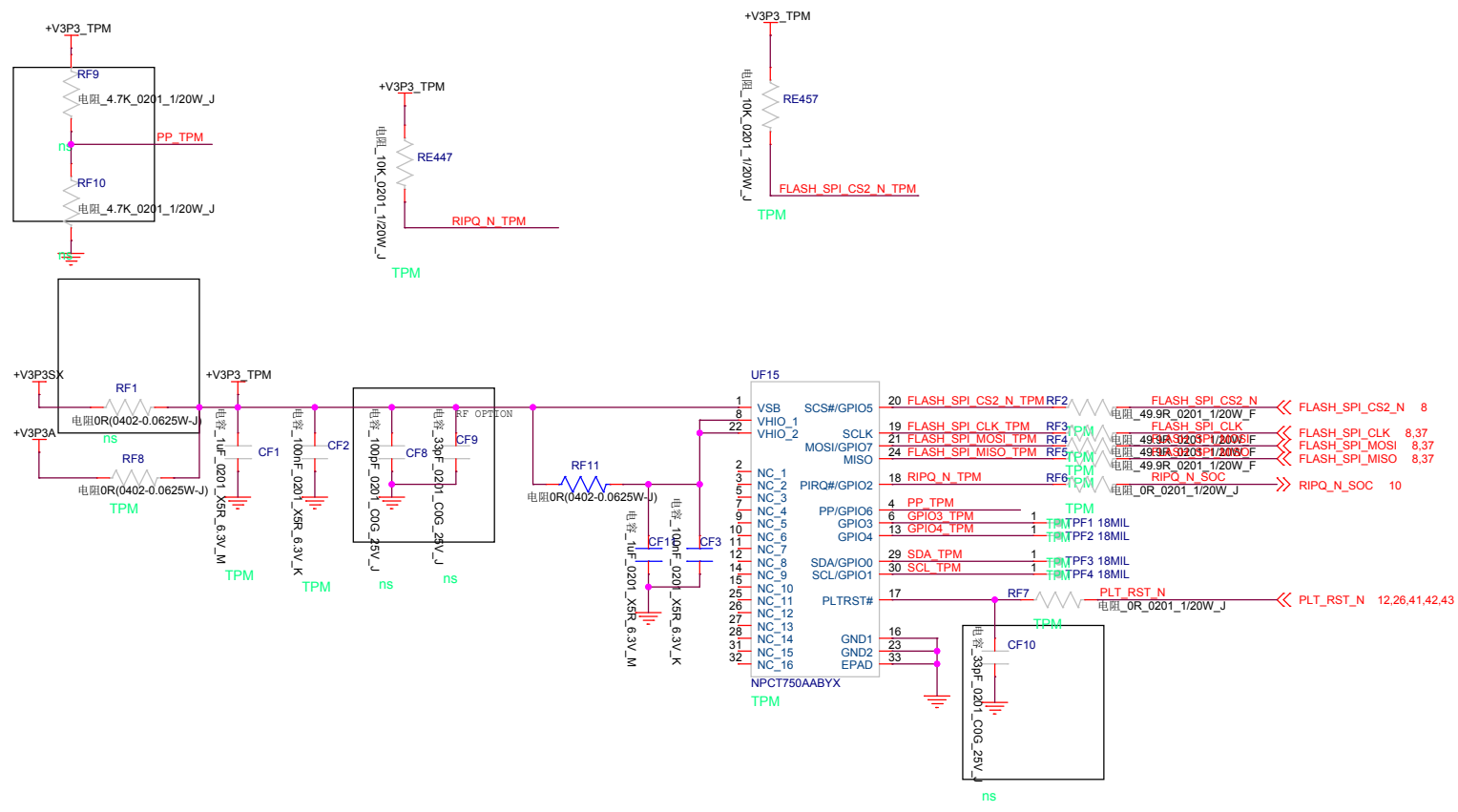
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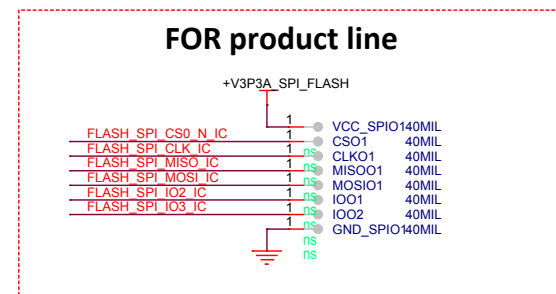
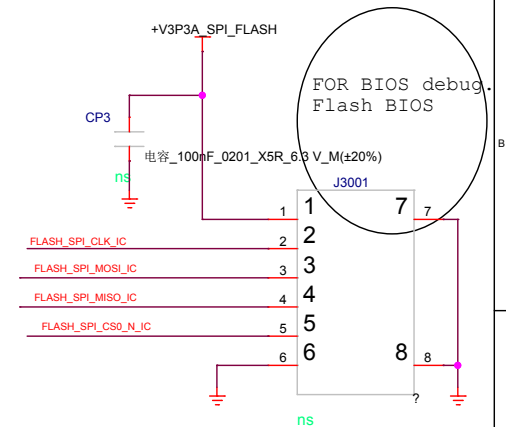
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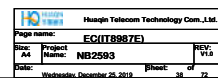
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| Date: Wednesday, December 25, 2019 | Sheet: 33 of 72 |
|---------------------------------------|--------------------|

ODD

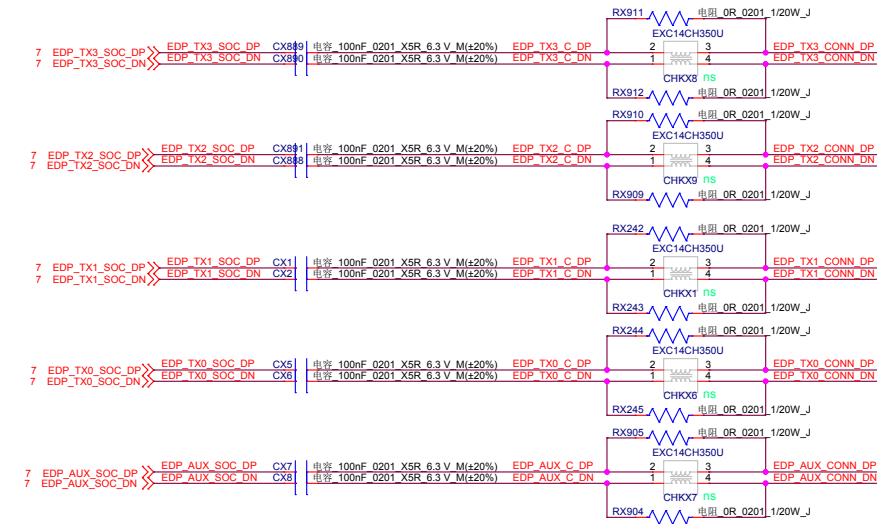




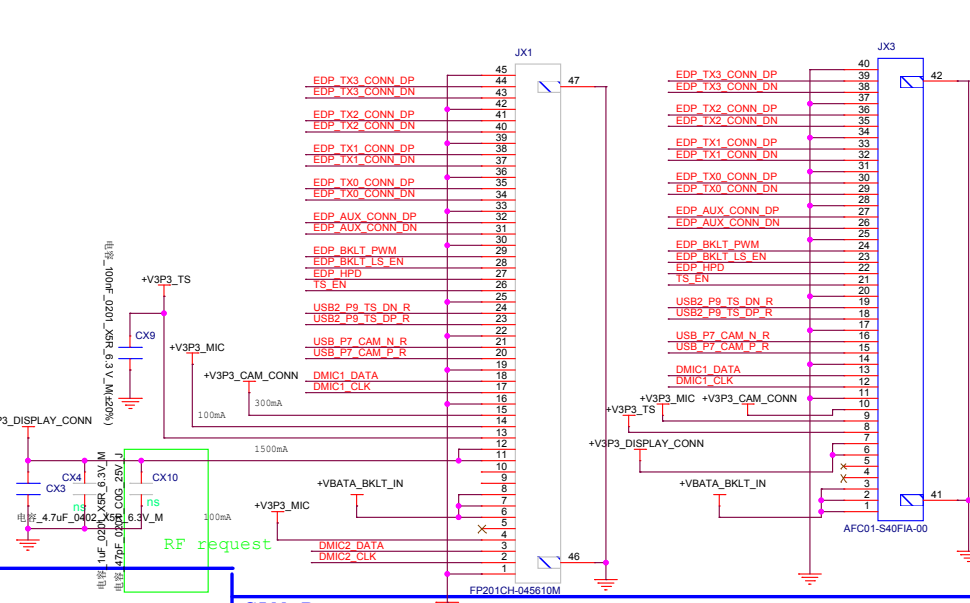
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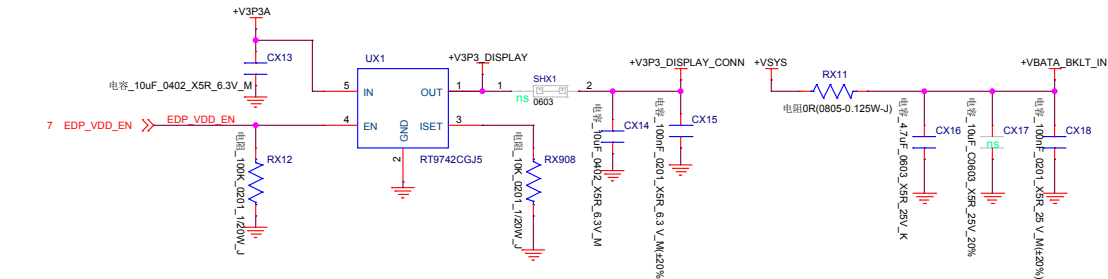
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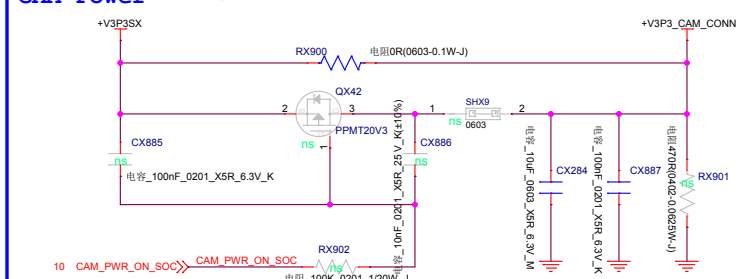
eDP & CAM & DMIC & Touch Panel CONN



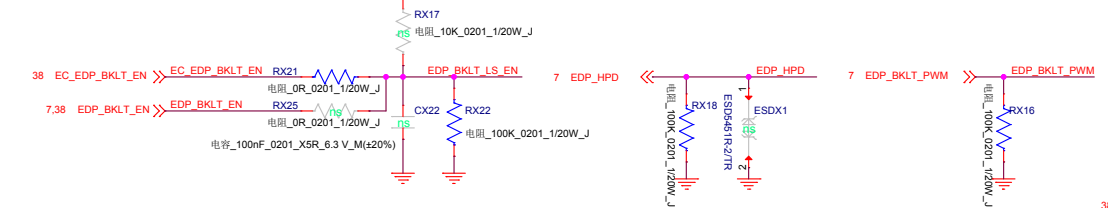
eDP VCC & BL Power



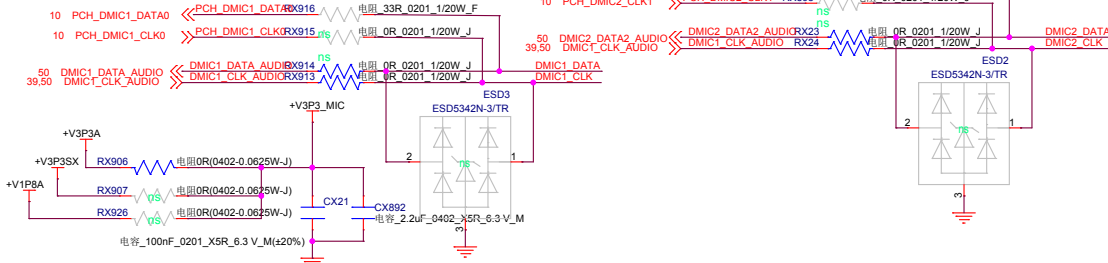
CAM Power



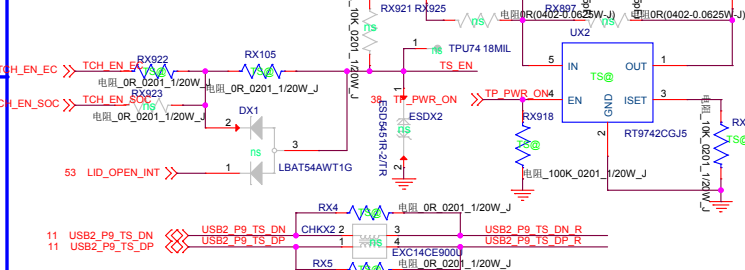
eDP Control



MIC



Touch Panel



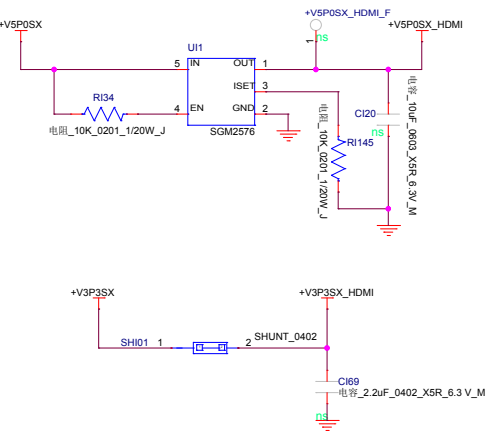
Huaqin Telecom Technology Co., Ltd.

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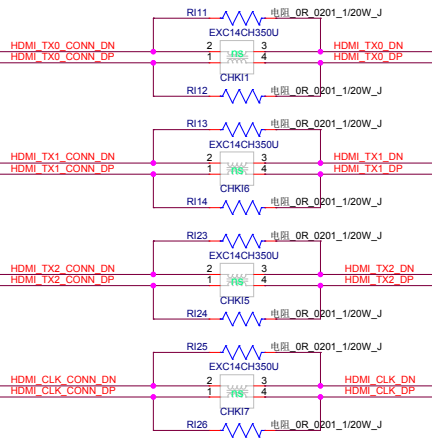
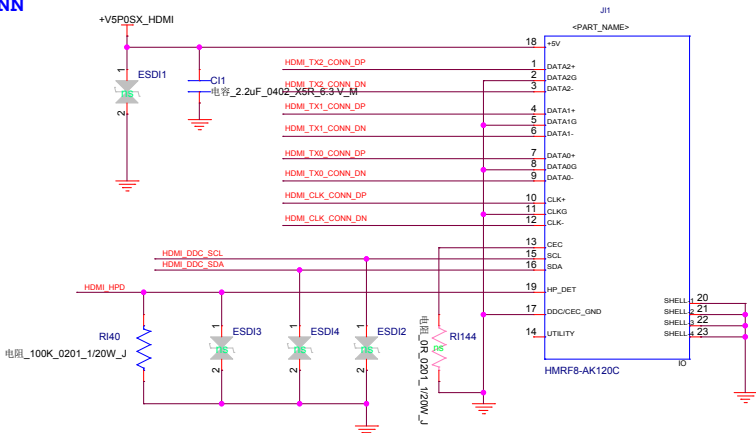
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Date: Wednesday, December 25, 2019 Sheet: 39 of 72

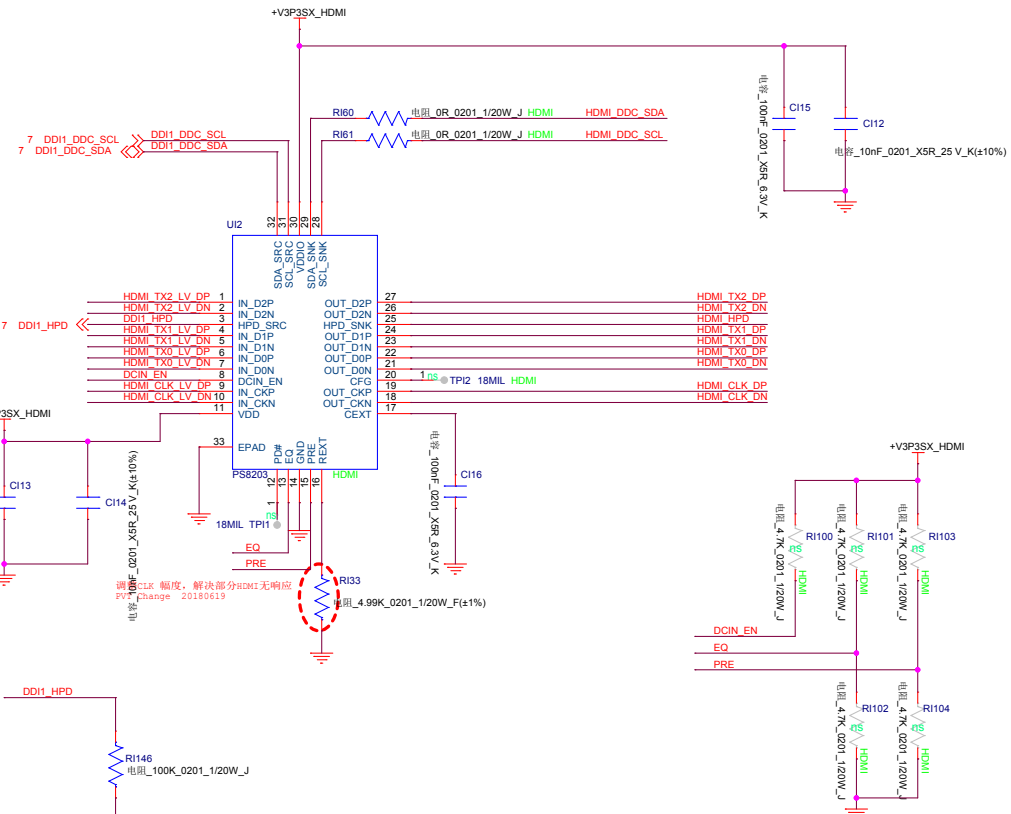
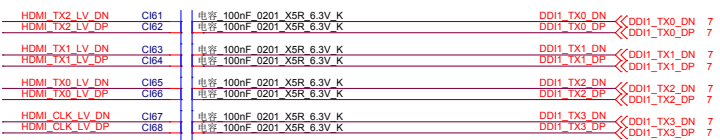
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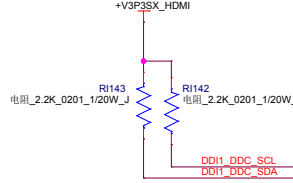
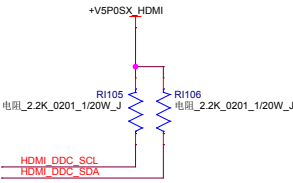
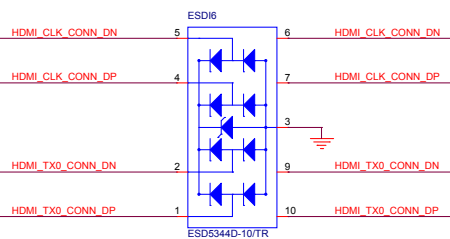
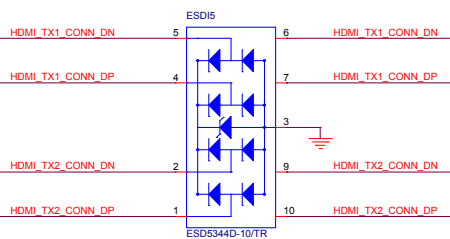
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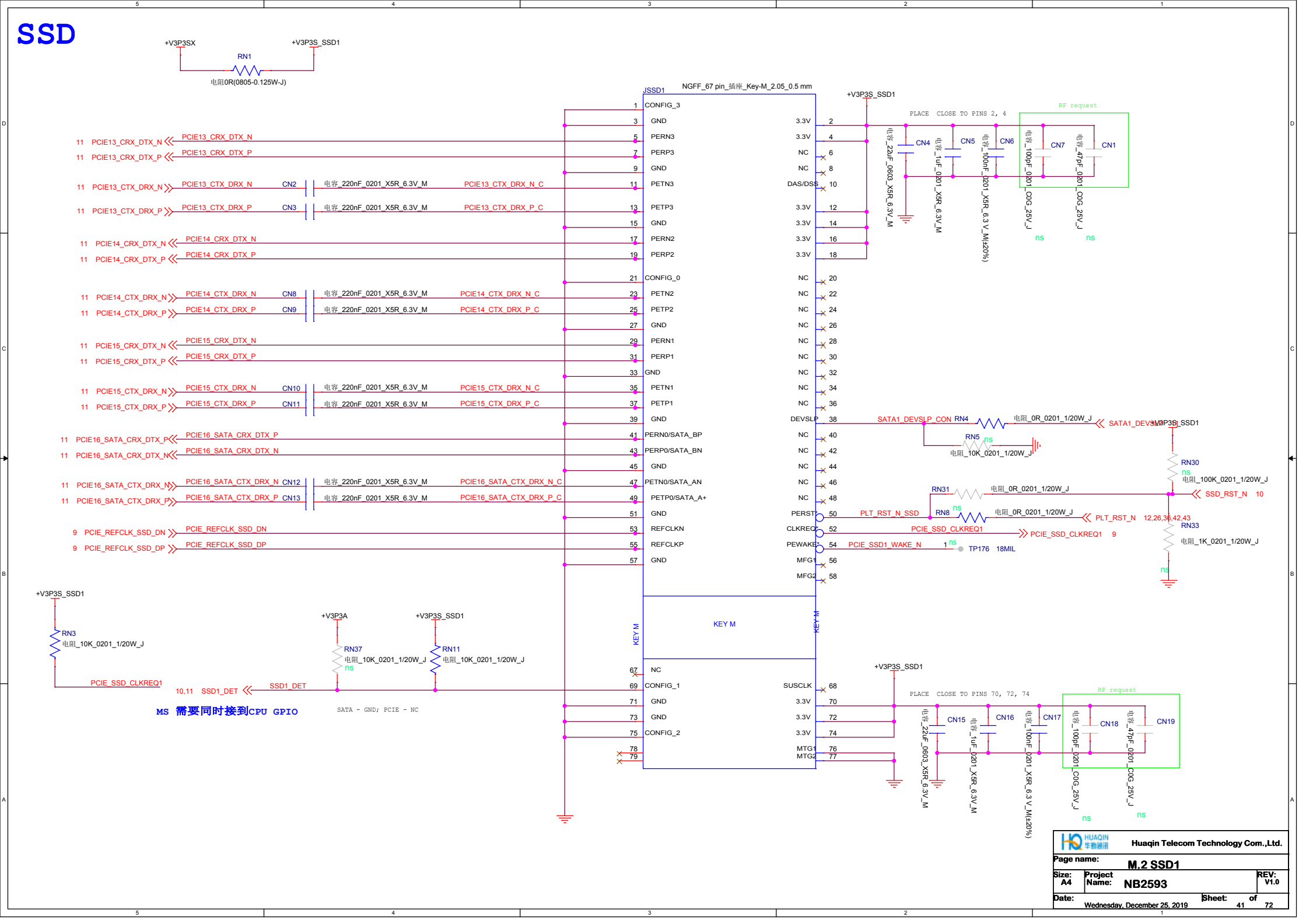
Signal

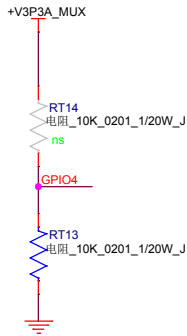


ESD



SSD

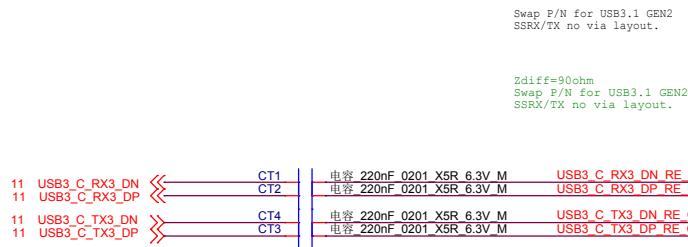




RT14
电阻_10K_0201_1/20W_J
ns

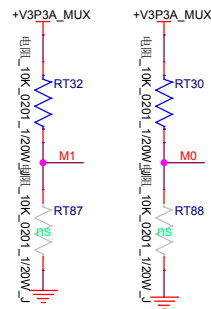
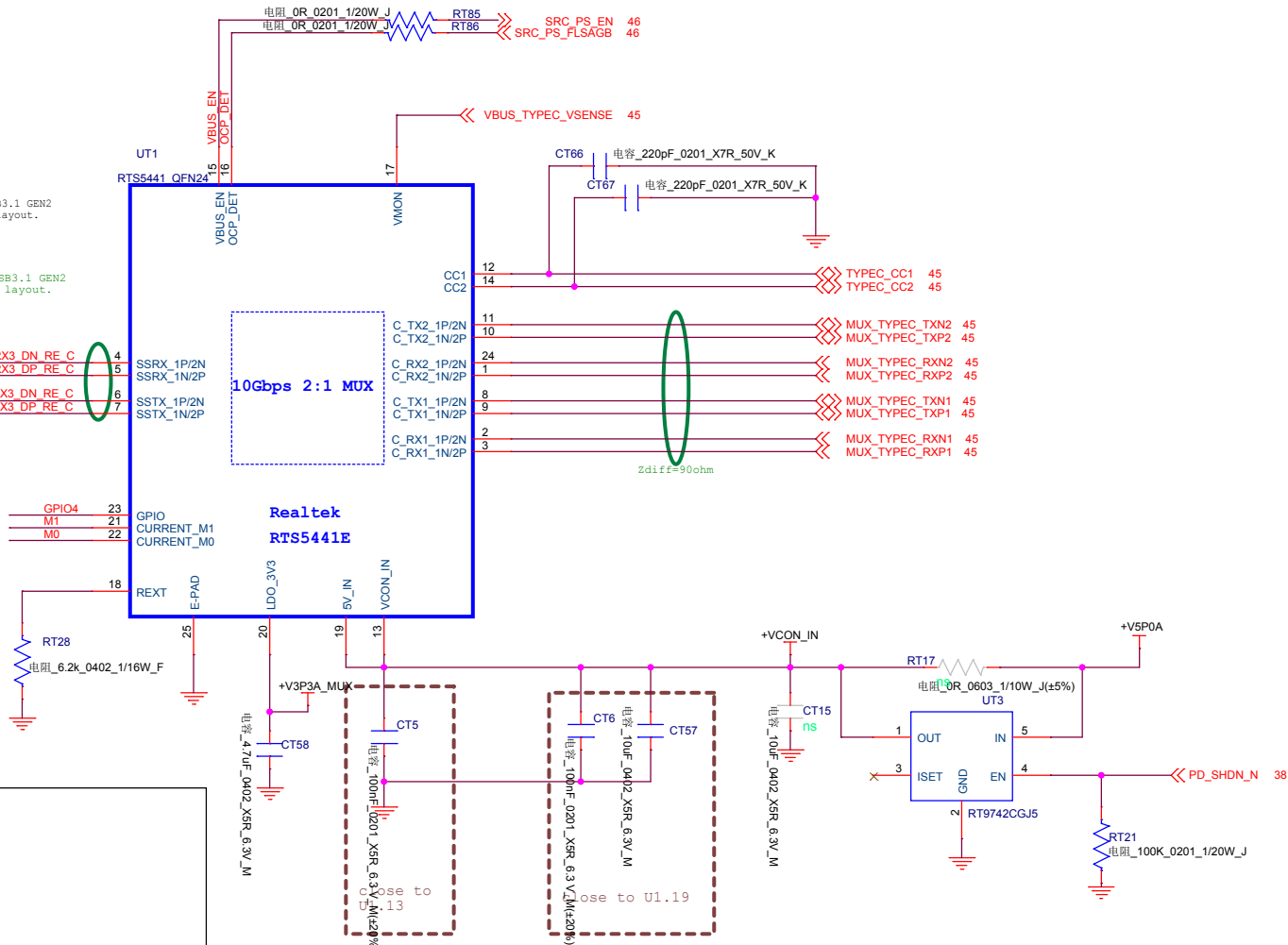
GPIO4

RT13
电阻_10K_0201_1/20W_J



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SSRX/TX no via layout.

Zdiff=90ohm
Swap P/N for USB3.1 GEN2
SSRX/TX no via layout.

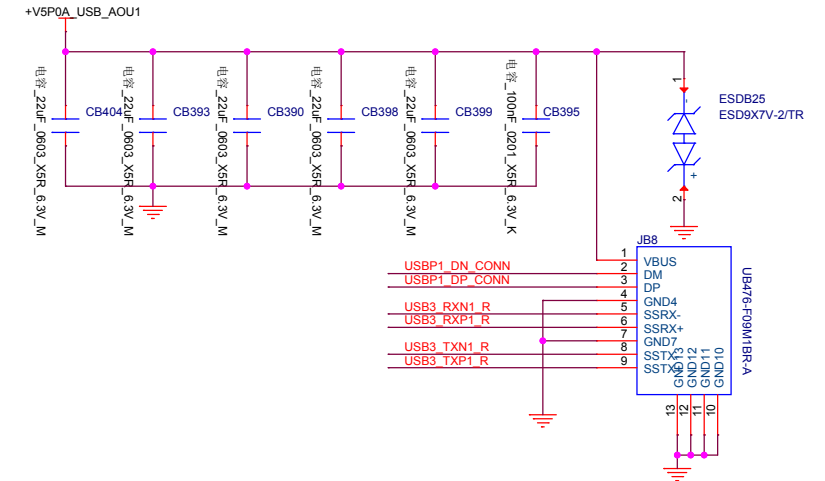
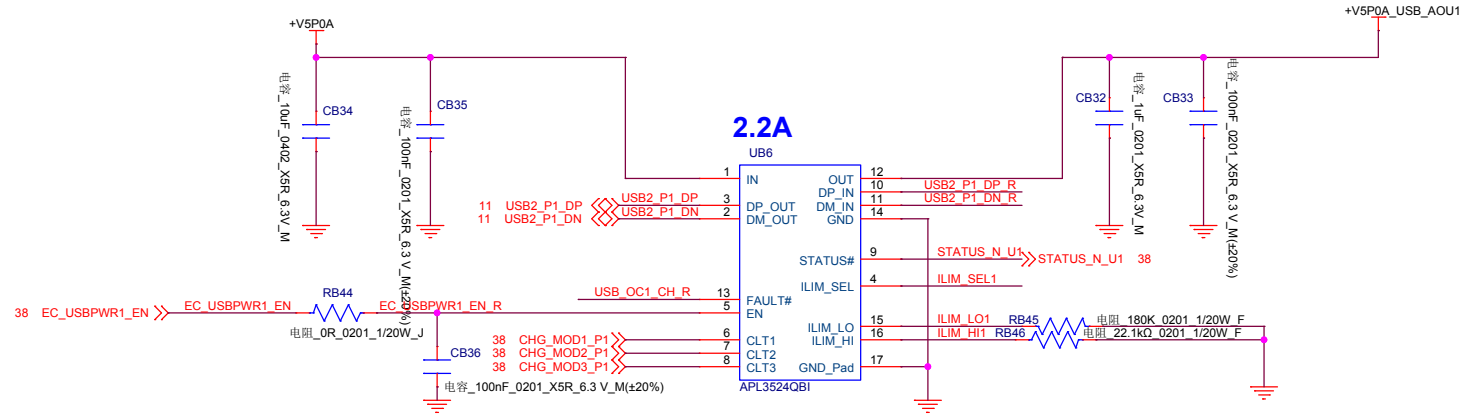


Rp configuration

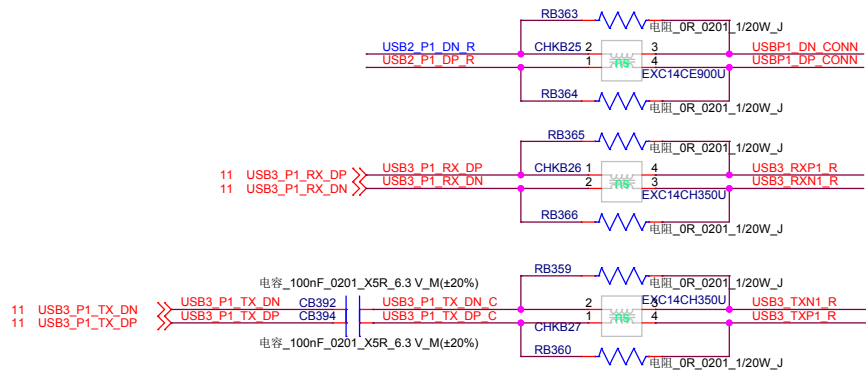
| | M1 | M0 | Note |
|-----------|----|----|--|
| Rp: 900mA | 0 | 1 | RT34/RT30 mount, RT32/RT35 don't mount |
| Rp: 1.5A | 1 | 0 | RT32/RT35 mount, RT34/RT30 don't mount |
| Rp: 3.0A | 1 | 1 | RT32/RT30 mount, RT34/RT35 don't mount |

Rp: 3.0A (now)

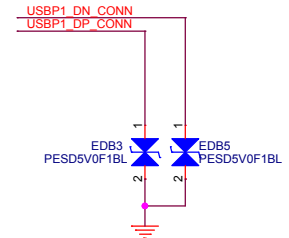
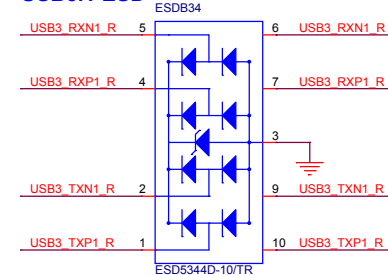
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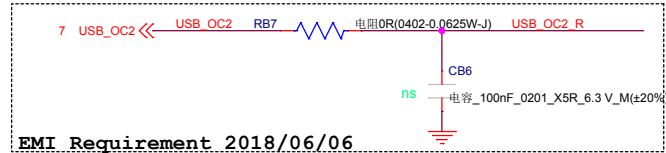
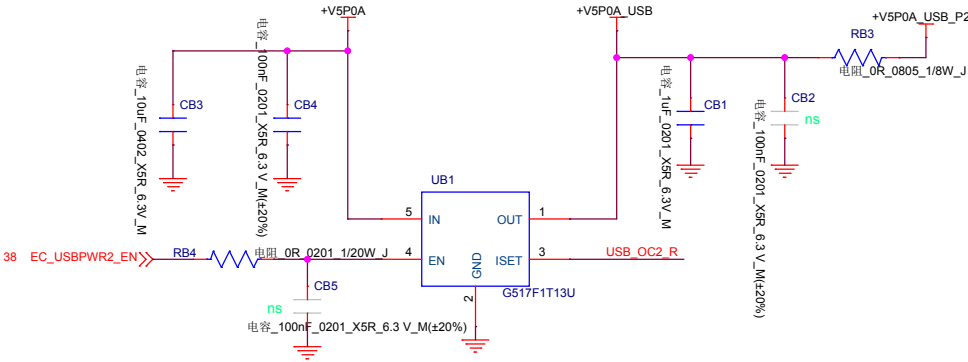
USB3.1 Signal



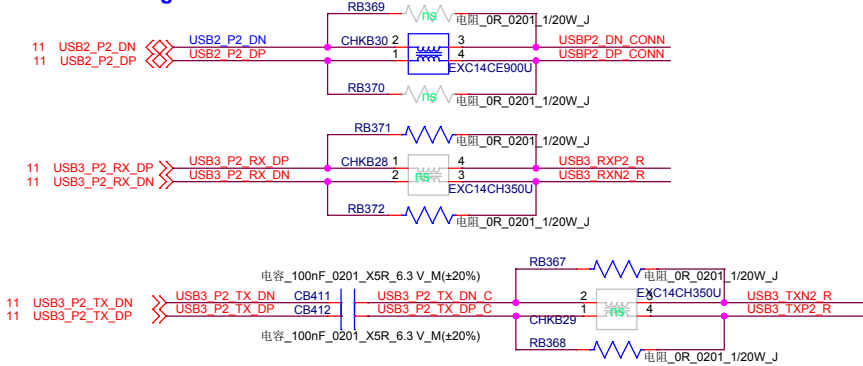
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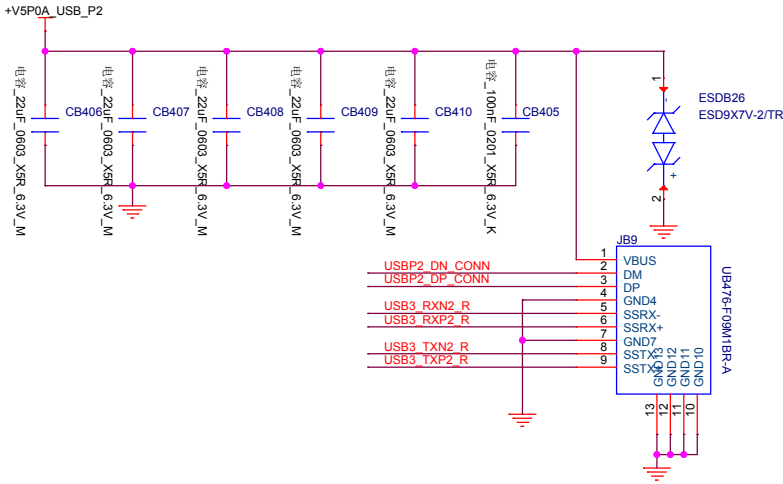
USB3.1 POWER Port2



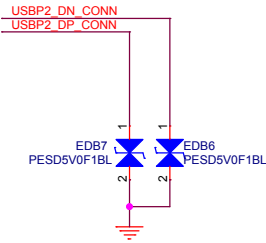
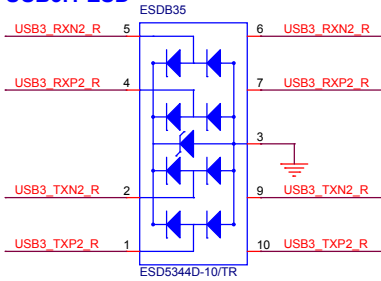
USB3.1 Signal



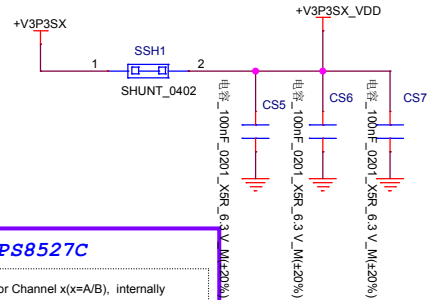
HUANWULIAO



USB3.1 ESD



HDD



For PS8527C

Equalization level setting for Channel x(x=A/B), internally tied to VDD2

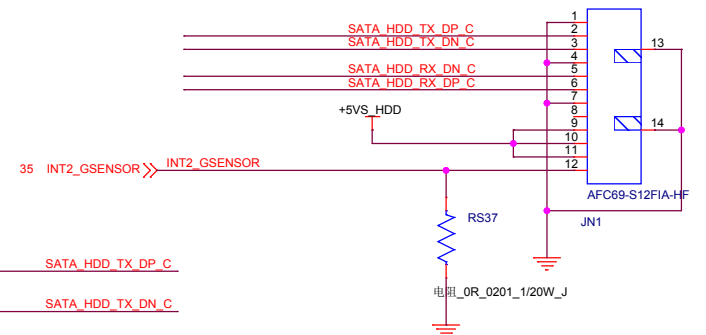
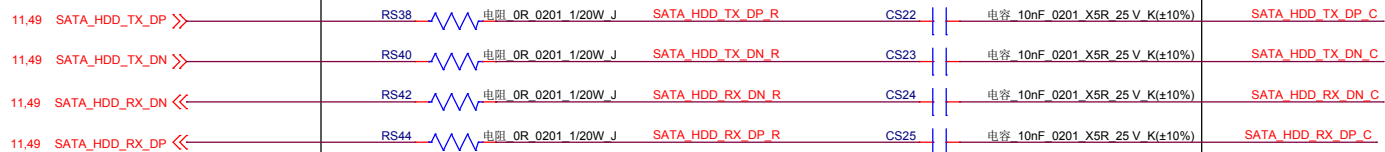
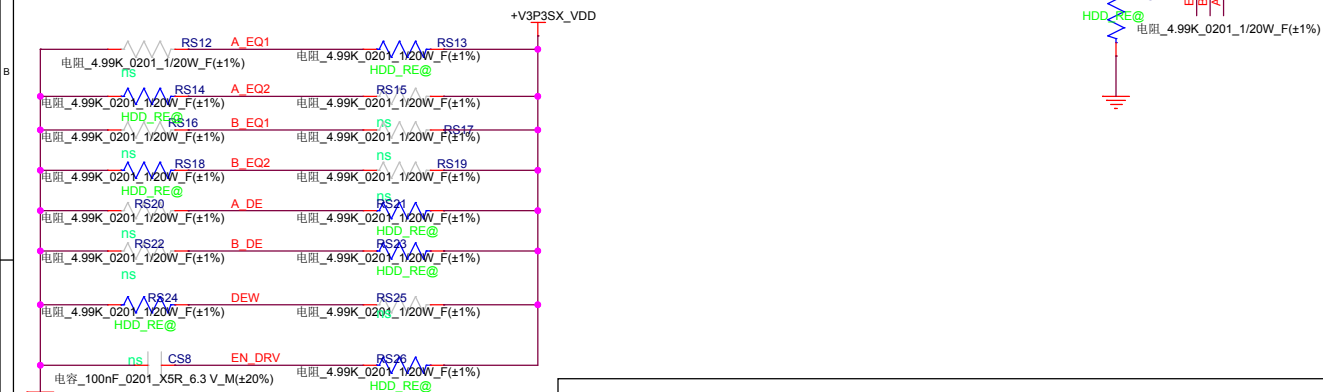
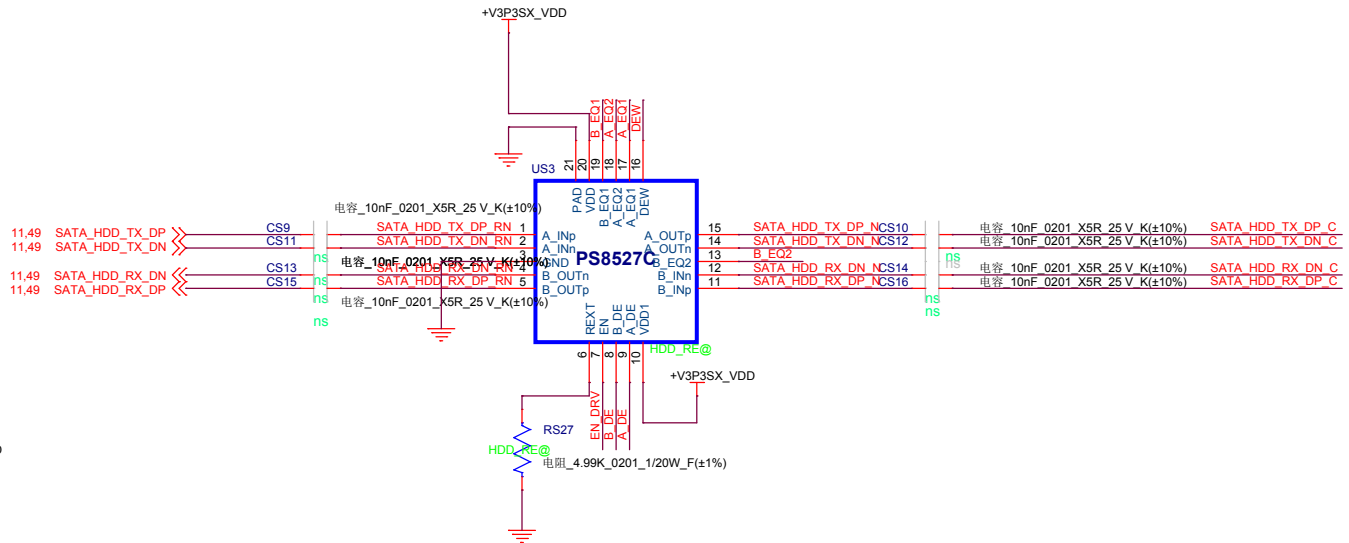
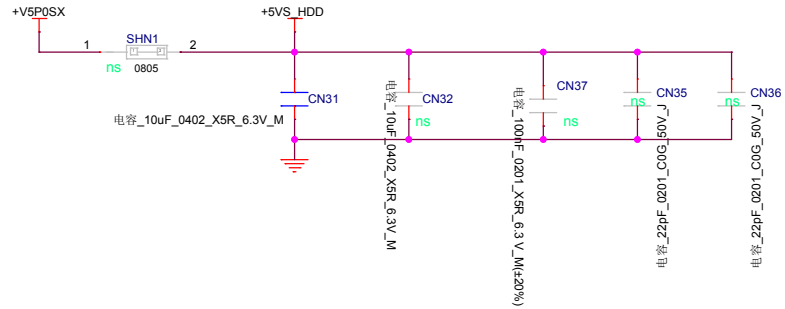
```
[x_EQ2, x_EQ1] ==
```

- L/M: for channel loss up to 2.4dB
- L/L: for channel loss up to 7.4dB
- L/H: for channel loss up to 14.4dB
- M/M: for channel loss up to 12.2dB
- M/L: for channel loss up to 9.4dB
- M/H: for channel loss up to 13.3dB
- H/M: for channel loss up to 6.2dB
- H/L: for channel loss up to 11.2dB
- H/H: for channel loss up to 5dB

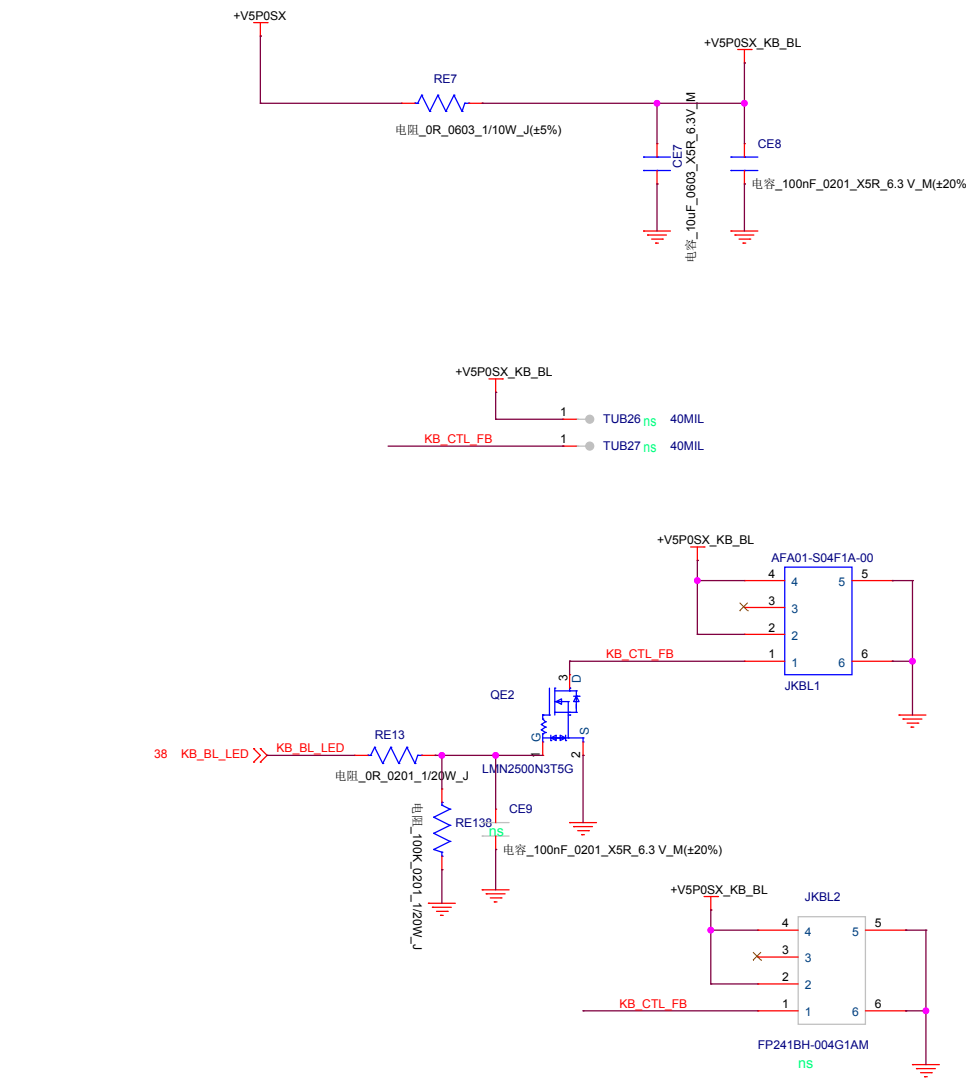
De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2

| |
|-----------|
| [x_DE] == |
| M: -3.5dB |
| L: 0dB |
| H: -1.5dB |

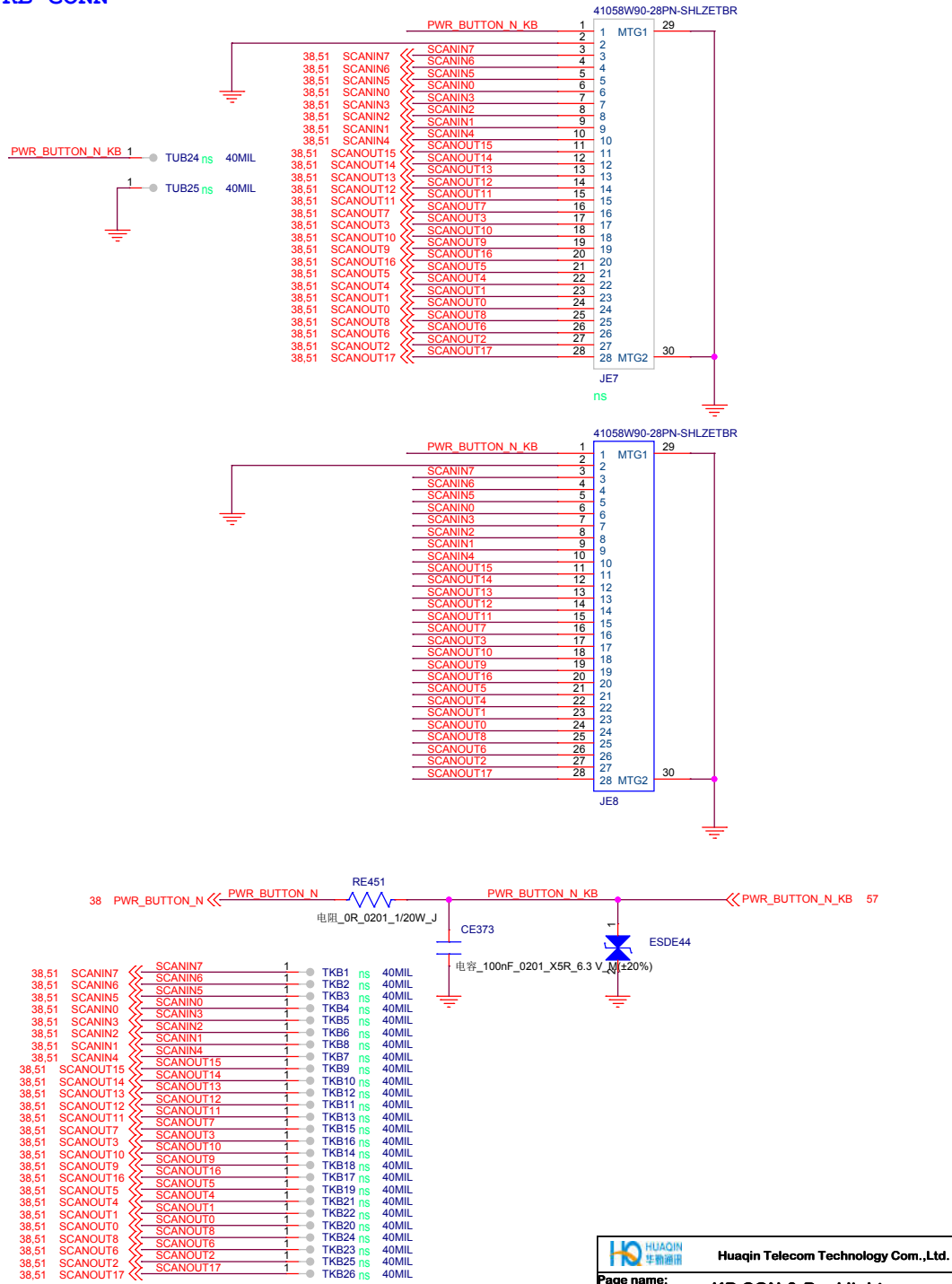
De-emphasis width adjustment, internally pulled down
[DEW] ==
L: for SATA3
H: for SATA2



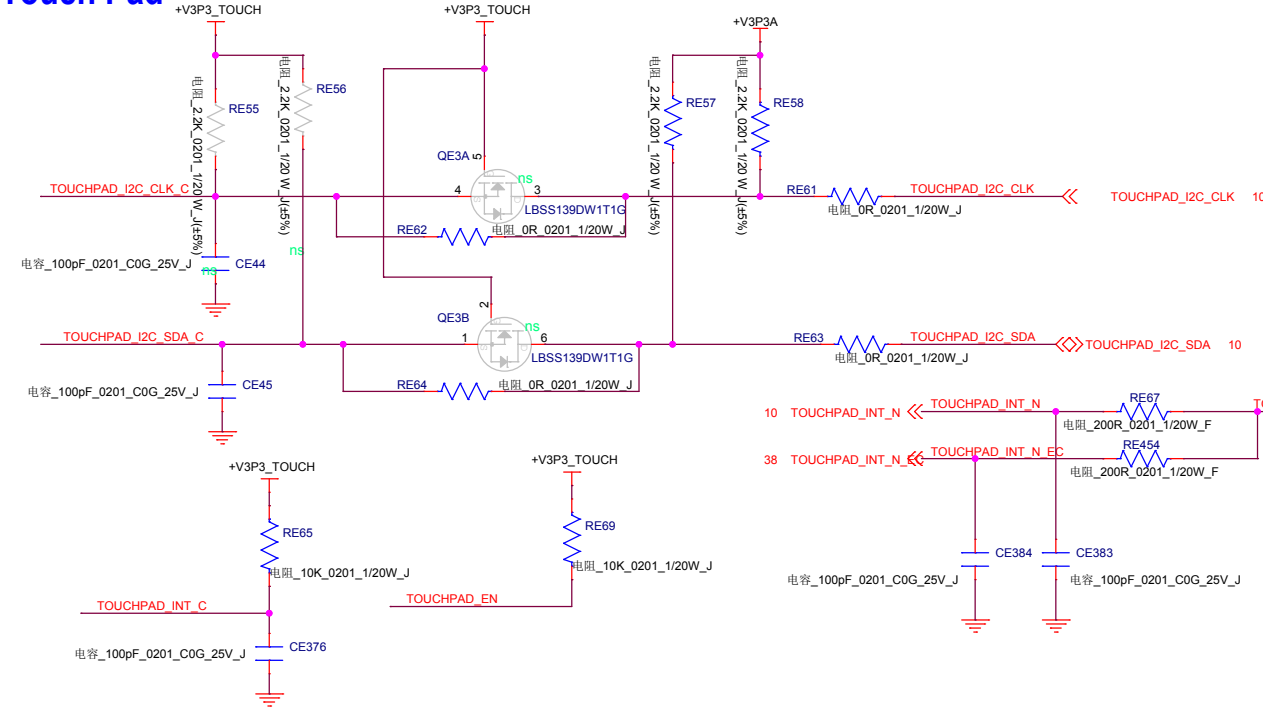
KB Backlight



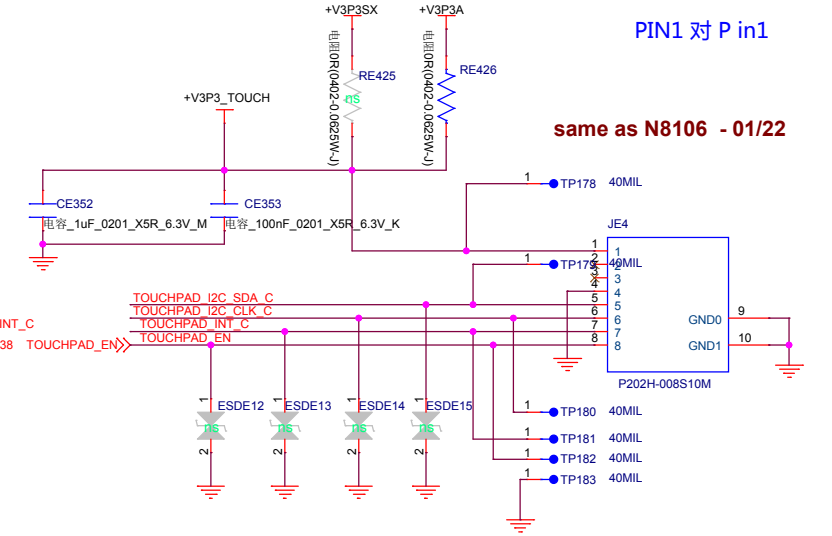
KB CONN



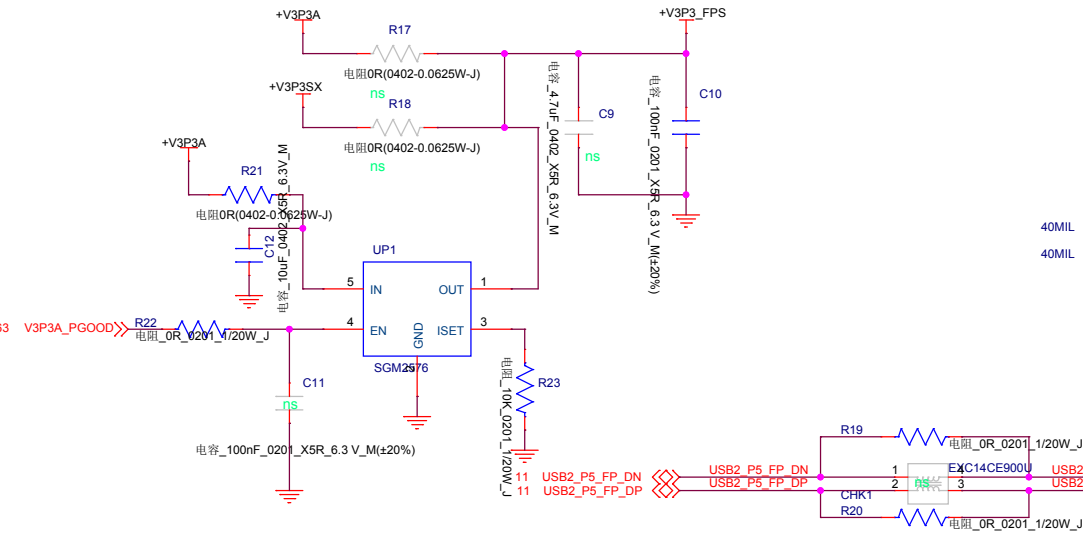
Touch Pad



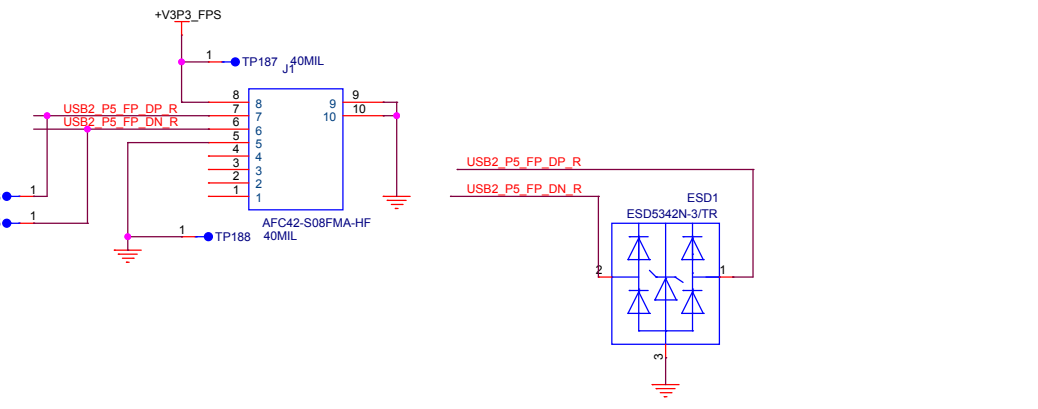
Touch Pad CONN



Finger Print



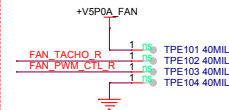
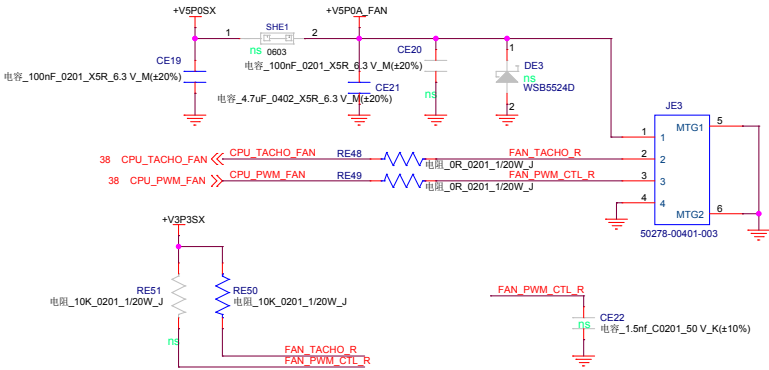
Finger Print CONN



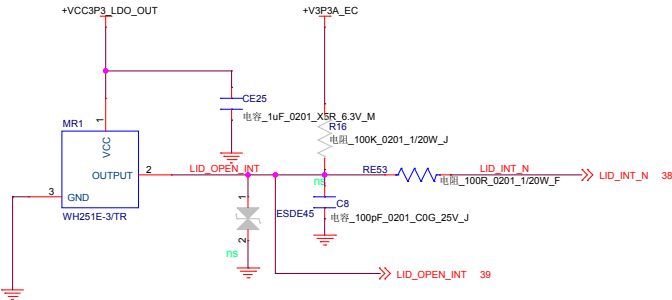
Voice input with LED

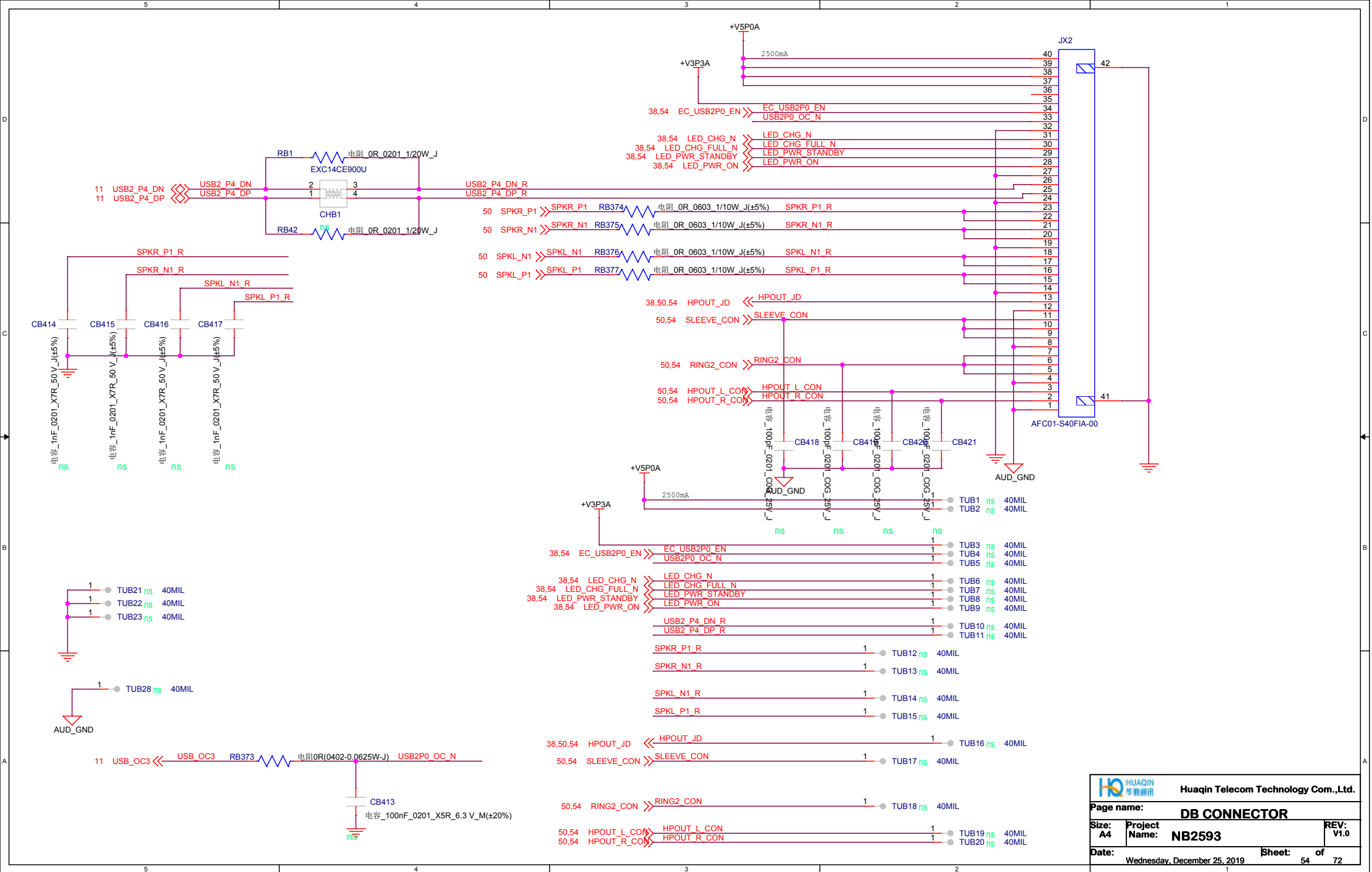
FAN CONN

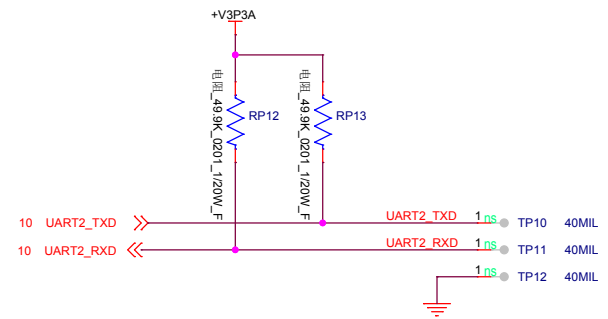
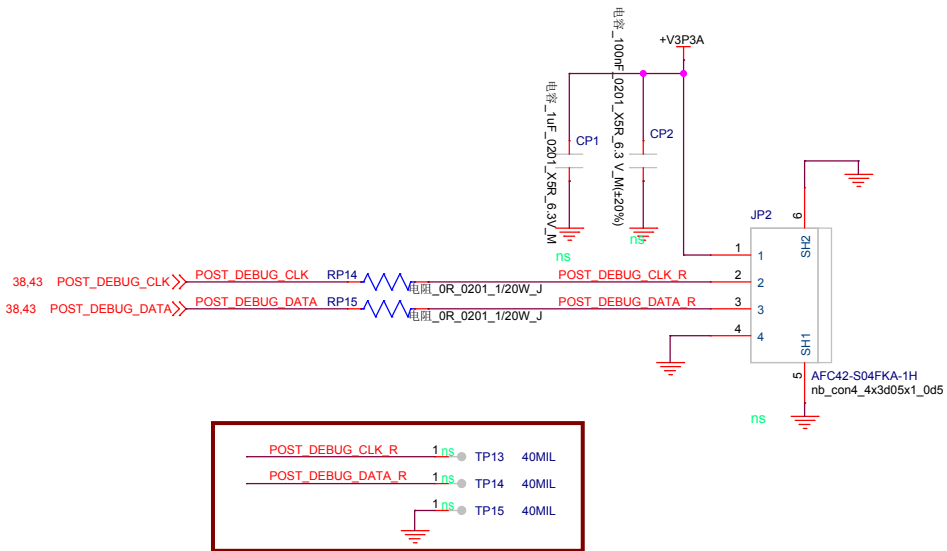
FOR product line



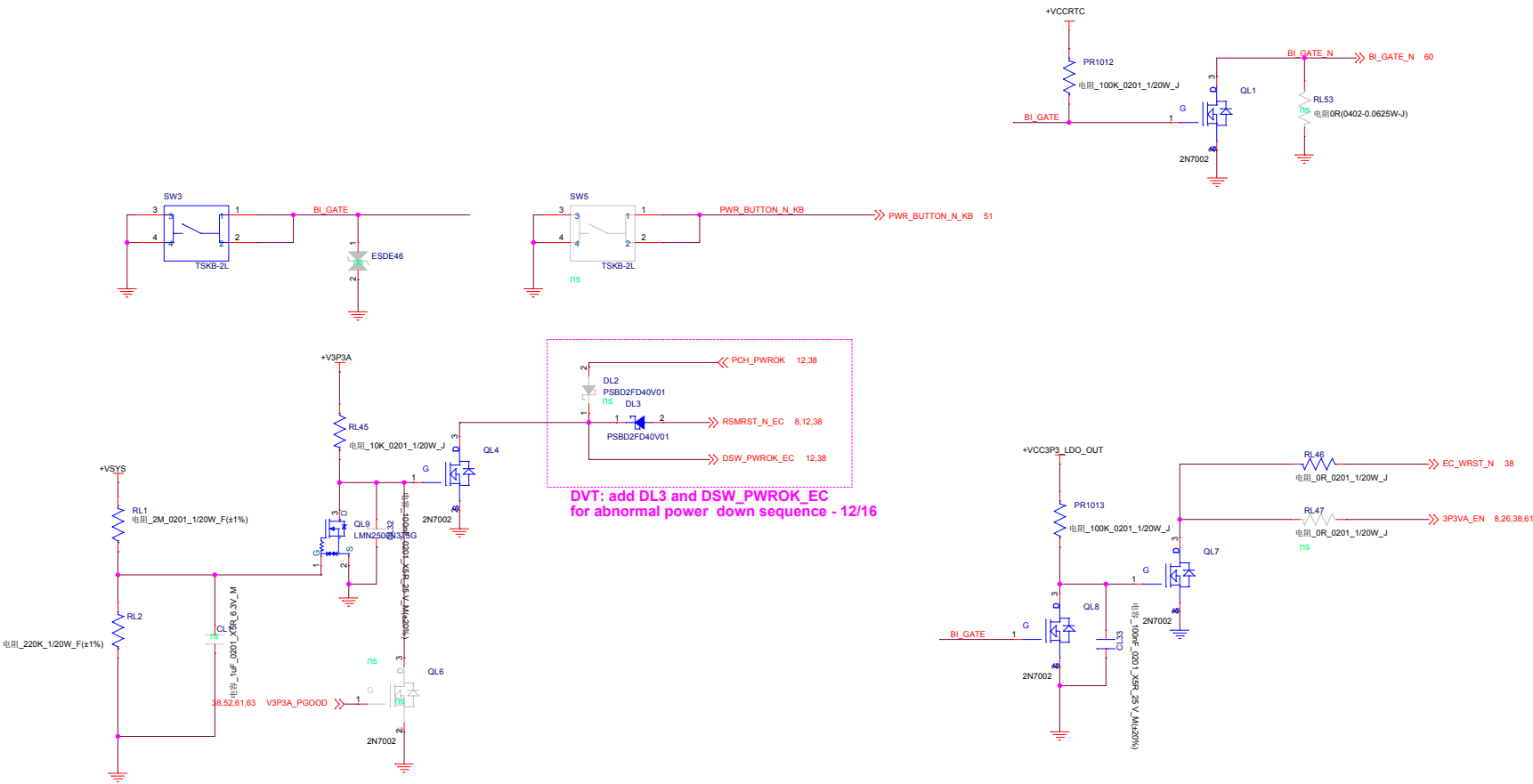
HALL





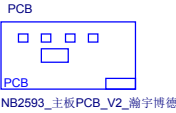
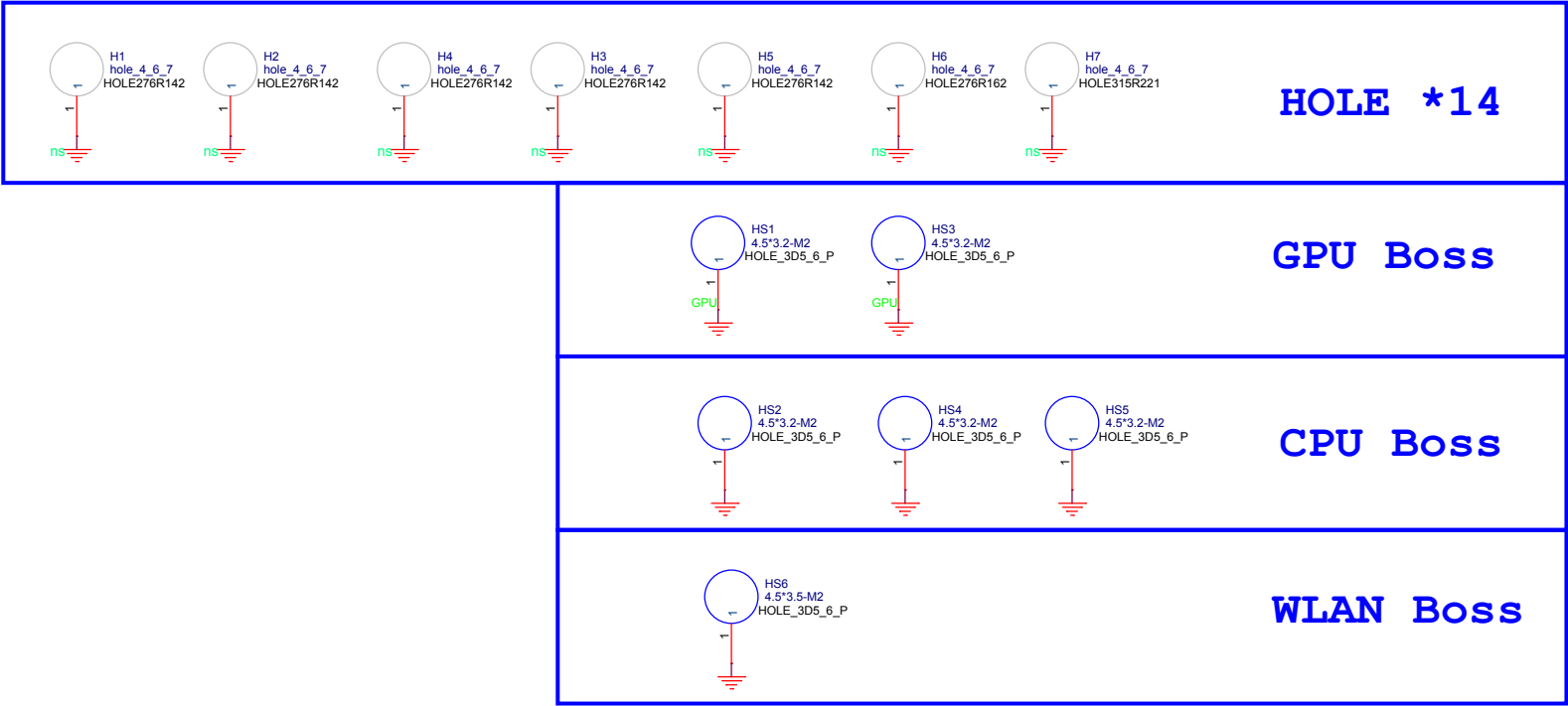


Reset BUTTON

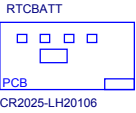


Need add HQ CODE and Stuff

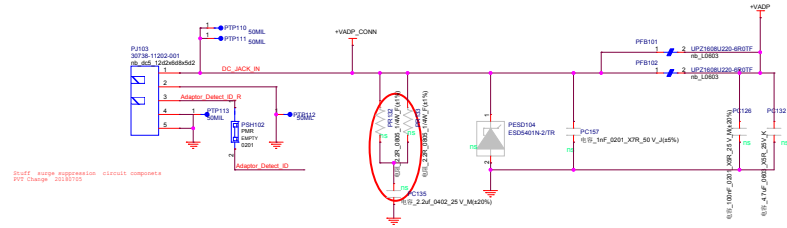
Thermal 螺母元件



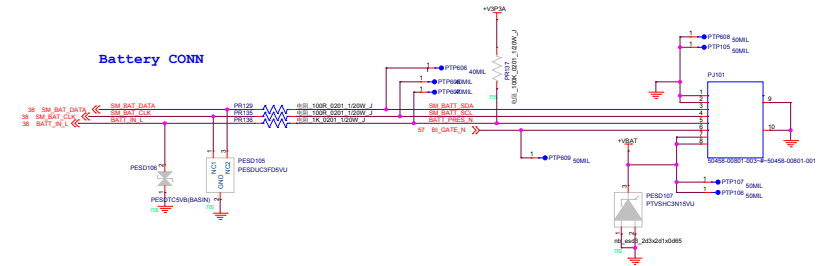
PCB



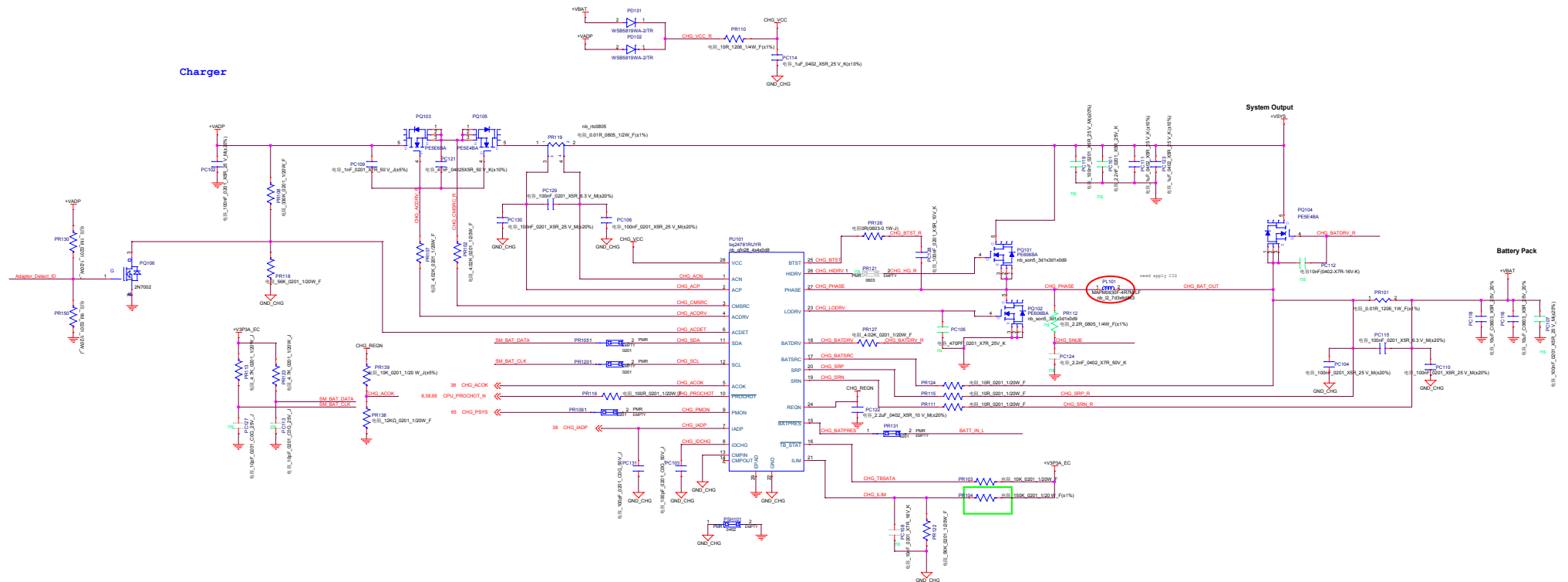
DC-IN



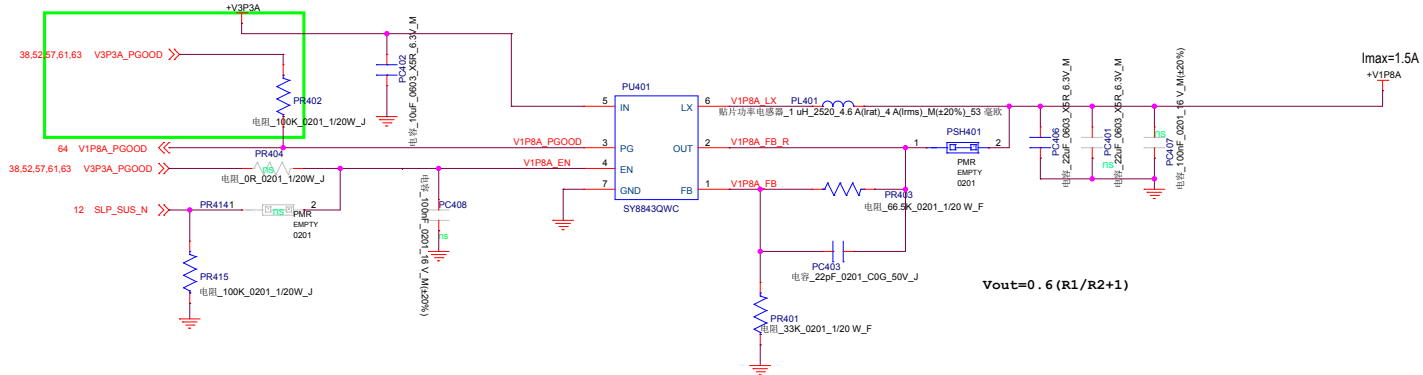
Battery CONN

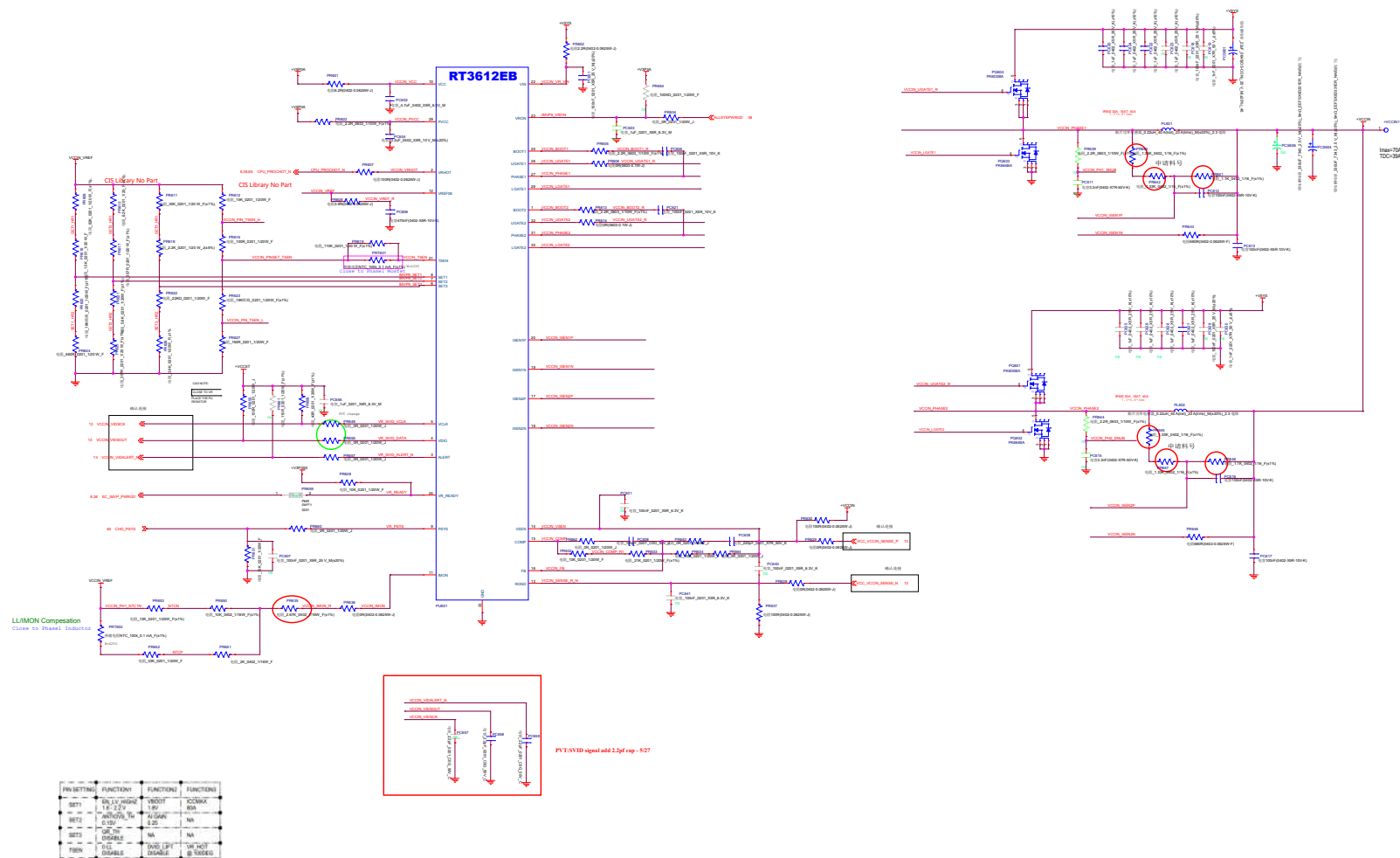


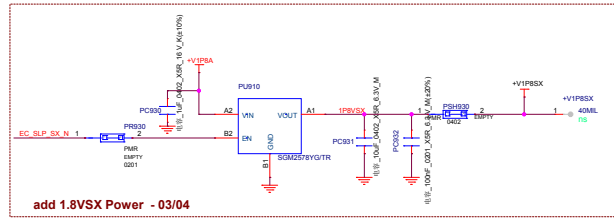
Charger



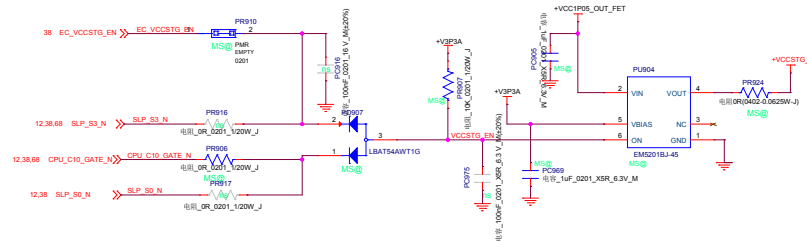
+V1P8A



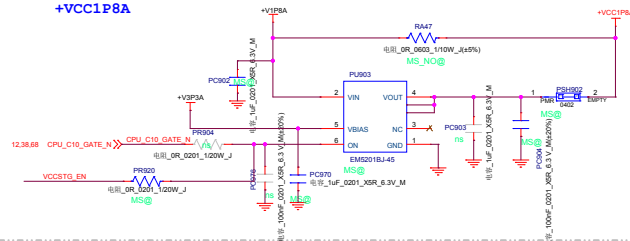




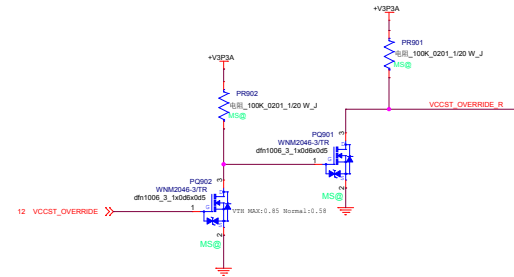
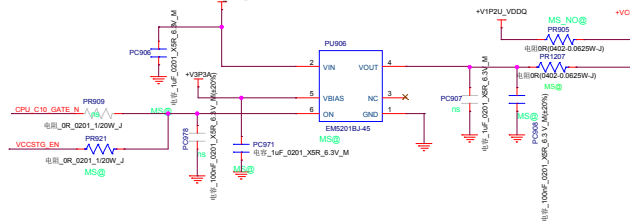
+VCCSTG_IO



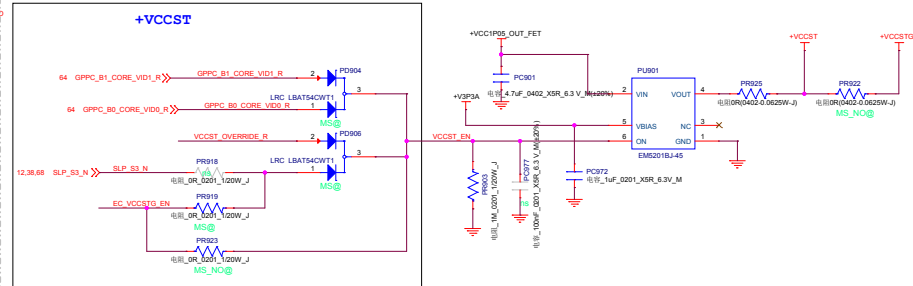
+VCC1P8A



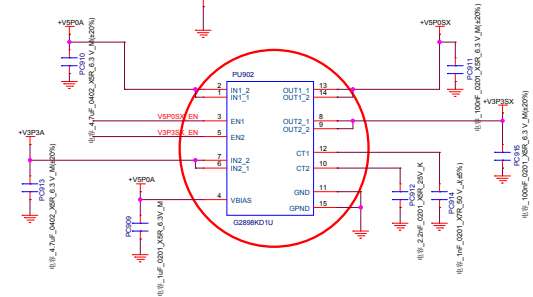
+VCCSPR_OC



+VCCST



+V3P3SX, +V5P0SX G2898



| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | |
| C | | | | | |
| B | | | | | |
| A | | | | | |

