HuaQin Confidential

NB8511/12_M/B Schematics Document

Intel ICL Lake U-Processor with LPDDR4

REV1.0

2019-02-01

Author	Leo.Liu & Payne.Zhang
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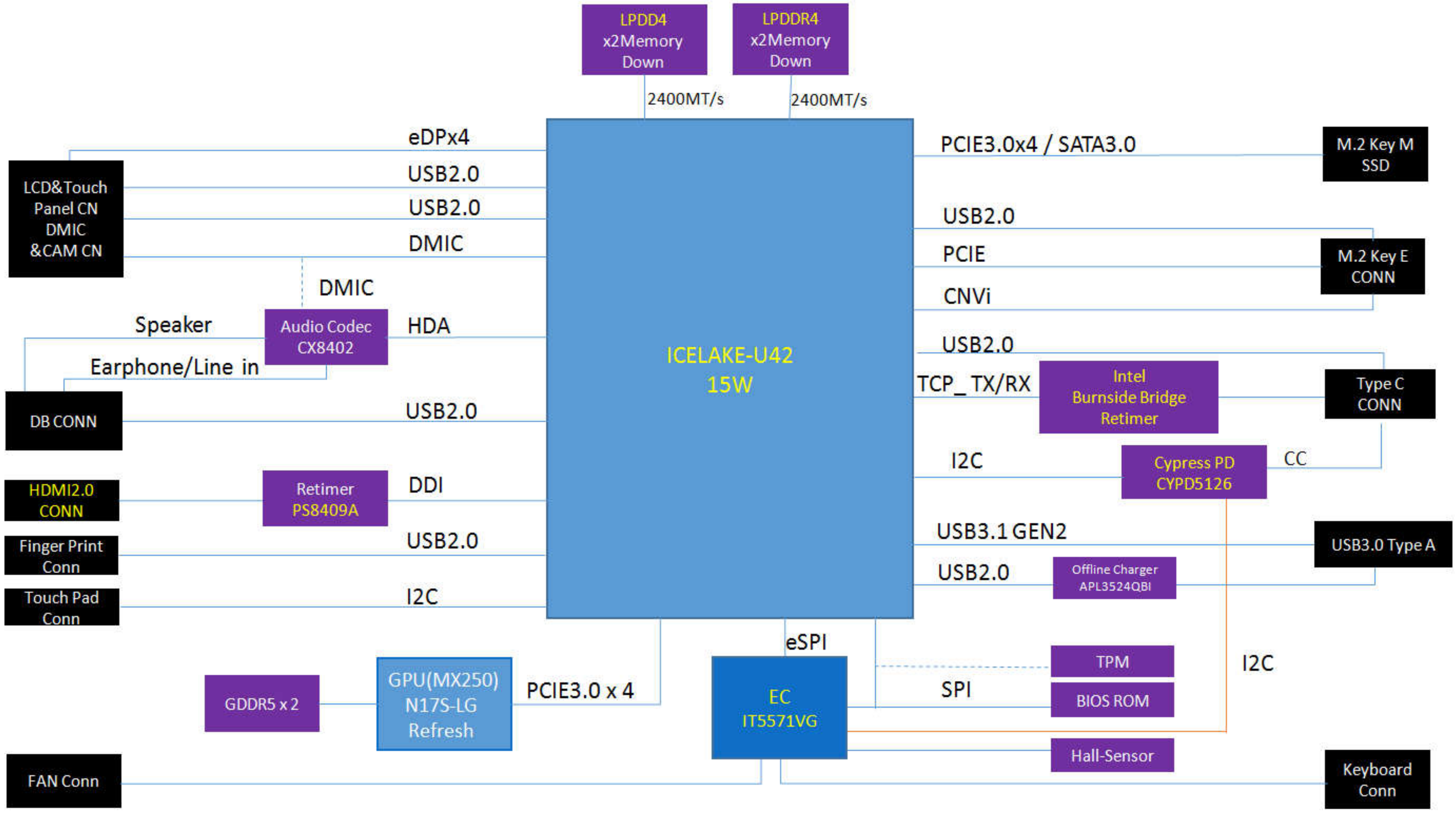

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MEM ID

HW_ID3	HW_ID2	HW_ID1	HW_ID0	Description	Total
0	0	0	0	SAMSUNG LPDDR4 3733 1GB K4F8E304HB-MGCJ LF+HF D20	4GB
0	0	0	1	HYNIX LPDDR4 3733 1GB H9HCNNN8KUMLHR-NME LF+HF DDP	4GB
0	0	1	0	MICRON LPDDR4 4266 2GB MT53E512M32D2NP-046 WT:E LF+HF Z11N	8GB
0	1	0	0	HYNIX LPDDR4 3733 2GB H9HCNNNBPUMLHR-NME LF+HF DE	8GB
0	1	0	0		16GB
1	0	0	0	HYNIX LPDDR4X 4266 4GB H9HCNNNCPMALHR-NEE LF+HF QDP	
				4x 16Gb(reserve)	

GPU ID

HW_ID5	HW_ID4	Description	
		N17-LG-Refresh	N17-LG
0	0	NC	NC
1	0	Mount	
1	1		Mount

KB BL ID

HW_ID6	Description
0	No keyboard Backlignt
1	Keyboard Backlignt

Reserve ID

HW_ID7	Description
0	Reserve
1	Reserve

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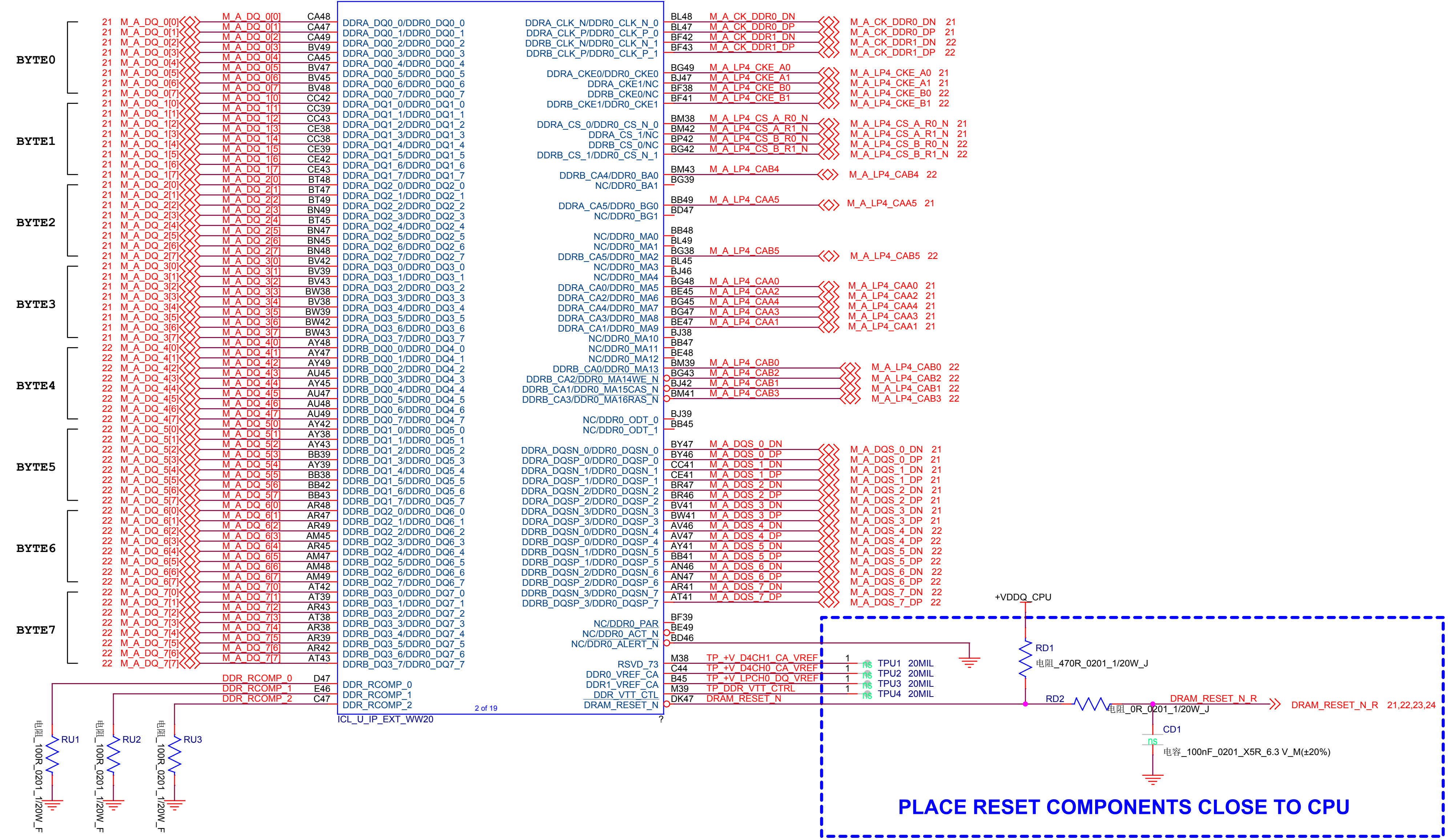
CHA



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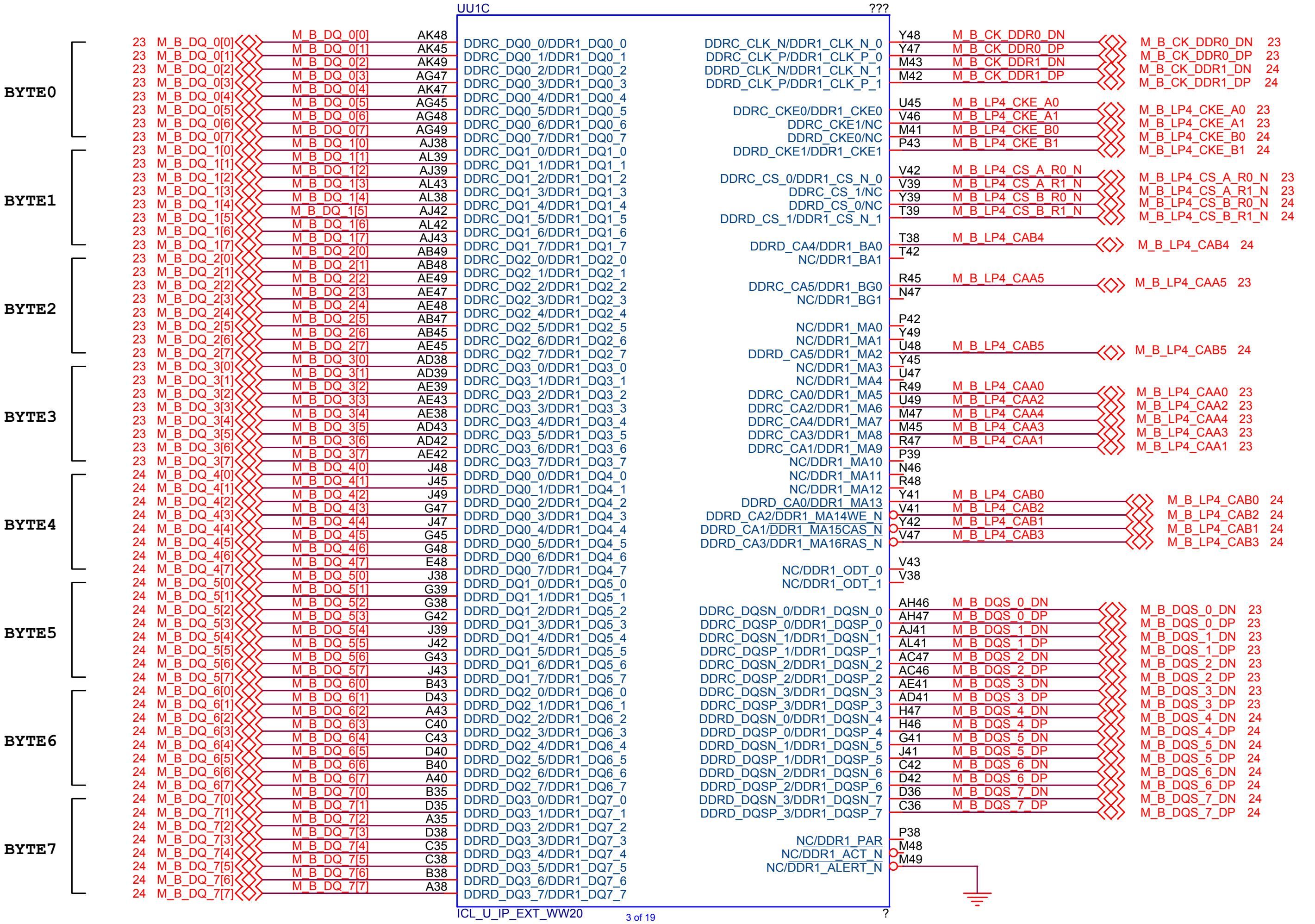
CHB



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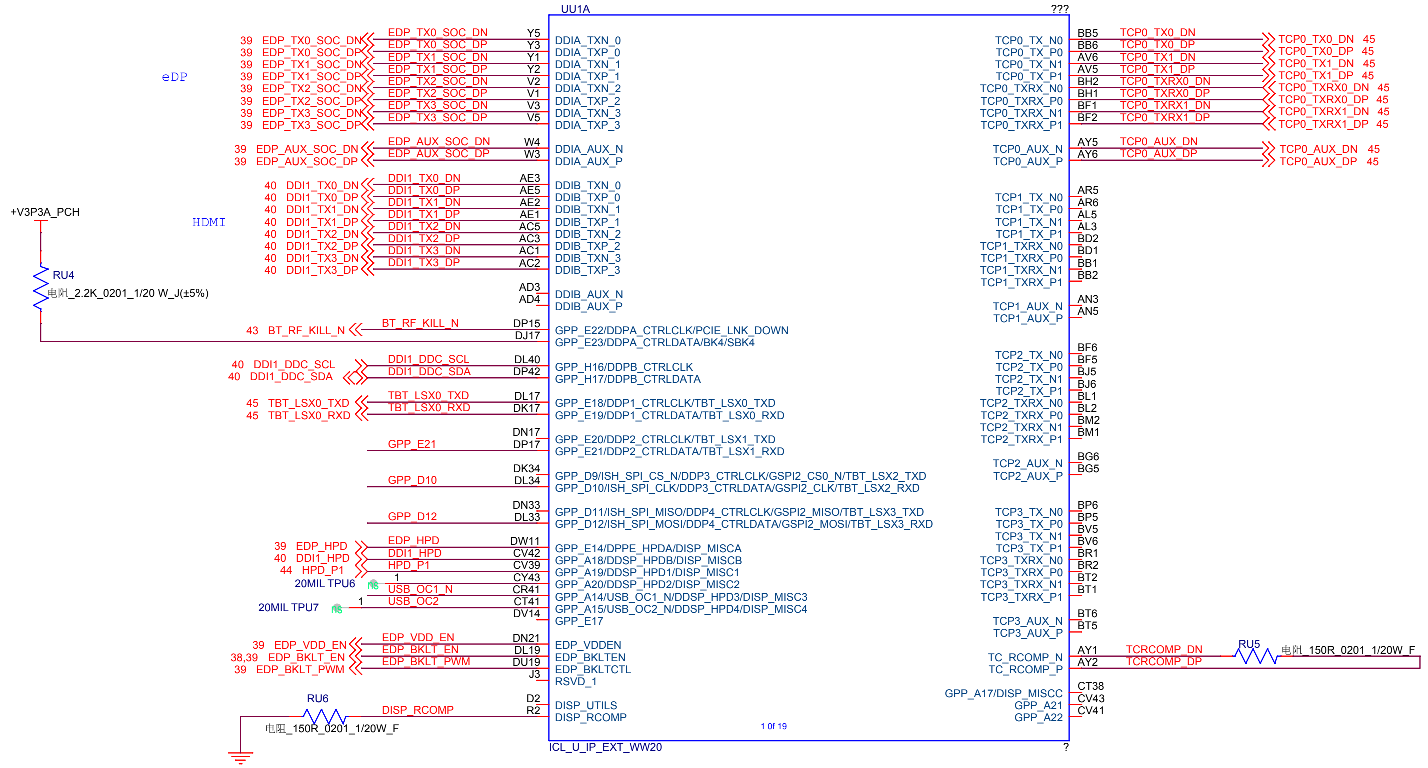
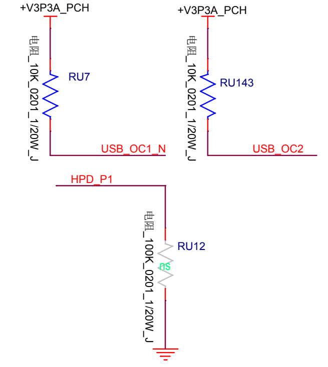
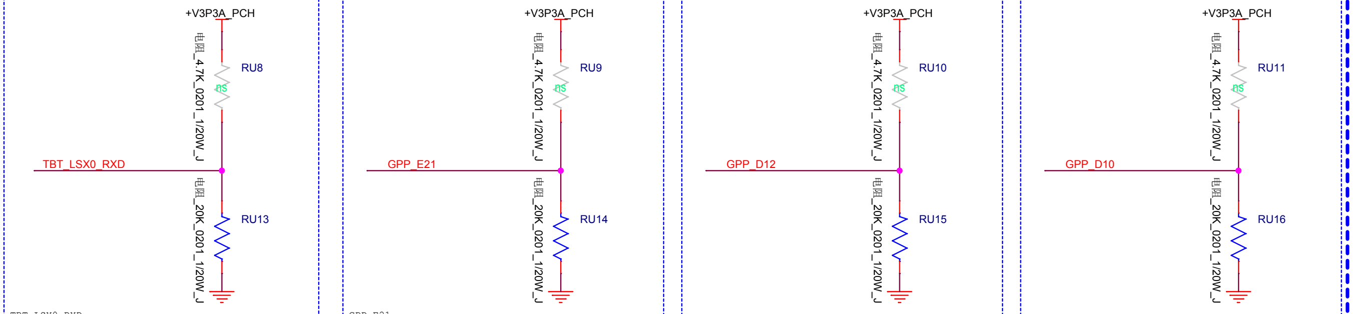




PCH STRAP---VCCIO CONFIGURATION



```
TBT_LSX0_RXD
0: DDP1 I2C / TBT LSx #0 / BSSB_LS #0 pins at 1.8V
1: DDP1 I2C / TBT LSx #0 / BSSB_LS #0 pins at 3.3V
```

```
GPP_E21
0 = DDP1 I2C / TBT LSx #0 / BSSB_LS #0 pins at 1.8V
1 = DDP1 I2C / TBT LSx #0 / BSSB_LS #0 pins at 3.3V
Internal 20K PD
```

```
GPP_D12
0: DDP4 I2C/TBT LSX #3/BSSB_LS #3 pins at 1.8V
```

```
GPP_D10
0: DDP3 I2C/TBT LSX #2/BSSB_LS #2 pins at 1.8V
```

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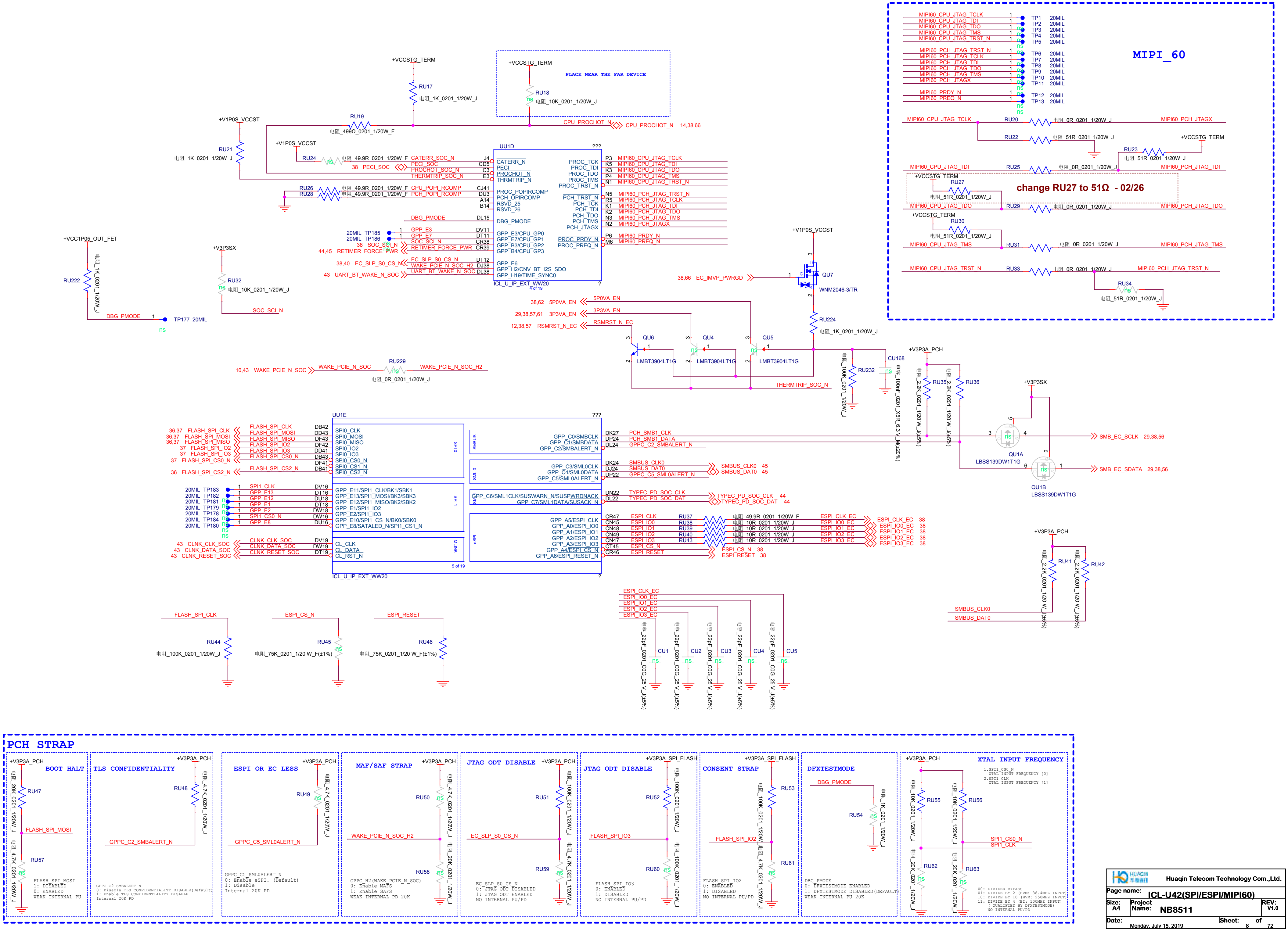

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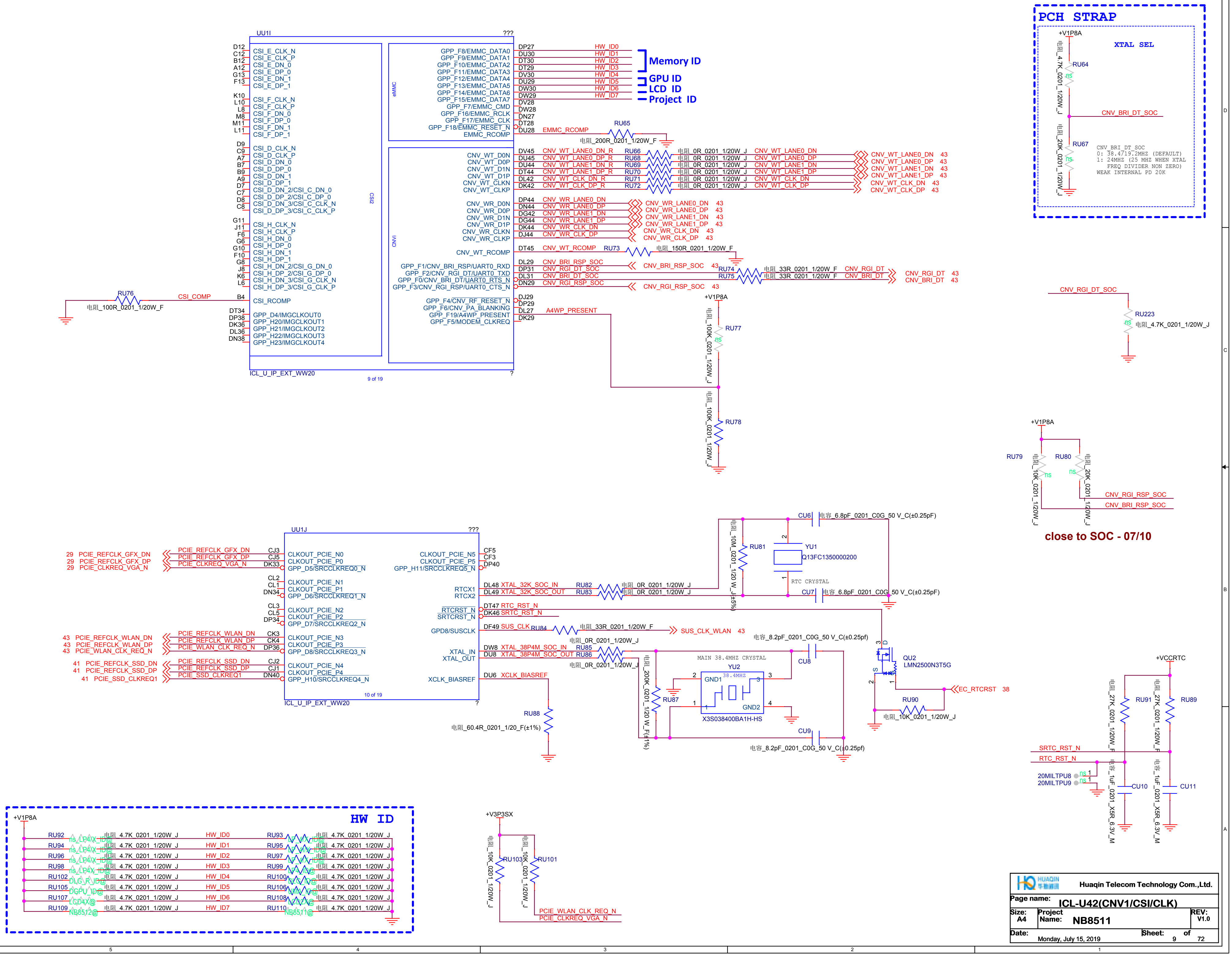

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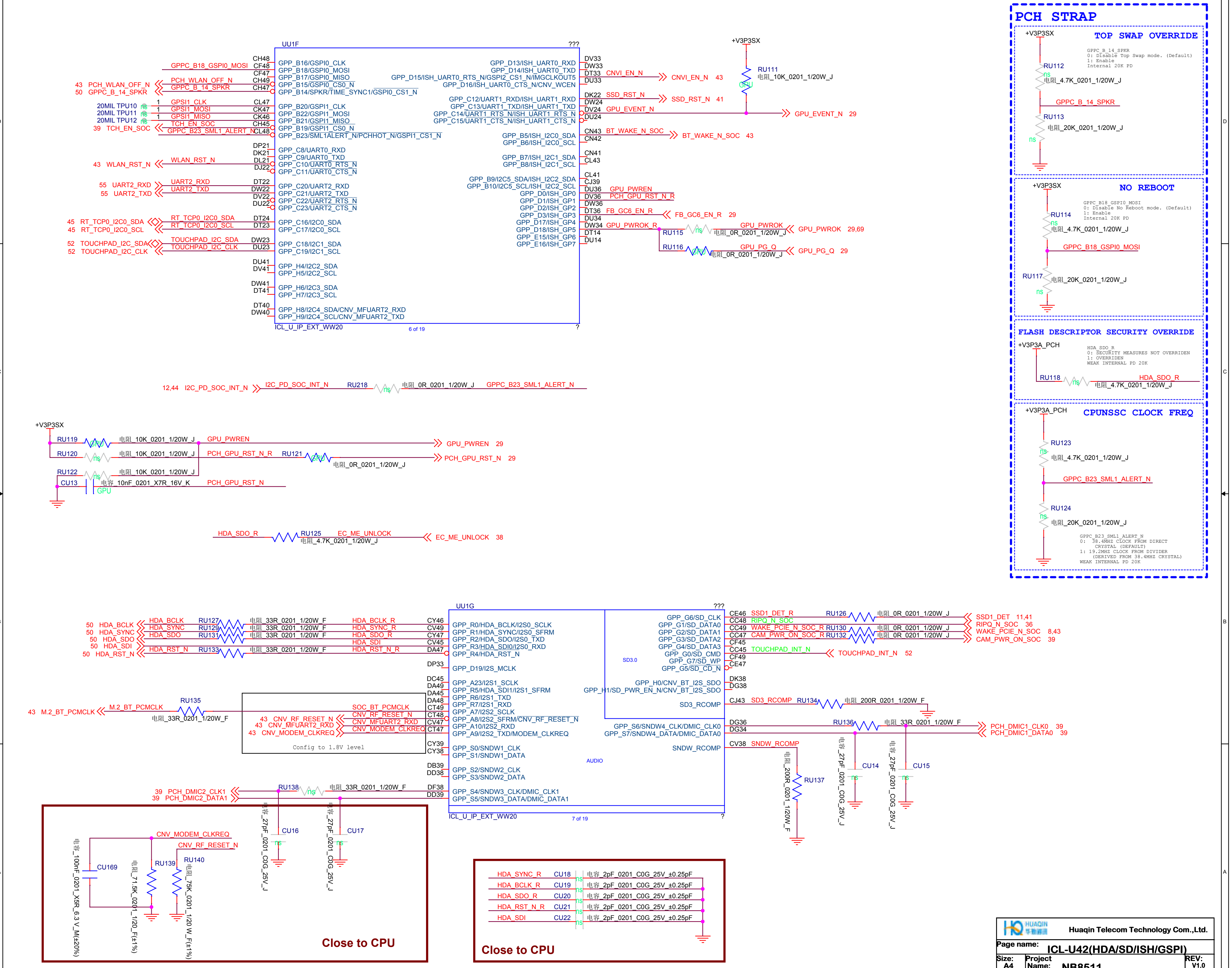

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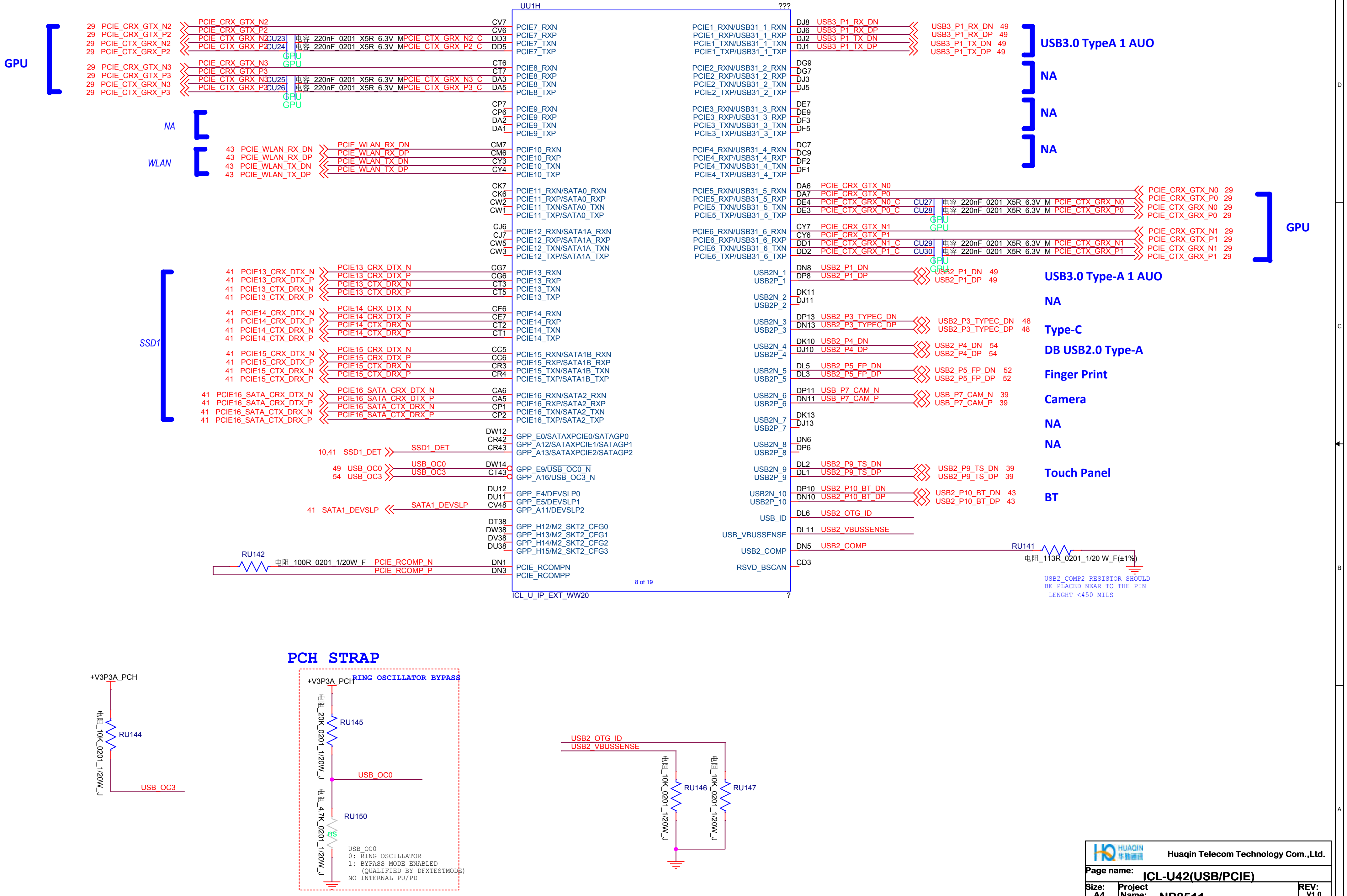

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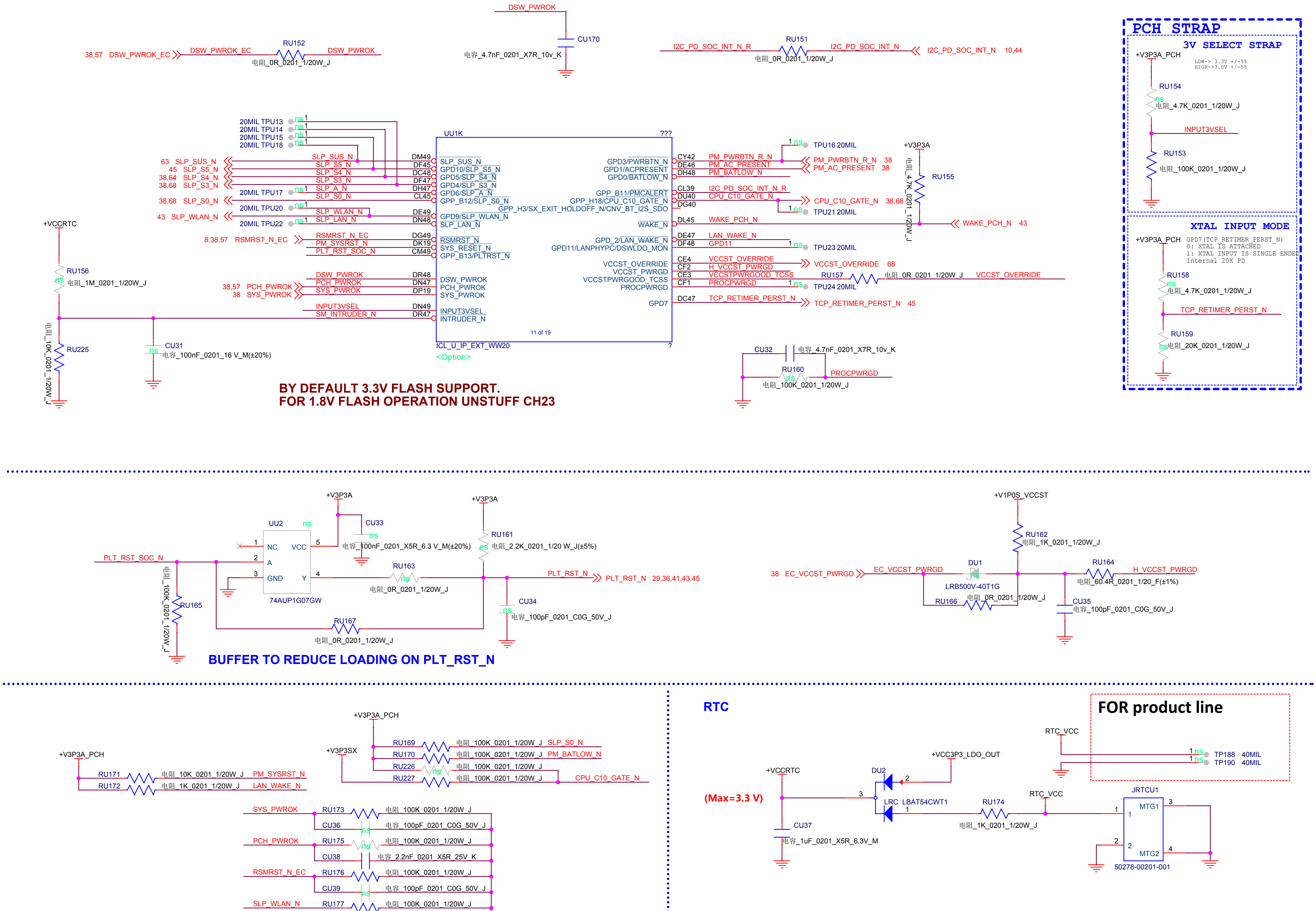

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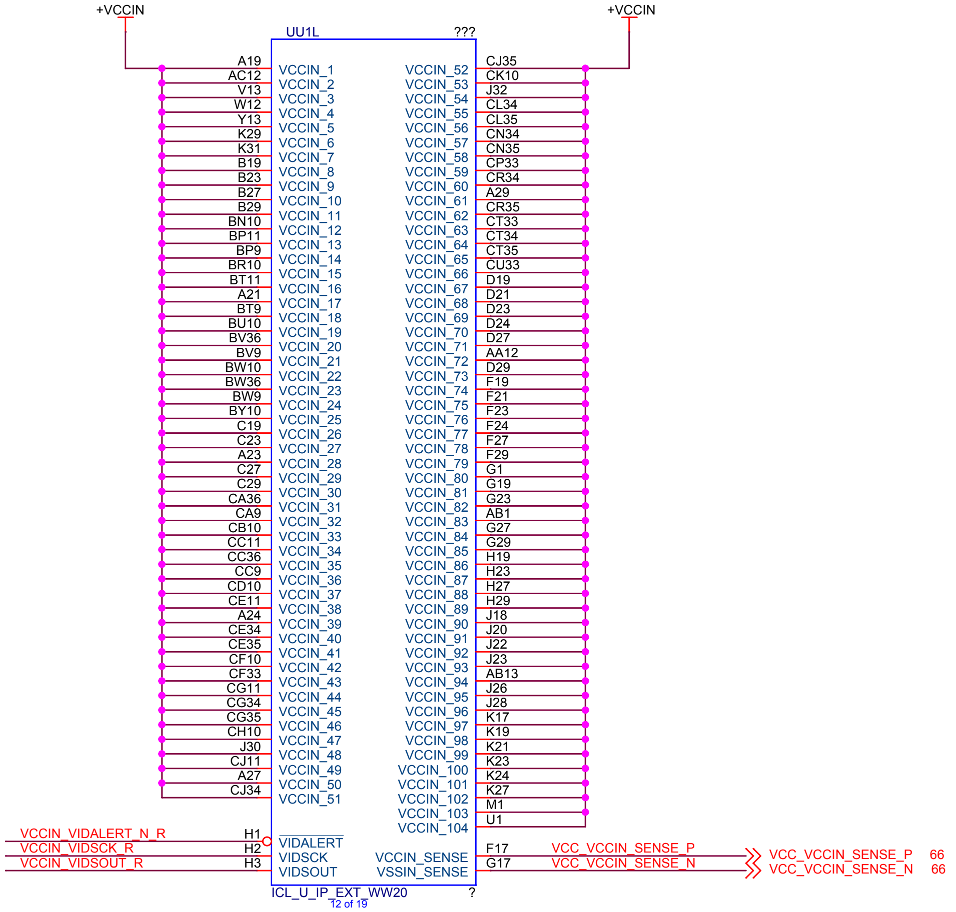
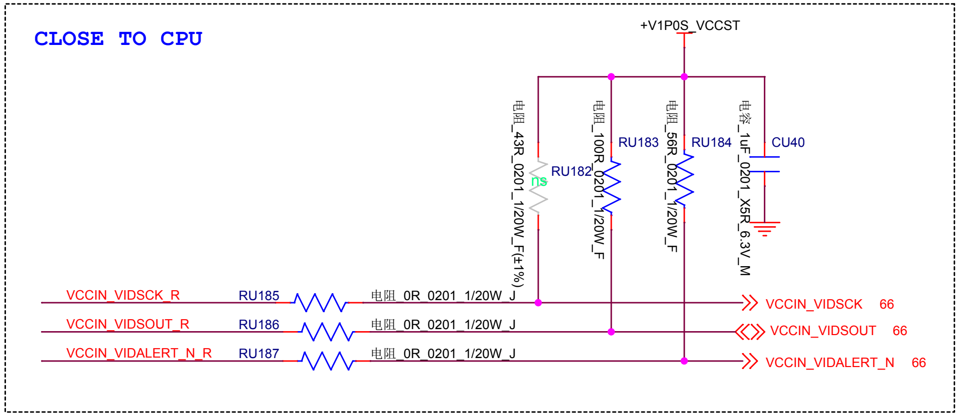
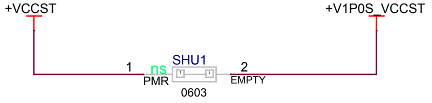


CLOSE TO CPU





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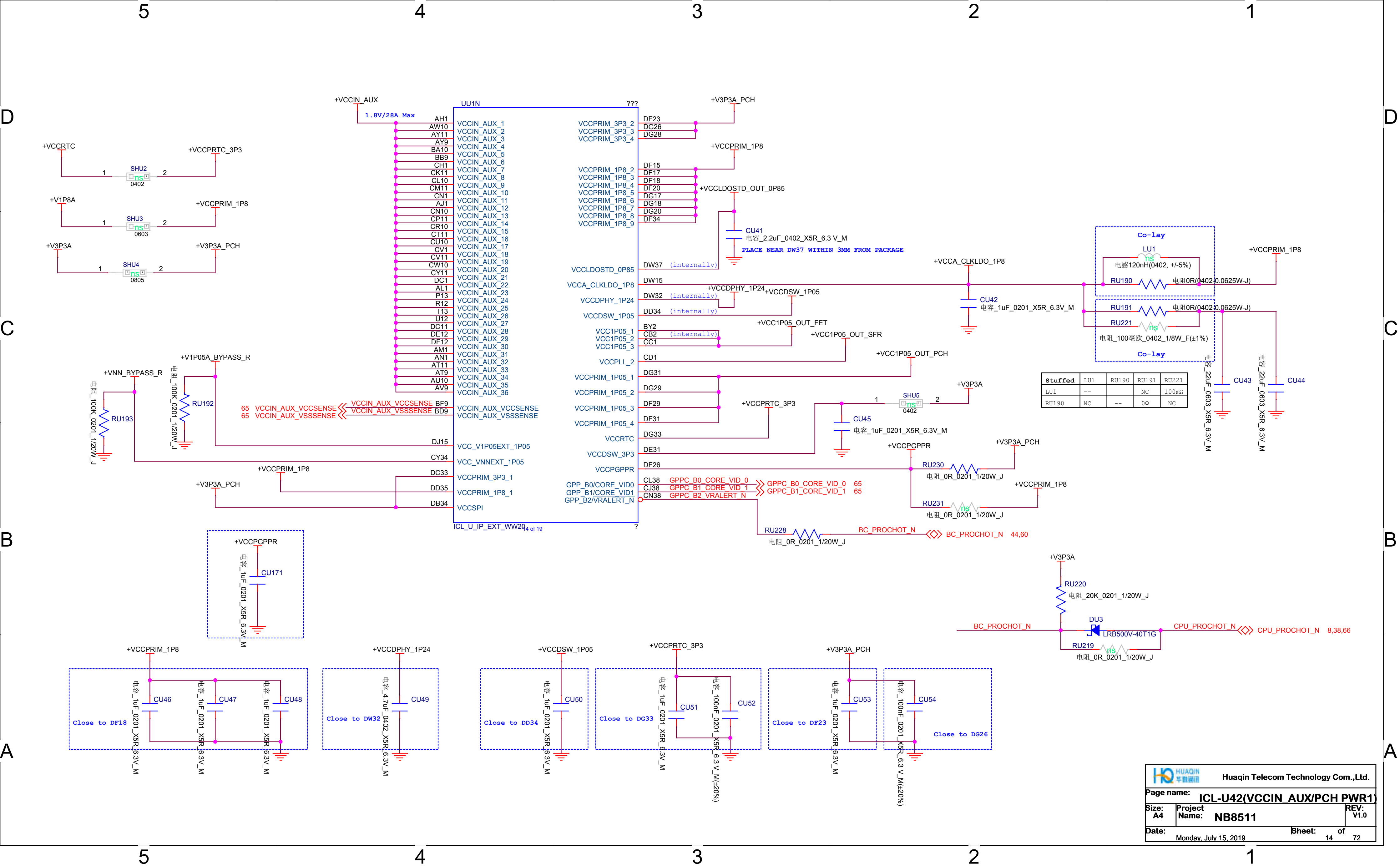

Stuffed	LU1	RU190	RU191	RU221
LU1	--		NC	100mΩ
RU190	NC	--	0Ω	NC

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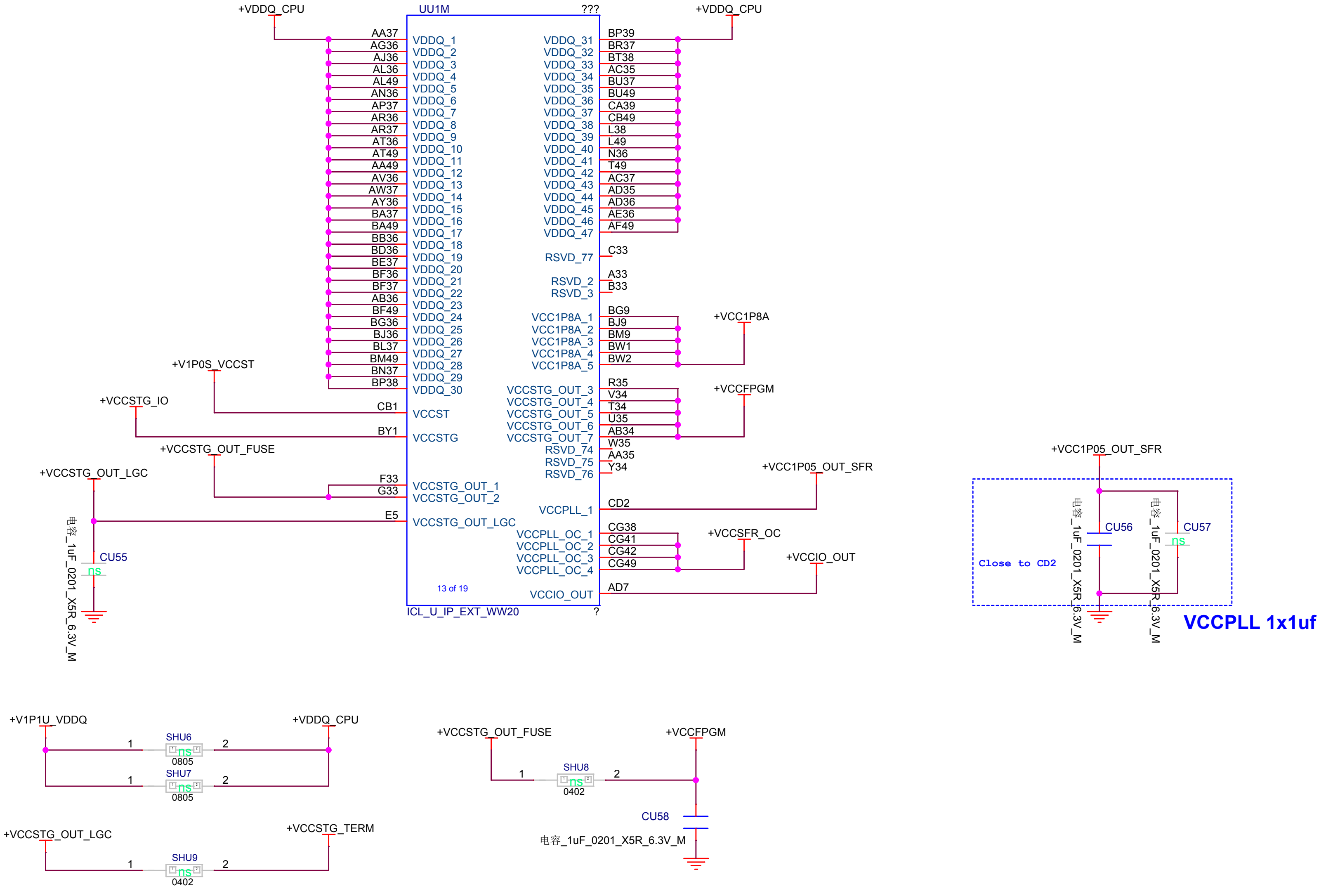

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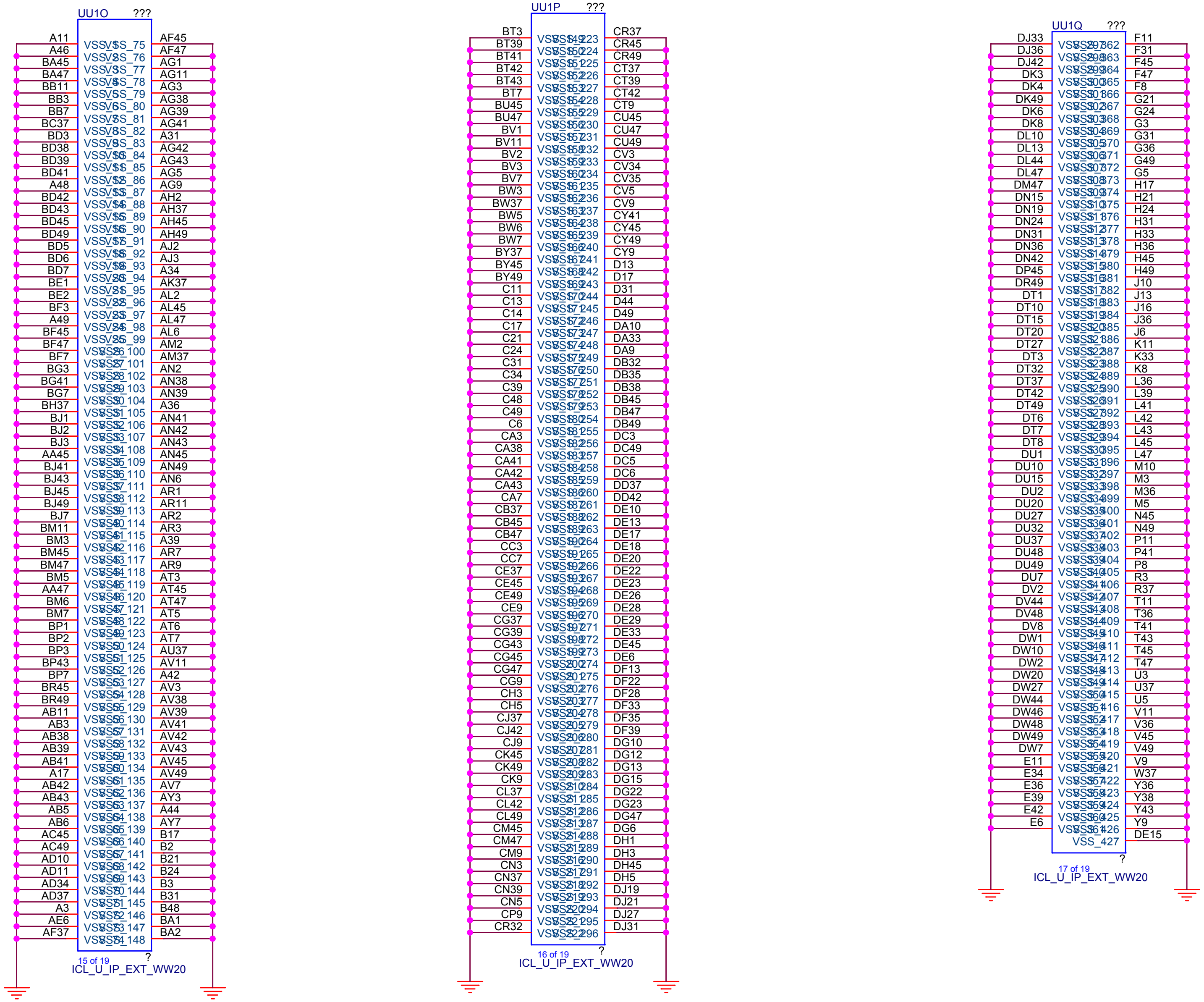

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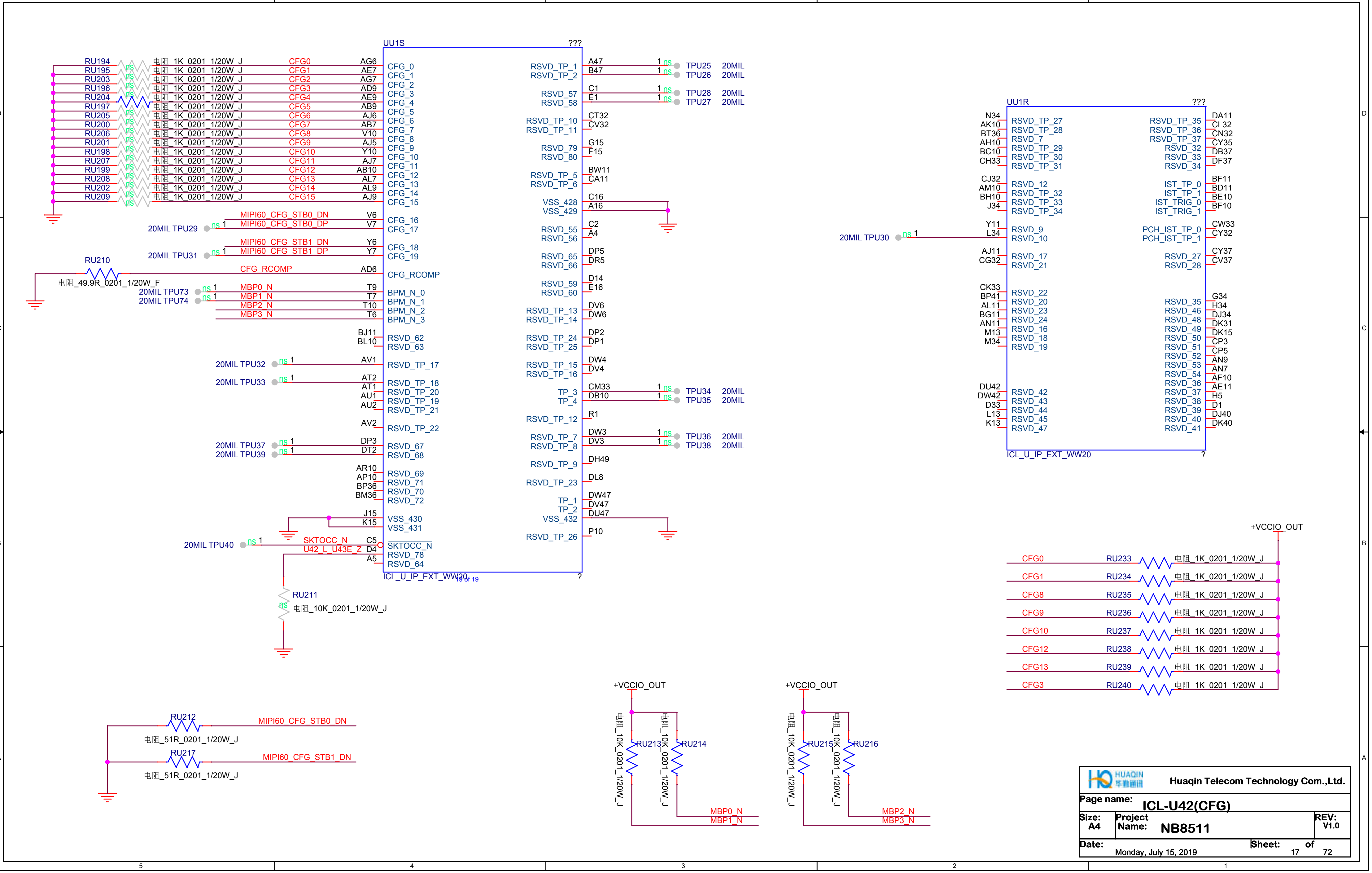

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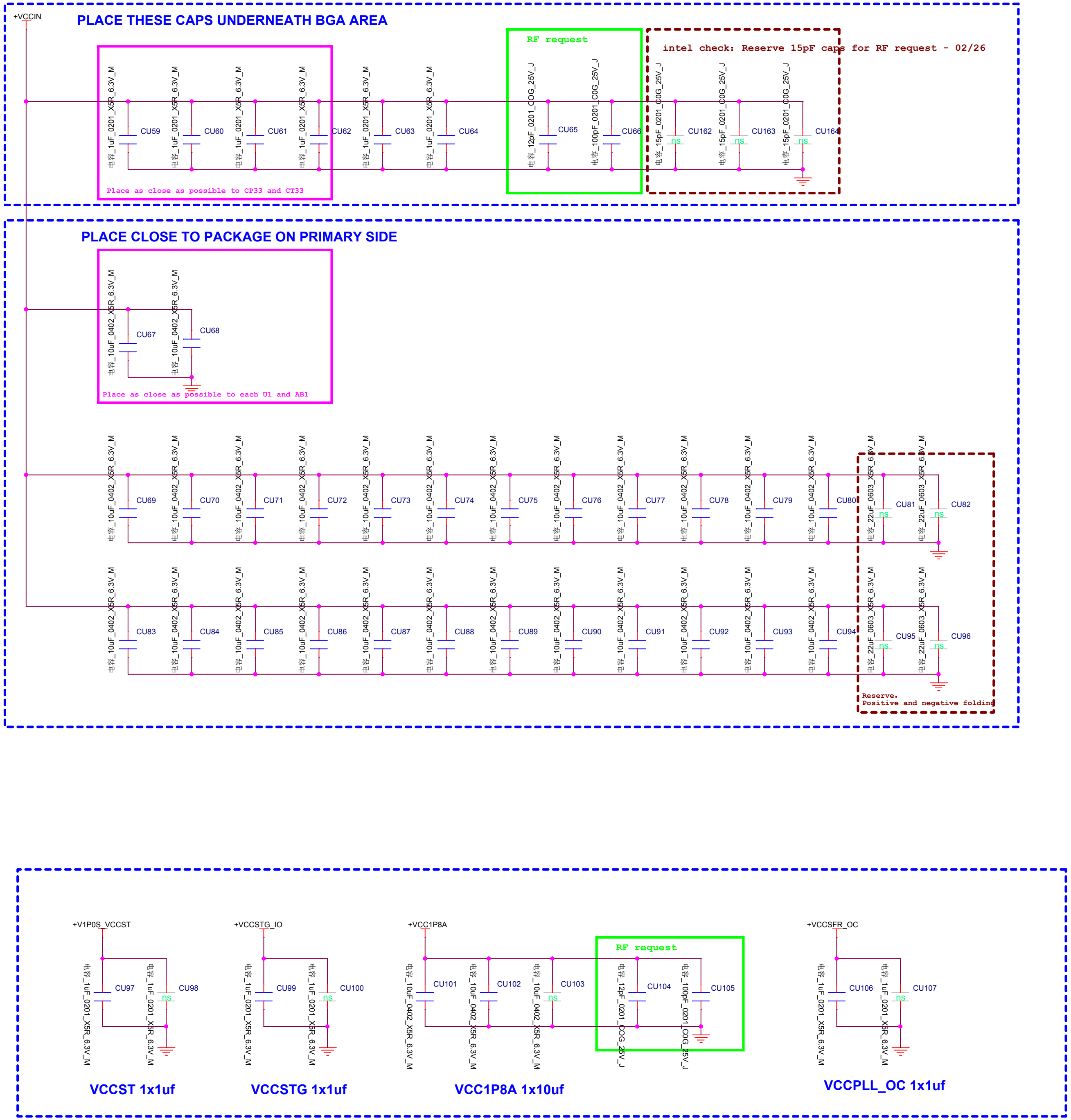

+VCCIN

PDG:4 x 1uF
2 x 10uF
10x 22uF
3x 47uF

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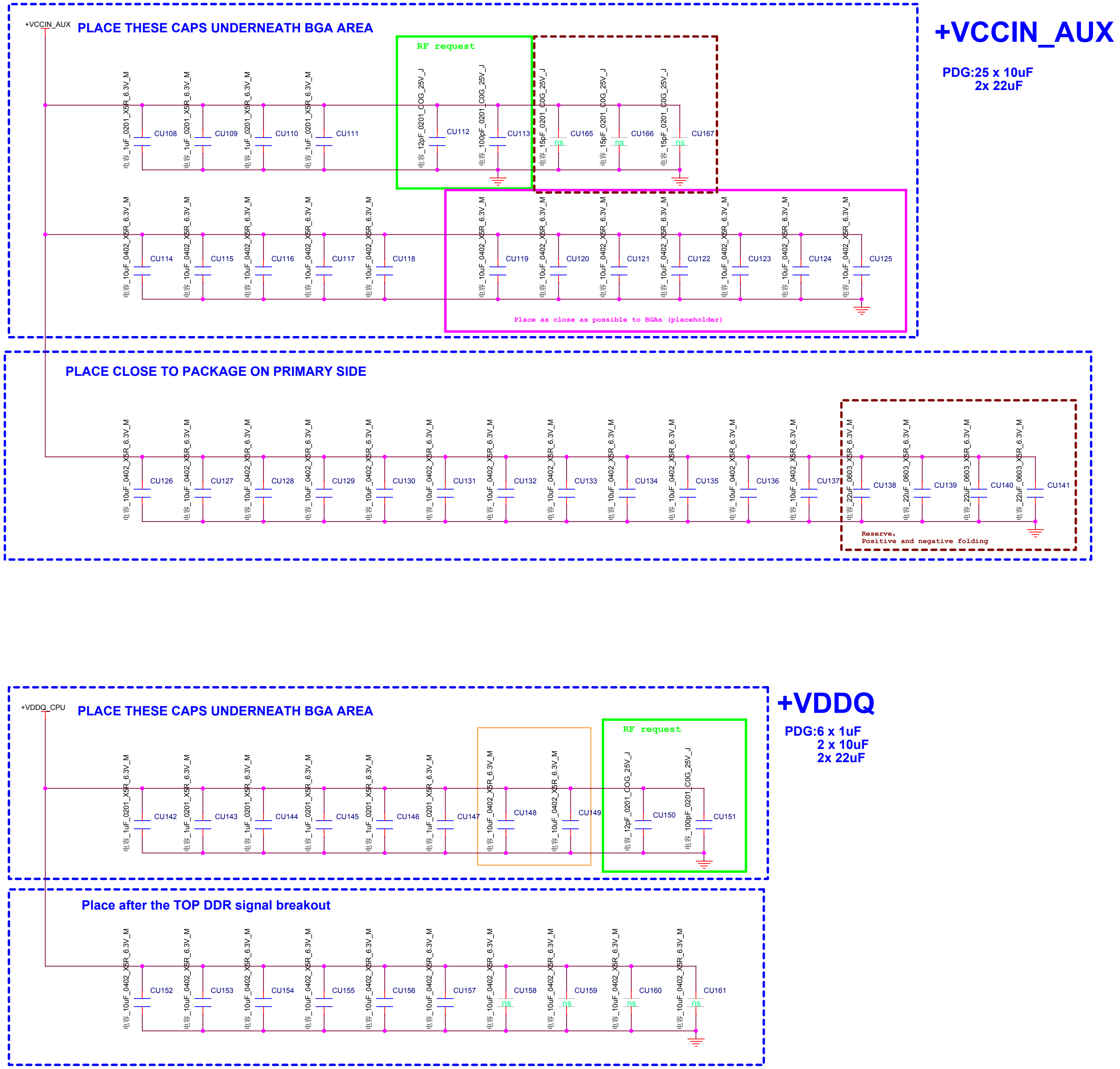

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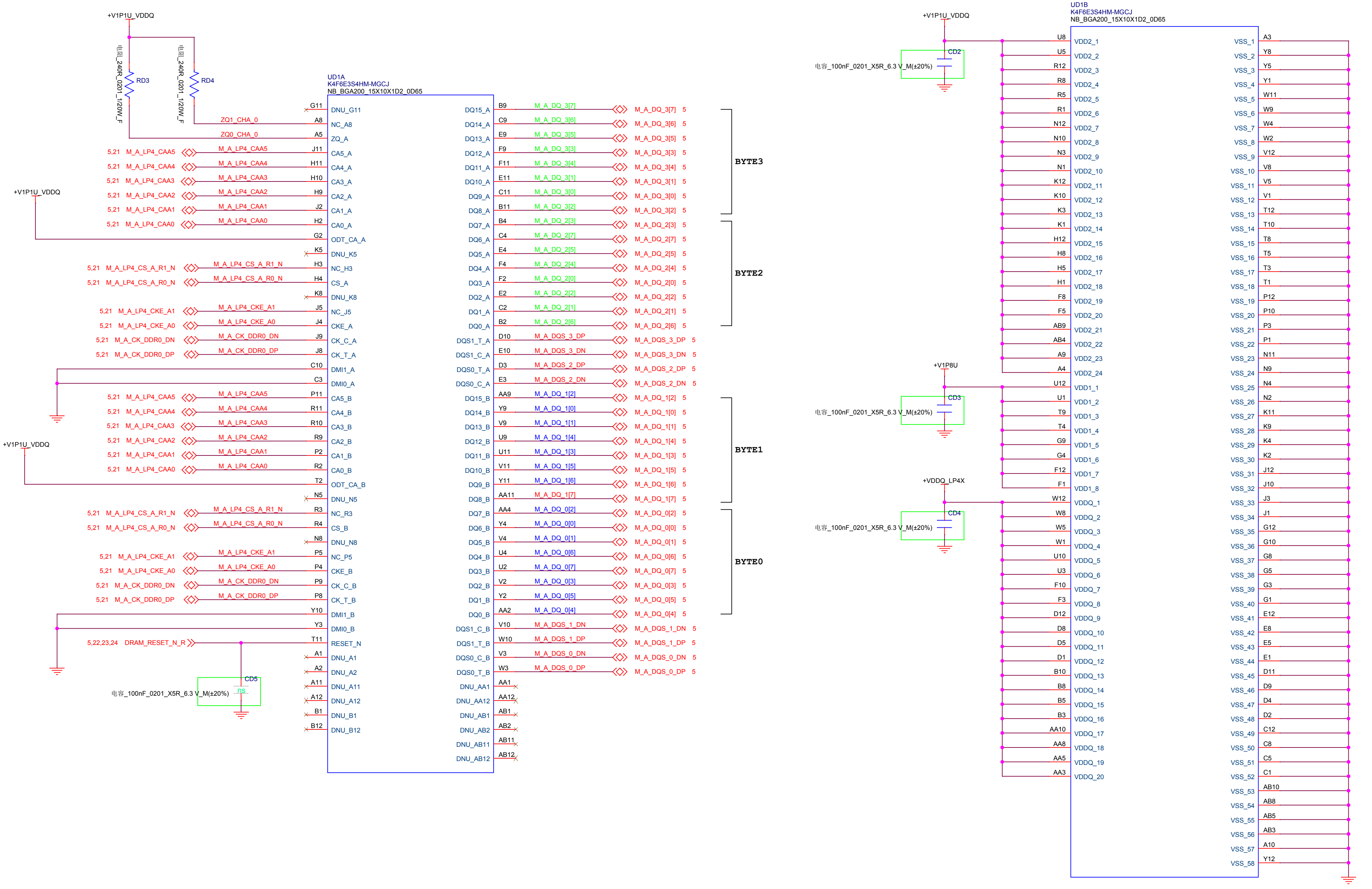
CHA-1



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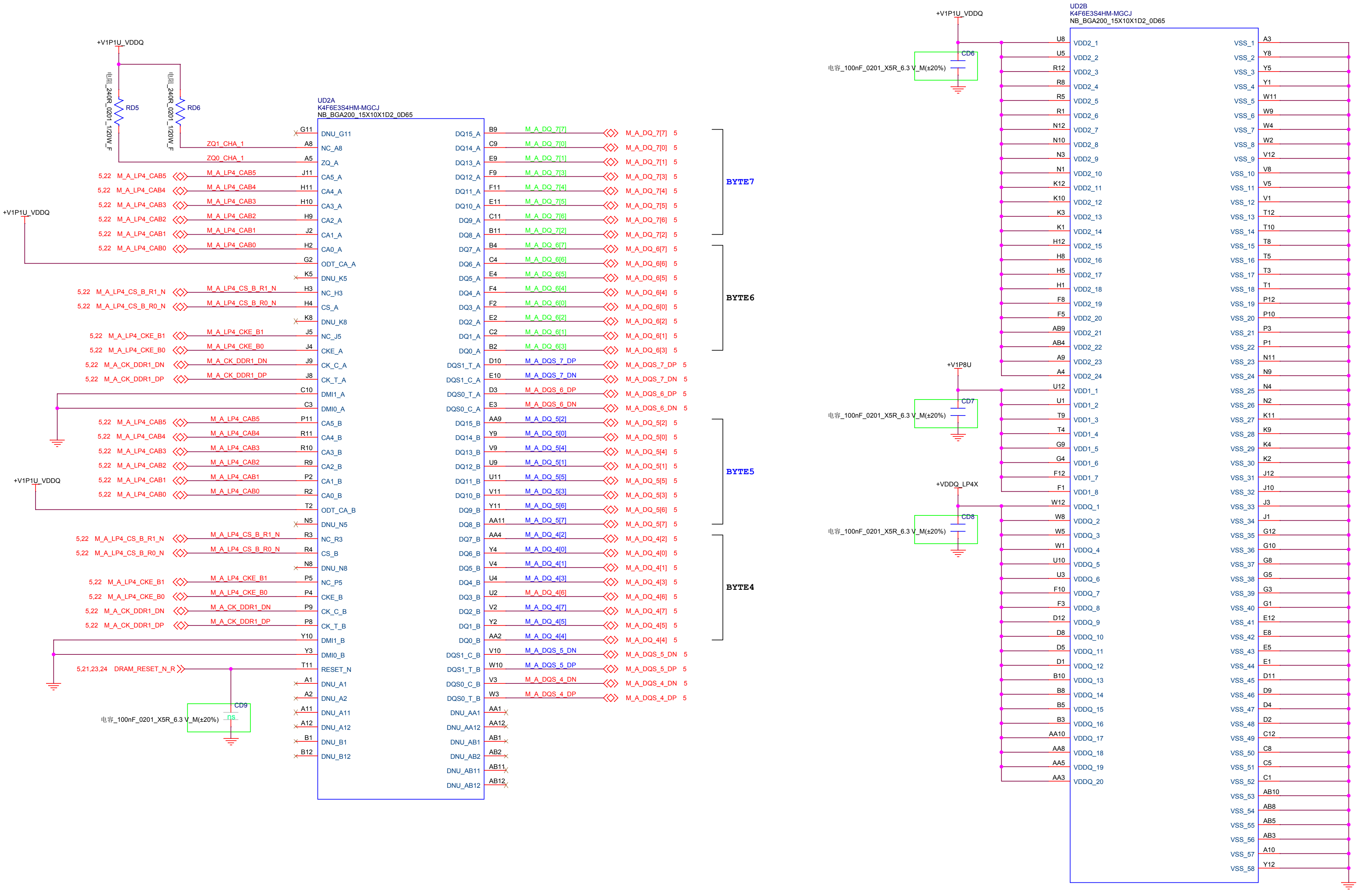
CHA-2



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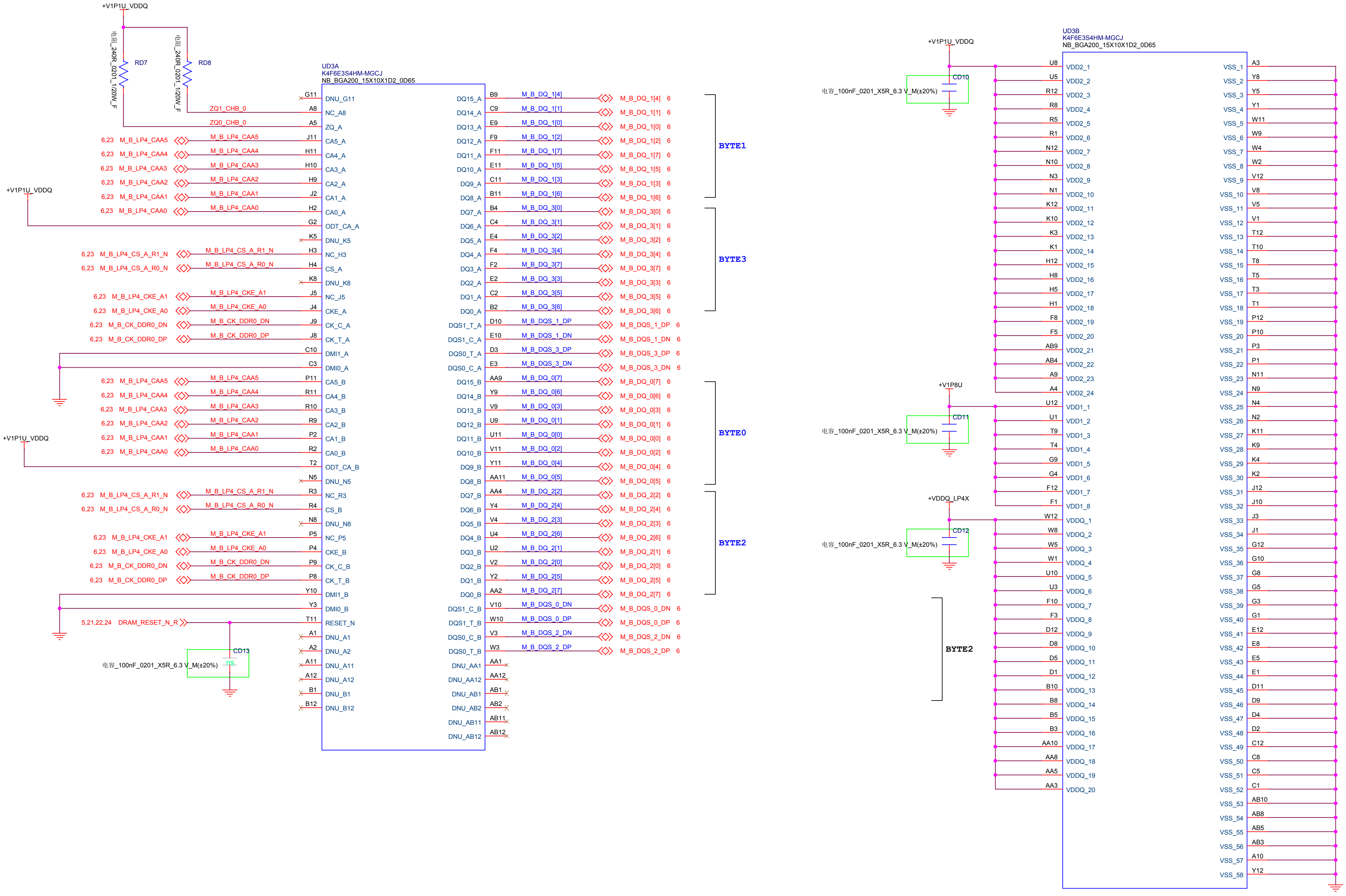

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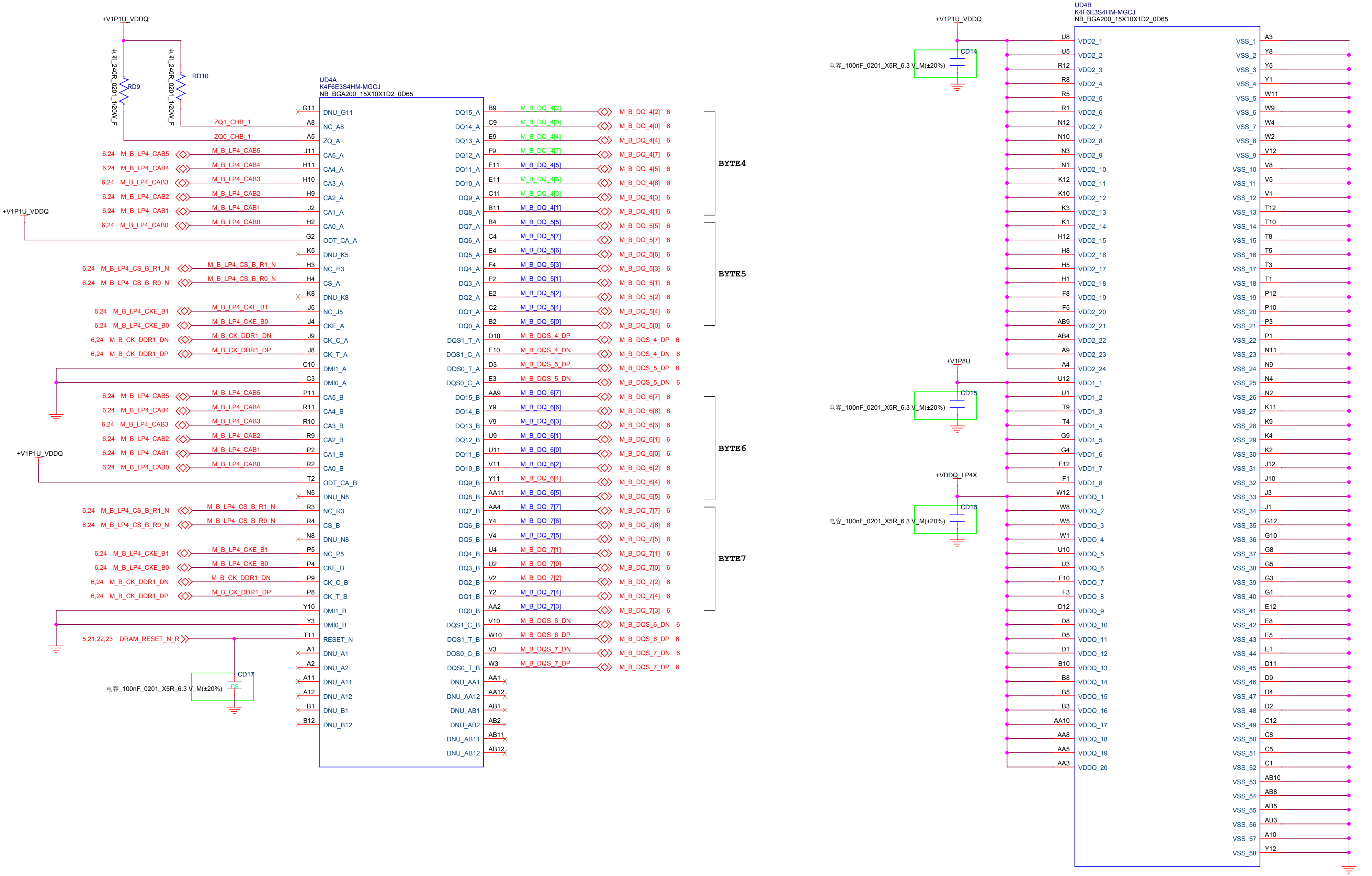
CHB-2



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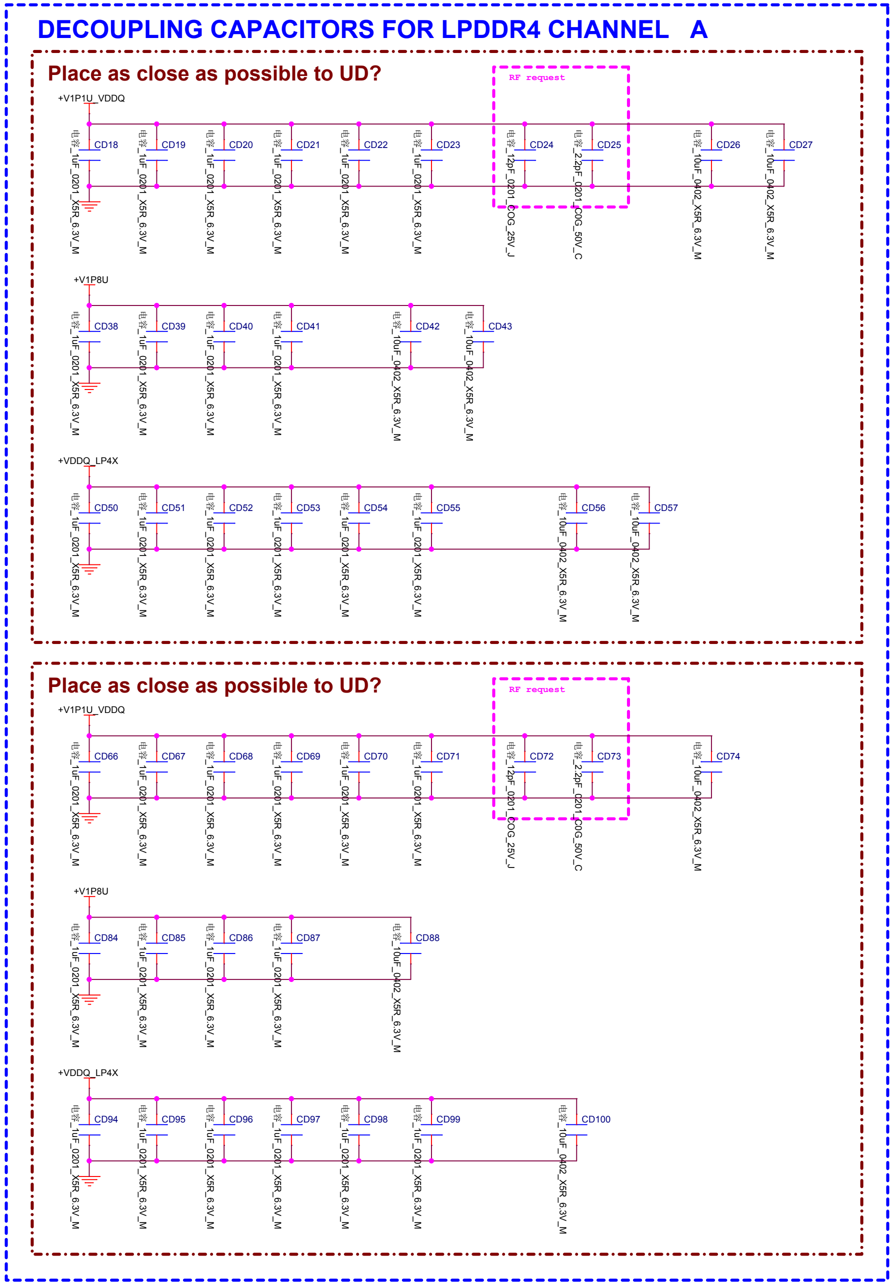

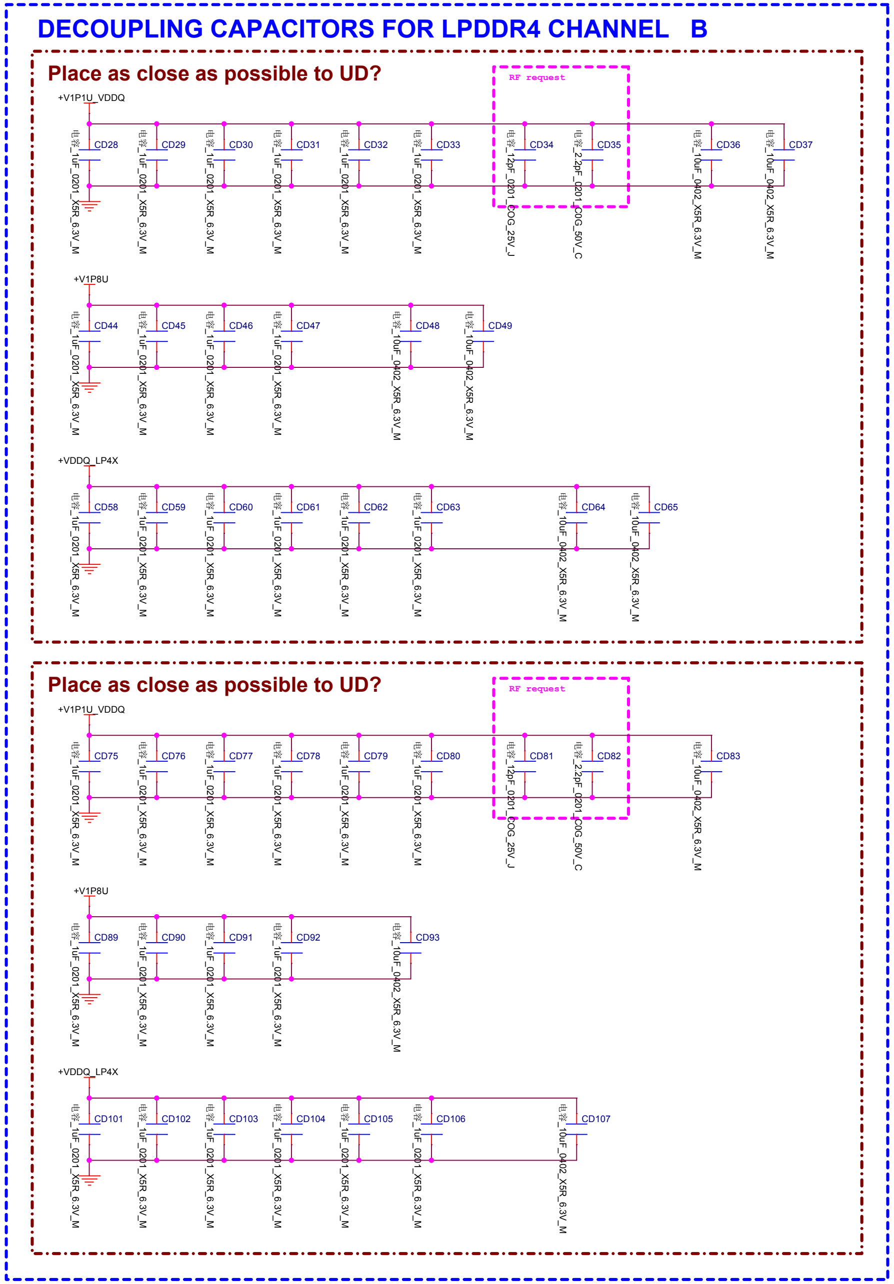

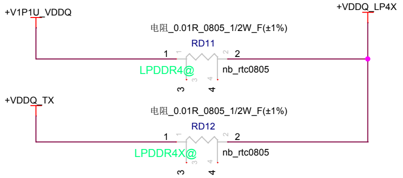

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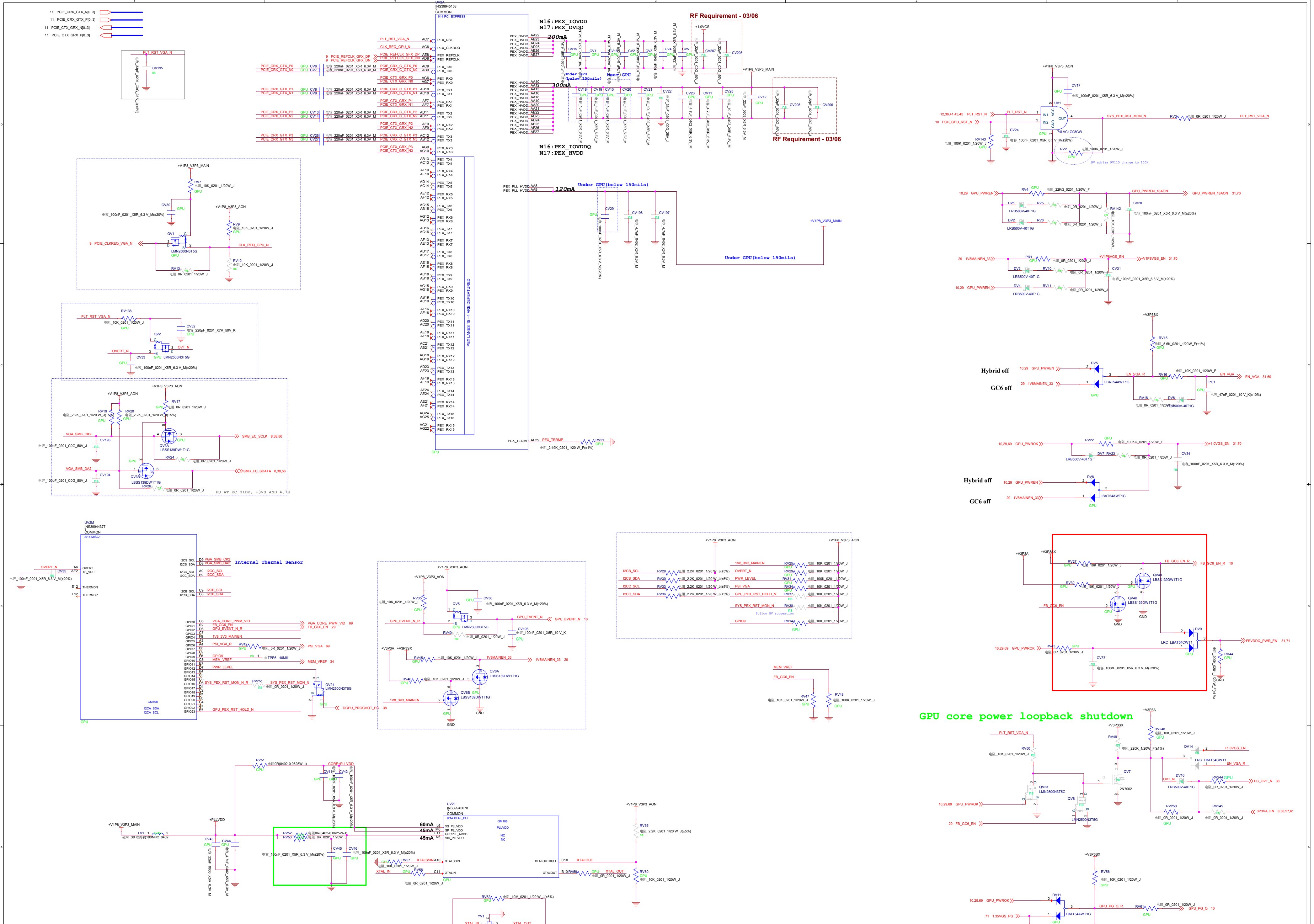

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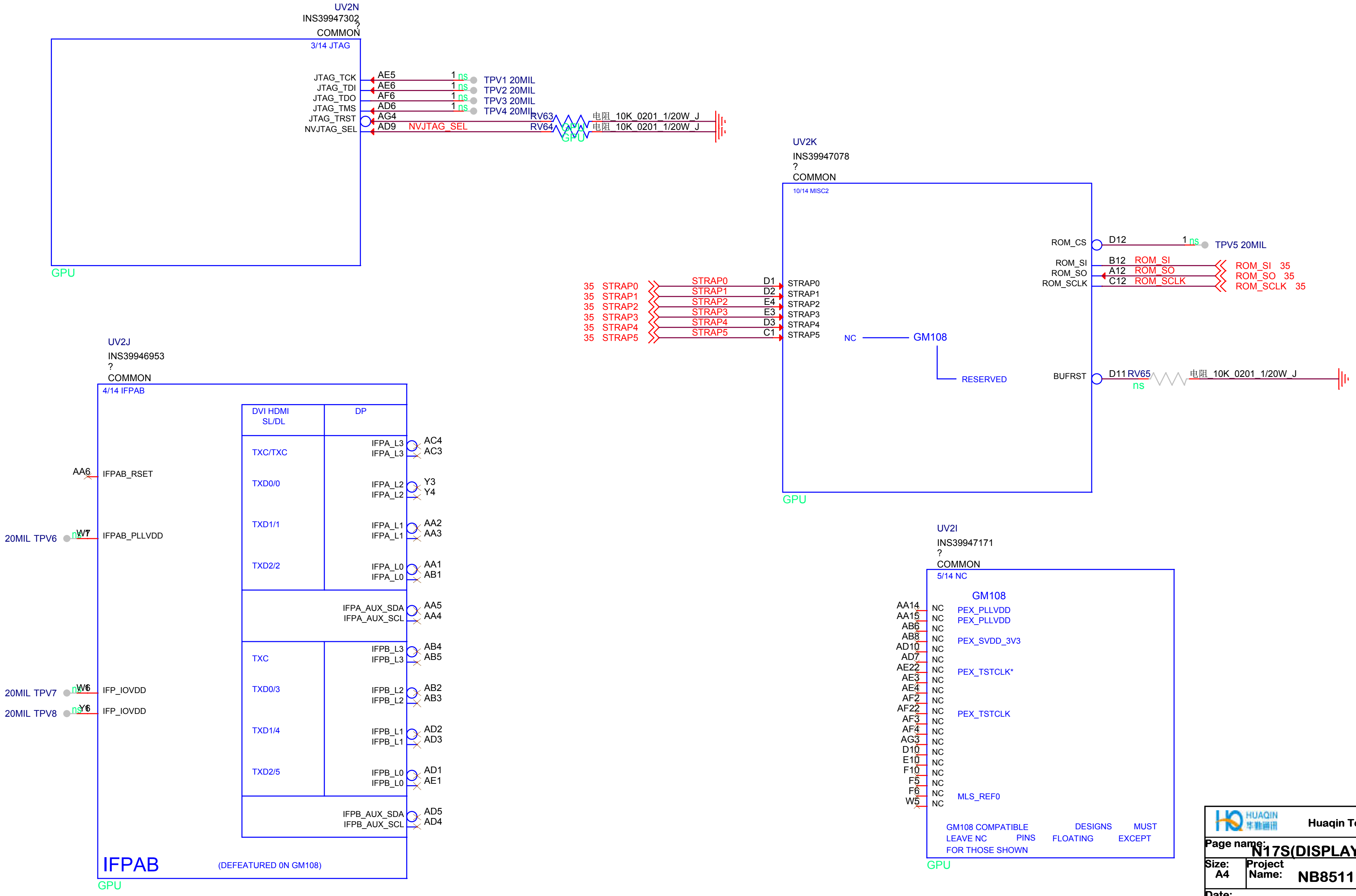

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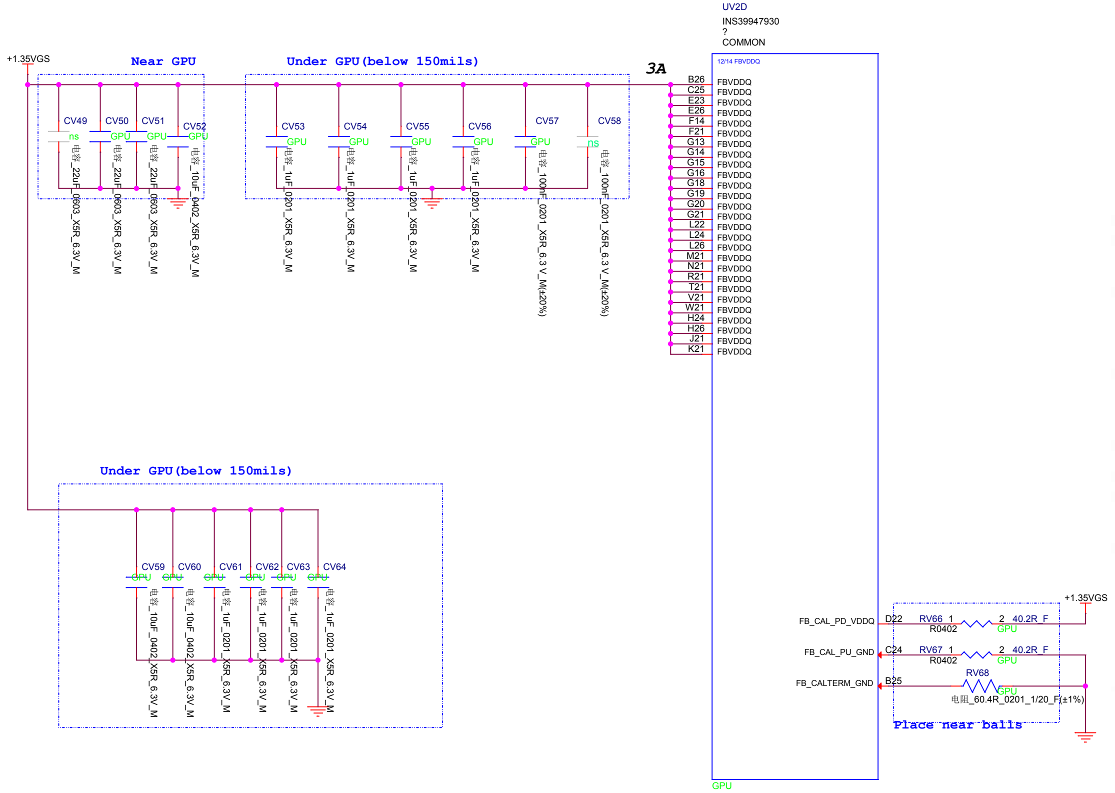


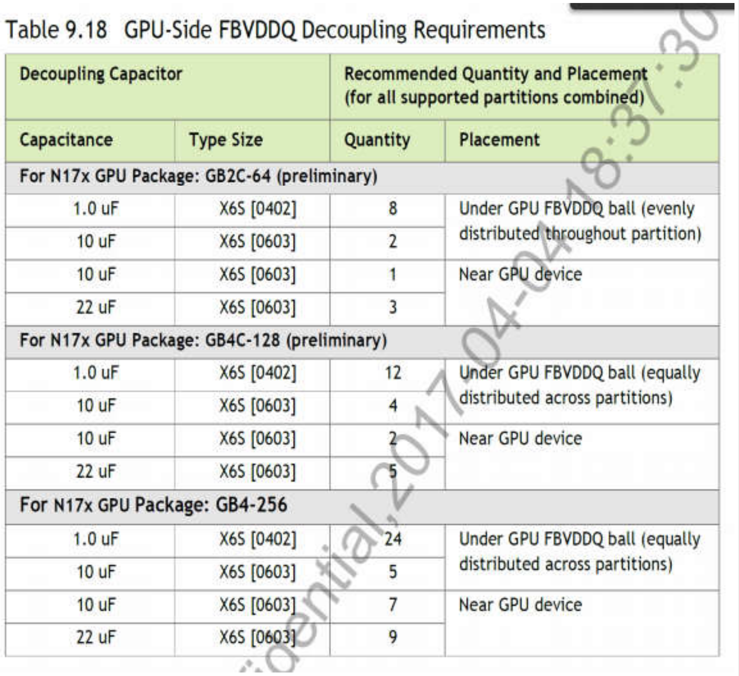
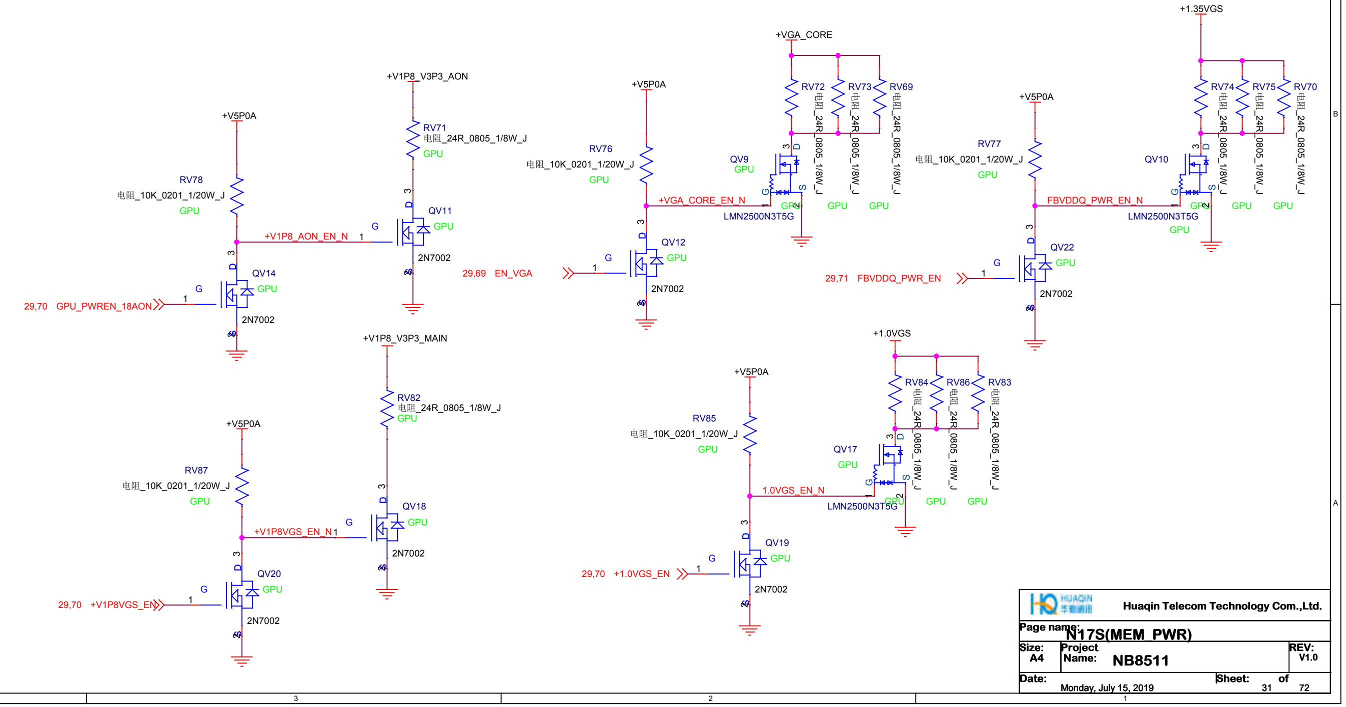


Table 9.18 GPU-Side FBVDDQ Decoupling Requirements

Decoupling Capacitor		Recommended Quantity and Placement (for all supported partitions combined)	
Capacitance	Type Size	Quantity	Placement
For N17x GPU Package: GB2C-64 (preliminary)			
1.0 uF	X6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
10 uF	X6S [0603]	2	
10 uF	X6S [0603]	1	Near GPU device
22 uF	X6S [0603]	3	
For N17x GPU Package: GB4C-128 (preliminary)			
1.0 uF	X6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Near GPU device
22 uF	X6S [0603]	5	
For N17x GPU Package: GB4-256			
1.0 uF	X6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
10 uF	X6S [0603]	5	
10 uF	X6S [0603]	7	Near GPU device
22 uF	X6S [0603]	9	

+V1P8A TO +V1P8_AON

Move to Power Page 2018/06/07



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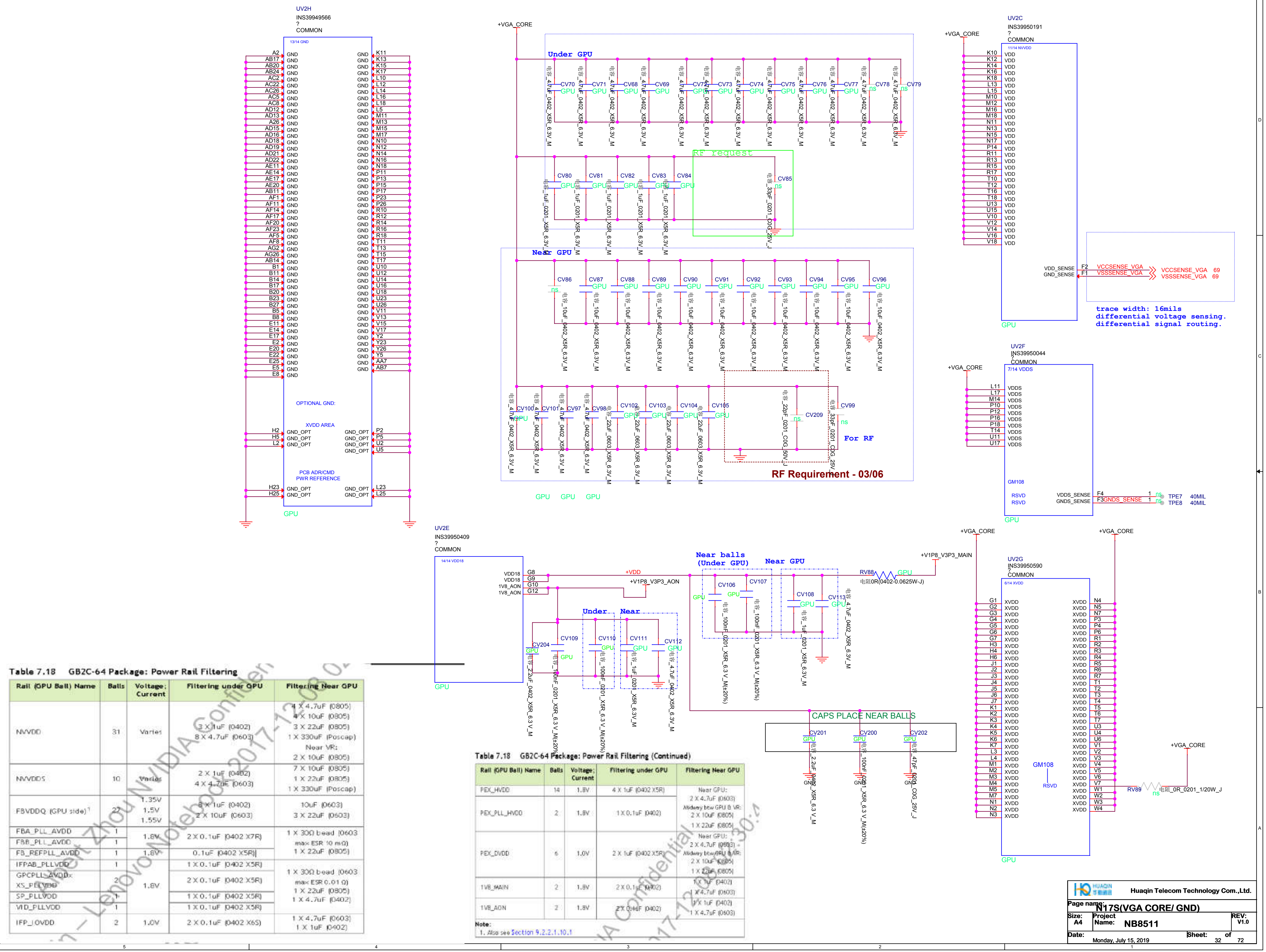

Table 7.18 GB2C-64 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies	3 X 1uF (0402) 8 X 4.7uF (0603)	4 X 4.7uF (0805) 4 X 10uF (0805) 3 X 22uF (0805) 1 X 330uF (Poscap) Near VR: 2 X 10uF (0805)
NVVDDS	10	Varies	2 X 1uF (0402) 4 X 4.7uF (0603)	7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Poscap)
FBVDDQ (GPU side)[1]	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 30Ω bead (0603 max ESR 10 mΩ) 1 X 22uF (0805)
FBB_PLL_AVDD	1			
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)	
IFPAB_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 30Ω bead (0603 max ESR 0.01 Ω) 1 X 22uF (0805) 1 X 4.7uF (0402)
GPCPLL_AVDDx XS_PLLVDD	2		2 X 0.1uF (0402 X5R)	
SP_PLLVDD	1		1 X 0.1uF (0402 X5R)	
VID_PLLVDD	1		1 X 0.1uF (0402 X5R)	
IFP_IOVDD	2	1.0V	2 X 0.1uF (0402 X6S)	1 X 4.7uF (0603) 1 X 1uF (0402)

Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	2	1.8V	1 X 0.1uF (0402)	
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
1V8_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)
1V8_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

Note:
1. Also see Section 9.2.2.1.10.1

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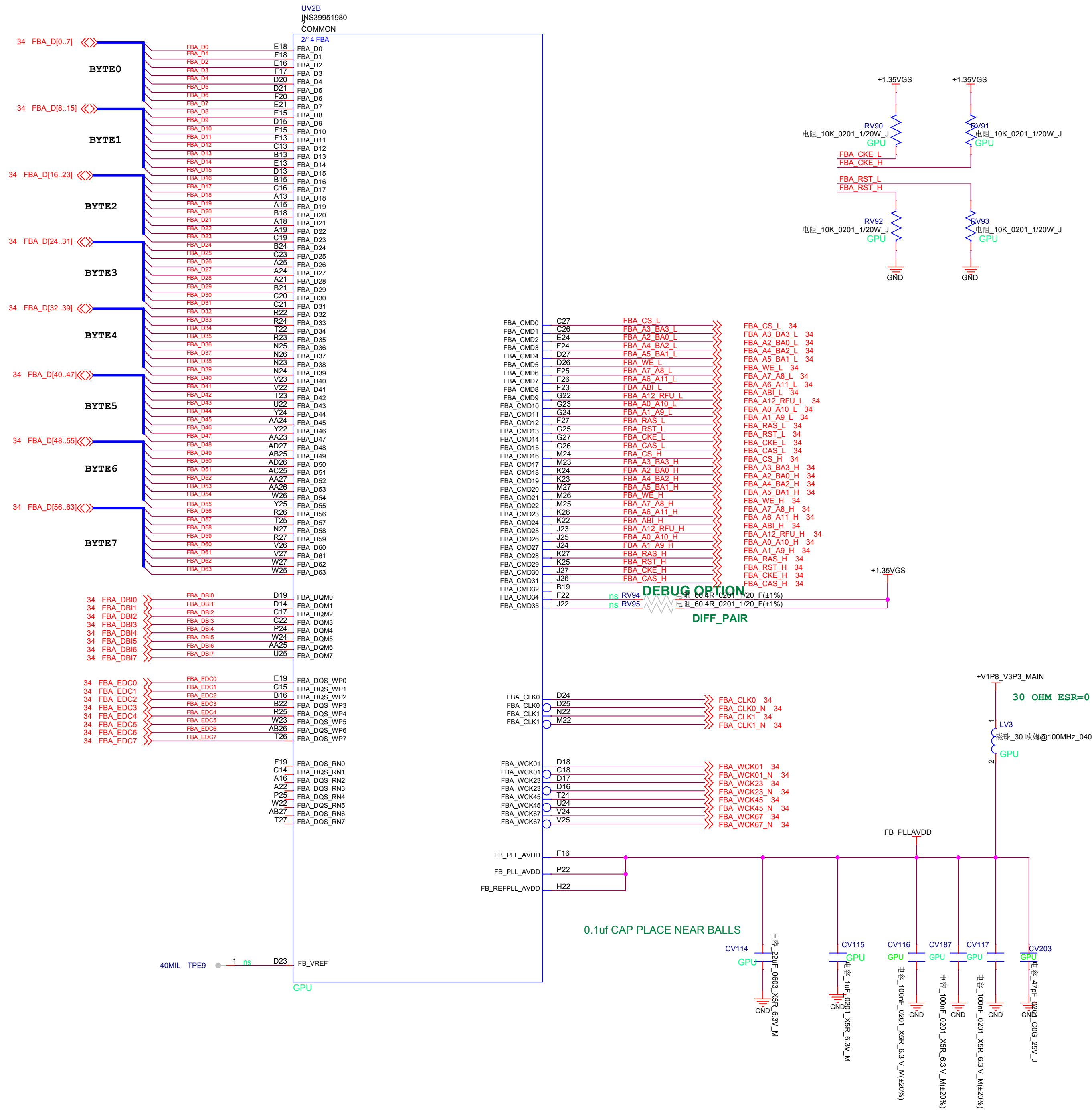

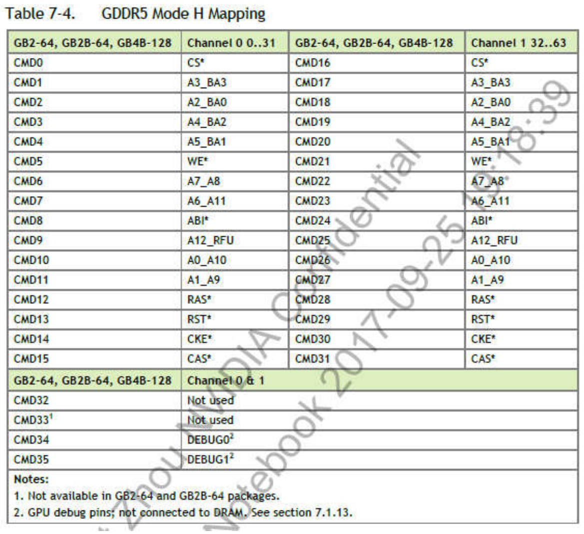

Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	**Channel 0 & 1**		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

Notes:

1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 7.1.13.

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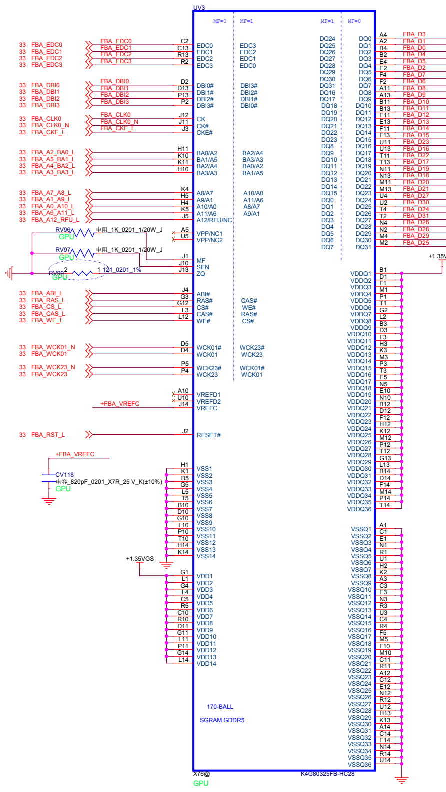
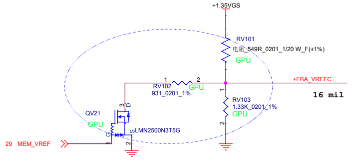
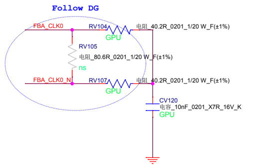
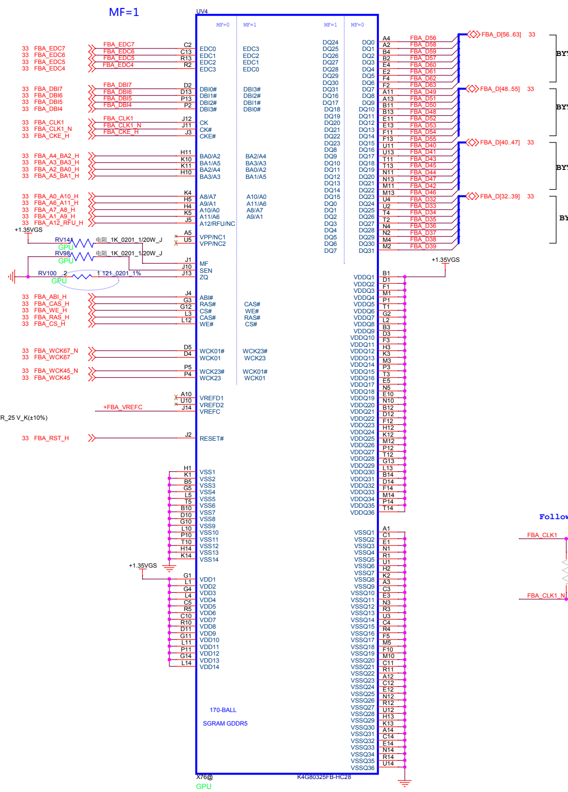
Memory - Lower 32 bits

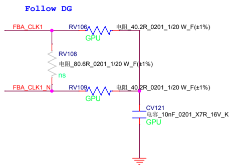


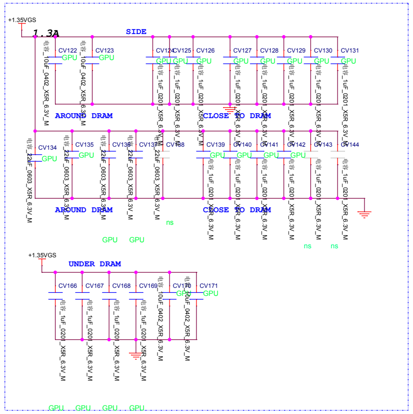




Memory - Upper 32 bits







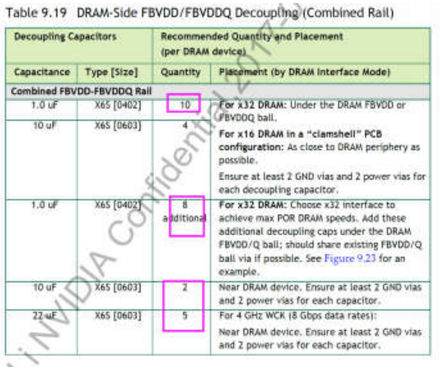
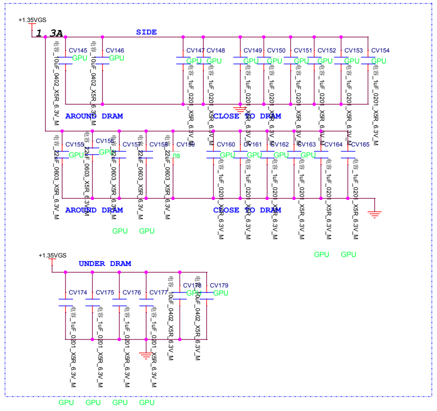
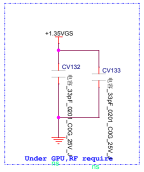


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	**Type [Size]**	**Quantity**	**Placement (by DRAM Interface Mode)**
Combined FBVDD-FBVDDQ Rail			
1.0 uF	X65 [0402]	10	**For x32 DRAM:** Under the DRAM FBVDD or FBVDDQ ball.
10 uF	X65 [0603]	4	**For x16 DRAM in a "clamshell" PCB configuration:** As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
1.0 uF	X65 [0402]	8 additional	**For x32 DRAM:** Choose x32 interface to achieve max POR DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X65 [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X65 [0603]	5	For 4 GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.





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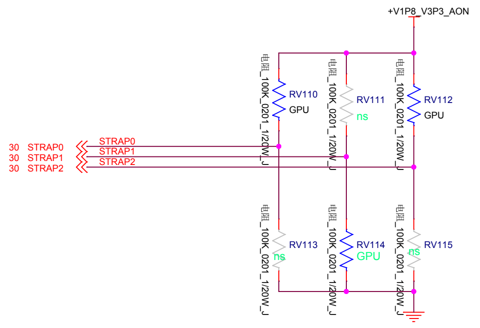

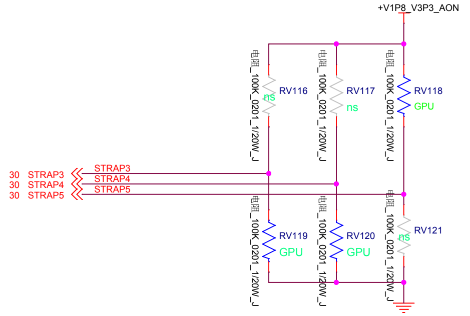

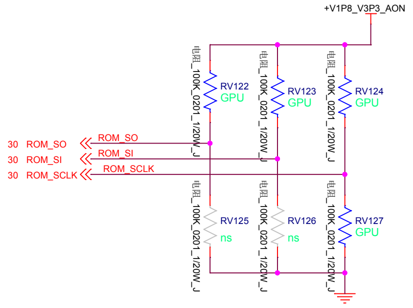

For N17

GPU	Vendor	Manufacturer	Strap	Strap2	Strap1	Strap0
N17S-G1	Samsung	K4G80325FB-HC28	0x0	L	L	L
	Micron	MT51J256M32HF-70:A	0x1	L	L	H
	Hynix	H5GC8H24MJR-ROC	0x2	L	H	L
	Micron	MT51J256M32HF-70:B	0x4	H	L	L
	Hynix	H5GC8H24AJR-ROC	0x5	H	L	H
N17S_G0/G2	Micron	MT51J256M32HF-80:B	0x9	L	M	L
	Hynix	H5GC8H24AJR-R2C	0xA	L	M	H

PN	MPN	STRAP	Vendor
HQ11121499000	K4G80325FB-HC28	0x00	Samsung
HQ11121497000	H5GQ8H24MJR-R4C	0x02	Hynix

Physical Strapping pin	Power Rail	RAM_CFG[3]	RAM_CFG[0x02]	RAM_CFG[1]	RAM_CFG[0x00]
STRAP0			L		L
STRAP1			H		L
STRAP2			L		L

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	M	Disable	Disable	Disable	Disable
ROM_SI	H				
ROM_SO	H				

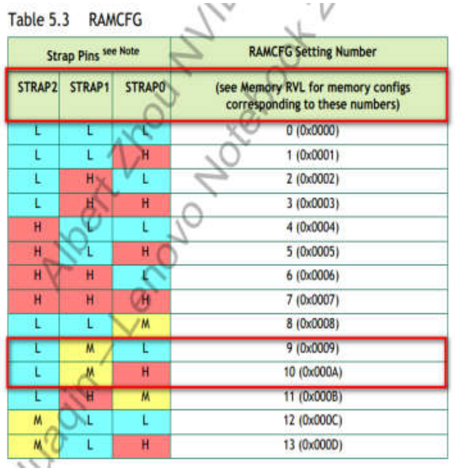

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

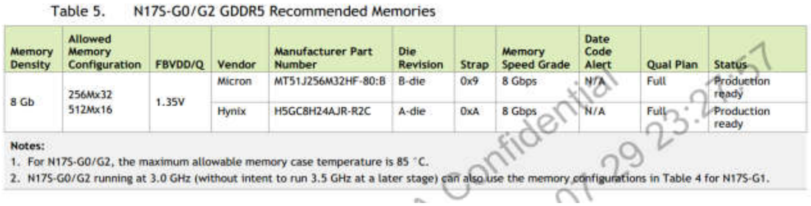

Table 5. N17S-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Notes:

1. For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
2. N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.

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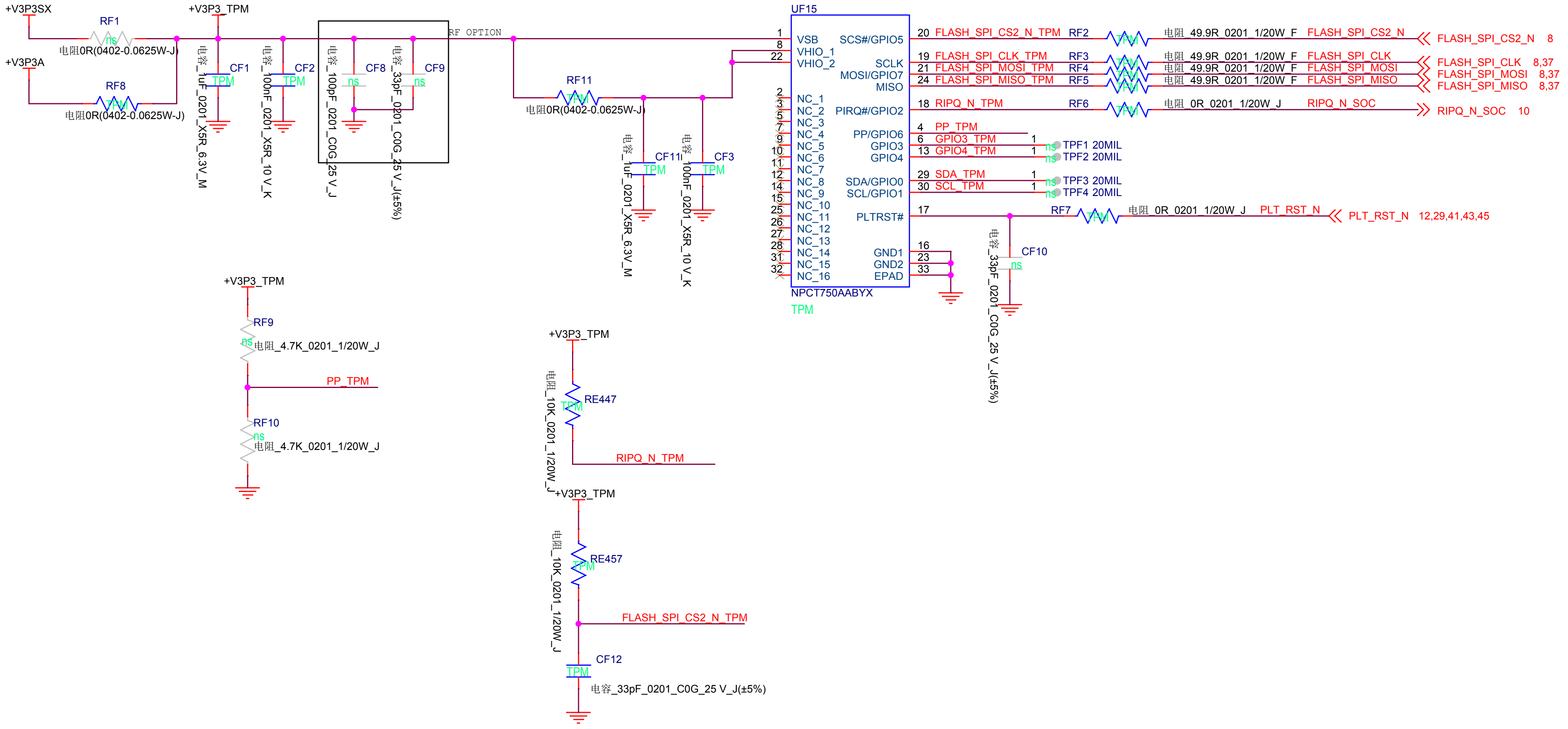

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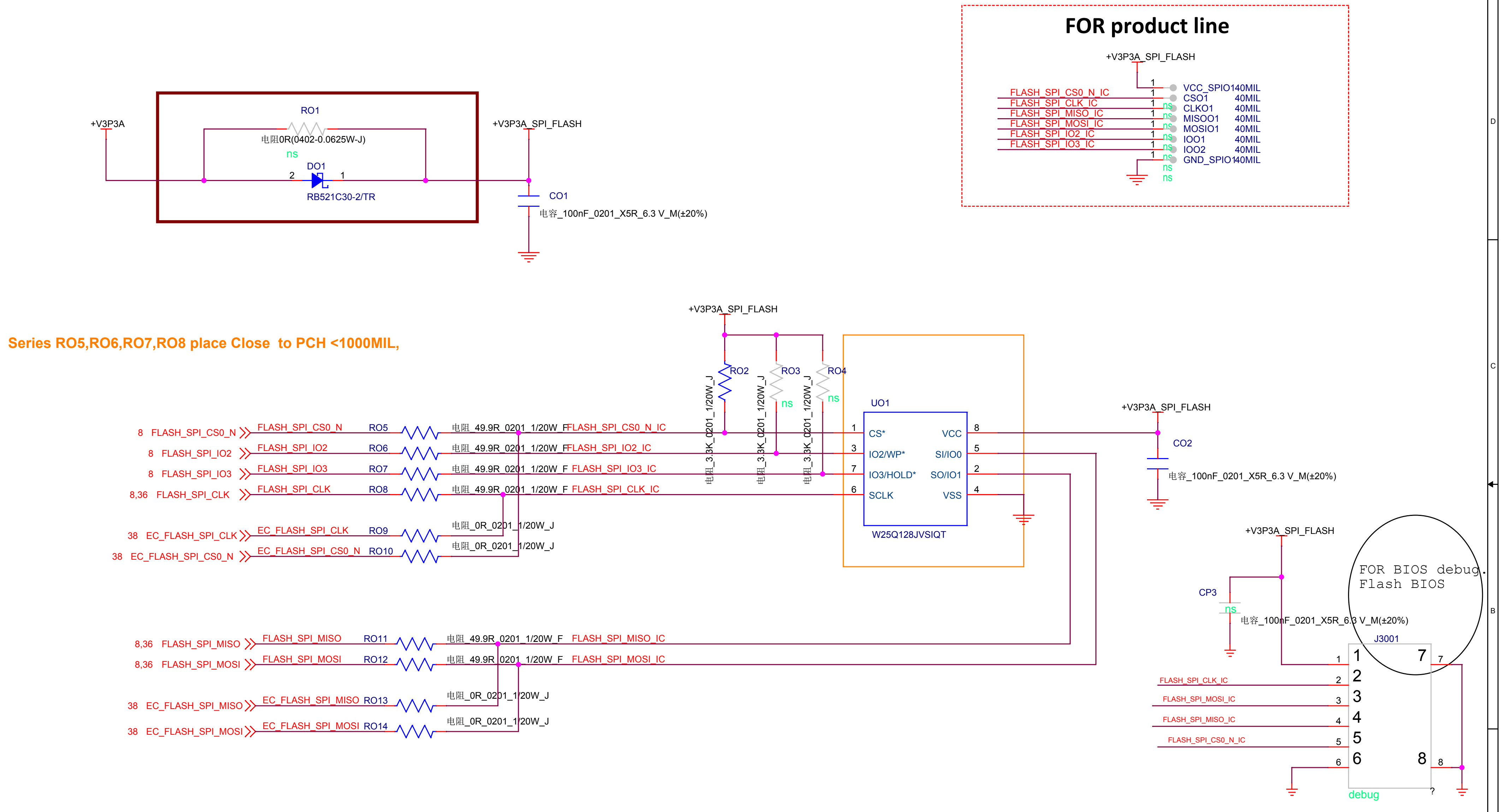

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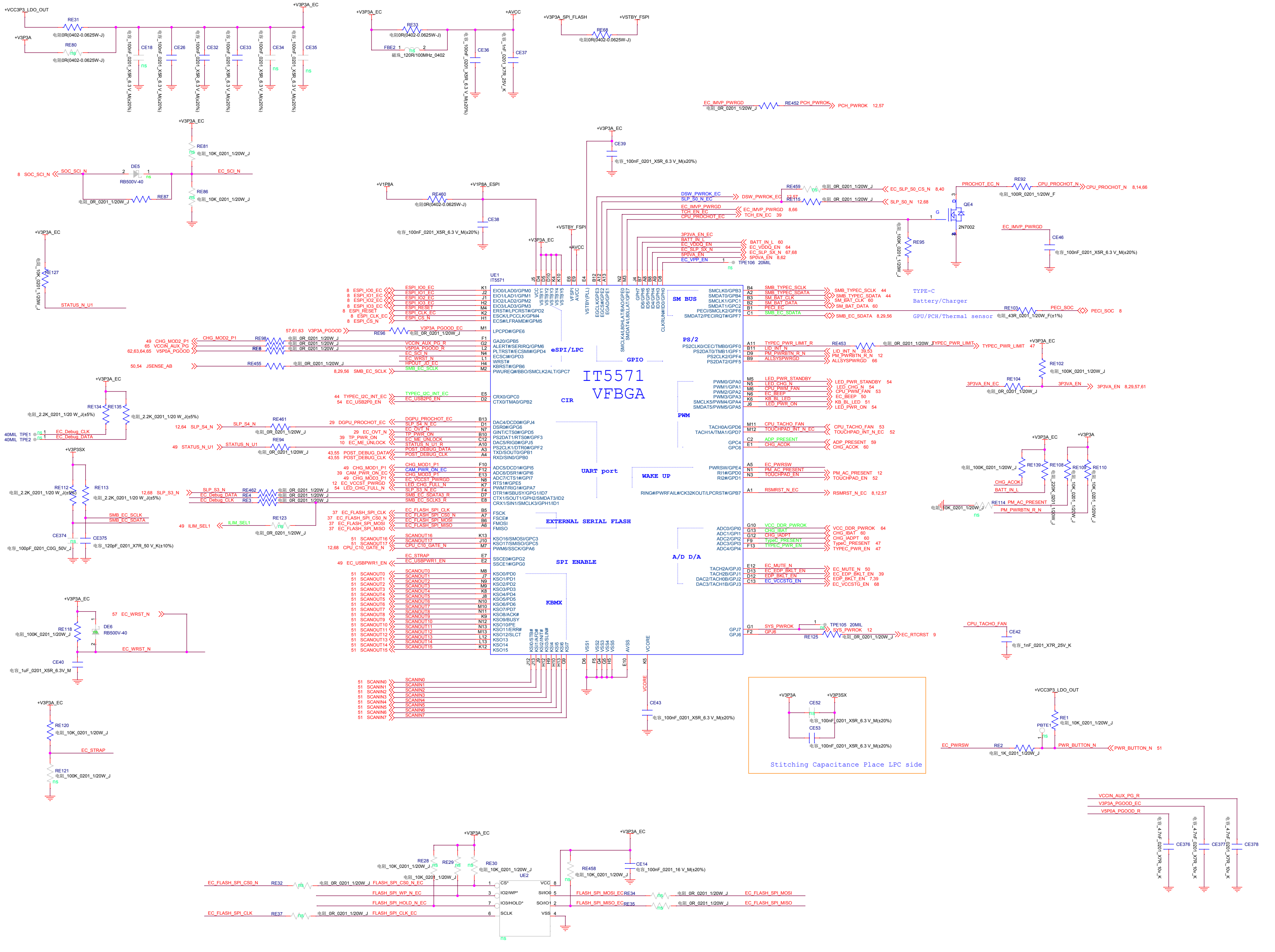

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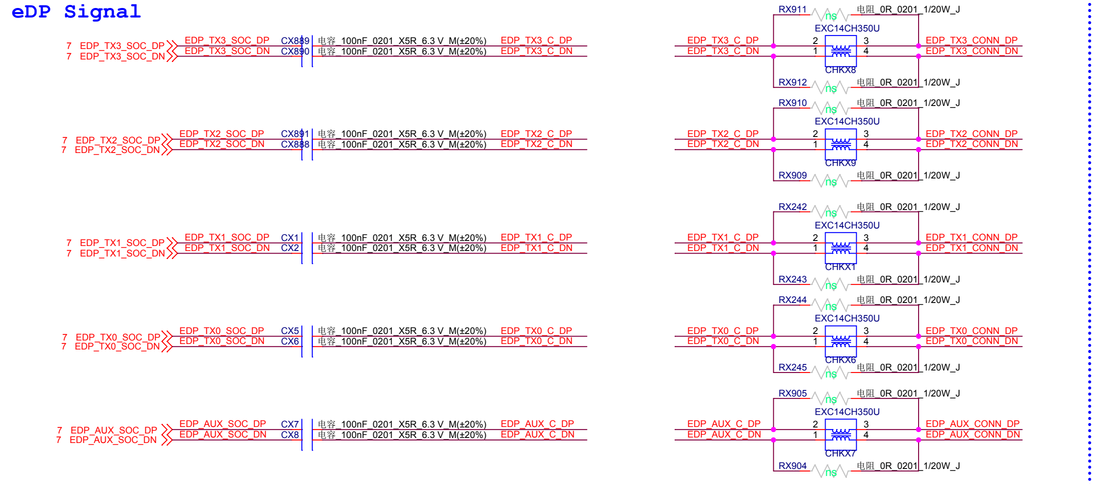
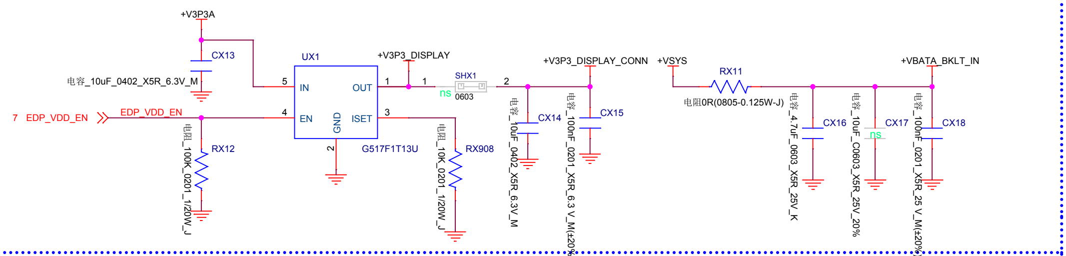
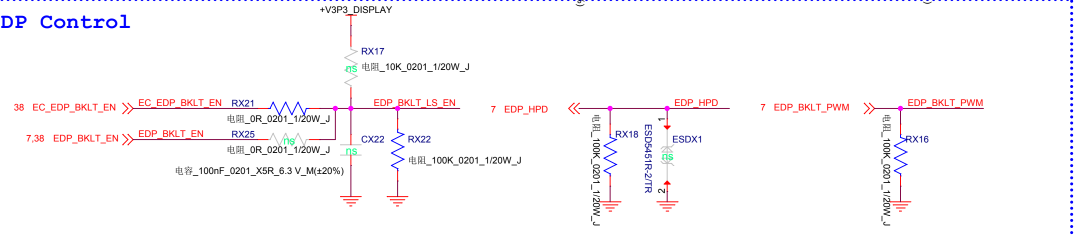
eDP Signal



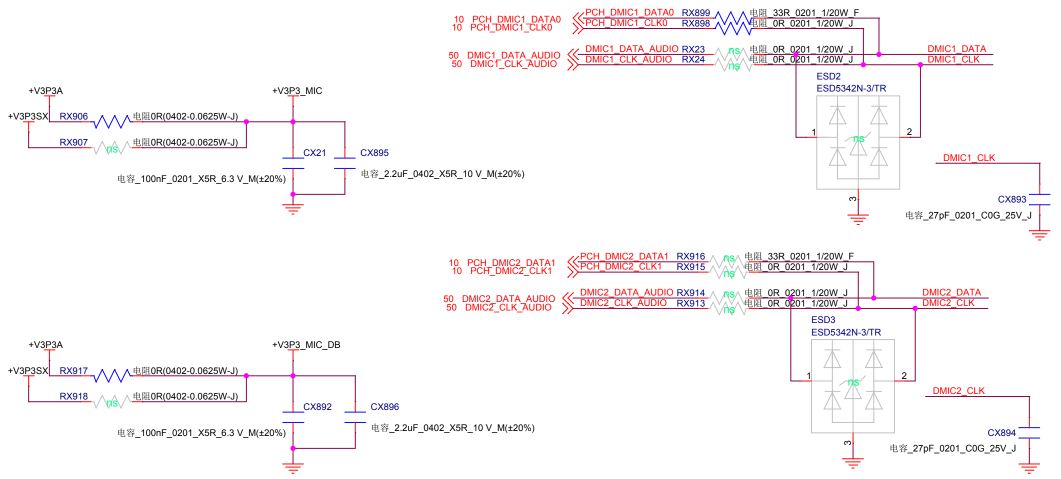
eDP VCC & BL Power



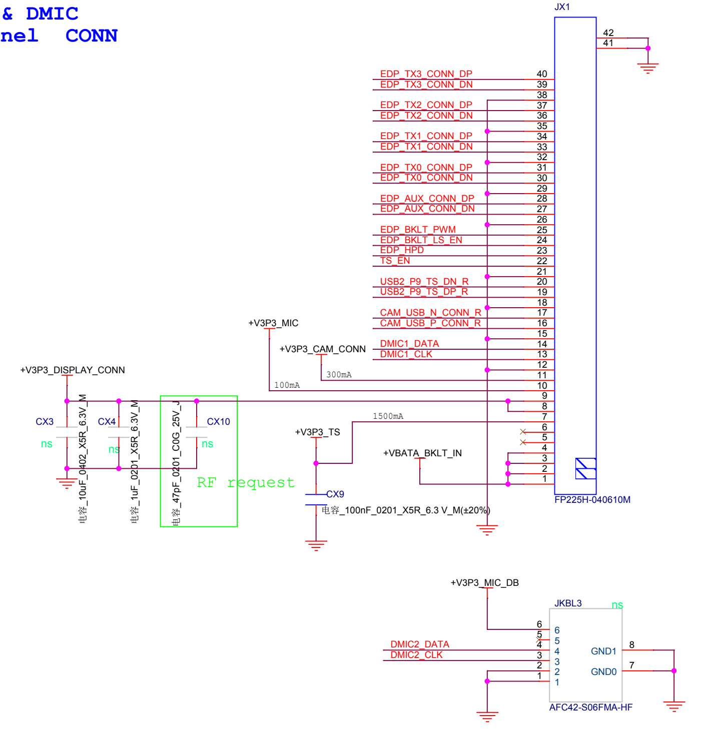
eDP Control



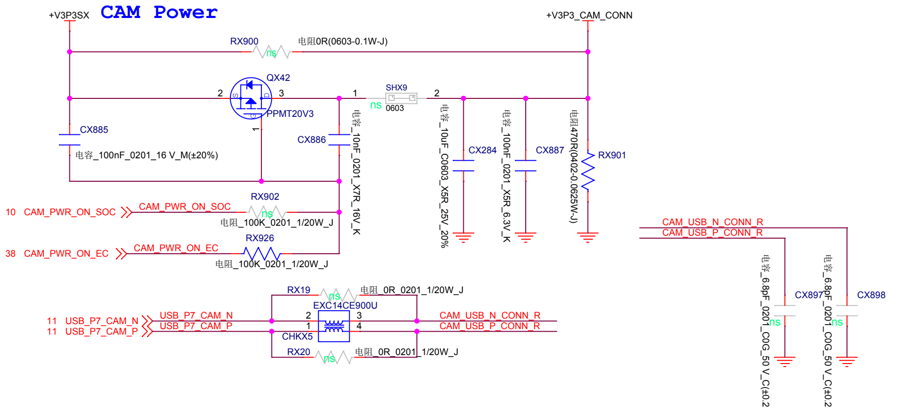
MIC



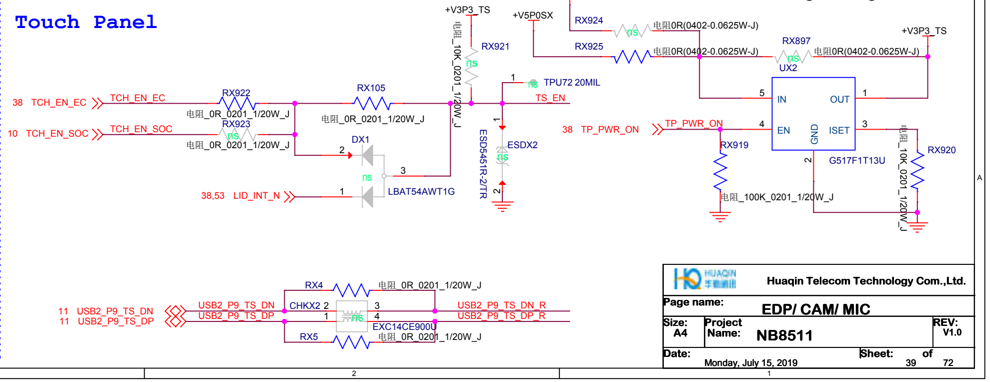
eDP & CAM & DMIC
& Touch Panel CONN



CAM Power



Touch Panel



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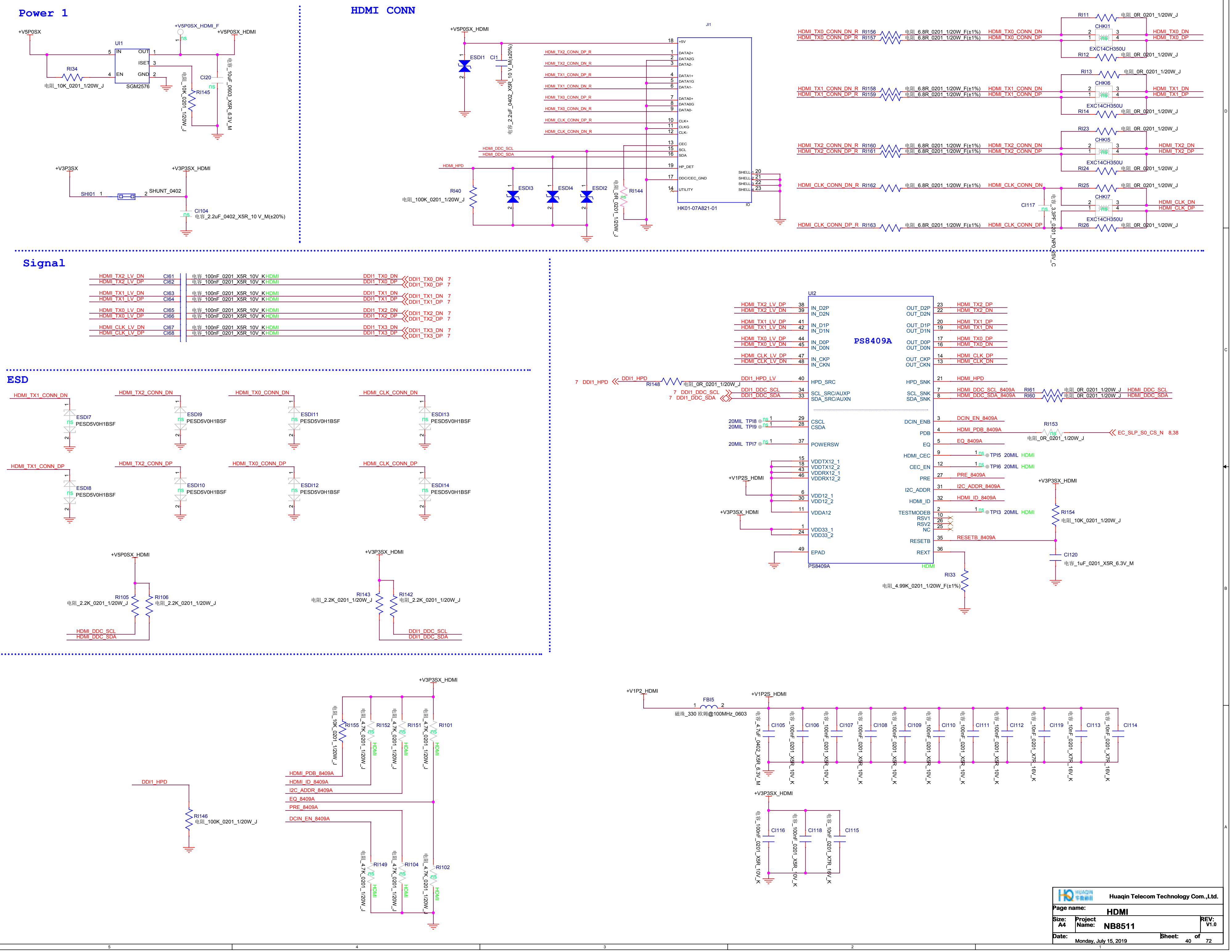

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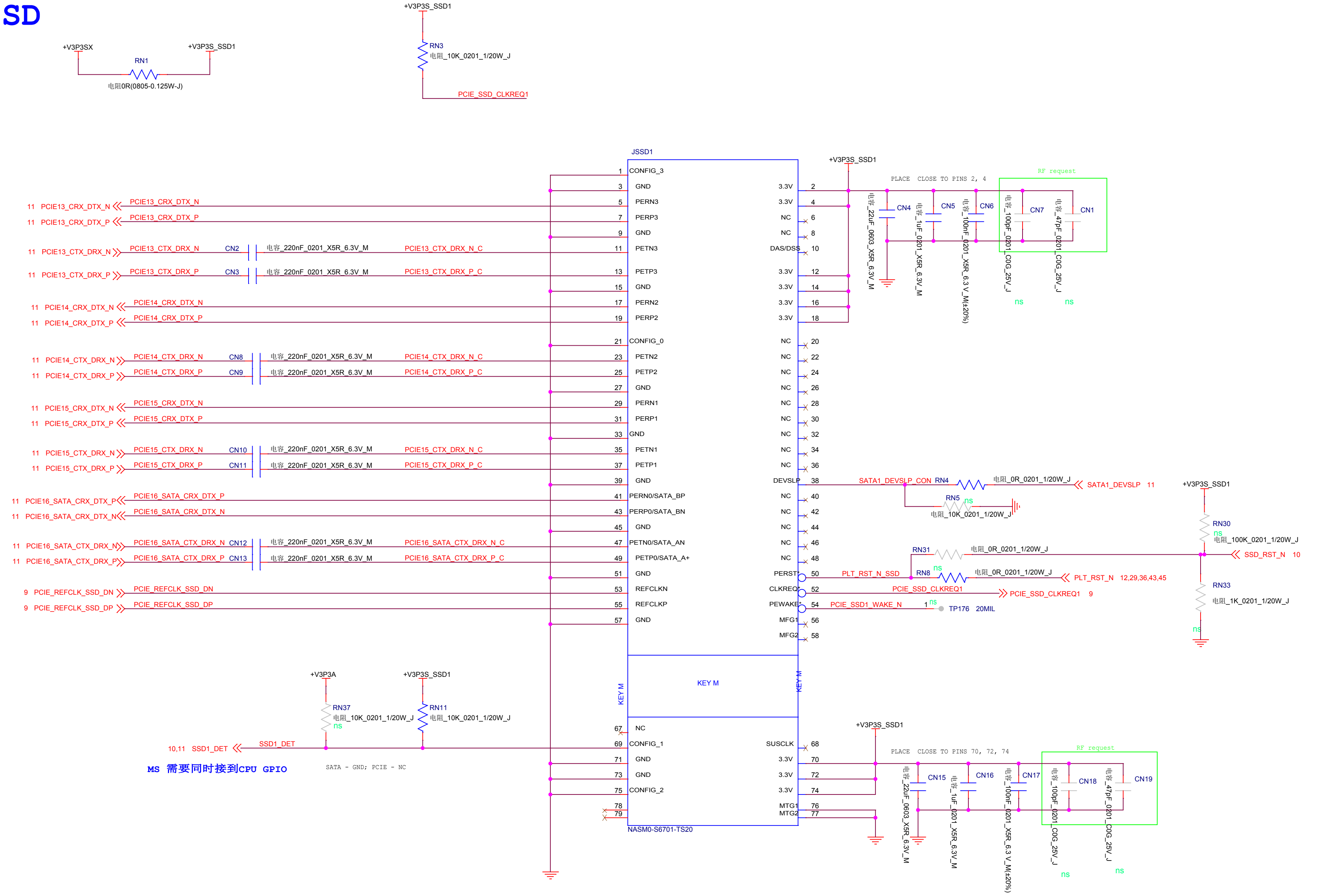
SSD



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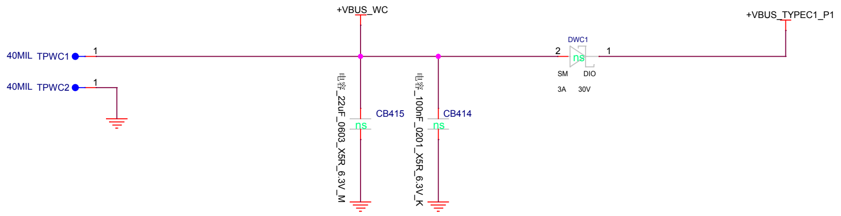

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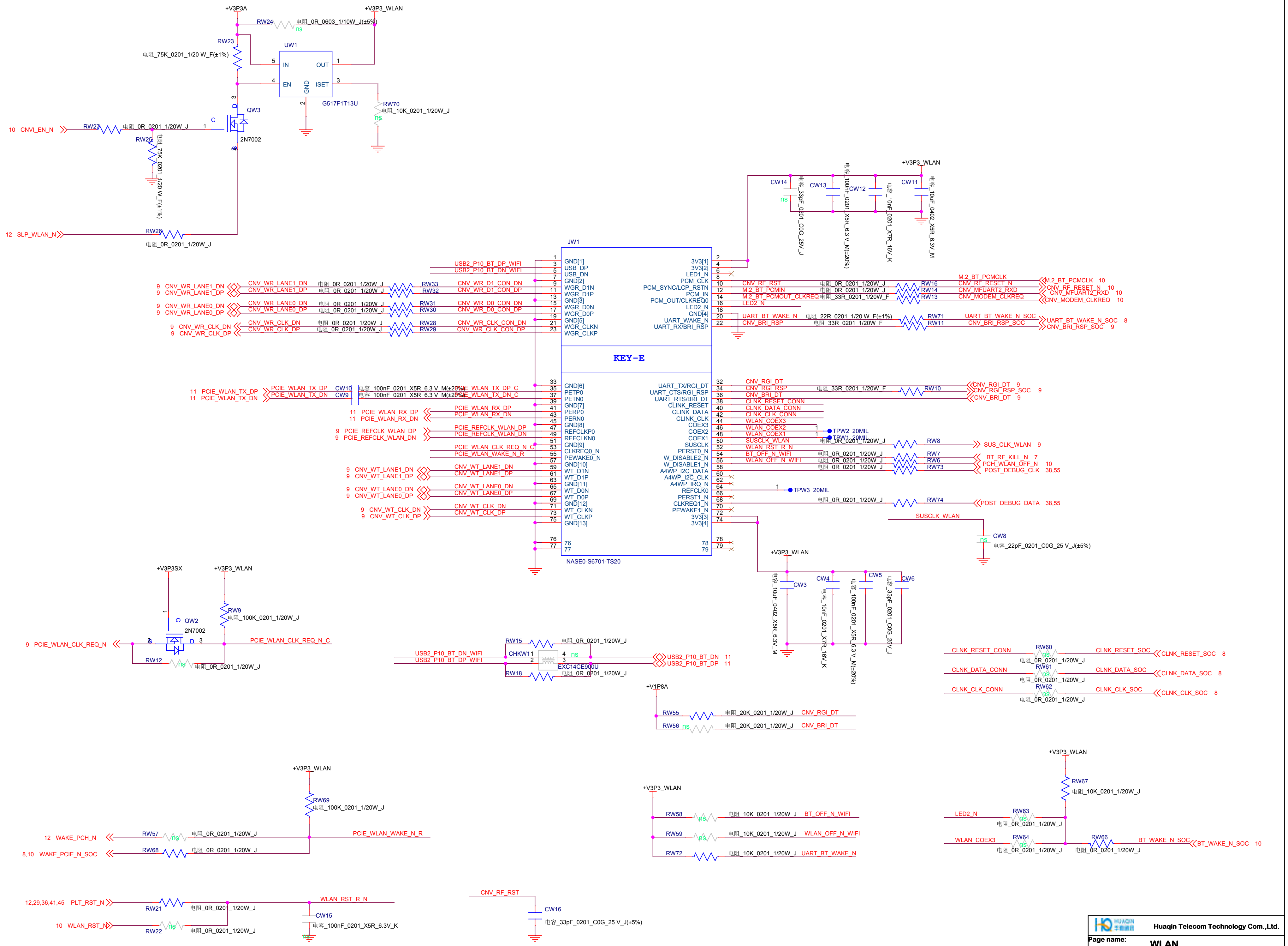

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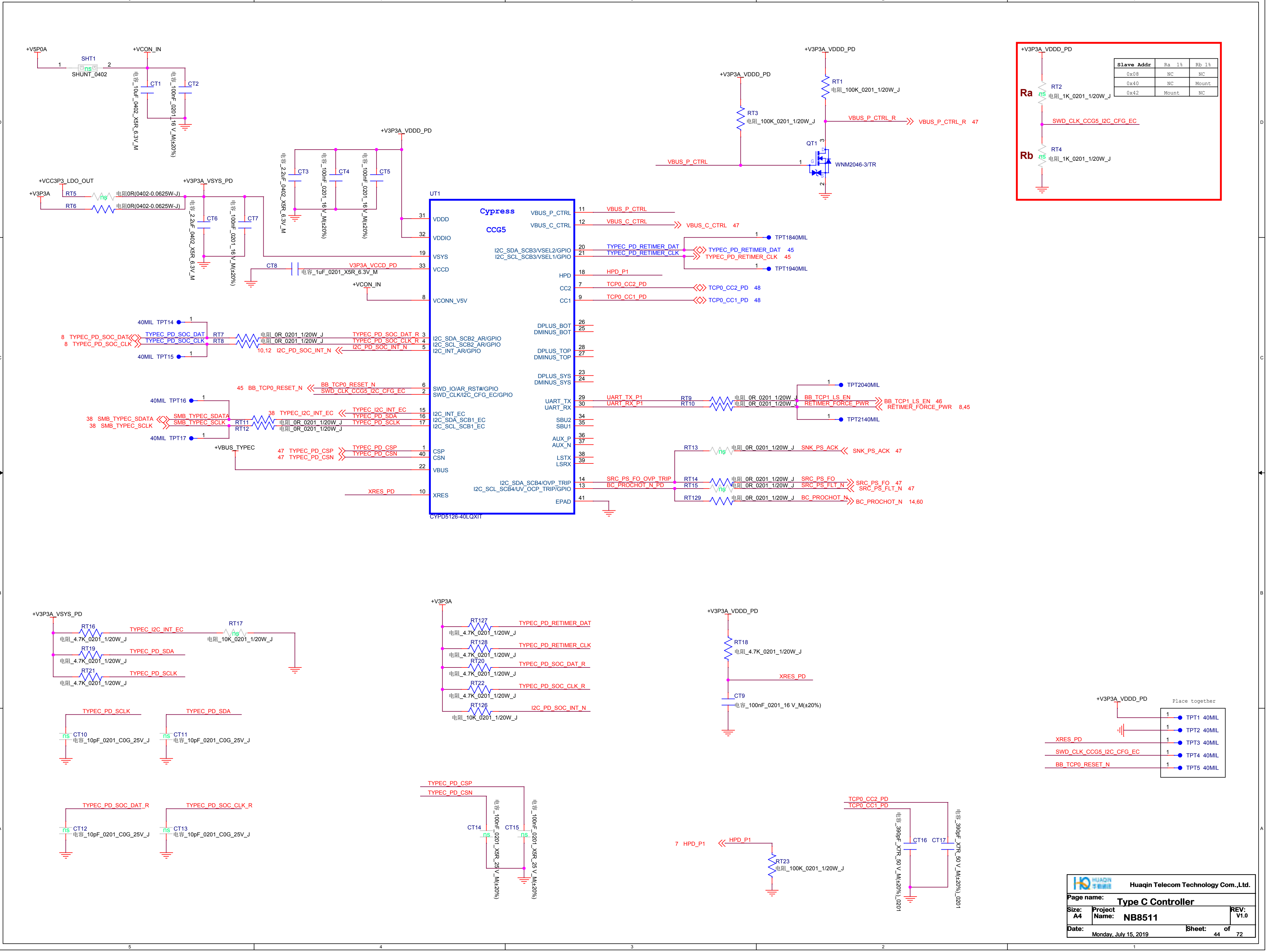

Slave Addr	Ra 1%	Rb 1%
0x08	NC	NC
0x40	NC	Mount
0x42	Mount	NC

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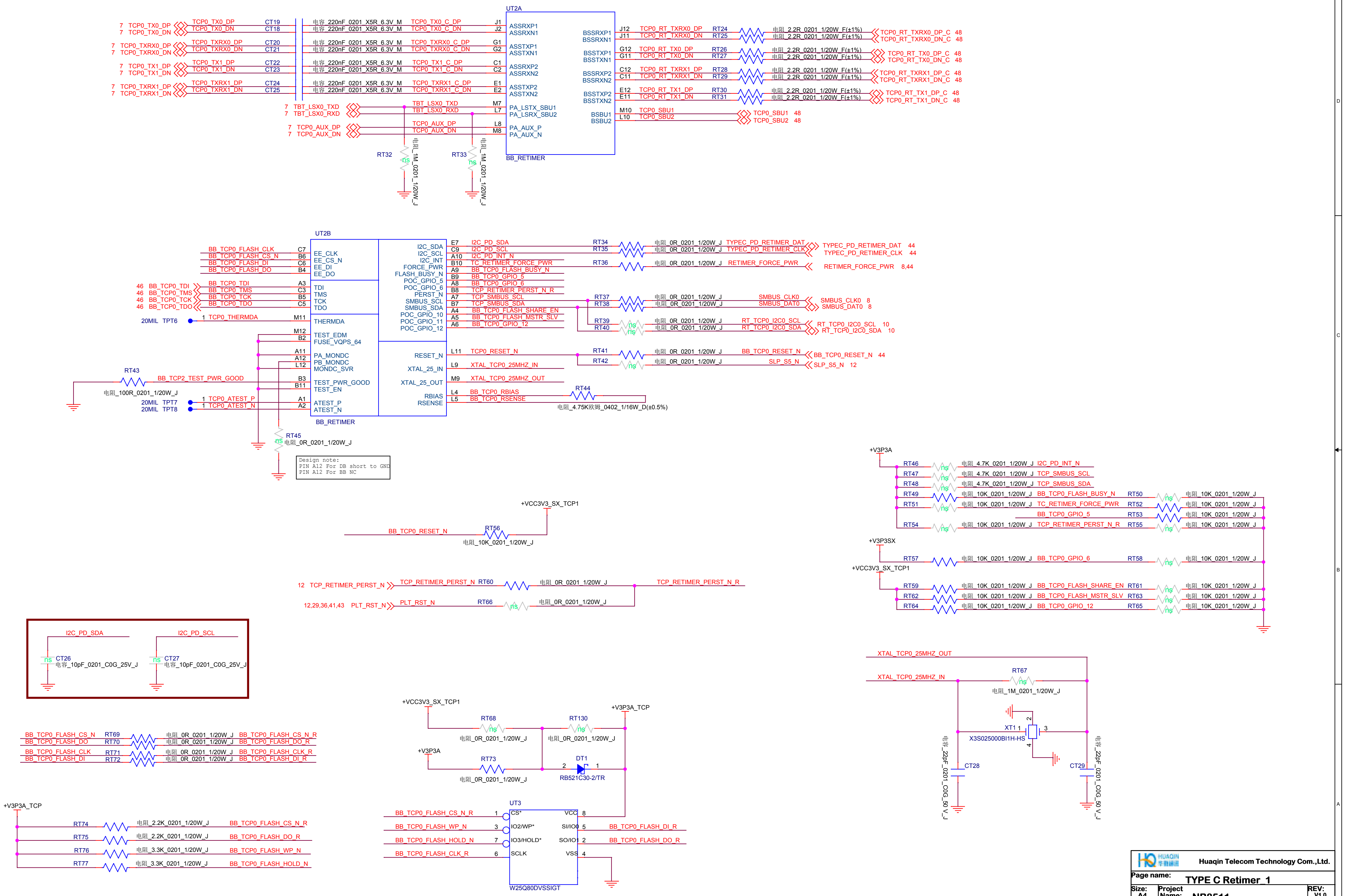

Design note:
PIN A12 For DB short to GND
PIN A12 For BB NC

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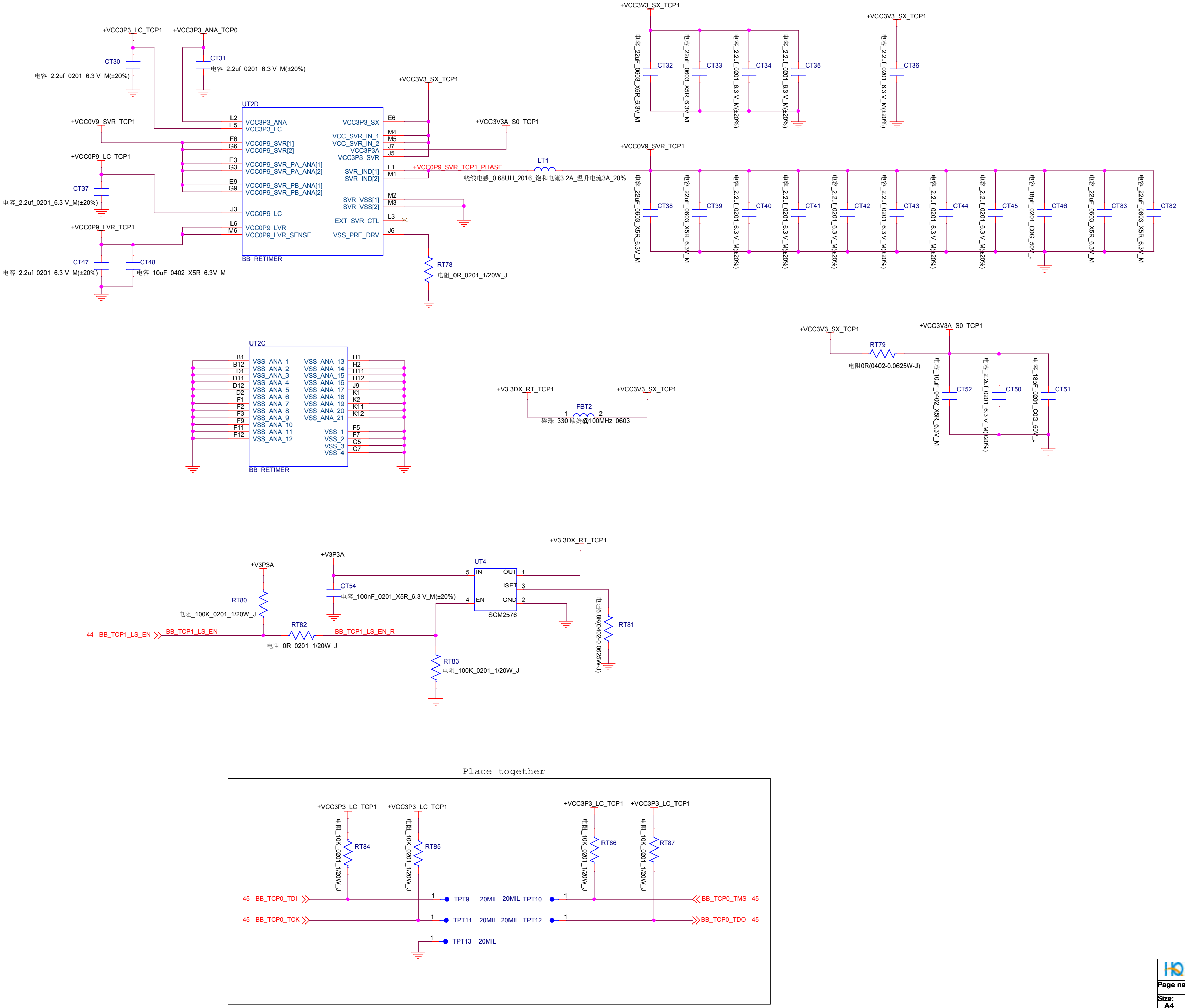

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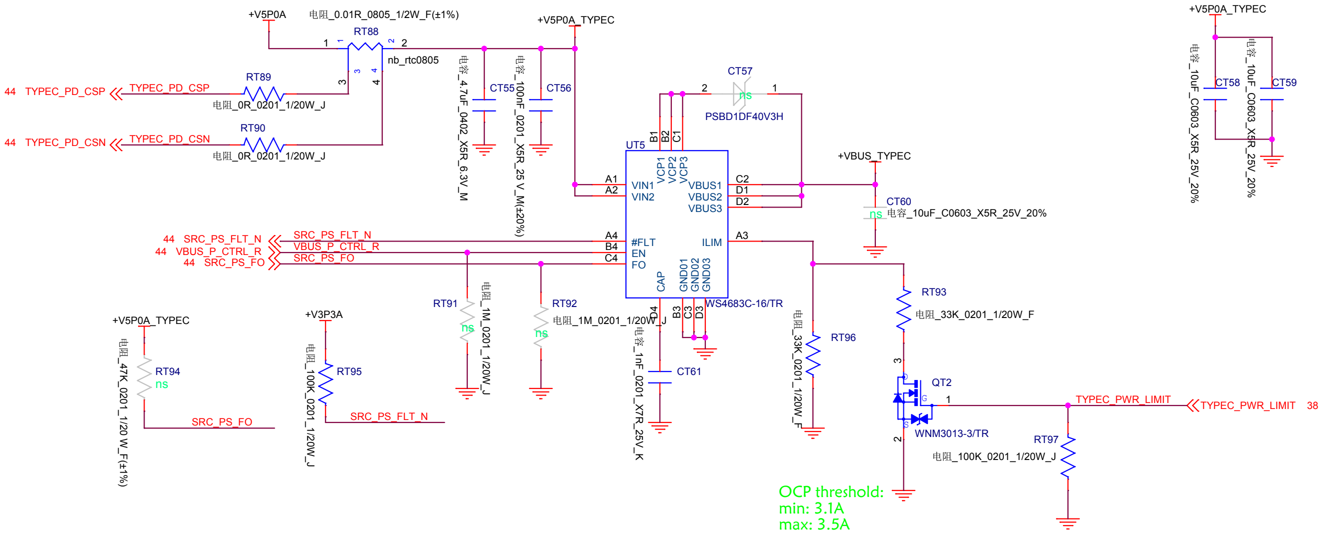

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max: 3.5A

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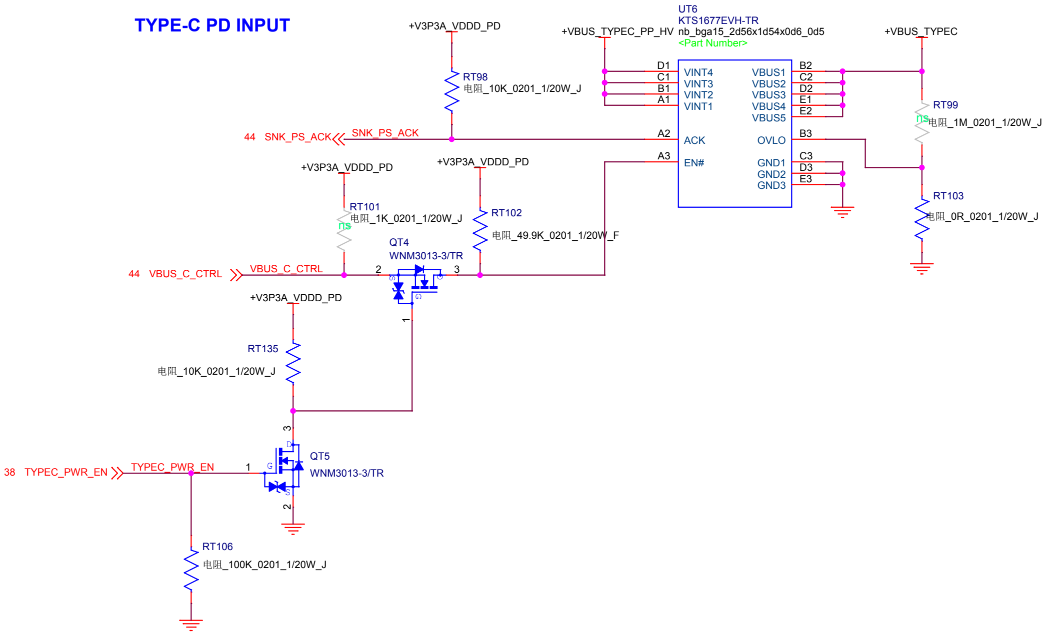

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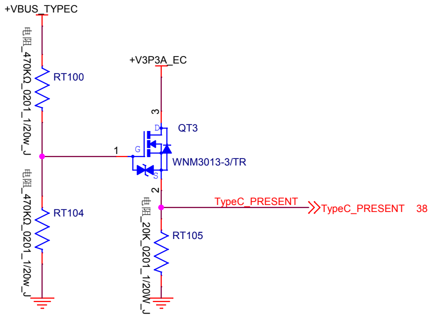

dead battery power on logic

Discharge

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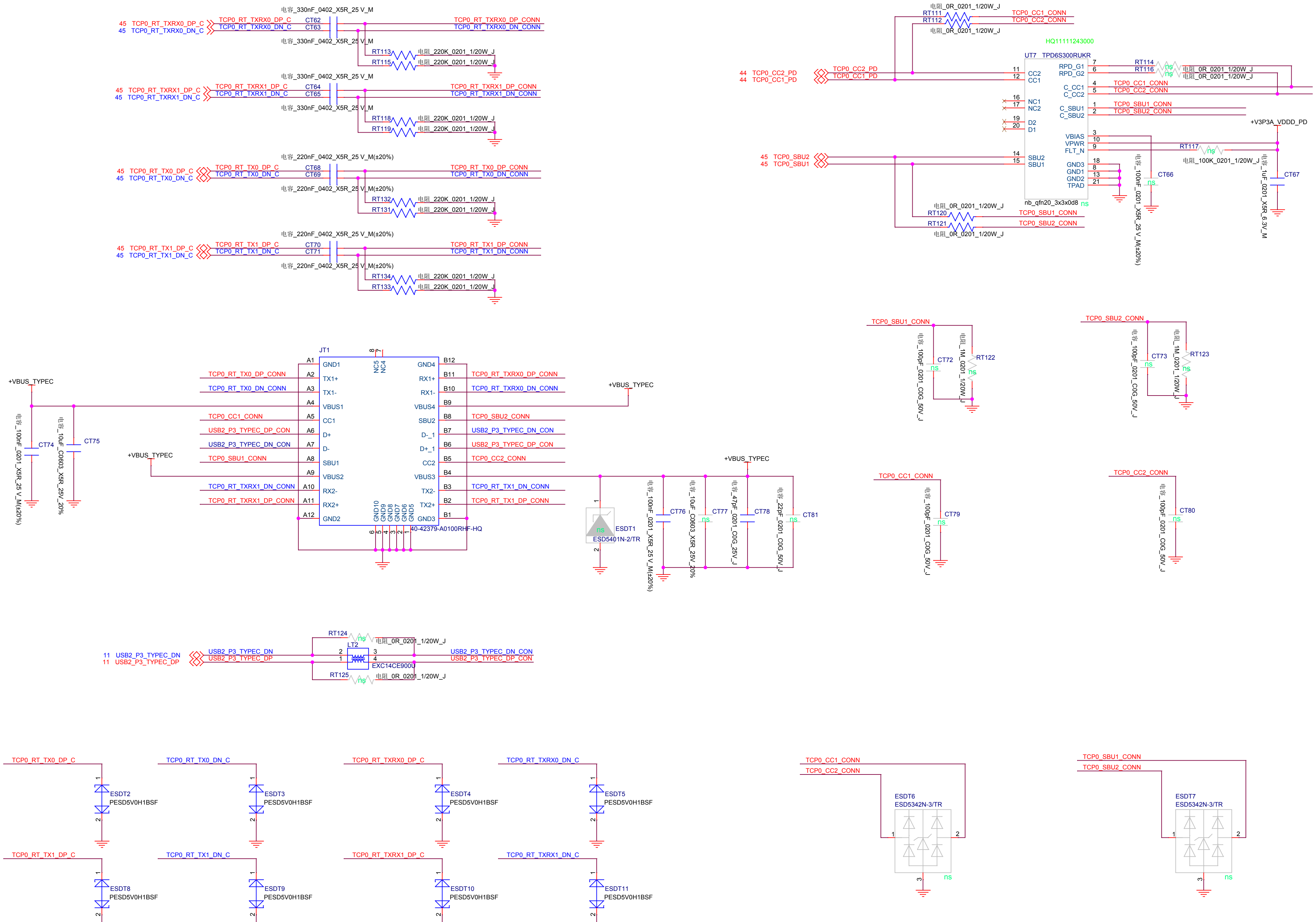

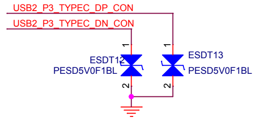

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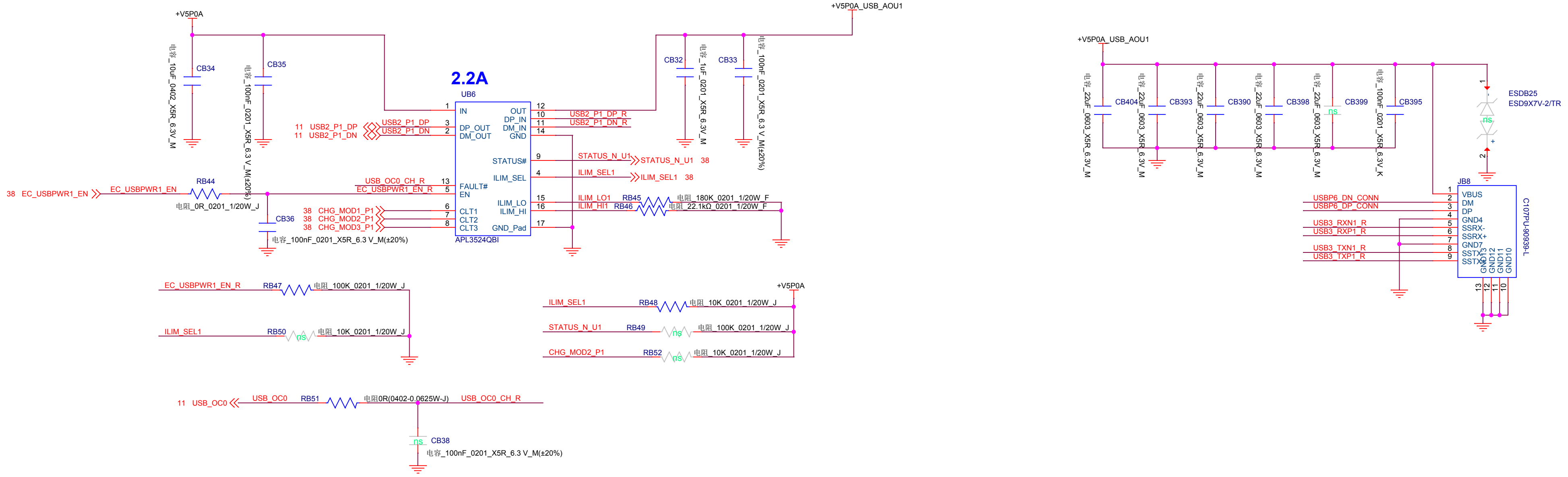
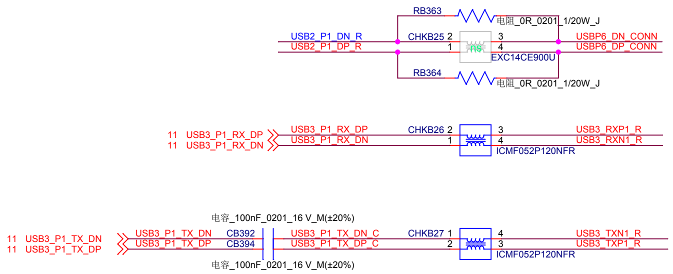
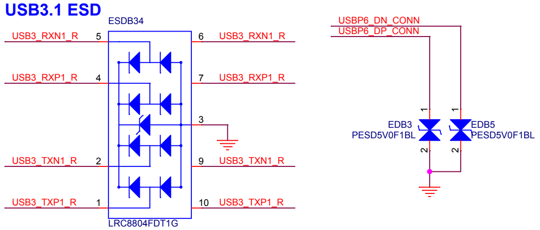
USB3.1 POWER Port1



USB3.1 Signal



USB3.1 ESD



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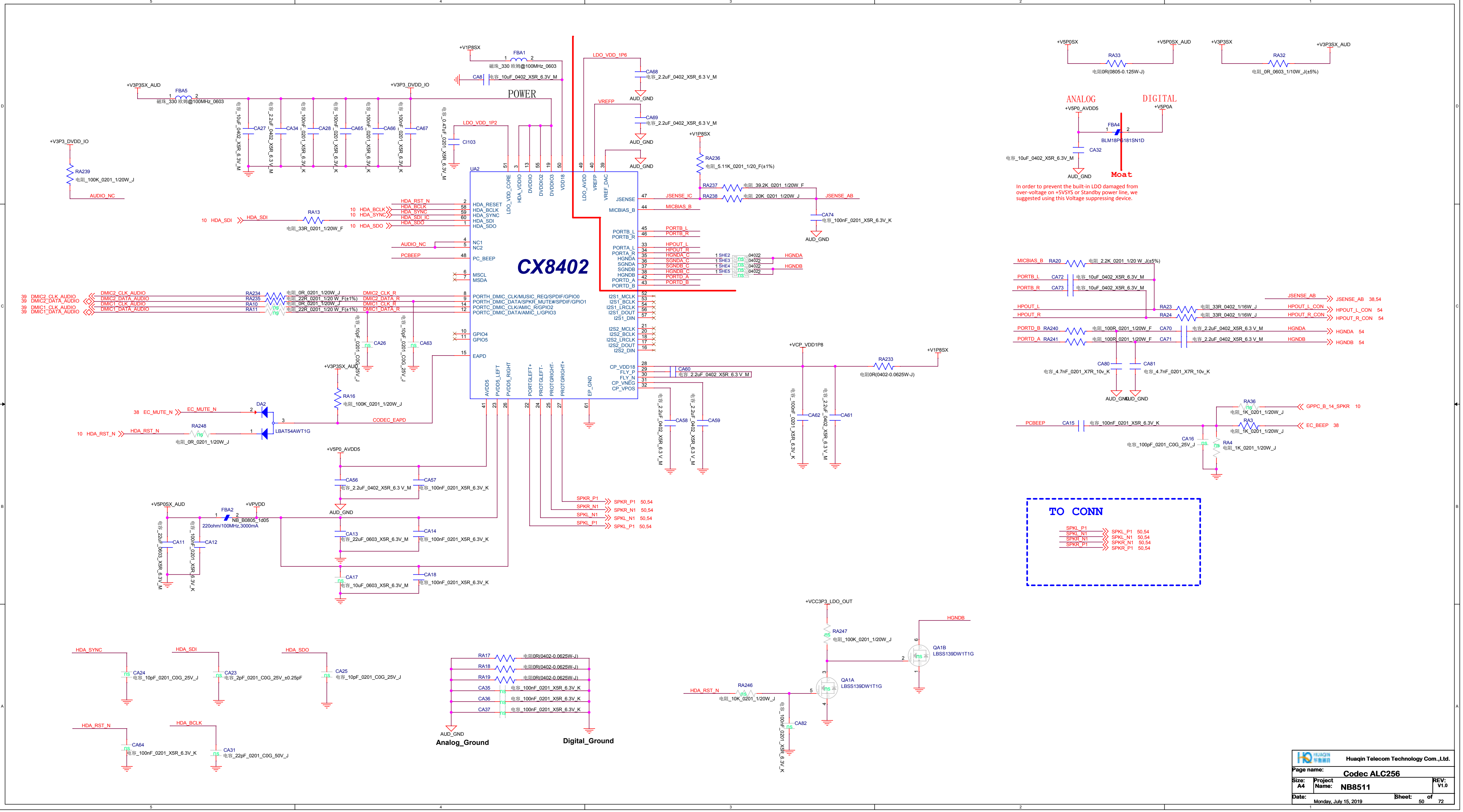

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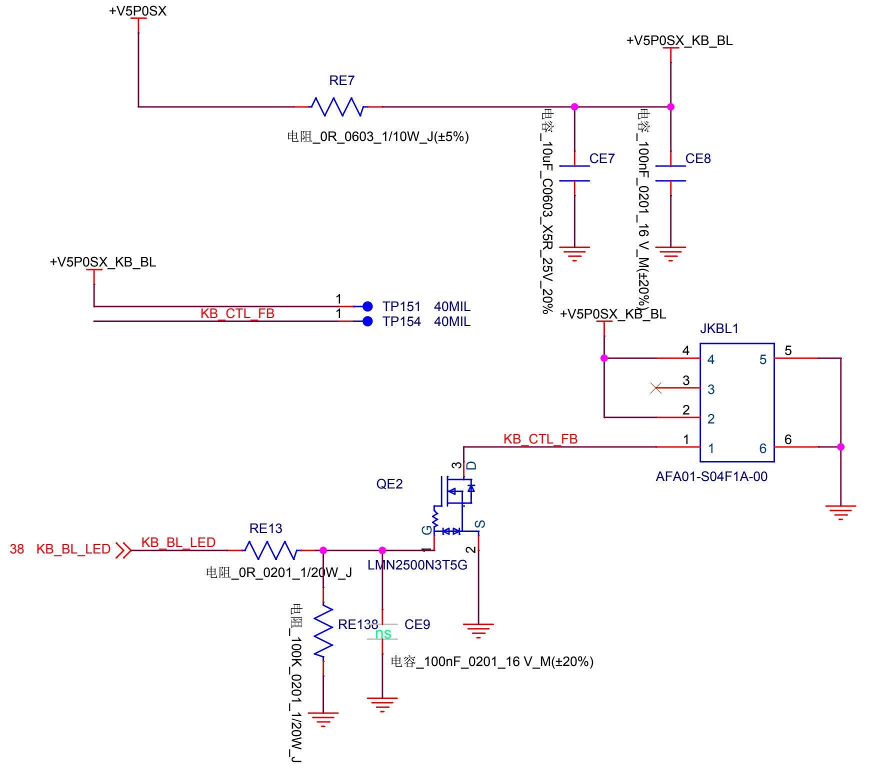
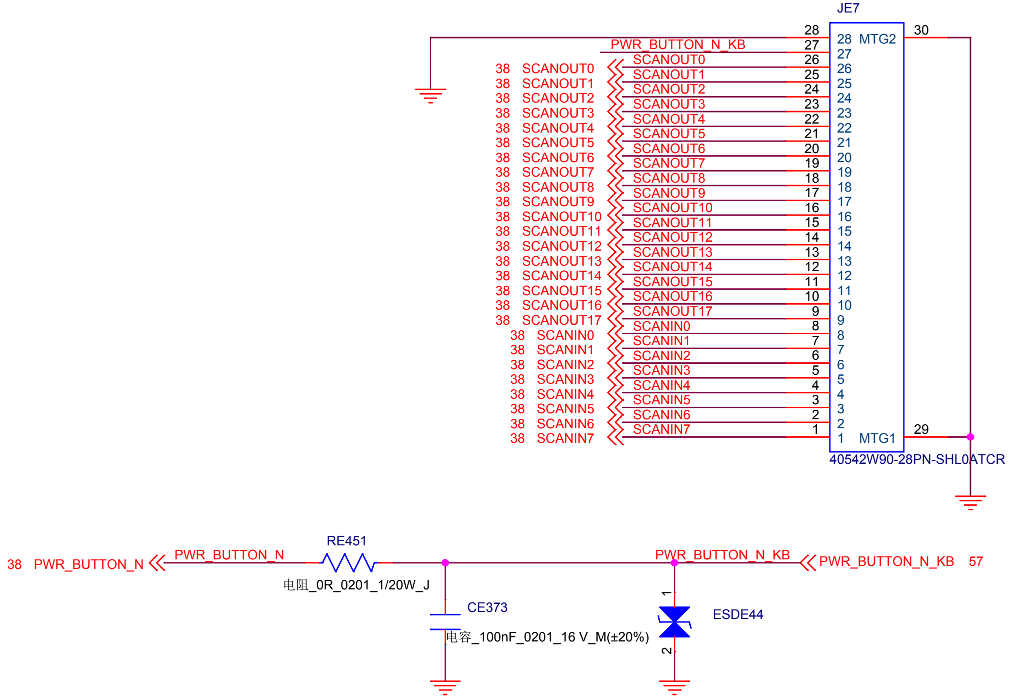
KB Backlight



KB CONN



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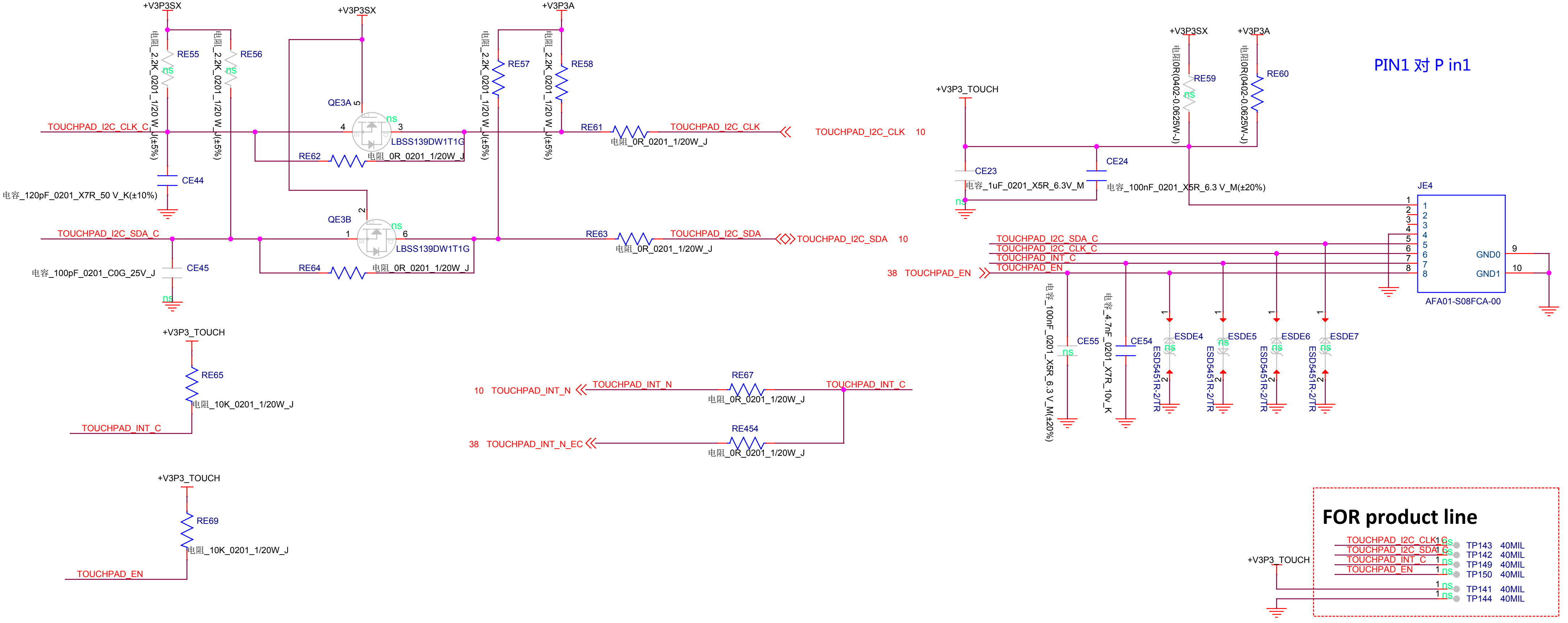
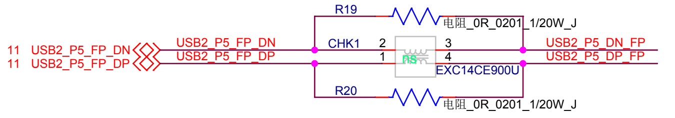
Touch Pad

Touch Pad CONN



Finger Print

Finger Print CONN



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Page name: TouchPad/ Finger Print

Size: A4 Project Name: NB8511 REV: V1.0

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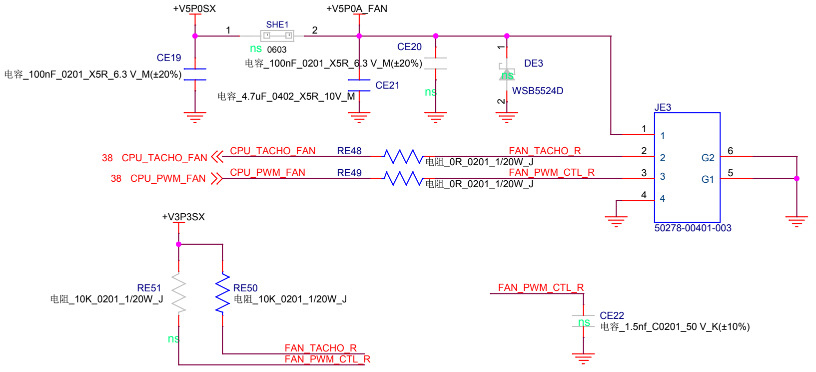
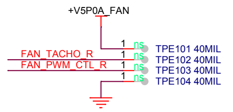
Voice input with LED-NC

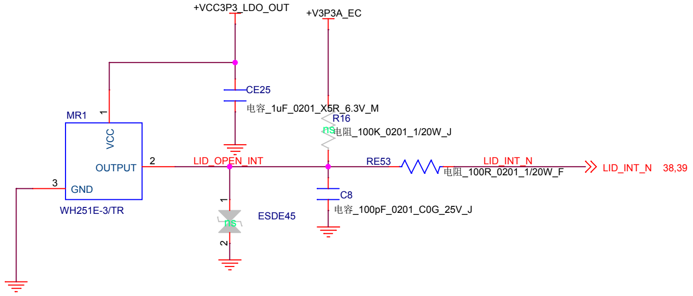
FAN CONN



FOR product line

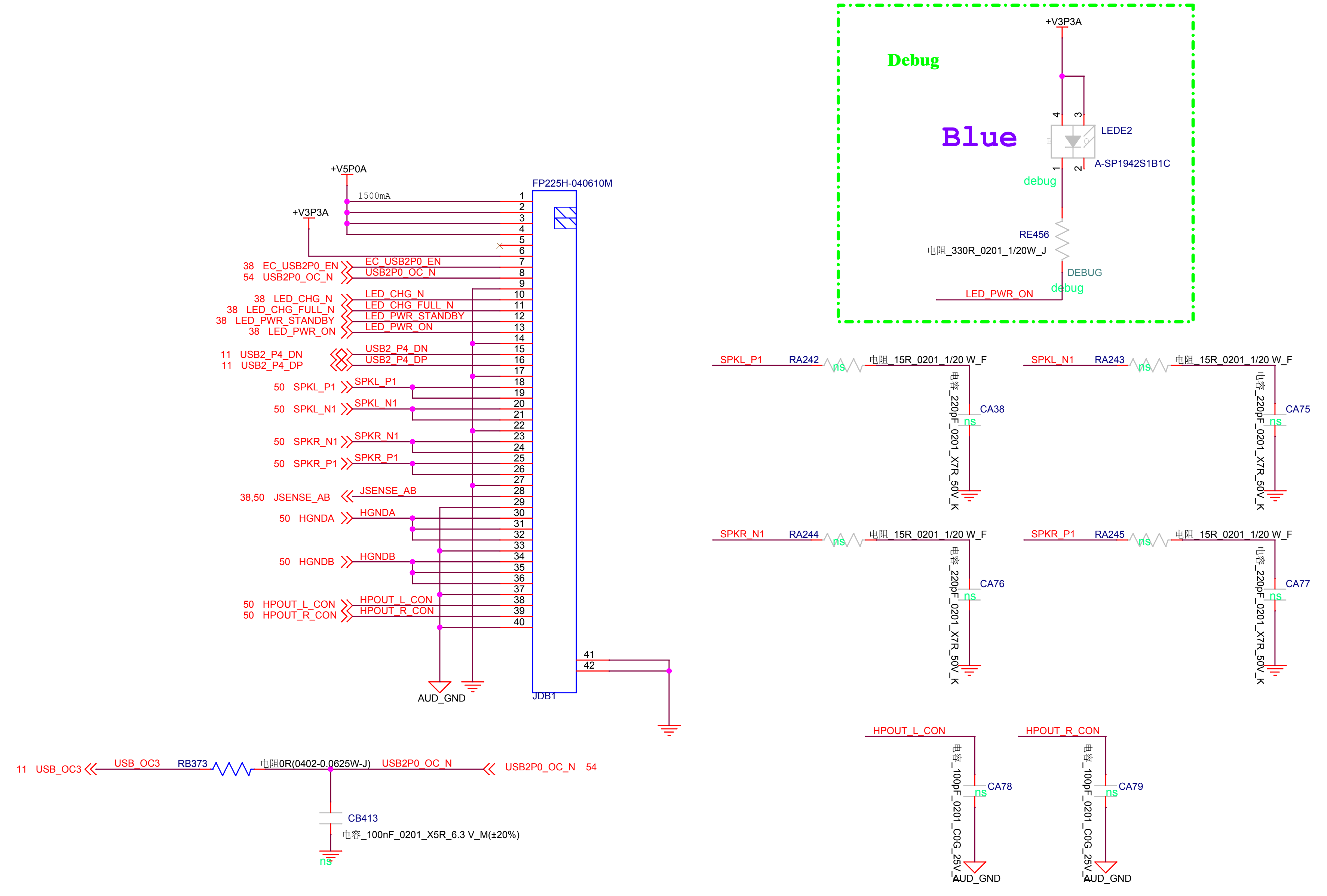


HALL



Huaqin Telecom Technology Com.,Ltd.

Page name:	G-SENSOR/FAN/LED/Hall	
Size: A4	Project Name: NB8511	REV: V1.0
Date: Monday, July 15, 2019	Sheet: 53 of 72	



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Page name:	DB CONNECTOR
Size: A4	Project Name: NB8511
REV:	V1.0
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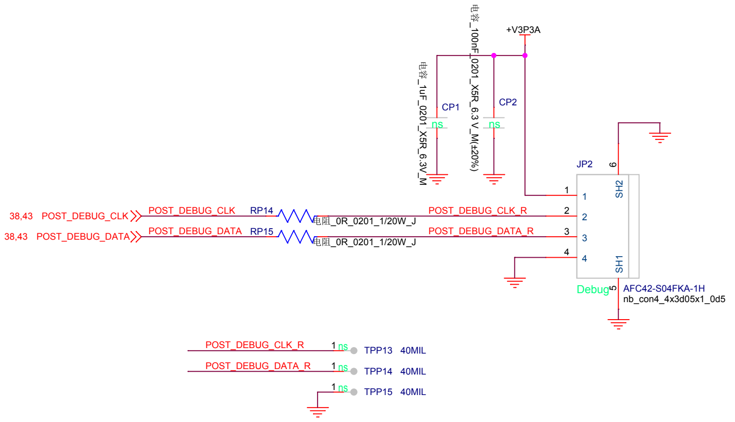

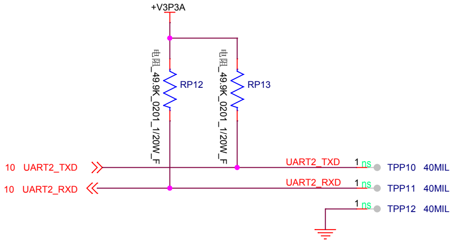

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Page name: **Debug Conn**

Size: **A4**
Project Name: **NB8511**
REV: **V1.0**

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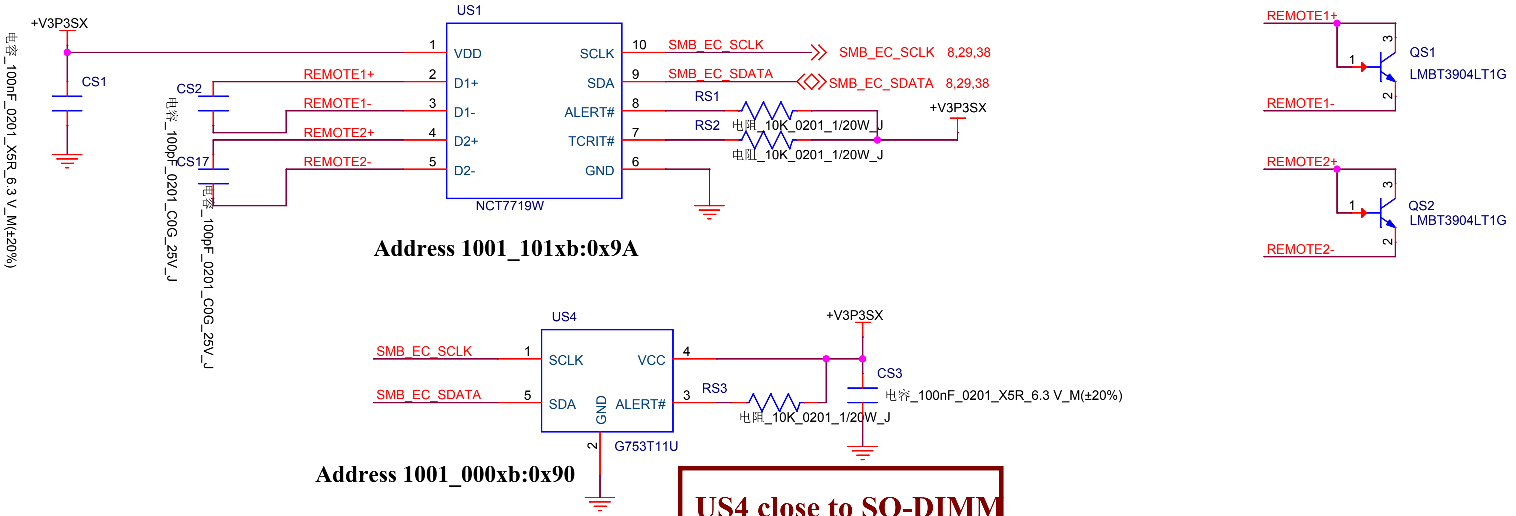
Sheet: 55 **of** 72

REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces

Close to charger



Address 1001_101xb:0x9A

Address 1001_000xb:0x90

US4 close to SO-DIMM

Between CPU and GPU

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Page name: Thermal sensor

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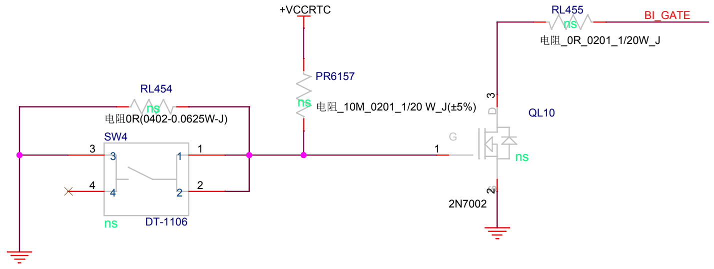
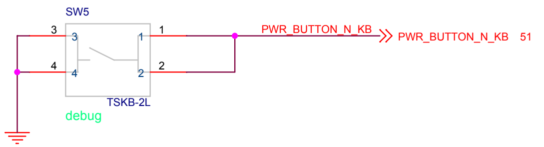
Reset BUTTON

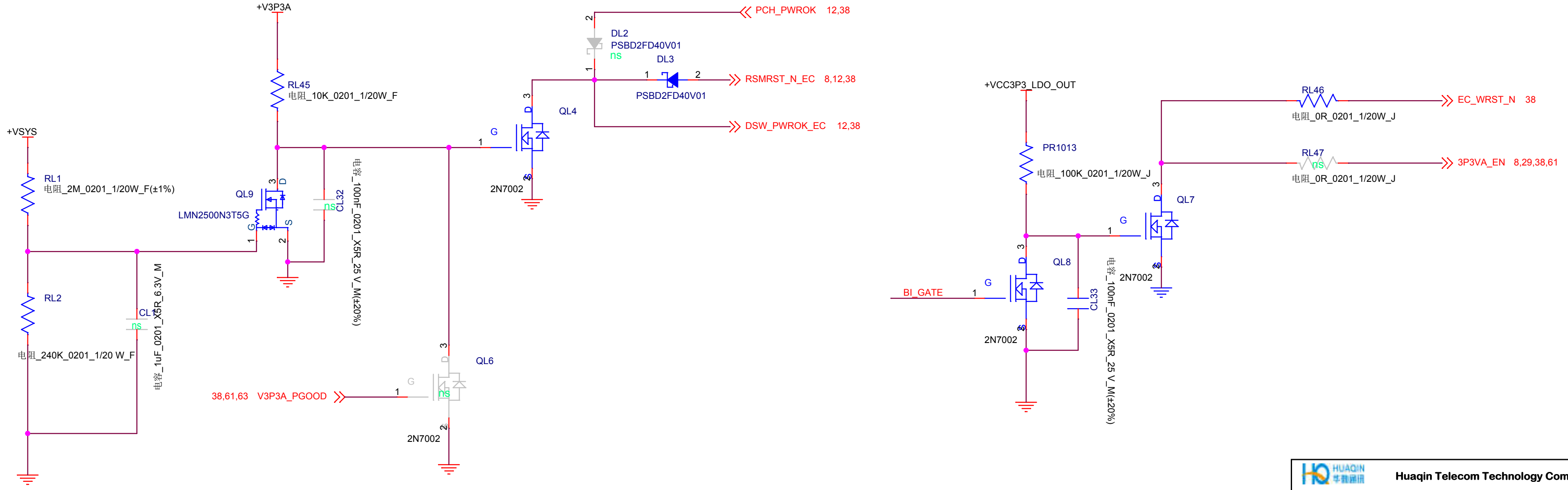
Open door BUTTON



Debug BUTTON



Abnormal PD logic



Huaqin Telecom Technology Com.,Ltd.

Page name: **Logic Circuit**

Size: A4
Project Name: **NB8511**
REV: V1.0

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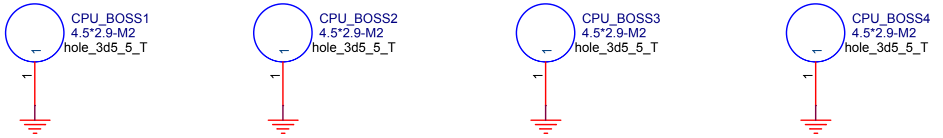
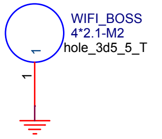
CPU螺母元件 *4

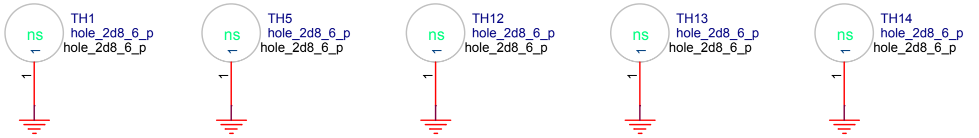


GPU螺母元件 *2

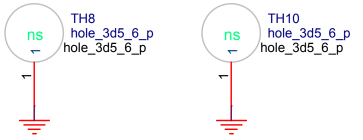
WIFI螺母元件 *1



HOLE *5



HOLE *2



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Page name: **BLANK**

Size: **A4**
Project Name: **NB8511**
REV: **V1.0**

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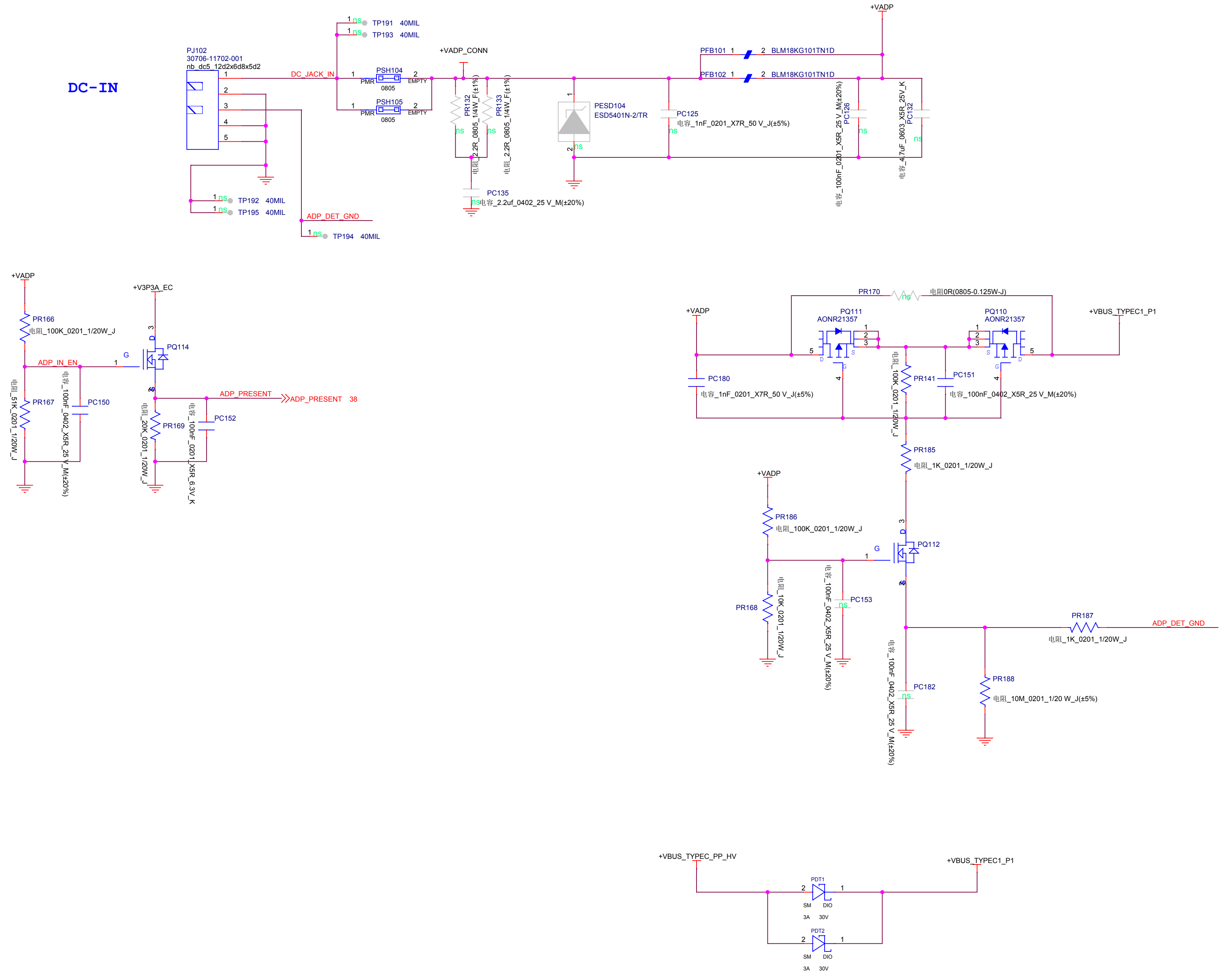

HUAQIN 华勤通讯 **Huaqin Telecom Technology Com.,Ltd.**

Page name: **DC-IN**

Size: A4 | Project Name: **NB8511** | REV: V1.0

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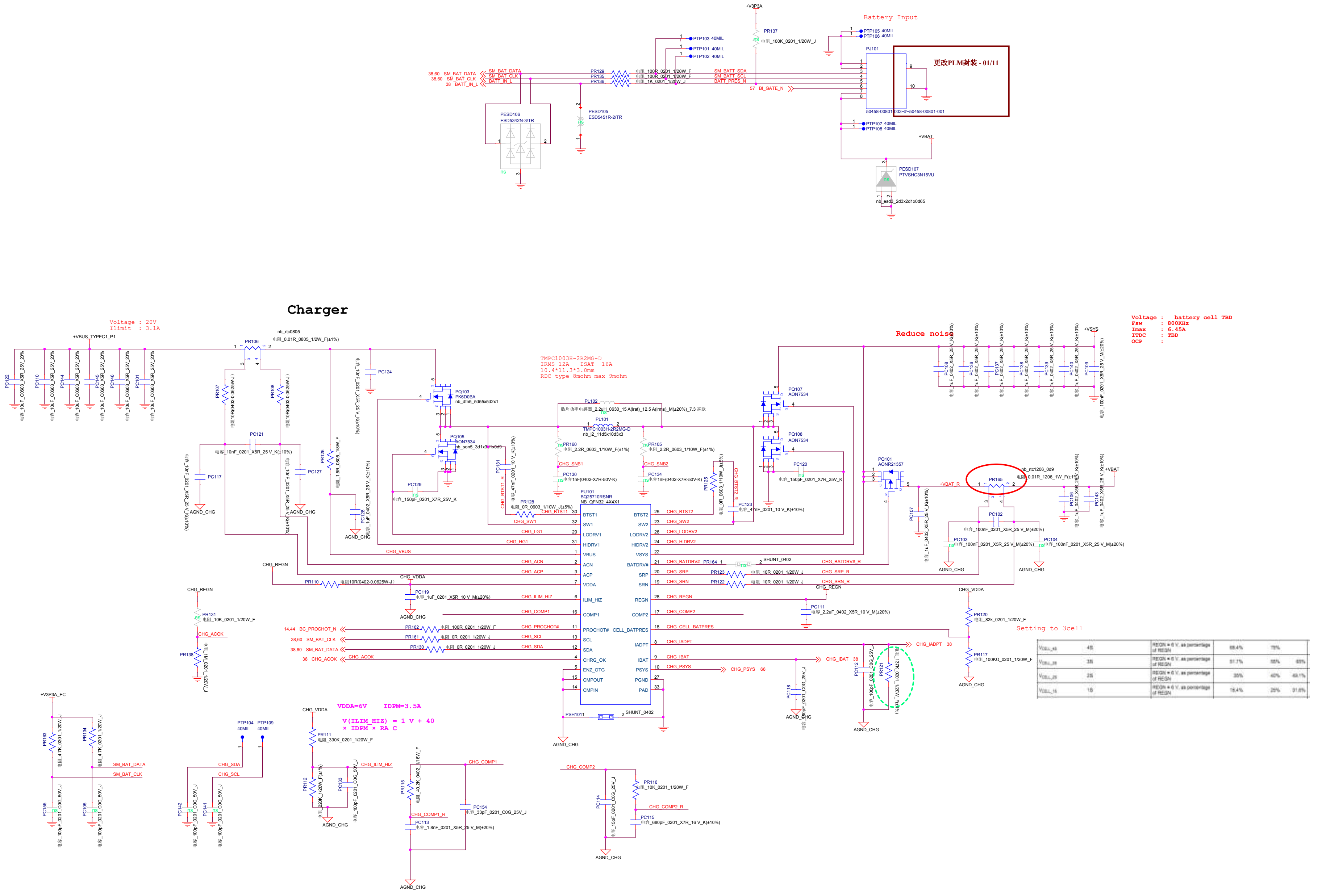
Charger



Voltage : 20V
Ilimit : 3.1A

TMPC1003H-2R2MG-D
IRMS 12A ISAT 16A
10.4*11.3*3.0mm
RDC type 8mohm max 9mohm

Reduce noise

Voltage : battery cell TBD
Fsw : 800KHz
Imax : 6.45A
ITDC : TBD
OCP :

Setting to 3cell

V_CELL_4S	4S	REGN = 6 V, as percentage of REGN	68.4%	75%	
V_CELL_3S	3S	REGN = 6 V, as percentage of REGN	51.7%	55%	65%
V_CELL_2S	2S	REGN = 6 V, as percentage of REGN	35%	40%	49.1%
V_CELL_1S	1S	REGN = 6 V, as percentage of REGN	18.4%	25%	31.6%

VDDA=6V IDPM=3.5A

V(ILIM_HIZ) = 1 V + 40 × IDPM × RA C

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Page name:	BATTERY CHARGER
Size: A4	Project Name: NB8511
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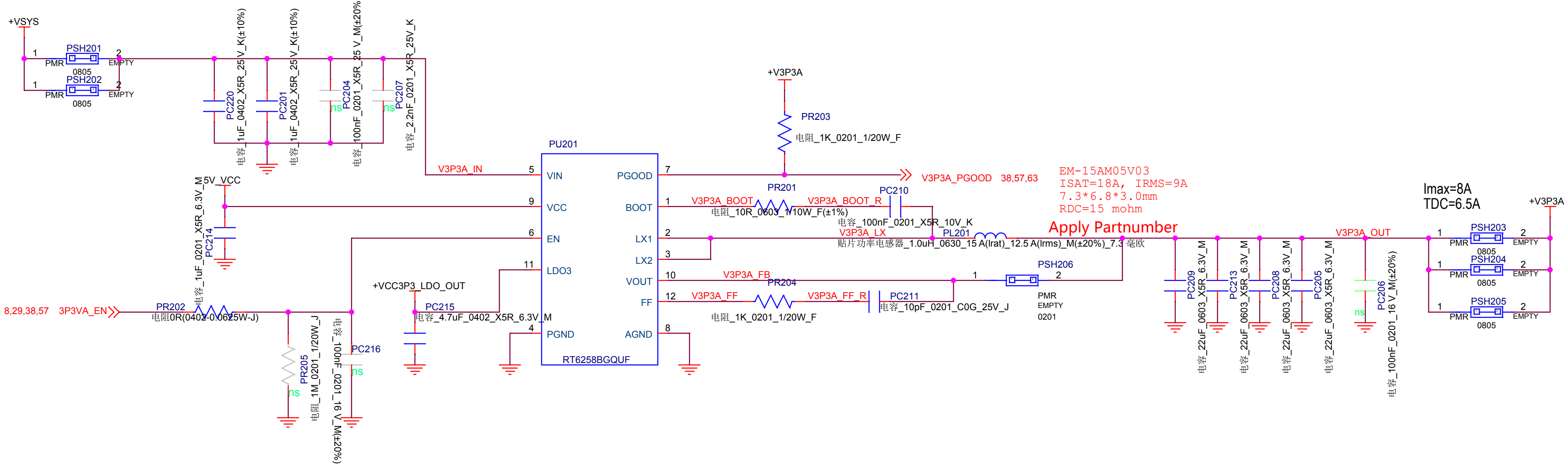
+V3P3A



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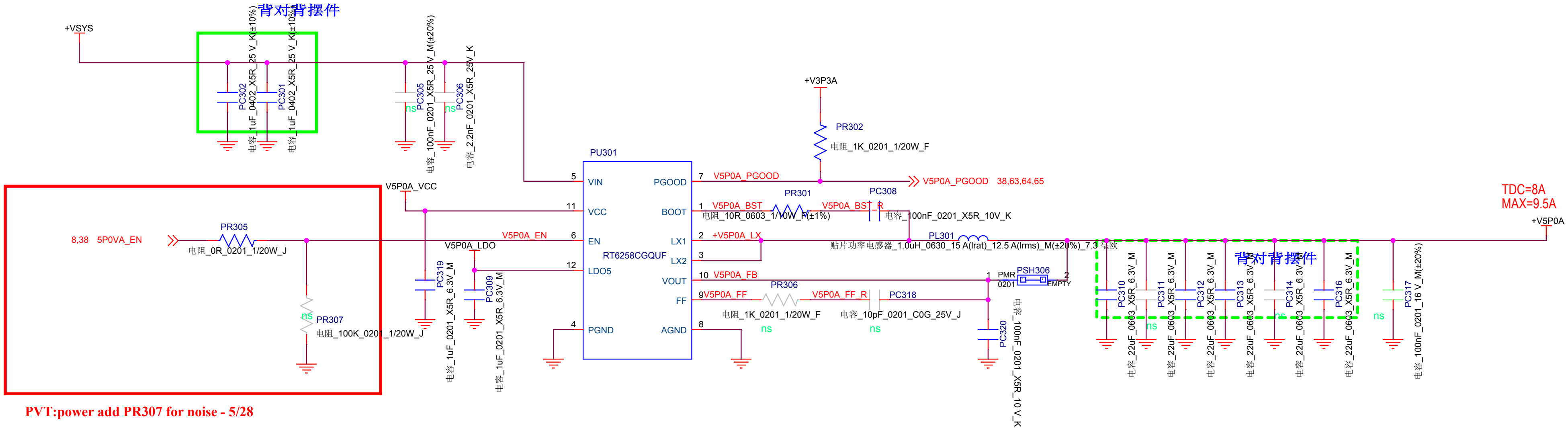
Page name:	POWER DELIVERY 5V 3.3V	
Size: A4	Project Name: ICELAKE	REV: V1.0
Date: Monday, July 15, 2019	Sheet: 61	of 72



PVT:power add PR307 for noise - 5/28

Huaqin Telecom Technology Com.,Ltd.

Page name: **POWER DELIVERY IMVP**

Size: A4
Project Name: **ICELAKE**
REV: V1.0

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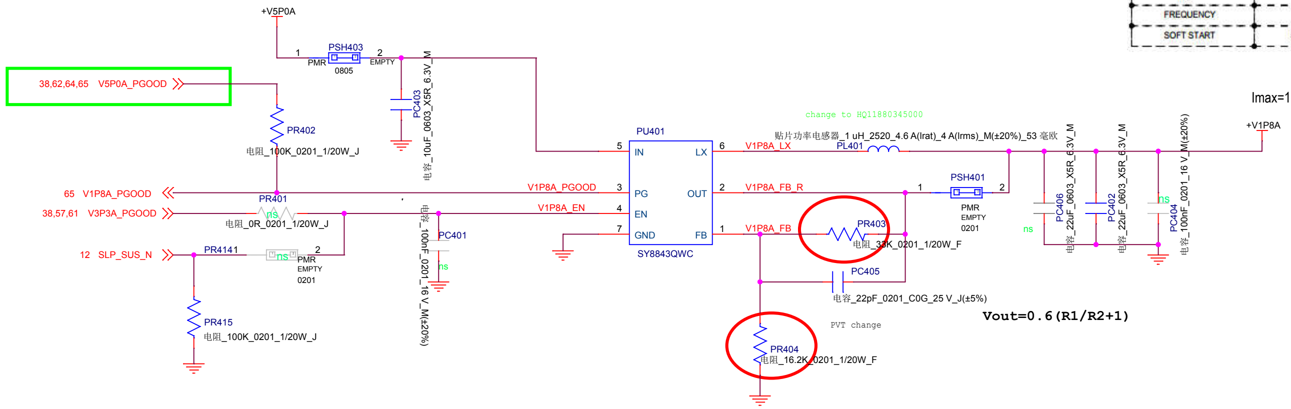
+V1P8A

PARAMETER	SETTING
OUTPUT VOLTAGE	1.8V
LOAD CURRENT	3 A
OCP	3.75 A
FREQUENCY	1 MHZ
SOFT START	500 U SEC



Imax=1.5A

Vout=0.6(R1/R2+1)

Huaqin Telecom Technology Com.,Ltd.	
Page name:	POWER DELIVERY 1.8V & 1.0
Size: A4	Project Name: ICE LAKE
REV:	V1.0
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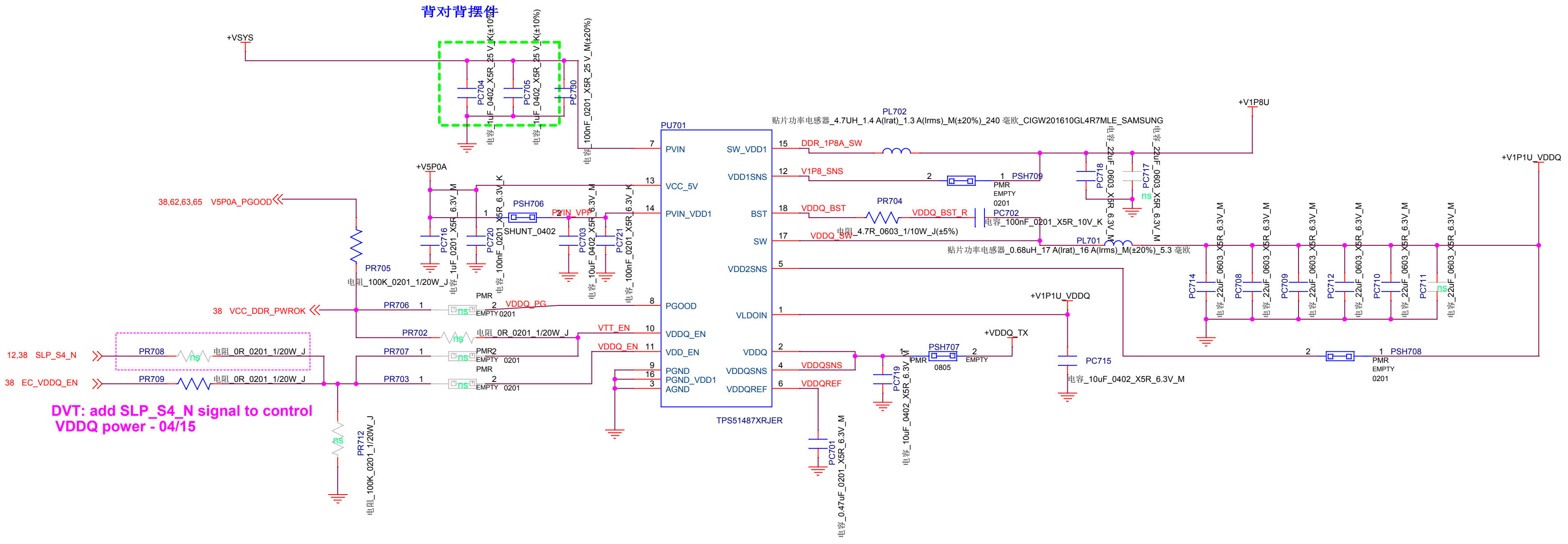

Huaqin Telecom Technology Com.,Ltd.

Page name: **BLANK**

Size: A4

Project Name: **NB8511**

REV: V1.0

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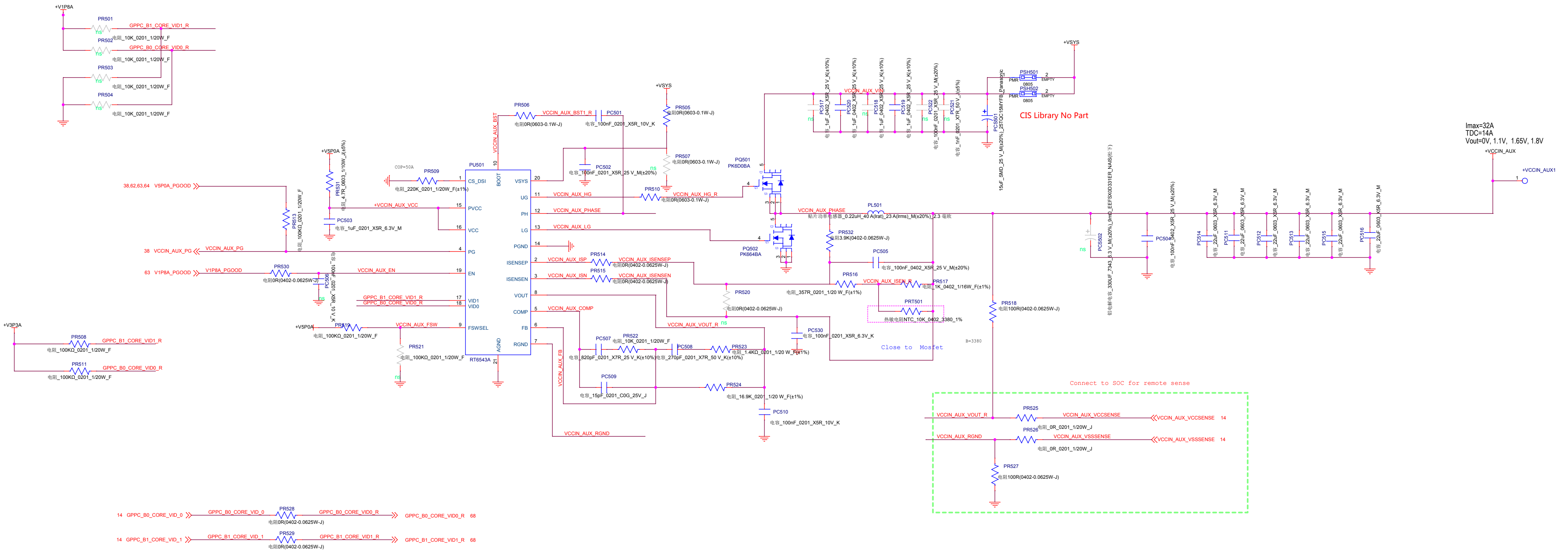

Huaqin Telecom Technology Com.,Ltd.

Page name: **POWER DELIVERY VCCIN_AUX**

Size: A4 **Project Name:** **ICELAKE** **REV:** V1.0

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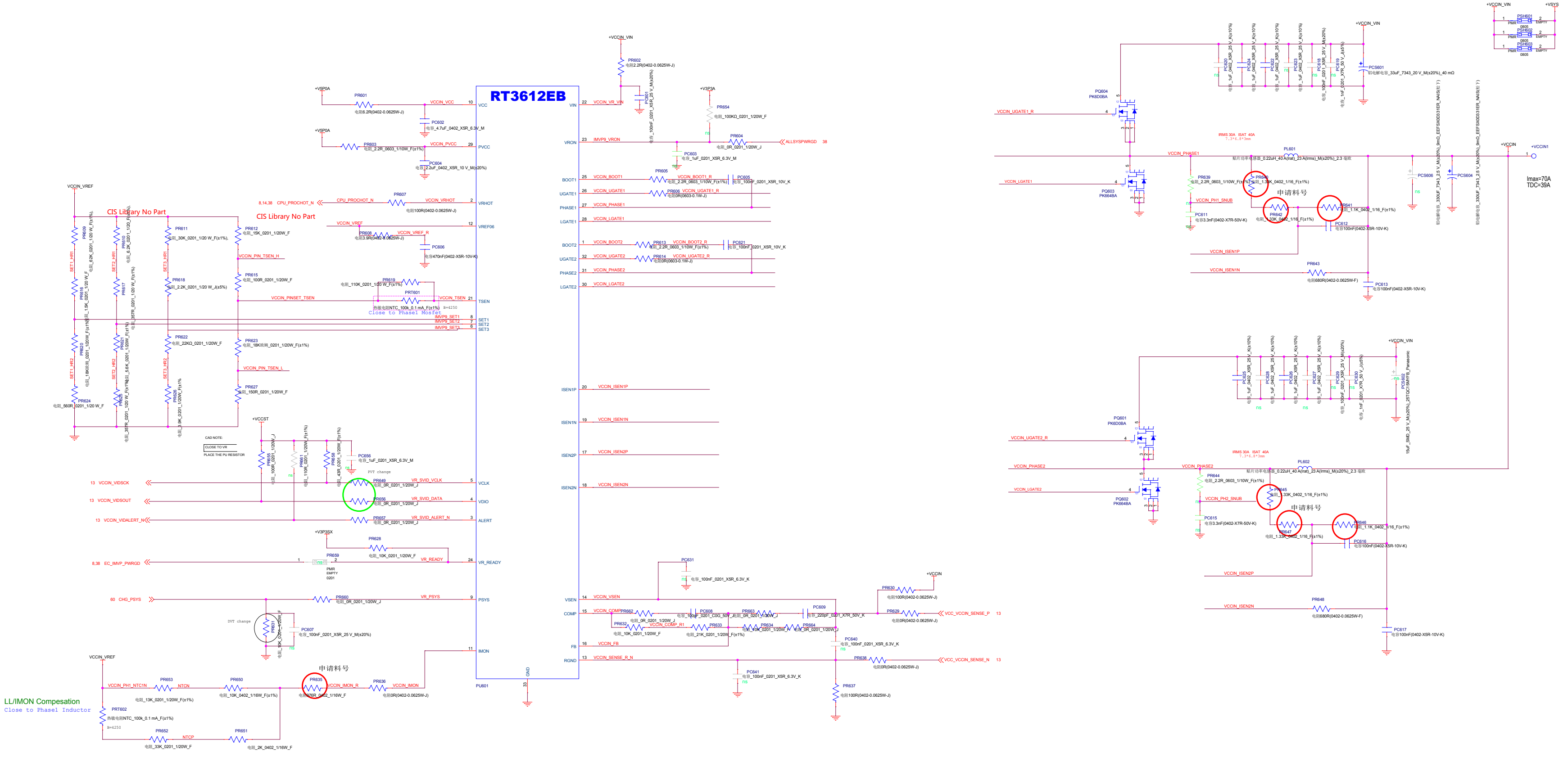

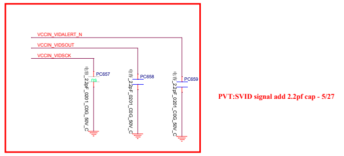

PIN SETTING	FUNCTION1	FUNCTION2	FUNCTION3
SET1	EN_LV_HIGHZ 1.6 - 2.2 V	VBOOT 1.8V	ICCMAX 80A
SET2	ANTIOVS_TH 0.15V	AI GAIN 0.25	NA
SET3	QR_TH DISABLE	NA	NA
TSEN	0 LL DISABLE	DVID_LIFT DISABLE	VR_HOT @ 100DEG

Huaqin Telecom Technology Com.,Ltd.
Page name: POWER DELIVERY IMVP
Size: A4
Project Name: ICELAKE
REV: V1.0
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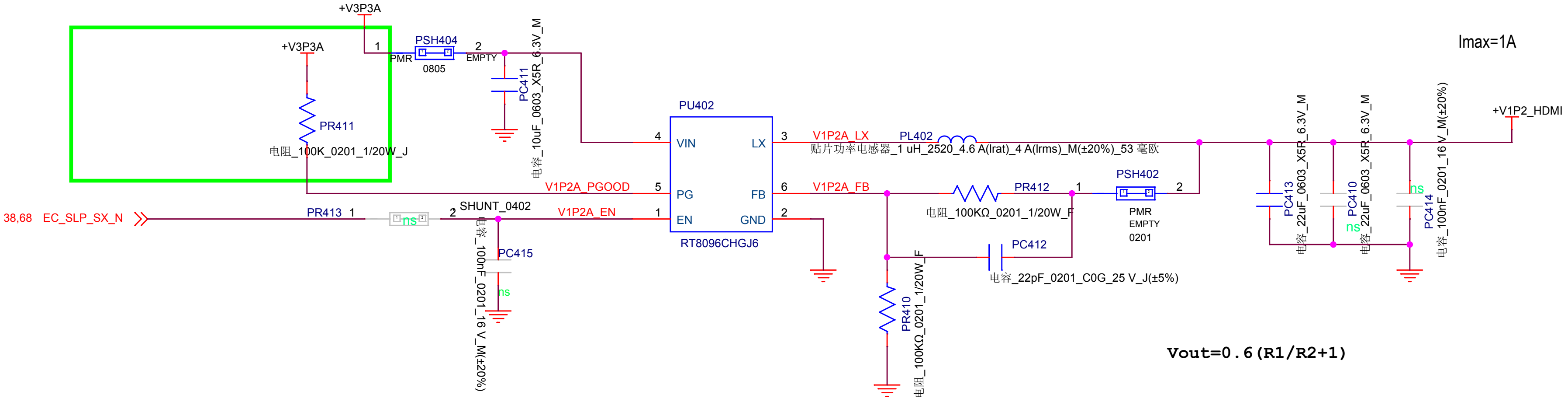

Huaqin Telecom Technology Com.,Ltd.

Page name: **Hole & Mark**

Size: A4
Project Name: **ICL-U42**
REV: V1.0

Date: Monday, July 15, 2019
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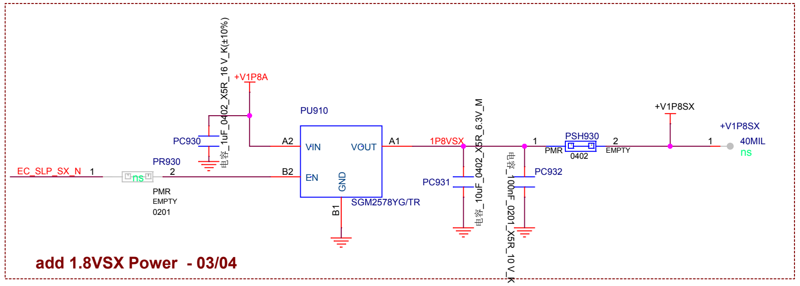
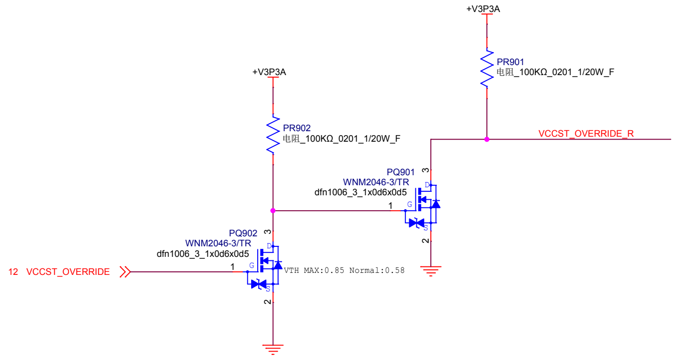
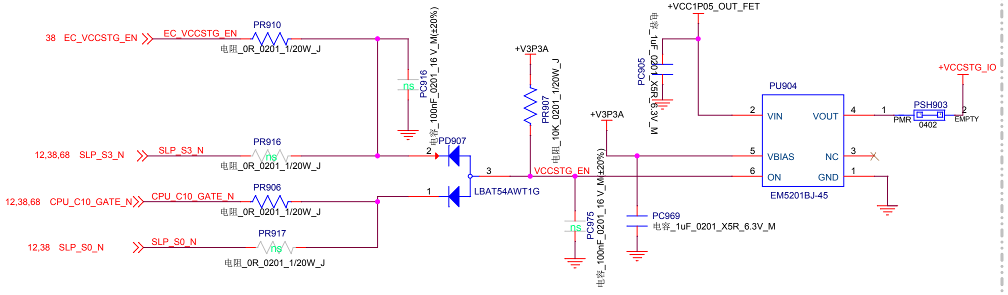
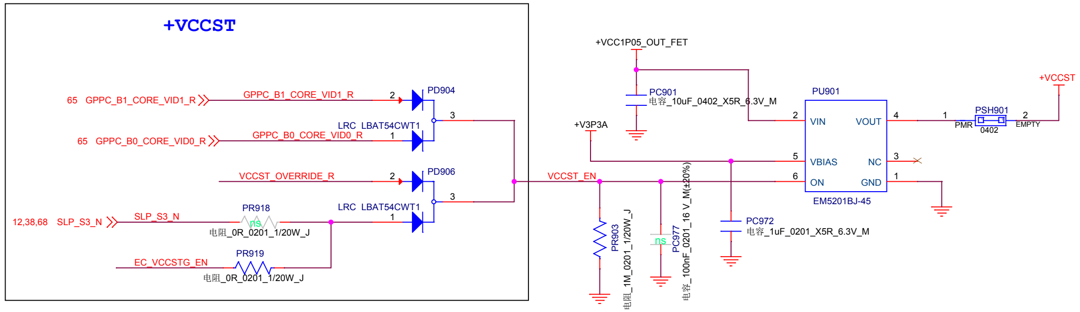




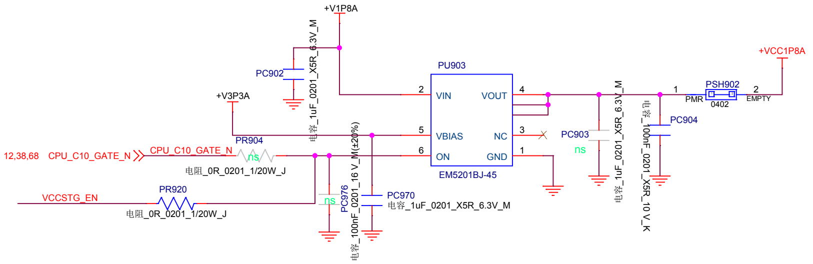
+VCCSTG_IO



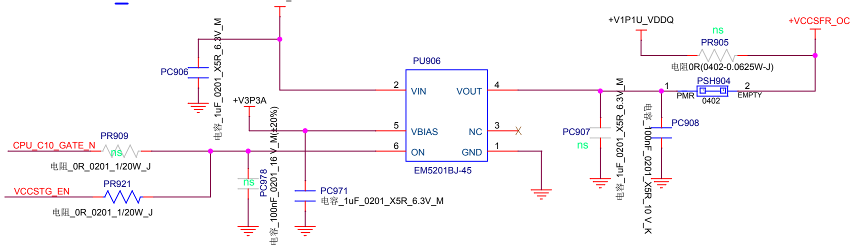
+VCCST



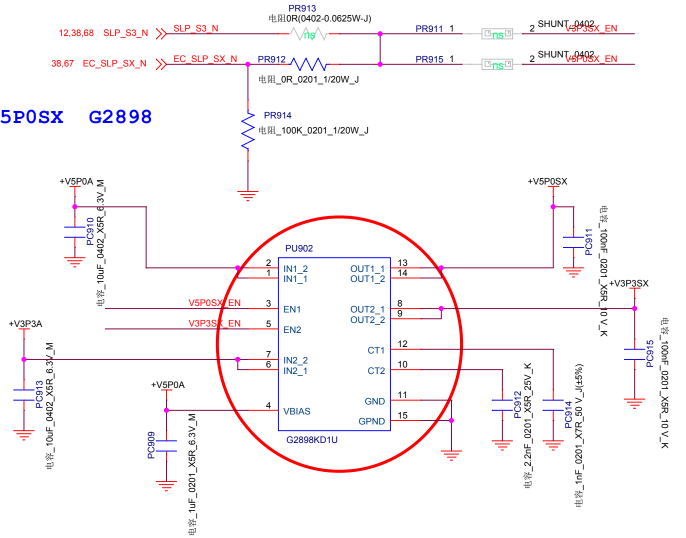
+VCC1P8A



+VCCSFR_OC



+V3P3SX,+V5P0SX G2898



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Page name: LOAD SWITCH

Size: A4 | Project Name: ICELAKE | REV: V1.0

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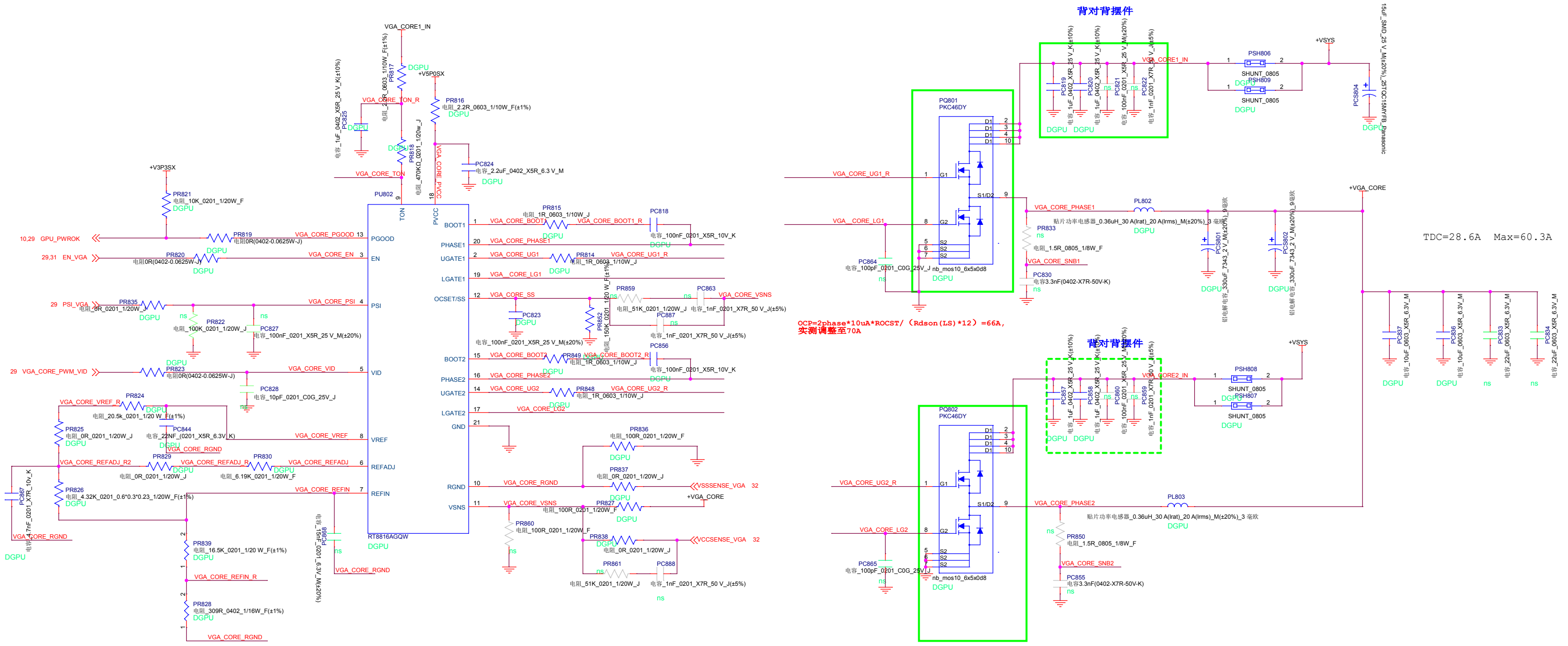

OCP=2phase*10uA*ROCST/（Rdson(LS)*12）=66A,
实测调整至70A

TDC=28.6A Max=60.3A

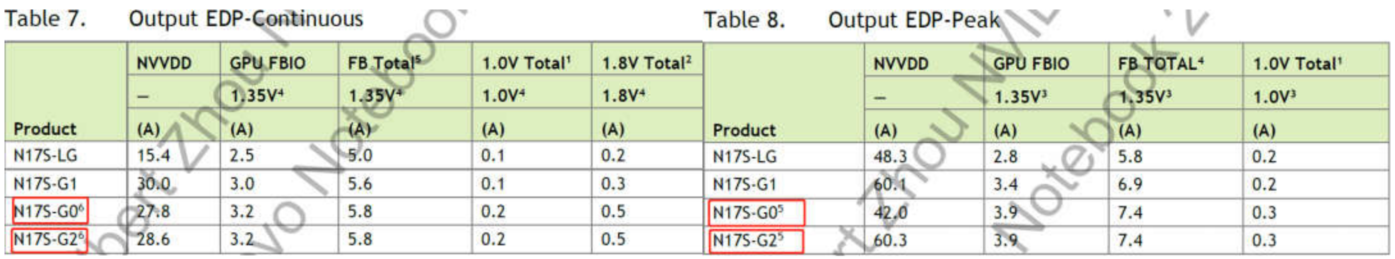

Table 7. Output EDP-Continuous

Product	NVVDD	GPU FBIO	FB Total[5]	1.0V Total[1]	1.8V Total[2]
	–	1.35V[4]	1.35V[4]	1.0V[4]	1.8V[4]
	(A)	(A)	(A)	(A)	(A)
N17S-LG	15.4	2.5	5.0	0.1	0.2
N17S-G1	30.0	3.0	5.6	0.1	0.3
N17S-G0[6]	27.8	3.2	5.8	0.2	0.5
N17S-G2[6]	28.6	3.2	5.8	0.2	0.5

Table 8. Output EDP-Peak

Product	NVVDD	GPU FBIO	FB TOTAL[4]	1.0V Total[1]
	–	1.35V[3]	1.35V[3]	1.0V[3]
	(A)	(A)	(A)	(A)
N17S-LG	48.3	2.8	5.8	0.2
N17S-G1	60.1	3.4	6.9	0.2
N17S-G0[5]	42.0	3.9	7.4	0.3
N17S-G2[5]	60.3	3.9	7.4	0.3

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Page name: POWER DELIVERY-GPU Core
Size: A4
Project Name: NB8511
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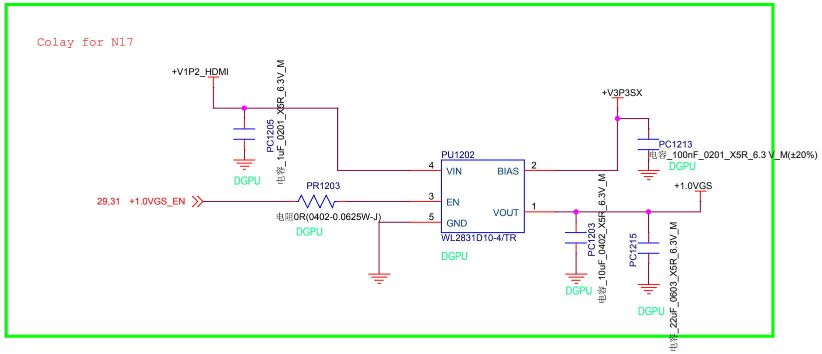

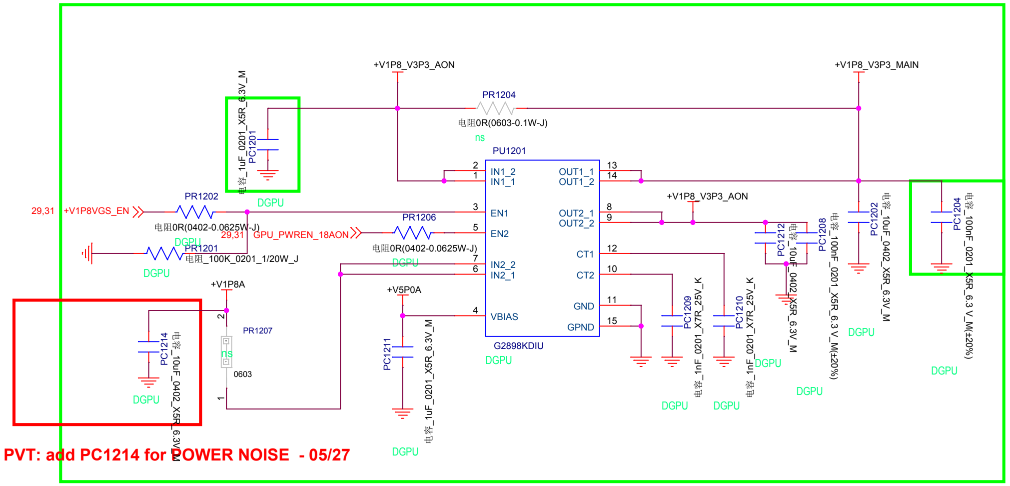

PVT: add PC1214 for POWER NOISE - 05/27

Huaqin Telecom Technology Com.,Ltd.

Page name: **POWER DELIVERY_1.0VGS&1.8VGS**

Size: A4
Project Name: **NB8511**
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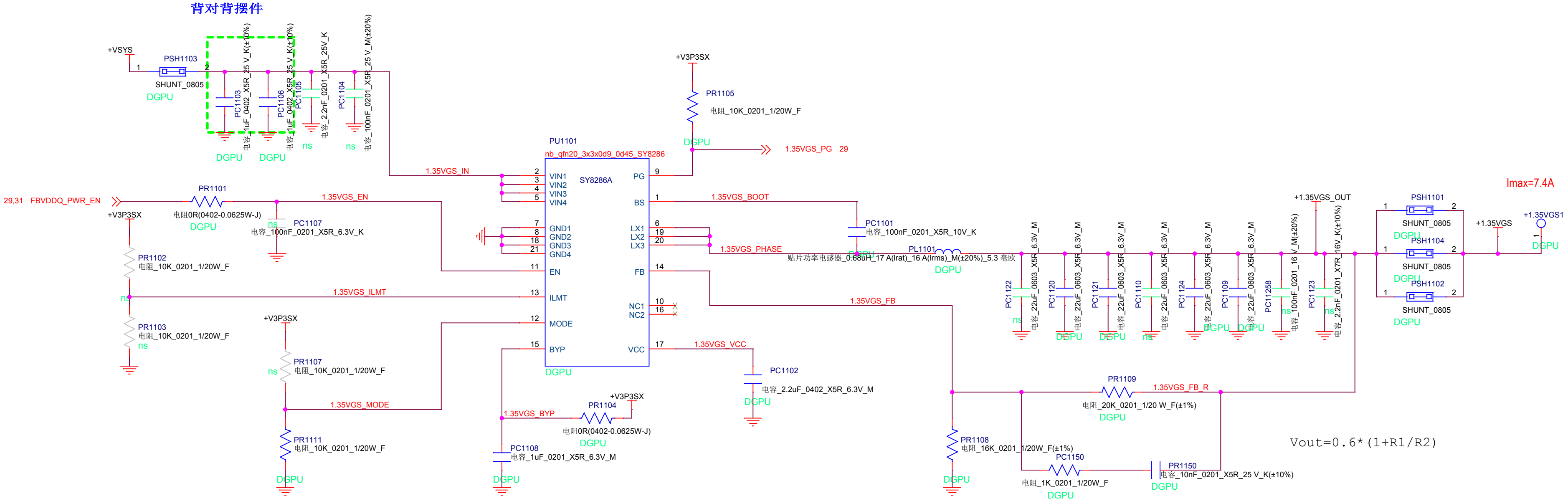

Imax=7.4A

Vout=0.6*(1+R1/R2)

stuff reduce S0 power consumption 11/5

PR1150:0Ω-10kΩ
PC1150:100pF-1nF 11/5

ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A

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Page name: POWER DELIVERY_1.35VGS
Size: A4
Project Name: NB8511
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5 4 3 2 1

D

C

B

A

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Page name:	**BLANK**	
Size: A4	**Project Name:** **NB8511**	**REV:** V1.0
Date:	Monday, July 15, 2019	**Sheet:** 72 **of** 72

5 4 3 2 1