

Compal Confidential

NTV00

LA-5661 Rev 1.0 Schematics

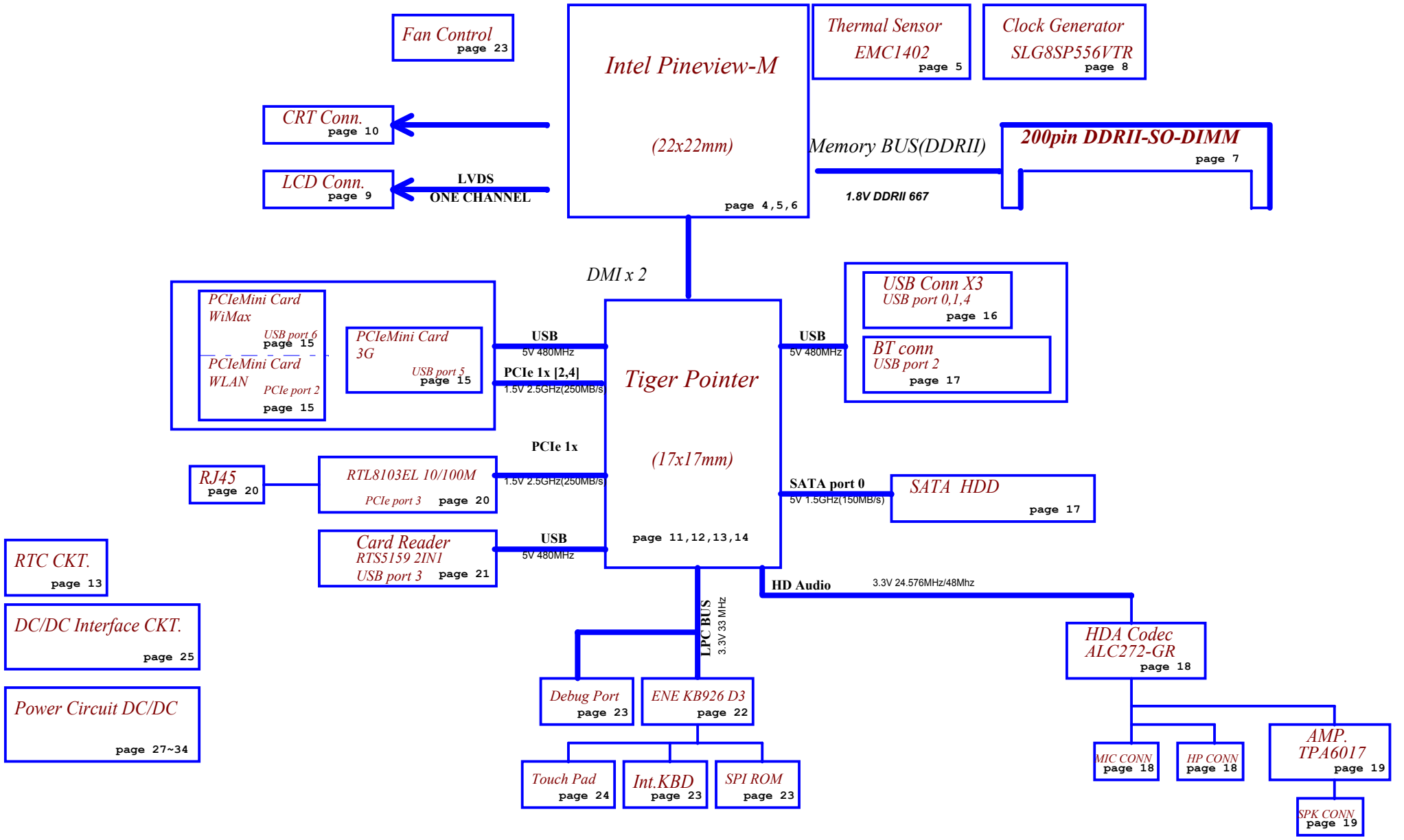
Intel PineView Processor/ Tiger point

2010-01-07 REV : 1.0

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				Size Custom	Document Number NTV00 LA5661P M/B
				Date Thursday, January 07, 2010	Rev 1.0
				Sheet	1 of 35

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Model Name : NTV00
File Name : LA-5661P



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				NTV00 LA5661P M/B	
				Date	Thursday, January 07, 2010
				Sheet	2 of 35
				Rev	1.0

Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.89VS	0.89VS GFX support voltage	ON	OFF	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	VCCP switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BTO Option Table

Function	Mini PCI-E SLOT				STAR			
description								
explain	Wi-Fi	WiMax	3G		POWER SAVING			
BTO	WLAN@	WIMAX@	3G@		STAR@			

Function			
description			
explain			
BTO			

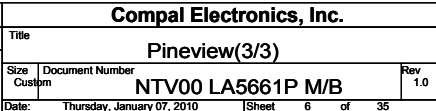
EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 010X b

EC SM Bus2 address

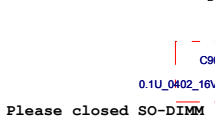
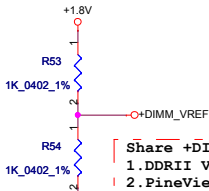
Tiger point SM Bus address

Device	Address
Clock Generator (SLG8SP56VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

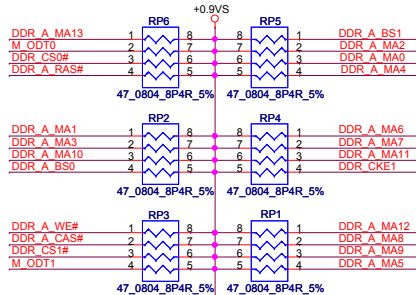
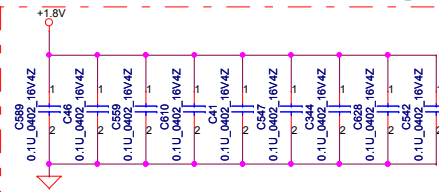
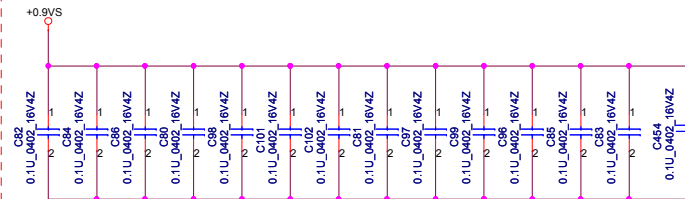
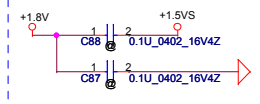


4 DDR_A_DQS#[0..7]
4 DDR_A_D[0..63]
4 DDR_A_DM[0..7]
4 DDR_A_DQS[0..7]
4 DDR_A_MA[0..14]

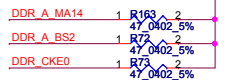
Layout Note:
Place near JDDR1



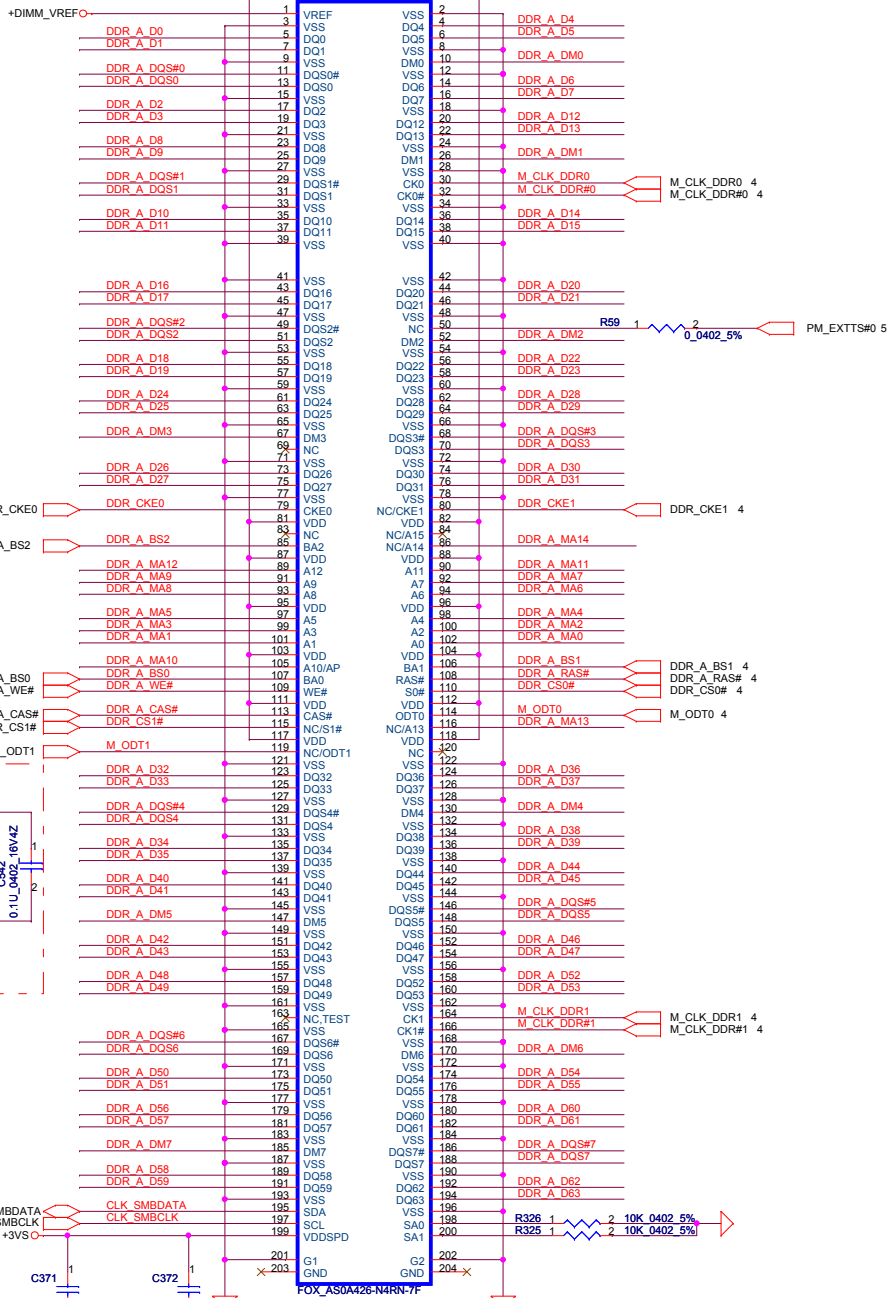
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely DIMMA, all trace length<1000 mil

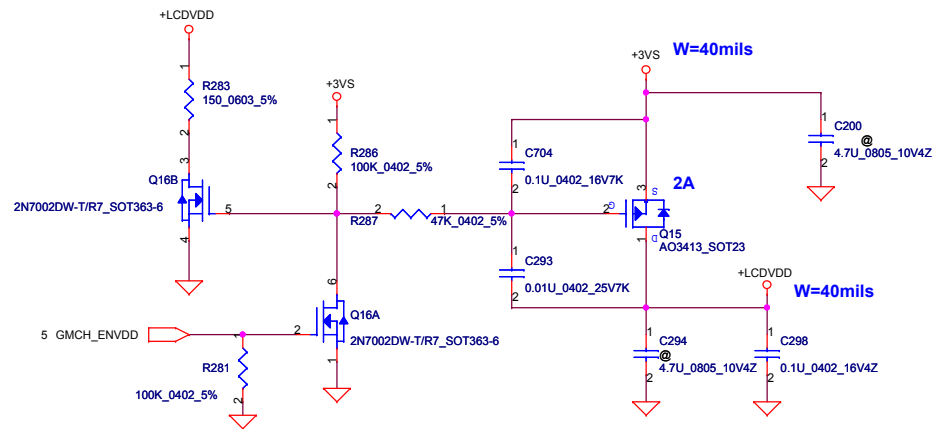


Layout Note:
Place these resistor closely DIMMA, all trace length Max=1000 mil



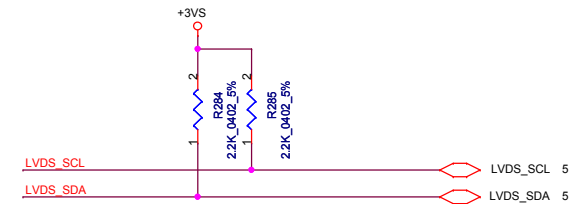
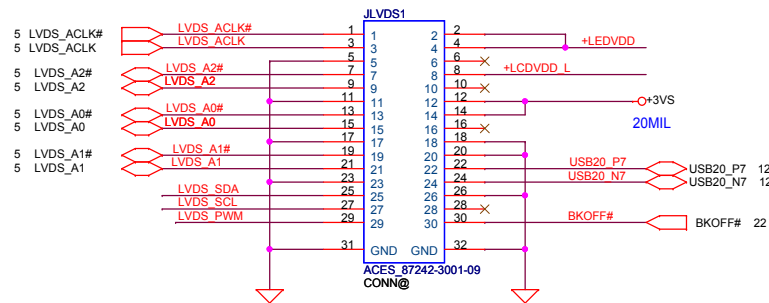
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				Deciphered Date				DDRII-SODIMMA			
				2010/11/10				Size Document Number			
								Custom			
								NTV00 LA5661P M/B			
								Date: Thursday, January 07, 2010			
								Sheet 7 of 35			
								Rev 1.0			

LCD POWER CIRCUIT

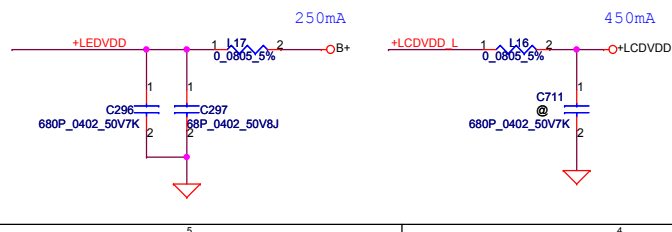
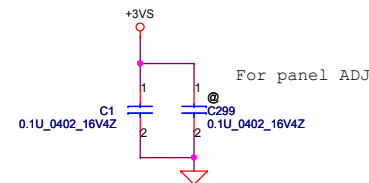
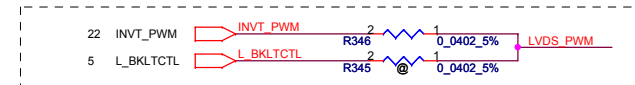


LED/PANEL BD. Conn.

Combine INT.CAMERA with
LVDS

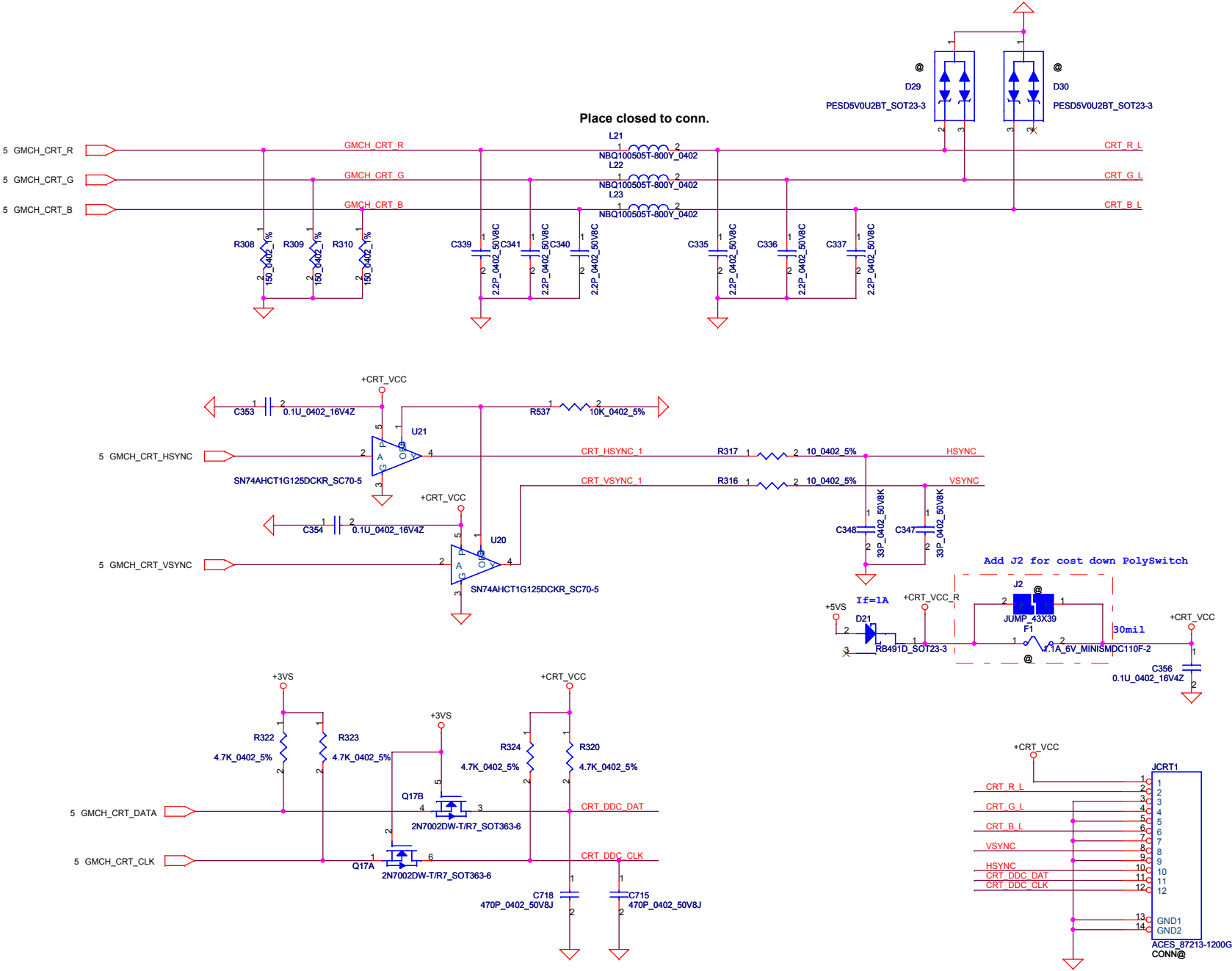


Option panel brightness control

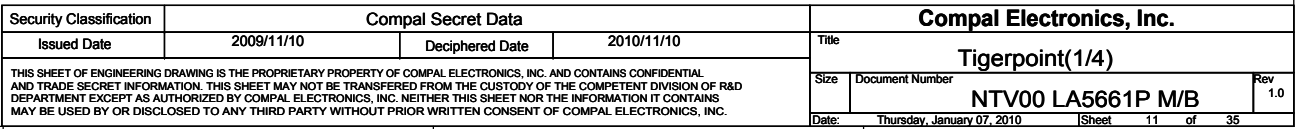


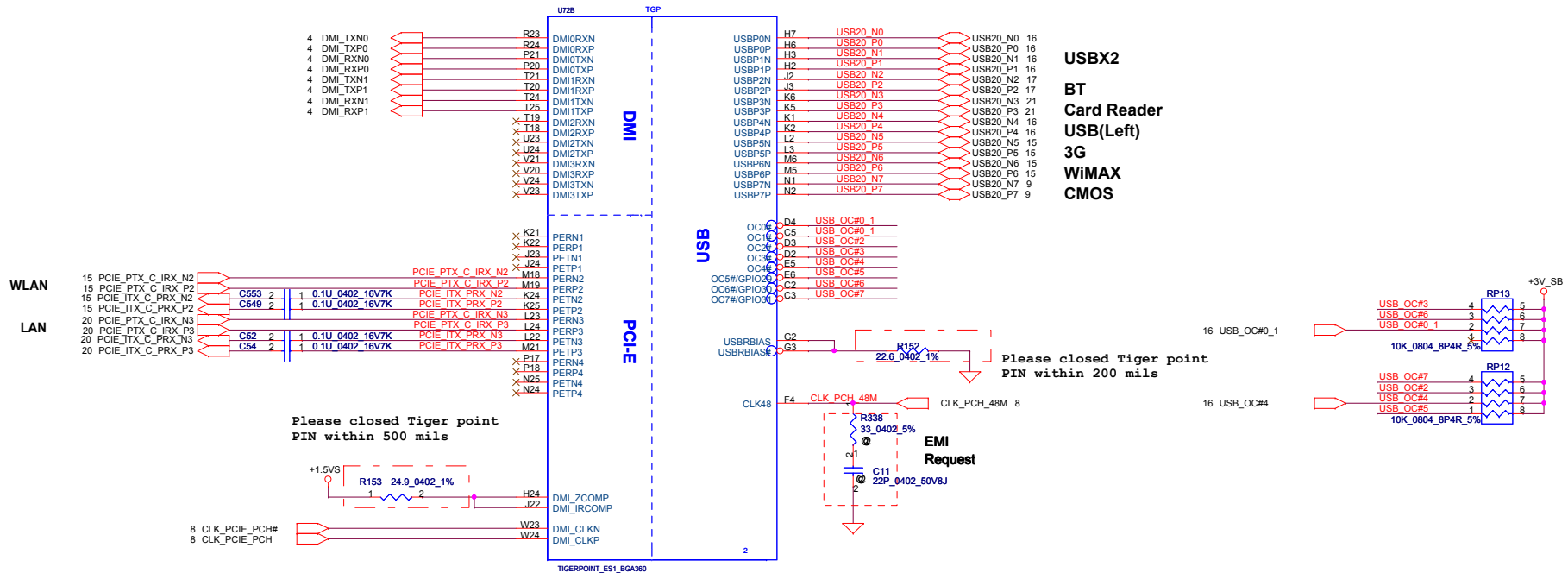
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				Size	Document Number	Rev	
				NTV00 LA5661P M/B		1.0	
				Date:	Thursday, January 07, 2010	Sheet	9 of 35

CRT CONNECTOR

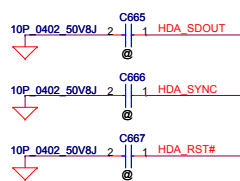
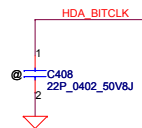
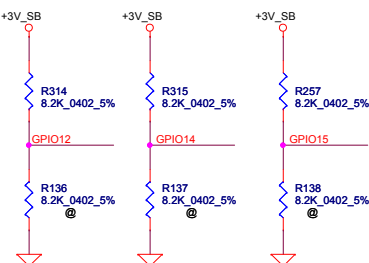
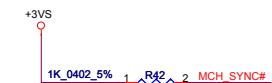
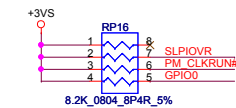
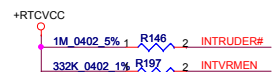
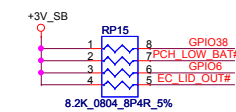
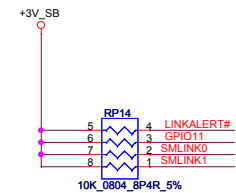
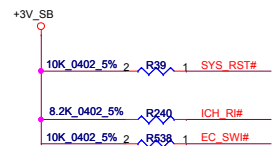
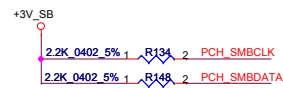


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Date	Thursday, January 07, 2010	Sheet	10	of	35

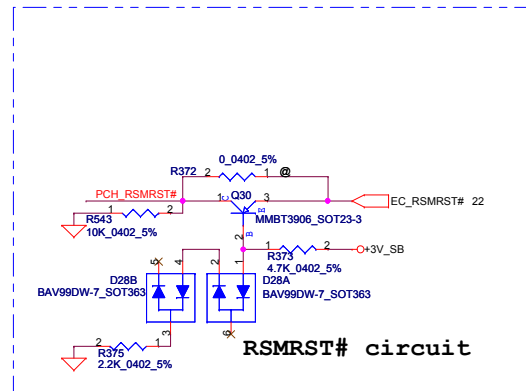
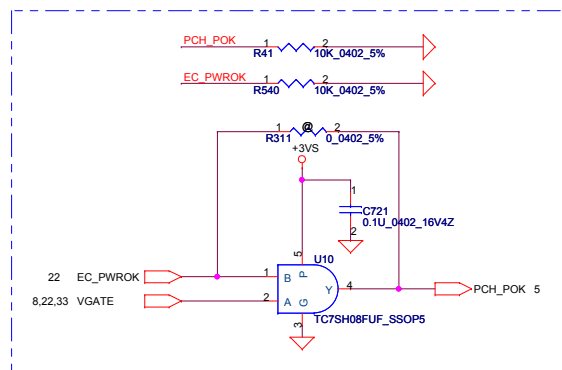
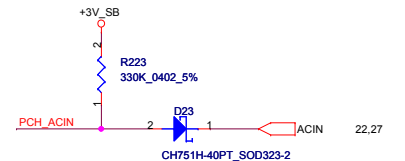
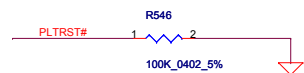
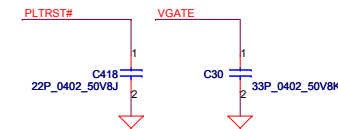
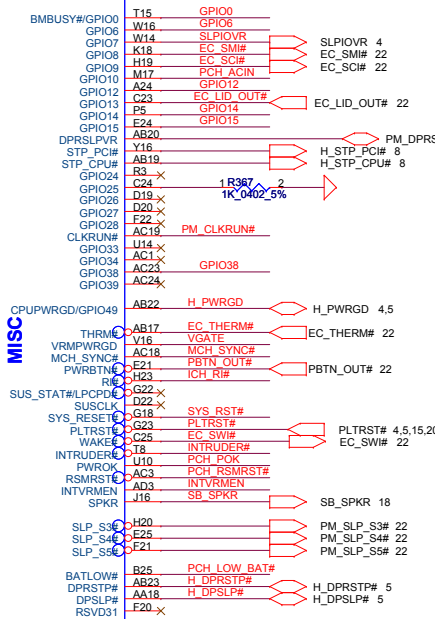
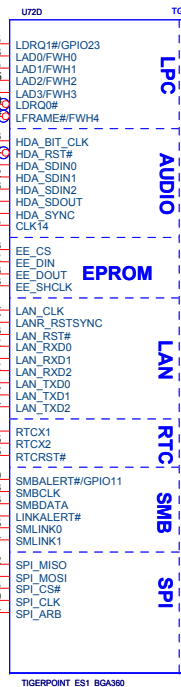
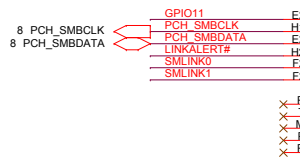
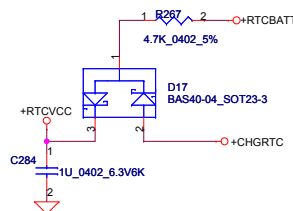
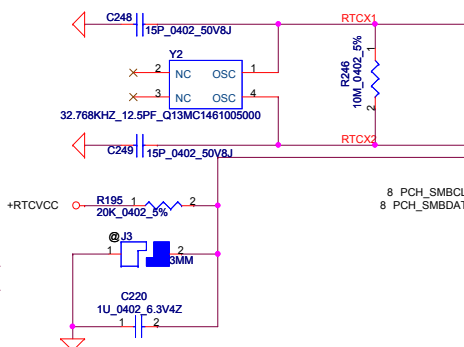




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				Custom	NTV00 LA5661P M/B
				Date	Thursday, January 07, 2010
				Sheet	12 of 35
				Rev	1.0

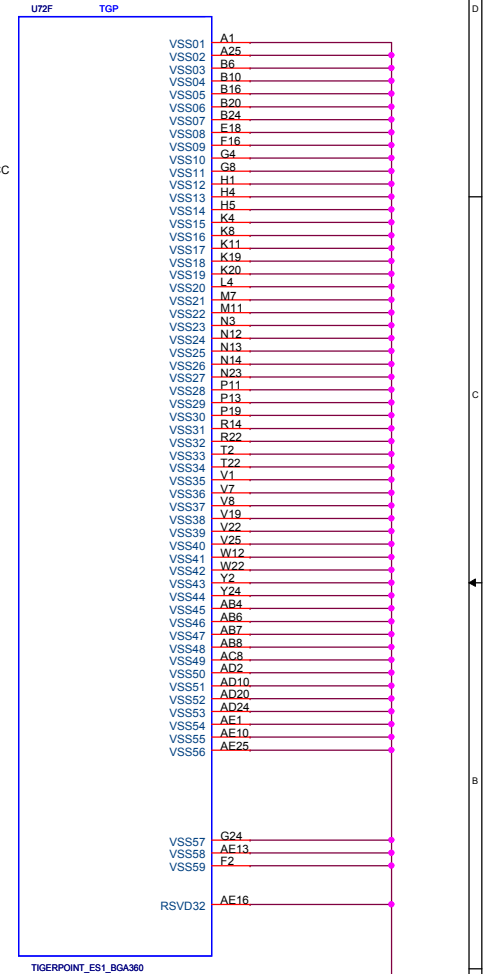
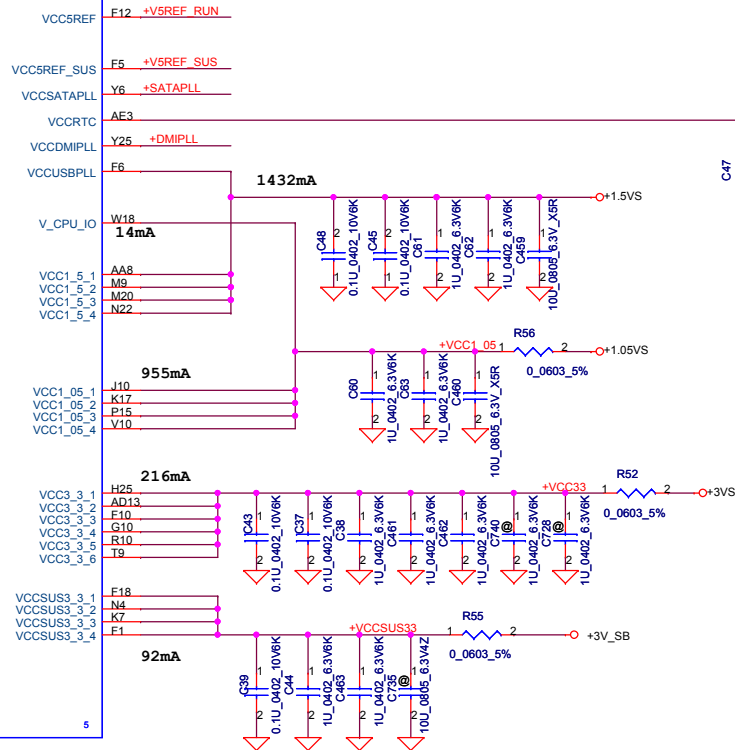
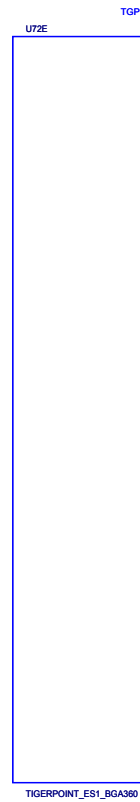
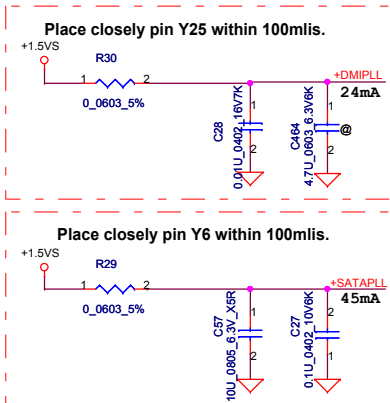
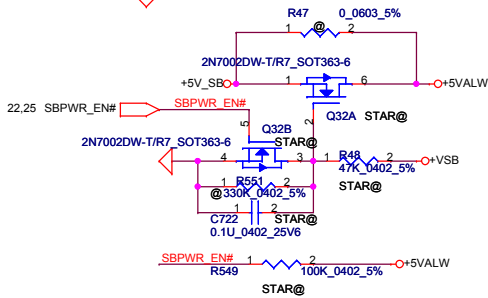
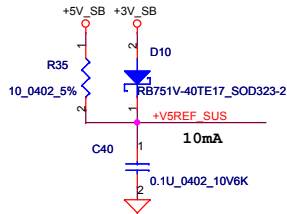
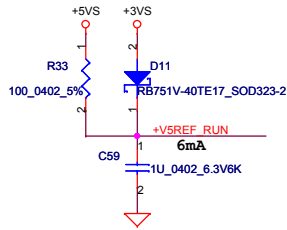


For EMI, Close to TigerPoint



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Title		Size		Rev	
Document Number		13		1.0	
Date		Thursday, January 07, 2010		Sheet	
				of	
				35	

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Size	Custom	Document Number	NTV00 LA5661P M/B		Rev
Date:	Thursday, January 07, 2010	Sheet	14	of	35

The diagram illustrates the pin connections for the FOX AS06226-S40N-7F USB-C connector. It is divided into three main sections: WLAN/WiFi, USB, and other signals.

WLAN/WiFi Section:

- Power:** +3VS is connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, and 55. A 120 mΩ resistor is connected between pins 1 and 3.
- Signals:**
 - WLAN_BT_DATA (pin 17) connects to WLAN_BT_DATA.
 - WLAN_BT_CLK (pin 18) connects to WLAN_BT_CLK.
 - WLAN_CLKREQ# (pin 8) connects to WLAN_CLKREQ#.
 - CLK_PCIE_WLAN# (pin 8) connects to CLK_PCIE_WLAN#.
 - PCIE_PTX_C_IRRX_N2 (pin 12) connects to PCIE_PTX_C_IRRX_N2.
 - PCIE_PTX_C_IRRX_P2 (pin 12) connects to PCIE_PTX_C_IRRX_P2.
 - PCIE_ITX_C_PRX_N2 (pin 12) connects to PCIE_ITX_C_PRX_N2.
 - PCIE_ITX_C_PRX_P2 (pin 12) connects to PCIE_ITX_C_PRX_P2.
- Other:** A 3.3V regulator (R60, 0.0402 5%) is connected to pins 1, 2, and 3. A 100K 0402 5% resistor (R68) is connected to pin 1.

USB Section:

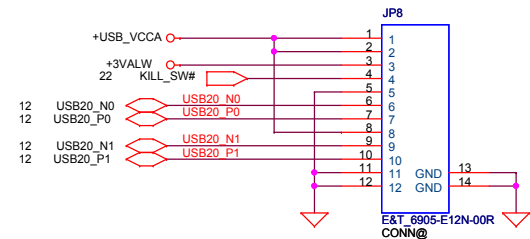
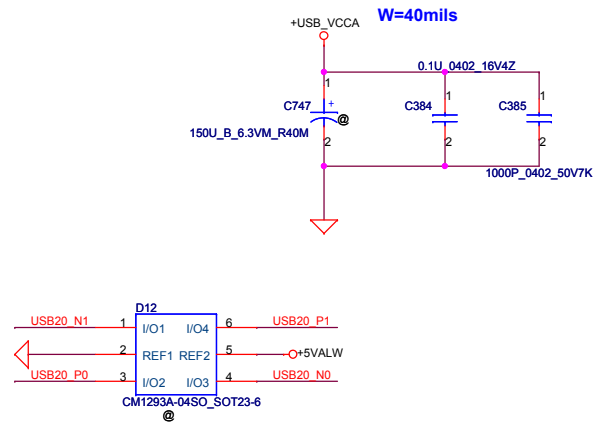
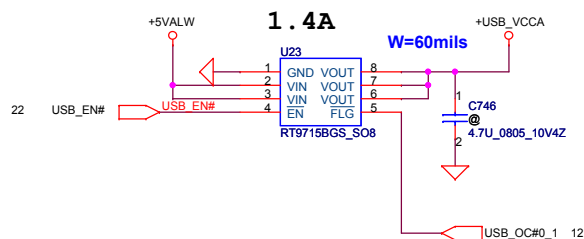
- Power:** +1.5VS is connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, and 55. A 120 mΩ resistor is connected between pins 1 and 3.
- Signals:**
 - WL_OFF# (pin 22) connects to WL_OFF#.
 - PLTRST# (pin 22) connects to PLTRST#.
 - CLK_SMBCLK (pin 7, 8) connects to CLK_SMBCLK.
 - CLK_SMBDATA (pin 7, 8) connects to CLK_SMBDATA.
 - USB20_N6 (pin 12) connects to USB20_N6.
 - USB20_P6 (pin 12) connects to USB20_P6.
 - WLAN_LED#_MO (pin 40) connects to WLAN_LED#_MO.
- Other:** A 3.3V regulator (R418, 100K 0402 5%) is connected to pins 1, 2, and 3. A 100K 0402 5% resistor (R418) is connected to pin 1.

Other Signals:

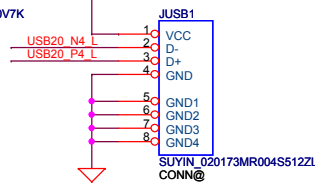
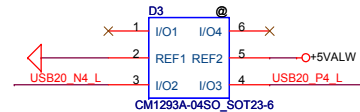
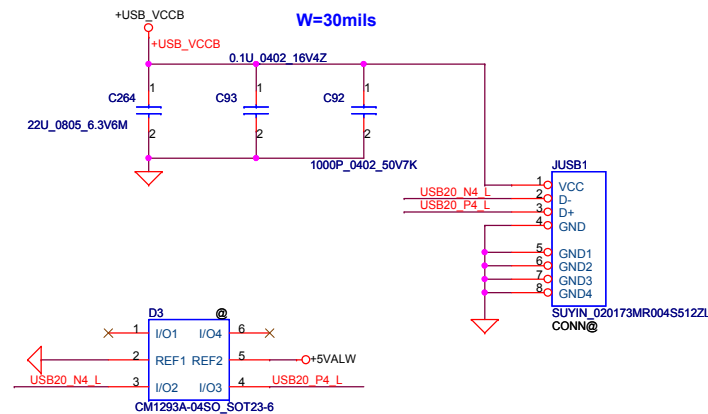
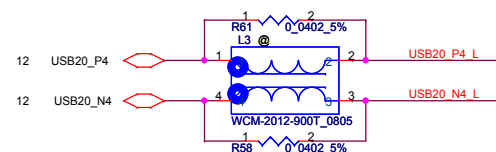
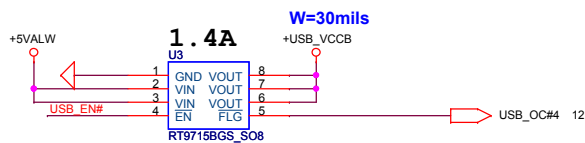
- TX_P80_DATA (pin 1) connects to TX_P80_DATA.
- C_RX_P80_CLK (pin 1) connects to C_RX_P80_CLK.
- Debug card using (pin 1) connects to Debug card using.
- 10P 0402 50VJ (pin 1) connects to 10P 0402 50VJ.
- 10P 0402 50VJ (pin 1) connects to 10P 0402 50VJ.

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				NTV00 LA5661P M/B		
				Date:	Thursday, January 07, 2010	Sheet 15 of 35

USB X2

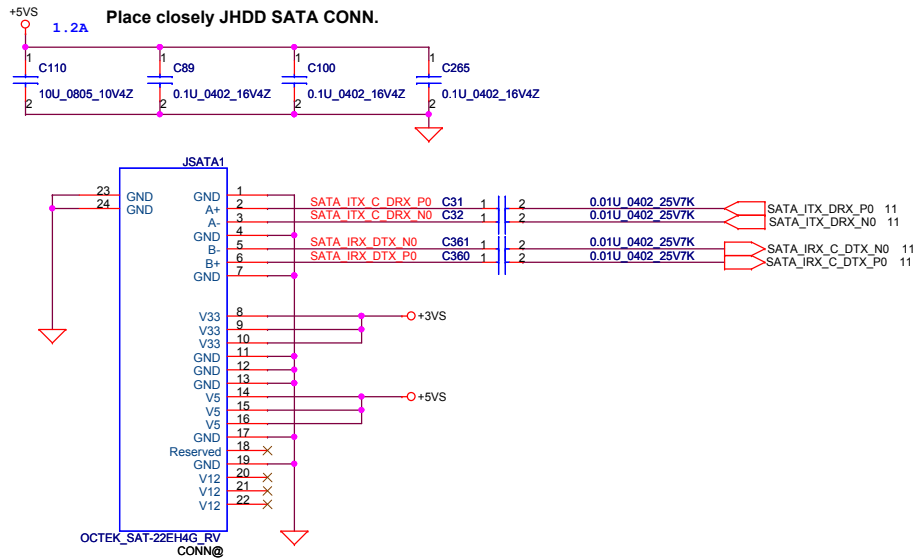


USB Board--Left

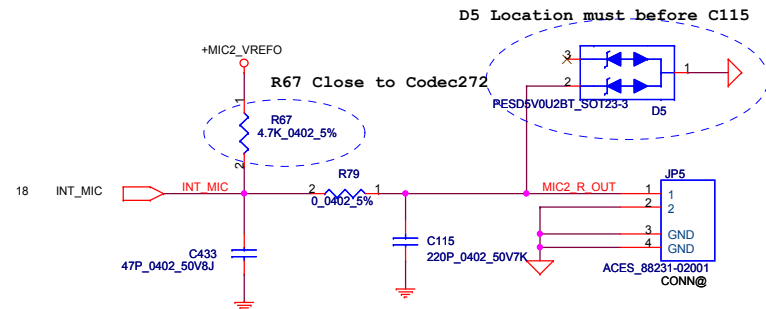
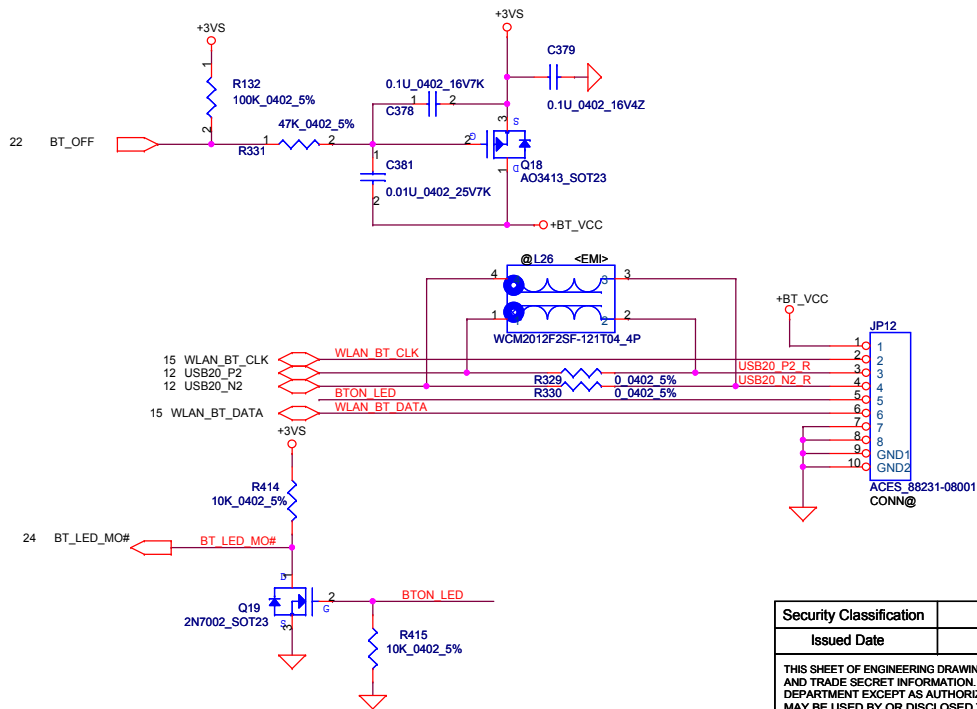


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						Size		Document Number		Rev	
								NTV00 LA5661P M/B		1.0	
						Date		Thursday, January 07, 2010		Sheet 16 of 35	

SATA Conn.

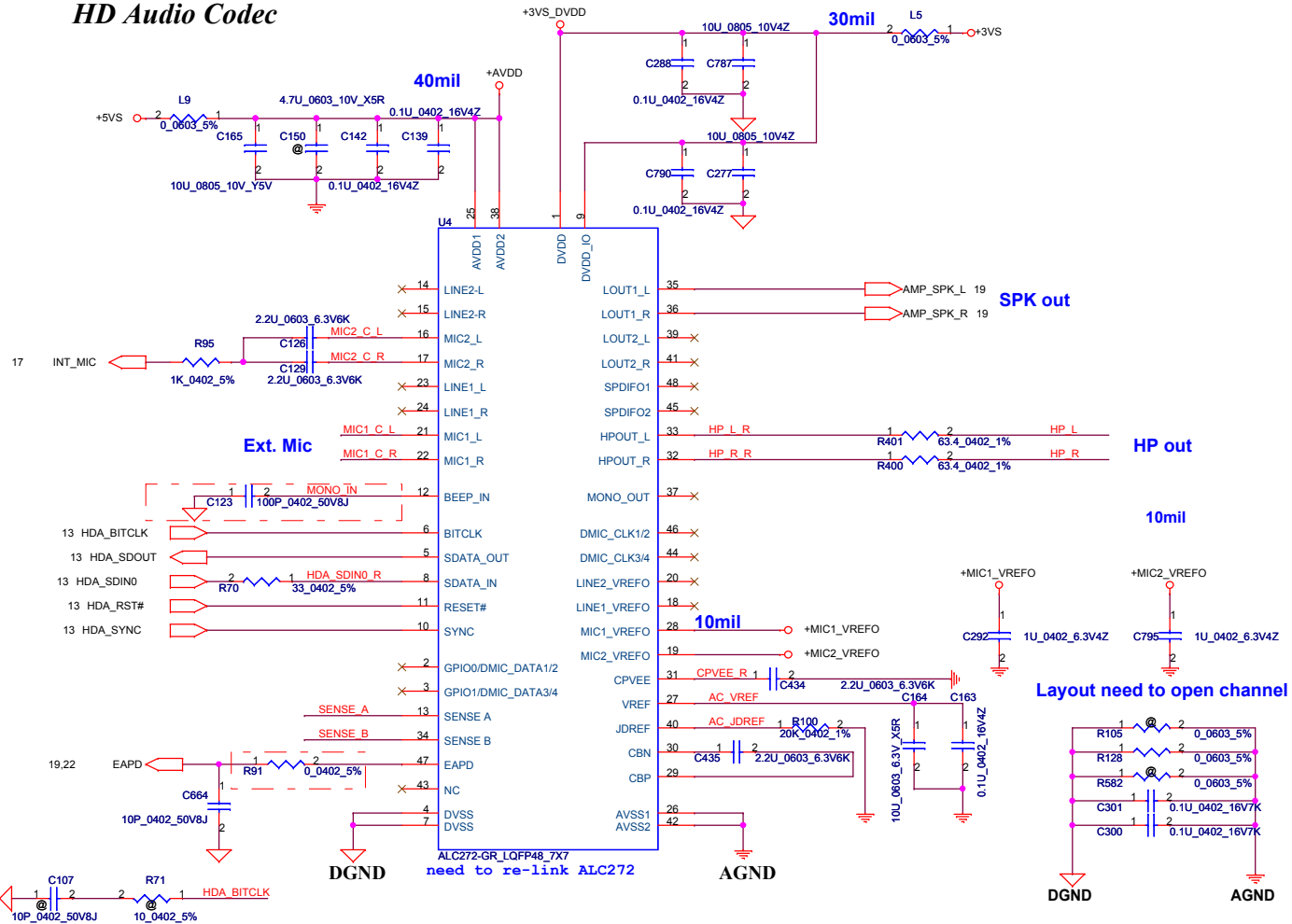


BlueTooth Interface



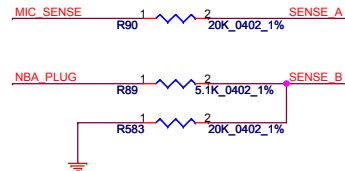
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
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						Size		Document Number		Rev	
						Custom		NTV00 LA5661P M/B		1.0	
						Date:		Thursday, January 07, 2010		Sheet 17 of 35	

HD Audio Codec



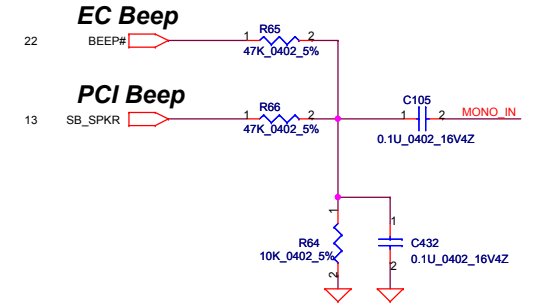
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	Headphone out

place close to chip

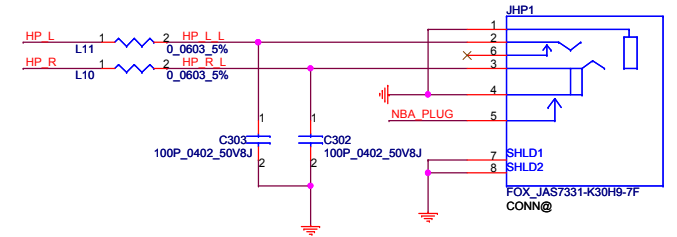


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				Custom	NTV00 LA5661P M/B	1.0
				Date:	Thursday, January 07, 2010	Sheet 18 of 35

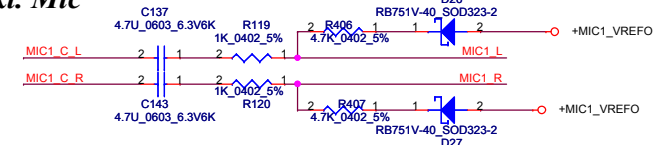
Beep sound



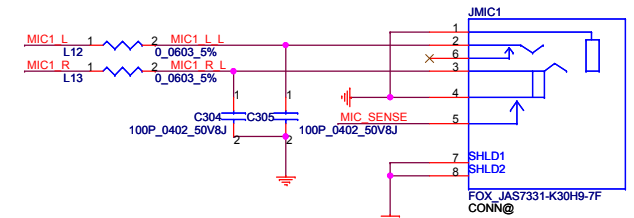
Head Phone JACK



Ext. Mic

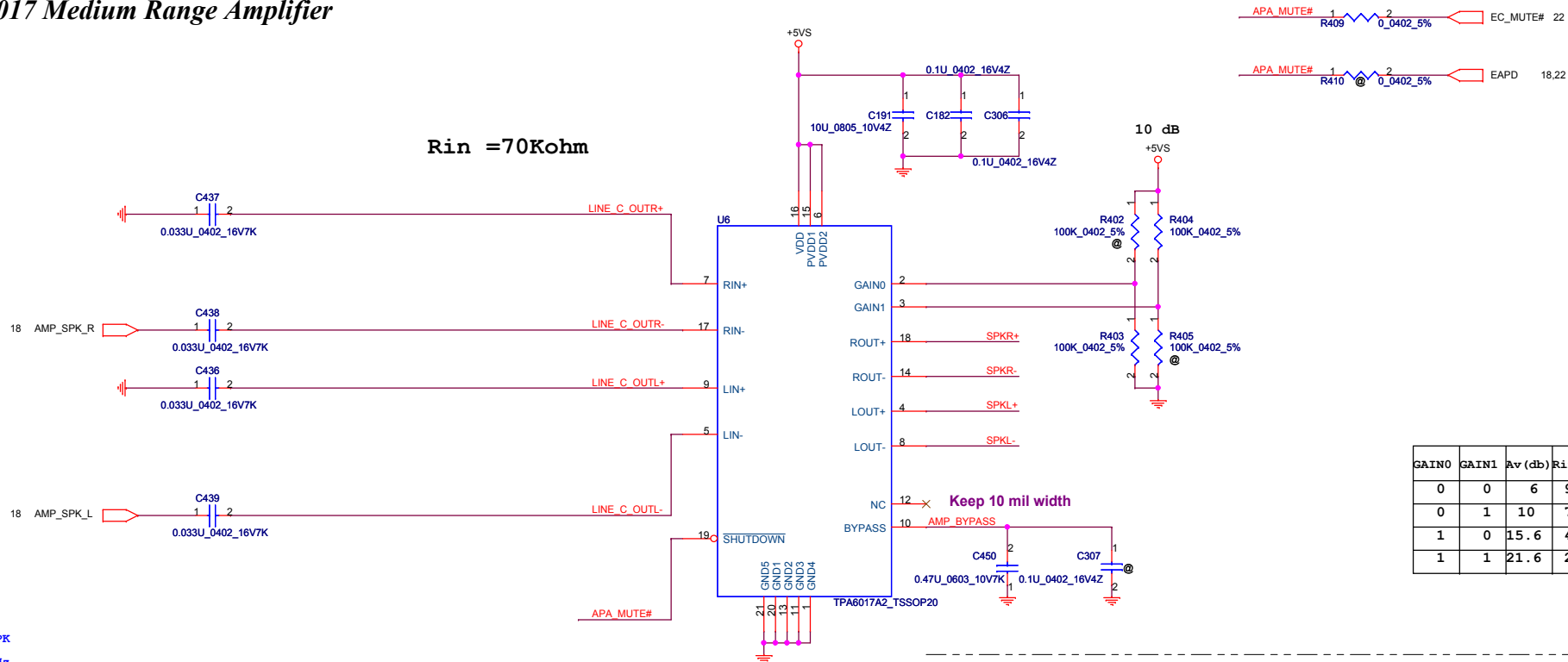


Ex.MIC JACK



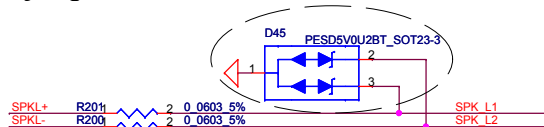
TPA6017 Medium Range Amplifier

Rin =70Kohm



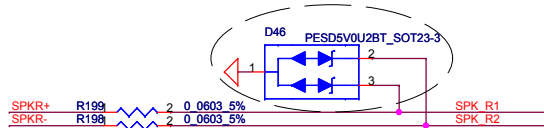
Use mono SPK
setting 68Hz
F=1/2nRC --> -3db
C=0.033U, R=70K, F=68Hz

Left Speaker Connector

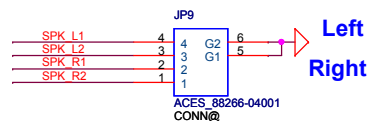


7/3 Change to SCA00000T00 for ESD request

Right Speaker Connector

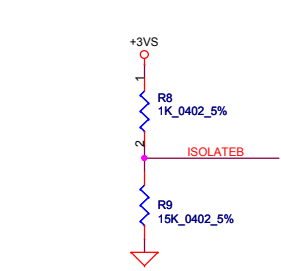
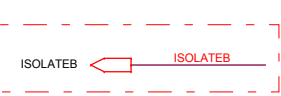
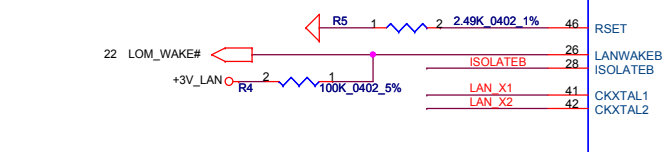
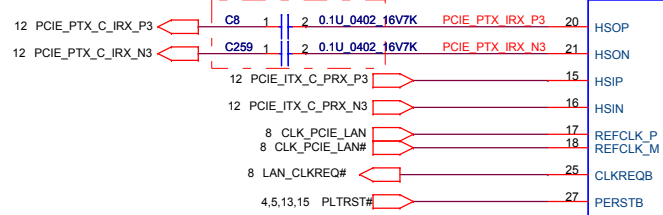


7/3 Change to SCA00000T00 for ESD request

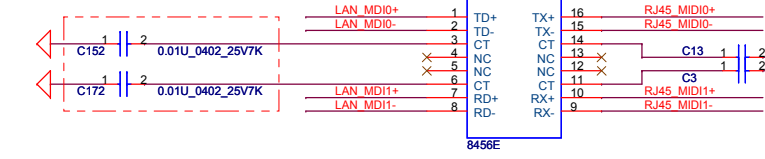


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						Size		Document Number		Rev	
						Custom		NTV00 LA5661P M/B		1.0	
						Date:		Thursday, January 07, 2010		Sheet 19 of 35	

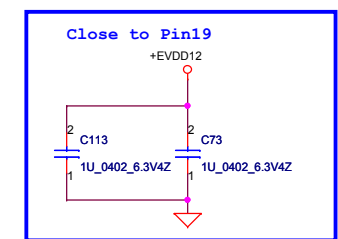
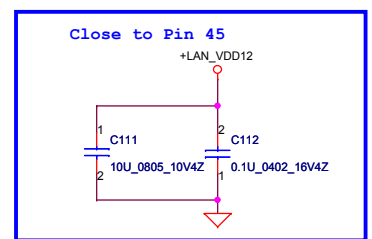
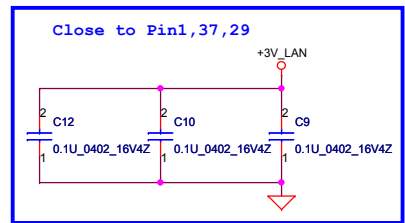
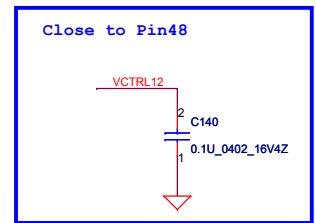
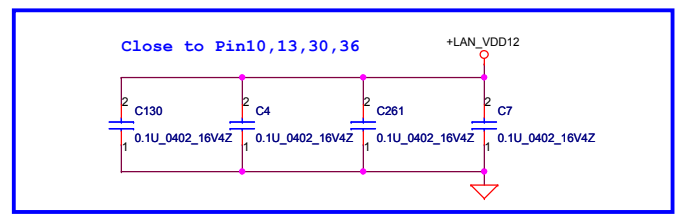
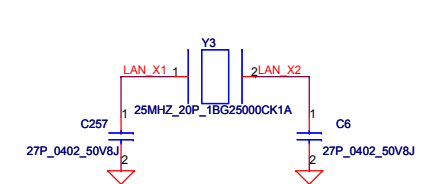
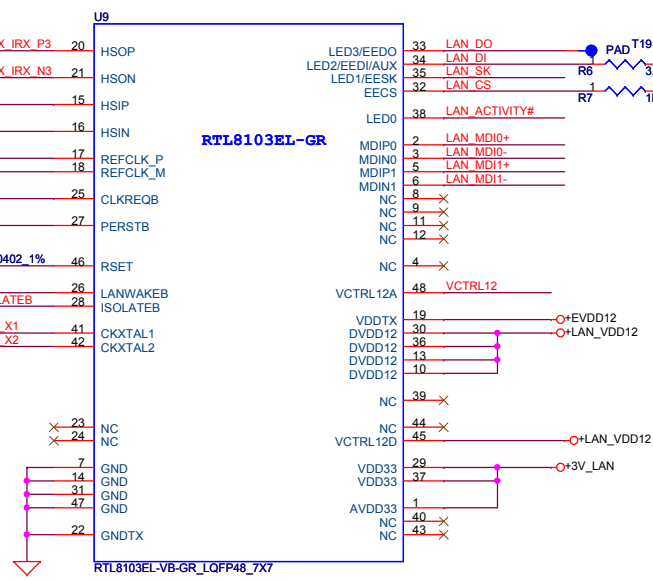
Place Close to Chip



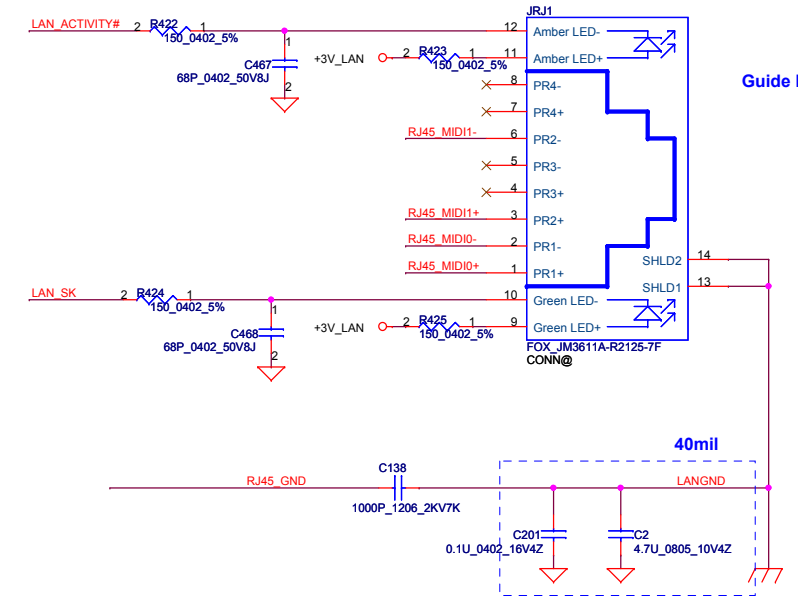
Place C152,C172 closed to T18



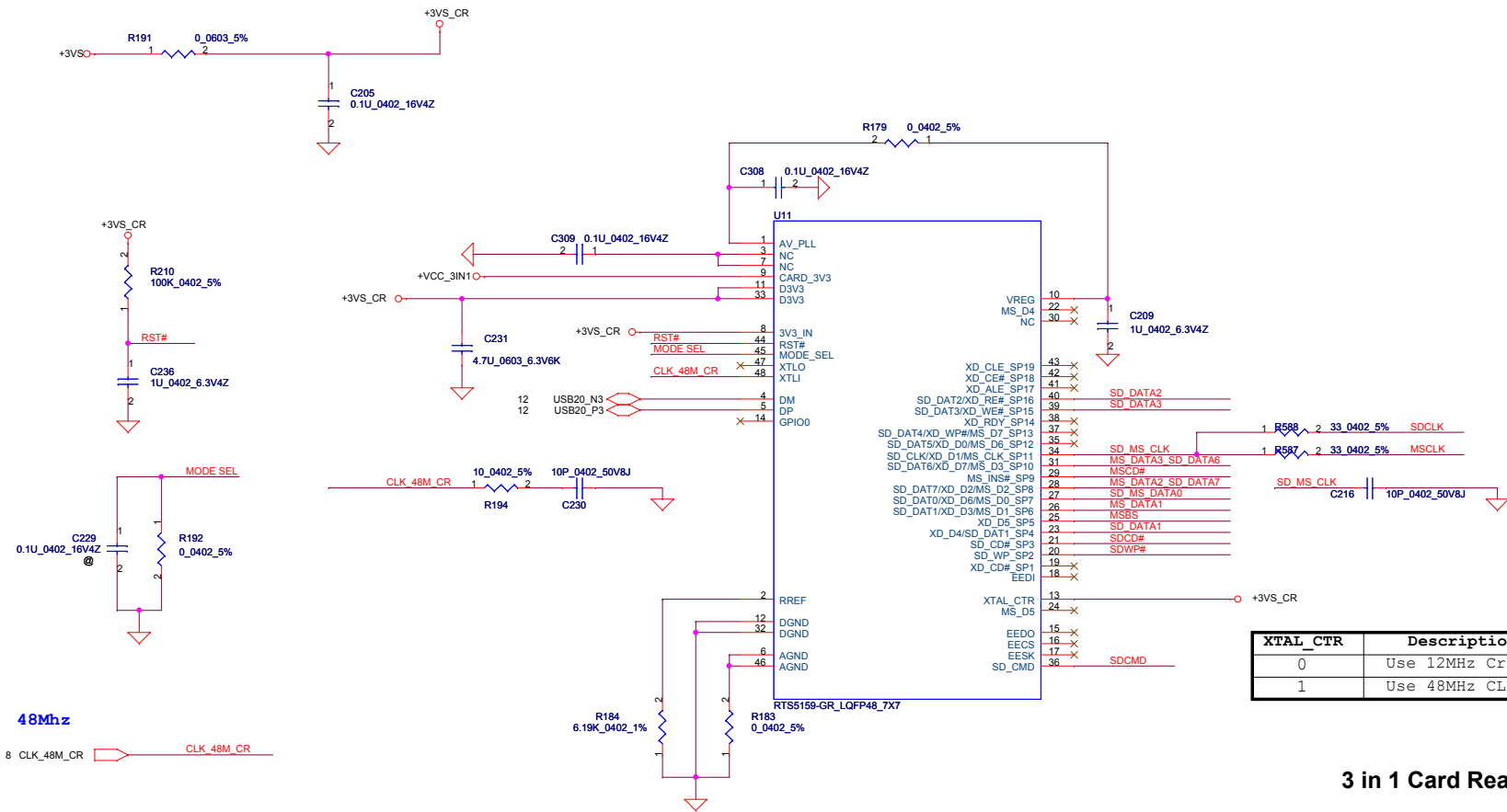
RTL8103EL-GR



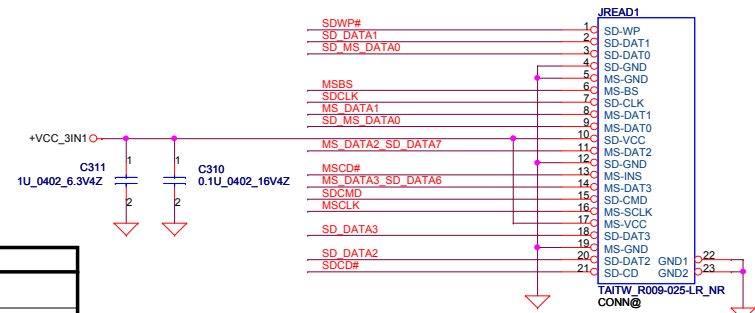
Lan Conn.



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Size	Custom	Document Number	NTV00 LA5661P M/B	Rev	1.0
Date	Thursday, January 07, 2010	Sheet	20	of	35

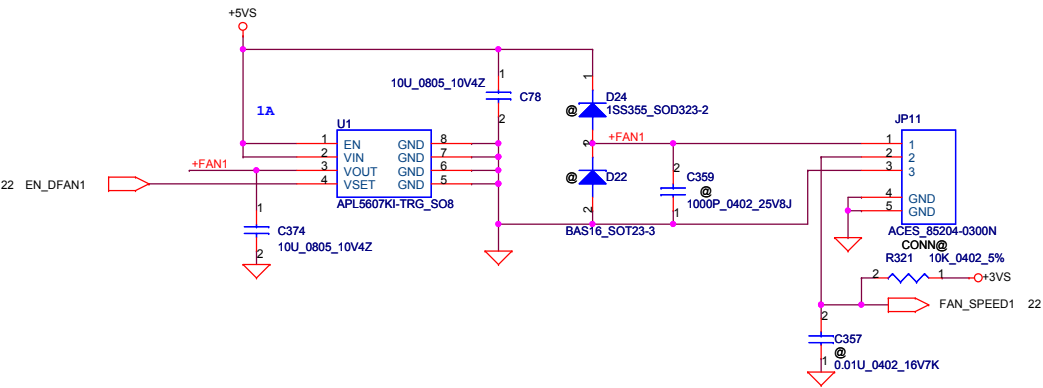


3 in 1 Card Reader

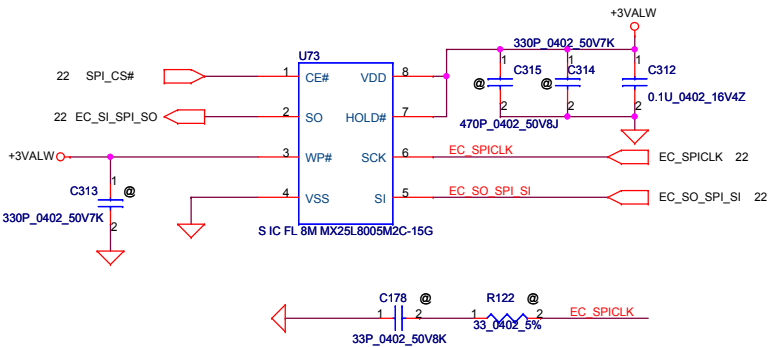


R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

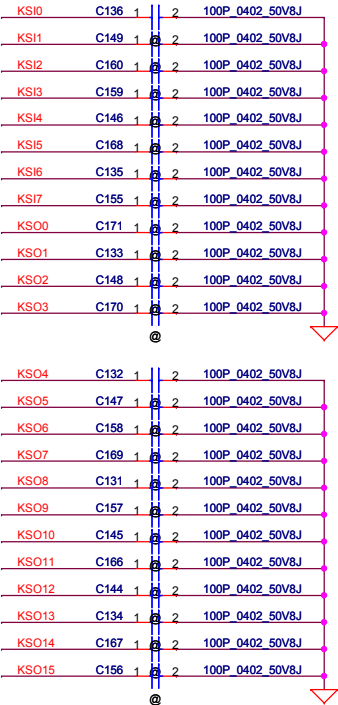
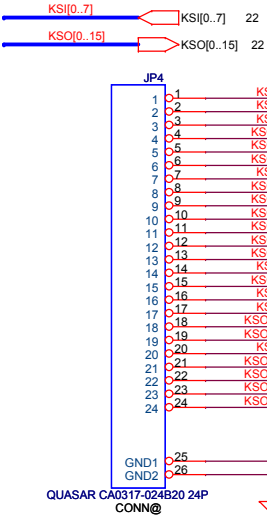
FAN Control Circuit



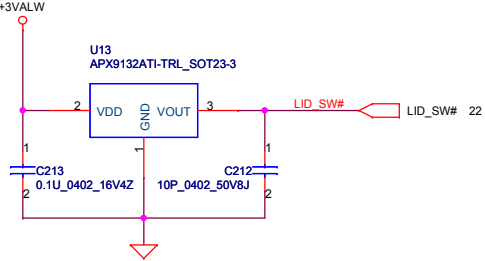
SPI Flash (16Mb*1)



KEYBOARD
CONN .

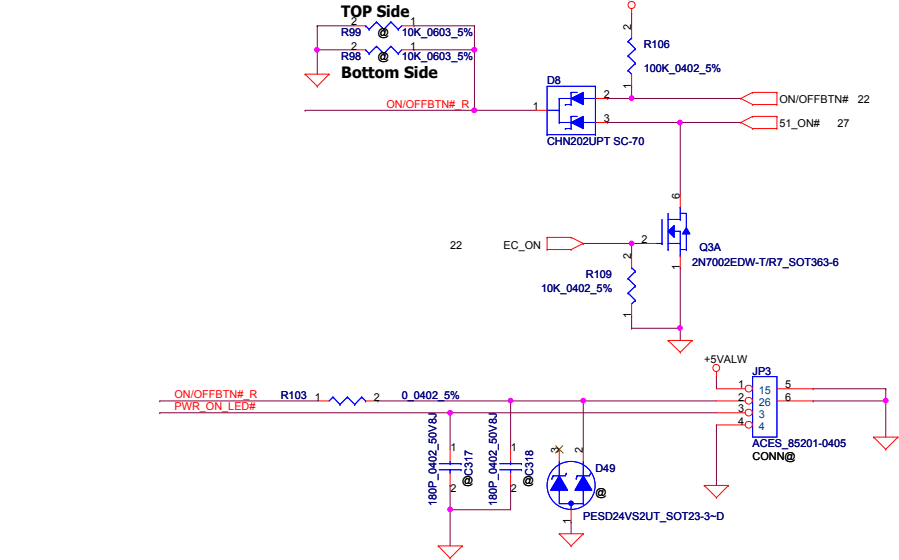


Lid SW

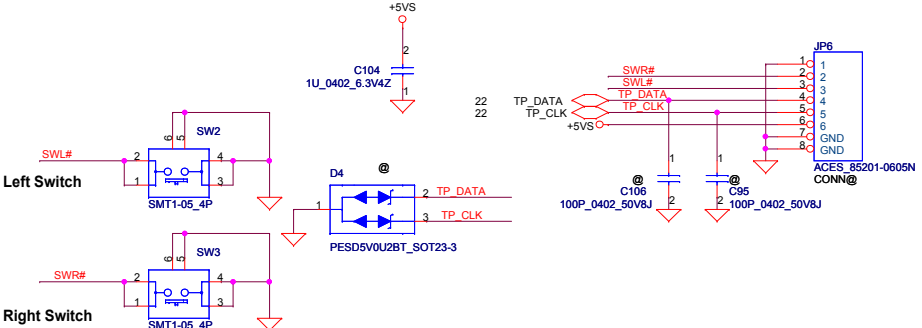


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					NTV00 LA5661P M/B	1.0
				Date:	Thursday, January 07, 2010	Sheet 23 of 35

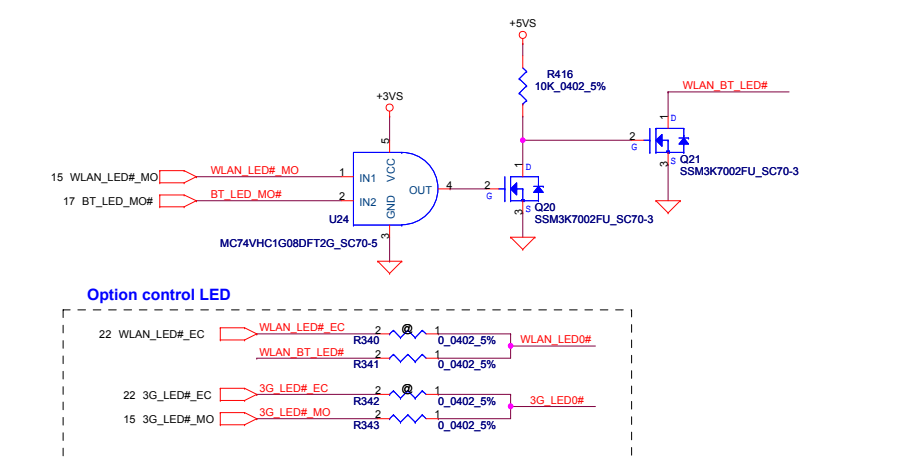
Power Button



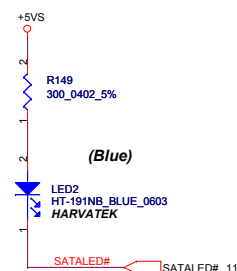
Touch/B Connector



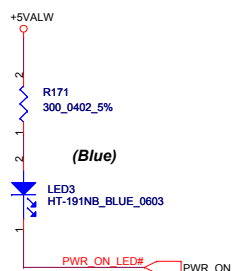
ISPD



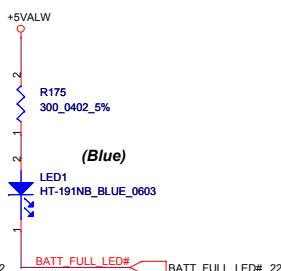
HDD_LED



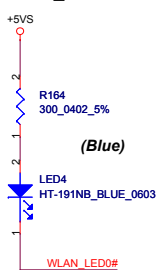
Power_LED



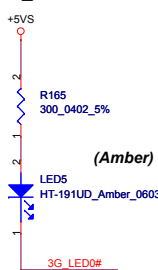
Charge_LED



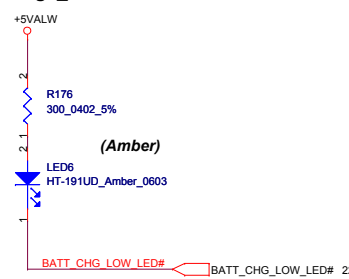
WLAN_LED



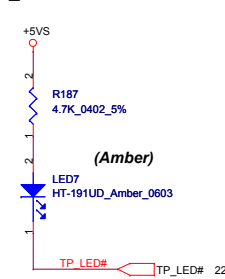
3G_LED



Charge_LED

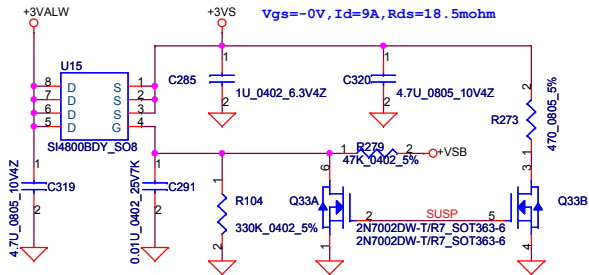


TP_LED

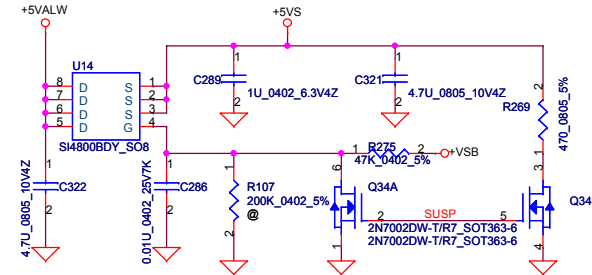


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Size	Document Number	Rev		Date	
Custom	NTV00 LA5661P M/B	1.0		Thursday, January 07, 2010	
Sheet		24		of 35	

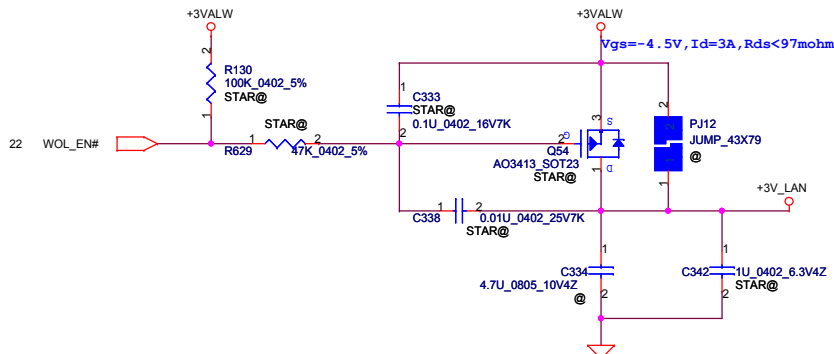
+3VALW TO +3VS



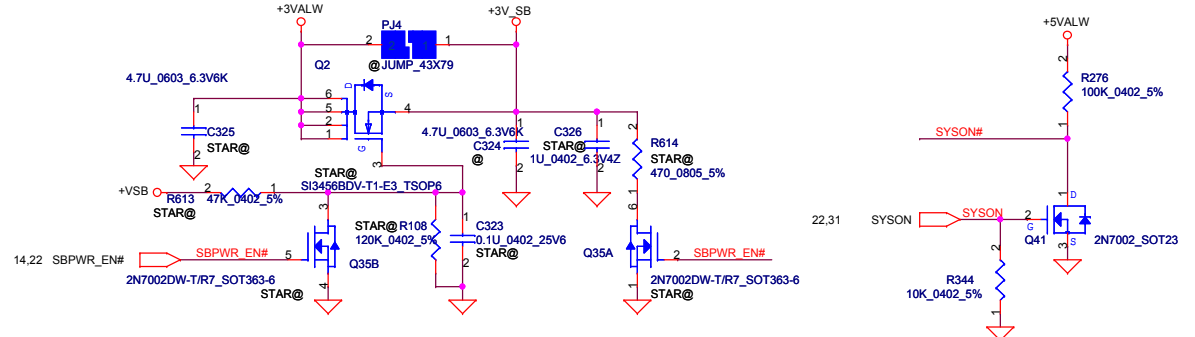
+5VALW TO +5VS



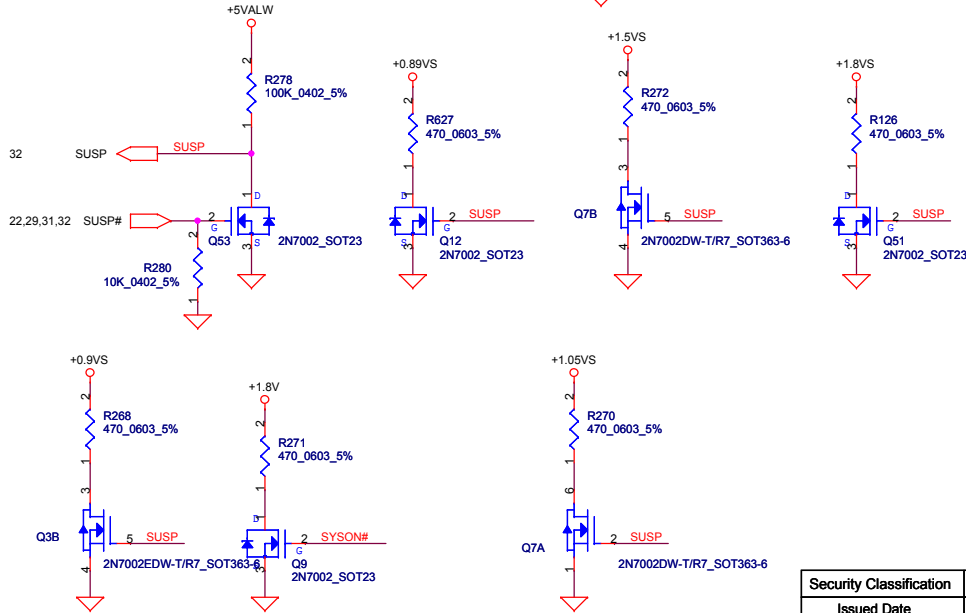
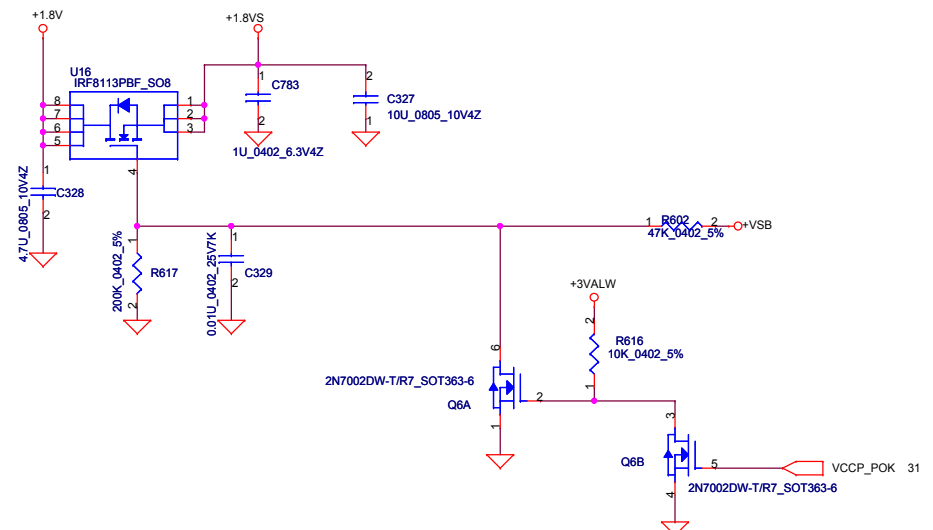
+3VALW TO +3V_LAN



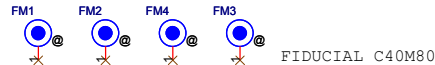
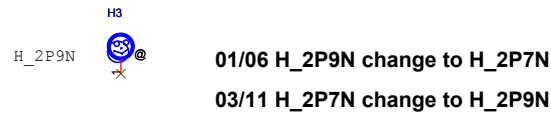
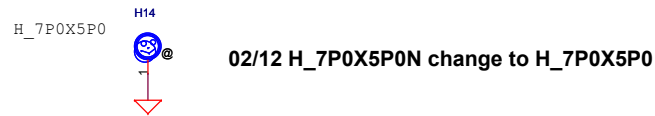
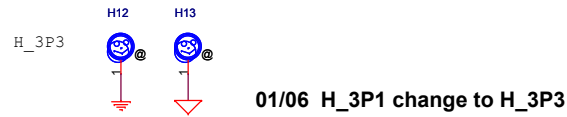
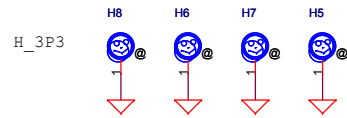
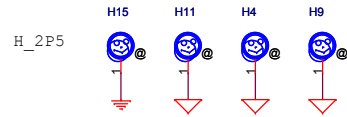
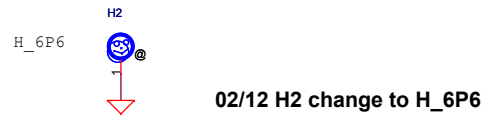
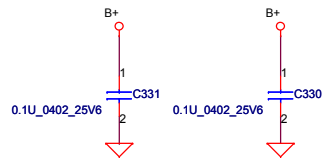
+3VALW TO +3V_SB



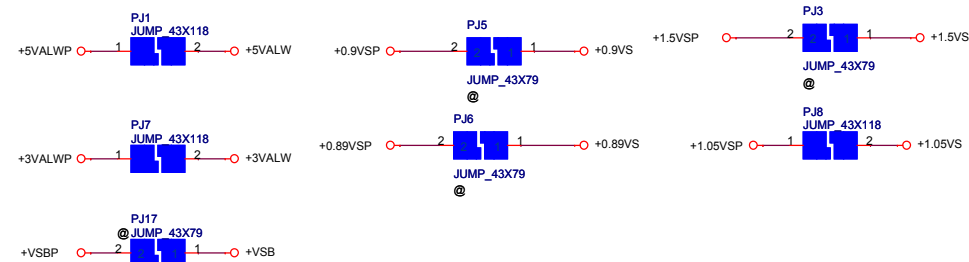
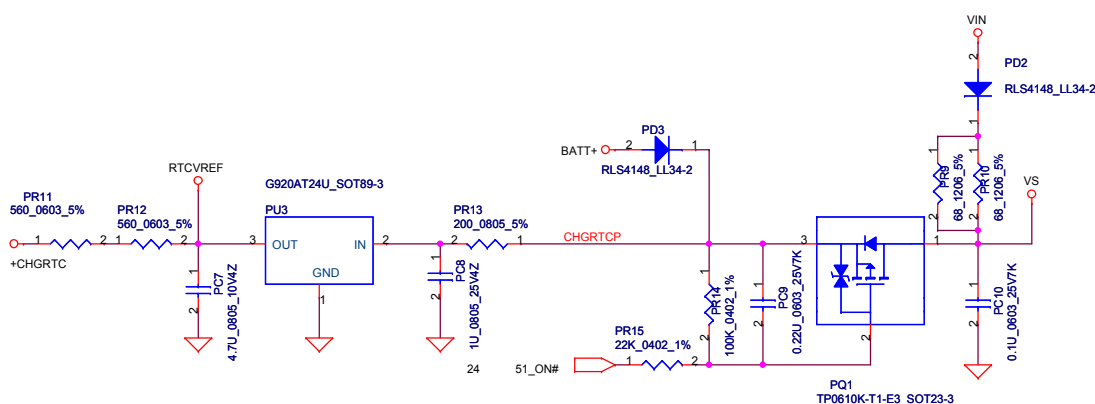
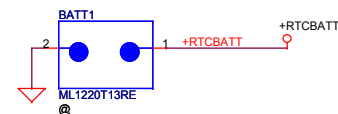
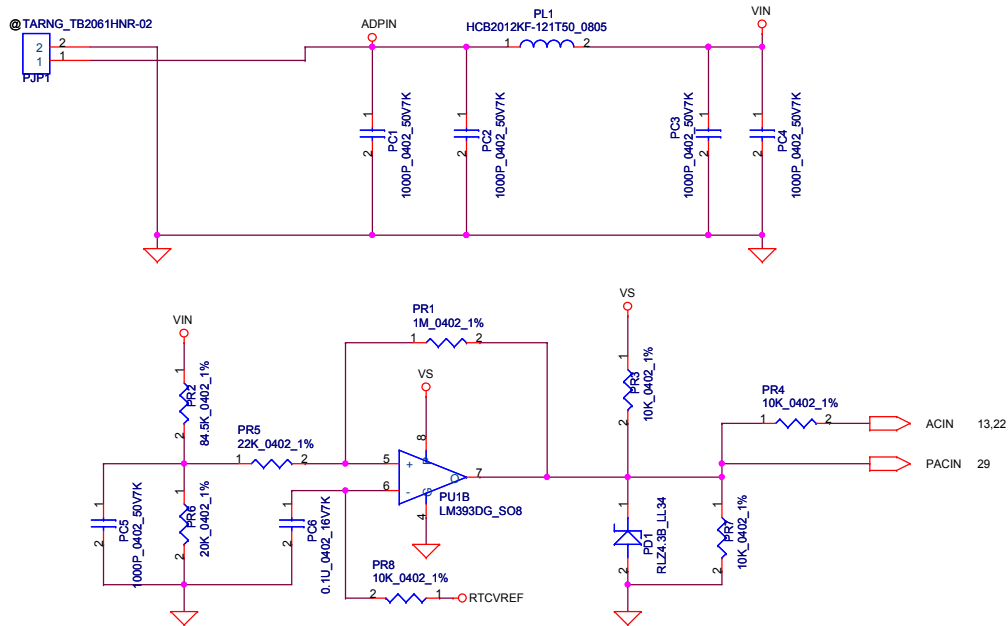
+1.8V TO +1.8VS



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Size		Document Number		Rev	
Custom		NTV00 LA5661P M/B		1.0	
Date		Thursday, January 07, 2010		Sheet 25 of 35	

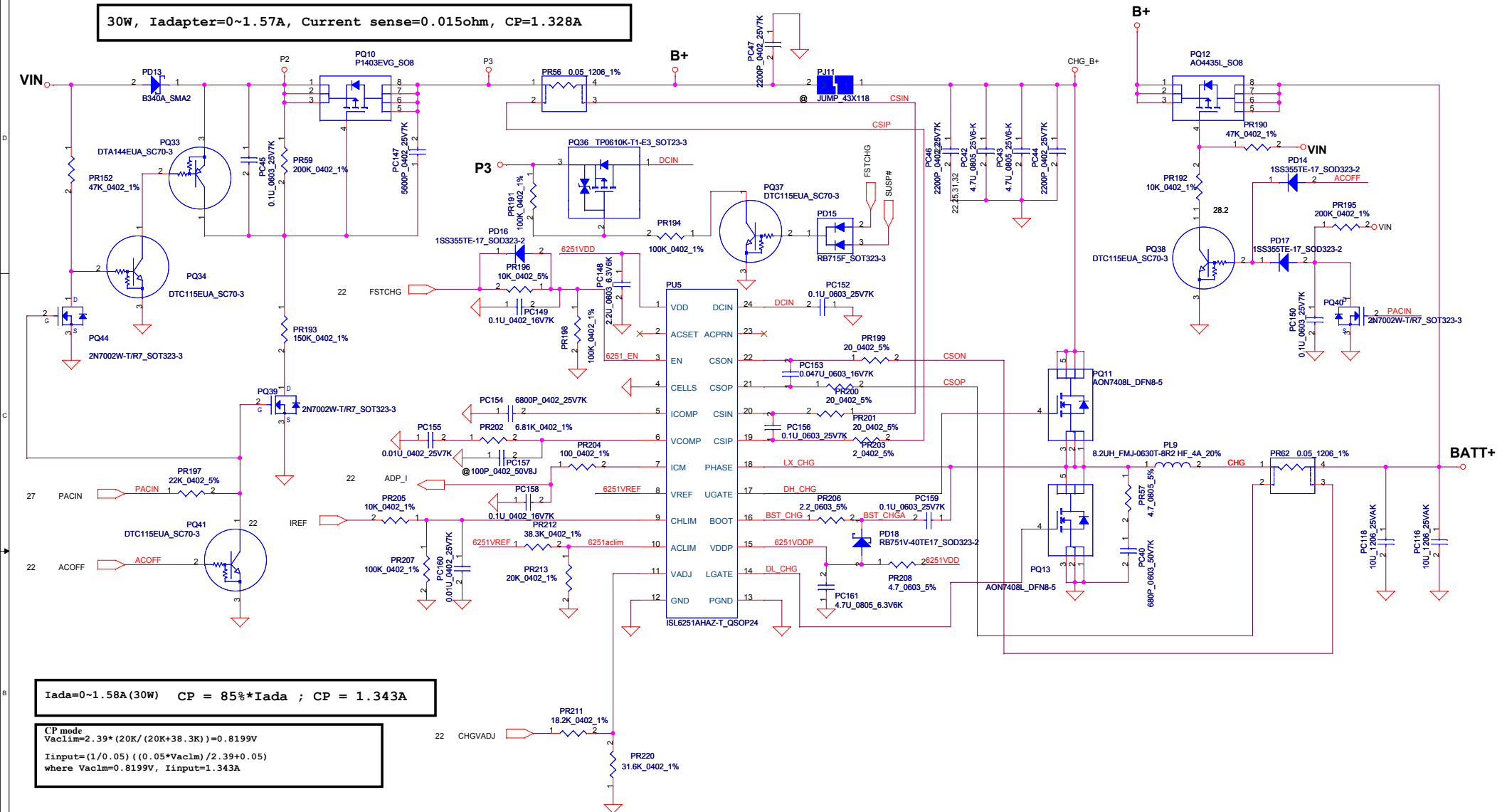


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					DC INTERFACE
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				NTV00 LA5661P M/B	
				Date	Rev
				Thursday, January 07, 2010	1.0
				Sheet	26 of 35



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Size	Custom	Document Number	NTV00 LA5661P M/B	Rev	1.0
Date:	Thursday, January 07, 2010	Sheet	27	of	35

30W, Iadapter=0~1.57A, Current sense=0.015ohm, CP=1.328A



I_{ada}=0~1.58A(30W) CP = 85%*I_{ada} ; CP = 1.343A

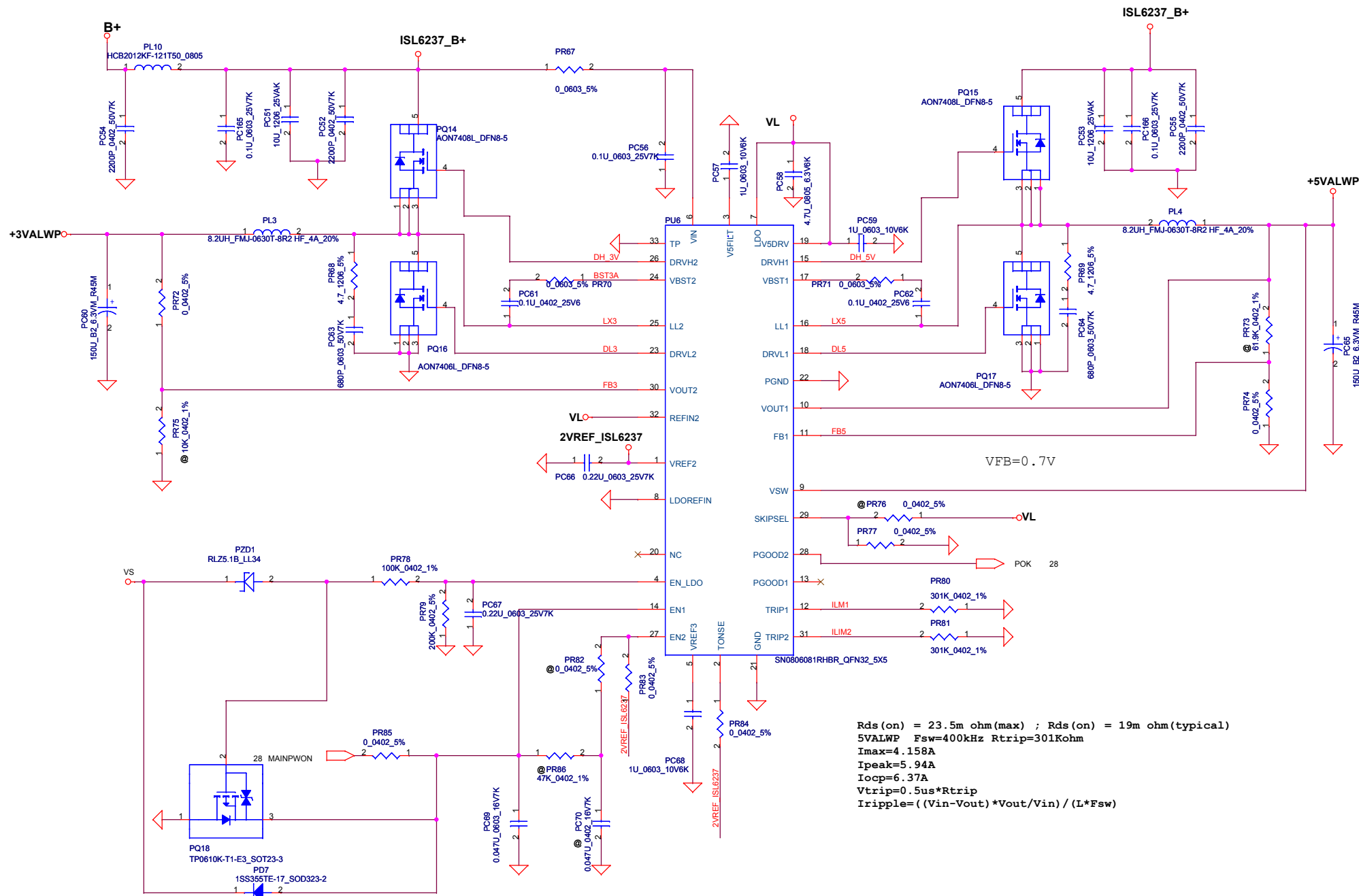
CP mode
 $V_{ac1m} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$
 $I_{input} = (1 / 0.05) * ((0.05 * V_{ac1m}) / 2.39 + 0.05)$
 where $V_{ac1m} = 0.8199V$, $I_{input} = 1.343A$

CC=0.3~3A
IREF=1.1*Icharge
IREF=0.33V~3.3V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

```
VADJ-->VREF-->4.41V
VADJ--->Ground--->3.39V
Vcell=(0.175*VADJ+3.99)
```

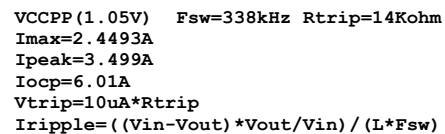
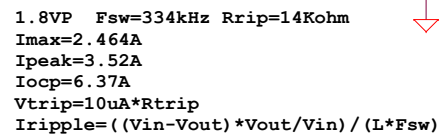
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								Size	Document Number			NTV00 LA5661P M/B			Rev	1.0
								Date:		Thursday, January 07, 2010			Sheet	29	of	35



$R_{ds(on)} = 23.5m \text{ ohm(max)} ; R_{ds(on)} = 19m \text{ ohm(typical)}$
 $5VALWP \text{ Fsw}=400kHz \text{ Rtrip}=301Kohm$
 $I_{max}=4.158A$
 $I_{peak}=5.94A$
 $I_{ocp}=6.37A$
 $V_{trip}=0.5us \cdot R_{trip}$
 $I_{ripple} = ((V_{in}-V_{out}) \cdot V_{out}/V_{in}) / (L \cdot F_{sw})$

$R_{ds(on)} = 23.5m \text{ ohm(max)} ; R_{ds(on)} = 19m \text{ ohm(typical)}$
 $3.3VALWP \text{ Fsw}=300kHz \text{ Rtrip}=301K$
 $I_{max}=4.319A$
 $I_{peak}=6.17A$
 $I_{ocp}=6.43A$
 $V_{trip}=0.5us \cdot R_{trip}$
 $I_{ripple} = ((V_{in}-V_{out}) \cdot V_{out}/V_{in}) / (L \cdot F_{sw})$

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				Custom	NTV00 LA5661P M/B
				Date	Thursday, January 07, 2010
				Sheet	30 of 35
				Rev	1.0



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Issued Date	2009/11/10	Deciphered Date	2010/11/10	Title 1.05VP/1.8VP		
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				Custom	NTV00 LA5661P M/B	1.0
				Date:	Thursday, January 07, 2010	Sheet 31 of 35

Page

EVT-2

Reason for change

Change PC77,PC87,PC125 from 10V to 6.3V

Add PR233 for enable CLK_GEN by HW request

Add snubber for EMI request

Change CPU OCP from 6A to 9A, PR210 from 1.8K to 2.61K

Change PC77, PC87, PC125 from 10V to 6.3V for standard part

DVT

Romve BattOVP function, EC support

Combine OTP to LM393

Change OTP from 89 to 92 degree for thermal request

Change PL15 to common part

PVT

shortage in factory

HW request

change net name

cost consideration

prevent noise coupling

prevent floating

adjust sequence

HW circuit request

OCP modify for power budget

cost consideration

PreMP

increase OTP setting point

Modify list

Add PR57, PC40, PR68, PC63, PR69, PC64,

Add PR90, PC80, PR98, PC90, PR148, PC129, PR122, PC109

Change PR210 from 1.8K to 2.61K

Del PU4, PC115,PC117,PR138,PR139,PR140,PR141

DEL PD5

Change PR20 from 10K to 8.87K

Change PC9,PC135 from 0.22U_1206 to 0.22U_0603
Change PC42,PC43 from 0.22U_1206 to 0.22U_0805
Change PC66 from 0.22U_0603_10V7K to 0.22U_0603_25V7K

Add B+>>+VSB circuit and +VSB jump

Add PGOOD circuit in PU8

change CLK_EN# to CLK_ENABLE#, +VCCPP to +1.05VSP, +VCCP to +1.05VS, SPOK to POK, BATT_TEMP to BATT_TEMPA

change PU7,PU8,PU13 from TPS51117RGYR to RT8209BGQW

change PR101 13.7k to 3.65k and PR102 31.6k to 8.87k
change PR93 30.1k to 8.87k and PR94 20.5k to 6.04k
change PR147 5.9k to 1.91k and PR94 31.6k to 10k

Add 30K resistance between EN pin and GND in PU7,8,13

change PR21 from 100K to 806K

change page-off connector to port

change PR80,81 from 210K to 270K and PR92 from 14.7K to 10K and PR210 from 2.61K to 3K

take off PC98 and CPU_CORE jump

change PR20 from 8.87K to 7.68K

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				Size	Document Number	Rev
				Custom	NTV00 LA5661P M/B	1.0
Date:				Thursday, January 07, 2010	Sheet	34 of 35

PIR (Product Improve Record)

SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/02	6	Change C278 footprint from B2 to D2	Cost down
2	12/02	5	Add R193,R221,R209,R214,R218,R224 closed to Processor Pin	EMI request
3	12/03	14	Remove R562 let +VCC1_5 connect to +1.5VS directly	Layout shape non-enough
4	12/03	7	Add C589,C46,C559,C610,C41,C547,C344,C628,C542	Layout signal dirty
5	12/03	13	Add C665,C666,C667	Layout signal dirty
6	12/03	15	Add C668,C669	Layout signal dirty
7	12/08	6	Change C278 PN to SGA00001Q80	Power request

SCHEMATIC CHANGE LIST
REVISION CHANGE: 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/28	13	Change BT_OFF to EC Pin29	Leverage DVT
2	12/28	14	R47 reserve	BOM change
3	12/28	13	C408 reserve	BOM change
4	12/28	16	C747 reserve	BOM change
5	12/28	23	Change U73 PN to SA00000XT00	BIOS request
6	12/28	22	Change RP17 to R87,R88,R413,R417	EC request

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						PIR
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Size		Document Number			Date	
		NTV00 LA5961P M/B			Thursday, January 07, 2010	
		Sheet 35 of 35				

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