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Compal Confidential

KTV00 Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

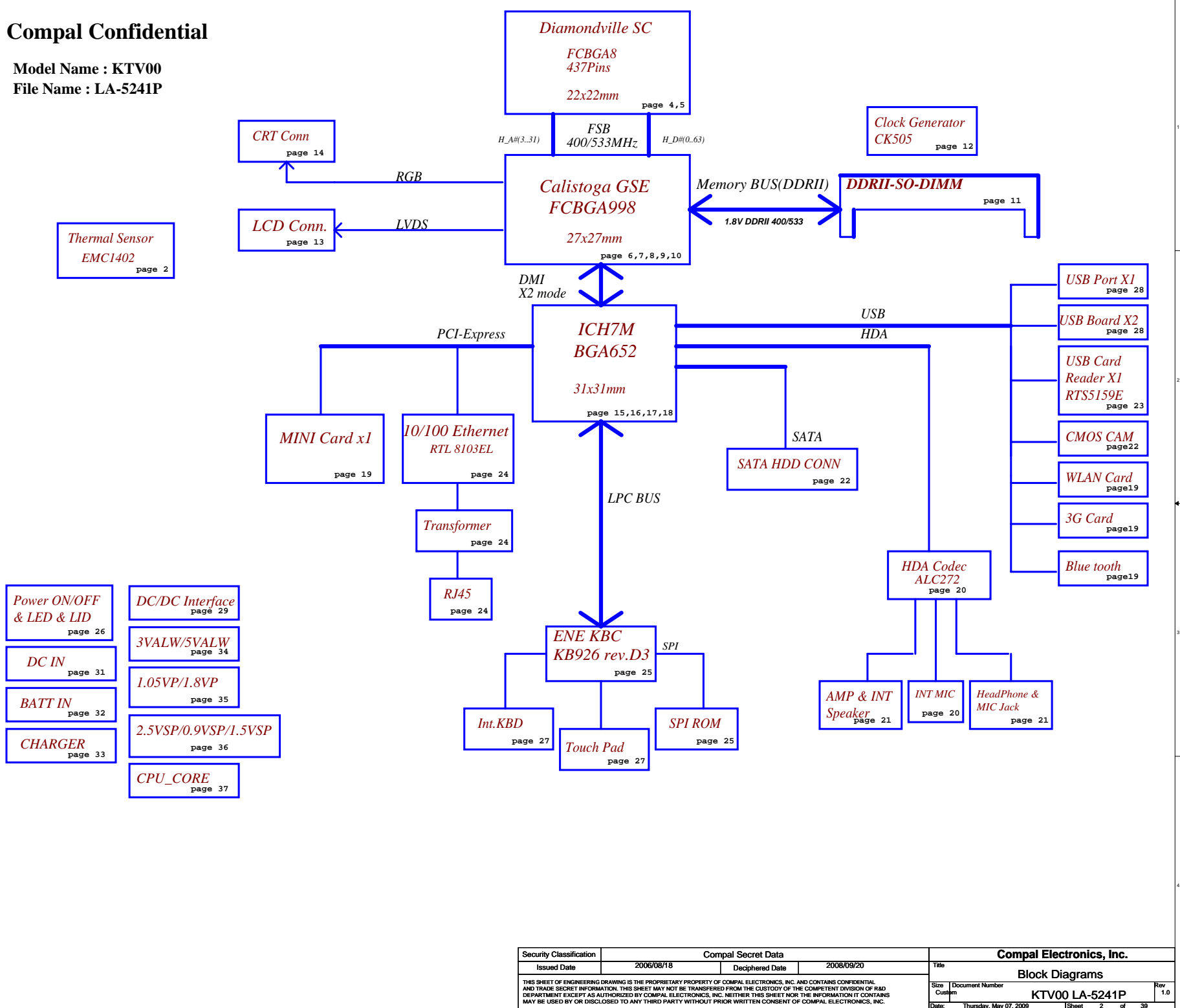
2009-05-07

REV: 1.0

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				Rev	1.0

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Model Name : KTV00
File Name : LA-5241P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

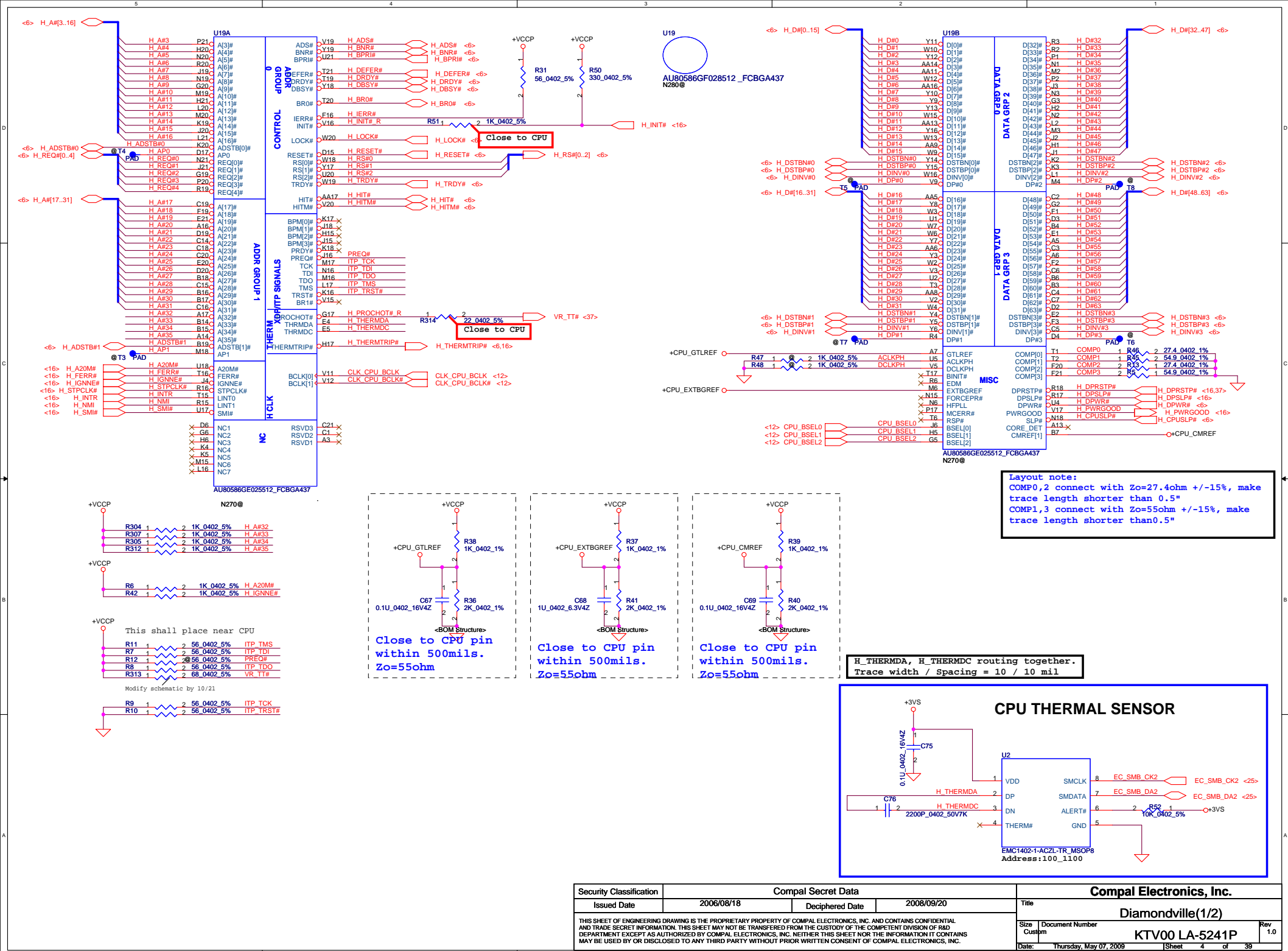
EC SM Bus1 address

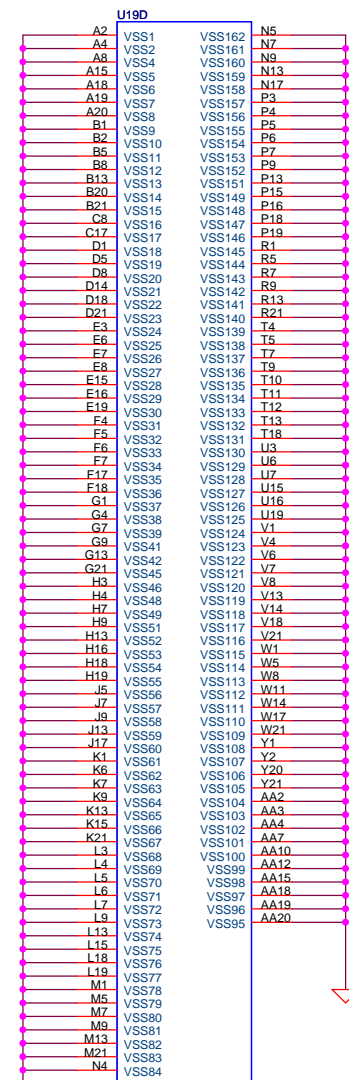
Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b

EC SM Bus2 address

ICH7M SM Bus address

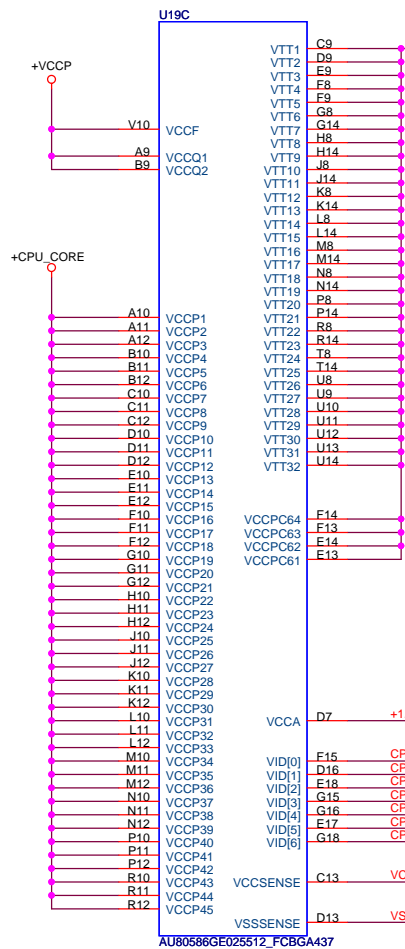
Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb





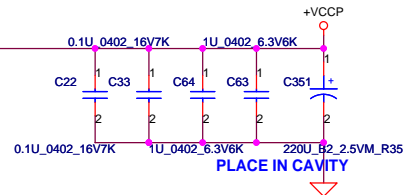
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N270@

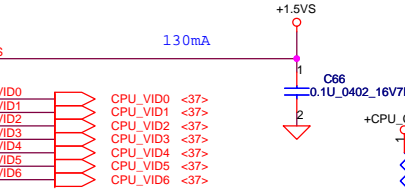


N270@

AU80586GE025512_FCBGA437



PLACE IN CAVITY



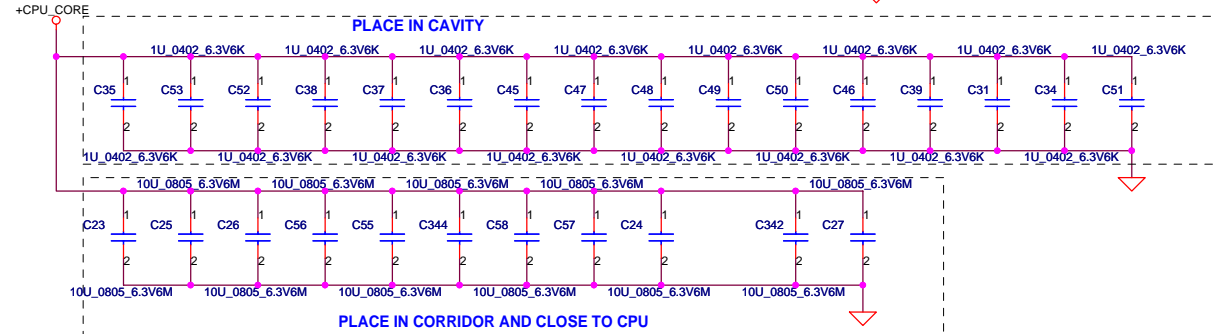
130mA



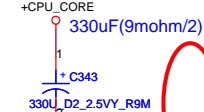
100_0402_1%

100_0402_1%

Length match within 25 mils
The trace space 7 mils,
Zo=27.4ohm



PLACE IN CORRIDOR AND CLOSE TO CPU

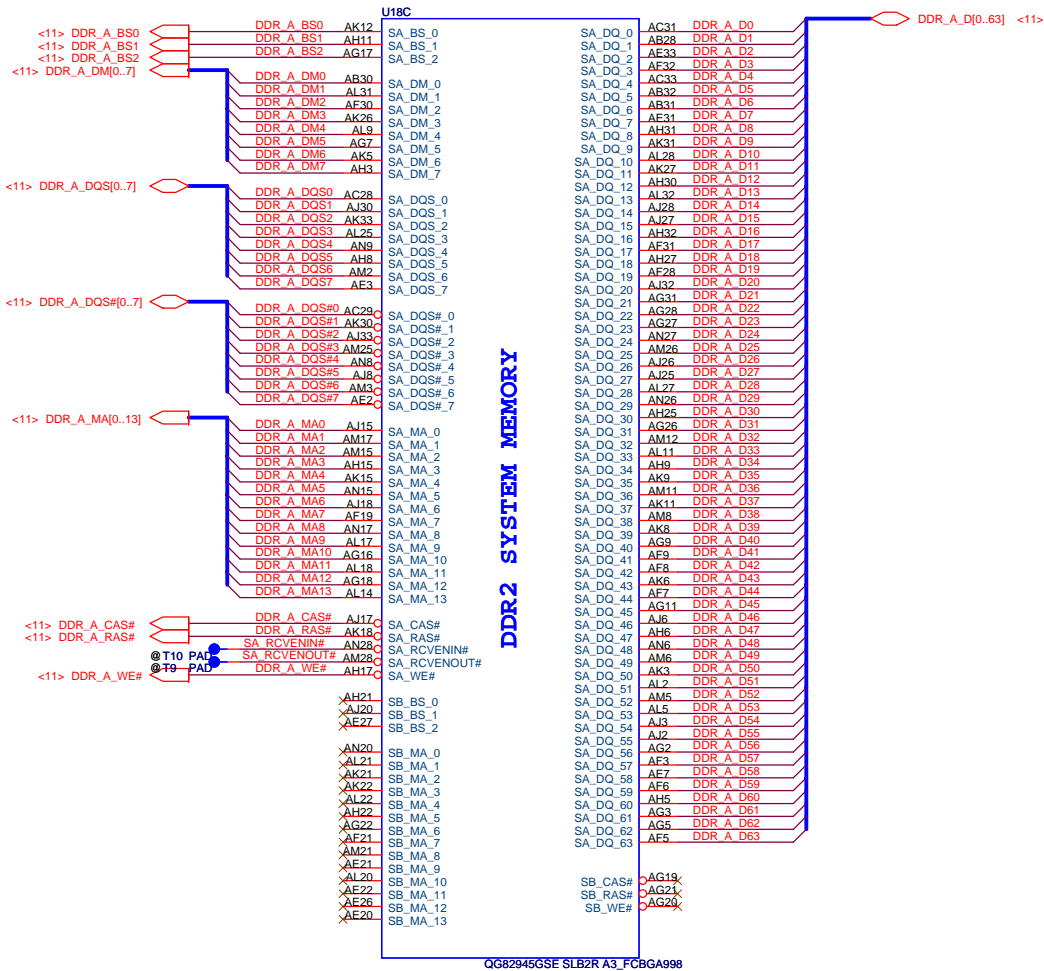


12/29 Remove C331-->330U

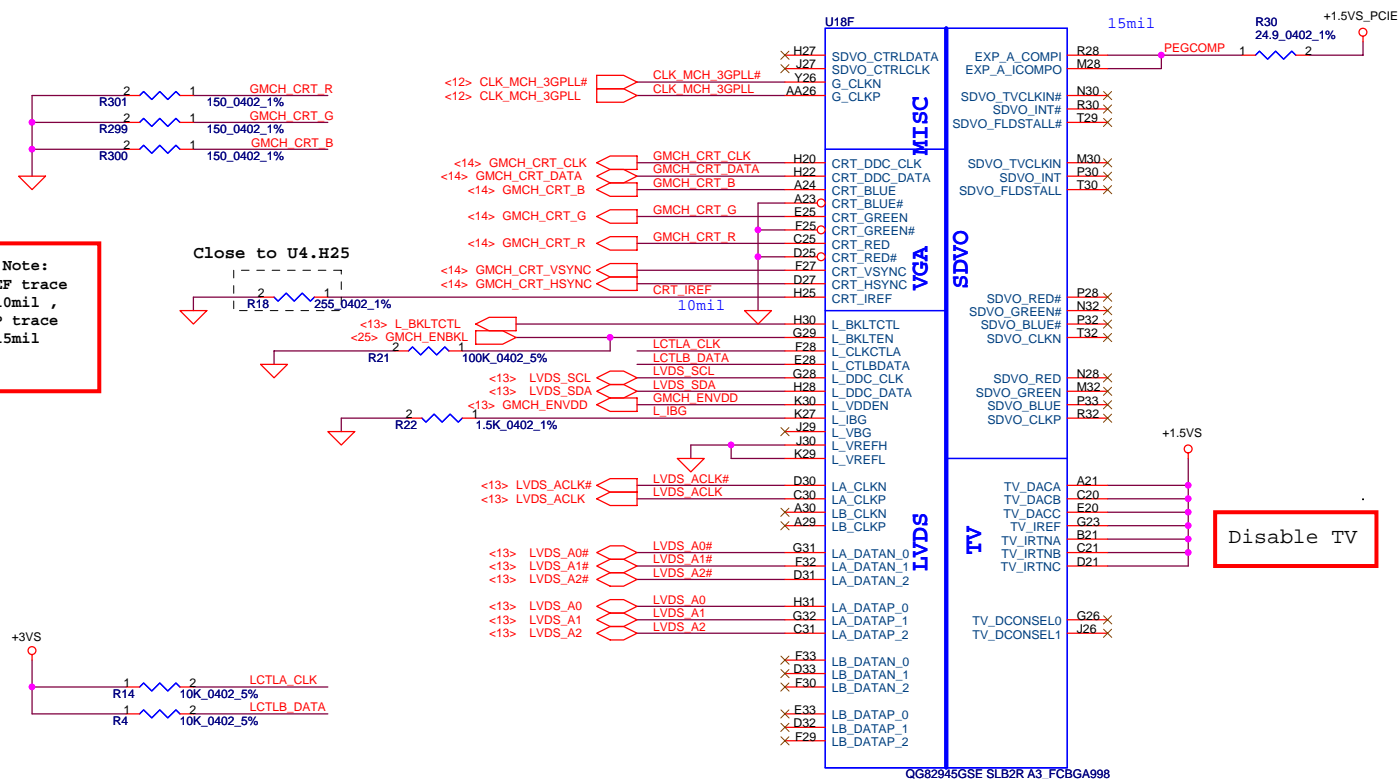
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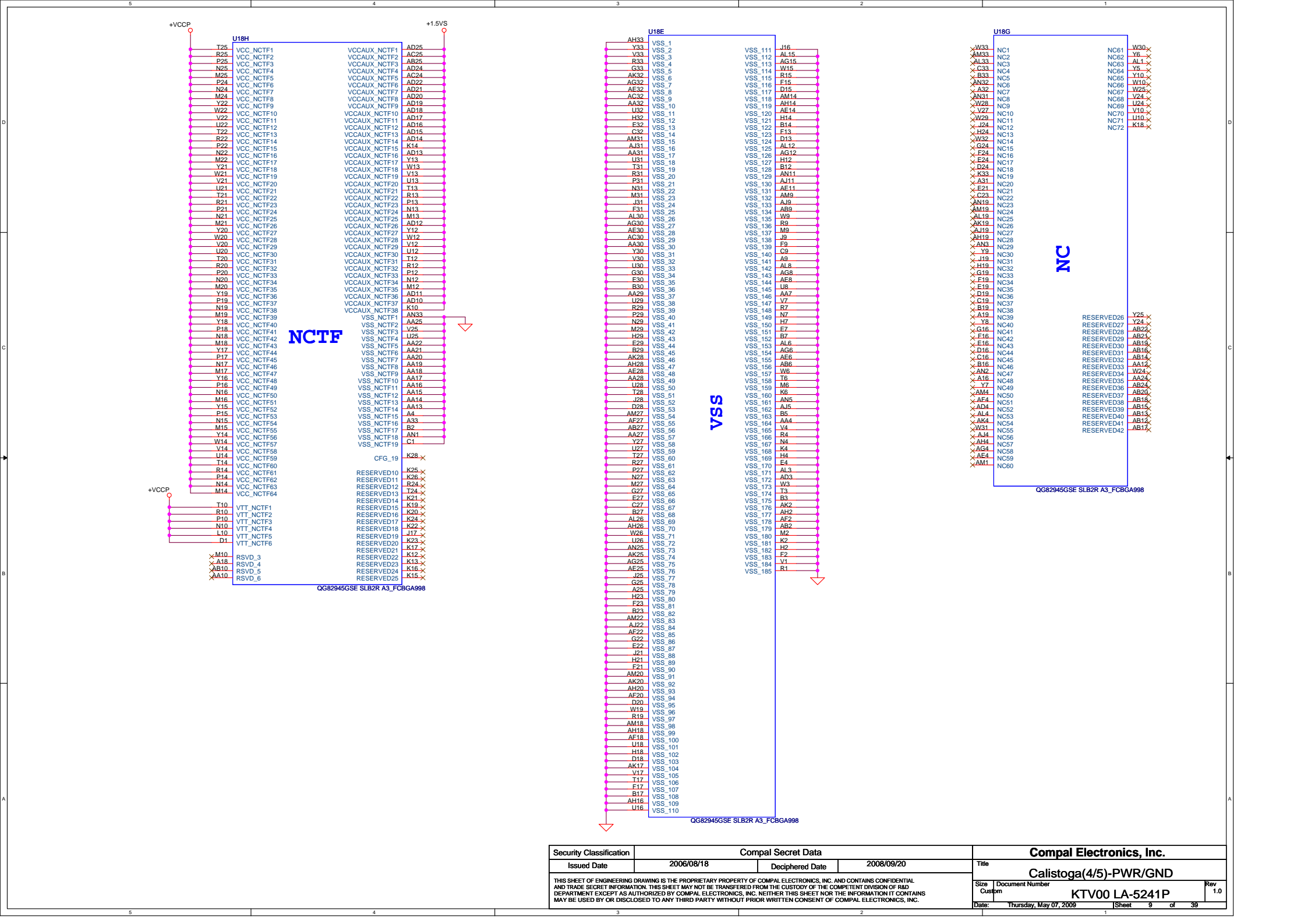
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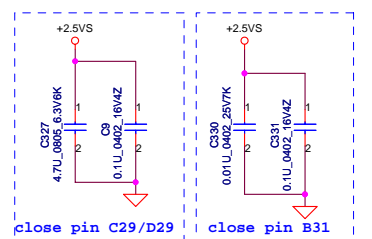
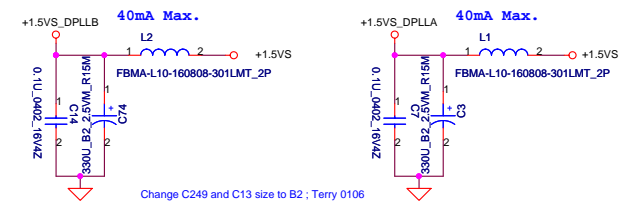
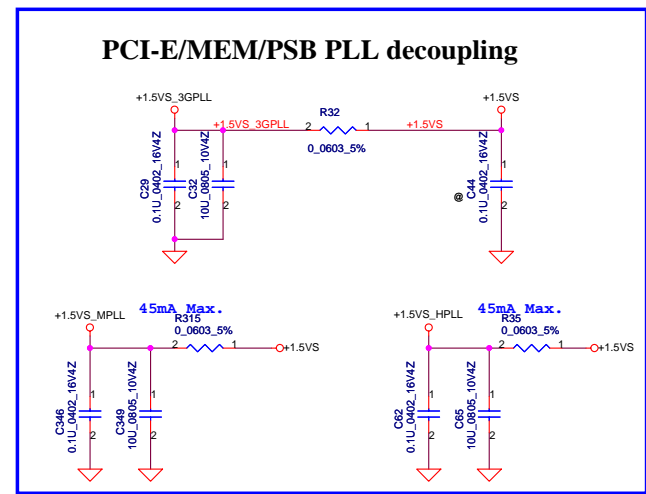
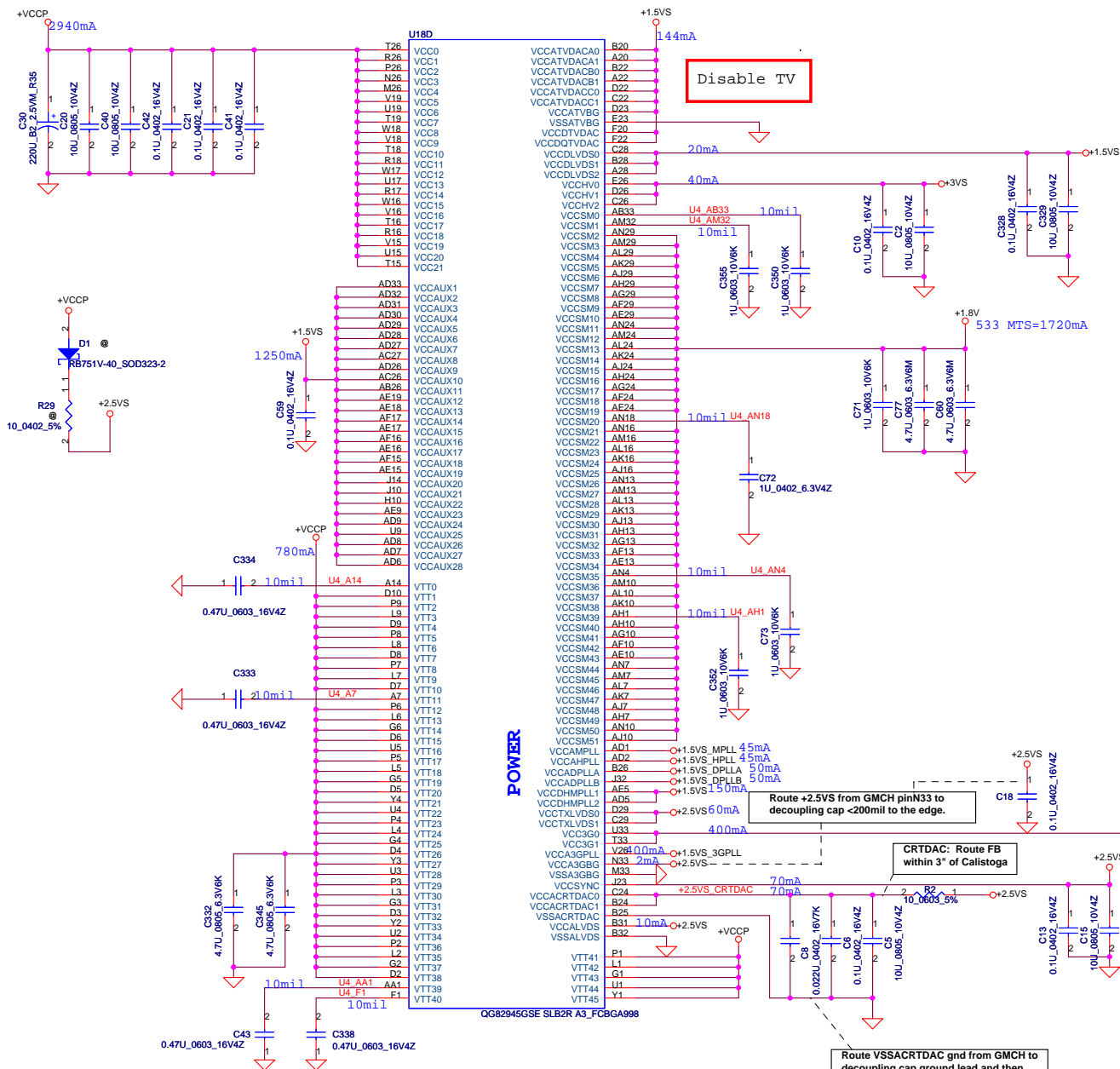
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Issued Date	2006/08/18	Deciphered Date	2008/09/20	Title Calistoga (1/5)-GTL/DMI/DDR		
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Layout Note:
CRT_IREF trace
width 10mil ,
PEGCOMP trace
width 15mil



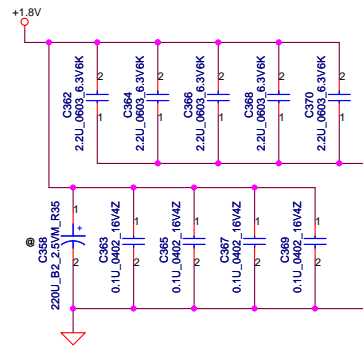




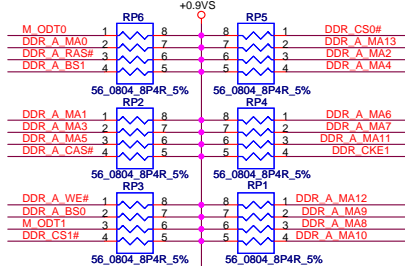
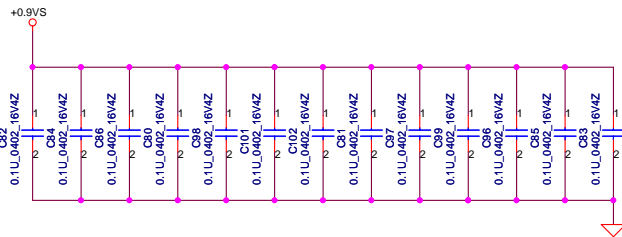
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Issued Date	2006/08/18	Deciphered Date	2008/09/20	Calistoga(5/5)-PWR/GND	
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<7> DDR_A_DQS#[0..7]
 <7> DDR_A_D[0..63]
 <7> DDR_A_DM[0..7]
 <7> DDR_A_DQS[0..7]
 <7> DDR_A_MA[0..13]

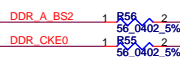
Layout Note:
 Place near JDIM1



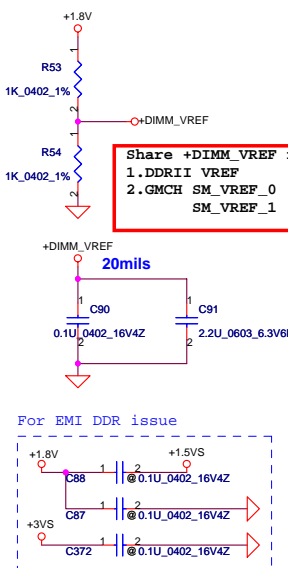
Layout Note:
 Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
 Place these resistor closely DIMMA, all trace length < 750 mil

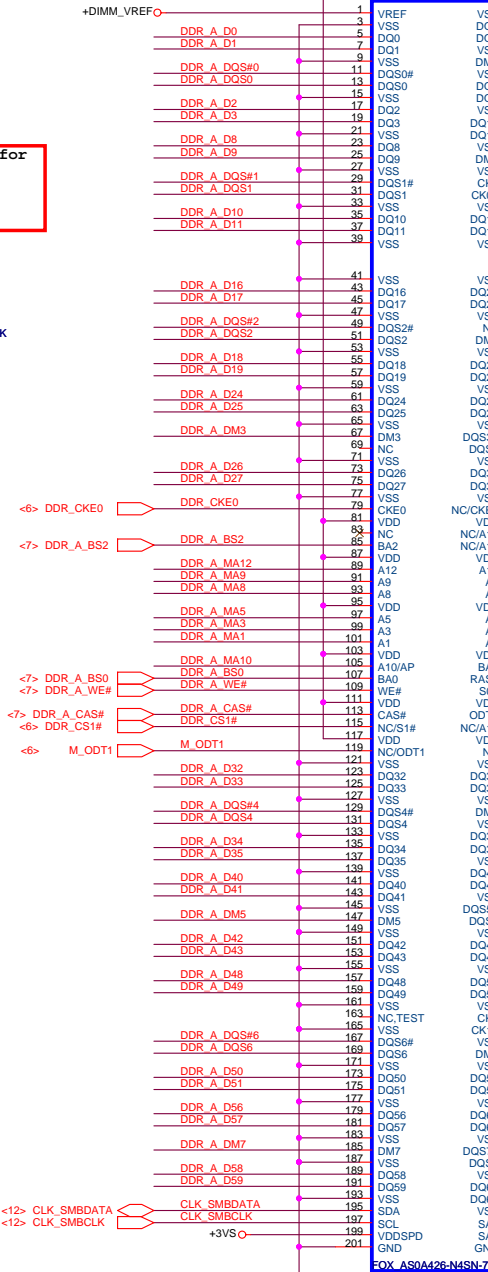
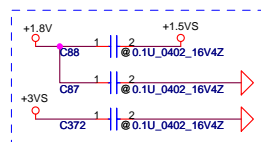


Layout Note:
 Place these resistor closely DIMMA, all trace length Max=1.3"

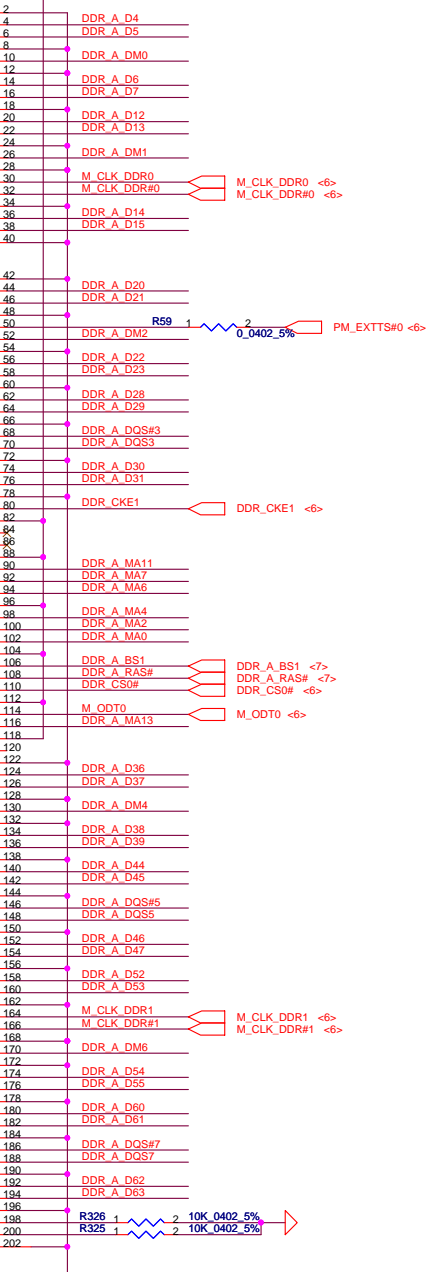


Share +DIMM_VREF for
 1.DDRII VREF
 2.GMCH SM_VREF_0
 SM_VREF_1

For EMI DDR issue

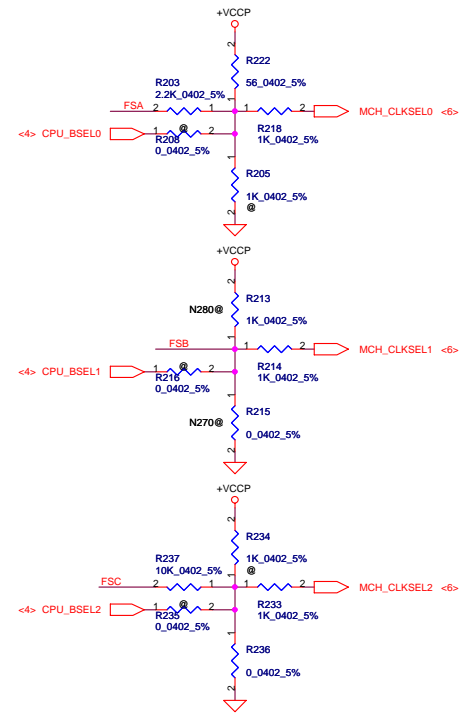


DIMMA

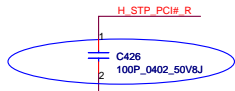


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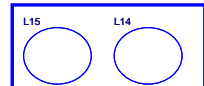
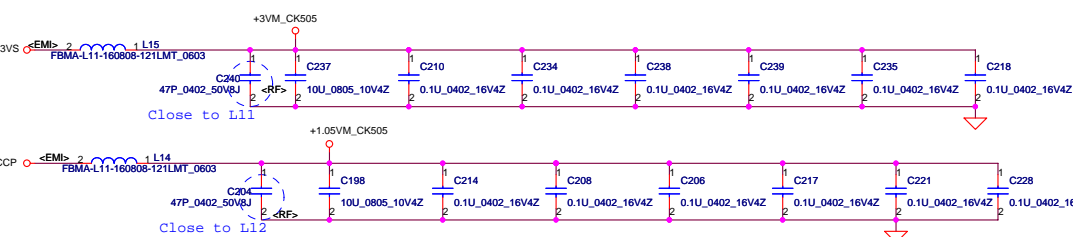
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



0211 Add C426 for power noise

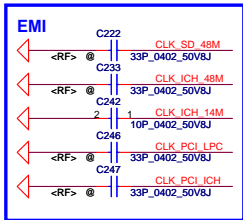
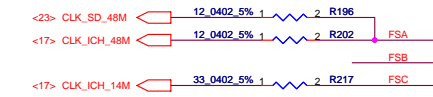


C426 close to U12



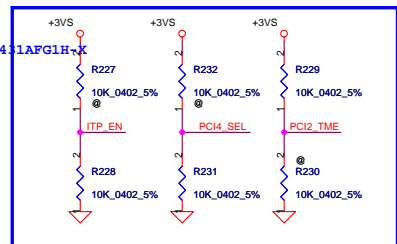
0118 change L14 & L15 to 0.0603

0120 Add C403 for noise
Change C403 from 100p to 330p 0319

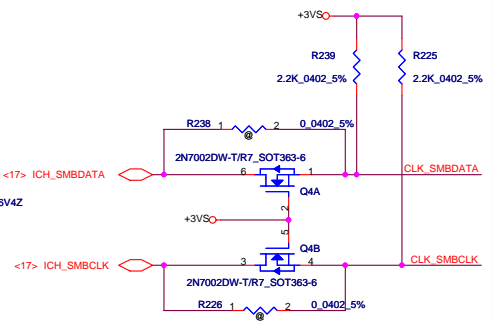


For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME:0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

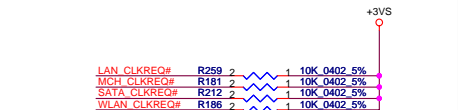


SA000020K00 (Silego : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)

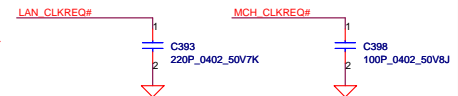


SRC PORT LIST

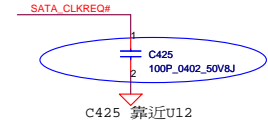
PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	SATA HDD
SRC3	MCH_3GPLL
SRC4	
SRC6	PCIE_WLAN
SRC7	
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	



0120 Add C393 C398 for power noise
Change C393 from 100p to 220p 0319.



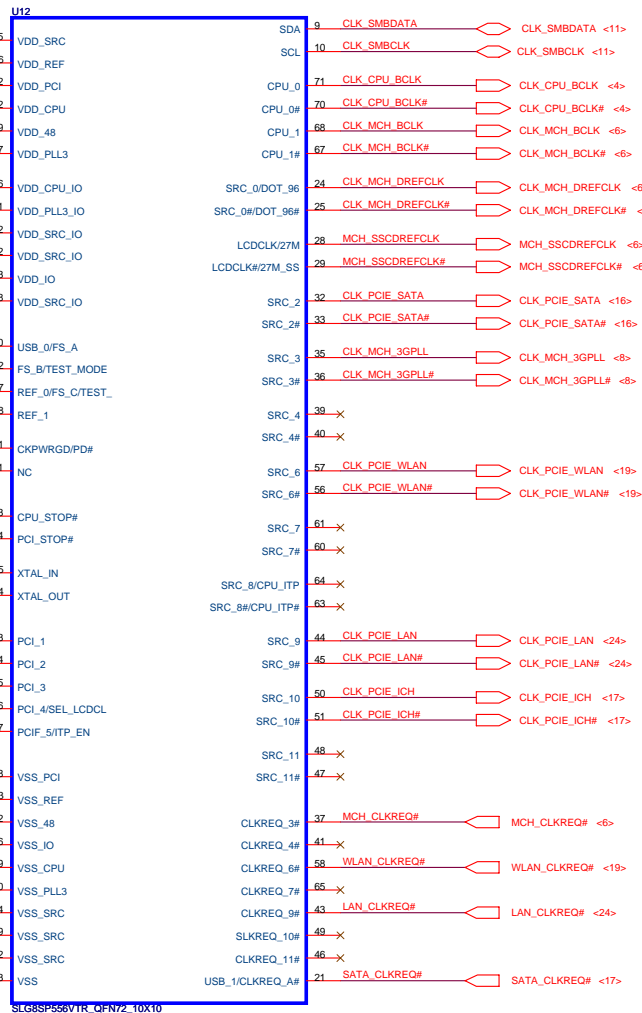
0210 Add C425 for power noise



C425 靠近U12

REQ PORT LIST

PORT	DEVICE
REQ_3#	MCH_3GPLL
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	
REQ_A#	SATA

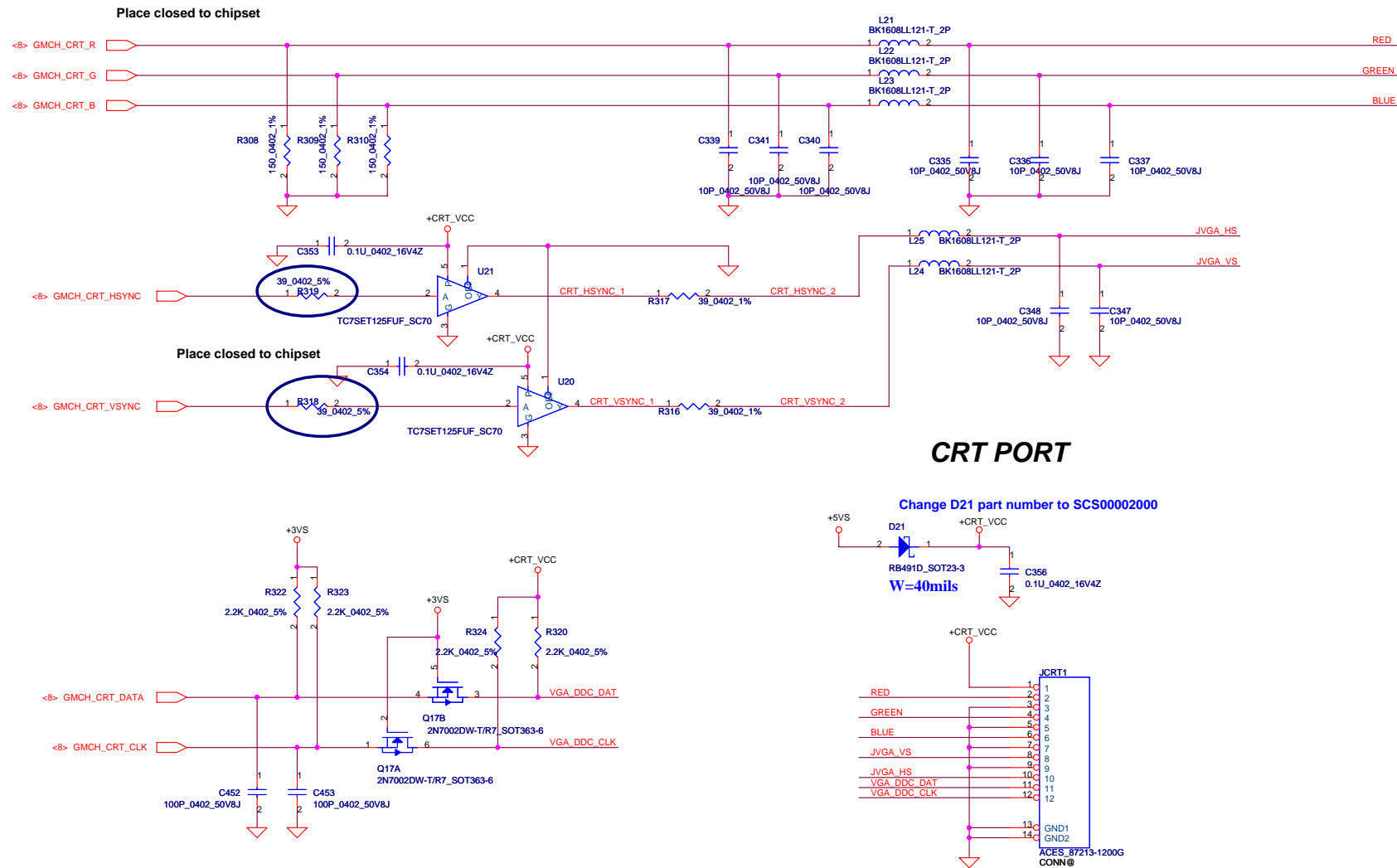


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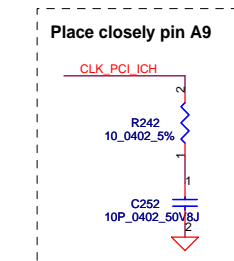
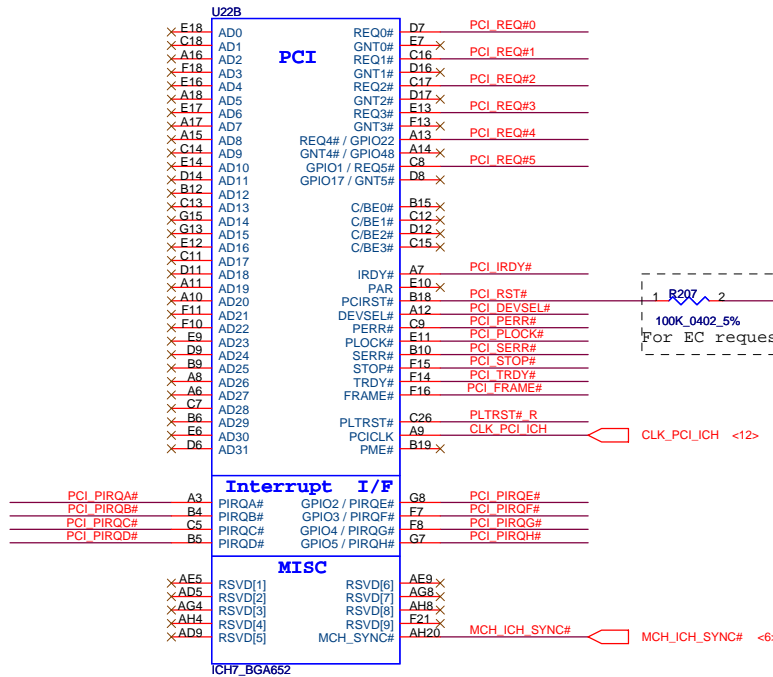
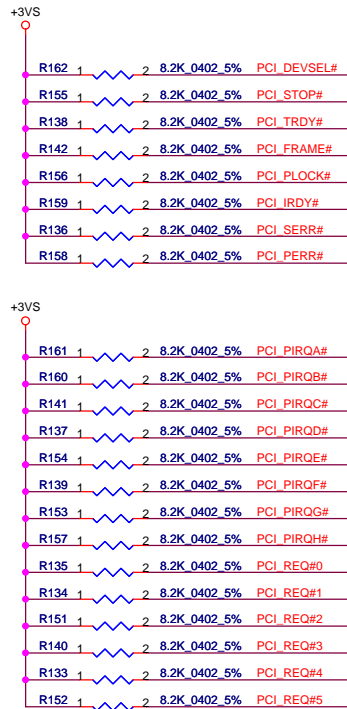
Compal Electronics, Inc.		
Clock Generator CK505		
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LED PANEL/CMOS. Conn.

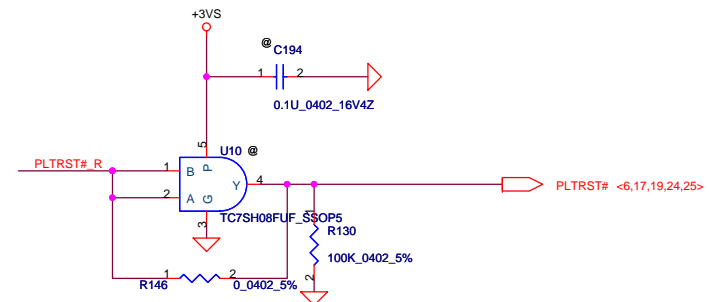
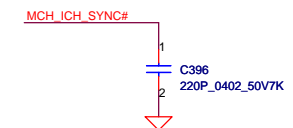
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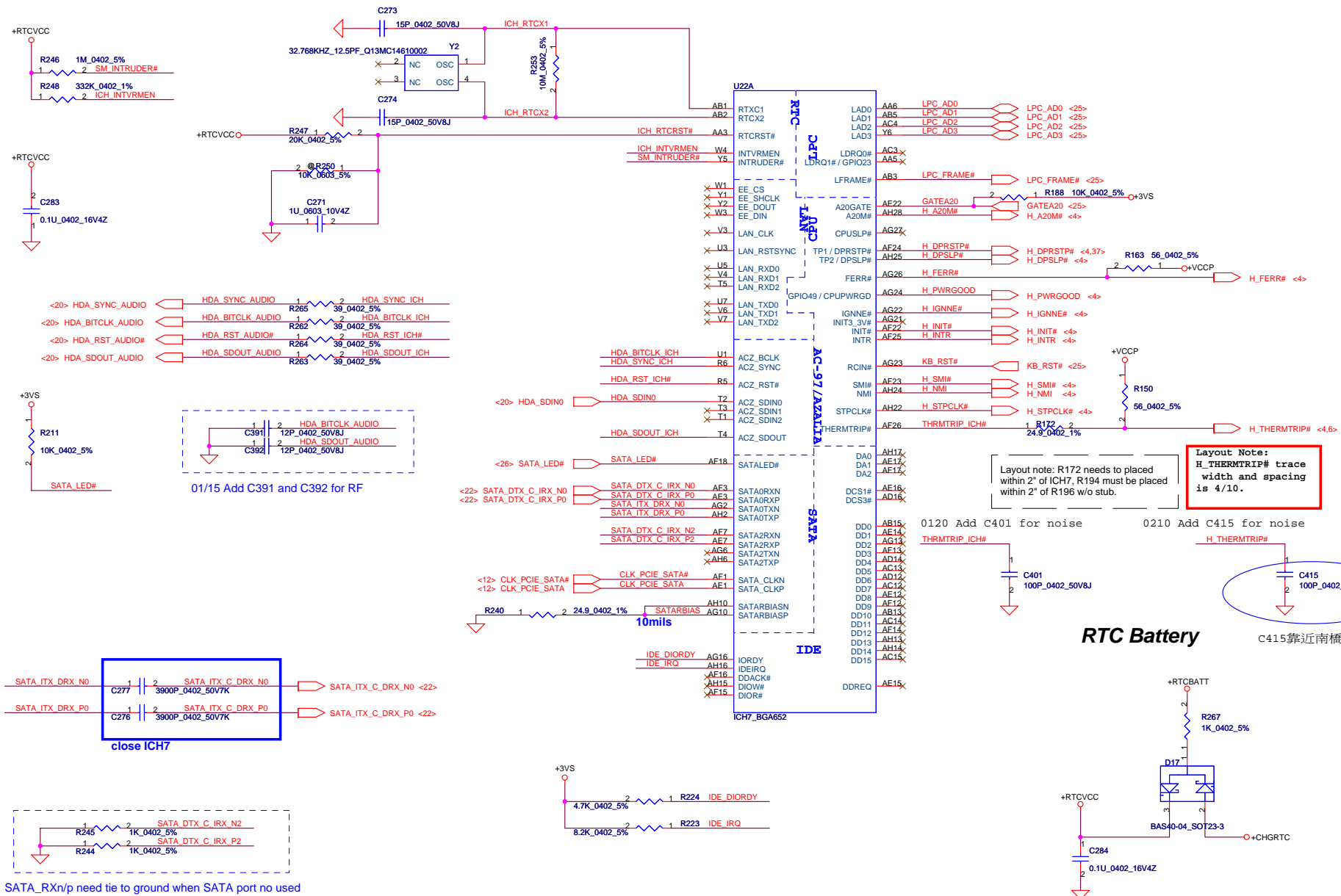
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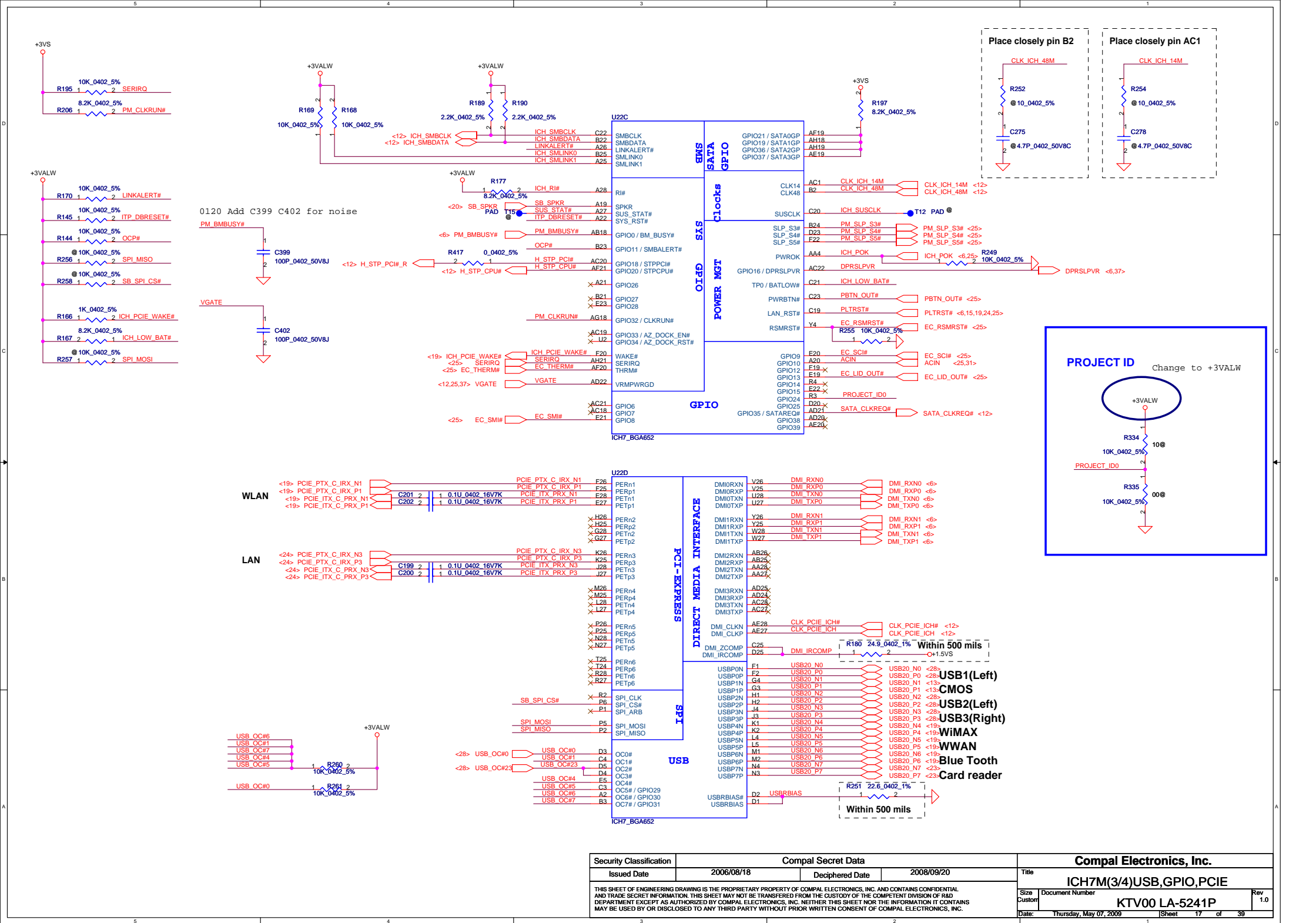
0120 Add C396 for noise
Change C396 from 100p to 220p 0319

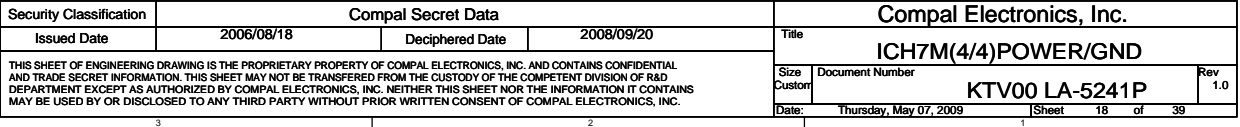


Change C273 C274 from 18P to 15P; 20090204

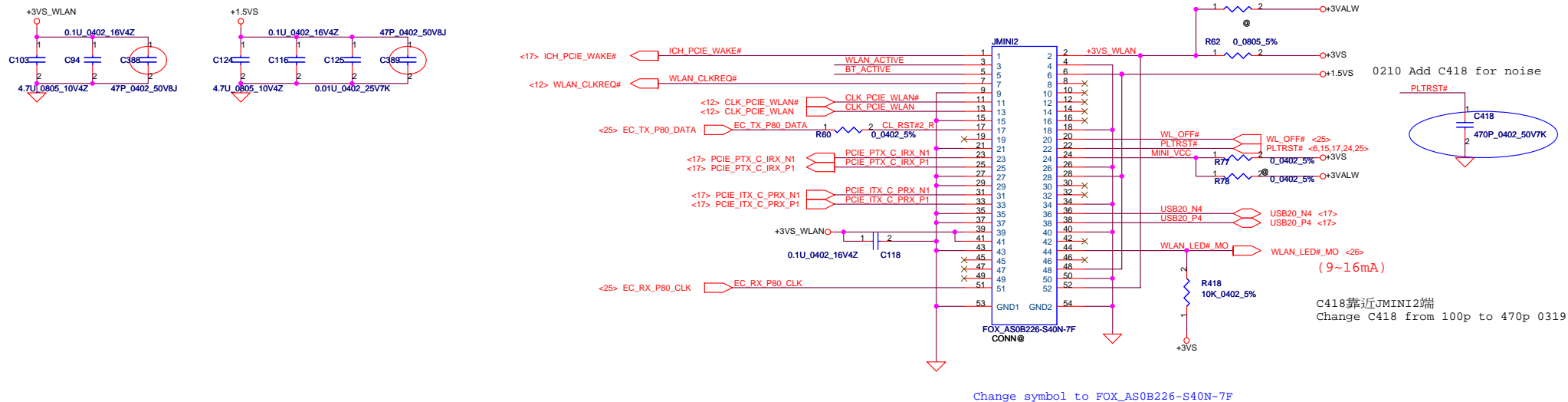


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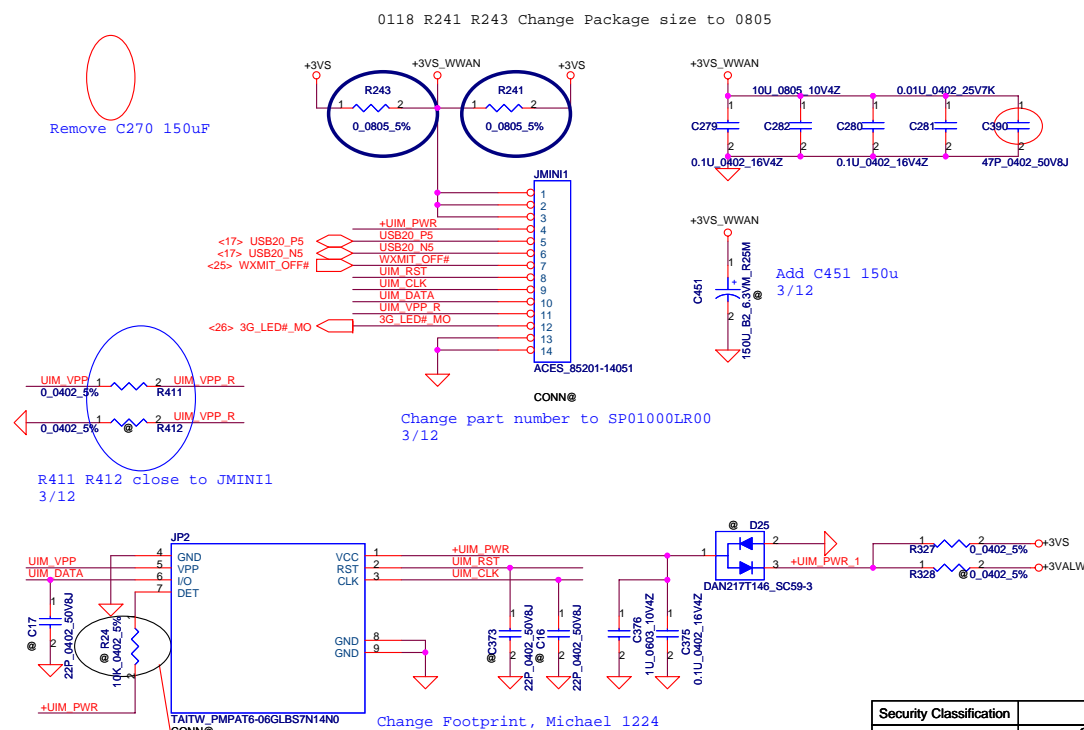




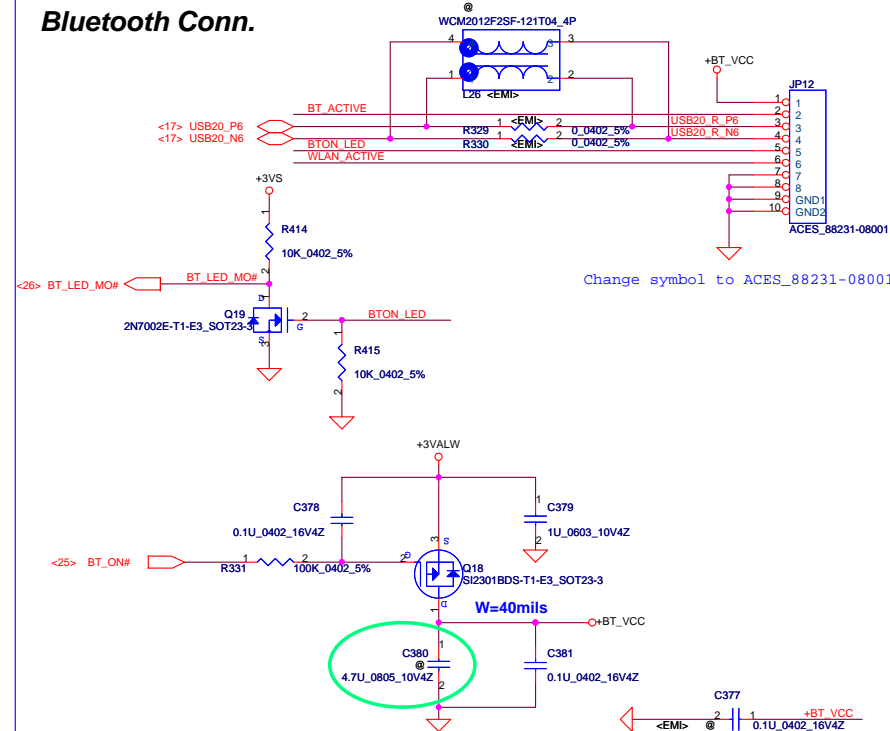
Mini-Express Card for WLAN



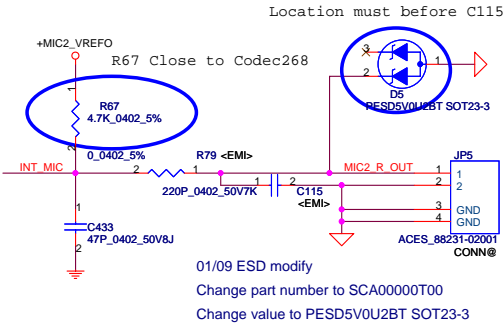
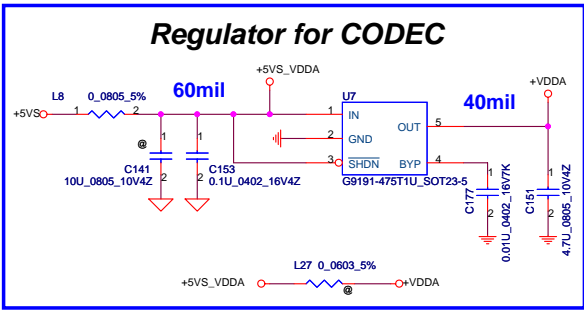
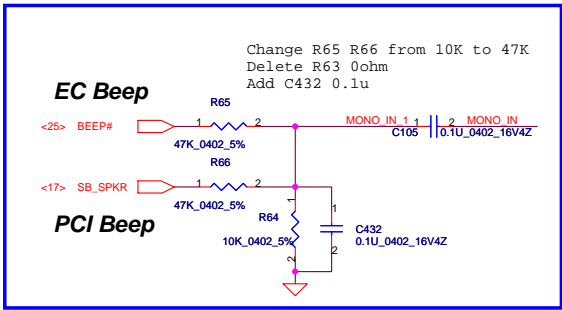
Mini-Express Card for 3G



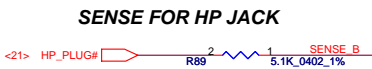
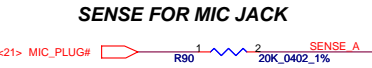
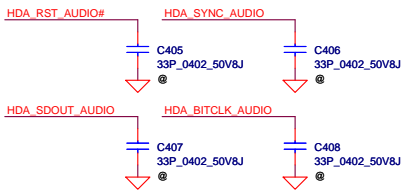
Bluetooth Conn.



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				Size	Document Number
				KTV00 LA-5241P	
				Date	Thursday, May 07, 2009
				Sheet	19 of 39



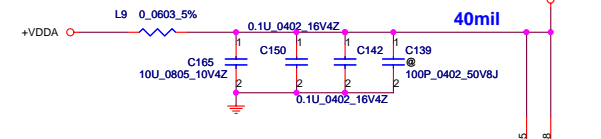
0120 Add C405 C406 C407 C408 for Noise



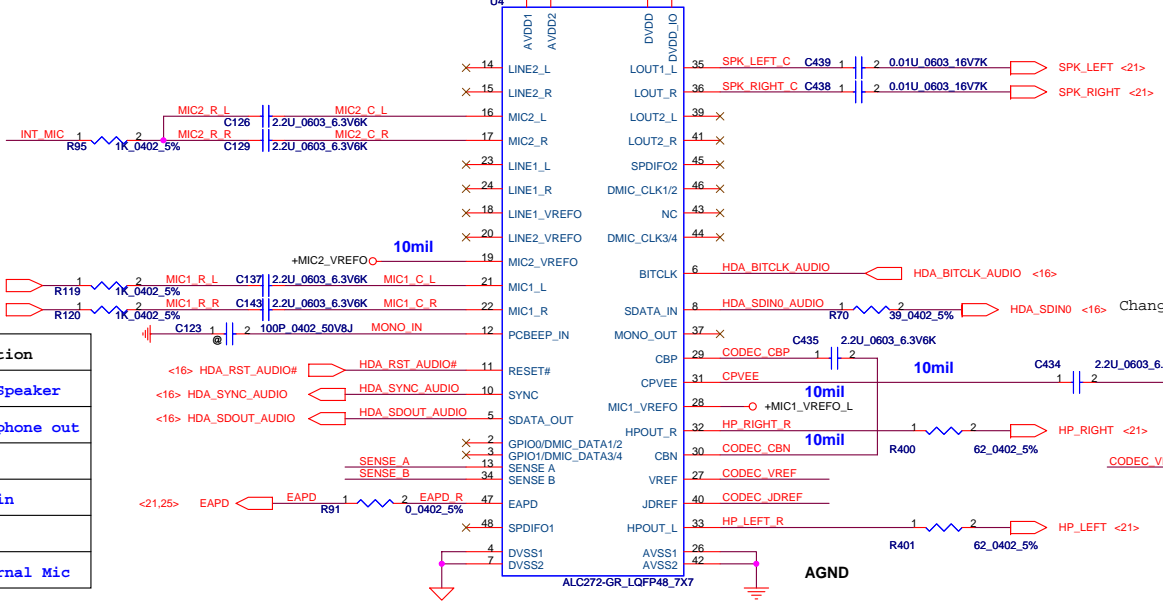
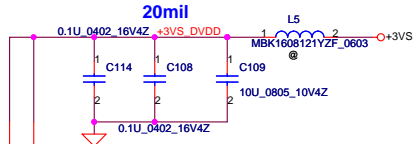
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	
MIC1(Pin21/22)	External	Mic in
MONO-OUT(Pin37)	Internal	
MIC2(Pin16/17)	Internal	Internal Mic

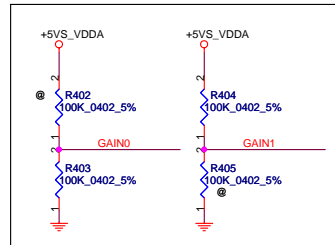
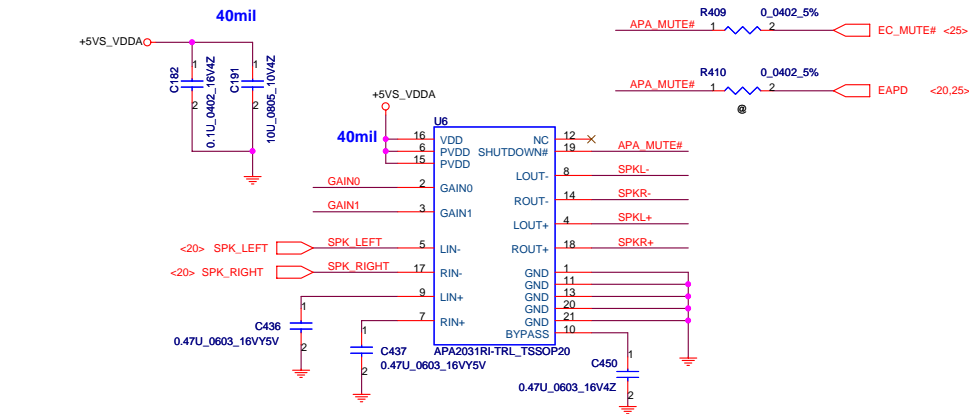
Sense Pin	Impedance	Codec Signals	Funncion
SENSE A	5.1K	LOUT1(PIN35,36)	SPEAKER
	10K	LINE1(PIN23,24)	LINE IN1
	20K	MIC1(PIN21,22)	MIC JACK
	39.2K	LOUT2(PIN39,41)	SPEAKER
SENSE B	5.1K	HPOUT(PIN 45, 46)	HP JACK
	20K	MIC2 (PIN16,17)	MIC
	39.2K	LINE2 (PIN 43, 44)	LINE IN2

Place C165 C150 near Pin25
C142 near Pin38



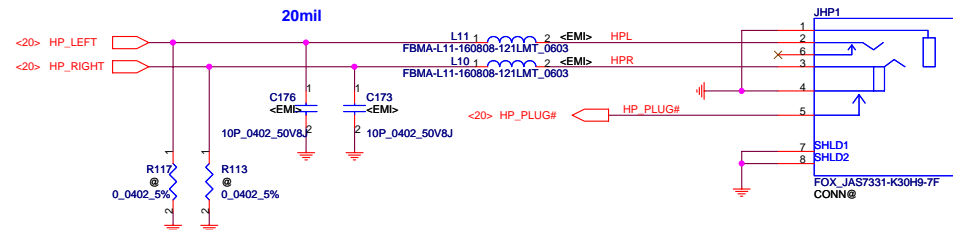
Place C109 C108 near Pin1
C114 near Pin9





GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

LINE Out/Headphone Out

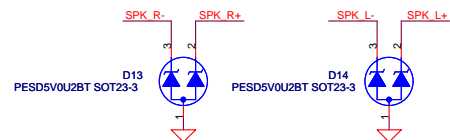


Int. Speaker Conn.



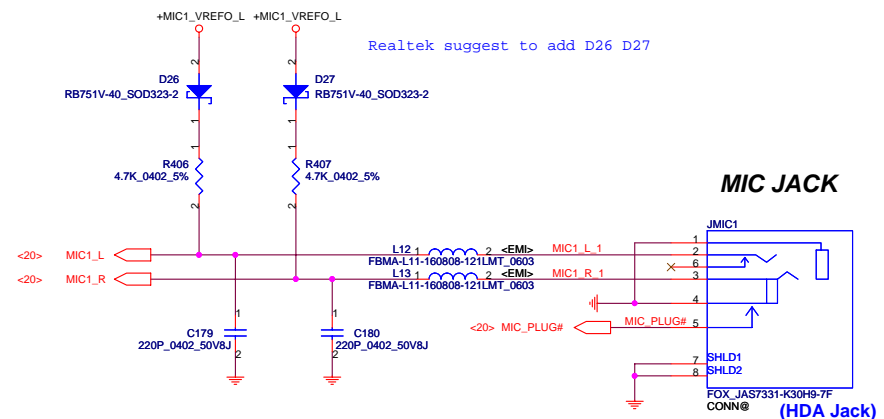
Change to SM01000AL00
20081114

Change Footprint, Michael 1224
Swap speaker pin definition, Michael 0304



01/09 ESD modify
Change part number to SCA00000T00
Change value to PESD5V0U2BT SOT23-3

Realtek suggest to add D26 D27

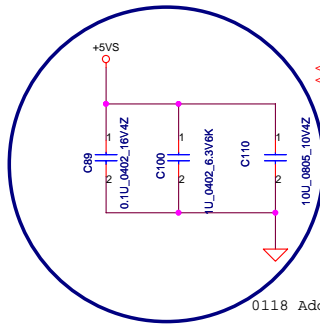


MIC JACK

(HDA Jack)

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				KTV00 LA-5241P	
				Date: Thursday, May 07, 2009	Rev 1.0
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SATA HDD Conn.



0118 Add C89 C100 C110 close to JSATA1

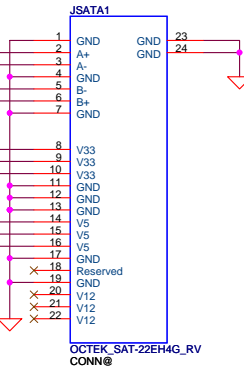
<16> SATA_ITX_C_DRX_P0
<16> SATA_ITX_C_DRX_N0

SATA_ITX_C_DRX_P0
SATA_ITX_C_DRX_N0

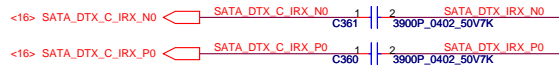
SATA_DTX_IRX_N0
SATA_DTX_IRX_P0

+3VS

+5VS



Change Footprint, Michael 1224



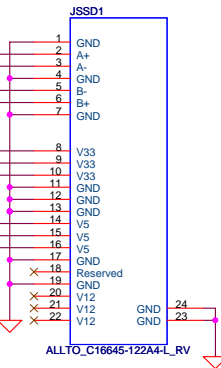
<16> SATA_ITX_C_DRX_P0
<16> SATA_ITX_C_DRX_N0

SATA_ITX_C_DRX_P0
SATA_ITX_C_DRX_N0

SATA_DTX_IRX_N0
SATA_DTX_IRX_P0

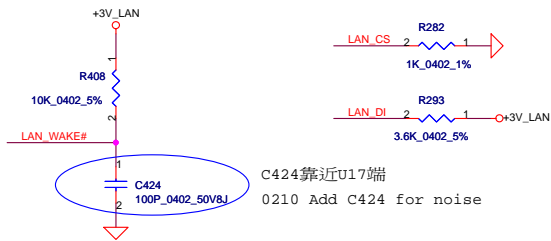
+3VS

+5VS

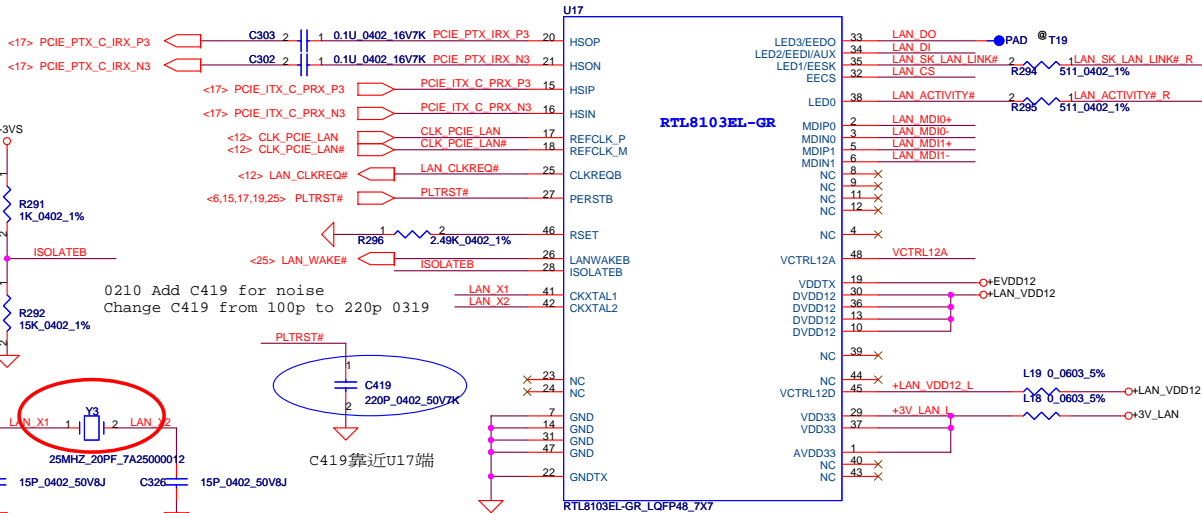


0121 Change Part Number DC010004R00

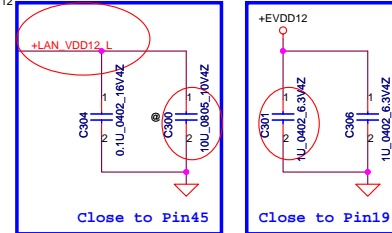
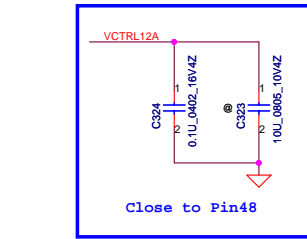
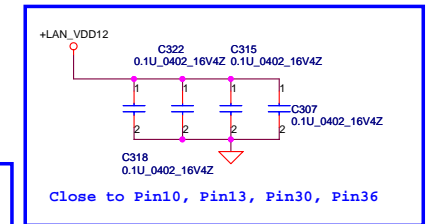
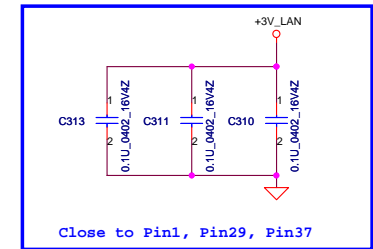
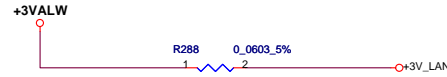
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Issued Date	2006/08/18	Deciphered Date	2008/09/20	Title	
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Change C884 from mount to @

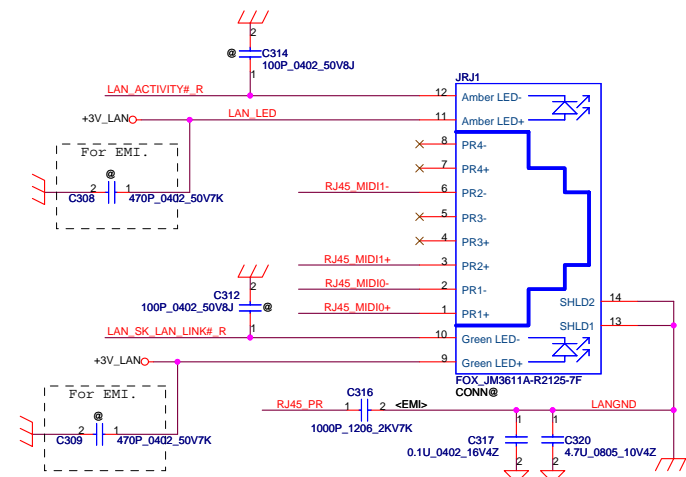
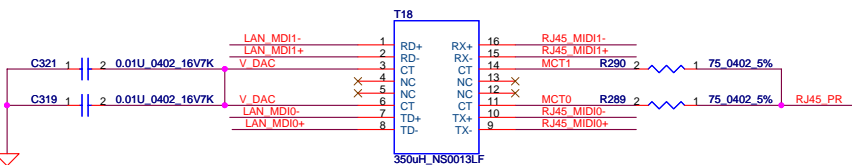


Change Y5 part number from SJ100006M00 to SJ100003300
Change Y5 footprint from Y_7A14300083_2P to Y_7A25000012_2P
Change Y5 value from 25MHZ 12PF X5H025000FC1H-H to 25MHZ_20PF_7A25000012
Change C325 C326 from 27p to 15p; 20090204



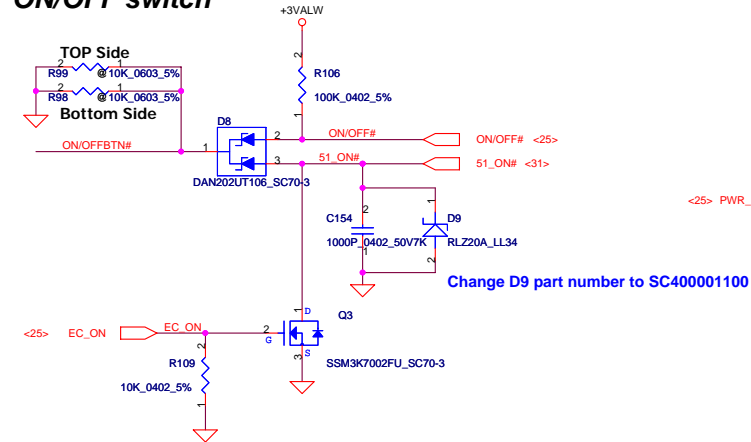
Change C833 from @ to mount

Change JRJ45 footprint FOX_JM3611A-R2125-7F_12P-T to FOX_JM36113-P2221-7F_12P



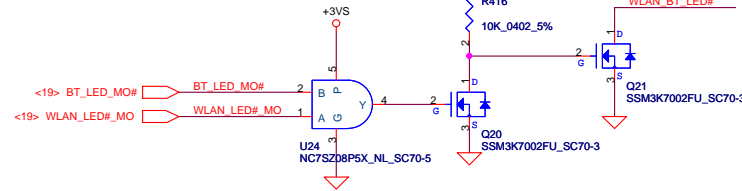
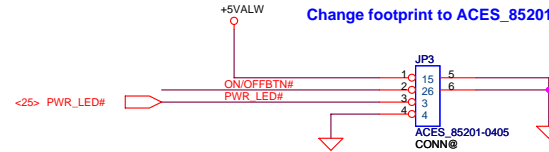
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Issued Date		2006/08/04		Deciphered Date		2008/09/20		Title		RTL 8103EL	
Size		Custom		Document Number		KTV00 LA-5241P		Rev		1.0	
Date		Thursday, May 07, 2008		Sheet		24		of		39	

ON/OFF switch

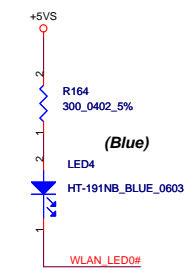


To PWR/B Conn.

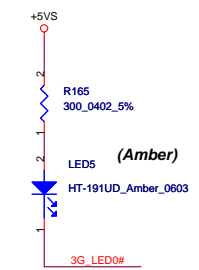
Change part number to SP01000KC00
Change value to ACES_85201-0405
Change footprint to ACES_85201-0405_4P



WLAN_LED

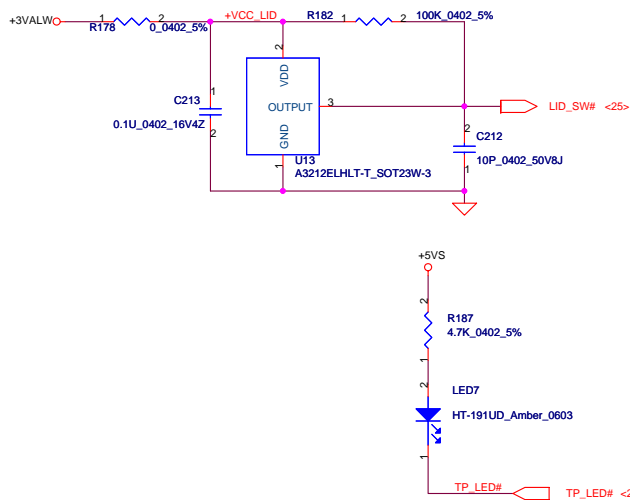
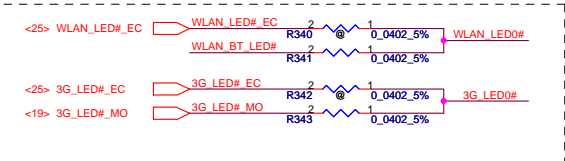


3G_LED

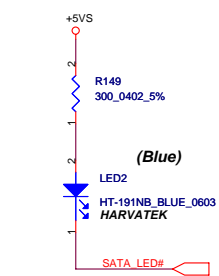


Add BOM structure @ for R340 R342
20090204

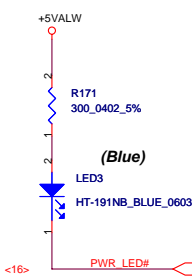
Option control LED



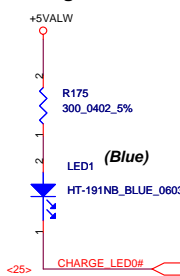
HDD LED



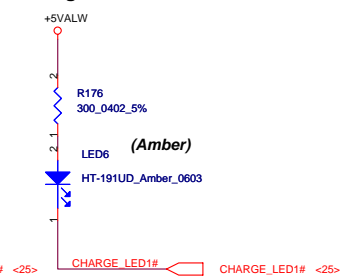
Power_LED



Charge_LED



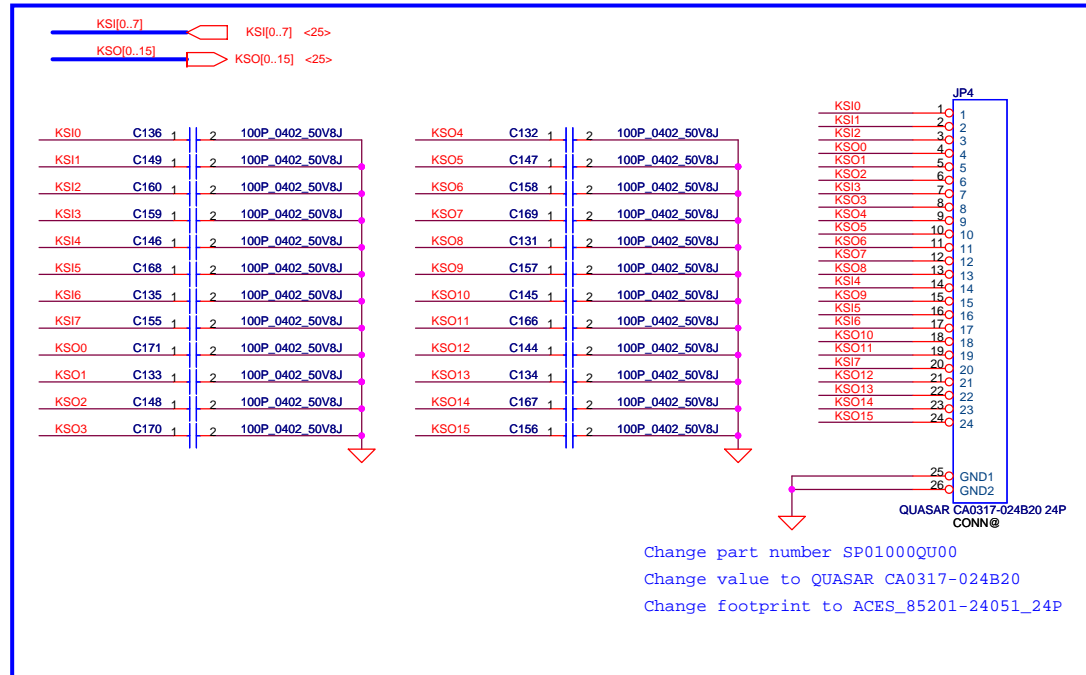
Charge_LED



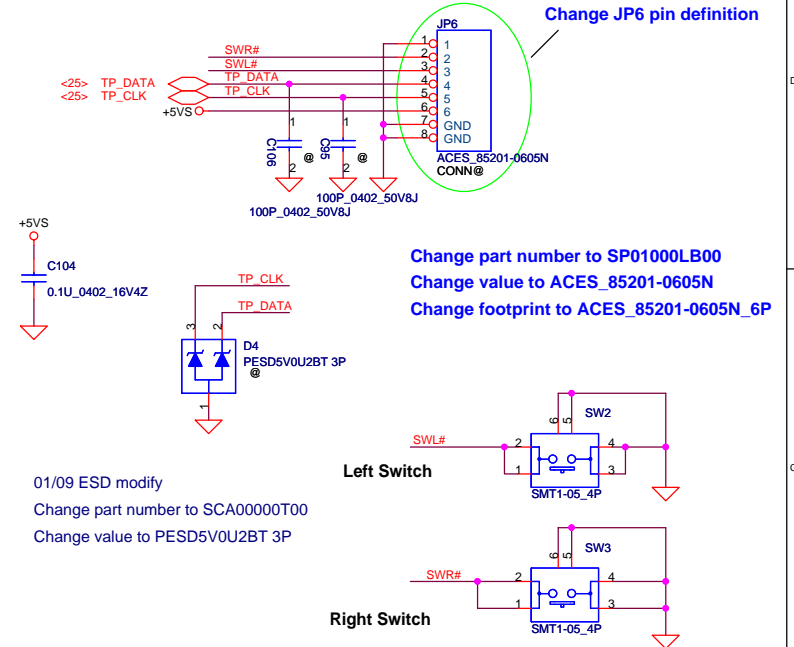
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18		Deciphered Date		2008/09/20		Title	
										LID SW/LED/CMOS	
										KTV00 LA-5241P	
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										Date: Thursday, May 07, 2009	
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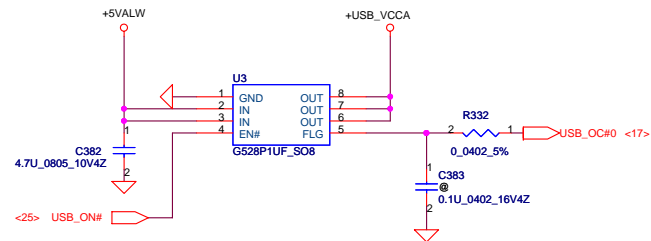
INT_KBD Conn.



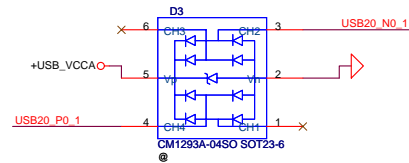
To TP/B Conn.



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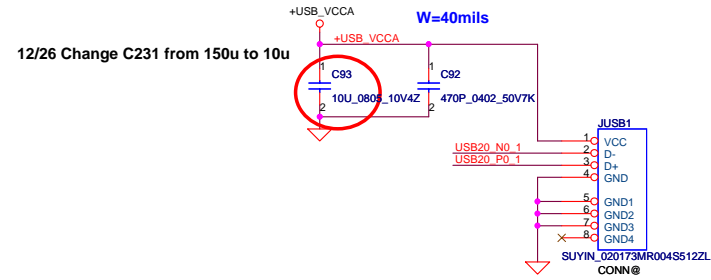


01/12 Change regulator circuit to G528P1

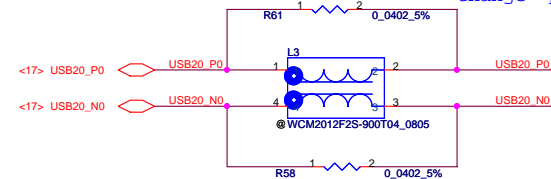


01/15 Change part value to CM1293A-04SO SOT23-6

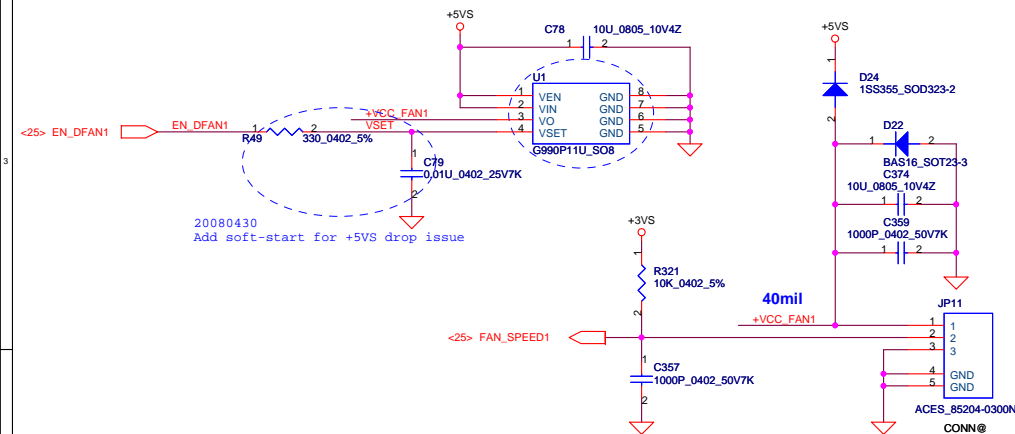
USB CONN. 1



Change part number to LTCX0016D00

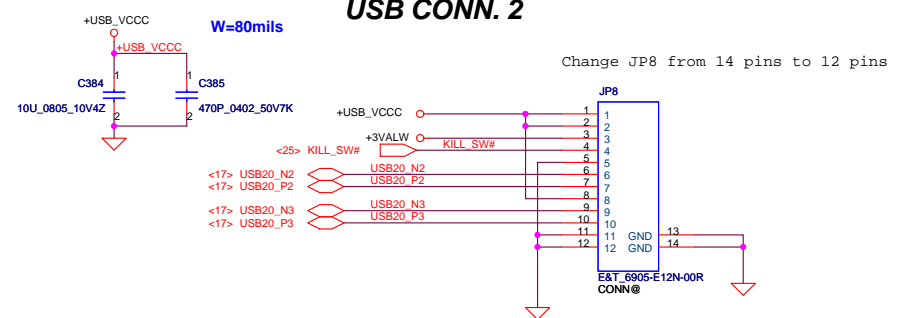


FAN1 Conn

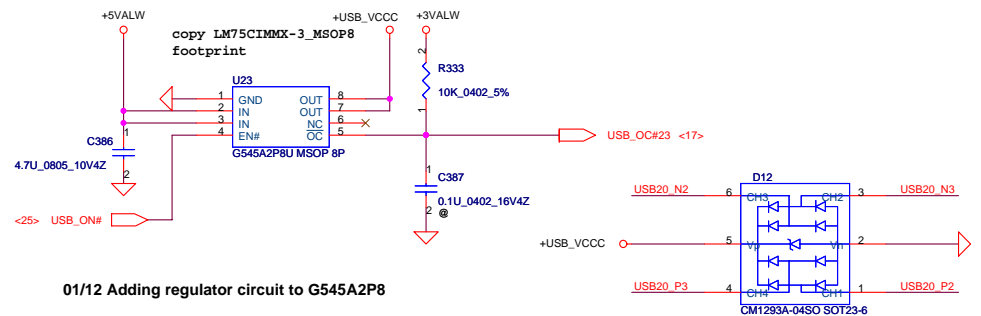


<25> EN_DFAN1

<25> FAN_SPEED1



Change JP8 from 14 pins to 12 pins

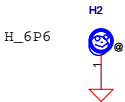


01/12 Adding regulator circuit to G545A2P8

01/15 Change part value to CM1293A-04SO SOT23-6

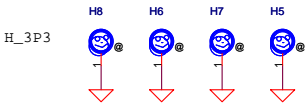
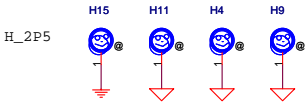
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2008/09/20	USB PORTS/FAN		
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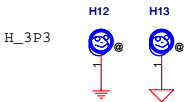


02/12 H2 change to H_6P6

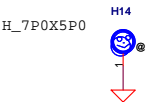
01/06 Add a H_2P7
Remove H1 01/22



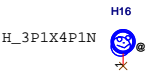
01/06 H_3P8 change to H_3P3



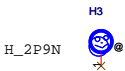
01/06 H_3P1 change to H_3P3



02/12 H_7P0X5P0N change to H_7P0X5P0



01/06 Add a H_3P1X4P1N



01/06 H_2P9N change to H_2P7N
03/11 H_2P7N change to H_2P9N

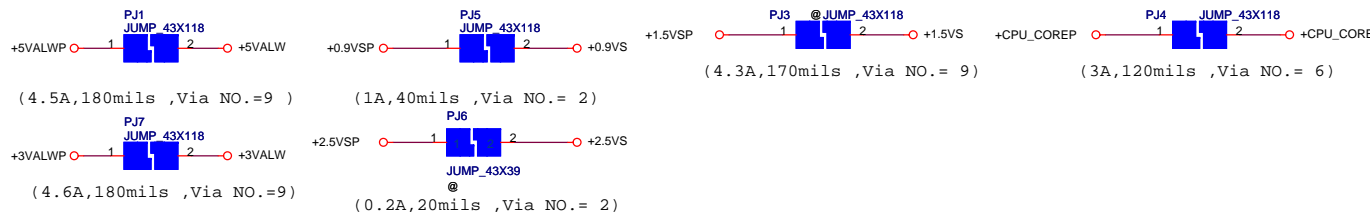
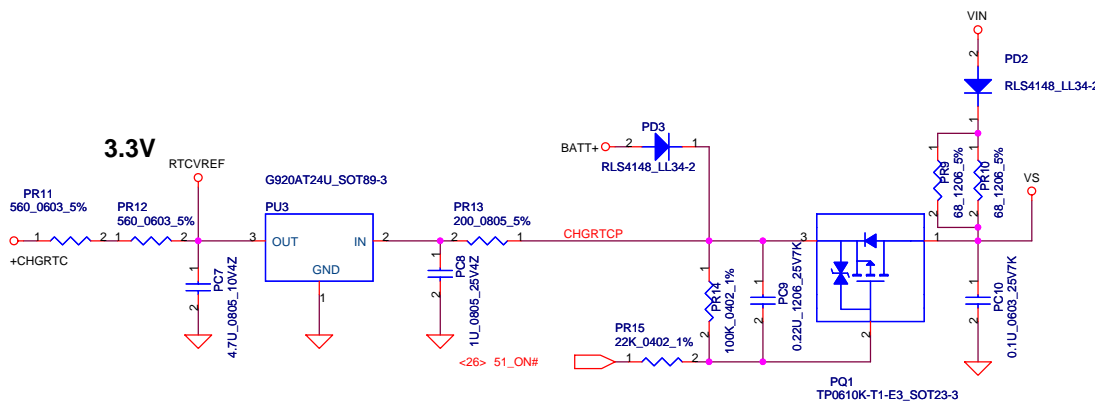
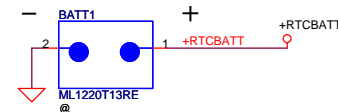
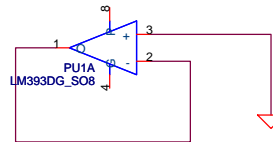
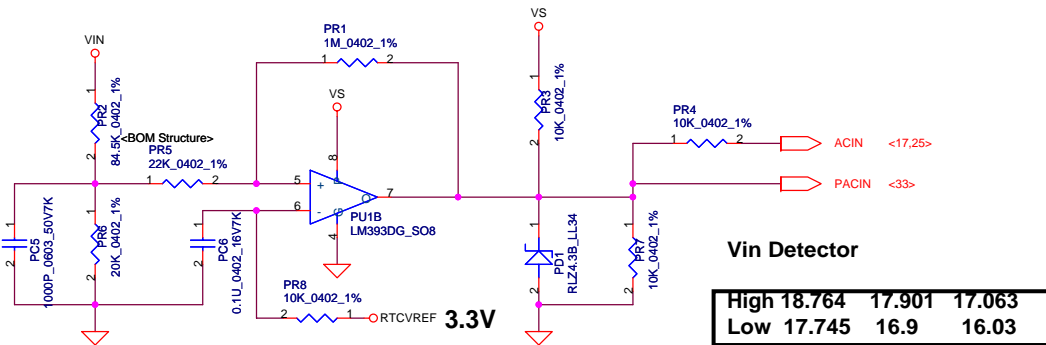
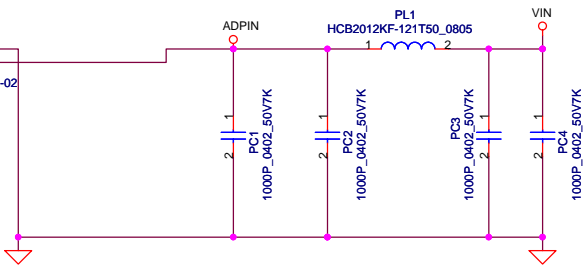


FIDUCIAL_C40M80

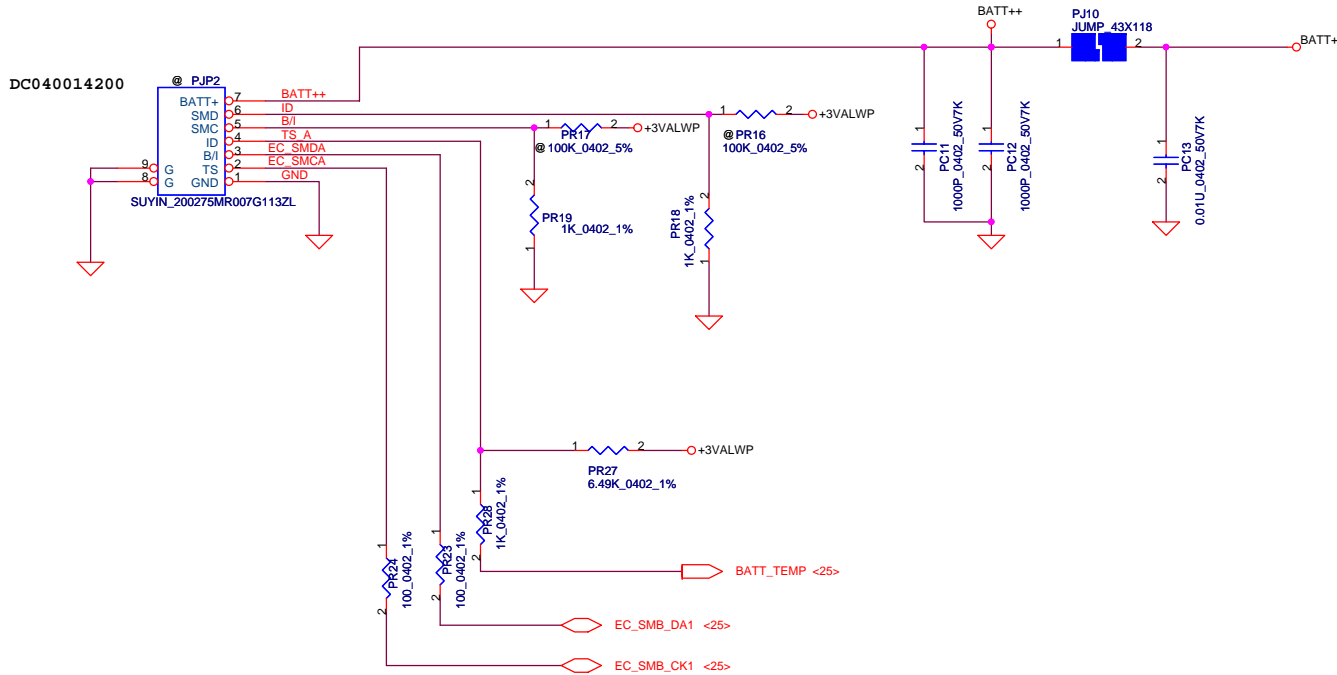
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Size	Document Number		Rev			
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DC301007D00

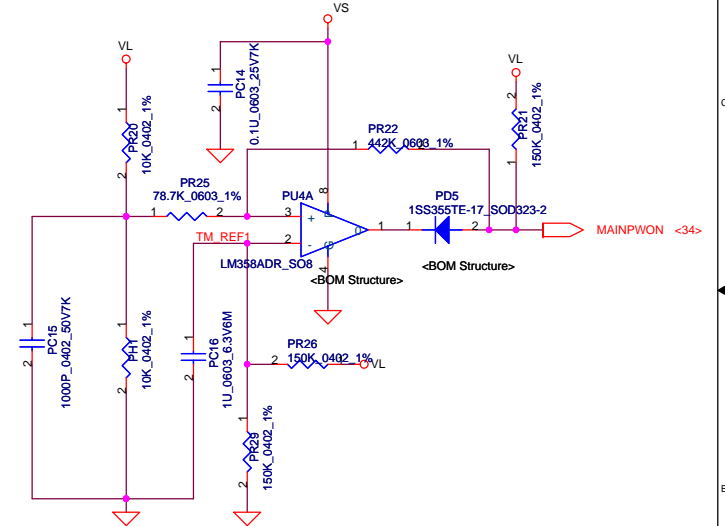
PJP1
@TARNG_TB2061HNR-02



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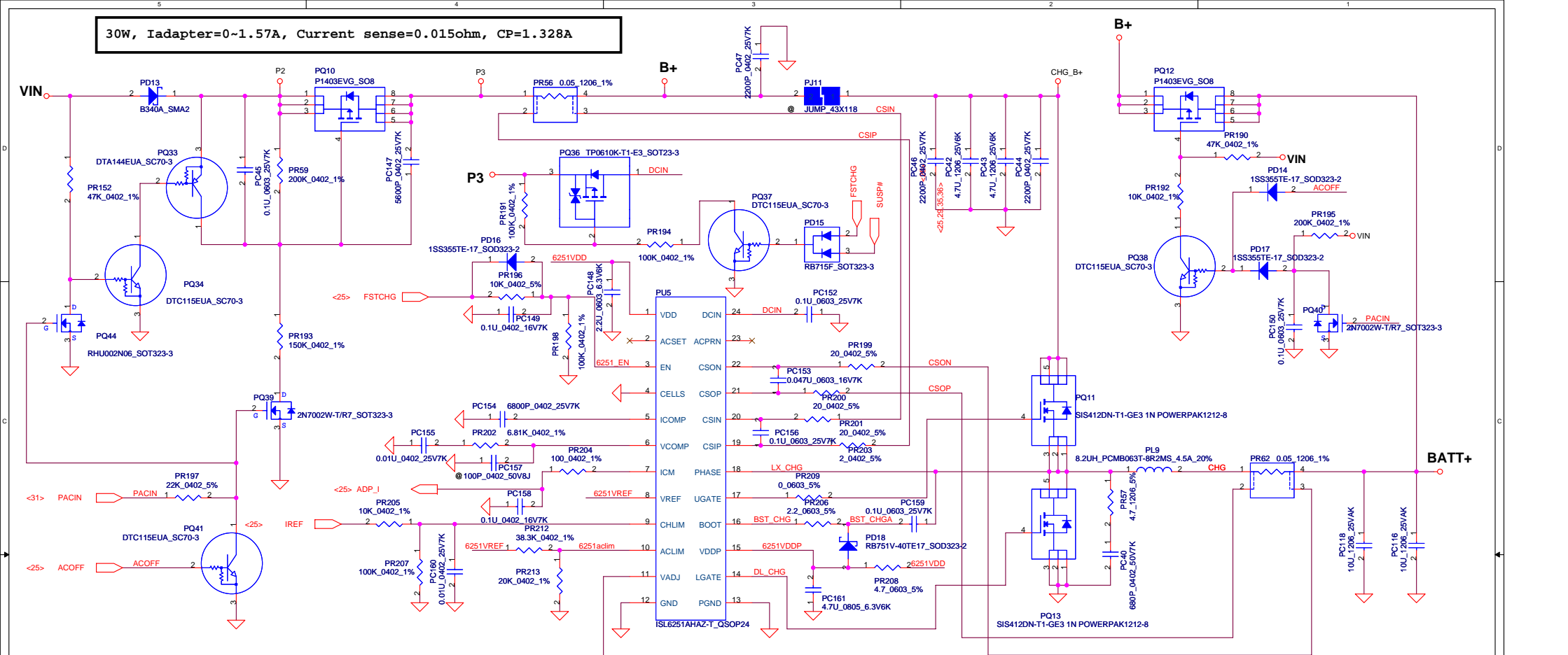


PH1 under CPU botten side :
CPU thermal protection at 89 degree C
Recovery at 70 degree C



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30W, Iadapter=0~1.57A, Current sense=0.015ohm, CP=1.328A



$I_{ada}=0\sim 1.58A(30W)$ $CP = 85\% \cdot I_{ada}$; $CP = 1.343A$

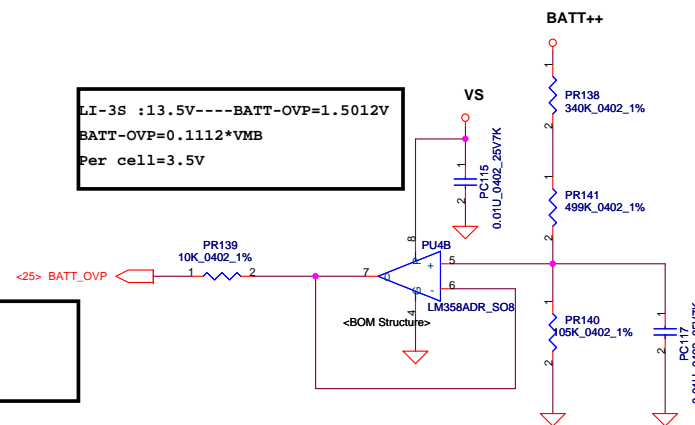
CP mode
 $V_{acli m}=2.39*(20K/(20K+38.3K))=0.8199V$
 $I_{i n p u t}=(1/0.05)((0.05*V_{acli m})/2.39+0.05)$
 where $V_{acli m}=0.8199V$, $I_{i n p u t}=1.343A$

CC=0.3~3A
IREF=1.1*Icharge
IREF=0.33V~3.3V

CALIBRATE#	Pre Cell
H	4.35V
L	3.99V

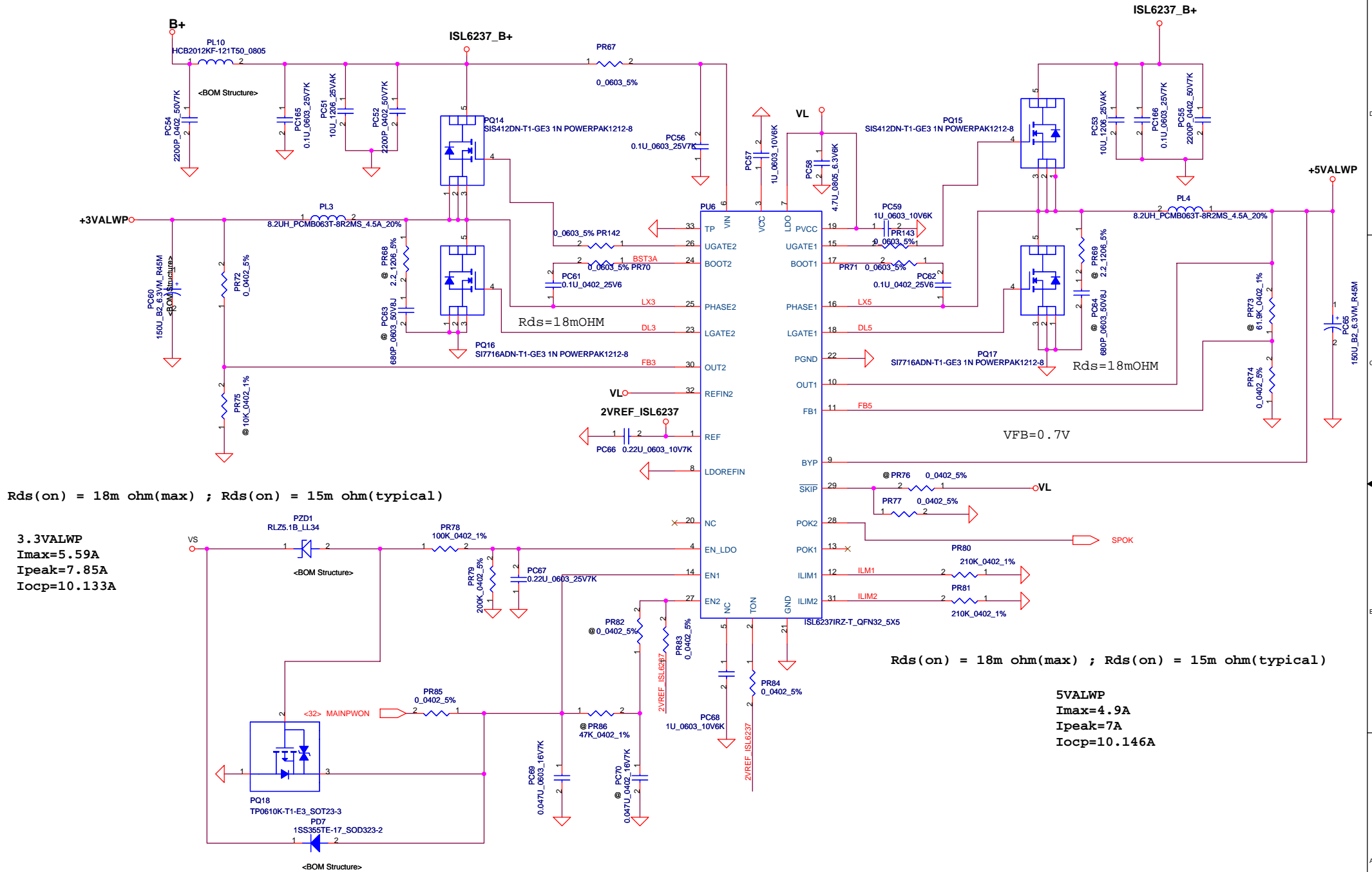
```
VADJ-->VREF-->4.41V
VADJ--->Ground--->3.39V
Vcell=(0.175*VADJ+3.99)
```

```
LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V
```

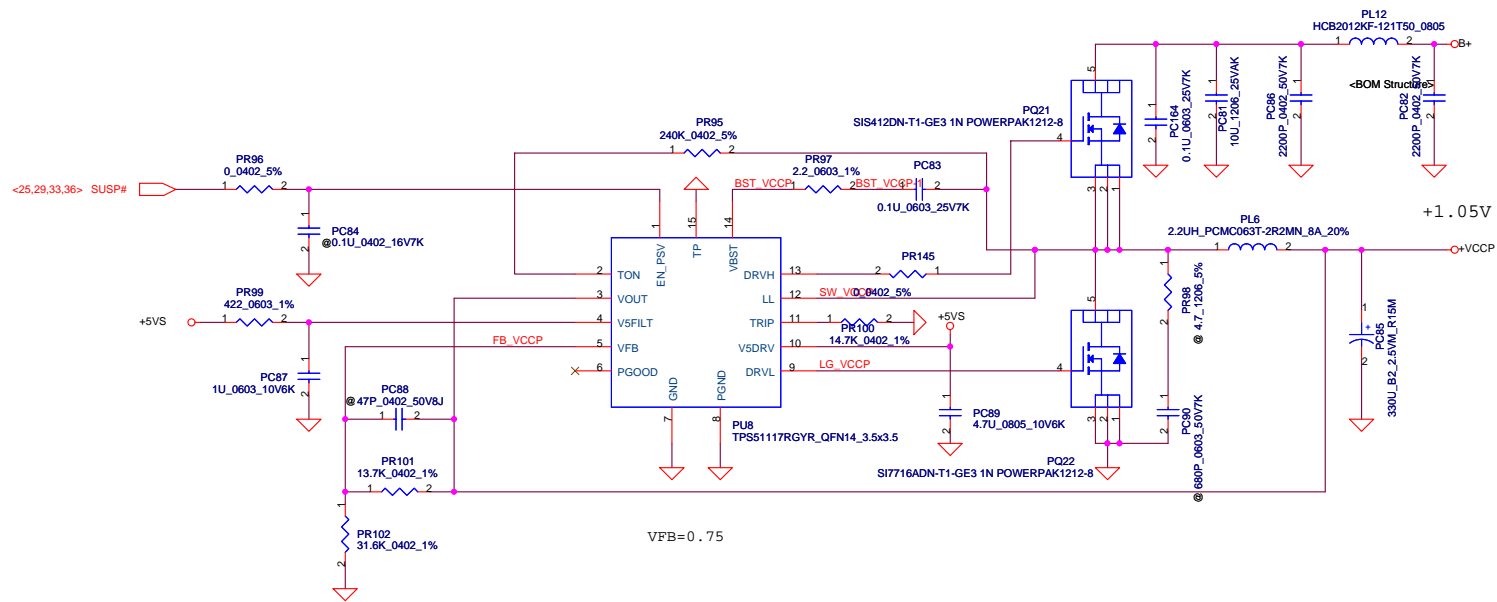
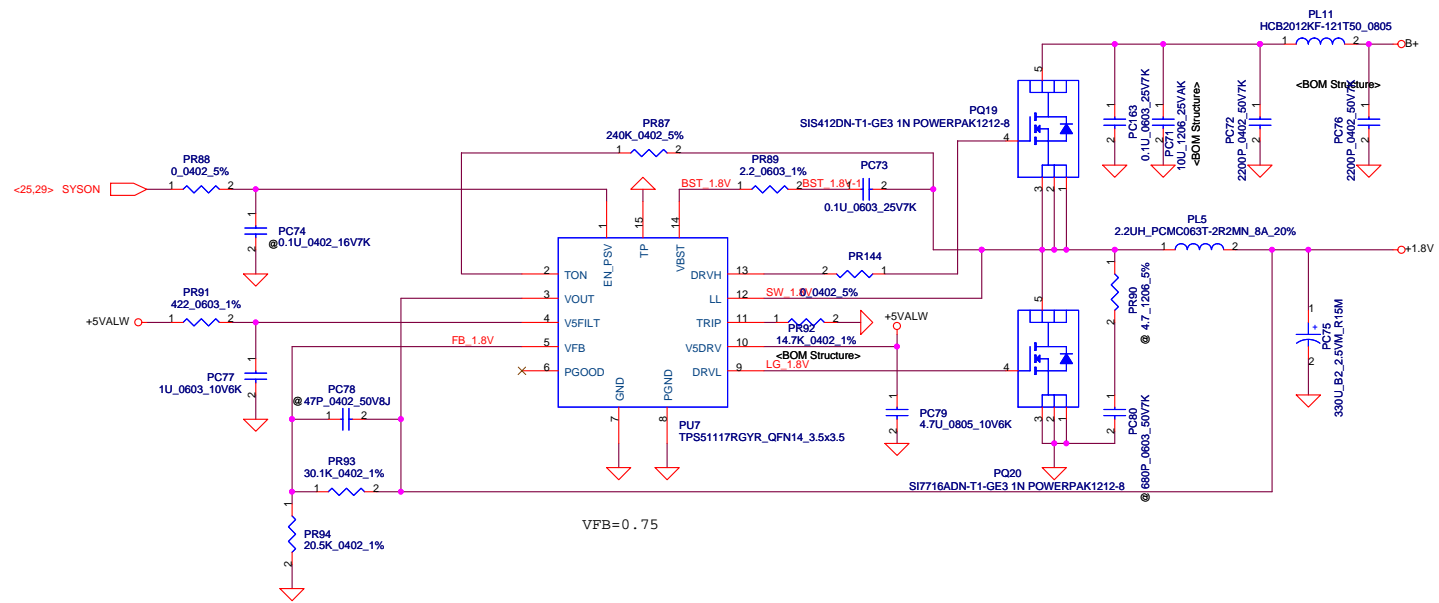


Charger ADJ	Calibrate#	PR211	PR220
4.2V	N/A	@	@
3.99V	L	301K	499K
4.35V	H	301K	499K

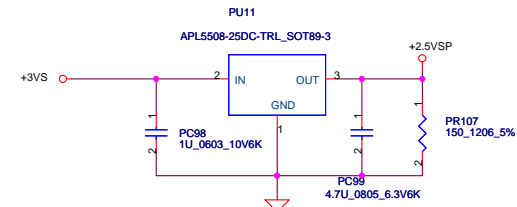
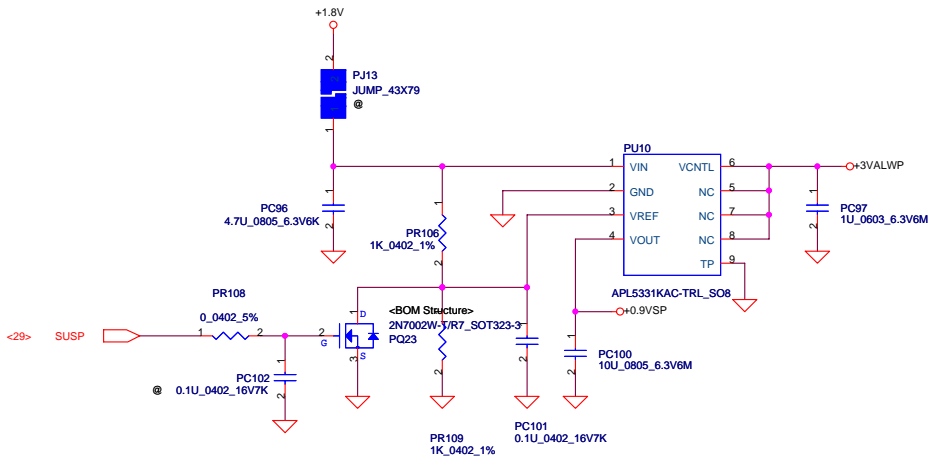
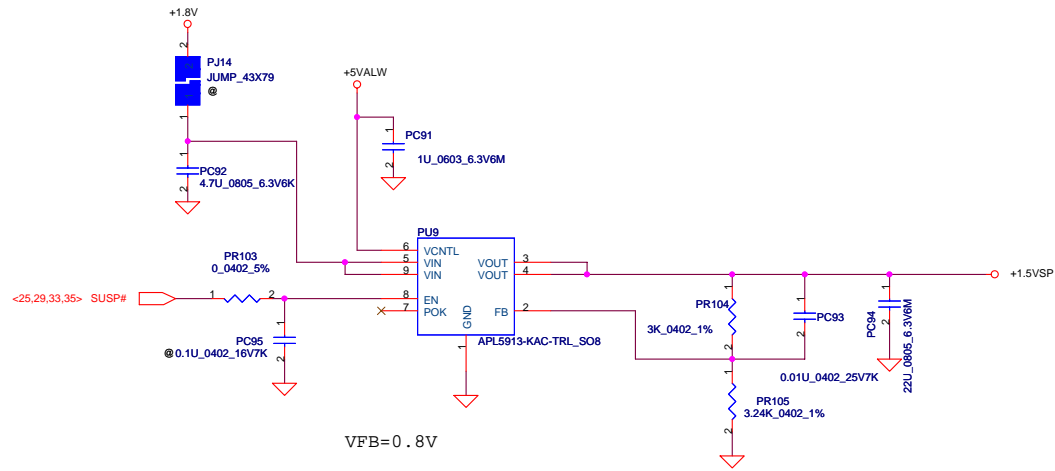
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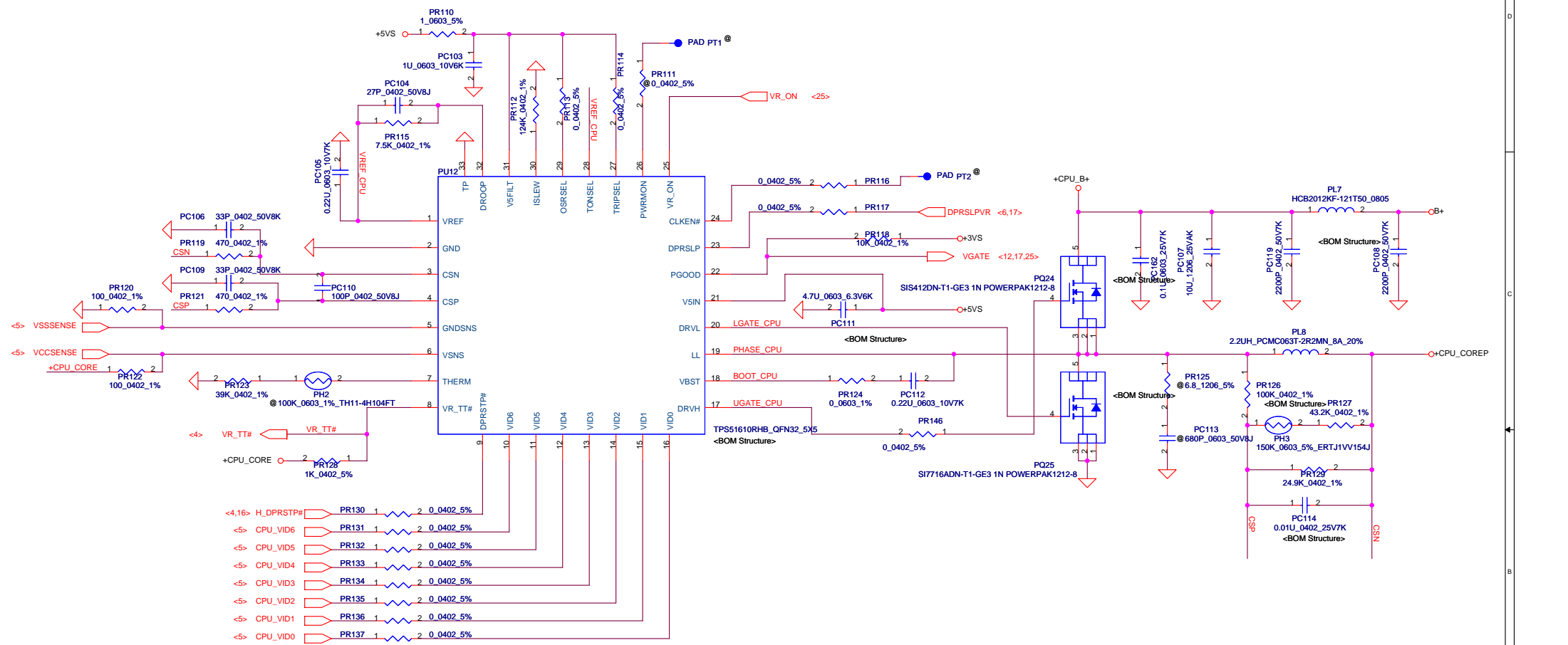
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				1.05VP/1.8VP					
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				2.5VSP/0.9VSP/1.5VSP			
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EVT

Reason for change

Solve back to back mos and discharge mos open toghter issue

The compnent is the some but vender are not

Modify 3,5V OCP set

The 150U_B2_6.3VM_R25M no 2nd source

modify load line

Add B+ bead for filter

Change 1.8V and VCCP OCP set

HW want to change 1.8V output voltage

HW want to change 1.5V output voltage

Modify CPU OCP set

Change KV value from 0.1091 to 10.019

DVT

Cost down

Modify list

Add PQ33,PQ34,PQ44,PR152

Change PQ23 to SB000006800 and change PD5,PD7 to SC100001K00.

Change PR80 ,PR81 to 210K

Change PC60,PC65 to S POLY C 150U 6.3V M B2 LESR45M PSL H1.9

Change PR115 10.5K to 7.5K

Change PJ12,PJ15,PJ16 to bead

Change PR92 and PR100 to 14.7K

Change PR94 to 20.5K

Change PR104 to 3K and PR105 to 3.24K

Change PR126 to 100K and PR129 to 24.9K

Change PR211 301K to 18.2K and PR220 499K to 31.6K

Change PH1 to SL200000U00

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- <8/25>
1. Update Power SCH
- <8/26>
1. Update Power SCH
2. Change
 D7 SC300000D00 to SC300000O00
3.Change
 C49、C50 SE071180K80 to SE071180J80
- <8/27>
1. Updata Power SCH
2. Modify
 RJ45 temp footprint FOX_JM3611A-R4122-7F_12P-T
- <8/28>
1. Updata Power SCH
- <9/1>
1. Updata Screw
- <9/5>
1. SWAP USB20_1 Signal.
- <9/10>
1. Remove Mini card pin55、pin56 的GND。
2. Change JREAD1.42、H26 to GNDA。
- <9/12>
1. Swap 3G ESD pin neme。
- <9/15>
1. Update Audio Jack footprint
2. Chcnge R641、R642 300ohm to 511ohm for Arthros。
3. Update L footprint。
- <9/16>
1. Update POWER SCH.
- <9/17>
1. Update POWER SCH.
2. ADD R380、R383 for ESD.
- <9/18>
1. Update ATHEROS 10/100 LAN <AR8132/AR8114>
- <9/24>
1. Change C870 0.1u to 1u.
- <9/26>
1. R88 change to 0ohm.

- <10/21>
1.Remove C389 for Audio can't detect issue on page 16
2.Add KSO1/KSO2 PU +3VALW on page25
3.Add R205 for schematic mistake on page 04
4.Change EC RST to PLTRST on page 25
5.Add J8 to cost down Audio LDO on page 20
6.Add R72 to reserve +3VALW for 3G on page 19
7.Reserve C238 for CRTDAC on page 10
8.Add R87 for Debug card on page 19
9.Change C108/C255 to 0.1uF for random hang issue
10.Change JP3 pin assignment on page 28
- <10/21>
1. Update Power SCH
- <10/29>
1. Audio AMP 10dB update to 6dB
- <11/3>
1. Update Power SCH
- <11/4>
1. Change R373、R374 to 56.2 ohm for DA-HP FSOV
2. Add C834、C851 for 3G noise
3. Change KB926 C1 to D2
4. Card reader RT5158E change to RT5159-GR
- <11/5>
1. Swap D7 pin define
- <11/10>
1. EC add R79、R90、R92 for SMS wakeup。

- <11/28>
1. Reserve C40、C46、C47、C233
2. R617 change to 0ohm for RTS5159
3. R68 200K change to 100K for sequence
4. Remove C47
5. Add D30 for LVDS
6. Add C55 0.1U
7. U2 Change to SA000017B00
 -because RT9715 Can't protect

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