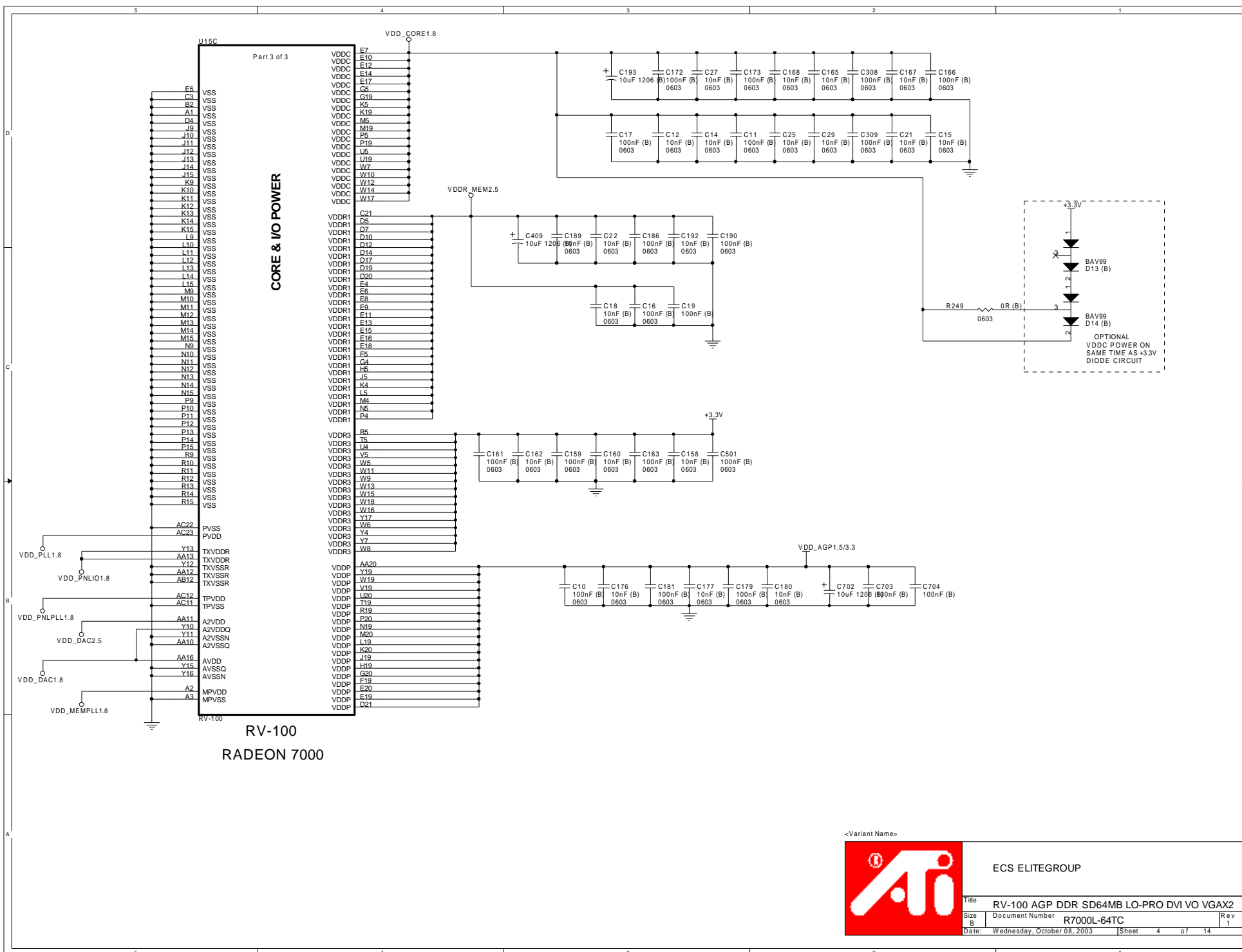


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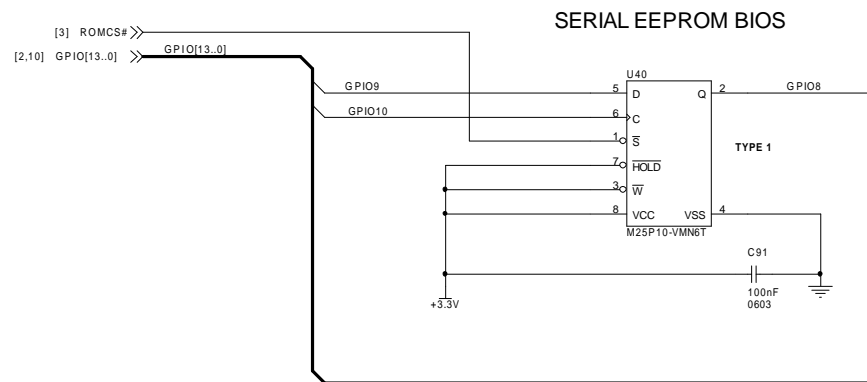


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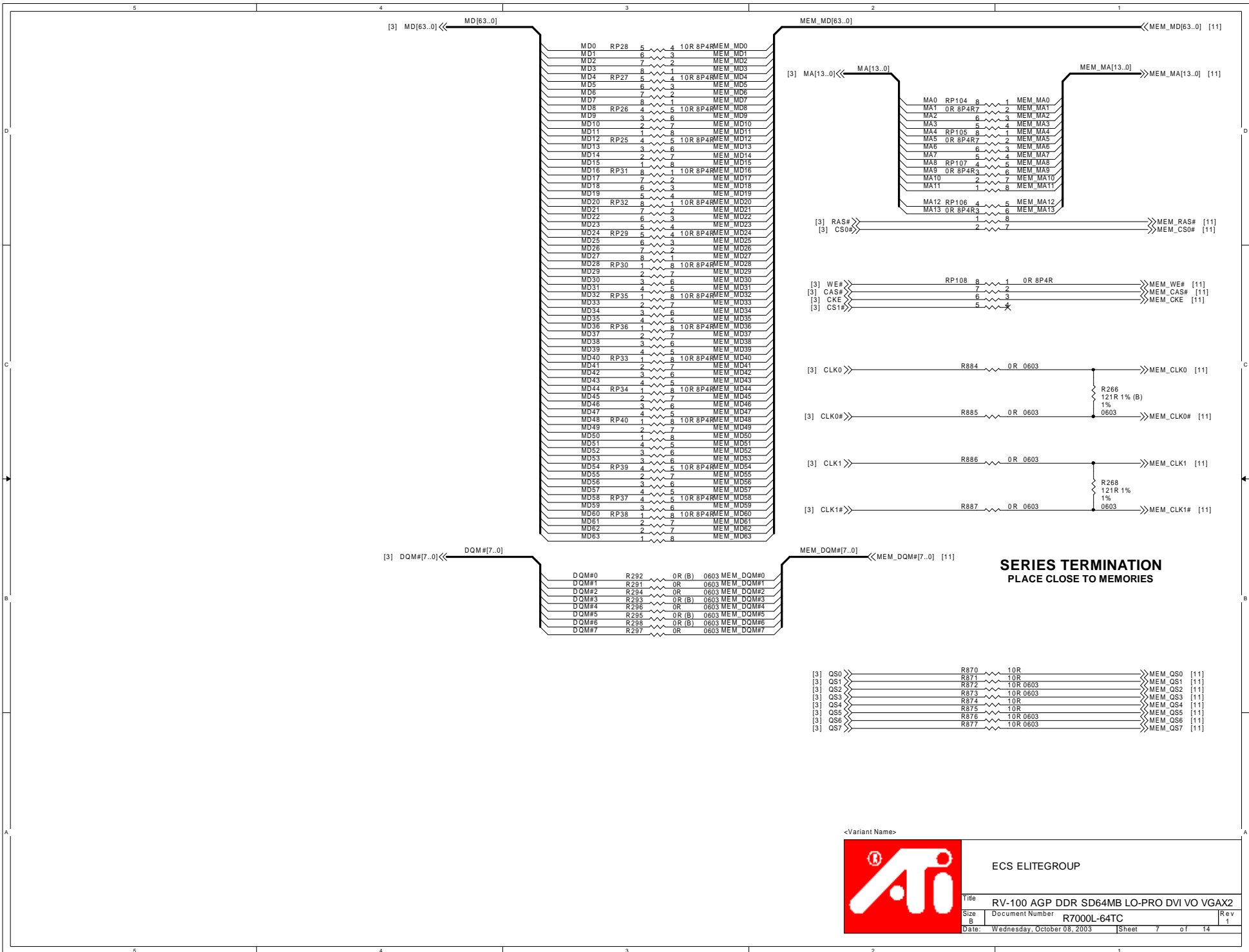


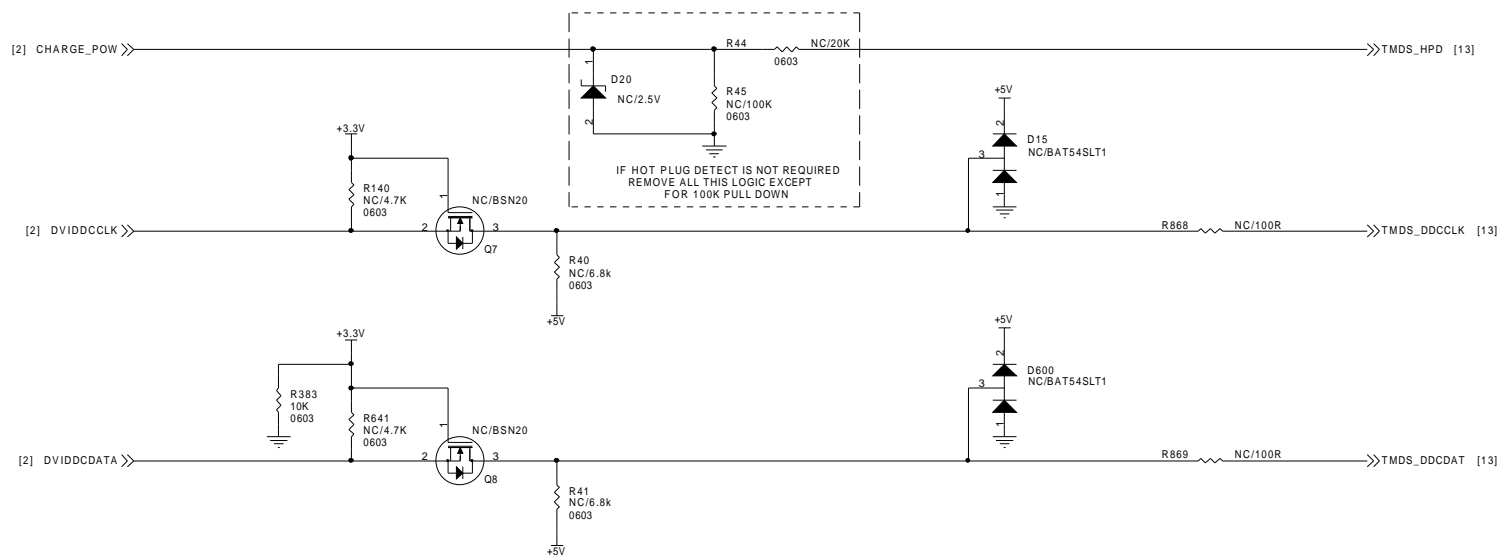
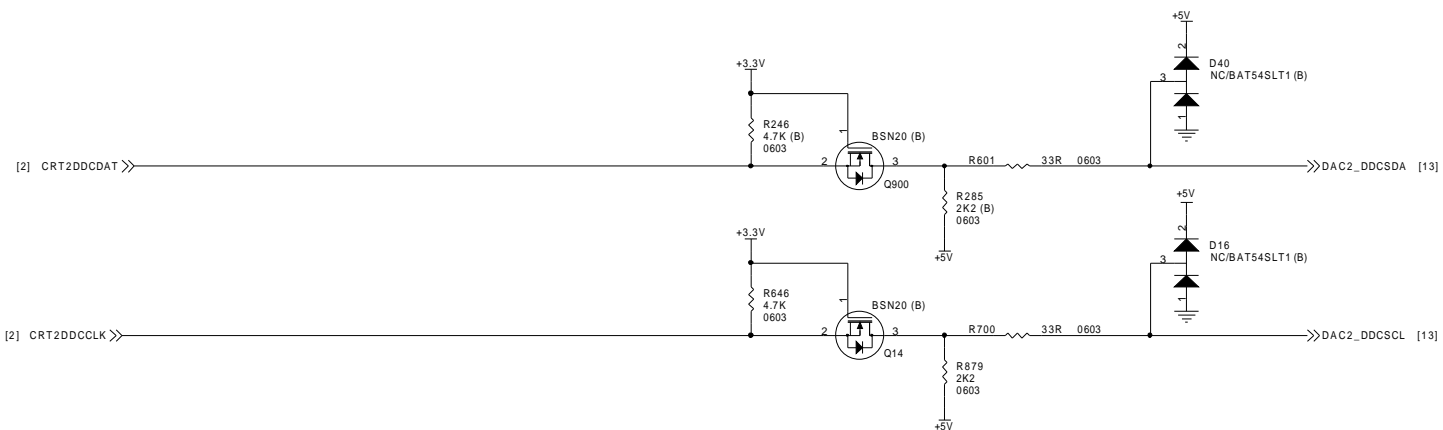
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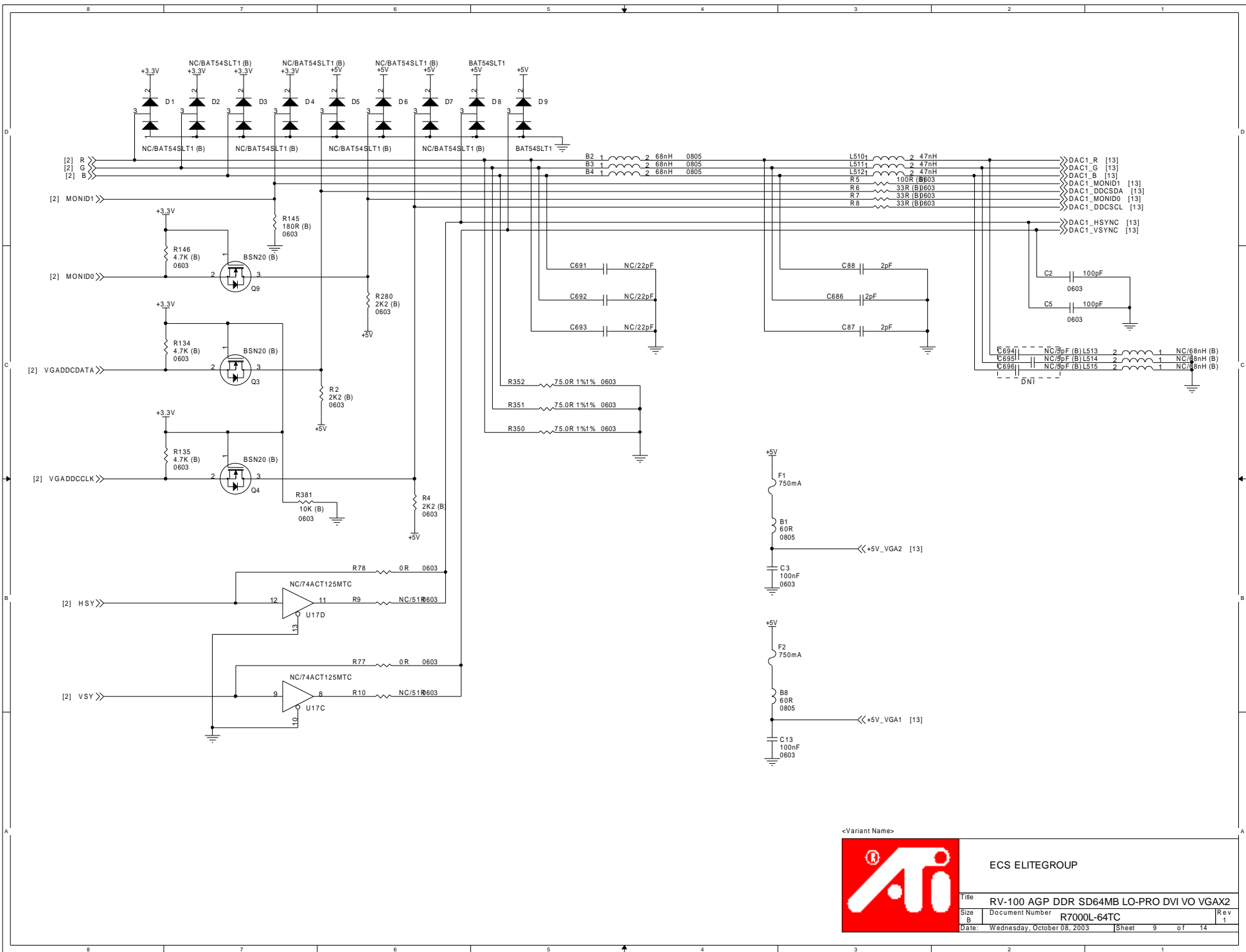
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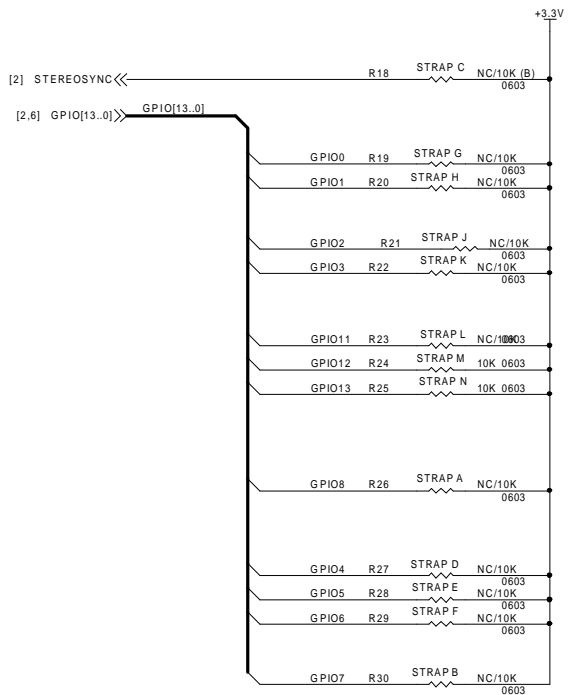


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STRAP C	INTERRUPT
DNI	ENABLE (DEFAULT)
10K	DISABLE

STRAP H	STRAP G	AGP1X CLOCK FEEDBACK PHASE ADJUSTMENT WRT REFCLK (CPUCLK)
DNI	DNI	(DEFAULT) SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP K	STRAP J	AGP CLOCK PHASE ADJUSTMENT BETWEEN X1 AND X2 CLOCK
DNI	DNI	(DEFAULT) SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP N	STRAP M	STRAP L	ROM IDENTIFIER
			SEE PINOUT SPEC FOR OPTION SETTINGS

STRAP A	ID DISABLE
DNI	NORMAL OPERATION
10K	SHUT DOWN

STRAP D	STRAP E	STRAP F	BUS_TYPE
			SEE PIN BASED STRAPS IN PINOUT SPEC


STRAP B	VGA
DNI	ENABLE (DEFAULT)
10K	DISABLE

NOTE: THE RV-100 SUPPORTS THE USE OF STRAP RESISTORS (AS AN ALTERNATIVE TO CUSTOMIZED BIOS) TO CONFIGURE CERTAIN ASPECTS OF THE GRAPHICS SUBSYSTEM. THE USE OF EXTERNAL STRAPS PROVIDES ADDED FLEXIBILITY AND EASE OF FUTURE UPGRADE. STRAPPED VALUES ARE LOADED INTO INTERNAL REGISTERS ON THE FIRST PCI COMMAND AFTER RESET# IS INACTIVE.

NOTE:  
THE I/O BUFFERS USE INTERNAL PULLDOWN RESISTOR. THIS DICTATES THE FOLLOWING STRAP CONFIGURATION:  
STRAP TO VCC VIA 10K RESISTOR.  
THIS PROVIDES THE LOGIC LEVELS SHOWN:  
'0' WHEN 10K RESISTOR NOT INSTALLED  
'1' WHEN 10K RESISTOR INSTALLED.

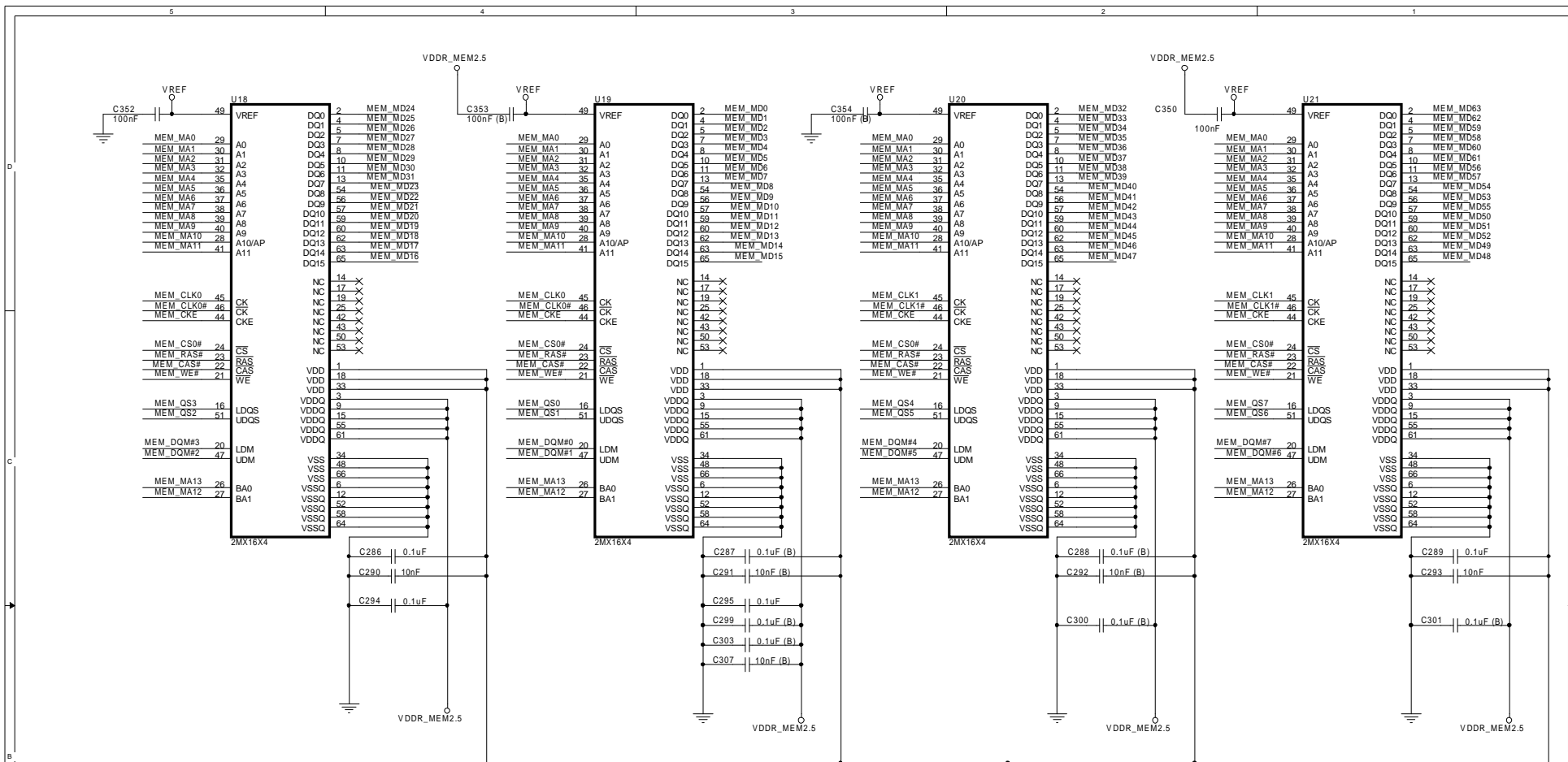
OPTION STRAPS

<Variant Name>



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## Rank 0 of 64MB DDR 8X16 SDRAM

[7] MEM\_QS0 << MEM\_QS0  
[7] MEM\_QS1 << MEM\_QS1  
[7] MEM\_QS2 << MEM\_QS2  
[7] MEM\_QS3 << MEM\_QS3  
[7] MEM\_QS4 << MEM\_QS4  
[7] MEM\_QS5 << MEM\_QS5  
[7] MEM\_QS6 << MEM\_QS6  
[7] MEM\_QS7 << MEM\_QS7

[7] MEM\_CLK1 << MEM\_CLK1#  
[7] MEM\_CLK1# << MEM\_CLK0  
[7] MEM\_CLK0 << MEM\_CLK0#  
[7] MEM\_CLK0# << MEM\_CLK0

[7] MEM\_CS0# << MEM\_CS0#  
[7] MEM\_RAS# << MEM\_RAS#  
[7] MEM\_CAS# << MEM\_CAS#  
[7] MEM\_WE# << MEM\_WE#  
[7] MEM\_CKE << MEM\_CKE

[7] MEM\_DQM# [7..0] << MEM\_DQM# [7..0]

[7] MEM\_MD [63..0] << MEM\_MD [63..0]

[7] MEM\_MA [13..0] << MEM\_MA [13..0]

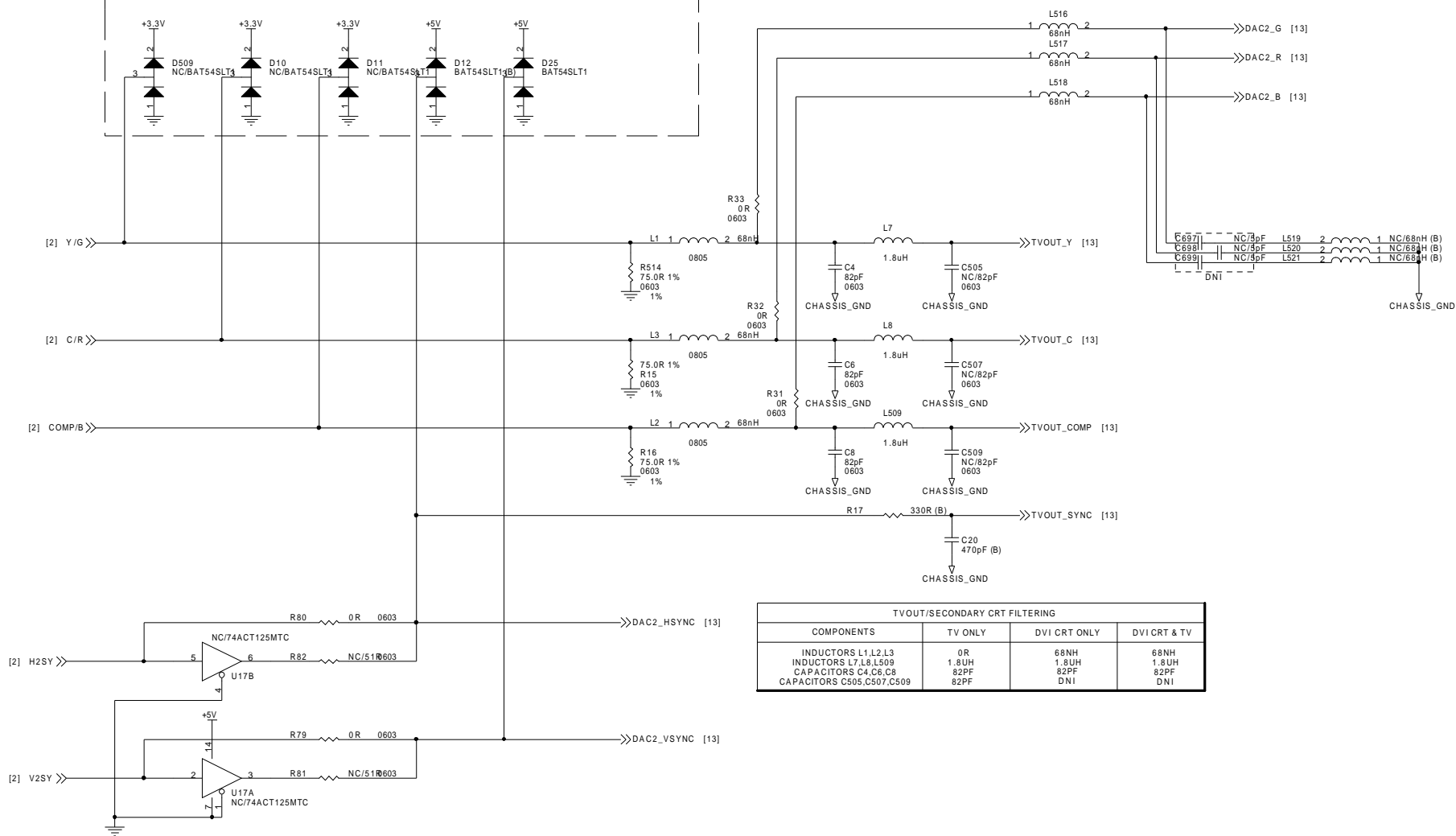
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# OPTIONAL ESD PROTECTION DIODES



TVOUT/SECONDARY CRT FILTERING			
COMPONENTS	TV ONLY	DVI CRT ONLY	DVI CRT & TV
INDUCTORS L1,L2,L3	0R	68NH	68NH
INDUCTORS L7,L8,L509	1.8UH	1.8UH	1.8UH
CAPACITORS C4,C6,C8	82PF	82PF	82PF
CAPACITORS C505,C507,C509	82PF	DNI	DNI

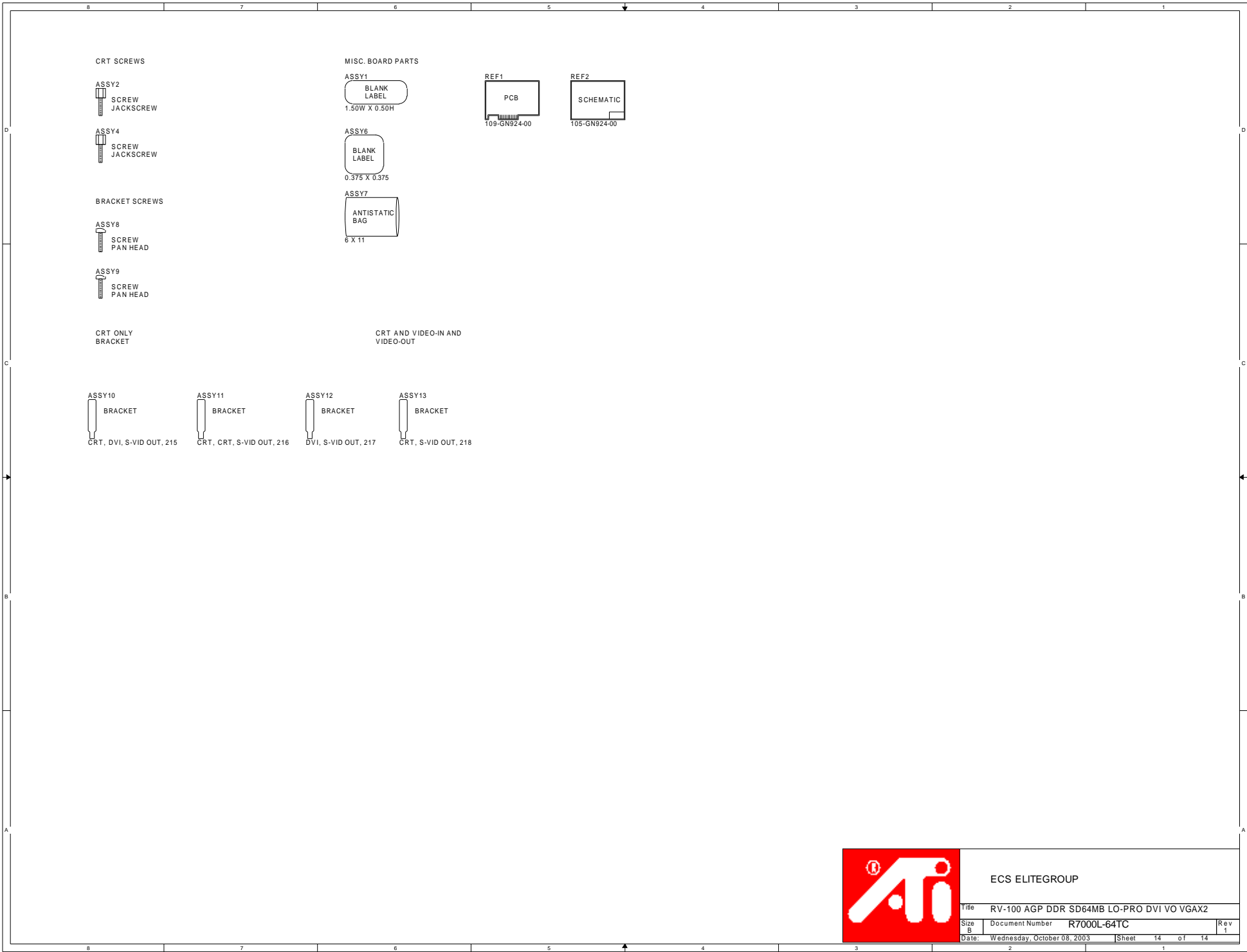
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Schematic No.  
CRT+DVI+TVOUT

Date:  
**Wednesday, October 08, 2003**

## REVISION HISTORY

Rev 1

1