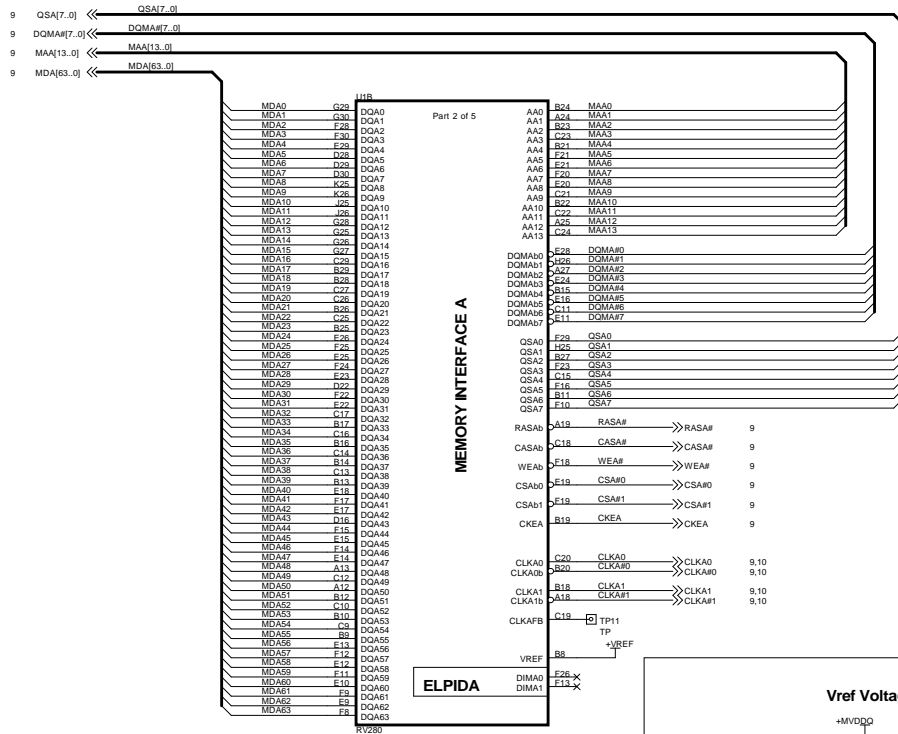
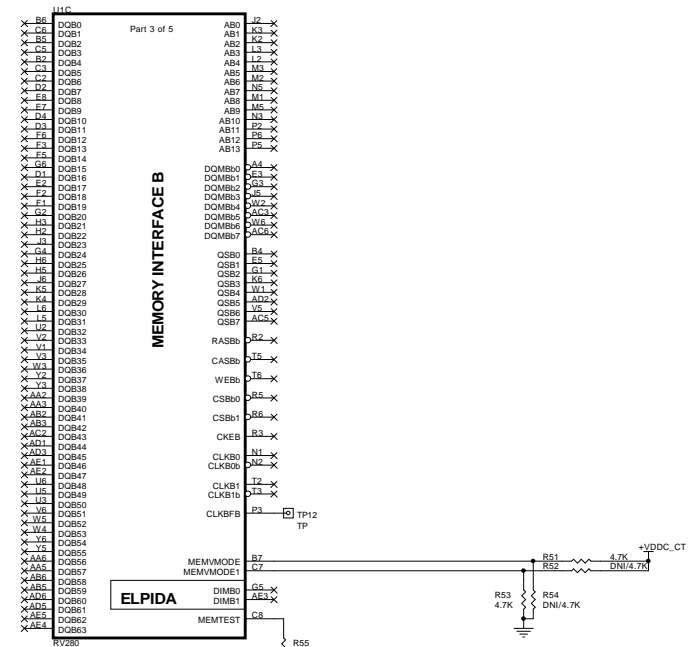


MEMORY CHANNEL A



MEMORY CHANNEL B



MEMMODE[1:0]	MEMORY I/O VOLTAGE	
01	2.5V (DDR)	Default
10	1.8V (DDR)	
11	3.3V (SDR)	



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Regulator for VDDC (ASIC Core)

Vin = 3.3V AGP

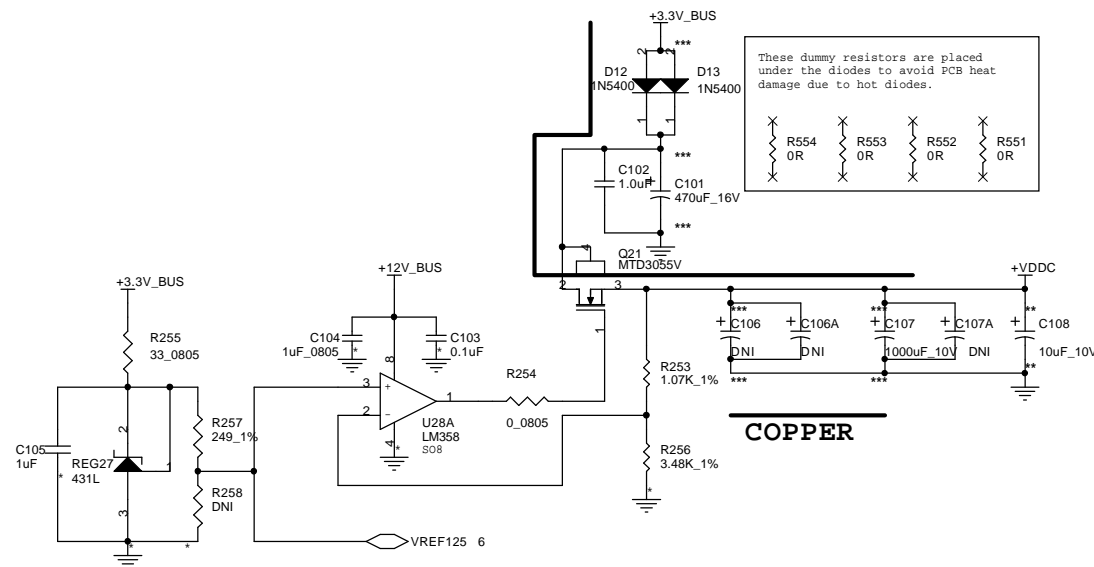
Vout = 1.5V ~ 1.62V

Iout = 4A MAX (load consumption)

Iout = 2.5A MAX (Power rail consumption)

Cout1 470uF thru hole capacitor (P/N 4051047700) has 30mR ESR where as 470uF SMT (P/N 4262047700) capacitor has 150mR ESR. For current below 4.5A, 1 thru 470uF is enough.

*** Indicate number of via required for the connection



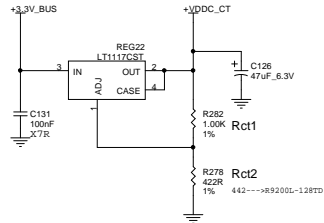
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Regulator for VDDC_CT (Core Transform) and AVDD/A2VDDQ/AVDDDI/A2VDDDI TXVDDR, LVDDRx, MPVDD

Vin = 3.3V AGP
Vout = 1.8V
Iout = 350mA + 100mA + 50mA = 500mA MAX
Iout = 600mA MAX (with PVDD/TPVDD)

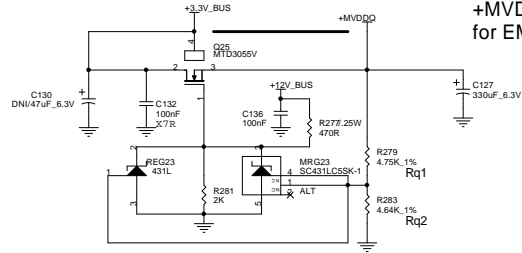
	Rct1	Rct2
1.8V	1K 3240100100 603	422R 3240422000 603
1.9V	1K 3240100100 603	499R 3240499000 603



Regulator for MVDDQ (MEM IO) and VDDR1

Vin = 3.3V AGP
Vout = 2.5V (TSOP)
Iout = 1200mA MAX
Iout = 1000mA Est. MAX

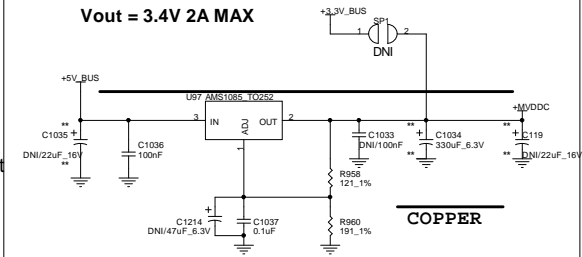
Q25 Pin2/4 should be soldered to board for heat dissipation and a GND fill area.



Placed close to +MVDDQ output for EMI

Regulator for MVDDC

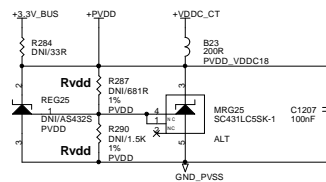
Vin = 5V
Vout = 3.4V 2A MAX



Placed close to +VDDC output for EMI

Regulator for PVDD (Core PLLs) and optional TPVDD (TMDS PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 25mA MAX (PVDD only)
Iout = 30mA MAX (PVDD + TPVDD)



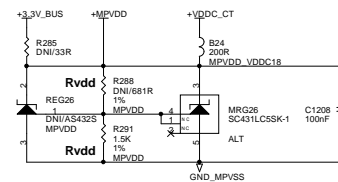
The value of resistor were chosen to reduce failure rate caused by possible defective regulators, i.e., 33R are used instead of 47R or 51R for more start up current. (3.465V - 1.8V) / 33R = 50.5mA

805 package resistor are required for sufficient power rating (0.1W rating). (3.465V - 1.8V) * 50.5mA = 0.085W; therefore, smaller resistor value would require 1206 package

Regulator for MPVDD (Memory PLLs)

Vin = 3.3V AGP
Vout = +1.8V
Iout = 10mA MAX

(Optional)

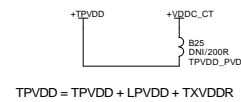


Regulator For TPVDD (TMDS PLLs)

Vin = +3.3V AGP
Vout = 1.8V
Iout = 15mA MAX

TPVDD might not be needed if PVDD can provide stable 1.8V

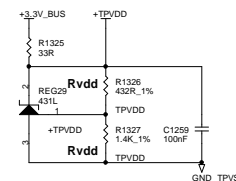
(Optional)



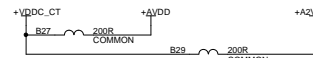
TPVDD = TPVDD + LPVDD + TXVDDR

Regulator for TPVDD (TMDS PLLs)

Vin = 3.3V AGP
Vout = +1.62V
Iout = 10mA MAX
15mA Estimateat MAX



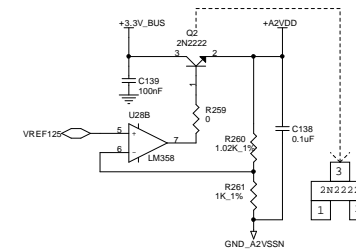
AVDD/A2VDDQ (1st DAC & 2nd DAC Band Gap)



Regulator For A2VDD (2nd DACs)

Vin = +3.3V AGP
Vout = 2.5V
Iout = 150mA MAX

A2VDD might not be needed if VDD can provide stable 2.5V



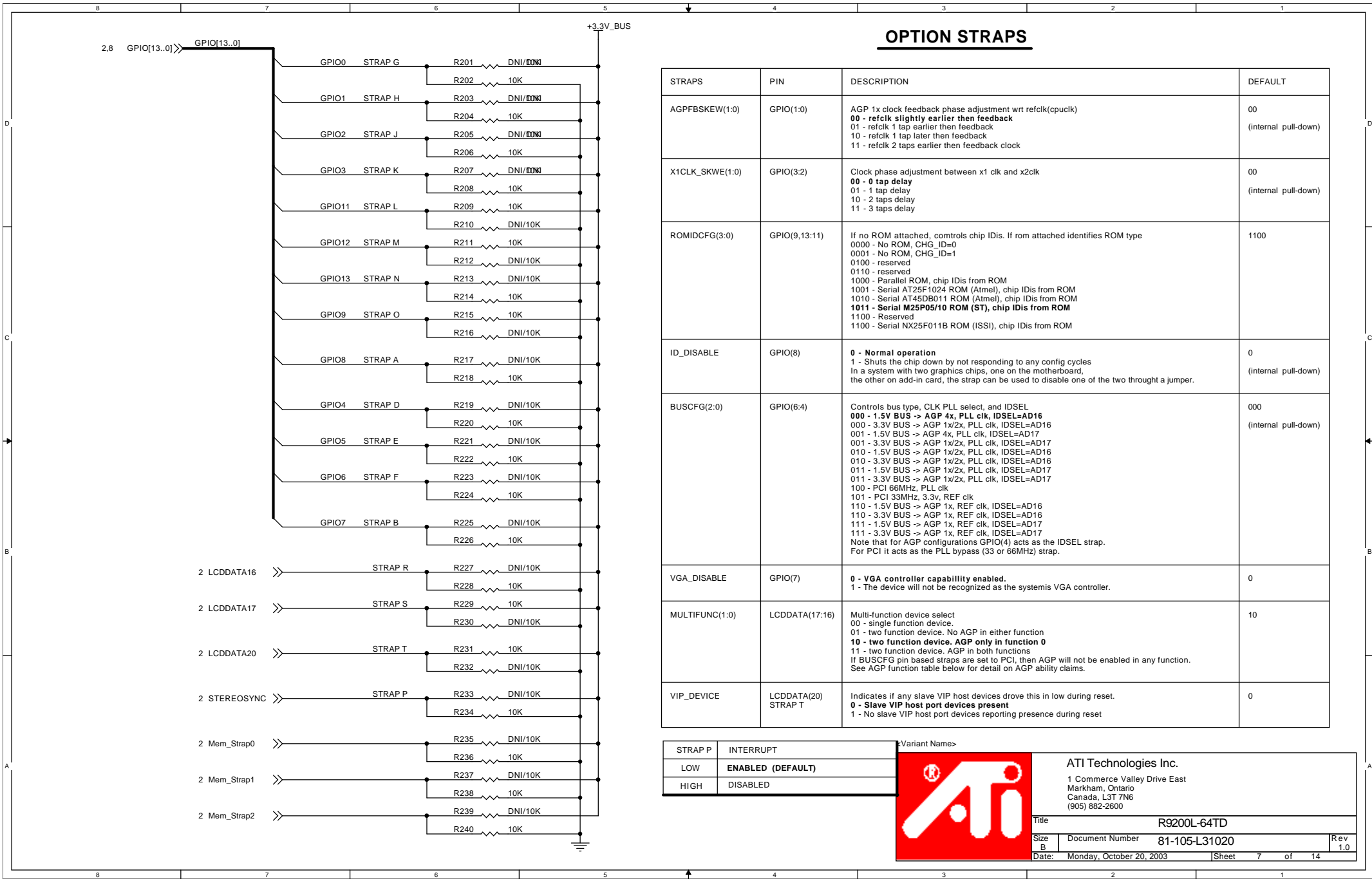
A2VDD and A2VSSN routed with at least 15 mil trace and not longer than 1.5 inch. A2VSSN with signal via to GND at the regulator

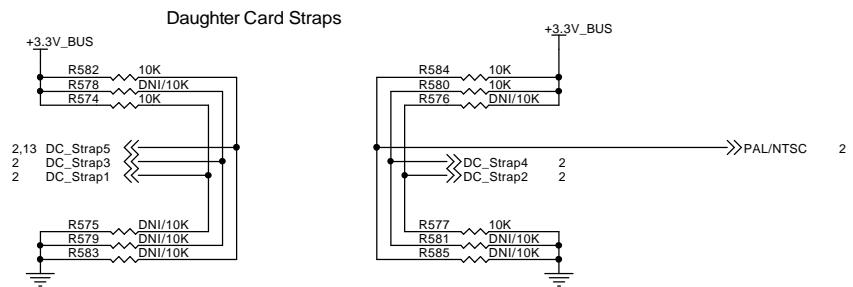
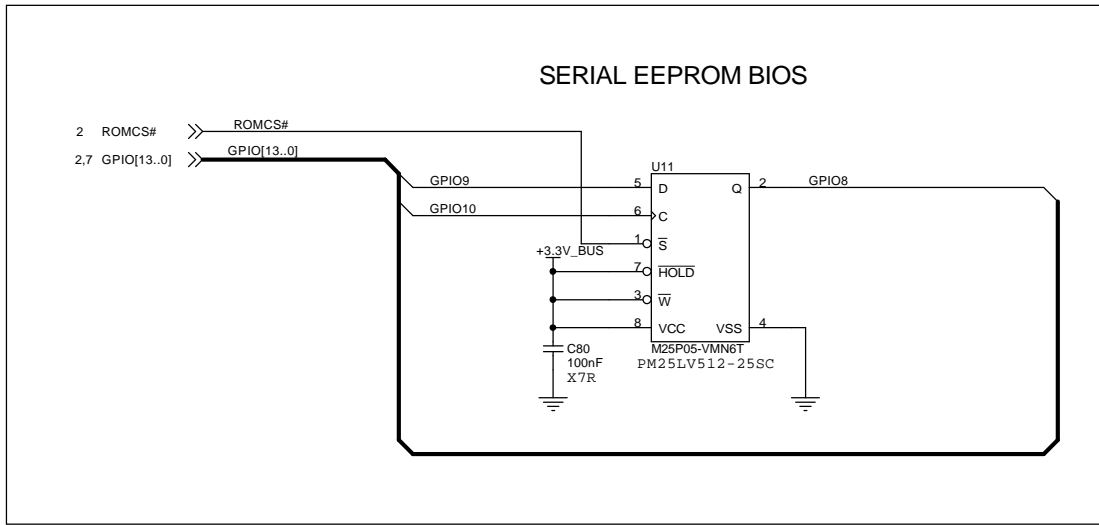
Some Part Ref's updated to 988 brd



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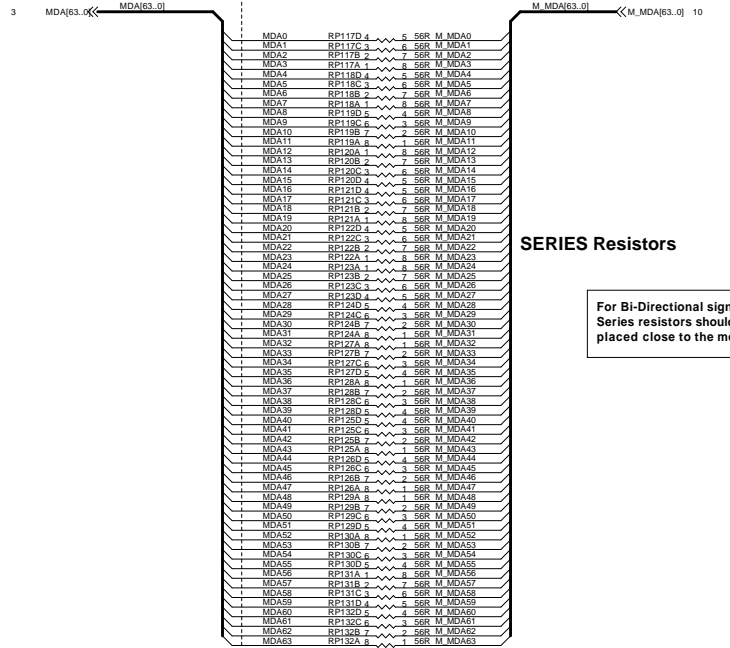
STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMD5 Enabled 0 - Disabled 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled 0 - Disabled 1 - Enabled
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19	DAC2 Configuration DAC2 Off DAC2 On as CRT DAC2 On as TVOUT DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)



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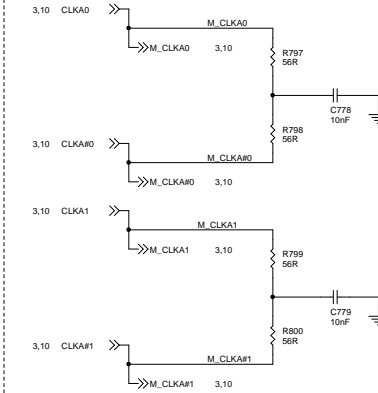
TERMINATION FOR MEMORY CHANNEL A



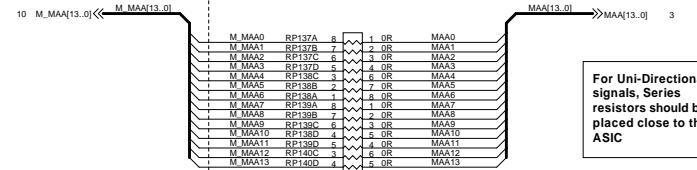
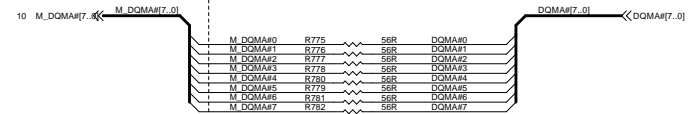
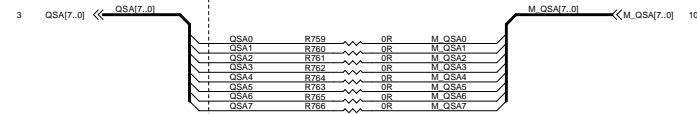
CLOCK terminations

Change from 1:1 spacing to at least a
2.5:1 spacing between the pair

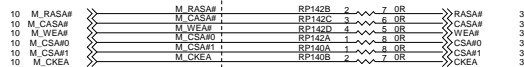
These resistors and caps must be placed to minimize any stubs. These
must also be placed after the memory



Proper Termination of QSA?



For Uni-Directional
signals, Series
resistors should be
placed close to the
ASIC



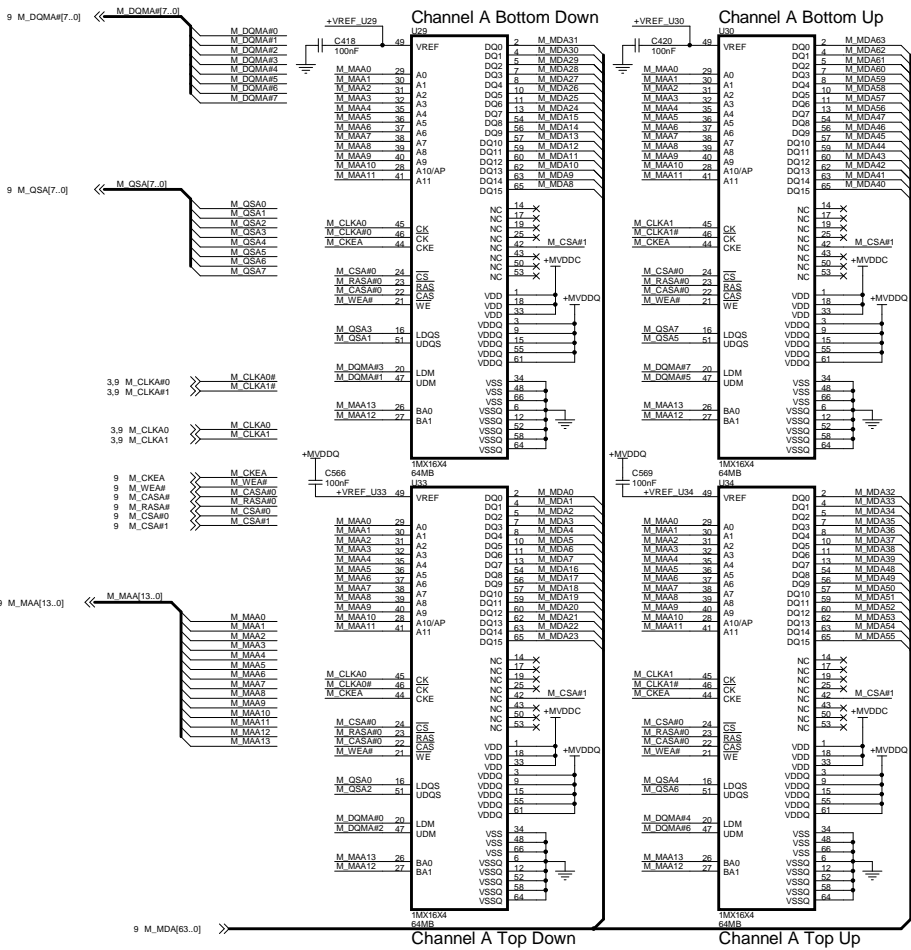
<Variant Name>



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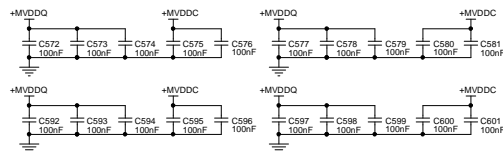
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DDR SDRAM 64Mbit 1Mx16x4

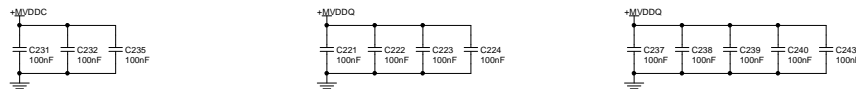


Put 1 1uF cap per power pin of memory



2 capacitors SHOULD BE PLACED CLOSE TO THE REFERENCE LAYER CHANGE OF CLOCKS FOR EMI REDUCE.

Place as many as possible.



DATA GROUP SHOULD BE ASSIGNED TO EACH DQS AND DQM ACCORDINGLY AND THIS MAPPING IS JUST FOR PLACEMENT AND ROUTING REASONS

All +VDD, MEM, IO and +VDD decoupling caps should be equally distributed per memory chip. As close to the pin as possible.

<Variant Names>

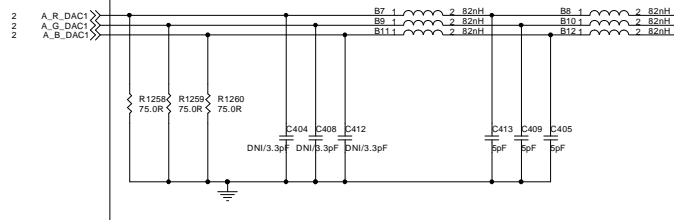


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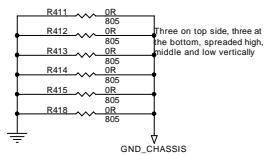
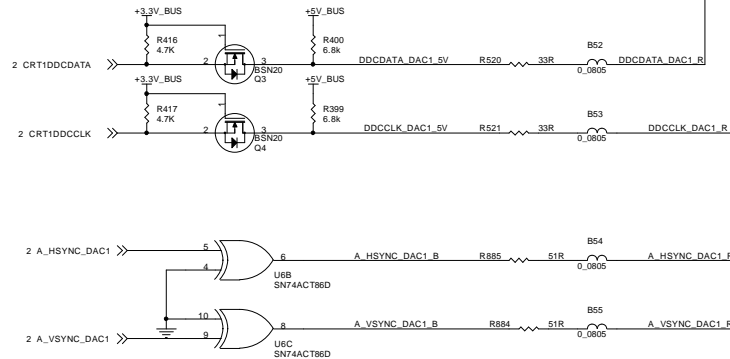
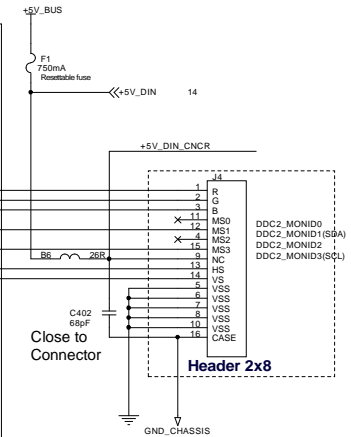
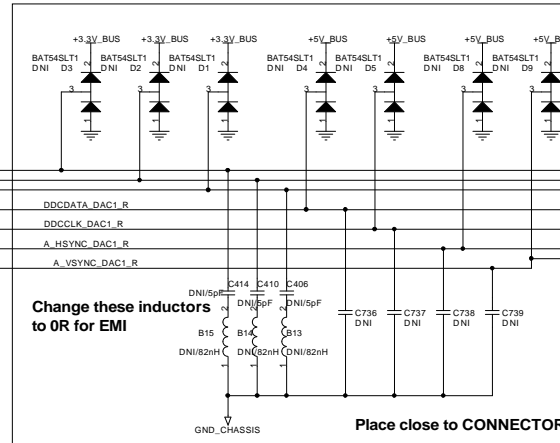
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PRIMARY CRT

Place close to ASIC



OPTIONAL ESD/HOTPLUG PROTECTION DIODES



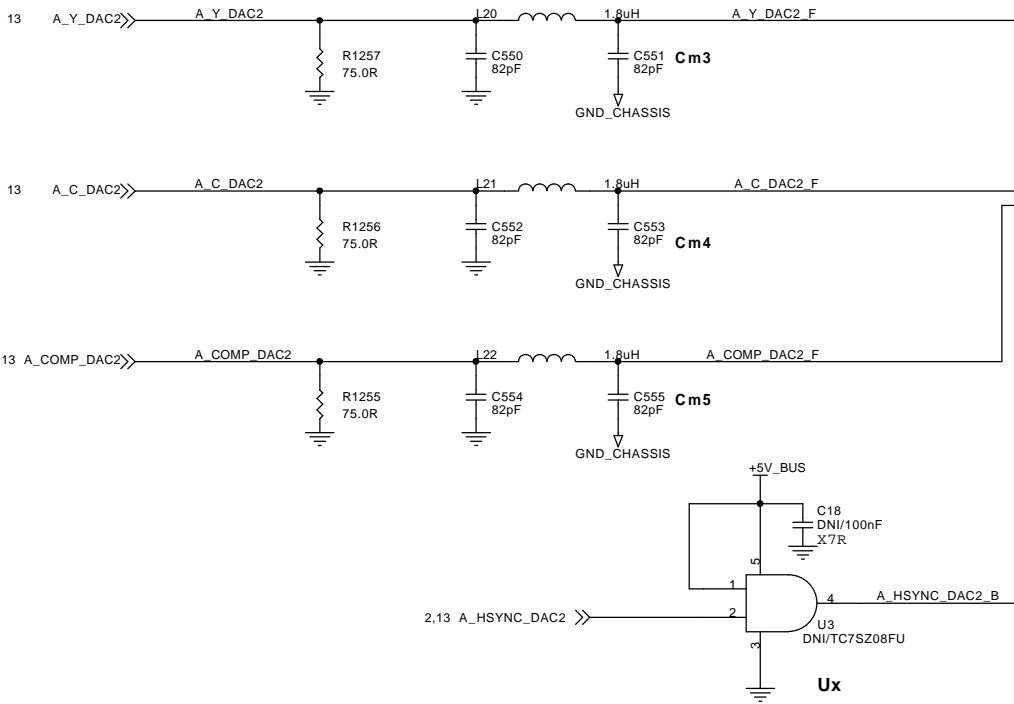
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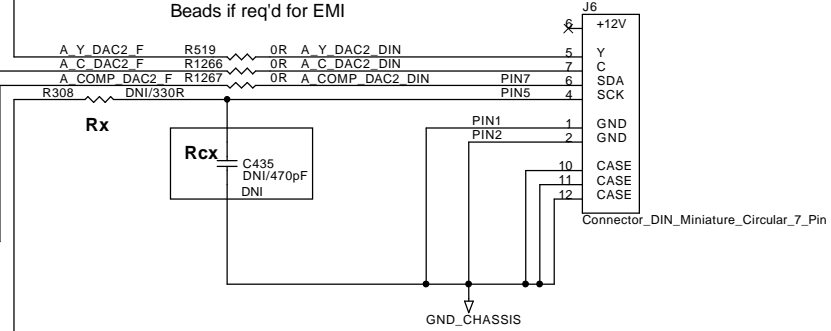
Place Resistors close to ASIC.



Add alternate part for 7 pin Svideo
6071001500

Place near connector
0R leaves footprint for Ferrite
Beads if req'd for EMI

TV Out (SVHS)



HSync to Connector	Rx = 330R, Rcx = 470pF, Ux INSTALL
HSync NOT Connected	Rx = DNI, Rcx = 0R, Ux = DNI

<Variant Name>

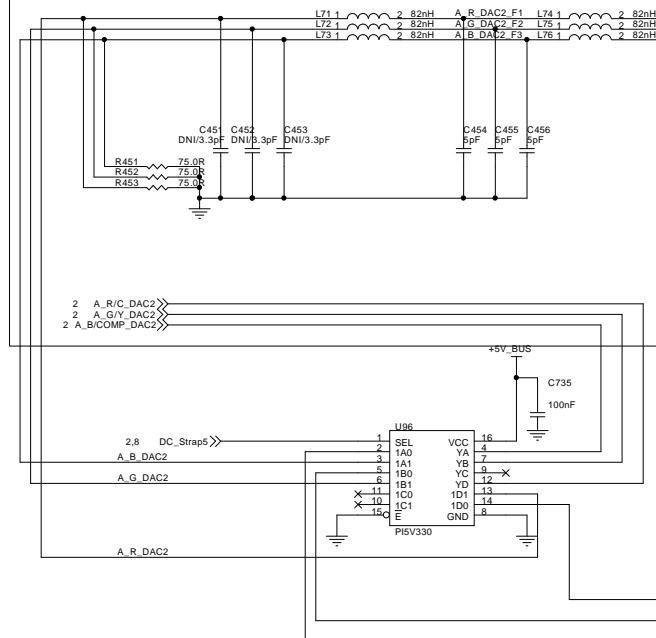


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SECONDARY CRT

Place close to connector DVI1

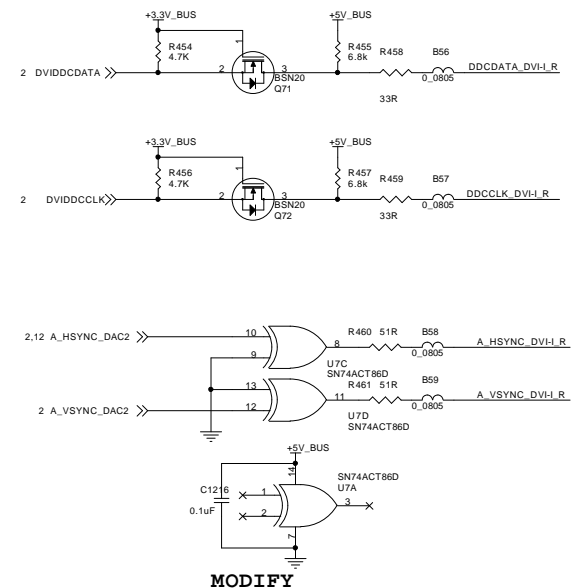


TO J6

A_C_DAC2 << A_C_DAC2 12
A_Y_DAC2 << A_Y_DAC2 12
A_COMP_DAC2 << A_COMP_DAC2 12

A_R_DVI-I 14
A_G_DVI-I 14
A_B_DVI-I 14
DDCDATA_DVI-I_R 14
DDCCLK_DVI-I_R 14
A_HSYNC_DVI-I_R 14
A_VSYNC_DVI-I_R 14

To DVI1



MODIFY

<Variant Name>



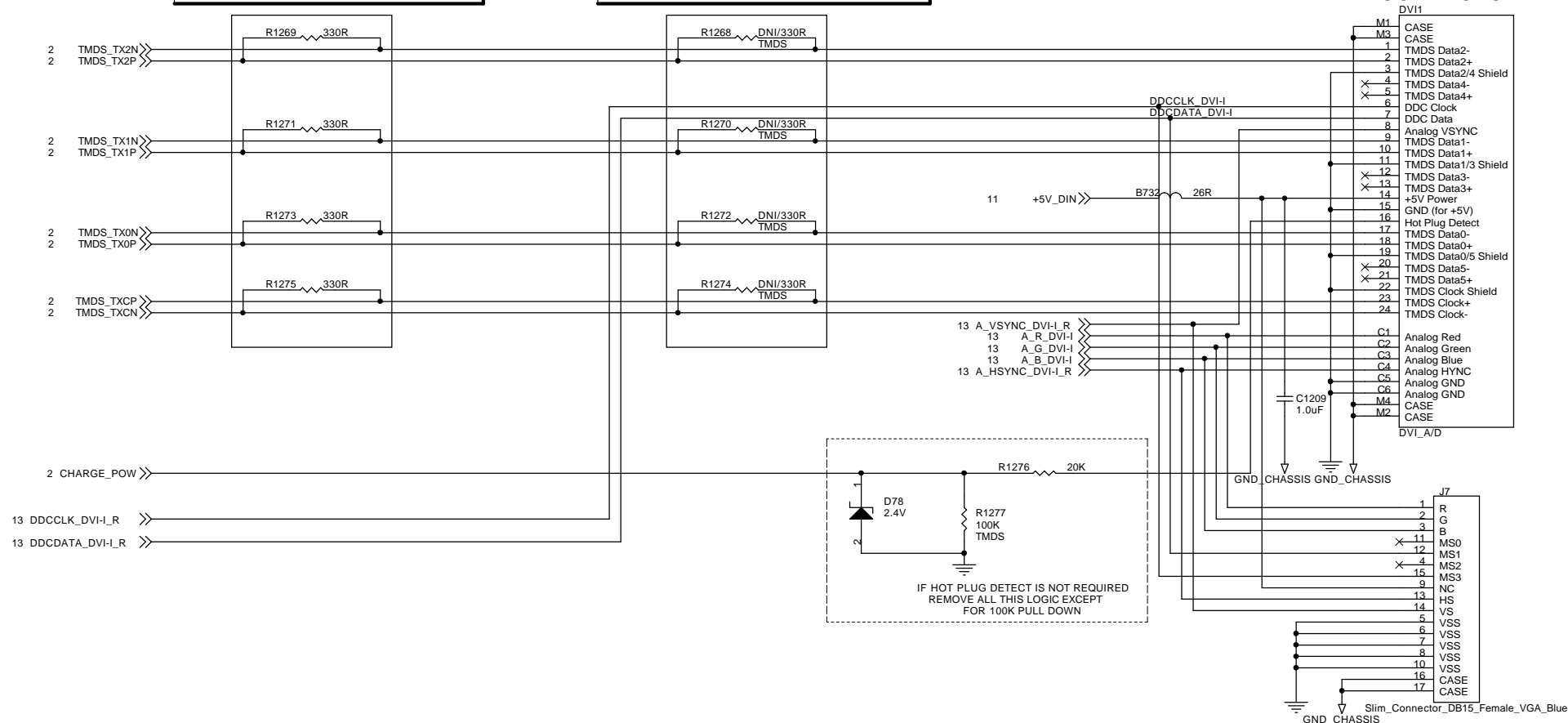
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INSTALL TERMINATION RESISTORS CLOSE TO ASIC

INSTALL TERMINATION RESISTORS CLOSE TO CONNECTOR

PRIMARY DVI-I CONNECTOR



<Variant Name>



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