

REFERENCE DESIGN

THESE SCHEMATICS ARE SUBJECT TO MODIFICATION AND DESIGN IMPROVEMENTS. PLEASE CONTACT ATI FIELD APPLICATION ENGINEERING BEFORE USING THE INFORMATION CONTAINED HEREIN.

RESTRICTION NOTICE

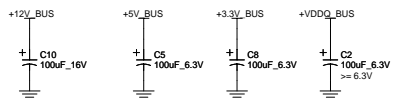
THESE SCHEMATICS CONTAIN INFORMATION WHICH IS PROPRIETARY TO AND IS THE PROPERTY OF ATI, AND MAY NOT BE USED, REPRODUCED OR DISCLOSED IN ANY MANNER WITHOUT EXPRESSED WRITTEN PERMISSION FROM ATI.



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO		
Size	Document Number	81-105-L50XXX	Rev
Date	Wednesday, May 12, 2004	Sheet	1 of 15

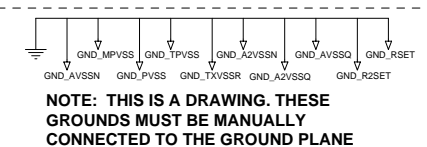
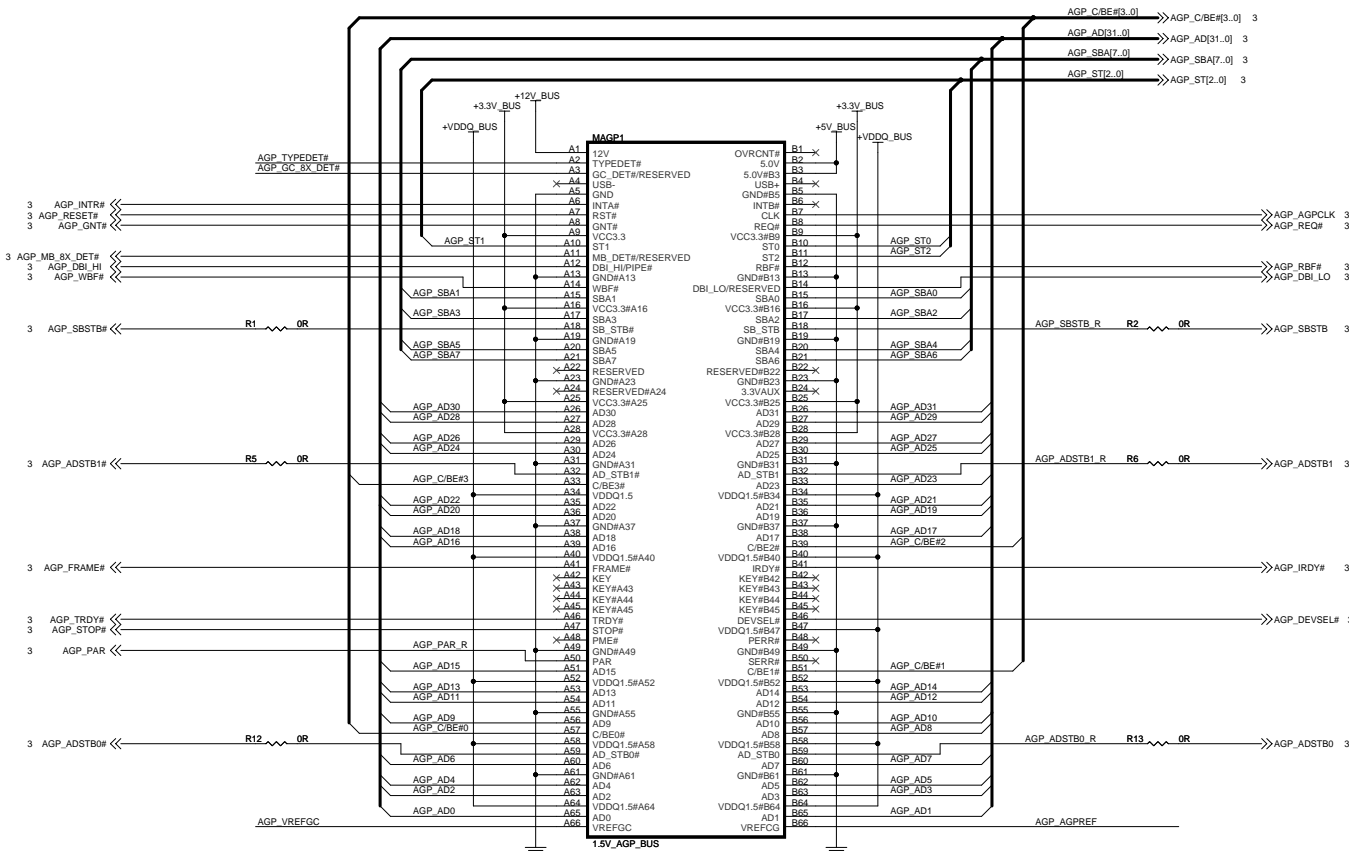
LAYOUT NOTE: SOME OF THE CAPS BELOW MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING



Use 47µF Tant. 16V 20% D size (P/N 4230047600), 800mS Max. ESR and Max. ripple 430mA @ 100kHz or 100µF, Alum. 6.3V 20% 6.3mm dia (P/N 4261010700), 440mS Max. ESR and Max. ripple 230mA @ 100kHz or 47µF, Alum. 6.3V 20% 5mm dia (P/N 4262047600), 760mS Max. ESR and Max. ripple 150mA @ 100kHz

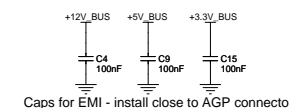
Place C2 on left side of AGP connector

4X/8X AGP BUS

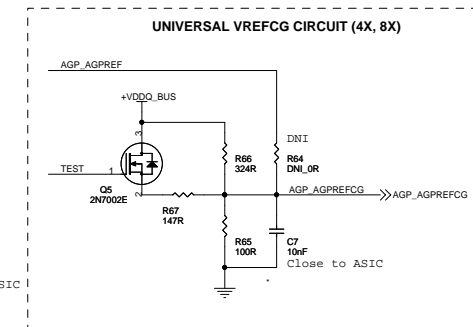
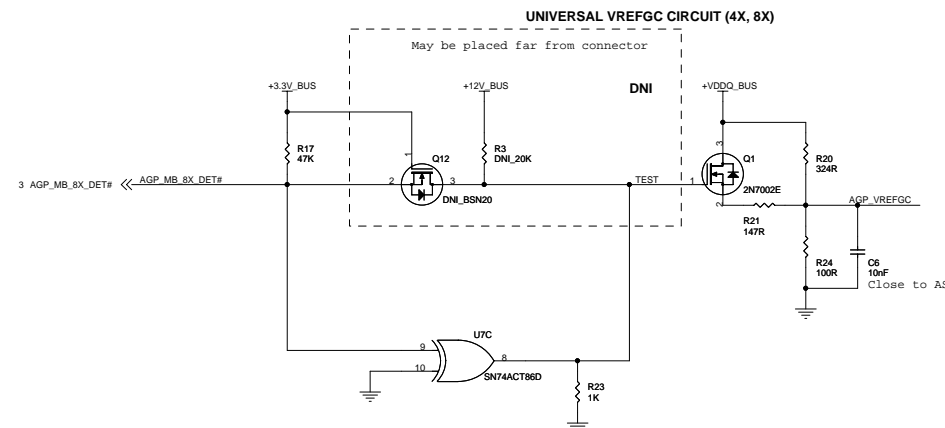
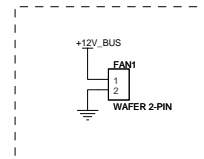
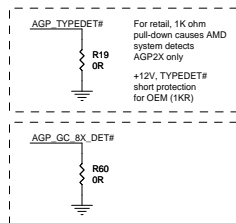


NOTE: THIS IS A DRAWING. THESE GROUNDS MUST BE MANUALLY CONNECTED TO THE GROUND PLANE

SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND

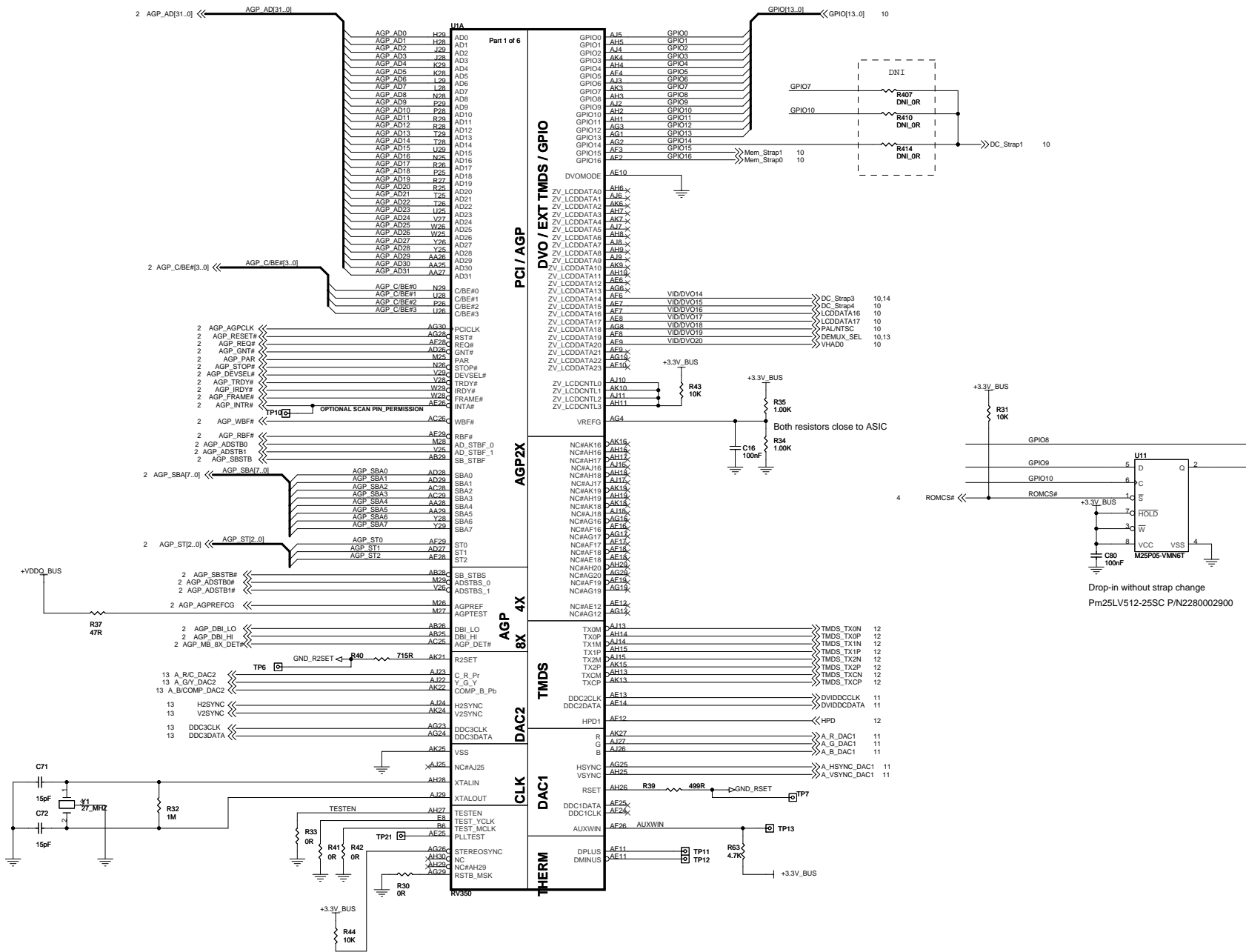


Caps for EMI - install close to AGP connector



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title			
AGPBX RV350 64/128M TSOP DVI-Sim_VGA VO			
Size	Document Number	Rev	
C	81-105-L50XXX	1.0	
Date:	Wednesday, May 12, 2004	Sheet	2 of 15

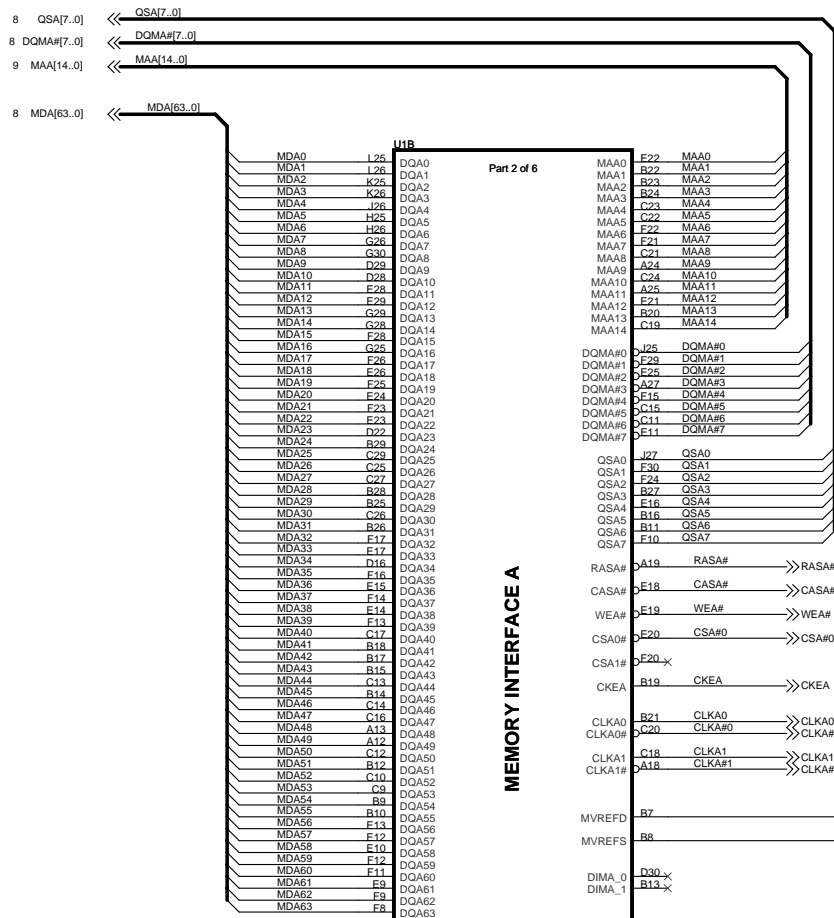


IT IS RECOMMENDED TO ALLOW SERIES RESISTOR
FOOT PRINTS ON THE INDICATED AGP CONTROL SIGNALS
TO ADDRESS ANY LAYOUT NOISE RELATED
SIGNAL DAMPING REQUIREMENTS

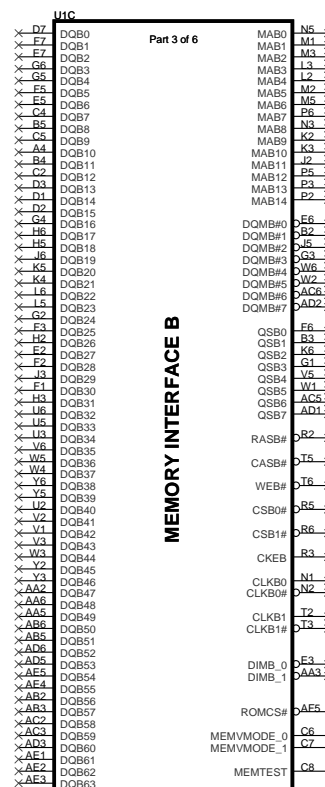


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: **AGP8X RV350 64/128M TSOP DVI-I/Sim_VGA V0**
Size: **Document Number** 81-105-L50XXX
Date: **Wednesday, May 12, 2004** Sheet **3** of **15**



PLACE C351/152 VERY CLOSE TO ASIC
R56/57/58/59 CLOSE TO ASIC AS WELL



LAYOUT NOTE: SOME OF THE RESISTORS R51-54 MAY BE REMOVED IF SPACE IS AN ISSUE, ASK BEFORE REMOVING

FOR 2.5V VDDR1
MEMVMODE_0 = VDDC
MEMVMODE_1 = GND
FOR 1.8V VDDR1
MEMVMODE_0 = GND
MEMVMODE_1 = VDDC
(SEE DESIGN GUIDE)



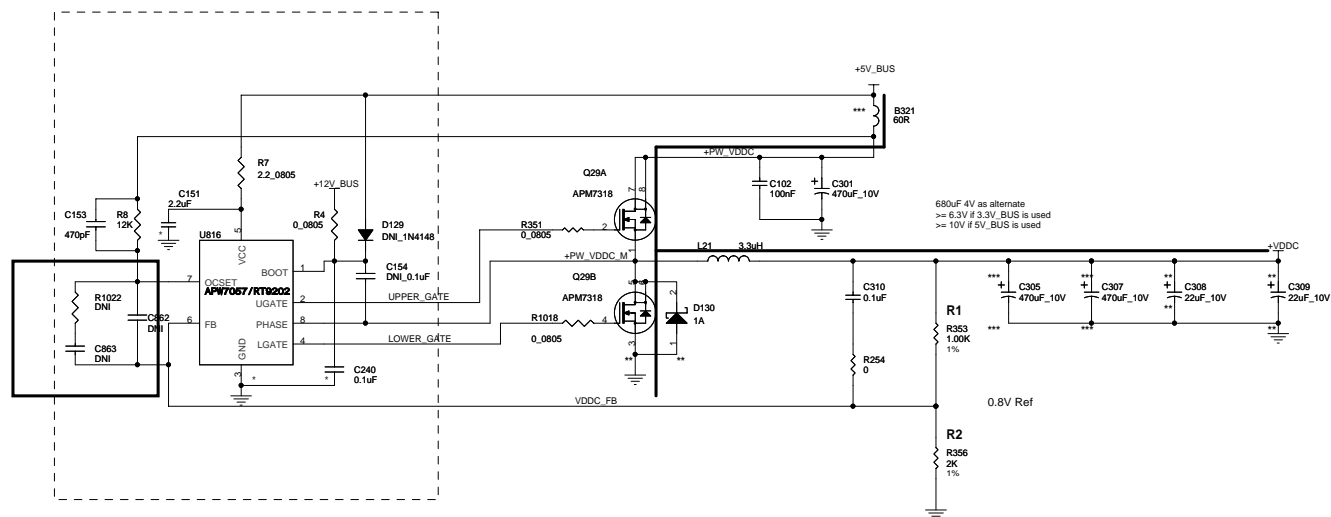
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO
Size: Custom
Document Number: 81-105-L50XXX
Date: Wednesday, May 12, 2004
Sheet: 4 of 15
Rev: 1.0

Vin = 5.0V AGP
Vout = 1.2V
Iout = Unknown (7A MAX at 350MHz) (load consumption)
Iout = 3A MAX (Power rail consumption)

Vin = 5.0V AGP
Vout = 1.2V
Iout = Unknown (7A MAX at 350MHz) (load consumption)
Iout = 3A MAX (Power rail consumption)

Part	Vout	R1	R2
APW7057 RT9202 0.8V Ref	1.2V	1.00K 1% ATI P/N 3240100100	2.00K 1% ATI P/N 3240110100
	1.3V	1.00K 1% ATI P/N 3240100100	1.6K 1% ATI P/N
	1.62V	1.00K 1% ATI P/N 3240100100	976R 1% ATI P/N 3240976000
	2.5V	1.00K 1% ATI P/N 3240100100	475R 1% ATI P/N 3240475300
	3.3V TSOP Memory	1.00K 1% ATI P/N 3240100100	324R 1% ATI P/N 3240332000
	3.45V TSOP Memory	1.00K 1% ATI P/N 3240100100	301 1% ATI P/N 3240301000



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title				AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO			
Size		Document Number					Rev
C		81-105-L50XXX					1.0
Date:			Wednesday, May 12, 2004		Sheet		6 of 15

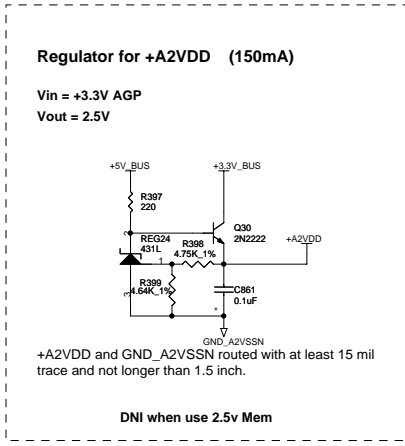
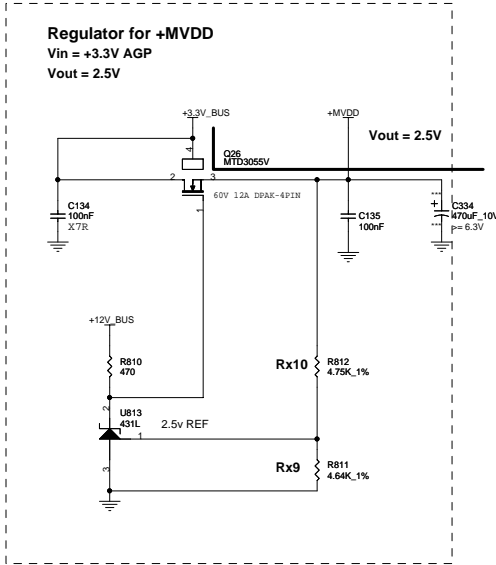
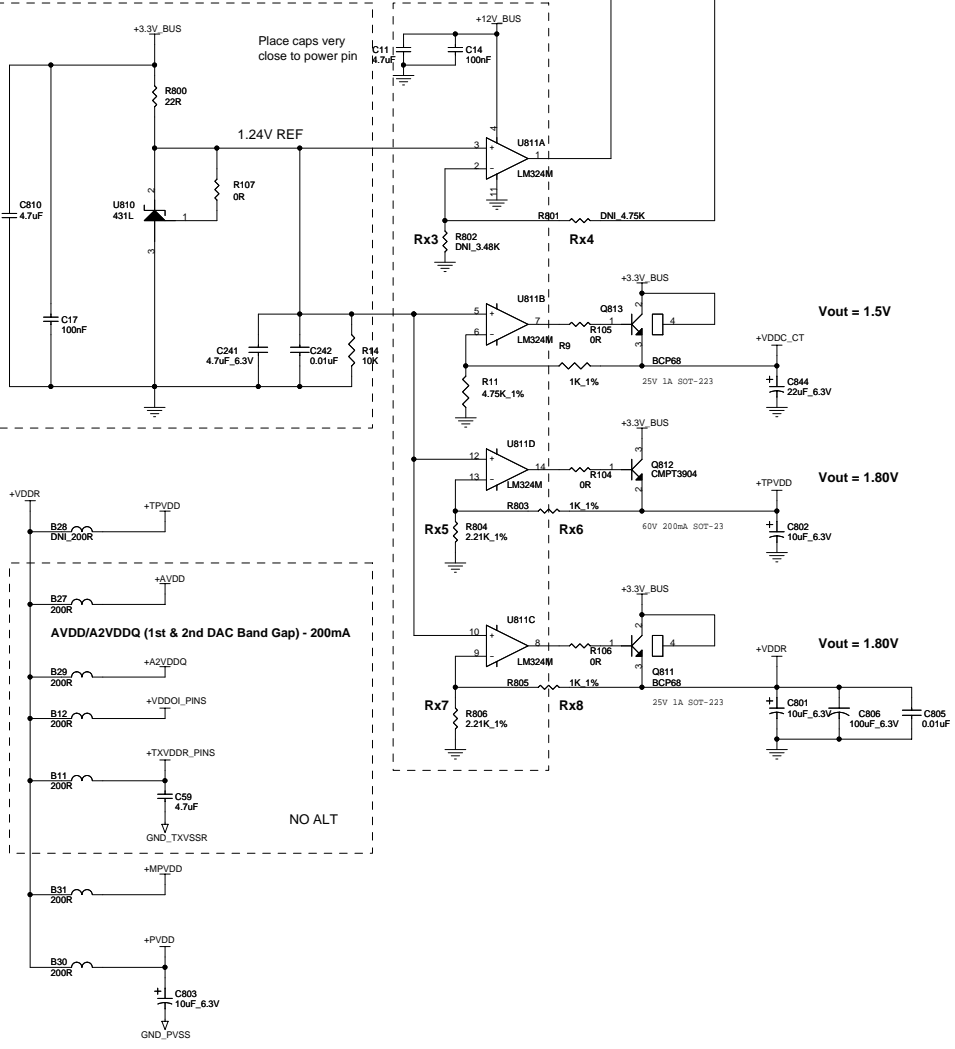
+MVDD	Rx3 / Rx9	Rx4 / Rx10	Memory
2.5V			Infineon, 16Mx16, 200MHZ, Samsung, 8Mx16, 250MHZ,
2.6V			Samsung, 16Mx16, 200MHZ

REF2	Rx1	Rx2
1.5V [-0.02V/+0.02V]		
+TPVDD / +VDDR		
1.800V		
1.847V		
1.855V		

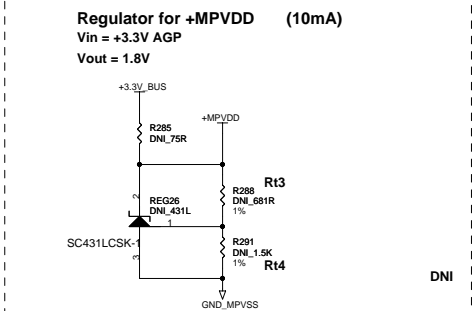
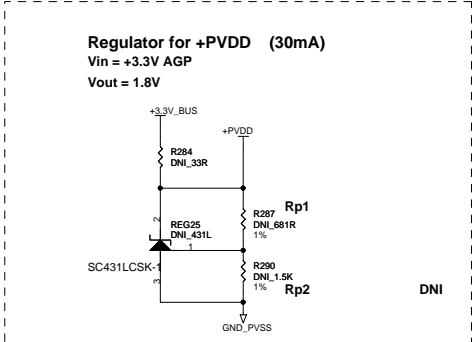
Regulator for :

- +MVDD/+A2VDD
- +VDDC_CT
- +PVDD/+MPVDD
- +VDDR4

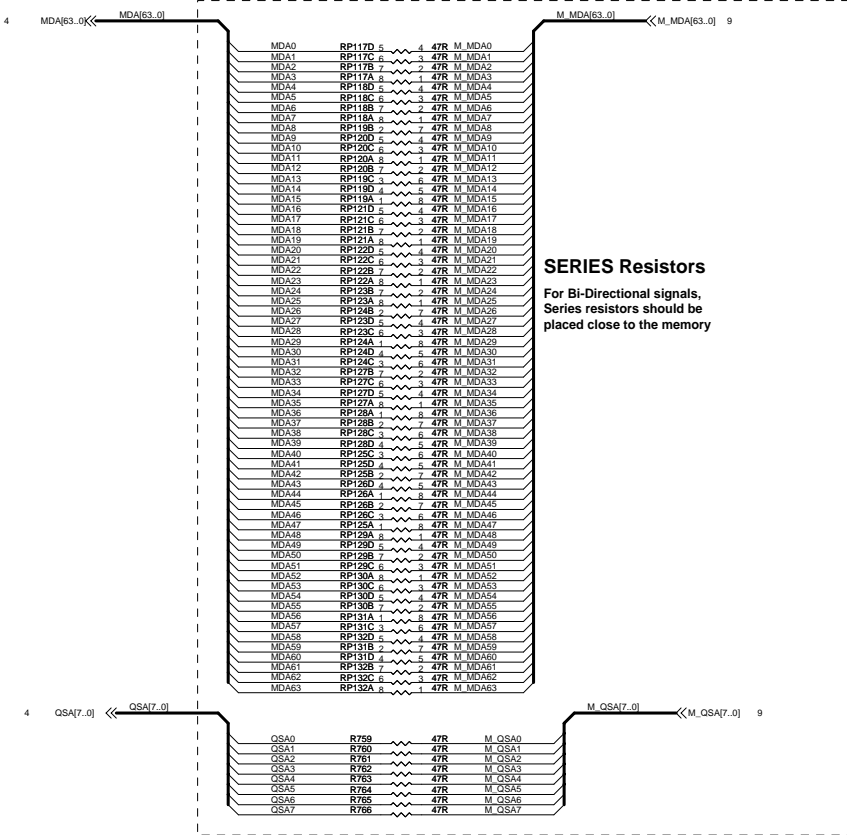
Vout = 3.3V



	Rp1 / Rt1/Rt3	Rp2 / Rt2/Rt4
1.61V +0.01V/-0.01V	432R 3240432000	1.5K 3230015200
1.69V +0.01V/-0.01V	432R 3240432000	1.21K 3240121100
1.718V +0.01V/-0.01V	562R 3240562000	1.5K 3230015200
1.8175V +0.01V/-0.01V	681R 3240681000	1.5K 3230015200



TERMINATION FOR
MEMORY
CHANNEL A

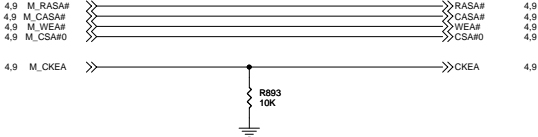
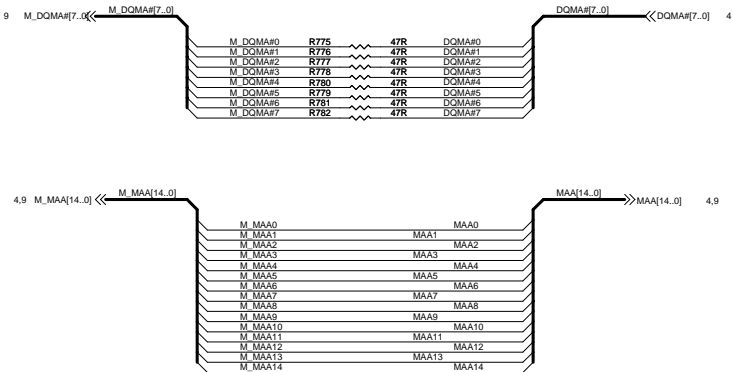
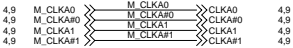
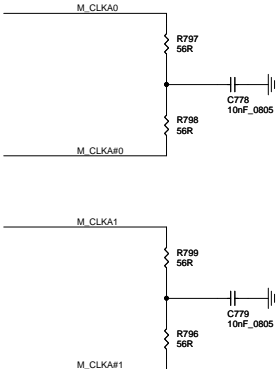


SERIES Resistors
For Bi-Directional signals,
Series resistors should be
placed close to the memory

CLOCK
terminations

Change from 1:1 spacing to at least a
2.5:1 spacing between the pair

These resistors and caps must be placed to minimize any stubs. These
must also be placed after the memory



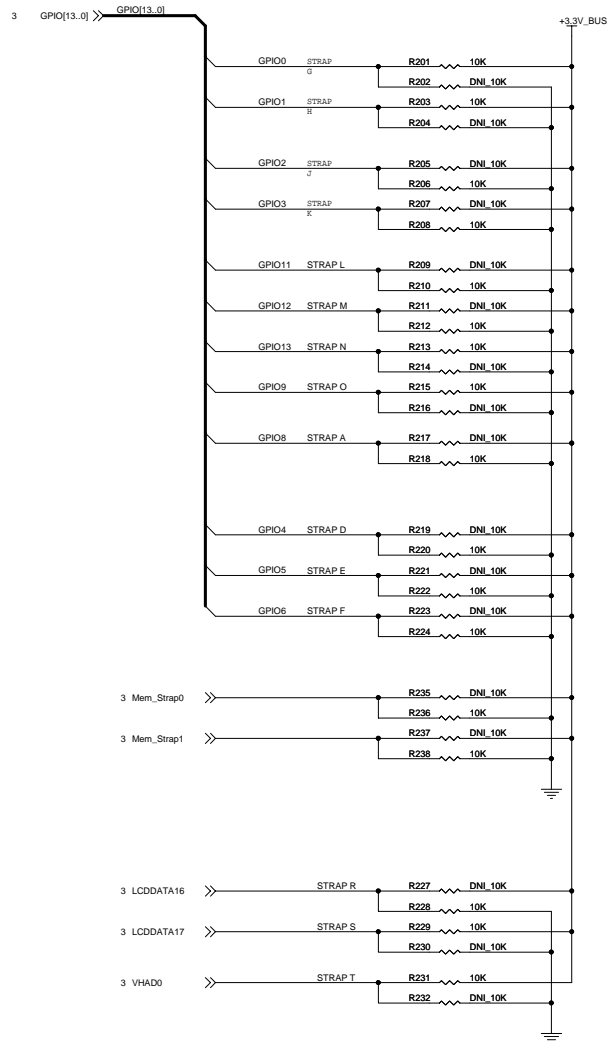
ATI Technologies Inc.

1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2800

Title	AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO		
Size	Document Number	81-105-L50XXX	Rev 1.0
Date	Wednesday, May 12, 2004	Sheet 8 of 15	

Title				AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO			
Size		Document Number				Rev	
Custom		81-105-L50XXX				1.0	
Date: Wednesday, May 12, 2004				Sheet 9 of 15			

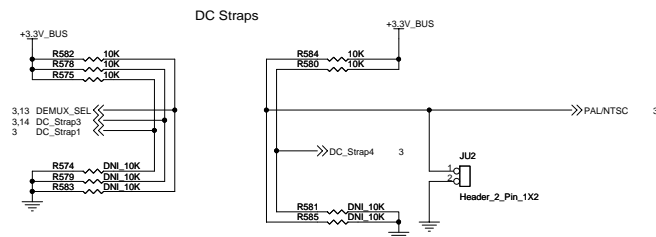
OPTION STRAPS



STRAPS	PIN	DESCRIPTION	DEFAULT
AGPFSKEW(1:0)	GPIO(1:0)	AGP 1x clock feedback phase adjustment wrt refclk(spuck) 00 - refclk slightly earlier then feedback 01 - refclk 1 tap earlier then feedback 10 - refclk 1 tap later then feedback 11 - refclk 2 taps earlier then feedback clock	00 (internal pull-down)
X1CLK_SKWE(1:0)	GPIO(3:2)	Clock phase adjustment between x1 clk and x2clk 00 - 0 tap delay 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (internal pull-down)
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 0000 - No ROM, CHG_ID=0 0001 - No ROM, CHG_ID=1 0100 - reserved 0110 - reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	1001
ID_DISABLE	GPIO(8)	0 - Normal operation 1 - Shuts the chip down by not responding to any config cycles In a system with two graphics chips, one on the motherboard, the other on add-in card, the strap can be used to disable one of the two through a jumper.	0 (internal pull-down)
BUSCFG(2:0)	GPIO(6:4)	Controls bus type, CLK PLL select, and IDSEL 000 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD16 000 - 3.3V BUS -> AGP 1x2x, PLL clk, IDSEL=AD16 001 - 1.5V BUS -> AGP 4x, PLL clk, IDSEL=AD17 001 - 3.3V BUS -> AGP 1x2x, PLL clk, IDSEL=AD17 010 - 1.5V BUS -> AGP 1x2x, PLL clk, IDSEL=AD16 010 - 3.3V BUS -> AGP 1x2x, PLL clk, IDSEL=AD16 011 - 1.5V BUS -> AGP 1x2x, PLL clk, IDSEL=AD17 011 - 3.3V BUS -> AGP 1x2x, PLL clk, IDSEL=AD17 100 - PCI 66MHz, PLL clk 101 - PCI 33MHz, 3.3v, REF clk 110 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD16 110 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD16 111 - 1.5V BUS -> AGP 1x, REF clk, IDSEL=AD17 111 - 3.3V BUS -> AGP 1x, REF clk, IDSEL=AD17 Note that for AGP configurations GPIO(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66MHz) strap.	000 (internal pull-down)
MULTIFUNC(1:0)	LCDDATA(17:16)	Multi-function device select 00 - single function device. 01 - two function device. No AGP in either function 10 - two function device. AGP only in function 0 11 - two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims.	00
VIP_DEVICE	LCDDATA(20) STRAP T	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	0

STRAP P	INTERRUPT
LOW	ENABLED (DEFAULT)
HIGH	DISABLED

STRAPS	PIN	DESCRIPTION
DC_STRAP1	LCDDATA12	Internal TMDs Enabled 0 - Disabled 1 - Enabled
DC_STRAP2	LCDDATA13	Video Capture Enabled 0 - Disabled 1 - Enabled THIS STRAP IS NOT PRESENT ON THIS CARD!
DC_STRAP4 DC_STRAP5	LCDDATA15 LCDDATA19	DAC2 Configuration 0 0 0 1 1 0 1 1 DAC2 Off DAC2 On as CRT DAC2 On as TVOUT DAC2 On as TVOUT and CRT
DC_STRAP6	LCDDATA18	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)
DC_STRAP3	LCDDATA14	Connected to Component TV-Out Detect pin Normally high, pulled low by Component TVO dongle

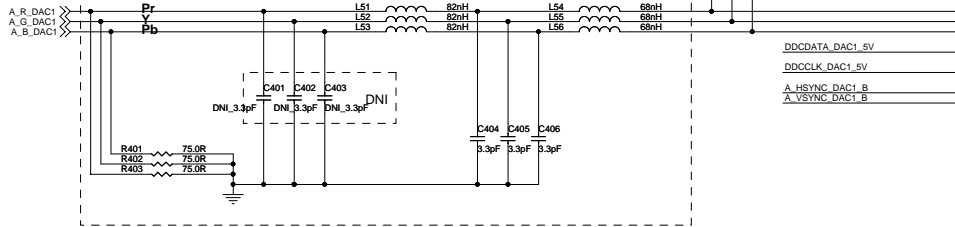


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title: AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO
Size: Document Number 81-105-L50XXX Rev 1.0
Customer: Date: Wednesday, May 12, 2004 Sheet 10 of 15

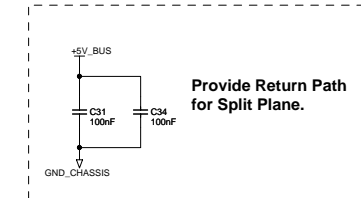
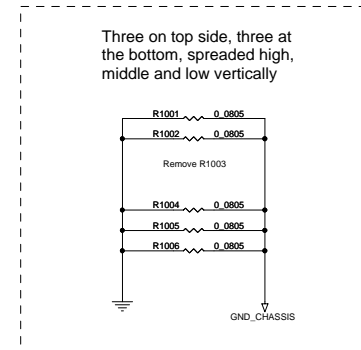
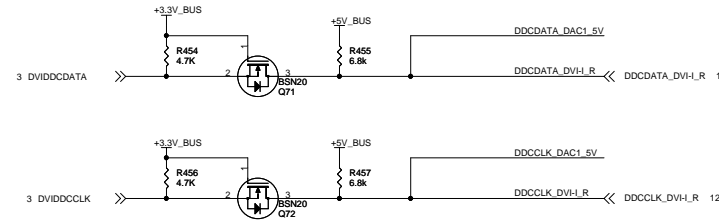
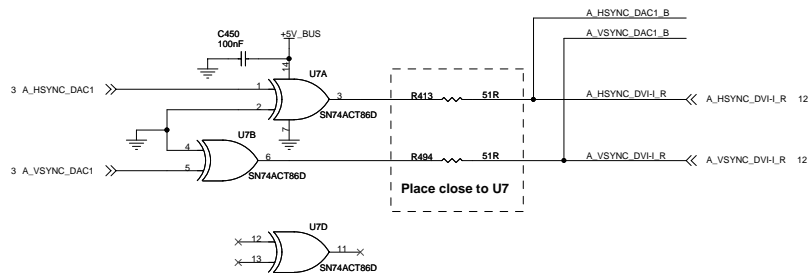
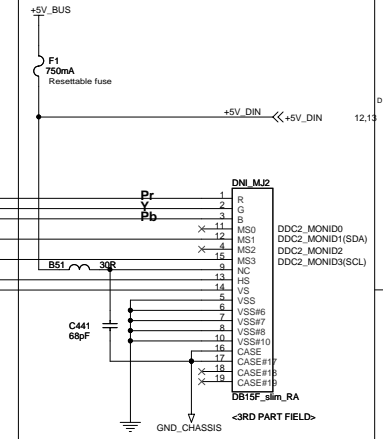
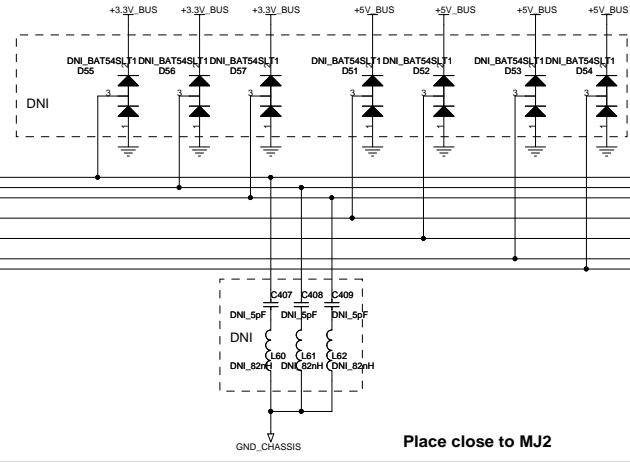
PRIMARY CRT

Place close to MJ2

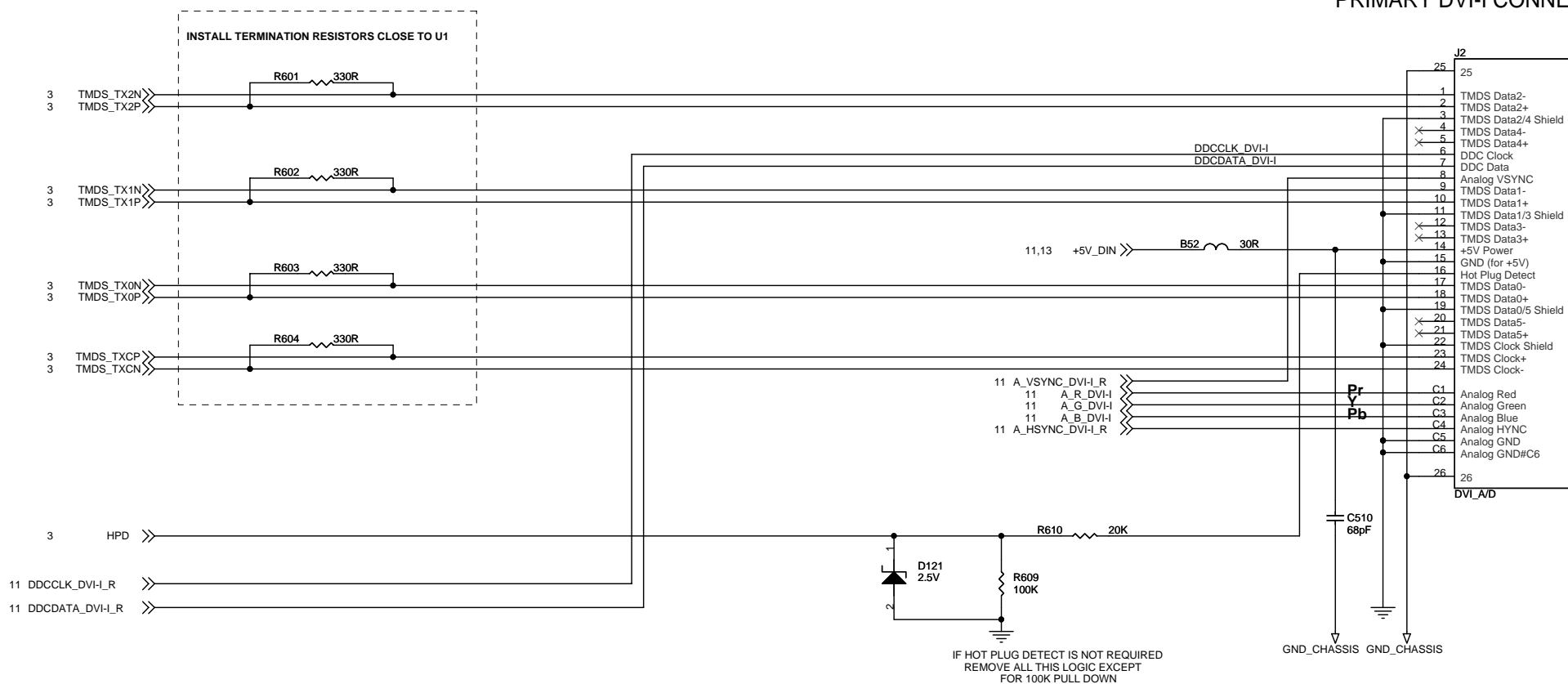


OPTIONAL ESD/HOTPLUG PROTECTION DIODES

LAYOUT NOTE: MAY BE POSSIBLE TO REMOVE ALL DIODES ABOVE IF THERE'S NO SPACE, ASK BEFORE REMOVING.

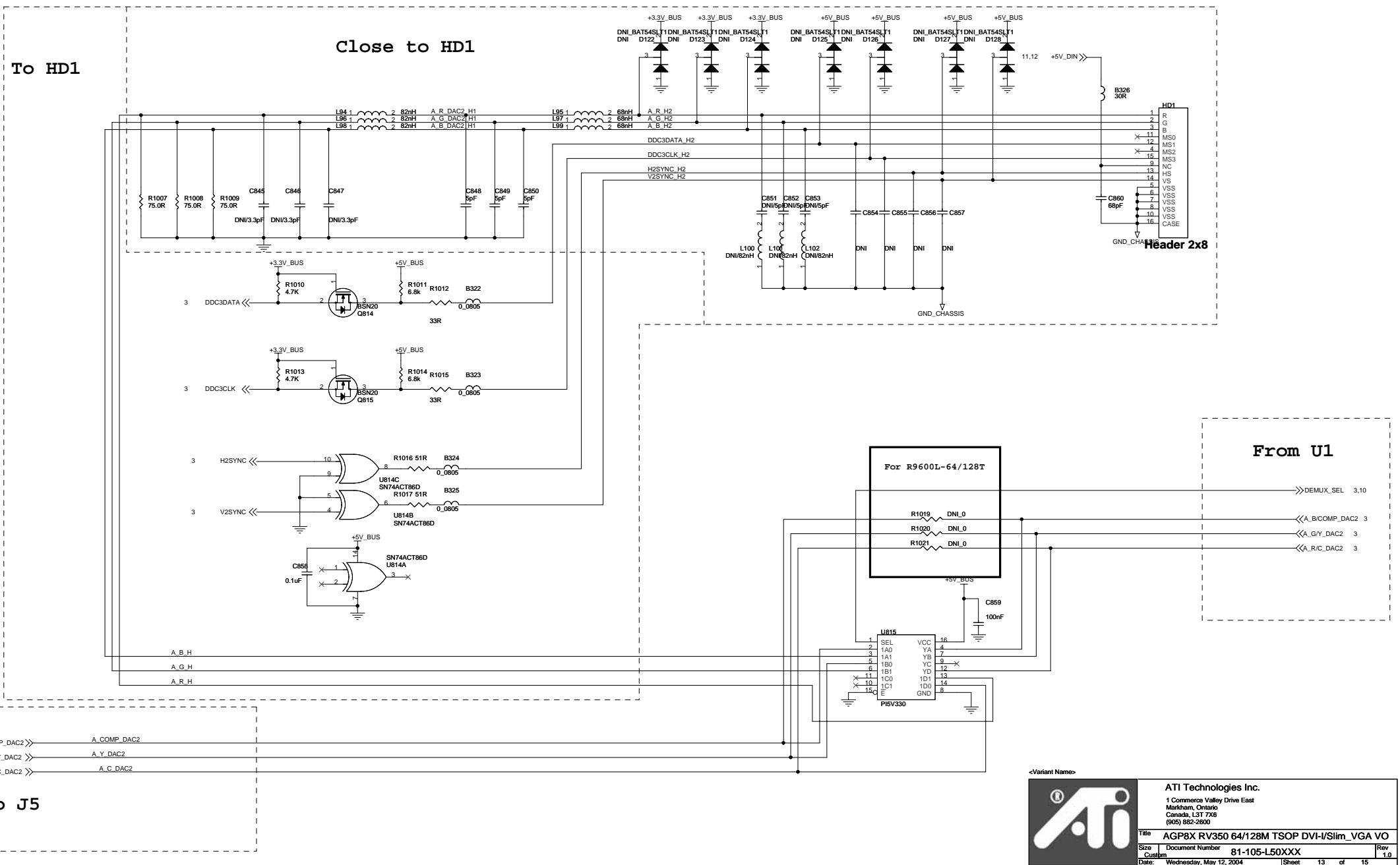


PRIMARY DVI-I CONNECTOR



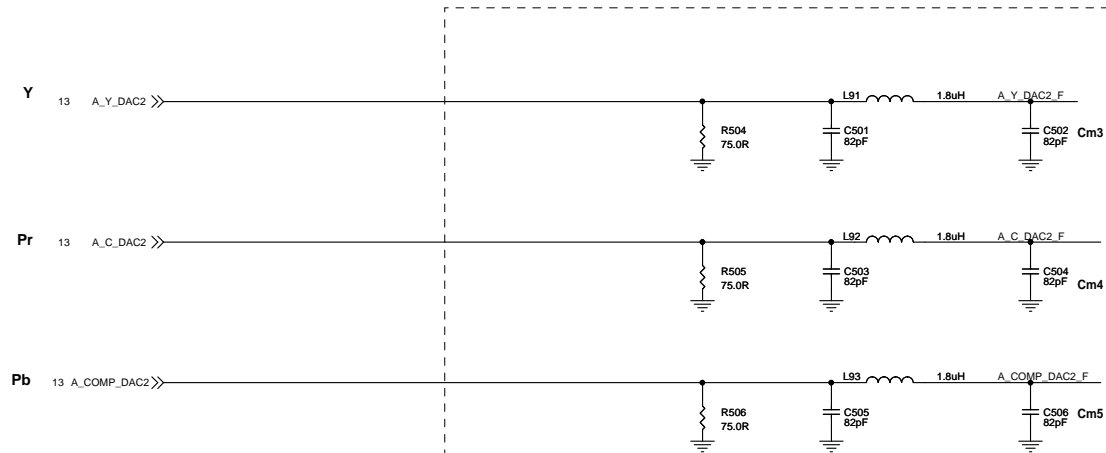
ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title		AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO	
Size	Document Number	81-105-L50XXX	
B			Rev 1.0
Date:	Wednesday, May 12, 2004	Sheet 12	of 15

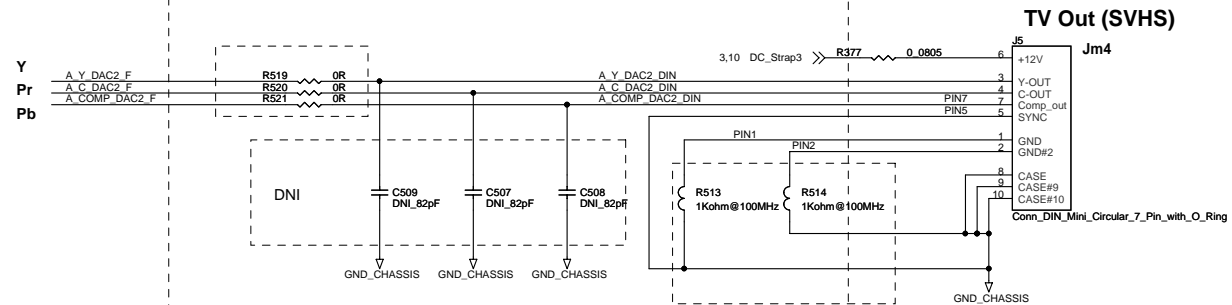


ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title				AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO			
Size		Document Number				Rev	
Custom		81-105-L50XXX				1.0	
Date: Wednesday, May 12, 2004				Sheet 13 of 15			

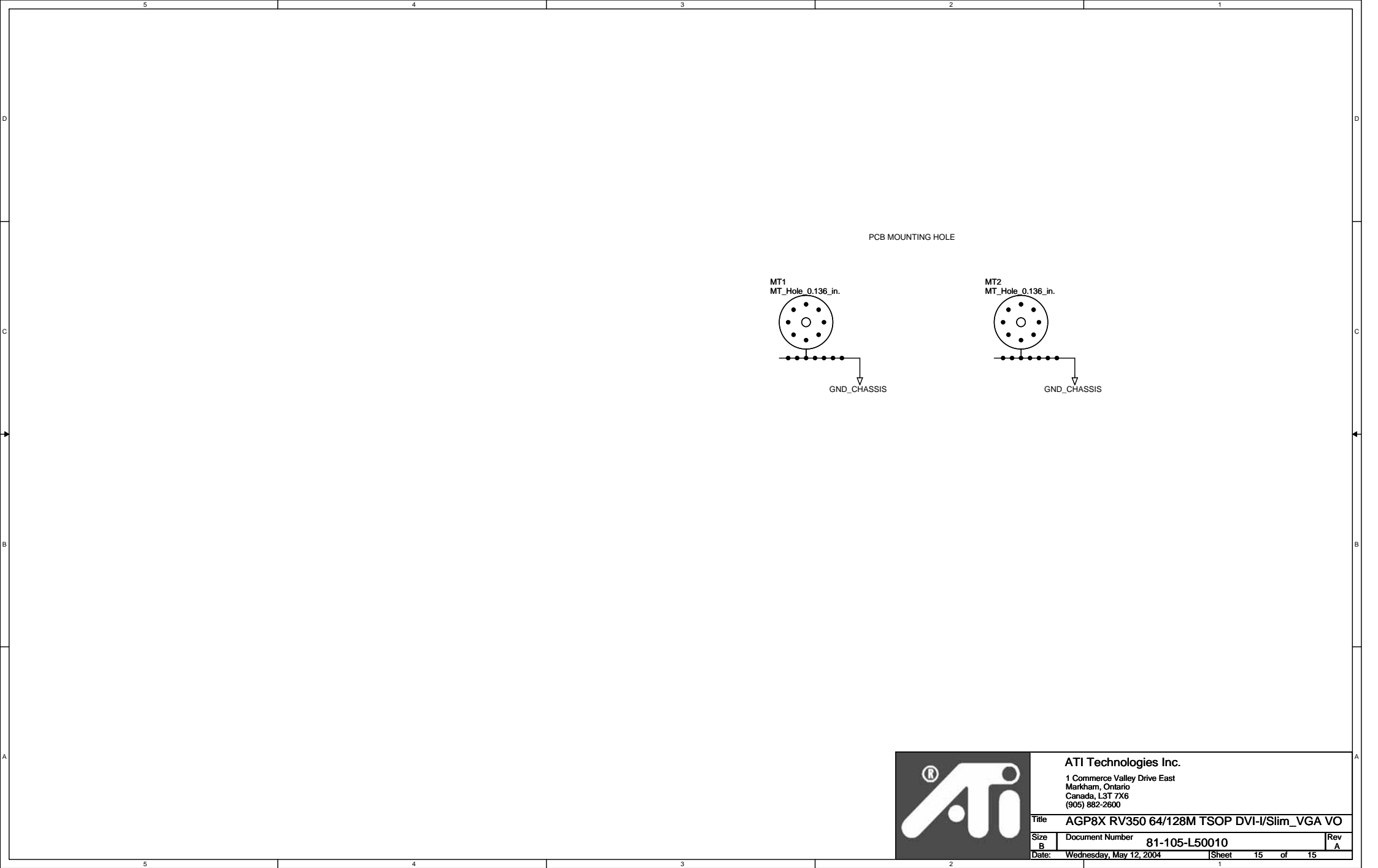


Place close to connector J5



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2800

Title	AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO		
Size	Custom	Document Number	81-105-L50XXX
Date	Wednesday, May 12, 2004	Sheet	14 of 15
Rev	1.0		



ATI Technologies Inc.
1 Commerce Valley Drive East
Markham, Ontario
Canada, L3T 7X6
(905) 882-2600

Title	AGP8X RV350 64/128M TSOP DVI-I/Slim_VGA VO		
Size	Document Number	81-105-L50010	Rev
B			A
Date:	Wednesday, May 12, 2004	Sheet	15 of 15