H61H2-A

Rev : 1.0

ECS CONFIDENTIAL

TABLE OF CONTENTS

REVISION HISTORY:

Rev	Date	Notes
V.A	2010/12/16	Change from H67H2-M3: 1. Rear IO(VGA and DVI) 2. Three PCIEX1 Slots 3. Super IO change to IT8728 4. CPU PWM and VCCIO change to UPI 5. Remove USB3.0 6. Remove EZ Charger
	Component 893PCS	
V.1.0	2011/01/20 81-605-Y96100	Change from V.A: 1.All-Solid Capacitor 2.Fix EZ charger 3. RT to 0402

RD - ELI

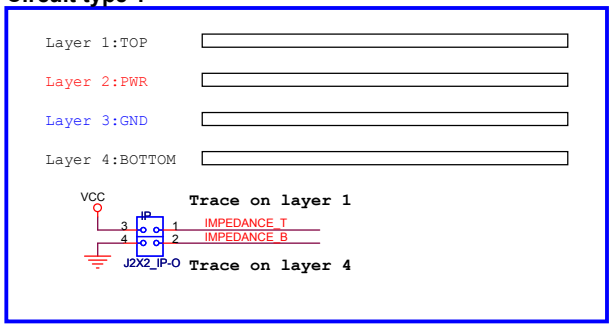
LAYOUT : Bing

NOTE:

Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev1_5.pdf

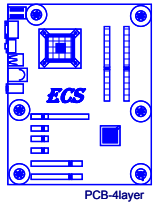
443554_443554_Intel6Series_C200Series_Chipset_EDS_Rev1_5.pdf

Circuit type 1



PCB Impedance control

Impedance (OHM)	Trace Width (mil)	(S/W/S)	Trace Length (inch)	Pre-preg	Default
50	4	(16/4/16)	8	1080	TOP BOTTOM
60	5	(20/5/20)	10	2116	INT



PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

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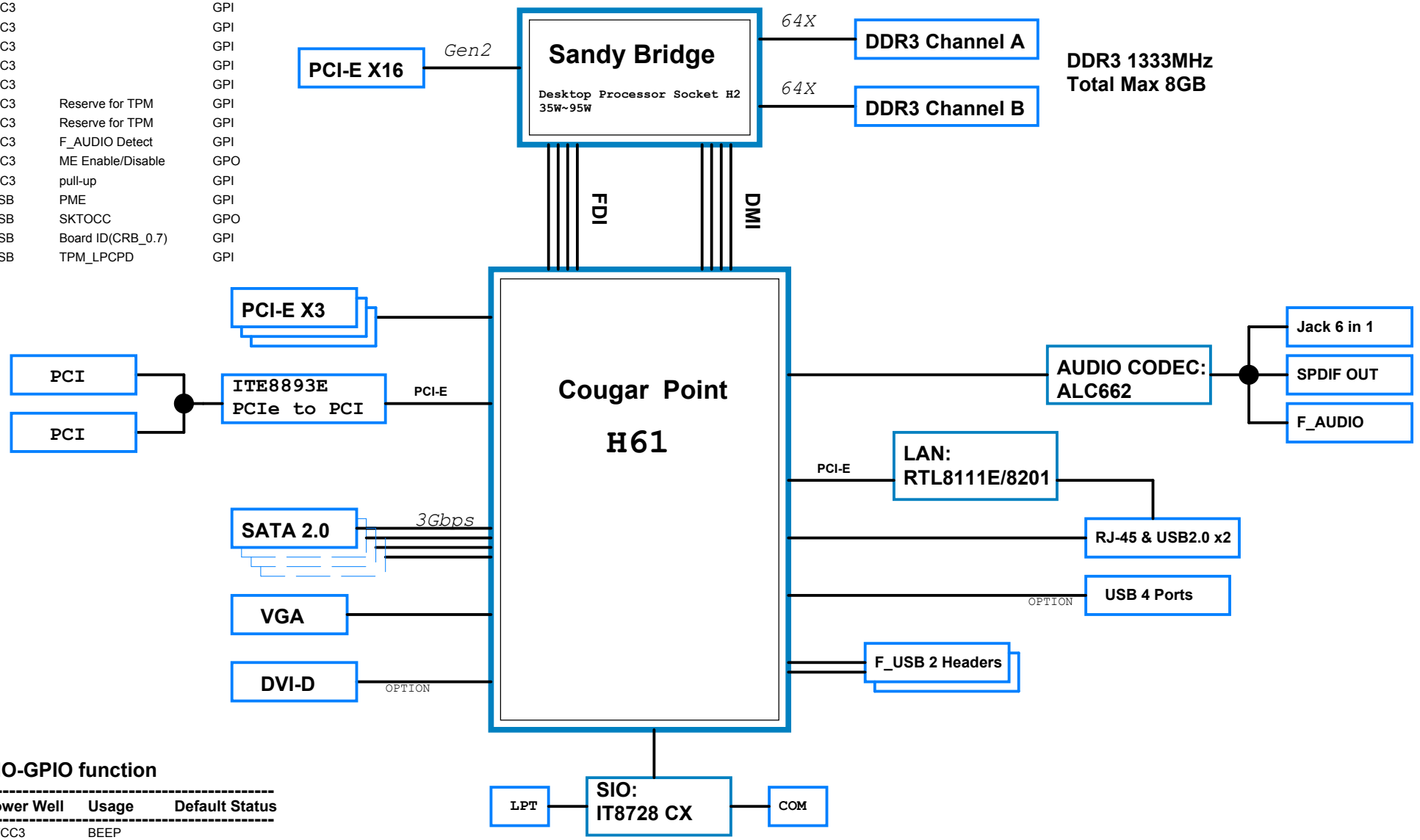
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

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Title: Block Diagram

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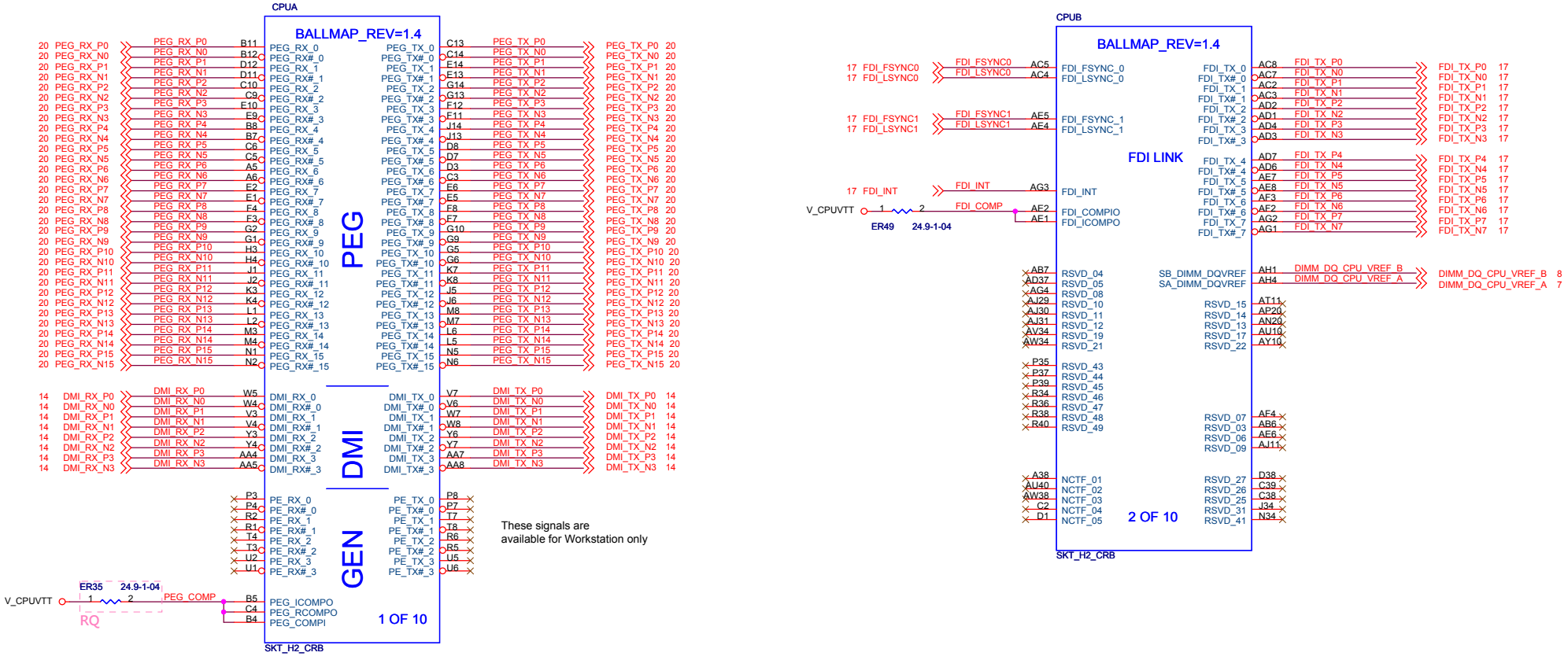
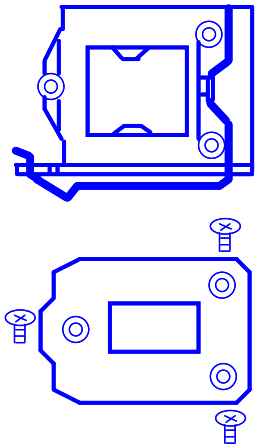


SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

CPU(104)
CPU_SUBASSY_STEEL



01-201-082010 PCH BD82H61 B2

11-018-115124 SOCKET.CPU..LGA 1155P SMD..G/F..BLACK.ACA-ZIF-096-P02.LOTES

11-018-115013 SOCKET.CPU..LGA 1155P SMD.G/F.BLACK.2069965-3.TYCO

20-800-005111 SUBASSY.STEEL.LGA 1155P.W/BACK PLATE.ACA-ZIF-082-P23.LOTES

20-800-004811 SUBASSY.STEEL.LGA 1156P.W/BACK PLATE.2069838-4.TYCO

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Title	CPU - DMI/FDI/PEG	
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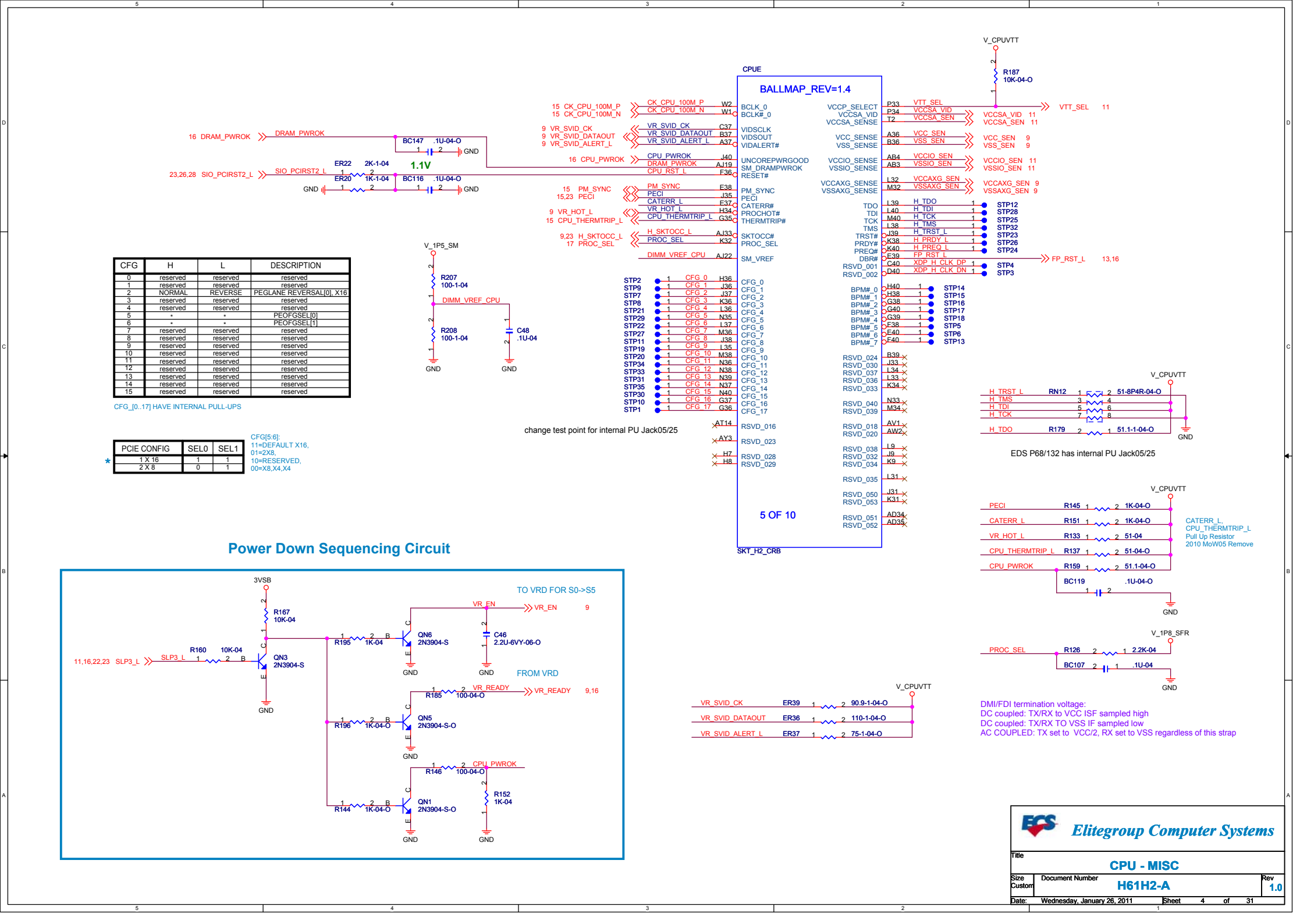
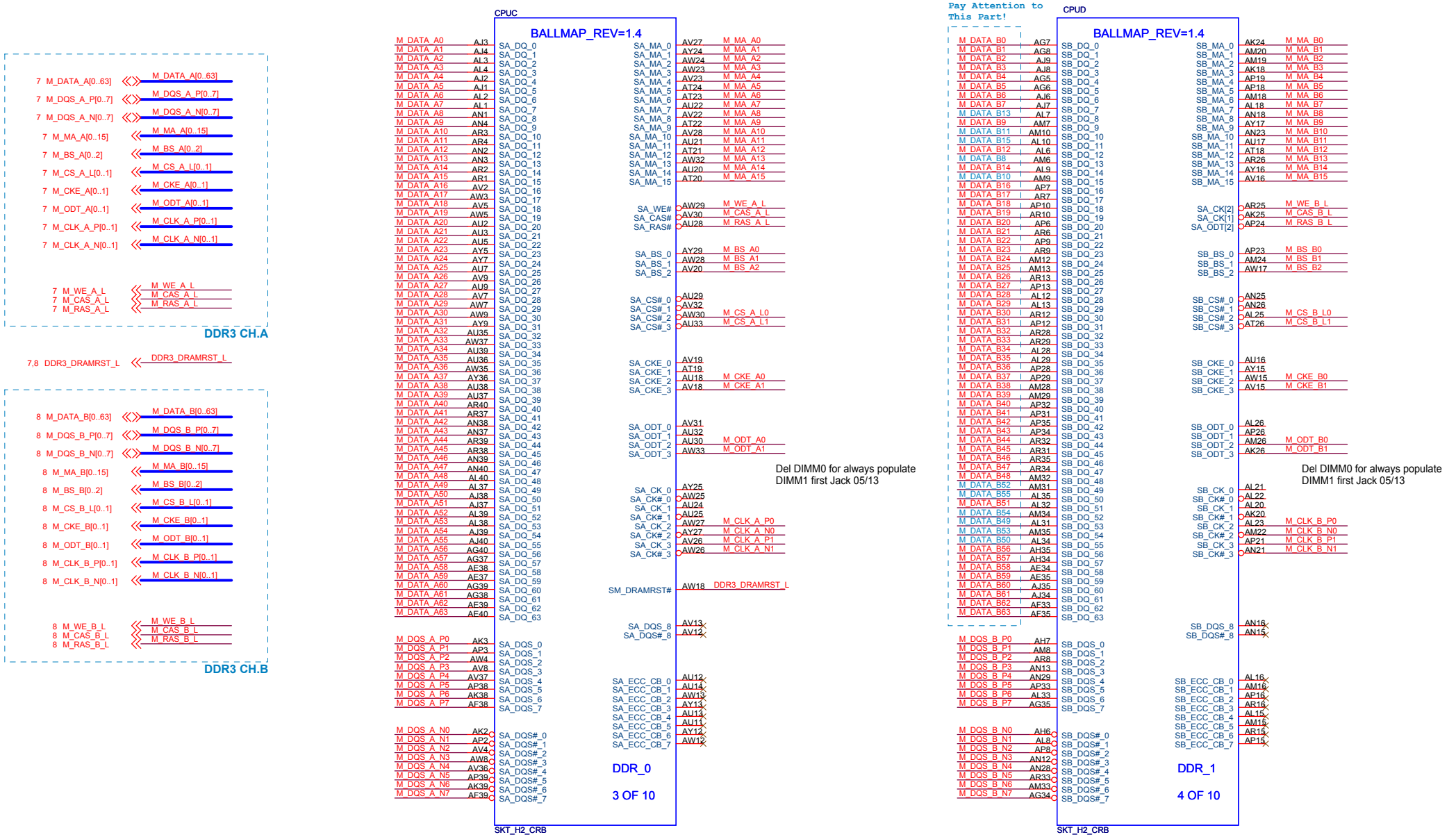


CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SEL0	SEL1
* 1 X 16	1	1
2 X 8	0	1



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Title	CPU - DDR3	
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MAX 112A

1.05V/1.00V
MAX 8.5A

1.5V
MAX 4.5A

MAX 35A

0.925V/0.85V
MAX 8.8A

1.8V
MAX 1A

CPUF
BALLMAP_REV=1.4
6 OF 10
SKT_H2_CRB

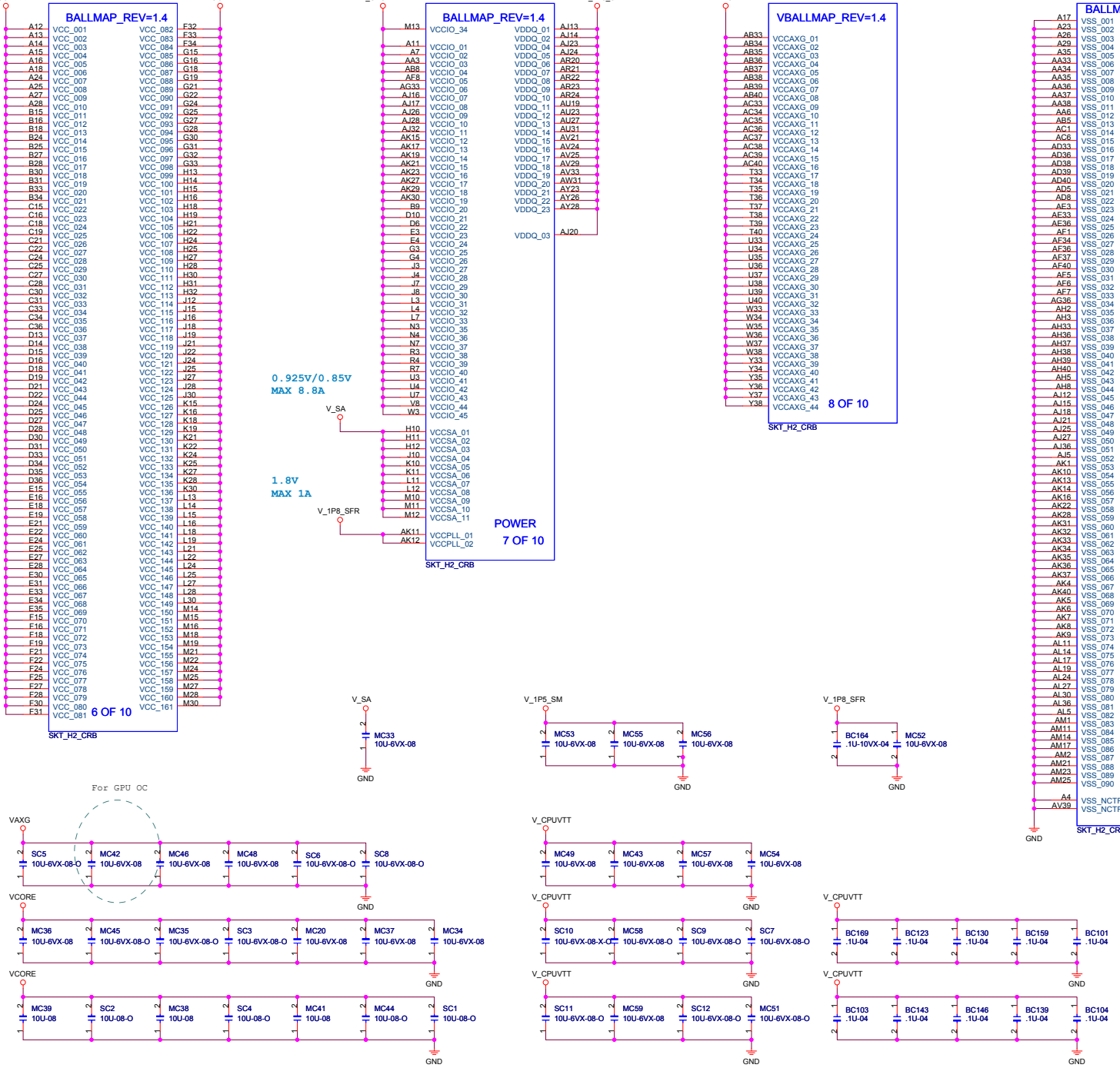
CPUG
BALLMAP_REV=1.4
POWER
7 OF 10
SKT_H2_CRB

CPUH
VBALLMAP_REV=1.4
8 OF 10
SKT_H2_CRB

CPUI
BALLMAP_REV=1.4
9 OF 10
SKT_H2_CRB

CPUJ
BALLMAP_REV=1.4
10 of 10
SKT_H2_CRB

For GPU OC



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Title: CPU - PWR

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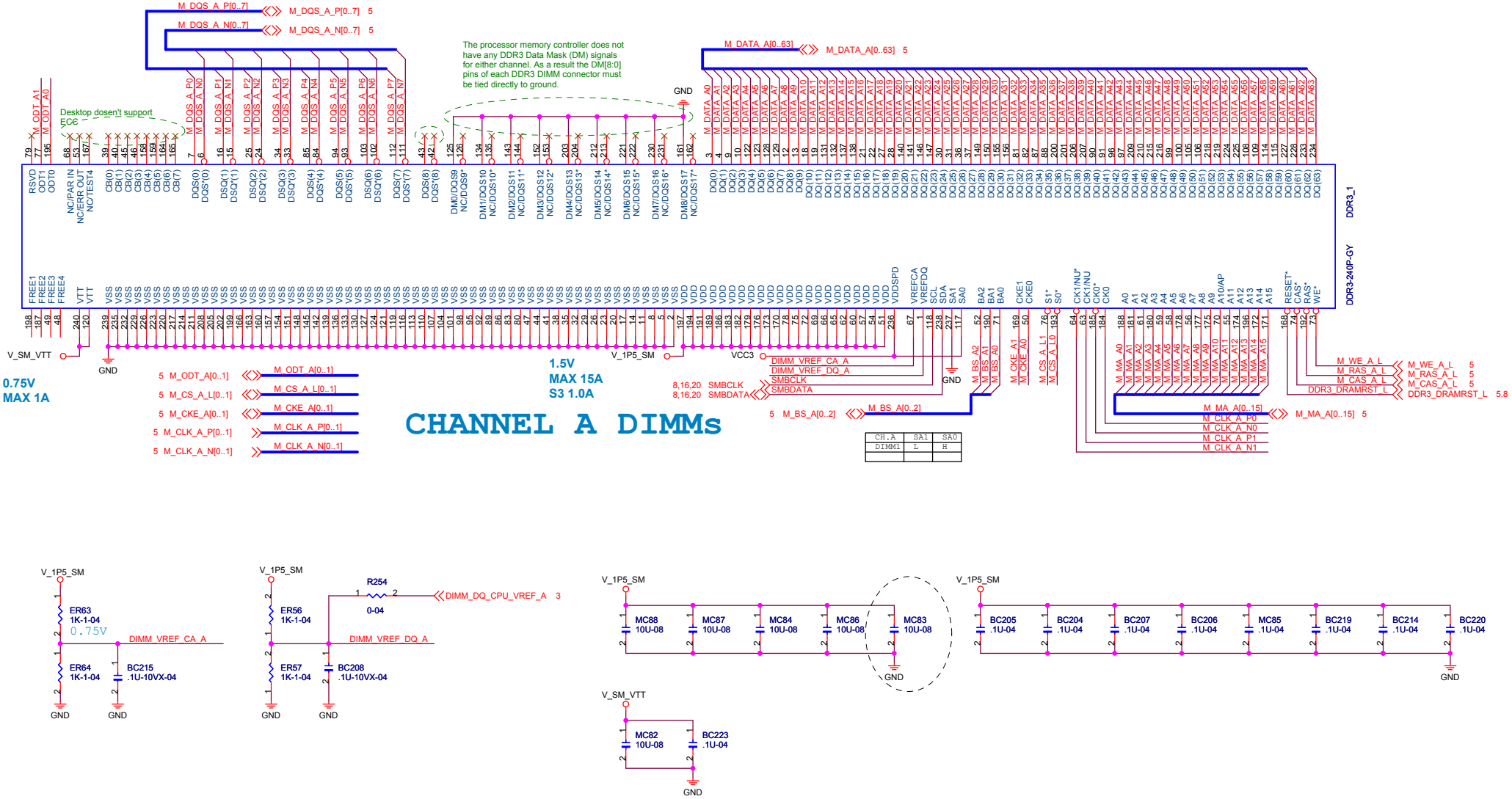

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Title: DDR3 - CH_A_DIMM1

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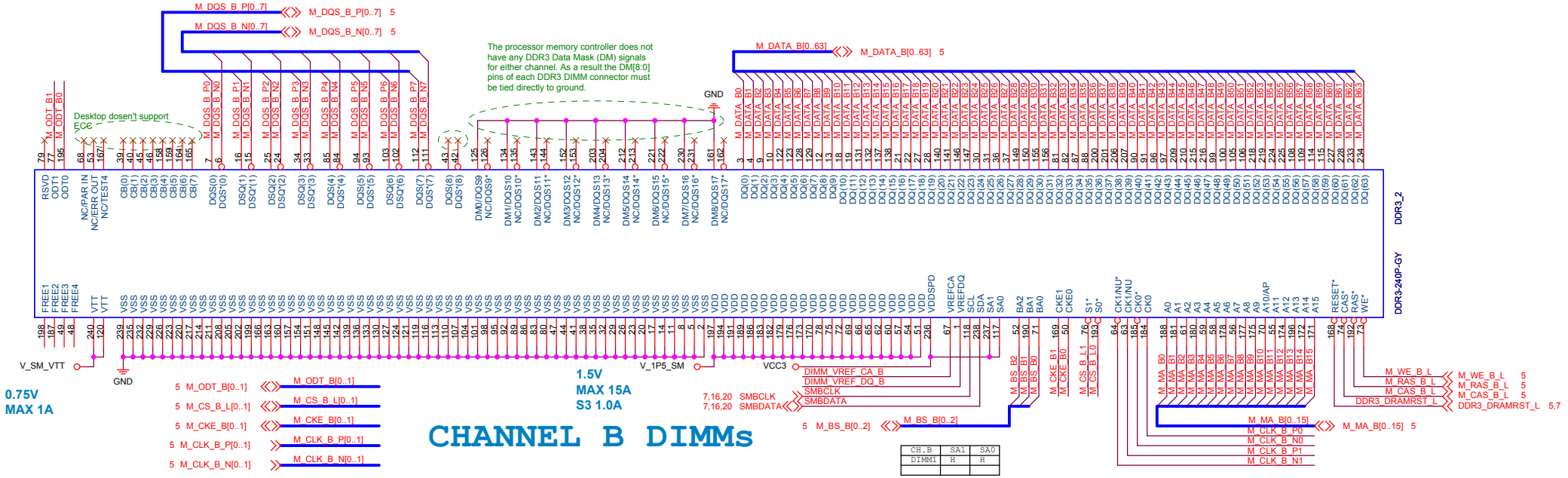
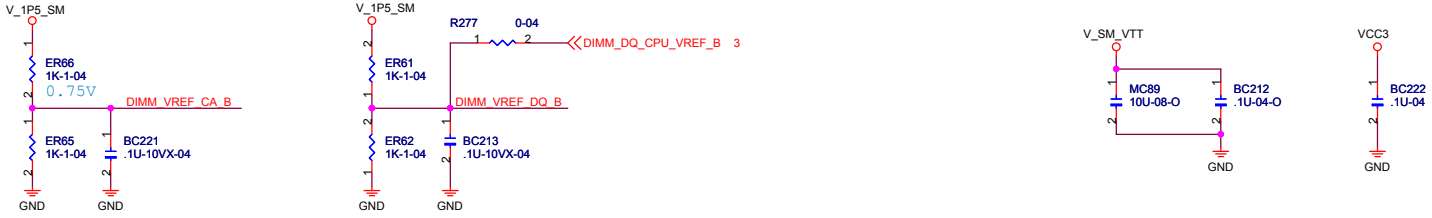


CHANNEL B DIMMs



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Title: DDR3 - CH_B_DIMM2			
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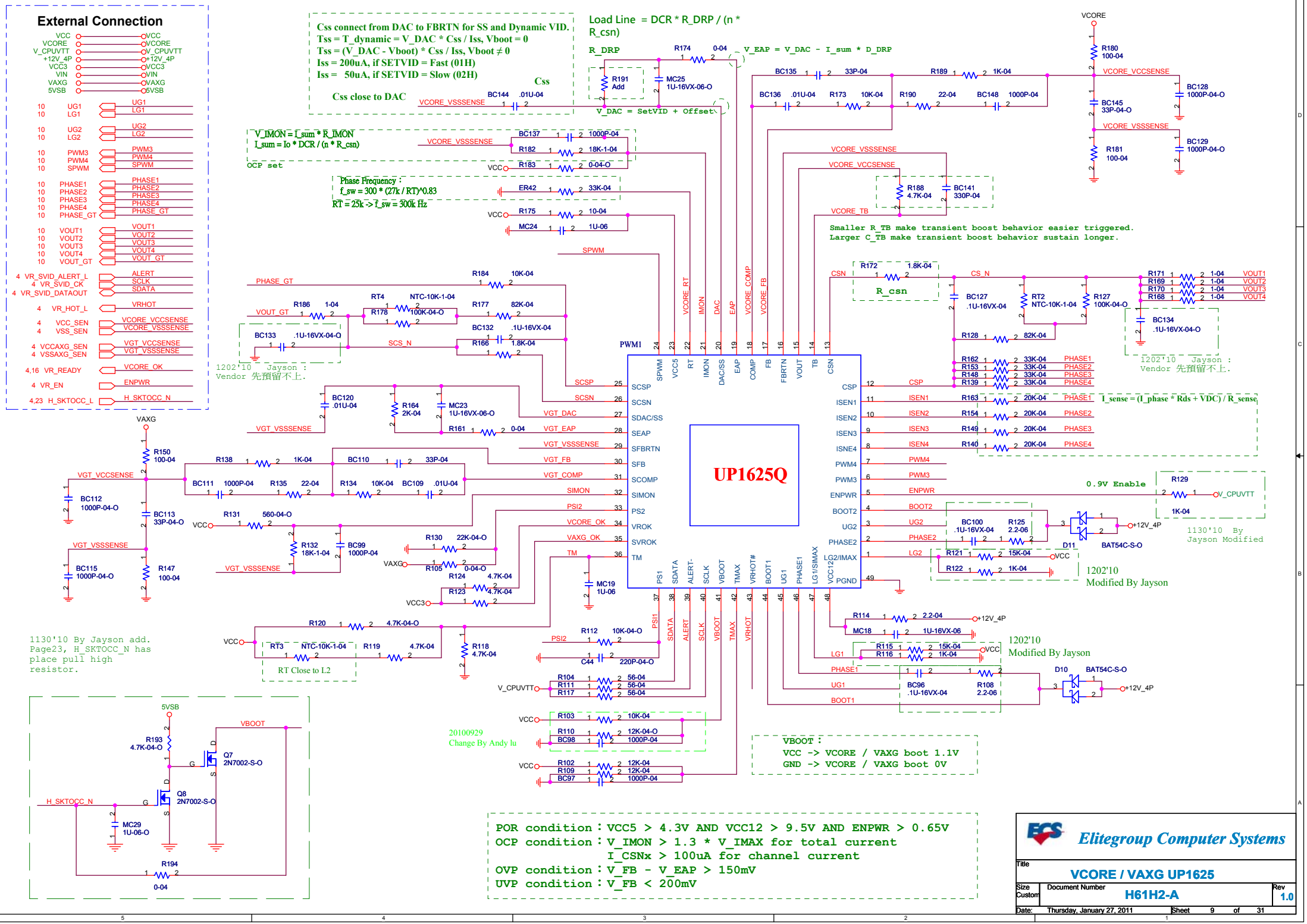
External Connection
VCC
VCORE
V_CPUVTT
+12V_4P
VCC3
VIN
VAXG
5VSB
UG1
LG1
UG2
LG2
PWM3
PWM4
SPWM
PHASE1
PHASE2
PHASE3
PHASE4
PHASE_GT
VOUT1
VOUT2
VOUT3
VOUT4
VOUT_GT
ALERT
SCLK
SDATA
VRHOT
VCORE_VCCSENSE
VCORE_VSSSENSE
VGT_VCCSENSE
VGT_VSSSENSE
VCORE_OK
ENPWR
H_SKTOCC_N
Css connect from DAC to FBRTN for SS and Dynamic VID.
Tss = T_dynamic = V_DAC * Css / Iss, Vboot = 0
Tss = (V_DAC - Vboot) * Css / Iss, Vboot ≠ 0
Iss = 200uA, if SETVID = Fast (01H)
Iss = 50uA, if SETVID = Slow (02H)
Css close to DAC
Load Line = DCR * R_DRP / (n * R_csn)
R_DRP
V_EAP = V_DAC - I_sum * D_DRP
V_DAC = SetVID + Offset
V_IMON = I_sum * R_IMON
I_sum = Io * DCR / (n * R_csn)
OCP set
Phase Frequency :
f_sw = 300 * (27k / RT)^0.83
RT = 25k -> f_sw = 300k Hz
Smaller R_TB make transient boost behavior easier triggered.
Larger C_TB make transient boost behavior sustain longer.
R_csn
I_sense = (I_phase * Rds + VDC) / R_sense
0.9V Enable
1202'10 Jayson : Vendor 先預留不上.
1202'10 By Jayson Modified
1202'10 Modified By Jayson
1130'10 By Jayson add. Page23, H_SKTOCC_N has place pull high resistor.
RT Close to L2
20100929 Change By Andy lu
VBOOT :
VCC -> VCORE / VAXG boot 1.1V
GND -> VCORE / VAXG boot 0V
UP1625Q
POR condition : VCC5 > 4.3V AND VCC12 > 9.5V AND ENPWR > 0.65V
OCP condition : V_IMON > 1.3 * V_IMAX for total current
I_CSNx > 100uA for channel current
OVP condition : V_FB - V_EAP > 150mV
UVP condition : V_FB < 200mV
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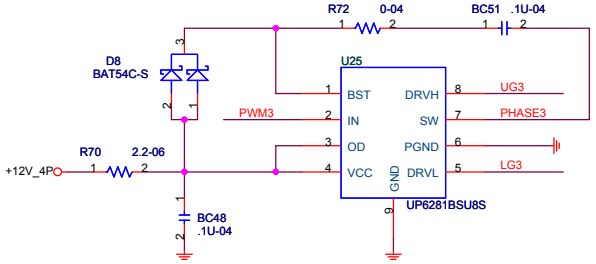
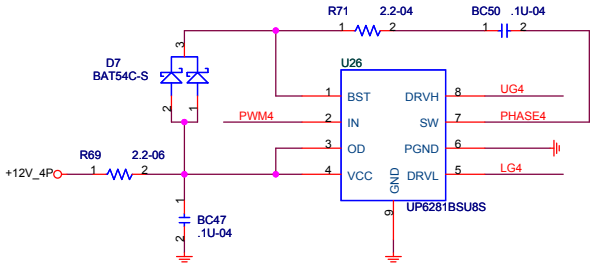
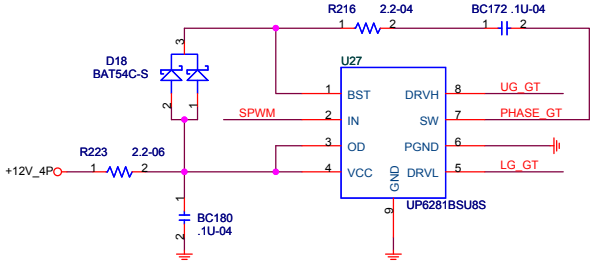
External Connection

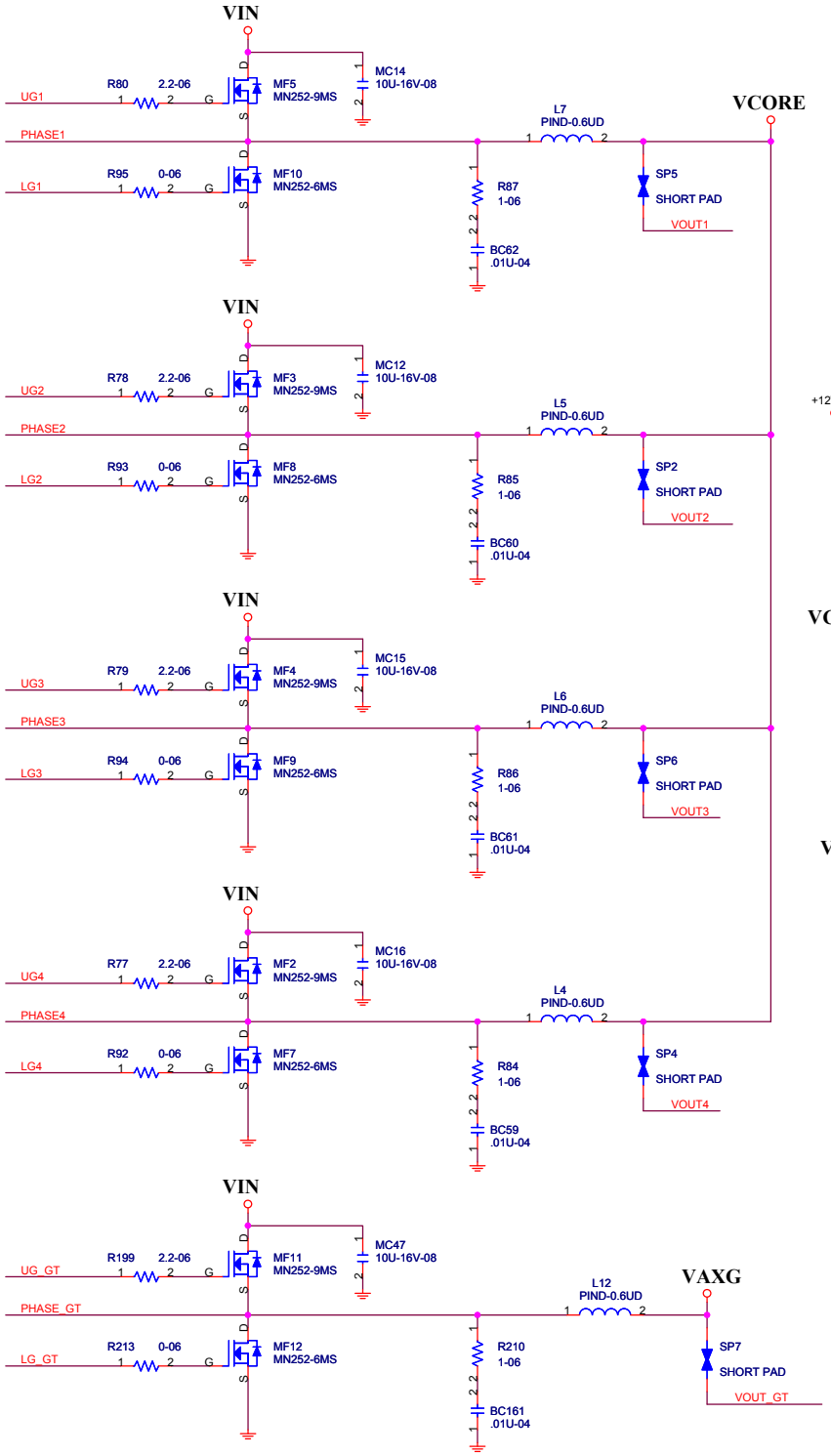
VCC, VCORE, VAXG, +12V_4P, VCC3, VIN

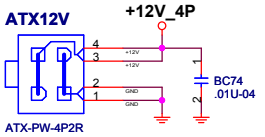
9 UG1, LG1
9 UG2, LG2
9 PWM3, PWM4, SPWM
9 PHASE1, PHASE2, PHASE3, PHASE4, PHASE_GT
9 VOUT1, VOUT2, VOUT3, VOUT4, VOUT_GT

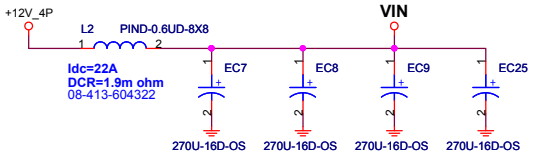


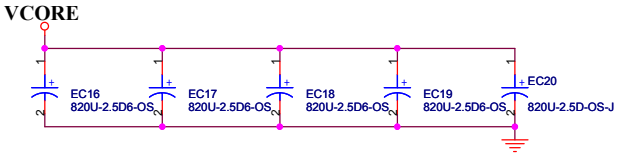


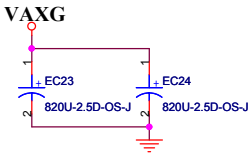












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Title: VCORE / VAXG UP6281

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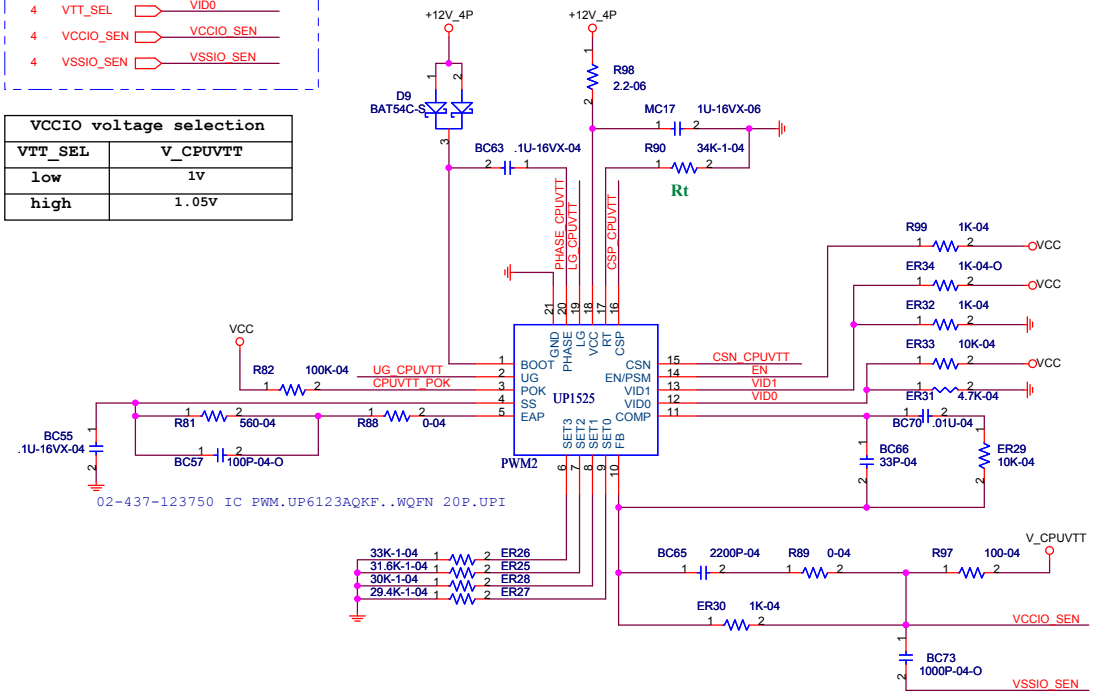
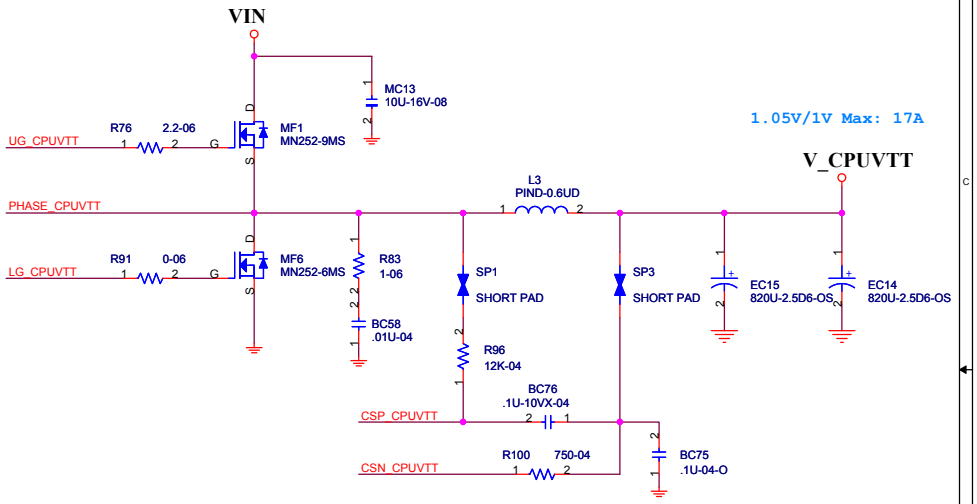
External Connection

	VCC	VCC
	3VSB	3VSB
	5VSB	5VSB
	V_1P05_PCH	V_1P05_PCH
	V_CPUVTT	V_CPUVTT
4	VTT_SEL	VID0
4	VCCIO_SEN	VCCIO_SEN
4	VSSIO_SEN	VSSIO_SEN

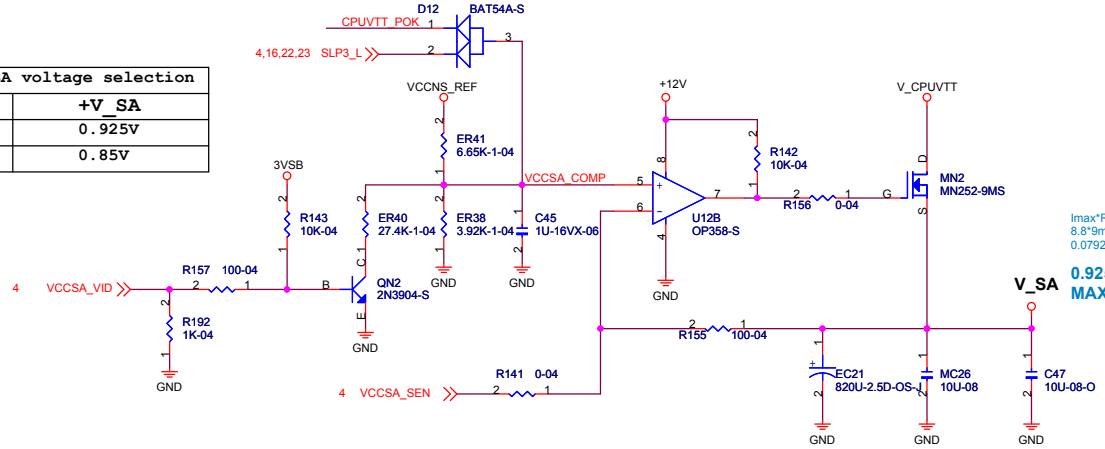
VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

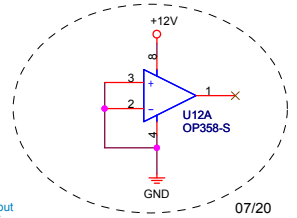
VID Reference Voltage Selection Table		
VID1	VID0	V_CPUVTT
0	0	SET0(1.2V*Rset0/Rt) = 1.0376V
0	1	SET1(1.2V*Rset1/Rt) = 1.0588V
1	0	SET2(1.2V*Rset2/Rt) = 1.1152V
1	1	SET3(1.2V*Rset3/Rt) = 1.1647V





VCCSA voltage selection	
VID	+V_SA
* 0	0.925V
1	0.85V





Imax*Rdson< Vin-Vout
8.8*9m < 1.00-0.925
0.0792 < 0.075

0.925V/0.85V
MAX 8.8A

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GP63	GP64	V_DIMM
0	1	1.26V
0	0	1.36V
1	1	1.56V
1	0	1.71V

DIMM Voltage

DIMM_5VDUAL

DDR3

1.56V@TDC 15A, MAX 20A

V_1P5_SM

For Non-AMT

1.07V

6.2A +2.5A

Chipset Power OCP Rocset (ER98) 15.4KΩ(36A)
Iocset=(40uA*Rocset-0.4V)/Rdson(low side MOSFET)

V_DIMM=0.8V*(1+RT/RB)

GP_V1.05:default OD-->1.05V
Low==>1.1V

0.75V
MAX 0.6A

1.84V
MAX 1.6A

3.36V

Vo=1.25(1+Rb/Rt)
169/100

Refer to page28

3VSB_IO

Vo=Vin*Rb/(Rt+Rb)-0.7
3VSB IO Max=25mA

reserve for LG_DIMM refer to VCC Jack 06/22

EC to MLCC

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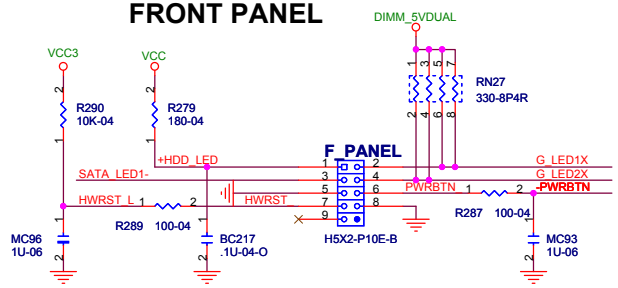
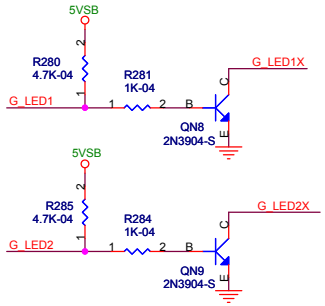
FRONT PANEL

External Connection

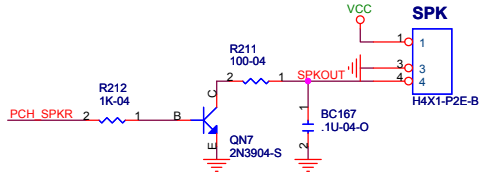
15 SATALED_L — SATA_LED1-
4,16 FP_RST_L — HWRST_L
23 FP_PWRBTN_L — -PWRBTN
23 G_LED1 — G_LED1
23 G_LED2 — G_LED2
16 PCH_SPKR — PCH_SPKR





	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	GB	YB	OFF	OFF

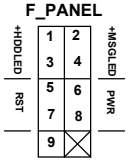
B:Blinking

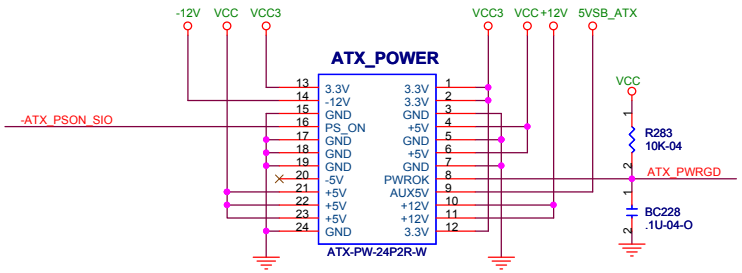


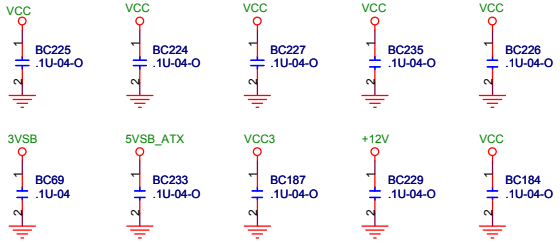
POWER CONNECTOR

External Connection

5VSB_ATX — 5VSB_ATX
VCC3 — VCC3
-12V — -12V
5VSB — 5VSB
VCC — VCC
+12V — +12V
23 PSON_L — -ATX_PSON_SIO
23 ATX_PWRGD — ATX_PWRGD





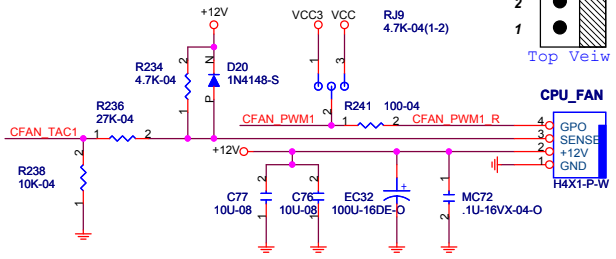


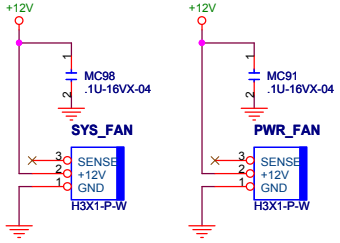
For EMI.

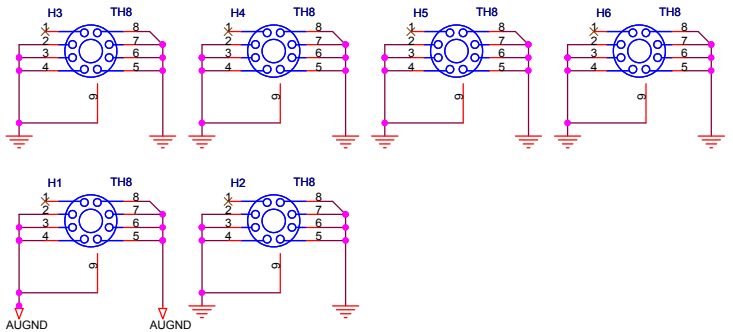
FAN

External Connection

+12V — +12V
VCC — VCC
23 CFAN_PWM1 — CFAN_PWM1
23 CFAN_TAC1 — CFAN_TAC1



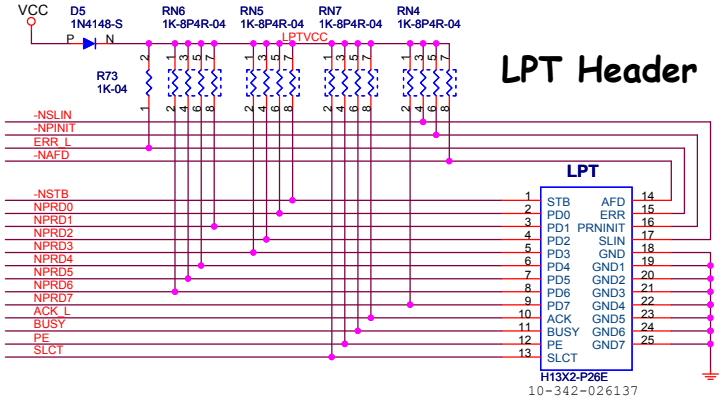




LPT Ports

External Connection

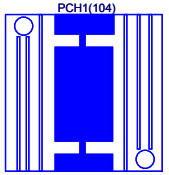
23 PD1 — NPRD1
23 PD4 — NPRD4
23 PD5 — NPRD5
23 PD6 — NPRD6
23 PD0 — NPRD0
23 PD2 — NPRD2
23 STB_L — -NSTB
23 PD3 — NPRD3
23 PD7 — NPRD7
23 AFD_L — -NAFD
23 PINIT_L — -NPINIT
23 SLIN_L — -NSLIN
23 ERR_L — ERR_L
23 ACK_L — ACK_L
23 BUSY — BUSY
23 PE — PE
23 SLCT — SLCT



LPT Header

10-342-026137

604

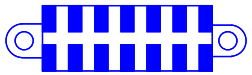


20-120-011476

JP-R

CR2032

JP-WI-P6.25



20-120-011933

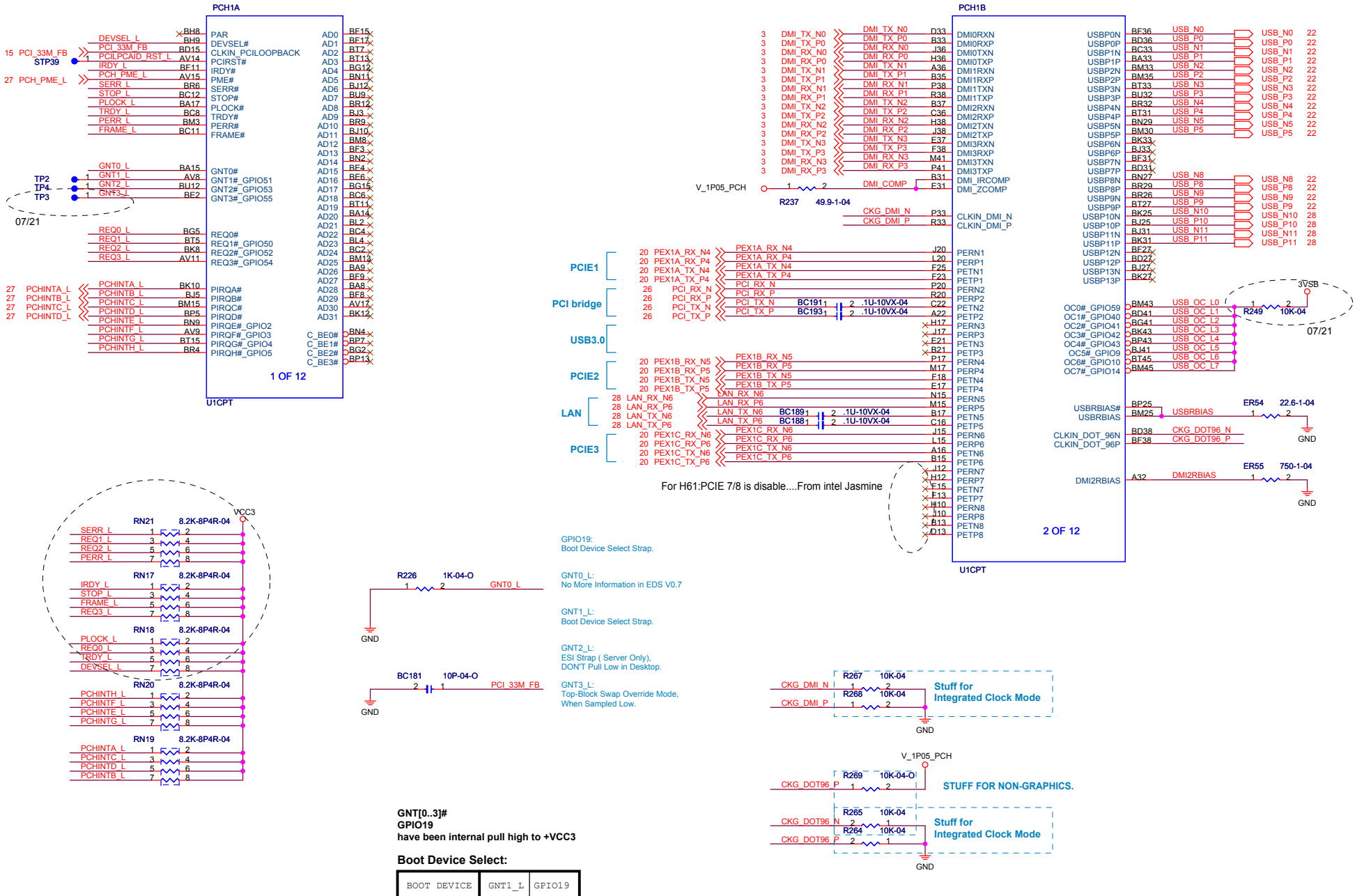
Elitegroup Computer Systems

Title: Front Panel,FAN,PowerConn,GND,104

Size: Custom | Document Number: H61H2-A | Rev: 1.0

Date: Wednesday, January 26, 2011 | Sheet 13 of 31

For H61:USB 6/7/12/13 is disable



GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
* SPI	1	1

Elitegroup Computer Systems

Title: PCH - DMI/PCI/PE/USB

Size: Custom | Document Number: H61H2-A | Rev: 1.0

Date: Wednesday, January 26, 2011 | Sheet 14 of 31

For H61:SATA port2/3 is disable....From 440377 file

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0, ALSO SUPPORT SATA2.0, SATA1.0.

PCH1H

CLKOUT_PCI0 AT11
CLKOUT_PCI1 AN14
CLKOUT_PCI2 AT12
CLKOUT_PCI3 AT17
CLKOUT_PCILOOPBACK AT14
CLKOUTFLEX0_GPIO64 AT9
CLKOUTFLEX1_GPIO65 BA5
CLKOUTFLEX2_GPIO66 AW5
CLKOUTFLEX3_GPIO67 BA2
XCLK_RCOMP AL2
REFCLK14IN AN8
XTAL25_OUT AJ5
XTAL25_IN AJ3

23 SIO33M — R217 22-04 — SIO33M_R
14 PCI_33M_FB — R219 22-04 — PCI_33M_FB_R
23 SIO48M — R220 22-04 — SIO48M_R
V_1P05_PCH — ER52 90.9-1-04 — XCLK_RCOMP
CKG_14M

PDG 0.7 33 Ω ± 5% for Single-End (except PCI Clocks)

IN

Layout Note:
PCI Clock Max 15000MILS

XTAL_25M_PCH_OUT
XTAL_25M_PCH_IN
ER50 1M-04
X2 X-25M
C50 22P-04
C49 22P-04
GND

CLKIN_GND1_N R27 CKG_CPU_N
CLKIN_GND1_P P27 CKG_CPU_P
CLKIN_GND0_N W53 CK_PD_N
CLKIN_GND0_P V52 CK_PD_P
CLKOUT_ITPXDP_N R52
CLKOUT_ITPXDP_P N52
CLKOUT_PCIE7N AE2
CLKOUT_PCIE7P AF1
CLKOUT_DMI_N P31 CK_CPU_100M_N 4
CLKOUT_DMI_P R31 CK_CPU_100M_P 4
CLKOUT_DP_N N56
CLKOUT_DP_P M55
CLKOUT_PCIE0N AE6
CLKOUT_PCIE0P AC6
CLKOUT_PCIE1N AA5 CK_PE_100M_PCI_L 26
CLKOUT_PCIE1P W5 CK_PE_100M_PCI_H 26
CLKOUT_PCIE2N AB12 CK_PE_100M_LAN_L 28
CLKOUT_PCIE2P AB14 CK_PE_100M_LAN_H 28
CLKOUT_PCIE3N AB9 PEX1C_100M_N 20
CLKOUT_PCIE3P AB8 PEX1C_100M_P 20
CLKOUT_PCIE4N Y9 PEX1B_100M_N 20
CLKOUT_PCIE4P Y8 PEX1B_100M_P 20
CLKOUT_PCIE5N AF3 PEX1A_100M_N 20
CLKOUT_PCIE5P AG2 PEX1A_100M_P 20
CLKOUT_PCIE6N AB3
CLKOUT_PCIE6P AA2
CLKOUT_PEG_A_N AG8 PEX16_100M_N 20
CLKOUT_PEG_A_P AG9 PEX16_100M_P 20
CLKOUT_PEG_B_N AE12
CLKOUT_PEG_B_P AE11

8 of 12

U1CPT

CPU
USB3.0
PCI Bridge
LAN
PCIE3
PCIE2
PCIE1
PCIEx16

MOBILE ONLY, NOT FOR DESKTOP.

* NON AMT
FROM SIO
STP57 PCH_CL_CLK1 BA50
STP61 PCH_CL_DATA1 BF50
STP58 PCH_CL_RST1_L BF49
16,23 PWRGD — PCH_MEPWROK_R BC46
Connect to PWROK on the PCH if not supporting M3

Jack 08/10
12 GP_V1.05
TP5 GPIO69_USBDET2 BM18
TP6 GPIO70_USBDET3 BN17
23 THERMAL ALERT — THERMAL ALERT BP15
STP55 SST_CTL BC43
TP18 GP22 BA53
TP25 GPIO38_KMDET BE54
TP20 GPIO39_CASE0 BF55
TP10 GPIO48_CASE1 AW53

V_1P05_PCH
BC195 .1U-04-O
GND
STITCHING CAPS.

PCH1C

CL_CLK1 BA50
CL_DATA1 BF50
CL_RST1# BF49
APWROK BC46
PWM0 BN21
PWM1 BT21
PWM2 BM20
PWM3 BN19
GP17_BOMDET1 BT17 TACH0_GPIO17
GP1_BOMDET2 BR19 TACH1_GPIO1
GP6_BOMDET3 BA22 TACH2_GPIO6
GP7_BOMDET4 BR16 TACH3_GPIO7
GP_V1.05 BU16 TACH4_GPIO68
GPIO69_USBDET2 BM18 TACH5_GPIO69
GPIO70_USBDET3 BN17 TACH6_GPIO70
THERMAL ALERT BP15 TACH7_GPIO71
SST BC43
GP22 BA53 SCLOCK_GPIO22
GPIO38_KMDET BE54 SLOAD_GPIO38
GPIO39_CASE0 BF55 SDATAOUT0_GPIO39
GPIO48_CASE1 AW53 SDATAOUT1_GPIO48
NC_1 AY20

SATA0RXN AC56 SATA_RX_N0 — SATA_RX_N0 22
SATA0RXP AB55 SATA_RX_P0 — SATA_RX_P0 22
SATA0TXN AE46 SATA_TX_N0 — SATA_TX_N0 22
SATA0TXP AE44 SATA_TX_P0 — SATA_TX_P0 22
SATA1RXN AA53 SATA_RX_N1 — SATA_RX_N1 22
SATA1RXP AA56 SATA_RX_P1 — SATA_RX_P1 22
SATA1TXN AG49 SATA_TX_N1 — SATA_TX_N1 22
SATA1TXP AG47 SATA_TX_P1 — SATA_TX_P1 22
SATA2RXN AL50
SATA2RXP AL49
SATA2TXN AL56
SATA2TXP AL53
SATA3RXN AN46
SATA3RXP AN44
SATA3TXN AN56
SATA3TXP AM55
SATA4RXN AN49 SATA_RX_N4 — SATA_RX_N4 22
SATA4RXP AN50 SATA_RX_P4 — SATA_RX_P4 22
SATA4TXN AT50 SATA_TX_N4 — SATA_TX_N4 22
SATA4TXP AT49 SATA_TX_P4 — SATA_TX_P4 22
SATA5RXN AT46 SATA_RX_N5 — SATA_RX_N5 22
SATA5RXP AT44 SATA_RX_P5 — SATA_RX_P5 22
SATA5TXN AV50 SATA_TX_N5 — SATA_TX_N5 22
SATA5TXP AV49 SATA_TX_P5 — SATA_TX_P5 22
CLKIN_SATA_N AF55 CKG_SATA_N
CLKIN_SATA_P AG56 CKG_SATA_P
SATALED# BF57 SATALED_L — SATALED_L 13
SATAICOMPI AJ55
SATAICOMPO AJ53 SATA1RCOMP — ER59 37.4-1-04 — V_1P05_PCH
SATA0GP_GPIO21 BC54 GPIO21_COM2_DET — TP16
SATA1GP_GPIO19 AY52 GPIO19 — TP22
SATA2GP_GPIO36 BB55 GPIO36_TCM_PST_L — TP27
SATA3GP_GPIO37 BG53 GPIO37_TCM — TP15
SATA4GP_GPIO16 AU56 GPIO16 — TP13
SATA5GP_GPIO49 BA56 GPIO49 — TP12
SATA3COMPI AE54
SATA3RCOMPO AE52 SATA3RCOMP — R261 49.9-1-04 — V_1P05_PCH
TP16 AE50 PCH_TP16 — STP56
SATA3RBIAS AC52 SATA3RBIAS — ER60 750-1-04 — GND
A20GATE BB57 A20GATE — A20GATE 23
INIT3_3V# BN56 INIT3_3V_L — TP19
RCIN# BG56 KBRST_L — KBRST_L 23
SERIRQ AV52 SER_IRQ — SER_IRQ 23
THRMTRIP# E56 CPU_THERMTRIP_L — CPU_THERMTRIP_L 4
PECI H48 PECI_PCH
PMSYNCH F55 PM_SYNC — PM_SYNC 4
PECI_PCH — R270 0-04-O — PECI 4,23

3 OF 12

07/21
10/11

Reserve for BOM Detect.

Default GPI set to Pull Up:

VCC3
RN25 8.2K-8P4R-04
SER_IRQ
A20GATE
KBRST_L
R232 10K-04
THERMAL ALERT

GPIO36_TCM_PST_L, GPIO37_TCM: TCM Header In Eanble TCM, Disable TPM.

GPIO16, GPIO49: Reserve for TPM.

R257 10K-04 CKG_SATA_N
R256 10K-04 CKG_SATA_P
GND
Stuff for Integrated Clock Mode

BC173 10P-04-O SIO33M_R
BC176 10P-04-O PCI_33M_FB_R
BC182 10P-04-O SIO48M_R
GND

R263 10K-04 CK_PD_P
R262 10K-04 CK_PD_N
R240 10K-04 CKG_CPU_P
R242 10K-04 CKG_CPU_N
GND

R221 10K-04 CKG_14M
CKa
GND
Stuff for Integrated Clock Mode

Clock Mode	CLK GEN. IDT CV184 Circuit.	CKa
* Integrated Clock Mode	X	V
Buffer Through Mode	V	X

RJ8 10K-04(1-2) GP1_BOMDET2
Detect USB3.0 control IC
RJ7 10K-04(1-2) GP17_BOMDET1
RJ6 10K-04(1-2) GP6_BOMDET3
RJ5 10K-04(1-2) GP7_BOMDET4
VCC3
GND

Elitegroup Computer Systems

Title: PCH - SATA / CLK

Size: Custom
Document Number: H61H2-A
Rev: 1.0

Date: Wednesday, January 26, 2011
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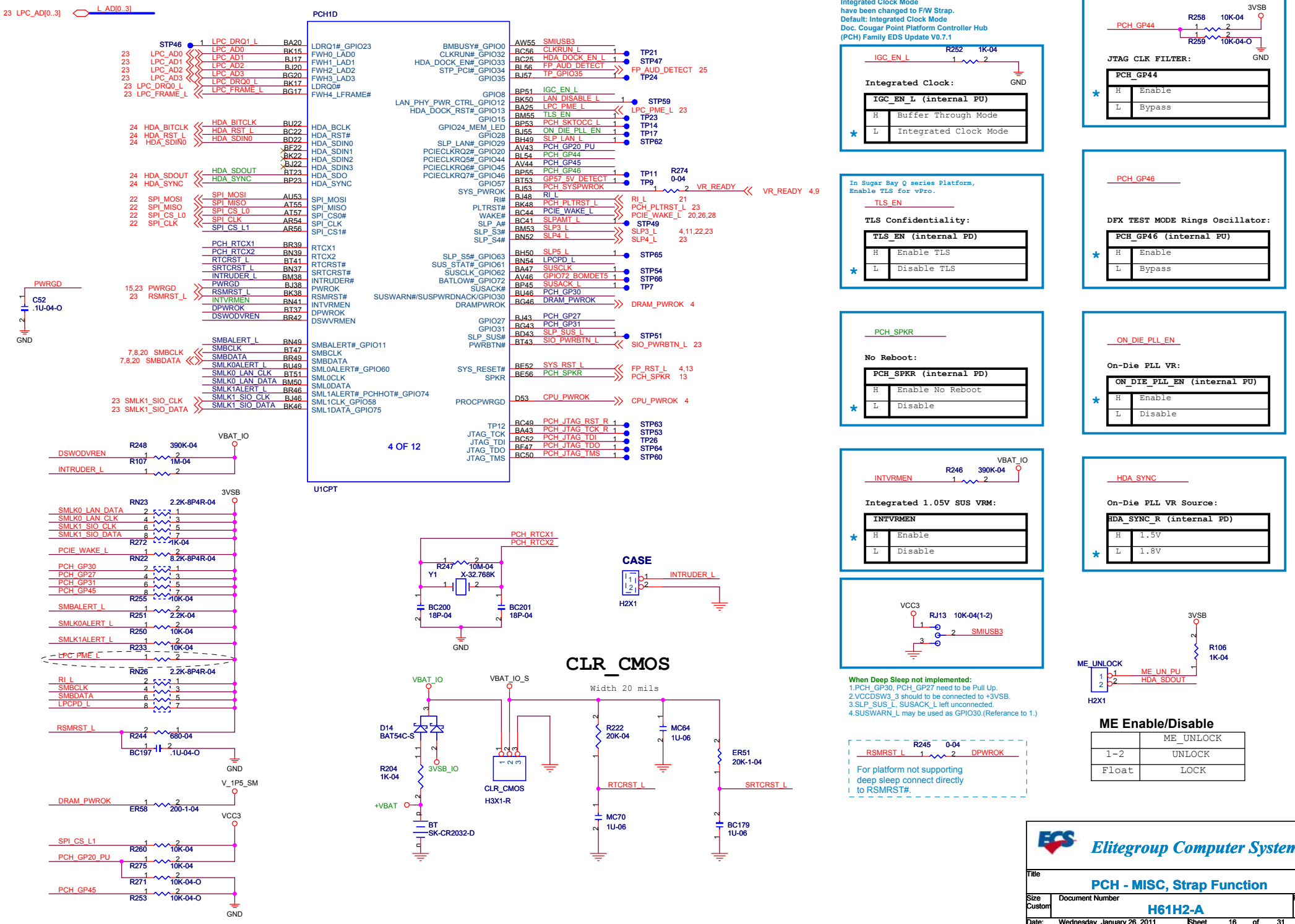
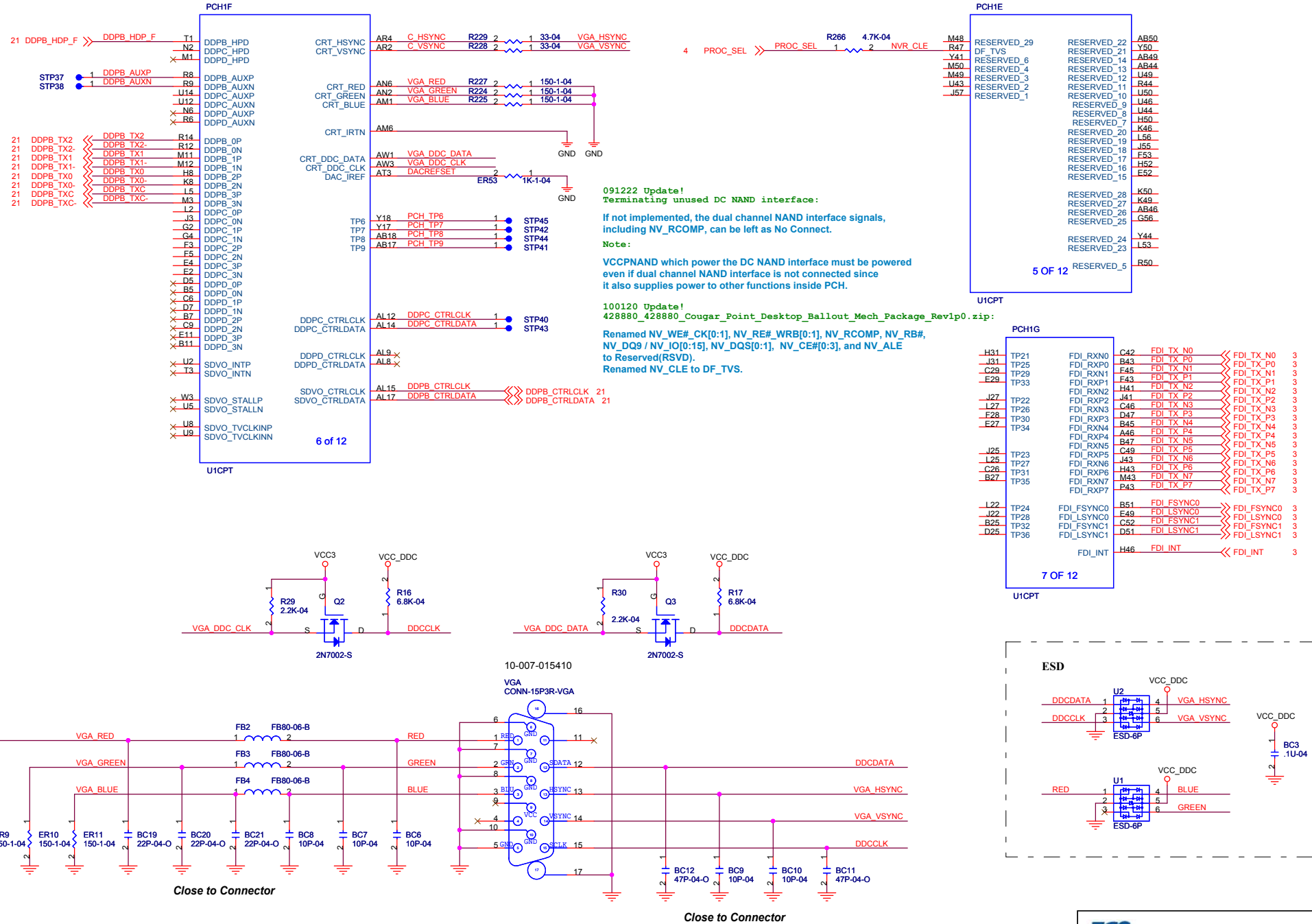
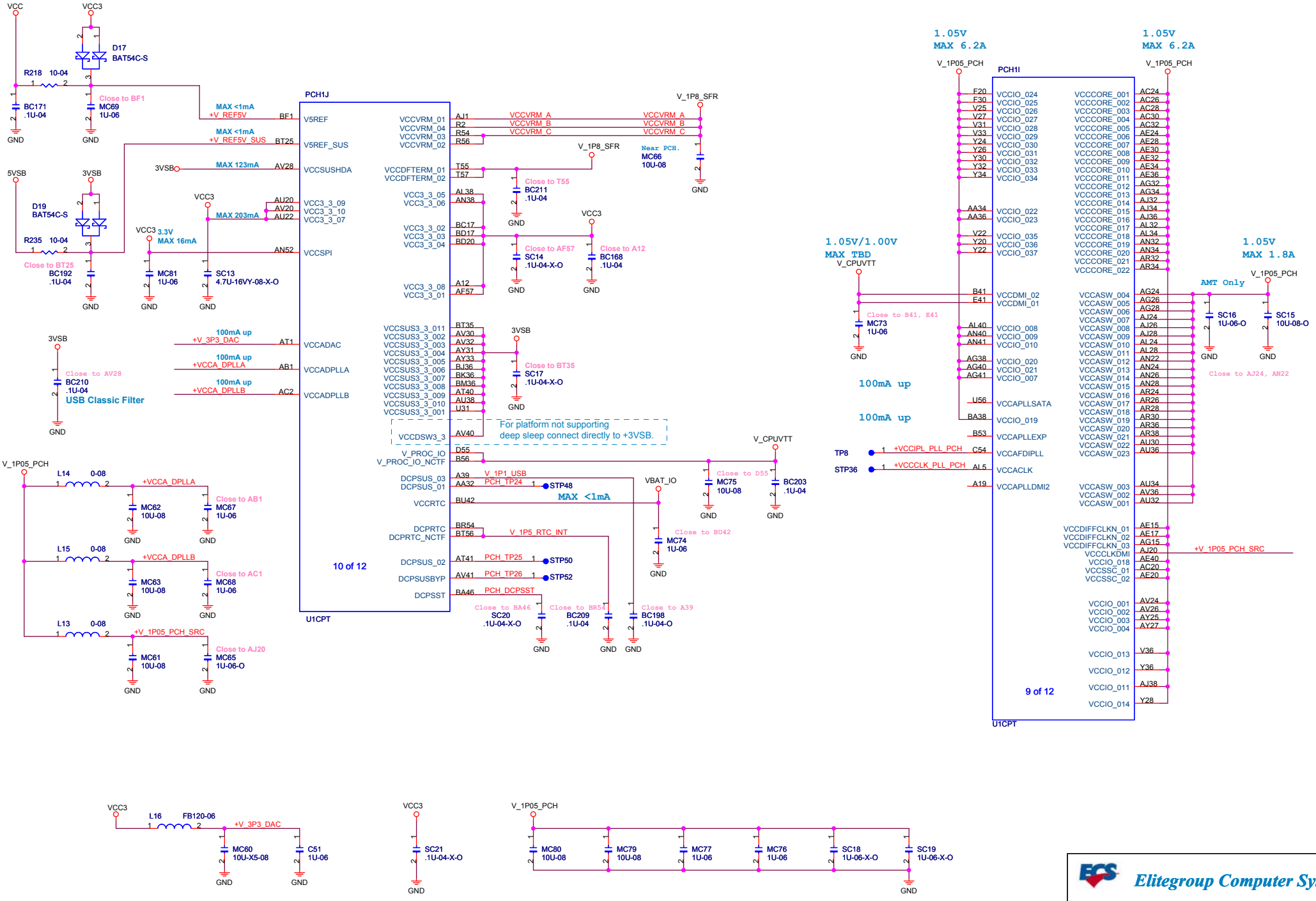
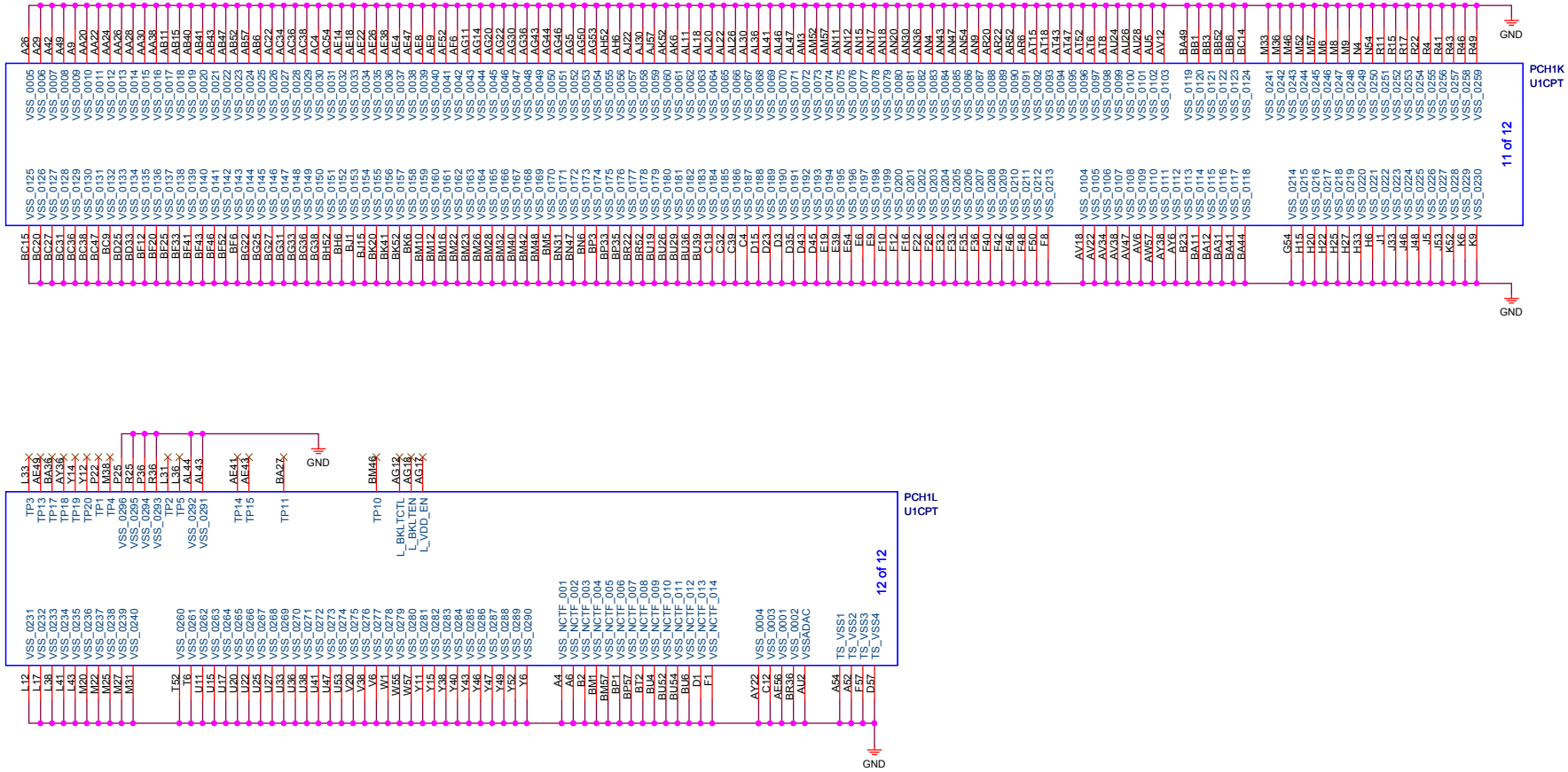

23 LPC_AD[0..3]
L_AD[0..3]
PCH1D
STP46
LPC_DRQ1_L
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ0_L
LPC_FRAME_L
HDA_BITCLK
HDA_RST_L
HDA_SDIN0
HDA_SDOUT
HDA_SYNC
SPI_MOSI
SPI_MISO
SPI_CS_L0
SPI_CLK
SPI_CS_L1
PCH_RTCX1
PCH_RTCX2
RTCRST_L
SRTCRST_L
INTRUDER_L
PWRGD
RSMRST_L
INTVRMEN
DPWROK
DSWODVREN
SMBALERT_L
SMBCLK
SMBDATA
SMLK0ALERT_L
SMLK0_LAN_CLK
SMLK0_LAN_DATA
SMLK1ALERT_L
SMLK1_SIO_CLK
SMLK1_SIO_DATA
LDRQ1#_GPIO23
FWH0_LAD0
FWH1_LAD1
FWH2_LAD2
FWH3_LAD3
LDRQ0#
FWH4_LFRAME#
HDA_BCLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_SYNC
SPI_MOSI
SPI_MISO
SPI_CS0#
SPI_CLK
SPI_CS1#
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
PWROK
RSMRST#
INTVRMEN
DPWROK
DSWVRMEN
SMBALERT#_GPIO11
SMBCLK
SMBDATA
SML0ALERT#_GPIO60
SML0CLK
SML0DATA
SML1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO58
SML1DATA_GPIO75
BMBUSY#_GPIO0
CLKRUN#_GPIO32
HDA_DOCK_EN#_GPIO33
STP_PCI#_GPIO34
GPIO35
GPIO8
LAN_PHY_PWR_CTRL_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO24_MEM_LED
GPIO28
SLP_LAN#_GPIO29
PCIECLKRQ2#_GPIO20
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK
RI#
PLTRST#
WAKE#
SLP_A#
SLP_S3#
SLP_S4#
SLP_S5#_GPIO63
SUS_STAT#_GPIO61
SUSCLK_GPIO62
BATLOW#_GPIO72
SUSACK#
SUSWARN#/SUSPWRDNACK/GPIO30
DRAMPWROK
GPIO27
GPIO31
SLP_SUS#
PWRBTN#
SYS_RESET#
SPKR
PROCPWRGD
TP12
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
SMIUSB3
CLKRUN_L
HDA_DOCK_EN_L
FP_AUD_DETECT
TP_GPIO35
IGC_EN_L
LAN_DISABLE_L
LPC_PME_L
TLS_EN
PCH_SKTOCC_L
ON_DIE_PLL_EN
SLP_LAN_L
PCH_GP20_PU
PCH_GP44
PCH_GP45
PCH_GP46
GP57_5V_DETECT
PCH_SYSPWROK
RI_L
PCH_PLTRST_L
PCIE_WAKE_L
SLPAMT_L
SLP3_L
SLP4_L
SLP5_L
LPCPD_L
SUSCLK
GPIO72_BOMDET5
SUSACK_L
PCH_GP30
DRAM_PWROK
PCH_GP27
PCH_GP31
SLP_SUS_L
SIO_PWRBTN_L
SYS_RST_L
PCH_SPKR
CPU_PWROK
PCH_JTAG_RST_R
PCH_JTAG_TCK_R
PCH_JTAG_TDI
PCH_JTAG_TDO
PCH_JTAG_TMS
4 OF 12
U1CPT
VR_READY
VR_READY 4,9
TP21
STP47
FP_AUD_DETECT 25
TP24
STP59
LPC_PME_L 23
TP23
TP14
TP17
STP62
TP11
TP9
R274
0-04
RI_L 21
PCH_PLTRST_L 23
PCIE_WAKE_L 20,26,28
STP49
SLP3_L 4,11,22,23
SLP4_L 23
STP65
STP54
STP66
TP7
DRAM_PWROK 4
STP51
SIO_PWRBTN_L 23
FP_RST_L 4,13
PCH_SPKR 13
CPU_PWROK 4
STP63
STP53
TP26
STP64
STP60
PWRGD
C52
.1U-04-O
GND
15,23 PWRGD
23 RSMRST_L
7,8,20 SMBCLK
7,8,20 SMBDATA
23 SMLK1_SIO_CLK
23 SMLK1_SIO_DATA
VBAT_IO
R248 390K-04
R107 1M-04
DSWODVREN
INTRUDER_L
3VSB
RN23 2.2K-8P4R-04
SMLK0_LAN_DATA
SMLK0_LAN_CLK
SMLK1_SIO_CLK
SMLK1_SIO_DATA
R272 1K-04
PCIE_WAKE_L
RN22 8.2K-8P4R-04
PCH_GP30
PCH_GP27
PCH_GP31
PCH_GP45
R255 10K-04
SMBALERT_L
R251 2.2K-04
SMLK0ALERT_L
R250 10K-04
SMLK1ALERT_L
R233 10K-04
LPC_PME_L
RN26 2.2K-8P4R-04
RI_L
SMBCLK
SMBDATA
LPCPD_L
RSMRST_L
R244 680-04
BC197 .1U-04-O
GND
V_1P5_SM
DRAM_PWROK
ER58 200-1-04
VCC3
SPI_CS_L1
R260 10K-04
PCH_GP20_PU
R275 10K-04
R271 10K-04-O
PCH_GP45
R253 10K-04-O
GND
PCH_RTCX1
PCH_RTCX2
R247 10M-04
Y1 X-32.768K
BC200 18P-04
BC201 18P-04
GND
CASE
H2X1
INTRUDER_L
CLR_CMOS
Width 20 mils
VBAT_IO
VBAT_IO_S
D14 BAT54C-S
R204 1K-04
3VSB_IO
+VBAT
BT SK-CR2032-D
CLR_CMOS H3X1-R
R222 20K-04
MC70 1U-06
MC64 1U-06
RTCRST_L
ER51 20K-1-04
SRTCRST_L
BC179 1U-06
Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap. Default: Integrated Clock Mode
Doc. Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1
IGC_EN_L
R252 1K-04
GND
Integrated Clock:
IGC_EN_L (internal PU)
H Buffer Through Mode
L Integrated Clock Mode
In Sugar Bay Q series Platform, Enable TLS for vPro.
TLS_EN
TLS Confidentiality:
TLS_EN (internal PD)
H Enable TLS
L Disable TLS
PCH_SPKR
No Reboot:
PCH_SPKR (internal PD)
H Enable No Reboot
L Disable
INTVRMEN
VBAT_IO
R246 390K-04
Integrated 1.05V SUS VRM:
INTVRMEN
H Enable
L Disable
VCC3
RJ13 10K-04(1-2)
SMIUSB3
When Deep Sleep not implemented:
1.PCH_GP30, PCH_GP27 need to be Pull Up.
2.VCCDSW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected.
4.SUSWARN_L may be used as GPIO30.(Reference to 1.)
R245 0-04
RSMRST_L
DPWROK
For platform not supporting deep sleep connect directly to RSMRST#.
3VSB
PCH_GP44
R258 10K-04
R259 10K-04-O
GND
JTAG CLK FILTER:
PCH_GP44
H Enable
L Bypass
PCH_GP46
DFX TEST MODE Rings Oscillator:
PCH_GP46 (internal PU)
H Enable
L Bypass
ON_DIE_PLL_EN
On-Die PLL VR:
ON_DIE_PLL_EN (internal PU)
H Enable
L Disable
HDA_SYNC
On-Die PLL VR Source:
HDA_SYNC_R (internal PD)
H 1.5V
L 1.8V
3VSB
R106 1K-04
ME_UNLOCK
ME_UN_PU
HDA_SDOUT
H2X1
ME Enable/Disable
ME_UNLOCK
1-2 UNLOCK
Float LOCK
Elitegroup Computer Systems
Title
PCH - MISC, Strap Function
Size Custom
Document Number H61H2-A
Rev 1.0
Date: Wednesday, January 26, 2011
Sheet 16 of 31

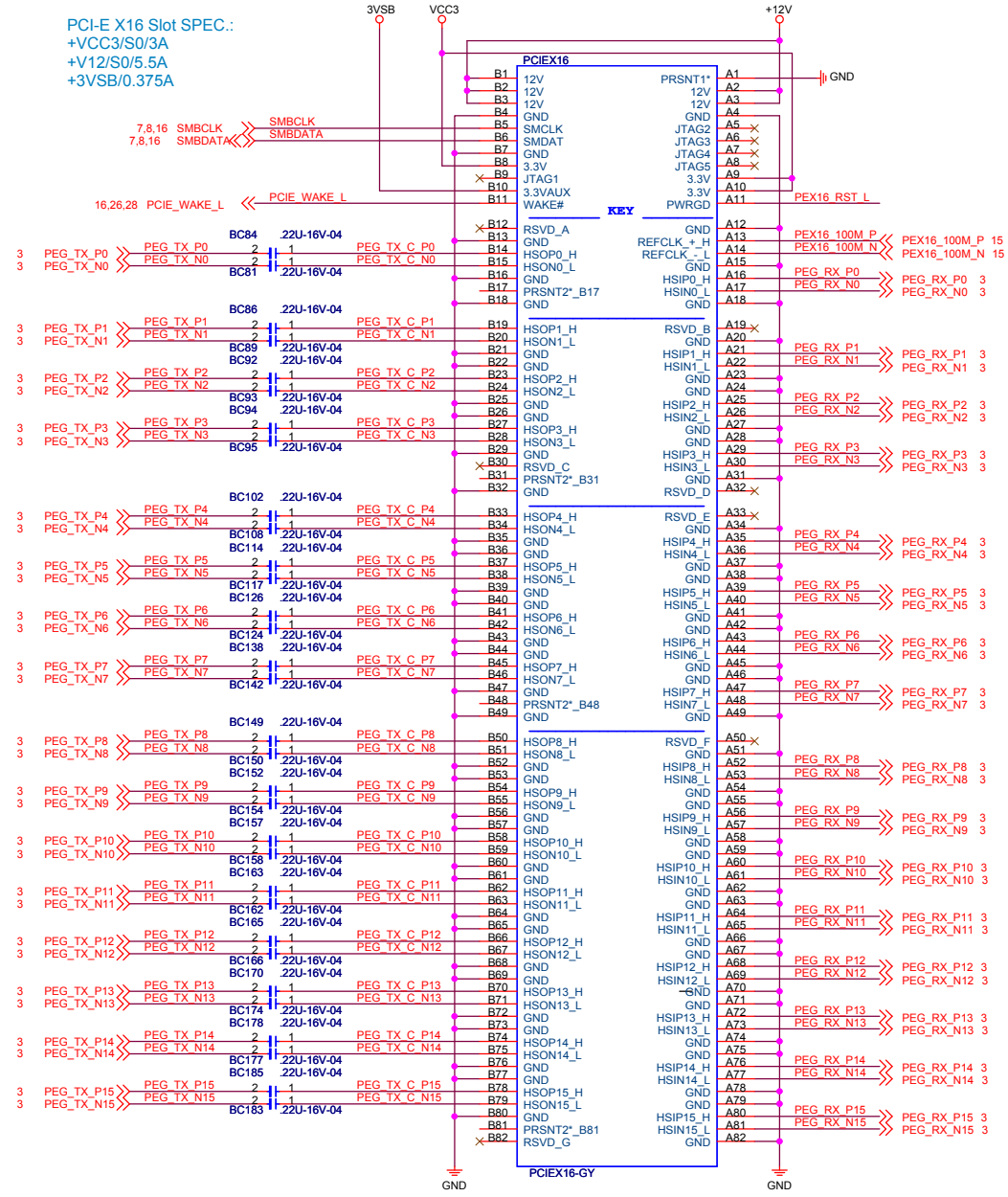


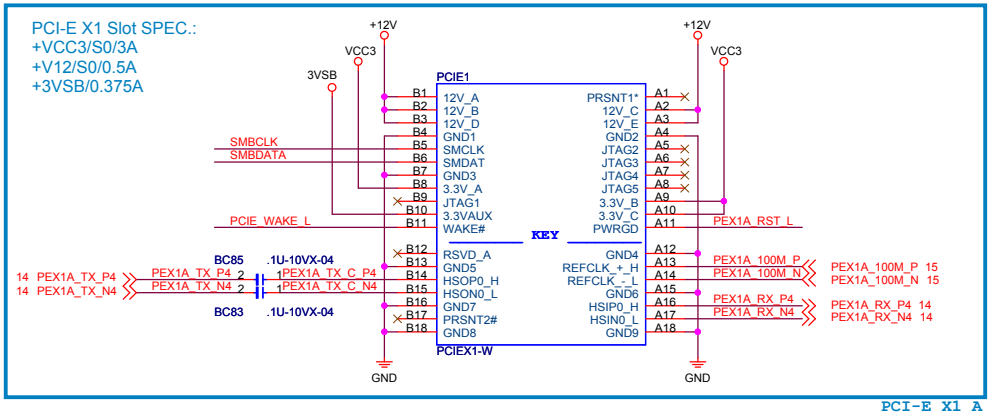
Company	Elitegroup Computer Systems
Title	PCH - DP/VGA/FDI
Size	Custom
Document Number	H61H2-A
Rev	1.0
Date	Wednesday, January 26, 2011
Sheet	17 of 31

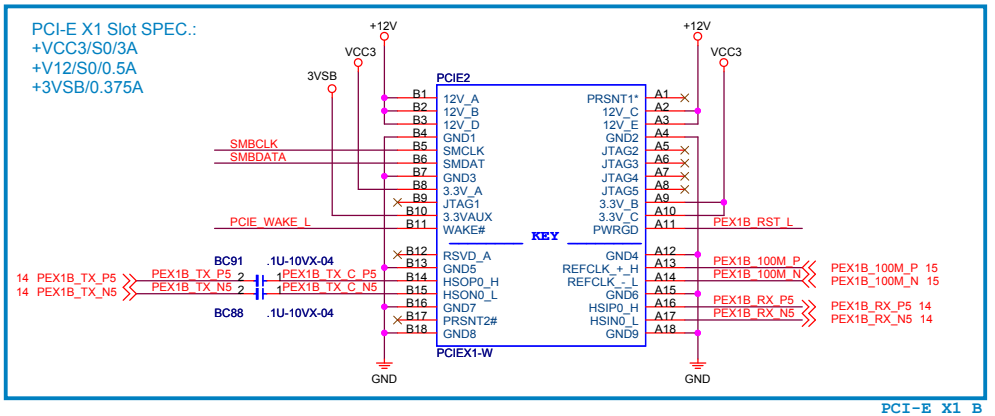

PCH1J
U1CPT
10 of 12
PCH1I
9 of 12
1.05V
MAX 6.2A
1.05V
MAX 6.2A
1.05V/1.00V
MAX TBD
1.05V
MAX 1.8A
100mA up
100mA up
MAX <1mA
MAX 123mA
MAX 203mA
3.3V
MAX 16mA
100mA up
100mA up
100mA up
USB Classic Filter
For platform not supporting
deep sleep connect directly to +3VSB.
AMT Only
Elitegroup Computer Systems
PCH - PWR
H61H2-A
Wednesday, January 26, 2011

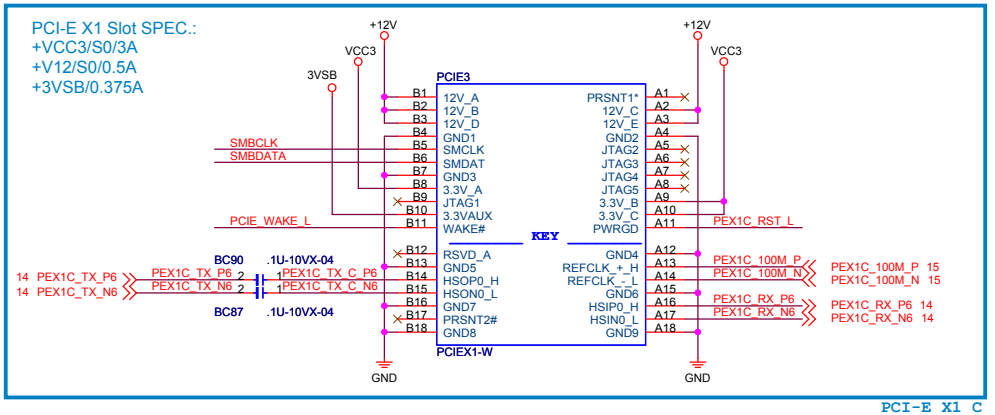


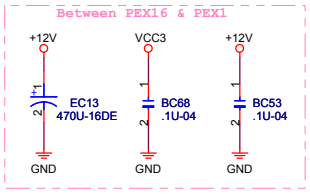
Elitegroup Computer Systems			
Title: PCH - GND			
Size: Custom	Document Number: H61H2-A		Rev: 1.0
Date: Wednesday, January 26, 2011	Sheet 19 of 31		

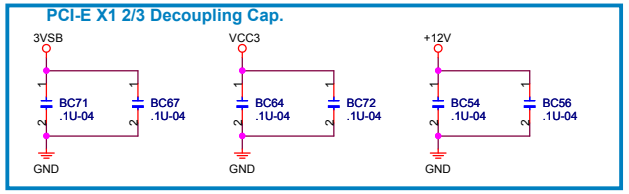












Elitegroup Computer Systems

Title: Slot - PCI-EX16/PCI-EX1

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Custom	H61H2-A	1.0

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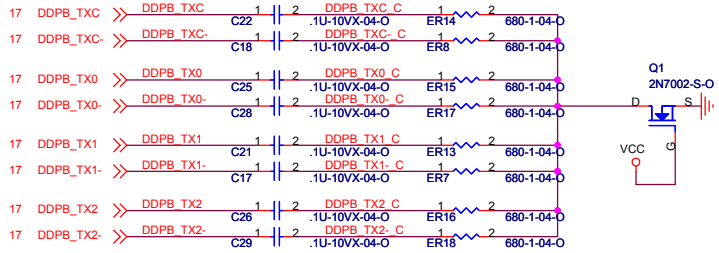

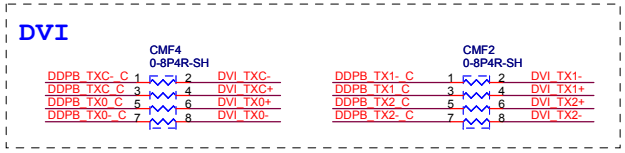

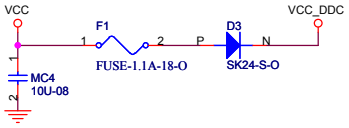

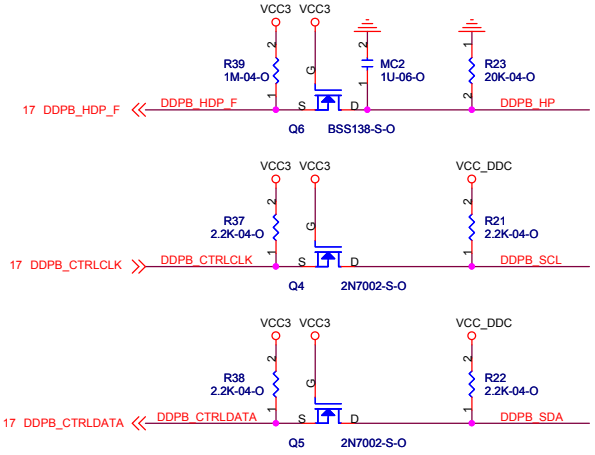

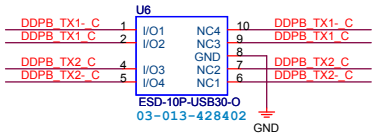

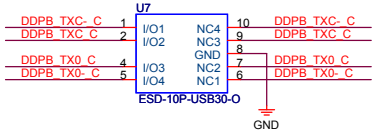

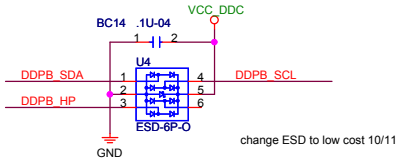

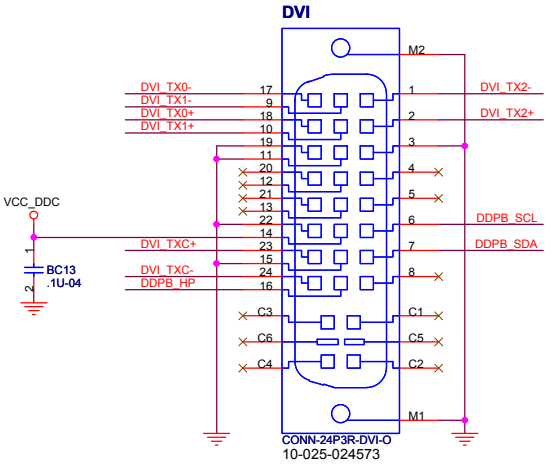

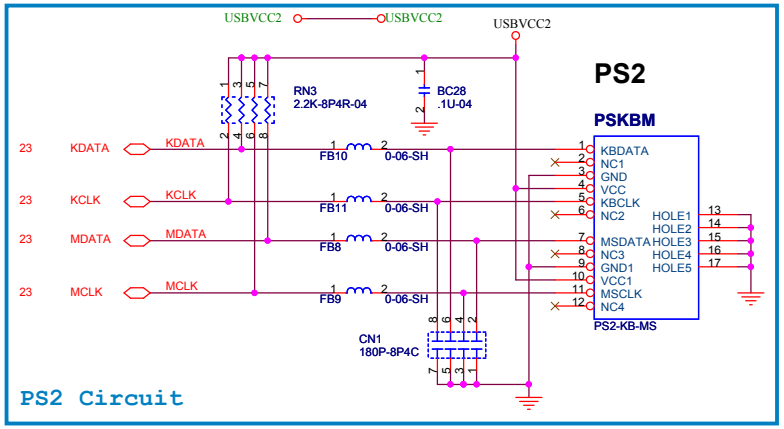

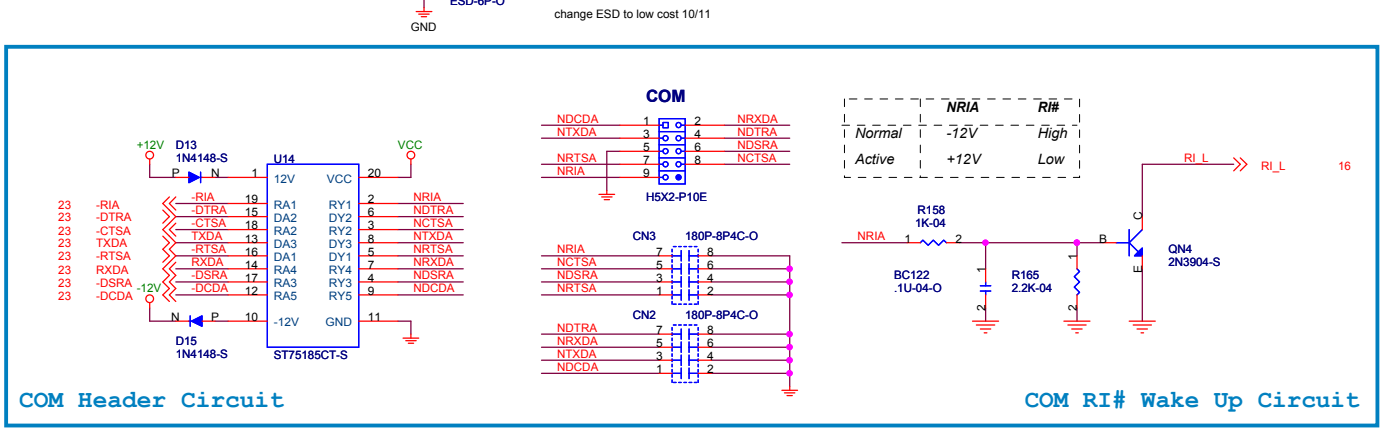

Elitegroup Computer Systems

Title: DVI&HDMI CONN&COM&PS2

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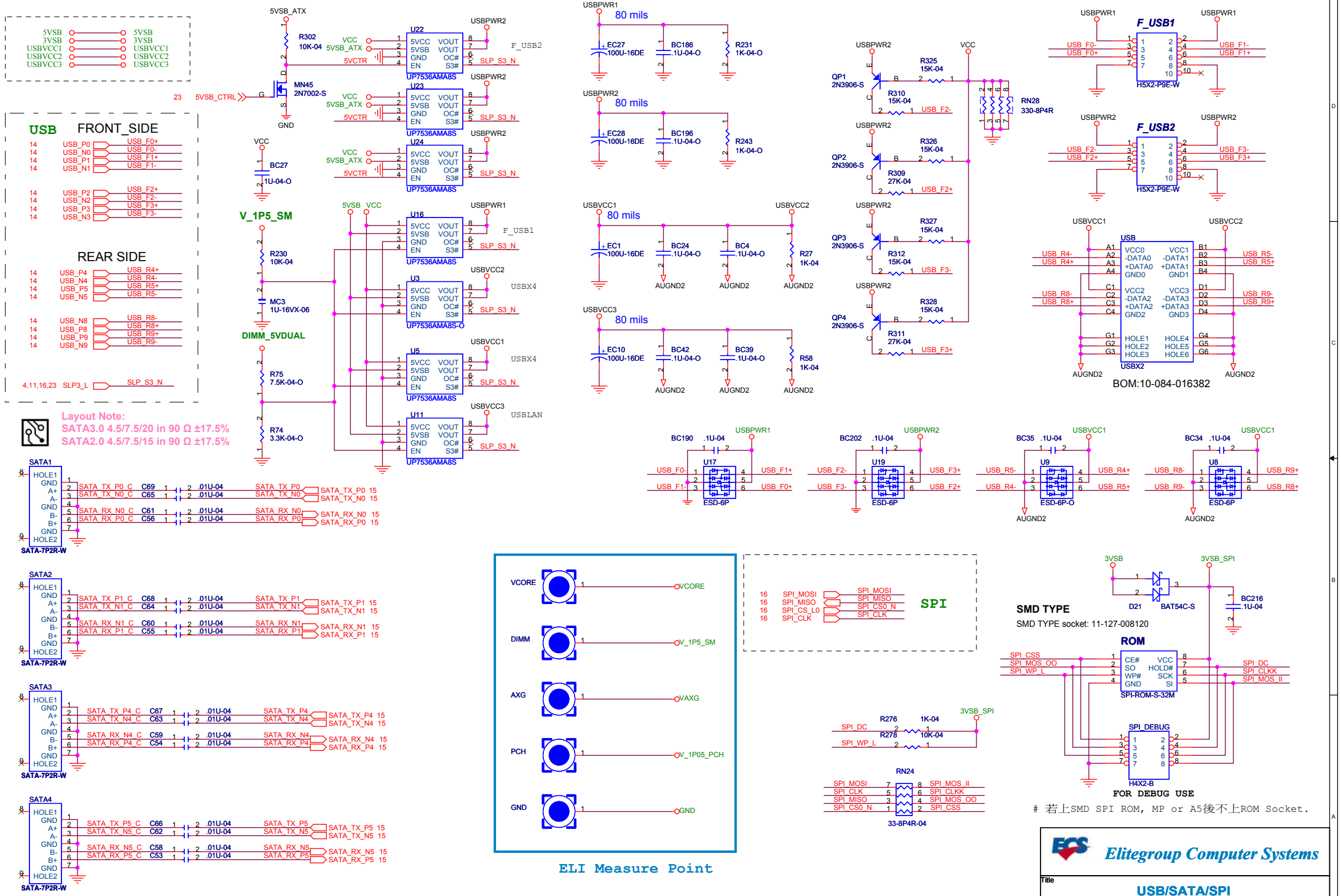
5VSB
3VSB
USBVCC1
USBVCC2
USBVCC3
USB
FRONT_SIDE
REAR SIDE
USB_P0
USB_N0
USB_P1
USB_N1
USB_P2
USB_N2
USB_P3
USB_N3
USB_P4
USB_N4
USB_P5
USB_N5
USB_P8
USB_N8
USB_P9
USB_N9
SLP_S3_L
SLP_S3_N
5VSB_ATX
R302
10K-04
MN45
2N7002-S
5VSB_CTRL
GND
VCC
BC27
1U-04-O
V_1P5_SM
R230
10K-04
MC3
1U-16VX-06
DIMM_5VDUAL
R75
7.5K-04-O
R74
3.3K-04-O
U22
U23
U24
U16
U3
U5
U11
UP7536AMA8S
UP7536AMA8S-O
F_USB2
F_USB1
USBX4
USBLAN
USBPWR1
USBPWR2
USBVCC1
USBVCC2
USBVCC3
80 mils
EC27
100U-16DE
BC186
.1U-04-O
R231
1K-04-O
EC28
BC196
R243
EC1
BC24
BC4
R27
EC10
BC42
BC39
R58
AUGND2
QP1
QP2
QP3
QP4
2N3906-S
R325
15K-04
R310
R326
R309
R327
R312
R328
R311
USB_F2-
USB_F2+
USB_F3-
USB_F3+
RN28
330-8P4R
F_USB1
F_USB2
H5X2-P9E-W
USB
VCC0
-DATA0
+DATA0
GND0
VCC1
-DATA1
+DATA1
GND1
VCC2
-DATA2
+DATA2
GND2
VCC3
-DATA3
+DATA3
GND3
HOLE1
HOLE2
HOLE3
HOLE4
HOLE5
HOLE6
USBX2
USB_R4-
USB_R4+
USB_R5-
USB_R5+
USB_R8-
USB_R8+
USB_R9-
USB_R9+
BOM:10-084-016382
Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%
SATA1
SATA2
SATA3
SATA4
SATA-7P2R-W
HOLE1
HOLE2
SATA_TX_P0_C
SATA_TX_N0_C
SATA_RX_N0_C
SATA_RX_P0_C
SATA_TX_P1_C
SATA_TX_N1_C
SATA_RX_N1_C
SATA_RX_P1_C
SATA_TX_P4_C
SATA_TX_N4_C
SATA_RX_N4_C
SATA_RX_P4_C
SATA_TX_P5_C
SATA_TX_N5_C
SATA_RX_N5_C
SATA_RX_P5_C
.01U-04
SATA_TX_P0
SATA_TX_N0
SATA_RX_N0
SATA_RX_P0
SATA_TX_P1
SATA_TX_N1
SATA_RX_N1
SATA_RX_P1
SATA_TX_P4
SATA_TX_N4
SATA_RX_N4
SATA_RX_P4
SATA_TX_P5
SATA_TX_N5
SATA_RX_N5
SATA_RX_P5
VCORE
DIMM
AXG
PCH
GND
V_1P05_PCH
VAXG
ELI Measure Point
SPI
SPI_MOSI
SPI_MISO
SPI_CS0_N
SPI_CLK
SMD TYPE
SMD TYPE socket: 11-127-008120
ROM
SPI-ROM-S-32M
SPI_CSS
SPI_MOS_OO
SPI_WP_L
SPI_DC
SPI_CLKK
SPI_MOS_II
D21
BAT54C-S
BC216
.1U-04
3VSB
3VSB_SPI
R276
R278
10K-04
RN24
33-8P4R-04
SPI_DEBUG
H4X2-B
FOR DEBUG USE
若上SMD SPI ROM, MP or A5後不上ROM Socket.
BC190
BC202
BC35
BC34
U17
U19
U9
U8
ESD-6P
ESD-6P-O
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USB/SATA/SPI
Size
Custom
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External Connection

3VSB 3VSB
5VSB 5VSB
VCC3 VCC3
VBAT_IO_S VBAT_IO_S
VCC VCC
V_1P5_SM V_1P5_SM
V_CPUVTT V_CPUVTT
VCORE VCORE

LPC
16 LPC_PME_L — LPCPME_L
16 LPC_DRQ0_L — -LPC_DRQ0
16 LPC_FRAME_L — -LPC_FRAME
16 LPC_AD[0..3] — L_AD[0..3]

COM
21 -RTSA — -RTSA
21 -DSRA — -DSRA
21 TXDA — TXDA
21 RXDA — RXDA
21 -DTRA — -DTRA
21 -DCDA — -DCDA
21 -RI — -RI
21 -CTSA — -CTSA

PS/2
21 KCLK — KDATA
21 KDATA — MCLK
21 MCLK — MDATA
21 MDATA — PLTRST_L

RST
16 PCH_PLTRST_L — -PCI_RSTY
20 SIO_PCIRST1_L — -PCIE_RSTY
4,26,28 SIO_PCIRST2_L — PD0

LPT
13 PD0 — PD1
13 PD1 — PD2
13 PD2 — PD3
13 PD3 — PD4
13 PD4 — PD5
13 PD5 — PD6
13 PD6 — PD7
13 PD7 — ERR_L
13 ERR_L — BUSY
13 BUSY — PE
13 PE — SLCT
13 SLCT — ACK_L
13 ACK_L — SLIN_L
13 SLIN_L — PINIT_L
13 PINIT_L — AFD_L
13 AFD_L — STB_L
13 STB_L — SIO_PCLK
15 SIO33M — SIO_CLK48
15 SIO48M — G_LED1
13 G_LED1 — G_LED2
13 G_LED2 — H_SKTOCC_N
4,9 H_SKTOCC_L — PCH_THRM_L
15 THERMAL ALERT — SML1CLK
16 SMLK1_SIO_CLK — SML1DATA
16 SMLK1_SIO_DATA — PECI
4,15 PECI — CFAN_TAC1
13 CFAN_TAC1 — CFAN_PWM1
13 CFAN_PWM1 — -KB_RST
15 KBRST_L — A20GATE_L
15 A20GATE — SERIRQ
15 SER_IRQ — -3VSBSW
12 -3VSBSW — RSMRST_N
16 RSMRST_L — -PANSHW
13 FP_PWRBTN_L — -PWRON
16 SIO_PWRBTN_L — -SLP3
4,11,16,22 SLP3_L — SLP4_L
16 SLP4_L — -ATX_PSON_SIO
13 PSON_L — ATX_PWRGD
13 ATX_PWRGD — PWROK
15,16 PWRGD — DDR_GP64
12 DDR_GP64 — DDR_GP63
12 DDR_GP63 — 5VSB_CTRL
22 5VSB_CTRL

SIO_PCIRST1_L : PCIE1、PCIE2
SIO_PCIRST2_L : CPU、LAN、PCI
SIO_PCIRST3_L : NA

IT8728F-CX

01-230-728092

IO
3VSB_IO

-RTSA -DSRA TXDA RXDA -DTRA -DCDA -RI
128 127 126 125 124 123 122 121 120 119 118 117 116 115 114 113 112 111 110 109 108 107 106 105 104 103
RI1# DCD1# DTR1#/JP4 SIN1 SOUT1/JP3 DSR1# RTS1# SML1CLK SML1DATA FAN_CTL4/VID_TURBO GP85/VDDA_EN GP66/VLDT_EN GP67/GATEA20 GND PD7/GP77/BUSSD2 PD6/GP76/BUSSD1 PD5/GP75/BUSSD0 PD4/GP74/BUSSI2 PD3/GP73/BUSSI1 PD2/GP72/BUSSI0 PD1/GP71 PD0/GP70 STB#/GP87/SMBC_M AFD#/GP86/SMBC_R ERR# INIT#/GP85/SMBD_M SLIN#/GP84/SMBD_R ACK#/GP83

-CTSA 1 CTS1#
2 FAN_CTL5/CIRRX2/GP16
PLTRST_L 3 PCIRSTIN#/CIRTX2/GP15
4 3VSB
DDR_GP64 5 VCORE_EN/GP64
DDR_GP63 6 VCORE_GOOD/GP63
CFAN_TAC1 7 FAN_TAC1
CFAN_PWM1 8 FAN_CTL1
9 FAN_TAC2/GP52
10 FAN_CTL2/GP51
PCH_THRM_L 11 FAN_TAC3/GP37
12 FAN_CTL3/GP36
GP35 13 GP35
GP34 14 GP34
5VSB_CTRL 15 GNDD
16 5VSB_CTRL
17 5VAUX_SW
ATX_PWRGD 18 PWRGD2_50ms
19 ATXPG/GP30
20 SIN2/GP27
21 SOUT2/GP26
22 FAN_TAC4/DSR2#/GP25
23 FAN_TAC5/RTS2#/GP24
G_LED2 24 GP23/SI
G_LED1 25 GP22/SCK
26 DCD2#/GP21
27 CTS2#/GP20
28 RI2#/GP17
-DTRB 29 DTR2#
-RESETCON 30 CE_N/RESETCON#/CIRTX
31 PECI_RQT/GP14
PWROK 32 PWRGD1_30ms
-PCI_RSTY 33 PCIRST1#/GP12
-PCIE_RSTY 34 PCIRST2#/GP11
35 3VSB
-LPCPD 36 VCORE
PLTRST_L 37 LRESET#
-LPC_DRQ0 38 LDRQ#/JP1

BUSY/GP82 102 BUSY
PE/GP81 101 PE
SLCT/GP80 100 SLCT
99 AVCC3
VIN0 98 HM_VIN0
VIN1 97 HM_VIN1
VIN2 96 HM_VIN2
VIN3/ATXPG 95 HM_VIN3
VIN4/VLDT_12 94 HM_VIN4
VIN5/VDDA_25 93 HM_VIN5
VIN6/VDIMM_STR 92 HM_VIN6
VREF 91 HM_VREF
TMPIN1 90 TMP_SYS
TMPIN2 89
TMPIN3 88
TS_D- 87
GNDA 86
RSMRST#/CIRRX1/GP55 85 RSMRST_N
PCIRST3#/GP10/VDIMM_STR_EN 84 SIO_PCIRST3_L
MCLK/GP56 83 MCLK
MDAT/GP57 82 MDATA
KCLK/GP60 81 KCLK
KDAT/GP61 80 KDATA
3VSBSW#/GP40 79 -3VSBSW
PWRGD3_150ms 78 PWRGD3
SUSC#/GP53 77 SLP4_L
PSON#/GP42 76 -ATX_PSON_SIO
PANSHW#/GP43 75 -PANSHW
74 GNDD
PME#/GP54 73 LPCPME_L
PWRON#/GP44 72 -PWRON
SUSS# 71 -SLP3
SYS_3VSB 70
VBAT 69
COPEN# 68 -CASE_OPEN
3VSB 67
GP47 66 GP47
DSKCHG# 65

SERIRQ 39 LFRAME# 40 LAD0 41 LAD1 42 LAD2 43 LAD3 44 KRST#/GP62 45 GA20/JP5 46 PCICLK 47 SOJGP50 48 GND 49 VCC 50 DENSEL# 51 MTRA# 52 SST/AMDTSI_D/PECI_AVA/MTRB# 53 DRVA# 54 PECI/SBTSI_C/DRVB# 55 WDATA# 56 SMBC_R2/DIR# 57 SMBC_M2/STEP# 58 SMBD_R2/HDSEL# 59 SMBD_M2/WGATE# 60 RDATA# 61 TRK0# 62 INDEX# 63 WPT# 64

SERIRQ
-LPC_FRAME
L_AD0
L_AD1
L_AD2
L_AD3
-KB_RST
A20GATE_L
SIO_PCLK
SIO_CLK48
PECI

VCC3 — R67 0-04-O — BC46 .022U-04
RTCVCC — CLOSE TO PIN69 — MC7 1U-06
VCC3 — CLOSE TO PIN99 — BC1 .1U-04, MC1 1U-06-O
3VSB_IO — BC5 .1U-04, BC44 .1U-04
3VSB_IO — MC8 1U-06, MC9 10U-08, MC11 10U-08 — CLOSE TO PIN67

VCC3 — R49 100-04-O — MN1 2N7002-S-O — -ATX_PSON_SIO
VCC3 — BC22 1U-06 — FB5 0-06-SH — HM_AGND — R26 0-04 — RSMRST_N
VCC3 — R46 0-04 — PWROK — 5VSB_ATX
3VSB_IO — R48 4.7K-04, R53 4.7K-04 — -PANSHW
VBAT_IO — 3VSB_IO
-LPC_DRQ0 R68 1K-04-O
JP3 -DTRA, JP2 TXDA, JP4 -RTSA, JP5 A20GATE_L R66 1K-04, JP6 -DTRB R34 1K-04-O — RN1 1K-8P4R-04
RTCVCC — -CASE_OPEN R60 1M-04
VCC3 — -PCIE_RSTY R59 1K-04-O, -PCI_RSTY R54 1K-04, PWROK R35 1K-04, PWRGD3 R45 1K-04, -RESETCON R44 1K-04
3VSB — RN2 1K-8P4R-04 — MCLK, MDATA, KCLK, KDATA, SIO_PCIRST3_L R31 1K-04, LPCPME_L R55 1K-04, GP47 R65 100-04
CFAN_TAC1 C7 470P-04-O
SIO_CLK48 C43 470P-04-O

Thermal and Voltage Monitor

HM_AGND — RT1 NTC-10K-1-04 — C20 .1U-04
TMP_SYS — ER6 10K-1-04
HM_VREF — * HM_VIN1 for VAXG

HM_VIN0 R5 1K-04 — VCORE
HM_VIN1 ER2 10K-04 — VAXG
HM_VIN2 ER1 31.6K-1-04 — +12V
BC2 .1U-04, ER3 10K-1-04 — HM_AGND
HM_VIN3 R10 7.15K-1-04 — VCC
C5 .1U-04, R15 10K-1-04 — HM_AGND
HM_VIN4 R14 10K-04 — V_CPUVTT
HM_VIN5 R19 10K-04 — V_1P5_SM
HM_VIN6 ER5 10K-04 — V_1P05_PCH

* HM_VIN0 for VCORE
* HM_VIN5 for V_DIMM
* HM_VIN4 for CPUVTT
* HM_VIN6 for V_1P05_PCH

BIOS SELECTION

BIOS SELECTION HI: LO: — RJ17 10K-04(2-3) — VCC3 — GP35
BIOS SELECTION HI: LO: — RJ18 10K-04(2-3) — VCC3 — GP34

5VSB — R239 4.7K-04 — PWROK — Q9 2N7002-S — H_SKTOCC_N — MC71 1U-06-O

EuP

3VSB — R286 0-06-O — 3VSB_IO
5VSB — R297 0-08-O — 5VSB_ATX
Option

5VSB_ATX — R291 10K-04 — MC100 1U-06 — MC99 4.7U-08-O — MS1 — 5VSB
5VSB_CTRL — R292 10K-04
NPSO8-S

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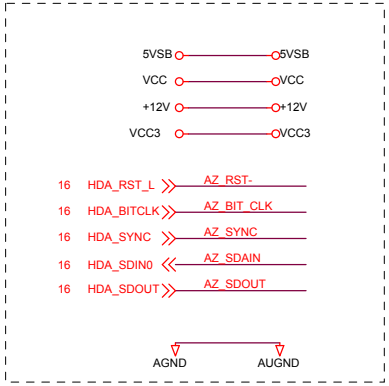
External Connection

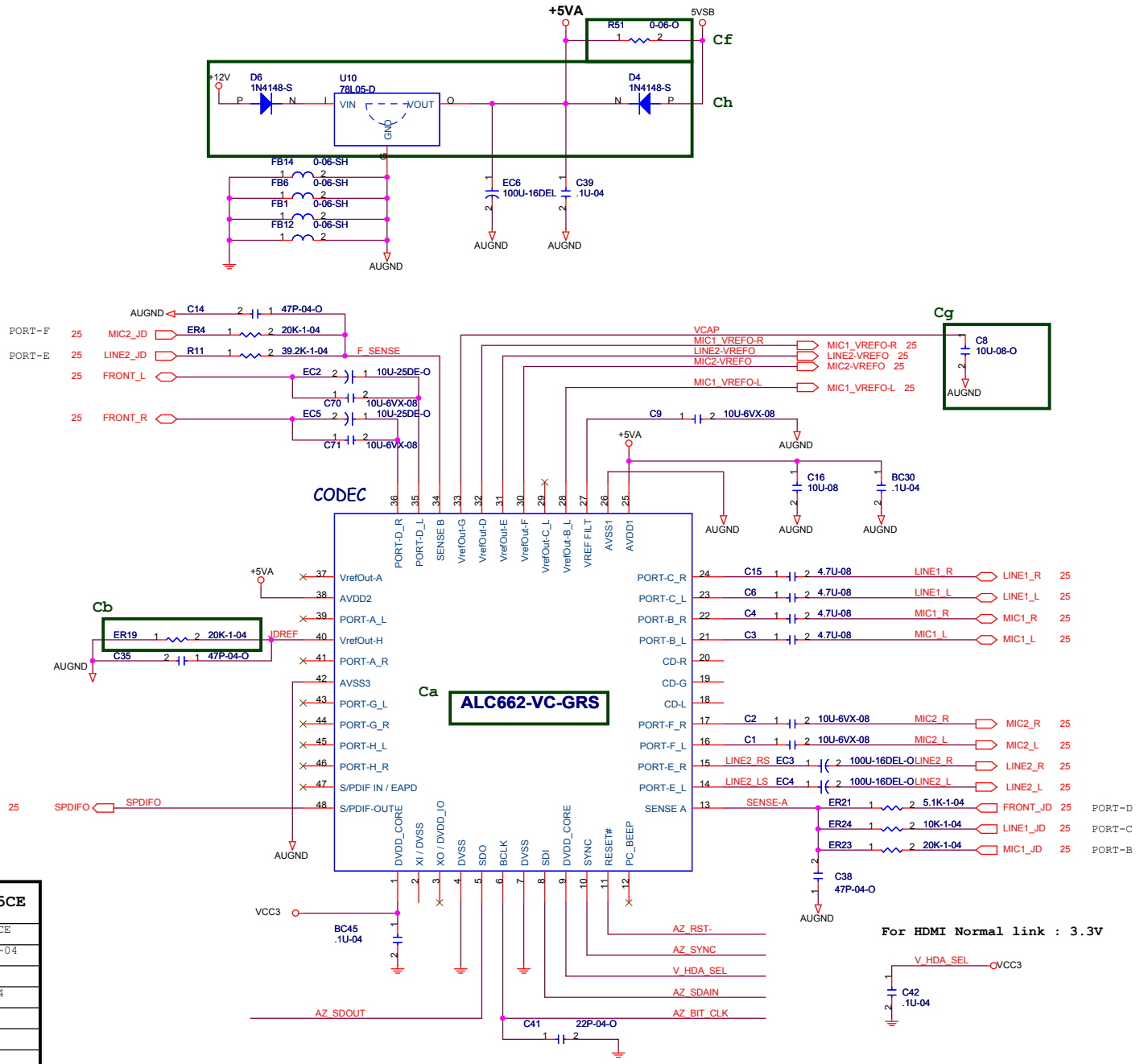


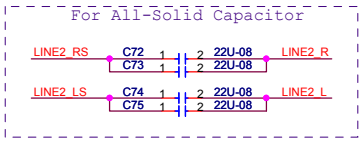
* VCC1.5 can remove for non-Intel G4X plateform

BOM Difference

Location	ALC662	VT1705	VT1705CE
Ca	ALC662-VC-GRS	VT1705	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	75-04	75-04
Cf	X	X	V
Cg	X	X	V
Ch	V	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.





Elitegroup Computer Systems

Title: AUDIO VT1705/ALC662 (CHIP)

Size: Custom | Document Number: H61H2-A | Rev: 1.0

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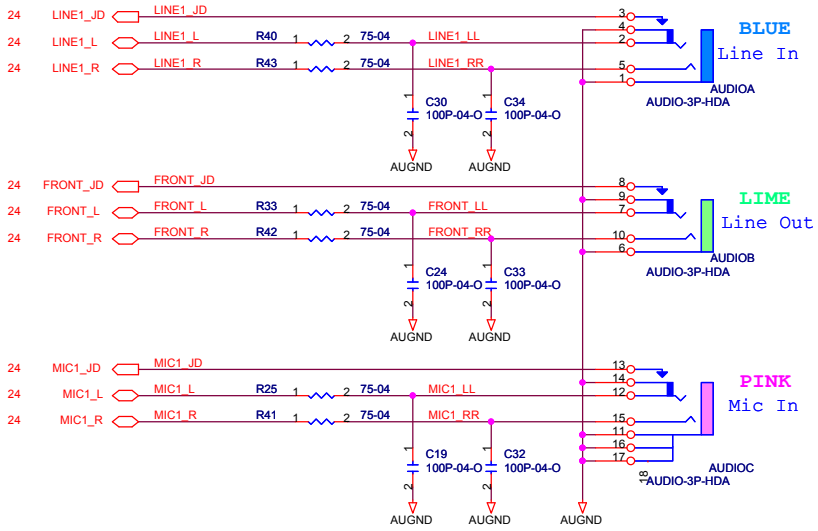
External Connection

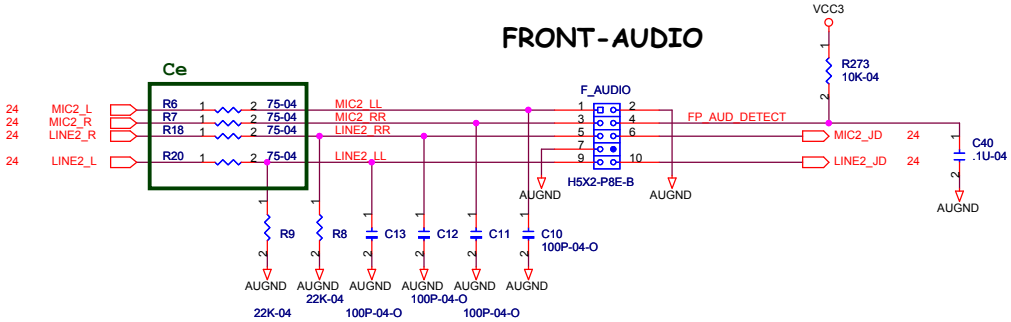
16 FP_AUD_DETECT <<< FP_AUD_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

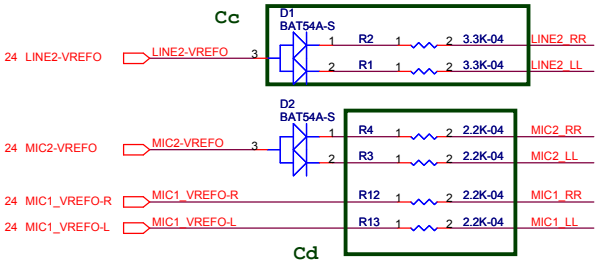
REAR-AUDIO Non re-tasking for rear panel



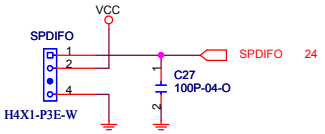
FRONT-AUDIO

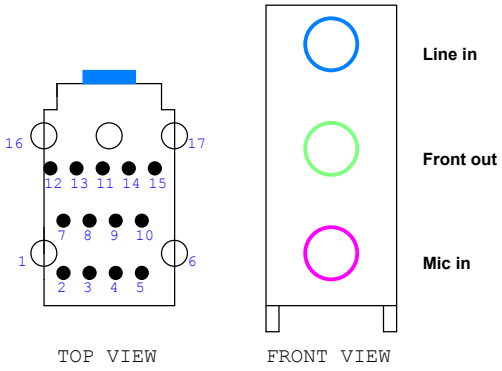


MIC Bias



SPDIF-OUT





Elitegroup Computer Systems		
Title: AUDIO VT1705/ALC662 (PANEL)		
Size: Custom	Document Number: H61H2-A	Rev: 1.0
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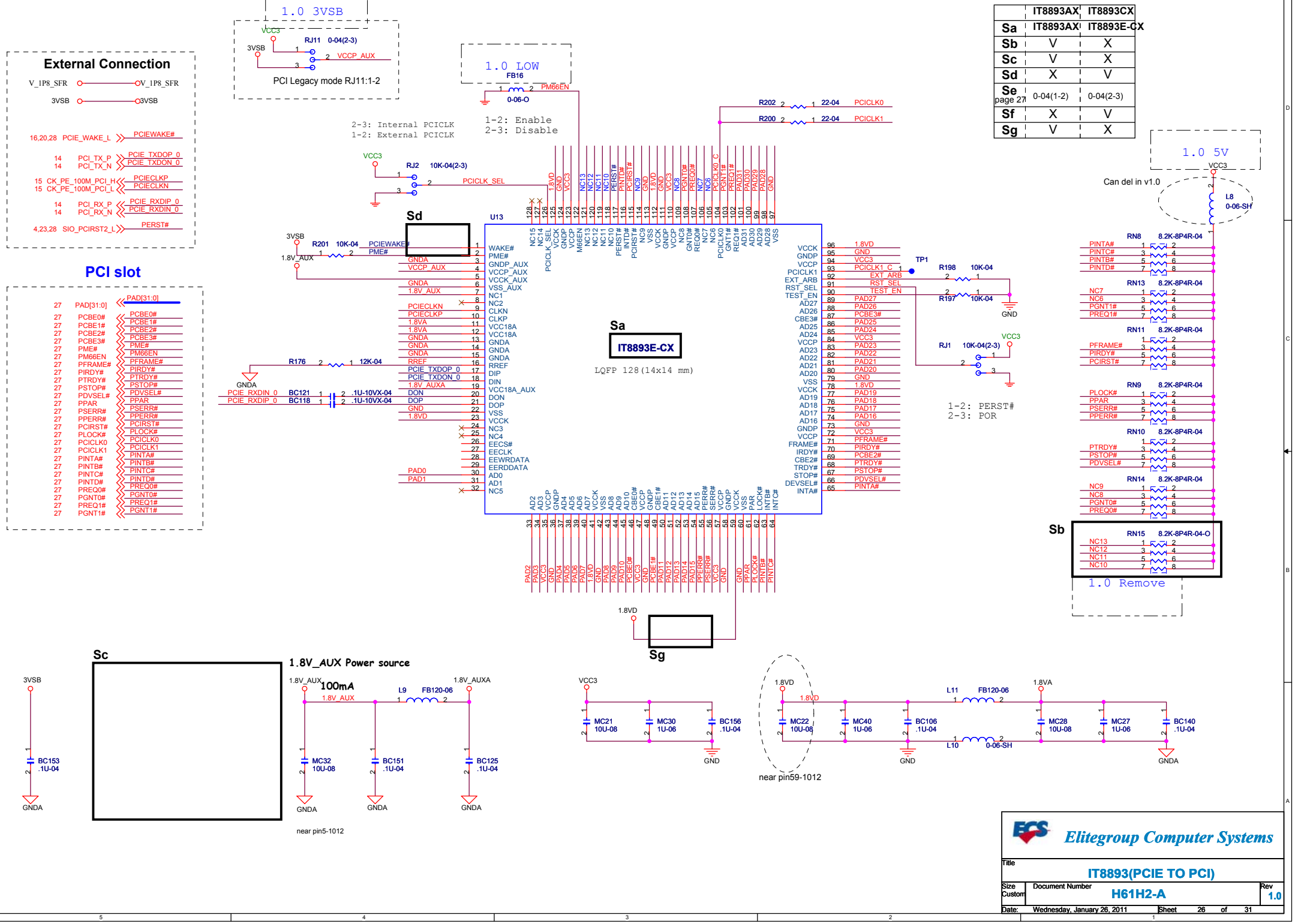

	IT8893AX	IT8893CX
Sa	IT8893AX	IT8893E-CX
Sb	V	X
Sc	V	X
Sd	X	V
Se	0-04(1-2)	0-04(2-3)
Sf	X	V
Sg	V	X

page 27

Elitegroup Computer Systems

Title: IT8893(PCIE TO PCI)

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External Connection

VCC — VCC
-12V — -12VD
+12V — +12VD

COMMON

PAD[31:0]
PCIRST#
PCBE0#
PCBE1#
PCBE2#
PCBE3#
PME#
PM66EN
PFRAME#
PIRDY#
PTRDY#
PSTOP#
PDVSEL#
PPAR
PSERR#
PPERR#
PCICLK0
PLOCK#
PINTA#
PINTB#
PINTC#
PINTD#
PREQ0#
PGNT0#
PCICLK1
PREQ1#
PGNT1#

PCHINTA_L
PCHINTB_L
PCHINTC_L
PCHINTD_L
PCH_PME_L

PCI CHIP

PCI1

PCI1 — PCI-W

3VSB
PCIRST#
PCICLK0
R136 22-04
PAD16

PCI2

PCI2 — PCI-W

3VSB
PCIRST#
PCICLK1
R113 22-04
PAD17

PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD

PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA

Se For page 26

R203 0-04-O
PME# — PCI_PME#

For ITE chipset auto power-on issue.

As document WW32 2010 Sandy Bridge and Cougar Point Based Platforms Field Message of the Week

Reserve for Intel PCI Legacy

R101 0-04
PCH_PME_L — PCI_PME#

RJ12 0-04(2-3)
PCHINTA_L — PCI_INTA#
PINTA#

RJ15 0-04(2-3)
PCHINTC_L — PCI_INTC#
PINTC#

RJ14 0-04(2-3)
PCHINTB_L — PCI_INTB#
PINTB#

RJ16 0-04(2-3)
PCHINTD_L — PCI_INTD#
PINTD#

VCC3
RN16 8.2K-8P4R-04
SMBCLK1
SMBDAT1
REQ64A-
ACK64A-
R214 8.2K-04
REQ64B-
R215 8.2K-04
ACK64B-

BC80 10P-04-O
PCICLK1
BC82 10P-04-O
PCICLK0
BC79 10P-04-O
PCIRST#
GND

07/20

VCC3
EC12 560U-6.3D-OS
BC131 .1U-04
BC105 .1U-04
BC155 .1U-04-O
GND

VCC
EC11 560U-6.3D-OS
BC175 .1U-04-O
BC52 .1U-04-O
BC31 .1U-04-O
GND

Elitegroup Computer Systems

Title: Slot - PCI1 & PCI2

Size	Document Number	Rev
Custom	H61H2-A	1.0

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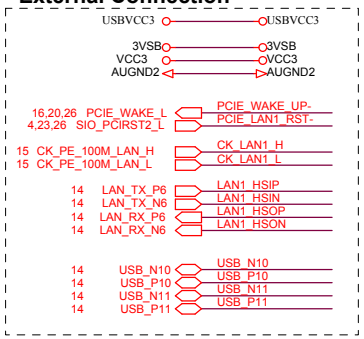
External Connection



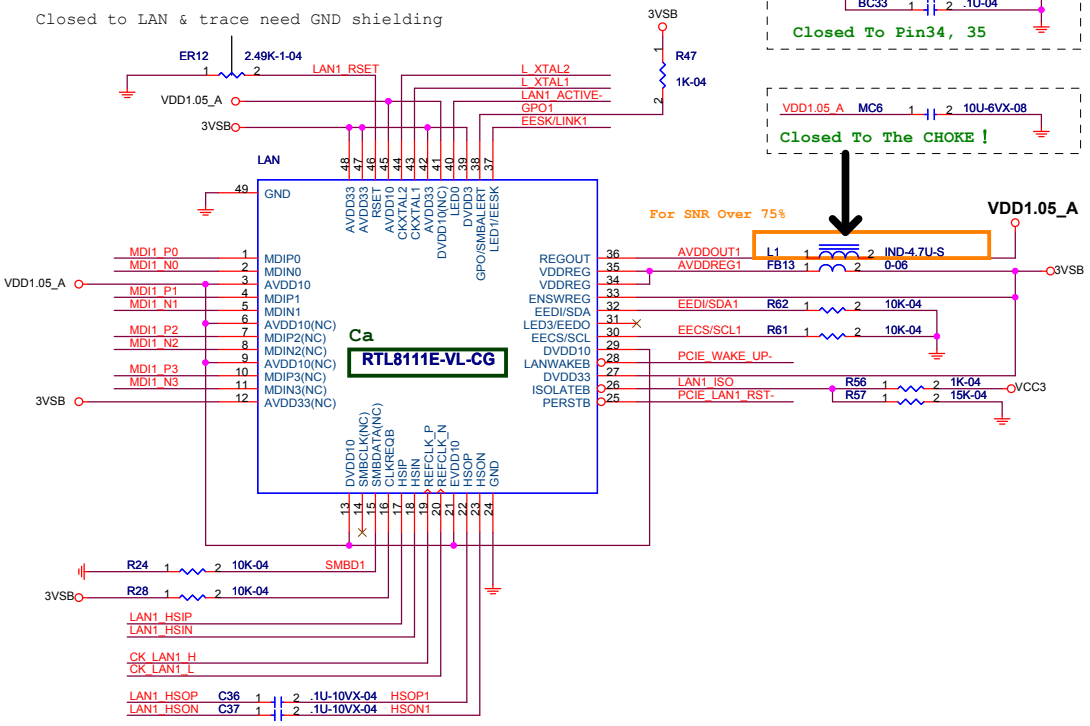
新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

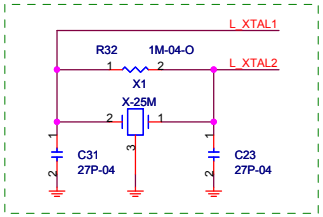
LAN_HSIP/N請接到SB的PCIE TX端

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

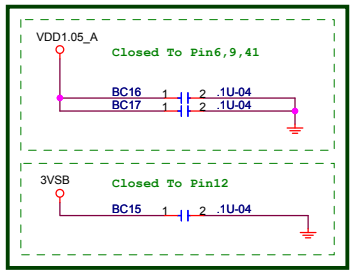
Closed to LAN & trace need GND shielding

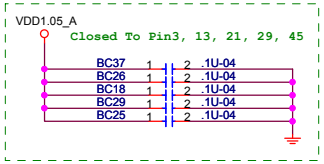


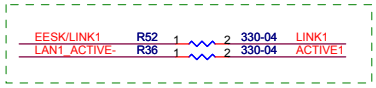
For SNR Over 75%

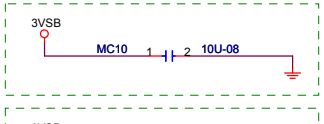


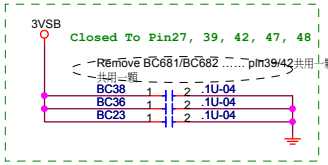
Cb

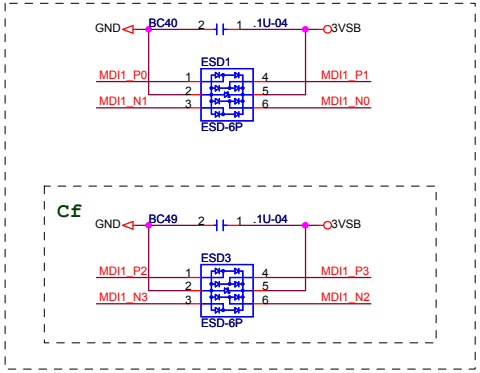


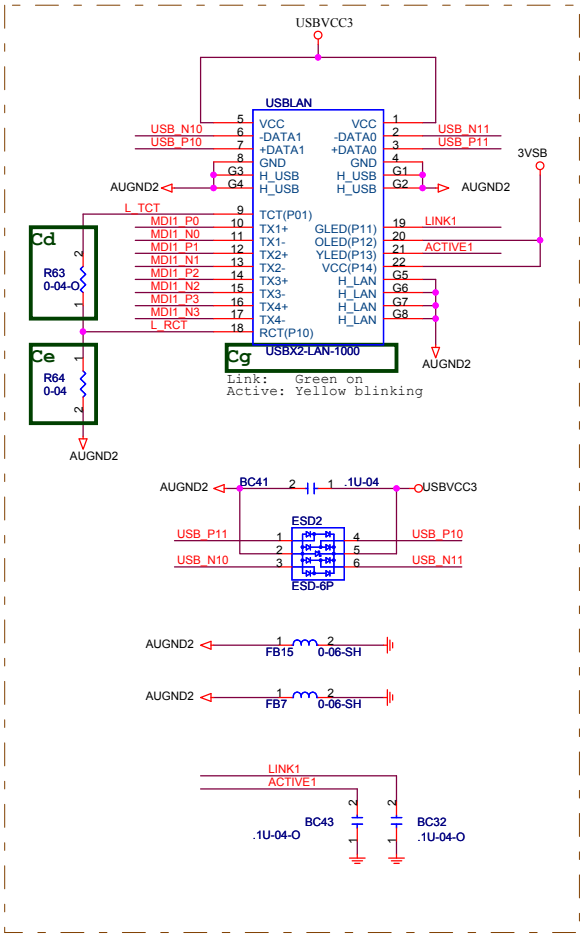












BOM Difference

	RTL8111E-VL-CG 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-VB-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cf	V	X
Cg	USBX2-LAN-1000	USBX2-LAN-100

Elitegroup Computer Systems

Title: RTL8111E / RTL8105E

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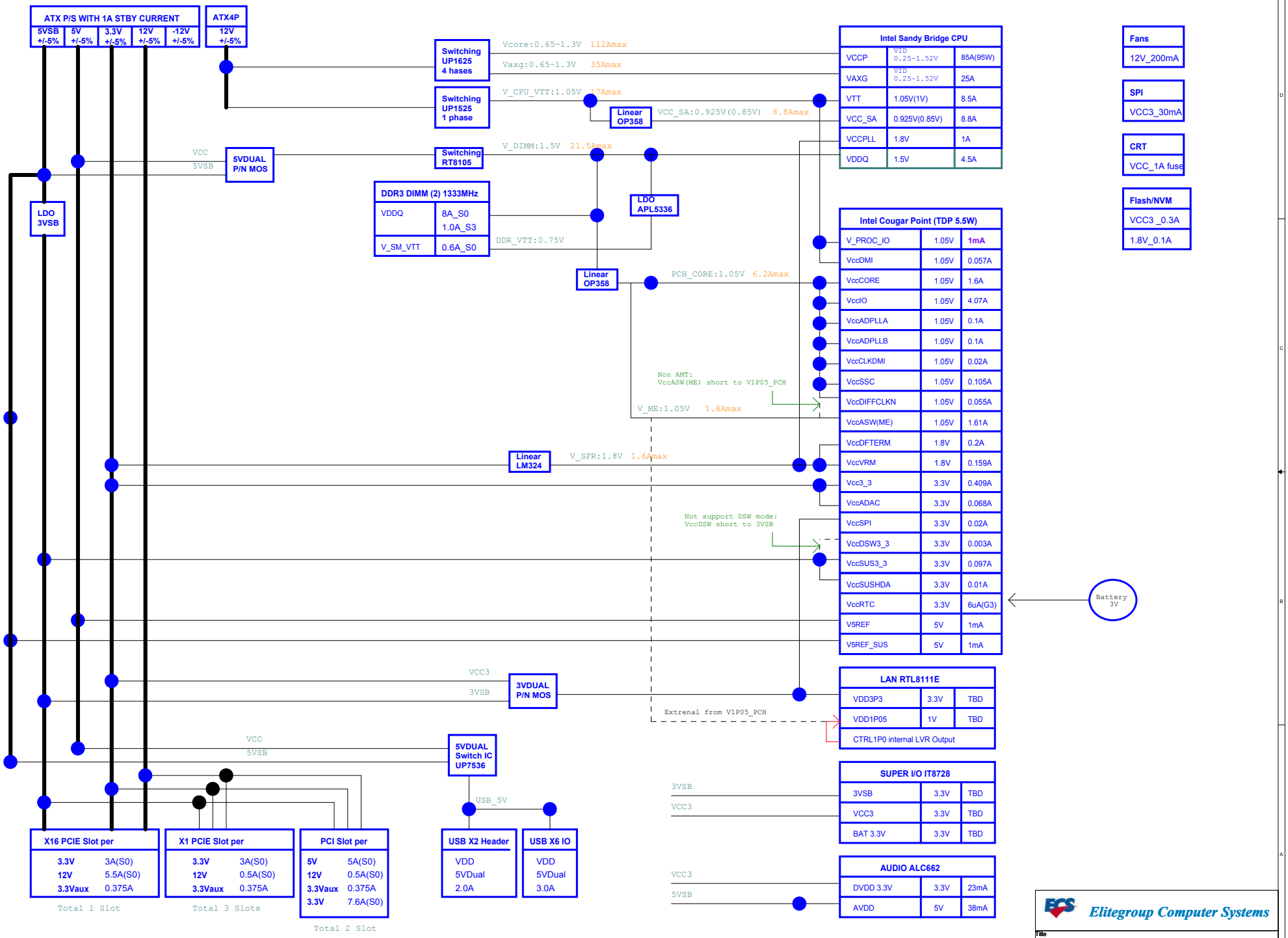
ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
Switching UP1625 4 hases
Vcore:0.65~1.3V 112Amax
Vaxg:0.65~1.3V 35Amax
Switching UP1525 1 phase
V_CPU_VTT:1.05V 17Amax
Linear OP358
VCC_SA:0.925V(0.85V) 8.8Amax
Intel Sandy Bridge CPU
VCCP VID 0.25~1.52V 85A(95W)
VAXG VID 0.25~1.52V 25A
VTT 1.05V(1V) 8.5A
VCC_SA 0.925V(0.85V) 8.8A
VCCPLL 1.8V 1A
VDDQ 1.5V 4.5A
Fans
12V_200mA
SPI
VCC3_30mA
CRT
VCC_1A fuse
Flash/NVM
VCC3 _0.3A
1.8V_0.1A
VCC
5VSB
5VDUAL P/N MOS
Switching RT8105
V_DIMM:1.5V 21.5Amax
LDO 3VSB
DDR3 DIMM (2) 1333MHz
VDDQ 8A_S0 1.0A_S3
V_SM_VTT 0.6A_S0
LDO APL5336
DDR_VTT:0.75V
Linear OP358
PCH_CORE:1.05V 6.2Amax
Intel Cougar Point (TDP 5.5W)
V_PROC_IO 1.05V 1mA
VccDMI 1.05V 0.057A
VccCORE 1.05V 1.6A
VccIO 1.05V 4.07A
VccADPLLA 1.05V 0.1A
VccADPLLB 1.05V 0.1A
VccCLKDMI 1.05V 0.02A
VccSSC 1.05V 0.105A
VccDIFFCLKN 1.05V 0.055A
VccASW(ME) 1.05V 1.61A
VccDFTERM 1.8V 0.2A
VccVRM 1.8V 0.159A
Vcc3_3 3.3V 0.409A
VccADAC 3.3V 0.068A
VccSPI 3.3V 0.02A
VccDSW3_3 3.3V 0.003A
VccSUS3_3 3.3V 0.097A
VccSUSHDA 3.3V 0.01A
VccRTC 3.3V 6uA(G3)
V5REF 5V 1mA
V5REF_SUS 5V 1mA
Non AMT:
VccASW(ME) short to V1P05_PCH
V_ME:1.05V 1.8Amax
Linear LM324
V_SFR:1.8V 1.6Amax
Not support DSW mode:
VccDSW short to 3VSB
Battery 3V
VCC3
3VSB
3VDUAL P/N MOS
Extrenal from V1P05_PCH
LAN RTL8111E
VDD3P3 3.3V TBD
VDD1P05 1V TBD
CTRL1P0 internal LVR Output
VCC
5VSB
5VDUAL Switch IC UP7536
USB_5V
3VSB
VCC3
SUPER I/O IT8728
3VSB 3.3V TBD
VCC3 3.3V TBD
BAT 3.3V 3.3V TBD
VCC3
5VSB
AUDIO ALC662
DVDD 3.3V 3.3V 23mA
AVDD 5V 38mA
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 3 Slots
PCI Slot per
5V 5A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
3.3V 7.6A(S0)
Total 2 Slot
USB X2 Header
VDD
5VDual
2.0A
USB X6 IO
VDD
5VDual
3.0A
Elitegroup Computer Systems
Title
Power Delivery
Size C
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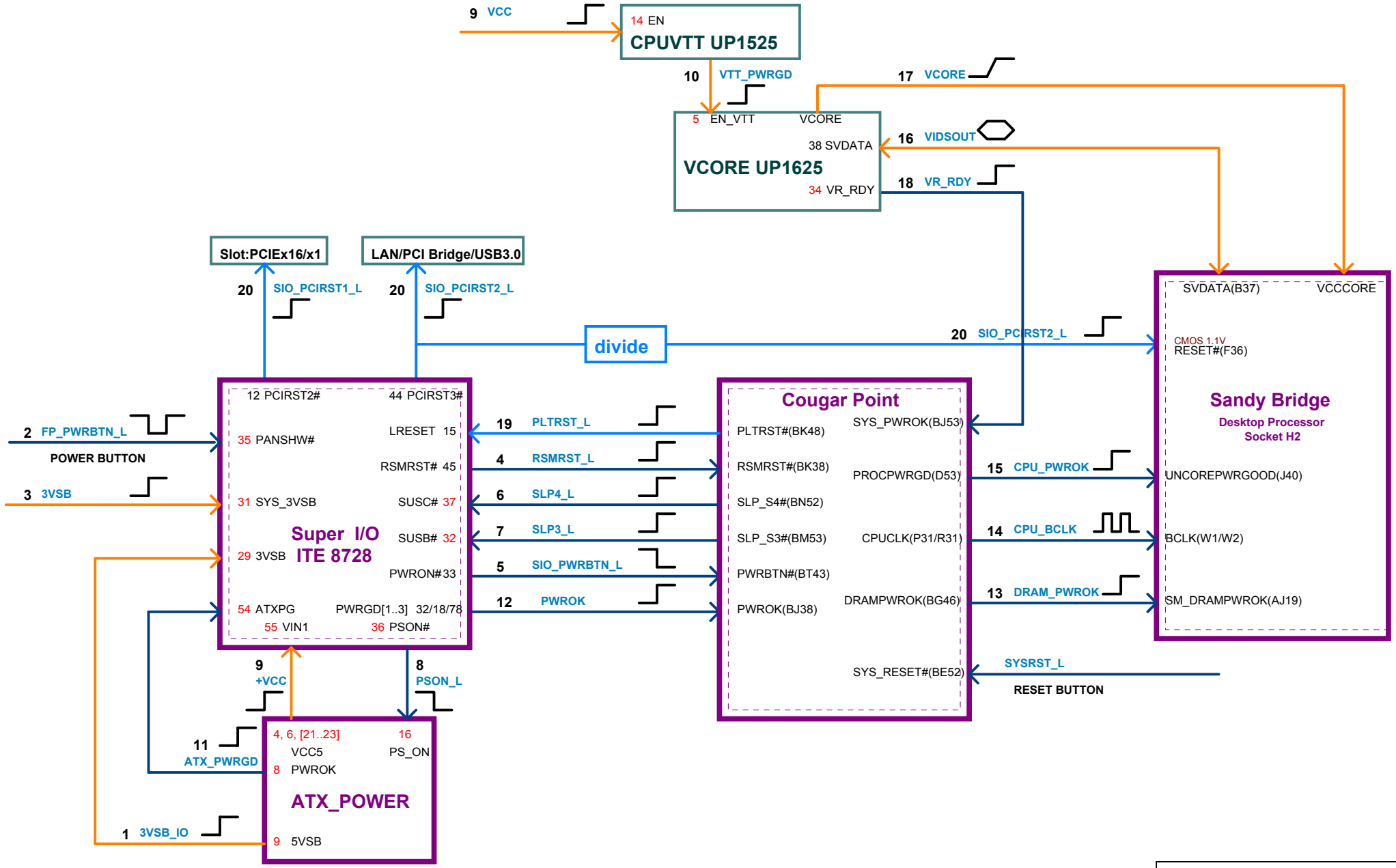

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Title: Power Sequence, Reset Diagram

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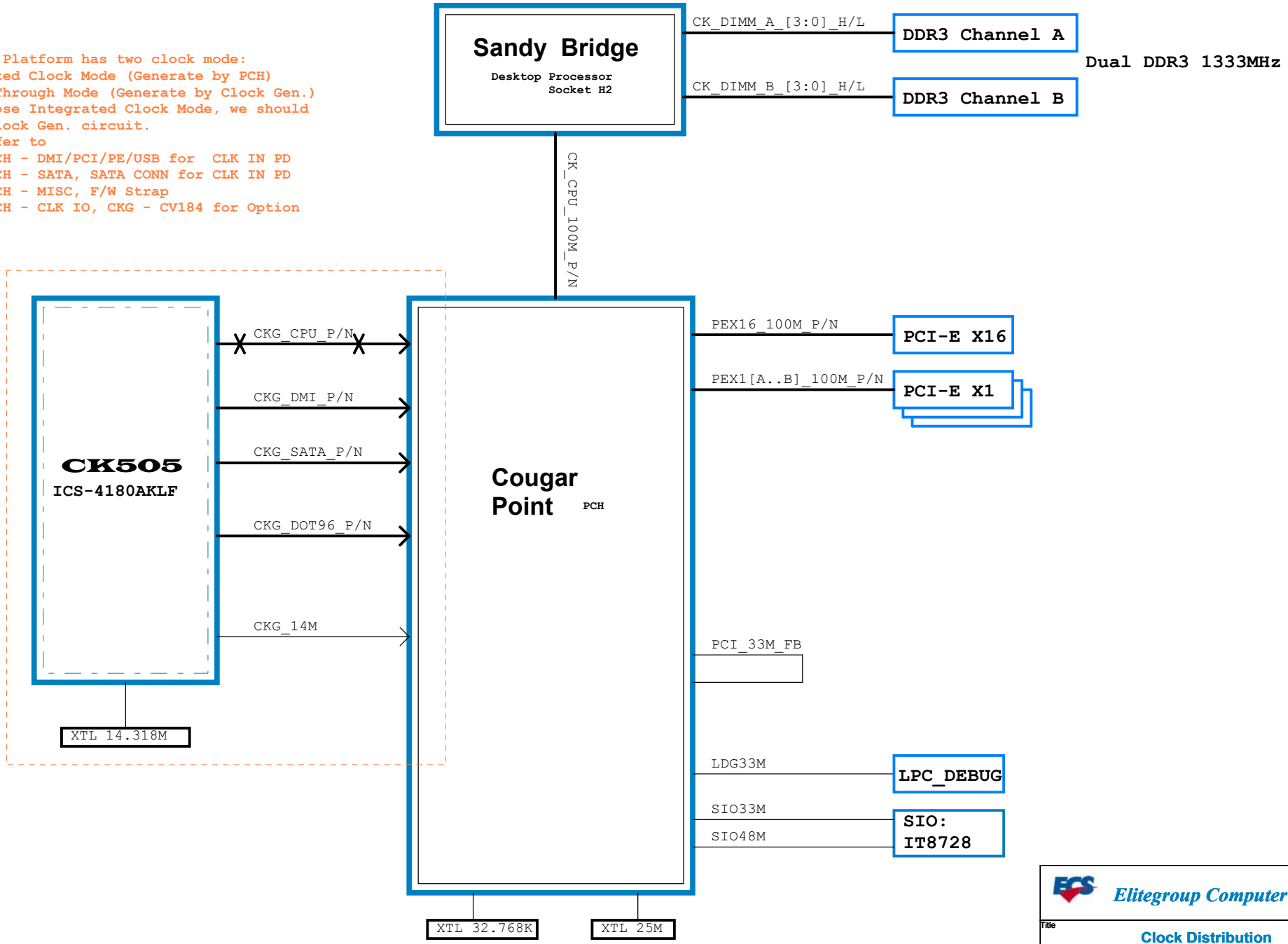
NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option



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Title	Clock Distribution	
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