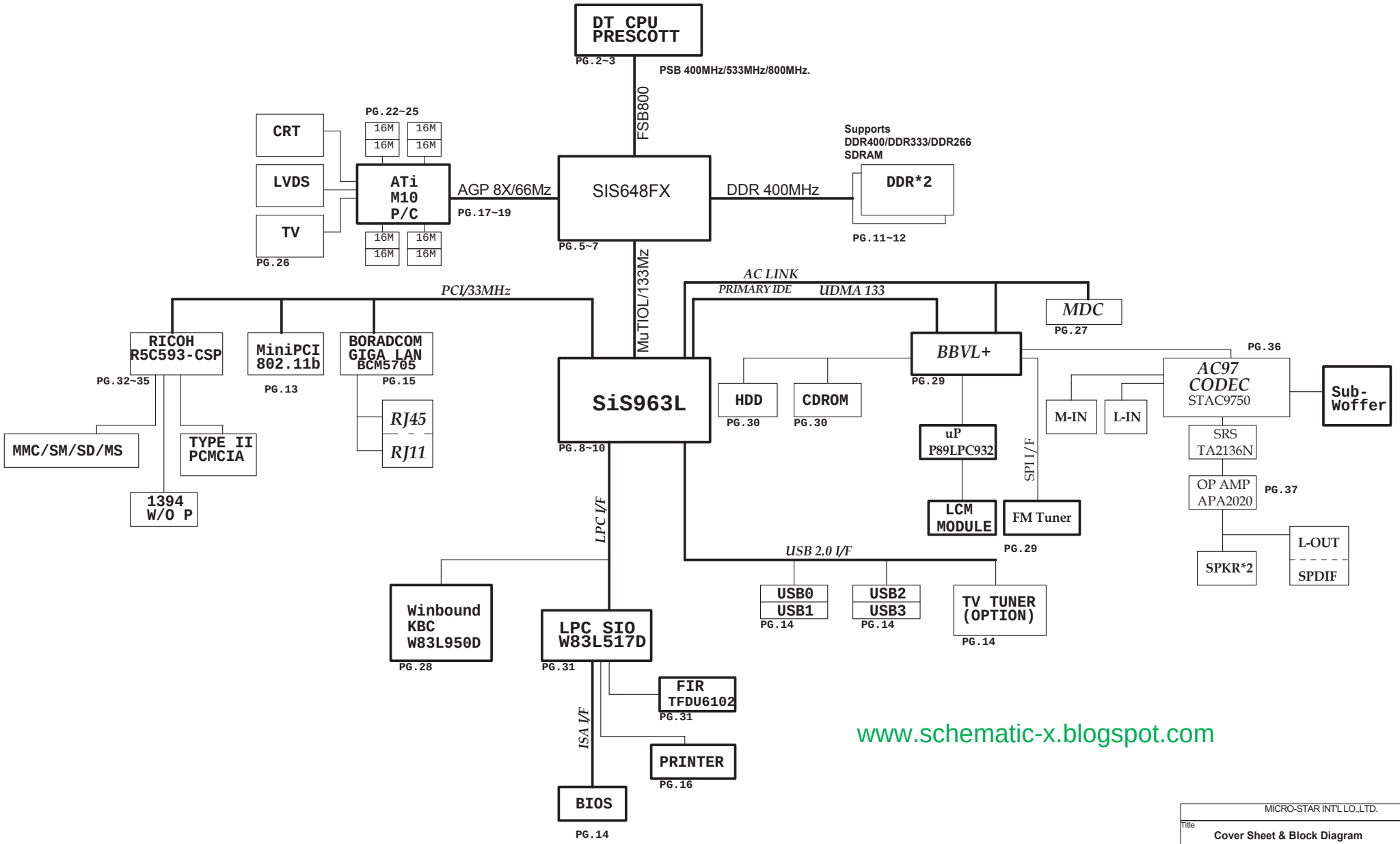
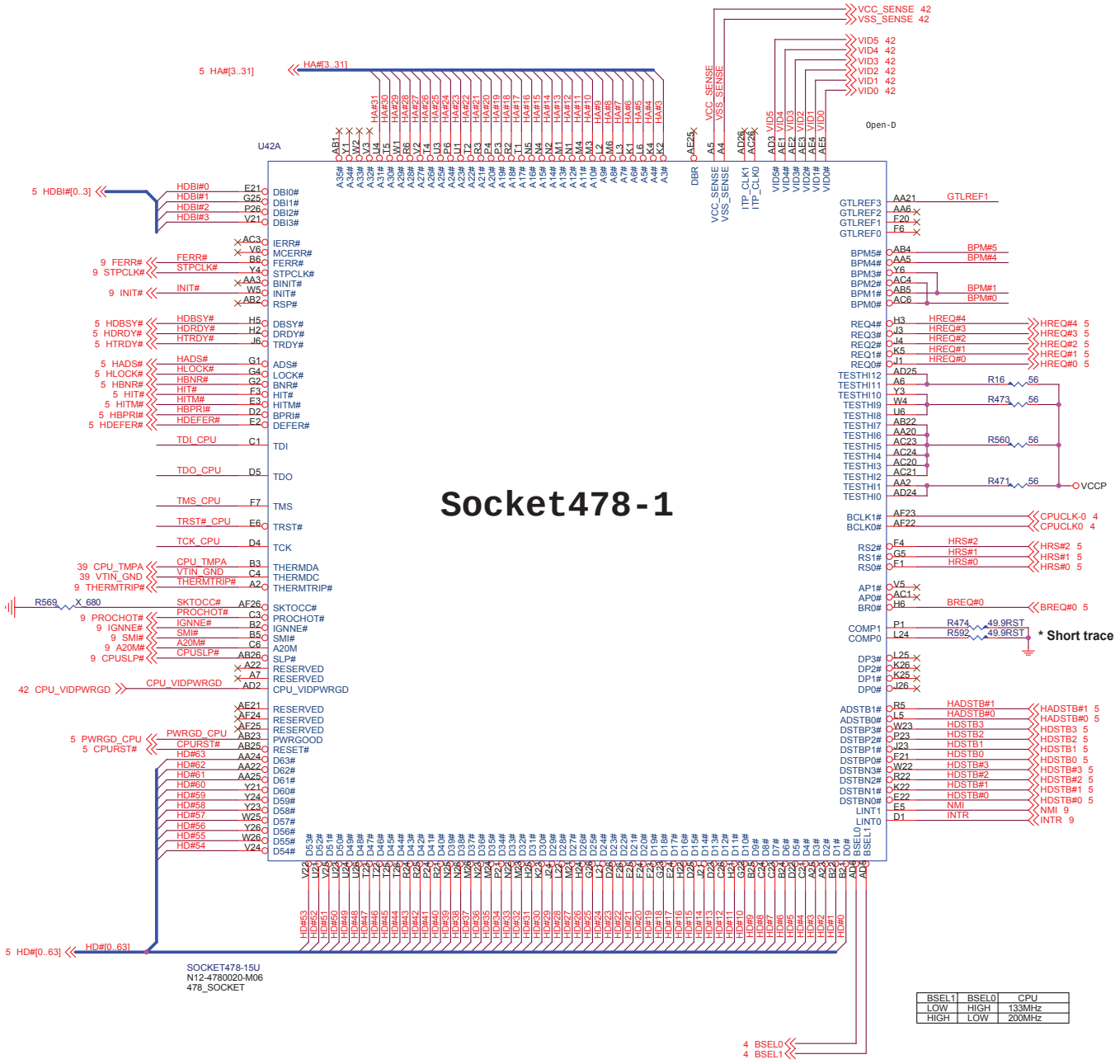
MS-1002 Ver:0C

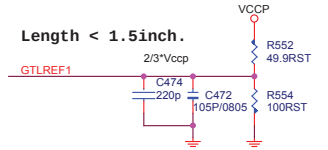
DTR MS-1002 System Block Diagram



MICRO-STAR INT'L LO.,LTD.		
Title: Cover Sheet & Block Diagram		
Size: Custom	Document Number: MS-1002 FROM MS-6785	Rev: 0C
Date: Wednesday, March 03, 2004	Sheet 1 of 44	



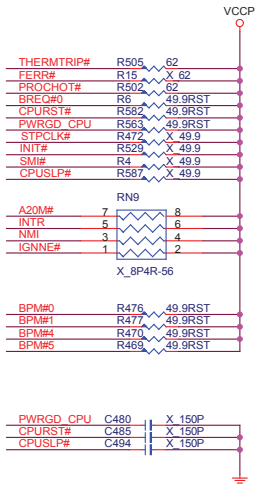
CPU GTL REFERNCE VOLTAGE BLOCK



Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

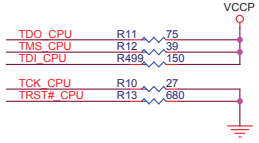
CPU STRAPPING RESISTORS

CLOSED TO SOCKET478



CPU ITP BLOCK

CLOSED TO SOCKET478




```
FERR#, STPCLK#, SMI#,
CPUSLP#, A20M#, INTR, NMI,
IGNNE#, INIT#
-----REGISTER CONTROLLER
NEED SETTING
```

BSEL1	BSEL0	CPU
LOW	HIGH	133MHz
HIGH	LOW	200MHz

MICRO-STAR INT'L CO.,LTD.

Title: **FCPGA478-1**

Size: Custom | Document Number: MS-1002 | Rev: 0A

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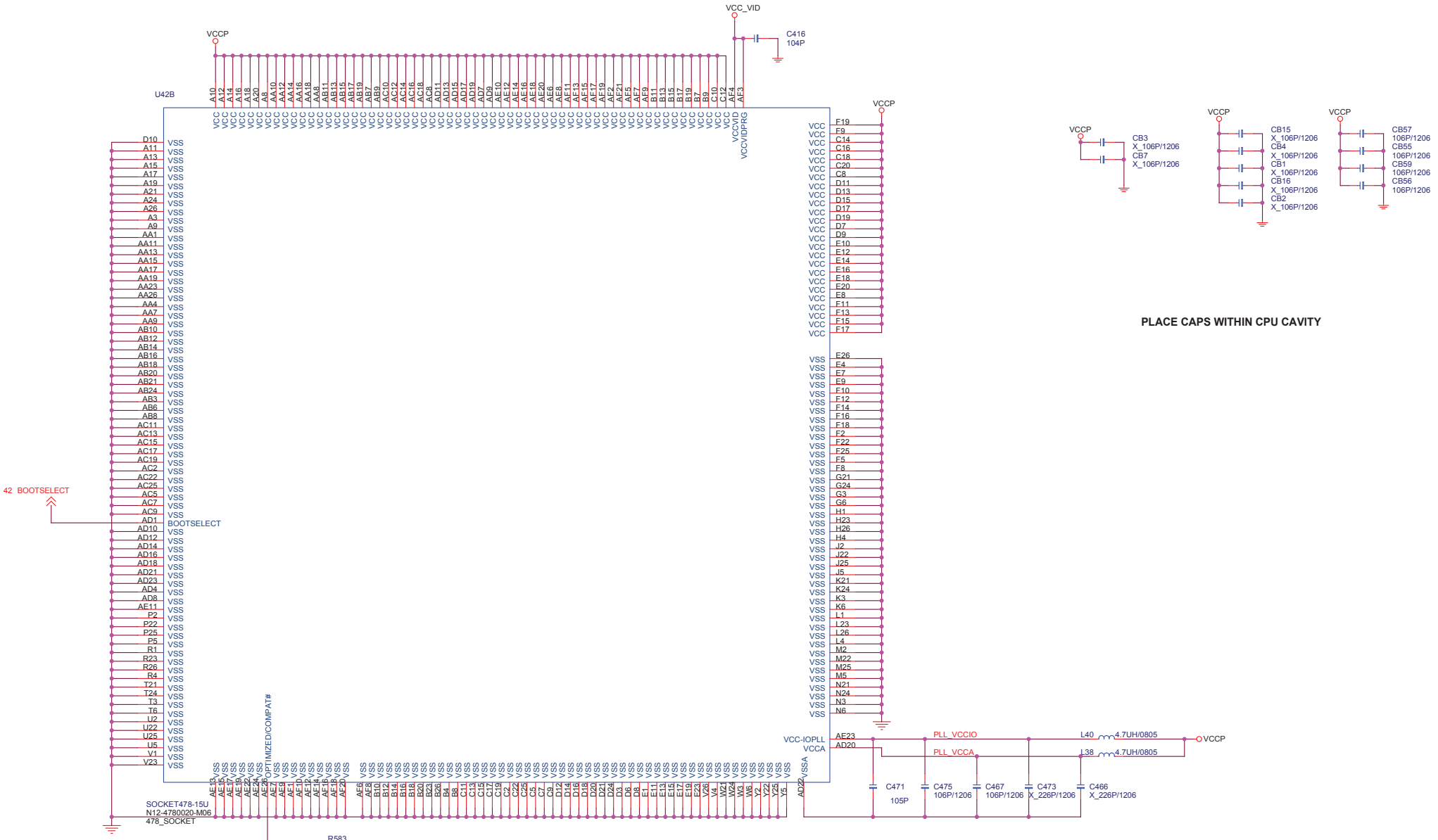
FOR NORTHWOOD CPU ONLY



PLACE CAPS WITHIN CPU CAVITY

	R1	R2
OPTIMIZED	49.9RST	OPEN
COMPAT#	OPEN	0

MICRO-STAR INT'L LO.,LTD.	
Title	FCPGA478-2
Size: Custom	Document Number: MS-1002
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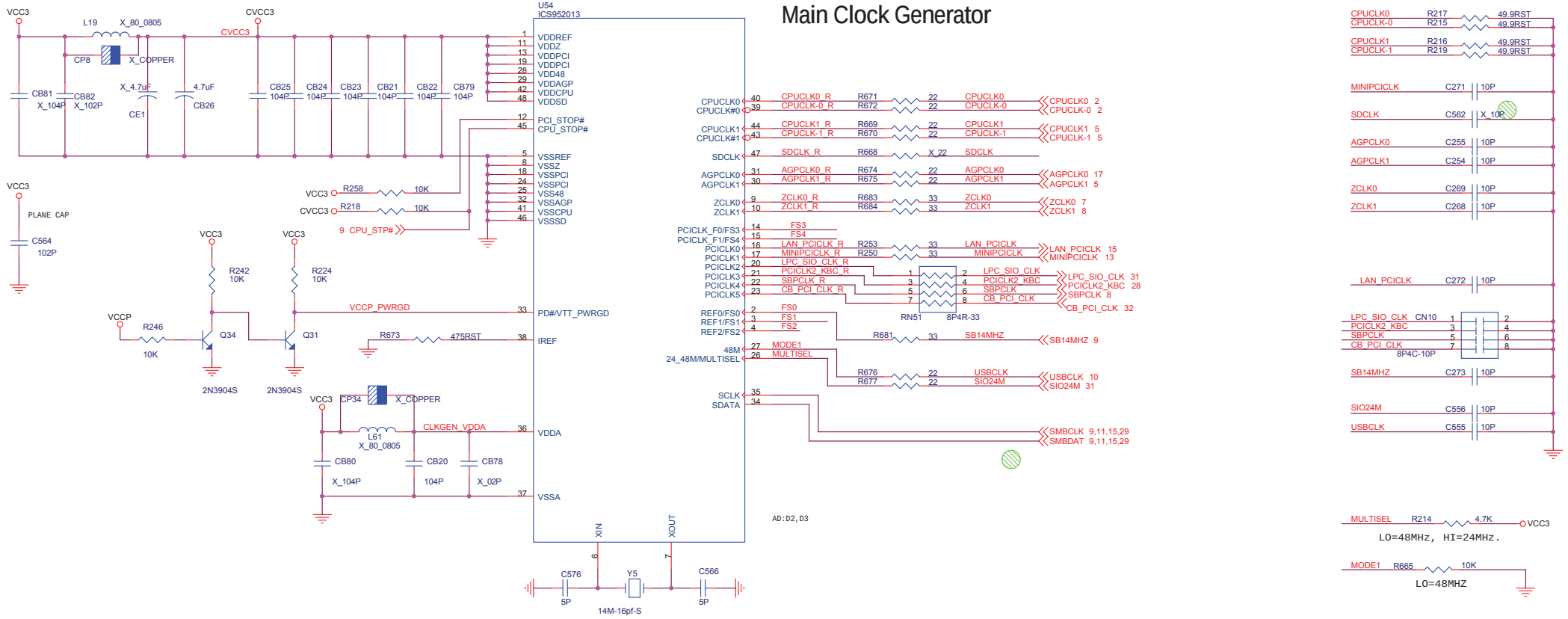
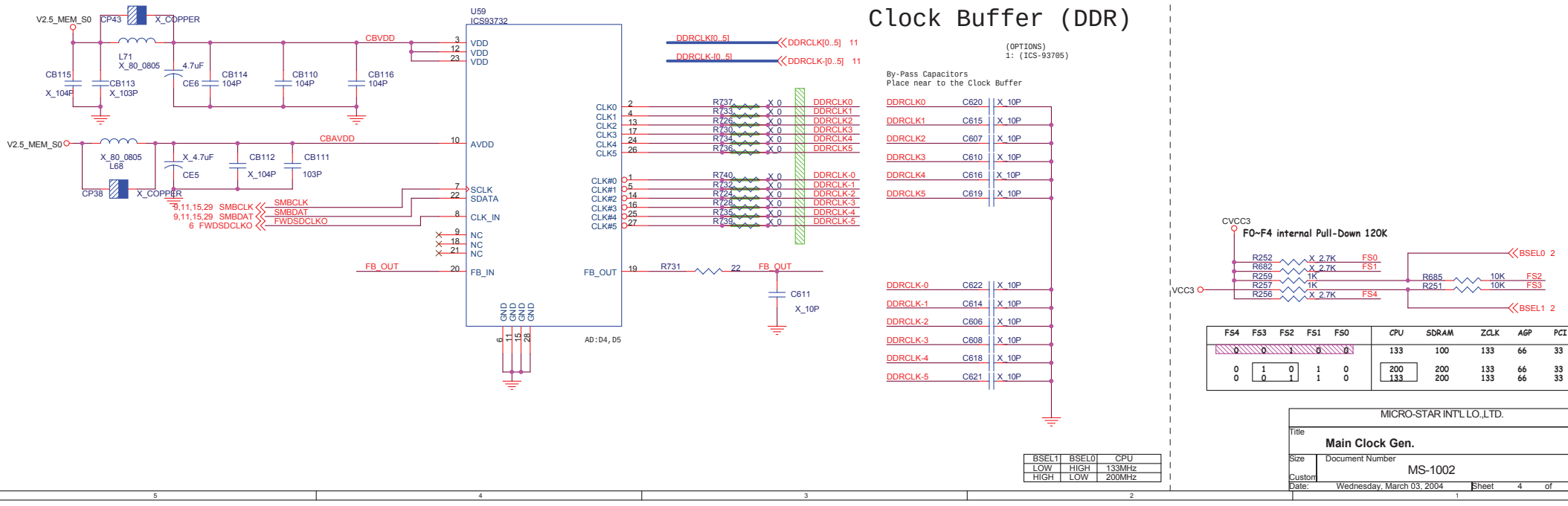
Date: Wednesday, March 03, 2004	Sheet 3 of 44

Main Clock Generator



Clock Buffer (DDR)



BSEL1	BSEL0	CPU
LOW	HIGH	133MHz
HIGH	LOW	200MHz

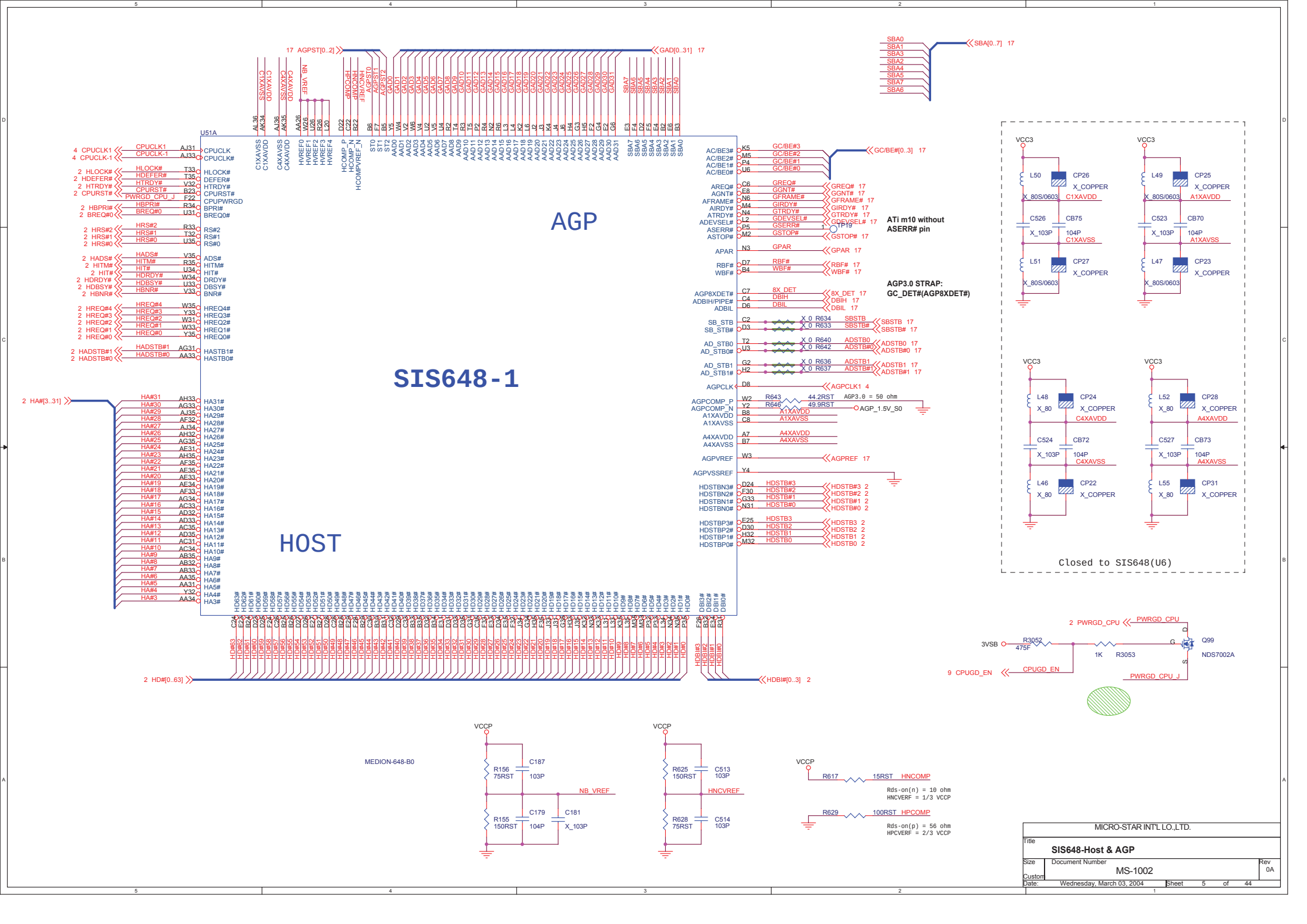
FS4	FS3	FS2	FS1	FS0	CPU	SDRAM	ZCLK	AGP	PCI
0	0	1	0	0	133	100	133	66	33
0	1	0	1	0	200	200	133	66	33
0	0	1	1	0	133	200	133	66	33

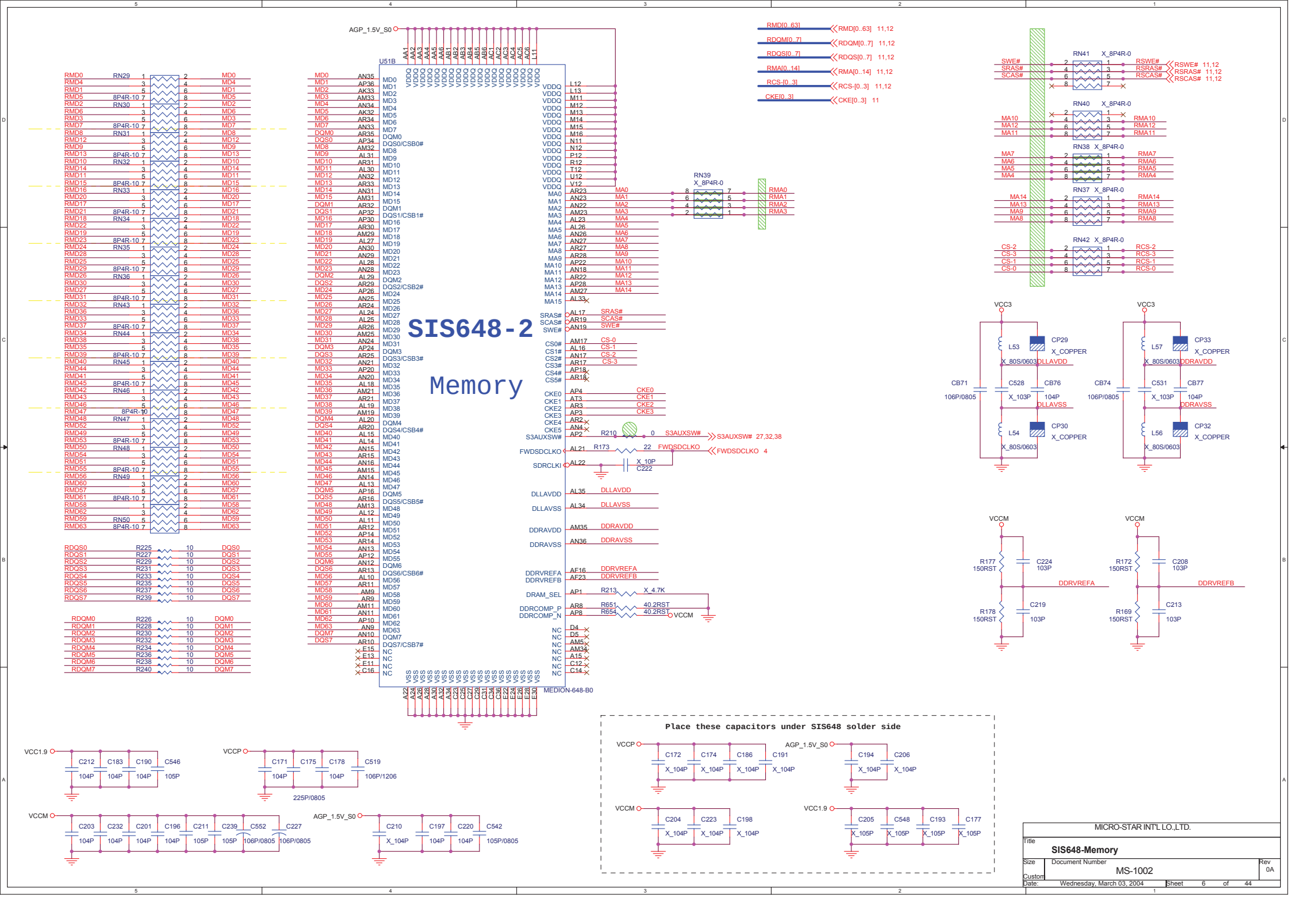
MICRO-STAR INT'L LO.,LTD.

Title: Main Clock Gen.

Size: Custom | Document Number: MS-1002 | Rev: 0A

Date: Wednesday, March 03, 2004 | Sheet 4 of 44


SIS648-1
AGP
HOST
U51A
ATi m10 without ASERR# pin
AGP3.0 STRAP: GC_DET#(AGP8XDET#)
Closed to SIS648(U6)
MEDION-648-B0
MICRO-STAR INT'L LO.,LTD.
SIS648-Host & AGP
MS-1002
Wednesday, March 03, 2004


SIS648-2
Memory
U51B
MEDION-648-B0
AGP_1.5V_S0
RMD[0..63]
RDQM[0..7]
RDQS[0..7]
RMA[0..14]
RCS-[0..3]
CKE[0..3]
RN29
RN30
RN31
RN32
RN33
RN34
RN35
RN36
RN43
RN44
RN45
RN46
RN47
RN48
RN49
RN50
8P4R-10
RDQS0
RDQS1
RDQS2
RDQS3
RDQS4
RDQS5
RDQS6
RDQS7
RDQM0
RDQM1
RDQM2
RDQM3
RDQM4
RDQM5
RDQM6
RDQM7
RN39
X_8P4R-0
RMA0
RMA1
RMA2
RMA3
SRAS#
SCAS#
SWE#
CS-0
CS-1
CS-2
CS-3
CKE0
CKE1
CKE2
CKE3
S3AUXSW#
FWDSDCLKO
SDRCLKI
DLLAVDD
DLLAVSS
DDRAVDD
DDRAVSS
DDRVREFA
DDRVREFB
DRAM_SEL
DDRCOMP_P
DDRCOMP_N
VCCM
RN41
RN40
RN38
RN37
RN42
RCS-2
RCS-3
RCS-1
RCS-0
VCC3
CP29
CP30
CP33
CP32
X_COPPER
X_80S/0603
DLLAVDD
DDRAVDD
DLLAVSS
DDRAVSS
CB71
CB76
CB74
CB77
106P/0805
C528
C531
X_103P
104P
L53
L54
L57
L56
VCCM
R177
R178
R172
R169
150RST
C224
C219
C208
C213
103P
DDRVREFA
DDRVREFB
Place these capacitors under SIS648 solder side
VCCP
AGP_1.5V_S0
VCC1.9
C172
C174
C186
C191
C194
C206
C204
C223
C198
C205
C548
C193
C177
X_104P
X_105P
MICRO-STAR INT'L LO.,LTD.
Title
SIS648-Memory
Size
Custom
Document Number
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Rev
0A
Date:
Wednesday, March 03, 2004
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6
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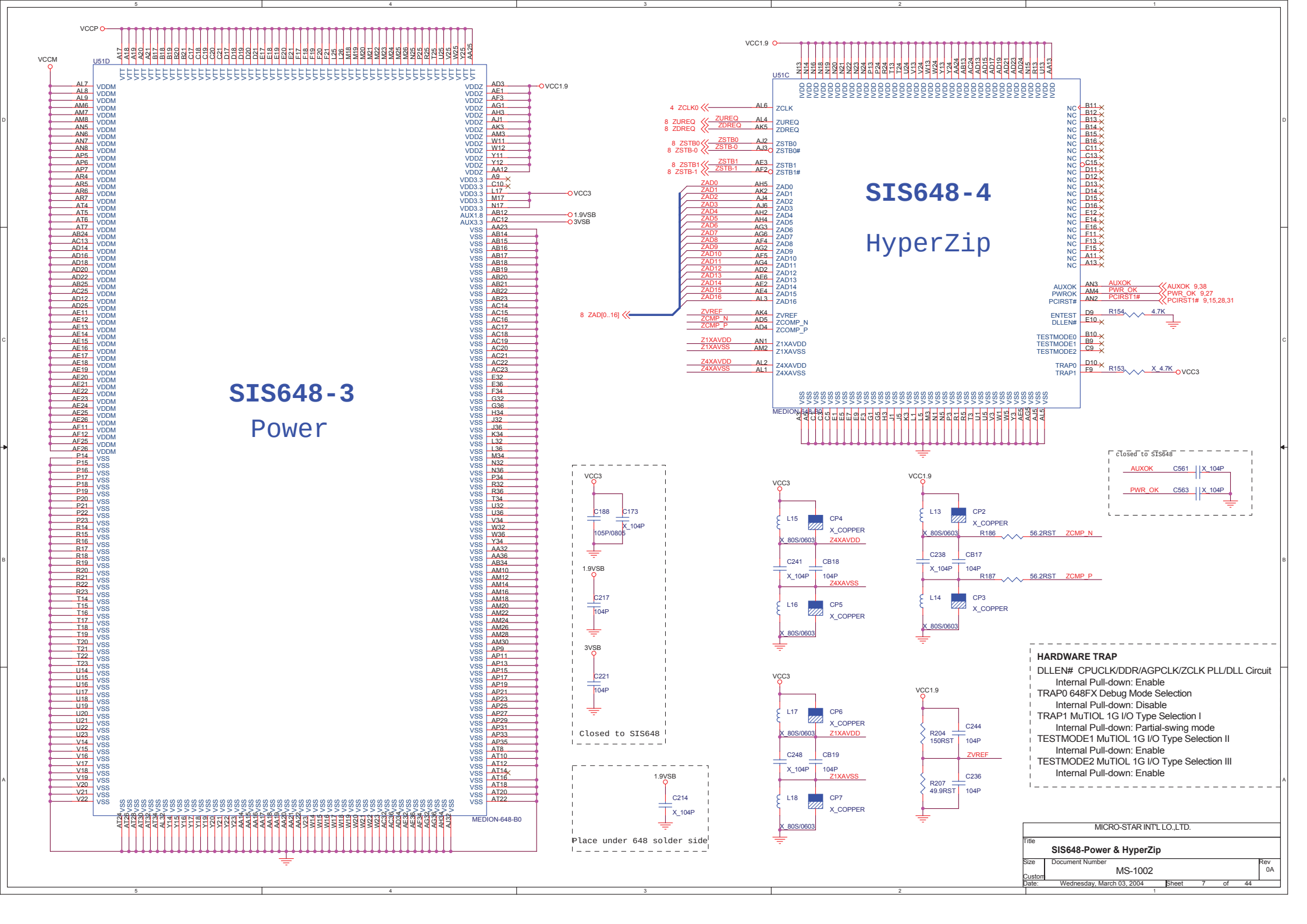
44


SIS648-3
Power
SIS648-4
HyperZip
U51D
U51C
MEDION-648-B0
VCCP
VCCM
VCC1.9
VCC3
1.9VSB
3VSB
8 ZAD[0..16]
Closed to SIS648
Place under 648 solder side
closed to SIS648
HARDWARE TRAP
DLLEN# CPUCLK/DDR/AGPCLK/ZCLK PLL/DLL Circuit
Internal Pull-down: Enable
TRAP0 648FX Debug Mode Selection
Internal Pull-down: Disable
TRAP1 MuTIOL 1G I/O Type Selection I
Internal Pull-down: Partial-swing mode
TESTMODE1 MuTIOL 1G I/O Type Selection II
Internal Pull-down: Enable
TESTMODE2 MuTIOL 1G I/O Type Selection III
Internal Pull-down: Enable
MICRO-STAR INT'L LO.,LTD.
Title
SIS648-Power & HyperZip
Size
Custom
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MS-1002
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0A
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X	PGNT#0	PREQ#0
X	PGNT#1	PREQ#1
MINIPCI	PGNT#2	PREQ#2
CARDREADER	PGNT#3	PREQ#3
GIGALAN	PGNT#4	PREQ#4

Enable Intergrated Resister
LPC 73[4:0]=11111

PREQ#[0:4], IDEREQA, ICHRDYA, IDEIRQA, IDEREQB, ICHRDYB, IDEIRQB
------- REGISTER NEED SETTING

PCI

IDE

963-1

HyperZip

SIS963-B1

PCI BUS PULL-UP
Enable internal Intergrated Resister.

RN78 10P8R-2.2K
PERR# DEVSEL# STOP# PLOCK# SERR# IRDY# FRAME# TRDY#

PREQ#4 R719 X_4.7K
LPC 73[4:0]=11111

RN119 8P4R-2.2K
INTD# INTB# INTA# INTC#

Put near 963 Chip.
ZSTB0 R727 X_4.7K
ZSTB1 R721 X_4.7K
ZSTB-0 R729 X_4.7K
ZSTB-1 R725 X_4.7K

Analog Power supplies of Transzip function for 963 Chip.

Title	SIS963-1 PCI & IDE & HyperZip
Size	Document Number: MS-1002
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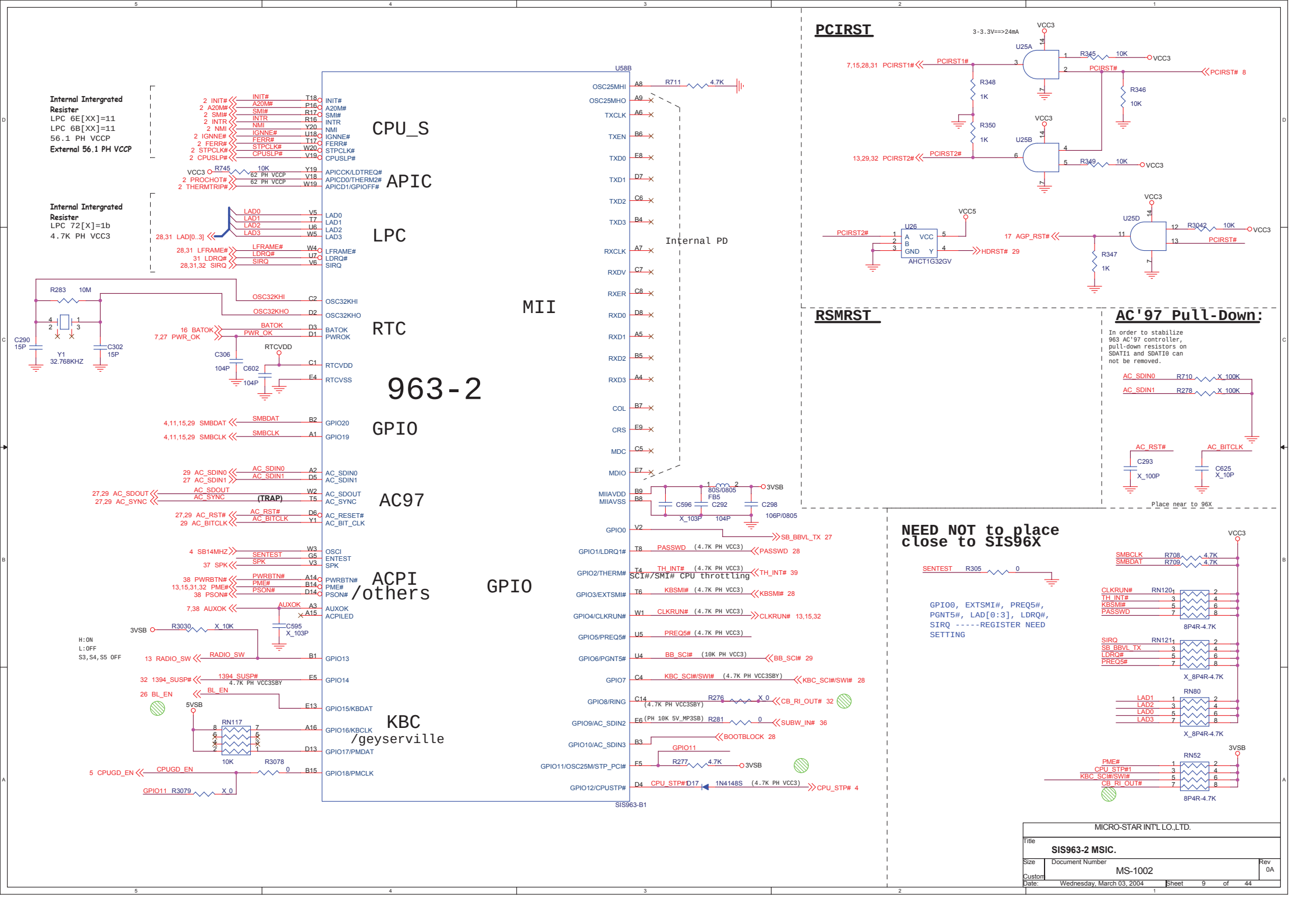
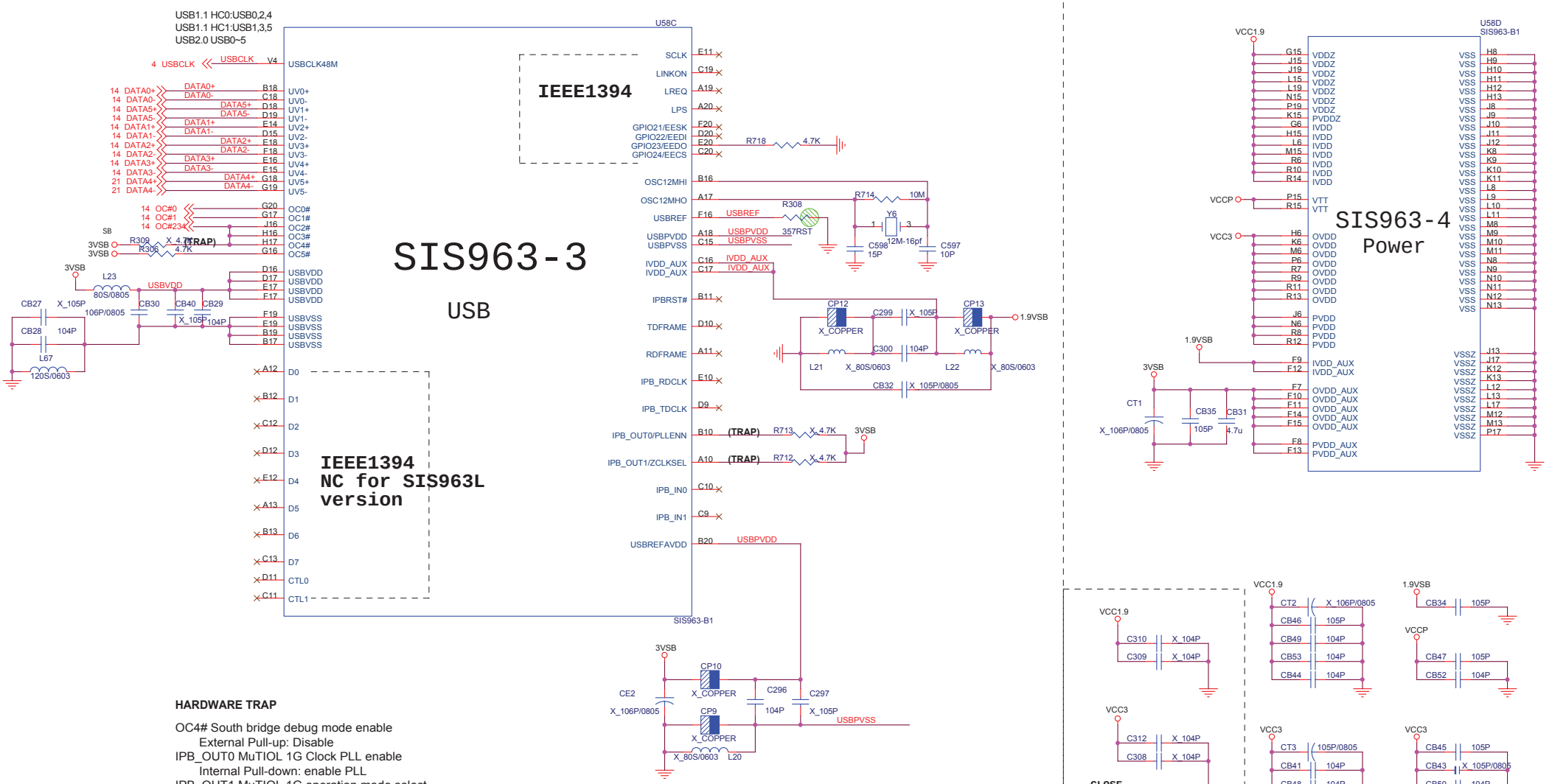
Date:	Wednesday, March 03, 2004
Sheet	8 of 44

MICRO-STAR INT'L LO.,LTD.


Internal Intergrated Resister
LPC 6E[XX]=11
LPC 6B[XX]=11
56.1 PH VCCP
External 56.1 PH VCCP
CPU_S
APIC
Internal Intergrated Resister
LPC 72[X]=1b
4.7K PH VCC3
LPC
RTC
963-2
MII
Internal PD
GPIO
AC97
ACPI /others
GPIO
KBC /geyserville
SIS963-B1
PCIRST
RSMRST
AC'97 Pull-Down:
In order to stabilize 963 AC'97 controller, pull-down resistors on SDATI1 and SDATI0 can not be removed.
Place near to 96X
NEED NOT to place close to SIS96X
GPIO0, EXTSMI#, PREQ5#, PGNT5#, LAD[0:3], LDRQ#, SIRQ -----REGISTER NEED SETTING
H:ON
L:OFF
S3,S4,S5 OFF
MICRO-STAR INT'L LO.,LTD.
SIS963-2 MSIC.
MS-1002
Wednesday, March 03, 2004



MICRO-STAR INT'L CO.,LTD.

Title: SIS963-3/4 USB & Power

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Addr =1010000b

Addr =1010001b

TYPE 1

TYPE 2

DM2

DM1

0:Damping
47/(33):Term

10:Damping
47/(33):Term

DDR-SODIMM-5MM

DDR-SODIMM-9MM

N13-2000010-A10
DDR_SODIMM_STD

N13-2000040-A10
ddr_sodimm_c1470800

RN116 10K

10K RN118

RN114 10K

10K RN115

DDRVREF GEN. & DECOUPLING

R243 75 1%

R247 75 1%

C278 1000P

C280 1000P

C570 1000P

C584 1000P

C294 0.1u

C270 0.1u

R269 X_0

R263 X_0

R267 10K

R261 10K

RN113

X_8P4R-470

NOTE:

VDDID IS A TRAP ON THE DIMM MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDD!=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

DIMM DECOUPLING

C276 0.1u
C582 0.1u
C587 0.1u
C573 0.1u
C571 0.1u
C588 0.1u
C572 0.1u
C275 0.1u
C574 0.1u
C586 0.1u
C581 0.1u
C603 0.1u

Title: 200 PIN NB DDR SO-DIMM SKT

Size: Custom | Document Number: MS-1002 | Rev: {RevCode}

Date: Wednesday, March 03, 2004 | Sheet 11 of 44

DDR TERMINATOR

SSTL-2 Termination Resistors

RMD[0..63]
RDQM[0..7]
RDQS[0..7]
RMA[0..14]
RCS-[0..3]

RMD[0..63] 6,11
RDQM[0..7] 6,11
RDQS[0..7] 6,11
RMA[0..14] 6,11
RCS-[0..3] 6,11

	SDR		Rs	DDR		Rs	Rtt
MD/DQM(/DQS)	LV-CMOS		0/10/-	SSTL-2		10	33
MA/Control	LV-CMOS		10	SSTL-2		0	33
CS	LV-CMOS		0	SSTL-2		0	47
CKE	OD 3.3V			OD 2.5V			

DDR_VTT

RN53 RMD0 RMD4 RMD1 RMD5 8P4R-47
RN54 RMD2 RMD6 RMD3 RMD7 8P4R-47
RN55 RMD8 RMD12 RMD9 RMD13 8P4R-47
RN56 RMD10 RMD14 RMD11 RMD15 8P4R-47
RN61 RMA14 RMA13 8P4R-47
RN57 RMD16 RMD20 RMD17 RMD21 8P4R-47
RN62 RMA9 RMA8 RMA7 RMA6 8P4R-47
RN60 RMD26 RMD30 RMD27 RMD31 8P4R-47
RN58 RMD18 RMD22 RMD19 RMD23 8P4R-47
RN59 RMD24 RMD28 RMD25 RMD29 8P4R-47
RN63 RMA5 RMA4 RMA3 RMA2 8P4R-47
RN68 RMD34 RMD38 RMD35 RMD39 8P4R-47

RDQM0 R289 47
RDQM1 R291 47
RDQM2 R293 47
RDQM3 R295 47
RDQM4 R297 47
RDQM5 R299 47
RDQM6 R301 47
RDQM7 R303 47

RDQS0 R288 47
RDQS1 R290 47
RDQS2 R292 47
RDQS3 R294 47
RDQS4 R296 47
RDQS5 R298 47
RDQS6 R300 47
RDQS7 R302 47

DDR_VTT

RN64 RMA1 RMA0 RMA10 RMA12 8P4R-47
RN67 RMD32 RMD36 RMD33 RMD37 8P4R-47
RN70 RMD42 RMD43 RMD46 RMD47 8P4R-47
RN66 RCS-2 RCS-3 RCS-1 RCS-0 8P4R-47

RN71 8P4R-47
RMD48 RMD52 RMD49 RMD53
RN72 RMD50 RMD54 RMD51 RMD55 8P4R-47
RN74 RMD58 RMD62 RMD59 RMD63 8P4R-47
RN73 RMD56 RMD60 RMD57 RMD61 8P4R-47

DDR_VTT

RN69 RMD40 RMD44 RMD41 RMD45 8P4R-47
RN65 RMA11 RSWE# RSRAS# RSCAS# 8P4R-47

6,11 RSWE#
6,11 RSRAS#
6,11 RSCAS#

DDR_VTT

DECOUPLING CAPACITOR FOR SSTL-2 END TERMIANTION VTT ISLAND
0603 Package placed within 200mils of VTT Termination R-packs

R873 100K

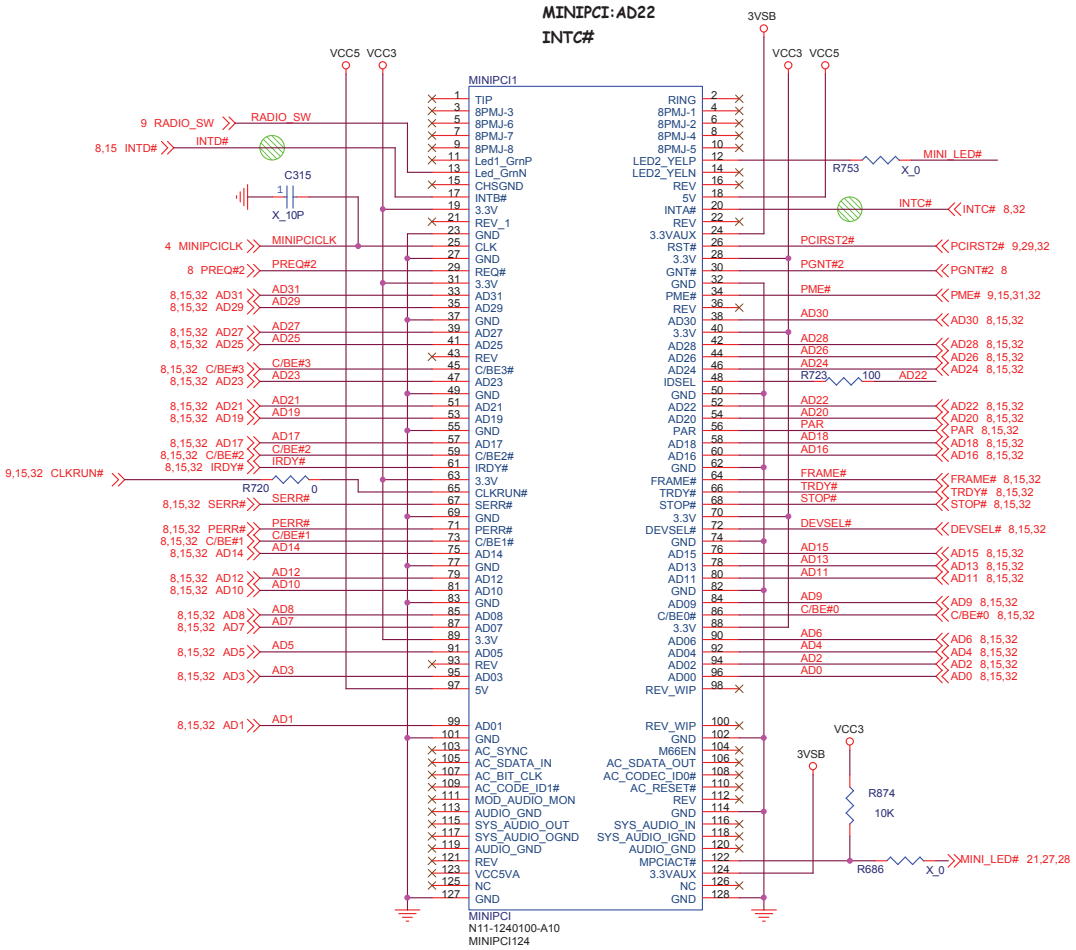
CB107 CB104 CB89 CB83
CB90 CB87 CB94 CB101
CB39 CB92 CB37 CB109
106P/1206 106P/1206
CB85 CB105 CB98 CB86
0.1u

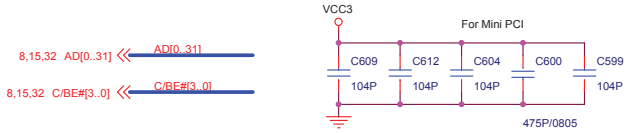
DDR_VTT

CB108 CB106 CB100 CB96
CB88 CB33 CB103 CB84
CB38 CB91 CB36 CB97
106P/1206 106P/1206
CB95 CB93 CB99 CB102
0.1u

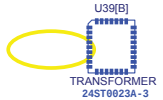
MICRO-STAR INT'L LO.,LTD.			
Title: DDR Terminator			
Size: Custom	Document Number: MS-1002		Rev: 0A
Date: Wednesday, March 03, 2004	Sheet 12 of 44		

Mini PCI



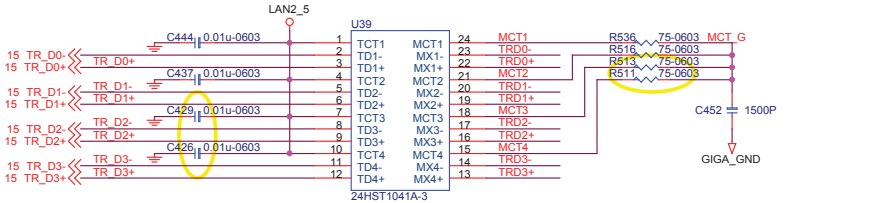


Broadcom 10/100 and Giga LAN

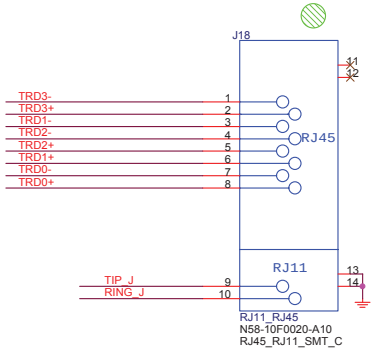


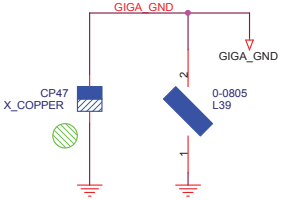
LAN MAGNETICS

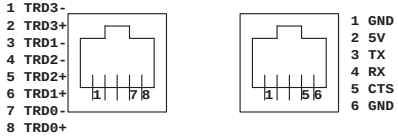
	BCM4401
NOT INSTALL	R209,R210 C149,C151
Transformer	H1267(L05-0100050-P21)

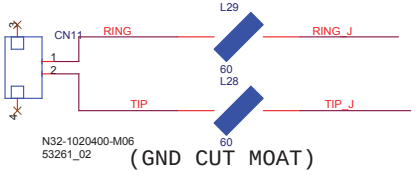


LAN CONNECTOR







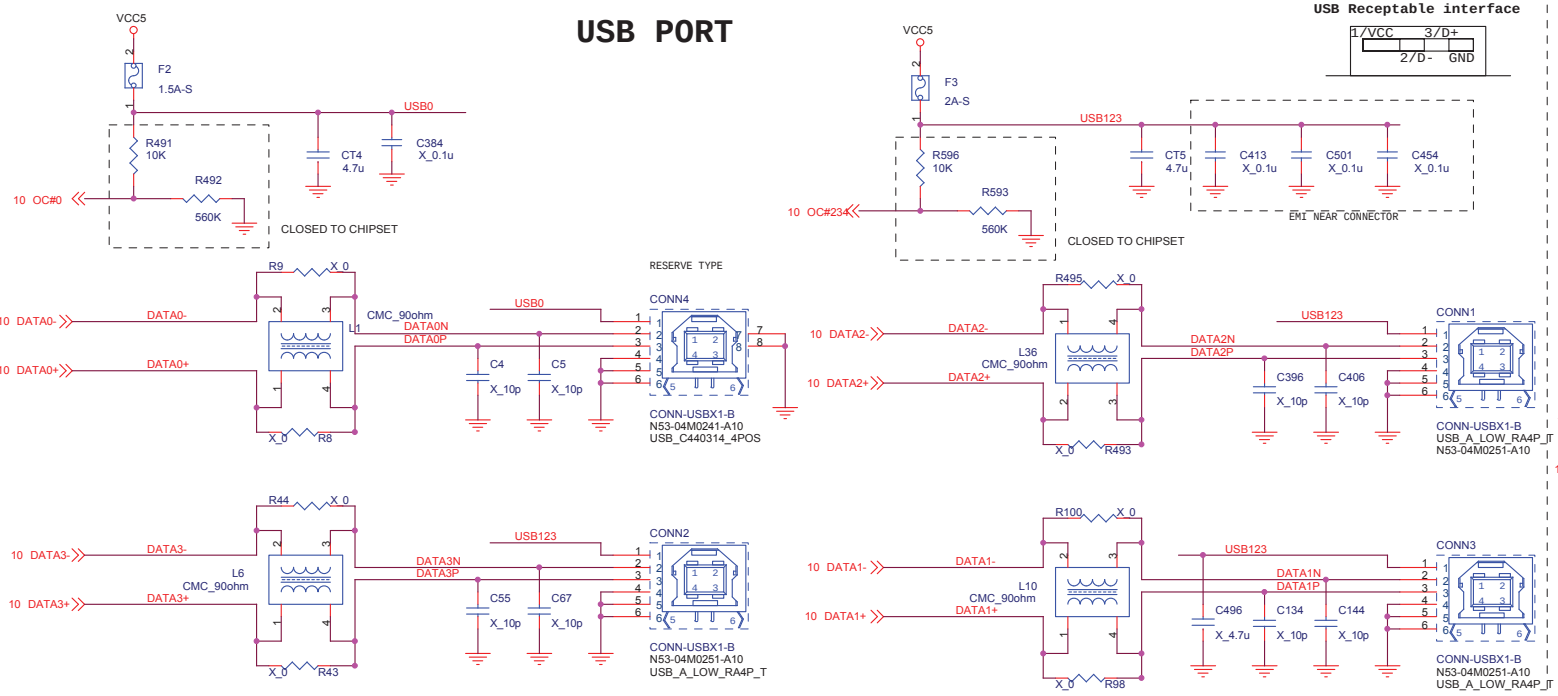


(GND CUT MOAT)

MICRO-STAR INT'L LO.,LTD.

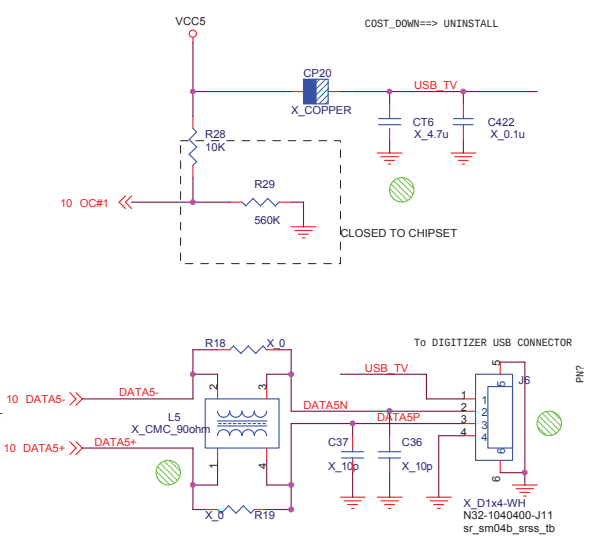
Title	Mini PCI	
Size: Custom	Document Number: MS-1002	Rev: 0A
Date: Thursday, March 04, 2004	Sheet 13 of 44	

USB PORT

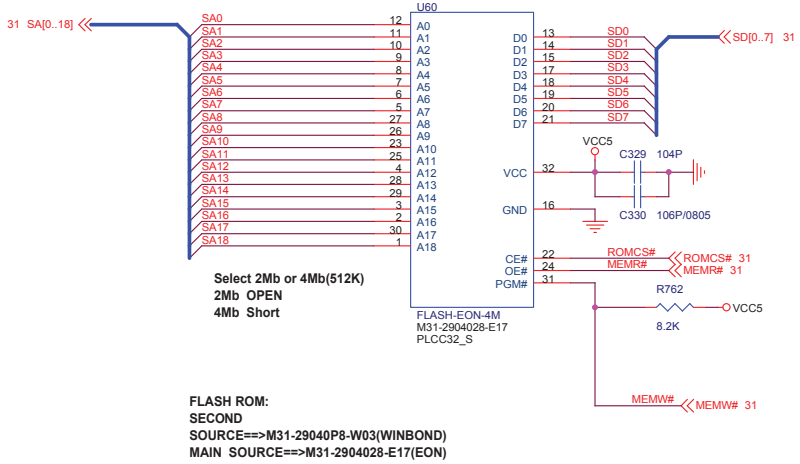


USB Receptable interface

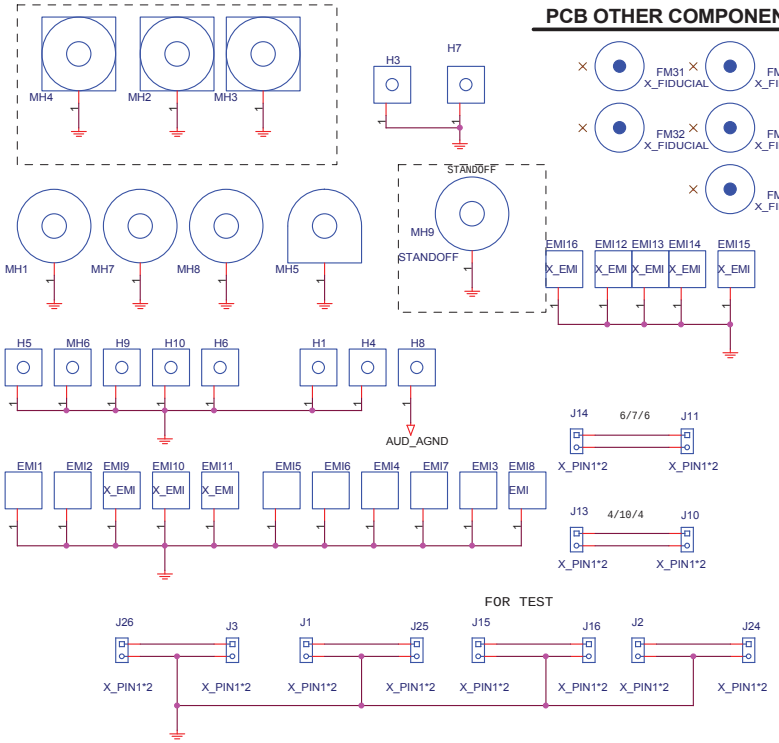
DIGITIZER USB PORT



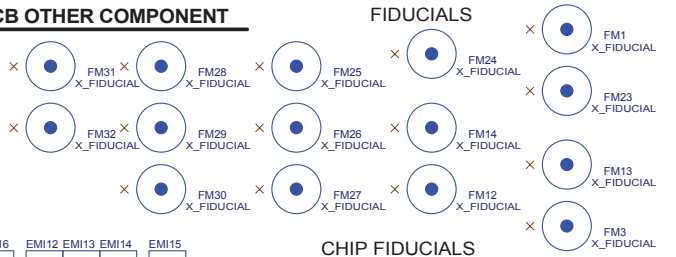
Flash Rom



FLASH ROM:
SECOND
SOURCE==>M31-29040P8-W03(WINBOND)
MAIN SOURCE==>M31-2904028-E17(EON)

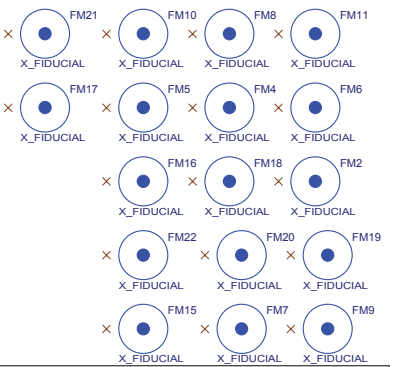


PCB OTHER COMPONENT

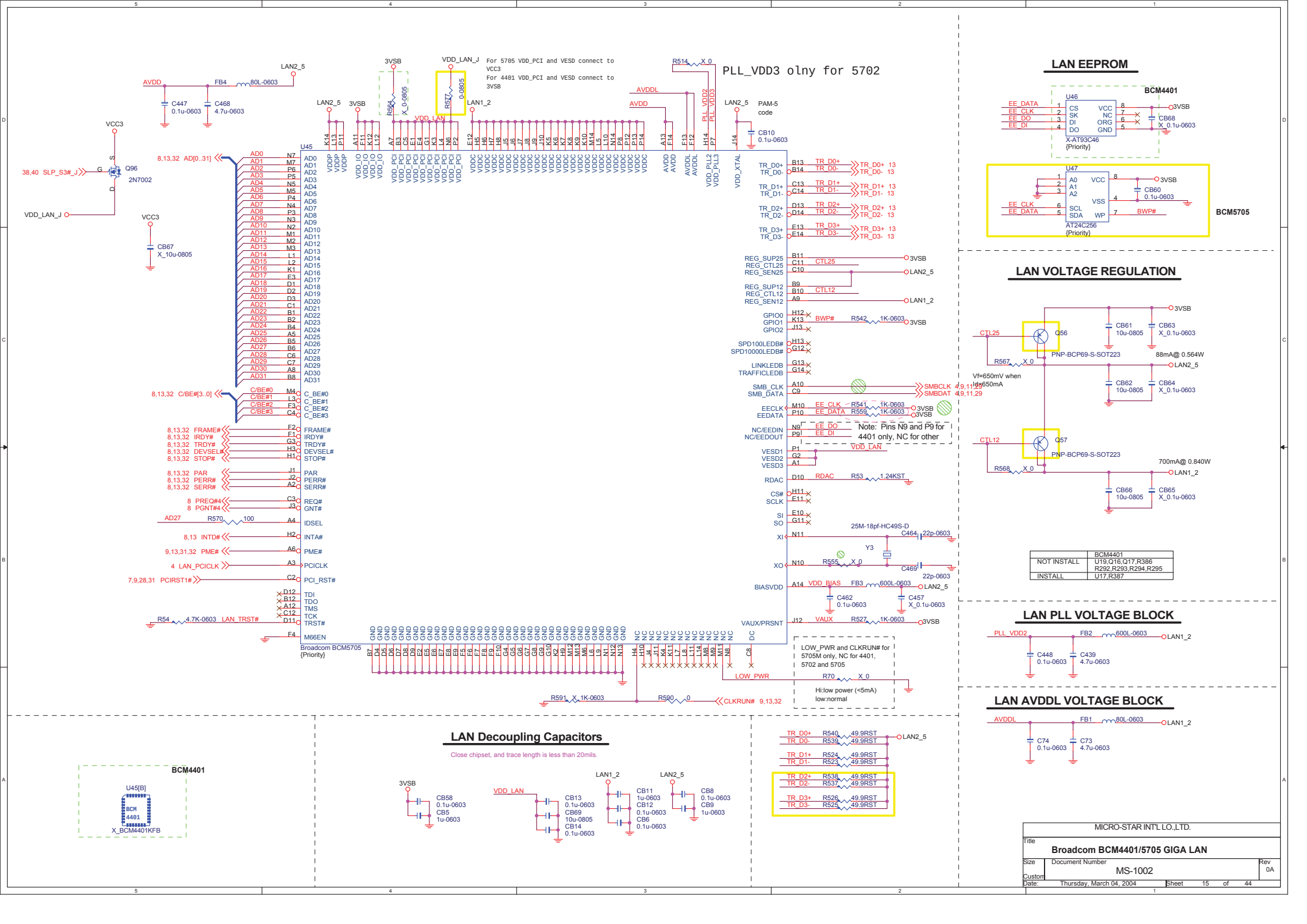


FIDUCIALS

CHIP FIDUCIALS

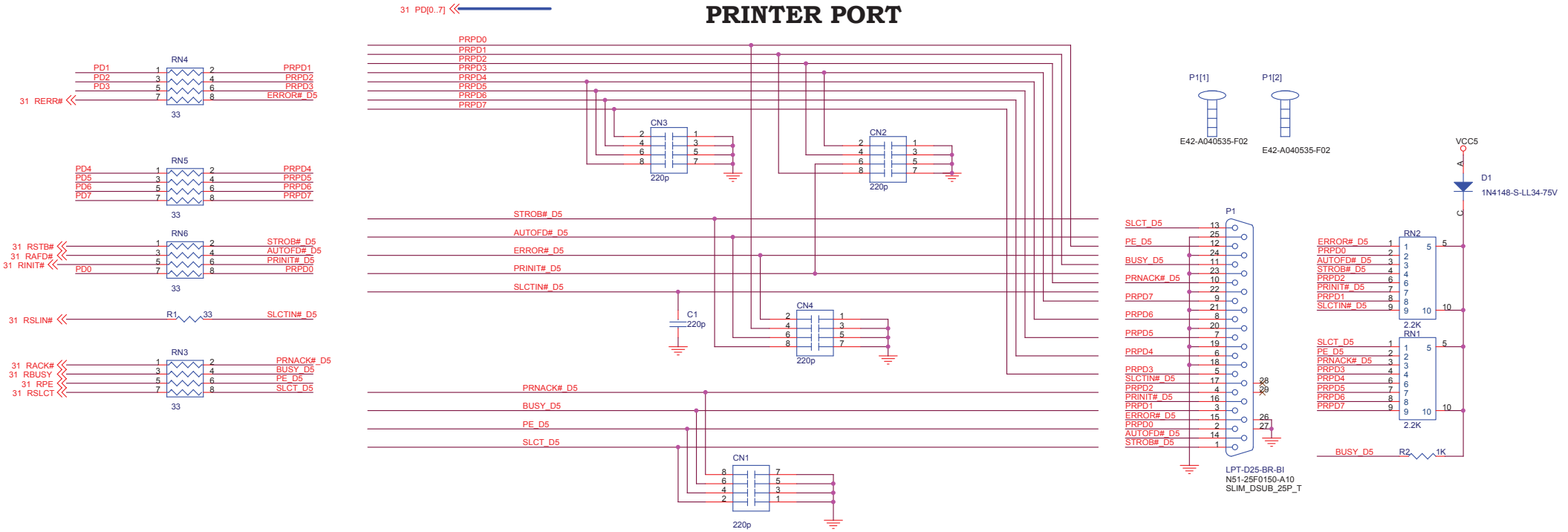


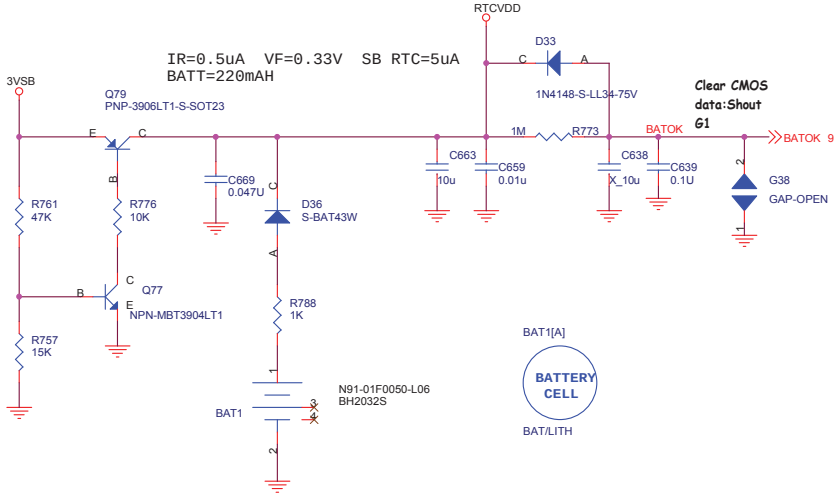
MICRO-STAR INT'L CO.,LTD.		
Title: USB port & BIOS TV_TUNER		
Size: Custom	Document Number: MS-1002	Rev: 0A
Date: Thursday, March 04, 2004	Sheet 14 of 44	

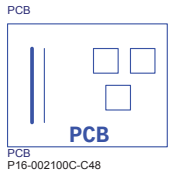

PLL_VDD3 olny for 5702
For 5705 VDD_PCI and VESD connect to VCC3
For 4401 VDD_PCI and VESD connect to 3VSB
LAN EEPROM
BCM4401
BCM5705
LAN VOLTAGE REGULATION
LAN PLL VOLTAGE BLOCK
LAN AVDDL VOLTAGE BLOCK
LAN Decoupling Capacitors
Close chipset, and trace length is less than 20mils.
Broadcom BCM5705 {Priority}
Note: Pins N9 and P9 for 4401 only, NC for other
LOW_PWR and CLKRUN# for 5705M only, NC for 4401, 5702 and 5705
Hi:low power (<5mA) low:normal
MICRO-STAR INT'L LO.,LTD.
Broadcom BCM4401/5705 GIGA LAN
MS-1002
Thursday, March 04, 2004

Parallel Port & COM1

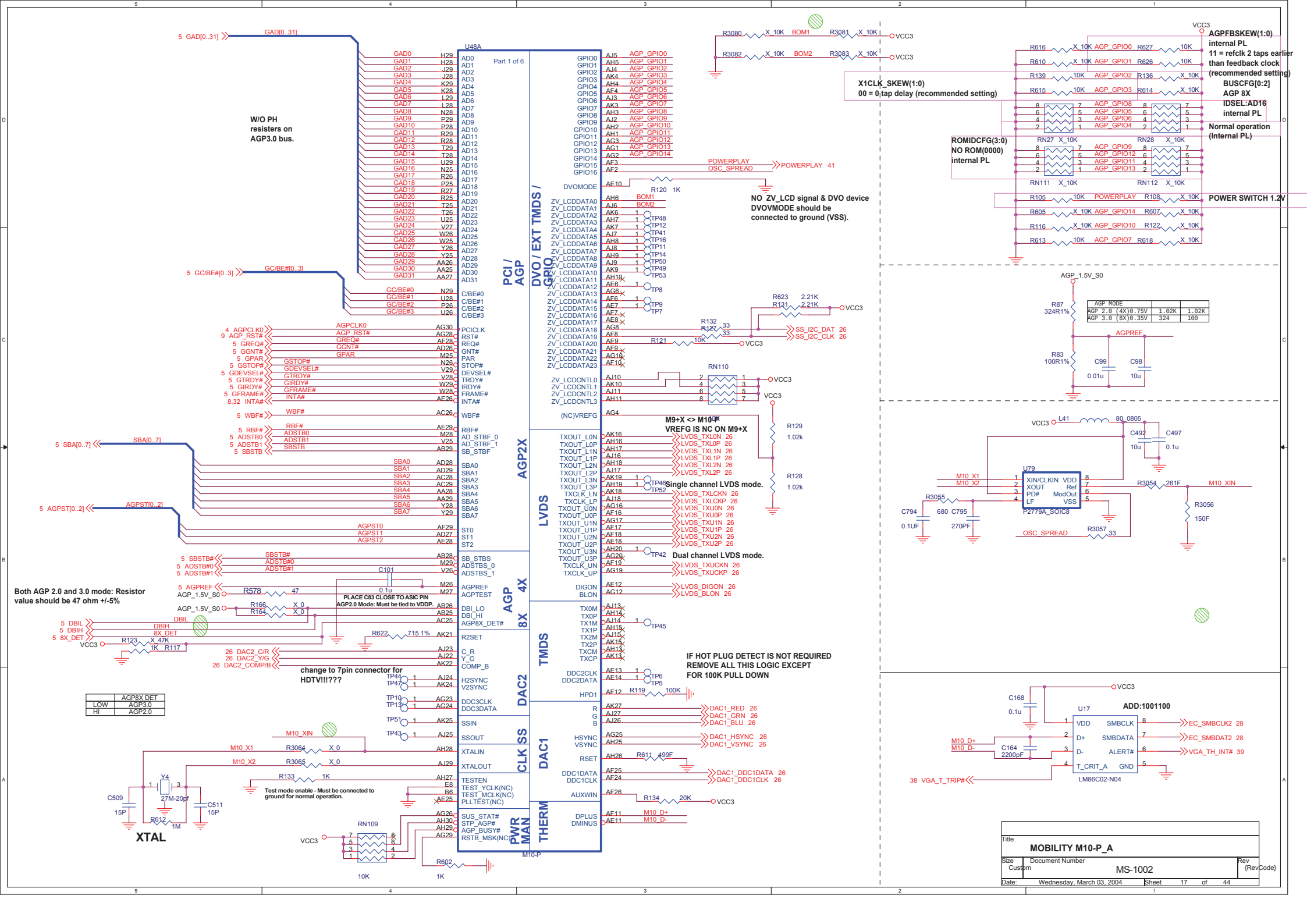
PRINTER PORT

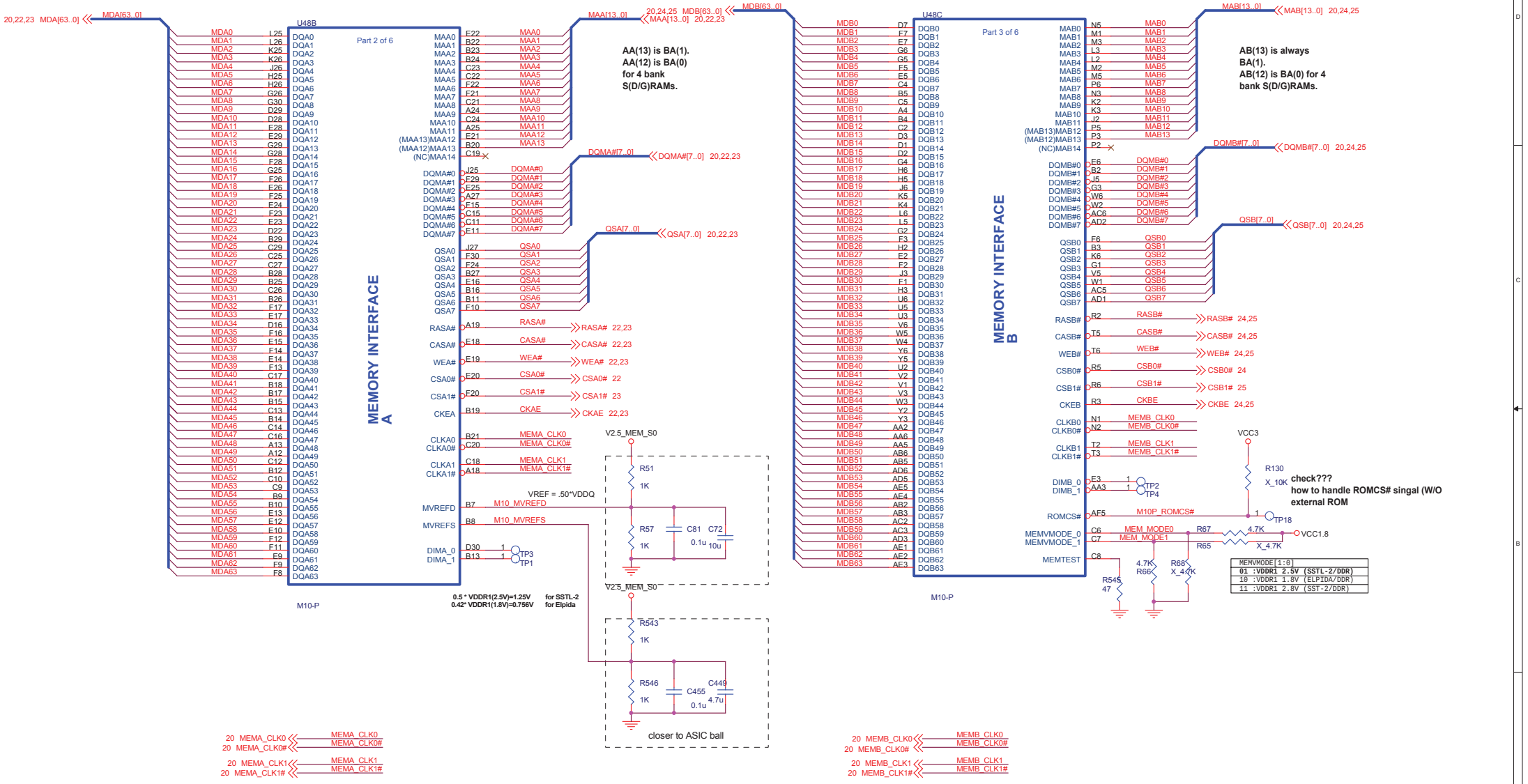




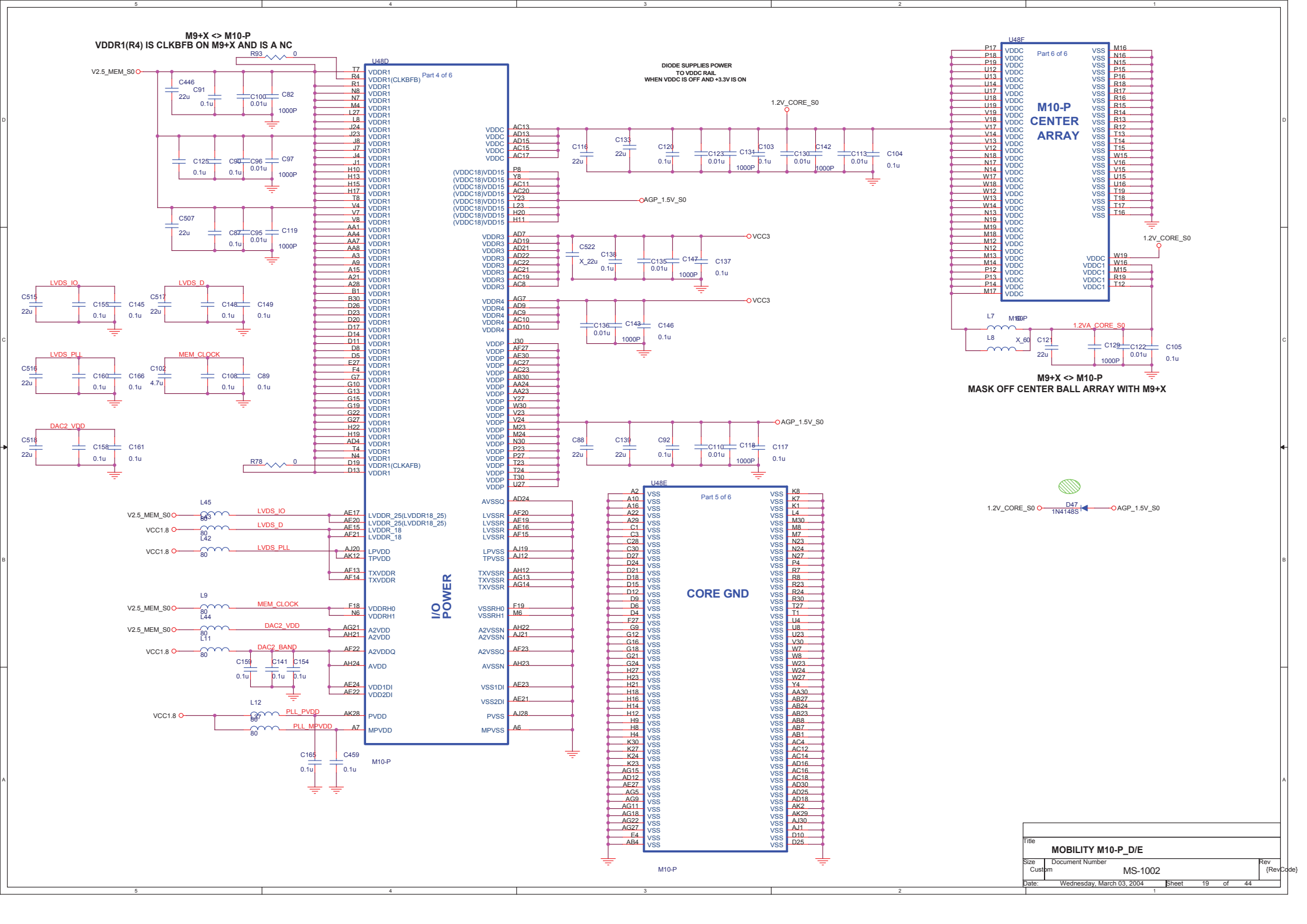


MICRO-STAR INT'L LO.,LTD.		
Title: RTC BAT/Parallel port/MANAUL PARTS		
Size: Custom	Document Number: MS-1002	Rev: 0A
Date: Thursday, March 04, 2004	Sheet 16 of 44	


W/O PH resisters on AGP3.0 bus.
Both AGP 2.0 and 3.0 mode: Resistor value should be 47 ohm +/-5%
PLACE C83 CLOSE TO ASIC PIN
AGP2.0 Mode: Must be tied to VDDP.
change to 7pin connector for HDTV!!!???
Test mode enable - Must be connected to ground for normal operation.
XTAL
X1CLK_SKEW(1:0)
00 = 0 tap delay (recommended setting)
NO ZV_LCD signal & DVO device DVOVMODE should be connected to ground (VSS).
M9+X <> M10+X
VREFG IS NC ON M9+X
Single channel LVDS mode.
Dual channel LVDS mode.
IF HOT PLUG DETECT IS NOT REQUIRED REMOVE ALL THIS LOGIC EXCEPT FOR 100K PULL DOWN
AGPFBSKEW(1:0)
internal PL
11 = refclk 2 taps earlier than feedback clock (recommended setting)
BUSCFG[0:2]
AGP 8X
IDSEL:AD16
internal PL
Normal operation (Internal PL)
ROMIDCFG(3:0)
NO ROM(0000)
internal PL
POWER SWITCH 1.2V
ADD:1001100
MOBILITY M10-P_A
MS-1002
Wednesday, March 03, 2004



Title	MOBILITY M10-P_B/C	
Size: Custom	Document Number: MS-1002	Rev: {RevCode}
Date: Wednesday, March 03, 2004	Sheet 18 of 44	


M9+X <> M10-P
VDDR1(R4) IS CLKBFB ON M9+X AND IS A NC
U48D
Part 4 of 6
I/O POWER
M10-P
DIODE SUPPLIES POWER
TO VDDC RAIL
WHEN VDDC IS OFF AND +3.3V IS ON
U48E
Part 5 of 6
CORE GND
M10-P
U48F
Part 6 of 6
M10-P CENTER ARRAY
M9+X <> M10-P
MASK OFF CENTER BALL ARRAY WITH M9+X
V2.5_MEM_S0
VCC1.8
1.2V_CORE_S0
AGP_1.5V_S0
VCC3
1.2VA_CORE_S0
LVDS_IO
LVDS_D
LVDS_PLL
MEM_CLOCK
DAC2_VDD
DAC2_BAND
PLL_PVDD
PLL_MPVDD
R93
R78
L45
L42
L9
L44
L11
L12
L7
L8
D47
1N4148S
Title
MOBILITY M10-P_D/E
Size
Custom
Document Number
MS-1002
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{RevCode}
Date:
Wednesday, March 03, 2004
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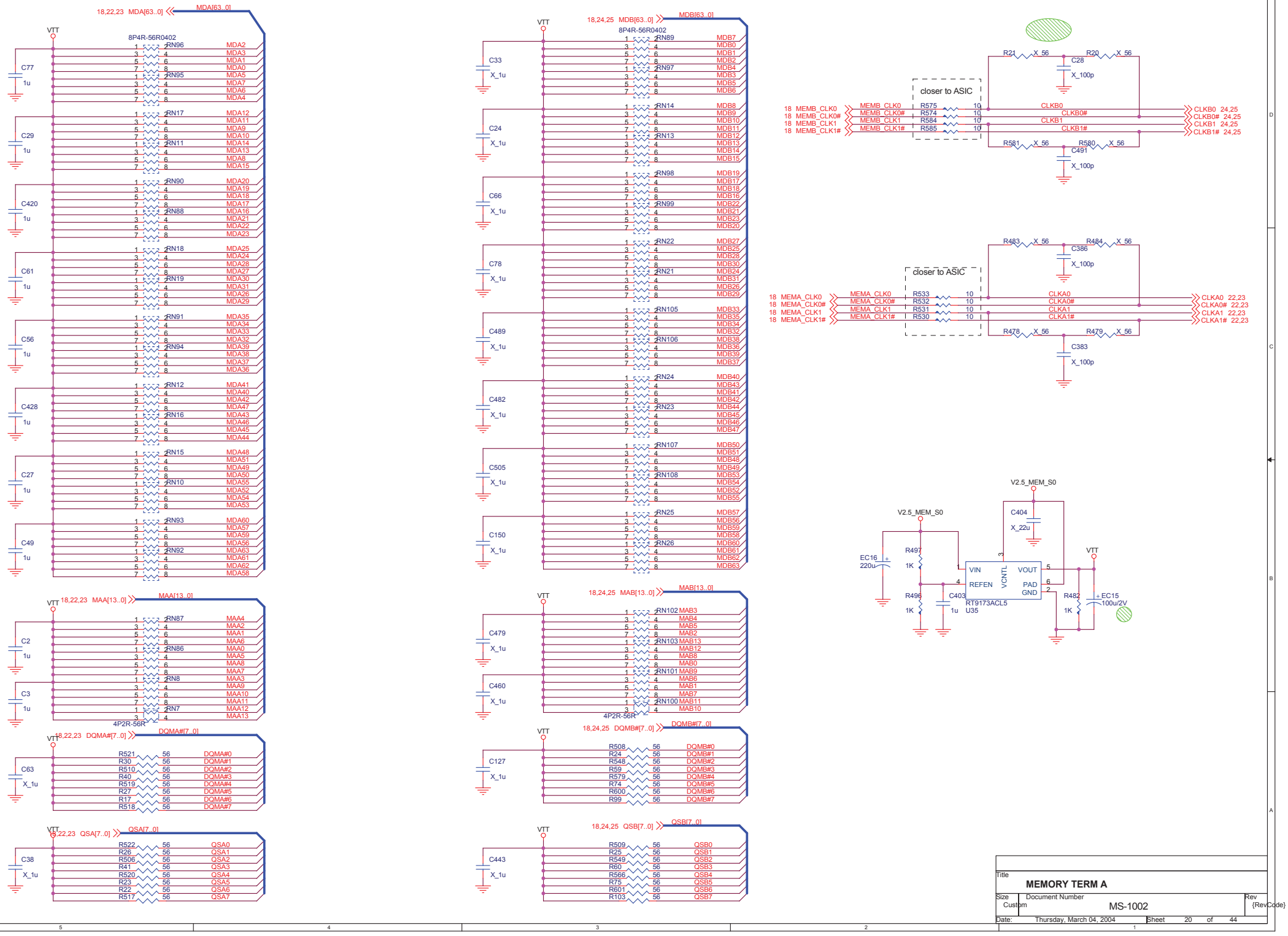
19
of
44


18,22,23 MDA[63..0]
MDA[63..0]
VTT
8P4R-56R0402
C77 1u
C29 1u
C420 1u
C61 1u
C56 1u
C428 1u
C27 1u
C49 1u
RN96 MDA2 MDA3 MDA1 MDA0
RN95 MDA5 MDA7 MDA6 MDA4
RN17 MDA12 MDA11 MDA9 MDA10
RN11 MDA14 MDA13 MDA8 MDA15
RN90 MDA20 MDA19 MDA18 MDA17
RN88 MDA16 MDA21 MDA22 MDA23
RN18 MDA25 MDA24 MDA28 MDA27
RN19 MDA30 MDA31 MDA26 MDA29
RN91 MDA35 MDA34 MDA33 MDA32
RN94 MDA39 MDA38 MDA37 MDA36
RN12 MDA41 MDA40 MDA42 MDA47
RN16 MDA43 MDA46 MDA45 MDA44
RN15 MDA48 MDA51 MDA49 MDA50
RN10 MDA55 MDA52 MDA54 MDA53
RN93 MDA60 MDA57 MDA59 MDA56
RN92 MDA63 MDA61 MDA62 MDA58
18,22,23 MAA[13..0]
MAA[13..0]
C2 1u
C3 1u
RN87 MAA4 MAA2 MAA1 MAA6
RN86 MAA0 MAA5 MAA8 MAA7
RN8 MAA3 MAA9 MAA10 MAA11
RN7 MAA12 MAA13
4P2R-56R
18,22,23 DQMA#[7..0]
DQMA#[7..0]
C63 X_1u
R521 R30 R510 R40 R519 R27 R17 R518
56 DQMA#0 DQMA#1 DQMA#2 DQMA#3 DQMA#4 DQMA#5 DQMA#6 DQMA#7
18,22,23 QSA[7..0]
QSA[7..0]
C38 X_1u
R522 R26 R506 R41 R520 R23 R22 R517
56 QSA0 QSA1 QSA2 QSA3 QSA4 QSA5 QSA6 QSA7
18,24,25 MDB[63..0]
MDB[63..0]
C33 X_1u
C24 X_1u
C66 X_1u
C78 X_1u
C489 X_1u
C482 X_1u
C505 X_1u
C150 X_1u
RN89 MDB7 MDB0 MDB1 MDB2
RN97 MDB4 MDB3 MDB5 MDB6
RN14 MDB8 MDB9 MDB10 MDB11
RN13 MDB12 MDB13 MDB14 MDB15
RN98 MDB19 MDB17 MDB18 MDB16
RN99 MDB22 MDB21 MDB23 MDB20
RN22 MDB27 MDB25 MDB28 MDB30
RN21 MDB24 MDB31 MDB26 MDB29
RN105 MDB33 MDB35 MDB34 MDB32
RN106 MDB38 MDB36 MDB39 MDB37
RN24 MDB40 MDB43 MDB41 MDB42
RN23 MDB44 MDB45 MDB46 MDB47
RN107 MDB50 MDB51 MDB48 MDB49
RN108 MDB53 MDB54 MDB52 MDB55
RN25 MDB57 MDB56 MDB59 MDB58
RN26 MDB60 MDB61 MDB62 MDB63
18,24,25 MAB[13..0]
MAB[13..0]
C479 X_1u
C460 X_1u
RN102 MAB3 MAB4 MAB5 MAB2
RN103 MAB13 MAB12 MAB8 MAB0
RN101 MAB9 MAB6 MAB1 MAB7
RN100 MAB11 MAB10
4P2R-56R
18,24,25 DQMB#[7..0]
DQMB#[7..0]
C127 X_1u
R508 R24 R548 R59 R579 R74 R600 R99
56 DQMB#0 DQMB#1 DQMB#2 DQMB#3 DQMB#4 DQMB#5 DQMB#6 DQMB#7
18,24,25 QSB[7..0]
QSB[7..0]
C443 X_1u
R509 R25 R549 R60 R566 R75 R601 R103
56 QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7
closer to ASIC
18 MEMB_CLK0
18 MEMB_CLK0#
18 MEMB_CLK1
18 MEMB_CLK1#
MEMB_CLK0 MEMB_CLK0# MEMB_CLK1 MEMB_CLK1#
R575 R574 R584 R585 10
CLKB0 CLKB0# CLKB1 CLKB1#
CLKB0 24,25
CLKB0# 24,25
CLKB1 24,25
CLKB1# 24,25
R21 X 56
R20 X 56
C28 X_100p
R581 X 56
R580 X 56
C491 X_100p
closer to ASIC
18 MEMA_CLK0
18 MEMA_CLK0#
18 MEMA_CLK1
18 MEMA_CLK1#
MEMA_CLK0 MEMA_CLK0# MEMA_CLK1 MEMA_CLK1#
R533 R532 R531 R530 10
CLKA0 CLKA0# CLKA1 CLKA1#
CLKA0 22,23
CLKA0# 22,23
CLKA1 22,23
CLKA1# 22,23
R483 X 56
R484 X 56
C386 X_100p
R478 X 56
R479 X 56
C383 X_100p
V2.5_MEM_S0
C404 X_22u
EC16 220u
R497 1K
R496 1K
C403 1u
RT9173ACL5
U35
VIN REFEN VCNTL VOUT PAD GND
R482 1K
EC15 100u/2V
VTT
Title
MEMORY TERM A
Size Custom
Document Number MS-1002
Rev {RevCode}
Date: Thursday, March 04, 2004
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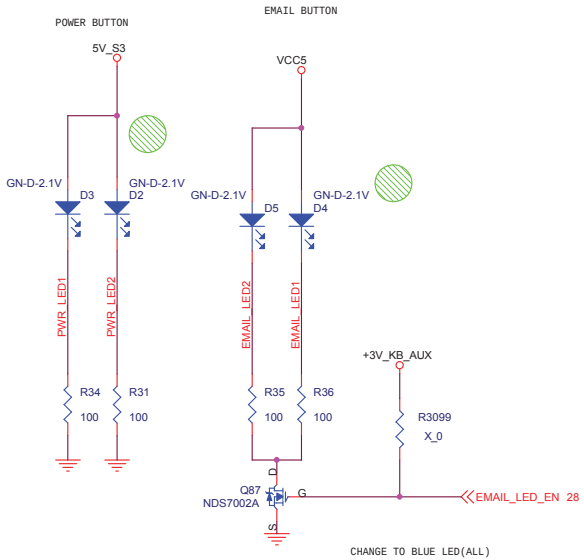
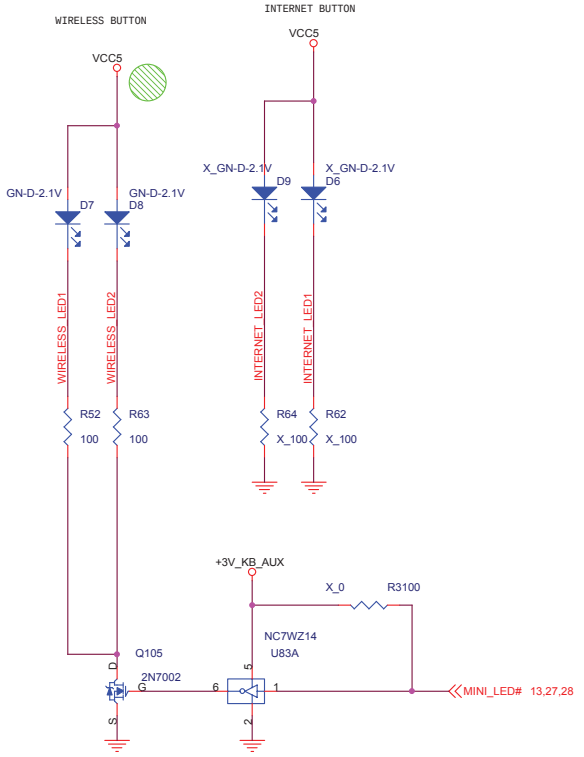
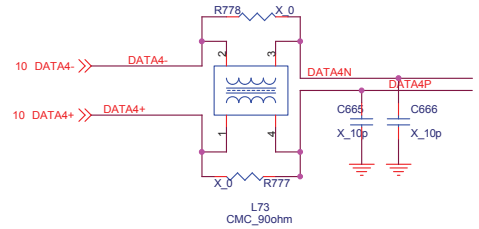
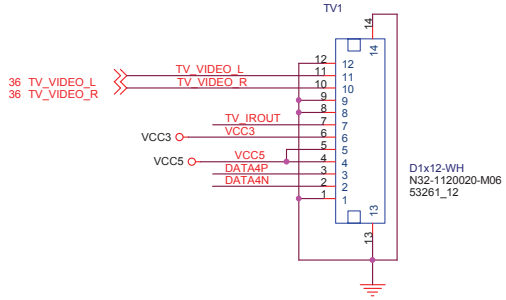
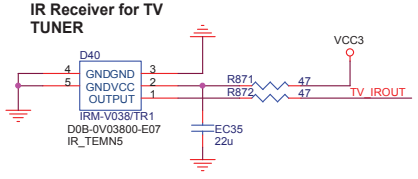


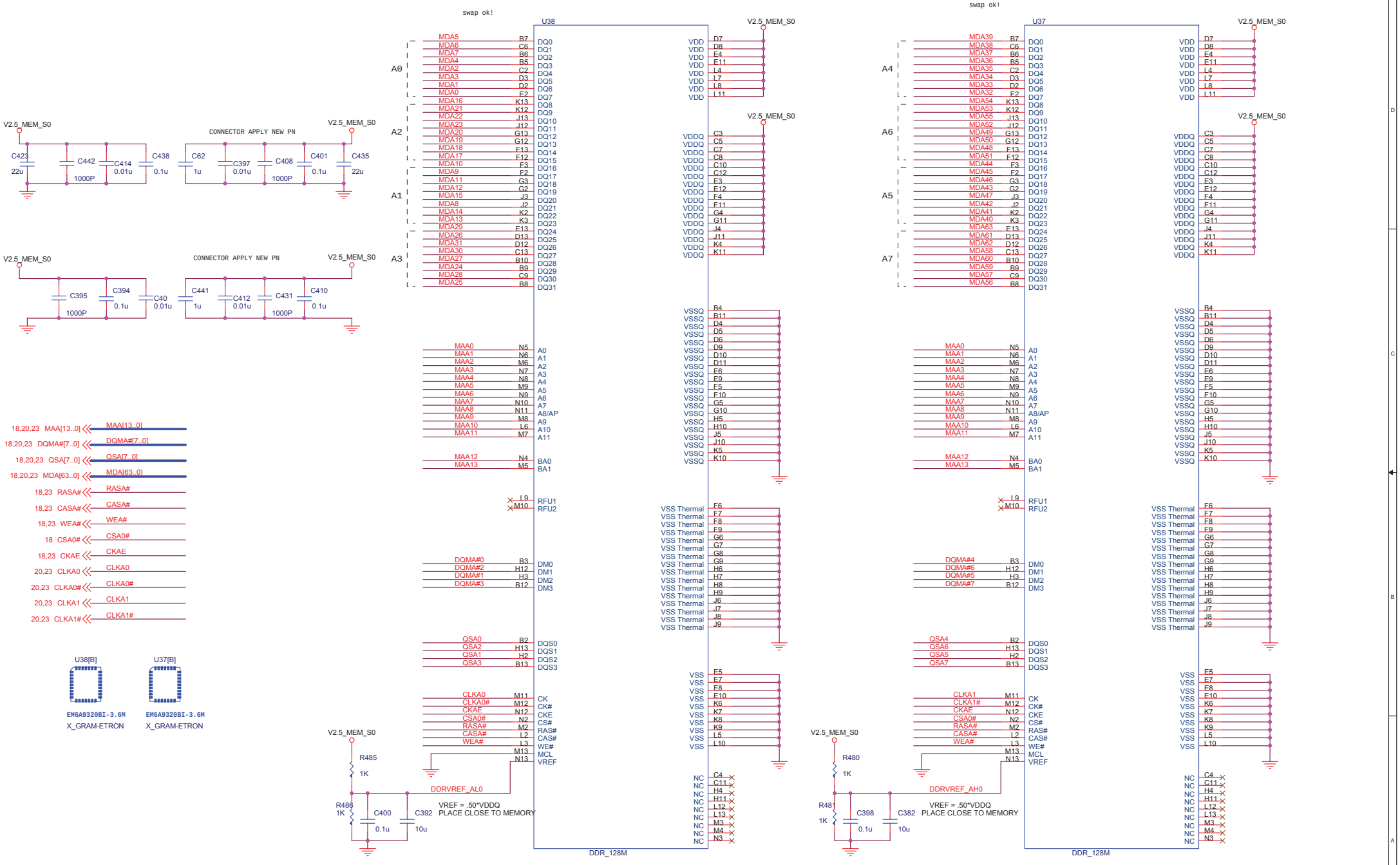








Title	MEMORY TERM B / BUTTON LED	
Size: Custom	Document Number: MS-1002	Rev: {RevCode}
Date: Thursday, March 04, 2004	Sheet 21 of 44	



	64MB	128MB
CSA0	V	V
CSA1	X	V
CSB0	V	V
CSB1	X	V

	4M * 32	8M * 32
Hynix	8 pieces	X
Samsung	8 pieces	8 pieces
Etron	8 pieces	8 pieces

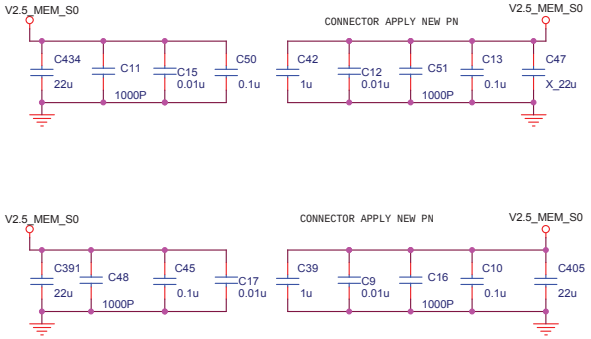
4MX32 DDR FBGA MEMORY

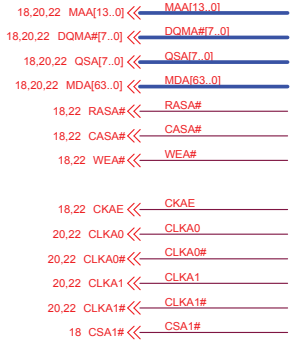
Title: **144 PIN DDR 4M/8M X 32 FBGA A0**

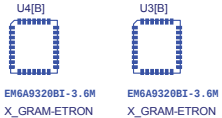
Size	Document Number	Rev
Custom	MS-1002	{RevCode}

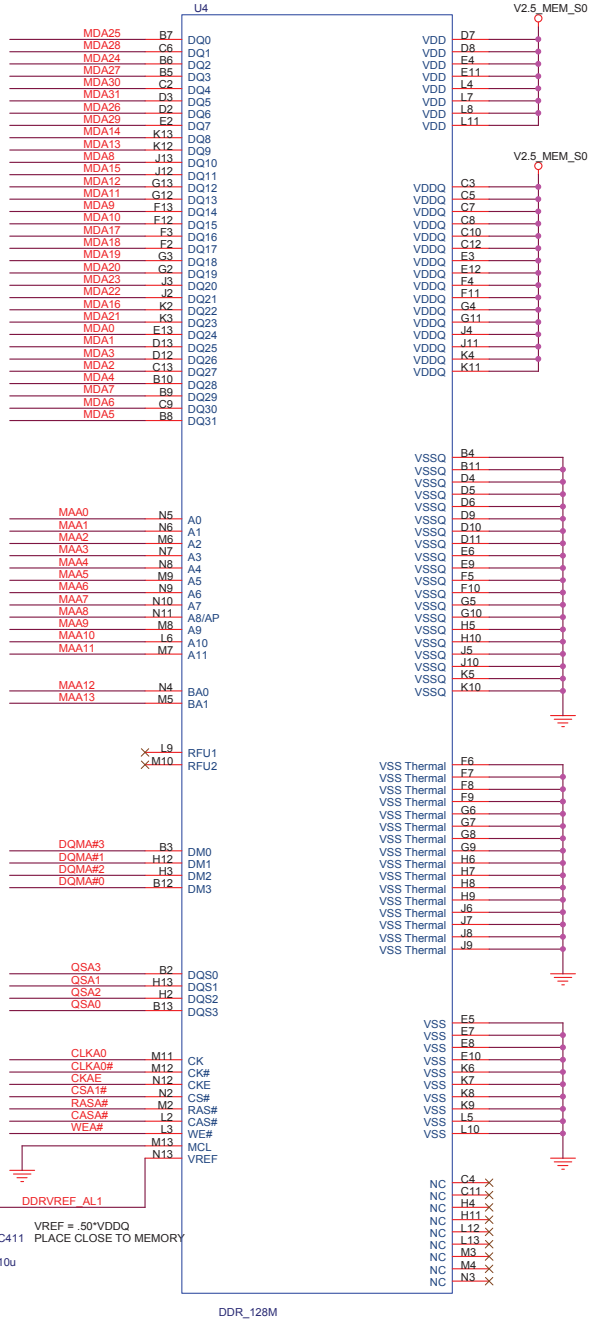
Date: Wednesday, March 03, 2004 Sheet 22 of 44

This Page compaments are uninstalled if SGRAM is 64MB

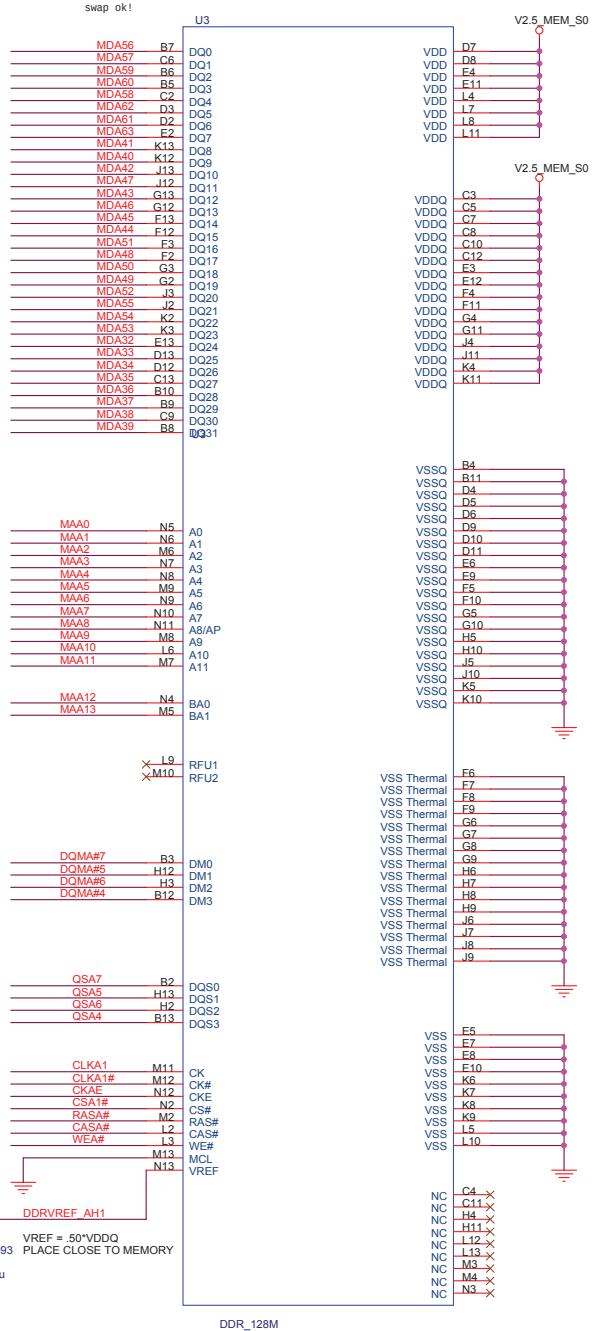




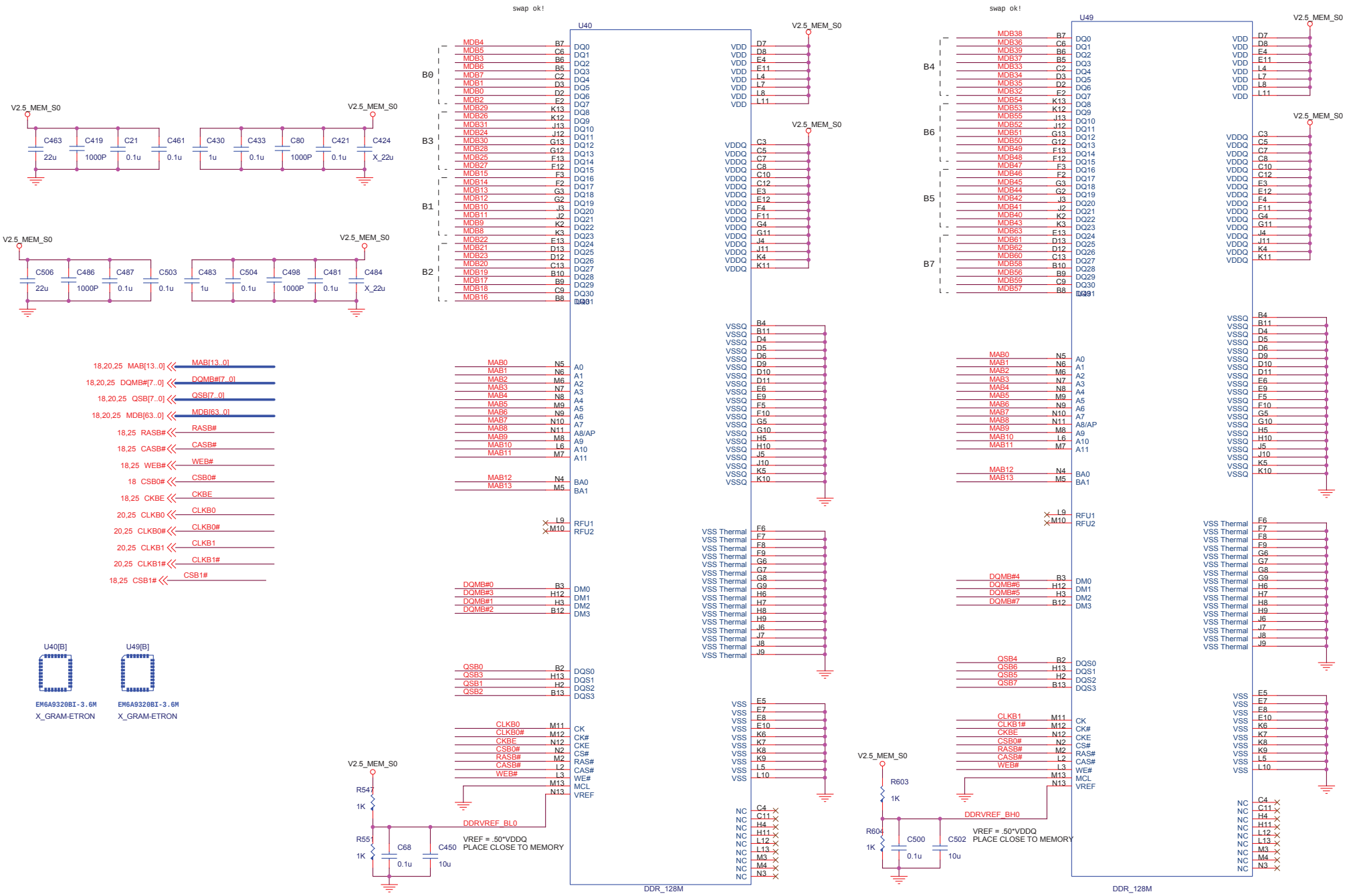




swap ok!



Title	4MX32 DDR FBGA MEMORY
	144 PIN DDR 4M/8M X 32 FBGA A1
Size: Custom	Document Number: MS-1002
Rev: {RevCode}	
Date: Wednesday, March 03, 2004	Sheet 23 of 44



Title	4MX32 DDR FBGA MEMORY
	144 PIN DDR 4M/8M X 32 FBGA B0
Size	Custom
Document Number	MS-1002
Rev	{RevCode}
Date:	Wednesday, March 03, 2004
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This Page compnents are uninstalled if SGRAM is 64MB

swap ok!

U6

U12

V2.5_MEM_S0

C20 22u, C79 1000P, C76 0.1u, C58 0.1u, C30 1u, C34 0.1u, C32 1000P, C64 0.1u, C19 X_22u

C508 22u, C499 1000P, C152 0.1u, C126 0.1u, C93 1u, C94 0.1u, C151 1000P, C114 0.1u, C476 X_22u

18,20,24 MAB[13..0]
18,20,24 DQMB#[7..0]
18,24 QSB[7..0]
18,24 MDB[63..0]
18,24 RASB#
18,24 CASB#
18,24 WEB#
18,24 CKBE
20,24 CLKB0
20,24 CLKB0#
20,24 CLKB1
20,24 CLKB1#
18 CSB1#

U6[B] EM6A9320BI-3.6M X_GRAM-ETRON

U12[B] EM6A9320BI-3.6M X_GRAM-ETRON

R503 1K, R500 1K, C31 0.1u, C417 10u

DDRVREF_BL1

VREF = .50*VDDQ PLACE CLOSE TO MEMORY

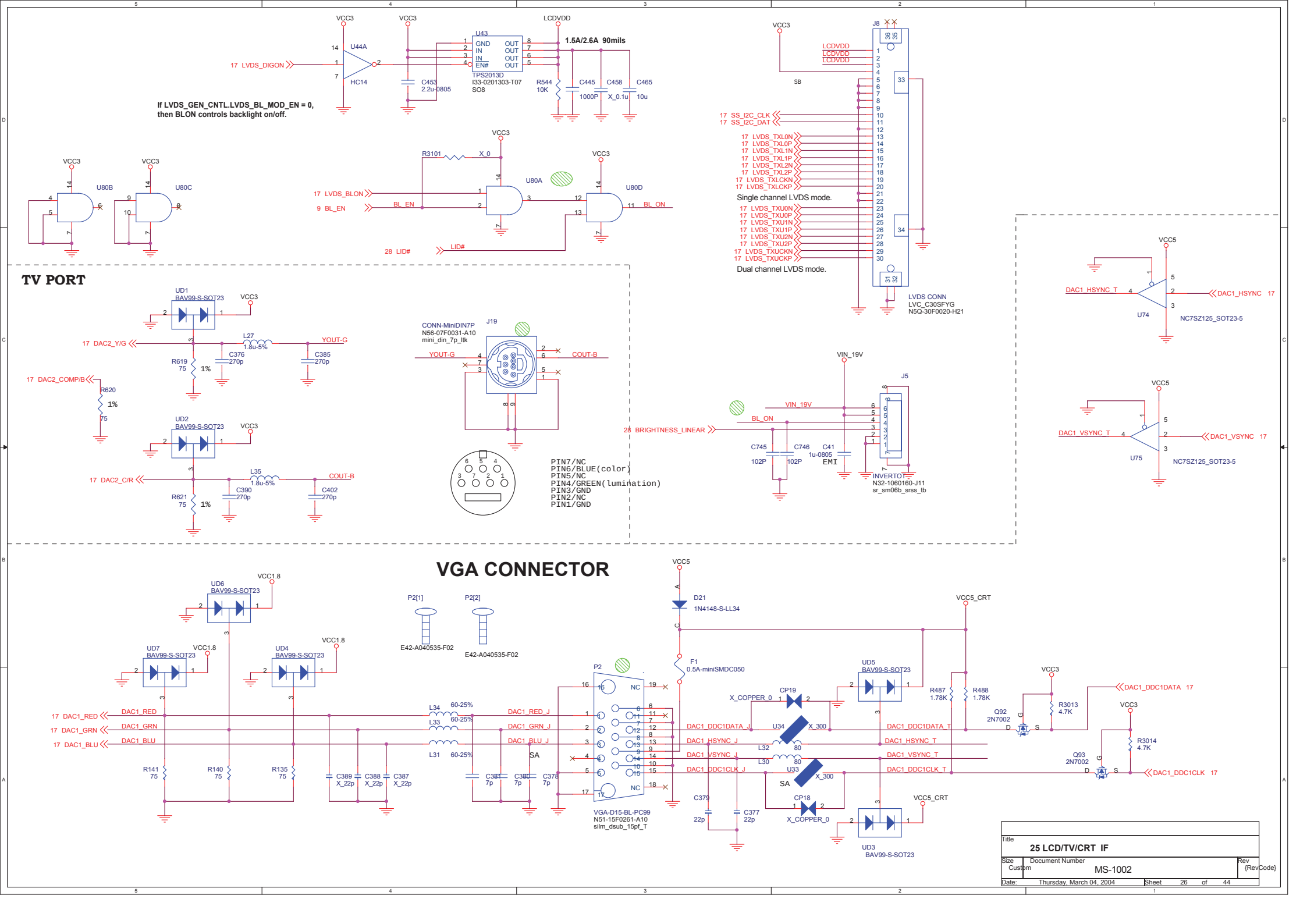
R76 1K, R79 1K, C107 0.1u, C109 10u

DDRVREF_BH1

VREF = .50*VDDQ PLACE CLOSE TO MEMORY

DDR_128M

Title	4MX32 DDR FBGA MEMORY
	144 PIN DDR 4M/8M X 32 FBGA B1
Size: Custom	Document Number: MS-1002
Rev	{RevCode}
Date: Wednesday, March 03, 2004	Sheet 25 of 44


VCC3
U44A
HC14
17 LVDS_DIGON
C453
2.2u-0805
U43
GND
IN
IN
EN#
OUT
OUT
OUT
OUT
TPS2013D
I33-0201303-T07
SO8
LCDVDD
1.5A/2.6A 90mils
R544
10K
C445
1000P
C458
X_0.1u
C465
10u
If LVDS_GEN_CNTL.LVDS_BL_MOD_EN = 0,
then BLON controls backlight on/off.
U80B
U80C
R3101
X_0
U80A
U80D
17 LVDS_BLON
9 BL_EN
BL_EN
BL_ON
28 LID#
LID#
J8
SB
17 SS_I2C_CLK
17 SS_I2C_DAT
17 LVDS_TXL0N
17 LVDS_TXL0P
17 LVDS_TXL1N
17 LVDS_TXL1P
17 LVDS_TXL2N
17 LVDS_TXL2P
17 LVDS_TXLCKN
17 LVDS_TXLCKP
Single channel LVDS mode.
17 LVDS_TXU0N
17 LVDS_TXU0P
17 LVDS_TXU1N
17 LVDS_TXU1P
17 LVDS_TXU2N
17 LVDS_TXU2P
17 LVDS_TXUCKN
17 LVDS_TXUCKP
Dual channel LVDS mode.
LVDS CONN
LVC_C30SFYG
N5Q-30F0020-H21
TV PORT
UD1
BAV99-S-SOT23
17 DAC2_Y/G
L27
1.8u-5%
YOUT-G
C376
270p
C385
270p
R619
75
1%
17 DAC2_COMP/B
R620
UD2
17 DAC2_C/R
L35
COUT-B
C390
C402
R621
J19
CONN-MiniDIN7P
N56-07F0031-A10
mini_din_7p_ltk
PIN7/NC
PIN6/BLUE(color)
PIN5/NC
PIN4/GREEN(lumination)
PIN3/GND
PIN2/NC
PIN1/GND
VIN_19V
J5
28 BRIGHTNESS_LINEAR
C745
102P
C746
C41
1u-0805
EMI
INVERTOT
N32-1060160-J11
sr_sm06b_srss_tb
VCC5
U74
DAC1_HSYNC_T
DAC1_HSYNC 17
NC7SZ125_SOT23-5
U75
DAC1_VSYNC_T
DAC1_VSYNC 17
VGA CONNECTOR
P2[1]
P2[2]
E42-A040535-F02
D21
1N4148-S-LL34
F1
0.5A-miniSMDC050
VCC5_CRT
UD6
VCC1.8
UD7
UD4
17 DAC1_RED
17 DAC1_GRN
17 DAC1_BLU
DAC1_RED
DAC1_GRN
DAC1_BLU
L34
L33
L31
60-25%
R141
R140
R135
75
C389
C388
C387
X_22p
DAC1_RED_J
DAC1_GRN_J
DAC1_BLU_J
SA
C381
C380
C378
7p
P2
NC
VGA-D15-BL-PC99
N51-15F0261-A10
silm_dsub_15pf_T
DAC1_DDC1DATA_J
DAC1_HSYNC_J
DAC1_VSYNC_J
DAC1_DDC1CLK_J
C379
22p
C377
22p
X_COPPER_0
CP19
CP18
UD5
UD3
U34
U33
X_300
L32
L30
80
DAC1_DDC1DATA_T
DAC1_HSYNC_T
DAC1_VSYNC_T
DAC1_DDC1CLK_T
R487
1.78K
R488
1.78K
Q92
2N7002
Q93
R3013
4.7K
R3014
4.7K
DAC1_DDC1DATA 17
DAC1_DDC1CLK 17
Title
25 LCD/TV/CRT IF
Size
Custom
Document Number
MS-1002
Rev
{RevCode}
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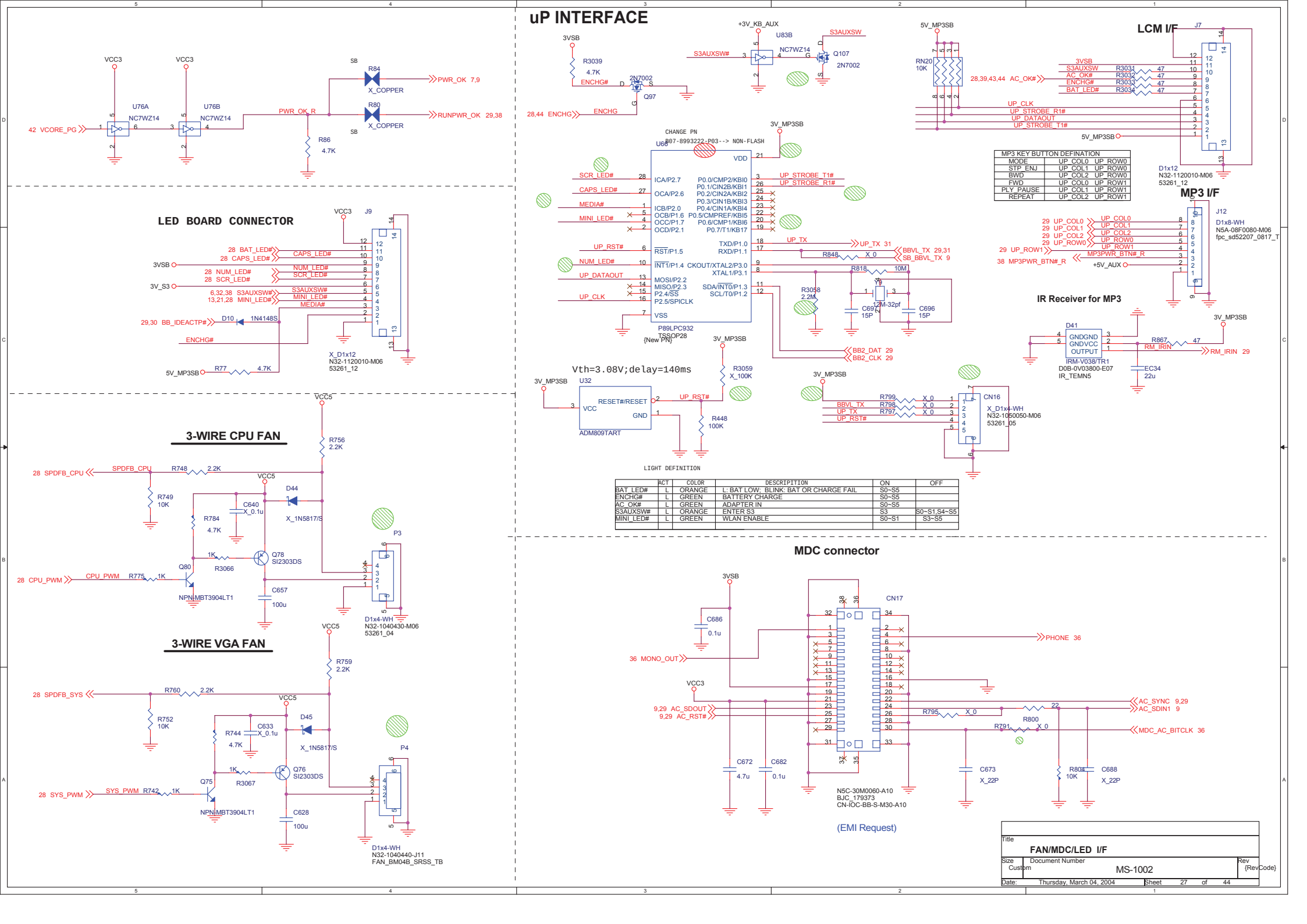
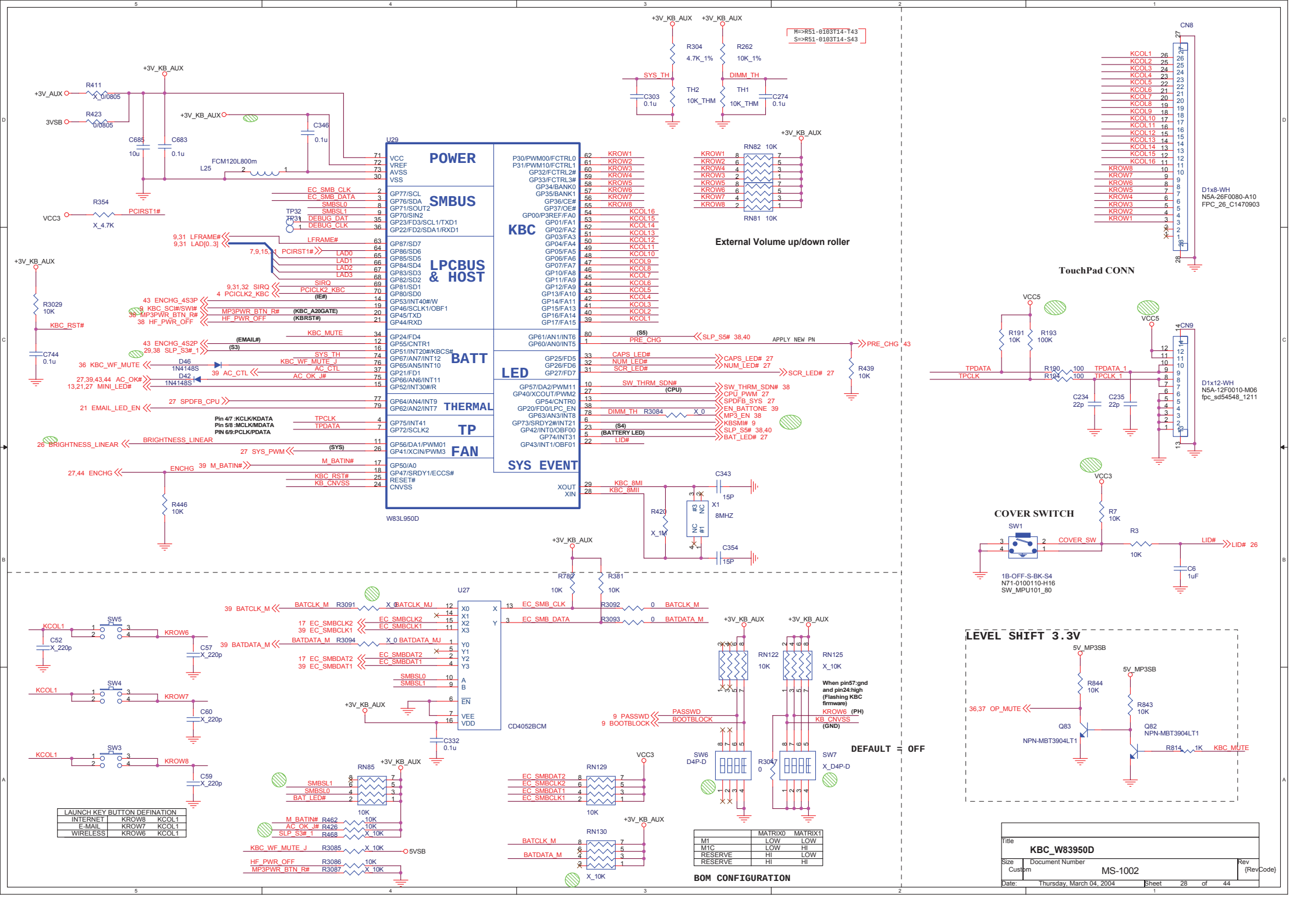

uP INTERFACE
LCM I/F
MP3 I/F
LED BOARD CONNECTOR
3-WIRE CPU FAN
3-WIRE VGA FAN
IR Receiver for MP3
MDC connector
CHANGE PN
P89LPC932
TSSOP28
{New PN}
Vth=3.08V;delay=140ms
ADM809TART
LIGHT DEFINITION
MP3 KEY BUTTON DEFINATION
N5C-30M0060-A10
BJC_179373
CN-IOC-BB-S-M30-A10
(EMI Request)
FAN/MDC/LED I/F
MS-1002
Thursday, March 04, 2004


U29
POWER
VCC
VREF
AVSS
VSS
SMBUS
GP77/SCL
GP76/SDA
GP71/SOUT2
GP70/SIN2
GP23/FD3/SCL1/TXD1
GP22/FD2/SDA1/RXD1
LPCBUS & HOST
GP87/SD7
GP86/SD6
GP85/SD5
GP84/SD4
GP83/SD3
GP82/SD2
GP81/SD1
GP80/SD0
GP53/INT40#/W
GP46/SCLK1/OBF1
GP45/TXD
GP44/RXD
BATT
GP24/FD4
GP55/CNTR1
GP51/INT20#/KBCS#
GP67/AN7/INT12
GP65/AN5/INT10
GP21/FD1
GP66/AN6/INT11
GP52/INT30#/R
THERMAL
GP64/AN4/INT9
GP62/AN2/INT7
TP
GP75/INT41
GP72/SCLK2
FAN
GP56/DA1/PWM01
GP41/XCIN/PWM3
SYS_EVENT
GP50/A0
GP47/SRDY1/ECCS#
RESET#
CNVSS
KBC
P30/PWM00/FCTRL0
P31/PWM10/FCTRL1
GP32/FCTRL2#
GP33/FCTRL3#
GP34/BANK0
GP35/BANK1
GP36/CE#
GP37/OE#
GP00/P3REF/FA0
GP01/FA1
GP02/FA2
GP03/FA3
GP04/FA4
GP05/FA5
GP06/FA6
GP07/FA7
GP10/FA8
GP11/FA9
GP12/FA9
GP13/FA10
GP14/FA11
GP15/FA13
GP16/FA14
GP17/FA15
LED
GP61/AN1/INT6
GP60/AN0/INT5
GP25/FD5
GP26/FD6
GP27/FD7
GP57/DA2/PWM11
GP40/XCOUT/PWM2
GP54/CNTR0
GP20/FD0/LPC_EN
GP63/AN3/INT8
GP73/SRDY2#/INT21
GP42/INT0/OBF00
GP74/INT31
GP43/INT1/OBF01
XOUT
XIN
W83L950D
+3V_KB_AUX
+3V_AUX
3VSB
VCC3
R411
X_0/0805
R423
0/0805
C685
10u
C683
0.1u
C346
0.1u
FCM120L800m
L25
R354
X_4.7K
PCIRST1#
TP32
TP31
DEBUG_DAT
DEBUG_CLK
EC_SMB_CLK
EC_SMB_DATA
SMBSL0
SMBSL1
LFRAME#
LAD0
LAD1
LAD2
LAD3
SIRQ
PCICLK2_KBC
(IE#)
MP3PWR_BTN_R#
(KBC_A20GATE)
HF_PWR_OFF
(KBRST#)
KBC_MUTE
(EMAIL#)
(S3)
SYS_TH
KBC_WF_MUTE_J
AC_CTL
AC_OK_J#
D46
1N4148S
D42
1N4148S
SPDFB_CPU
EMAIL_LED_EN
Pin 4/7 :KCLK/KDATA
Pin 5/8 :MCLK/MDATA
PIN 6/9:PCLK/PDATA
TPCLK
TPDATA
BRIGHTNESS_LINEAR
SYS_PWM
(SYS)
M_BATIN#
ENCHG
KBC_RST#
KB_CNVSS
R3029
10K
KBC_RST#
C744
0.1u
R446
10K
R304
4.7K_1%
R262
10K_1%
M=>R51-0103T14-T43
S=>R51-0103T14-S43
SYS_TH
TH2
10K_THM
DIMM_TH
TH1
10K_THM
C303
0.1u
C274
0.1u
RN82 10K
RN81 10K
External Volume up/down roller
KROW1
KROW2
KROW3
KROW4
KROW5
KROW6
KROW7
KROW8
KCOL16
KCOL15
KCOL14
KCOL13
KCOL12
KCOL11
KCOL10
KCOL9
KCOL8
KCOL7
KCOL6
KCOL5
KCOL4
KCOL3
KCOL2
KCOL1
PRE_CHG
SLP_S5# 38,40
APPLY NEW PN
CAPS_LED#
NUM_LED#
SCR_LED#
R439
10K
SW_THRM_SDN#
(CPU)
CPU_PWM 27
SPDFB_SYS 27
EN_BATTONE 39
MP3_EN 38
KBSNI# 9
SLP_S5# 38,40
BAT_LED# 27
(S4)
(BATTERY LED)
LID#
C343
15P
X1
8MHZ
C354
15P
R420
X_1M
CN8
D1x8-WH
N5A-26F0080-A10
FPC_26_C1470903
TouchPad CONN
VCC5
R191
10K
R193
100K
TPDATA
TPCLK
R190
100
R194
100
TPDATA_1
TPCLK_1
C234
22p
C235
22p
CN9
D1x12-WH
N5A-12F0010-M06
fpc_sd54548_1211
COVER SWITCH
SW1
COVER_SW
R7
10K
R3
10K
LID#
LID# 26
C6
1uF
1B-OFF-S-BK-S4
N71-0100110-H16
SW_MPU101_80
R780
10K
R381
10K
U27
CD4052BCM
BATCLK_M
BATDATA_M
EC_SMBCLK2
EC_SMBCLK1
EC_SMBDAT2
EC_SMBDAT1
EC_SMB_CLK
EC_SMB_DATA
R3091
R3092
R3093
R3094
C332
0.1u
SW5
SW4
SW3
KCOL1
KROW6
KROW7
KROW8
C52
X_220p
C57
X_220p
C60
X_220p
C59
X_220p
LAUNCH KEY BUTTON DEFINATION
INTERNET KROW8 KCOL1
E-MAIL KROW7 KCOL1
WIRELESS KROW6 KCOL1
RN85
SMBSL1
SMBSL0
BAT_LED#
M_BATIN# R462
AC_OK_J# R426
SLP_S3#_1 R468
10K
KBC_WF_MUTE_J R3085
HF_PWR_OFF R3086
MP3PWR_BTN_R# R3087
X_10K
5VSB
RN129
RN130
RN122
RN125
10K
X_10K
When pin57:gnd and pin24:high (Flashing KBC firmware)
PASSWD
BOOTBLOCK
KB_CNVSS
(GND)
KROW6 (PH)
SW6
D4P-D
SW7
X_D4P-D
R3047
0
DEFAULT = OFF
MATRIX0 MATRIX1
M1 LOW LOW
M1C LOW HI
RESERVE HI LOW
RESERVE HI HI
BOM CONFIGURATION
LEVEL SHIFT 3.3V
5V_MP3SB
R844
10K
R843
10K
OP_MUTE
Q83
NPN-MBT3904LT1
Q82
NPN-MBT3904LT1
R814
1K
KBC_MUTE
Title
KBC_W83950D
Size
Custom
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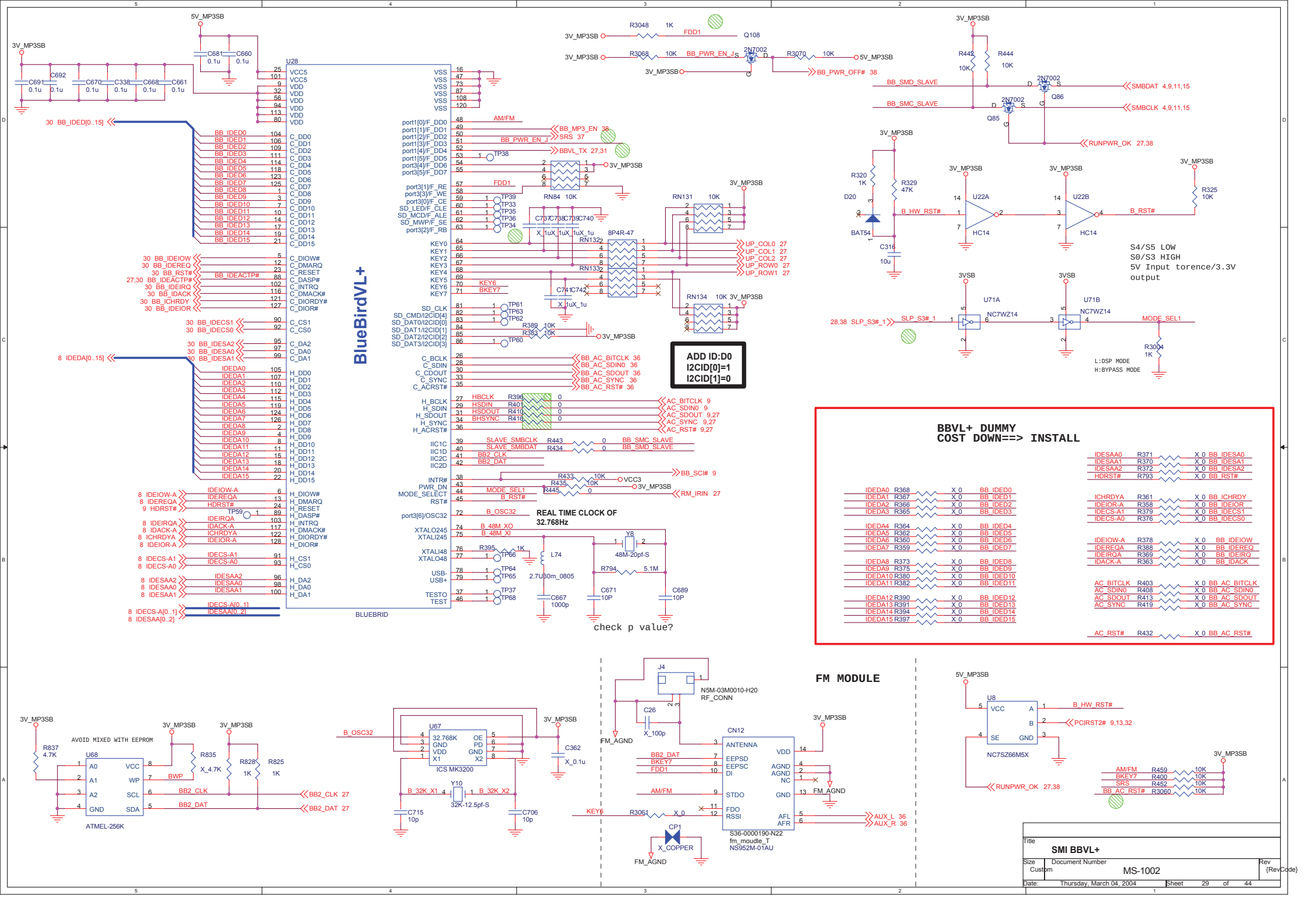
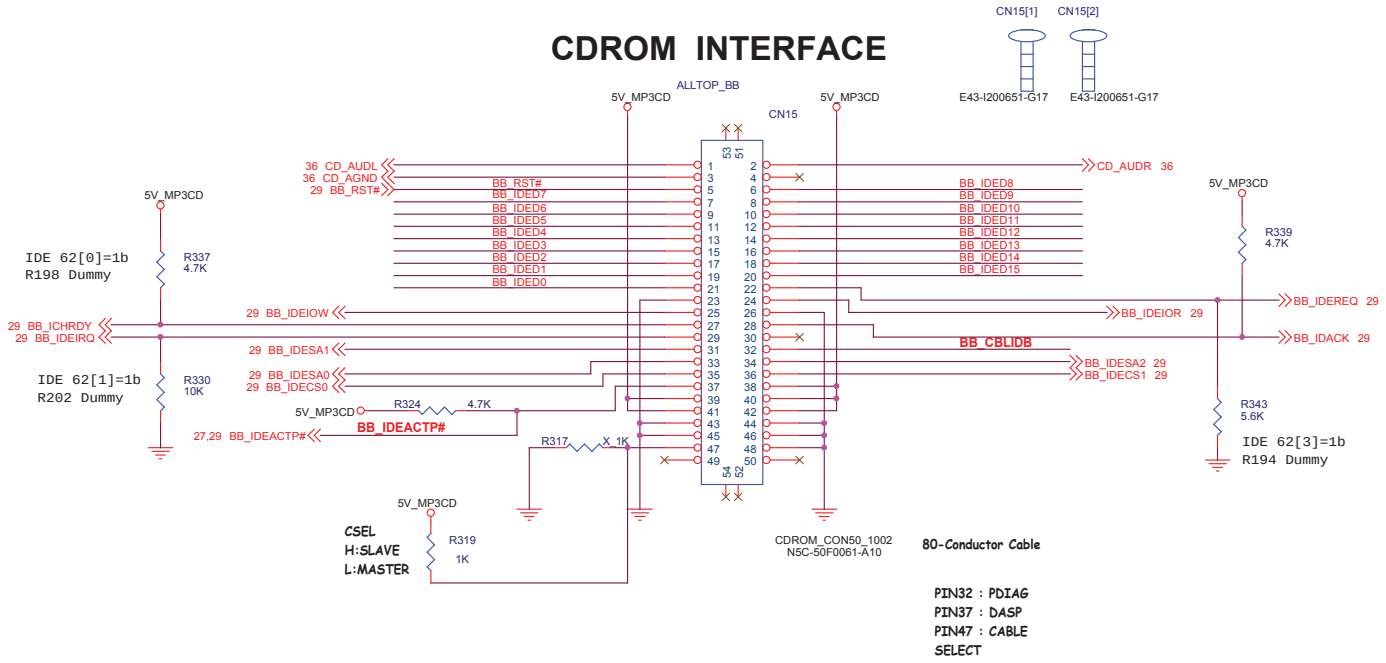
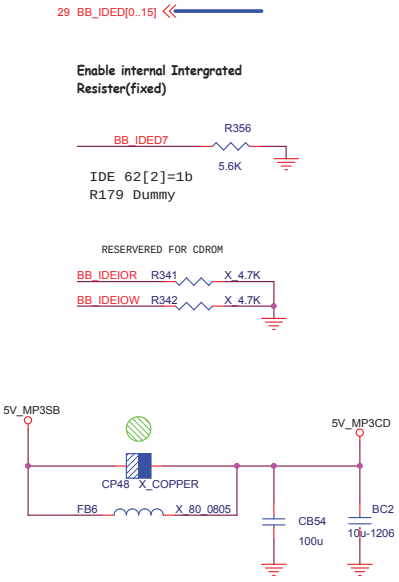
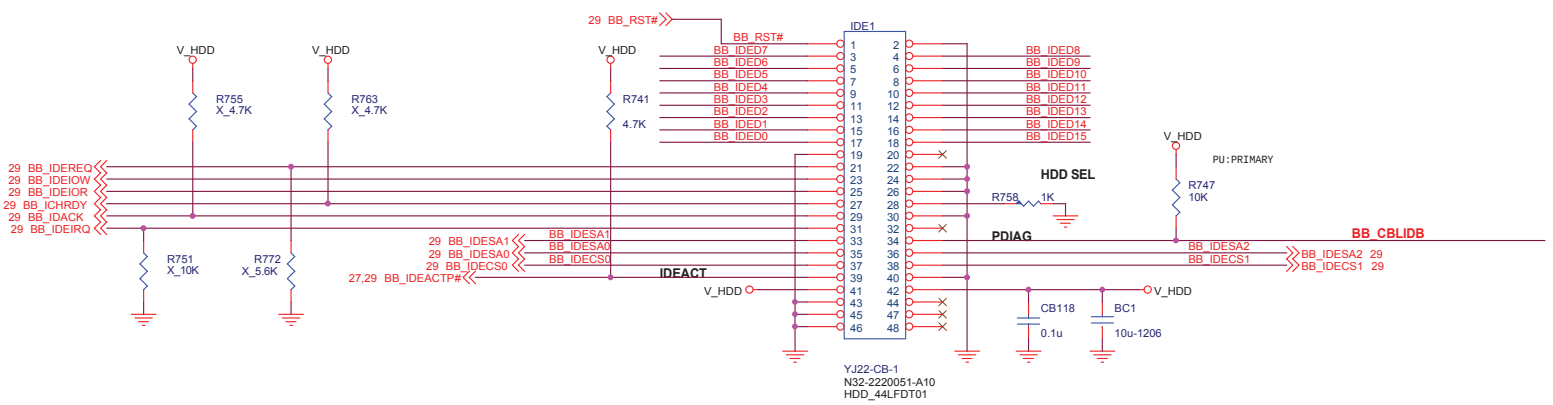

BlueBirdVL+
BLUEBIRD
U28
ADD ID:D0
I2CID[0]=1
I2CID[1]=0
REAL TIME CLOCK OF
32.768Hz
check p value?
BBVL+ DUMMY
COST DOWN==> INSTALL
FM MODULE
S4/S5 LOW
S0/S3 HIGH
5V Input torence/3.3V
output
L:DSP MODE
H:BYPASS MODE
AVOID MIXED WITH EEPROM
ATMEL-256K
ICS MK3200
N5M-03M0010-H20
RF_CONN
S36-0000190-N22
fm_moudle_T
NS952M-01AU
NC7SZ66M5X
SMI BBVL+
MS-1002
Thursday, March 04, 2004

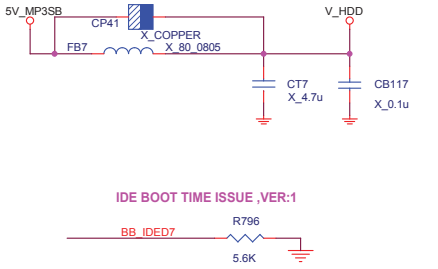
CDROM INTERFACE





HDD INTERFACE





Title	CDROM/HDD	
Size: Custom	Document Number: MS-1002	Rev: {RevCode}
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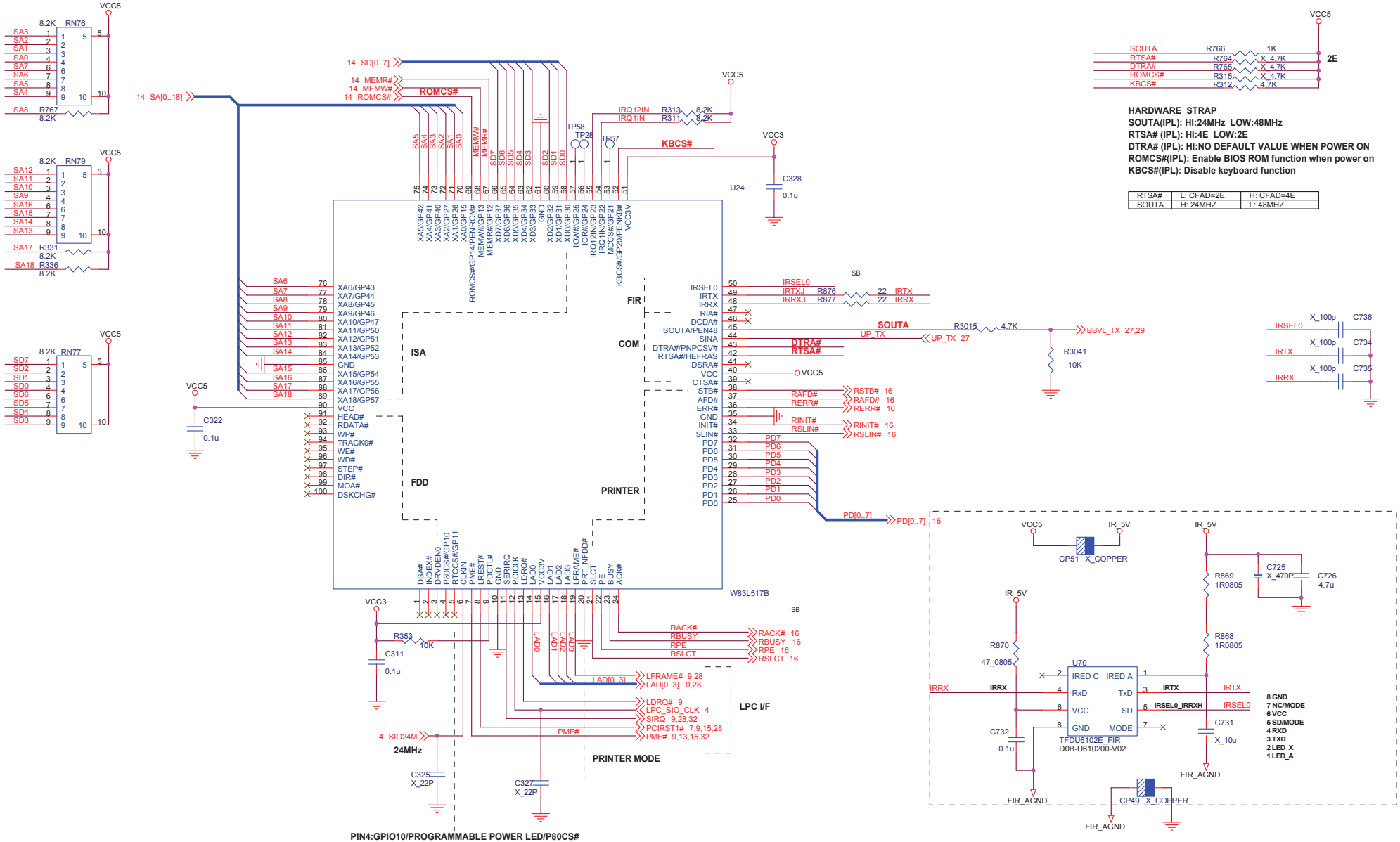
HARDWARE STRAP
SOUTA(IPL): HI:24MHz LOW:48MHz
RTSA# (IPL): HI:4E LOW:2E
DTRA# (IPL): HI:NO DEFAULT VALUE WHEN POWER ON
ROMCS#(IPL): Enable BIOS ROM function when power on
KBCS#(IPL): Disable keyboard function
RTSA# L: CFAD=2E H: CFAD=4E
SOUTA H: 24MHZ L: 48MHZ
W83L517B
ISA
FDD
FIR
COM
PRINTER
LPC I/F
PRINTER MODE
24MHz
PIN4:GPIO10/PROGRAMMABLE POWER LED/P80CS#
PIN5:GPIO11/WATCH DOG TIMER/RTCCS#
TFDU6102E_FIR
D0B-U610200-V02
8 GND
7 NC/MODE
6 VCC
5 SD/MODE
4 RXD
3 TXD
2 LED_X
1 LED_A
W83L517 SIO
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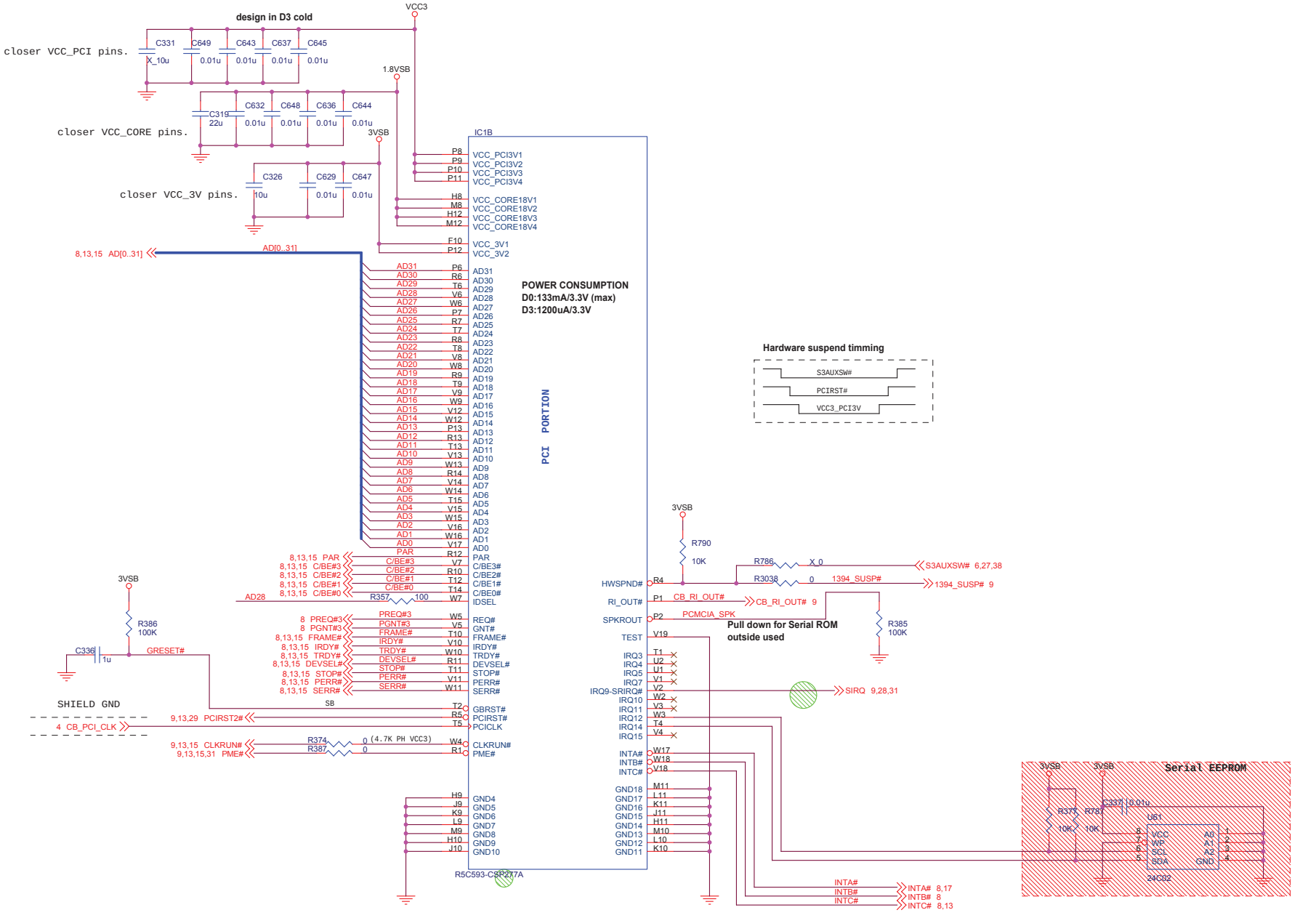

Title	P1 5C593/PCI	
Size: Custom	Document Number: MS-1002	Rev: {RevCode}
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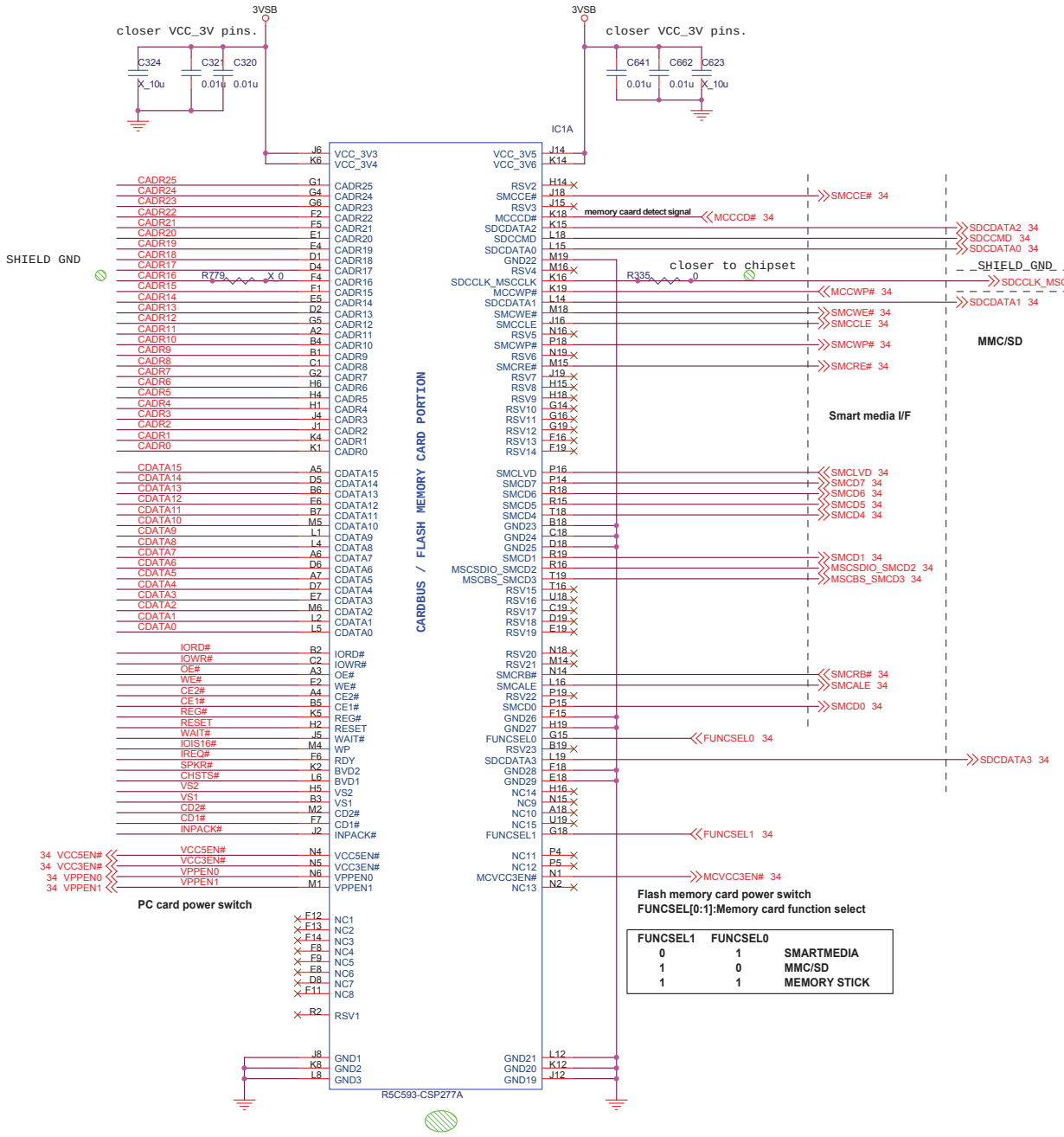
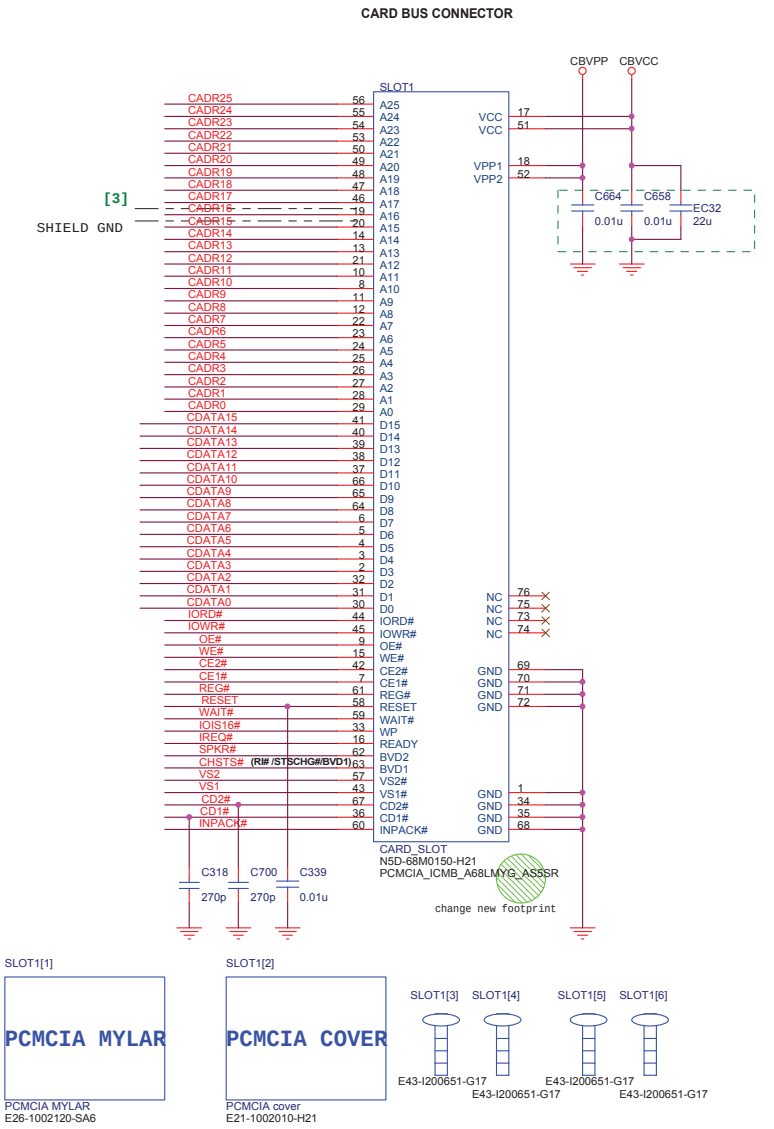
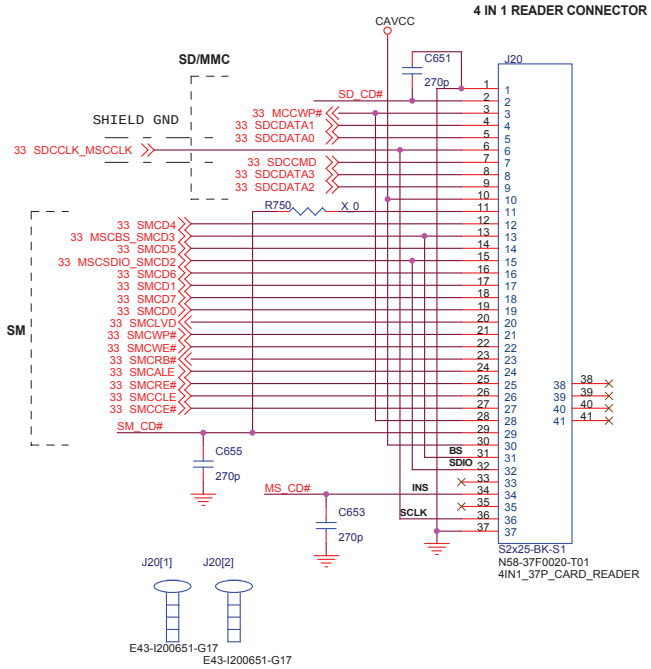
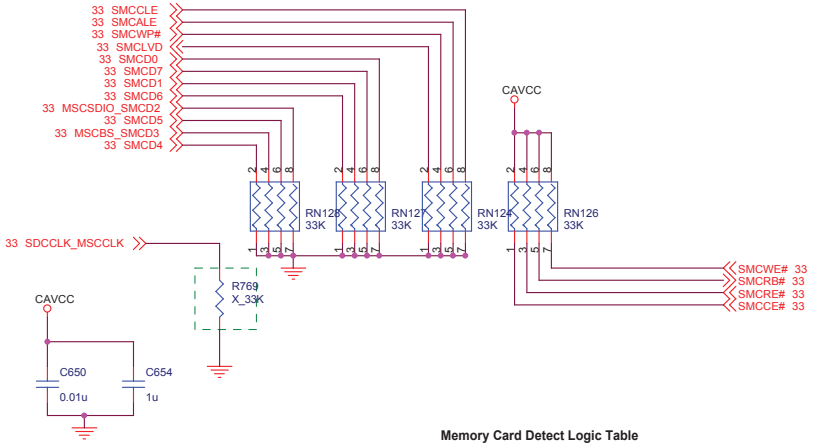


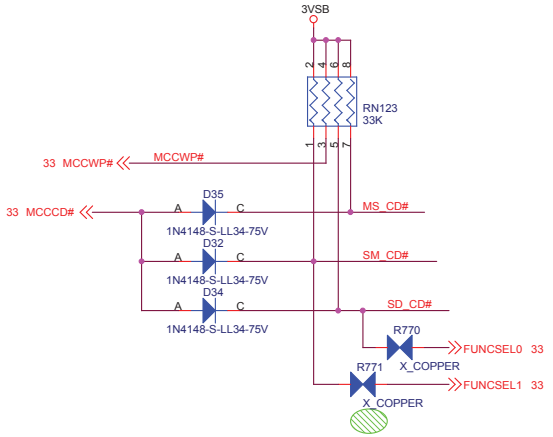
FUNCSEL1	FUNCSEL0	
0	1	SMARTMEDIA
1	0	MMC/SD
1	1	MEMORY STICK



Title	P2 5C593/CARDBUS/FLASH_MEMOR		
Size: Custom	Document Number: MS-1002		Rev: {RevCode}
Date: Thursday, March 04, 2004	Sheet 33 of 44		

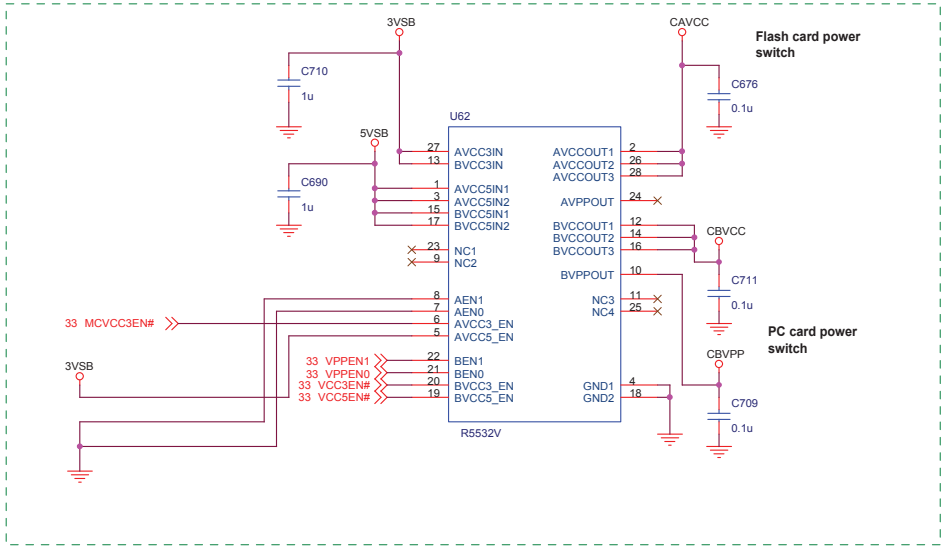






Memory Card Detect Logic Table

MS_CD#	SM_CD#	SD_CD#	->	Detected Card
0	0	0		X
0	0	1		X
0	1	0		X
0	1	1	->	MemoryStick Detected
1	0	0		X
1	0	1	->	SmartMedia Detected
1	1	0	->	SD/MMC Detected
1	1	1	->	Not Detected



Title	P4 FLASH_CARD_SLOT/CRT	
Size	Document Number MS-1002	Rev
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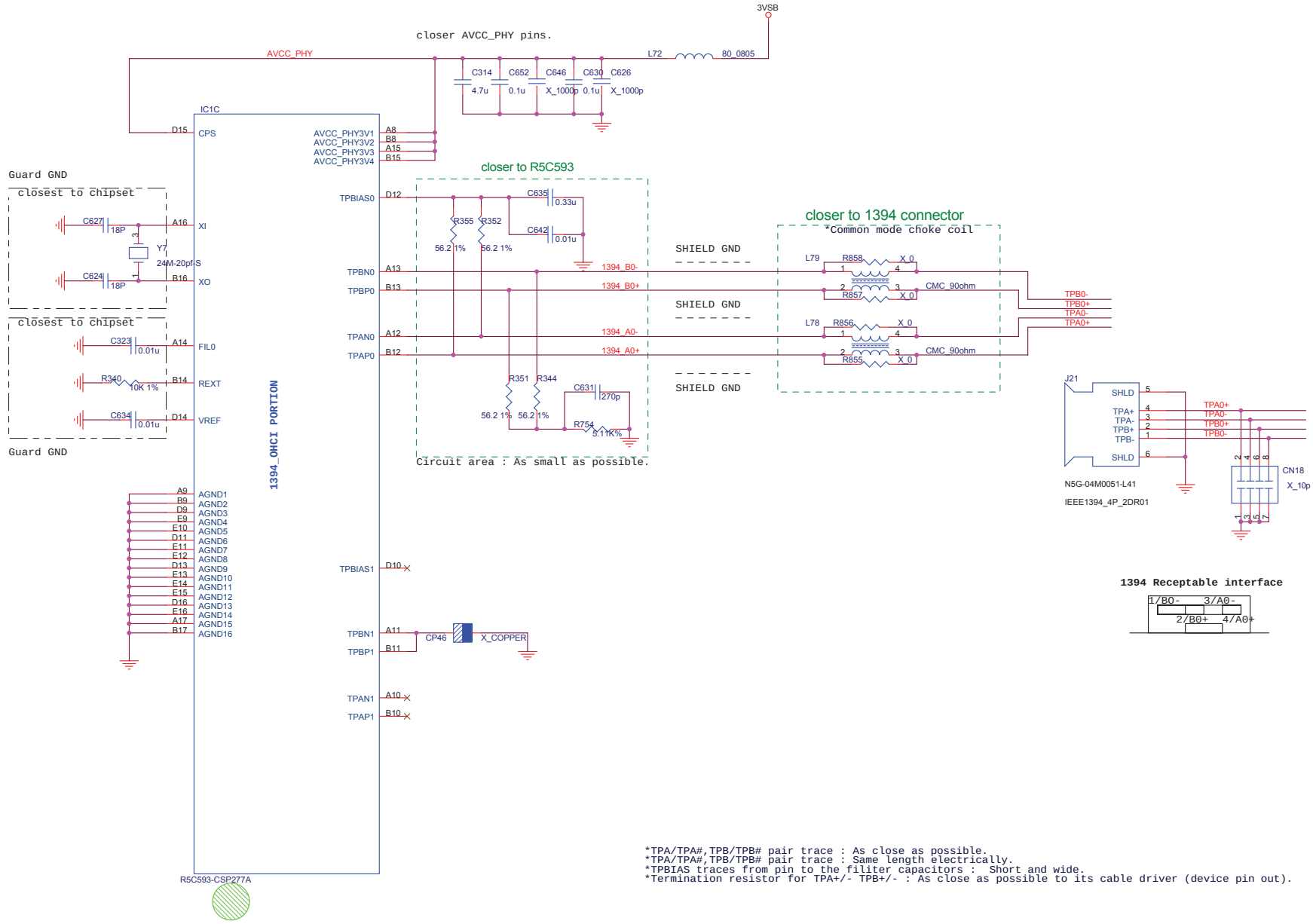
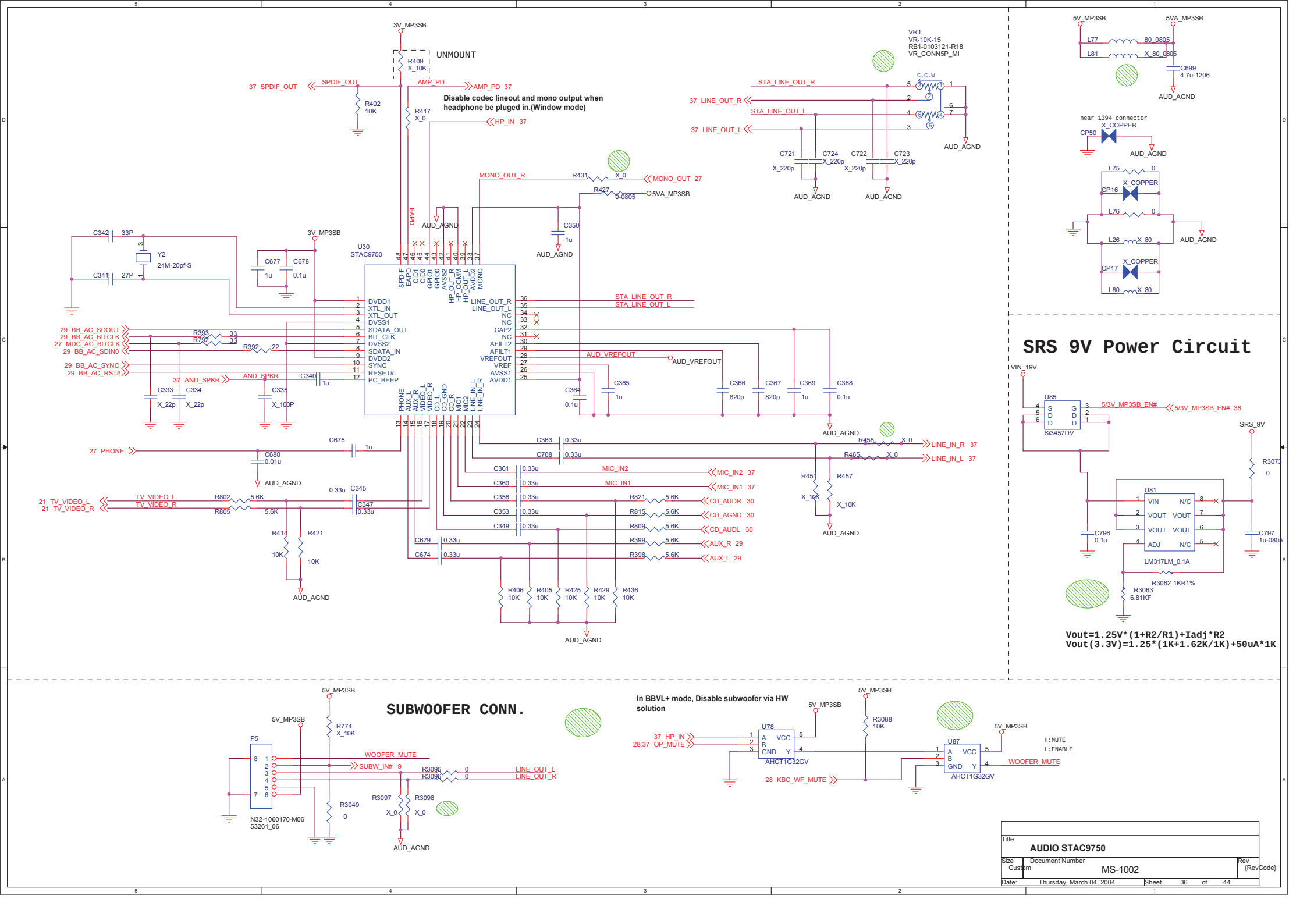


Title	P5 5C593/1394OHCI		
Size: Custom	Document Number: MS-1002	Rev: {RevCode}	
Date: Wednesday, March 03, 2004	Sheet 35 of 44		


3V_MP3SB
UNMOUNT
R409 X_10K
37 SPDIF_OUT
SPDIF_OUT
AMP_PD
AMP_PD 37
R402 10K
R417 X_0
HP_IN 37
Disable codec lineout and mono output when headphone be pluged in.(Window mode)
VR1
VR-10K-15
RB1-0103121-R18
VR_CONN5P_MI
STA_LINE_OUT_R
37 LINE_OUT_R
STA_LINE_OUT_L
37 LINE_OUT_L
C.C.W
AUD_AGND
C721 X_220p
C724 X_220p
C722 X_220p
C723 X_220p
MONO_OUT_R
R431 X_0
MONO_OUT 27
R427 0-0805
5VA_MP3SB
EAPD
AUD_AGND
C350 1u
U30
STAC9750
C342 33P
C341 27P
Y2
24M-20pf-S
C677 1u
C678 0.1u
SPDIF
EAPD
CID1
CID0
GPIO1
GPIO0
AVSS2
HP_OUT_R
HP_COMM
HP_OUT_L
AVDD2
MONO
DVDD1
XTL_IN
XTL_OUT
DVSS1
SDATA_OUT
BIT_CLK
DVSS2
SDATA_IN
DVDD2
SYNC
RESET#
PC_BEEP
LINE_OUT_R
LINE_OUT_L
NC
NC
CAP2
NC
AFILT2
AFILT1
VREFOUT
VREF
AVSS1
AVDD1
29 BB_AC_SDOUT
29 BB_AC_BITCLK
27 MDC_AC_BITCLK
29 BB_AC_SDIN0
29 BB_AC_SYNC
29 BB_AC_RST#
R393 33
R792 33
R392 22
C333 X_22p
C334 X_22p
C335 X_100P
37 AND_SPKR
AND_SPKR
C340 1u
STA_LINE_OUT_R
STA_LINE_OUT_L
AUD_VREFOUT
C364 0.1u
C365 1u
C366 820p
C367 820p
C369 1u
C368 0.1u
PHONE
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_GND
CD_R
MIC1
MIC2
LINE_IN_L
LINE_IN_R
27 PHONE
C675 1u
C680 0.01u
C363 0.33u
C708 0.33u
R458 X_0
R465 X_0
LINE_IN_R 37
LINE_IN_L 37
C361 0.33u
C360 0.33u
MIC_IN2
MIC_IN1
MIC_IN2 37
MIC_IN1 37
C356 0.33u
C353 0.33u
C349 0.33u
R821 5.6K
R815 5.6K
R809 5.6K
CD_AUDR 30
CD_AGND 30
CD_AUDL 30
21 TV_VIDEO_L
21 TV_VIDEO_R
TV_VIDEO_L
TV_VIDEO_R
R802 5.6K
R805 5.6K
0.33u C345
C347 0.33u
R414 10K
R421 10K
C679 0.33u
C674 0.33u
R399 5.6K
R398 5.6K
AUX_R 29
AUX_L 29
R451 X_10K
R457 X_10K
R406 10K
R405 10K
R425 10K
R429 10K
R436 10K
5V_MP3SB
5VA_MP3SB
L77 80_0805
L81 X_80_0805
C699 4.7u-1206
near 1394 connector
X_COPPER
CP50
L75 0
CP16
L76 0
L26 X_80
CP17
L80 X_80
SRS 9V Power Circuit
VIN_19V
U85
Si3457DV
5/3V_MP3SB_EN#
5/3V_MP3SB_EN# 38
SRS_9V
R3073 0
U81
LM317LM_0.1A
C796 0.1u
C797 1u-0805
R3062 1KR1%
R3063 6.81KF
Vout=1.25V*(1+R2/R1)+Iadj*R2
Vout(3.3V)=1.25*(1K+1.62K/1K)+50uA*1K
SUBWOOFER CONN.
P5
R774 X_10K
WOOFER_MUTE
SUBW_IN# 9
R3095 0
R3096 0
LINE_OUT_L
LINE_OUT_R
R3049 0
R3097 X_0
R3098 X_0
N32-1060170-M06
53261_06
In BBVL+ mode, Disable subwoofer via HW solution
37 HP_IN
28,37 OP_MUTE
U78
AHCT1G32GV
R3088 10K
28 KBC_WF_MUTE
U87
H:MUTE
L:ENABLE
Title
AUDIO STAC9750
Size
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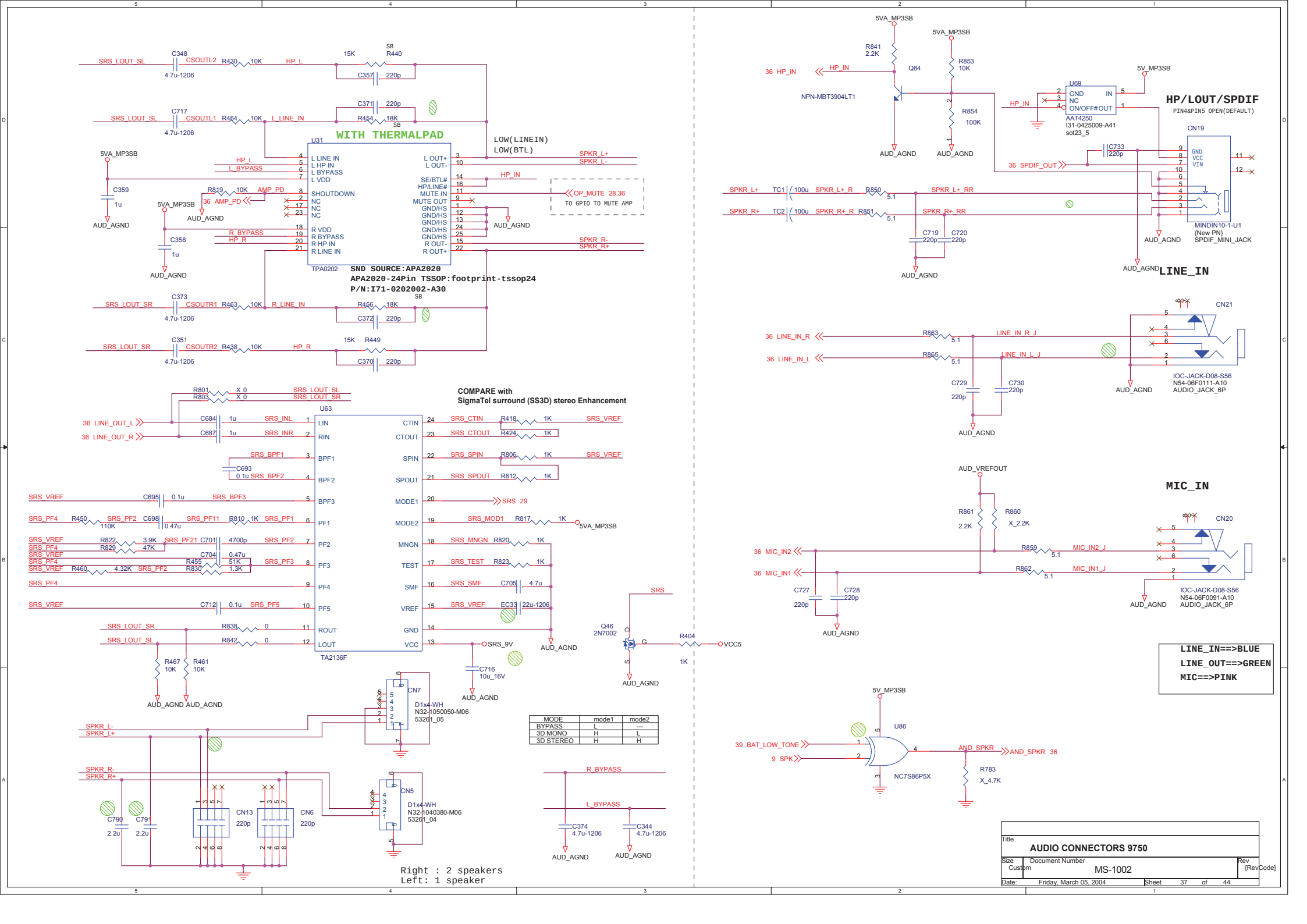
WITH THERMALPAD
LOW(LINEIN)
LOW(BTL)
U31
TPA0202
SND SOURCE:APA2020
APA2020-24Pin TSSOP:footprint-tssop24
P/N:I71-0202002-A30
COMPARE with
SigmaTel surround (SS3D) stereo Enhancement
U63
TA2136F
HP/LOUT/SPDIF
PIN4&PIN5 OPEN(DEFAULT)
LINE_IN
MIC_IN
LINE_IN==>BLUE
LINE_OUT==>GREEN
MIC==>PINK
AUDIO CONNECTORS 9750
MS-1002
Friday, March 05, 2004
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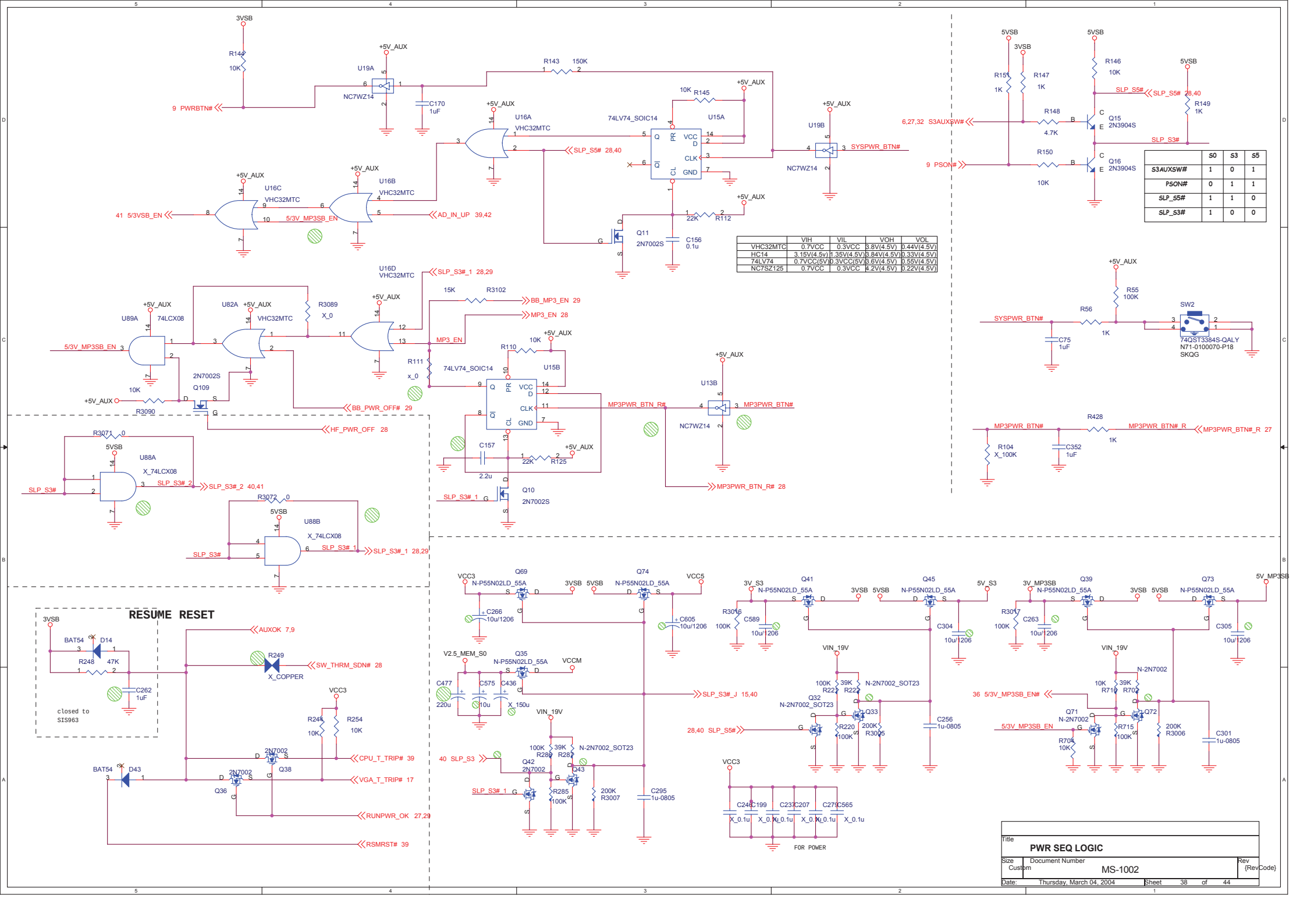
Right : 2 speakers
Left: 1 speaker



	VIH	VIL	VOH	VOL
VHC32MTC	0.7VCC	0.3VCC	3.8V(4.5V)	0.44V(4.5V)
HC14	3.15V(4.5v)	1.35V(4.5V)	3.84V(4.5V)	0.33V(4.5V)
74LV74	0.7VCC(5V)	0.3VCC(5V)	3.6V(4.5V)	0.55V(4.5V)
NC7SZ125	0.7VCC	0.3VCC	4.2V(4.5V)	0.22V(4.5V)

	S0	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S5#	1	1	0
SLP_S3#	1	0	0

Title	PWR SEQ LOGIC
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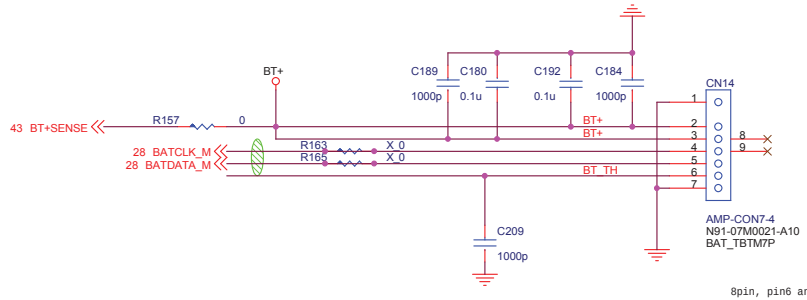
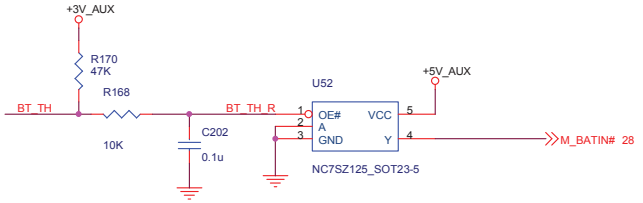
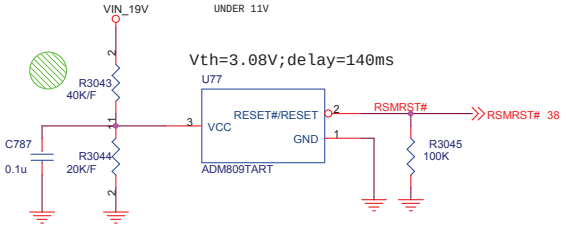
BATTERY CONNECTOR

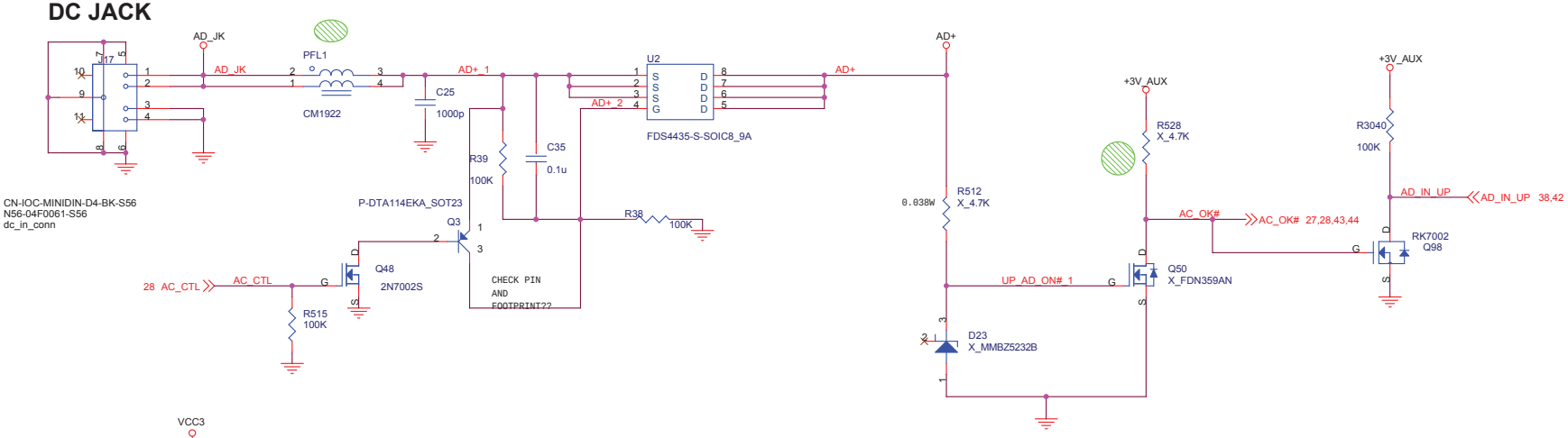


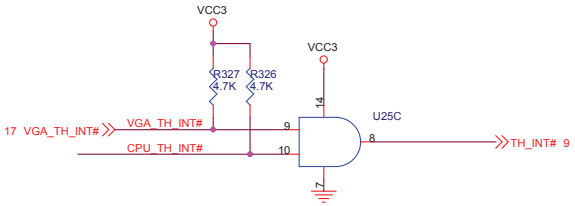
8pin, pin6 and pin7 need a empty space.

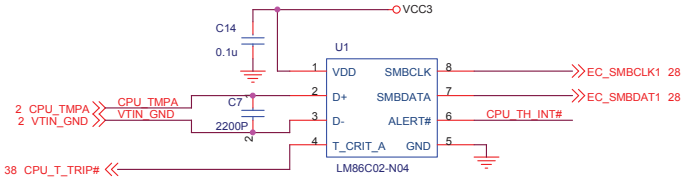


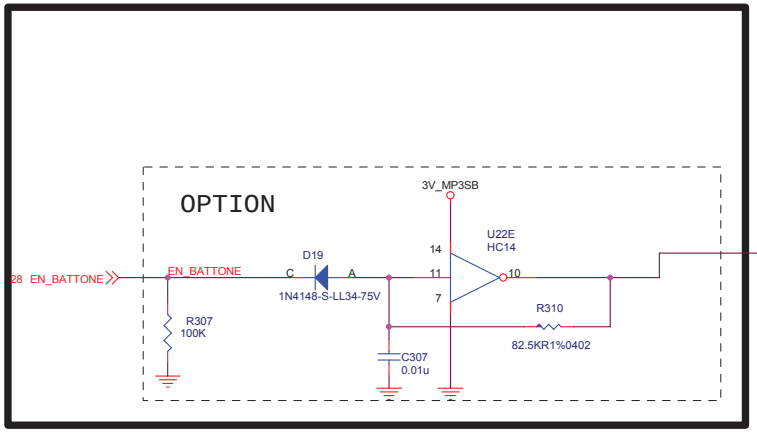


DC JACK









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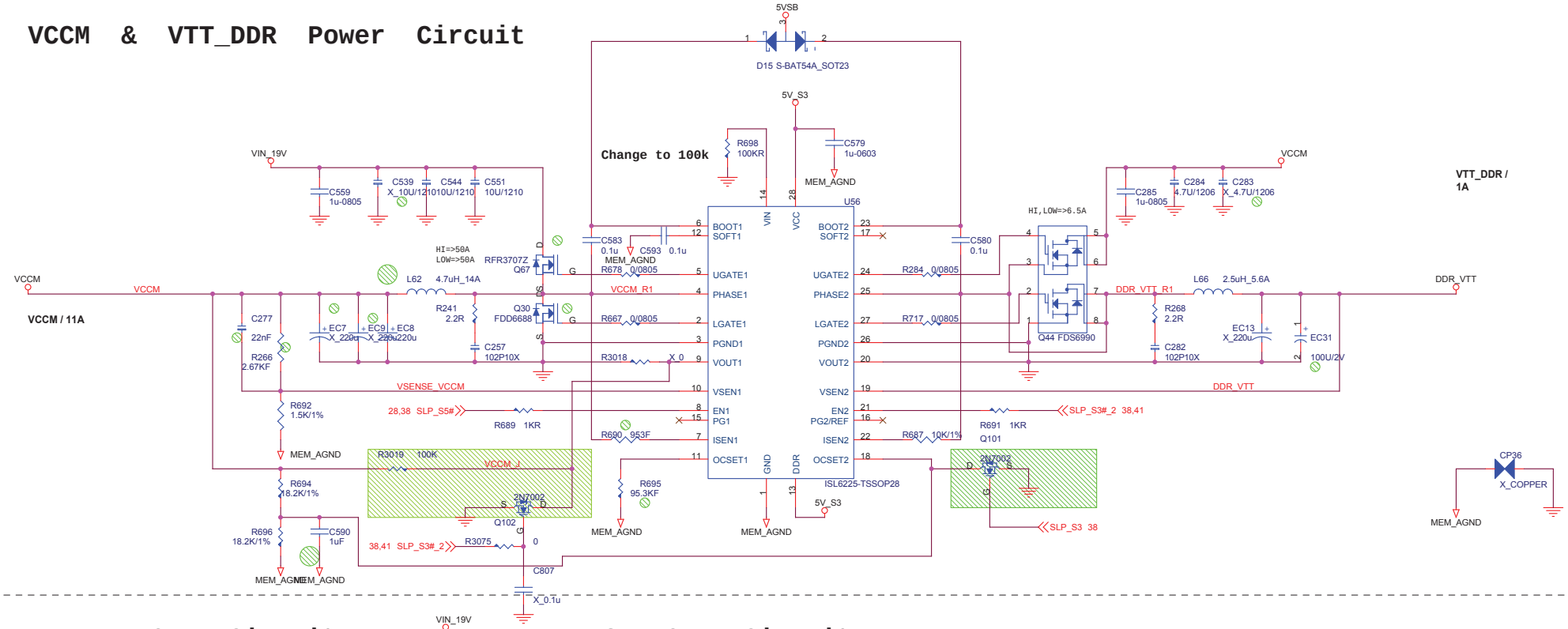
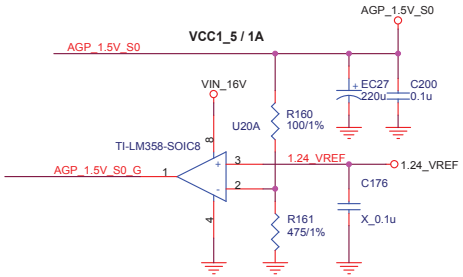
VCCM & VTT_DDR Power Circuit

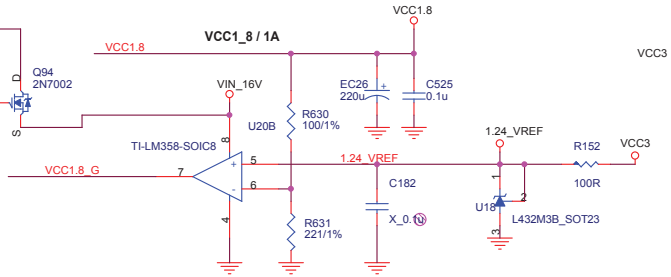


1.5V POWER Circuit



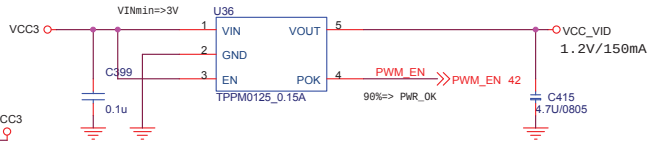
AGP_1.5V_S0(1.5V)=1.24*(475+100)/475

1.8V POWER Circuit

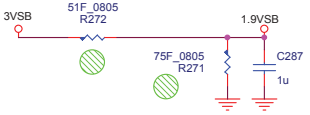


VCC1.8_M10(1.8V)=1.24*(221+100)/221

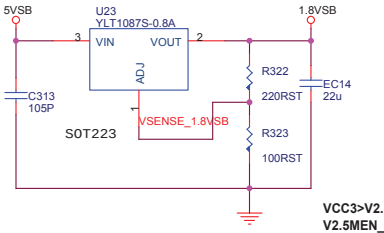
VCC_VID POWER Circuit



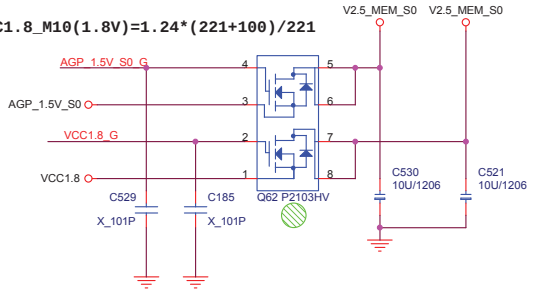
1.9VSB Circuit



VCC1.9SB(1.9V)=3.3*75/(54.9+75)



VCC3>V2.5MEM_S0>1.2_VCORE_S0>AGP_1.5V_S0
V2.5MEN_S0>VCC1.8



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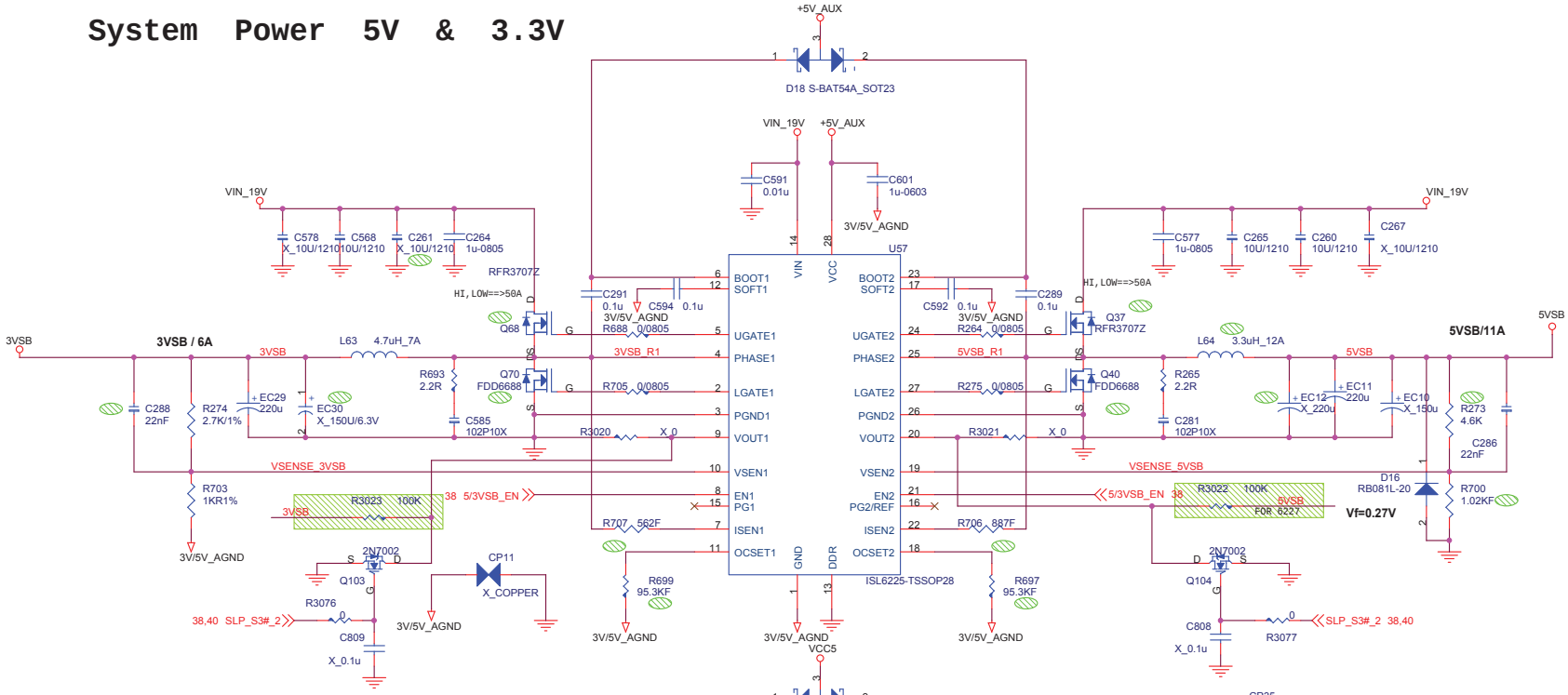
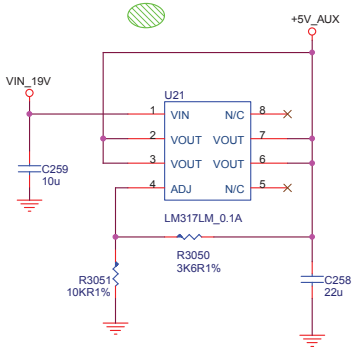
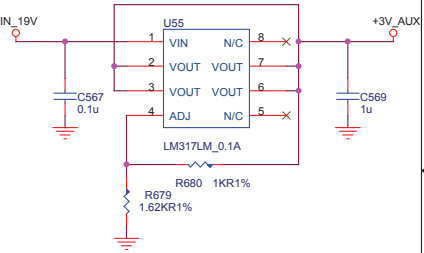
System Power 5V & 3.3V



5V_AUX Power Circuit

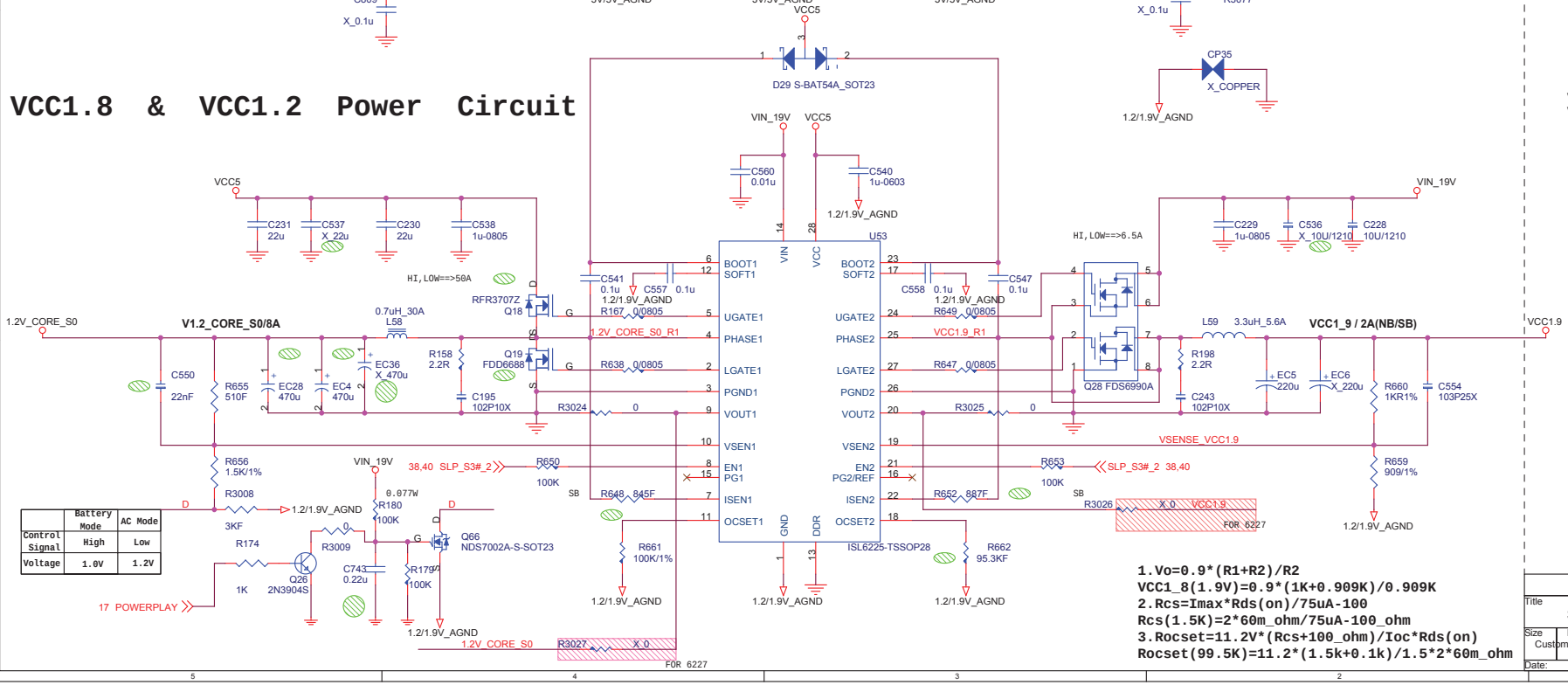


3V_AUX Power Circuit



Vout=1.25V*(1+R2/R1)+Iadj*R2
Vout(3.3V)=1.25*(1K+1.62K/1K)+50uA*1K

VCC1.8 & VCC1.2 Power Circuit



Control Signal	Battery Mode	AC Mode
Voltage	High	Low
	1.0V	1.2V

1.Vo=0.9*(R1+R2)/R2
VCC1_8(1.9V)=0.9*(1K+0.909K)/0.909K
2.Rcs=Imax*Rds(on)/75uA-100
Rcs(1.5K)=2*60m_ohm/75uA-100_ohm
3.Rocset=11.2V*(Rcs+100_ohm)/Ioc*Rds(on)
Rocset(99.5K)=11.2*(1.5k+0.1k)/1.5*2*60m_ohm

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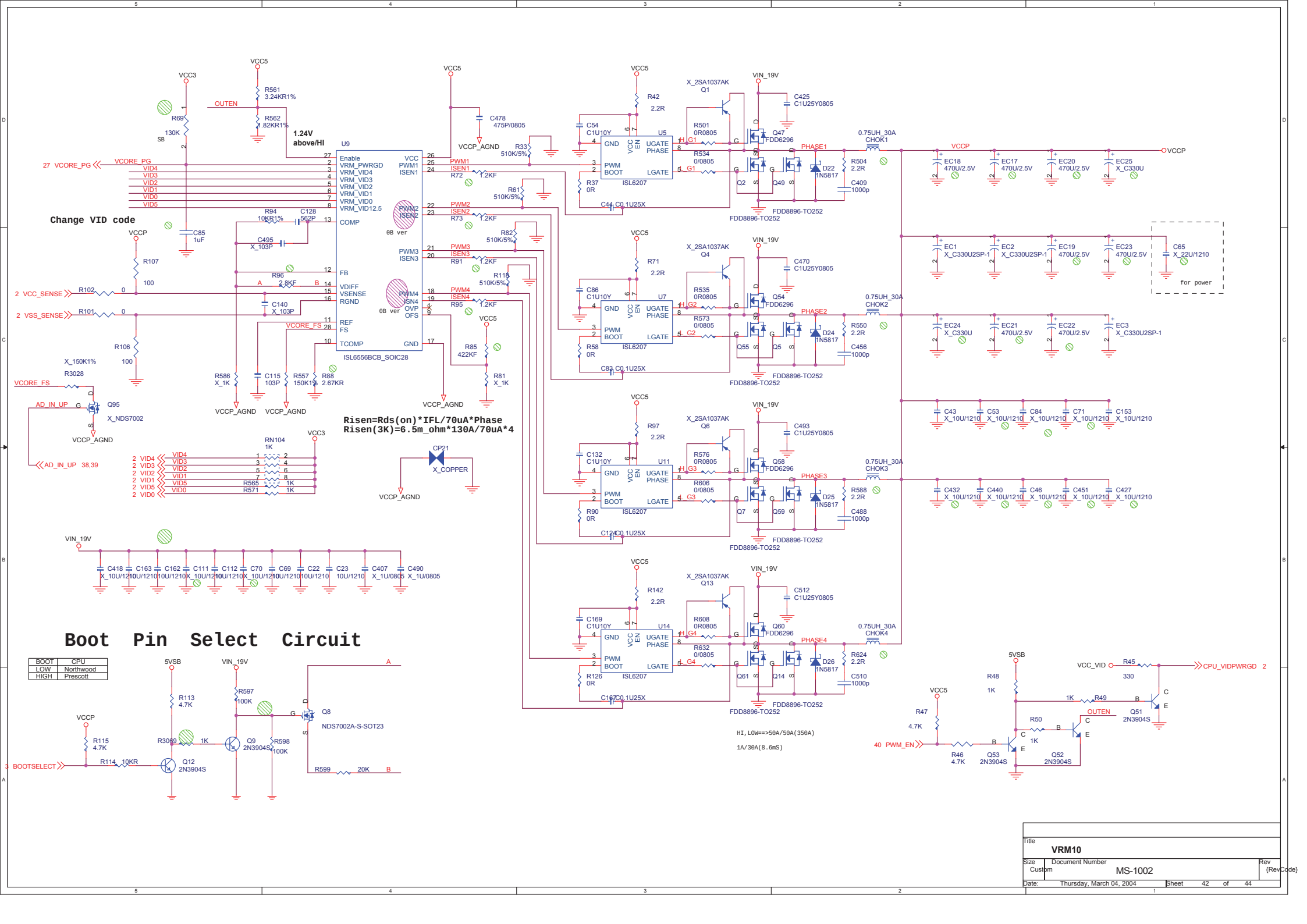
Change VID code
1.24V above/HI
Risen=Rds(on)*IFL/70uA*Phase
Risen(3K)=6.5m_ohm*130A/70uA*4
ISL6556BCB_SOIC28
ISL6207
FDD8896-TO252
Boot Pin Select Circuit
BOOT CPU
LOW Northwood
HIGH Prescott
HI,LOW==>50A/50A(350A)
1A/30A(8.6mS)
for power
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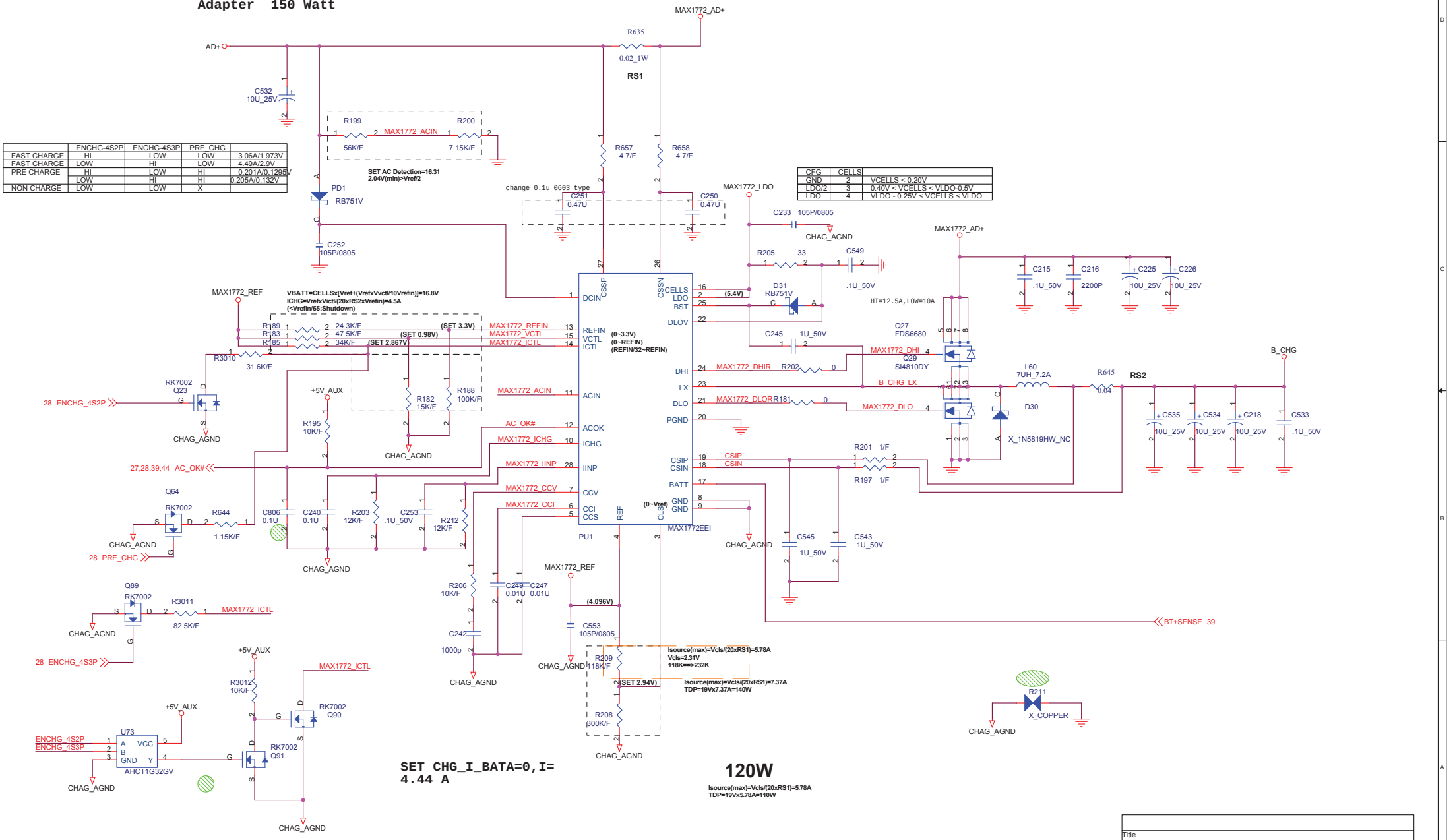
Adapter 150 Watt



	ENCHG-4S2P	ENCHG-4S3P	PRE_CHG	
FAST CHARGE	HI	LOW	LOW	3.06A/1.973V
FAST CHARGE	LOW	HI	LOW	4.49A/2.9V
PRE CHARGE	HI	LOW	HI	0.201A/0.1295V
	LOW	HI	HI	0.205A/0.132V
NON CHARGE	LOW	LOW	X	

CFG	CELLS	
GND	2	VCELLS < 0.20V
LDO/2	3	0.40V < VCELLS < VLDO-0.5V
LDO	4	VLDO - 0.25V < VCELLS < VLDO

SET CHG_I_BATA=0,I= 4.44 A

120W

Isource(max)=Vcls/(20xRS1)=5.78A
TDP=19Vx5.78A=110W

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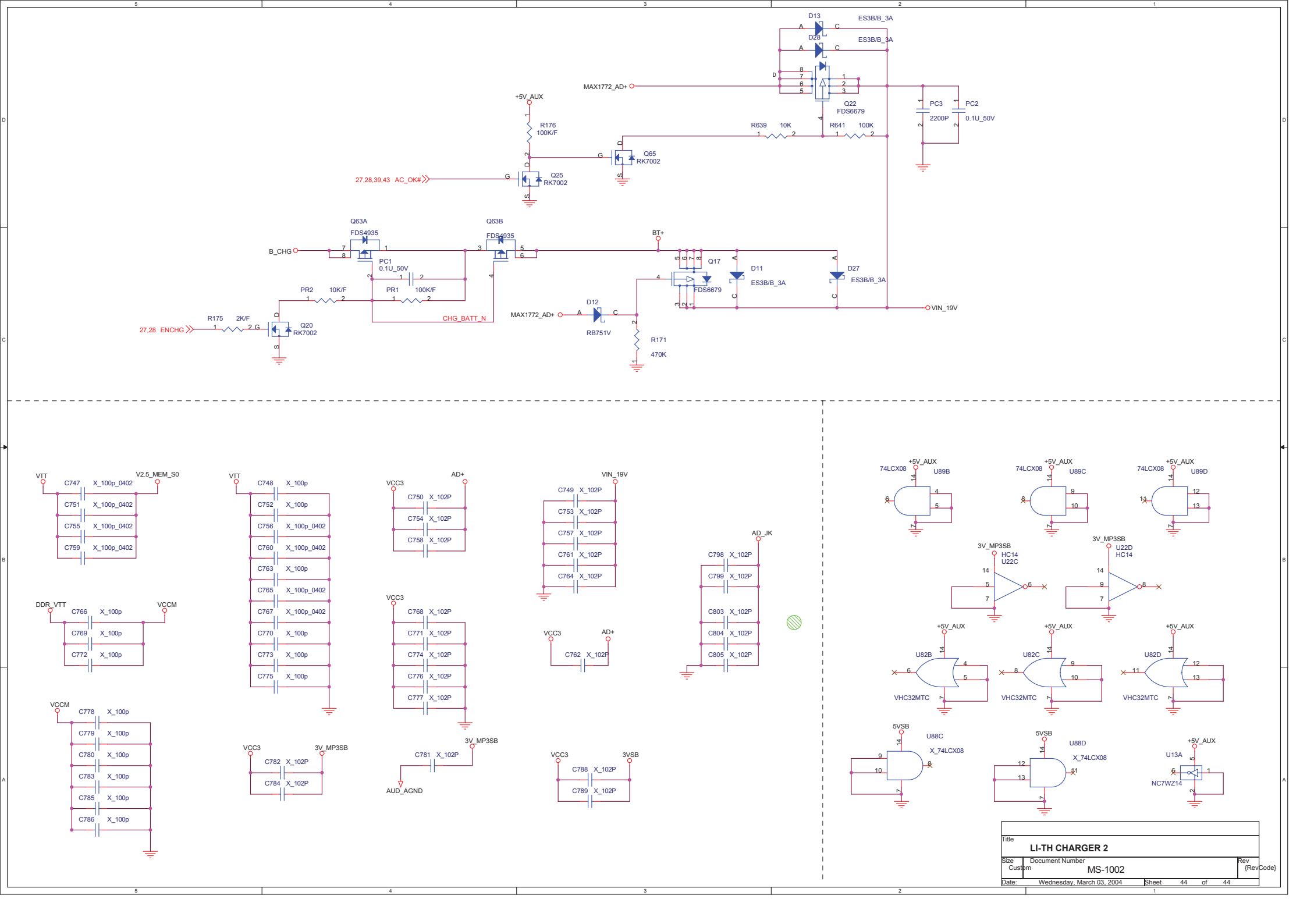

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