MS-7916

ATX

Ver:1.0

Intel -SharkBay plamform (Z97-XPOWER)

CPU:

Haswell-Reflash LGA1150

CPU ISL6388 12Phase

System Chipset:

Lynx Point Z97

Onboard Chip:

HD Audio Codec:ALC1150

LAN-Killer 2005

SIO:NCT6792D

Flash ROM: SPI 64 MB X2

CLK GEN: IDT6V49325

CLK BUF: 9DBV0841

USB Charge: SLG55583A

PWM:

VCORE: VRD12.5 -ISL6388 - 12Phase

DDR : UP1504S - 2Phase

PCH(1.05V) -OP+MOS

Other:

SATA3.0 x4(PCH)
*SATA3.0 x2 (ASM1061 SATA 6G *1)*
*M.2 X1(SATA*2/PCIE*2)*

*REAR USB3.0 X4 (ASM1074 *1)*
REAR USB3.0 X2 (PCH)
*REAR USB3.1 X2(ASM1042 *1)*
FRONT USB3.0 X2 (PCH)
REAR USB2.0 X2
*FRONT USB2.0 X4(Super Charge *2)*

Main Memory:

*DDRIII (800/1066/1333/1666MHz) * 4 (Dual Channel)*

ACPI:

UPI-uP7501+uP1714

Expansion Slots:

*PCI Express (X16) Slot * 3*

*PCI Express (X1) Slot * 4*

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Custom	Cover Sheet	1.0

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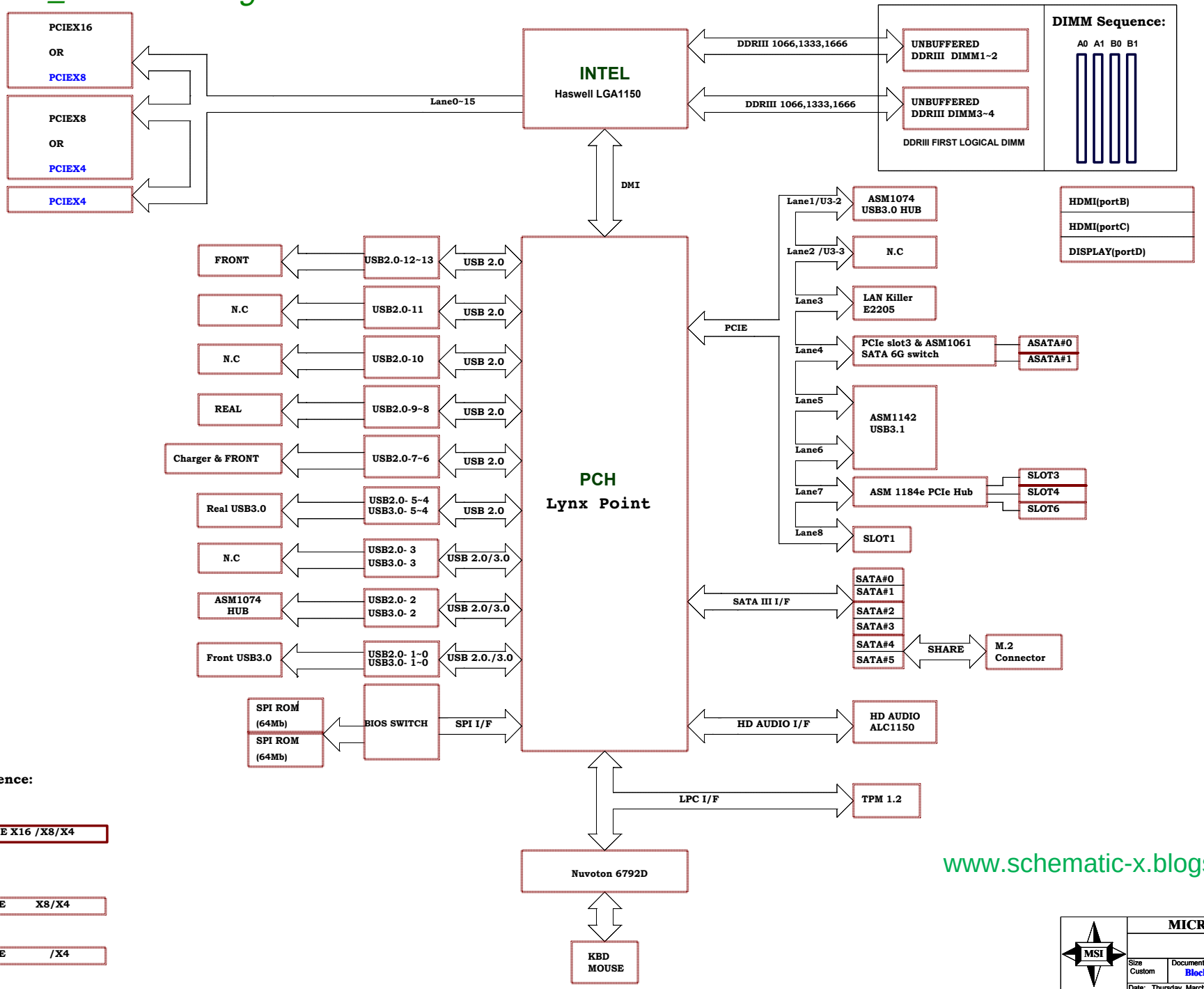
MS-7916_0A Block Diagram



Slot Sequence:

- PCIE X1
- PCIE X16 /X8/X4
- PCIE X1
- PCIE X1
- PCIE X8/X4
- PCIE X1
- PCIE /X4

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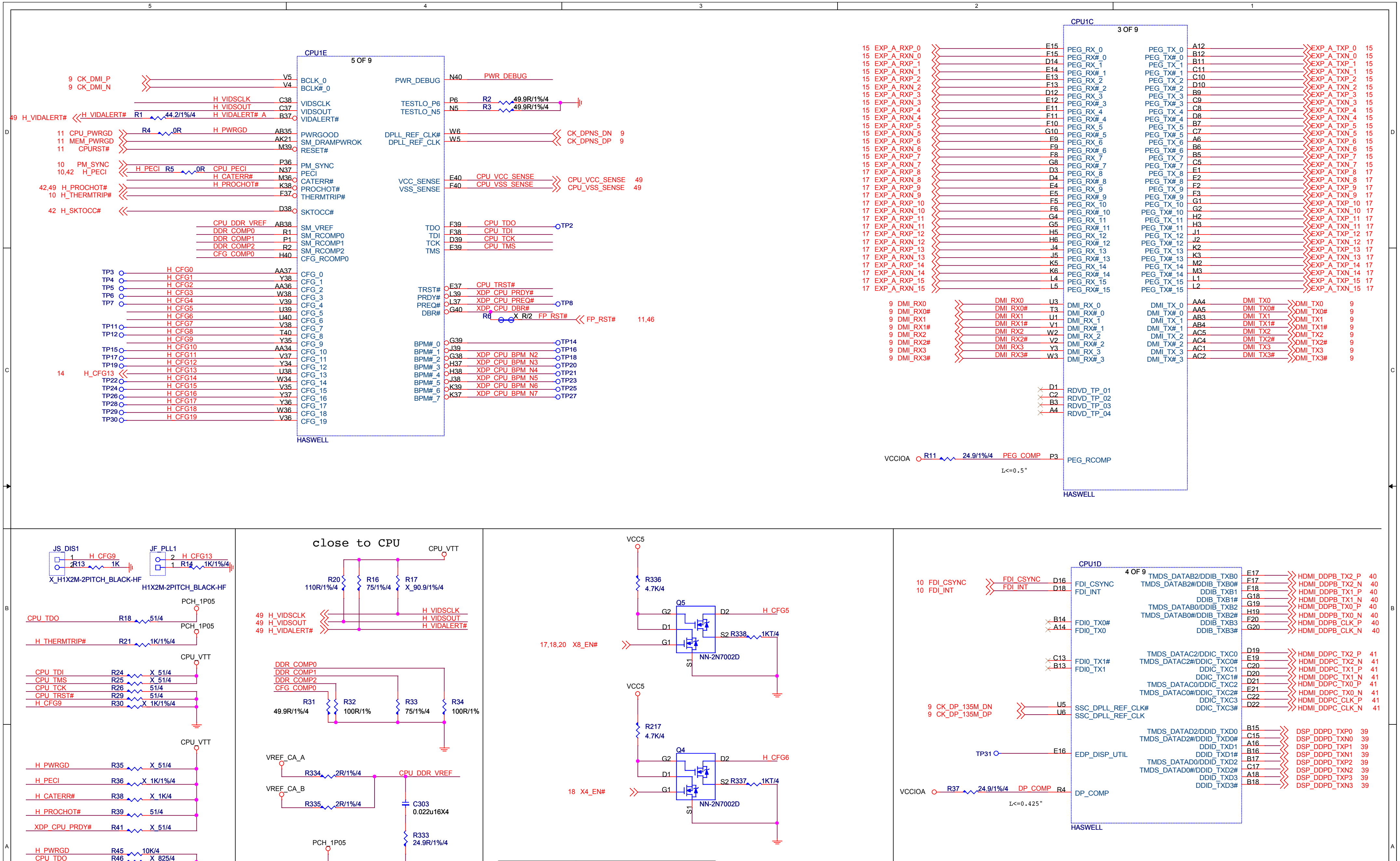

EN#		SLOT2	SLOT5	SLOT7
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	None	None	None
1	1	X16	X0	X0

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Size: Custom | Document Description: CPU-CNTL/CLK/MISC/PEG | Rev 1.0

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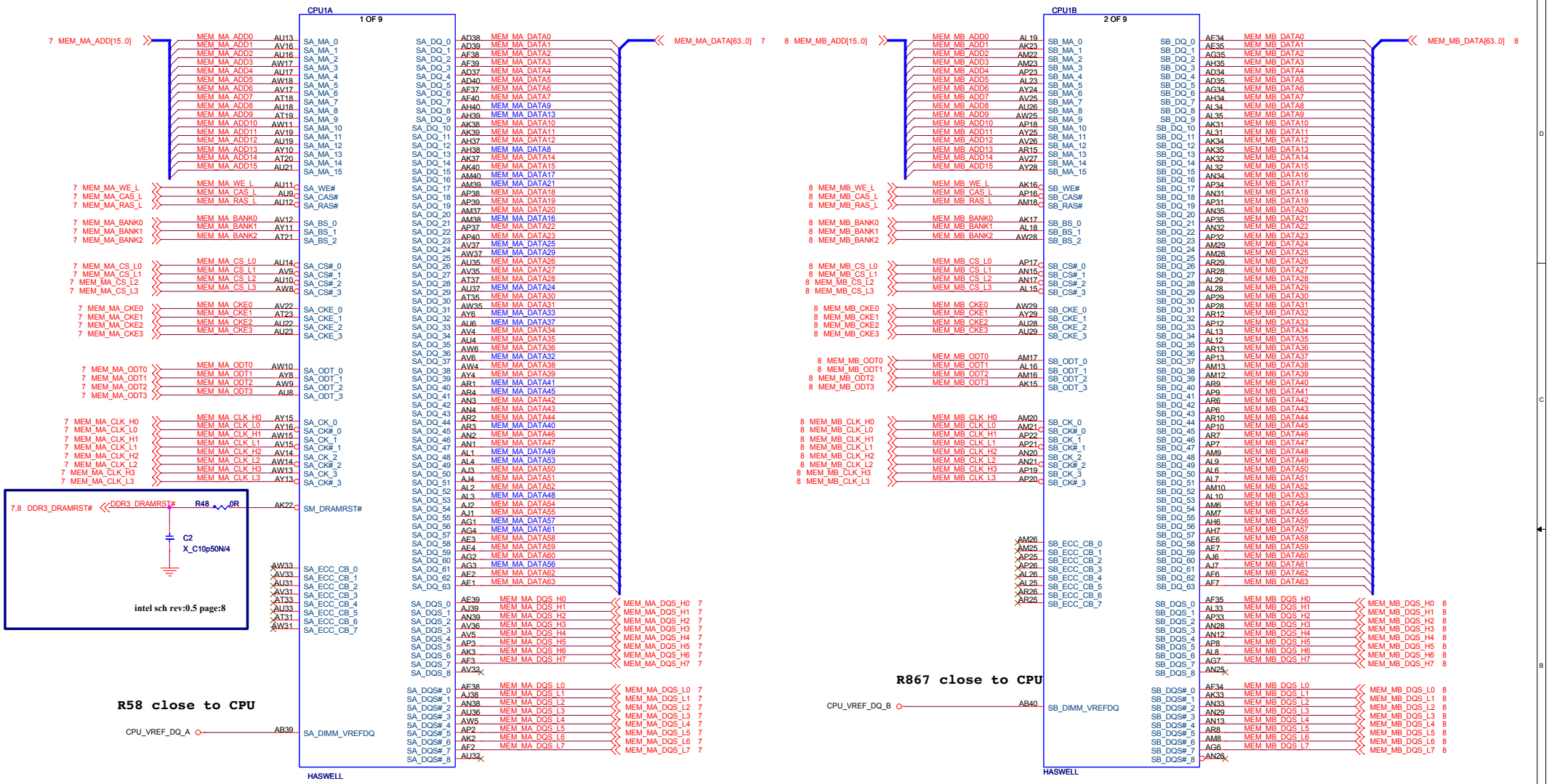

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7916
Size	Custom
Document Description	CPU-Memory
Rev	1.0
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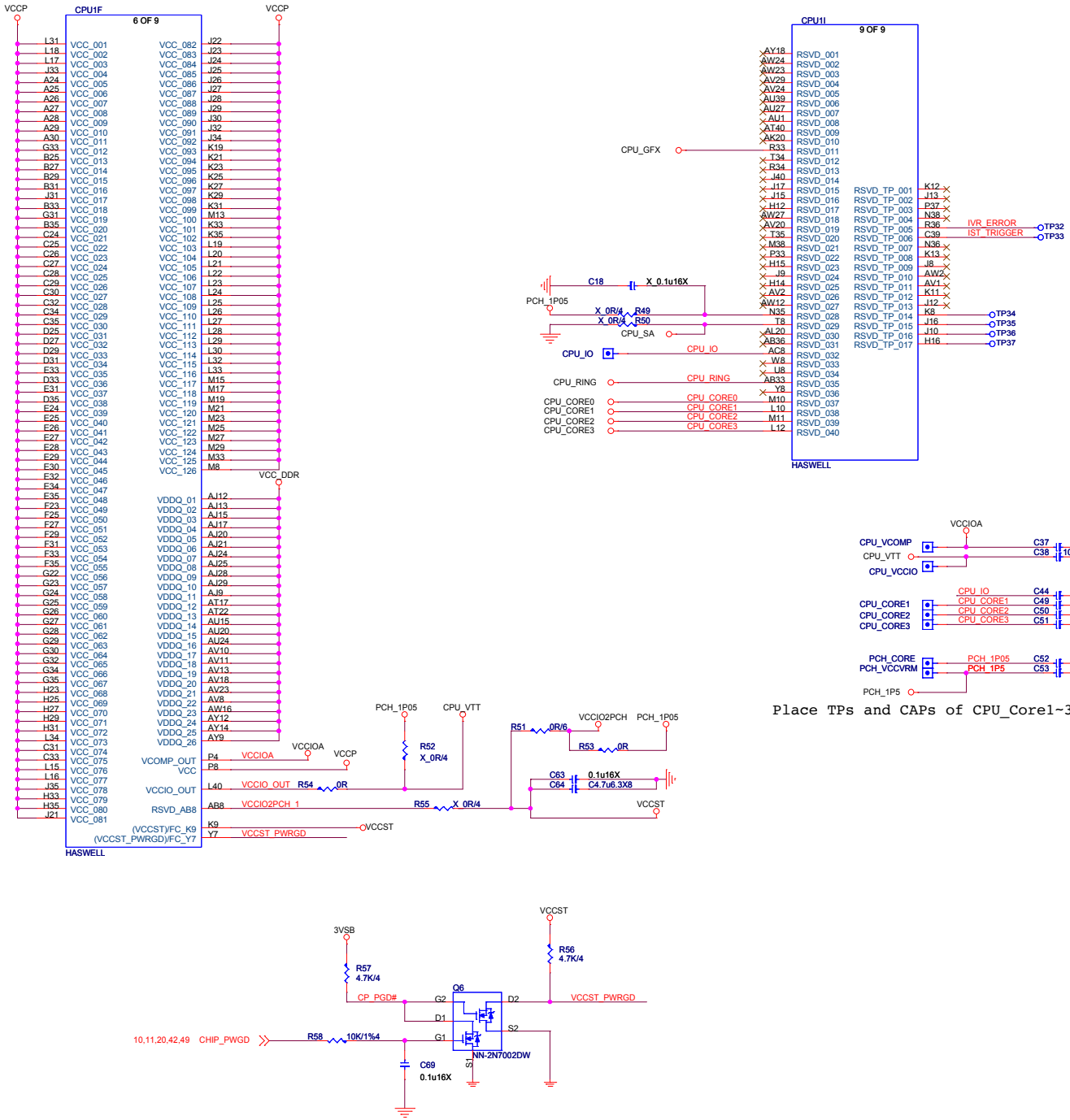
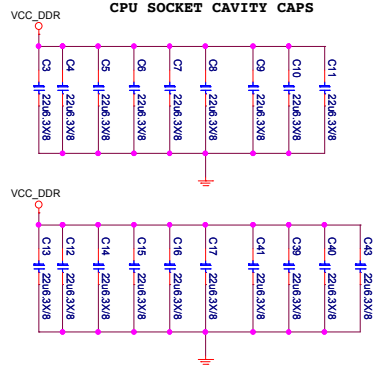


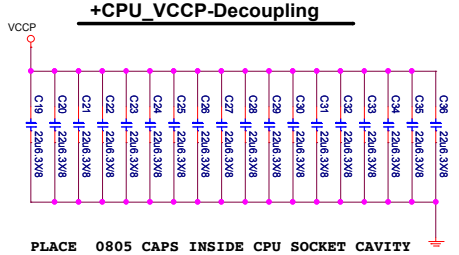
Place TPs and CAPs of CPU_Core1~3 next to Vcheck

+1.5V_DDR3-Decoupling

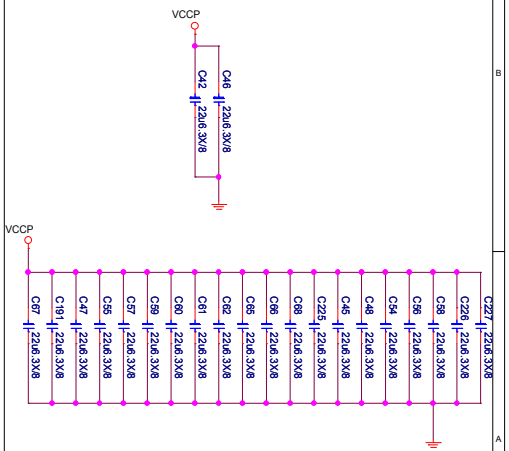
CPU SOCKET CAVITY CAPS



+CPU_VCCP-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY



MICRO-STAR INT'L CO.,LTD	
MS-7916	
Size: Custom	Document Description: CPU-Power
Rev: 1.0	
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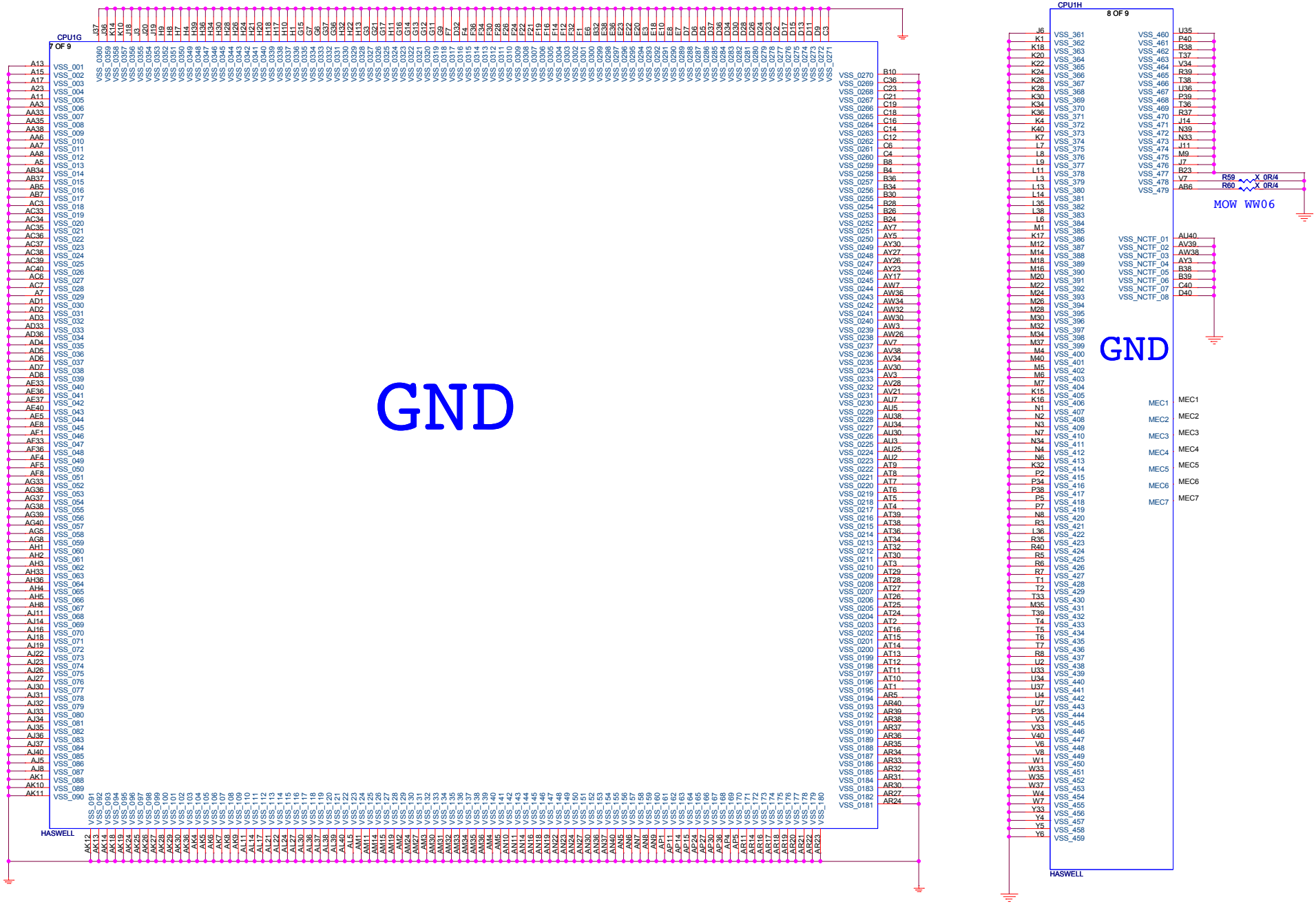

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU-GND	1.0

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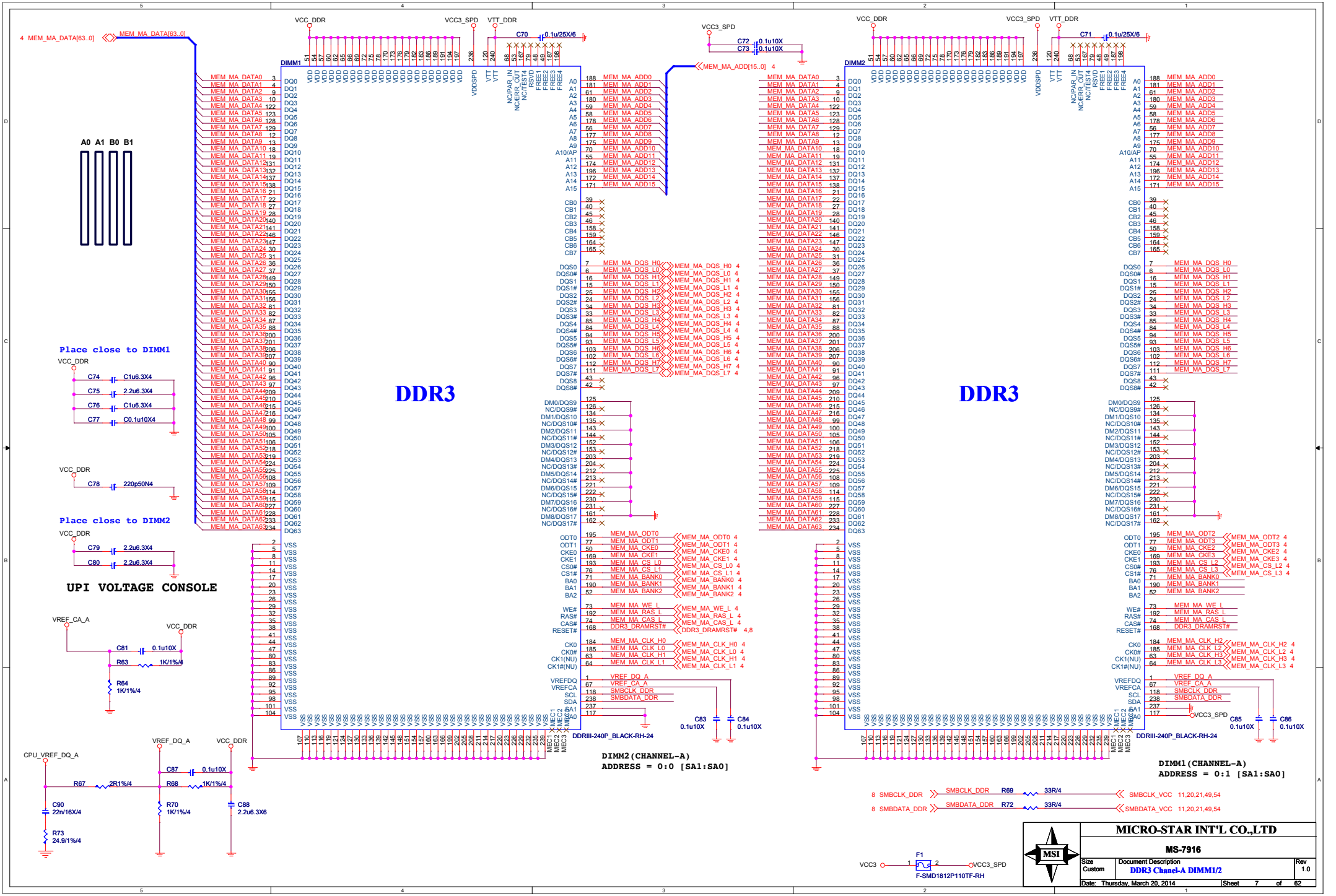
DDR3
DDR3
DIMM1
DIMM2
DDRIII-240P_BLACK-RH-24
DDRIII-240P_BLACK-RH-24
DIMM2(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
DIMM1(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
Place close to DIMM1
Place close to DIMM2
UPI VOLTAGE CONSOLE
A0 A1 B0 B1
MEM_MA_DATA[63..0]
MEM_MA_ADD[15..0]
VCC_DDR
VCC3_SPD
VTT_DDR
VREF_CA_A
VREF_DQ_A
CPU_VREF_DQ_A
SMBCLK_DDR
SMBDATA_DDR
SMBCLK_VCC 11,20,21,49,54
SMBDATA_VCC 11,20,21,49,54
MICRO-STAR INT'L CO.,LTD
MS-7916
DDR3 Chanel-A DIMM1/2
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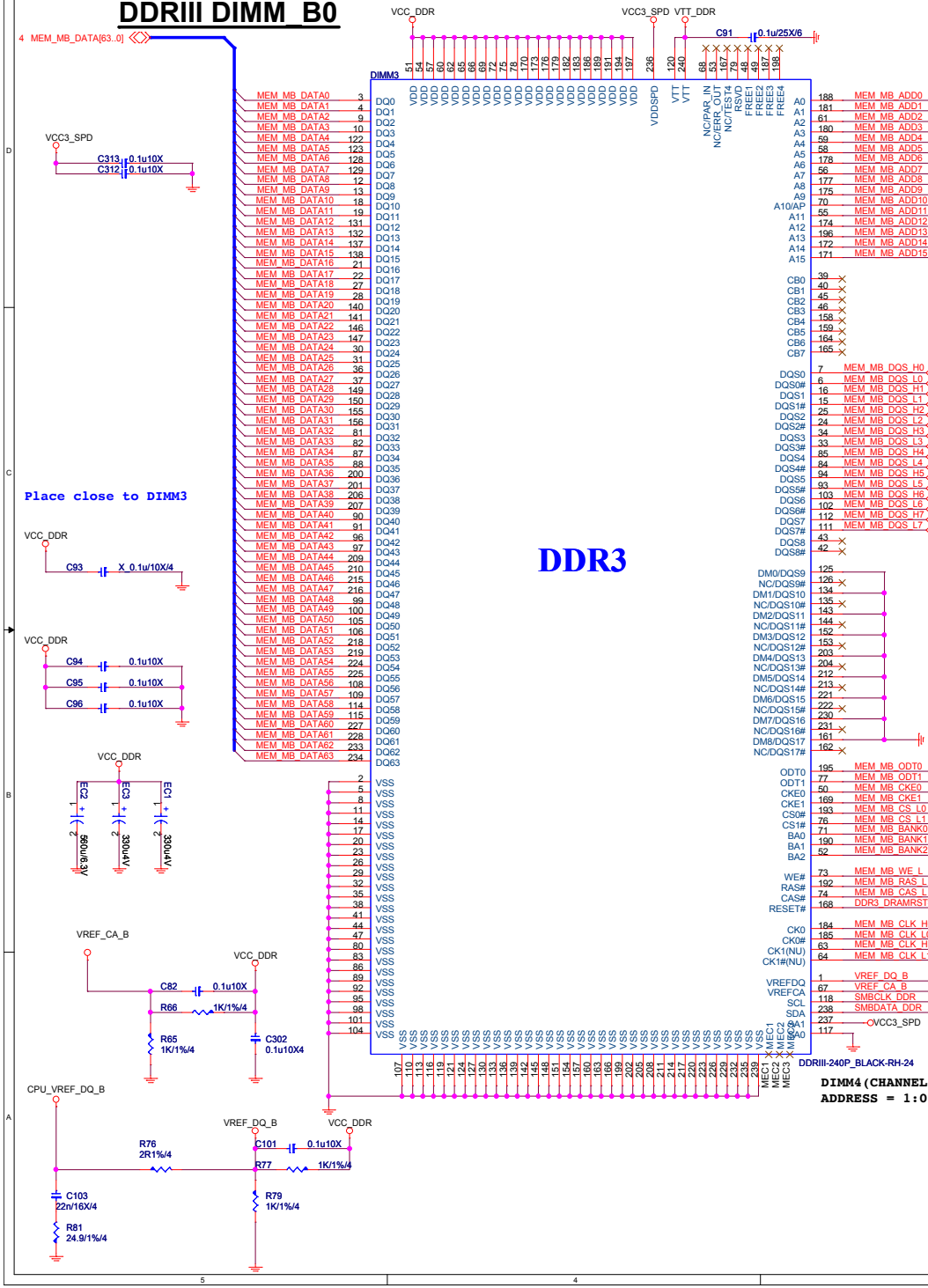
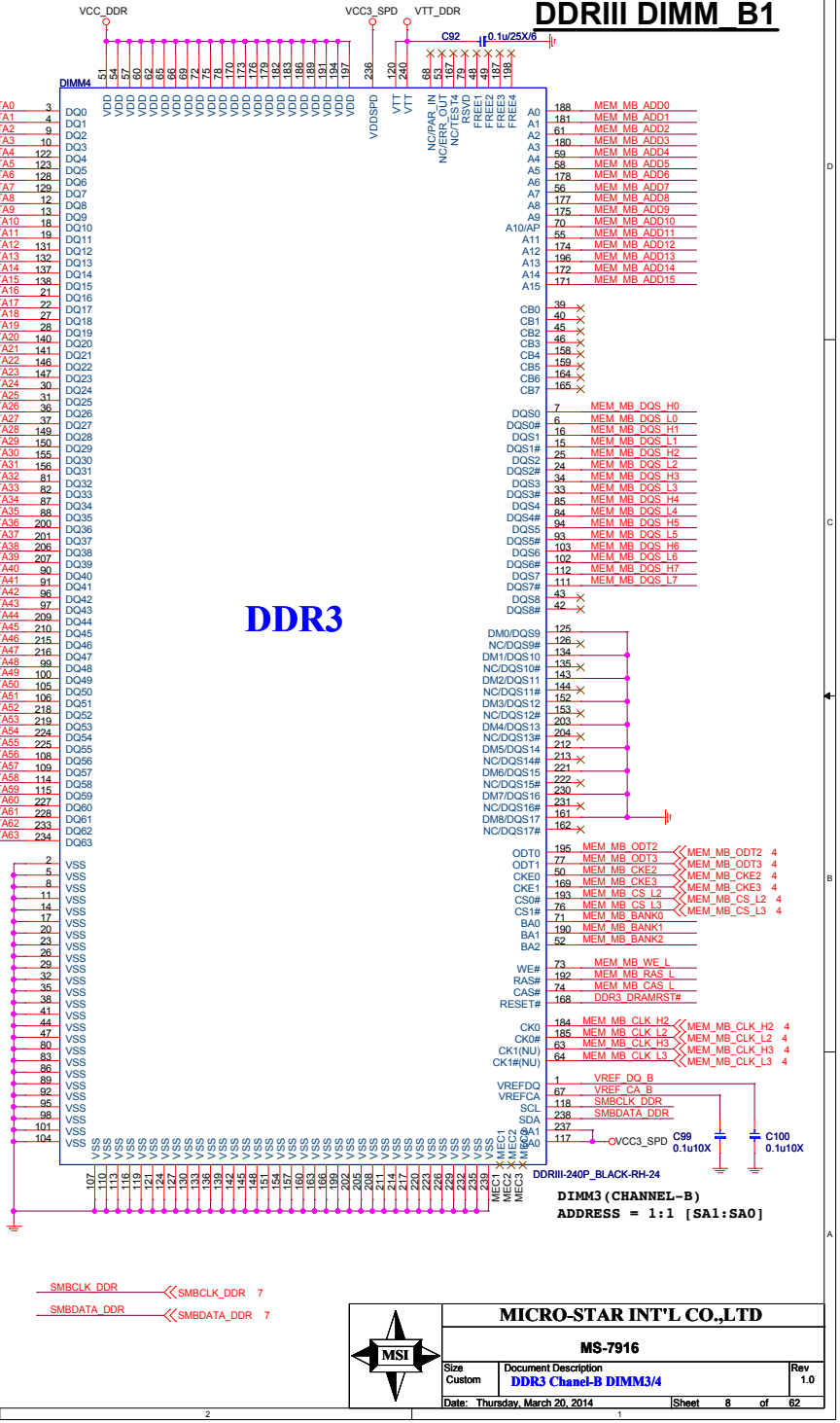
DDRIII DIMM_B0



DDRIII DIMM_B1



MICRO-STAR INT'L CO.,LTD	
MS-7916	
Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4
Rev: 1.0	
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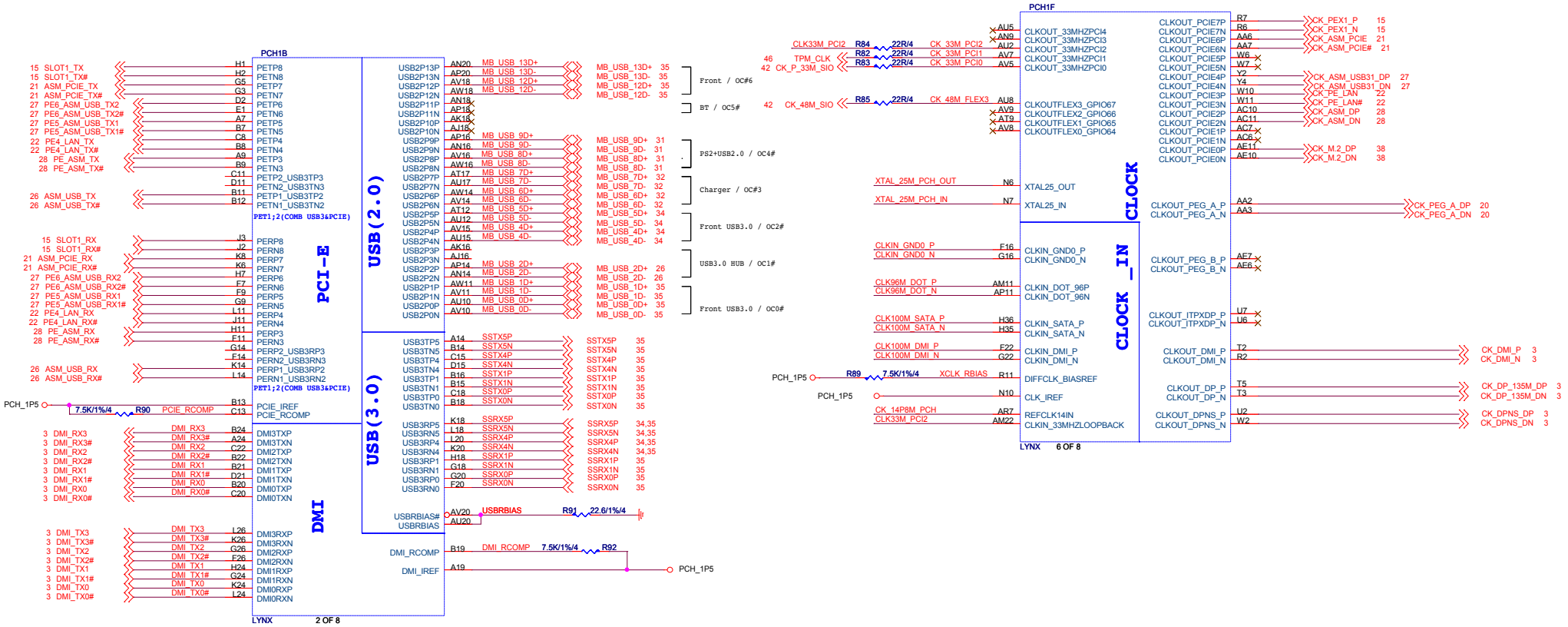
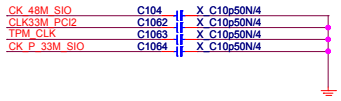
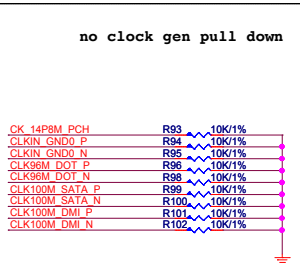
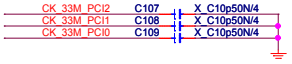
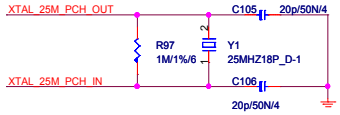








no clock gen pull down



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Custom	LYNX PCIE/DMI/USB/CLK	1.0

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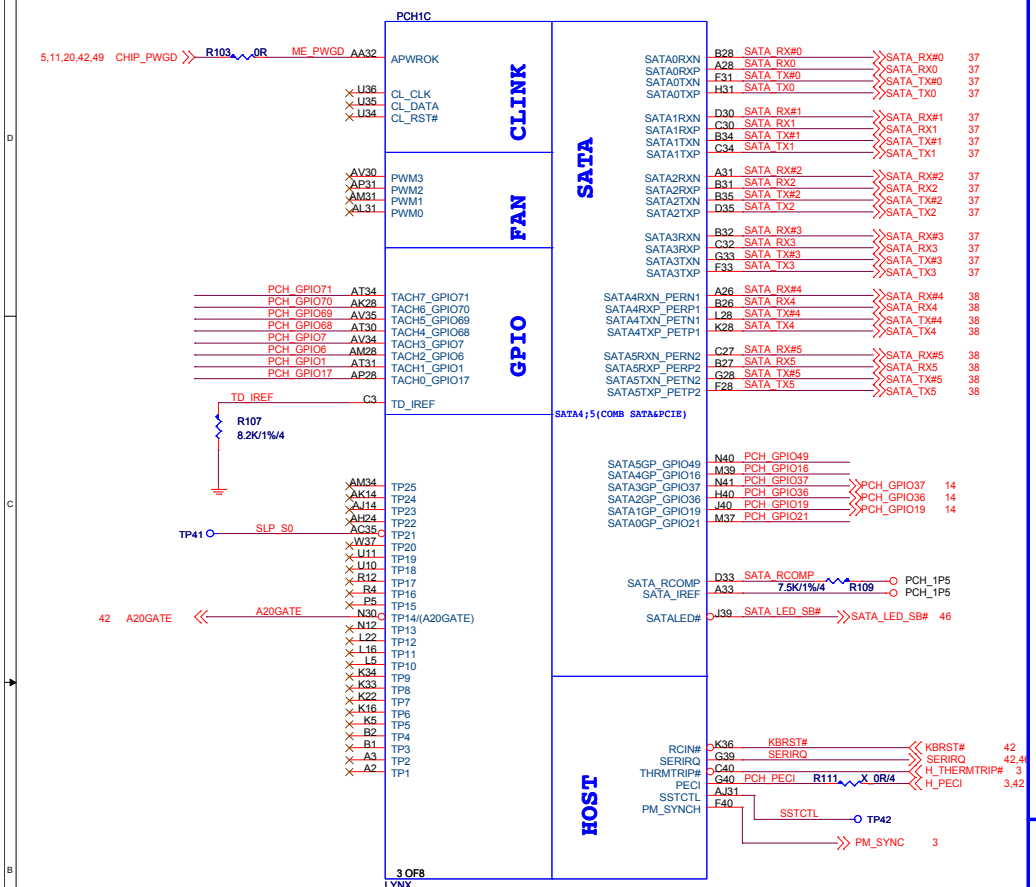

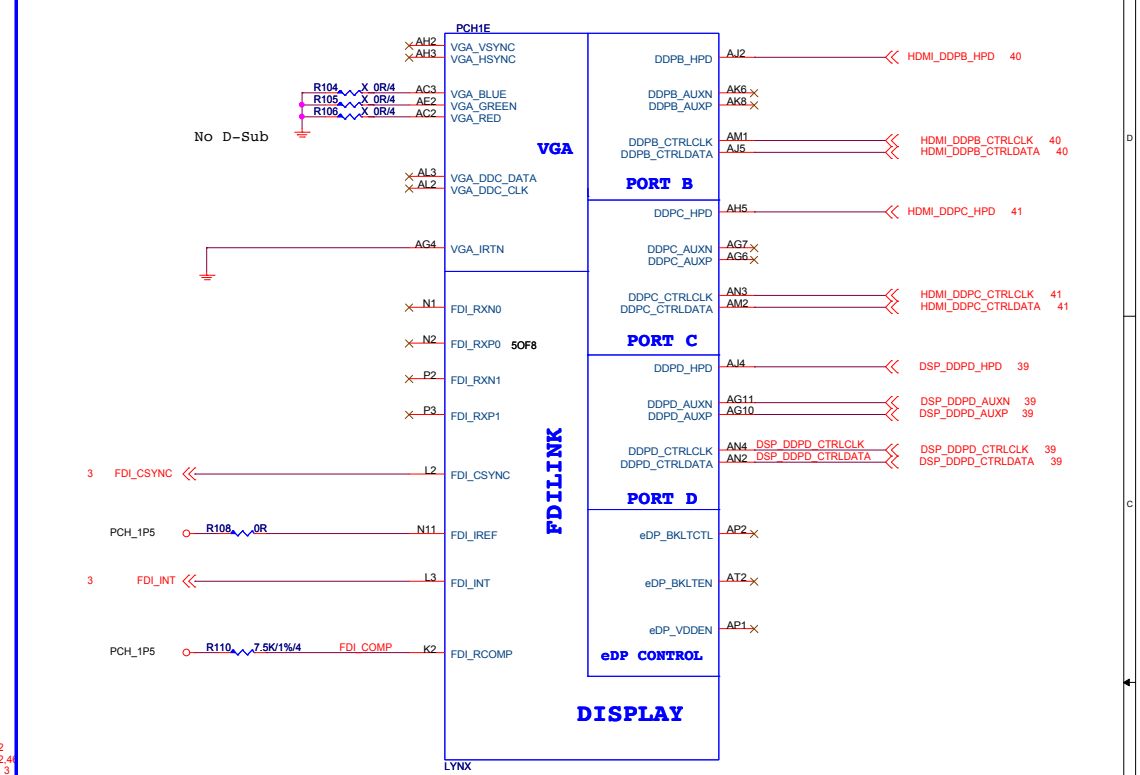

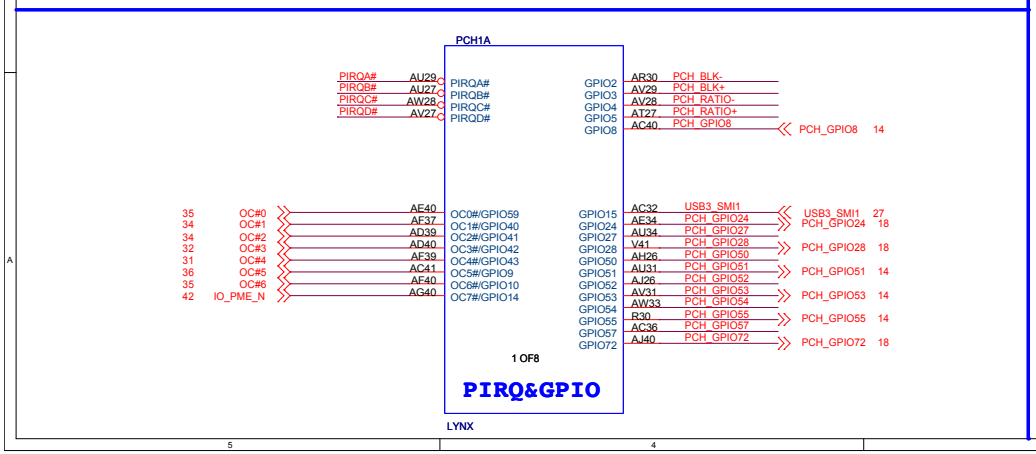

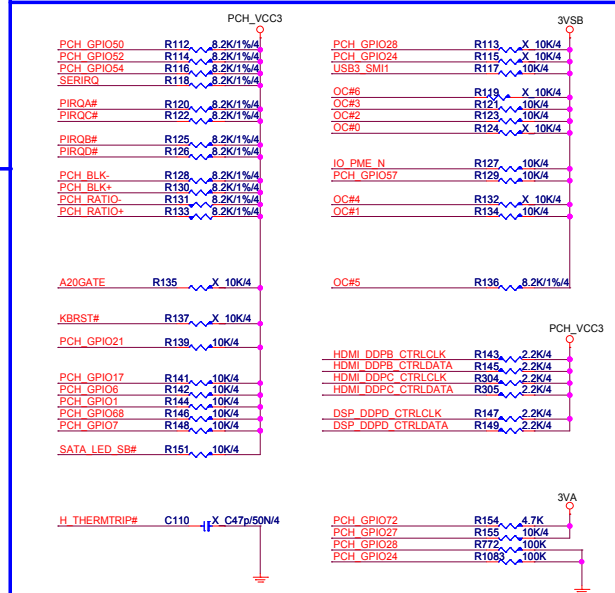

	GPIO16	GPIO49
0	PCIE	PCIE
1	SATA (Default)	SATA

PCH_GPIO49 R138 0R/4
PCH_GPIO16 R140 0R/4
PCH_M.2_DET 38

FOR BIOS USED OPT BOM

PCH_VCC3
PCH_GPIO69 R152 10K/4
PCH_GPIO70 R153 10K/4
PCH_GPIO71 R150 10K/4
PCH_GPIO69 R306 X 10K/4
PCH_GPIO70 R307 X 10K/4
PCH_GPIO71 R309 X 10K/4

MSI

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Size	Document Description	Rev
Custom	LYNX-SATA/HOST/FAN/GPIO/VGA	1.0

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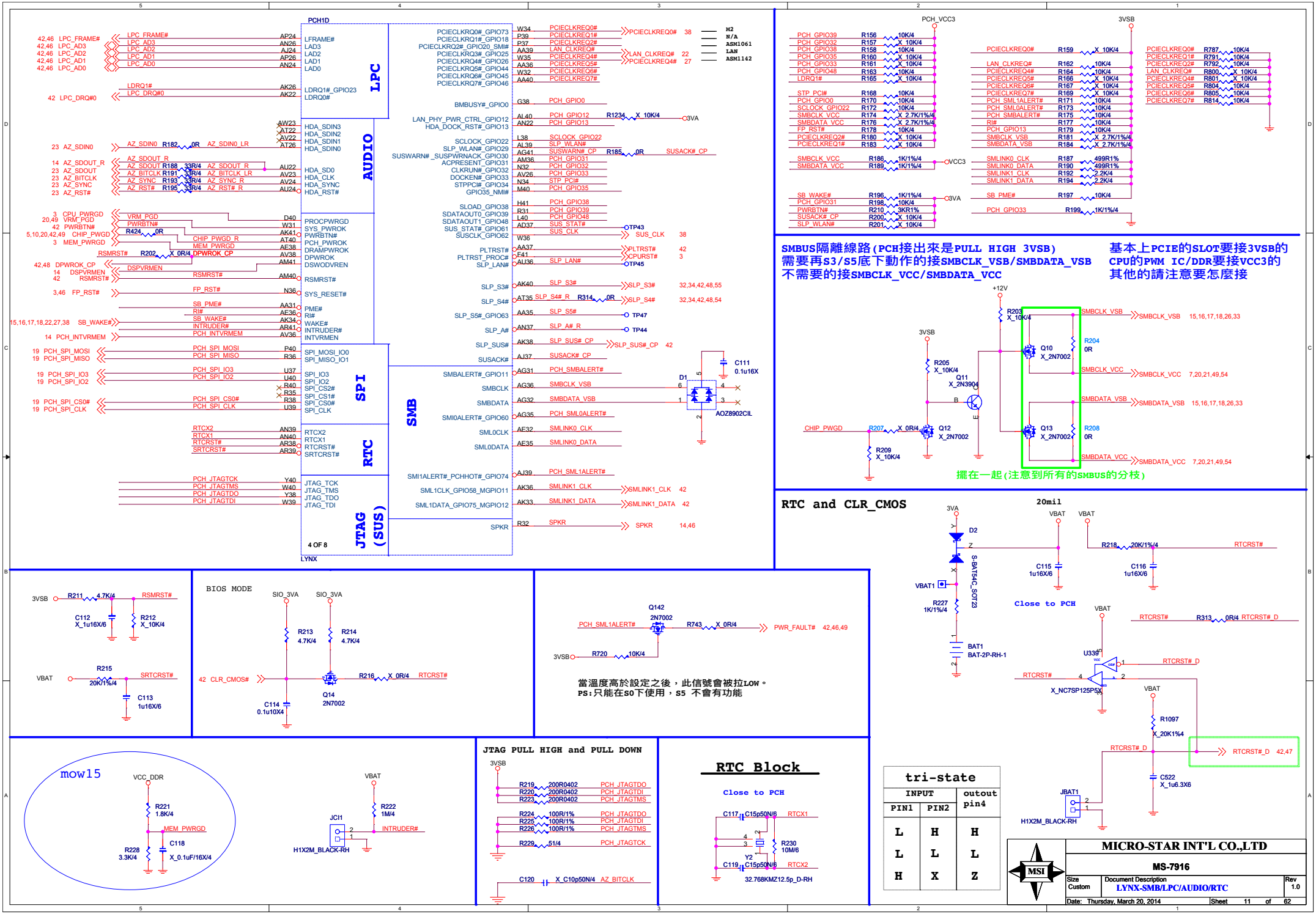
PCH1D
LPC
AUDIO
SPI
RTC
JTAG (SUS)
SMB
LFRAME#
LAD3
LAD2
LAD1
LAD0
LDRQ1#_GPIO23
LDRQ0#
HDA_SDIN3
HDA_SDIN2
HDA_SDIN1
HDA_SDIN0
HDA_SD0
HDA_CLK
HDA_SYNC
HDA_RST#
PROCPWRGD
SYS_PWROK
PWRBTN#
PCH_PWROK
DRAMPWROK
DPWROK
DSWODVREN
RSMRST#
SYS_RESET#
PME#
RI#
WAKE#
INTRUDER#
INTVRMEN
SPI_MOSI_IO0
SPI_MISO_IO1
SPI_IO3
SPI_IO2
SPI_CS2#
SPI_CS1#
SPI_CS0#
SPI_CLK
RTCX2
RTCX1
RTCRST#
SRTCRST#
JTAG_TCK
JTAG_TMS
JTAG_TDO
JTAG_TDI
4 OF 8
LYNX
SMBALERT#_GPIO11
SMBCLK
SMBDATA
SMI0ALERT#_GPIO60
SML0CLK
SML0DATA
SMI1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO58_MGPIO11
SML1DATA_GPIO75_MGPIO12
SPKR
PCIECLKRQ0#_GPIO73
PCIECLKRQ1#_GPIO18
PCIECLKRQ2#_GPIO20_SMI#
PCIECLKRQ3#_GPIO25
PCIECLKRQ4#_GPIO26
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
BMBUSY#_GPIO0
LAN_PHY_PWR_CTRL_GPIO12
HDA_DOCK_RST#_GPIO13
SCLOCK_GPIO22
SLP_WLAN#_GPIO29
SUSWARN#_SUSPWRNACK_GPIO30
ACPRESENT_GPIO31
CLKRUN#_GPIO32
DOCKEN#_GPIO33
STPPCI#_GPIO34
GPIO35_NMI#
SLOAD_GPIO38
SDATAOUT0_GPIO39
SDATAOUT1_GPIO48
SUS_STAT#_GPIO61
SUSCLK_GPIO62
PLTRST#
SLP_S3#
SLP_S4#
SLP_S5#_GPIO63
SLP_A#
SLP_SUS#
SUSACK#
PCH_SMBALERT#
SMBCLK_VSB
SMBDATA_VSB
PCH_SML0ALERT#
SMLINK0_CLK
SMLINK0_DATA
PCH_SML1ALERT#
SMLINK1_CLK
SMLINK1_DATA
SPKR
PCIECLKREQ0#
PCIECLKREQ1#
PCIECLKREQ2#
LAN_CLKREQ#
PCIECLKREQ4#
PCIECLKREQ5#
PCIECLKREQ6#
PCIECLKREQ7#
PCH_GPIO0
PCH_GPIO12
PCH_GPIO13
SCLOCK_GPIO22
SLP_WLAN#
SUSWARN# CP
PCH_GPIO31
PCH_GPIO32
PCH_GPIO33
STP_PCI#
PCH_GPIO35
SUS_STAT#
SUS_CLK
SLP_LAN#
SLP_S3#
SLP_S4#_R
SLP_S5#
SLP_A#_R
SLP_SUS# CP
SUSACK# CP
PCH_SMBALERT#
SMBCLK_VSB
SMBDATA_VSB
PCH_SML0ALERT#
SMLINK0_CLK
SMLINK0_DATA
PCH_SML1ALERT#
SMLINK1_CLK
SMLINK1_DATA
SUSACK#_CP
PCH_GPIO38
PCH_GPIO39
PCH_GPIO48
TP43
TP47
TP44
TP45
R1234 X_10K/4
R185 0R
R314 0R
M2
N/A
ASM1061
LAN
ASM1142
AOZ8902CIL
C111 0.1u16X
3VA
SUSACK# CP
SUSACK#_CP
SUS_CLK
SUS_SUS#
SUS_SUS#_CP
SLP_S3#
SLP_S4#
SLP_S5#
SLP_A#_R
SLP_LAN#
SMBCLK_VSB
SMBDATA_VSB
SMLINK0_CLK
SMLINK0_DATA
SMLINK1_CLK
SMLINK1_DATA
PCIECLKREQ0#
LAN_CLKREQ#
PCIECLKREQ4#
PCIECLKREQ5#
PCIECLKREQ6#
PCIECLKREQ7#
PCH_SML1ALERT#
PCH_SMBALERT#
RI#
PCH_GPIO13
SMBCLK_VSB
SMBDATA_VSB
SB_PME#
PCH_GPIO33
PCH_GPIO39
PCH_GPIO48
PCH_GPIO32
PCH_GPIO38
PCH_GPIO35
PCH_GPIO33
LDRQ1#
PCH_GPIO0
SCLOCK_GPIO22
SMBCLK_VCC
SMBDATA_VCC
FP_RST#
PCIECLKREQ2#
PCIECLKREQ1#
SB_WAKE#
PCH_GPIO31
PWRBTN#
SUSACK# CP
SLP_WLAN#
PCH_VCC3
3VSB
VCC3
R156 10K/4
R157 X_10K/4
R158 10K/4
R160 X_10K/4
R161 X_10K/4
R163 10K/4
R165 X_10K/4
R168 10K/4
R170 10K/4
R172 10K/4
R174 X_2.7K/1%/4
R176 X_2.7K/1%/4
R178 10K/4
R180 X_10K/4
R183 X_10K/4
R186 1K/1%/4
R189 1K/1%/4
R196 1K/1%/4
R198 10K/4
R210 3KR1%
R200 X_10K/4
R201 X_10K/4
R159 X_10K/4
R162 10K/4
R164 10K/4
R166 X_10K/4
R167 X_10K/4
R169 X_10K/4
R171 10K/4
R173 10K/4
R175 10K/4
R177 10K/4
R179 10K/4
R181 X_2.7K/1%/4
R184 X_2.7K/1%/4
R187 499R1%
R190 499R1%
R192 2.2K/4
R194 2.2K/4
R197 10K/4
R199 1K/1%/4
R787 10K/4
R791 10K/4
R792 10K/4
R800 X_10K/4
R801 X_10K/4
R804 10K/4
R805 10K/4
R814 10K/4
SMBUS隔離線路(PCH接出來是PULL HIGH 3VSB)
需要再S3/S5底下動作的接SMBCLK_VSB/SMBDATA_VSB
不需要的接SMBCLK_VCC/SMBDATA_VCC
基本上PCIE的SLOT要接3VSB的
CPU的PWM IC/DDR要接VCC3的
其他的請注意要怎麼接
+12V
R203 X_10K/4
R204 0R
R205 X_10K/4
Q10 X_2N7002
Q11 X_2N3904
Q12 X_2N7002
Q13 X_2N7002
R207 X_0R/4
R208 0R
R209 X_10K/4
CHIP_PWGD
SMBCLK_VCC
SMBDATA_VCC
7,20,21,49,54
15,16,17,18,26,33
擺在一起(注意到所有的SMBUS的分枝)
RTC and CLR_CMOS
20mil
VBAT
D2
S-BAT54C_SOT23
VBAT1
R227 1K/1%/4
BAT1
BAT-2P-RH-1
C115 1u16X/6
C116 1u16X/6
R218 20K/1%/4
RTCRST#
Close to PCH
R313 0R/4
RTCRST#_D
U339
X_NC7SP125P5X
R1097 X_20K/1%/4
C522 X_1u6.3X6
JBAT1
H1X2M_BLACK-RH
42,47
3VSB
R211 4.7K/4
RSMRST#
C112 X_1u16X/6
R212 X_10K/4
R215 20K/1%/4
SRTCRST#
C113 1u16X/6
BIOS MODE
SIO_3VA
R213 4.7K/4
R214 4.7K/4
42 CLR_CMOS#
R216 X_0R/4
RTCRST#
C114 0.1u10X4
Q14 2N7002
Q142 2N7002
PCH_SML1ALERT#
R743 X_0R/4
PWR_FAULT# 42,46,49
R720 10K/4
當溫度高於設定之後，此信號會被拉LOW。
PS:只能在S0下使用，S5 不會有功能
tri-state
INPUT
PIN1
PIN2
outout pin4
L H H
L L L
H X Z
mow15
VCC_DDR
R221 1.8K/4
MEM_PWRGD
C118 X_0.1uF/16X/4
R228 3.3K/4
VBAT
JCI1
R222 1M/4
INTRUDER#
H1X2M_BLACK-RH
JTAG PULL HIGH and PULL DOWN
R219 200R0402 PCH_JTAGTDO
R220 200R0402 PCH_JTAGTDI
R223 200R0402 PCH_JTAGTMS
R224 100R/1% PCH_JTAGTDO
R225 100R/1% PCH_JTAGTDI
R226 100R/1% PCH_JTAGTMS
R229 51/4 PCH_JTAGTCK
C120 X_C10p50N/4 AZ_BITCLK
RTC Block
Close to PCH
C117 C15p50N/6 RTCX1
R230 10M/6
Y2
C119 C15p50N/6 RTCX2
32.768KMZ12.5p_D-RH
MICRO-STAR INT'L CO.,LTD
MS-7916
Size Custom
Document Description LYNX-SMB/LPC/AUDIO/RTC
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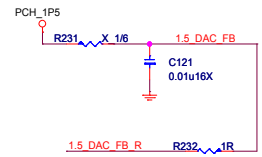
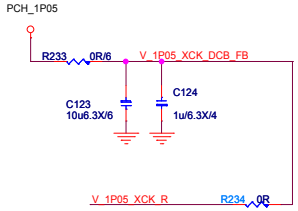
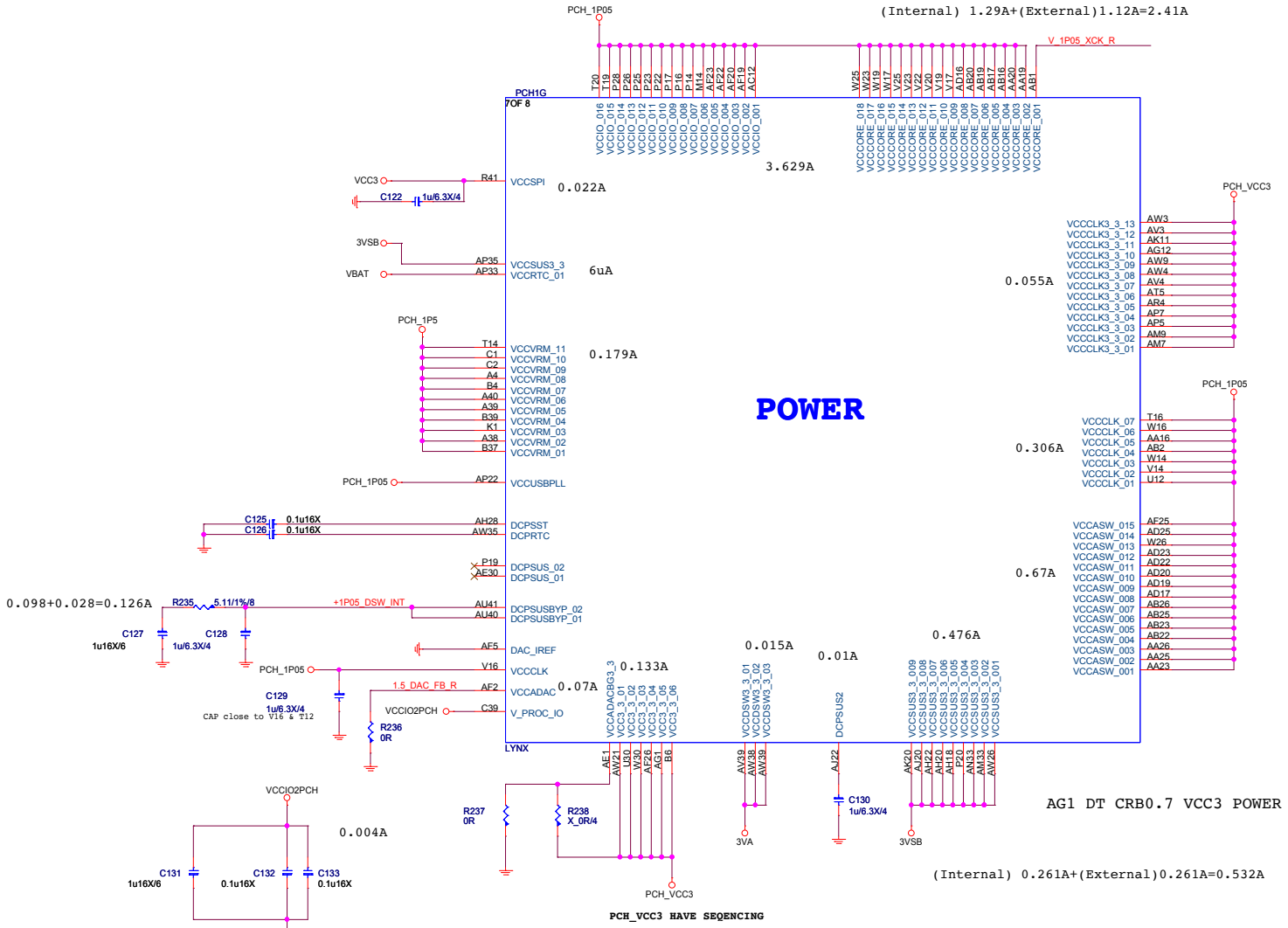
Change to 10UH if
VCCA_DPLLA/VCCA_DPLLB
has noise issue.





AF25 ;AD25 DT CRB0.7 ASW POWER

(Internal) 1.29A+(External)1.12A=2.41A

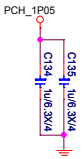


POWER

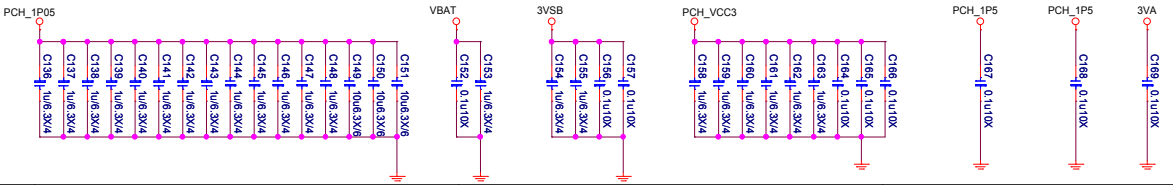
AG1 DT CRB0.7 VCC3 POWER

(Internal) 0.261A+(External)0.261A=0.532A

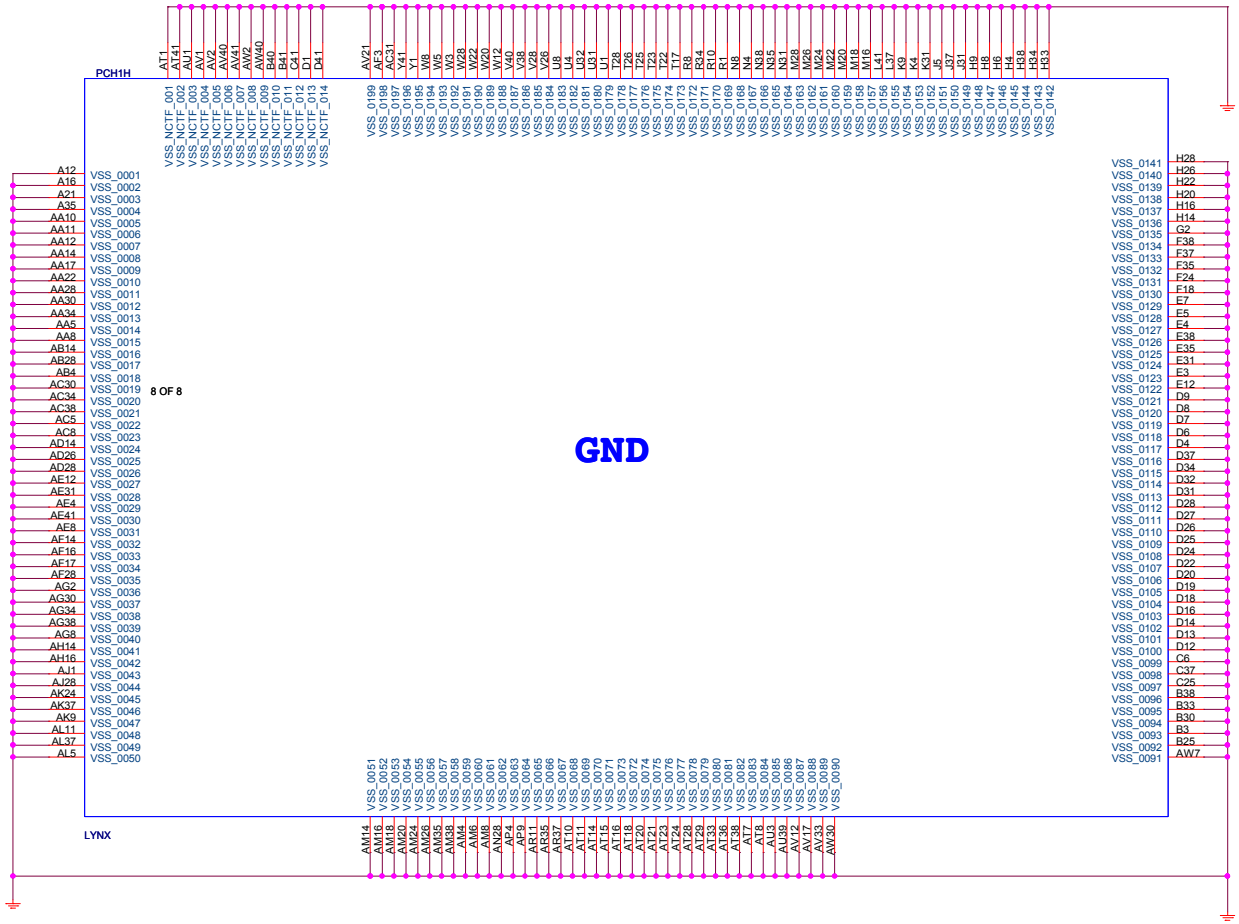
BACKSIDE for V14,U12,T6,V16



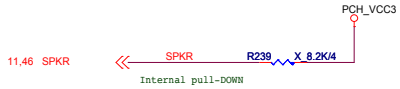
PCH decoupling cap

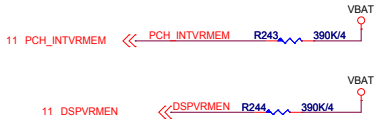


MICRO-STAR INT'L CO.,LTD		
MS-7916		
Size: Custom	Document Description: LYNX -POWER PIN	Rev: 1.0
Date: Thursday, March 20, 2014	Sheet 12 of 62	

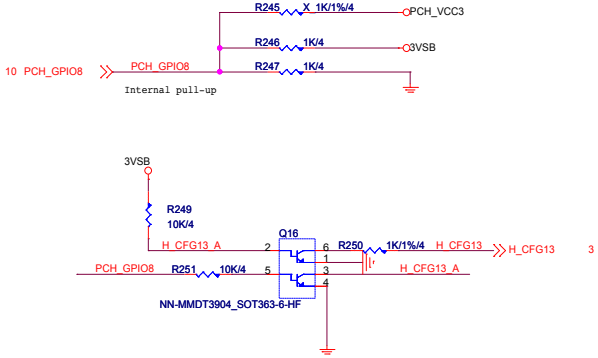


MICRO-STAR INT'L CO.,LTD	
MS-7916	
Size: Custom	Document Description: LYNX-GND
Rev: 1.0	
Date: Thursday, March 20, 2014	Sheet 13 of 62



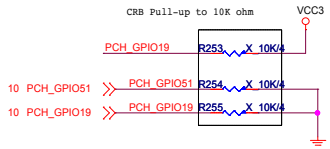


GPIO8



GPIO19 & GPIO51

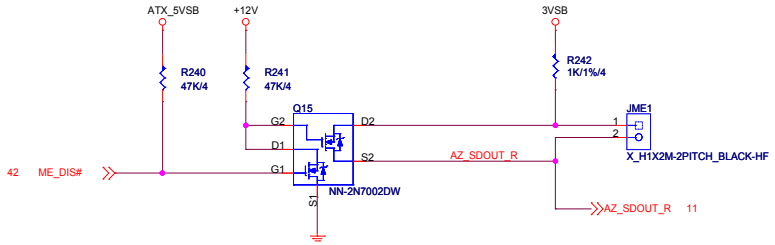
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1



Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

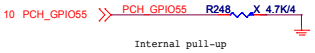
Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO55

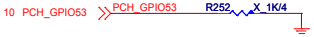
TOP BIOCK SWAP MODE



GPIO55
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

GPIO53



GPIO53
Connect to ground with 1k Ohm pull-down resistor.

GPIO36 & GPIO37

MICRO-STAR INT'L CO.,LTD	
MS-7916	
Size: Custom	Document Description: LYNX STRAPS
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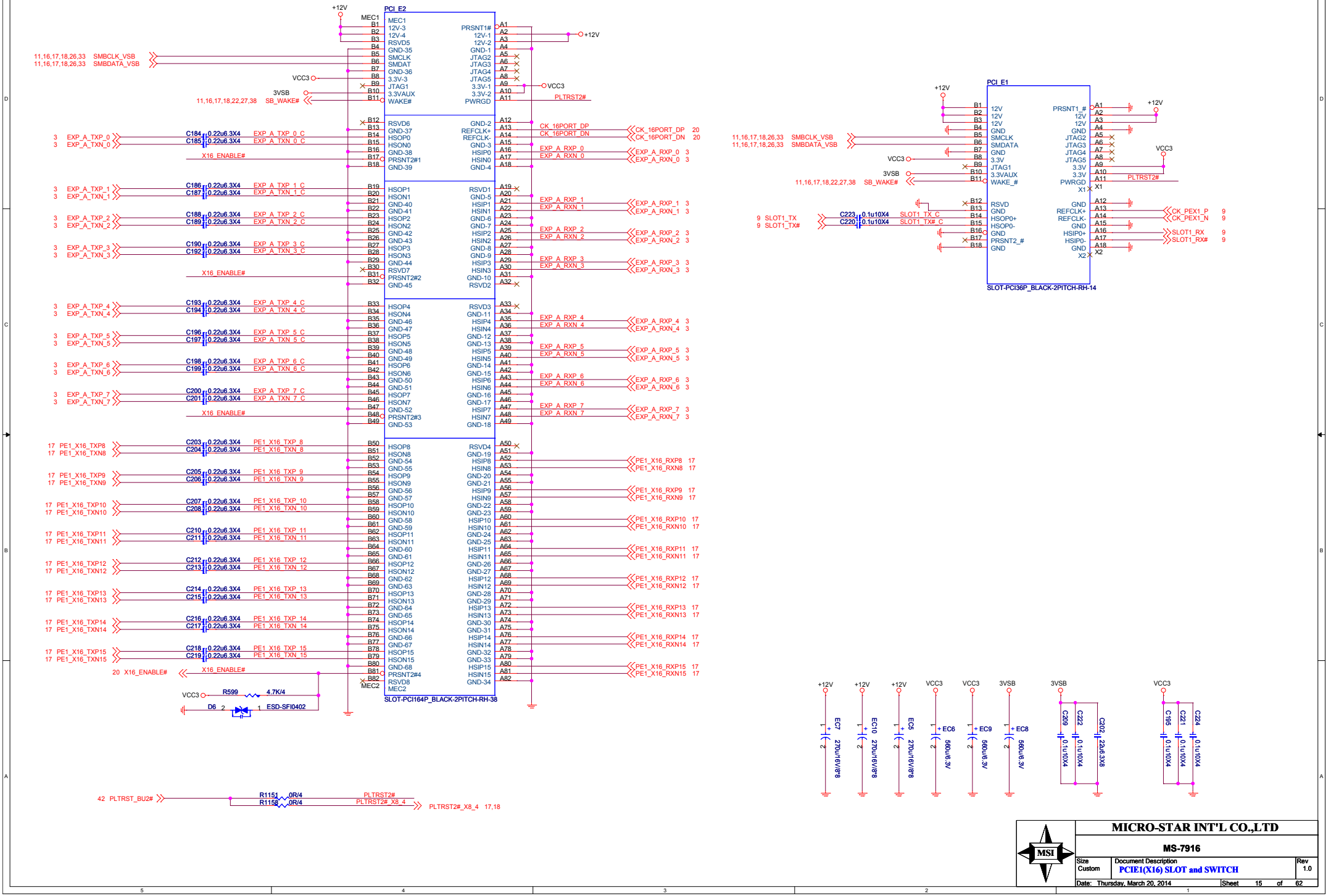
PCI_E2
SLOT-PCI164P_BLACK-2PITCH-RH-38
PCI_E1
SLOT-PCI36P_BLACK-2PITCH-RH-14
MICRO-STAR INT'L CO.,LTD
MS-7916
PCIE1(X16) SLOT and SWITCH
Size Custom
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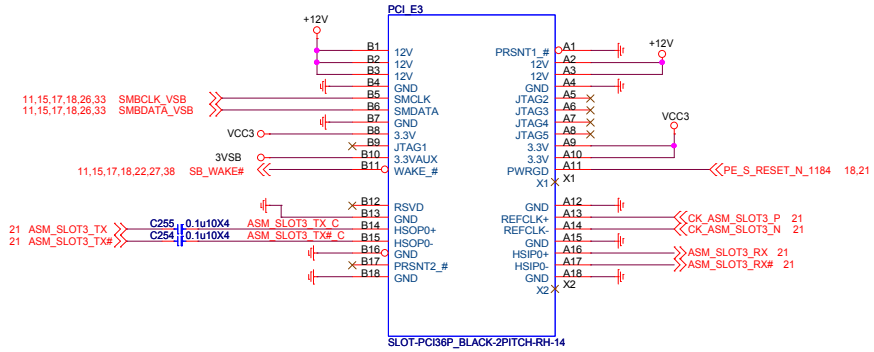

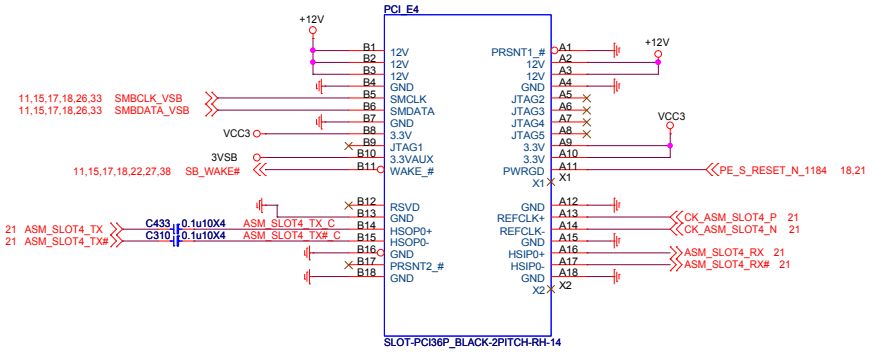

MICRO-STAR INT'L CO.,LTD

MS-7916

Size	Document Description	Rev
Custom	PCIE2(x16)PCIE7(x8)	1.0

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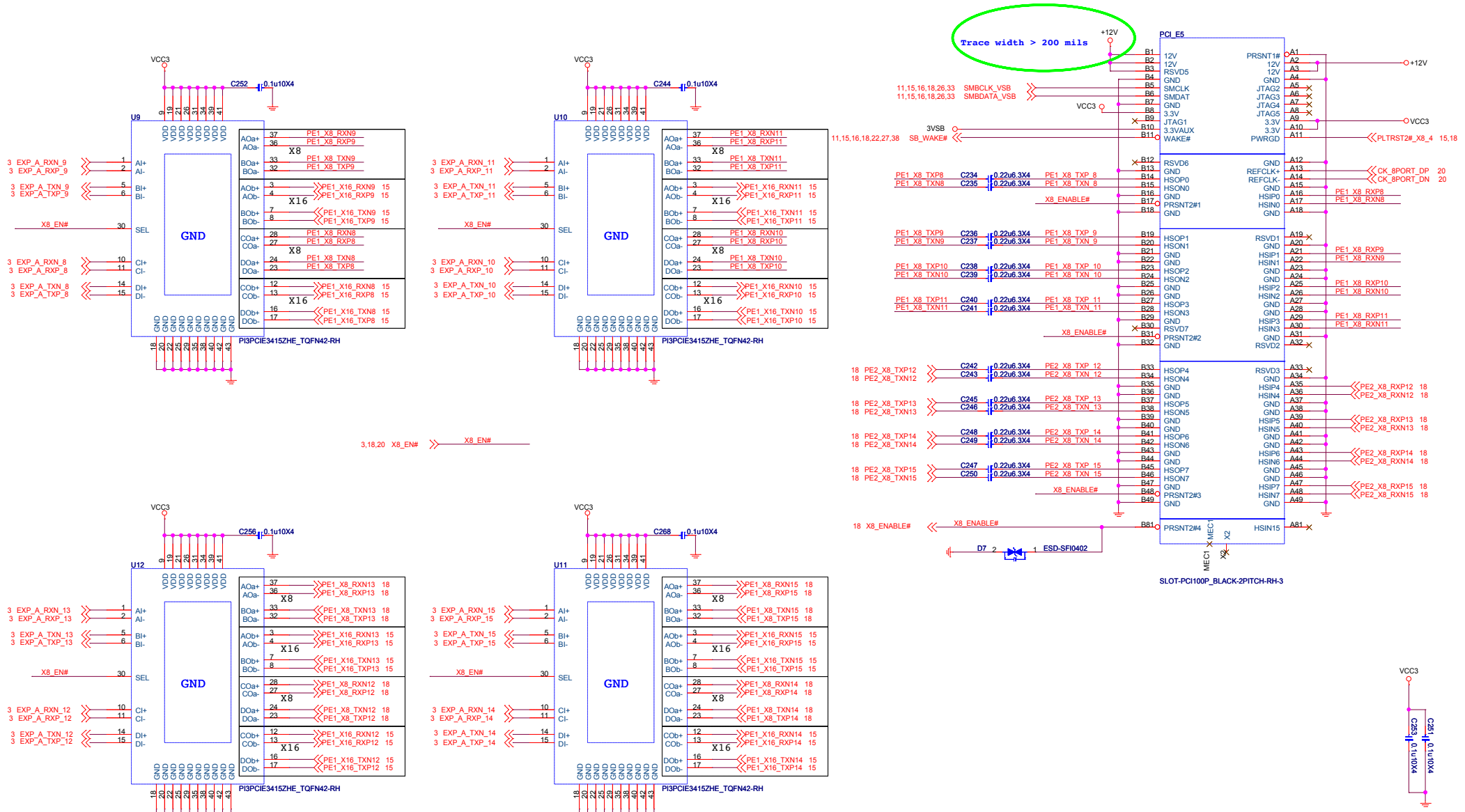
PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



MICRO-STAR INT'L CO.,LTD	
MS-7916	
Size: Custom	Document Description: PCIE3(X8)PCIE7(x8) SLOT
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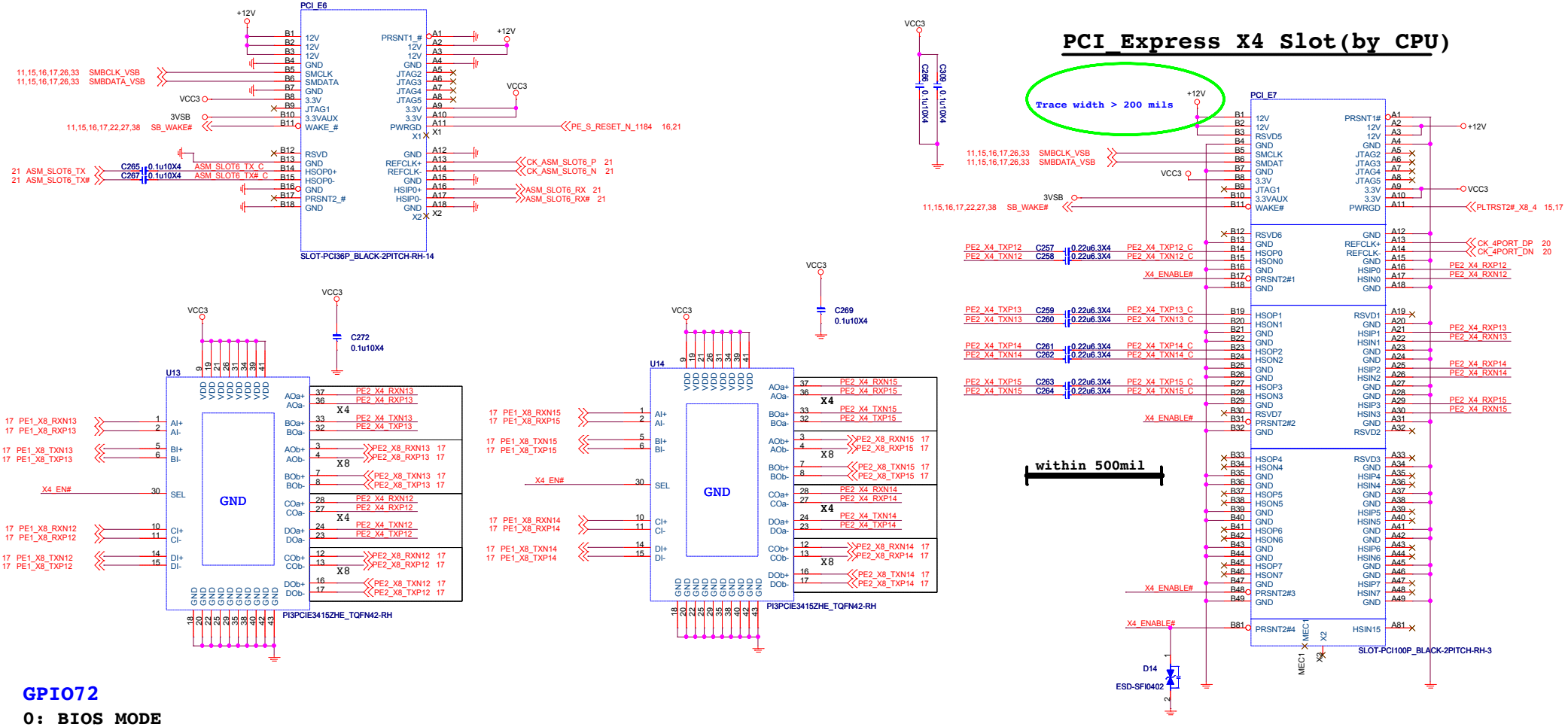
PCI_Express X4 Slot(by CPU)



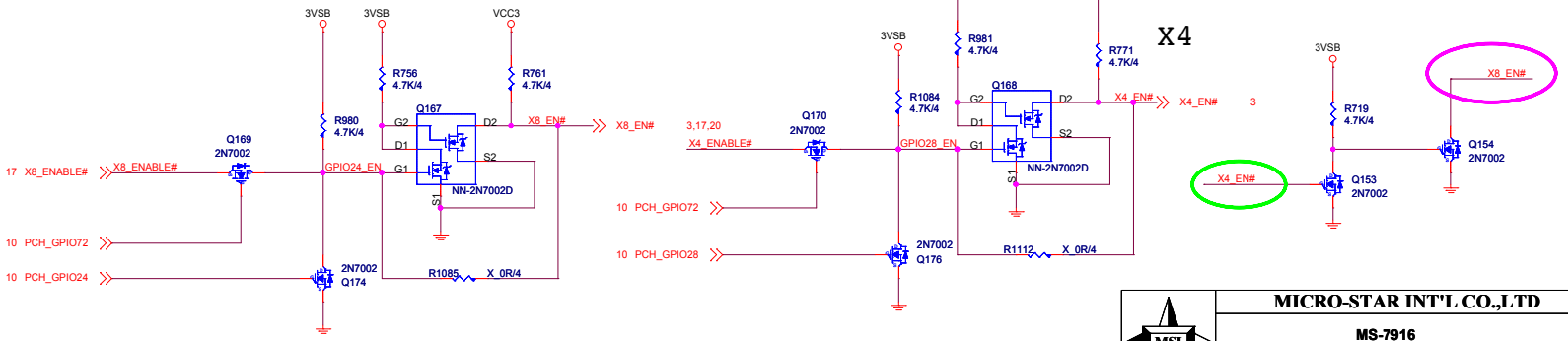
GPIO72

0: BIOS MODE
1: HW MODE

If USE HW MODE (Default)
PCH_GPIO24 & PCH_GPIO28 programming to GPI
PCH_GPIO72 programming GPO

If USE BIOS MODE
PCH_GPIO24 & PCH_GPIO28 & PCH_GPIO70
programming to GPO

PCH Status	GPIO24	GPIO28	GPIO72
AUTO	GPI	GPI	1
16,0,0	0	0	0
8,8,0	1	0	0
8,4,4	1	1	0



MICRO-STAR INT'L CO.,LTD	
MS-7916	
Size: Custom	Document Description: PCIE5(X16) SLOT and SWITCH
Rev: 1.0	
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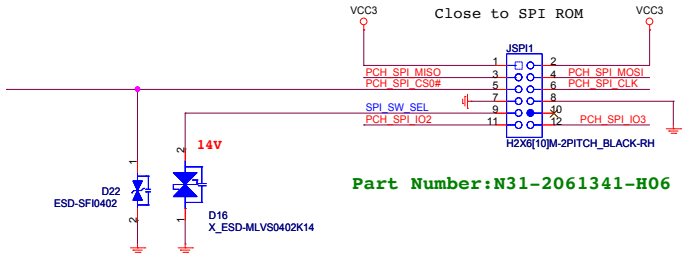
11 PCH_SPI_CS0# <<PCH_SPI_CS0#

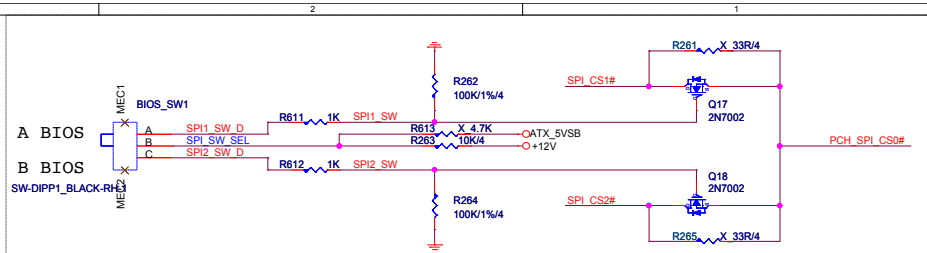
11 PCH_SPI_MOSI <<PCH_SPI_MOSI
11 PCH_SPI_MISO <<PCH_SPI_MISO
11 PCH_SPI_CLK <<PCH_SPI_CLK
11 PCH_SPI_IO2 <<PCH_SPI_IO2
11 PCH_SPI_IO3 <<PCH_SPI_IO3

SPI DEBUG PROT

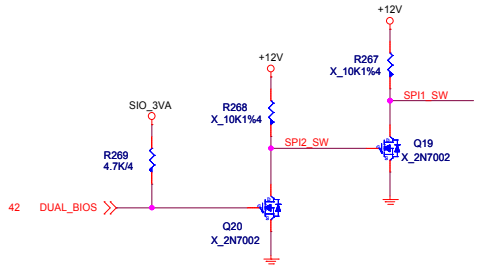
Close to SPI ROM

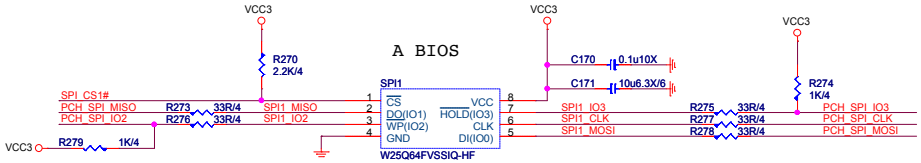


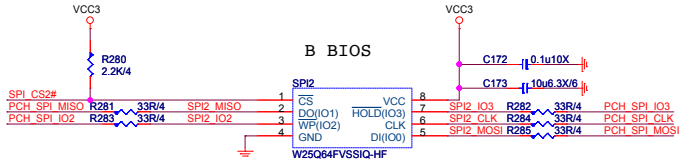
Part Number:N31-2061341-H06



BIOS MODE



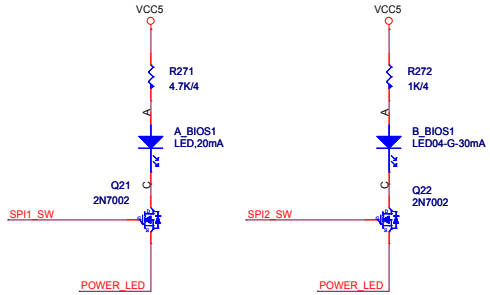


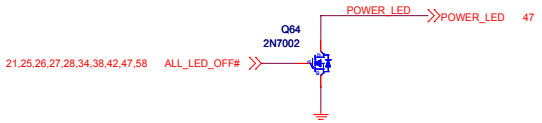


SPI FLASH ROM

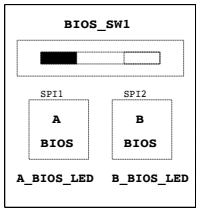
Place close to SB.

*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.

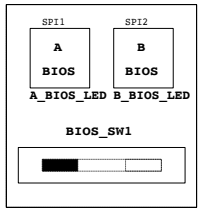




Placement 1



Placement 2



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
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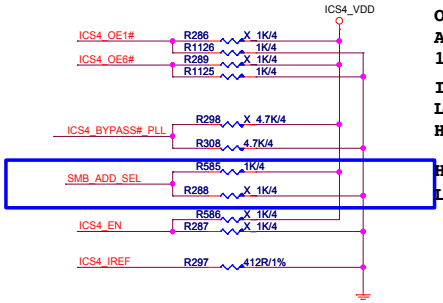
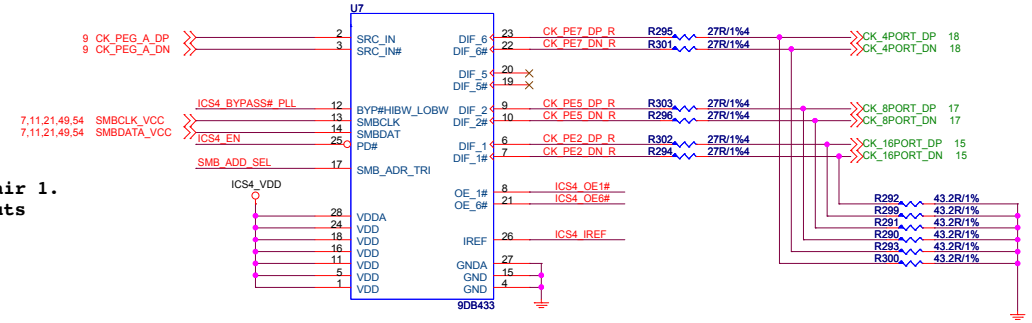
For PCIE Clock Jitter Issue



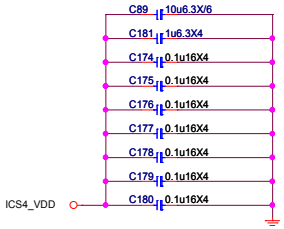
OE1# OE6#
Active low input for enabling DIF pair 1.
1 =disable outputs, 0 = enable outputs

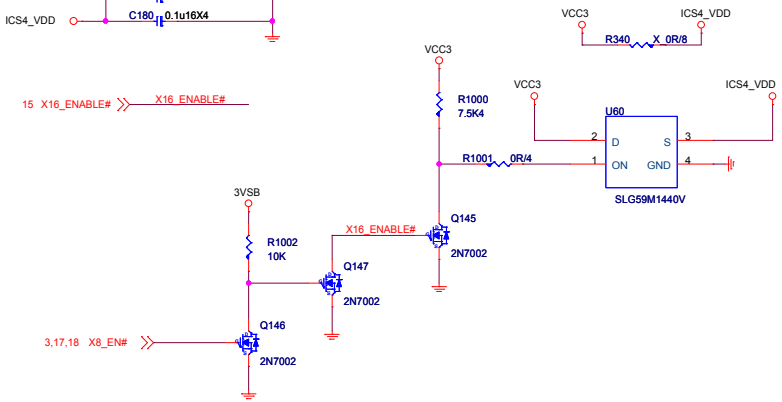
ICS4_BYPASS#_PLL
LOW:BYPASS
HIGH:PLL

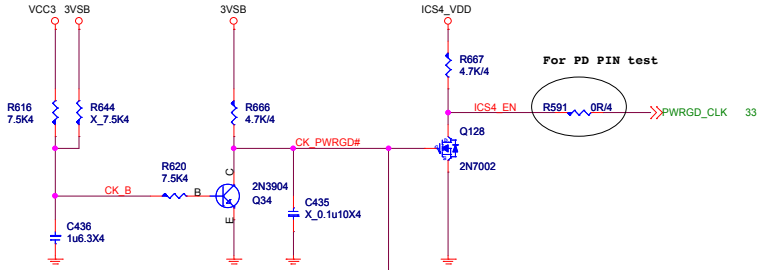
HIGH Address: D8/D9
LOW Address: DA/DB

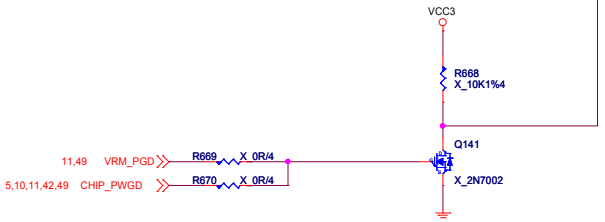


Address: D8/D9









MICRO-STAR INT'L CO.,LTD		
MS-7916		
Size: Custom	Document Description: Clock BUFFER831	Rev: 1.0
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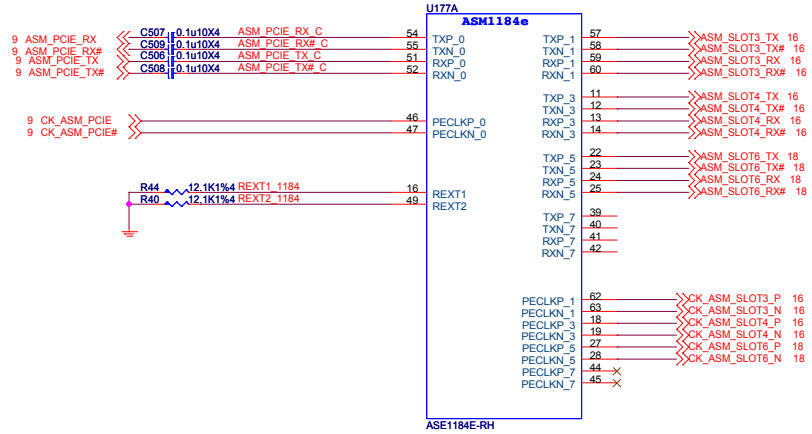
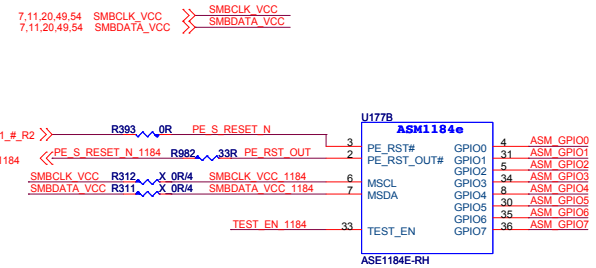
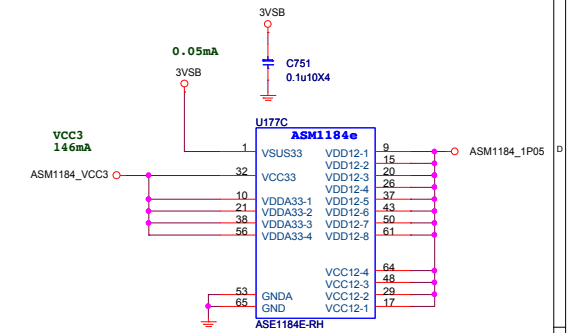
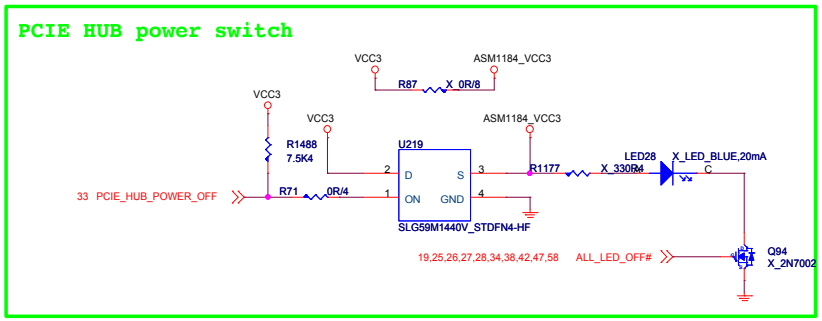
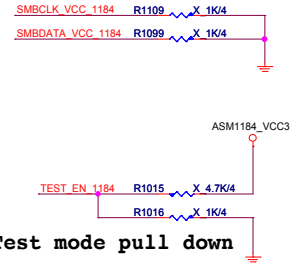
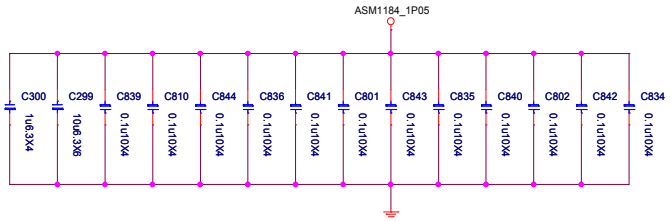










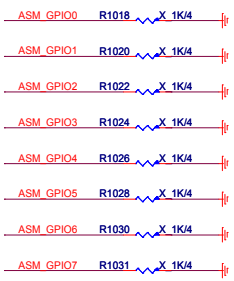


GPIO0	0:PLL mode; 1: bypass mode
GPIO1	clock buffer termination 0: disable ; 1: enable
GPIO2	Reserved for test mode
GPIO3	Reserved for ASM1184e
GPIO4	SMBus enable
GPIO5	SMBus address[0]
GPIO6	SMBus address[1]
GPIO7	SMBus address[2]
MSCL	I2C enable

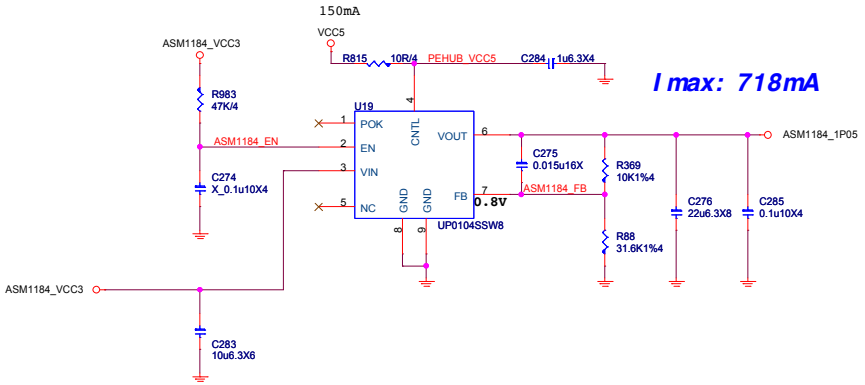
GPIO4	MSCL	Function
0	0	(MSCL,MSDA) is no function
0	1	(MSCL,MSDA) is I2C,chip is master
1	0	(MSCL,MSDA) is SMBus, chip is salve
1	1	(MSCL,MSDA) is SMBus, chip is salve

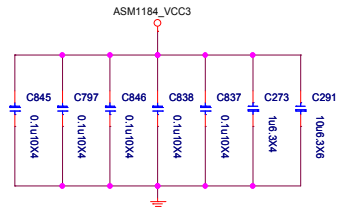
H/W Strapping

Internal pull high 50Kohm



ASM1184 PCIE HUB core Power





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Custom	ASM1184e PCIE HUB	1.0

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E2205-B Giga LAN

Pull-up resister RL1 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

LED0:
1=hi core voltage(overclocking)
0=low core voltage (non-overclocking)

LED1:
1=SWR mode
0=LDO mode

LED3:
1=25MHz clock
0=48MHz clock

CHOKEL1:
L04-47A7310-C08
L04-47A7680-T15

LL1:
L02-3018023-C08
L02-3018023-T19

VDD33 power trace should be wider than 30mils;
AVDD33 power trace should be wider than 30mils;
VDD_IO power trace should be wider than 30mils;
VDDIO_REG power trace should be wider than 20mils;
AVDDH power trace should be wider than 20mils;
AVDDL power traces should be wider than 20mils.
DVDDL power traces should be wider than 20mils.

10:
1. Support xD, not support SPI
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
01:
1. Support SPI, not support xD
2. Can support PPS, PPS at LED[0] or LED[1] or LED[2] which is selected by eFus
11:
1. Not support xD, not support SPI
2. Only support PPS, PPS always at CRIO13.

D0G-1020510-I05
D0G-8010510-SI0

D0G-05A050C-O05
D0G-05A0300-I14
D0G-06A050C-A68

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Size: Custom	Document Description: CLVRKVILLE_WGI218V	Rev: 1.0
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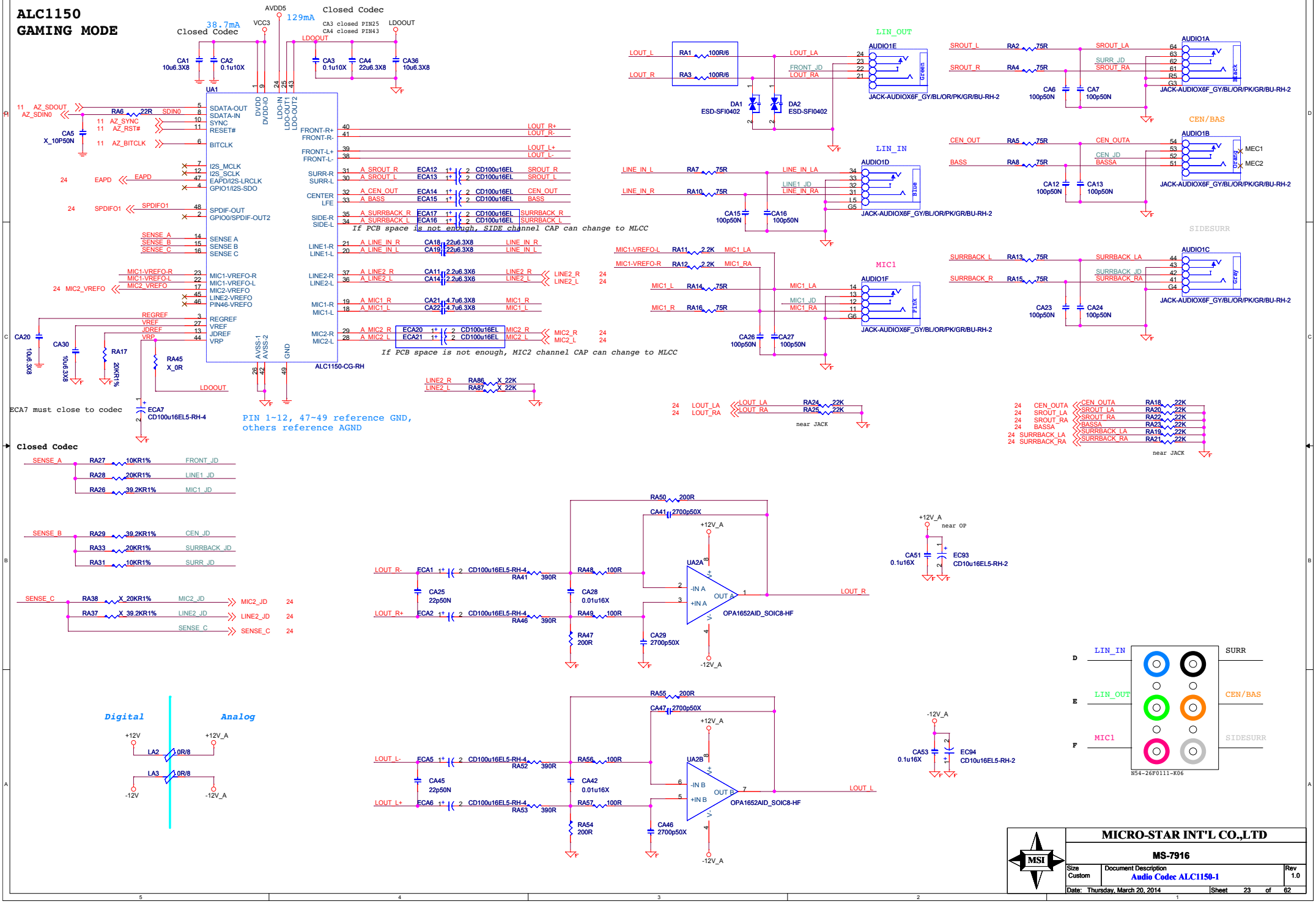
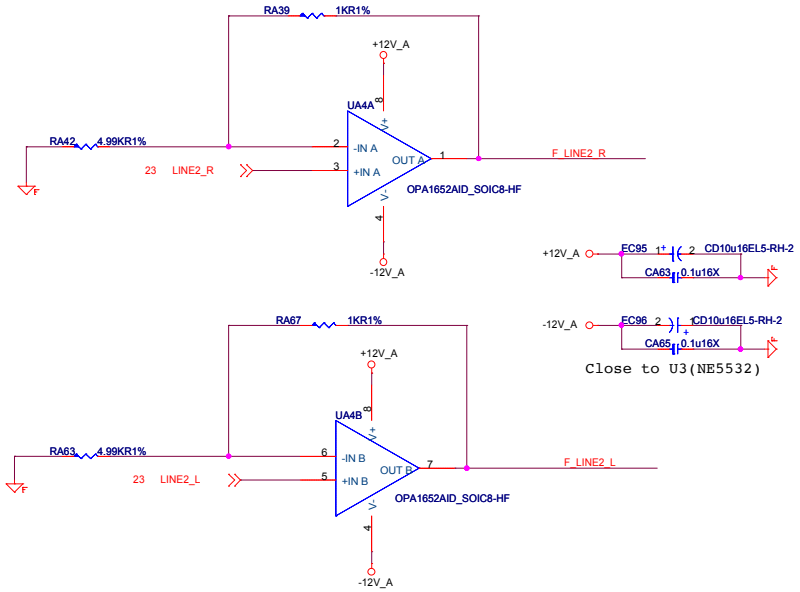
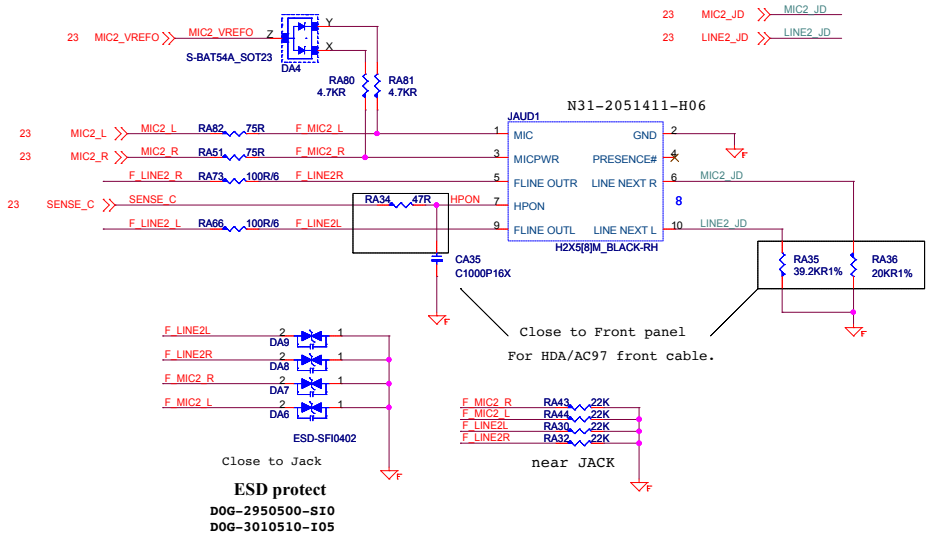
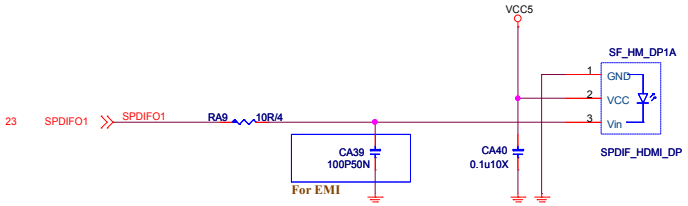
ALC1150
GAMING MODE





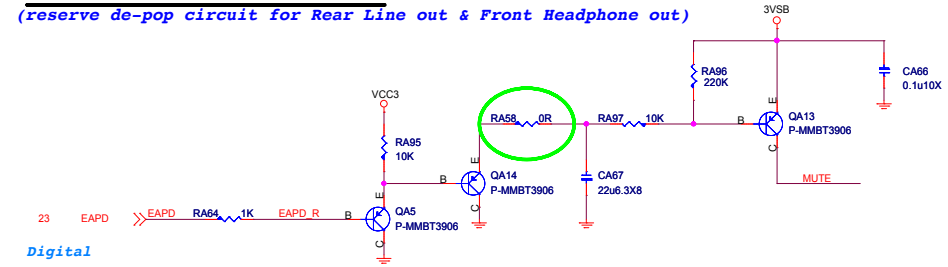


SPDIF OUT

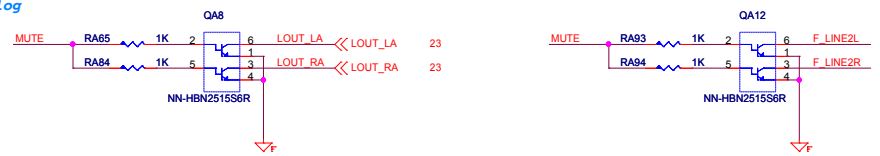


Rear Line OUT De-POP circuit

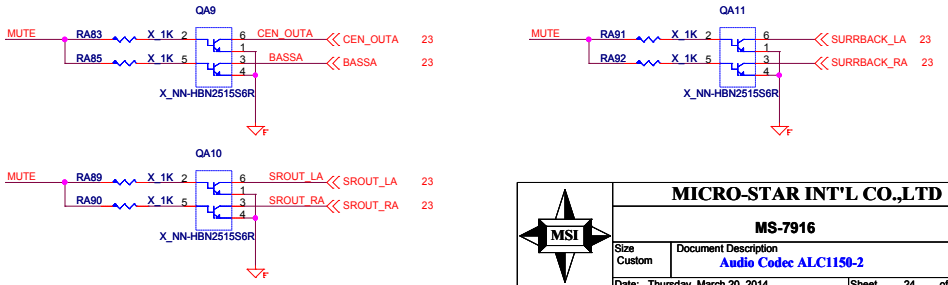
(reserve de-pop circuit for Rear Line out & Front Headphone out)



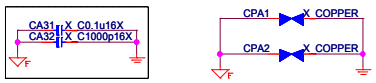
Analog



(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



EMI



MICRO-STAR INT'L CO.,LTD

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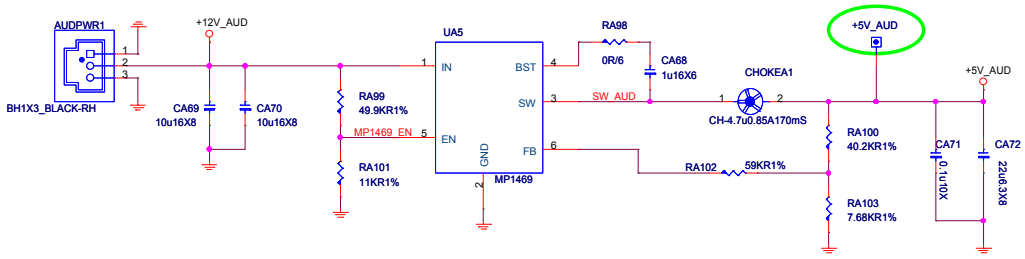
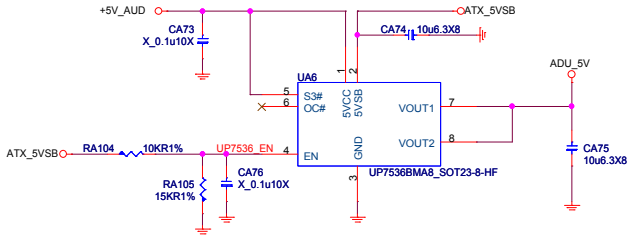
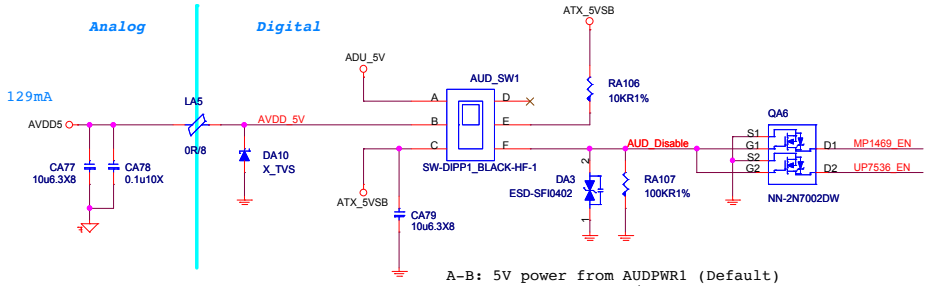
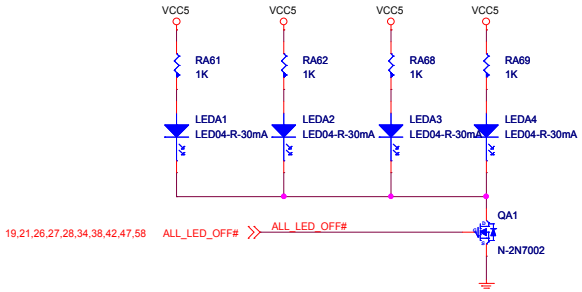


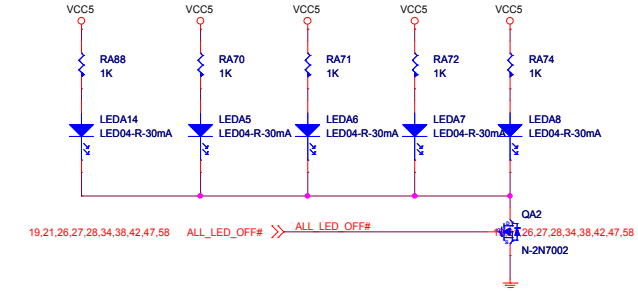


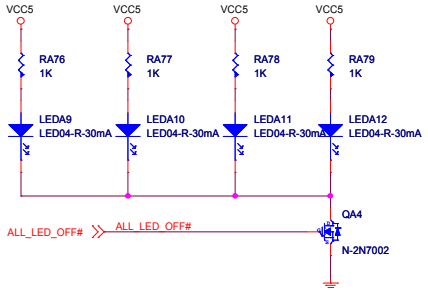


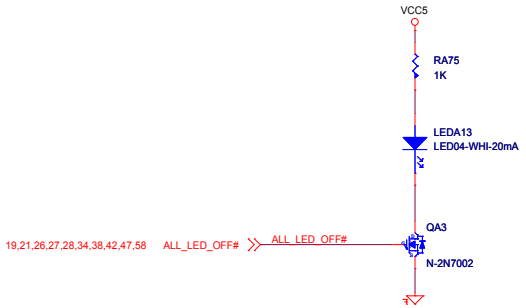
A-B: 5V power from AUDPWR1 (Default)
B-C: 5V power from M/B ATX_5VSB

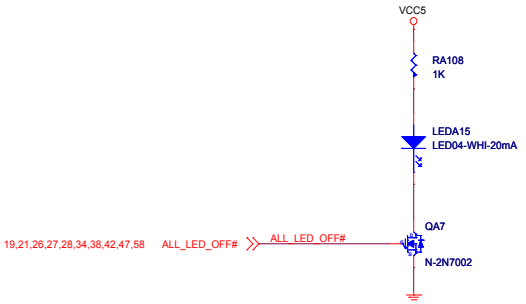
Audio moat is transparent and width 40mil

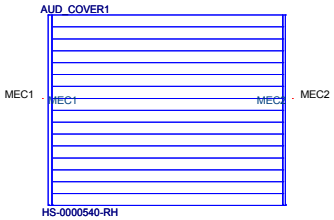












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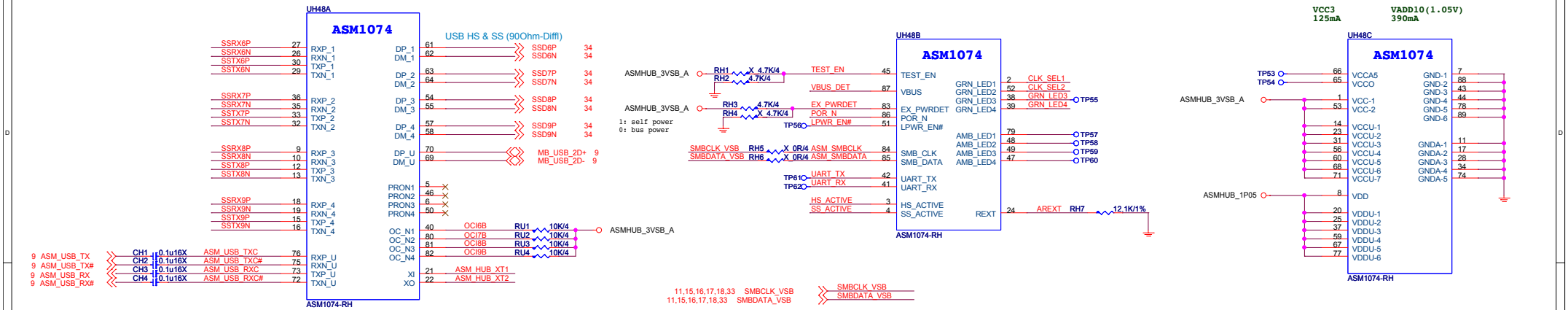
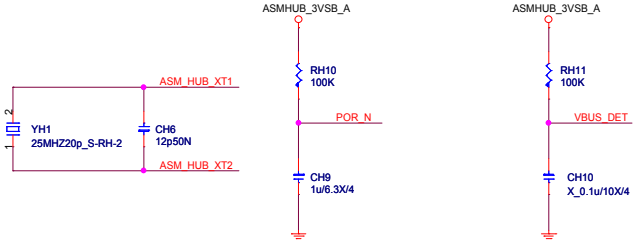
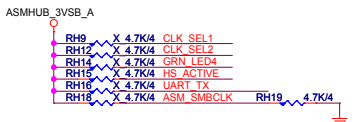




H/W Strapping

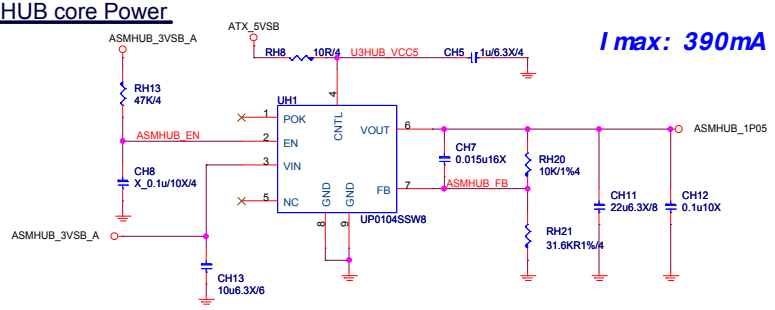


Strapping Table

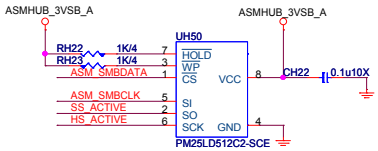
GRN_LED2 (CLK_SEL1)	GRN_LED1 (CLK_SEL0)	
0	0	25MHz Default
1	0	30MHz
1	1	20MHz

ASM1074 USB3.0 HUB core Power

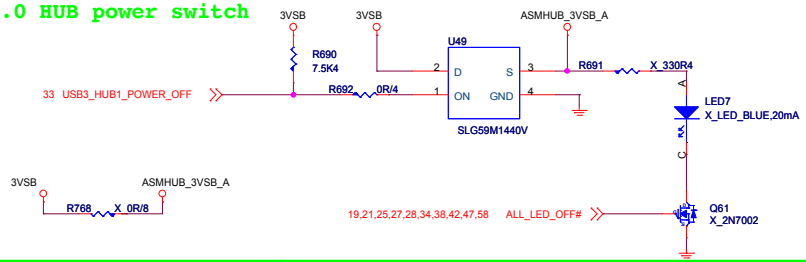
Imax: 390mA



Close to Connector



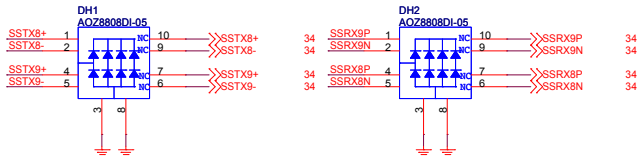
USB3.0 HUB power switch



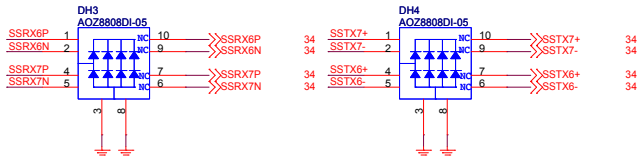
ESD Protection

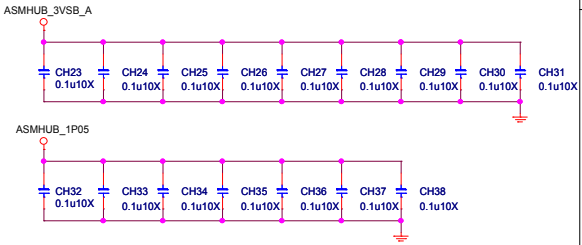
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

Close to Connector



Close to Connector





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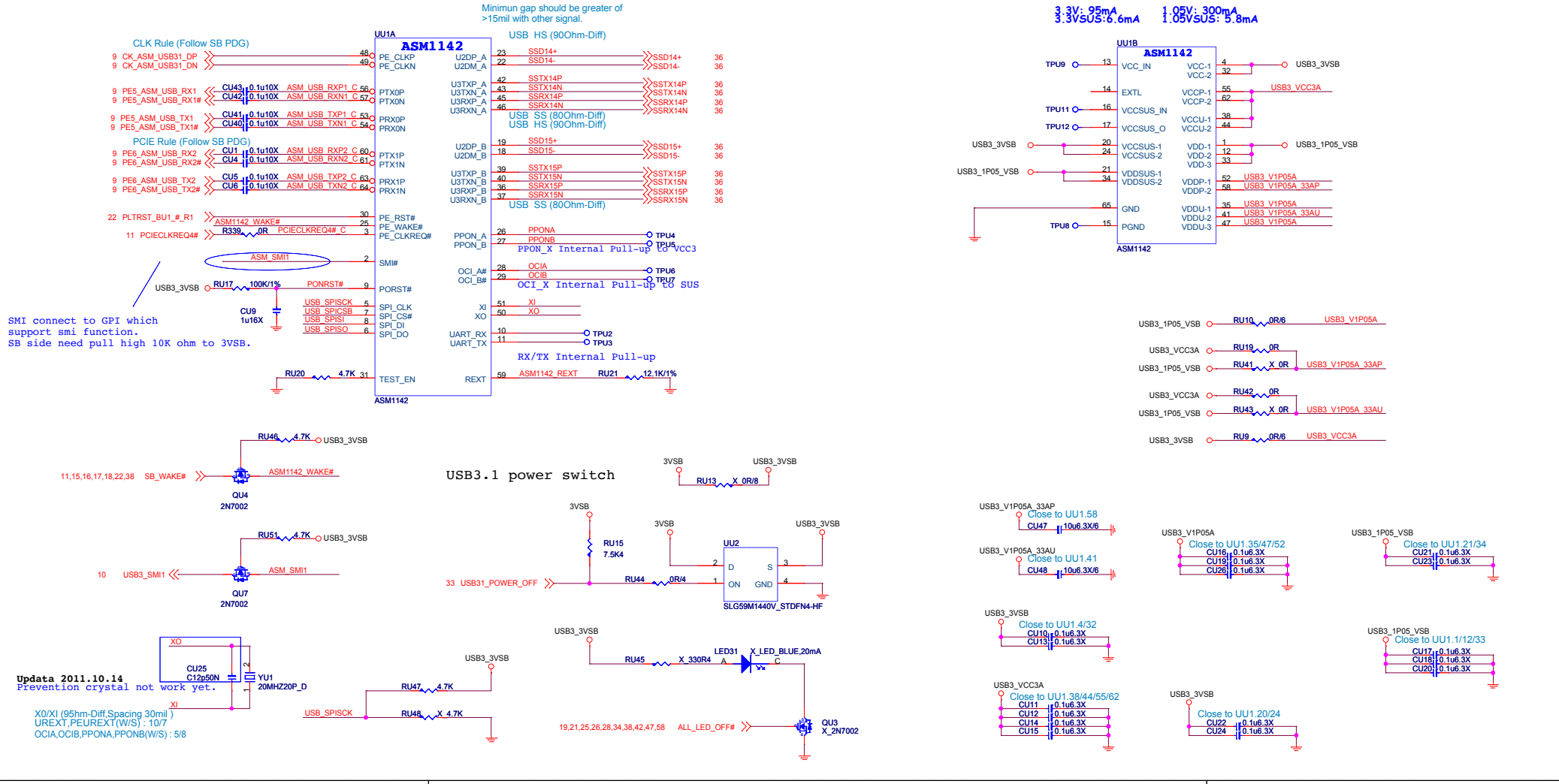
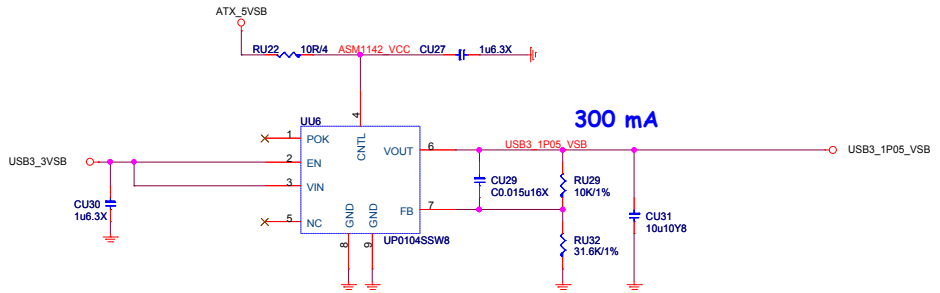
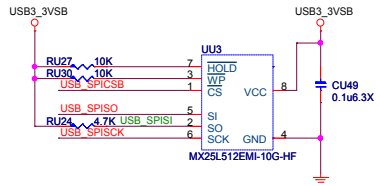


ASM1042 1.05 VSB Power



EEPROM



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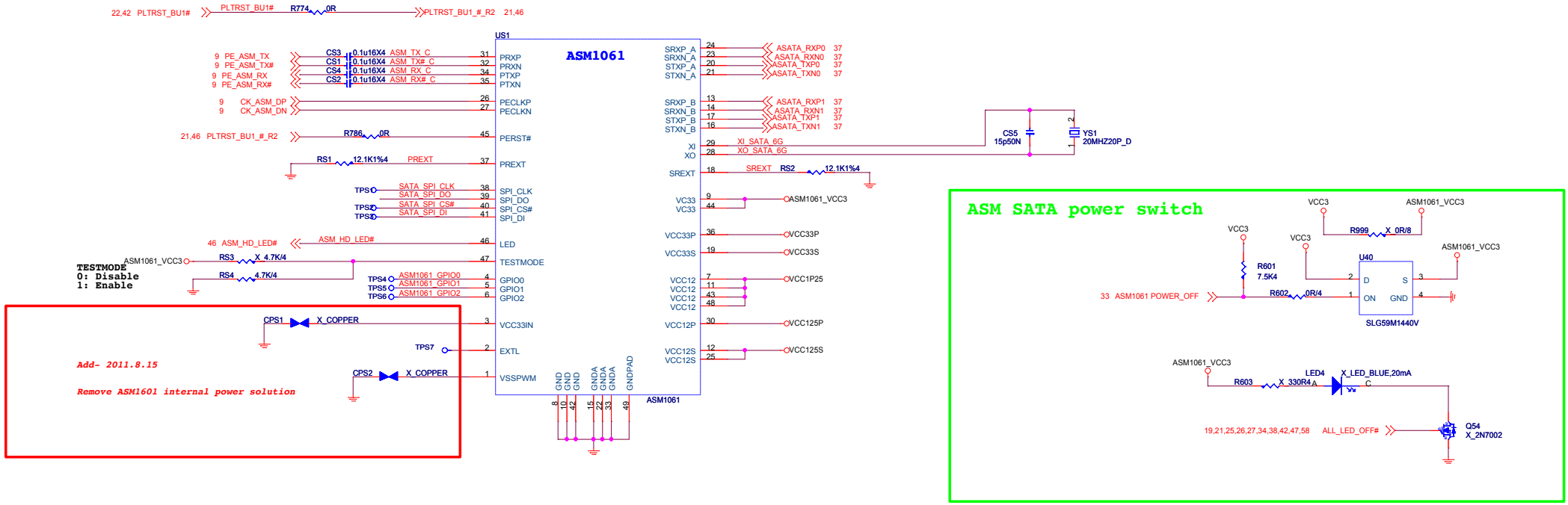
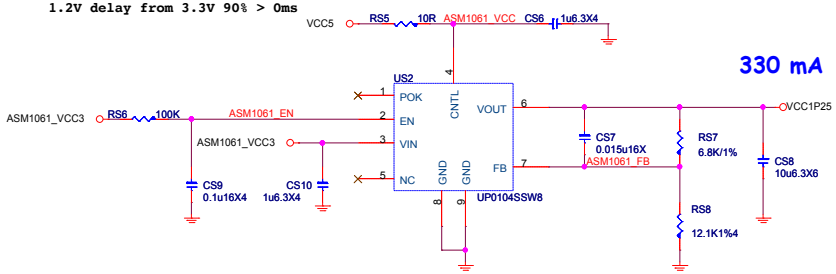
ASM1061 SATA6G



ASM SATA power switch

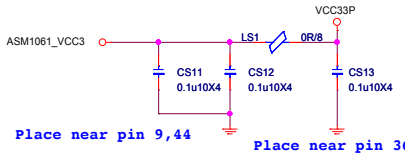
1.2V delay from 3.3V 90% > 0ms



330 mA

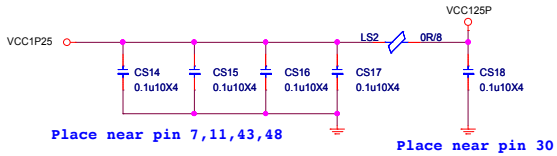
ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



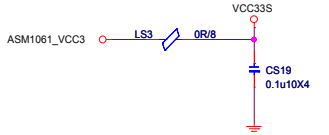
Place near pin 9,44

Place near pin 36

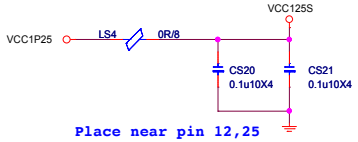


Place near pin 7,11,43,48

Place near pin 30

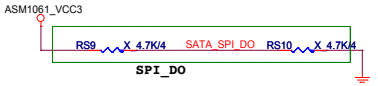


Place near pin 19



Place near pin 12,25

3.0



Add- 2011.3.18

SATA_SPI_DO don't need pull up (integrated pull-up)
or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

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MS-7916

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Custom	Clock GEN IDR5901	1.0

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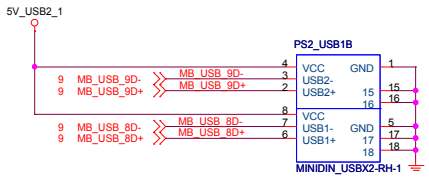
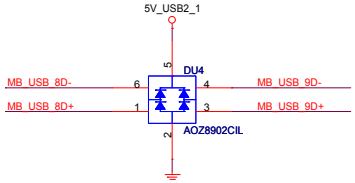
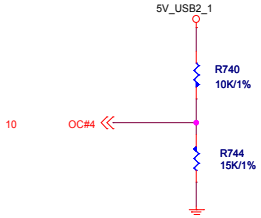
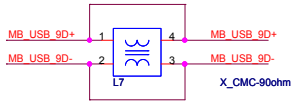
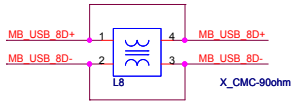
REAR USB PORT 8,9 (With PS2)











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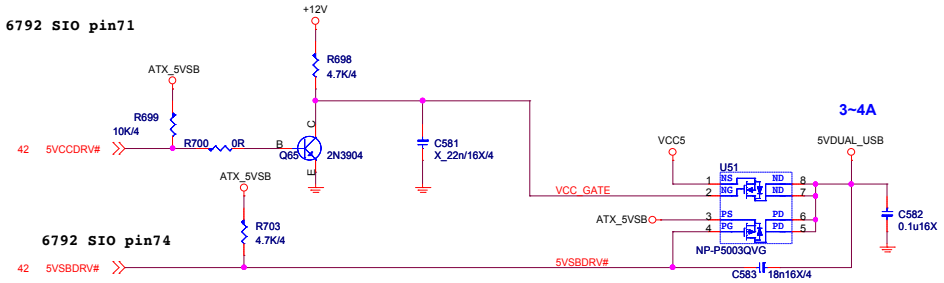
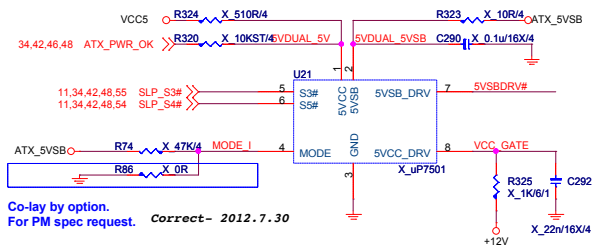
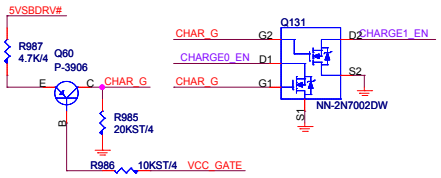
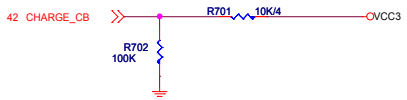
5VDUAL_USB - uP7501



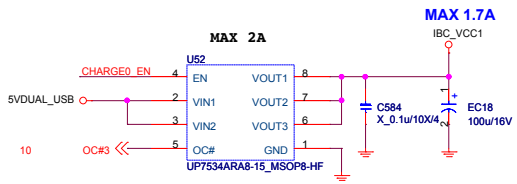


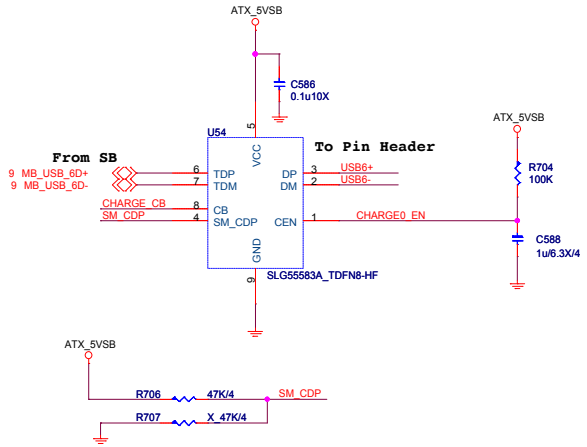


Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB

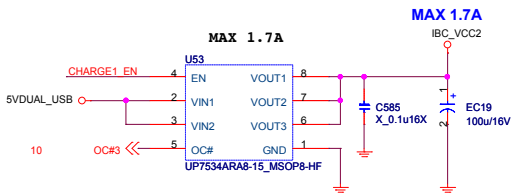


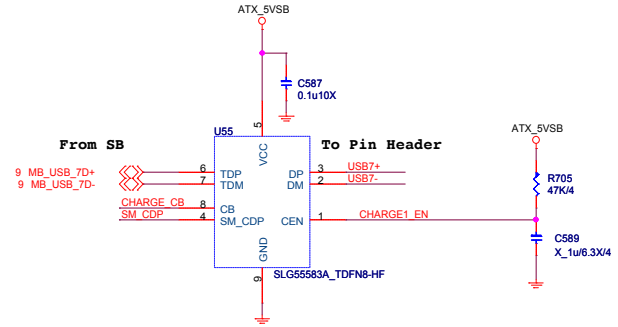
USB POWER PORT 0 For USB Charging



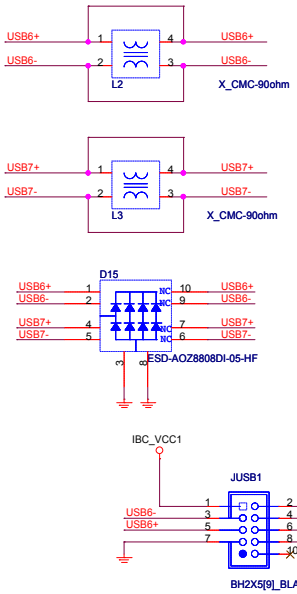


USB POWER PORT 1 For USB Charging





FRONT USB PORT 0,1



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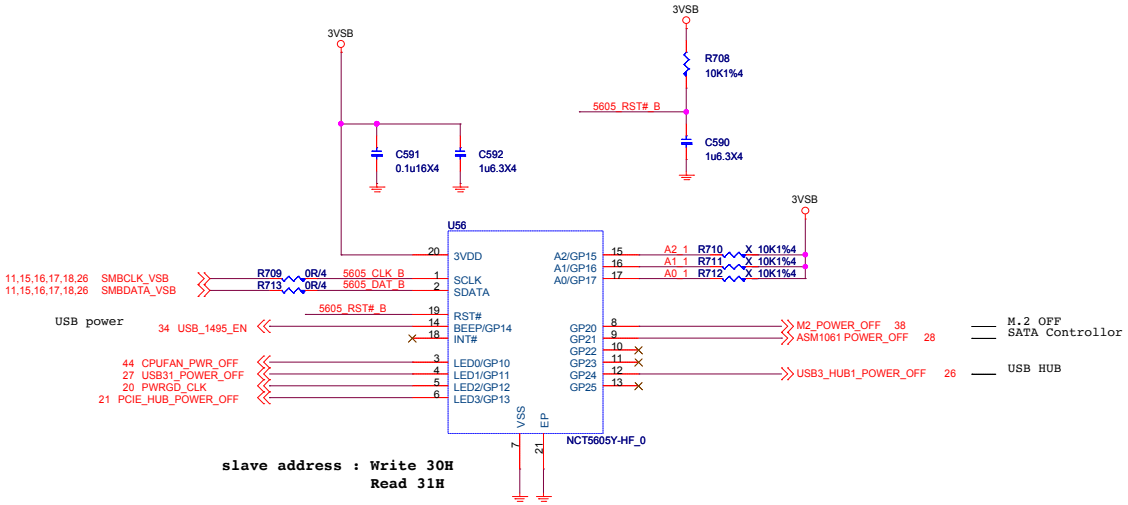

MSI	MICRO-STAR INT'L CO.,LTD	
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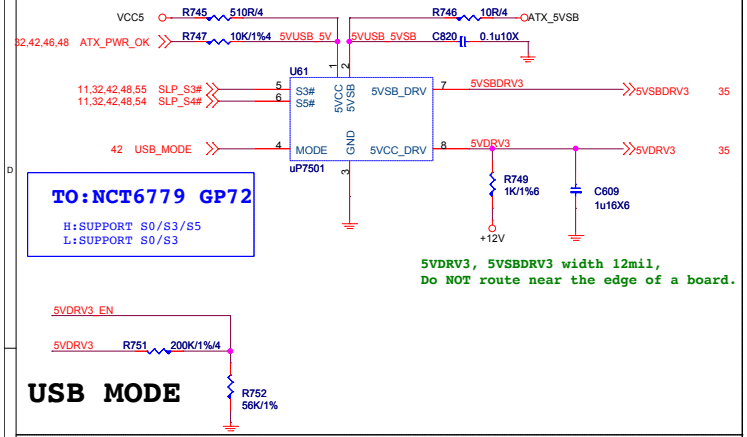
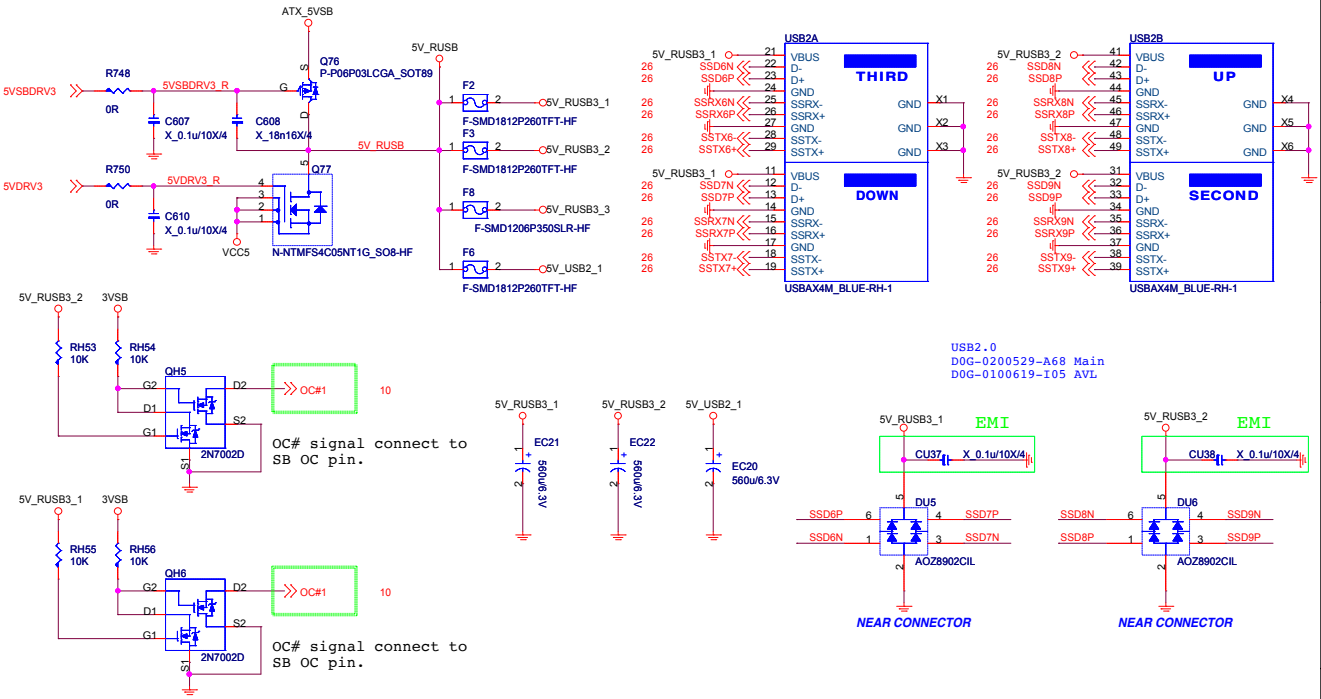
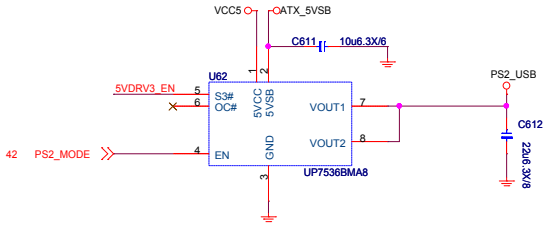
REAR USB3.0 POWER

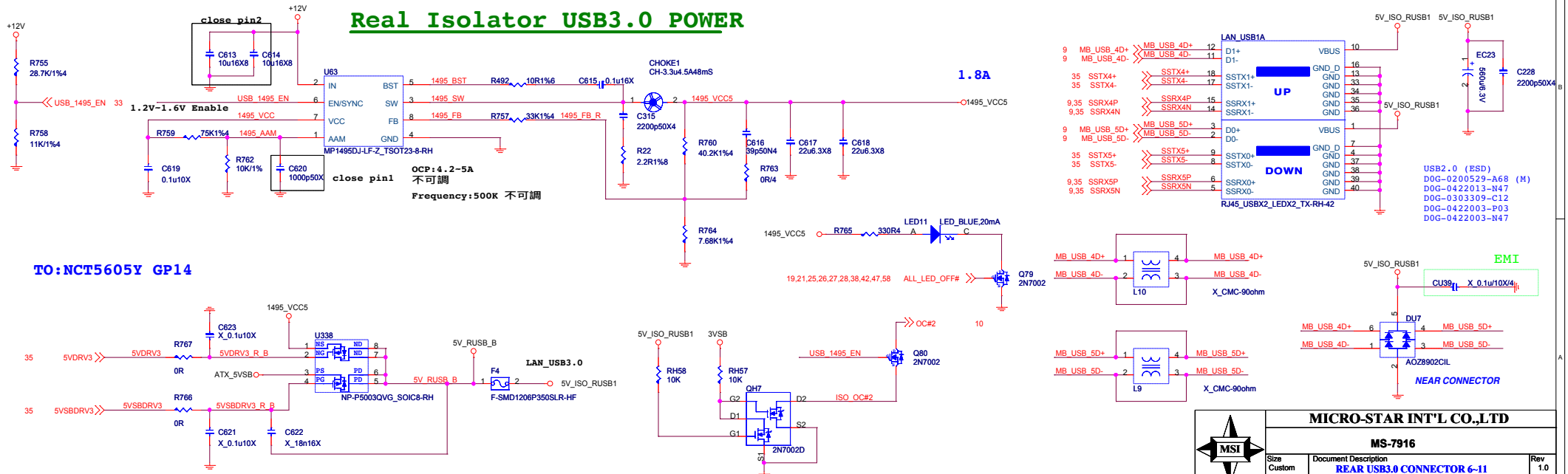




PS2 PORT POWER



Real Isolator USB3.0 POWER



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Size: Custom	Document Description: REAR USB3.0 CONNECTOR 6~11
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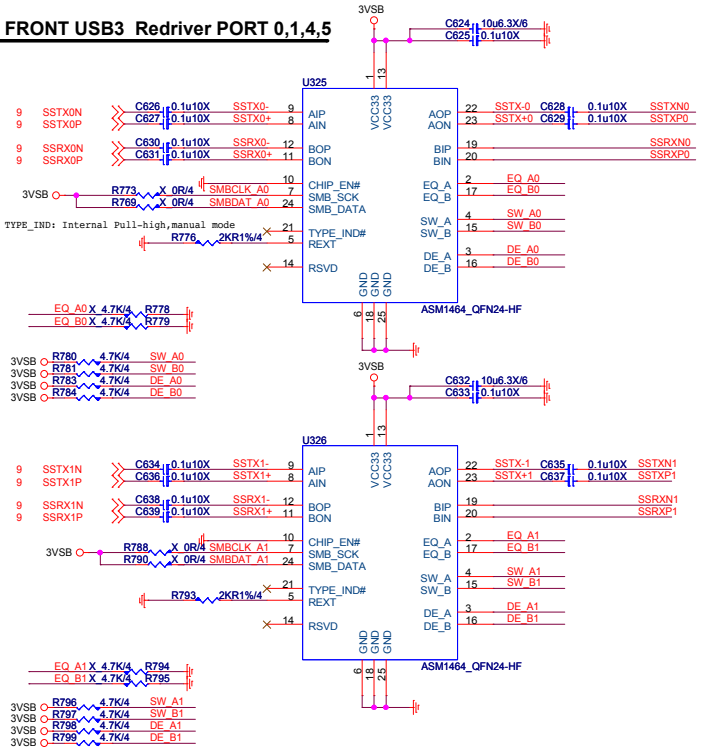
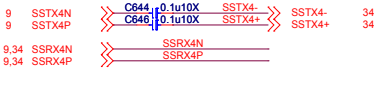
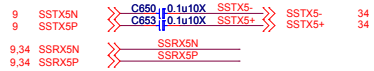
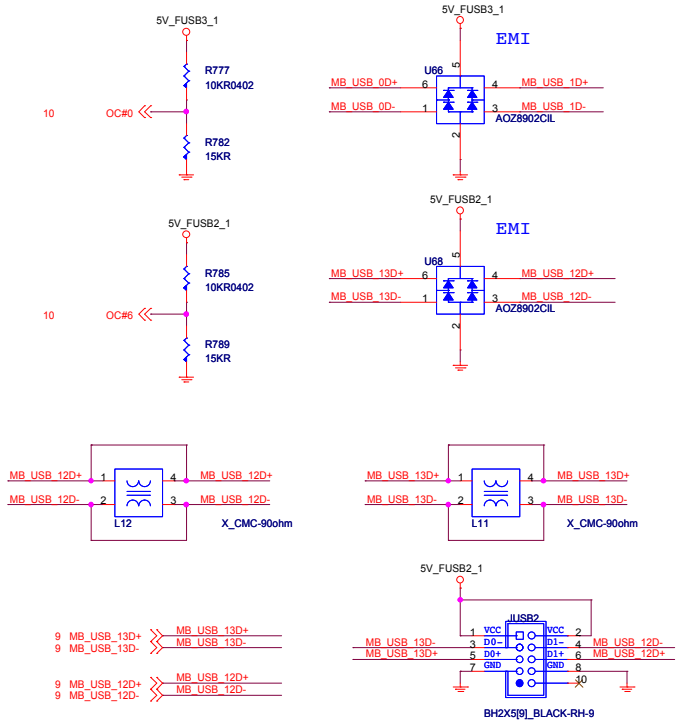
FRONT USB3 Redriver PORT 0,1,4,5

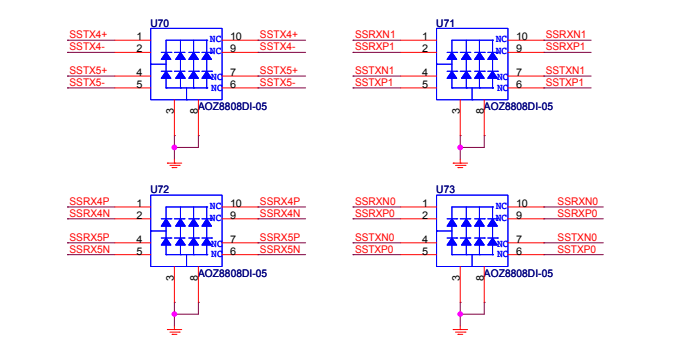




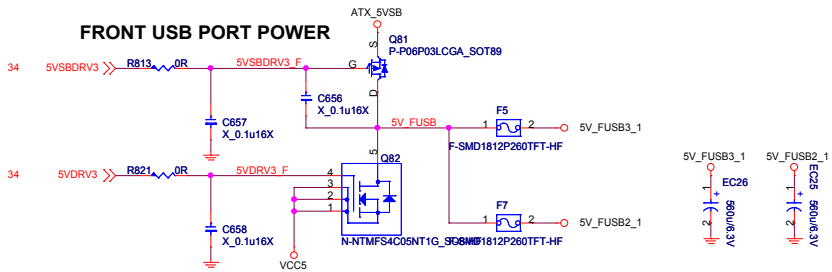


FRONT USB2 PORT 0,1,4,5,12,13

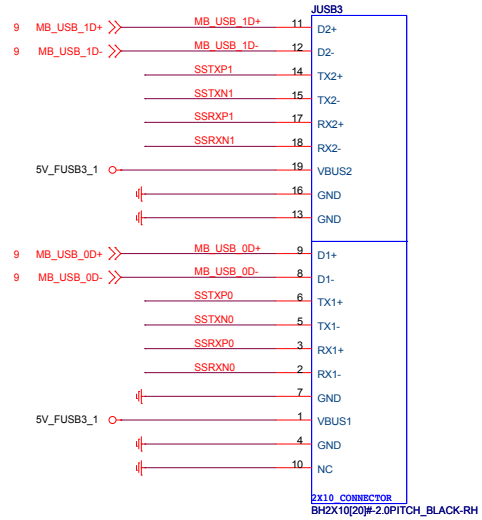




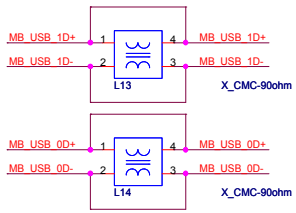
FRONT USB PORT POWER

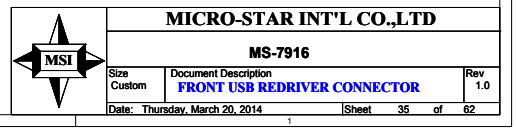


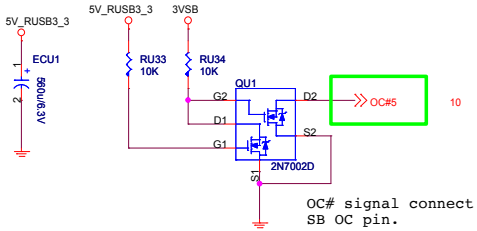
900 mA min 40mil. 900 mA min 40mil.



900 mA min 40mil. 900 mA min 40mil.



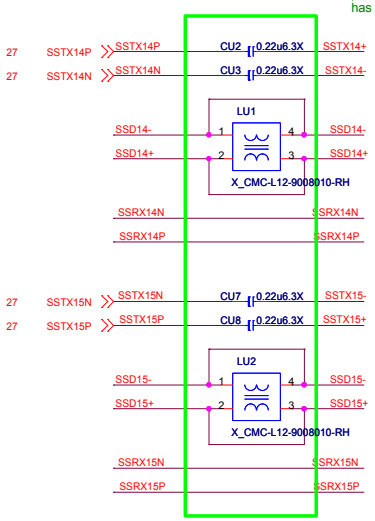




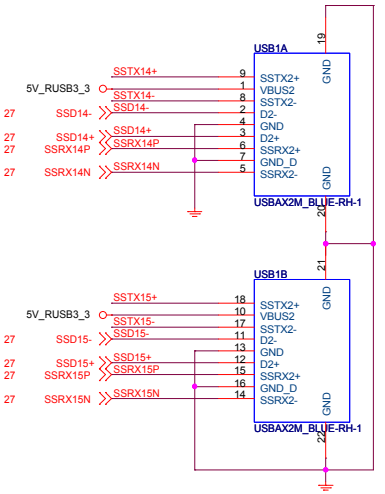
OC# signal connect to
SB OC pin.

Rear USB3 CONN

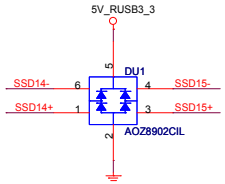
Important~~
If USB3.0 signal conect to front pin header,
please must less than 1.5 inch,short trace
has better eye diagram with some bad fly cable by SI customer.



若layout空間不足可不預留此部分choke

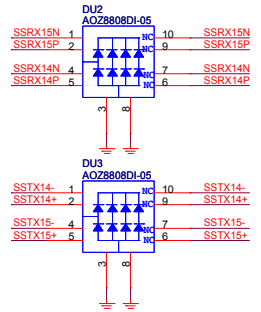


USB2.0
D0G-0200529-A68 Main
D0G-0100619-I05 AVL



ESD Protection

NEAR CONNECTOR



USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: REAR USB3.1 CONNECTOR_12/13	Rev: 1.0
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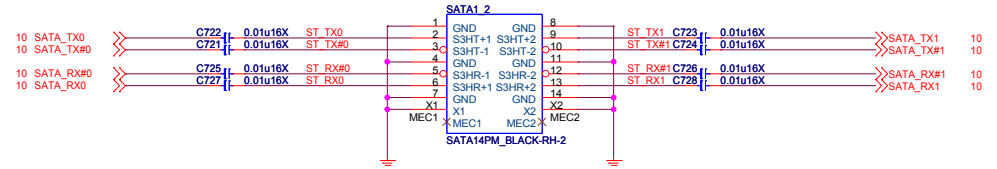
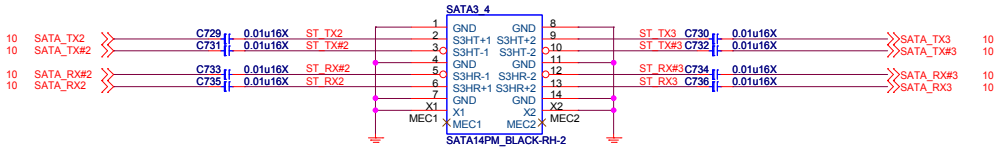
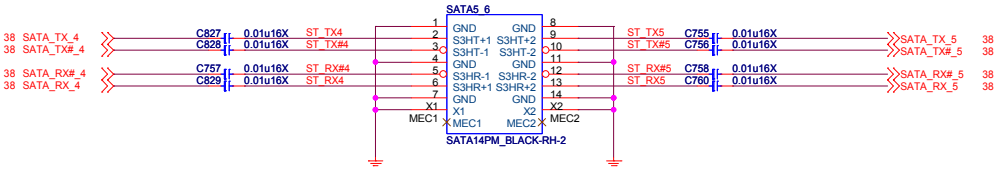
PCH



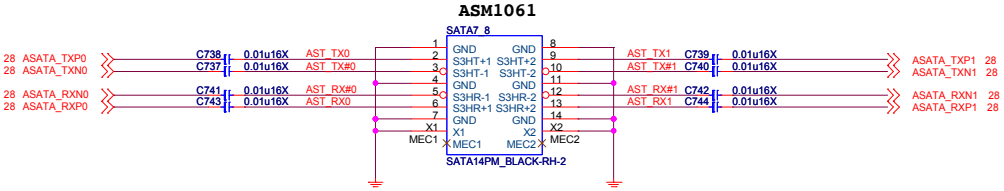
PCH



M.2 Share



ASM1061



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MS-7916		
Size: Custom	Document Description: SATA Connector	Rev: 1.0
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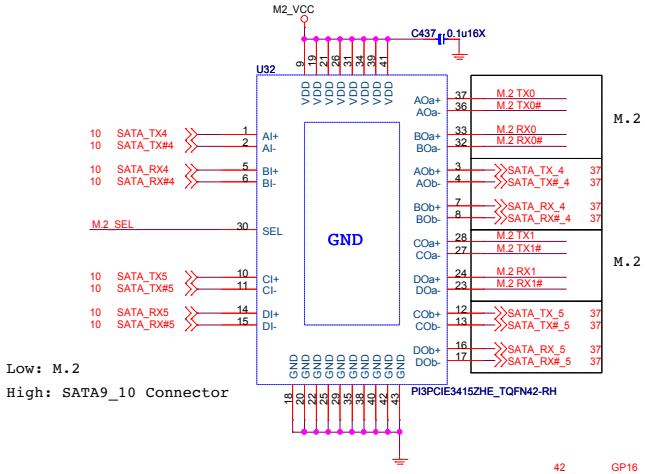
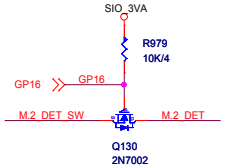
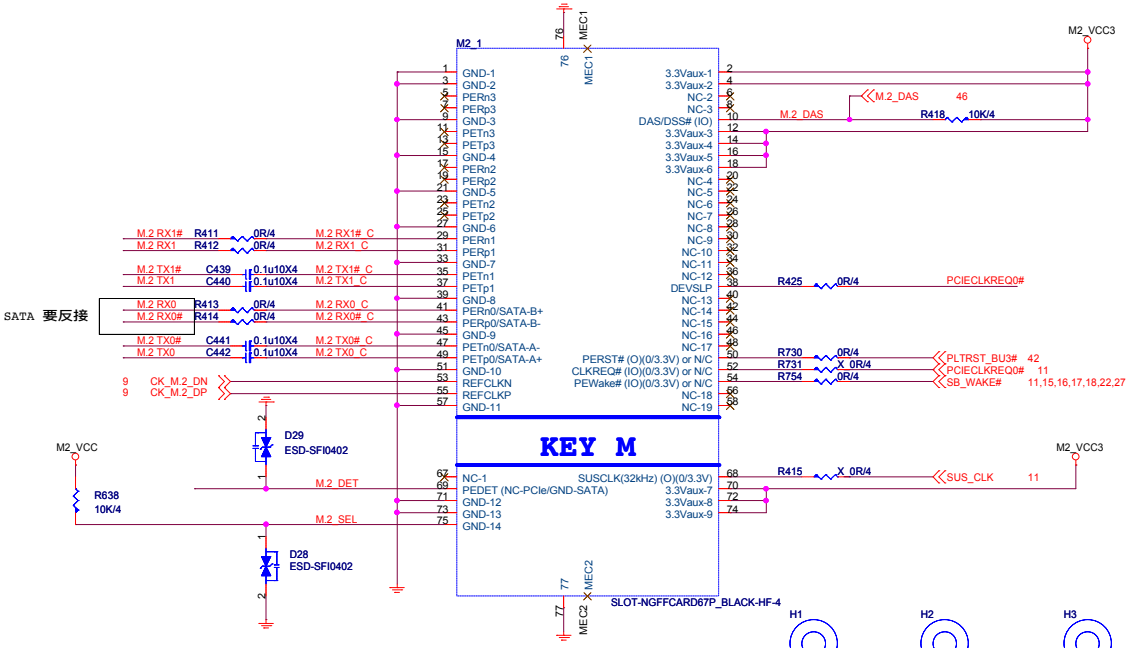
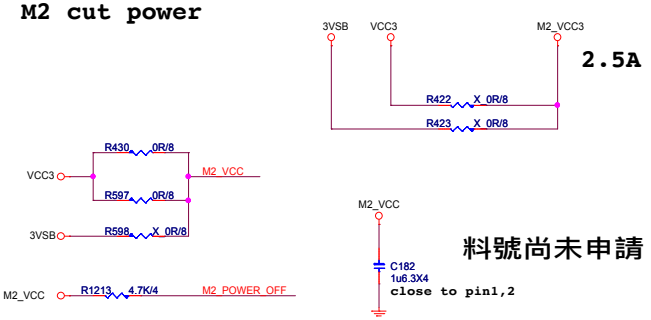




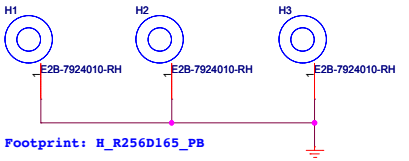


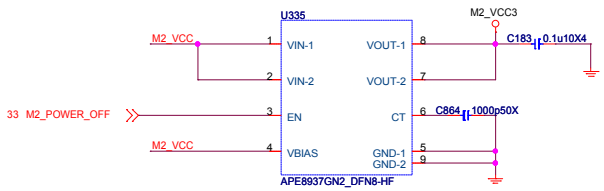
M2 cut power

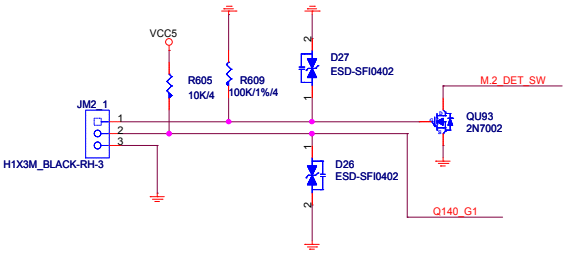


BIOS_MODE

GP10	GP11	PCH_SEL	Mode
0	0	1	M2-SATA
0	1	1	Int-SATA
1	0	0	M2-PCIE
1	1	1	AUTO

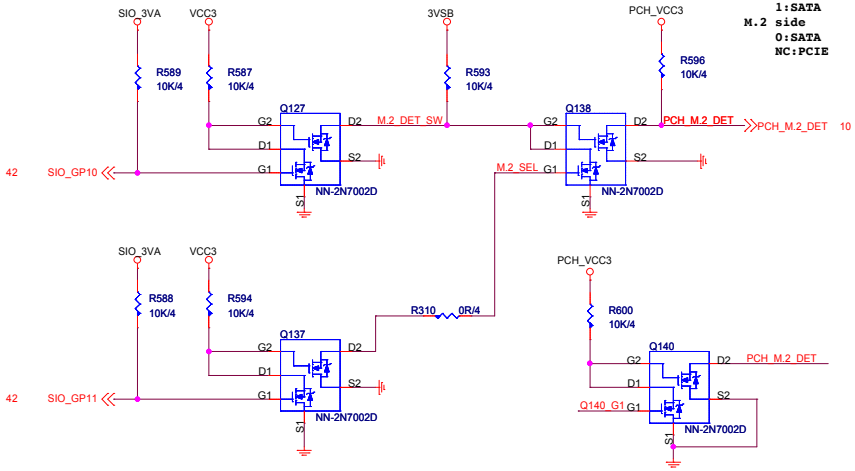


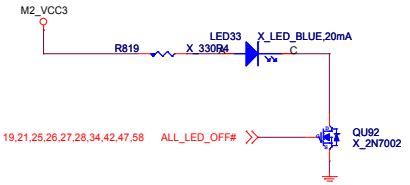


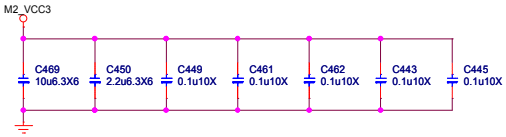


SATA & PCIE SWITCH

PCH side
0:PCIE
1:SATA
M.2 side
0:SATA
NC:PCIE







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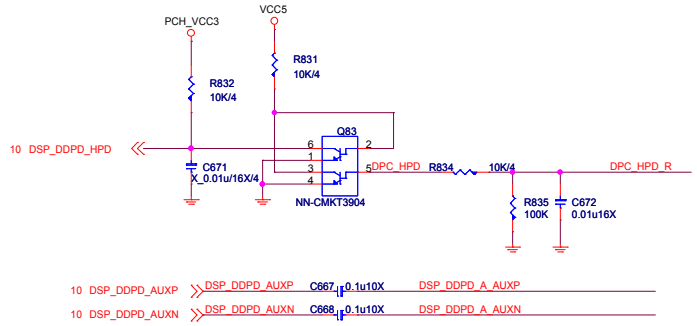
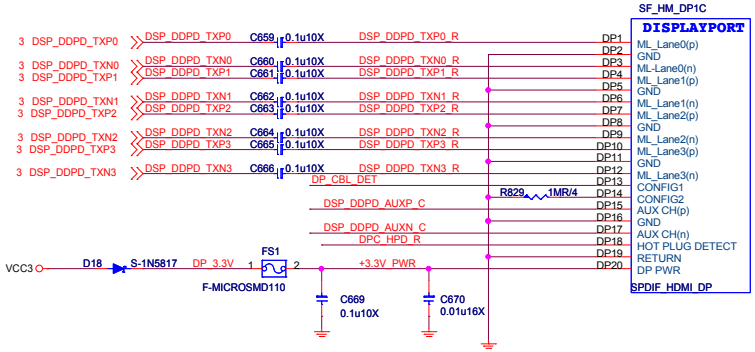
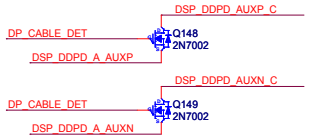


DP

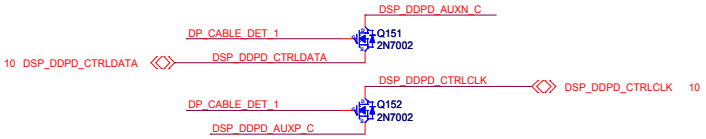


DisplayPort*Interoperability Implementation



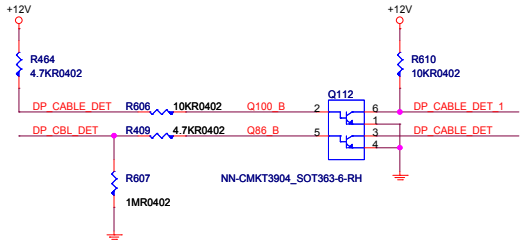
PS:DSP_DDPD_CTRLCLK

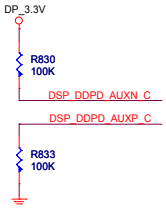
PULL HIGH 3.3V 2.2K ohm on chip side

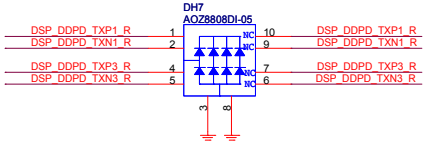


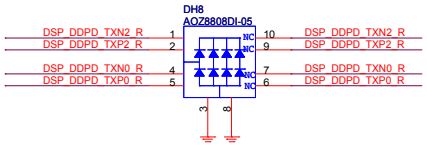
PS:DSP_DDPD_CTRLDATA

PULL HIGH 3.3V 2.2K ohm on chip side









DP_CBL_DET	DP	HDMI
HDMI_C_DNG_DETECT	L	H
DP_DEVICE_DETECT	H	L
HDMI_DEVICE_DETECT	L	H

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Custom	DISPLAY Connector	1.0

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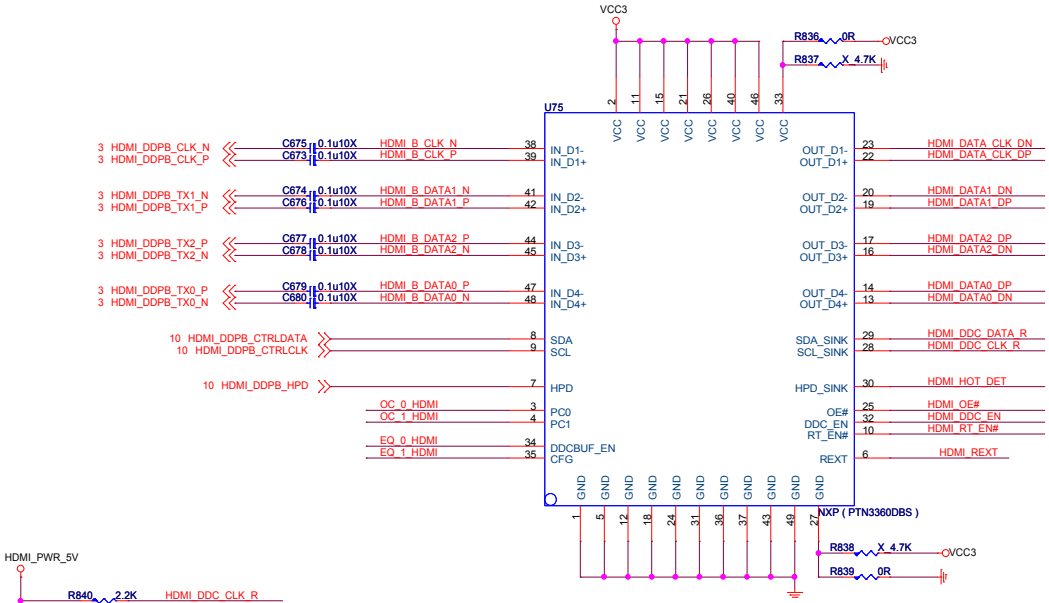
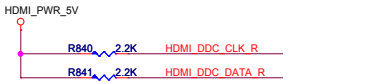
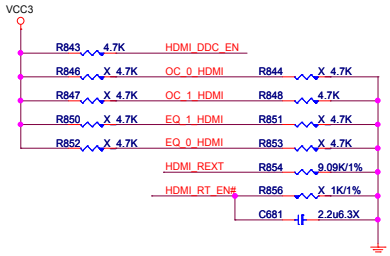
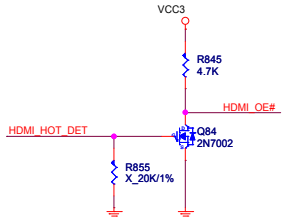
HDMI level shifter









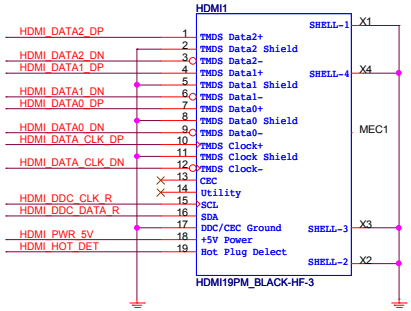
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

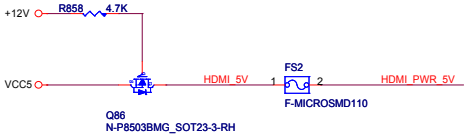
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

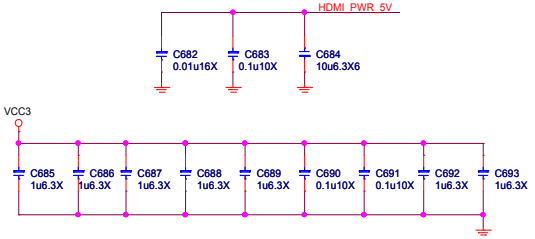
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	







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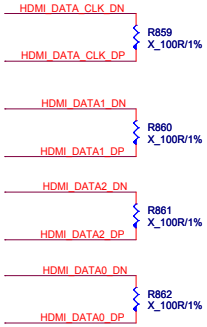
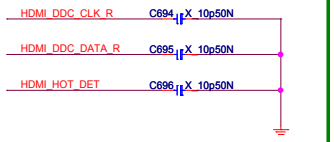


EMI cap.



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Custom	HDMI Connector 1	1.0

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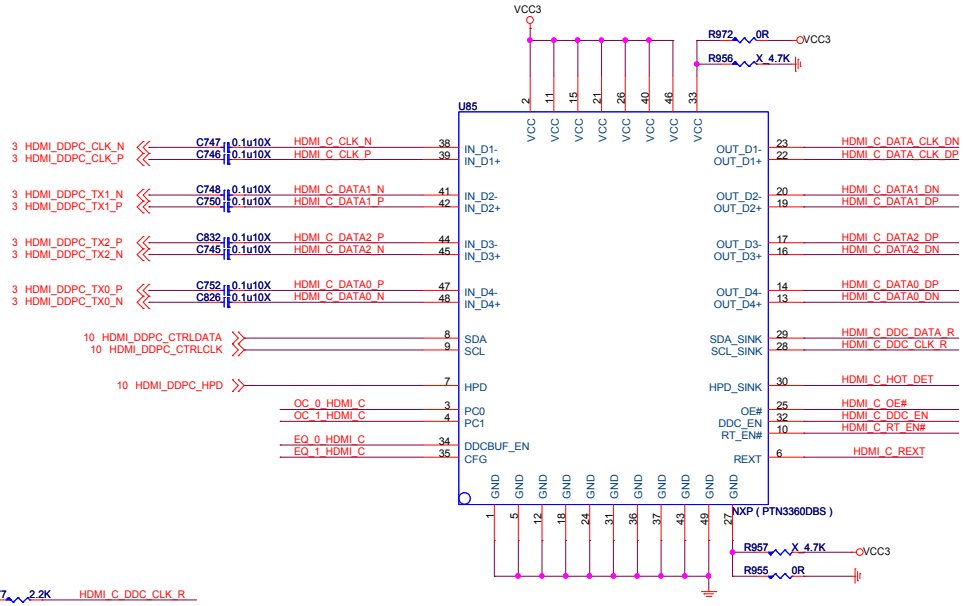
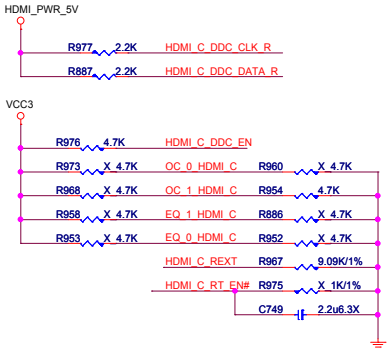
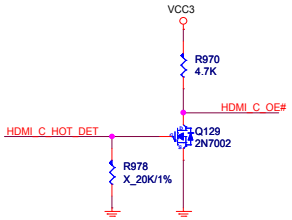
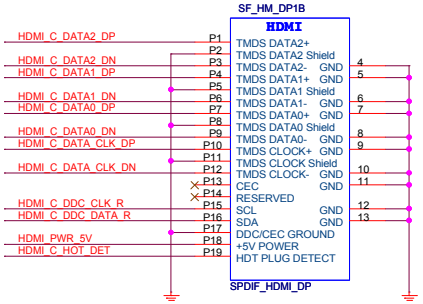
HDMI level shifter





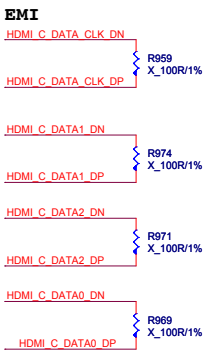


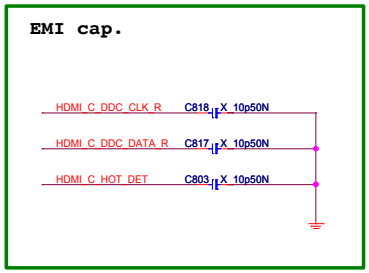


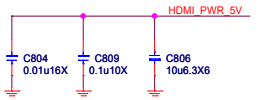
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifitng configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

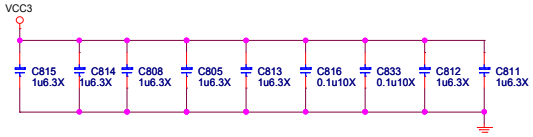
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	









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Custom	ASM1061 SATA6G	1.0

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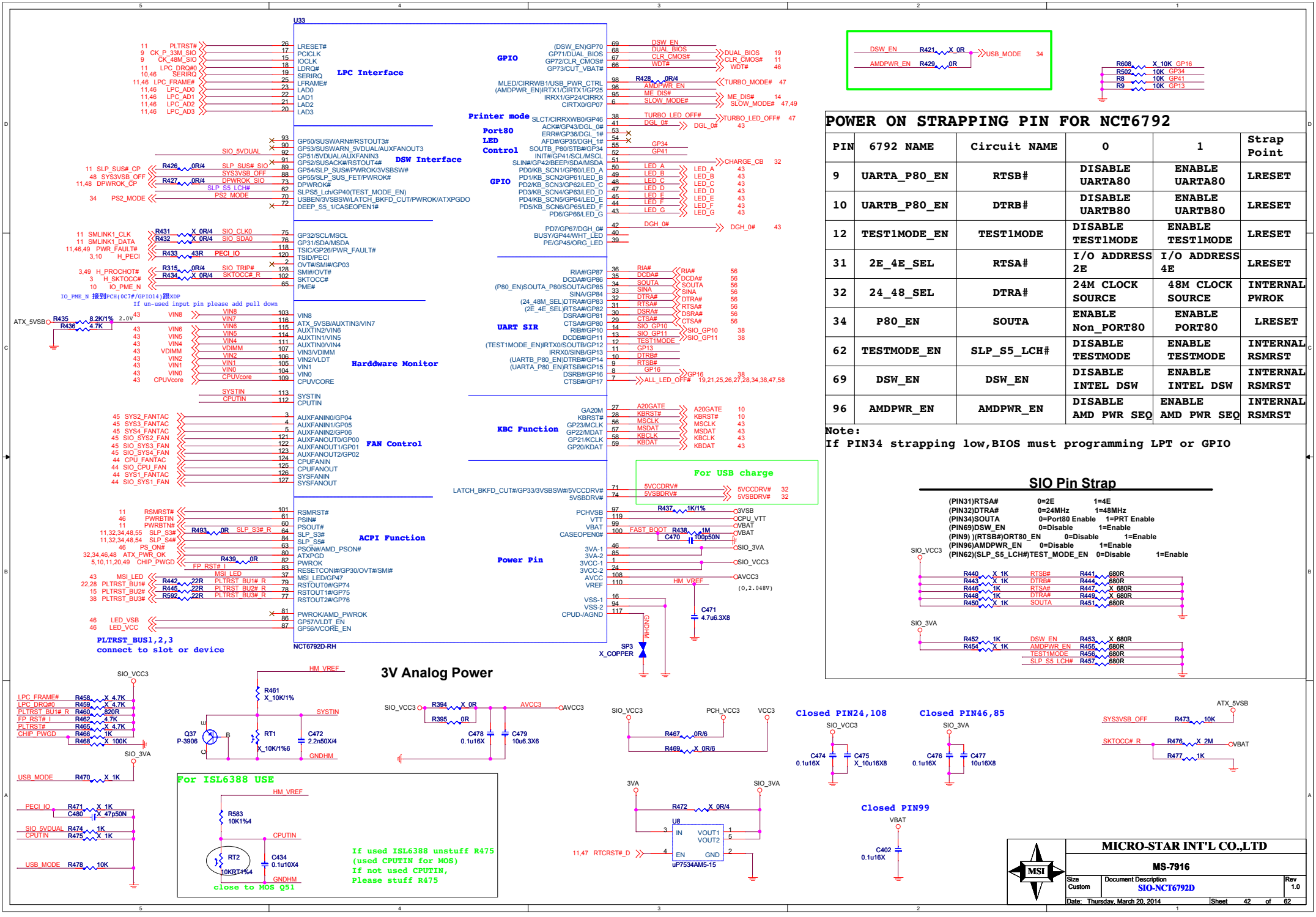

POWER ON STRAPPING PIN FOR NCT6792

PIN	6792 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	24_48_SEL	DTRA#	24M CLOCK SOURCE	48M CLOCK SOURCE	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
62	TESTMODE_EN	SLP_S5_LCH#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

SIO Pin Strap

(PIN31)RTSA# 0=2E 1=4E
(PIN32)DTRA# 0=24MHz 1=48MHz
(PIN34)SOUTA 0=Port80 Enable 1=PRT Enable
(PIN69)DSW_EN 0=Disable 1=Enable
(PIN9))(RTSB#)ORT80_EN 0=Disable 1=Enable
(PIN96)AMDPWR_EN 0=Disable 1=Enable
(PIN62)(SLP_S5_LCH#)TEST_MODE_EN 0=Disable 1=Enable

RTSB#	R441 680R	DSW_EN	R453 X_680R
DTRB#	R444 680R	AMDPWR_EN	R455 680R
RTSA#	R447 X_680R	TEST1MODE	R456 680R
DTRA#	R449 X_680R	SLP_S5_LCH#	R457 680R
SOUTA	R451 680R		

R440 X_1K		R452 1K	
R443 X_1K		R454 X_1K	
R446 1K			
R448 1K			
R450 X_1K			

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Size: Custom
Document Description: SIO-NCT6792D
Rev: 1.0
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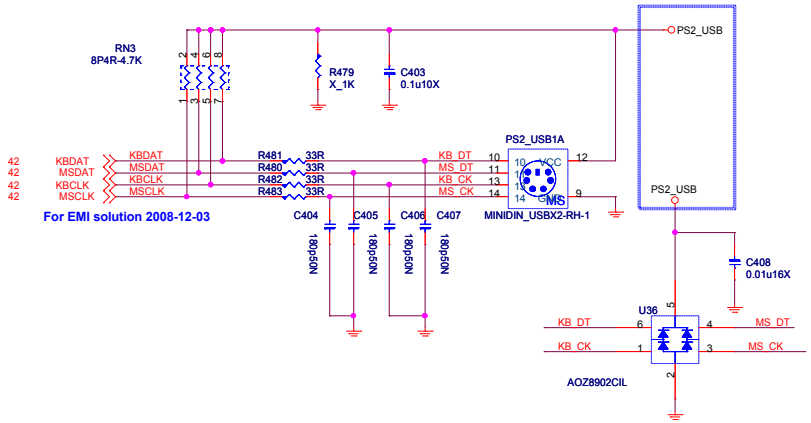
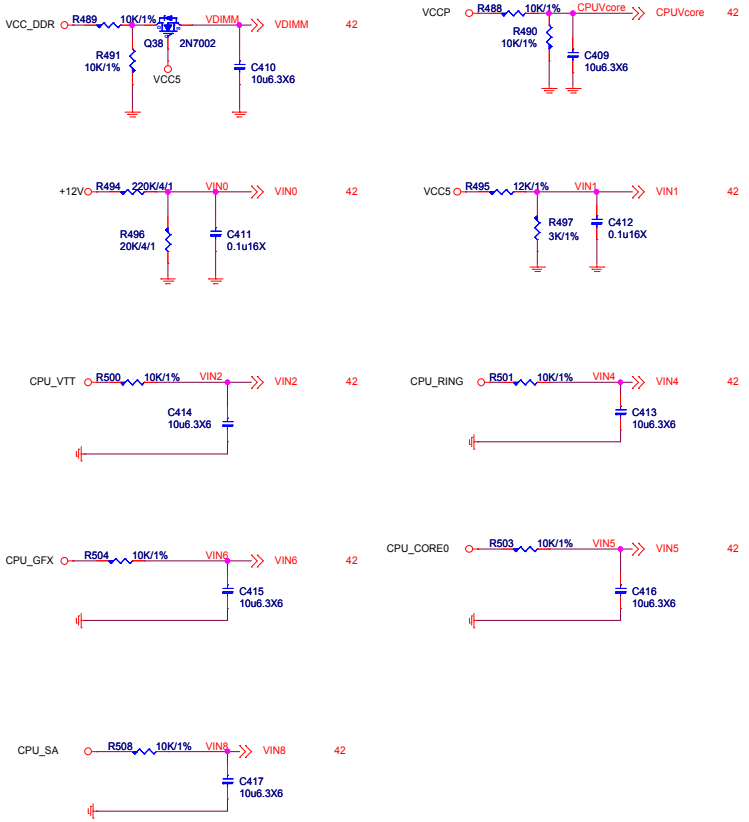
PS2 KEYBOARD & MOUSE CONNECTOR

可以切換在s5
底下是不是要有電

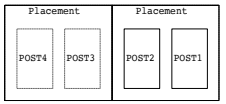


HW Monitor - Voltage

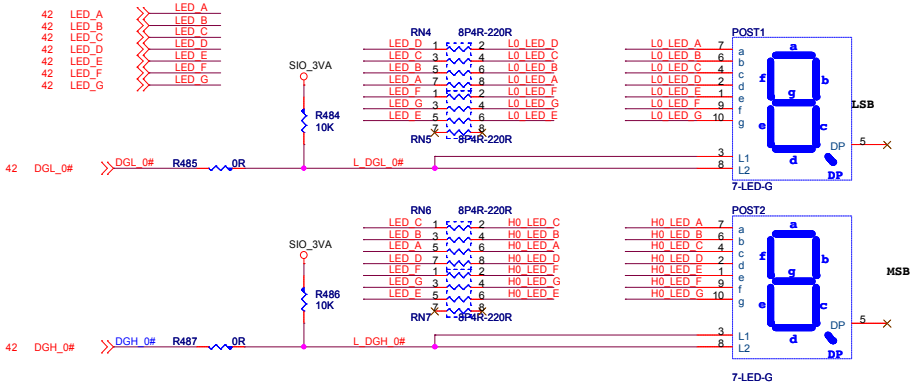
SIO HM Voltage voer 2V will not detect



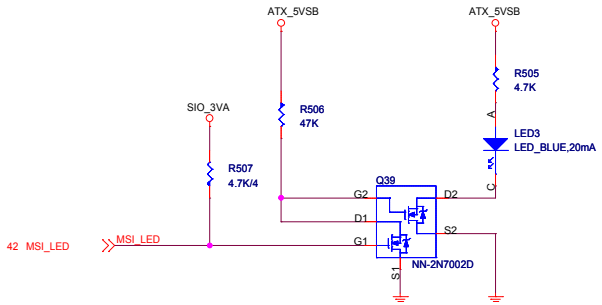
DEBUG LED



Placement一定要對
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)



MSI_LED



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: SIO-NCT6779D/PS2/Debug LED	Rev: 1.0
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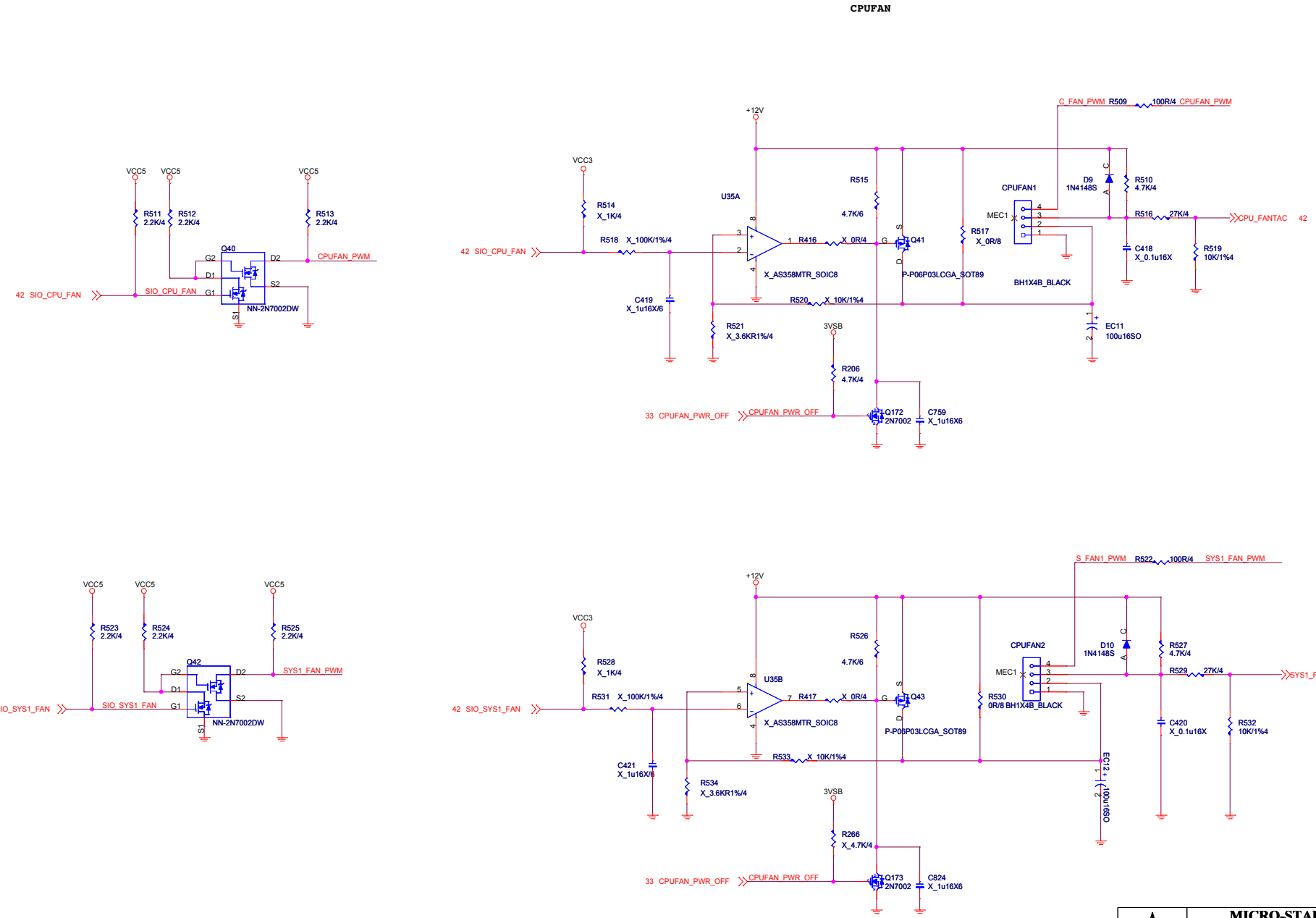
Type E : 4 PIN CPU FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: CPU FAN & SYSFAN1-2	Rev: 1.0
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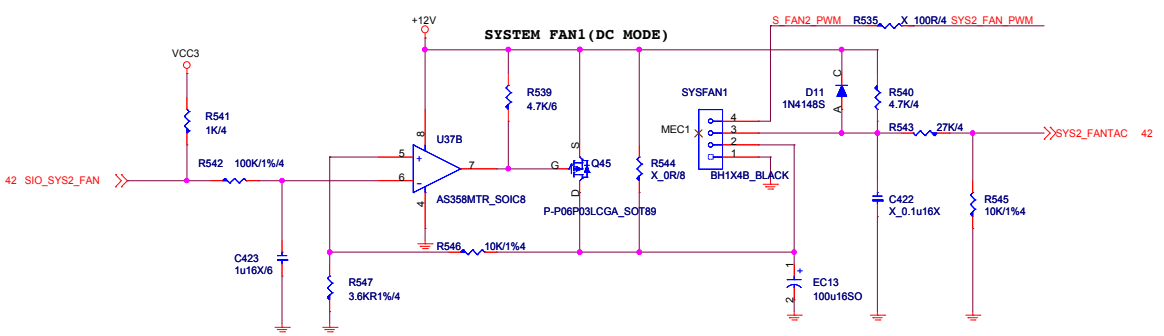
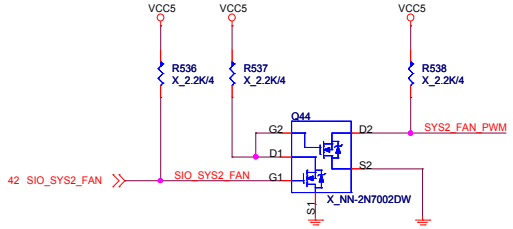
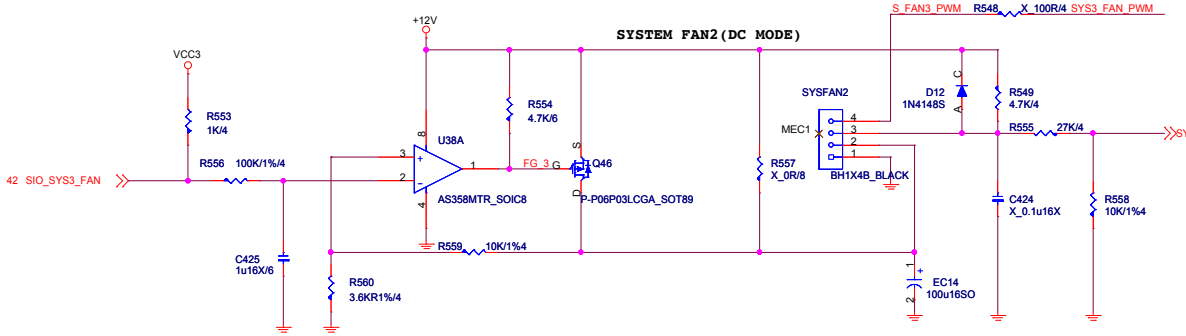
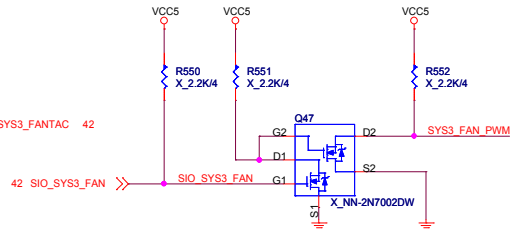
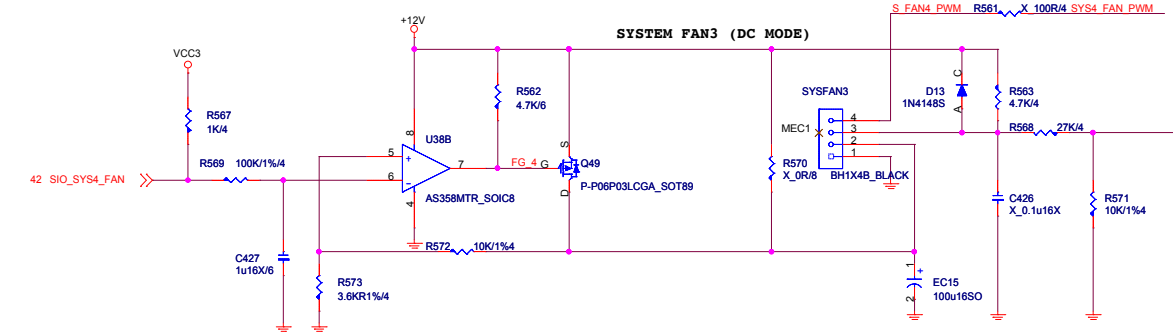


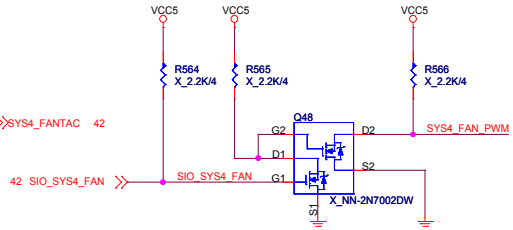


Type F : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/PWM MODE)(FOR NCT6776/5533)









MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SYSFAN3-6	1.0

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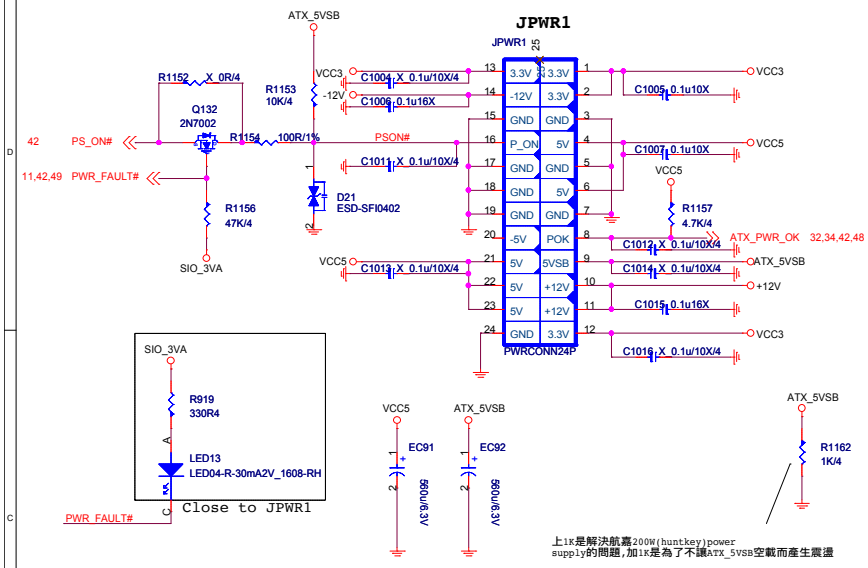
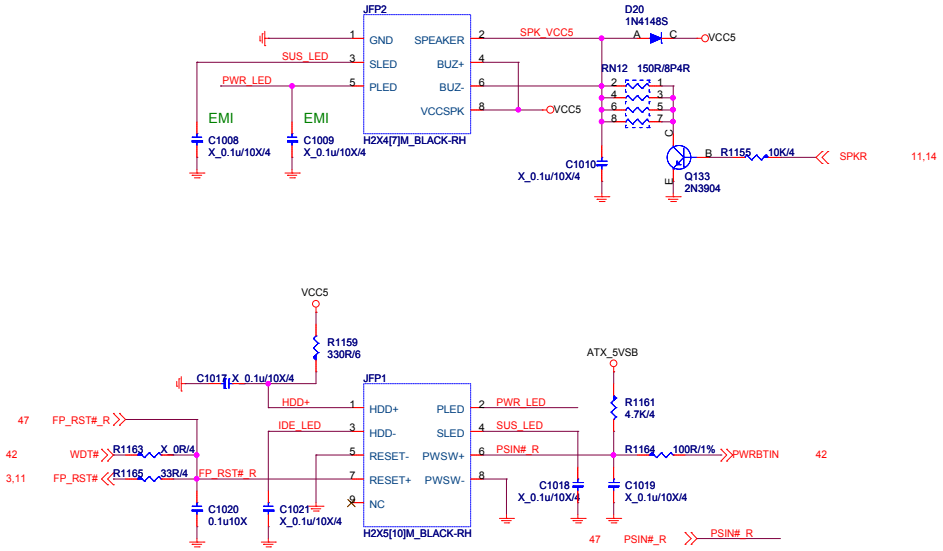
ATX POWER CONNECTOR

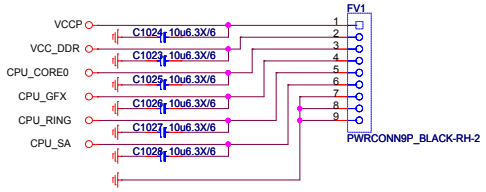


上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓ATX_5VSB空載而產生震盪

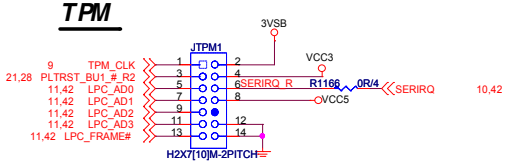
FRONT PANNEL

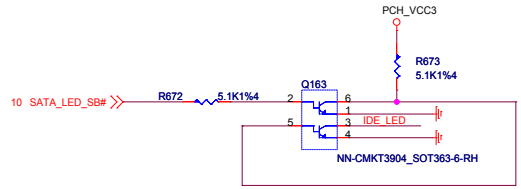


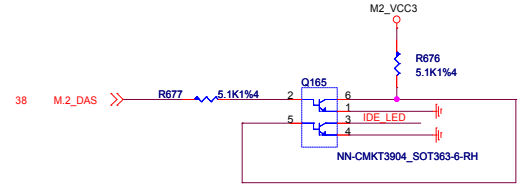
Voltage test point

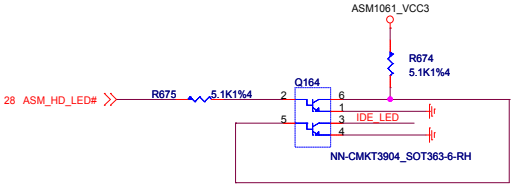


TPM

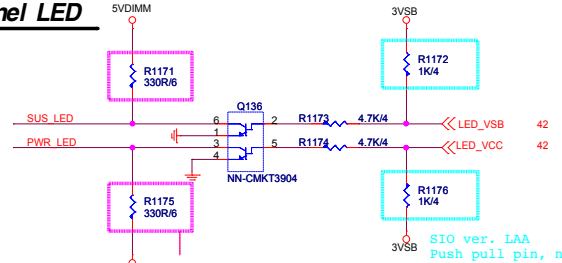








Front Panel LED



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MS-7916		
Size: Custom	Document Description: ATX F_Panel/EMI/TPM	Rev: 1.0
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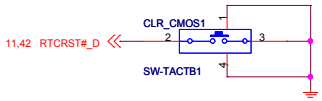
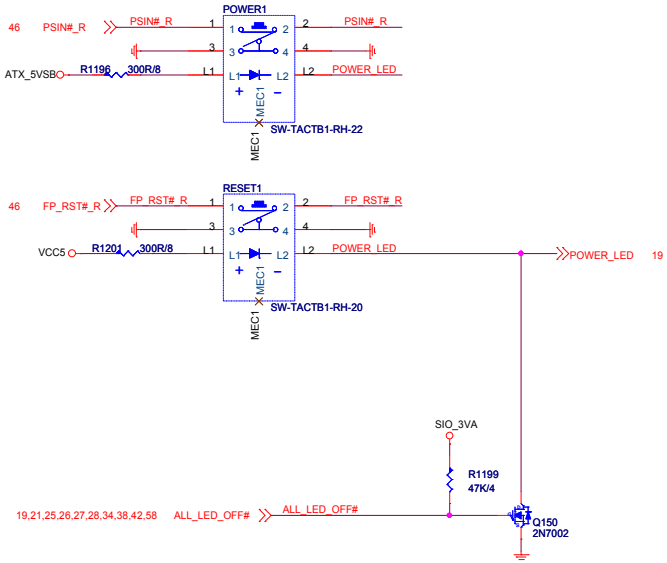
Clear CMOS button

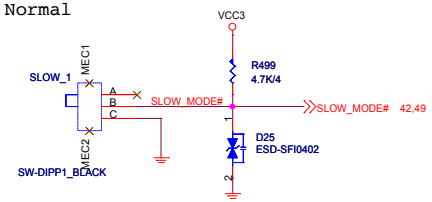


PWR/RST Botton



SLOW MODE

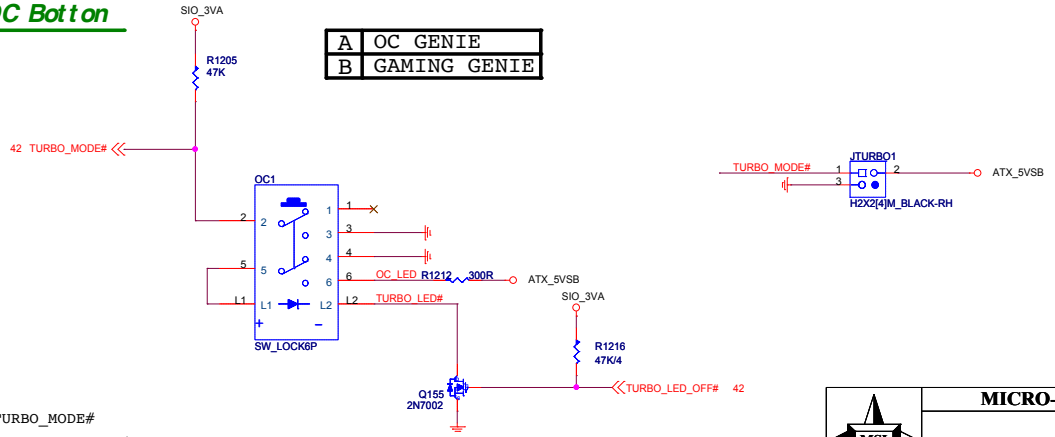
A Normal



B Slow Mode

OC Botton

A	OC GENIE
B	GAMING GENIE



TURBO_MODE#
Default: Low,disable OC
Push Bottom: high,Enable OC / Turn on LED

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Custom	BOTTON	1.0

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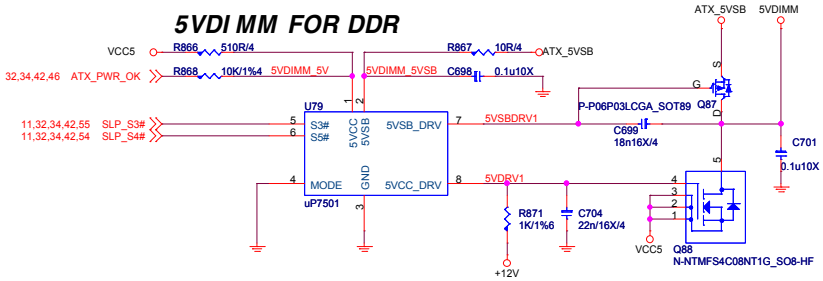
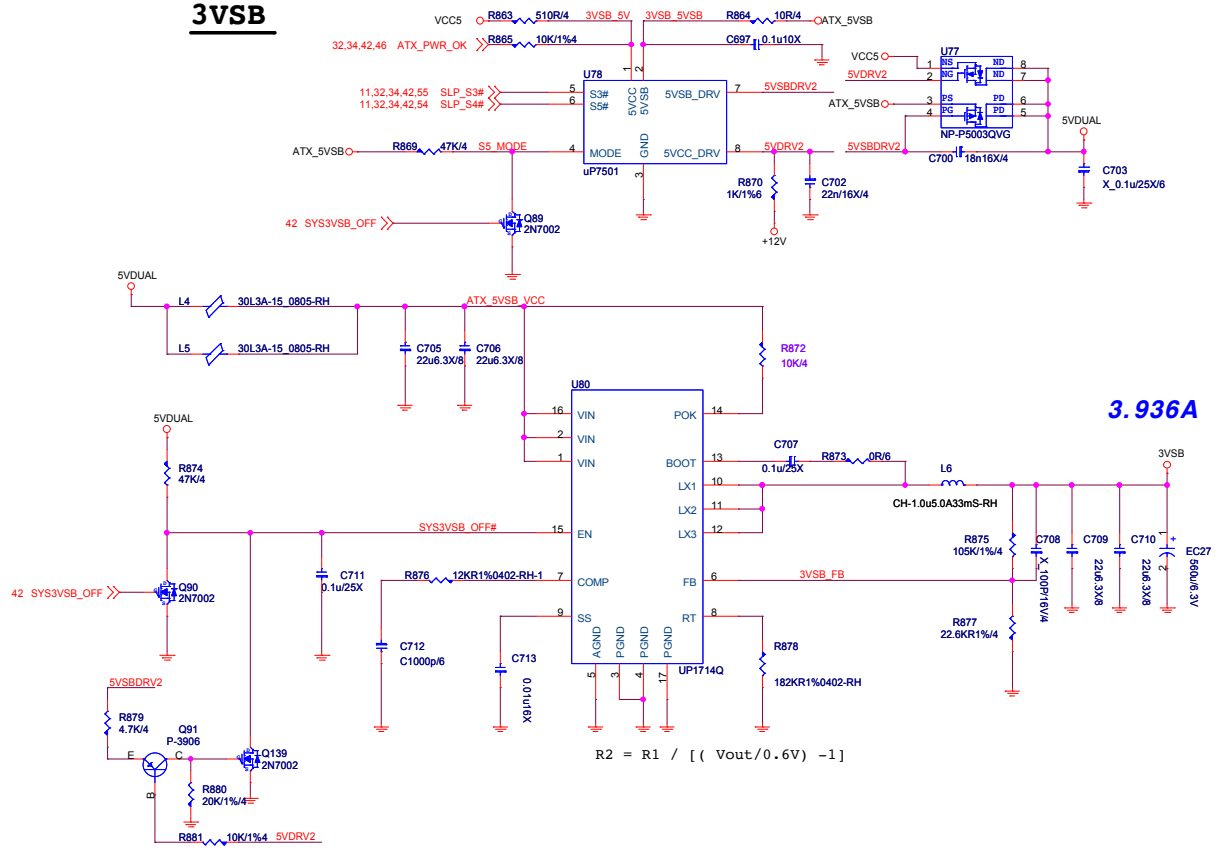
5VDI MM FOR DDR



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

5VDRV1看VCC5起來6-10ms後起來,因為當初挑power

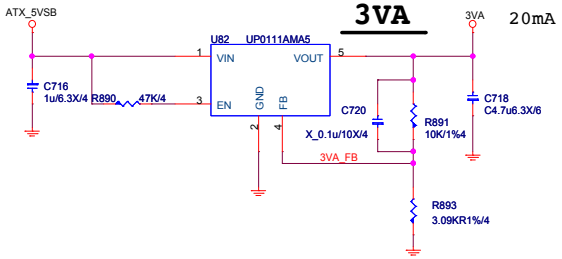
3VSB



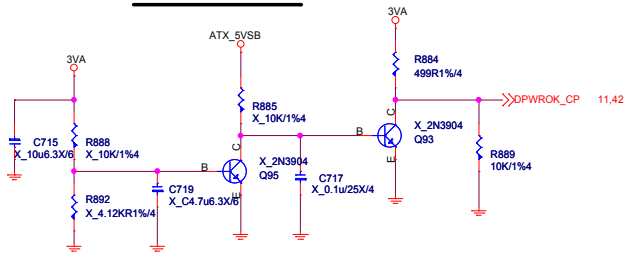
3.936A

R2 = R1 / [(Vout/0.6V) -1]

3VA



Deep Power OK



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	MS-7916	
Size: Custom	Document Description: ACPI controller UPI	Rev: 1.0
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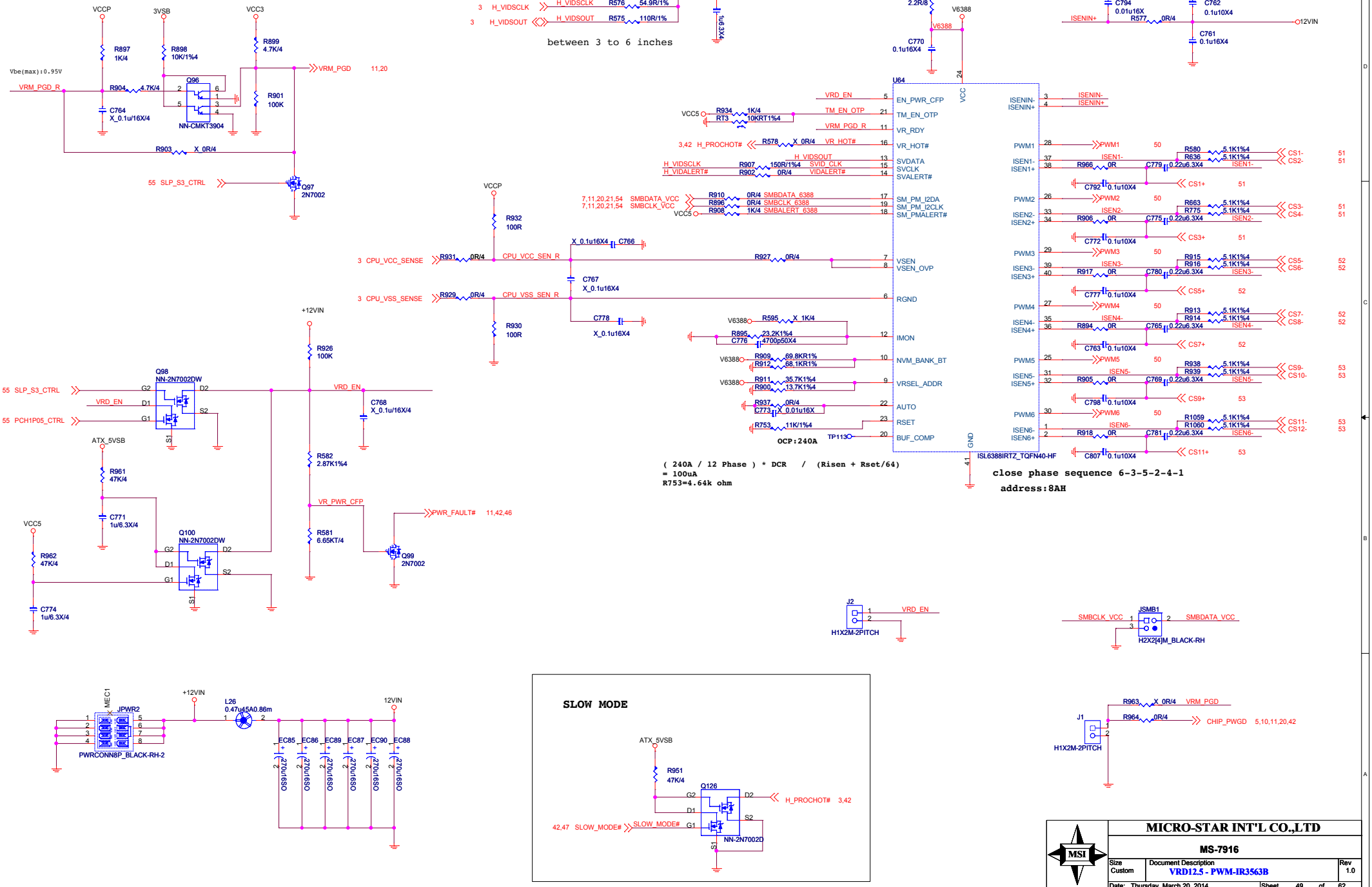
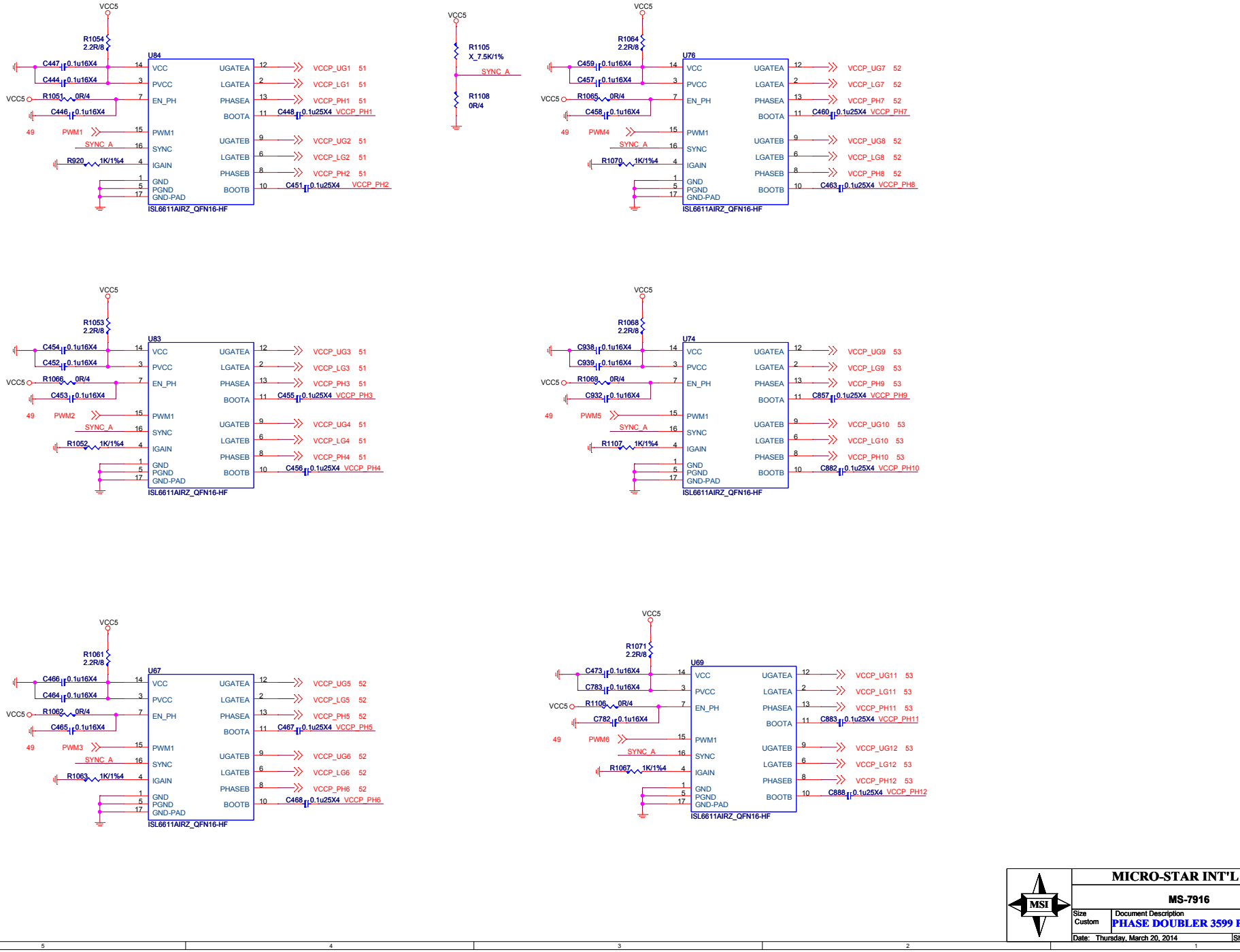
VRMPWRGD LEVEL SHIFT



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: VRD12.5 - PWM-IR3563B	Rev: 1.0
Date: Thursday, March 20, 2014	Sheet 49 of 62	



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: PHASE DOUBLER 3599 Phase1-16	Rev: 1.0
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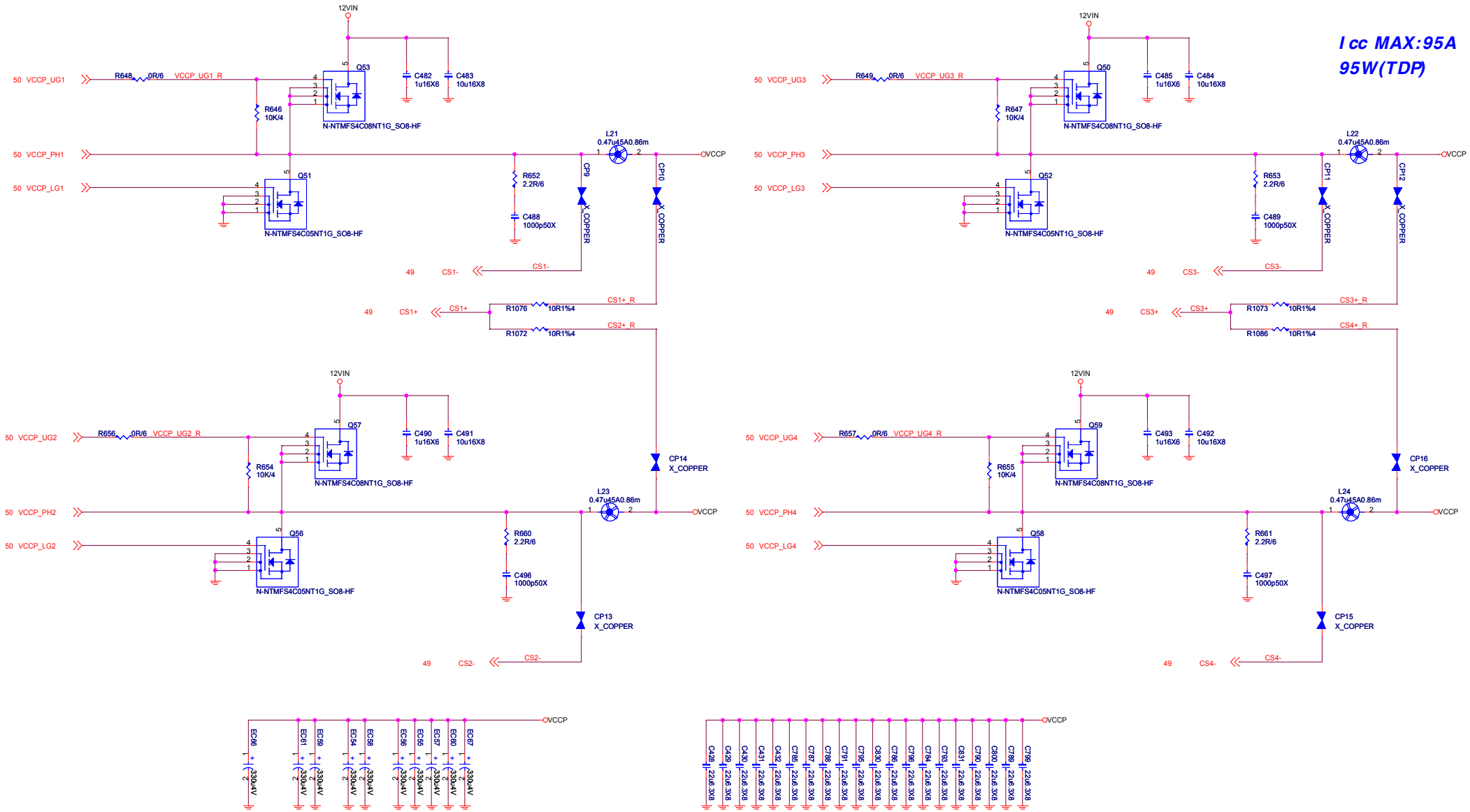
Icc MAX:95A
95W(TDP)
12VIN
50 VCCP_UG1
R648 0R/6 VCCP_UG1_R
Q53
N-NTMFS4C08NT1G_SO8-HF
C482 1u16X6
C483 10u16X8
R646 10K/4
50 VCCP_PH1
50 VCCP_LG1
Q51
N-NTMFS4C05NT1G_SO8-HF
L21 0.47u45A0.86m
VCCP
R652 2.2R/6
C488 1000p50X
CP9 X_COPPER
CP10 X_COPPER
49 CS1-
CS1-
49 CS1+
CS1+
R1076 10R1%4
CS1+_R
R1072 10R1%4
CS2+_R
12VIN
50 VCCP_UG3
R649 0R/6 VCCP_UG3_R
Q50
N-NTMFS4C08NT1G_SO8-HF
C485 1u16X6
C484 10u16X8
R647 10K/4
50 VCCP_PH3
50 VCCP_LG3
Q52
N-NTMFS4C05NT1G_SO8-HF
L22 0.47u45A0.86m
VCCP
R653 2.2R/6
C489 1000p50X
CP11 X_COPPER
CP12 X_COPPER
49 CS3-
CS3-
49 CS3+
CS3+
R1073 10R1%4
CS3+_R
R1086 10R1%4
CS4+_R
12VIN
50 VCCP_UG2
R656 0R/6 VCCP_UG2_R
Q57
N-NTMFS4C08NT1G_SO8-HF
C490 1u16X6
C491 10u16X8
R654 10K/4
50 VCCP_PH2
50 VCCP_LG2
Q56
N-NTMFS4C05NT1G_SO8-HF
L23 0.47u45A0.86m
VCCP
R660 2.2R/6
C496 1000p50X
CP14 X_COPPER
CP13 X_COPPER
49 CS2-
CS2-
12VIN
50 VCCP_UG4
R657 0R/6 VCCP_UG4_R
Q59
N-NTMFS4C08NT1G_SO8-HF
C493 1u16X6
C492 10u16X8
R655 10K/4
50 VCCP_PH4
50 VCCP_LG4
Q58
N-NTMFS4C05NT1G_SO8-HF
L24 0.47u45A0.86m
VCCP
R661 2.2R/6
C497 1000p50X
CP16 X_COPPER
CP15 X_COPPER
49 CS4-
CS4-
VCCP
EC86 EC81 EC89 EC54 EC88 EC56 EC55 EC57 EC90 EC87
330u4V
VCCP
C428 C429 C430 C431 C432 C785 C787 C788 C791 C795 C830 C786 C796 C784 C793 C831 C790 C800 C789 C799
22u6.3X8
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MS-7916
Size Custom
Document Description
VCOR IR3550 PHASE 1~8
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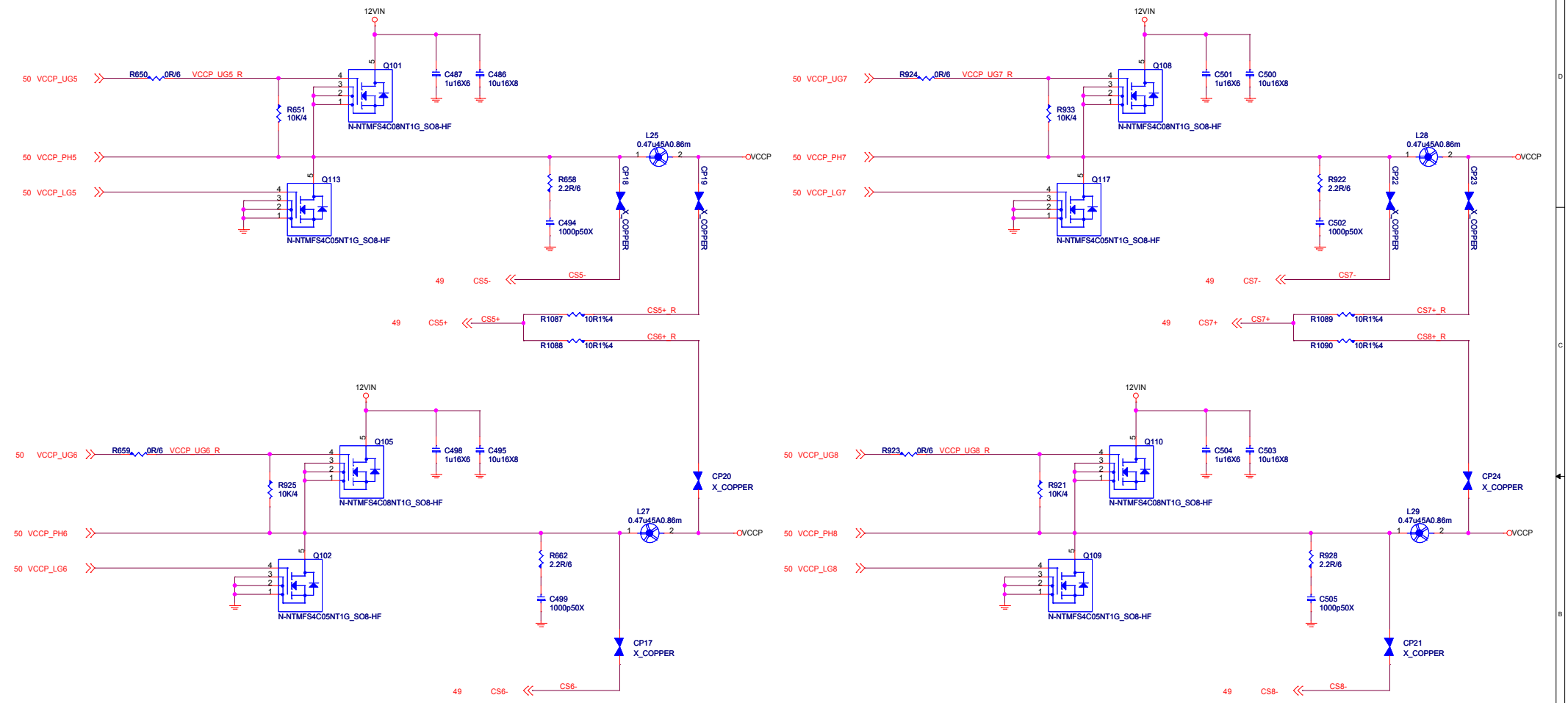

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: VCOR IR3550 PHASE 9~16	Rev: 1.0
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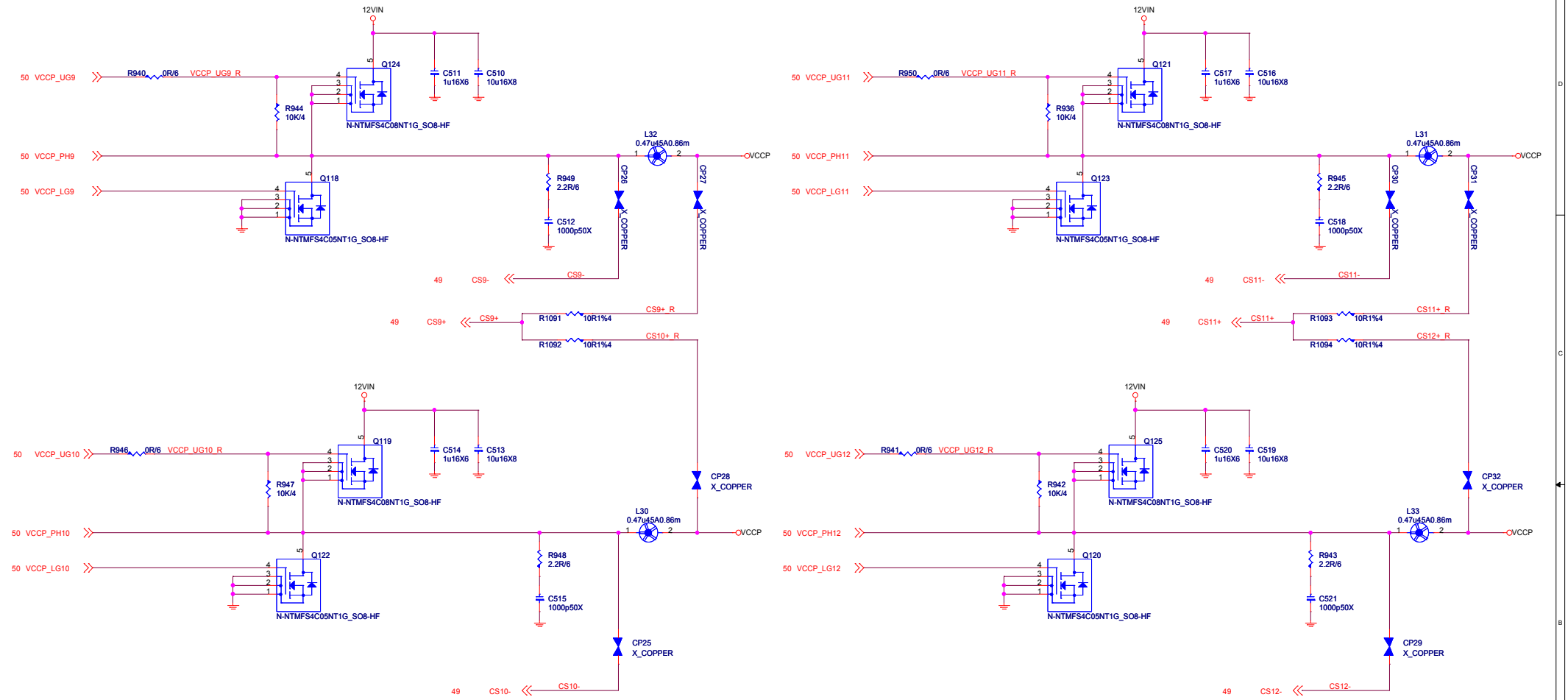

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: VCC CAP	Rev: 1.0
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DDR Power:1.5V

DDR3_1.5V 4.75A+12A+1.1A+6A=23.85A

4.75A FOR CPU

12A FOR 4DIMM

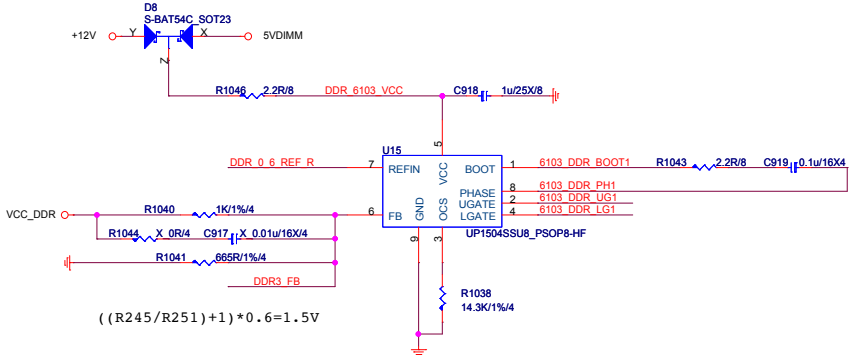
1.1A FOR DDR VTT

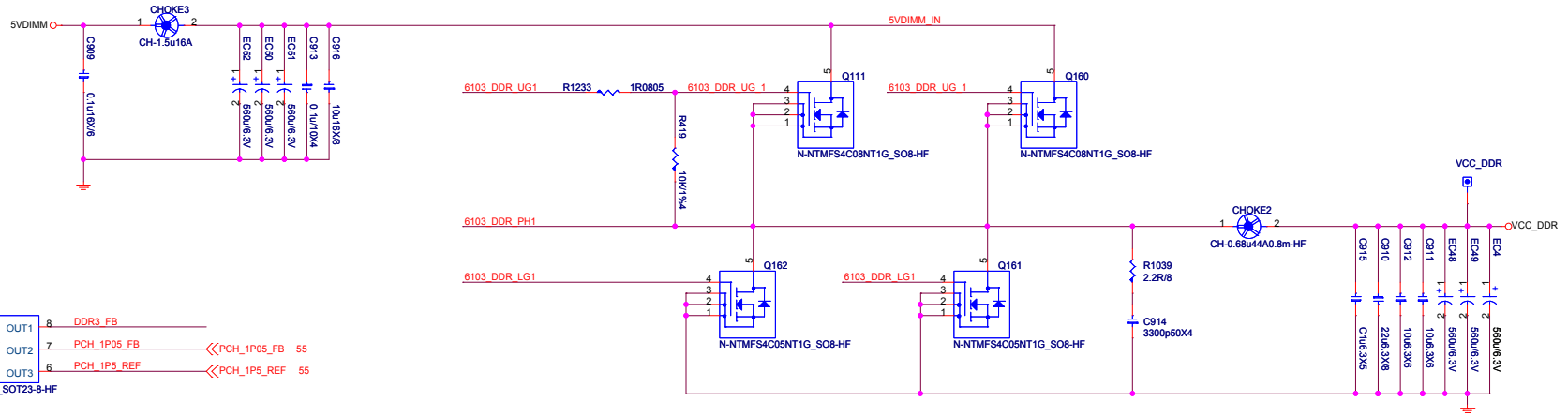
6A FOR PCH_Core 1.05V

OCP 23.85*1.5=36A

36A=(20uA*Rocs(R103)/(4*Rdson(Low side2mohm))

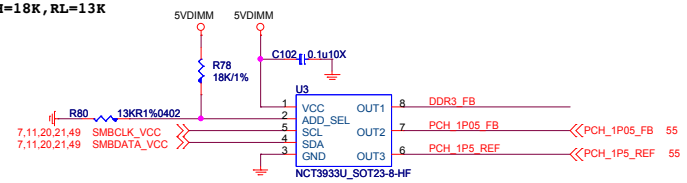
R103=14.3K ohm

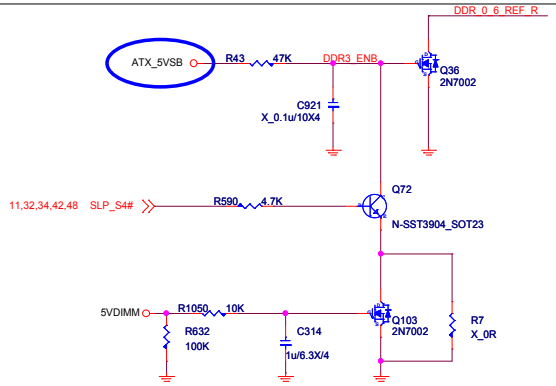




UPI VOLTAGE CONSOLE

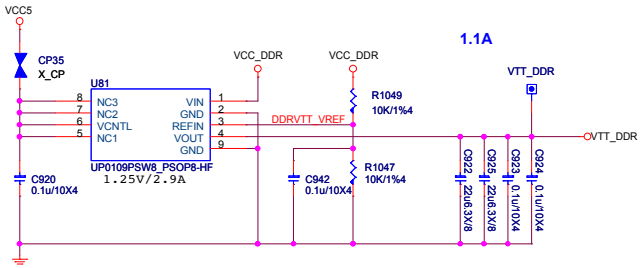
0x26:RH=18K,RL=13K

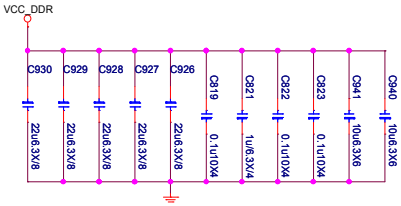




DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: UP1504S DDR POWER	Rev: 1.0
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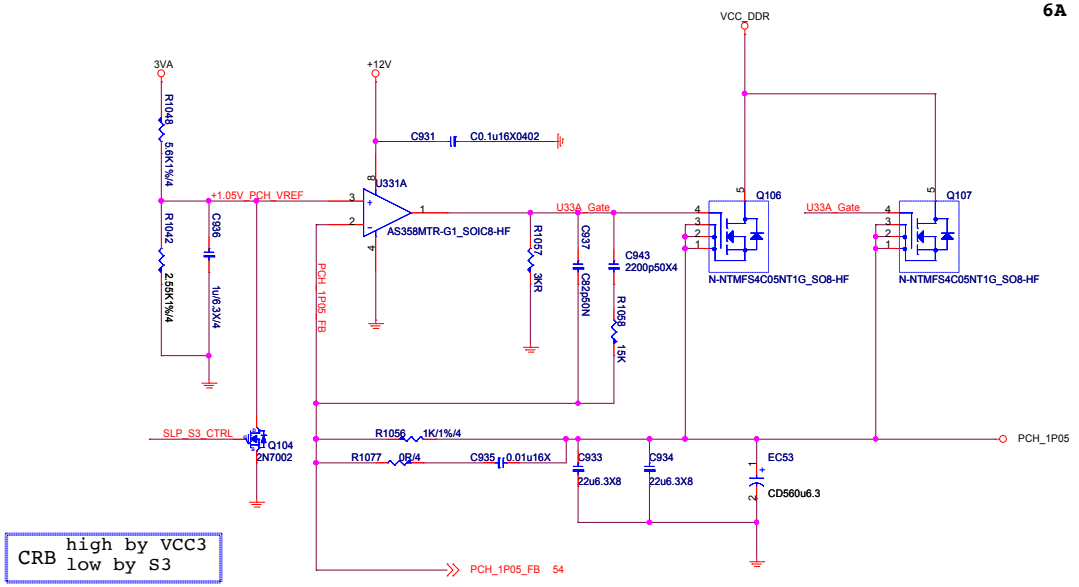
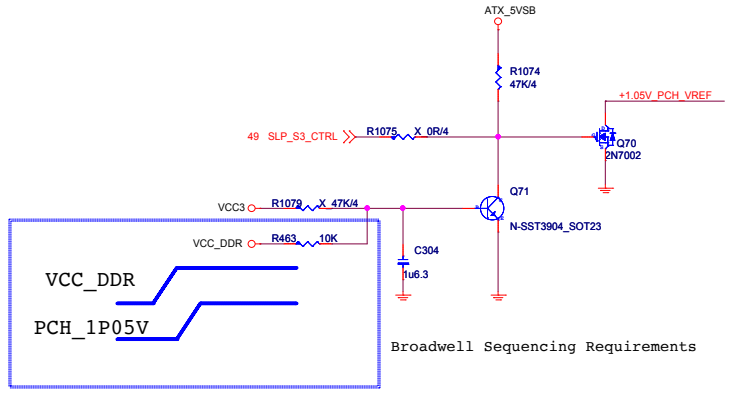
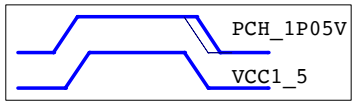
PCH Power:1.05V

6A





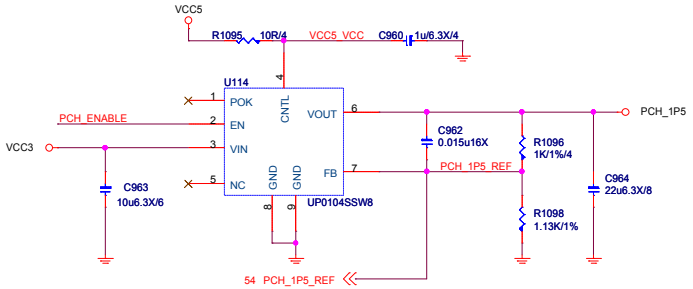
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH



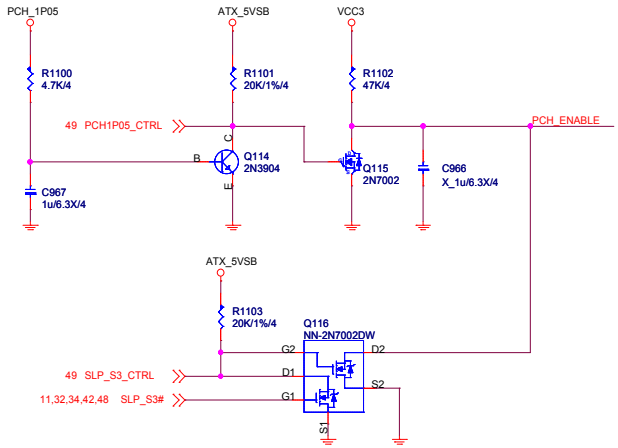
PCH_1P5

PCH: 0.35A

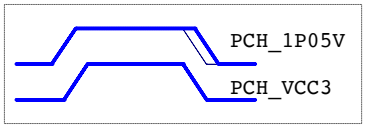
OV: 一階10mV



Waitting PCH_1P05 Ready

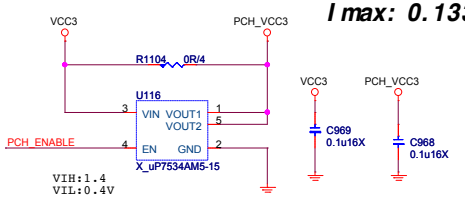


VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH

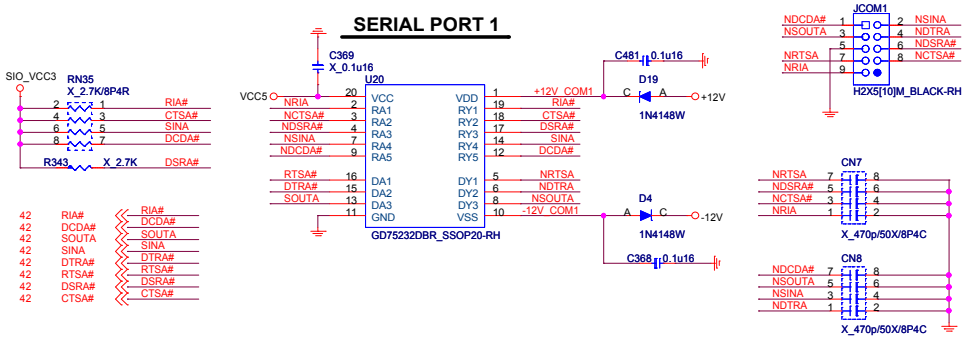


PCH_VCC3

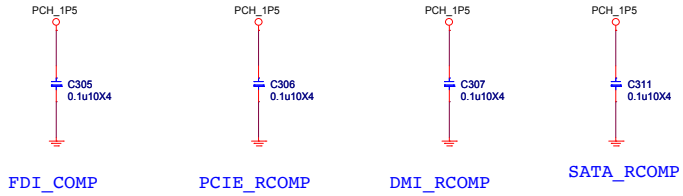
I max: 0.133A



MICRO-STAR INT'L CO.,LTD		
MS-7916		
Size: Custom	Document Description: LYNX Power -PV3101	Rev: 1.0
Date: Thursday, March 20, 2014	Sheet 55 of 62	



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7916	
Size: Custom	Document Description: XDP CPU & PCH	Rev: 1.0
Date: Thursday, March 20, 2014	Sheet 56 of 62	



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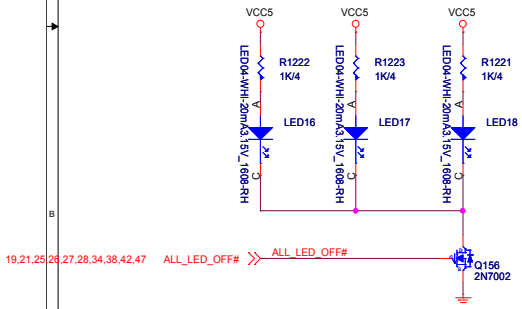
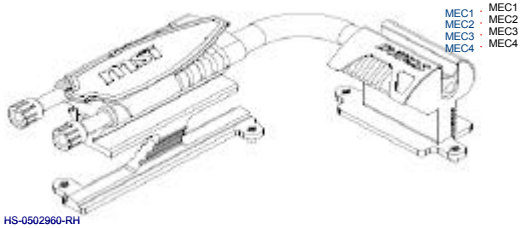
MS-7916		
Size: Custom	Document Description: EMI CAP	Rev: 1.0
Date: Thursday, March 20, 2014	Sheet 57 of 62	

PCH



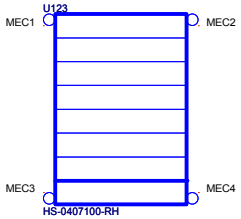
CPU Sink 料號

U122



HS-0502960-RH

PCH Sink 料號



HS-0407100-RH

HDMI_RLA1 — Real Label — X_HDMI_RLA

HDMI Label Part Number

HDMI_LA1 — Label — X_HDMI LABEL

HDMI Virtual Part Number

LA4 — AMI_BIOS LABLE — X_BIOS_LABLE

LABEL1 — MKT — X_BUY

CPU_H1 — CPU 鐵座 — CPU_H1

SLI_LA1 — Label — SLI LABEL

Creative — Label — Creative

LABEL2 — THX — X_MB3

VIRTU_LA1 — Label — X_Virtu Universal MVP LABEL

PCB1

7916_0A

BAT1_X1 — BAT-BCR2032P-RH

PD0-0791610-G37,精成,23,寶安恩斯邁廠(MSIS)
PD0-0791610-E48,競華,23,寶安恩斯邁廠(MSIS)

Simulation

SIM1 — SIM4 — X_PIN1*2
SIM2 — SIM3 — X_PIN1*2
SIM3 — SIM1 — X_PIN1*2
SIM4 — SIM2 — X_PIN1*2

Mounting Holes

MH2 — X_MH001
MH3 — X_MH001
MH4 — X_MH001
C753 0.1u10X
C754 0.1u10X
MH5 — X_MH001
MH6 — X_MH001
MH7 — X_MH001
MH8 — X_MH001
MH9 — X_MH001
MH10 — X_MH001

Optical Fiducial Marks-120

FM1 — X_FM
FM2 — X_FM
FM3 — X_FM
FM4 — X_FM
FM5 — X_FM
FM6 — X_FM
FM7 — X_FM
FM8 — X_FM

OPT	Configure	BOM	Function
		601-7751-10S	MS-7751 30 Z77 MPower 4*DDR3+3*PCI-Ex16,4*PCI-Ex1,+4*SATAII+2*SATAIII +8*USB2.0+8*USB3.0+HD 8Ch Audio+HDMI+DisplayPort+Gb LAN,Hi-C CAP,EuP,RoHS

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