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MS-7A95

ATX

Ver: 1.0

Basinfall Platform

CPU:

Skylake X/Kabylake X

System Chipset:

Kaby Lake PCH-X

Onboard Chip:

HD Audio Codec:ALC1220

LAN-Intel I219+I211

SIO:NTC6795D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

*DDRIV (UP to 2677MHz) * 8DIMM (4 Channel)*

ACPI:

MPS

PWM:

VR13 -IR35201

Expansion Slots:

*PCI Express (X16) Slot * 2*
*PCI Express (X8) Slot * 1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 2*

Other:

*SATA3.0 *8*
*USB2.0 *6 Ports (2R/4F)*
*REAR USB30*5 + USB3.1*1 & TYPEC*1*
*FRONT USB3.0 *4+TYPEC*1*

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MS-7A95

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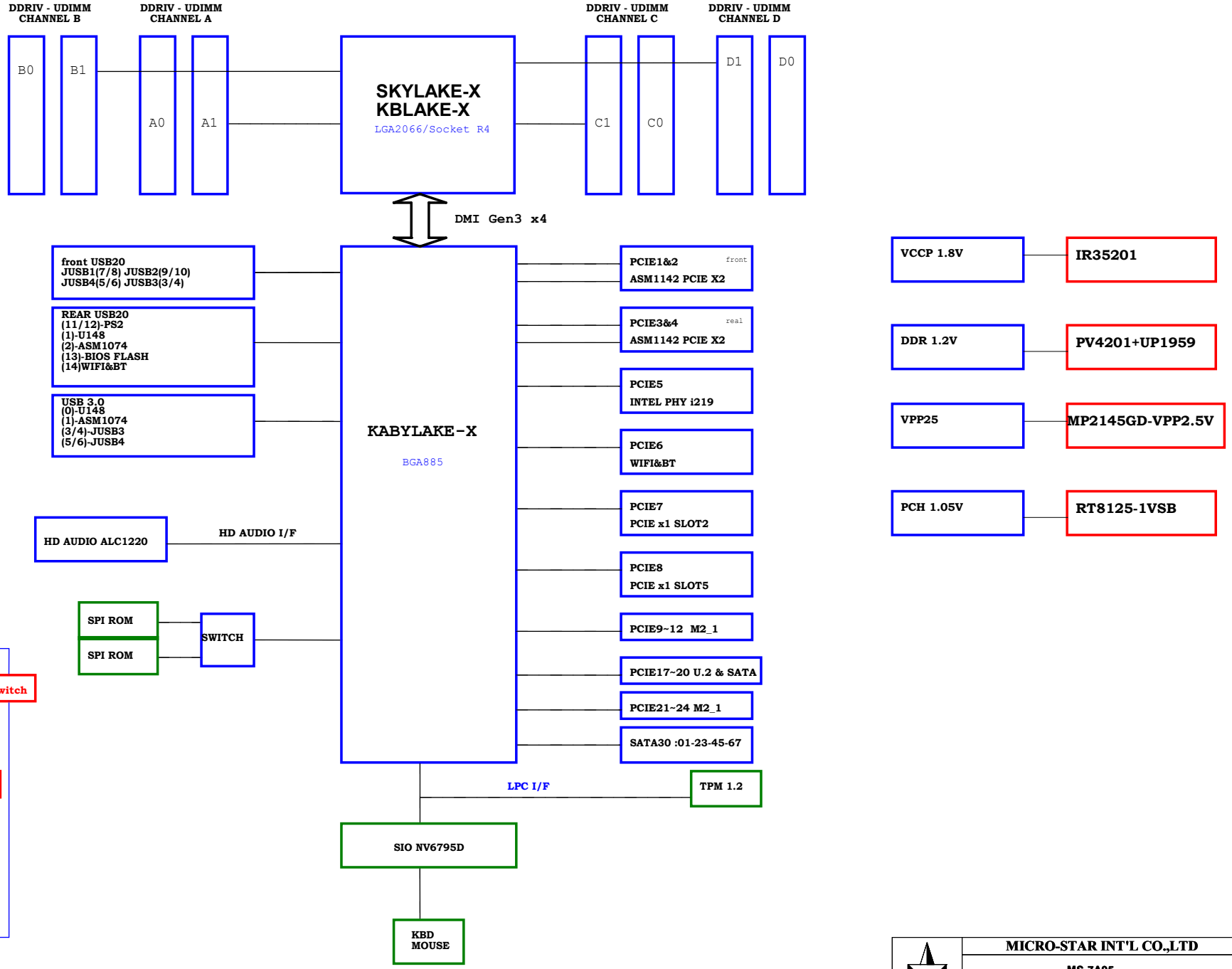
MS-7A95 Block Diagram



MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: Block Diagram
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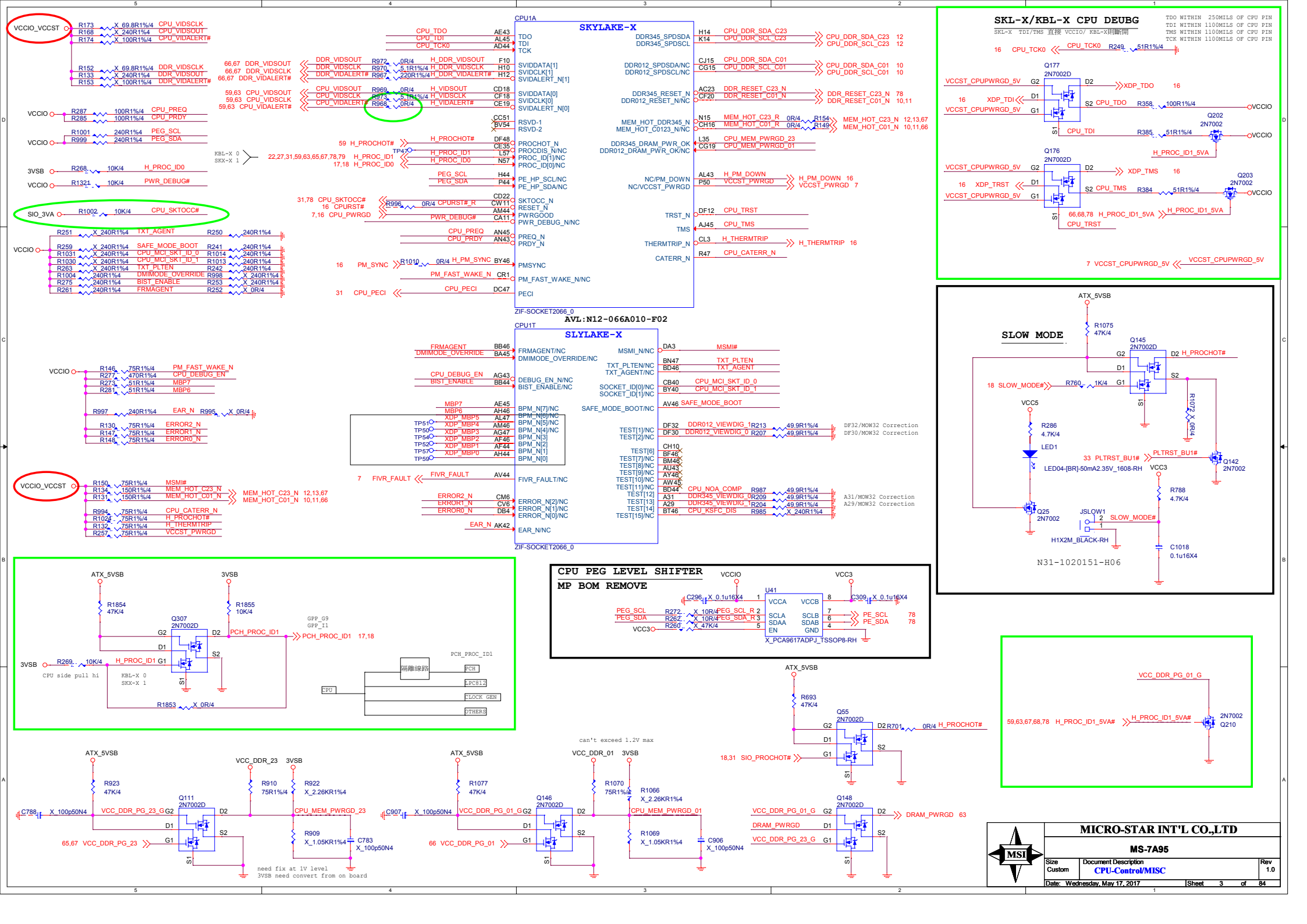
SKYLAKE-X
SLYLAKE-X
ZIF-SOCKET2066_0
AVL:N12-066A010-F02
SKL-X/KBL-X CPU DEUBG
SLOW MODE
CPU PEG LEVEL SHIFTER
MP BOM REMOVE
MICRO-STAR INT'L CO.,LTD
MS-7A95
CPU-Control/MISC
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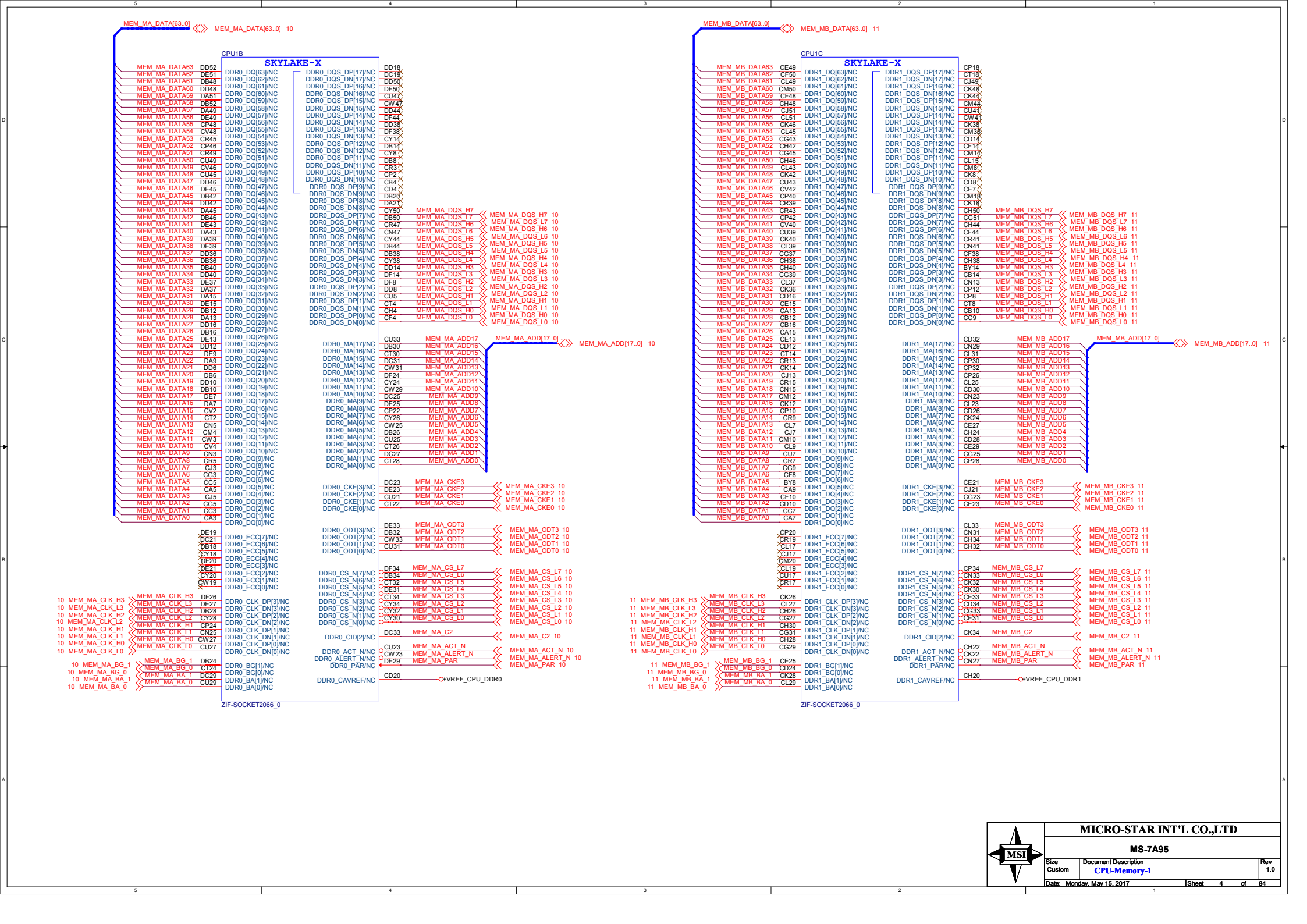

MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: CPU-Memory-1
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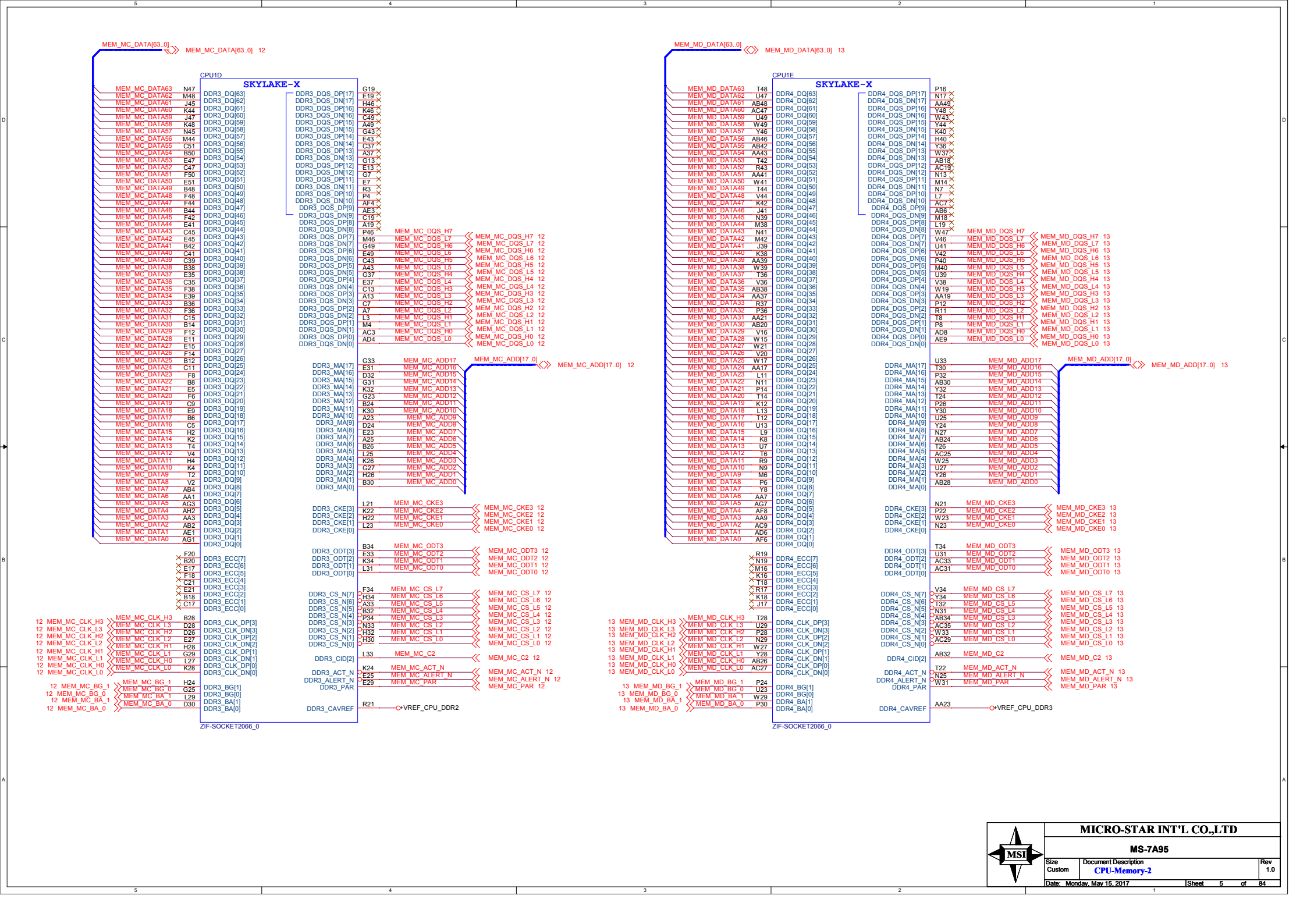
MEM_MC_DATA[63..0]
MEM_MC_DATA[63..0] 12
CPU1D
SKYLAKE-X
ZIF-SOCKET2066_0
MEM_MD_DATA[63..0]
MEM_MD_DATA[63..0] 13
CPU1E
SKYLAKE-X
ZIF-SOCKET2066_0
MEM_MC_ADD[17..0]
MEM_MC_ADD[17..0] 12
MEM_MD_ADD[17..0]
MEM_MD_ADD[17..0] 13
+VREF_CPU_DDR2
+VREF_CPU_DDR3
MICRO-STAR INT'L CO.,LTD
MS-7A95
Size
Custom
Document Description
CPU-Memory-2
Rev
1.0
Date: Monday, May 15, 2017
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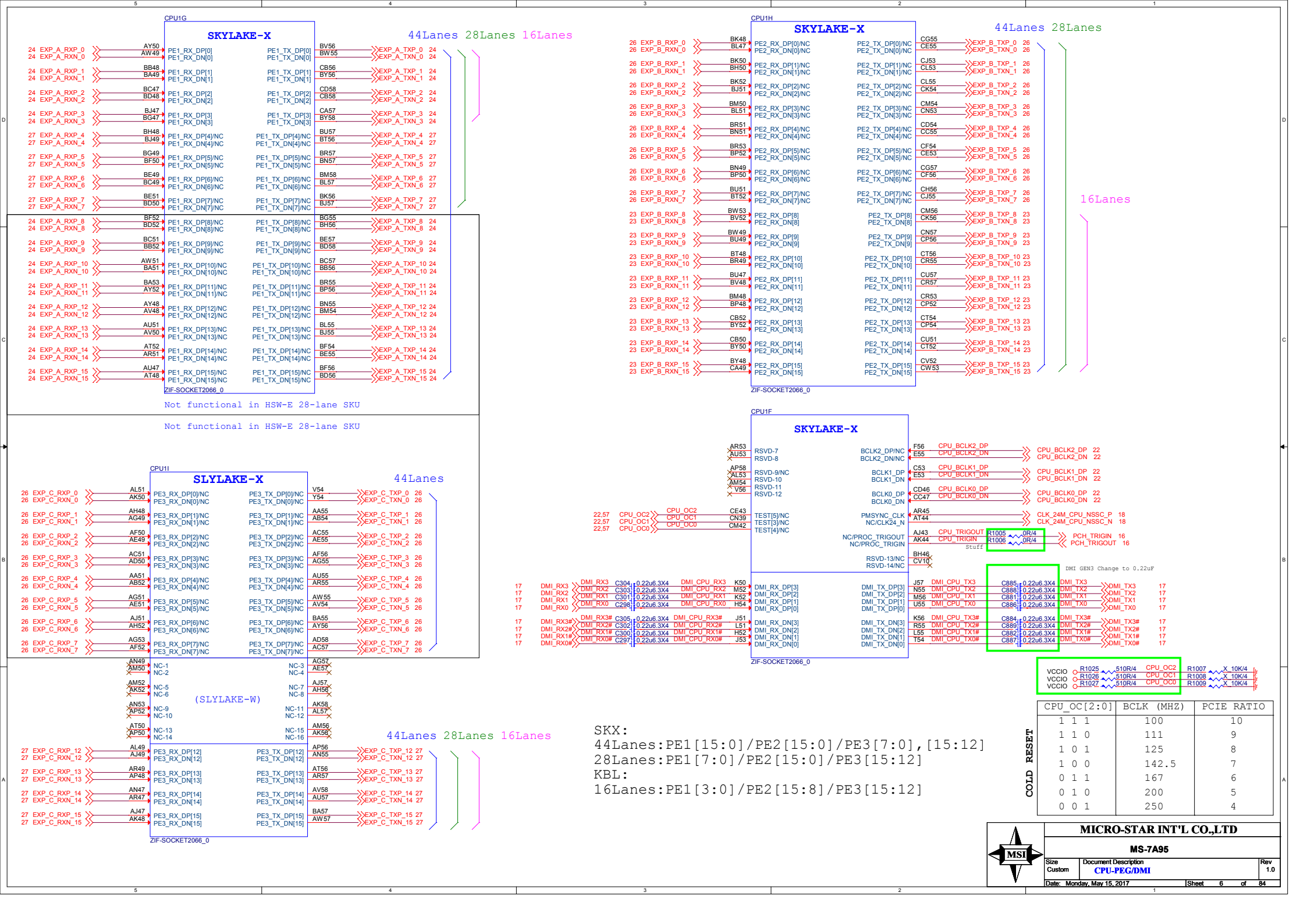
CPU1G
SKYLAKE-X
44Lanes 28Lanes 16Lanes
ZIF-SOCKET2066_0
Not functional in HSW-E 28-lane SKU
Not functional in HSW-E 28-lane SKU
CPU1I
SLYLAKE-X
44Lanes
(SLYLAKE-W)
ZIF-SOCKET2066_0
44Lanes 28Lanes 16Lanes
CPU1H
SKYLAKE-X
44Lanes 28Lanes
16Lanes
ZIF-SOCKET2066_0
CPU1F
SKYLAKE-X
ZIF-SOCKET2066_0
DMI GEN3 Change to 0.22uF
SKX:
44Lanes:PE1[15:0]/PE2[15:0]/PE3[7:0],[15:12]
28Lanes:PE1[7:0]/PE2[15:0]/PE3[15:12]
KBL:
16Lanes:PE1[3:0]/PE2[15:8]/PE3[15:12]
COLD RESET
CPU_OC[2:0] | BCLK (MHZ) | PCIE RATIO
1 1 1 | 100 | 10
1 1 0 | 111 | 9
1 0 1 | 125 | 8
1 0 0 | 142.5 | 7
0 1 1 | 167 | 6
0 1 0 | 200 | 5
0 0 1 | 250 | 4
MICRO-STAR INT'L CO.,LTD
MS-7A95
Size Custom
Document Description CPU-PEG/DMI
Rev 1.0
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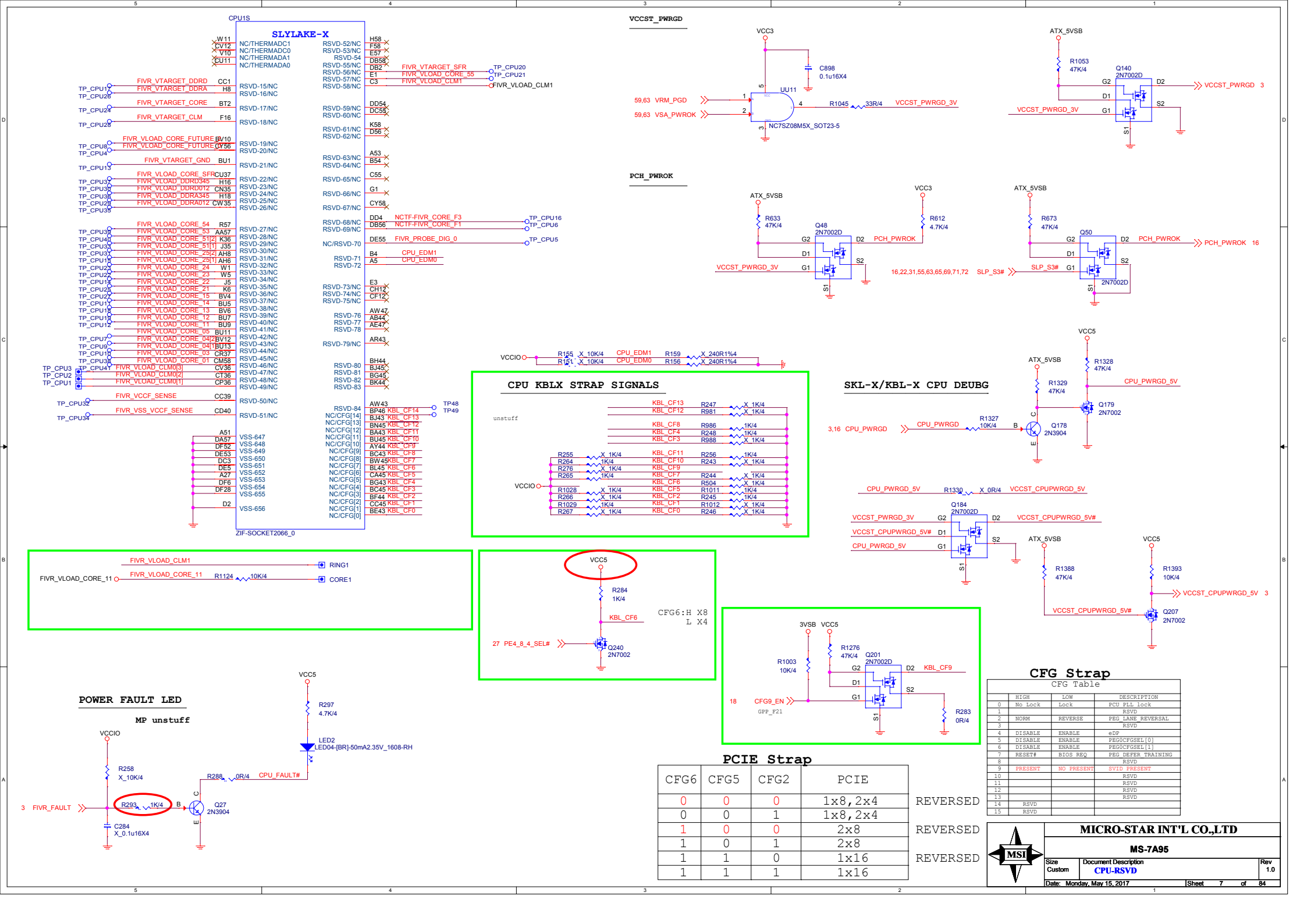


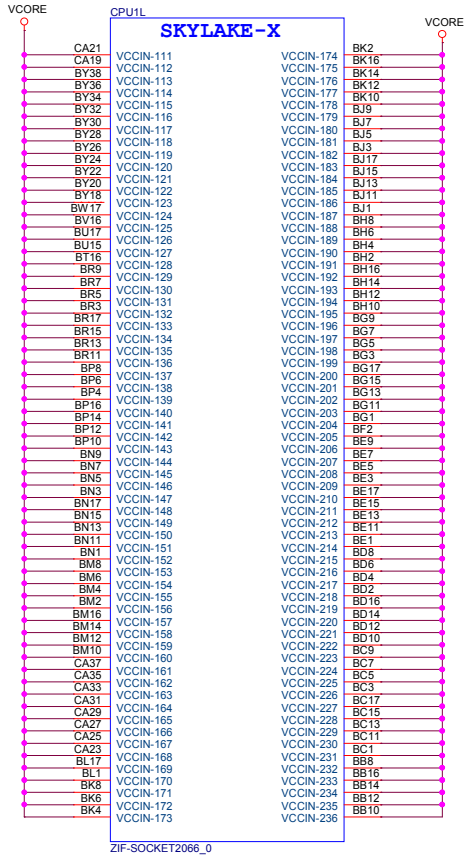
PCIE Strap

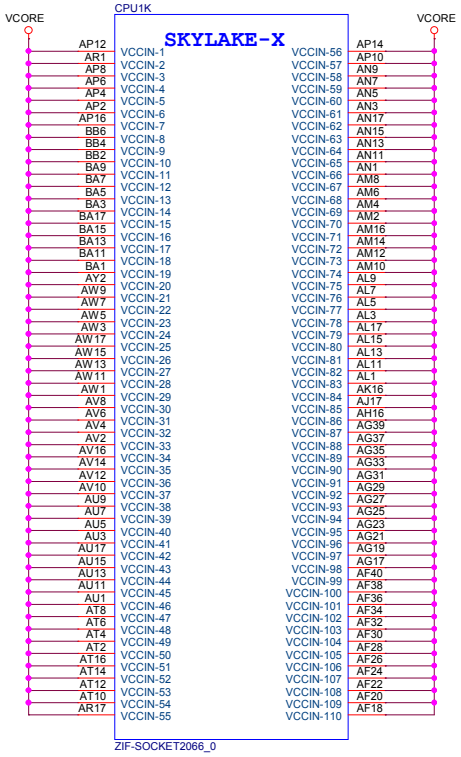
CFG6	CFG5	CFG2	PCIE	
0	0	0	1x8,2x4	REVERSED
0	0	1	1x8,2x4	
1	0	0	2x8	REVERSED
1	0	1	2x8	
1	1	0	1x16	REVERSED
1	1	1	1x16	

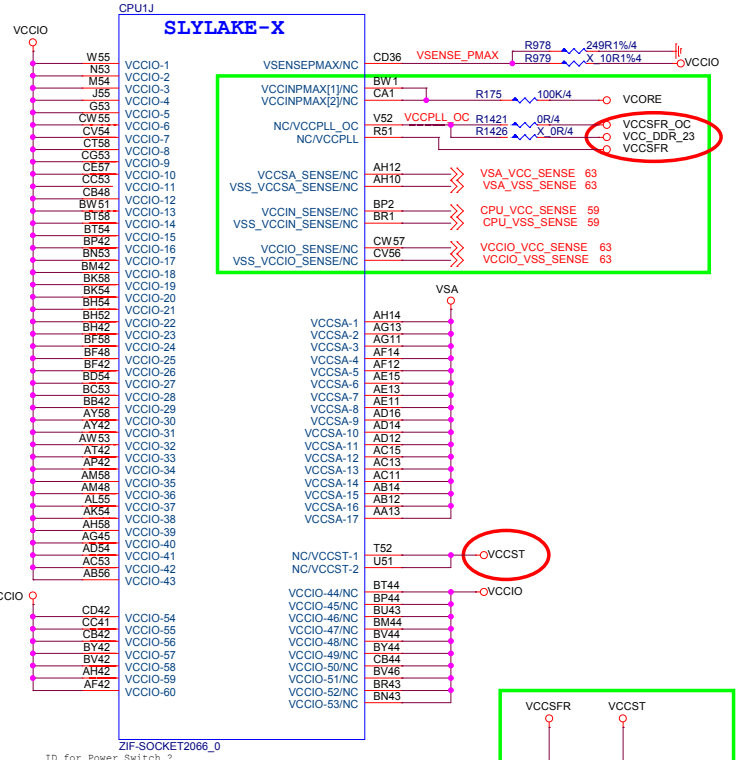
CFG Strap

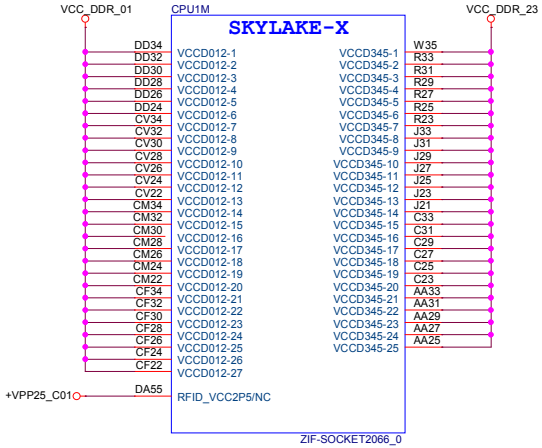
CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

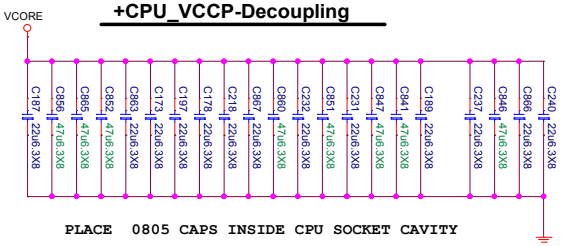




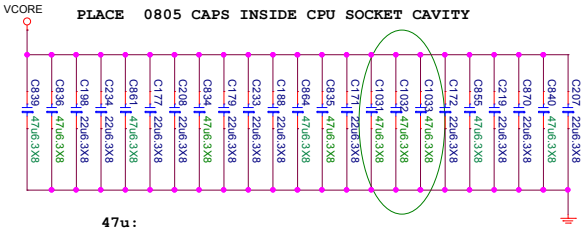




+CPU_VCCP-Decoupling



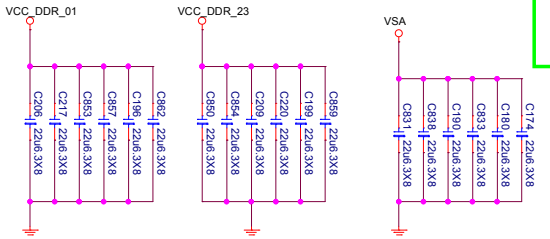
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY



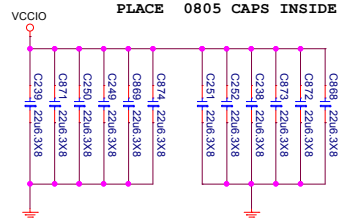
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY

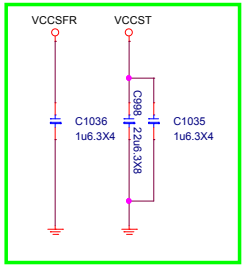
47u:
C11-4767314-M09
C11-4767314-S02
C11-4767314-T04
04/20 22u change to 47u for transient 16 pec
add 3 pec 47u

+CPU_DDR-Decoupling



PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY





MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size: Custom	Document Description: CPU-Power	Rev: 1.0
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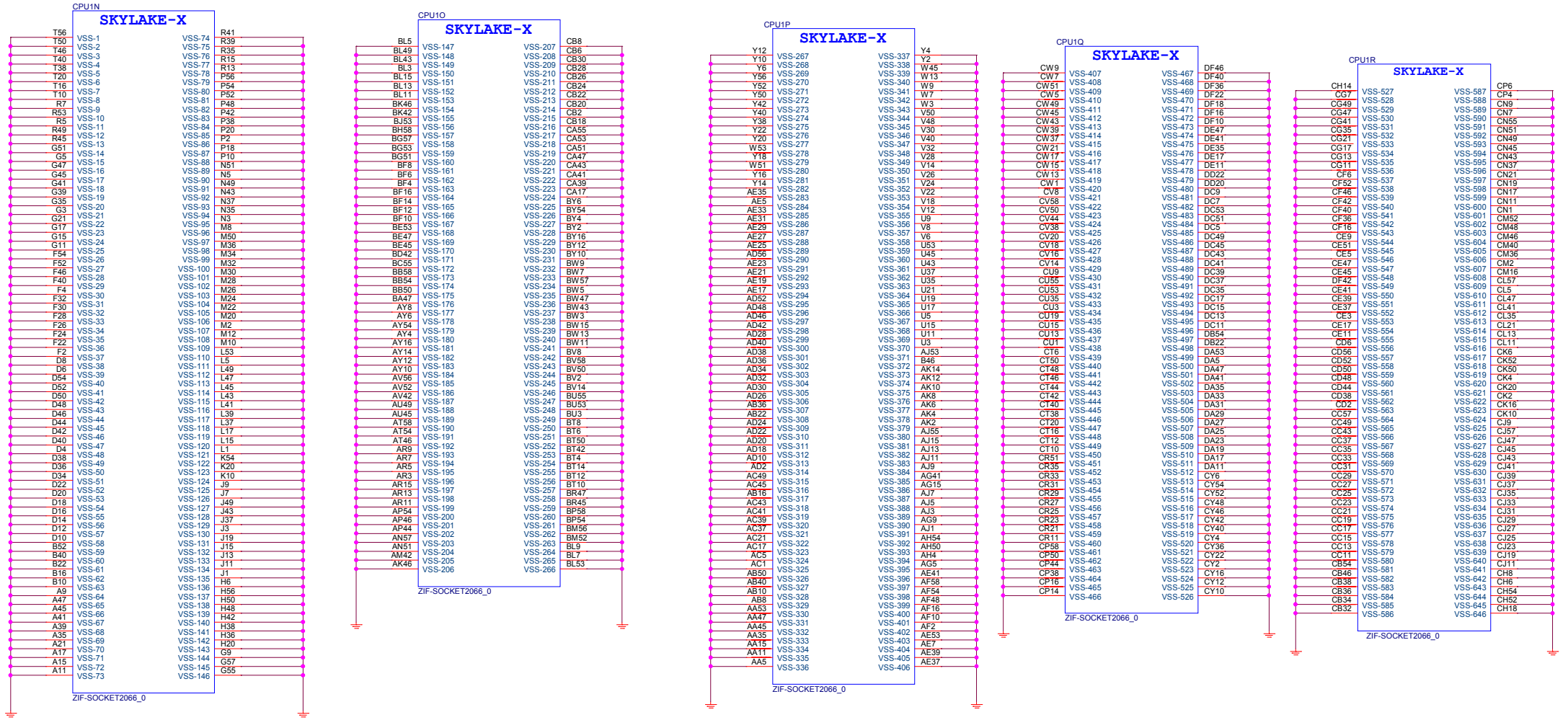

MICRO-STAR INT'L CO.,LTD

MS-7A95

Size	Document Description	Rev
Custom	CPU-GND	1.0

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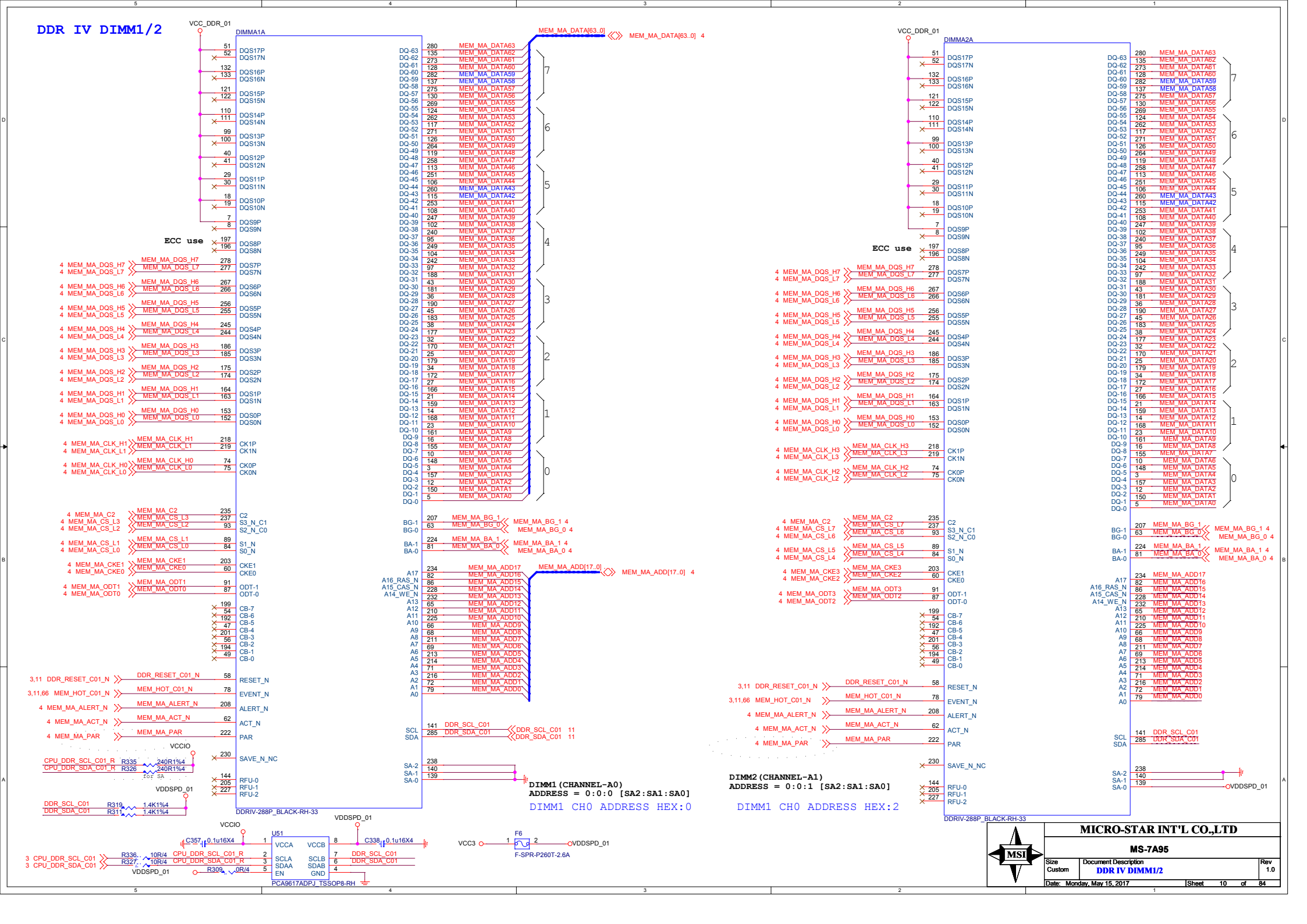
DDR IV DIMM1/2



MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: DDR IV DIMM1/2
Rev: 1.0	
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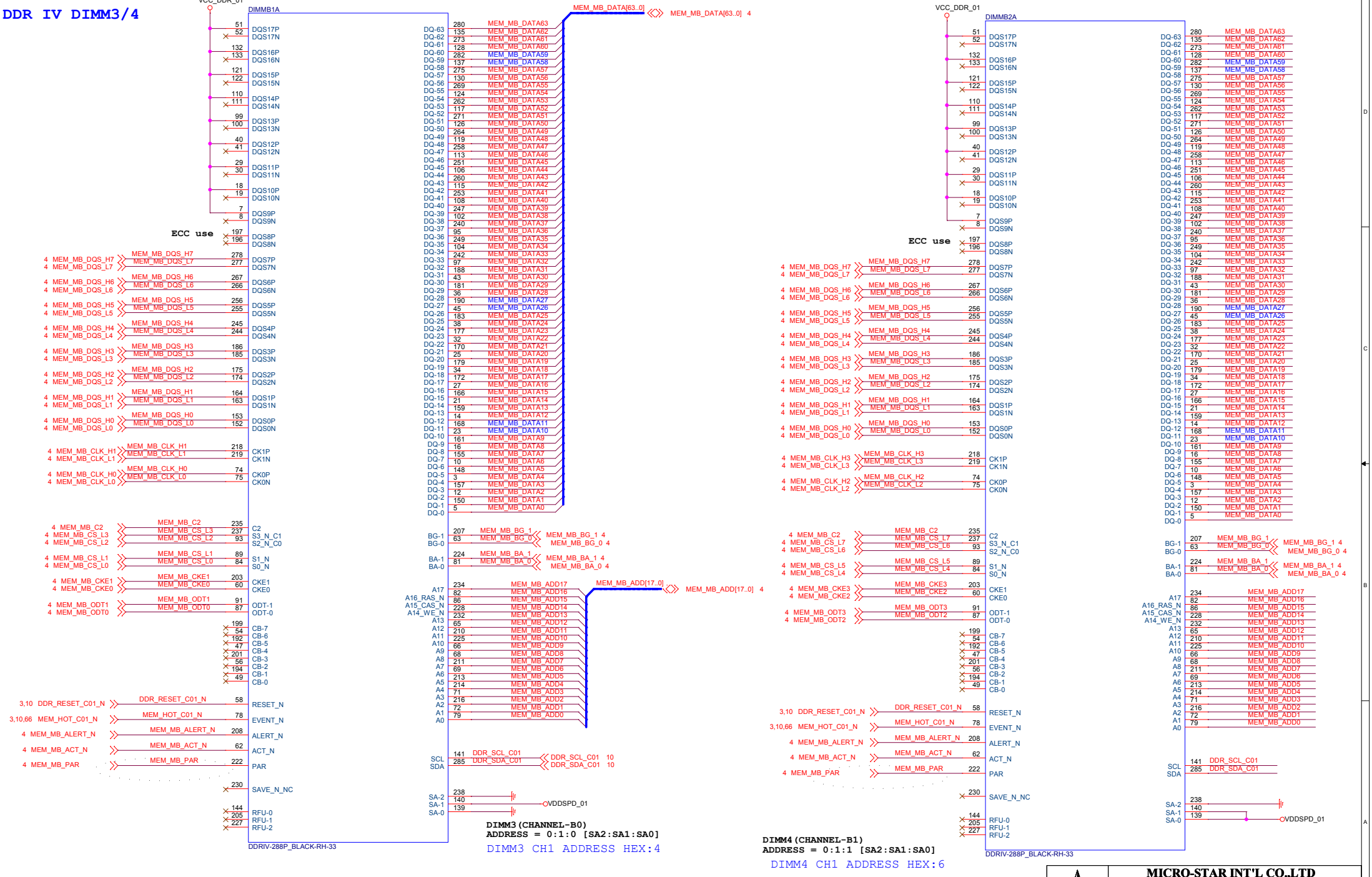
DDR IV DIMM3/4



MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: DDR IV DIMM3/4
Rev: 1.0	
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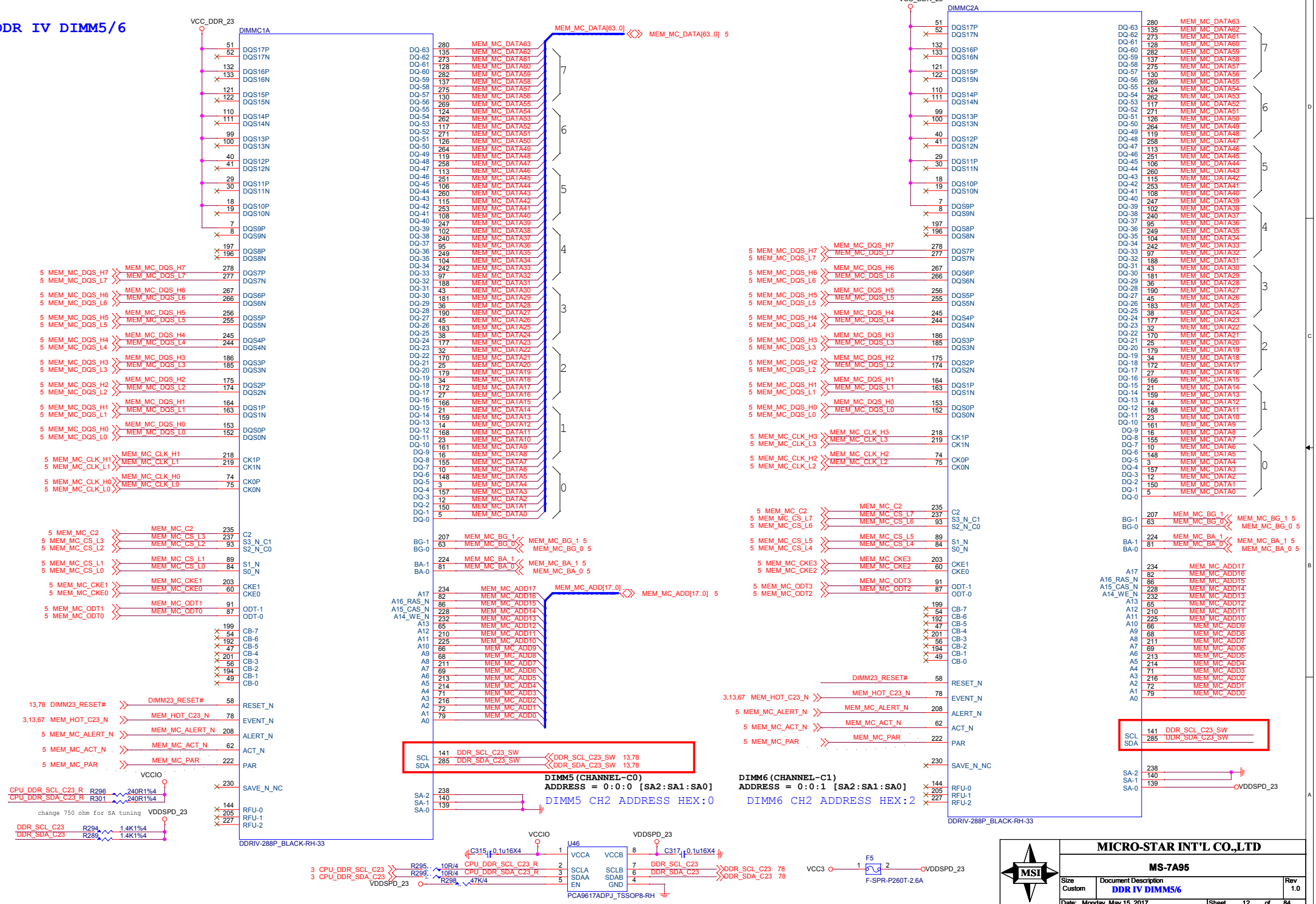
DDR IV DIMM5/6



MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: DDR IV DIMM5/6
Rev: 1.0	
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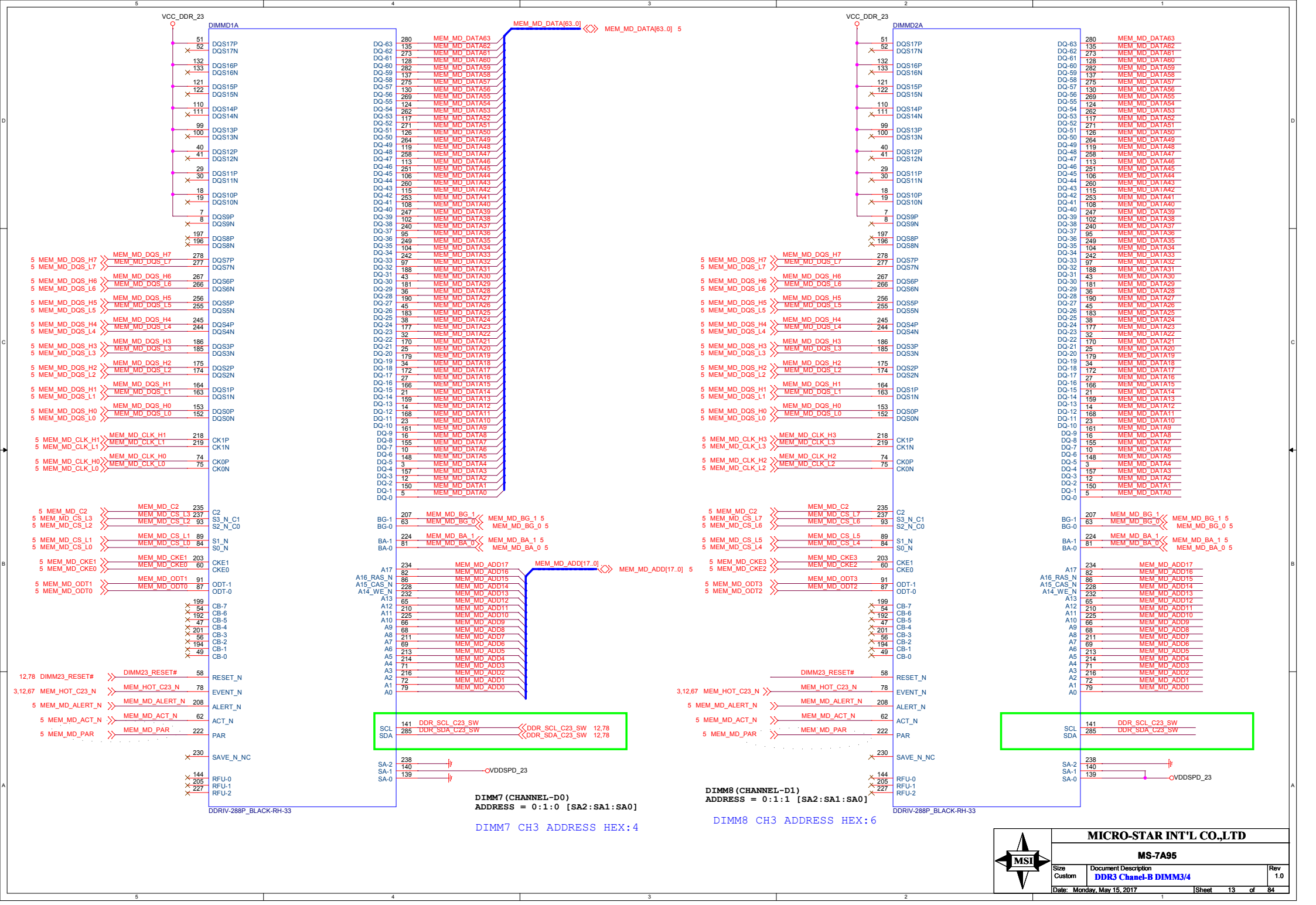
VCC_DDR_23
DIMMD1A
MEM_MD_DATA[63..0]
MEM_MD_DATA[63..0] 5
DDRIV-288P_BLACK-RH-33
DIMM7(CHANNEL-D0)
ADDRESS = 0:1:0 [SA2:SA1:SA0]
DIMM7 CH3 ADDRESS HEX:4
VCC_DDR_23
DIMMD2A
DDRIV-288P_BLACK-RH-33
DIMM8(CHANNEL-D1)
ADDRESS = 0:1:1 [SA2:SA1:SA0]
DIMM8 CH3 ADDRESS HEX:6
MEM_MD_ADD[17..0]
MEM_MD_ADD[17..0] 5
VDDSPD_23
MICRO-STAR INT'L CO.,LTD
MS-7A95
Size
Custom
Document Description
DDR3 Chanel-B DIMM3/4
Rev
1.0
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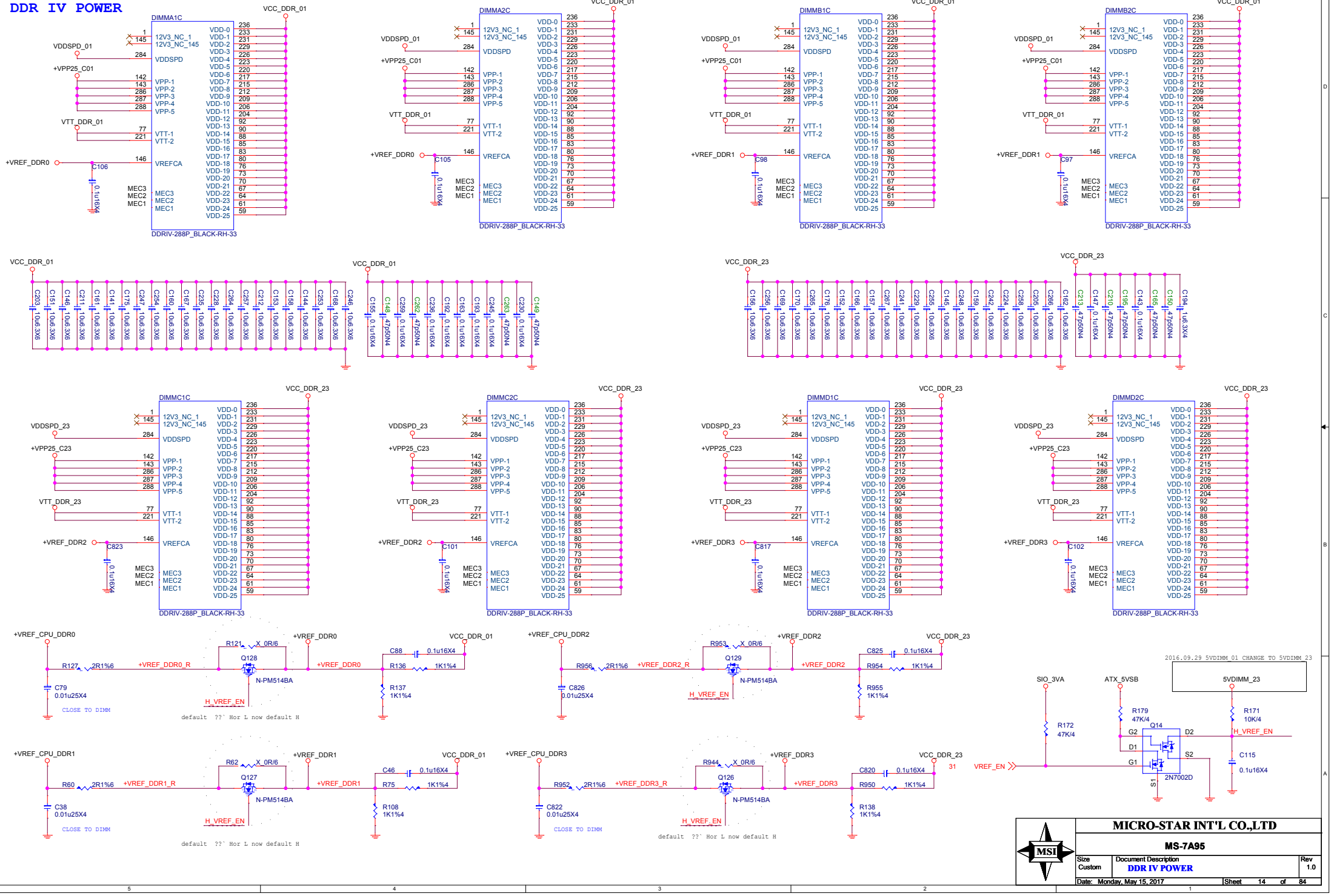
DDR IV POWER



MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size: Custom	Document Description: DDR IV POWER	Rev: 1.0
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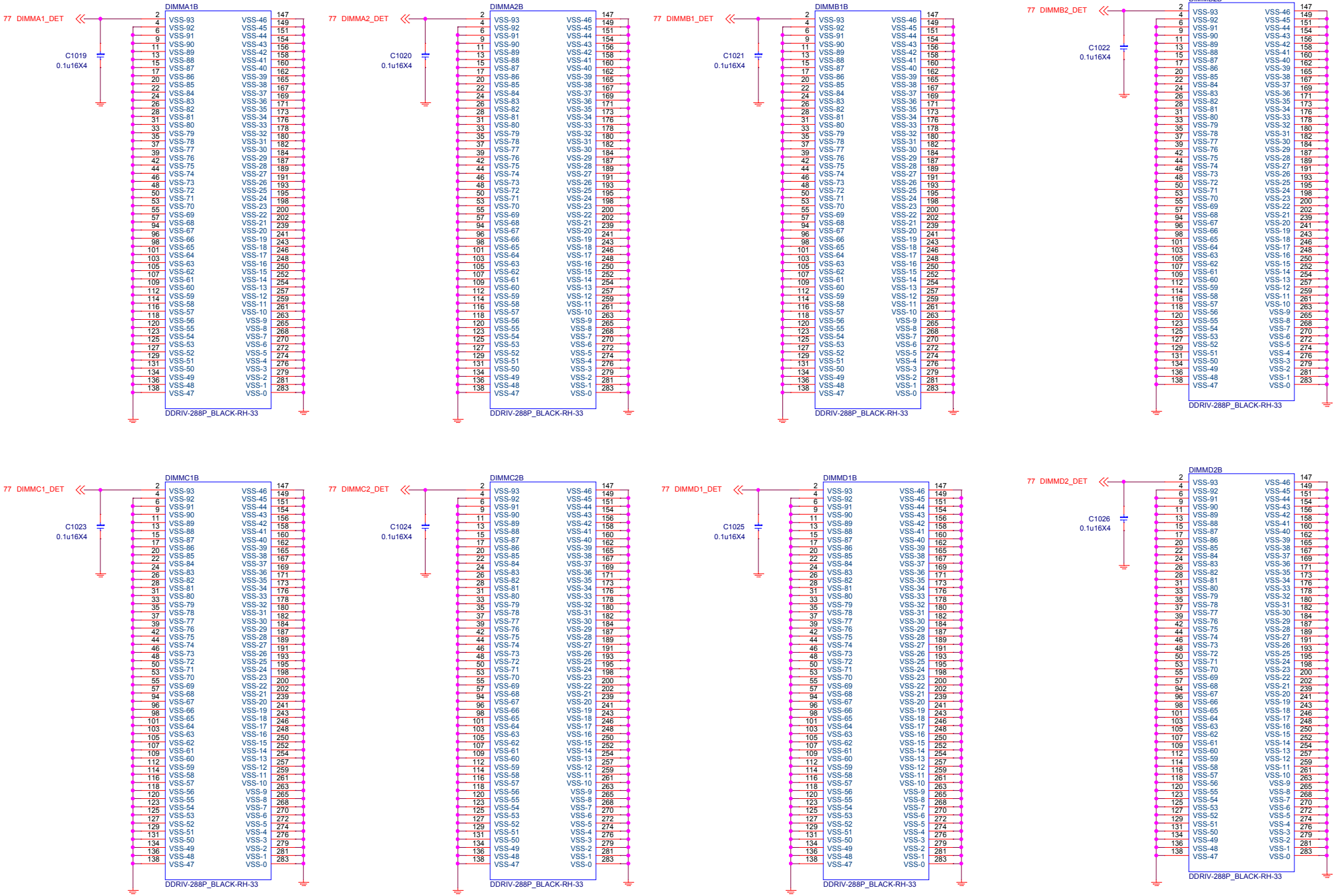
DDR IV GND



MICRO-STAR INT'L CO.,LTD			
MS-7A95			
Size: Custom	Document Description: DDR IV GND		Rev: 1.0
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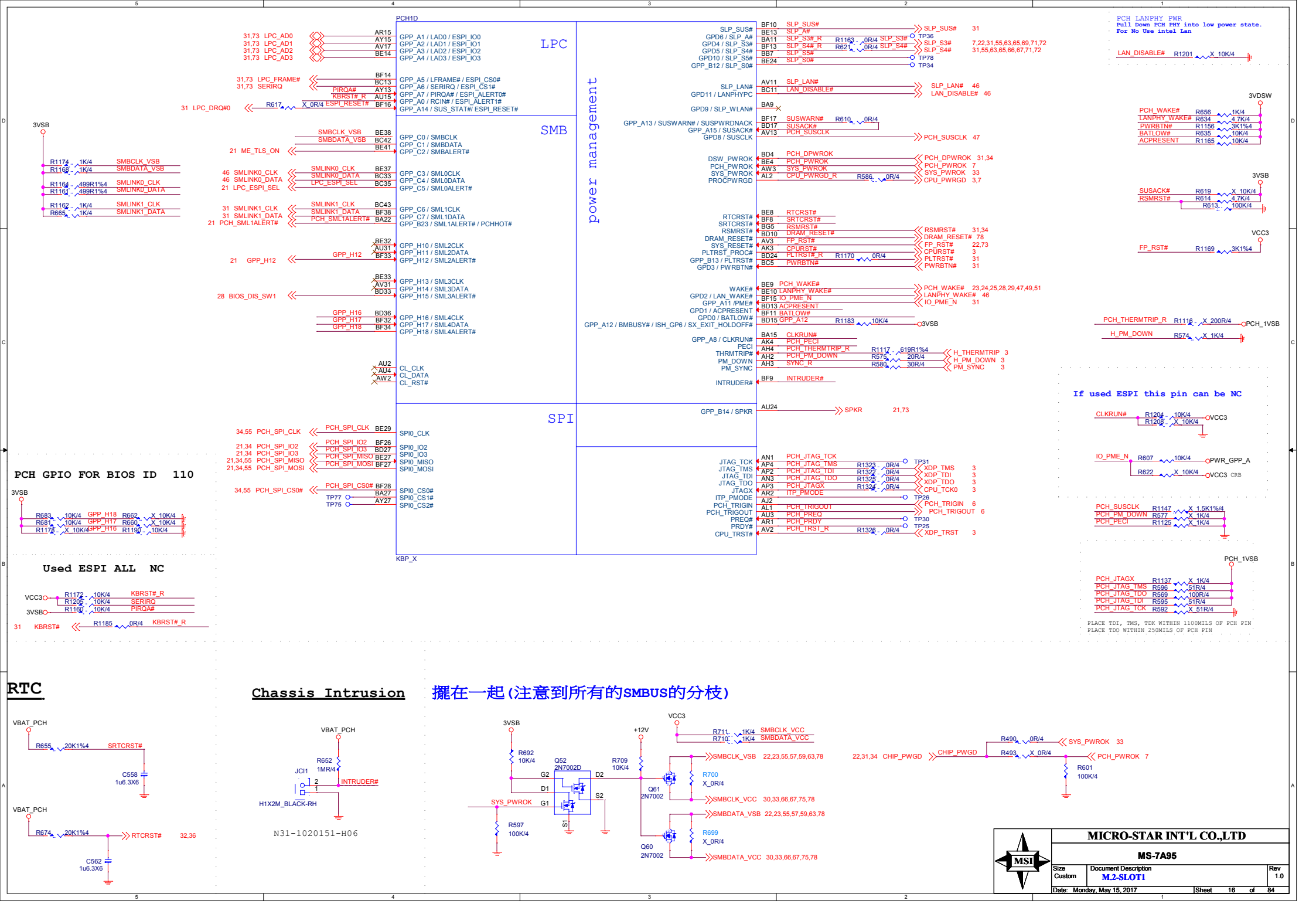
PCH1D
LPC
SMB
SPI
power management
KBP_X
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
If used ESPI this pin can be NC
PCH GPIO FOR BIOS ID 110
Used ESPI ALL NC
RTC
Chassis Intrusion
擺在一起(注意到所有的SMBUS的分枝)
N31-1020151-H06
PLACE TDI, TMS, TDK WITHIN 1100MILS OF PCH PIN
PLACE TDO WITHIN 250MILS OF PCH PIN
MICRO-STAR INT'L CO.,LTD
MS-7A95
M.2-SLOT1
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PCH1B

DMI

PCH1C

USB3

USB2

PCIE

PCH_AUDIO

PIN	Default Port Mapping
OC0#	PORT 0 1
OC1#	PORT 2 3
OC2#	PORT 4 5
OC3#	PORT 6 7
OC4#	PORT 8 9
OC5#	PORT 10 11
OC6#	PORT 12 13
OC7#	NO USE

KBP_X

JUSB1
JUSB3
USB3/ USB2
JUSB2
JUSB4/JUSB5
PS2_USB
USB1

USB2_COMP WITHIN 1 INCH

PCH1F

PORT B
PORT C
PORT D

Company	MICRO-STAR INT'L CO.,LTD
Model	MS-7A95
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Rev	1.0
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PCH_CLK

Used ESPI(GPPA) GPIO Group A will be come 1.8V leve)

PCH1E

GPP_A9 / CLKOUT_LPC0 / ESPI_CLK
GPP_A10 / CLKOUT_LPC1
GPP_A16 / CLKOUT_48
SKL_H Sever Only
LPC

RTC

24MHz

XCLK_BIASREF < 500 mil

KBP_X

PCH1A

GPIO

remove led x16、x8 LED gpio, use mcu control

Close to PCH

<1 inch

32.768KHZ12.5p

24MHZ20p

VROC pin header

BH1X4H-2PITCH_BLACK-RH-1

W/ SMI/NMI Funtion
GPP_B[23,20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]

GPP_D21
high:A0.A1 version for asm2142
low: for asm3142

BOM ID 0 0 0 AC
0 0 1 non AC

GPI GPP_D21
HIGH : A0,A1 Version FOR ASM2142
LOW : Furture Version FOR ASM2142

	R220	R227
CLK GEN	unstuff	unstuff
HOTKEY	Stuff	Stuff

0716

MICRO-STAR INT'L CO.,LTD

MS-7A95

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Custom	M.2-SLOT1	1.0

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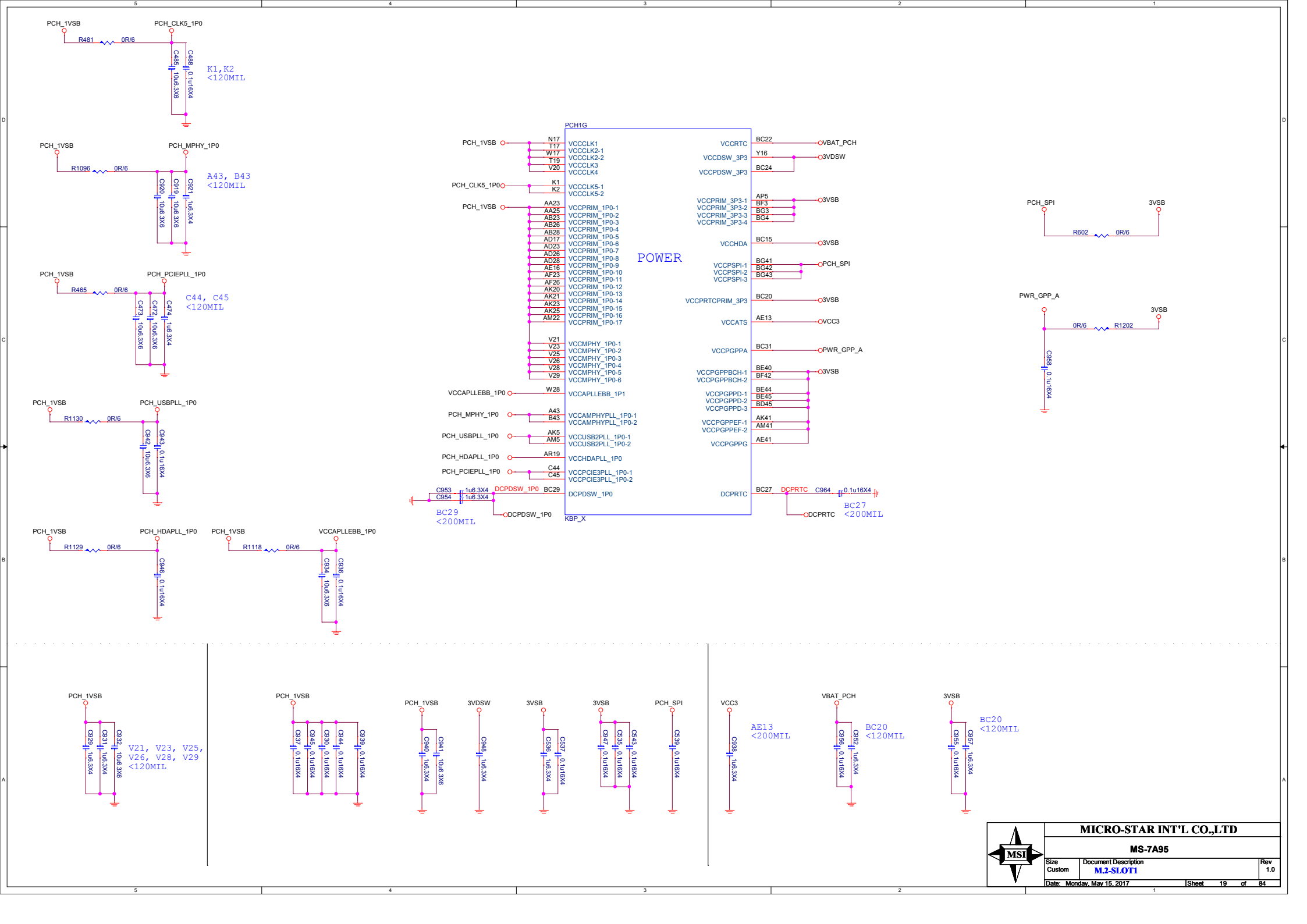

MICRO-STAR INT'L CO.,LTD

MS-7A95

Size	Document Description	Rev
Custom	M.2-SLOT1	1.0

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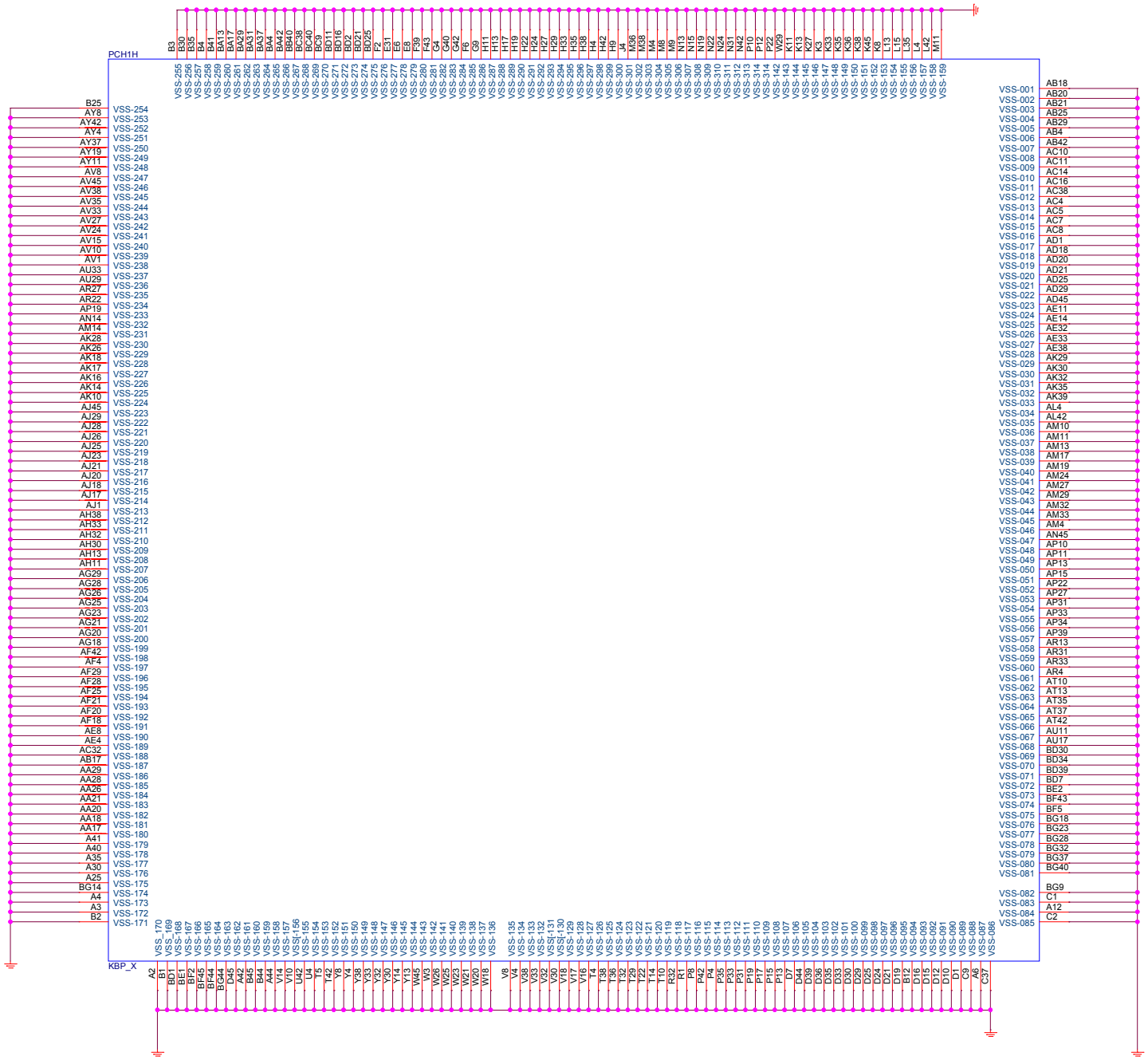
PCH1H
KBP_X
B25
AY8
AY42
AY4
AY37
AY19
AY11
AV8
AV45
AV38
AV35
AV33
AV27
AV24
AV15
AV10
AV1
AU33
AU29
AR27
AR22
AP19
AN14
AM14
AK28
AK26
AK18
AK17
AK16
AK14
AK10
AJ45
AJ29
AJ28
AJ26
AJ25
AJ23
AJ21
AJ20
AJ18
AJ17
AJ1
AH38
AH33
AH32
AH30
AH13
AH11
AG29
AG28
AG26
AG25
AG23
AG21
AG20
AG18
AF42
AF4
AF29
AF28
AF25
AF21
AF20
AF18
AE8
AE4
AC32
AB17
AA29
AA28
AA26
AA21
AA20
AA18
AA17
A41
A40
A35
A30
A25
BG14
A4
A3
B2
AB18
AB20
AB21
AB25
AB29
AB4
AB42
AC10
AC11
AC14
AC16
AC38
AC4
AC5
AC7
AC8
AD1
AD18
AD20
AD21
AD25
AD29
AD45
AE11
AE14
AE32
AE33
AE38
AK29
AK30
AK32
AK35
AK39
AL4
AL42
AM10
AM11
AM13
AM17
AM19
AM24
AM27
AM29
AM32
AM33
AM4
AN45
AP10
AP11
AP13
AP15
AP22
AP27
AP31
AP33
AP34
AP39
AR13
AR31
AR33
AR4
AT10
AT13
AT35
AT37
AT42
AU11
AU17
BD30
BD34
BD39
BD7
BE2
BF43
BF5
BG18
BG23
BG28
BG32
BG37
BG40
BG9
C1
A12
C2
B3
B30
B35
B4
B41
BA13
BA17
BA29
BA31
BA37
BA4
BA42
BB40
BC38
BC40
BC9
BD11
BD16
BD22
BD27
BD25
F2
E31
E6
E8
F39
F43
G4
G40
G42
F6
G9
H11
H13
H17
H19
H22
H24
H27
H29
H33
H35
H38
H4
H42
H9
J4
M36
M38
M4
M8
N13
N15
N19
N22
N24
N31
N42
P10
P22
P72
W29
K11
K13
K27
K3
K33
K35
K38
K45
K8
L13
L15
L35
L4
M11
VSS-001
VSS-002
VSS-003
VSS-004
VSS-005
VSS-006
VSS-007
VSS-008
VSS-009
VSS-010
VSS-011
VSS-012
VSS-013
VSS-014
VSS-015
VSS-016
VSS-017
VSS-018
VSS-019
VSS-020
VSS-021
VSS-022
VSS-023
VSS-024
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VSS-168
VSS-169
VSS-170
VSS-171
A2
B1
BD1
BE1
BF2
BF45
BF44
BG44
D45
A42
B45
B44
A44
V14
V10
U42
U4
T5
T42
Y8
Y4
Y38
Y33
Y32
Y30
Y14
Y13
W45
W3
W25
W23
W21
W20
W18
V8
V4
V34
V33
V32
V30
V18
V17
V16
T4
T38
T36
T32
T29
T22
T14
T10
R32
R31
P8
P42
P4
P35
P33
P31
P19
P17
P15
P13
D7
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B12
D16
D15
D12
D10
D1
C9
A6
C37
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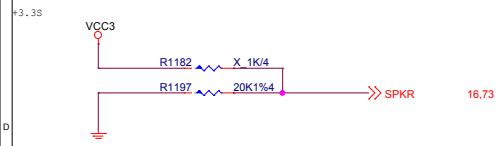
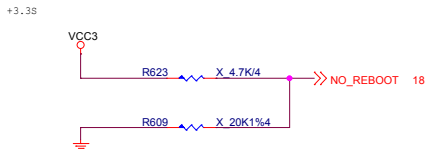
TOP SWAP OVERRIDE STRAP



HIGH: TOP_SWAP ENABLED
LOW : TOP_SWAP DISABLED

PCH HAS INTERNAL WEAK PD

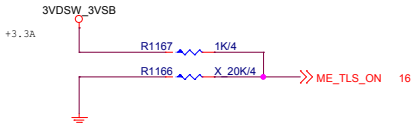
No Reboot OPTION



0 : NO-REBOOT (Default)
1 : REBOOT

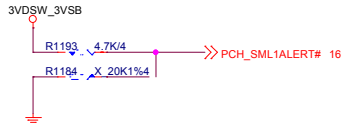
PCH HAS INTERNAL WEAK PD

AMT and SBA with confidentiality

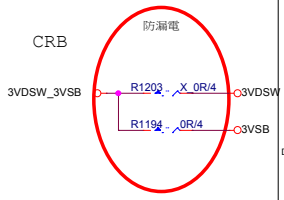


0 : DISABLE
1 : ENABLE (Default)

DCI ENABLE



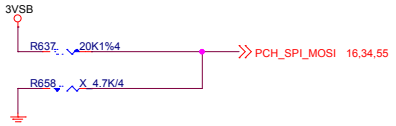
CRB



0 : DCI DISABLE
1 : DCI ENABLE (Default)

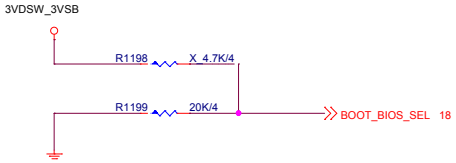
PCH HAS INTERNAL WEAK PD

Booot-HALT SEL STRAP



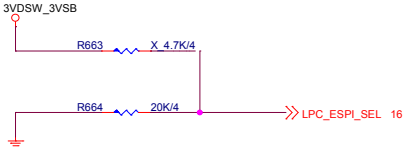
PCH HAS INTERNAL WEAK PU

Boot BIOS



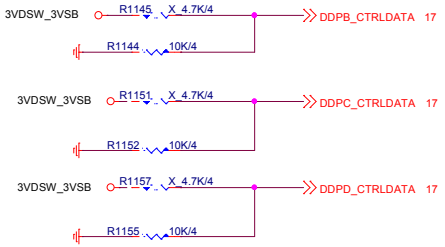
0 : SPI
1 : LPC

LPC eSPI Mode



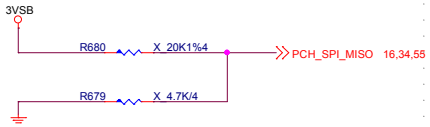
0 : LPC
1 : eSPI

DISPLAY PORT



0 : DISPLAY NOT DETECTED (Default)
1 : DISPLAY DETECTED

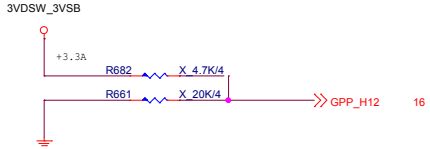
JTAG ODT SEL



HIGH: JTAG ODT ENABLED
LOW : JTAG ODT DISABLED

PCH HAS INTERNAL WEAK PU

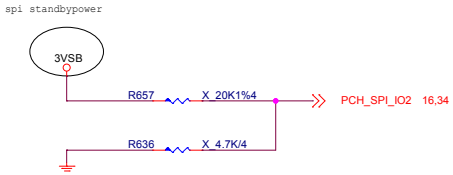
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

PCH HAS INTERNAL WEAK PD

CONSENT



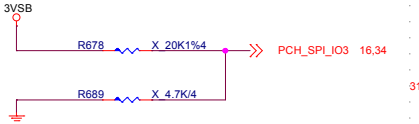
0 : CONSENT STRAP ENABLE
1 : CONSENT STRAP ENABLE

PCH HAS INTERNAL WEAK PU

DFX TEST MODE

UNSRTUFF: NORMAL
STUFF: TEST MODE

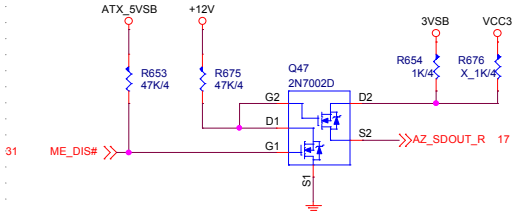
PERSONALITY



HIGH: PERSONALITY ENABLED
LOW : PERSONALITY DISABLED

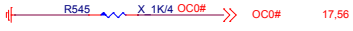
PCH HAS INTERNAL WEAK PU

HDA_SDO



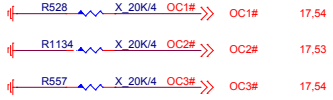
0 : SECURITY MEASURES OVERRIDEN
1 : SECURITY PER FLASH DESCRIPTOR

RING OSCILLATOR BYPASS (DFX)



0 : Ring Oscillator bypass
1 : Normal Mode

XTAL INPUT FREQUENCY [HVM MODE]



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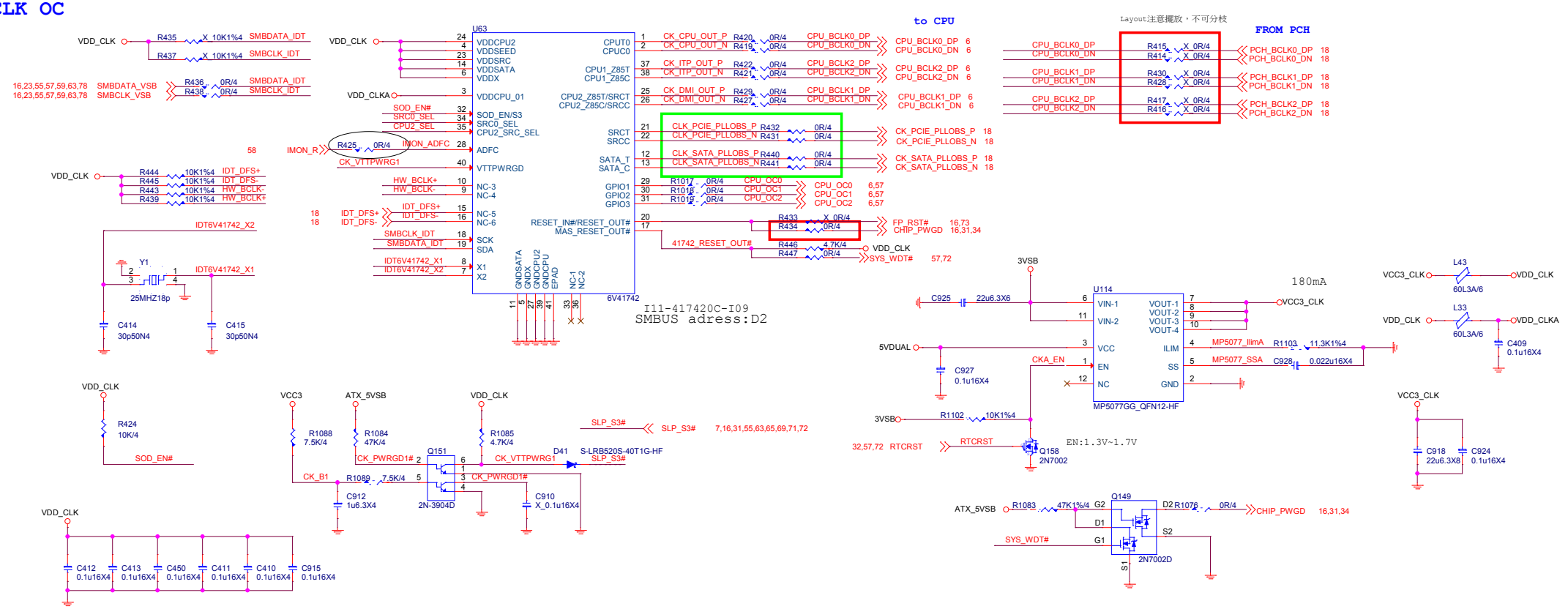
BCLK OC



SRC0_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

CPU2_SRC_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

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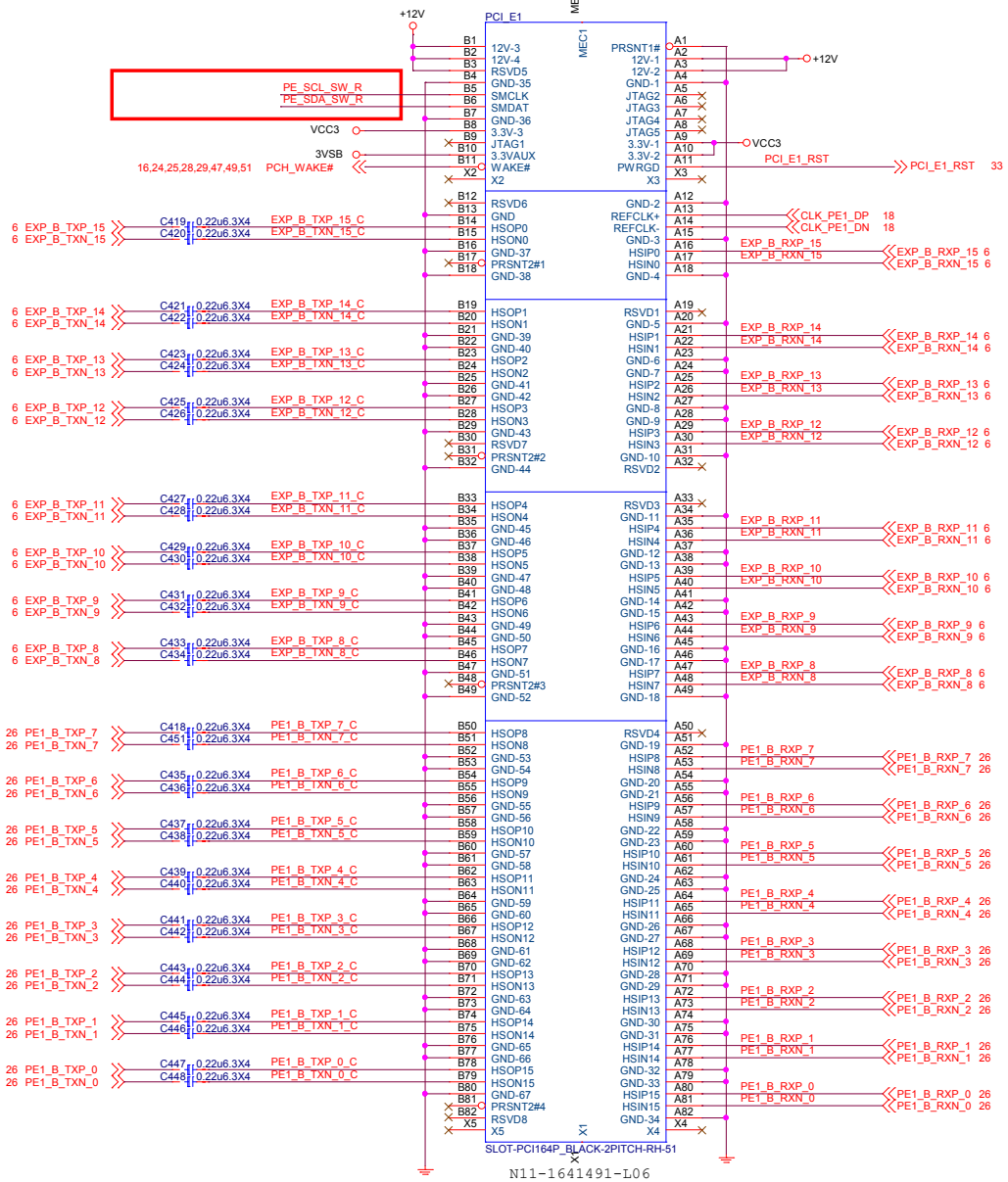
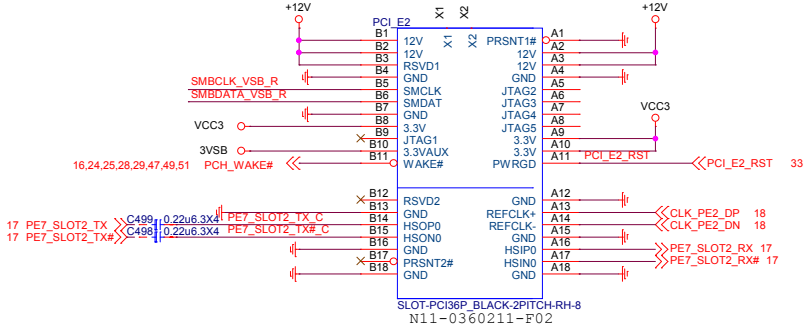
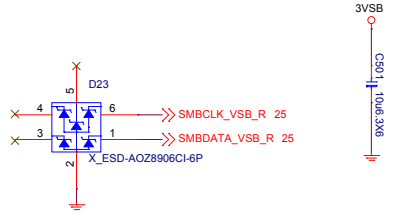
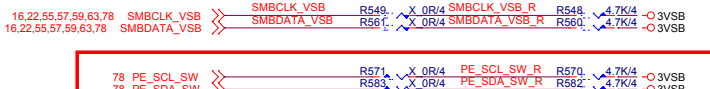
PCIE1(X16) & PCIE2(X1) Slots

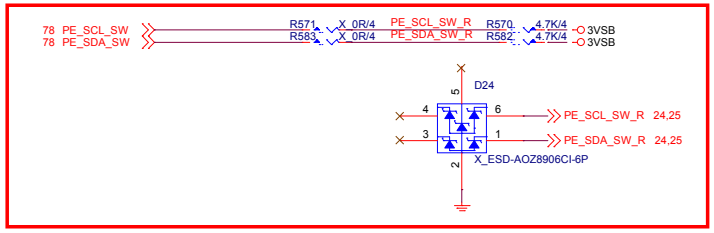


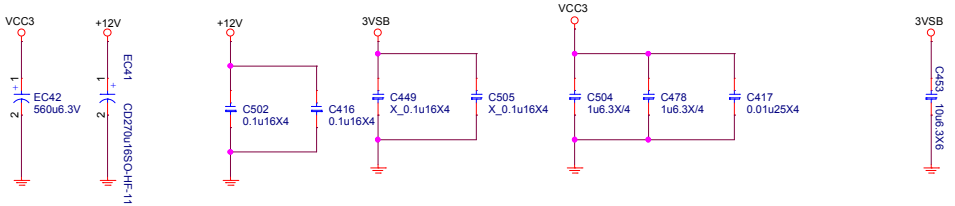


SMBUS ESD









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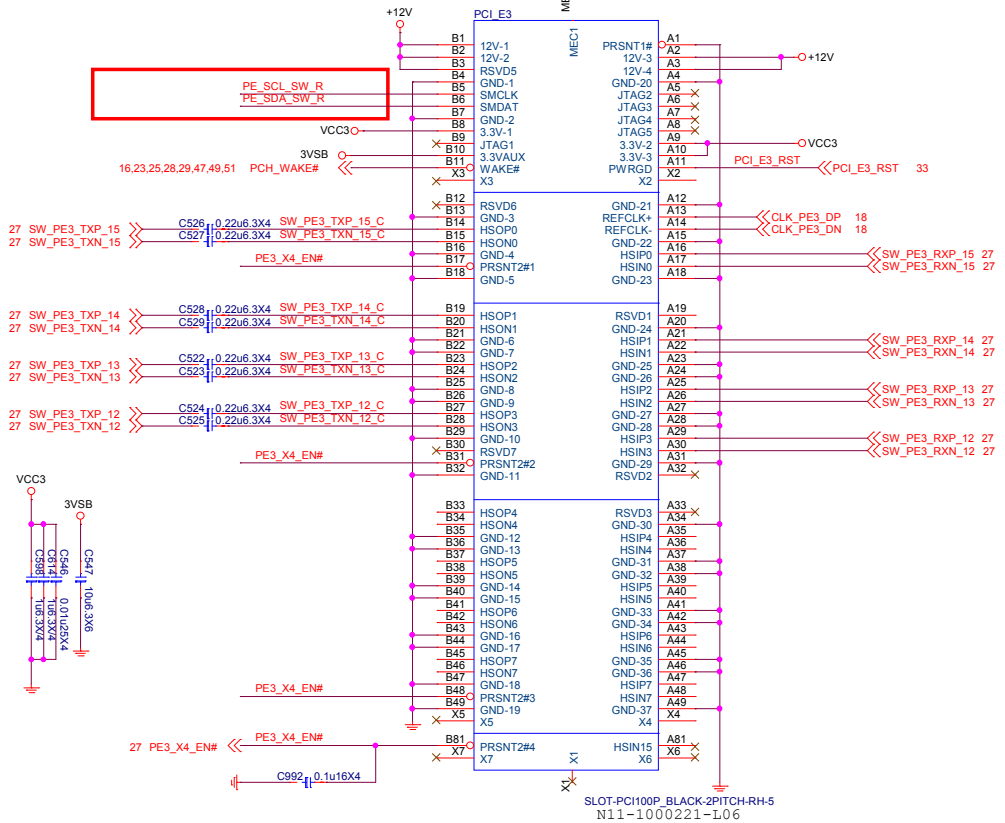

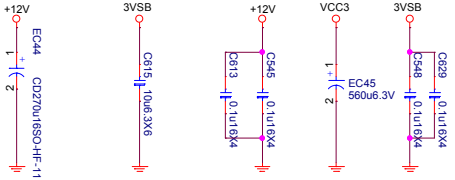

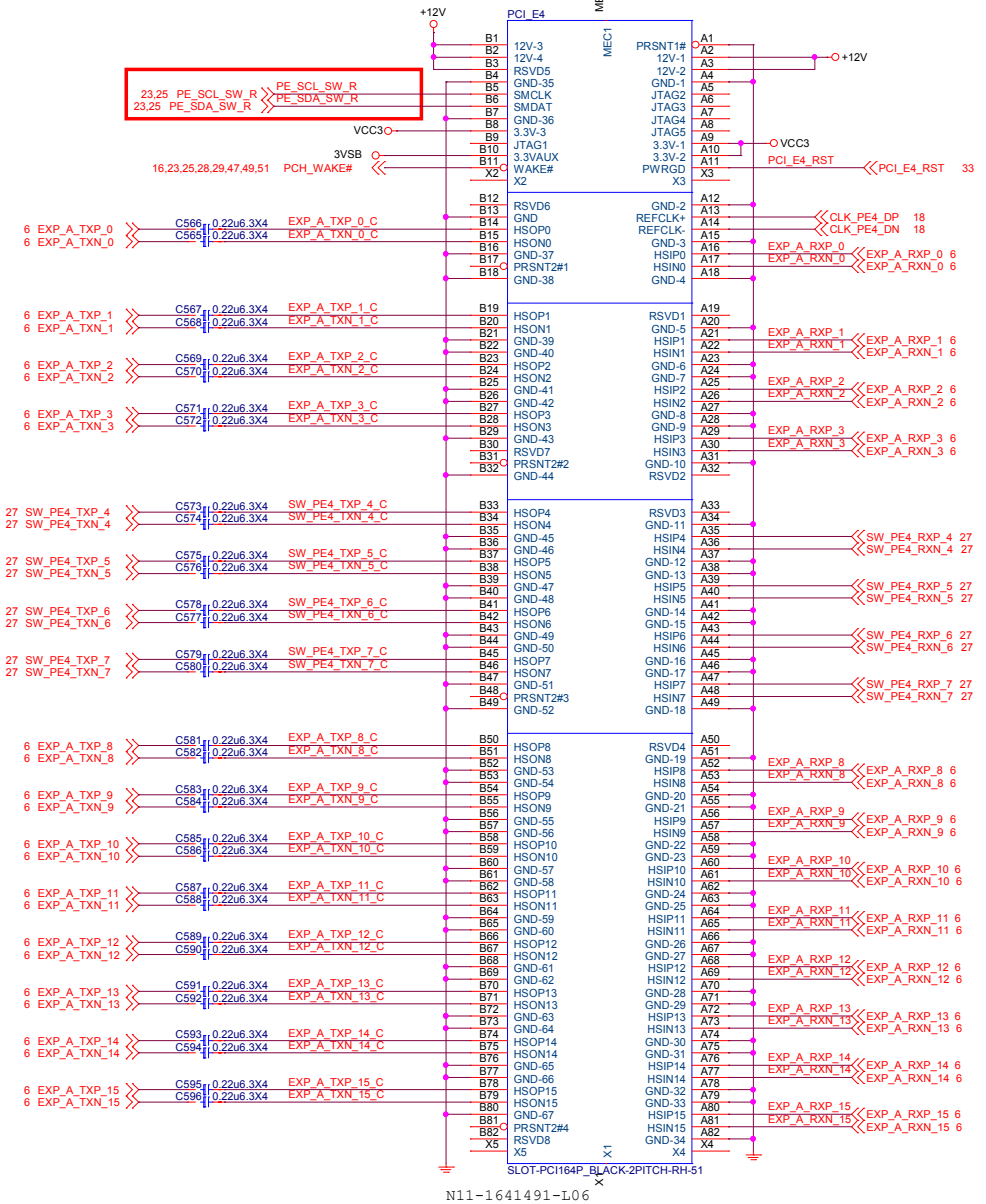

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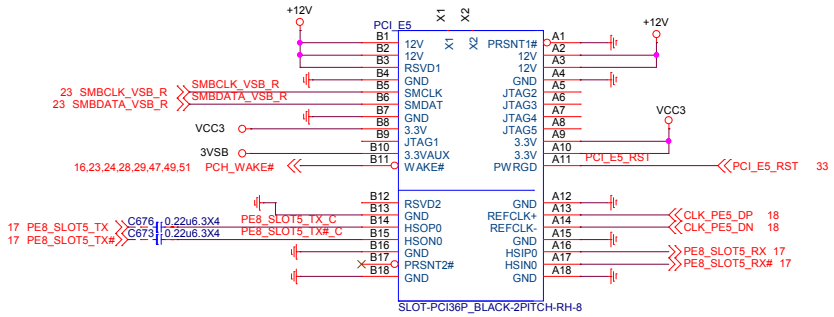
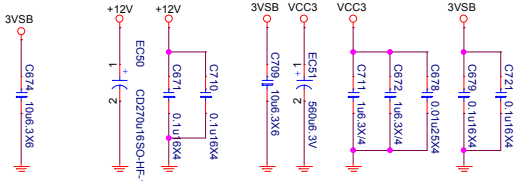
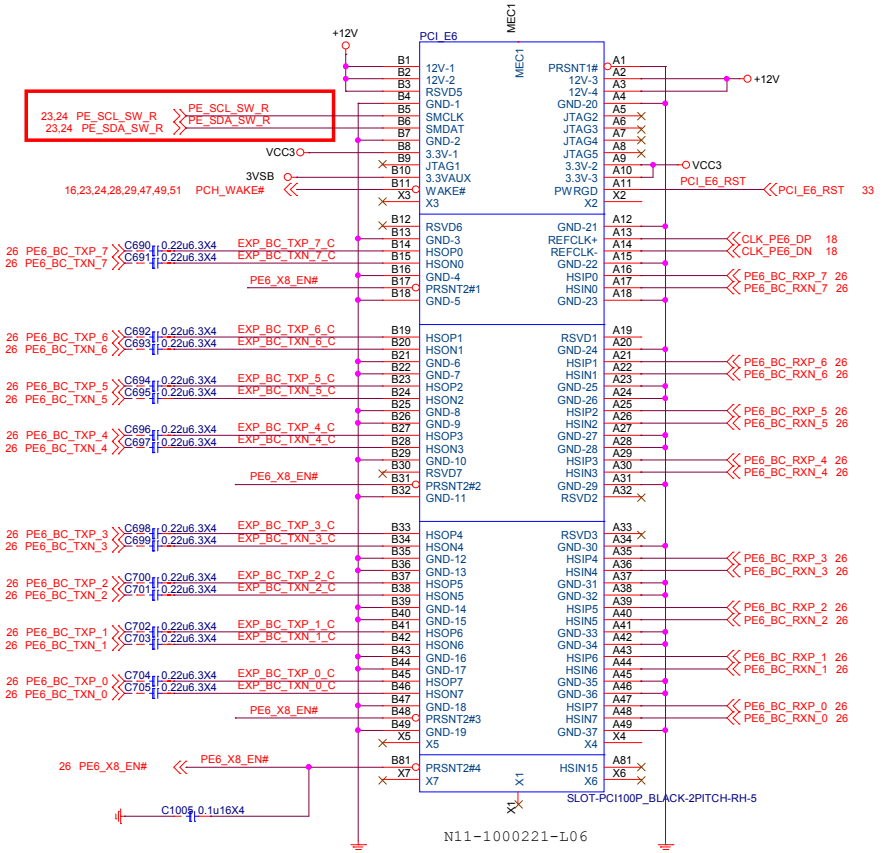


N11-0360211-F02





N11-1000221-L06

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Size: Custom	Document Description: M.2-SLOT1
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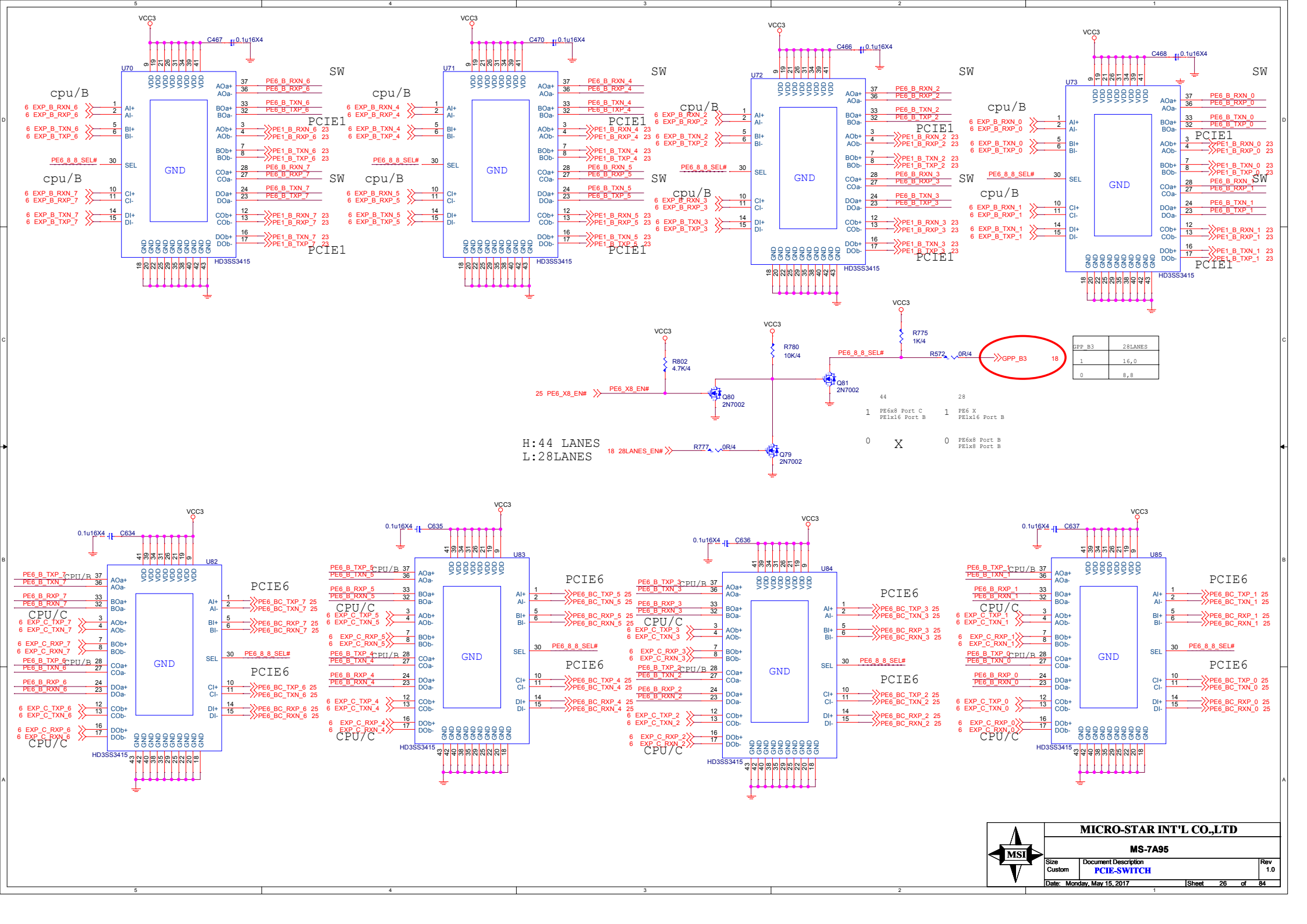
U70
U71
U72
U73
U82
U83
U84
U85
HD3SS3415
PCIE1
PCIE6
cpu/B
CPU/C
SW
GND
VCC3
C467 0.1u16X4
C470 0.1u16X4
C466 0.1u16X4
C468 0.1u16X4
C634 0.1u16X4
C635 0.1u16X4
C636 0.1u16X4
C637 0.1u16X4
PE6_8_8_SEL#
PE6_X8_EN#
28LANES_EN#
R802 4.7K/4
R780 10K/4
R775 1K/4
R572 0R/4
R777 0R/4
Q80 2N7002
Q81 2N7002
Q79 2N7002
GPP_B3
H:44 LANES
L:28LANES
GPP_B3 | 28LANES
1 | 16,0
0 | 8,8
1 PE6x8 Port C PE1x16 Port B
1 PE6 X PE1x16 Port B
0 X
0 PE6x8 Port B PE1x8 Port B
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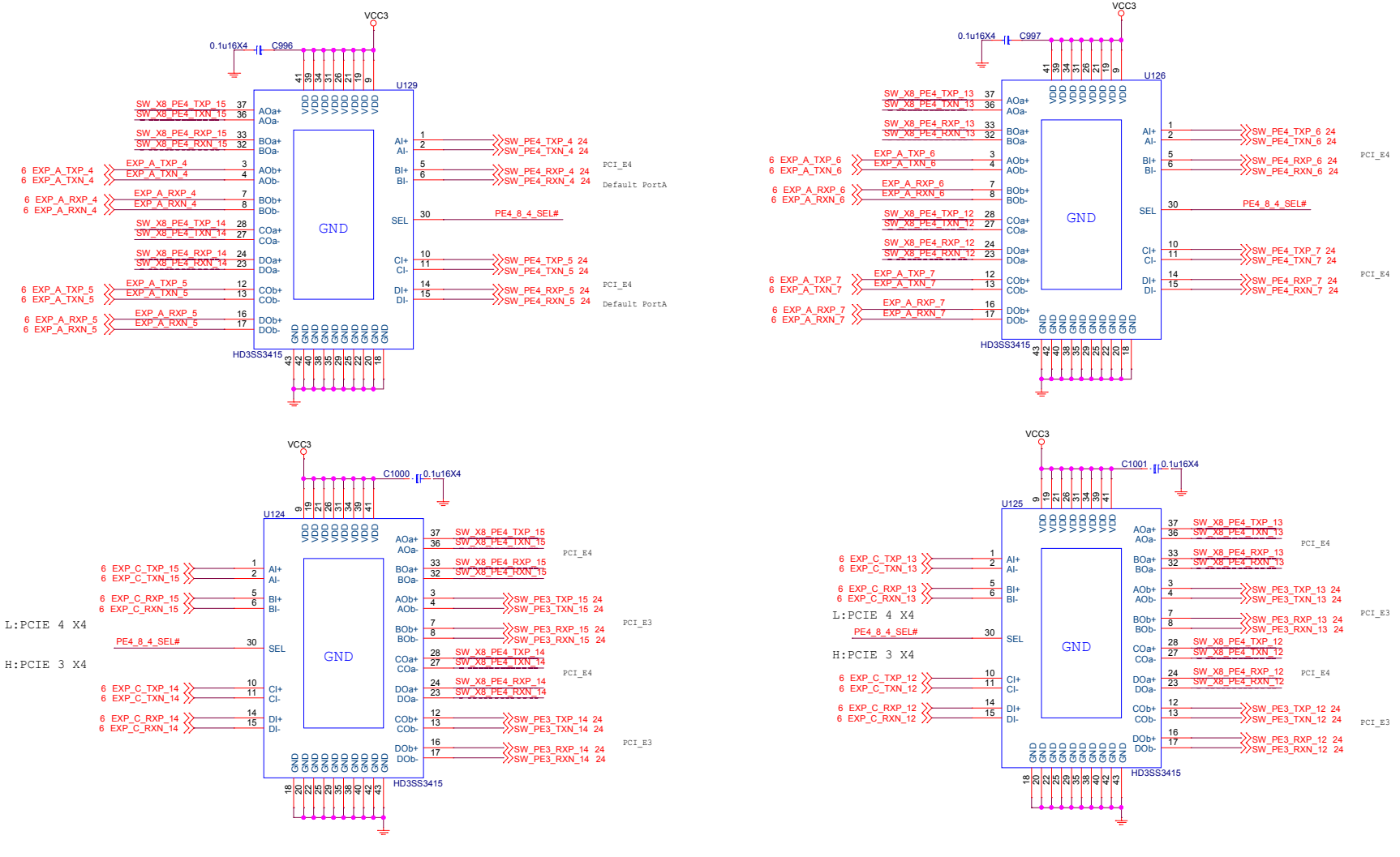

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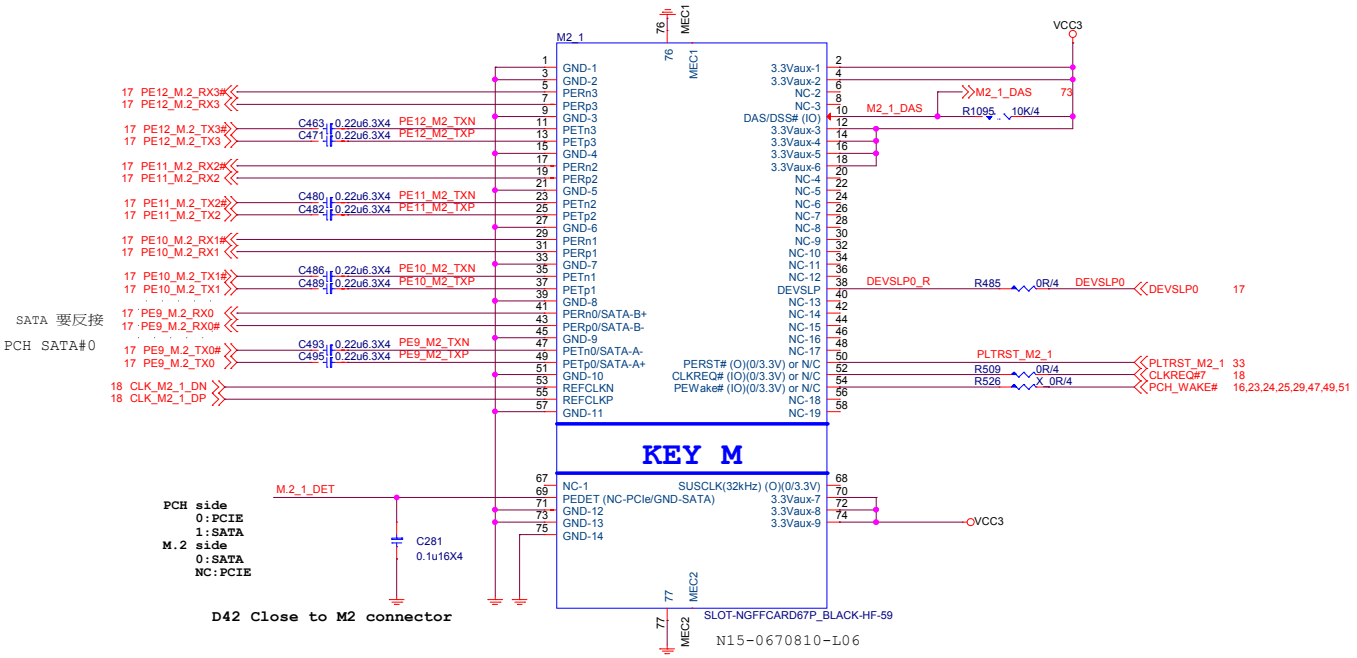
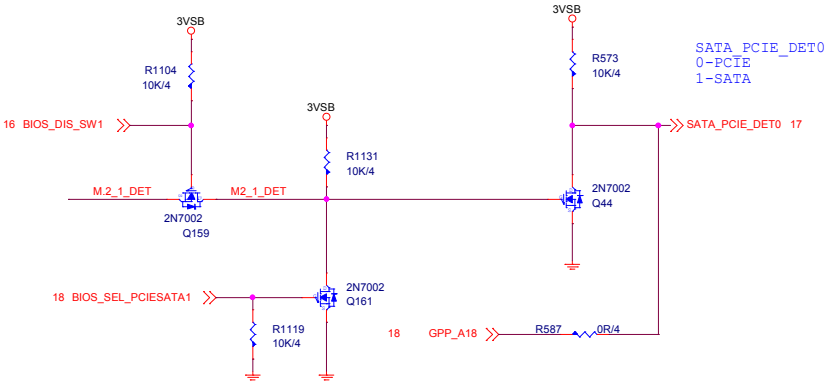
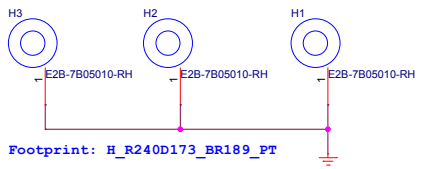
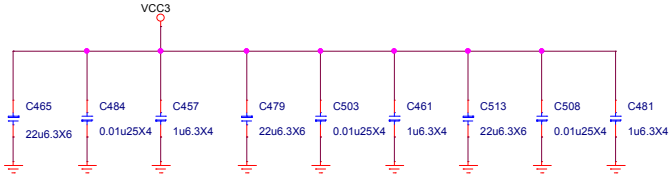




BIOS_MODE

BIOS_DIS_SW1	*BIOS_SEL_PCIESATA1*	*Mode*
0	*1*	***M2-SATA***
0	*0*	***M2-PCIE***
GPI(1)	*0*	*AUTO*





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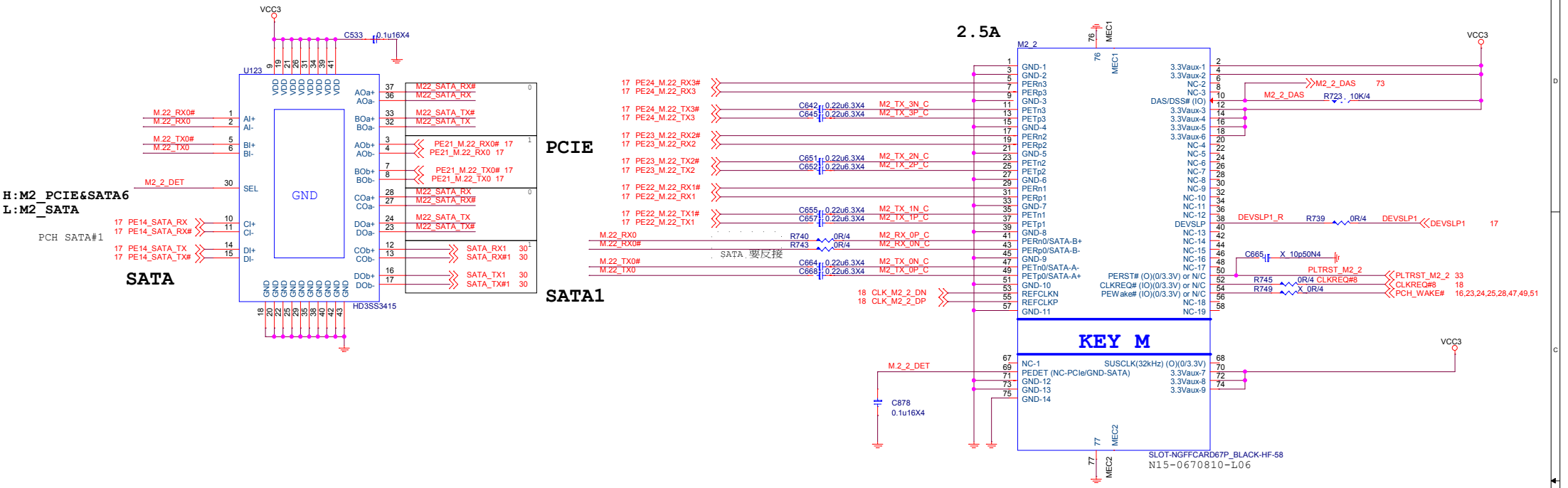
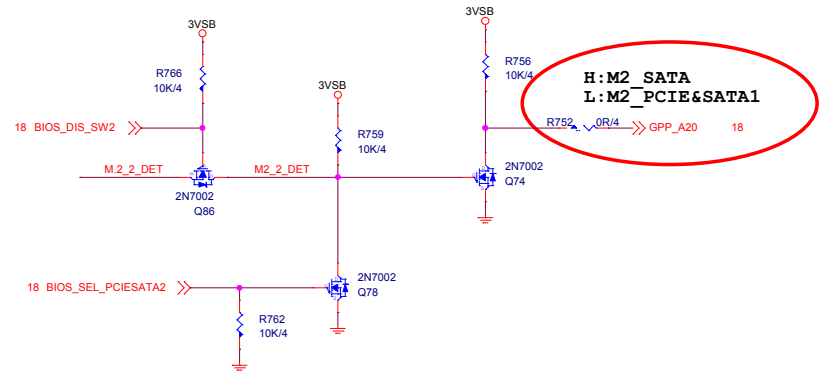
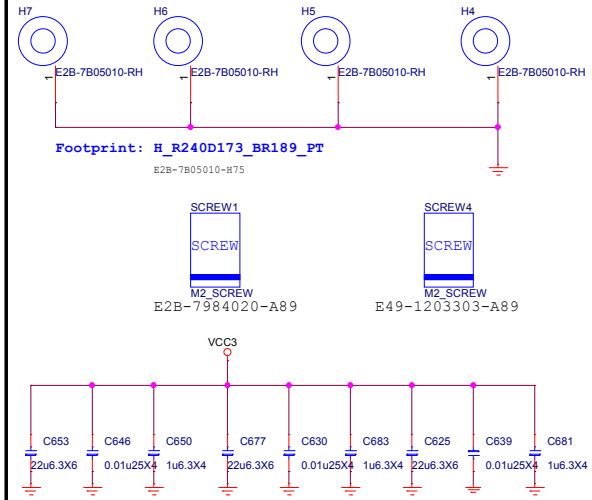




BIOS_MODE

BIOS_DIS_SW2	*BIOS_SEL_PCIESATA2*	*Mode*
0	*1*	*M2-SATA*
0	*0*	*M2-PCIE*
GPI(1)	*GPI(1)*	*AUTO*



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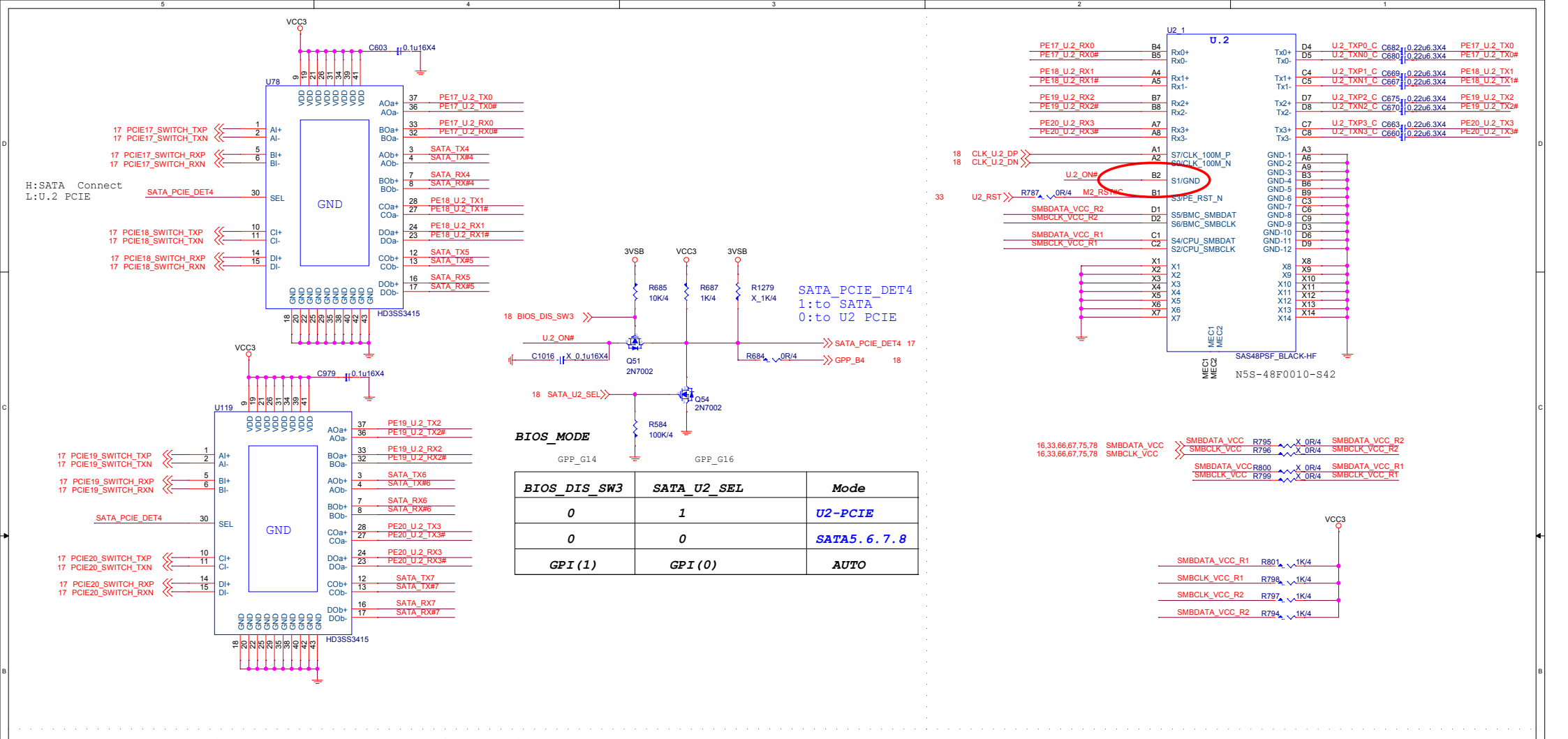
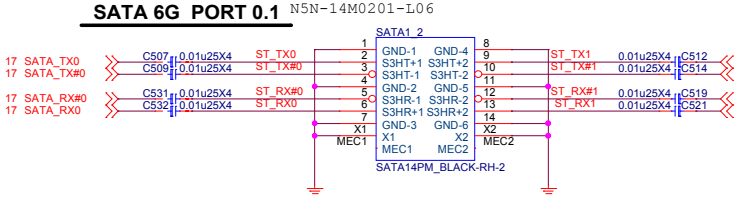


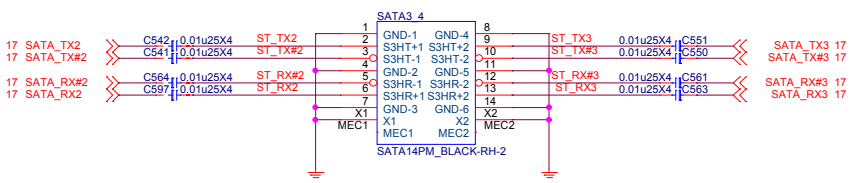
BIOS_DIS_SW3	SATA_U2_SEL	Mode
0	1	U2-PCIE
0	0	SATA5.6.7.8
GPI(1)	GPI(0)	AUTO

if M2_1&M2_2 use ,SATA1_2 connect is no function.

SATA 6G PORT 0.1 N5N-14M0201-L06

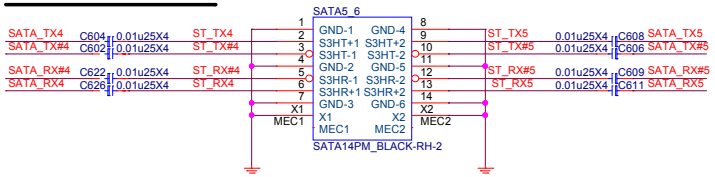


SATA 6G PORT 2.3 N5N-14M0201-L06

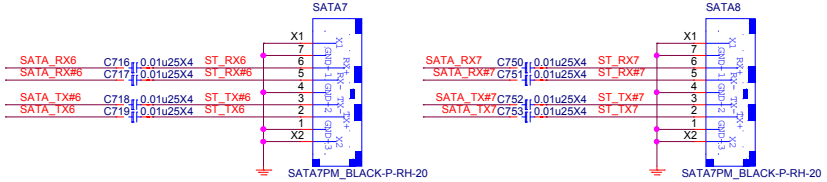


if U_2 use ,SATA5_6、SATA7、SATA8 connect is no function.

SATA 6G PORT 4.5 N5N-14M0201-L06



SATA 6G PORT 6.7 N5N-07M2441-H06



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Size: Custom	Document Description: U2/SATA-Conn
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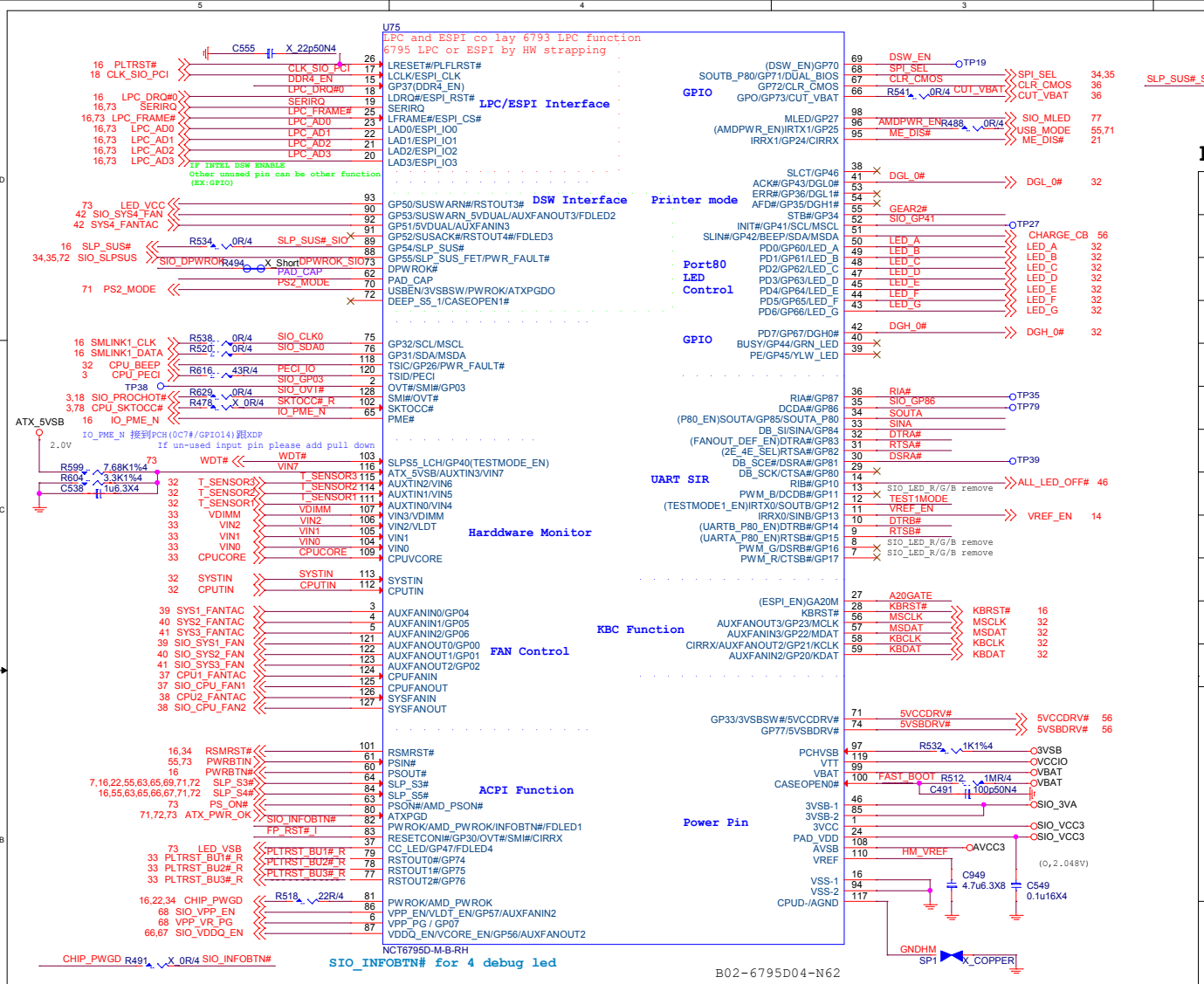
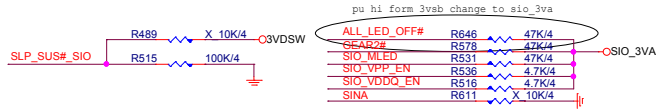
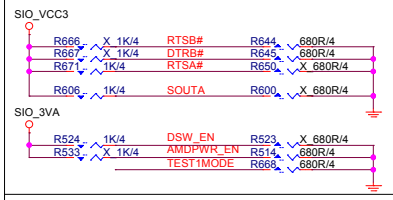


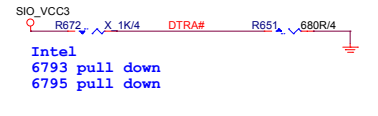


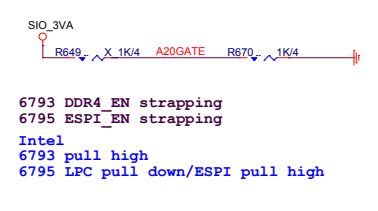
POWER ON STRAPPING PIN FOR NCT6793/6795

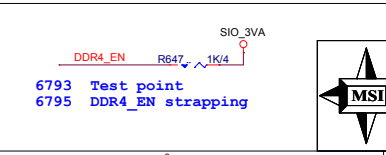
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

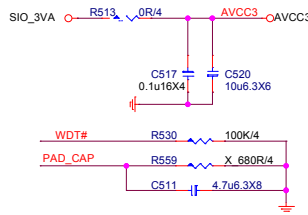


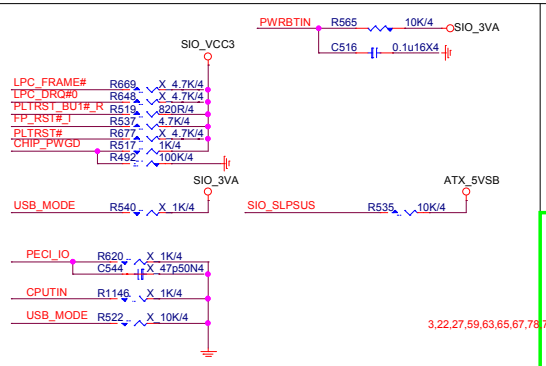


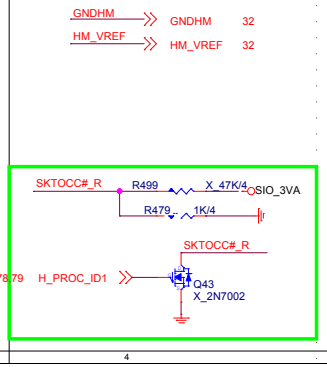


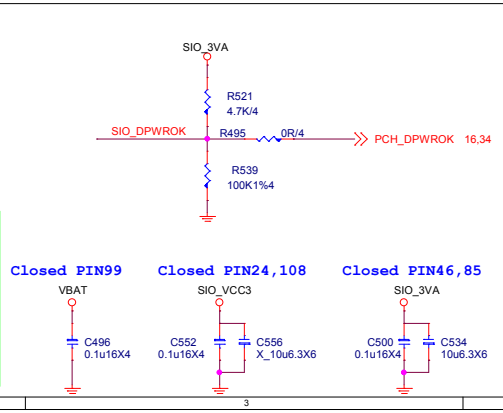


3V Analog Power









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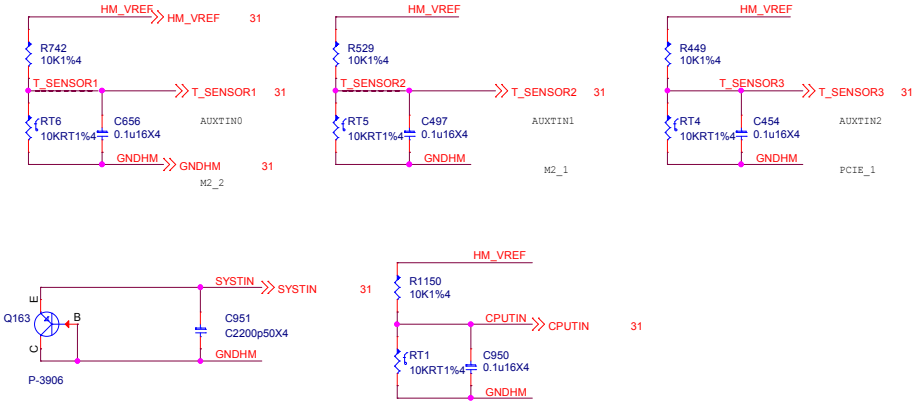
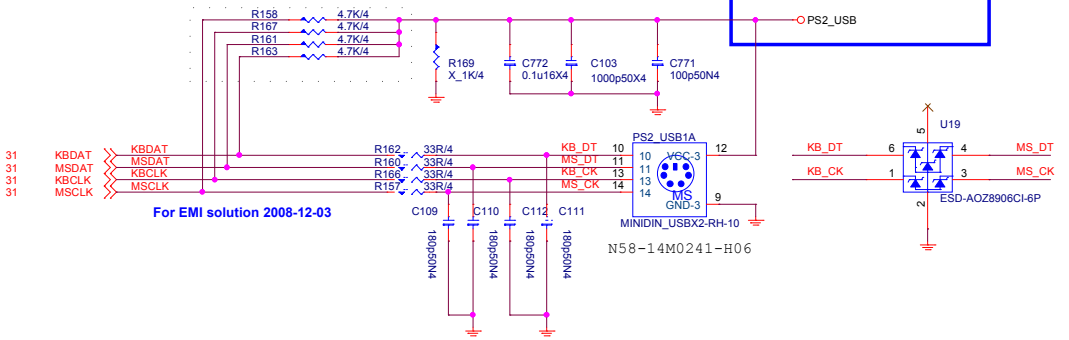
THERMAL



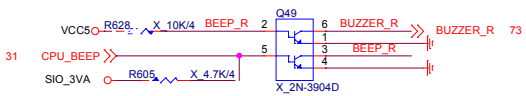
PS2 KEYBOARD & MOUSE CONNECTOR

0.5A

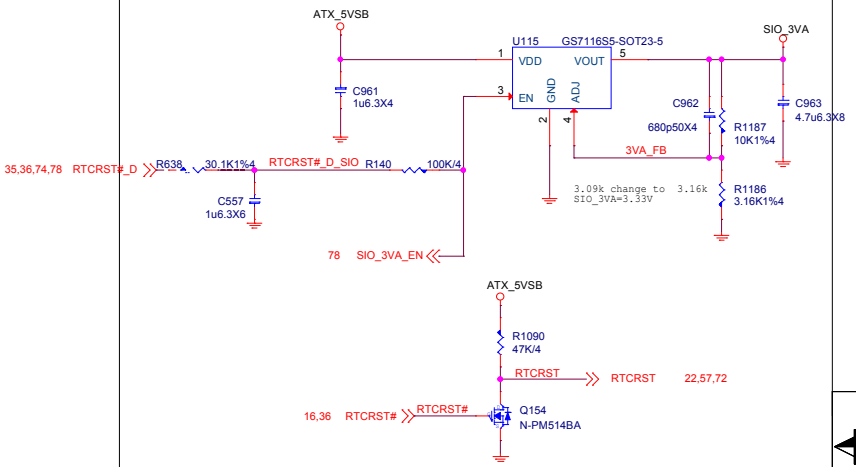
可以切換在s5
底下是不是要有電



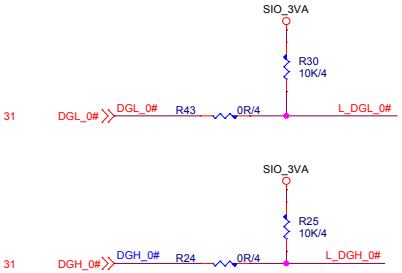
COM Port for BIOS Debug



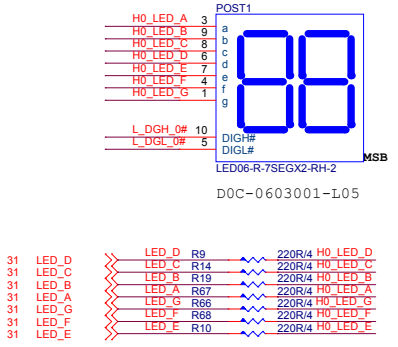
SLP_SUS Co-lay circuit



DEBUG LED



Debug LED OFF BIOS control



MICRO-STAR INT'L CO.,LTD

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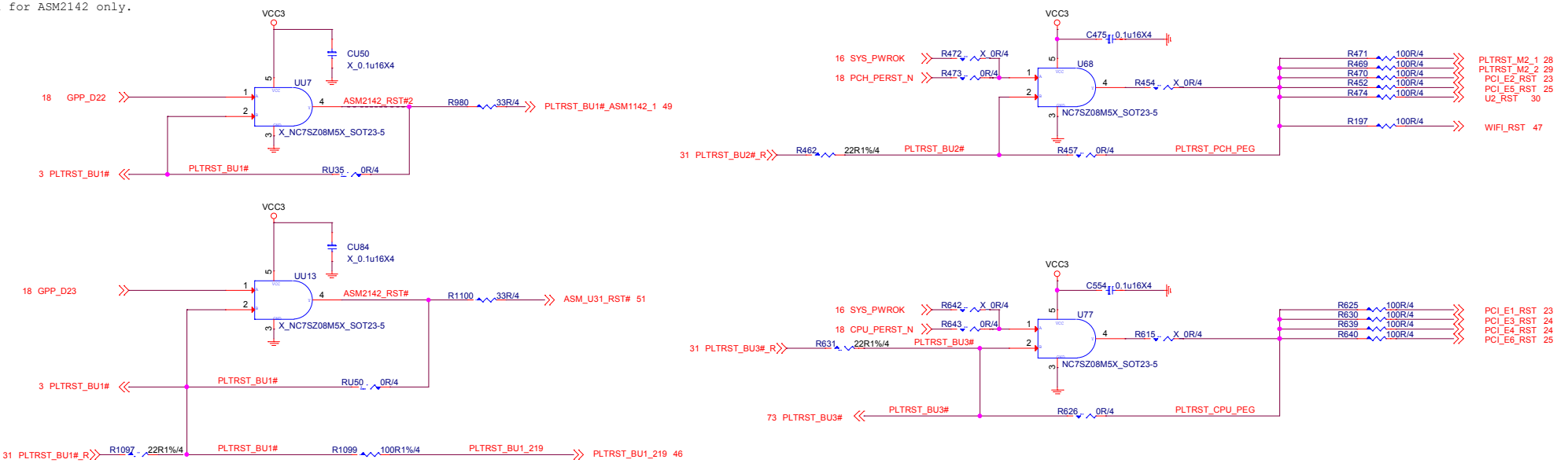
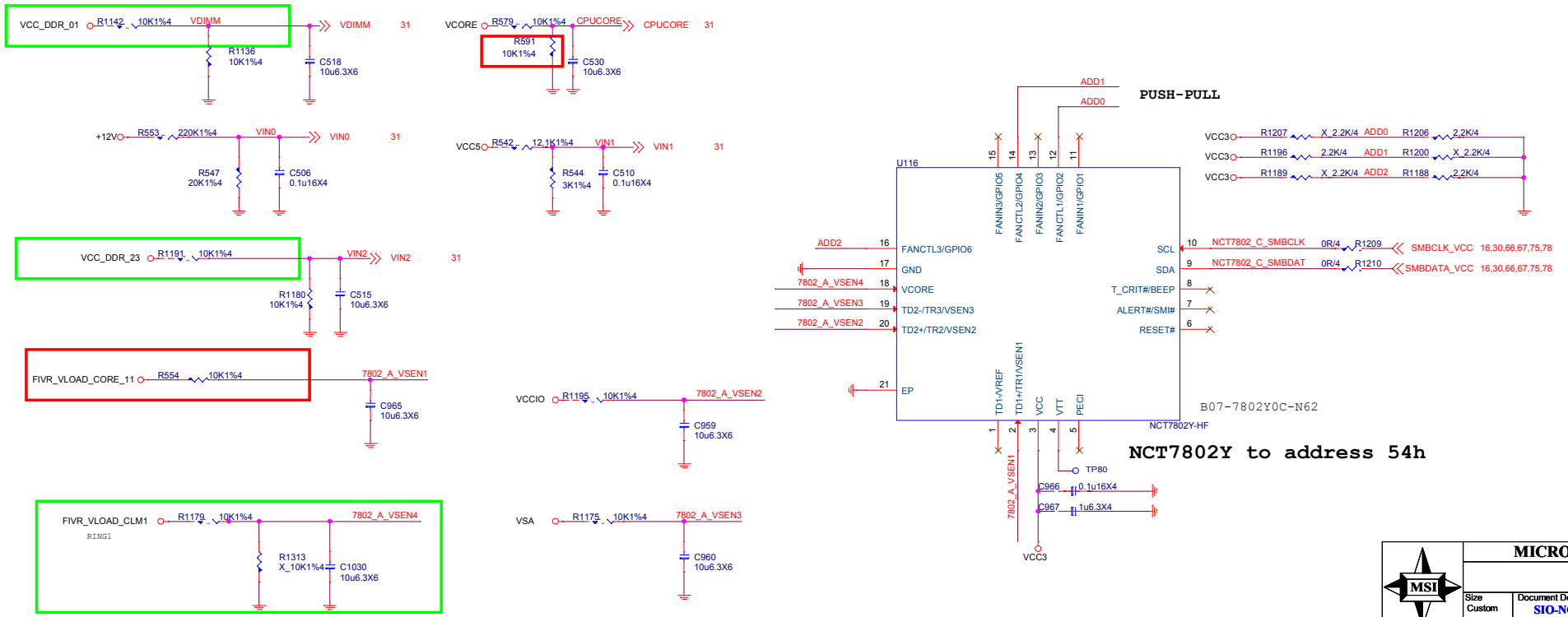
Reset control for ASM2142 only.



HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



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Size: Custom	Document Description: SIO-NCT6793D-3	Rev: 1.0
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16,55 PCH_SPI_CS0# PCH_SPI_CS0#
16,21,55 PCH_SPI_MOSI PCH_SPI_MOSI
16,21,55 PCH_SPI_MISO PCH_SPI_MISO
16,55 PCH_SPI_CLK PCH_SPI_CLK
16,21 PCH_SPI_IO2 PCH_SPI_IO2
16,21 PCH_SPI_IO3 PCH_SPI_IO3

Part Number:N31-2061341-H06

SPI CS# < 25pF
D0G-0402510-SI0

close to JSPI1 for ESD use

SPI_VCC3 R779 0R/6 3VSB

SPI DEBUG PROT
Close to SPI ROM

SPI_VCC3 SPI_VCC3 SPI_VCC3 C687 0.1u16X4

JSPI1
PCH_SPI_MISO PCH_SPI_MOSI
PCH_SPI_CS# PCH_SPI_CLK
SPI_SW_SEL
PCH_SPI_IO2 PCH_SPI_IO3
H2X6[10]M-2PITCH_BLACK

PCH_SPI_CS0# R772 0R/4
D26 ESD-AOZ8131D1
C1027 0.1u16X4

HW MODE

A BIOS
MEC1
BIOS_SW1
SW-DIP_BLACK-RH
N73-0100471-D02
A
B
C
SPI_SEL_R
SPI2_SW
C1028 0.1u16X4
R811 1K/4
R821 4.7K/4
SPI_SEL
SPI_VCC3
MEC2
B BIOS

Skylake use SPI_VCC3
Skylake use SPI_VCC3

SPI_VCC3 C714 0.1u16X4

SIO NCT6793 GP71

31,35 SPI_SEL
GPI default low
Active push pull high switch to SPI2
For auto testing in factory.

R812 100K1%4

U92
PCH_SPI_CS# SPI_SEL
D S2 VCC GND IN S1
SPI_CS1# SPI_CS2#
NC7SB3157P6X_SOT323-6

IN=0 , D connected to S2 (SPI1- A Bios)
IN=1 , D connected to S1 (SPI2- B Bios)

ATX_5VSB R786 10K/4 SPI_SW_SEL SPI_SW_SEL 55,78

16,31 PCH_DPWROK D32 S-LRB520S-40T1G-HF
16,31 RSMRST# D31 S-LRB520S-40T1G-HF
16,22,31 CHIP_PWGD D33 X_S-LRB520S-40T1G-HF
31,35,72 SIO_SLPSUS D30 S-LRB520S-40T1G-HF

SPI_VCC3
R770 X_1K/4 PCH_SPI_MOSI
R771 X_1K/4 PCH_SPI_MISO

SPI FLASH ROM

Place close to SB.

M31-2512853-W03
AVL:M31-2512832-M24

16M ROM For X299

A BIOS

SPI_VCC3 R747 2.2K/4
SPI_CS1#
PCH_SPI_MISO R750 33R/4 SPI1_MISO
PCH_SPI_IO2 R754 33R/4 SPI1_IO2
A_SPI1
CS SO(SIO1) WP(SIO2) GND VCC RESET(SIO3) SCLK SI(SIO0) EPAD
MX25L256-W25Q256
SPI_VCC3 C661 0.1u16X4 C666 10u6.3X6
SPI1_IO3 SPI1_CLK SPI1_MOSI
R748 33R/4 PCH_SPI_IO3
R755 33R/4 PCH_SPI_CLK
R761 33R/4 PCH_SPI_MOSI

B BIOS

SPI_VCC3 R744 2.2K/4
SPI_CS2#
PCH_SPI_MISO R751 33R/4 SPI2_MISO
PCH_SPI_IO2 R758 33R/4 SPI2_IO2
B_SPI1
CS SO(SIO1) WP(SIO2) GND VCC RESET(SIO3) SCLK SI(SIO0) EPAD
MX25L256-W25Q256
SPI_VCC3 C659 0.1u16X4 C662 10u6.3X6
SPI2_IO3 SPI2_CLK SPI2_MOSI
R746 33R/4 PCH_SPI_IO3
R753 33R/4 PCH_SPI_CLK
R763 33R/4 PCH_SPI_MOSI

*SPI_CLK & SPI_MOSI must be length matched to within 500mils. < 6 inch
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.

VCC5 R773 4.7K/4 A_BIOS1 LED04-R-20mA2.4V_1608-HF
VCC5 R767 1K/4 B_BIOS1 LED04-W-20mA3.9V

ATX_5VSB R805 47K/4 Q84 2N7002
SPI_SEL
Q76 2N7002D
SPI_SEL G2 D2
D1 S2
SPI1_SW G1 S1

ATX_5VSB C688 X_1u6.3X4 R778 X_47K/4
U90 X_GS7116S5-SOT23-5
VDD VOUT EN GND ADJ
SPI_VCC3 C712 X_680p50X4 R803 X_10K1%4
SPI_FB
C689 X_22u6.3X8
SIO_SLPSUS Q77 X_2N7002
R793 X_3.09K1%4

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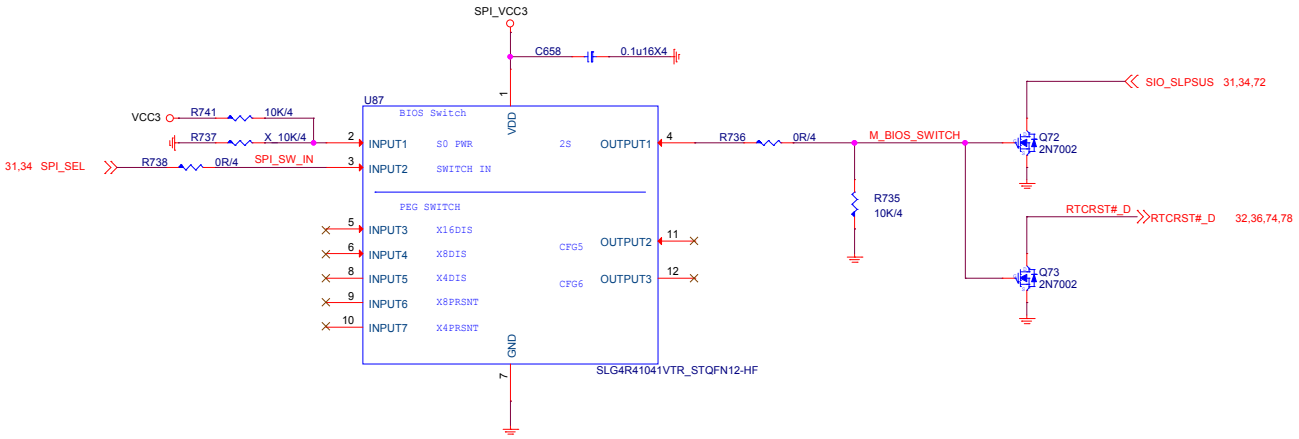
Skylake/Kabylake Path Circuit For Dual Bios



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Size: Custom	Document Description: Dual bios control-Silego	Rev: 1.0
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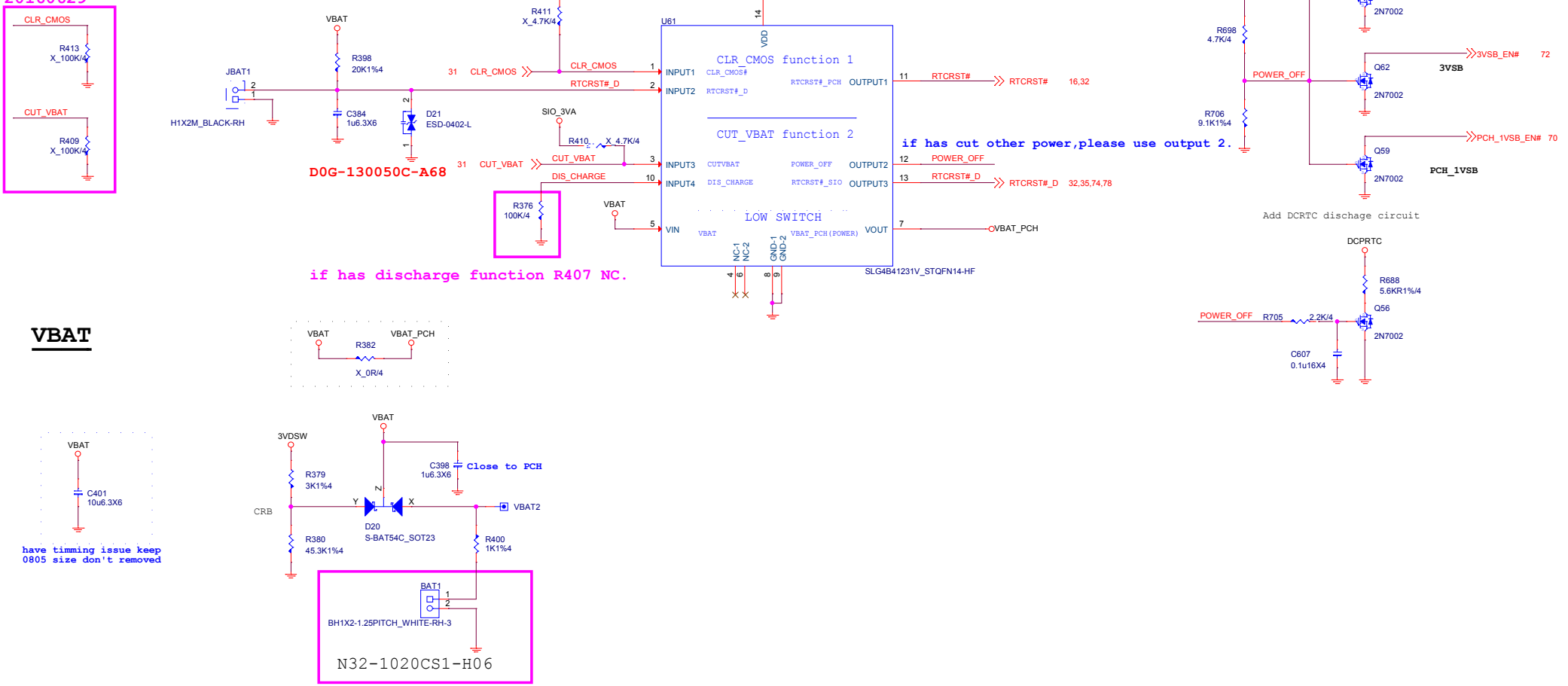
CUT VBAT

20160629



VBAT

have timming issue keep 0805 size don't removed

MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size: Custom	Document Description: CLR COMS/CUT VBAT	Rev: 1.0
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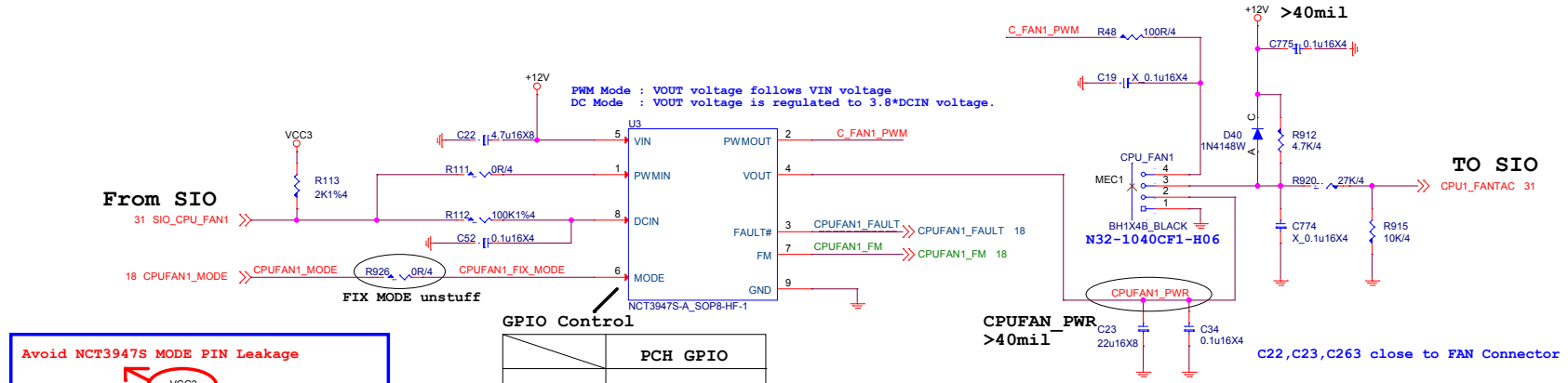
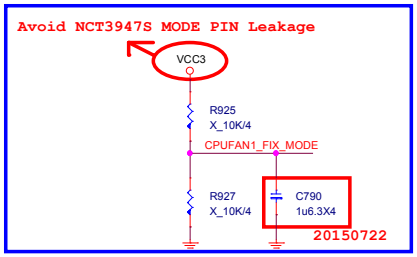
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



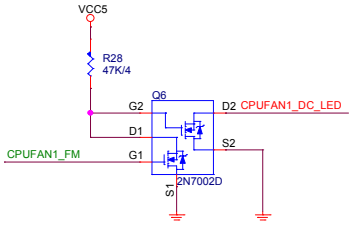
GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

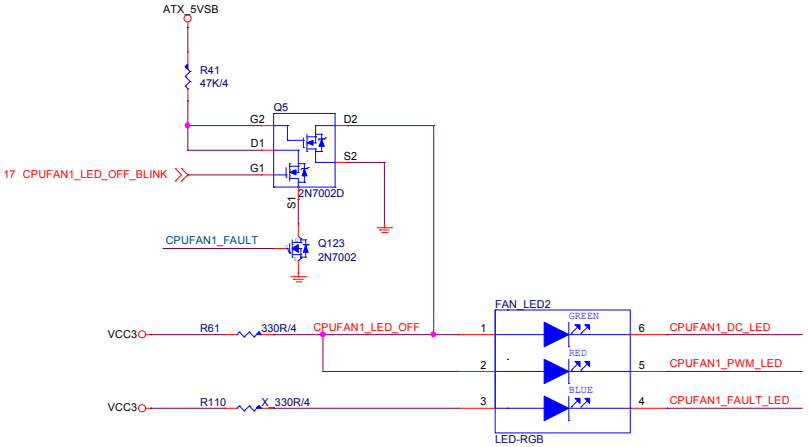
Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC



CHECK NCT3947S Sink Current

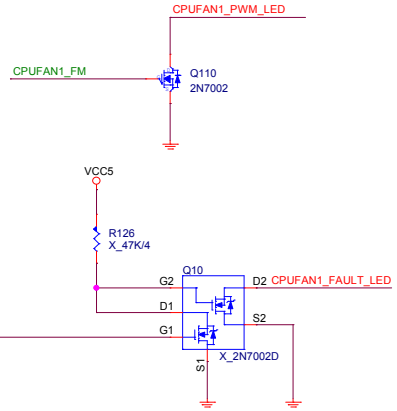


Forward Current 20mA
Pulse Forward Current 40-60mA

RGB

D0C-040S400-H91

DC_FAN_LED(綠)
PWM_FAN_LED(藍)
FAN_OCP_LED(紅)



MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: CPU FAN1
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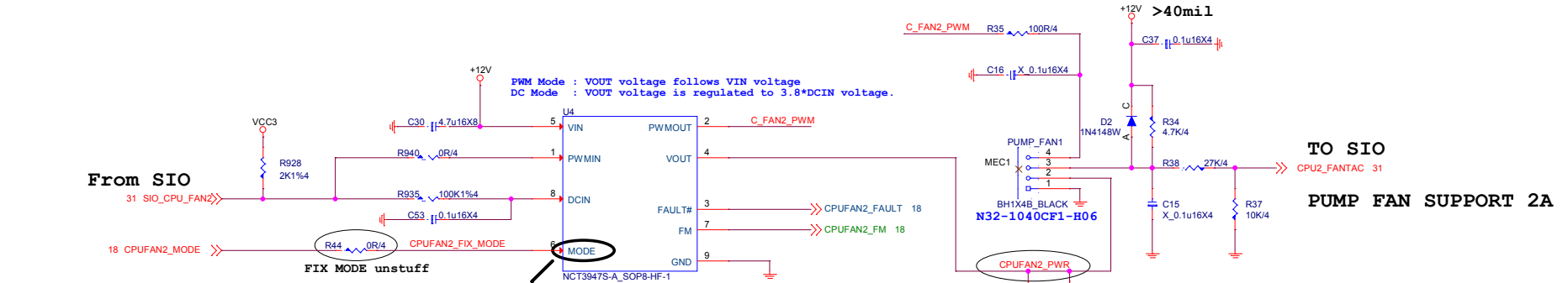
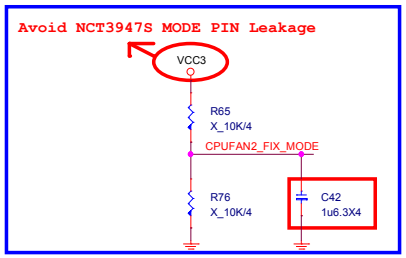
TYPE J : 4 PIN PUMP FAN USE NCT3947S USE PCH GPIO



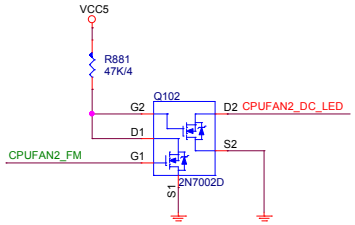
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

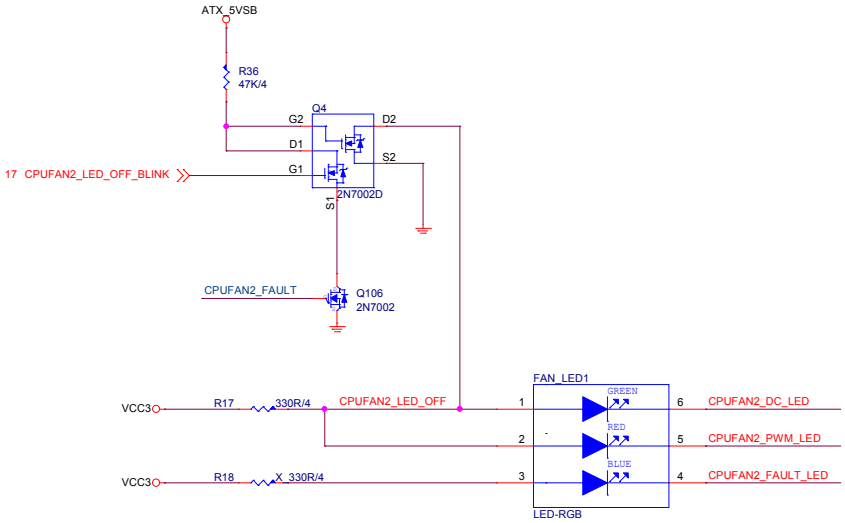
Internall pull up 1.65V



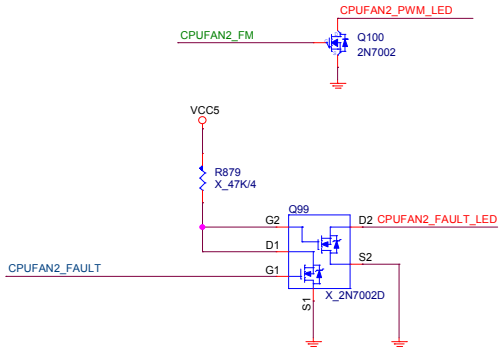
Resever For FIX DC or PWM MODE USE By PM SPEC



CHECK NCT3947S Sink Current



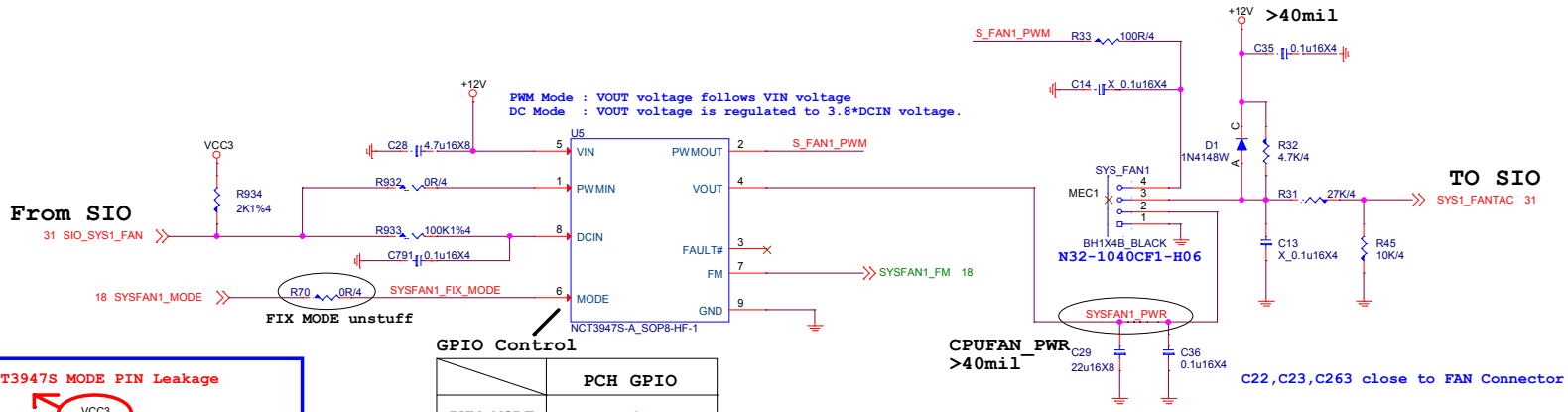
D0C-040S400-H91



CHECK NCT3947S Sink Current

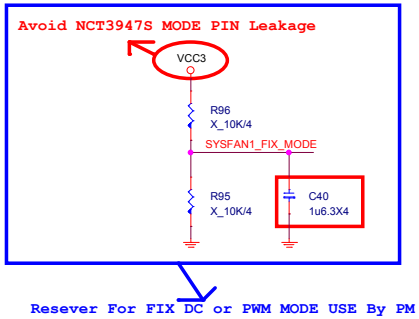
MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size: Custom	Document Description: CPU FAN2	Rev: 1.0
Date: Monday, May 15, 2017	Sheet 38 of 84	

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

MICRO-STAR INT'L CO.,LTD

MS-7A95

Size: Custom | Document Description: SYSTEM FAN1 | Rev: 1.0

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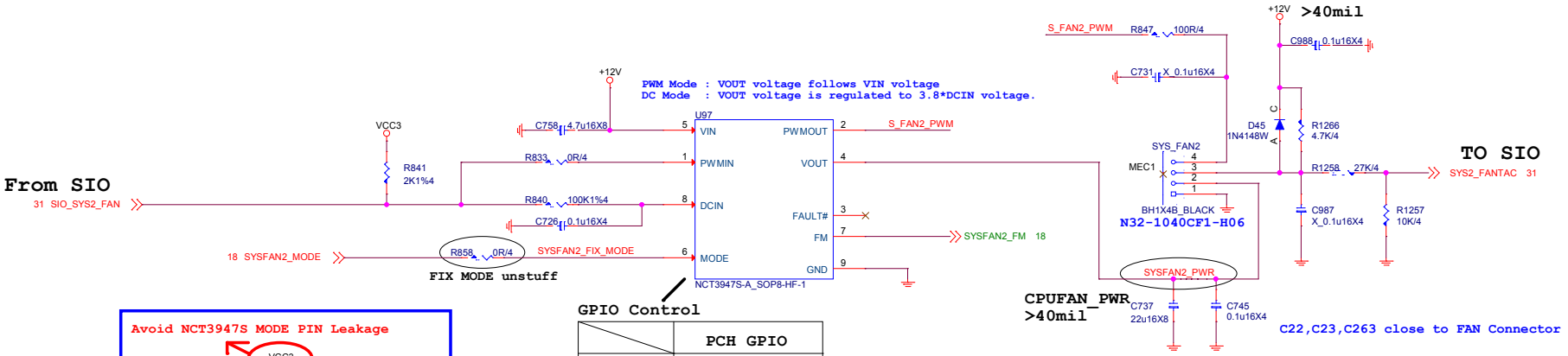
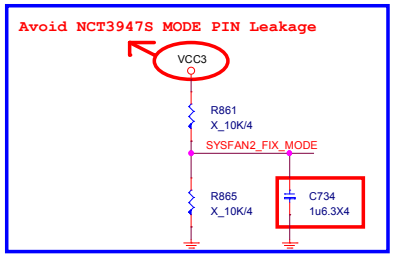
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

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MS-7A95	
Size: Custom	Document Description: SYSTEM FAN2
Rev: 1.0	
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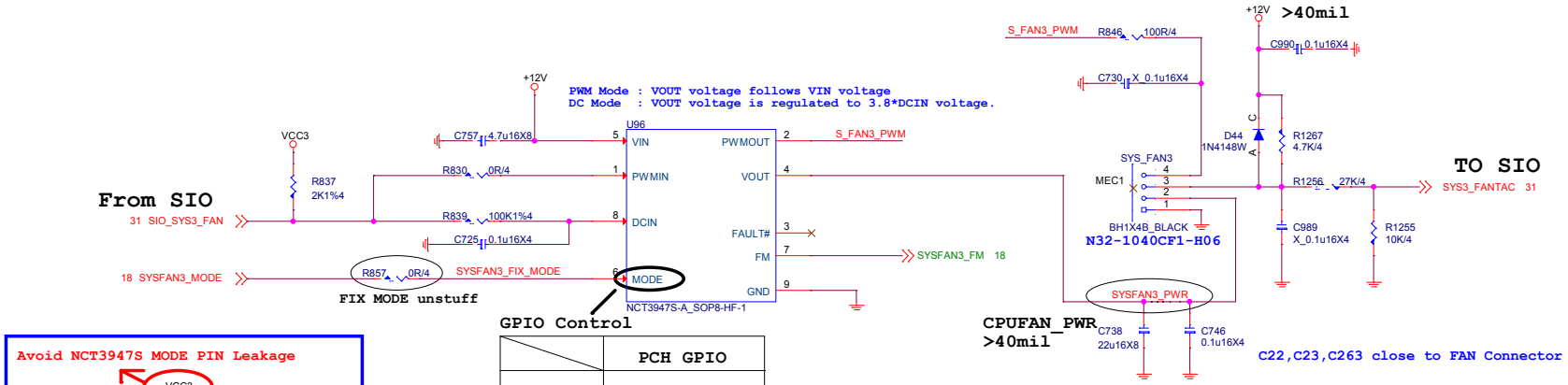
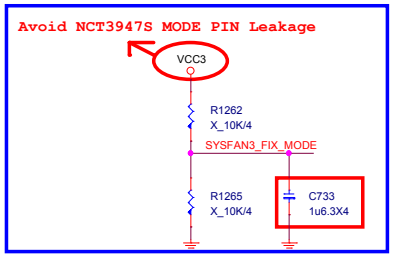
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

MICRO-STAR INT'L CO.,LTD

MS-7A95

Size: Custom | Document Description: SYSTEM FAN3 | Rev: 1.0

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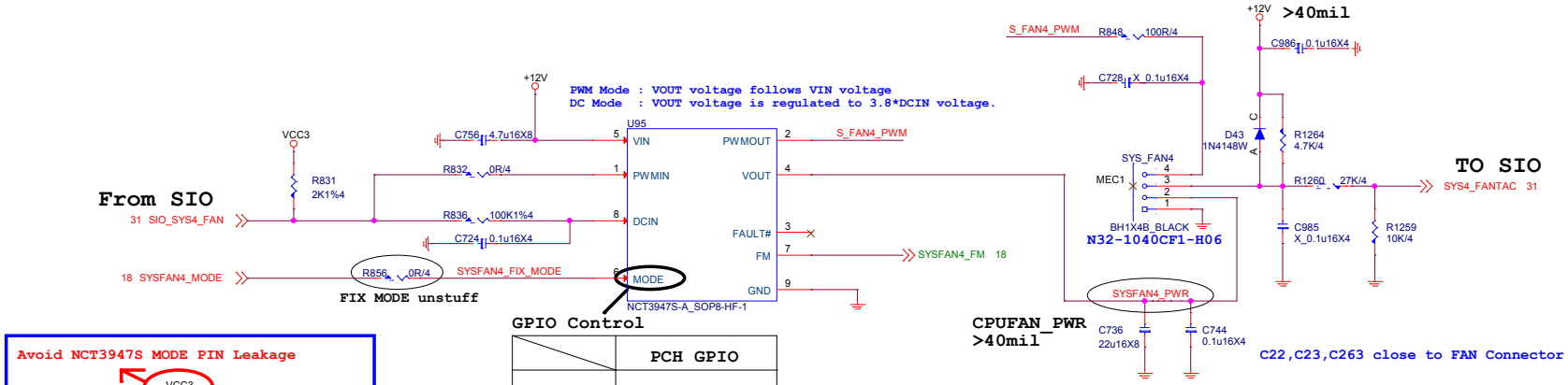
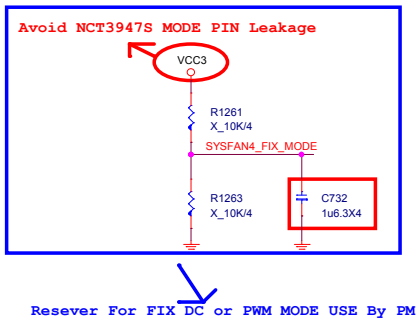
TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

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MS-7A95		
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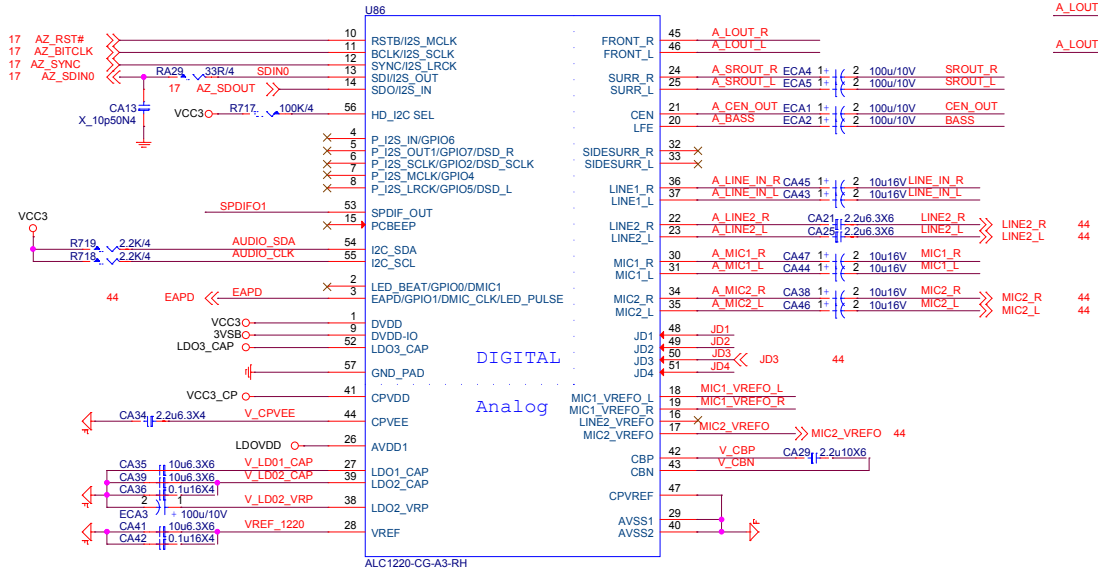
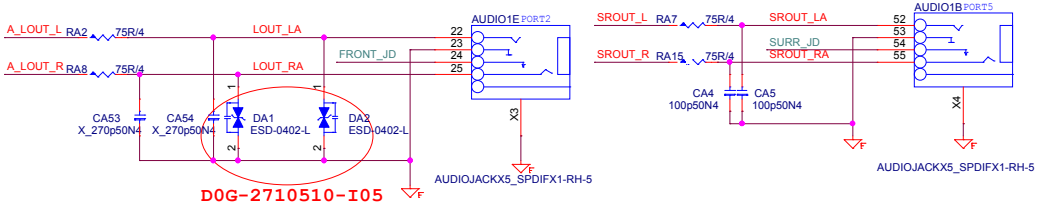
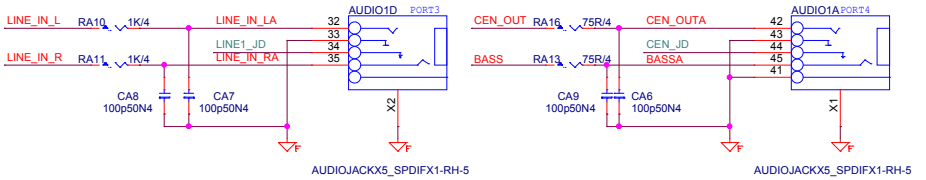
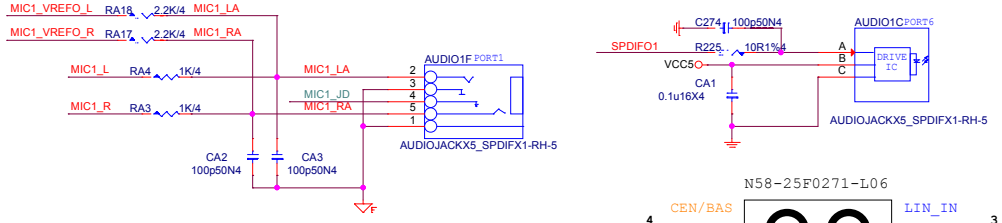
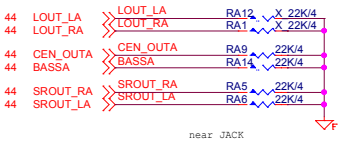
ALC1220

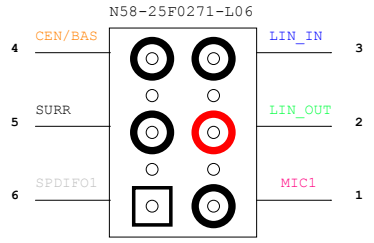


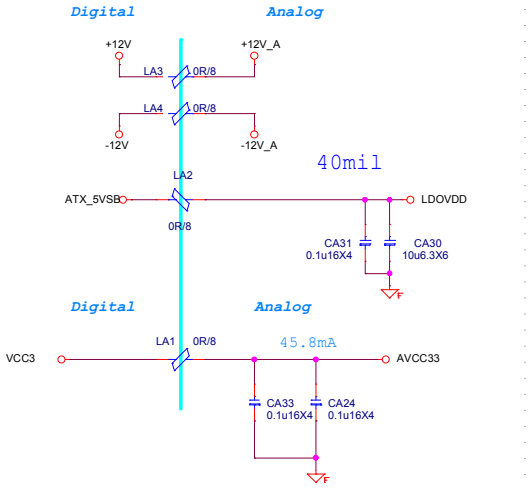




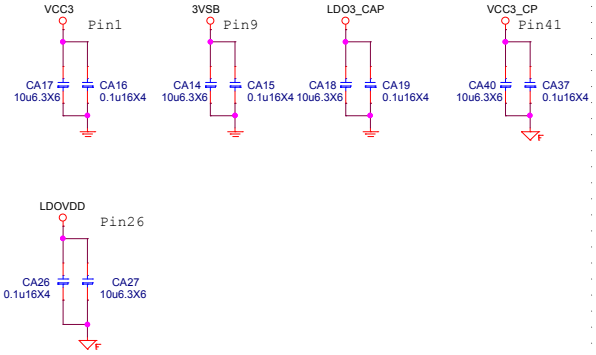




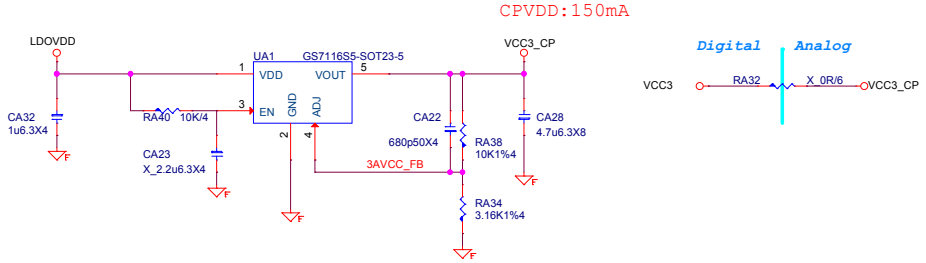




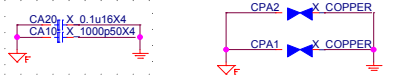
Closed Codec

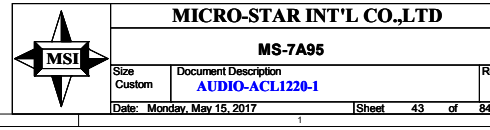


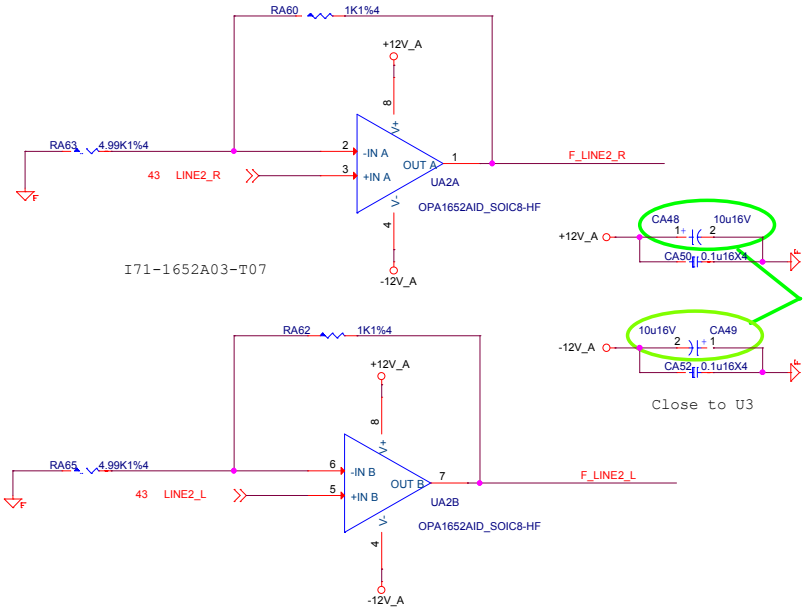
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

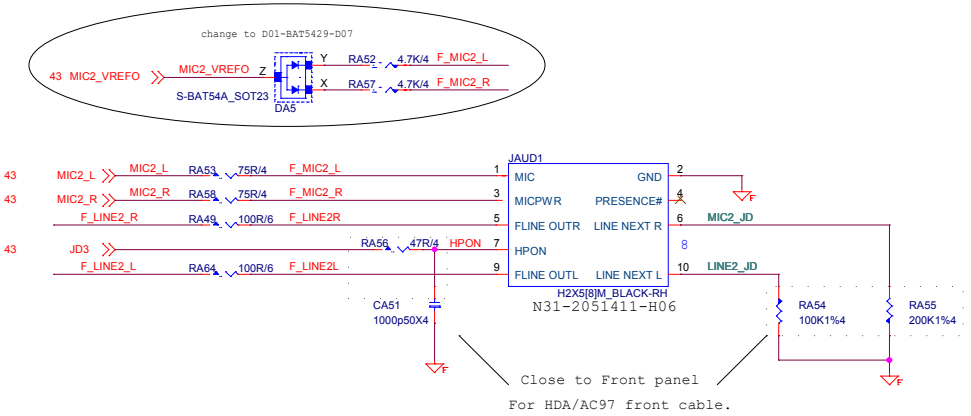


EMI





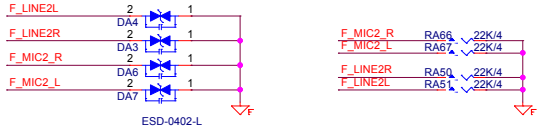




Close to Jack

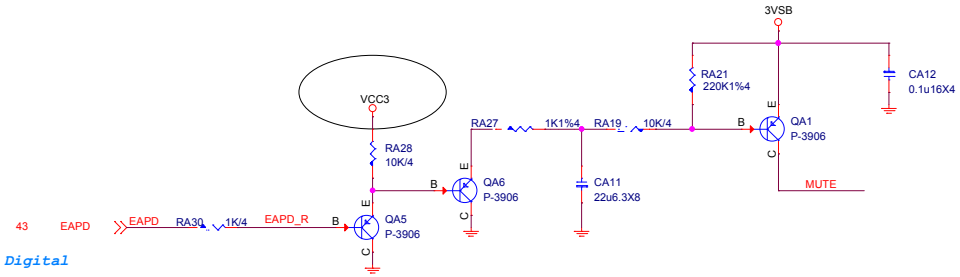
ESD protect

D0G-2950500-SI0
D0G-3010510-I05

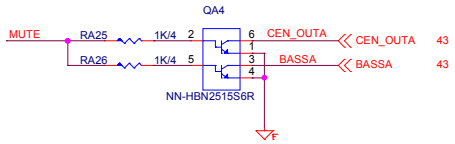


Rear Line OUT De-POP circuit

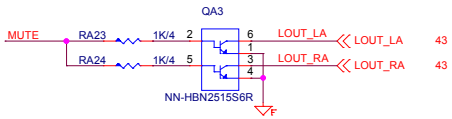
(De-pop circuit for Rear Line out & Front Headphone out)

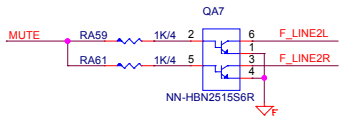


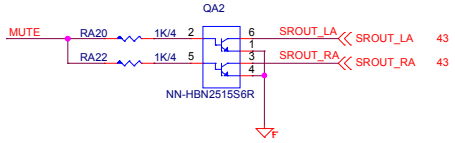
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)



Analog







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MICRO-STAR INT'L CO.,LTD

MS-7A95

Size	Document Description	Rev
Custom	AUDIO-ACL1220-3	1.0

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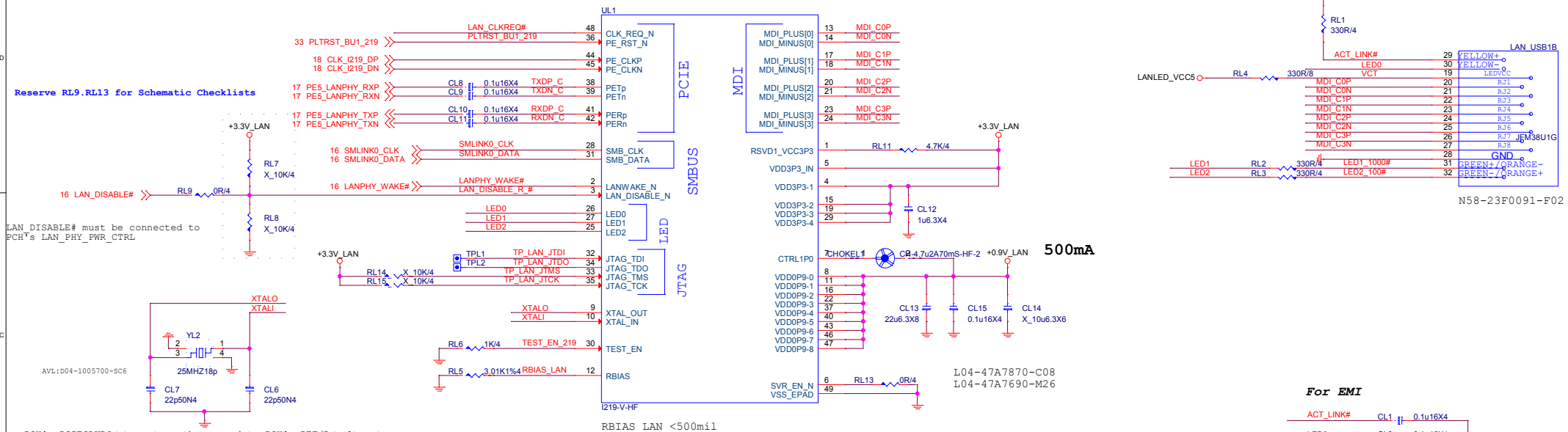
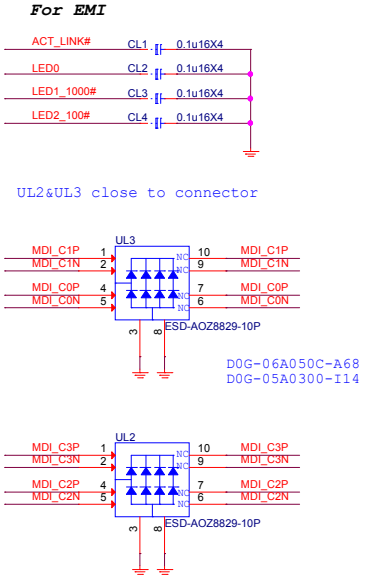
Intel I219V / I218V PHY





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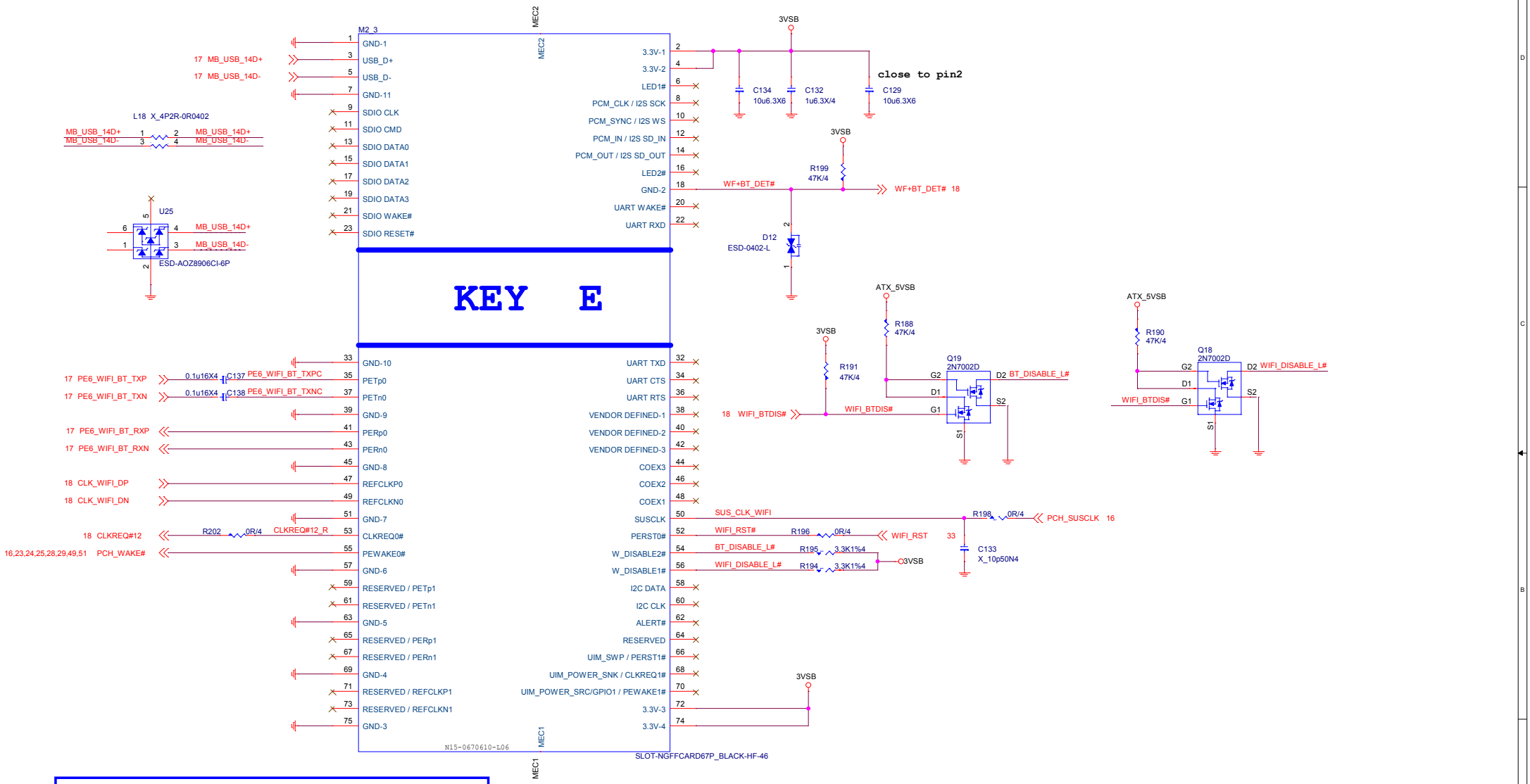

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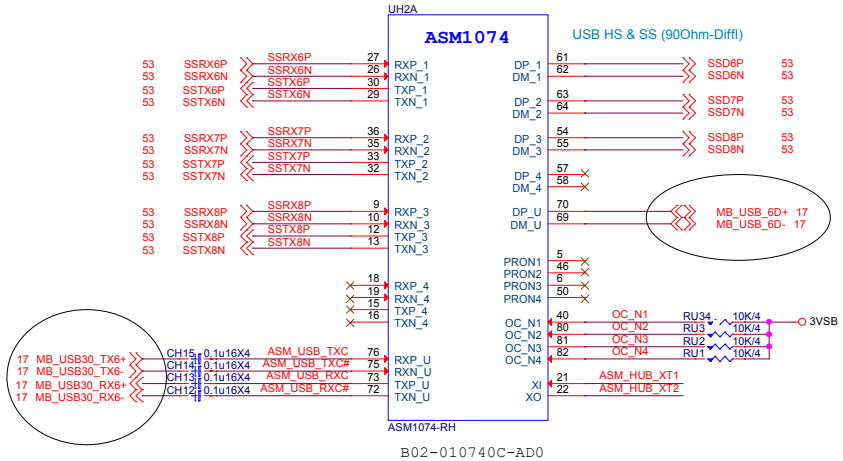
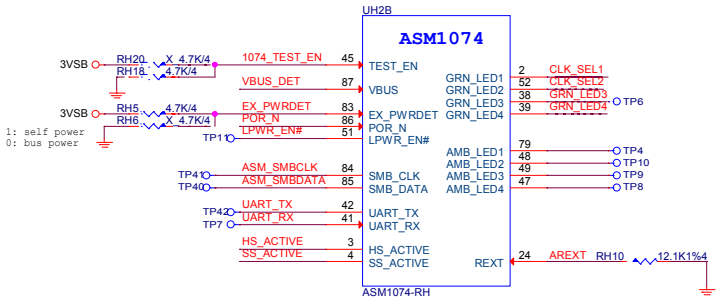
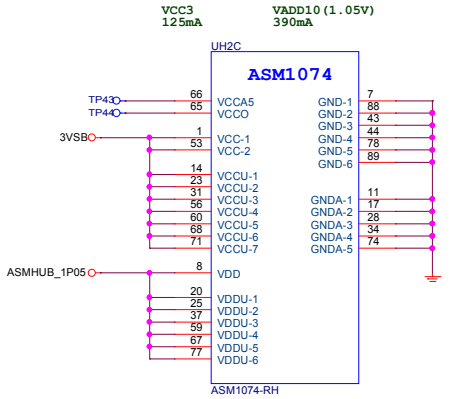
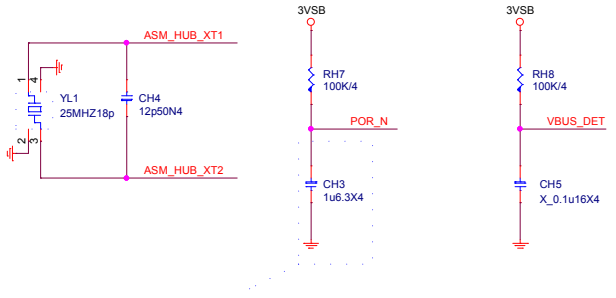
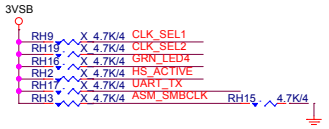








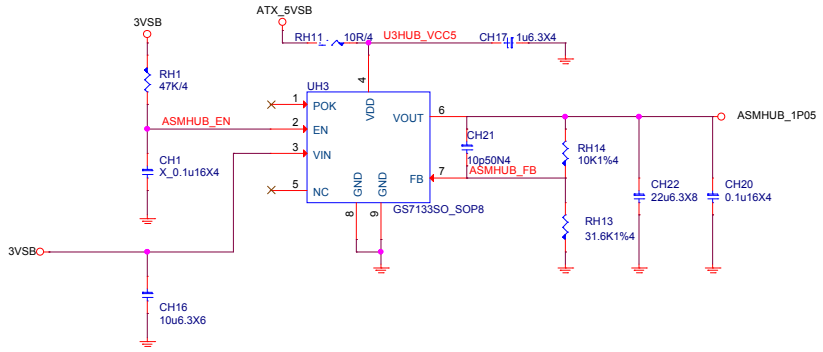
H/W Strapping

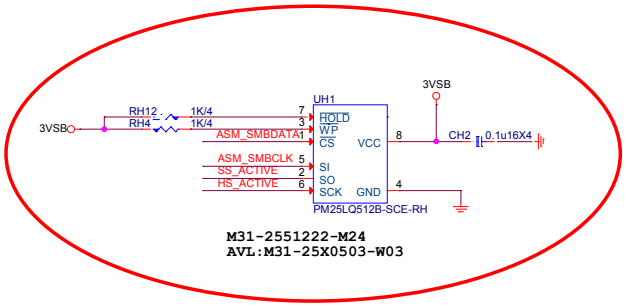


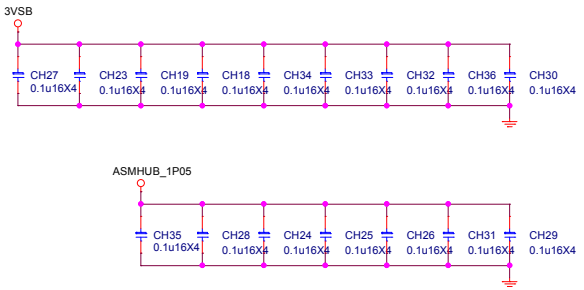
Strapping Table

GRN_LED2 (CLK_SEL1)	GRN_LED1 (CLK_SEL0)	
0	0	25MHz Default
1	0	30MHz
1	1	20MHz

ASM1074 USB3.0 HUB core Power







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MS-7A95	
Size: Custom	Document Description: ASM1074 USB3.0 HUB
Rev: 1.0	
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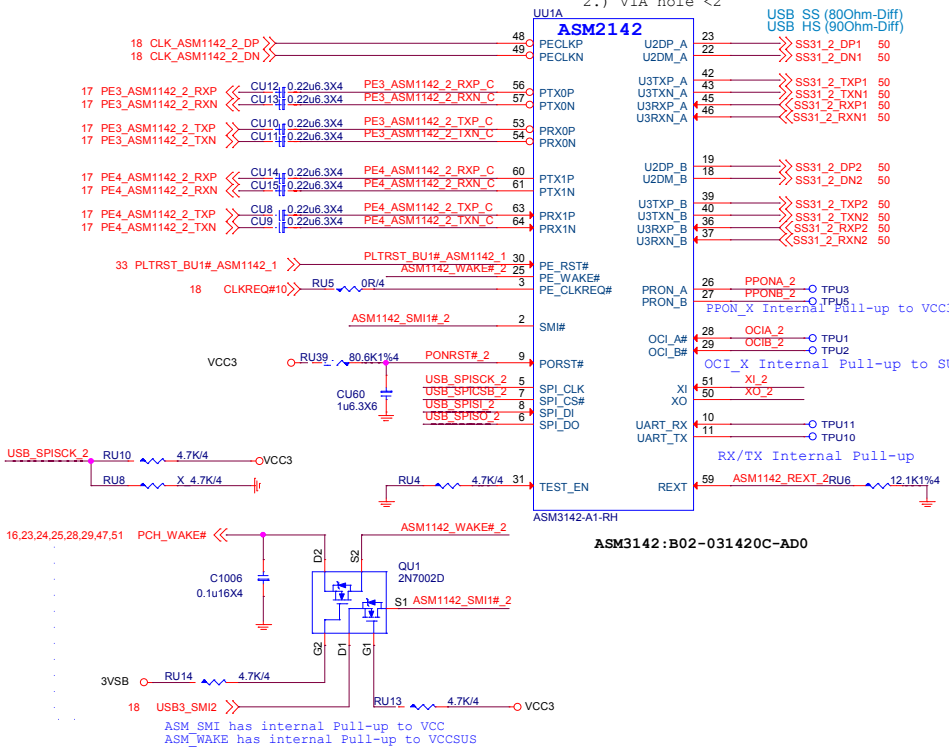
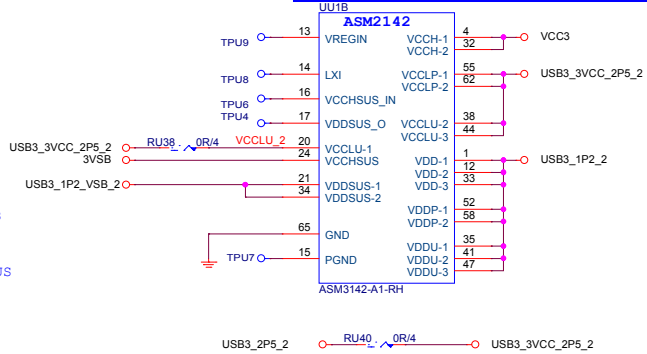
Layout Guide:

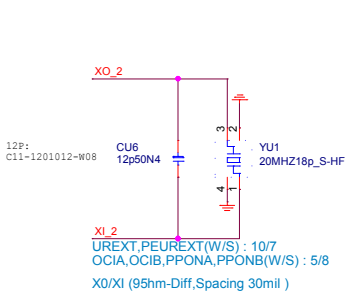
1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

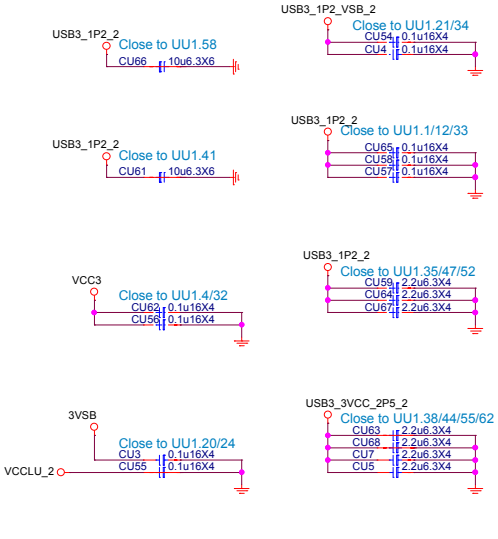


Power Consumption

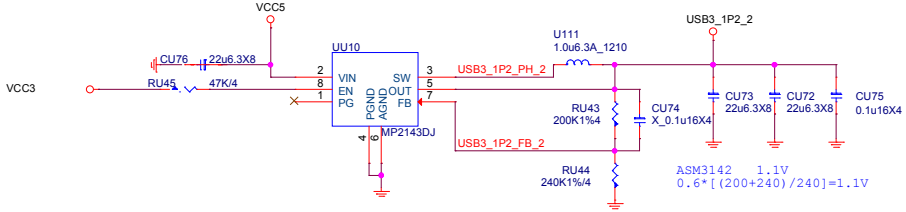
	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP
ASM3142	TBD	TBD	TBD	TBD	TBD	TBD

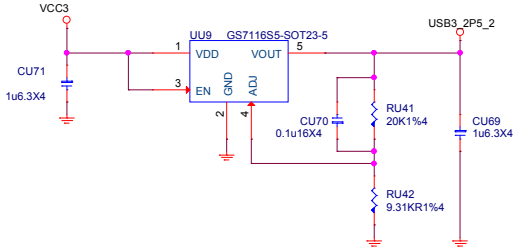




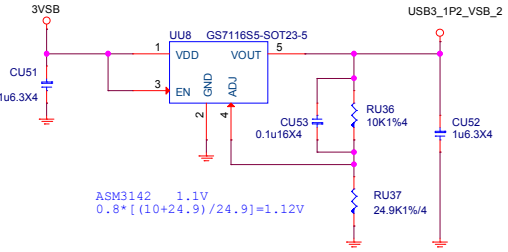


ASM3142 1.1 VCC Power

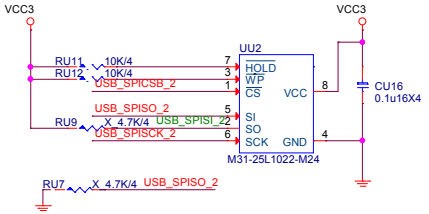




ASM3142 1.1 VSB Power



EEPROM



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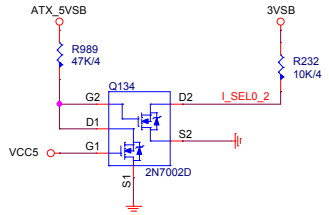
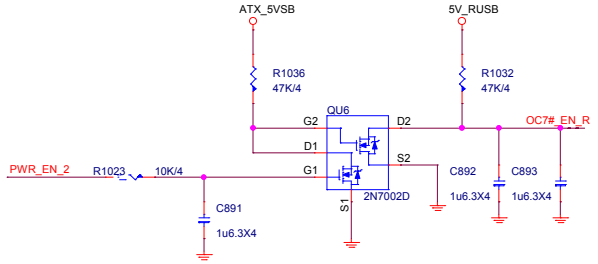
Current Mode

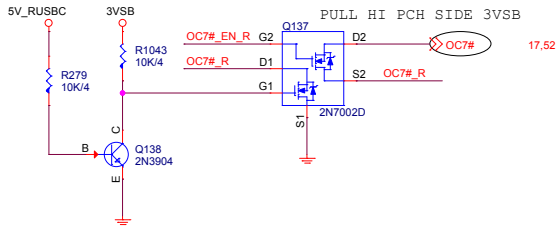


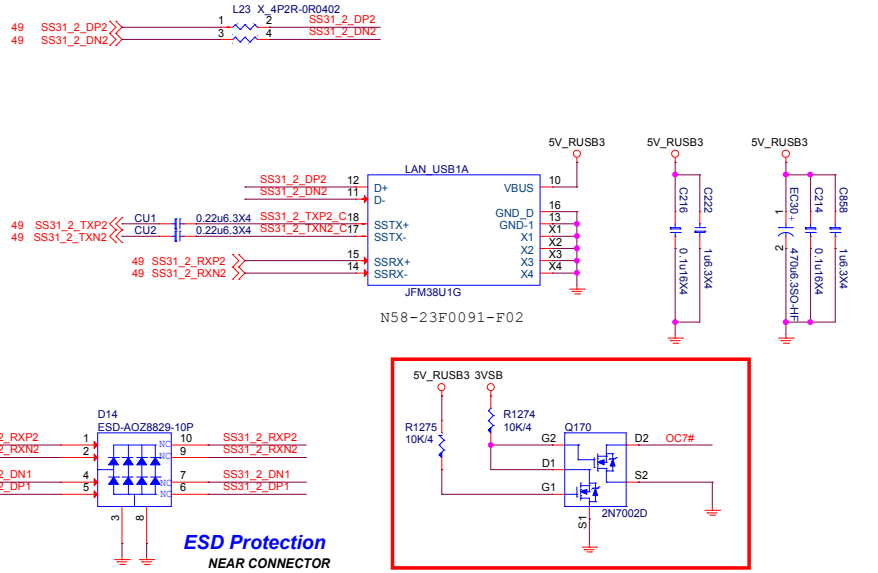
0	X	Default for 900mA
1	0	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

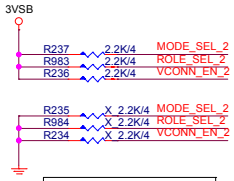
VBUS OC#







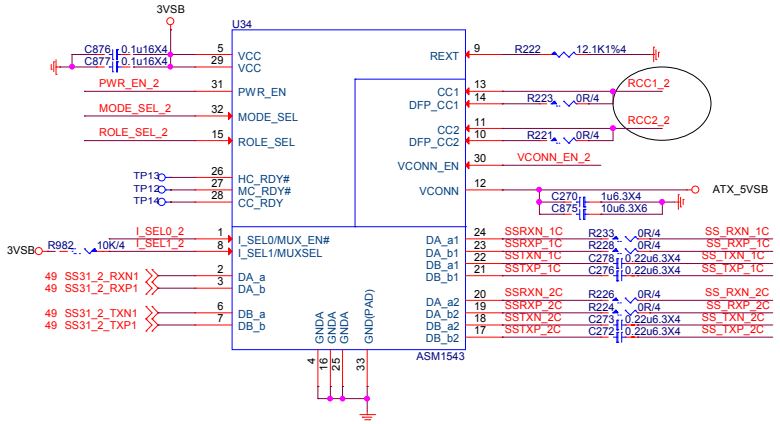
USB Type-C MUX with Configuration Channel (CC)

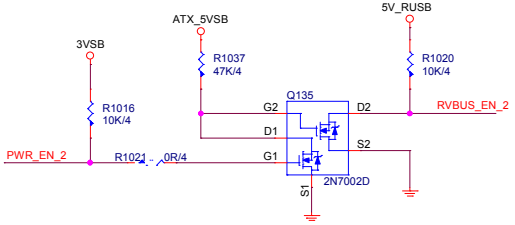


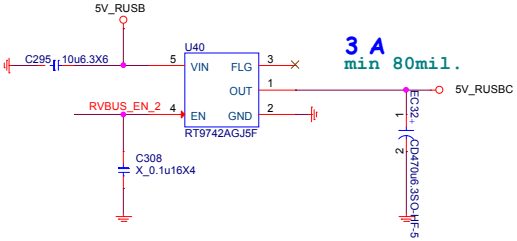
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

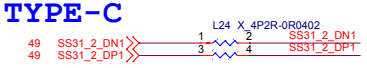
VCONN_EN	
1	enable
0	disable

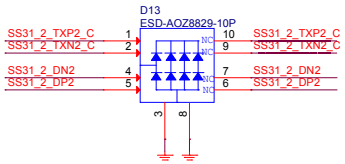




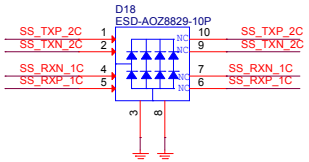


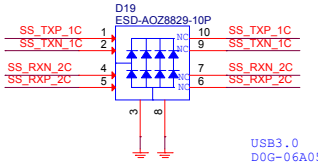
TYPE-C



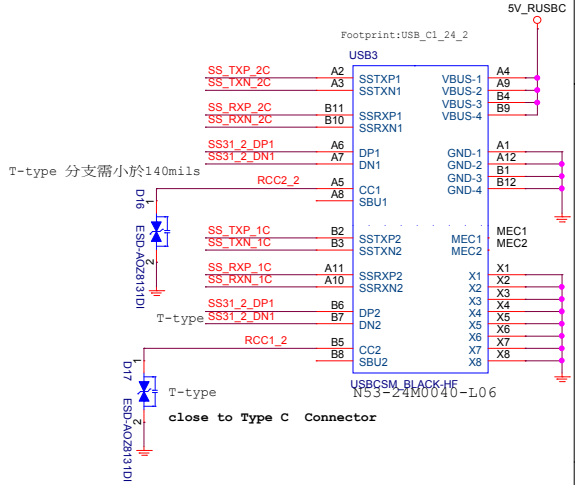


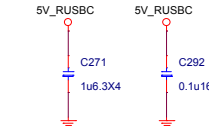
ESD Protection
NEAR CONNECTOR





USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A95	
Size: Custom	Document Description: USB TYPEC/A-2	Rev: 1.0
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Use 0.22uF cap for GEN3 , Gen2 use 0.1uf by Upstream SPEC

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

USB SS (80Ohm-Diff)
USB HS (90Ohm-Diff)

UU3A
ASM2142
ASM3142-A1-RH

ASM3142:B02-031420C-AD0

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP

UU3B
ASM2142
ASM3142-A1-RH

X0/XI (95hm-Diff,Spacing 30mil)

ASM3142 1.2 VCC Power

UU6
MP2143DJ

ASM3142 1.1V
0.6*[(200+240)/240]=1.1V

ASM3142 1.2 VSB Power

UU4 GS7116S5-SOT23-5
UU5 GS7116S5-SOT23-5

ASM2142 1.1V
0.8*[(10+24.9)/24.9]=1.12V

EEPROM

UU12
M31-25L1022-M24

M31-25L1022-M24
AVL:M31-25X2023-W03

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Custom	51.ASM2142AE FRONT-USB31-2	1.0

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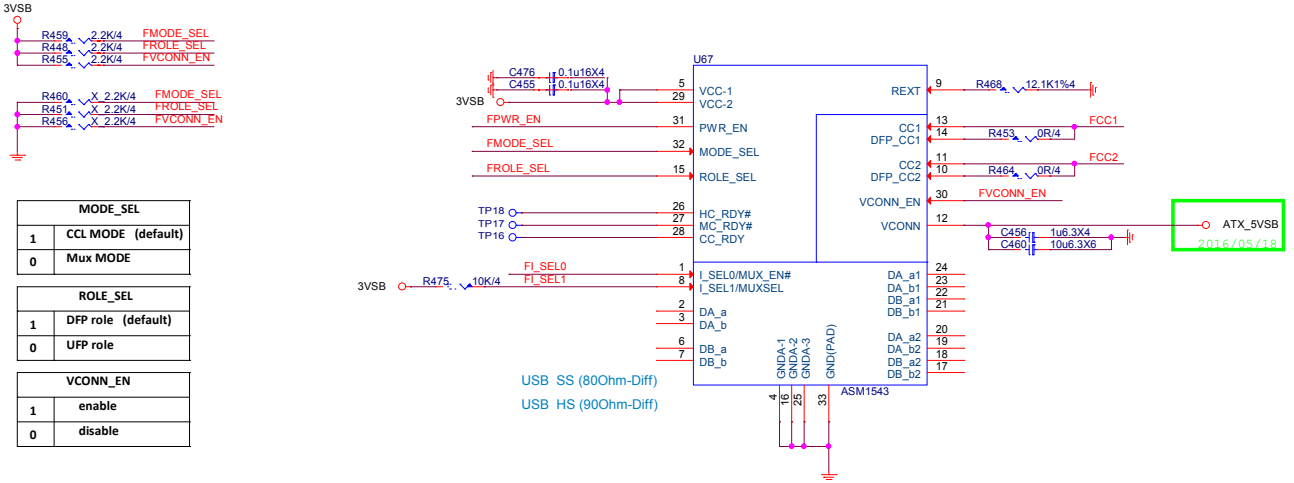
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

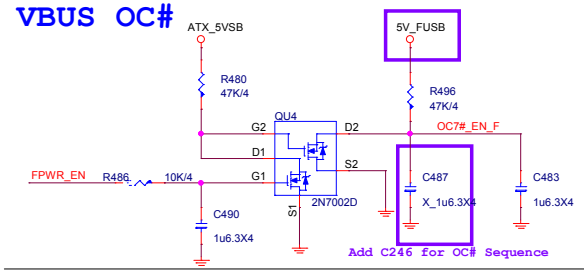


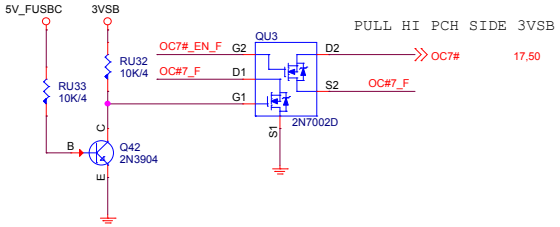
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

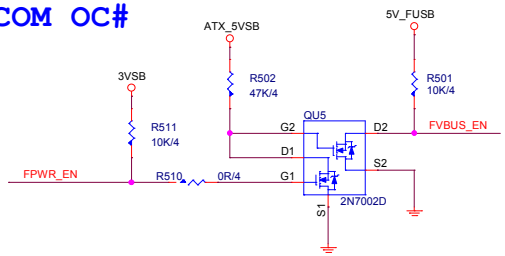
VCONN_EN	
1	enable
0	disable

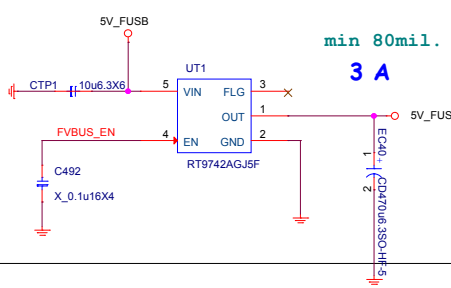
VBUS OC#



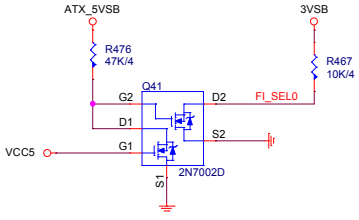


VCOM OC#





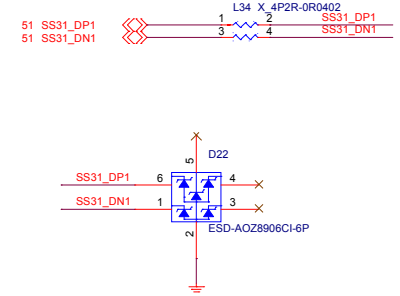
Current Mode

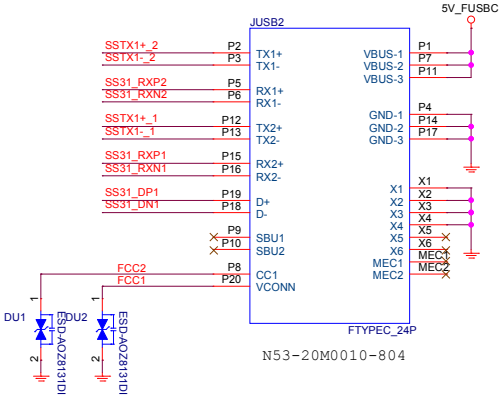


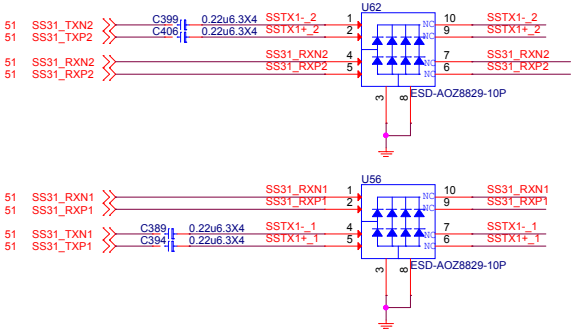
I_SEL0 : I_SEL1

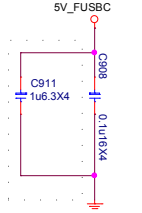
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode









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Size: Custom	Document Description: USB FRONT TYPE-C	Rev: 1.0
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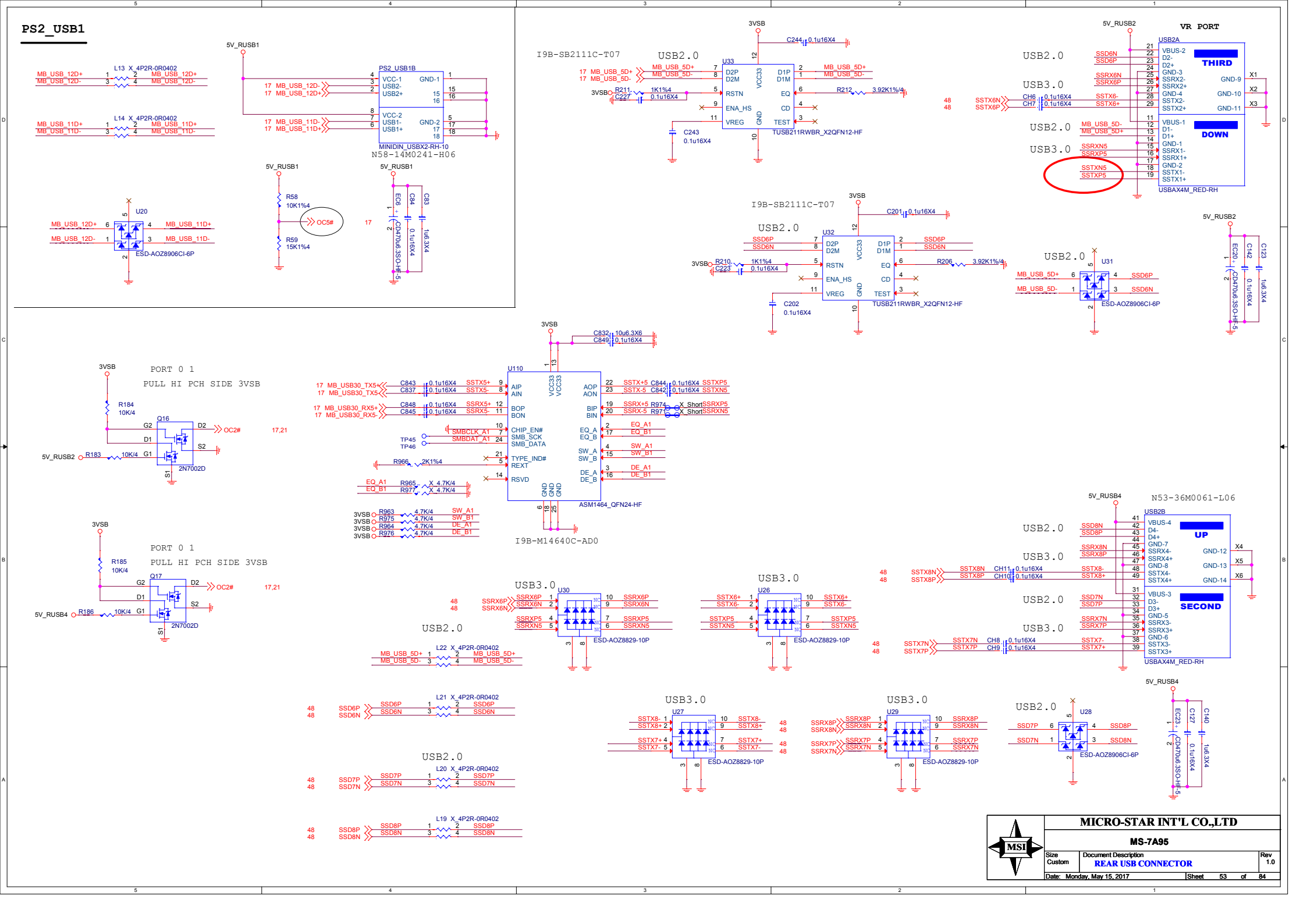
PS2_USB1
L13 X_4P2R-0R0402
L14 X_4P2R-0R0402
5V_RUSB1
PS2_USB1B
MINIDIN_USBX2-RH-10
N58-14M0241-H06
U20
ESD-AOZ8906CI-6P
R58
10K1%4
R59
15K1%4
OC5#
EC3
CD470u6.3SO-HF
C84
C83
0.1u16X4
1u6.3X4
I9B-SB2111C-T07
USB2.0
3VSB
U33
TUSB211RWBR_X2QFN12-HF
C244
0.1u16X4
C243
R211
1K1%4
R212
3.92K1%/4
C227
USB3.0
VR PORT
USB2A
THIRD
DOWN
USBAX4M_RED-RH
U32
C201
C202
R210
R206
U31
C142
C123
PORT 0 1
PULL HI PCH SIDE 3VSB
Q16
Q17
2N7002D
R184
10K/4
R185
R183
R186
OC2#
17,21
U110
ASM1464_QFN24-HF
I9B-M14640C-AD0
C832
10u6.3X6
C849
C843
C837
C848
C845
C844
C842
R974
R971
X_Short
TP45
TP46
R966
2K1%4
R965
R977
X_4.7K/4
R963
R975
R964
R976
4.7K/4
N53-36M0061-L06
USB2B
UP
SECOND
U30
U26
U27
U29
U28
ESD-AOZ8829-10P
L22 X_4P2R-0R0402
L21 X_4P2R-0R0402
L20 X_4P2R-0R0402
L19 X_4P2R-0R0402
MICRO-STAR INT'L CO.,LTD
MS-7A95
Size
Custom
Document Description
REAR USB CONNECTOR
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FRONT USB PORT 7,8

0D先Remove Redriver

L42 X_4P2R-0R0402
17 MB_USB_7D-
17 MB_USB_7D+
MB_USB_7D-
MB_USB_7D+

L41 X_4P2R-0R0402
17 MB_USB_8D-
17 MB_USB_8D+
MB_USB_8D-
MB_USB_8D+

U94
MB_USB_7D-
MB_USB_7D+
MB_USB_8D-
MB_USB_8D+
ESD-AOZ8906CI-6P
NEAR CONNECTOR

5V_FUSB1
C739 0.1u16X4
JUSB4
MB_USB_7D-
MB_USB_7D+
MB_USB_8D-
MB_USB_8D+
BH2X5[9]_BLACK-RH-9
N32-2051931-H06

17,2 OC3#
R854 10K1%4
R853 15K1%4
5V_FUSB1

C299 0.1u16X4 SSTXP1
C307 0.1u16X4 SSTXN1
17 MB_USB30_TX1+
17 MB_USB30_TX1-
17 MB_USB30_RX1+
17 MB_USB30_RX1-

C285 0.1u16X4 SSTXP2
C286 0.1u16X4 SSTXN2
17 MB_USB30_TX2+
17 MB_USB30_TX2-
17 MB_USB30_RX2+
17 MB_USB30_RX2-

JUSB1 180度
56 USB_2D+
56 USB_2D-
SSTXP2
SSTXN2
MB_USB30_RX2+
MB_USB30_RX2-
IBC_VCC2
GND-1
GND-2
56 USB_1D+
56 USB_1D-
SSTXP1
SSTXN1
MB_USB30_RX1+
MB_USB30_RX1-
GND-3
IBC_VCC1
VBUS-1
GND-4
NC
2X10 Connector
BH2X10[20]-2PITCH_BLACK-RH-11
N32-2101571-H06

L26 X_4P2R-0R0402
USB_1D+
USB_1D-
L25 X_4P2R-0R0402
USB_2D+
USB_2D-

U35
USB_1D+
USB_1D-
USB_2D+
USB_2D-
ESD-AOZ8906CI-6P

U42
ESD-AOZ8829-10P
SSTXP1
SSTXN1
MB_USB30_RX1+
MB_USB30_RX1-
Close to Connector

U38
ESD-AOZ8829-10P
SSTXP2
SSTXN2
MB_USB30_RX2+
MB_USB30_RX2-

IBC_VCC2
C332 0.1u16X4
IBC_VCC1
C312 0.1u16X4

FRONT USB PORT 9.10

L40 X_4P2R-0R0402
17 MB_USB_9D-
17 MB_USB_9D+
MB_USB_9D-
MB_USB_9D+

L39 X_4P2R-0R0402
17 MB_USB_10D-
17 MB_USB_10D+
MB_USB_10D-
MB_USB_10D+

U93
MB_USB_9D-
MB_USB_9D+
MB_USB_10D-
MB_USB_10D+
ESD-AOZ8906CI-6P
NEAR CONNECTOR

5V_FUSB1
C727 0.1u16X4
JUSB5
MB_USB_9D-
MB_USB_9D+
MB_USB_10D-
MB_USB_10D+
BH2X5[9]_BLACK-RH-9
N32-2051931-H06

17 OC4#
R835 10K1%4
R844 15K1%4
5V_FUSB1

5V_FUSB1
EC54
CD470u6.3SQ-HF-5

L36 X_4P2R-0R0402
MB_USB_3D+
MB_USB_3D-
L35 X_4P2R-0R0402
MB_USB_4D+
MB_USB_4D-

U66
MB_USB_3D+
MB_USB_3D-
MB_USB_4D+
MB_USB_4D-
ESD-AOZ8906CI-6P

U74
ESD-AOZ8829-10P
17 MB_USB30_RX4+
17 MB_USB30_RX4-
17 MB_USB30_RX3-
17 MB_USB30_RX3+
MB_USB30_RX4+
MB_USB30_RX4-
MB_USB30_RX3-
MB_USB30_RX3+

U69
ESD-AOZ8829-10P
17 MB_USB30_TX4+
17 MB_USB30_TX4-
17 MB_USB30_TX3-
17 MB_USB30_TX3+
C477 0.1u16X4
C464 0.1u16X4
C462 0.1u16X4
C458 0.1u16X4
SSTXP4
SSTXN4
SSTXP3
SSTXN3

5V_FUSB2
EC43
CD470u6.3SQ-HF-5
5V_FUSB2
C494 0.1u16X4

JUSB3 90度
17 MB_USB_4D+
17 MB_USB_4D-
SSTXP4
SSTXN4
MB_USB30_RX4+
MB_USB30_RX4-
5V_FUSB2
GND-1
GND-2
17 MB_USB_3D+
17 MB_USB_3D-
SSTXP3
SSTXN3
MB_USB30_RX3+
MB_USB30_RX3-
GND-3
5V_FUSB2
VBUS1
GND-4
NC
2X10 CONNECTOR
BH2X10[20]#-2PITCH_BLACK-RH-2
N32-2101581-H06

17,21 OC1#
R500 10K1%4
R484 15K1%4
5V_FUSB2

MSI
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Size Custom
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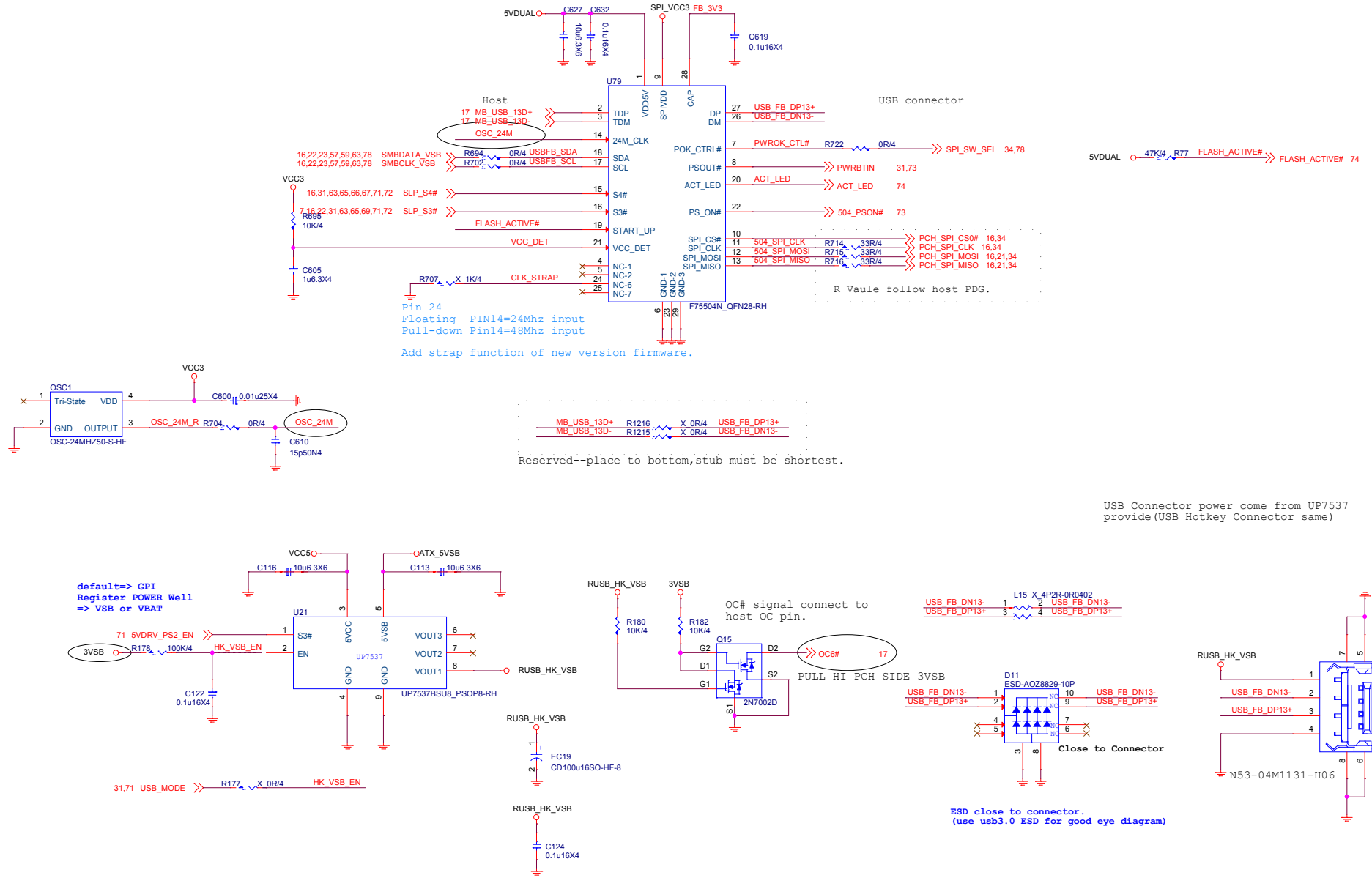
Host USB connector

F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A95	
Size: Custom	Document Description: BIOS FLASH F75504	Rev: 1.0
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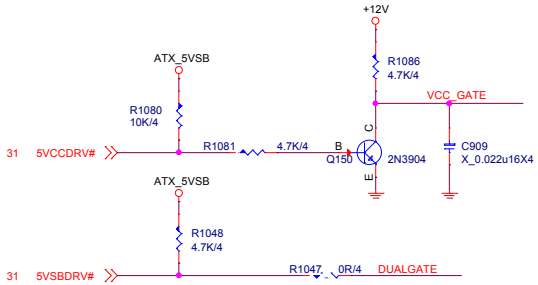
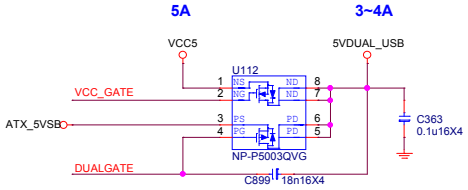
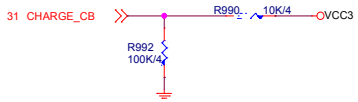
5VDUAL_USB

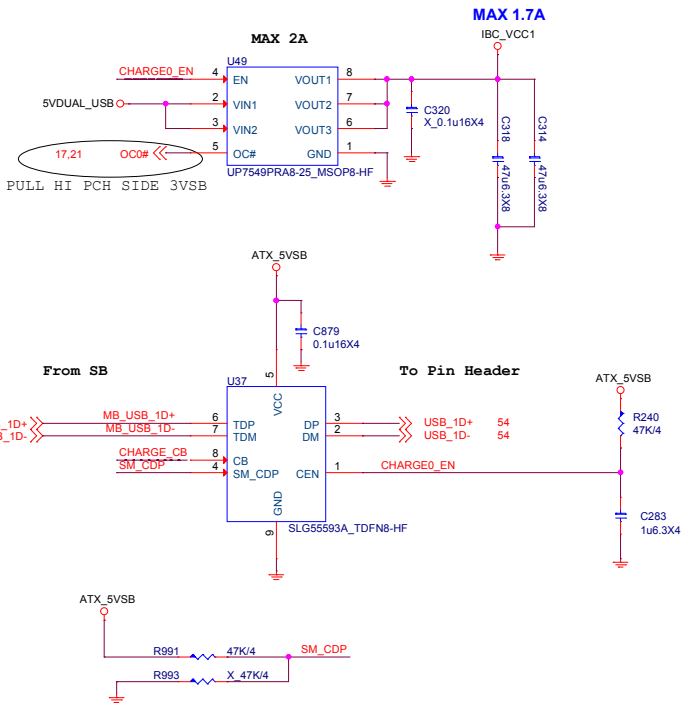




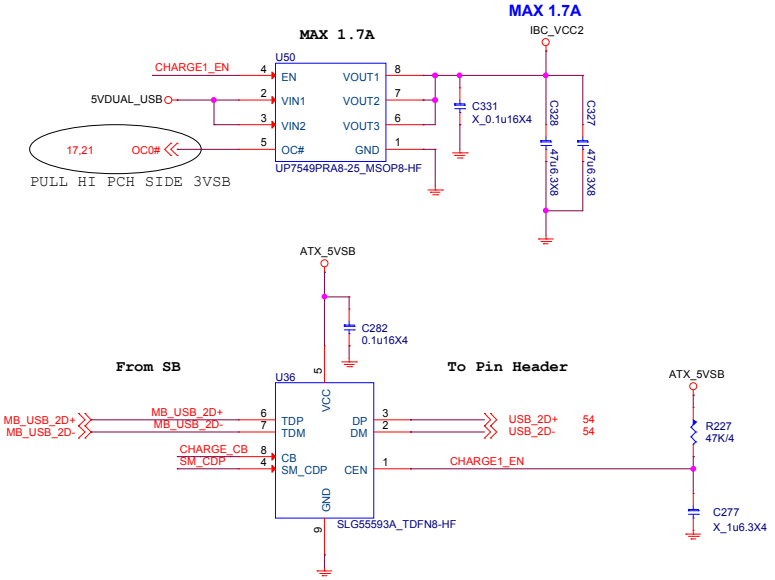
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



USB POWER PORT 0 For USB Charging

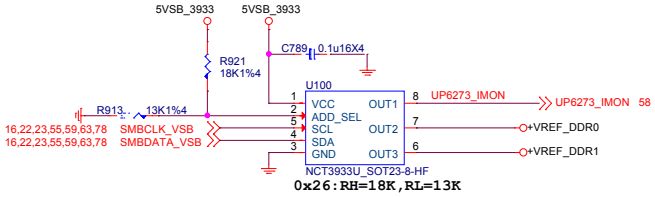


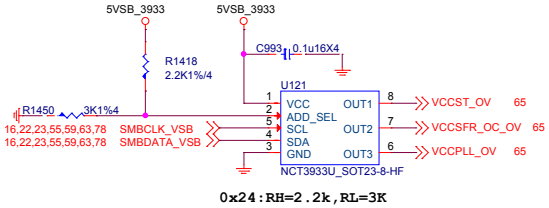
USB POWER PORT 1 For USB Charging

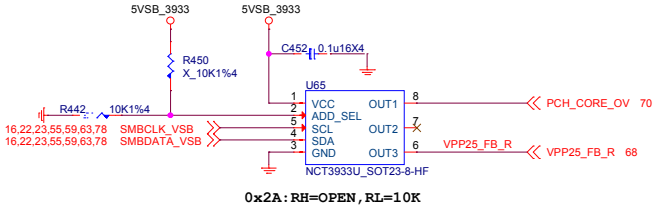


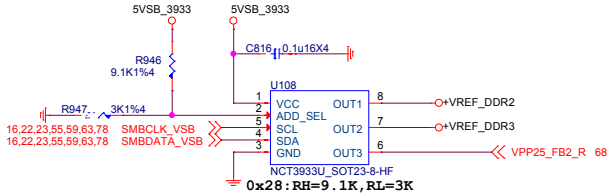
MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size: Custom	Document Description: USB CHARGE_SLG55593A	Rev: 1.0
Date: Monday, May 15, 2017	Sheet 56 of 84	

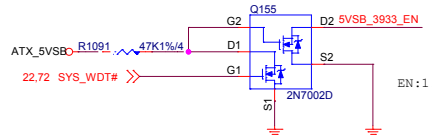
UPI VOLTAGE CONSOLE

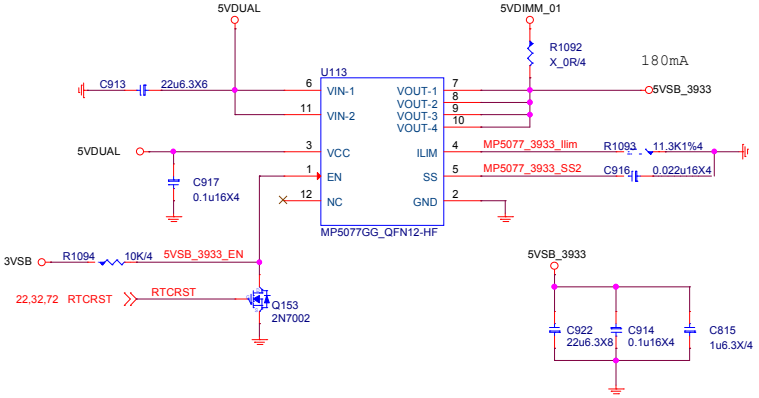








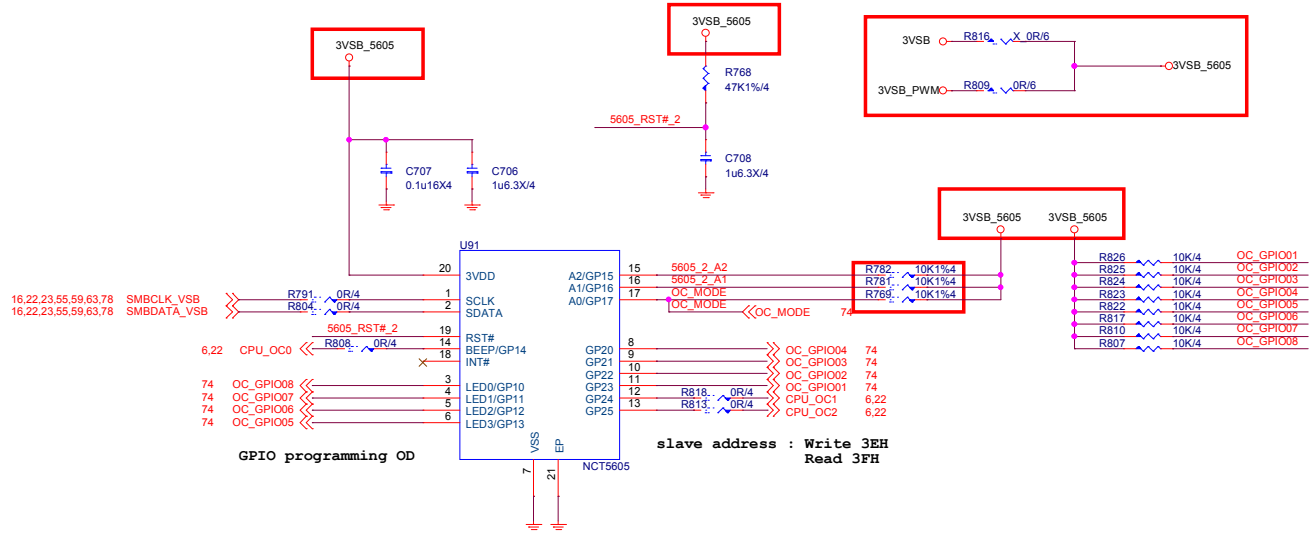




VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%

RSVD FOR OC



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	USB3.0 Connector	1.0

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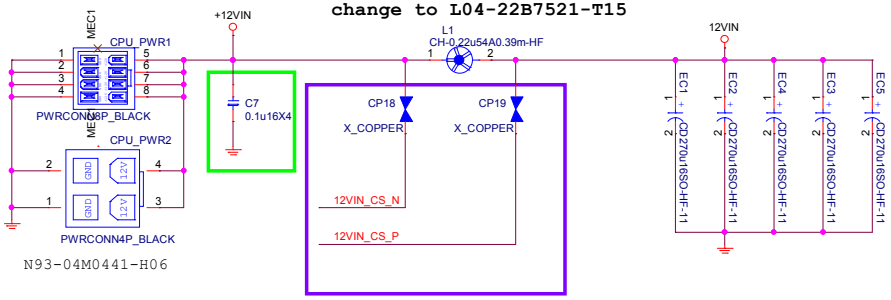
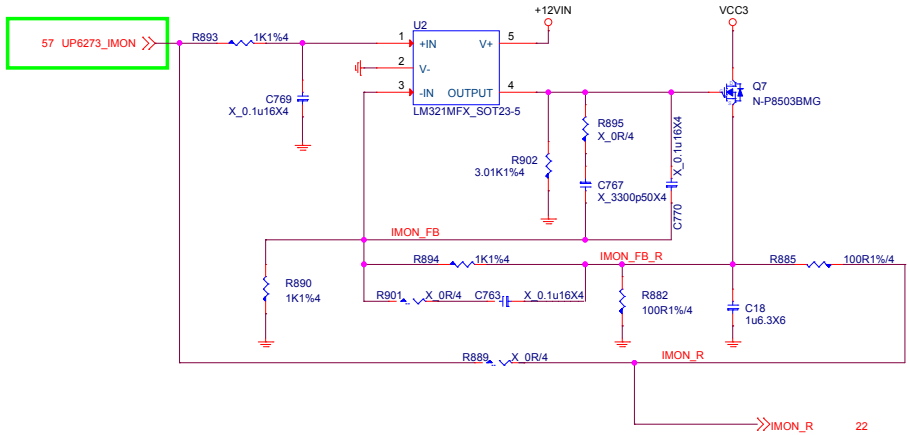
N93-08M0221-H06 Close Power Connector

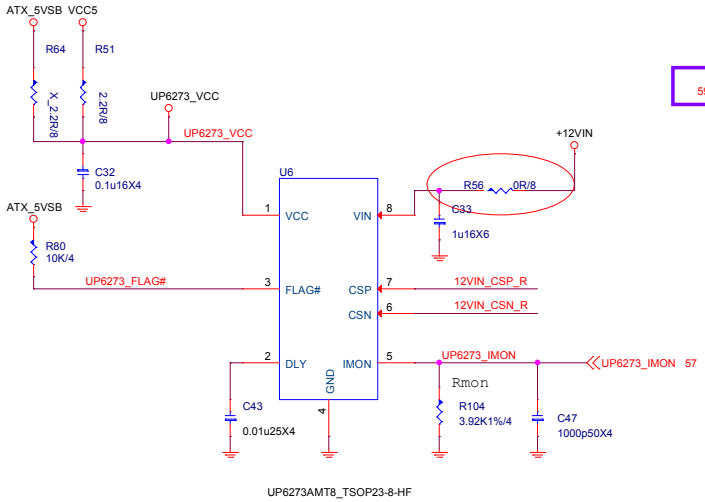
change to L04-22B7521-T15



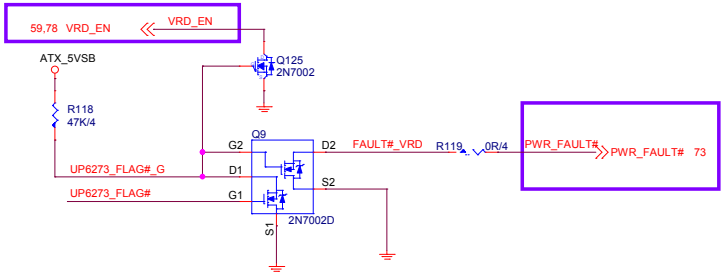
N93-04M0441-H06

Near PWM IC





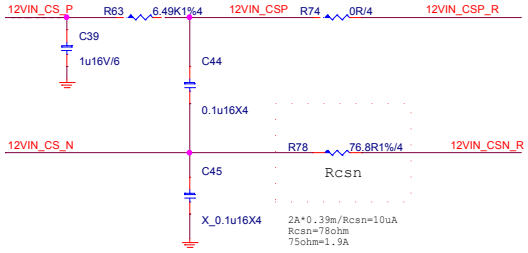
UP6273AMT8_TSOP23-8-HF



Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon

Rmon=(1.2x0.0768k)/(60x0.39m)
=3.9K

一階2A
Rimon5.1Kohm
Rcsn0.0768Kohm
DCR0.39mohm
Vimon1.2V
Iocp46.33484163A
ocp=60A



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VRMPWRGD LEVEL SHIFT

Vcore: ICC Max 100A
LL: 1.0 mohm
OCP: 400A

VSA: ICC Max 15A
OCP: 40A

PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X(IMVP8)

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

0x26:RH=18K,RL=13K

SMB Address: 0X70

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MS-7A95	
Size: Custom	Document Description: CPU PWR-IR35201
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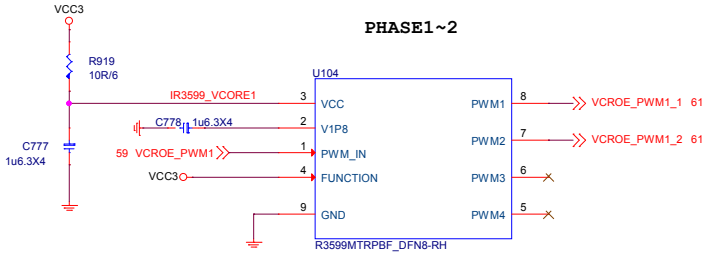
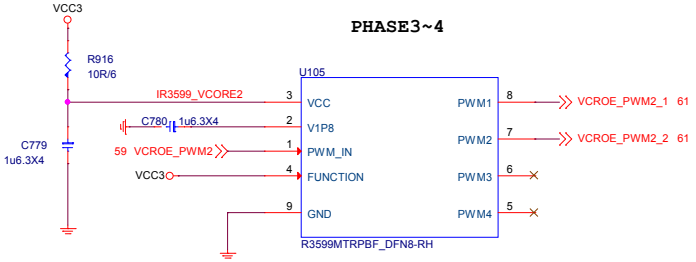
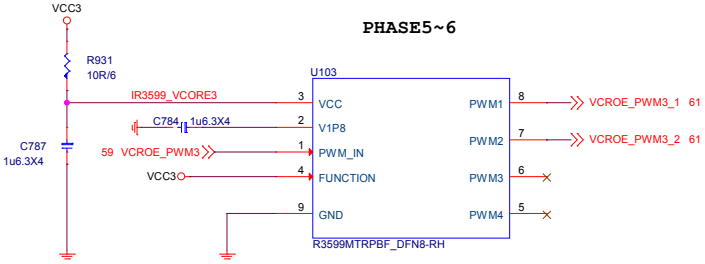
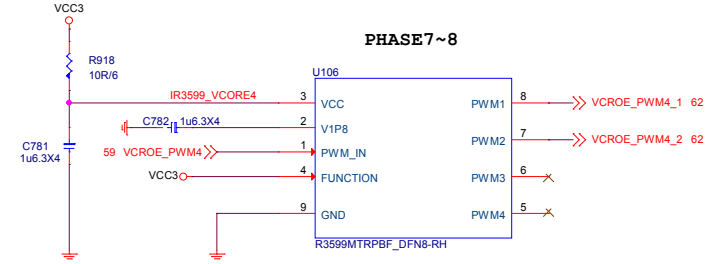
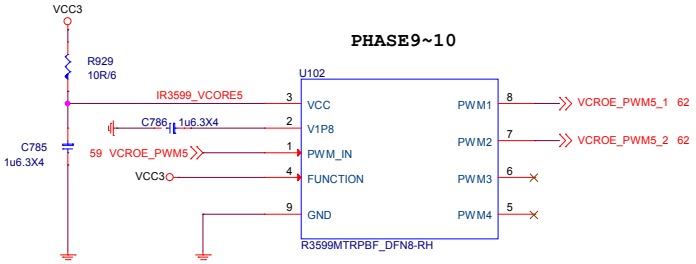
VCORE Double











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	MS-7A95	
Size: Custom	Document Description: CPU PWR-IR3599	Rev: 1.0
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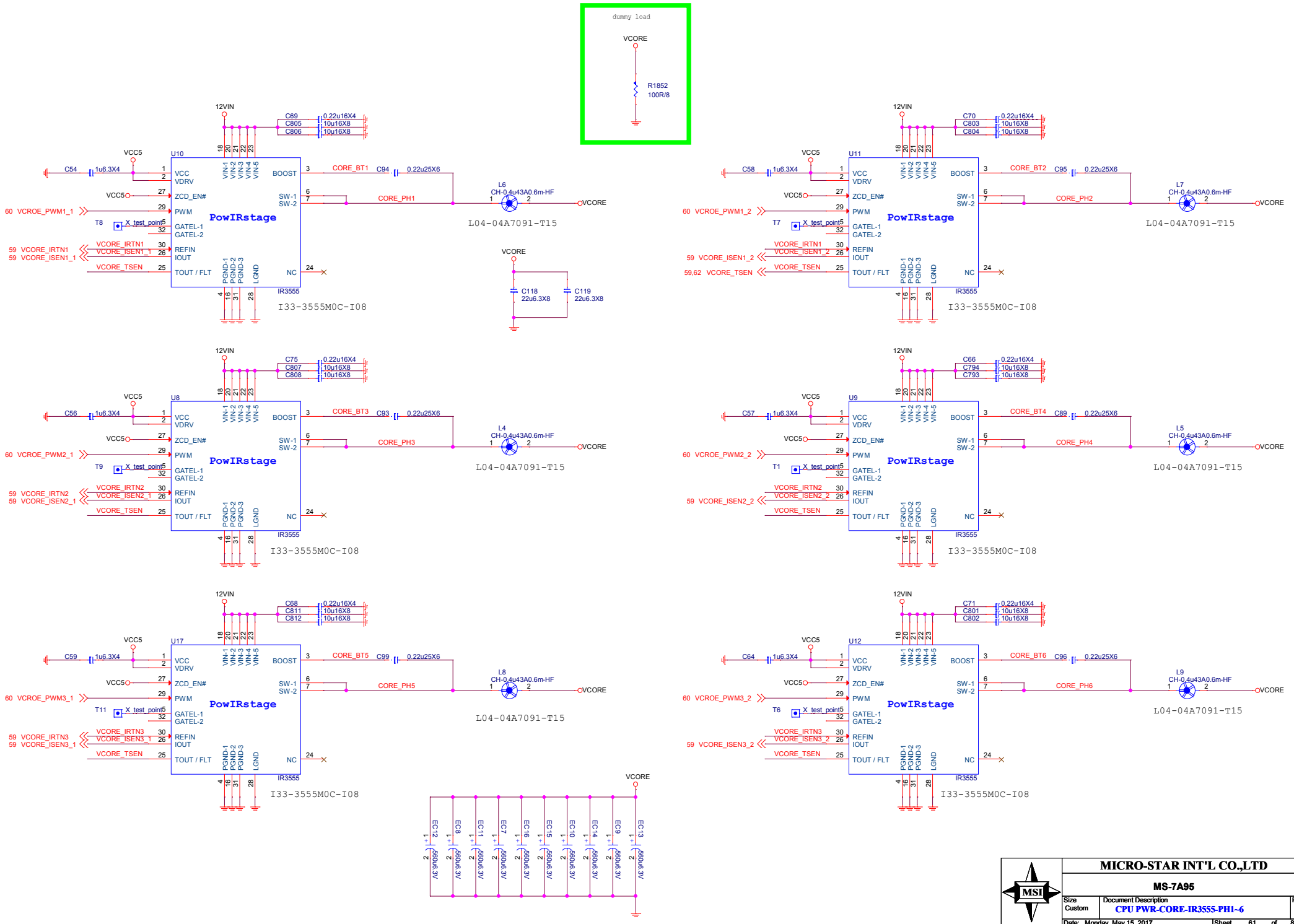

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MS-7A95		
Size: Custom	Document Description: CPU PWR-CORE-IR3555-PH1~6	Rev: 1.0
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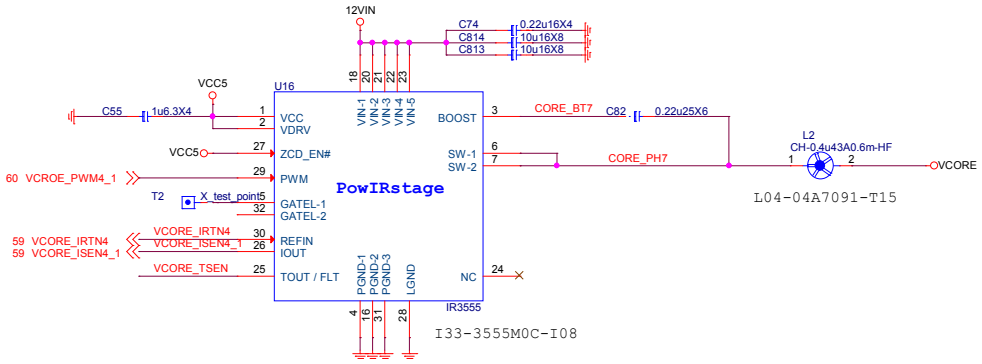

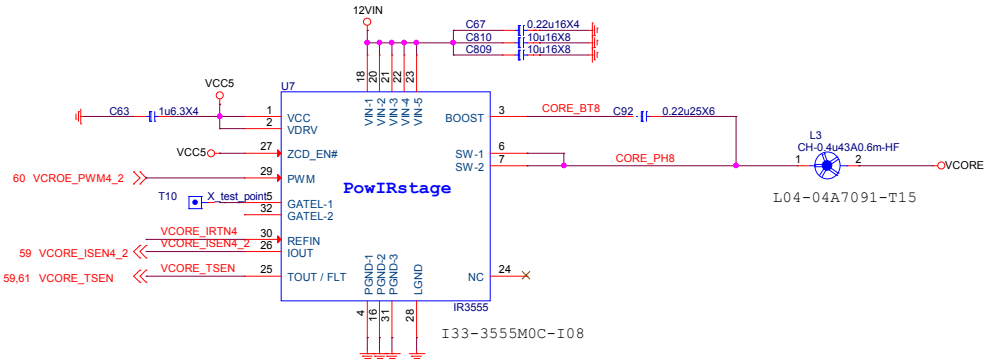

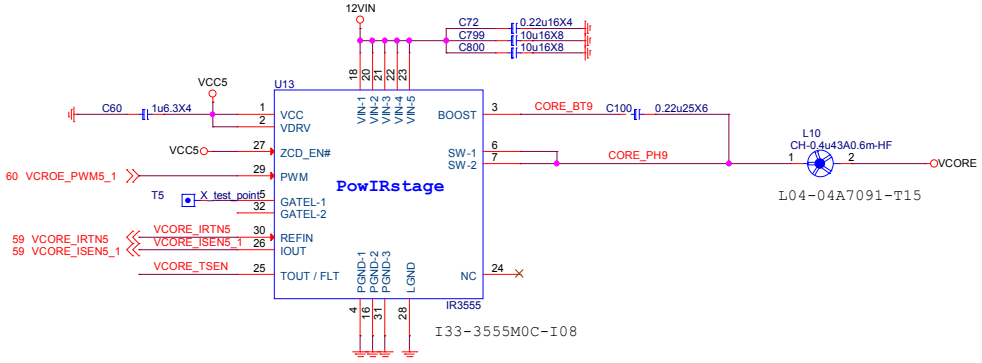

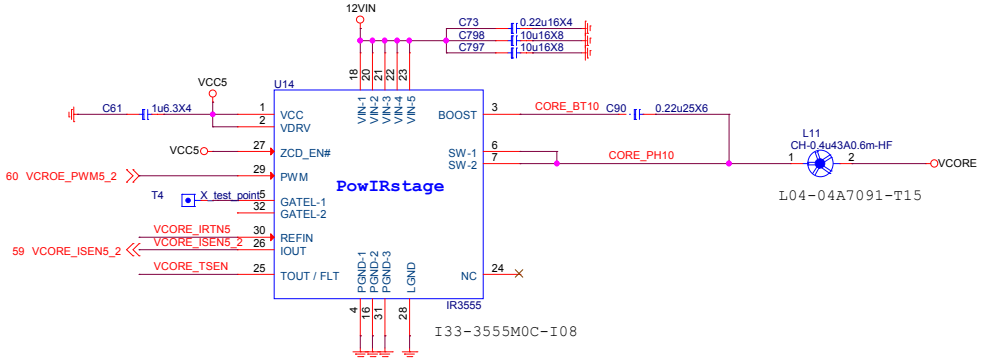

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Size	Document Description	Rev
Custom	CPU PWR-CORE-IR3555-PH7~10	1.0

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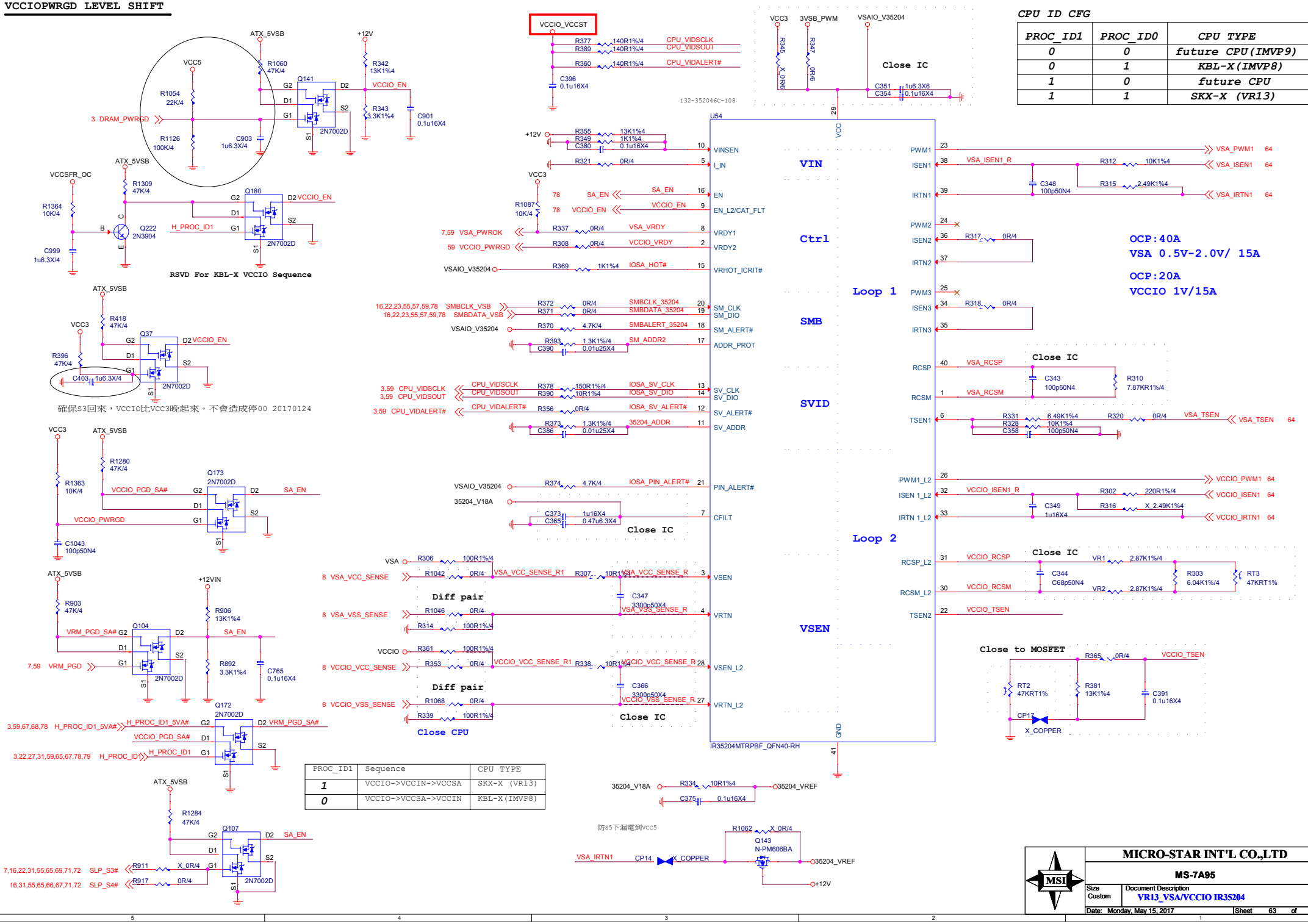
VCCIOPWRGD LEVEL SHIFT



CPU ID CFG

PROC_ID1	PROC_ID0	CPU TYPE
0	0	future CPU(IMVP9)
0	1	KBL-X(IMVP8)
1	0	future CPU
1	1	SKX-X (VR13)

PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X(IMVP8)

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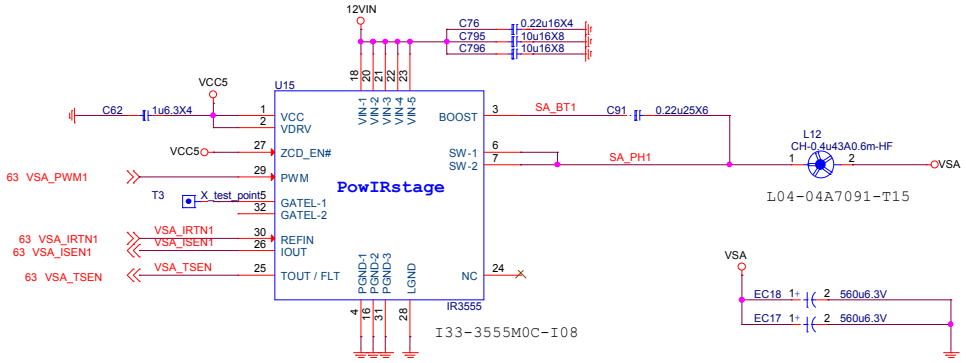
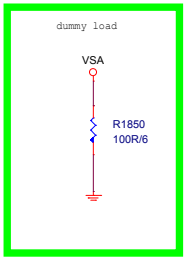
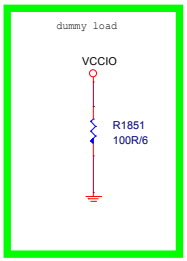
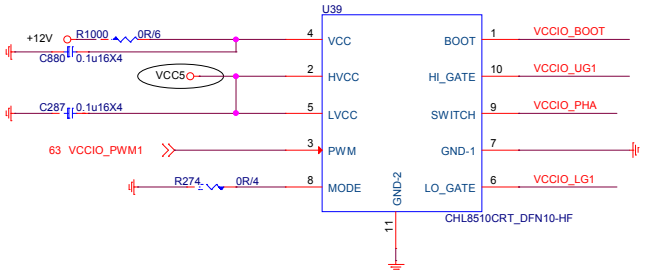
OCP:40A
VSA 0.5V-2.0V/ 15A

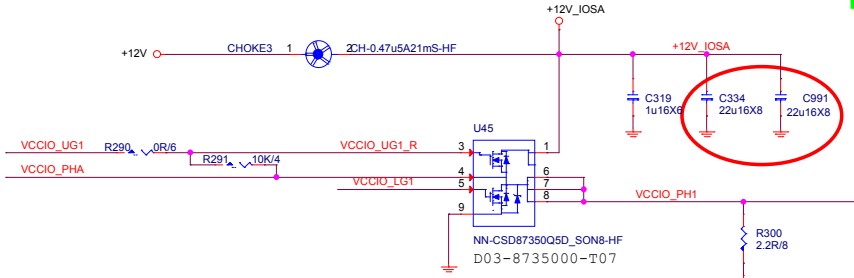






OCP:20A
VCCIO 1V/15A





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Size: Custom	Document Description: VCCIO/VSA 1+1 PHASE	Rev: 1.0
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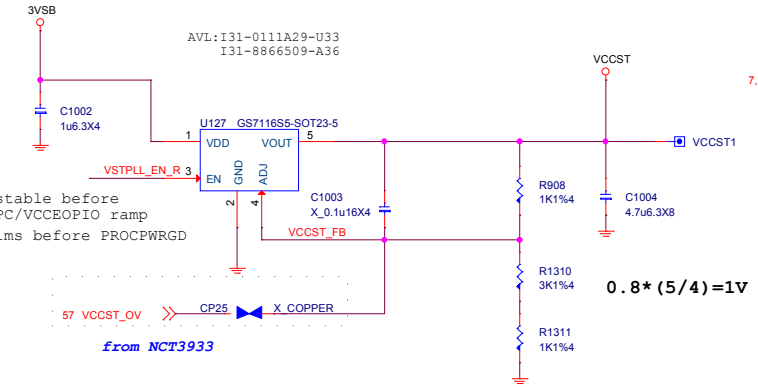
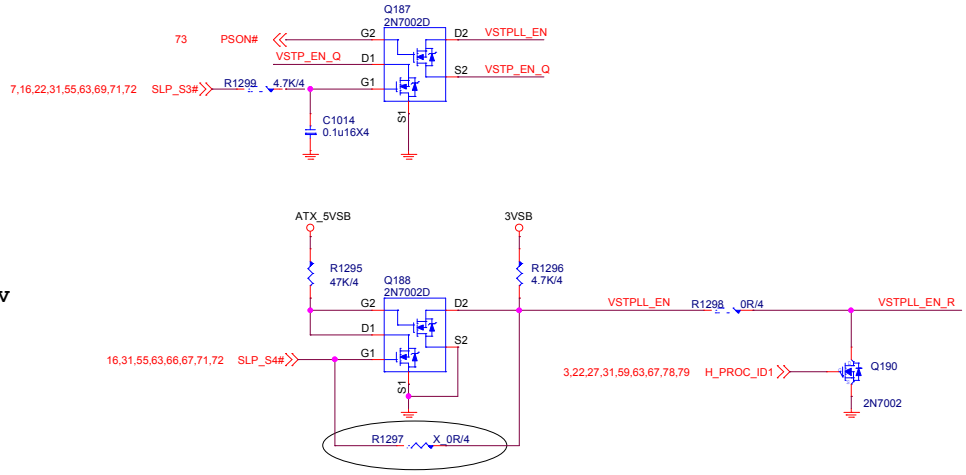
VCCST

1.0V; 60mA



VCCIO ramped and stable before
beginning of VCCOPC/VCCEOPIO ramp
VCCST/PLL stable 1ms before PROCPWRGD

0.8*(5/4)=1V

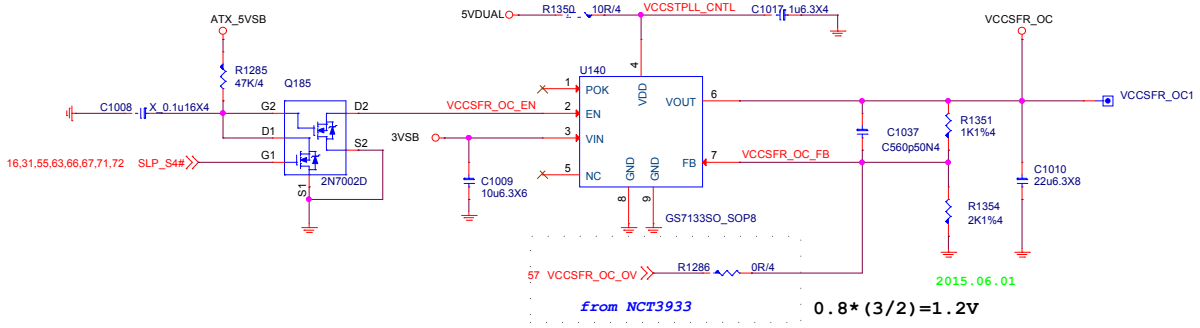


For non-OC system, configures +VCCSFR_OC as 1.2V

VCCSFR_OC

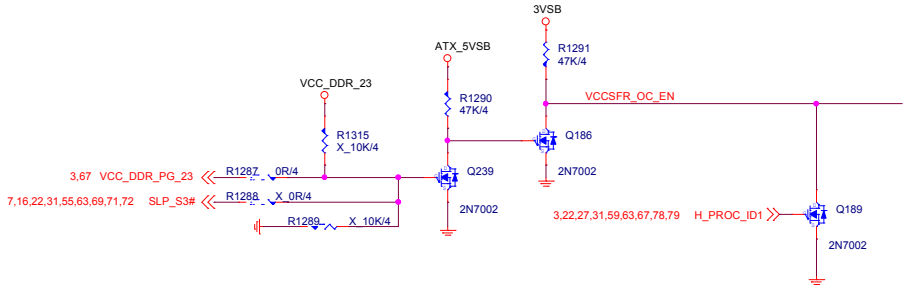
1.1V~1.5A; 500mA

EN:VIH1.2V
EN pin Maximum:VIN+0.3V



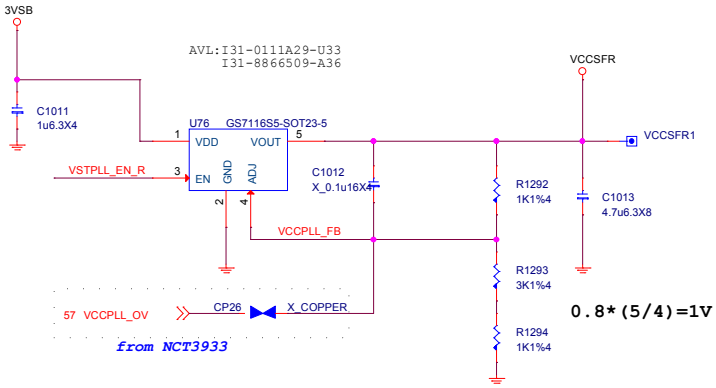
2015.06.01

0.8*(3/2)=1.2V



VCCSFR

1.0V; 150mA



0.8*(5/4)=1V

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Size: Custom	Document Description: CPU VCCST/VCCSFR/VCCSFR_OC	Rev: 10
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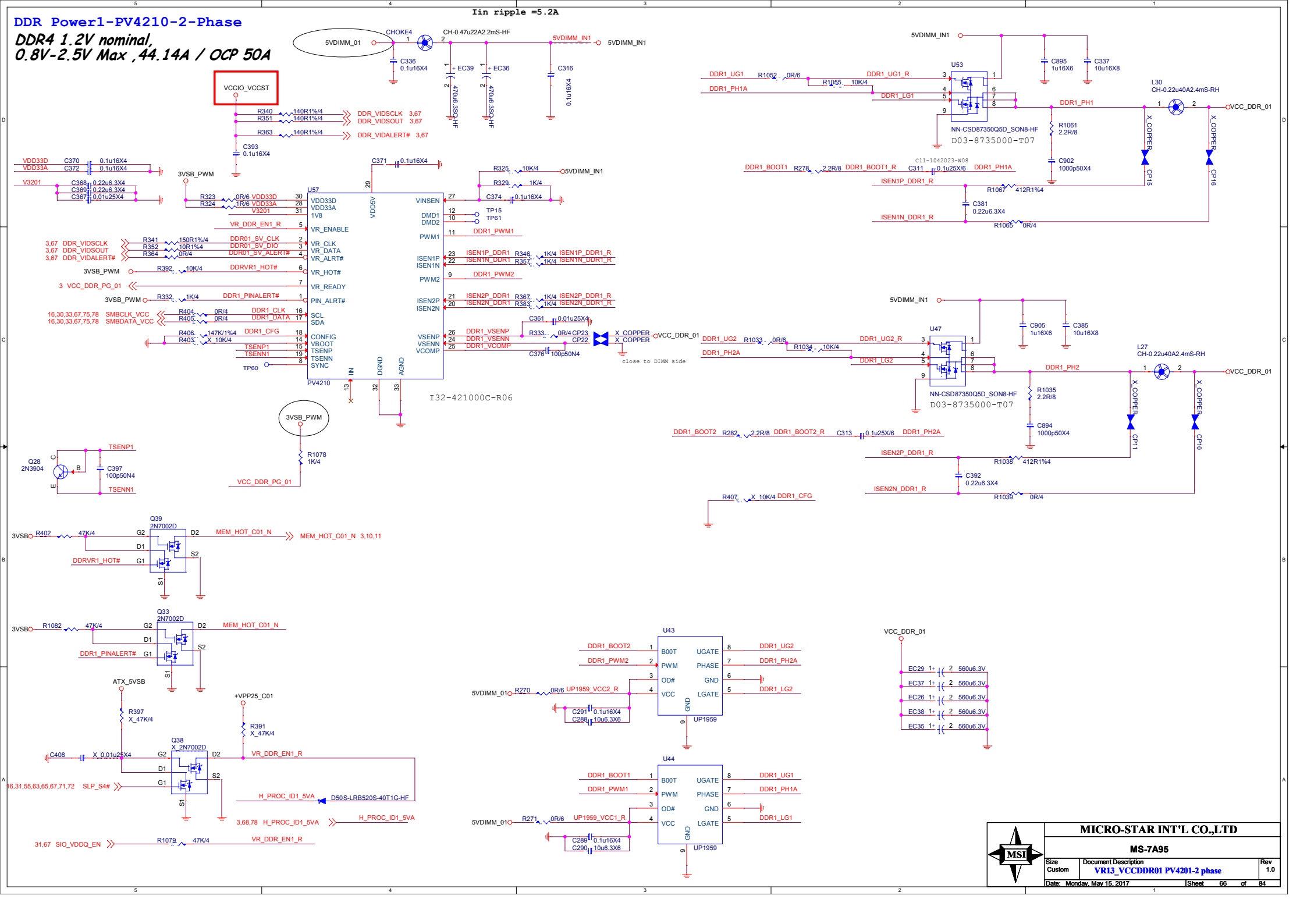
DDR Power1-PV4210-2-Phase

DDR4 1.2V nominal,
0.8V-2.5V Max ,44.14A / OCP 50A

Iin ripple =5.2A



MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size: Custom	Document Description: VR13_VCCDDR01 PV4201-2 phase	Rev: 1.0
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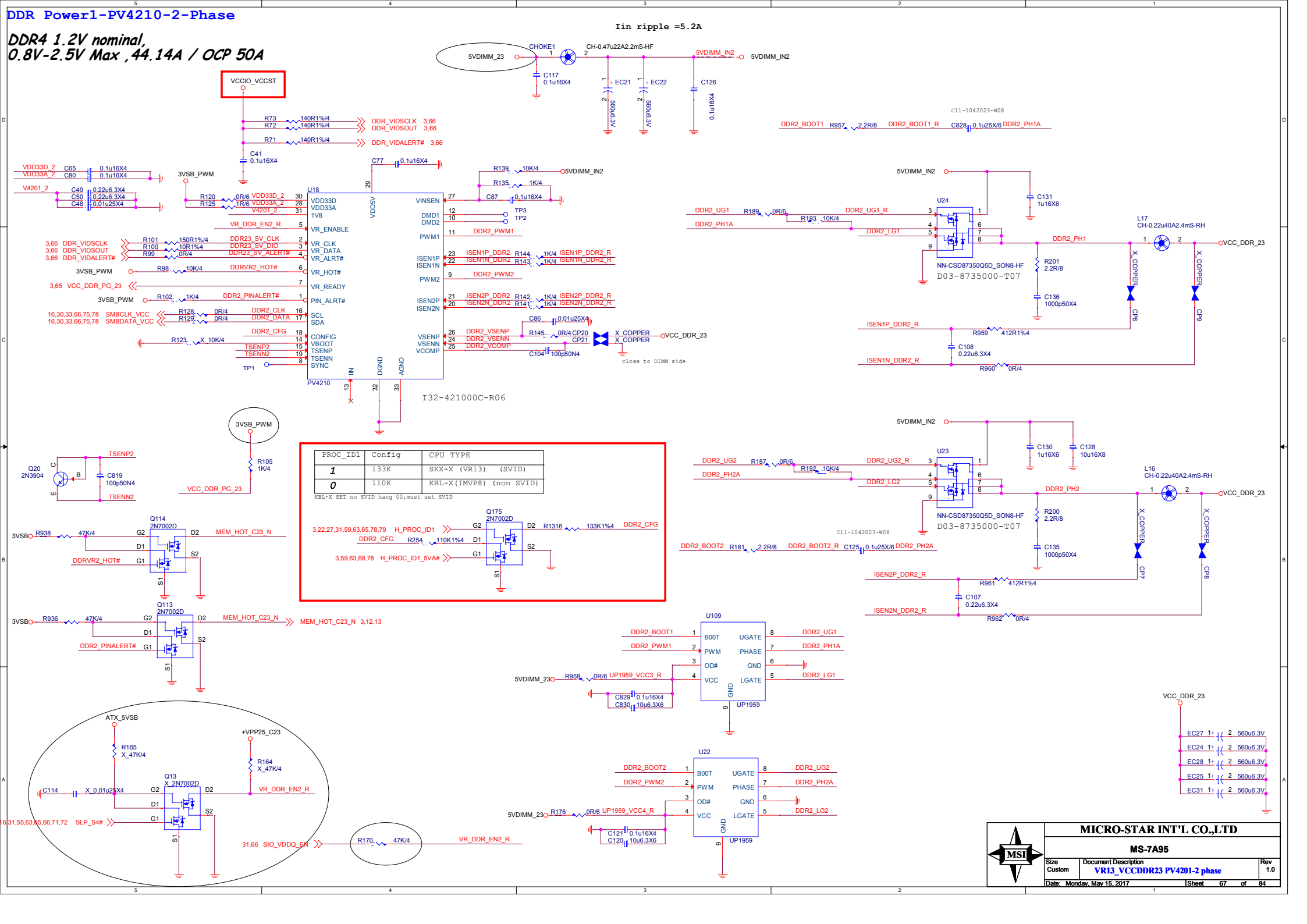
DDR Power1-PV4210-2-Phase

DDR4 1.2V nominal,
0.8V-2.5V Max ,44.14A / OCP 50A

Iin ripple =5.2A



MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: VR13_VCCDDR23 PV4201-2 phase
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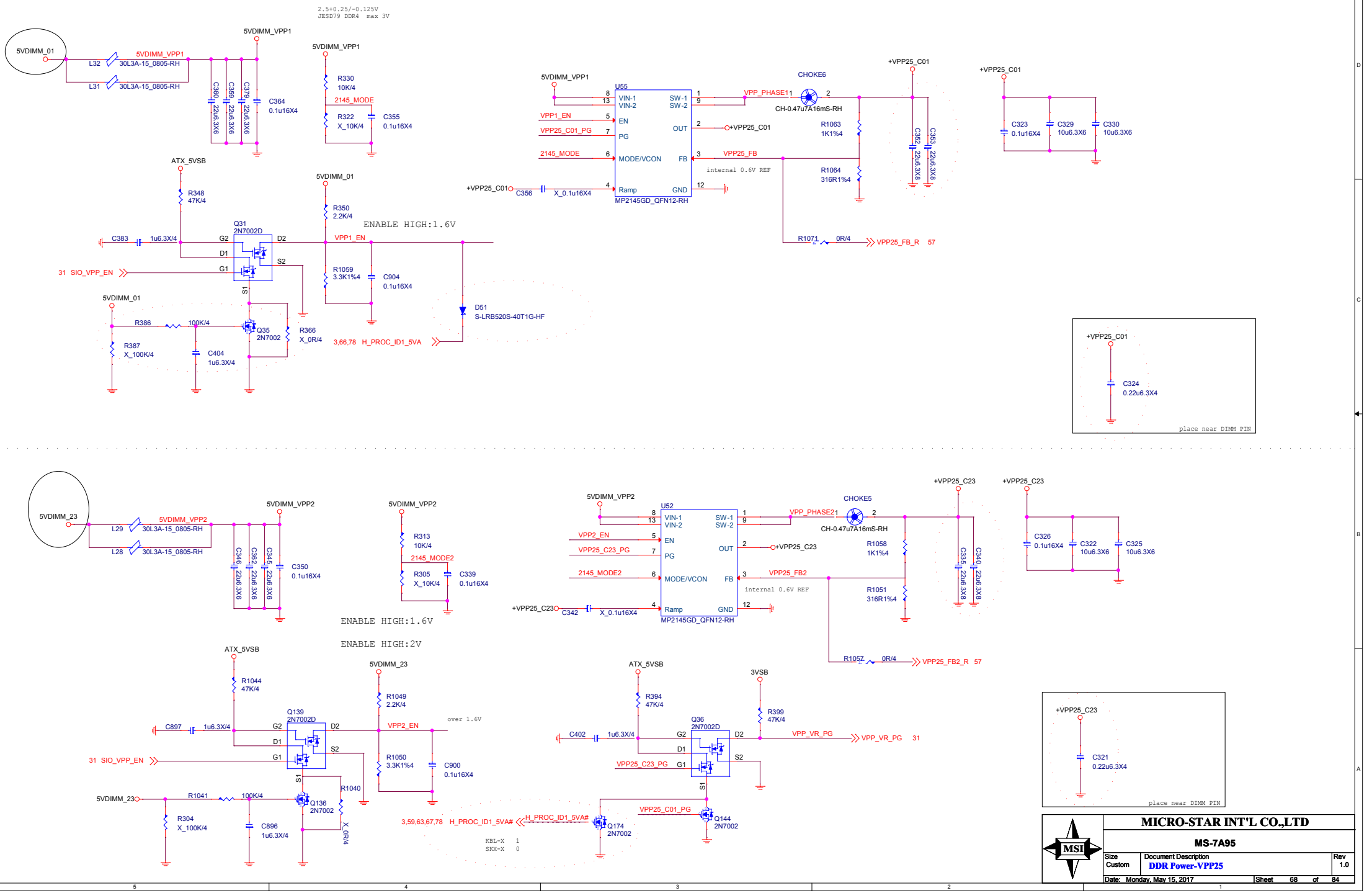
4DIMM :6A FOR DDR VPP



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Size: Custom	Document Description: DDR Power-VPP25	Rev: 1.0
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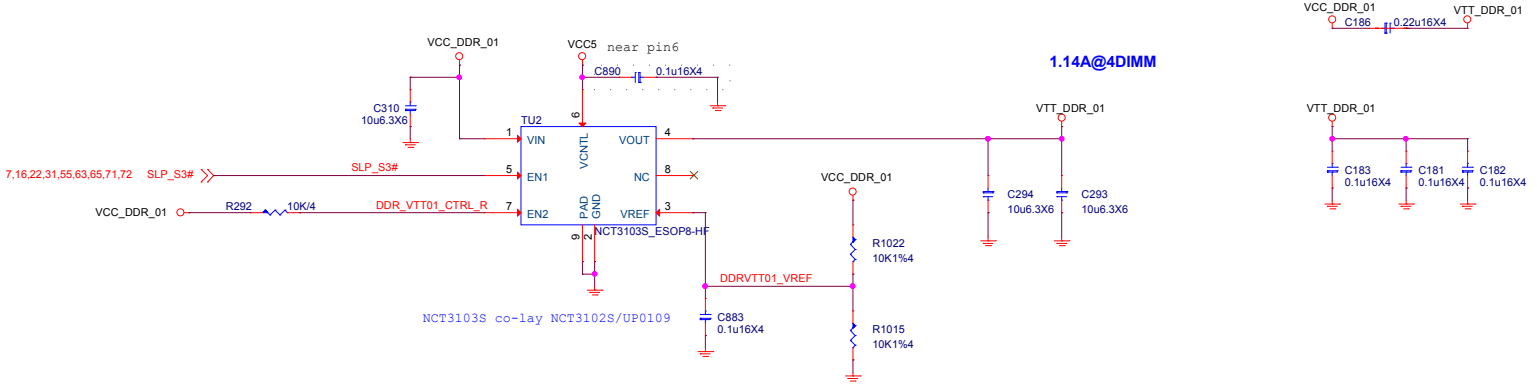
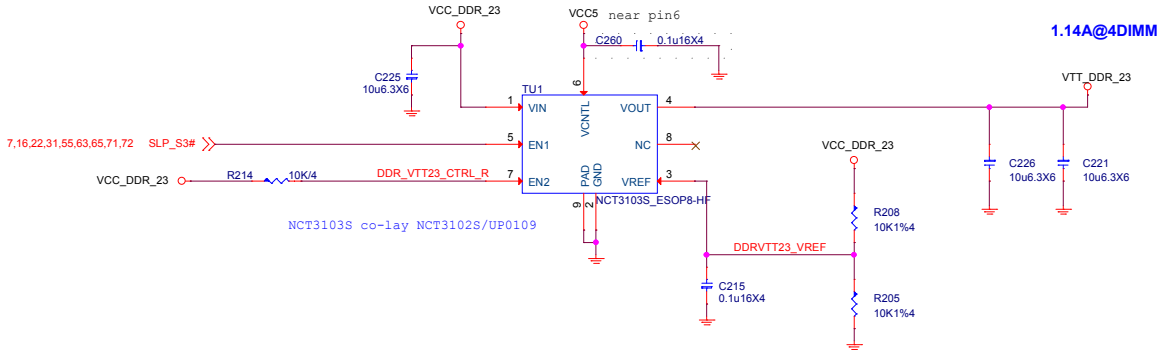
DDR VTT Power

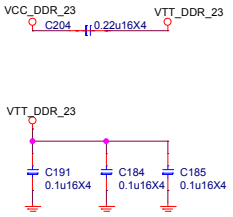
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





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Size: Custom	Document Description: VTTDDR	Rev: 1.0
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PCH_1VSB Power:1.0V,10A

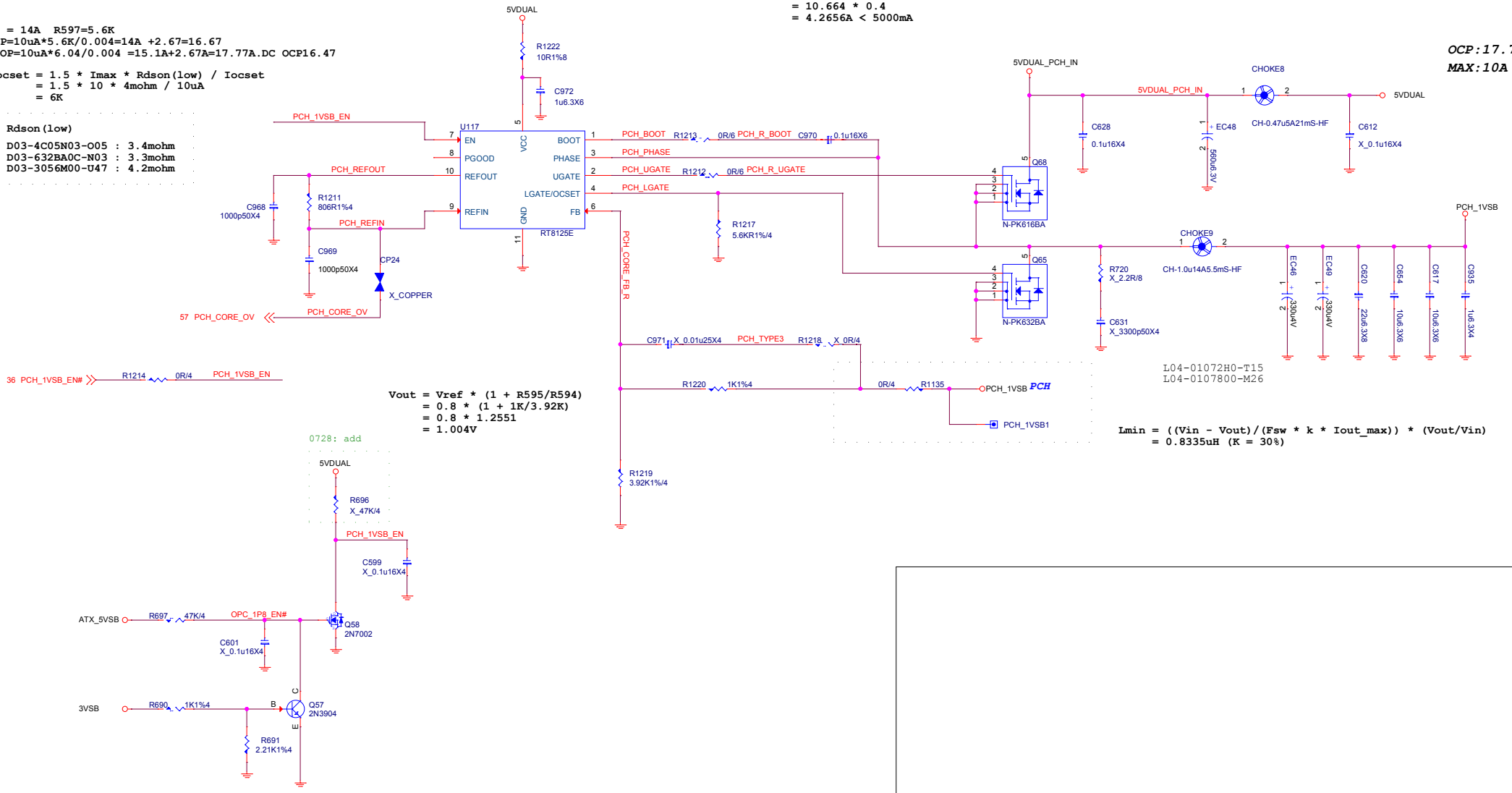
OCP = 14A R597=5.6K
IOCP=10uA*5.6K/0.004=14A +2.67=16.67
*IOOP=10uA*6.04/0.004 =15.1A+2.67A=17.77A.DC OCP16.47

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 10 * 4mohm / 10uA
= 6K

Rdson(low)
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

OCP:17.77
MAX:10A



Vout = Vref * (1 + R595/R594)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V

L04-01072H0-T15
L04-0107800-M26

Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

0728: add

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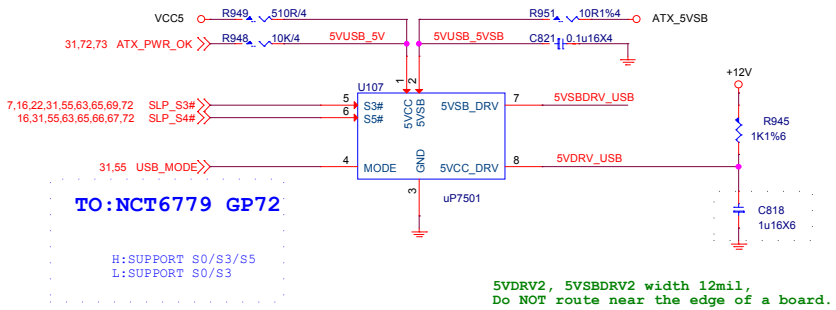
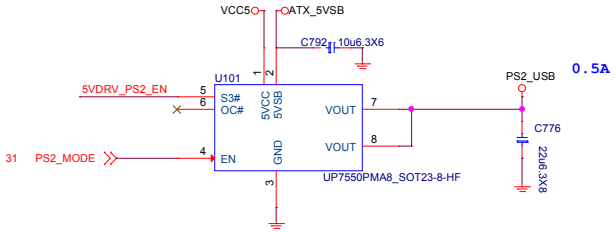
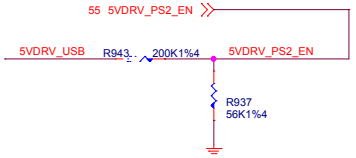
USB POWER



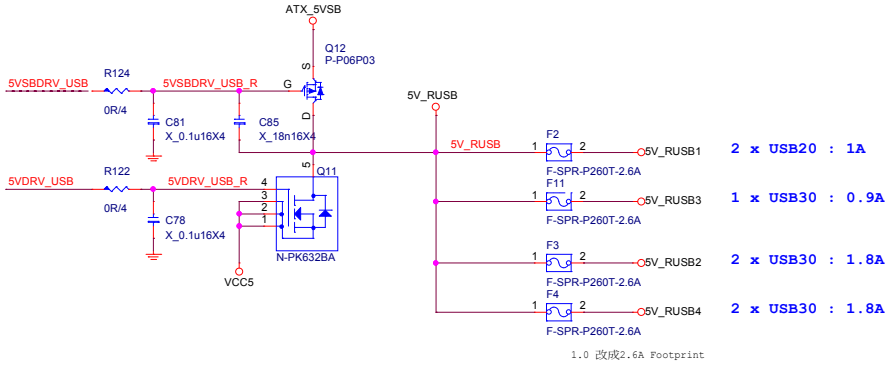
PS2 POWER



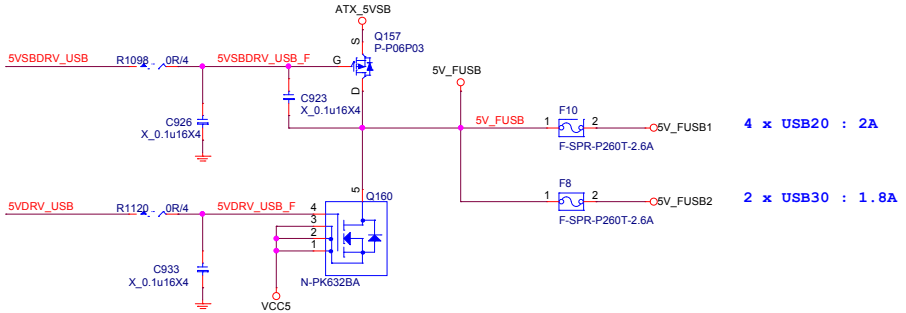
USB MODE



REAR USB PORT POWER



FRONT USB PORT POWER



MICRO-STAR INT'L CO.,LTD

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Custom	USB Power	1.0

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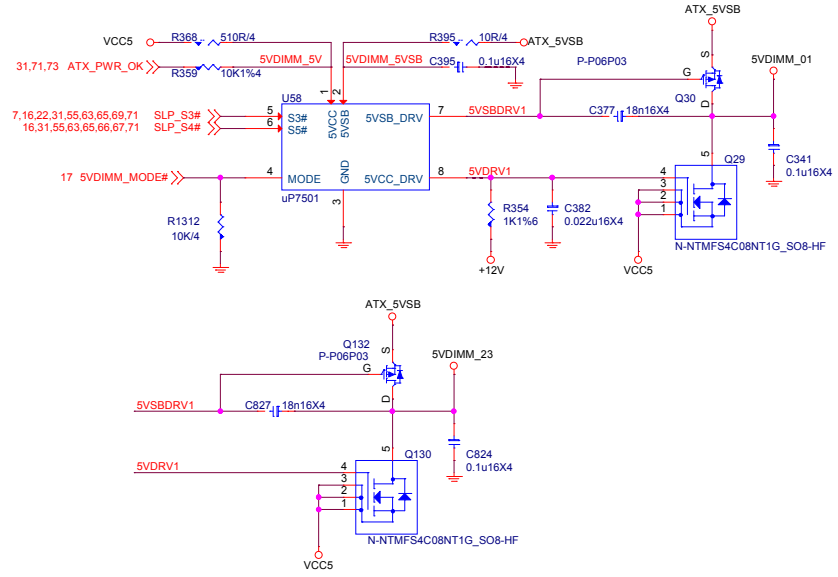
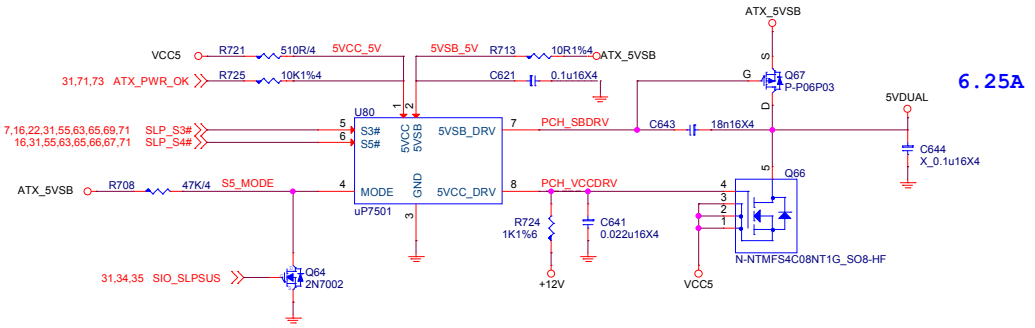
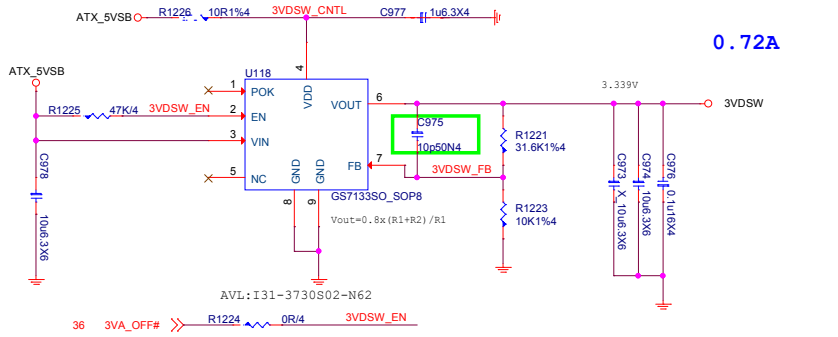
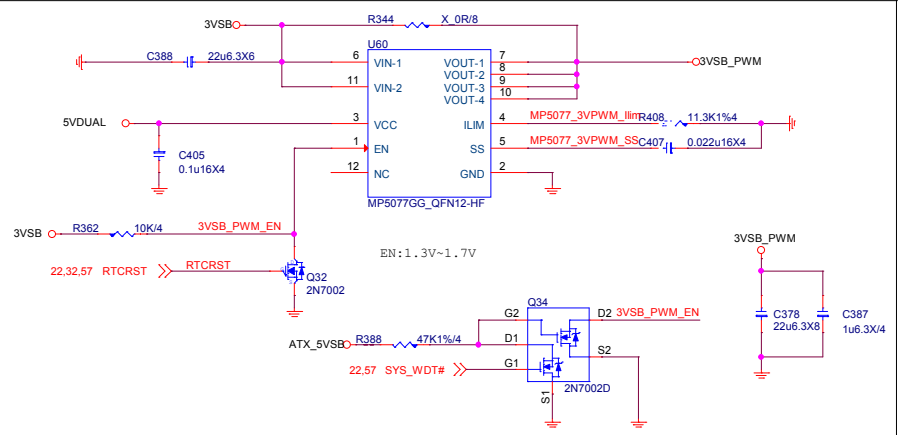
5VDIMM FOR DDR



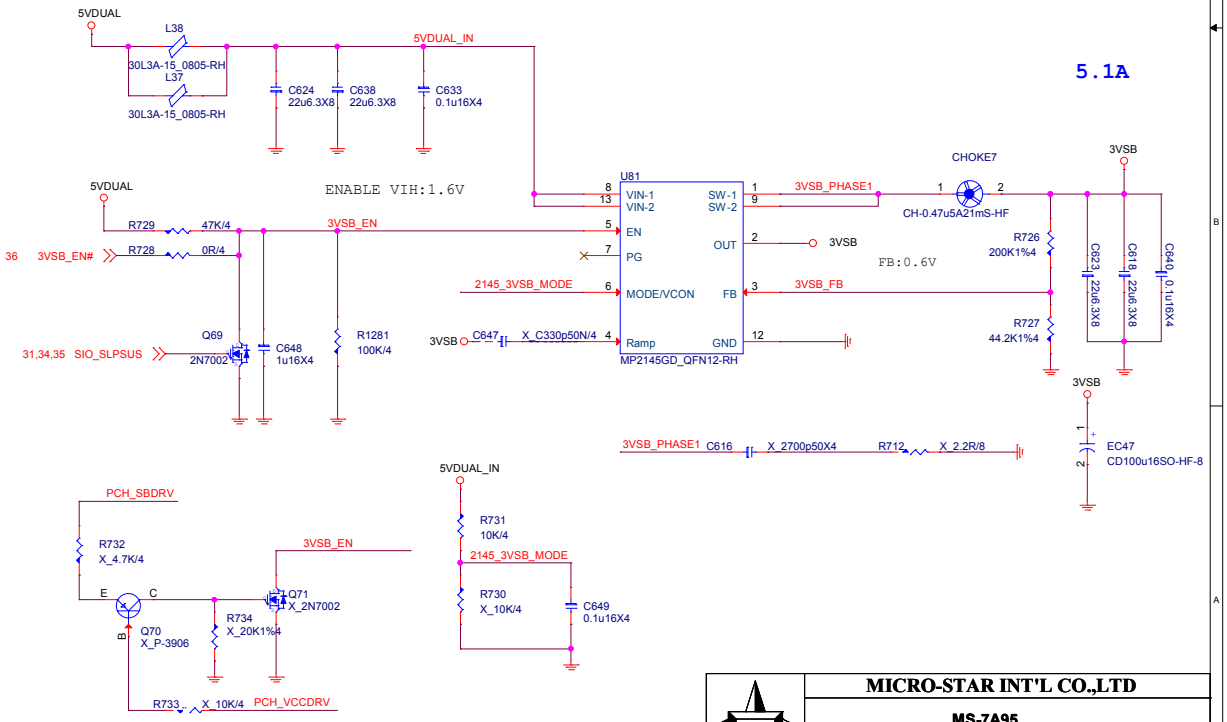


3VDSW





3VSB for OC & Gaming



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MS-7A95		
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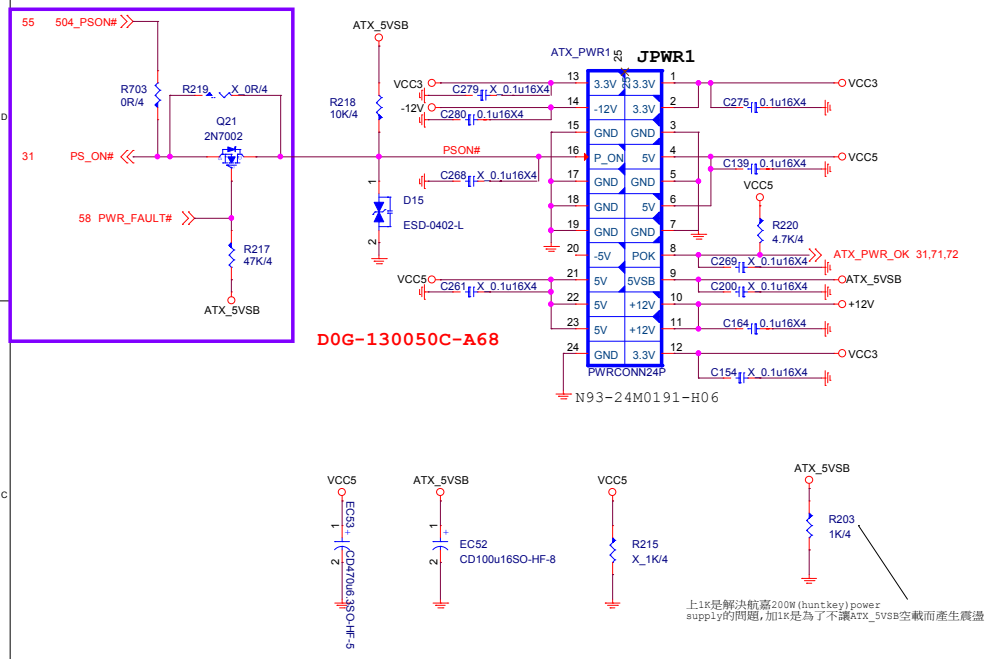
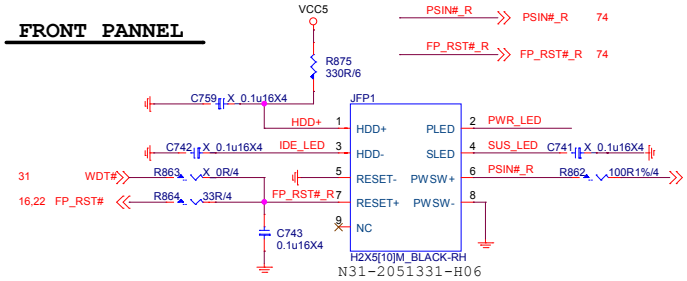
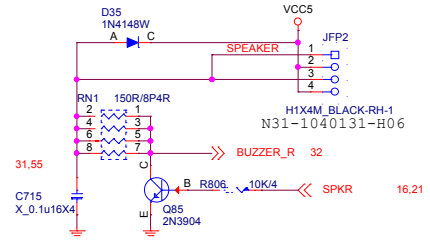
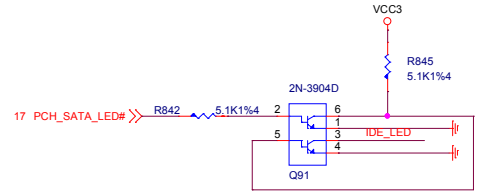
ATX POWER CONNECTOR

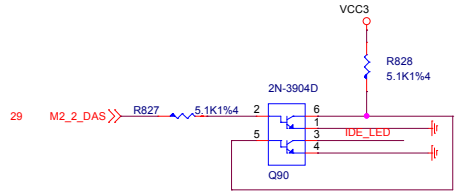


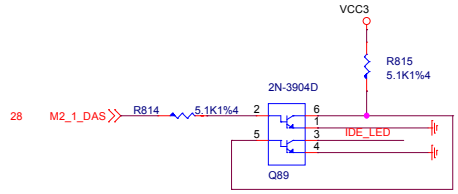
FRONT PANNEL



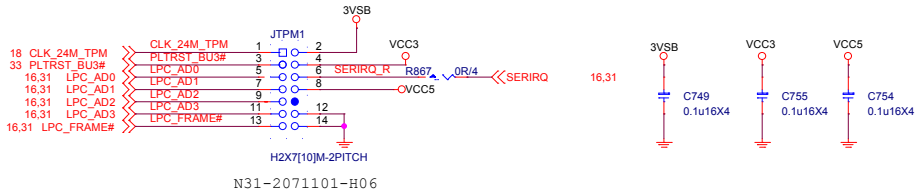




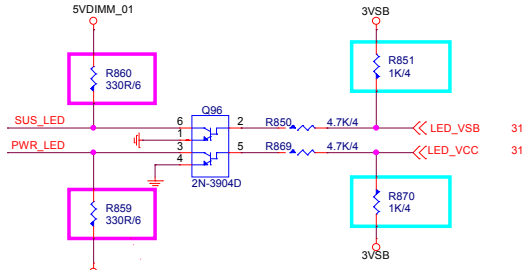




TPM Pin Header



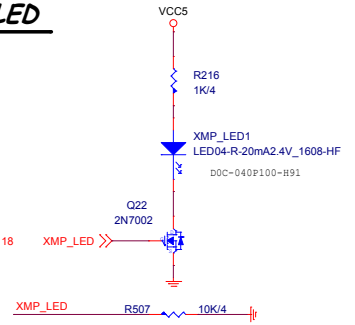
Front Panel LED



Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.

SIO ver. LAA
Push pull pin, no need to stuff resisters.

XMP LED



MICRO-STAR INT'L CO.,LTD	
MS-7A95	
Size: Custom	Document Description: ATX Connector/F_Panel
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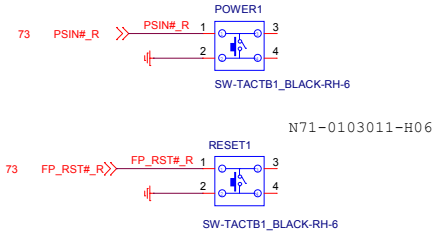
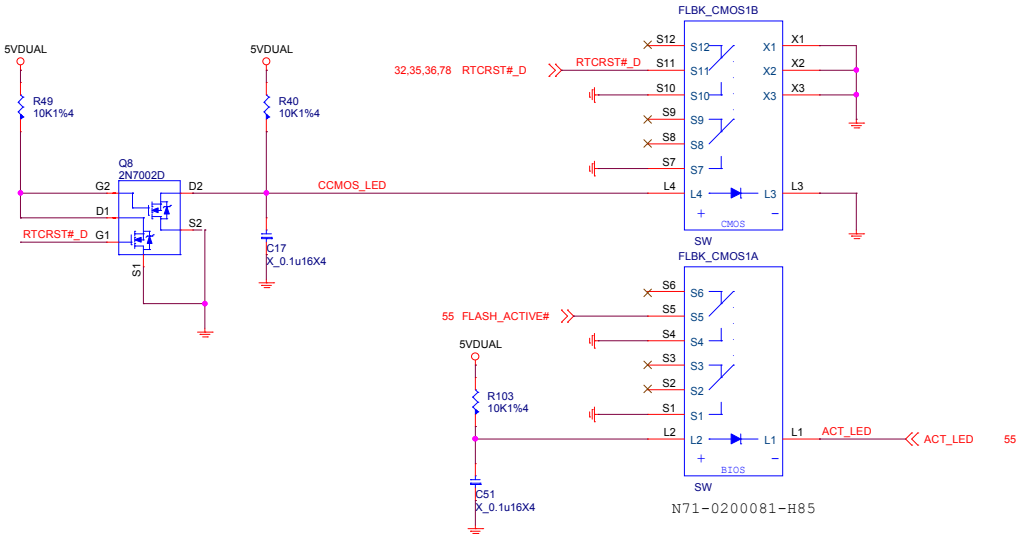
PWR/RST Botton

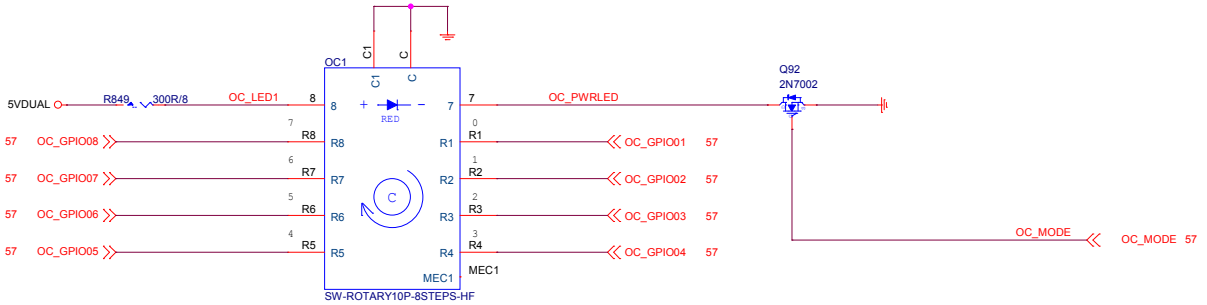


N71-0103011-H06



N71-0200081-H85

OC Genie



N7F-0100121-H06

MICRO-STAR INT'L CO.,LTD		
MS-7A95		
Size: Custom	Document Description: Botton and OC GENIE	Rev: 1.0
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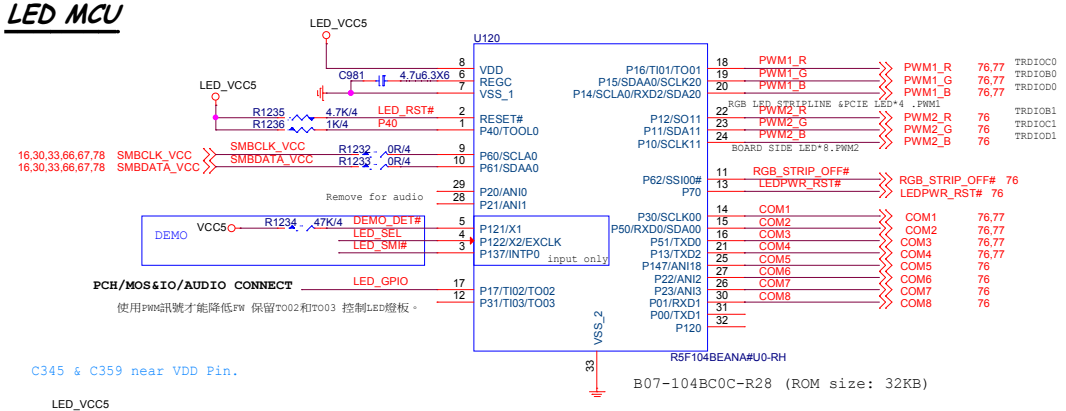
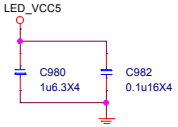
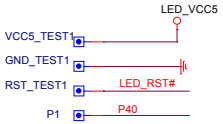
LED MCU

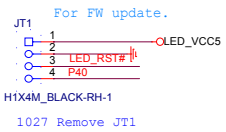


B07-104BC0C-R28 (ROM size: 32KB)

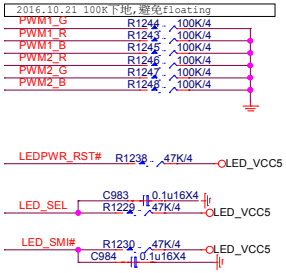
C345 & C359 near VDD Pin.







1027 Remove JT1



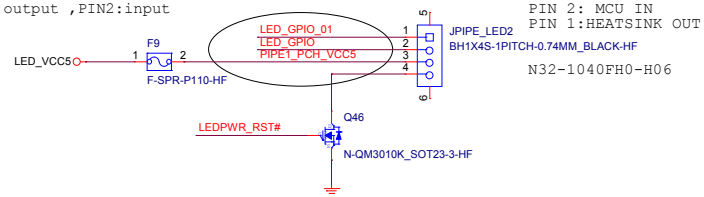
Control	Net Name	PWM USE	Connector
AUDIO Cover	LED_GPIO	No Use	JPIPE_LED1
PCH	LED_GPIO_01	No Use	JPIPE_LED2
MOS/IO cover	LED_GPIO_02	No Use	JPIPE_LED3
LED STRIPLINE	RGB_STRIP_OFF#	PWM1	JLED1
Board Side LED	COM1~8	PWM2	RGB LED
PCIE Side LED	COM1~4	PWM1	RGB LED

1 PCH HEATSINK LED

PCS LED*0.16W=W

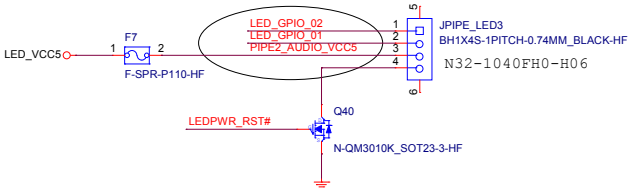
JPIPE:PIN1:output ,PIN2:input

PIN 2: MCU IN
PIN 1:HEATSINK OUT



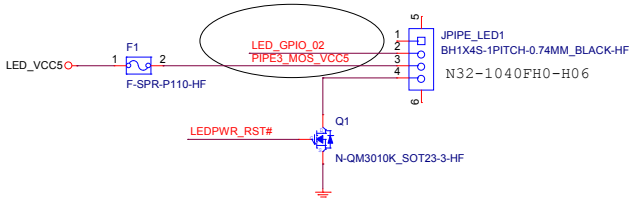
2 AUDIO/IO Cover LED

PCS LED*0.16W=W

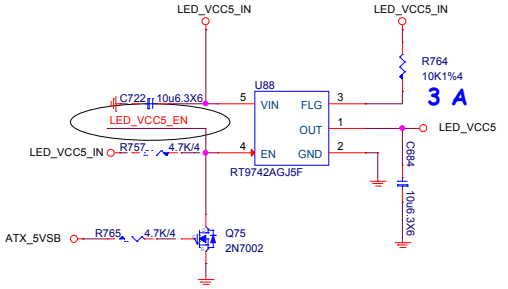


3 MOS HEATSINK LED

PCS LED*0.16W=W

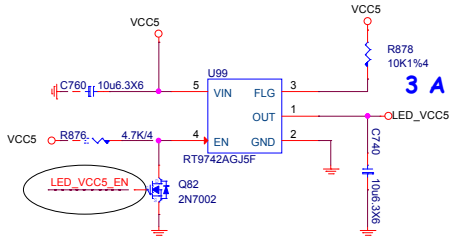


EXTERNAL POWER INPUT

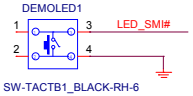


min 80mil.

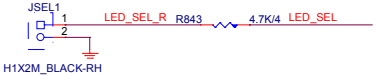
I36-9742A09-R11

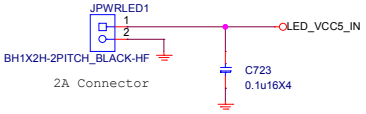


LED Demo Button



N71-0103011-H06





N32-1020CB1-H06

MICRO-STAR INT'L CO.,LTD

MS-7A95

Size: Custom
Document Description: LED MCU Control
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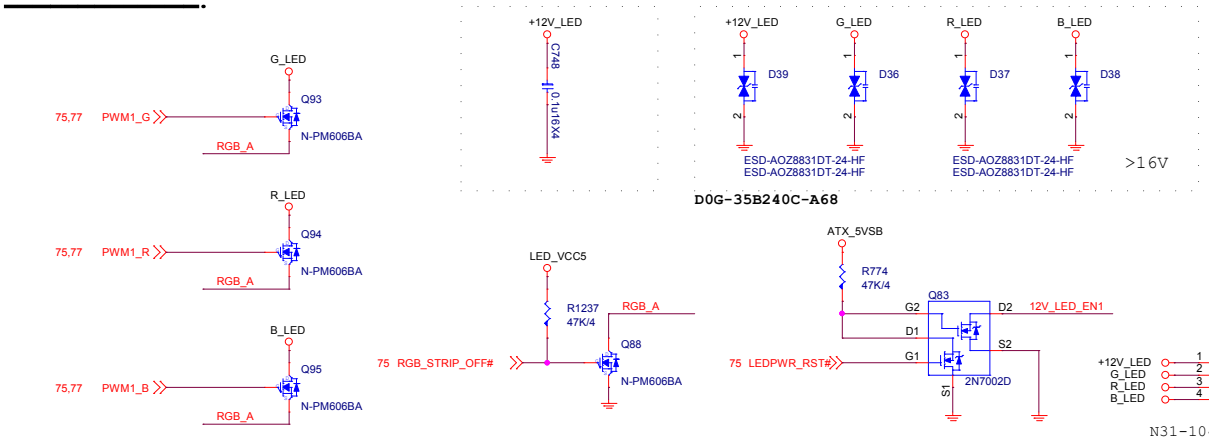
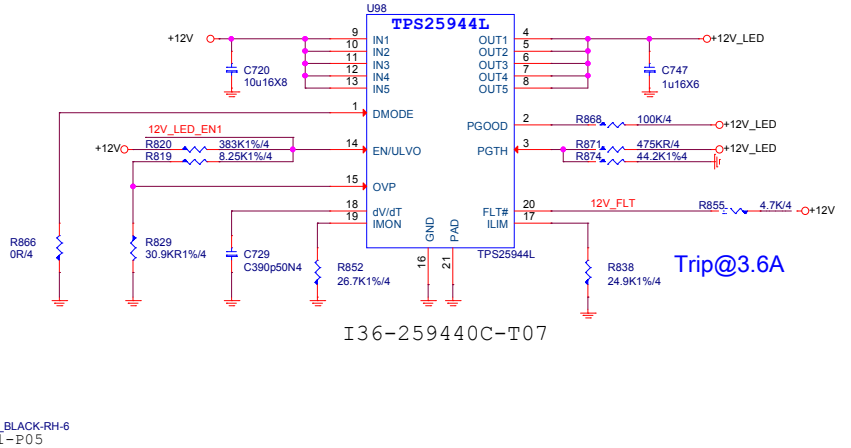
LED STRIPLINE

2016.07.06 only reserve now
2016.08.02 Add +12V_LED 0.1uF2016.08.02 stuff ESD

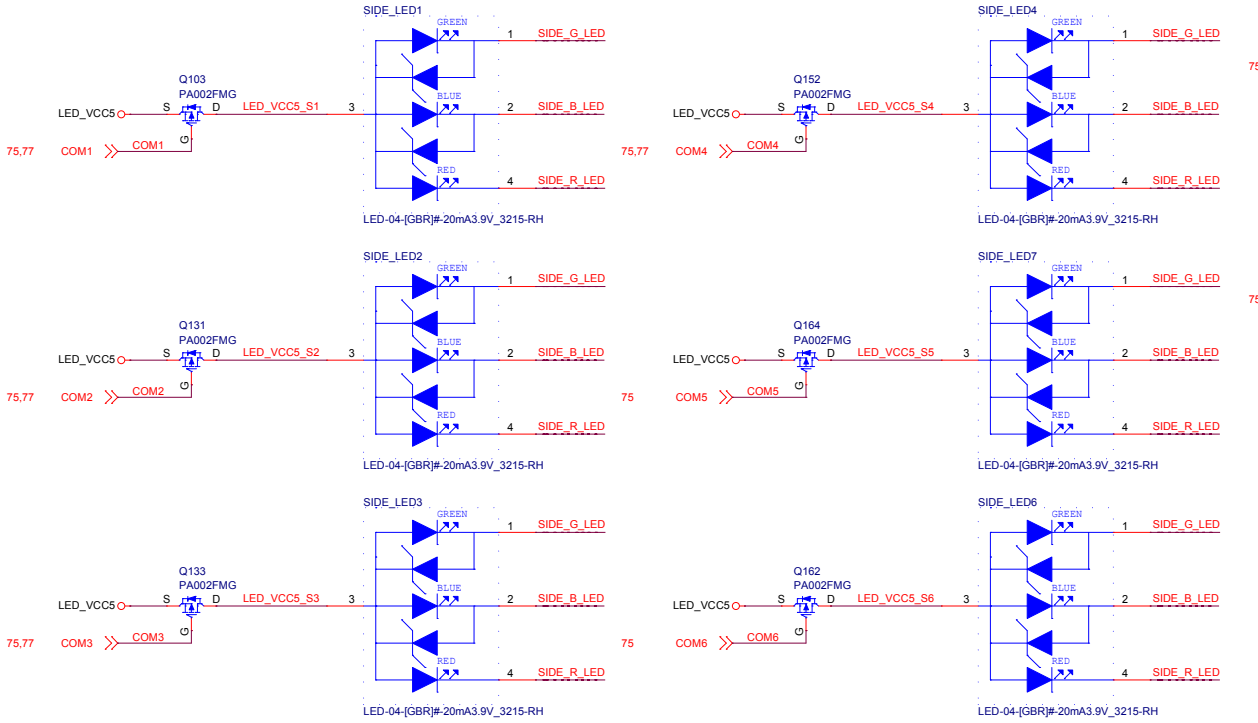


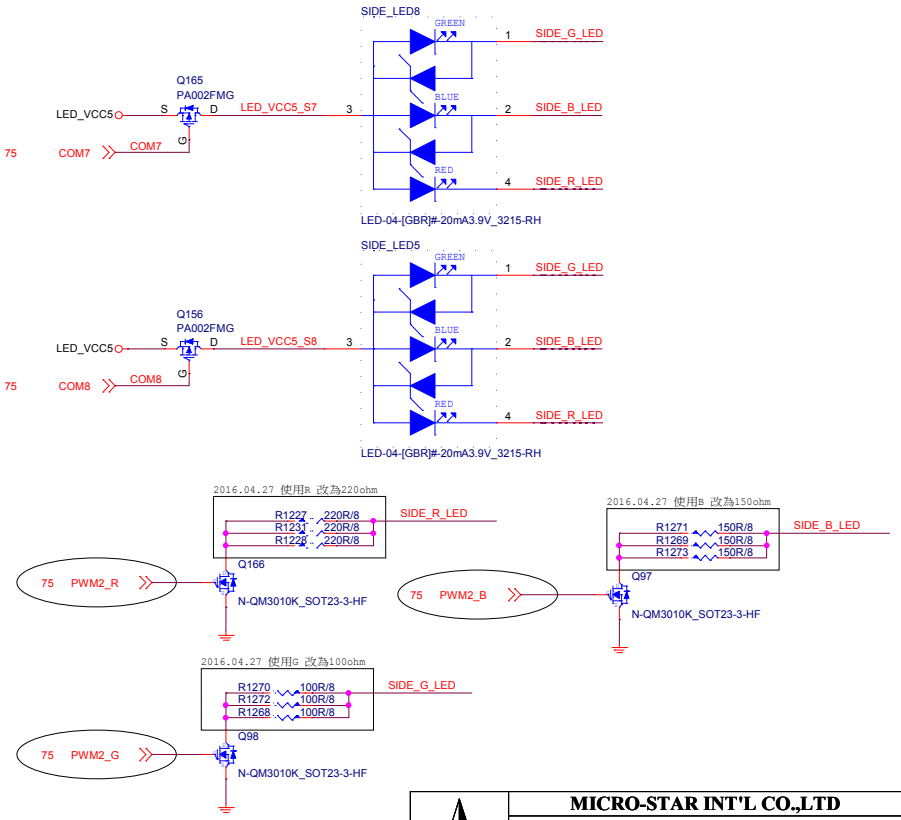


外接LED 燈條 (RGB)
---- PCB 文字面 (JLED1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) ,
長度限制為2公尺 (待7A20驗證)

BOARD SIDE LED *8

D0C-040R700-H91
Forward Current 20mA
Pulse Forward Current 30-60mA





MICRO-STAR INT'L CO.,LTD

MS-7A95

Size	Document Description	Rev
Custom	LED STRIP/BOARD SIDE LED	1.0

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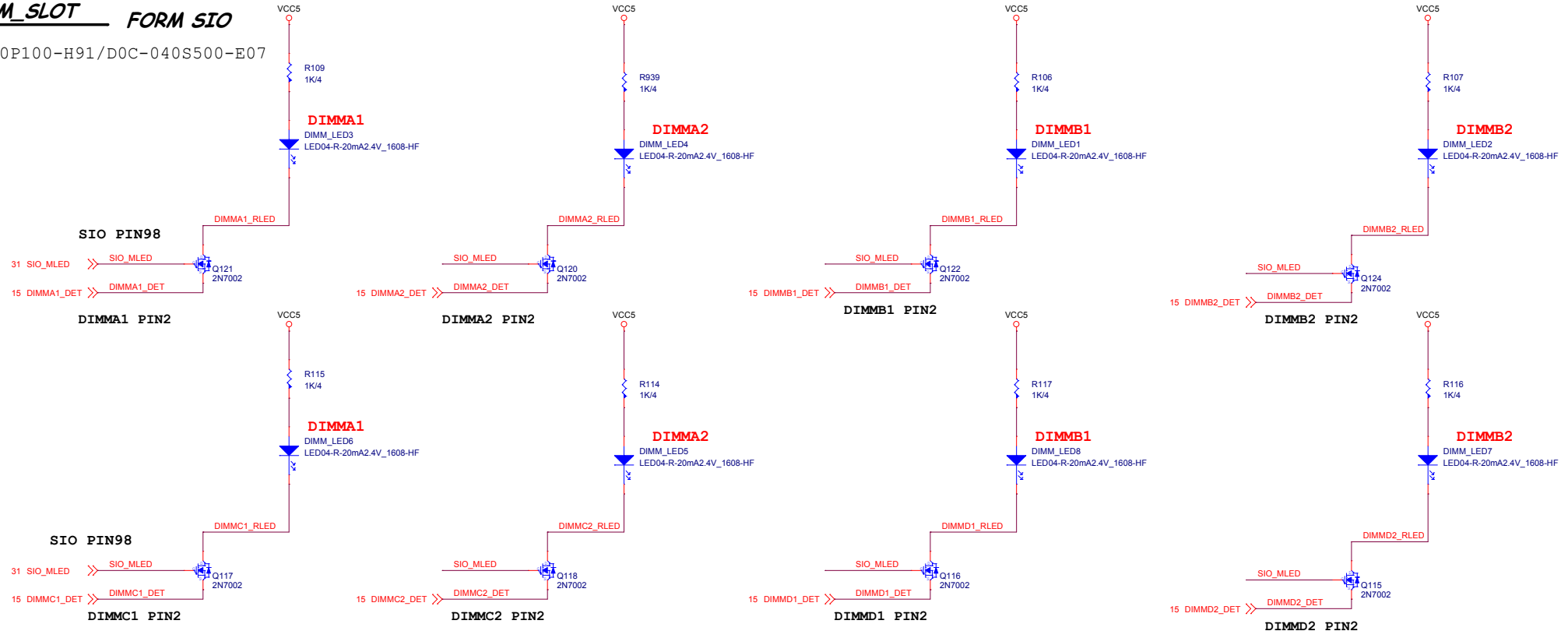
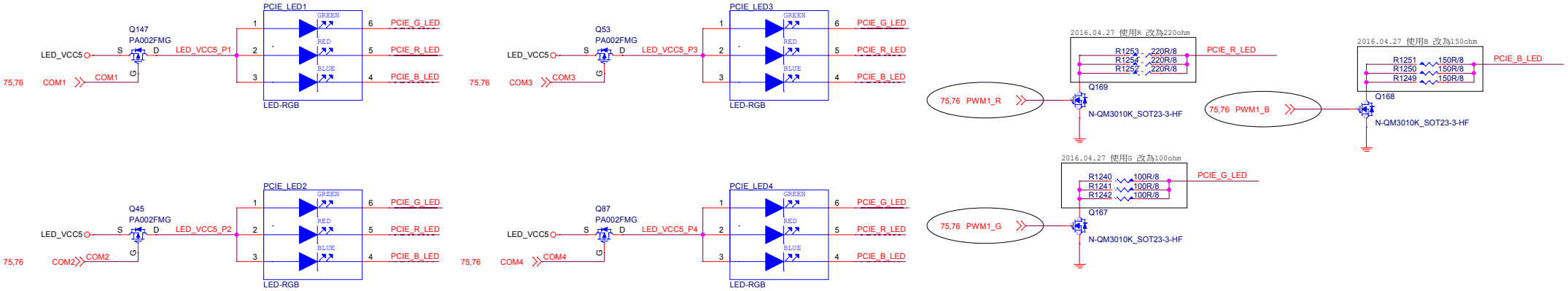
DIMM_SLOT FORM SIO

D0C-040P100-H91/D0C-040S500-E07



PCIE_SLOT LED*4 FORM MCU

D0C-040S400-H91



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A95	
Size: Custom	Document Description: DIMM LED	Rev: 1.0
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SKX:VCCIO
KBX:VCCST

ATX_5VSB
R1389 47K/4
Q204 2N7002D
3,59,63,67,68 H_PROC_ID1_5VA#
H_PROC_ID1_5VA#
G2 D2
D1
S2
G1
3,22,27,31,59,63,65,67,79 H_PROC_ID1
H_PROC_ID1
S1
ATX_5VSB
R1300 47K/4
H_PROC_ID1_5VA 3,66,68
C1039 X_0.1u16X4

VCCIO_VCCST
Q212 N-PM606BA
Q216 N-PM606BA
Q217 N-PM606BA
Q211 N-PM606BA
VCCIO
VCCST
H_PROC_ID1_5VA
H_PROC_ID1_5VA#

PEG_PCIE_SLOT SMBUS SWITCH

MP BOM remove

SKX:PEG
KBX:PCH

U131
16,22,23,55,57,59,63 SMBDATA_VSB
16,22,23,55,57,59,63 SMBCLK_VSB
3 PE_SDA
3 PE_SCL
SMBDATA_VSB 1
SMBCLK_VSB 2
PE_SDA 3
PE_SCL 4
5
1D+ 1D- 2D+ 2D- GND
NCY3956Y
OE# 6
D- 7 PE_SCL_SW PE_SCL_SW 23
D+ 8 PE_SDA_SW PE_SDA_SW 23
S 9 H_PROC_ID1
VCC 10 3VSB
11 C1041 X_0.1u16X4
X_NCT3958Y_DFN10-HF

OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

VCC3
R1414 X_1K/4 PE_SCL
R1417 X_1K/4 PE_SDA
R1424 X_1K/4 PE_SCL_SW
R1442 X_1K/4 PE_SDA_SW

DDR23_RESET SWITCH

SKX:PEG
KBX:PCH

3,59,63,67,68 H_PROC_ID1_5VA#
D53 S-LRB520S-40T1G-HF
R1422 4.7K/4
3VSB
C1040 0.1u16X4
VCC_DDR_23
3 DDR_RESET_C23_N
12,13 DIMM23_RESET#
R1301 X 470R1%4
R1308 0R/4
R1411 0R/4
U130
1OE_N VCC
1A 2OE_N
1B 2B
GND 2A
SN74CB3Q3306APWR_TSSOP8-RH
3VSB
H_PROC_ID1
R1302 0R/4 DIMM23_RESET#
R1303 0R/4
R1304 470R1%4
DRAM_RESET# 16
VCC_DDR_23
R1438 X 470R1%4
C995 X_0.1u16X4
DDR_RESET_C23_N R1413 X 0R/4 DIMM23_RESET#

DIMM_SLOT SMBUS SWITCH

SKX:PEG
KBX:PCH

U132
16,30,33,66,67,75 SMBDATA_VCC
16,30,33,66,67,75 SMBCLK_VCC
12 DDR_SDA_C23
12 DDR_SCL_C23
SMBDATA_VCC 1
SMBCLK_VCC 2
DDR_SDA_C23 3
DDR_SCL_C23 4
5
1D+ 1D- 2D+ 2D- GND
NCY3956Y
OE# 6
D- 7 DDR_SCL_C23_SW DDR_SCL_C23_SW 12,13
D+ 8 DDR_SDA_C23_SW DDR_SDA_C23_SW 12,13
S 9 H_PROC_ID1
VCC 10 3VSB
11 C1042 0.1u16X4
NCT3958Y_DFN10-HF
VCC3
R1443 X 1K/4 DDR_SCL_C23_SW
R1447 X 1K/4 DDR_SDA_C23_SW

OE#	S	D+	D-	Function
H	X	Hi-Z	Hi-Z	Disable
L	L	1D+	1D-	D=1D
L	H	2D+	2D-	D=2D

MCU For PWM

VCC3 R1407 X 0R/4
3VSB R1408 0R/4
LPC812_VDD
C1015 1u6.3X4
U122
LPC812
VDD 12
RESET#/PIO0_5 3
PIO0_4/WAKEUP/TRST# 4
PIO0_1/ACMP_I2/CLKIN/TDI 9
PIO0_0/ACMP_I1/TDO 16
SWCLK/PIO0_3/TCK 5
SWDIO/PIO0_2/TMS 6
PIO0_6/VDDCMP 15
VSS 13
PIO0_7 14
PIO0_10 8
PIO0_11 7
PIO0_12 2
PIO0_13 1
PIO0_8/XTALIN 11
PIO0_9/XTALOUT 10
LPC812
LPC812_RST
USART_TXD
ID1_MCU
USART_RXD
LPC812_TCK
LPC812_TMS
MCU_CLRMOS
3,22,27,31,59,63,65,67,79 H_PROC_ID1
R1412 100R/4
R1390 4.7K/4
+12V R1397 47K/4
Q196 2N7002
R1305 47K/4
SMBUS_ON
R1408 1K/4
Slave
SMBCLK_812 0R/4 R1401
SMBDATA_812 0R/4 R1398
ISP_ENTRY_MOSI
MCU_TEST
SMBCLK_VSB 16,22,23,55,57,59,63
SMBDATA_VSB 16,22,23,55,57,59,63
Master
SMCLK_MCU
SMDATA_MCU
SMCLK_MCU R1404 4.7K/4
SMDATA_MCU R1405 4.7K/4
USART_RXD R1406 47K/4
LPC812_VDD
SPI_SW_SEL 34,55
MCU_CLRMOS
Q208 2N7002
SIO_3VA_EN 32
Q209 2N7002
RTCRST#_D 32,35,36,74
Q206 X_2N7002
R1447 1K/4
3,31 CPU_SKTOCC# R550 10K/4
Q205 2N7002

Q197 2N7002D
SMBUS_ON G2 D2 SMBCLK_VSB
SMBDATA_VSB D1 S2 SMCLK_MCU
SMBUS_ON G1
S1
SMDATA_MCU

Q198 2N7002D
SMBUS_ON G2 D2 SA_EN SA_EN 63
63 VCCIO_EN VCCIO_EN D1
SMBUS_ON G1 S2
S1

PCH
MASTER
SMBUS_0
MCU
SLAVE MASTER
SMBUS_ON
SMBUS_1
SW
Slave Device

LPC812_VDD
R1423 47K/4
J1
1 MCU_TEST
2
C1029 0.1u16X4
H1X2M_BLACK-RH

58,59 VRD_EN
VRD_EN
SMBUS_ON
Q199 2N7002

LPC812_VDD
R1410 10K/4
JISP1
1 ISP_ENTRY
2
R1457 1K/4 ISP_ENTRY_MOSI
H1X2M_BLACK-RH
N31-1020151-H06
DA8 X_ESD-0402-L

SMBUS_ON
PWM1 (IR35201)
VRD_EN
PWM2 (IR35204)
VCCIO_EN
SA_EN

JTAG for SW DEBUG

MP BOM remove

LPC812_VDD
R1395 100K/4
C1038 0.1u16X4
JTAG1
LPC812_RST
LPC812_TMS
LPC812_TCK
R1403 4.7K/4
R1400 4.7K/4
X_H1X4M_BLACK-RH-1

LPC812_VDD
R1391 20K/4
R1415 4.7K/4 USART_TXD
JB1
H1X3M_BLACK-RH-3
USART_RX
USART_TX
R1306 100R/4 USART_RXD
R1307 100R/4 USART_TXD

燒錄CONNECT

USART_TXD
DA9 X_ESD-0402-L
USART_RXD
DA10 X_ESD-0402-L

MSI
MICRO-STAR INT'L CO.,LTD
MS-7A90
Size Custom
Document Description SKX/KBX SWITCH
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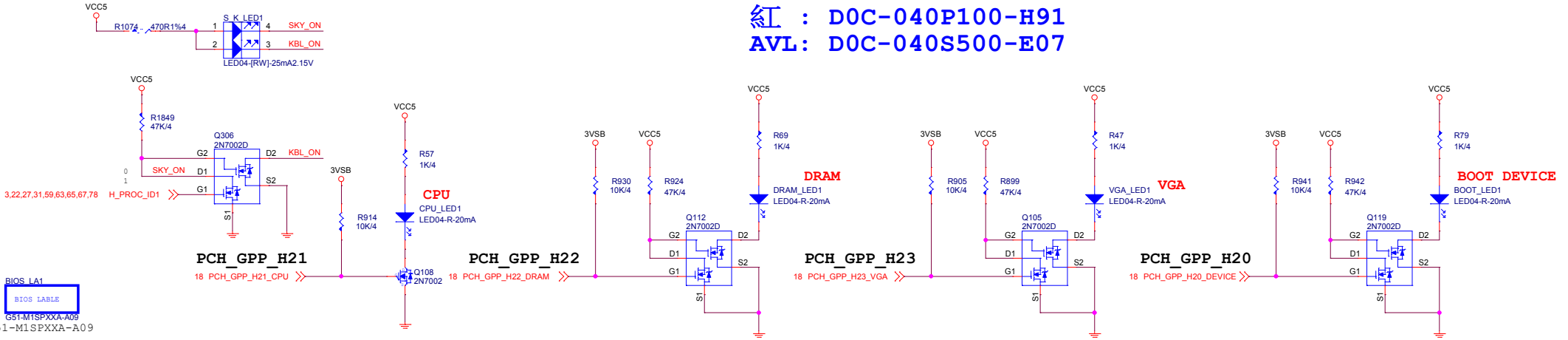
LED
紅 : D0C-040P100-H91
AVL: D0C-040S500-E07



GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，4個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED滅掉。
5. 因此最後正常順利開機後，四個LED燈都是滅掉的。
（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

BIOS_LA1
BIOS LABLE
G51-M1SPXXA-A09
G51-M1SPXXA-A09

SLI1
Label
VIRTUAL
Y01-RNVIDIL-000

SSE1
Label
VIRTUAL
Y02-MA00101-SSE

XSPLT1
Label
VIRTUAL
Y02-MA00401-XSP

NAHIMIC1
Label
VIRTUAL
Y02-MU00100-NAH

CFOS1
Label
VIRTUAL
Y02-MU00170-CFO

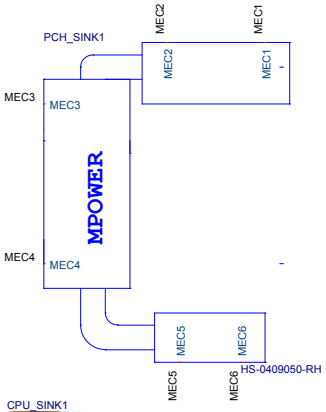
MKT1
Label
VIRTUAL
G51-M1SPL72-Q13

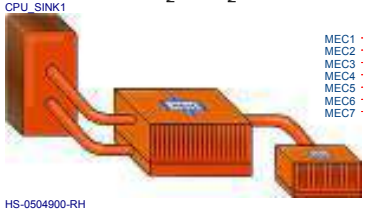
M2_COVER1
M2 Cover
M2_COVER1
E31-0001400-A87

M2_COVER2
M2 Cover
M2_COVER2
E31-0001390-A87

VR_COVER1
VR Cover
X1
X2
E21-7A63020-RH
E21-7A63020-A91

E31-0409050-A87





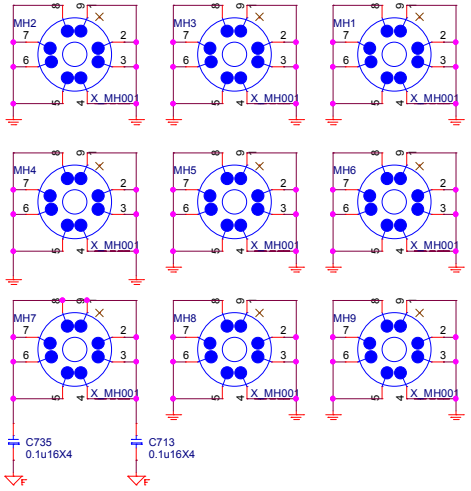
E31-0504900-A87

CPU_H1
CPU 鐵座
CPU_ILM1
E21-7A95020-L06
AVL:E21-7A95-050-F02

CPU_H2
CPU 鐵座
X_CPU_BP1

CHOKE_COVER1
CHOKE Cover
X1
X2
X_CHOKE_COVER

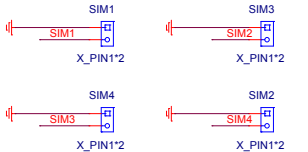
Mounting Holes



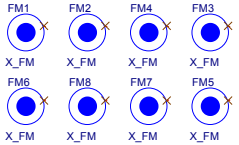
BAT1_X1
BAT-CR2032

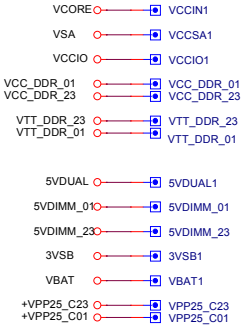
PCB1
7A95_11
PD0-07A9511-G37

Simulation



Optical Fiducial Marks-120





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Size	Document Description	Rev
Custom	Manual Parts	1.0

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