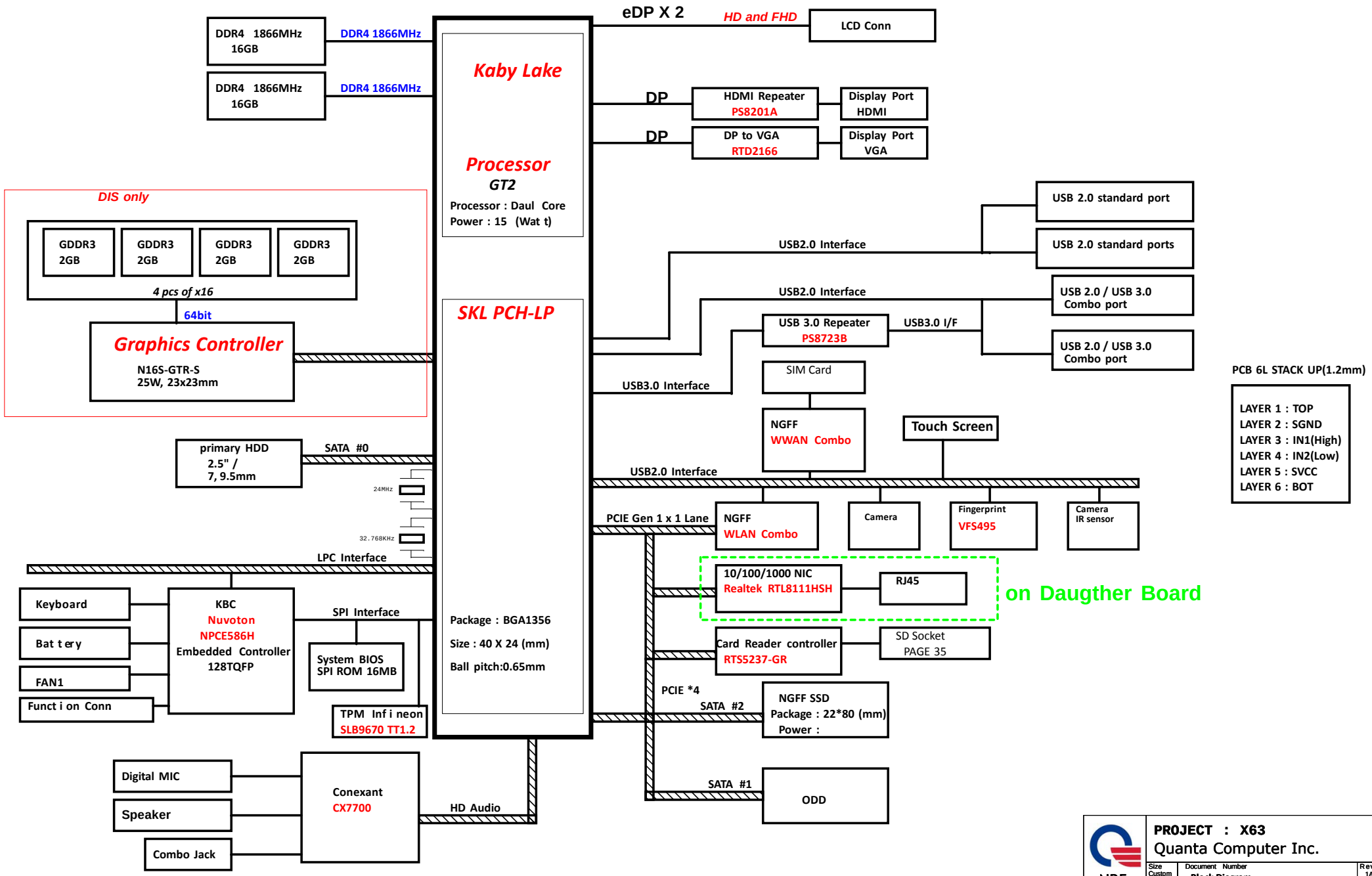
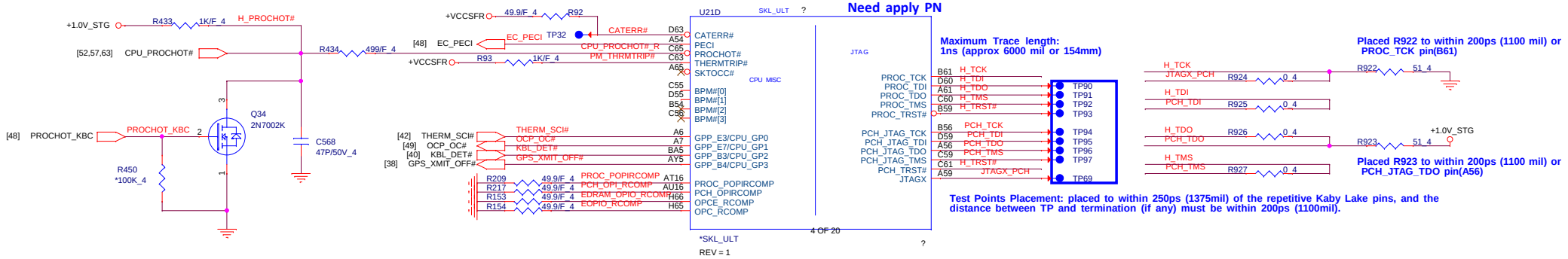
2015 400 series Kaby Lake 15"/ 17" (UMA/DIS) Block Diagram 01



NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: Block Diagram	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 1 of 67	



Need apply PN

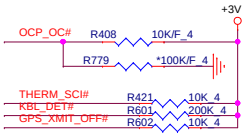
Maximum Trace length: 1ns (approx 6000 mil or 154mm)

Placed R922 to within 200ps (1100 mil) or PROC_TCK pin(B61)

Placed R923 to within 200ps (1100 mil) or PCH_JTAG_TDO pin(A56)

Test Points Placement: placed to within 250ps (1375mil) of the repetitive Kaby Lake pins, and the distance between TP and termination (if any) must be within 200ps (1100mil).

Processor pull-up (CPU)



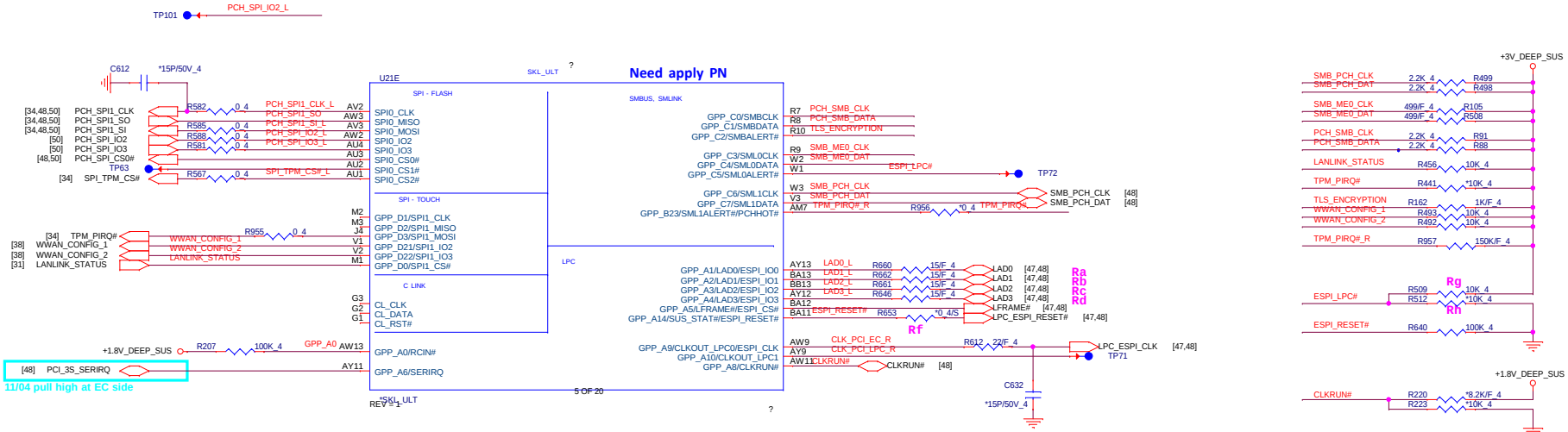
+1.0V_STG [11,13]
+VCCSFR [3,9,11,13,48]
+3V [3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

NB5

PROJECT : X63
Quanta Computer Inc.

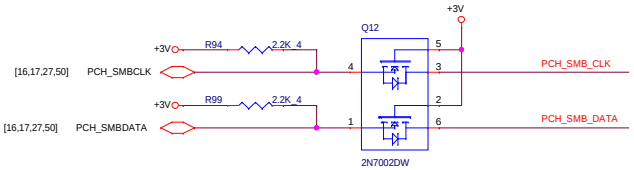
Size	Document Number	Rev
Custom	02 -- SKYLAKE 2/20(MISC/ JTAG)	1A

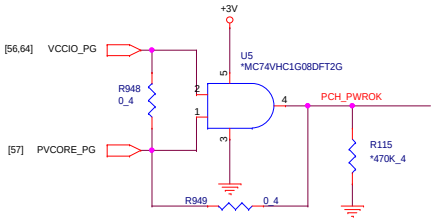
Date: Thursday, May 19, 2016 | Sheet 2 of 67



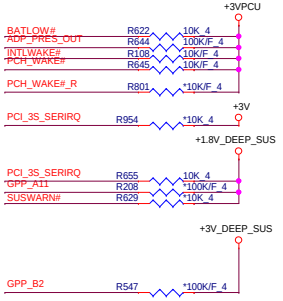
LPC & ESPI TABLE			
		LPC MODE	ESPI MODE
R660	Ra	0Ω	15Ω
R662	Rb	0Ω	15Ω
R661	Rc	0Ω	15Ω
R646	Rd	0Ω	15Ω
R653	Rf	UNINSTAL	INSTAL
R509	Rg	UNINSTAL	INSTAL
R512	Rh	INSTAL	UNINSTAL

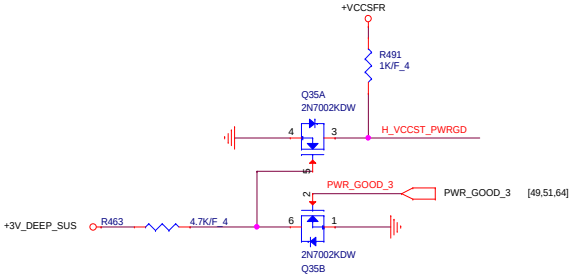
DDR/DRAM/GPU/XDP

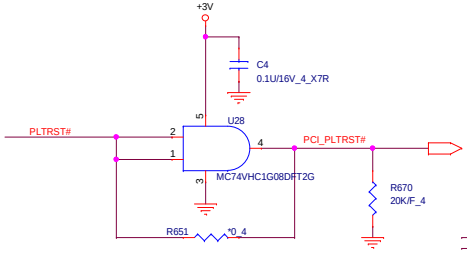




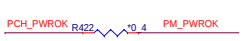
PCH Pull-high/low(CLG)







System PWR_OK(CLG)



+3V_DEEP_SUS [4,5,6,8,10,37,43,47,48,50,56,59,64]
+3VPCU [10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
+3V_ALW [9,41,51,52,53,59,63,64,67]
+3V [2,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59]
+VCCSFR [2,9,11,13,48]
+3V_RTC [9,10,48]

Skylake (GPIO)

04

Need apply PN

U21F — SKL_ULT ?

LPSS

NFC_DWL_REQ	AN8	GPP_B15/GSPI0_CS#
GPP_B16	AP7	GPP_B16/GSPI0_CLK
TP20 / [46] CR_RST#	AP8	GPP_B17/GSPI0_MISO
[26] IR_ENABLE	AR7	GPP_B18/GSPI0_MOSI
CAMERA_ON	AM5	GPP_B19/GSPI1_CS#
[26] CAMERA_ON / [47,49] NMI_SMI_DBG#	AN7	GPP_B20/GSPI1_CLK
NFC_HOST_INT	AP5	GPP_B21/GSPI1_MISO
BOOT_SPI#	AN5	GPP_B22/GSPI1_MOSI
[47] UART0_RXD	AB1	GPP_C8/UART0_RXD
[47] UART0_TXD	AB2	GPP_C9/UART0_TXD
[24] FPR_LOCK#	W4	GPP_C10/UART0_RTS#
UART0_CTS# / TP54	AB3	GPP_C11/UART0_CTS#
FPR_OFF	AD1	GPP_C20/UART2_RXD
[24] FPR_OFF / HDD_HALTLED	R530 1K/F_4	AD2 GPP_C21/UART2_TXD
[50] HDD_HALTLED / [36] ACCEL_INT	AD3	GPP_C22/UART2_RTS#
RUNSCI_EC# / TP136	AD4	GPP_C23/UART2_CTS#
TP8 I2C_TS_SDA	U7	GPP_C16/I2C0_SDA
TP7 I2C_TS_SCL	U6	GPP_C17/I2C0_SCL
	U8	
TP53 GPP_C19	U9	GPP_C18/I2C1_SDA
		GPP_C19/I2C1_SCL
TP19 GPP_F4	AH9	GPP_F4/I2C2_SDA
TP12 GPP_F5	AH10	GPP_F5/I2C2_SCL
	AH11	
	AH12	GPP_F6/I2C3_SDA
		GPP_F7/I2C3_SCL
GPP_F8	AF11	GPP_F8/I2C4_SDA
TP11 GPP_F9	AF12	GPP_F9/I2C4_SCL

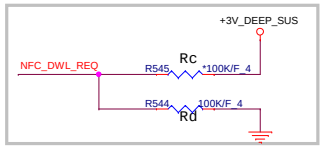
ISH

GPP_D9	P2	WWAN_TRANSMIT_OFF# / GPP_D10 → TP34 / WWAN_TRANSMIT_OFF# [33,38]
GPP_D10	P3	
GPP_D11	P4	
GPP_D12	P1	
GPP_D5/ISH_I2C0_SDA	M4	CR_PWREN# / CR_PWREN# [46]
GPP_D6/ISH_I2C0_SCL	N3	
GPP_D7/ISH_I2C1_SDA	N1	
GPP_D8/ISH_I2C1_SCL	N2	
GPP_F10/I2C5_SDA/ISH_I2C2_SDA	AD11	GPP_F10
GPP_F11/I2C5_SCL/ISH_I2C2_SCL	AD12	GPP_F11 → TP9
GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA	U1	BT_OFF / BT_OFF [37]
GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL	U2	MSATA_DET / MSATA_DET [43]
GPP_D15/ISH_UART0_RTS#	U3	MPHY_PWREN
GPP_D16/ISH_UART0_CTS#/SML0BALERT#	U4	WWANSSD_M2 / WWANSSD_M2 [38]
	AC1	PCH_LAN_RST#
GPP_C12/UART1_RXD/ISH_UART1_RXD	AC2	PCH_WLAN_RST#
GPP_C13/UART1_TXD/ISH_UART1_TXD	AC3	PCH_SLP_S0IX#
GPP_C14/UART1_RTS#/ISH_UART1_RTS#	AB4	TOUCH_RST# / PCH_SLP_S0IX# [48] / TP55
GPP_C15/UART1_CTS#/ISH_UART1_CTS#		
GPP_A18/ISH_GP0	AY8	GPP_A18
GPP_A19/ISH_GP1	BA8	GPP_A19 → TP138 / TP139
GPP_A20/ISH_GP2	BB7	SWD_CLK_SOC R944 0R_2 / SWD_CLK_PCH [44,47]
GPP_A21/ISH_GP3	BA7	SWD_IO_SOC R945 0R_2 / SWD_IO_PCH [44,47]
GPP_A22/ISH_GP4	AY7	SWD_XRES_SOC R946 0R_2 / SWD_XRES_PCH [44,47]
GPP_A23/ISH_GP5	AW7	
GPP_A12/BM_BUSY#/ISH_GP6	AP13	ISH_GP6 R621 0_4 / SX_EXIT_HOLDOFF# [48]

6 OF 20

*SKL_ULT
REV = 1

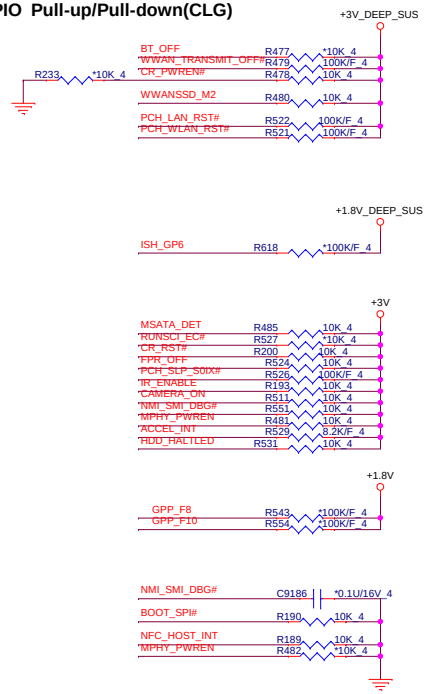
?



Conexant CX7501 & CX7700 TABLE (SI stage)

	CX7501	CX7700
Rc	UNINSTALL	INSTALL
Rd	INSTALL	UNINSTALL

GPIO Pull-up/Pull-down(CLG)



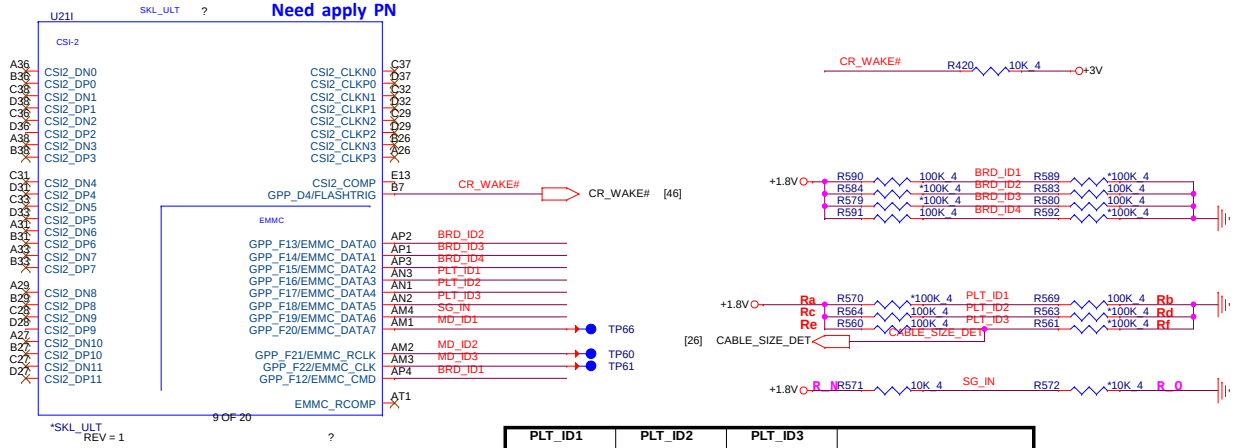
+1.8V [5,8,30,55,64]
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
+3V_DEEP_SUS [3,5,6,8,10,37,43,47,48,50,56,59,64]
+3V [2,3,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

NB5

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	04 – SKYLAKE (GPIO)	1A
Date: Thursday, May 19, 2016	Sheet 4 of 67	

	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	PPMT
	GPIO15	GPIO34	GPIO35	GPIO40	LPI-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB0	0	0	0	0	
DB1	0	0	0	1	
DB2	0	0	1	0	
	0	0	1	1	
SI	0	1	0	0	
SIB	0	1	0	1	
SI2	0	1	1	0	
	0	1	1	1	
Pre-PV	1	0	0	0	
PV	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
MV1	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	



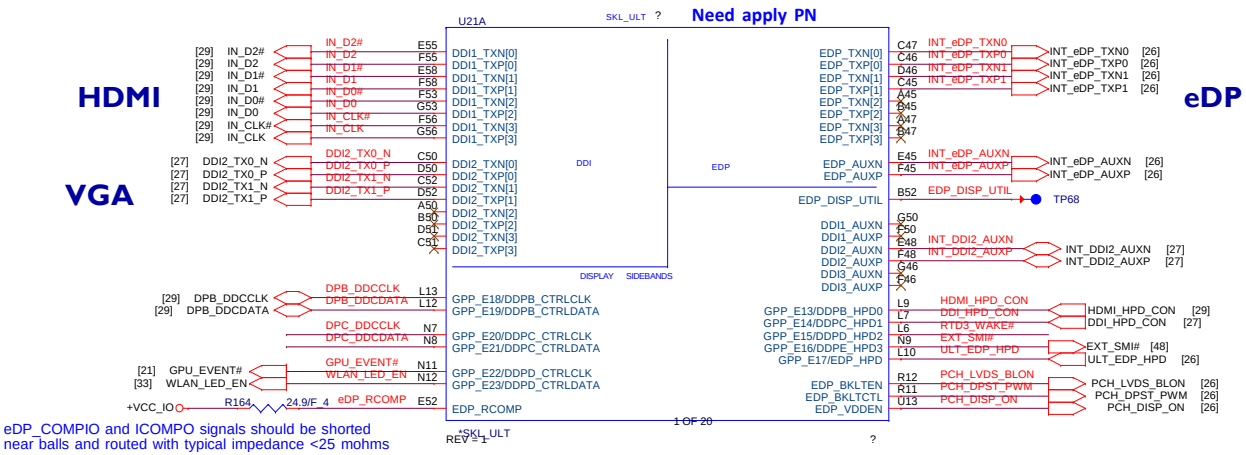
PLT_ID1	PLT_ID2	PLT_ID3	
Ra	Rc	Re	H
Rb	Rd	Rf	L
0	0	0	13.3"
0	0	1	14"
0	1	1	15.6"
0	1	1	17.3"

Cable detect

SG_IN	Install	Un-Install
UMA	R572 R_O	R571 R_N
DIS	R571 R_N	R572 R_O

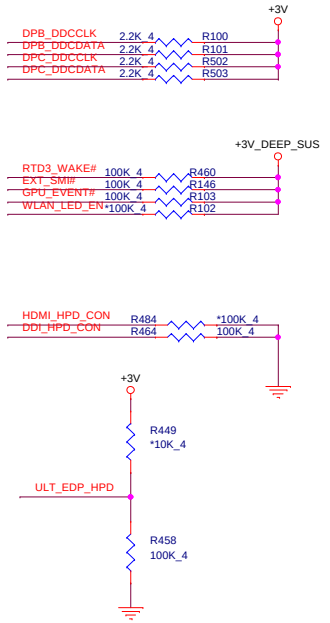
HDMI

VGA



eDP

eDP_COMPIO and ICOMPO signals should be shorted
near balls and routed with typical impedance <25 mohms



NB5	PROJECT : X63 Quanta Computer Inc. Size: Custom Document Number: 05 -- SKYLAKE (eDP/DDI/Board ID) Rev: 1A Date: Thursday, May 19, 2016 Sheet 5 of 67

SkyLake ULT Processor (DDR4)

[16] M_A_DQ[63:0]
[17] M_B_DQ[63:0]
[16] M_A_DQSN[7:0]
[16] M_A_DQSP[7:0]
[17] M_B_DQSP[7:0]
[17] M_B_DQSN[7:0]

Need apply PN

U21B — SKL_ULT — 2 OF 20 — *SKL_ULT REV = 1

U21C — SKL_ULT — 3 OF 20 — *SKL_ULT REV = 1

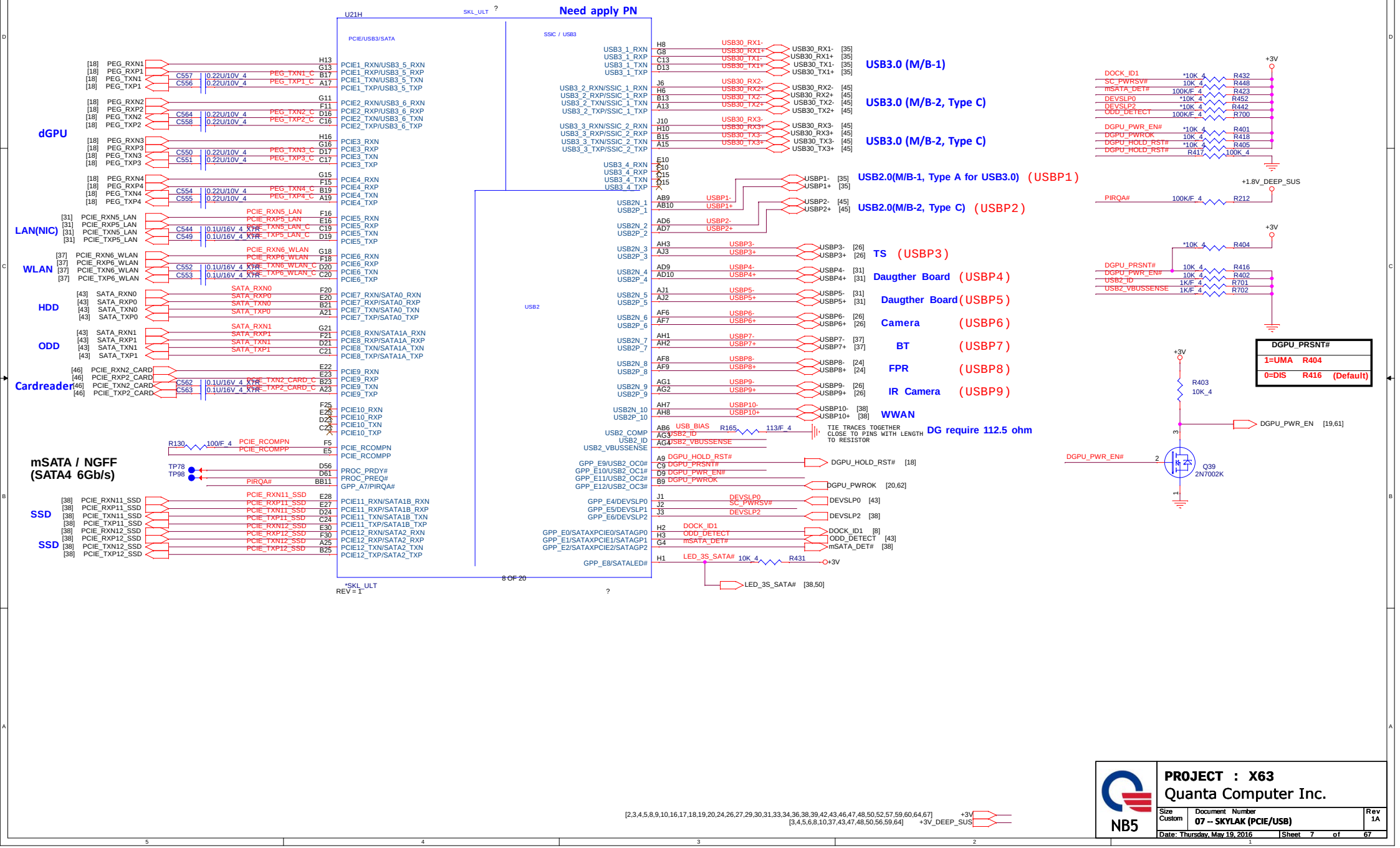
DDR CH - A

DDR CH - B

20mils width

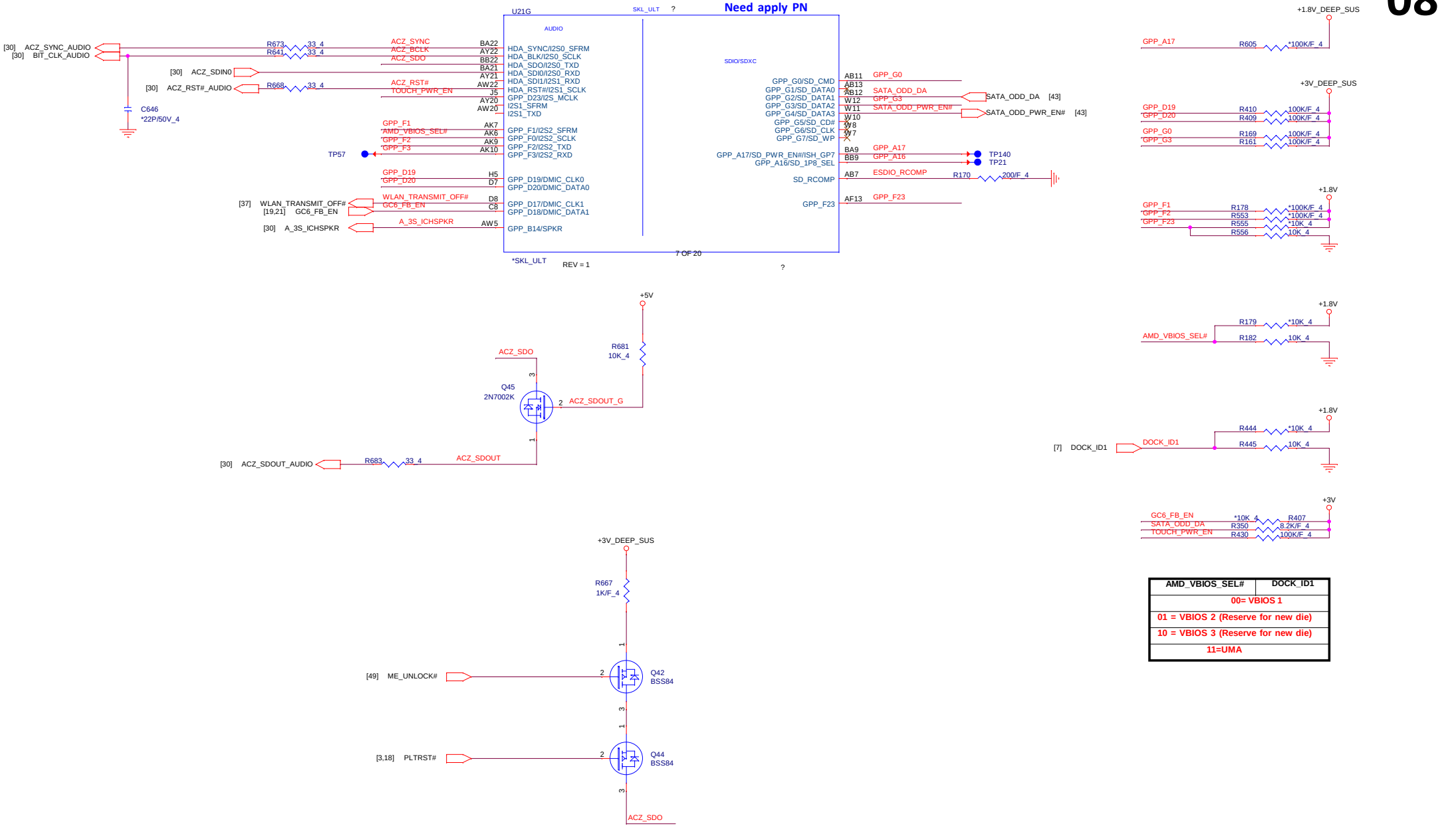
RCOMP
Trace width > 12mil
Trace length < 500 mil

PROJECT : X63		
Quanta Computer Inc.		
NB5	Size: Custom	Document Number: 06 -- SKYLAKE (DDR3-A/B I/F) Rev: 1A
	Date: Thursday, May 19, 2016	Sheet 6 of 67



[2,3,4,5,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V
[3,4,5,6,8,10,37,43,47,48,50,56,59,64] +3V_DEEP_SUS

NB5	PROJECT : X63 Quanta Computer Inc.	
Size Custom	Document Number 07 -- SKYLAK (PCIE/USB)	Rev 1A
Date: Thursday, May 19, 2016	Sheet 7 of 67	



AMD_VBIOS_SEL#	DOCK_ID1
00= VBIOS 1	
01 = VBIOS 2 (Reserve for new die)	
10 = VBIOS 3 (Reserve for new die)	
11=UMA	

NB5

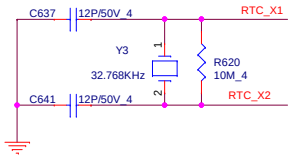
PROJECT : X63

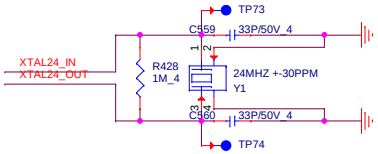
Quanta Computer Inc.

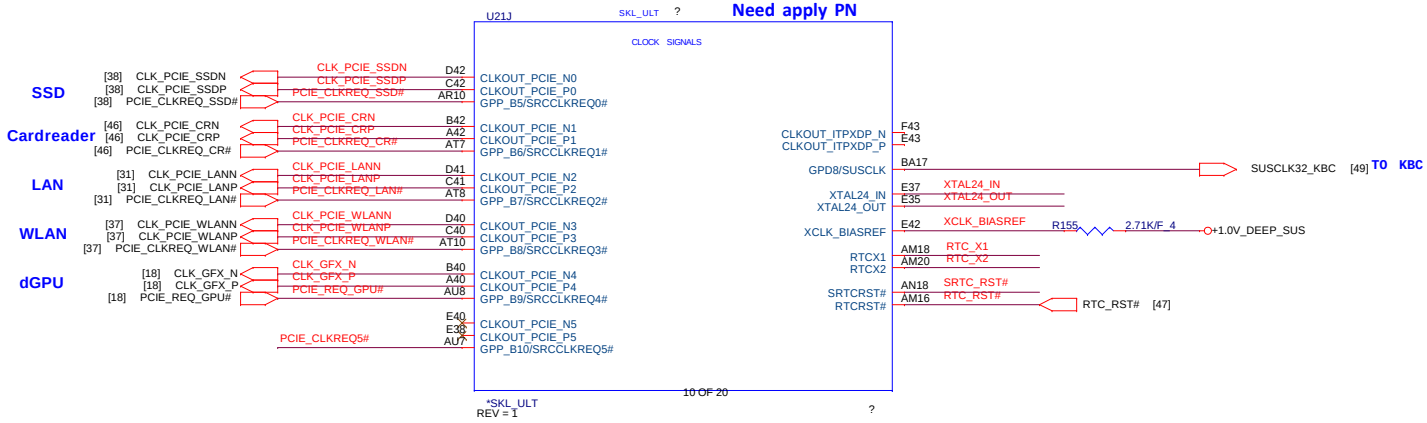
Size	Document Number	Rev
Custom	08 -- SKYLAKE (HDA)	1A

Date: Thursday, May 19, 2016 | Sheet 8 of 67

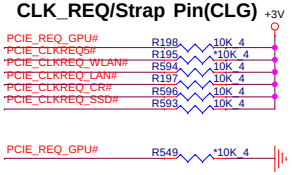
RTC Clock 32.768KHz



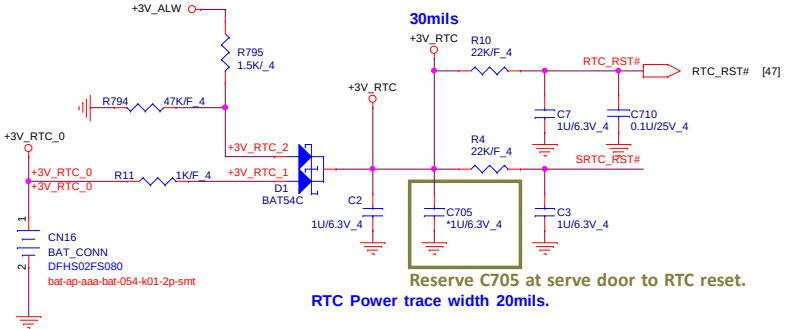


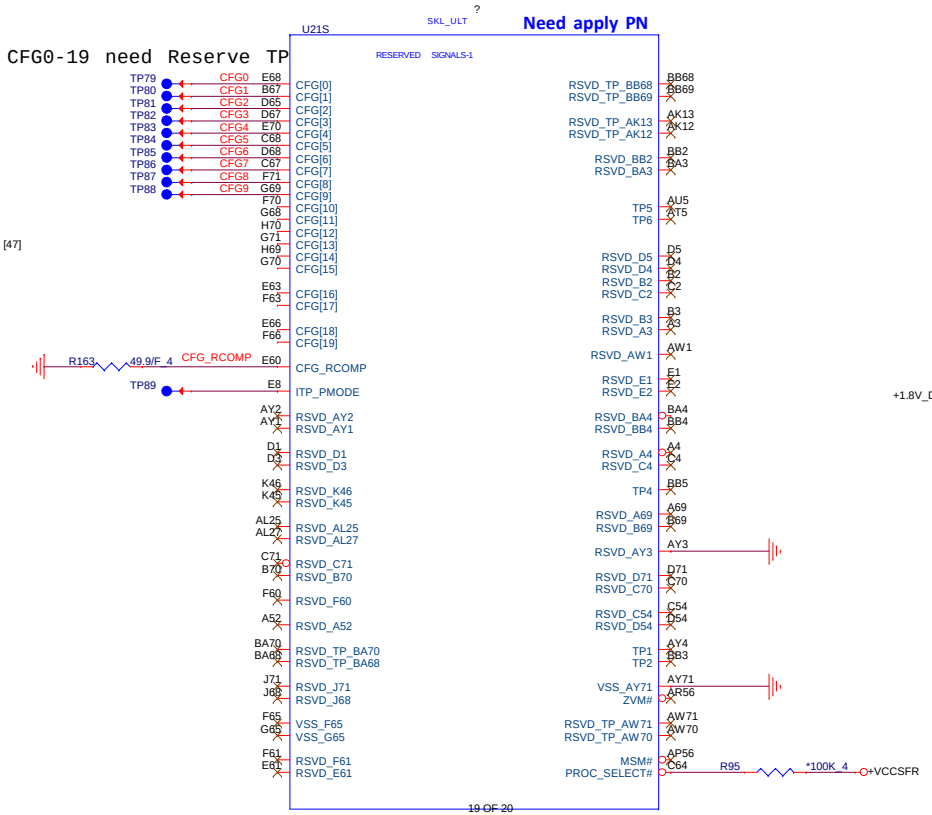


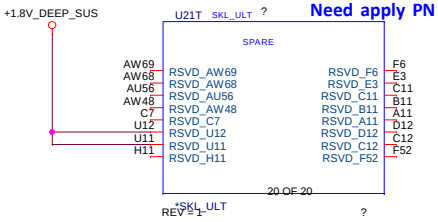
CLK_REQ/Strap Pin(CLG)

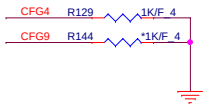


RTC Circuitry(RTC)







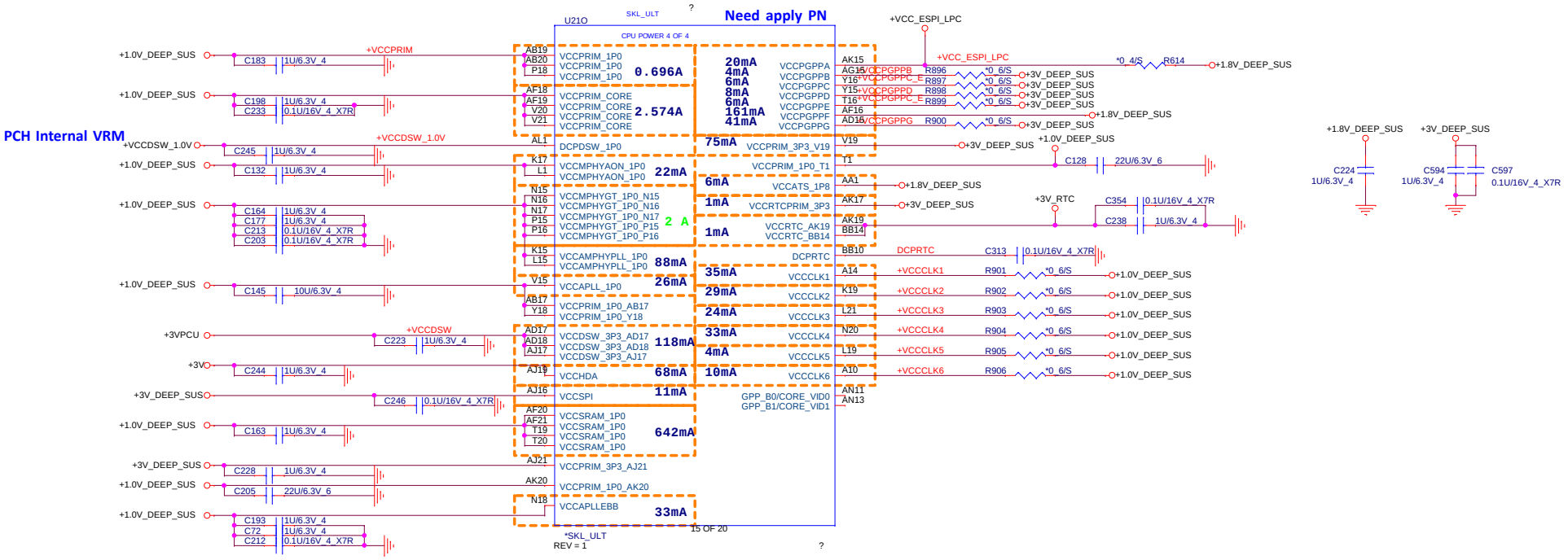


+1.0V_DEEP_SUS [10,55,56,59]
+VCCSFR [2,3,11,13,48]
+3V [2,3,4,5,7,8,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]

NB5

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- SKYLAKE (CLK/RSV/RTC)	1A
Date: Thursday, May 19, 2016	Sheet 9 of 67	

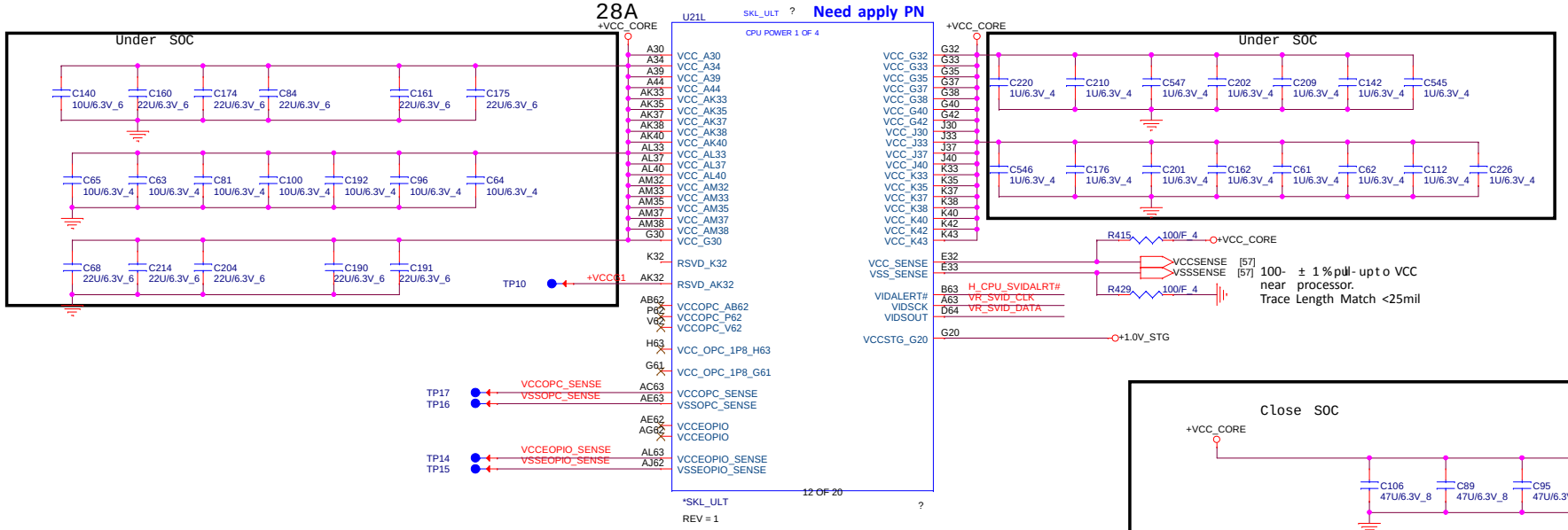


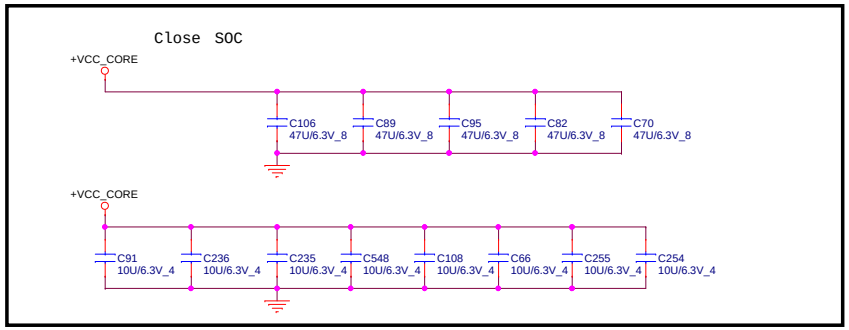
+3V_DEEP_SUS [3,4,5,6,8,37,43,47,48,50,56,59,64]
+3VPCU [3,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
+1.0V_DEEP_SUS [9,55,56,59]
+VCC_PRIM
+3V [2,3,4,5,7,8,9,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67]
+1.8V_DEEP_SUS [3,4,7,8,9,48,50,55,64]

NB5

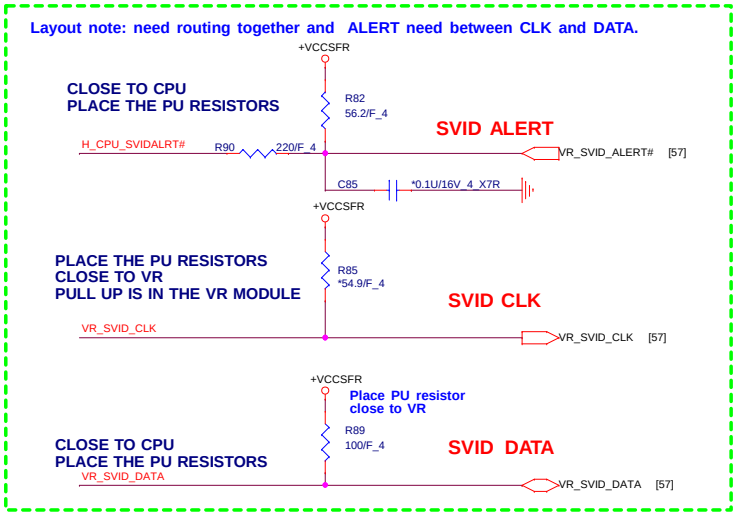
PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- SKYLAKE (PCH POWER)	1A
Date: Thursday, May 19, 2016	Sheet 10 of 67	





Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

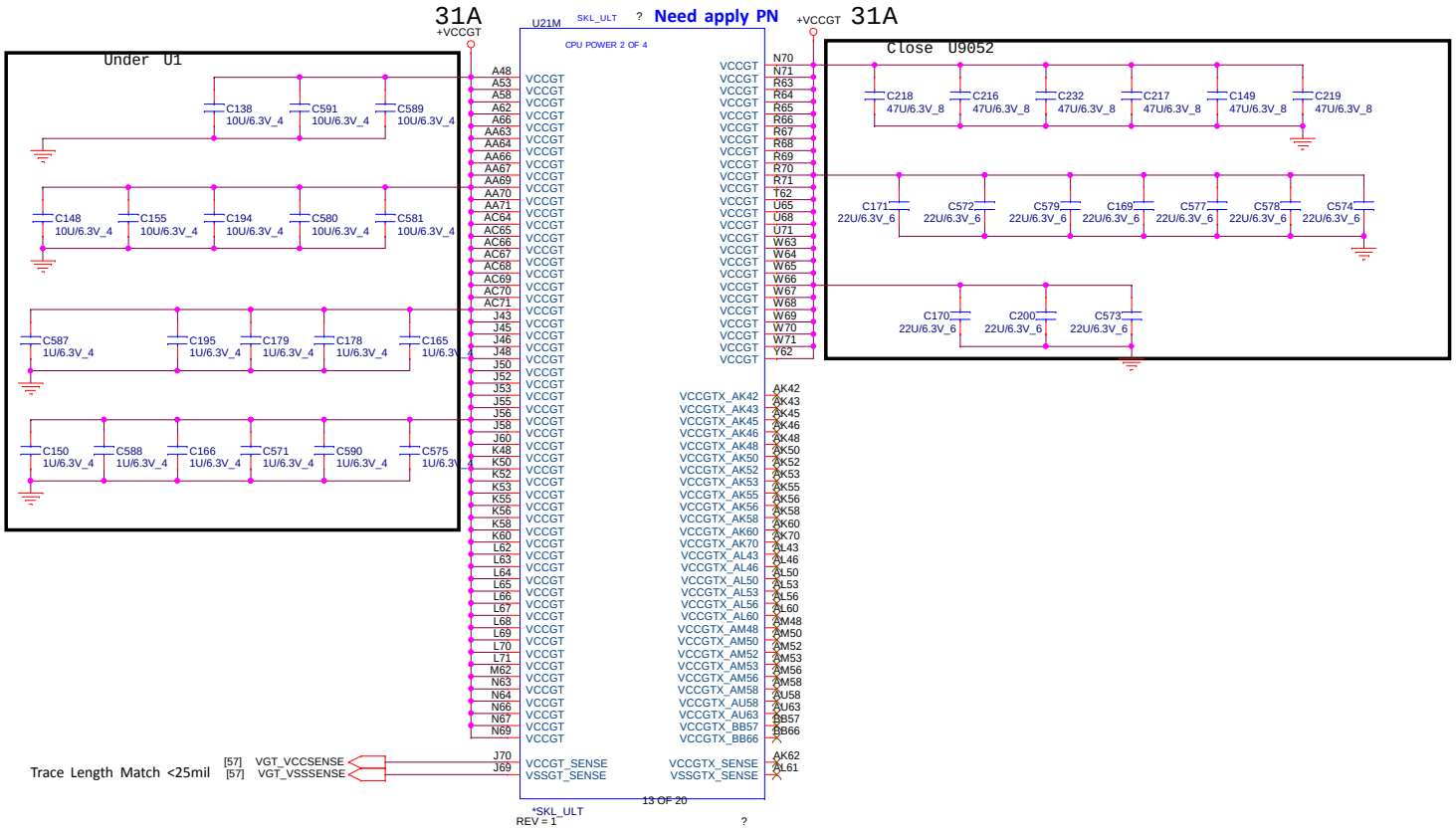


+1.8V [4,5,8,30,55,64]
+VCC_CORE [57]
+VCCSFR [2,3,9,13,48]
+1.0V_STG [2,13]

NB5

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE (POWER-1)	1A
Date: Thursday, May 19, 2016	Sheet 11 of 67	



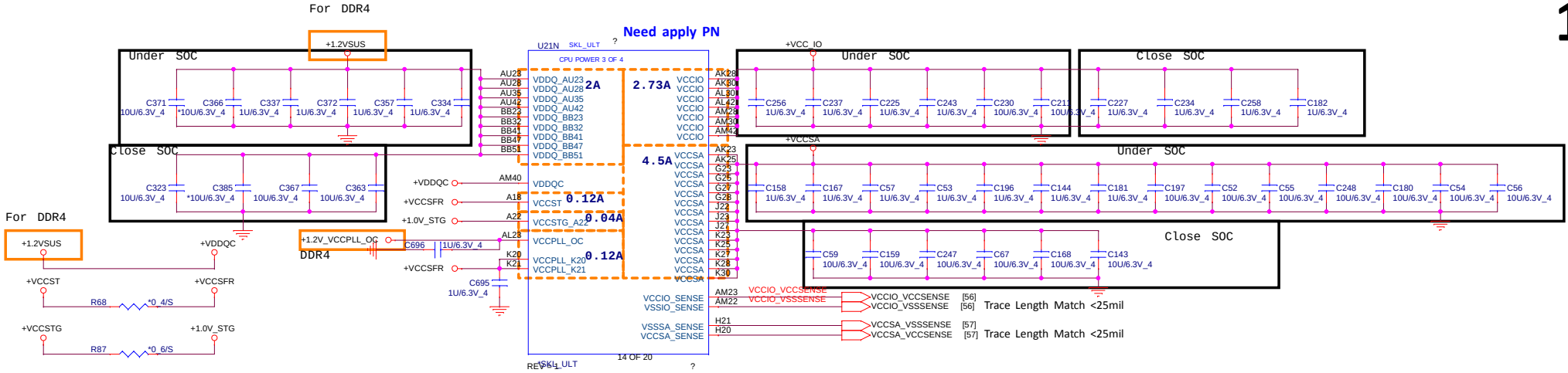
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

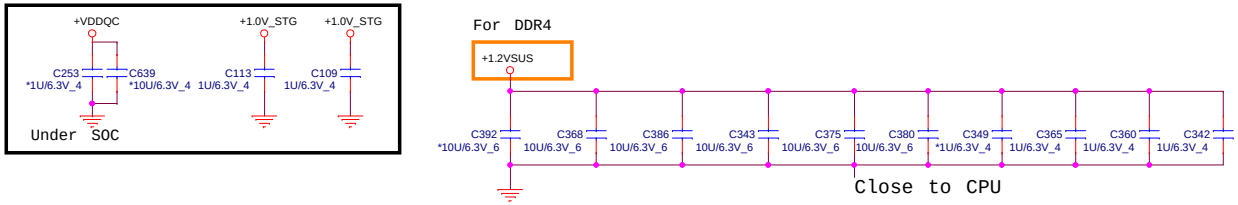
NB5

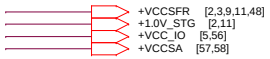
PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- SKYLAKE (POWER-2)	1A

Date: Thursday, May 19, 2016 Sheet 12 of 67







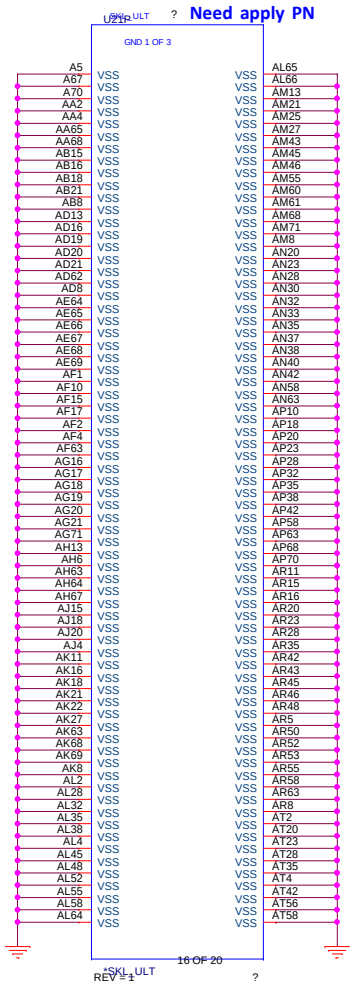
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

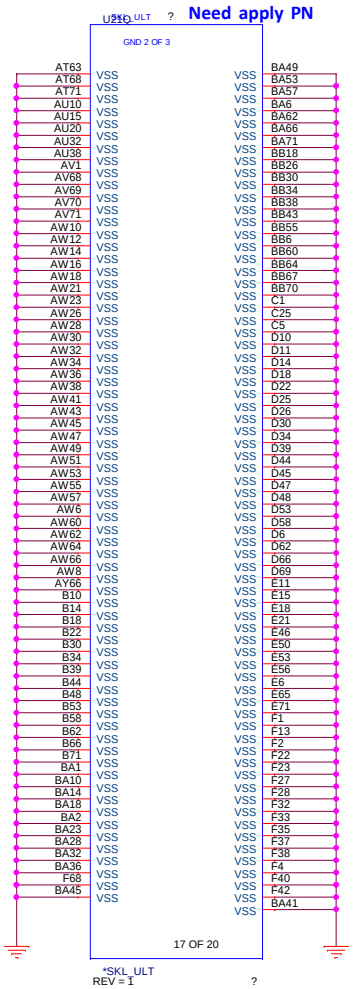
NB5

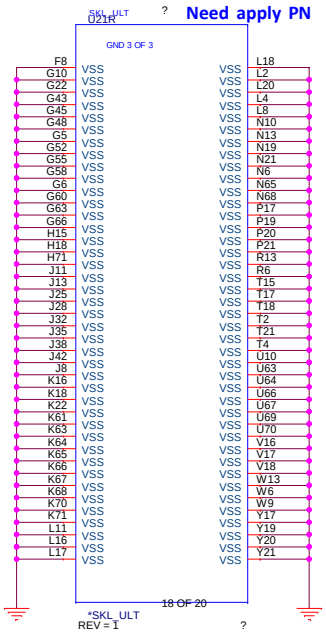
PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- SKYLAKE (POWER-3)	1A

Date: Thursday, May 19, 2016 | Sheet 13 of 67

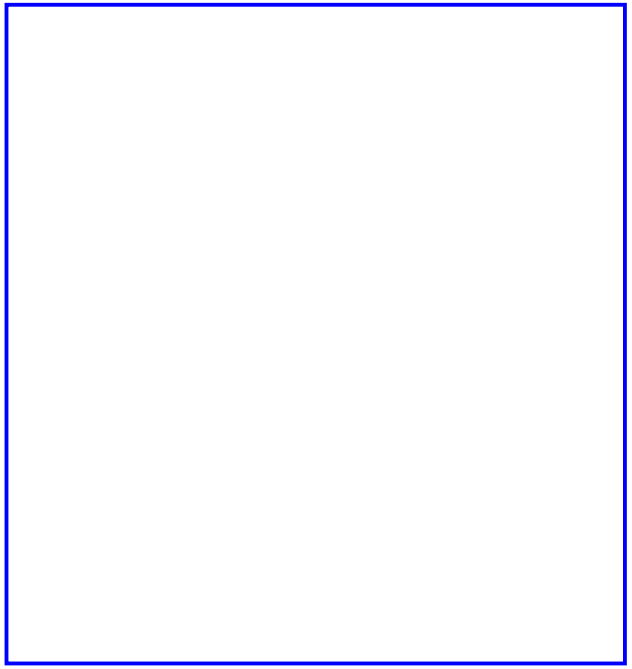






NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 14 -- SKYLAKE (GND)	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 14 of 67	

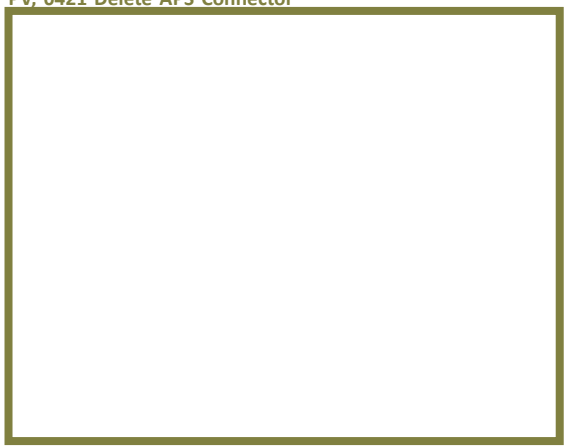
10/28 Del XDP



15

11/03 Del XDP

PV, 0421 Delete APS Connector



11/03 Del XDP

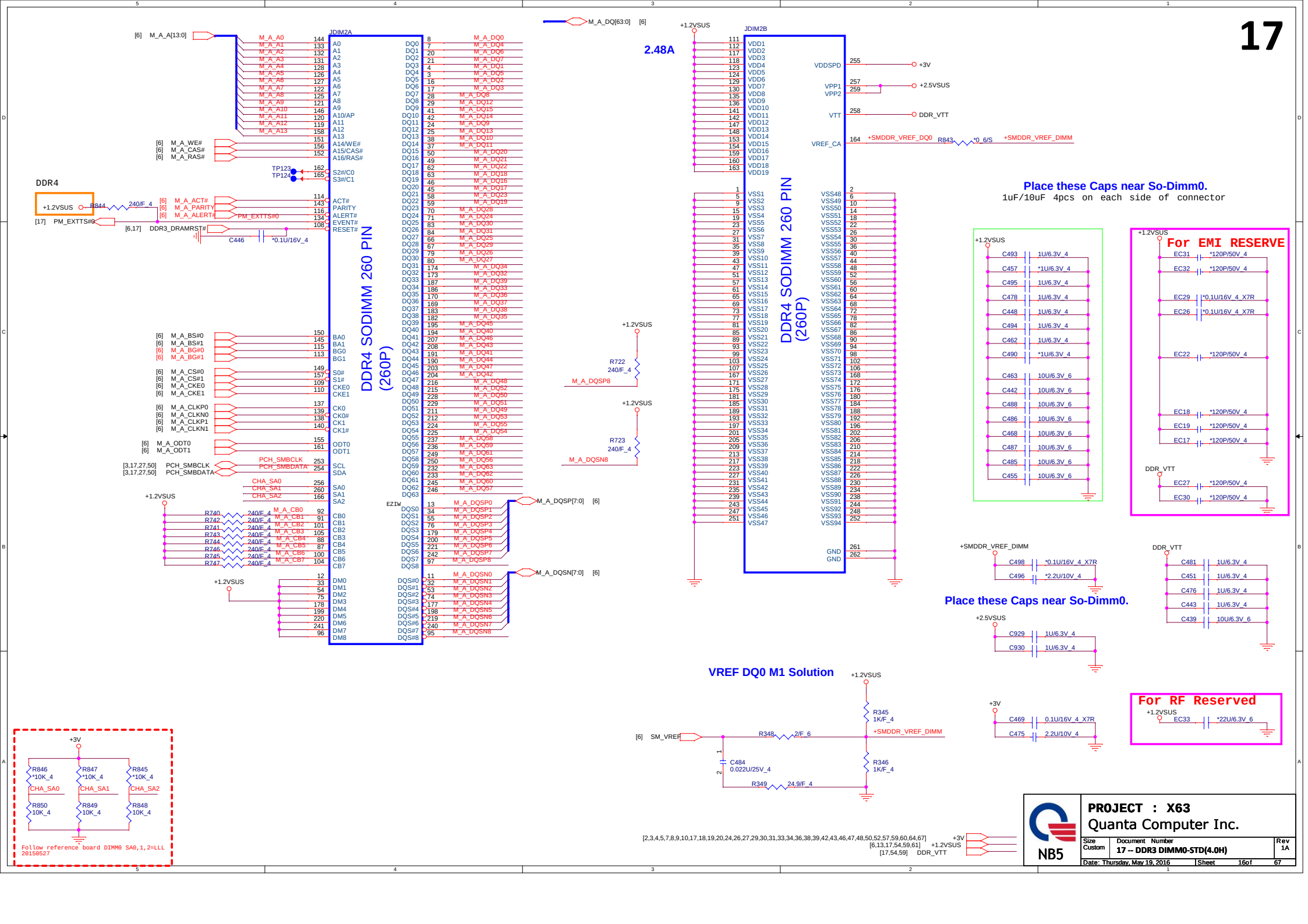
NB5

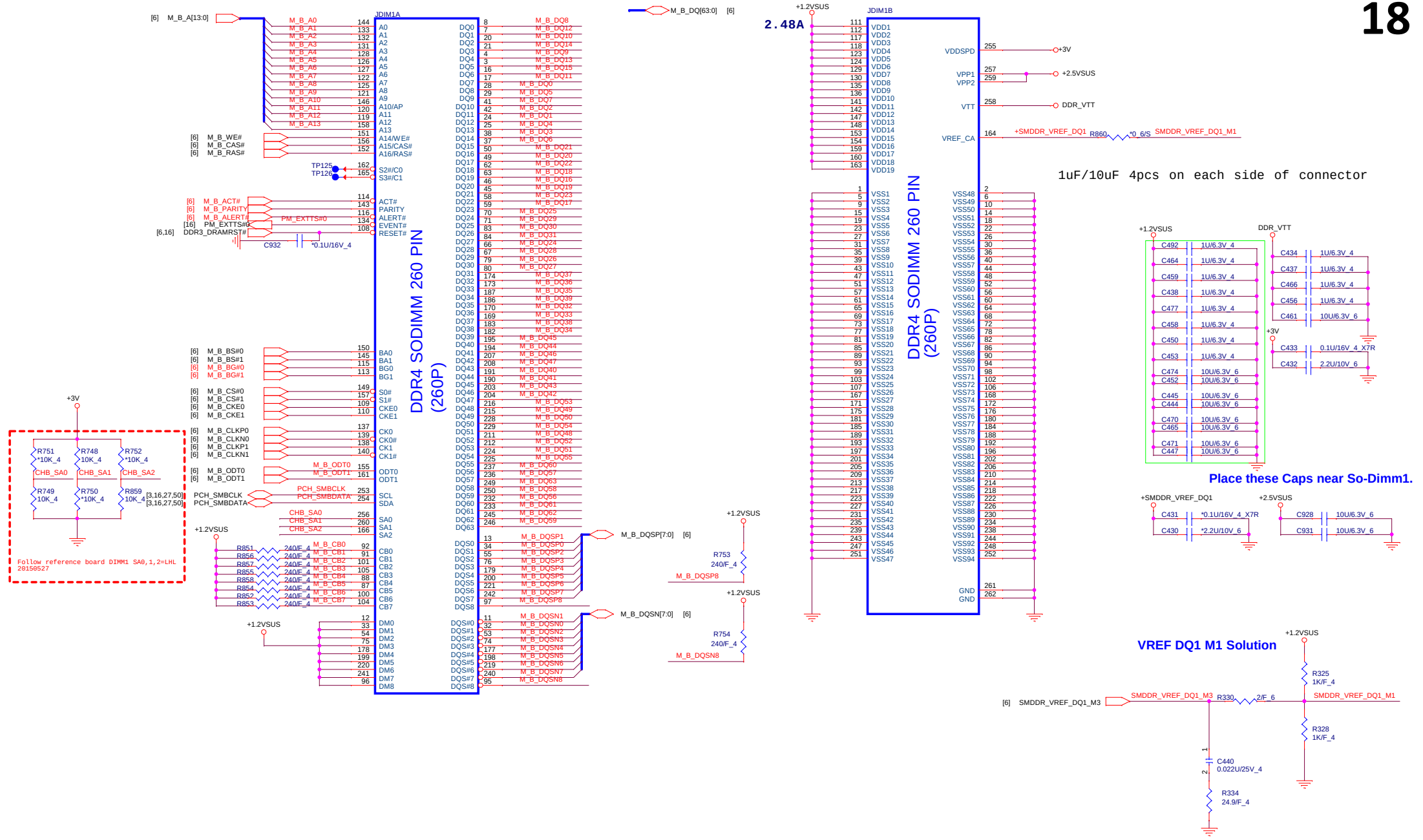
PROJECT : X63

Quanta Computer Inc.

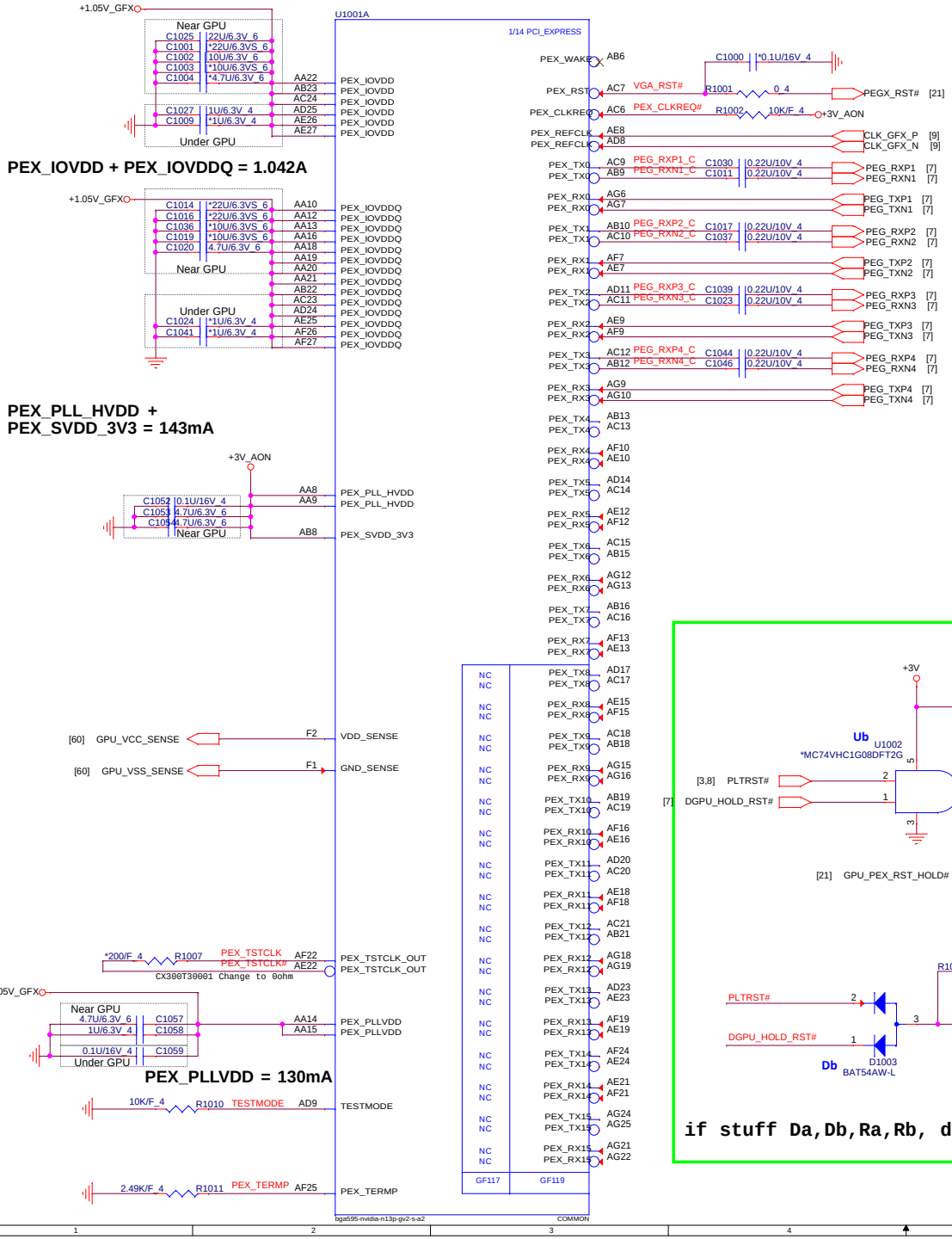
Size	Document Number	Rev
	15 -- HSW XDP & APS	1A

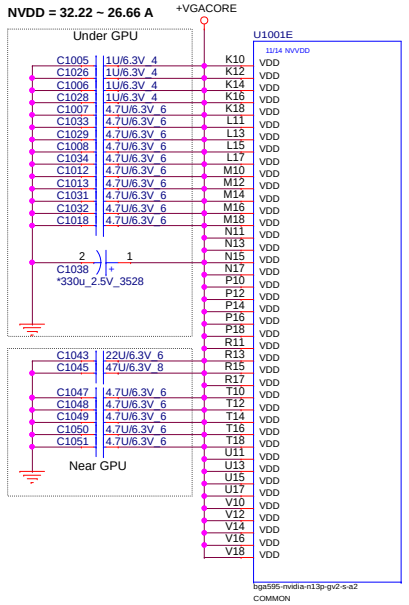
Date: Thursday, May 19, 2016 | Sheet 15 of 67

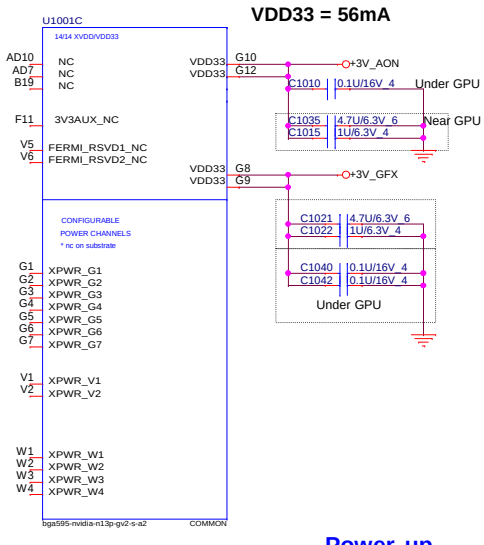

JDIM2A
DDR4 SODIMM 260 PIN (260P)
JDIM2B
DDR4 SODIMM 260 PIN (260P)
DDR4
2.48A
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
For EMI RESERVE
Place these Caps near So-Dimm0.
VREF DQ0 M1 Solution
For RF Reserved
Follow reference board DIMM0 SA0,1,2=LLL 20150527
PROJECT : X63
Quanta Computer Inc.
NB5
Size Custom
Document Number 17 -- DDR3 DIMM0-STD(4.0H)
Rev 1A
Date: Thursday, May 19, 2016
Sheet 16of 67

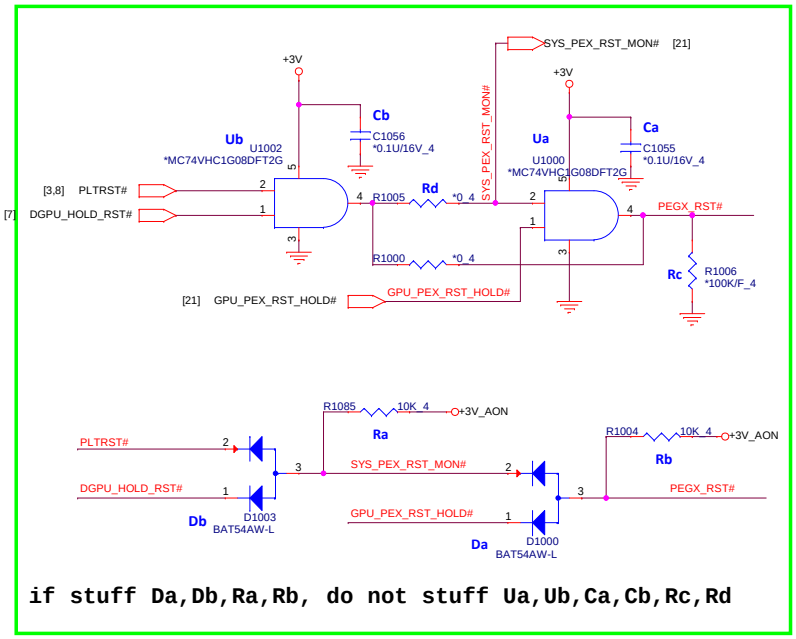


PROJECT	X63
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: 18 -- DDR3 DIMM1-RVS(4.0H)
Rev: 1A	
Date: Thursday, May 19, 2016	Sheet: 17of 67

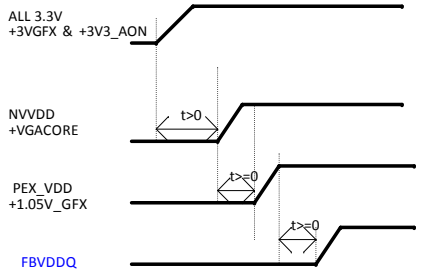


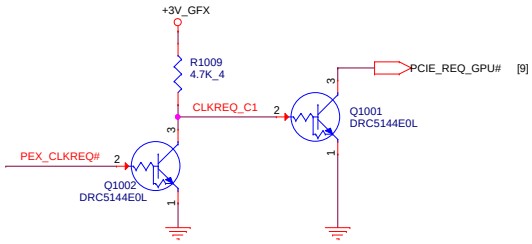




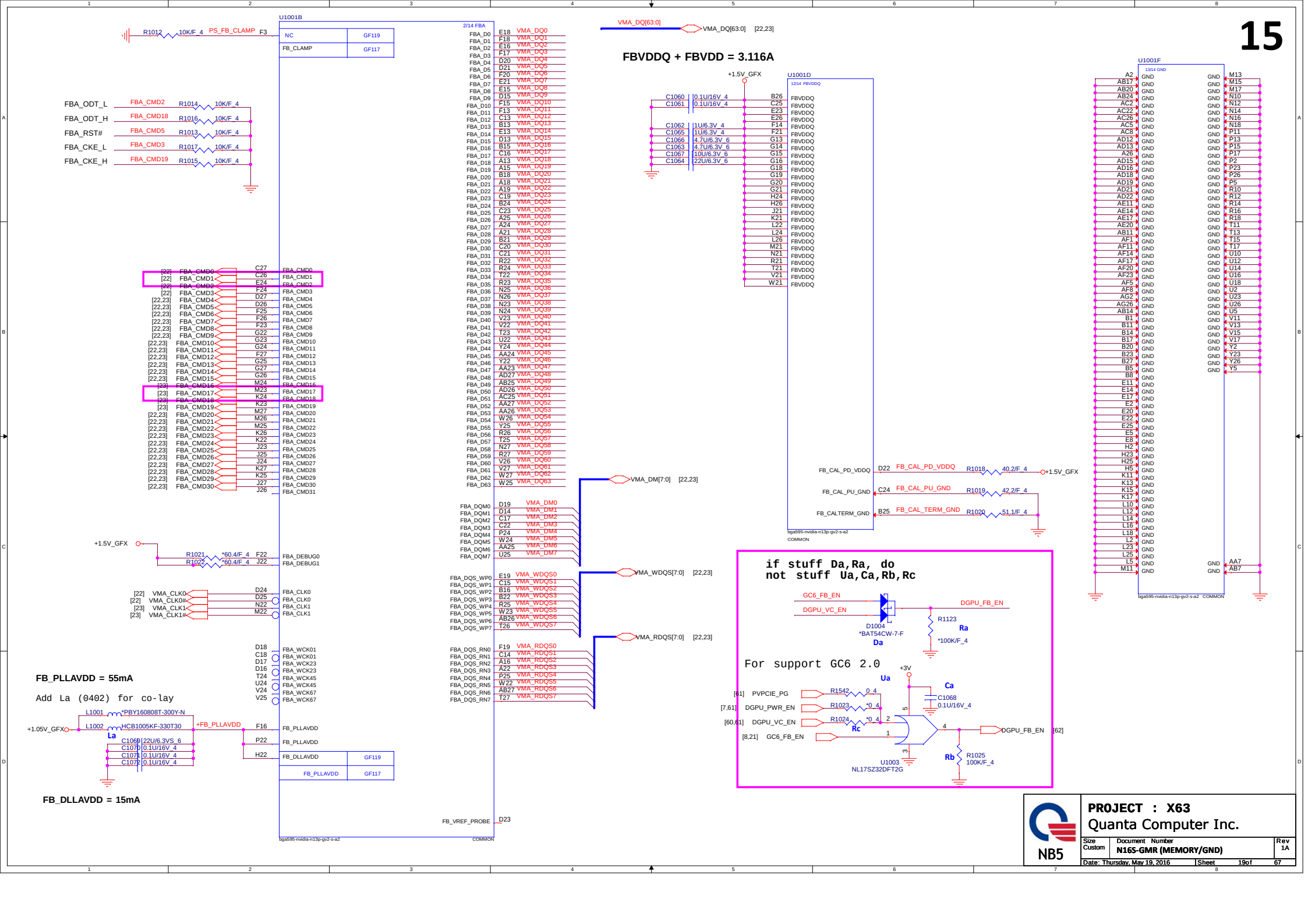


Power up sequence

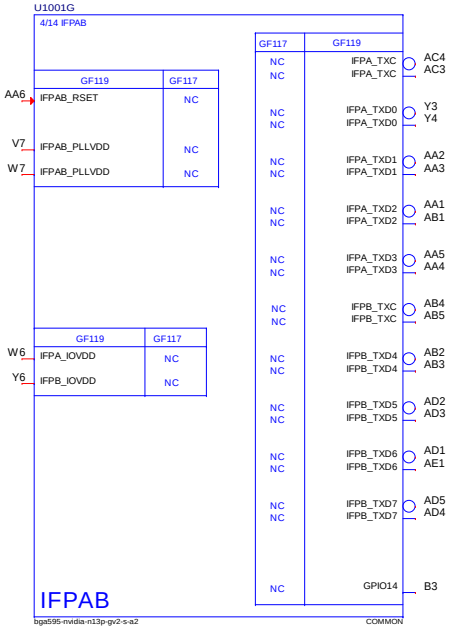


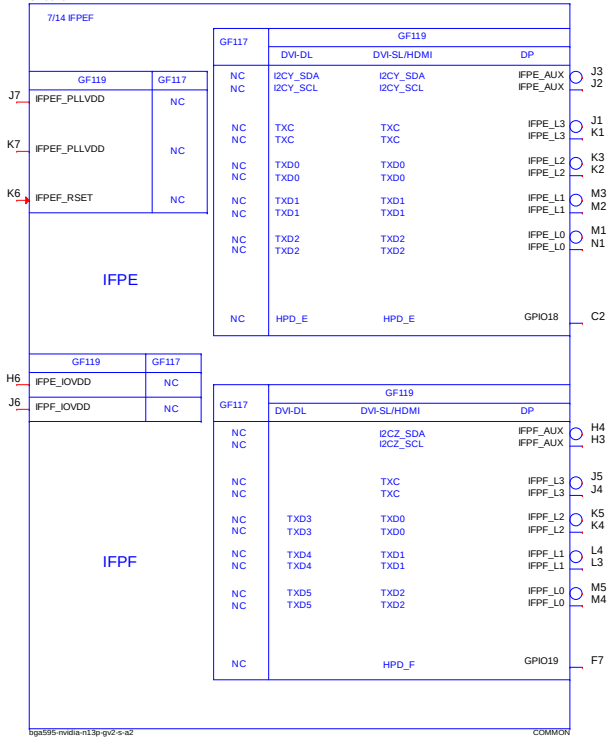


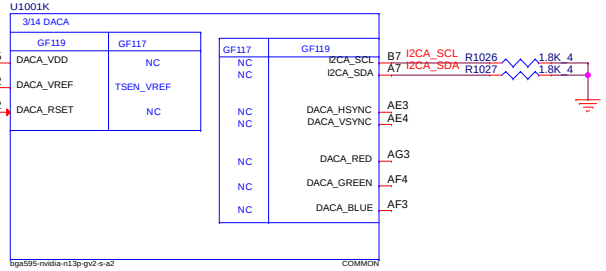
NB5	PROJECT : X63 Quanta Computer Inc.	
	Size: Custom Document Number: N16S-GMR (PCIE I/F) /NVDD	Rev: 1A
	Date: Thursday, May 19, 2016	Sheet 18of 67

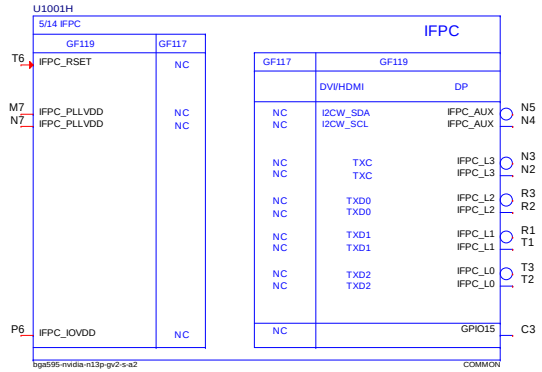


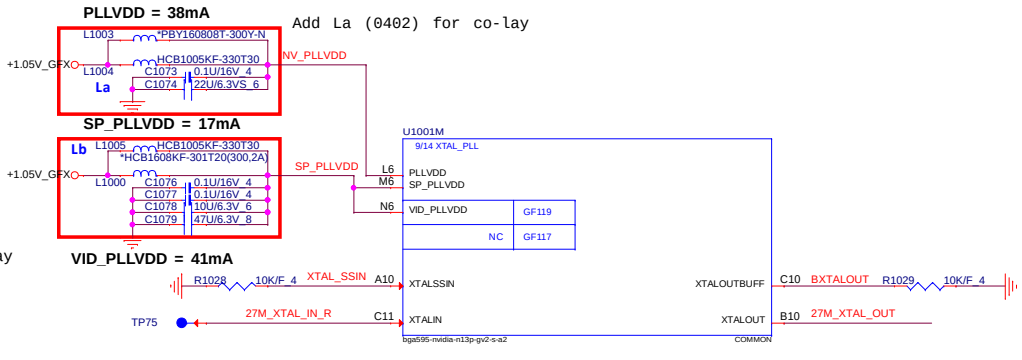
NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: N16S-GMR (MEMORY/GND)	Rev: 1A
Date: Thursday, May 19, 2016	Sheet: 19of 67	

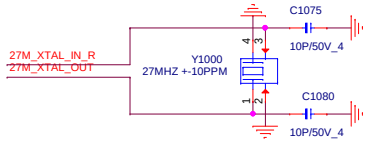


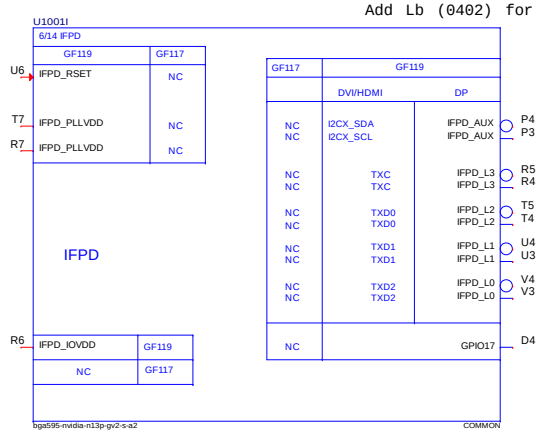


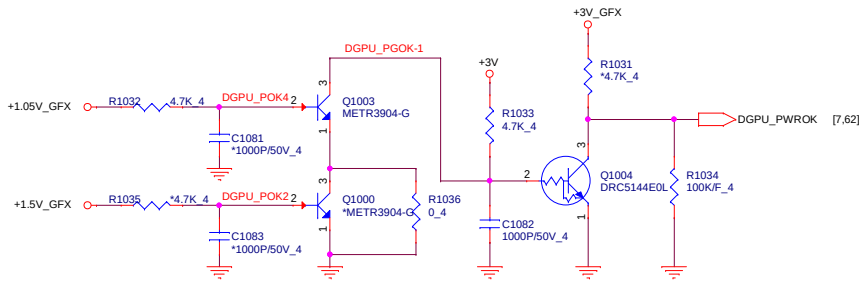




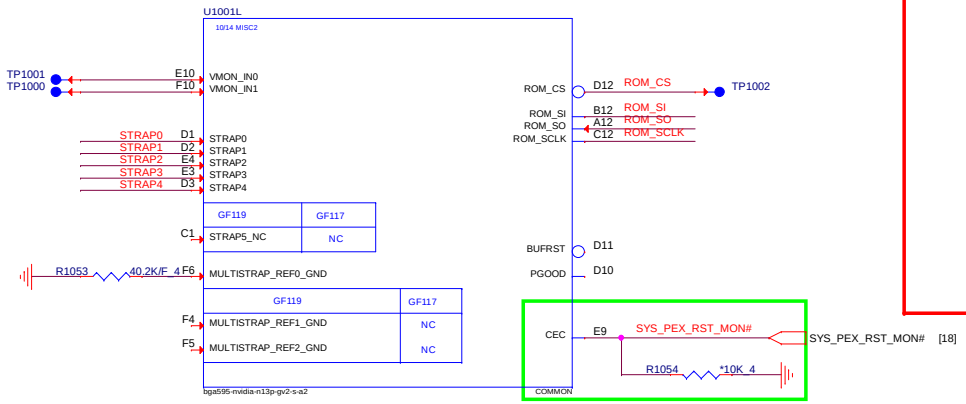


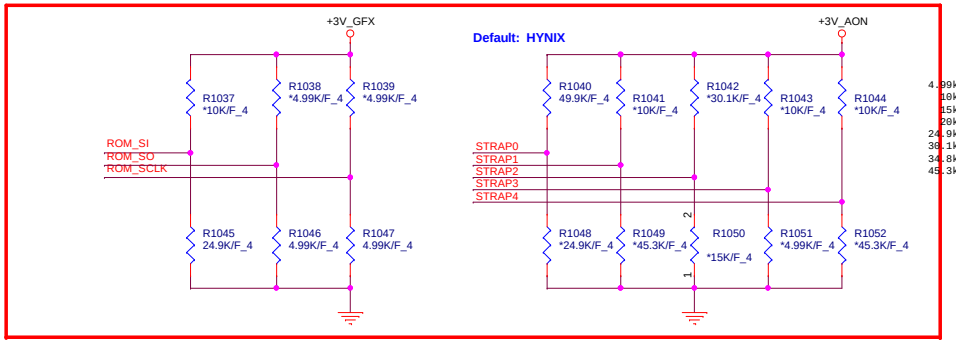


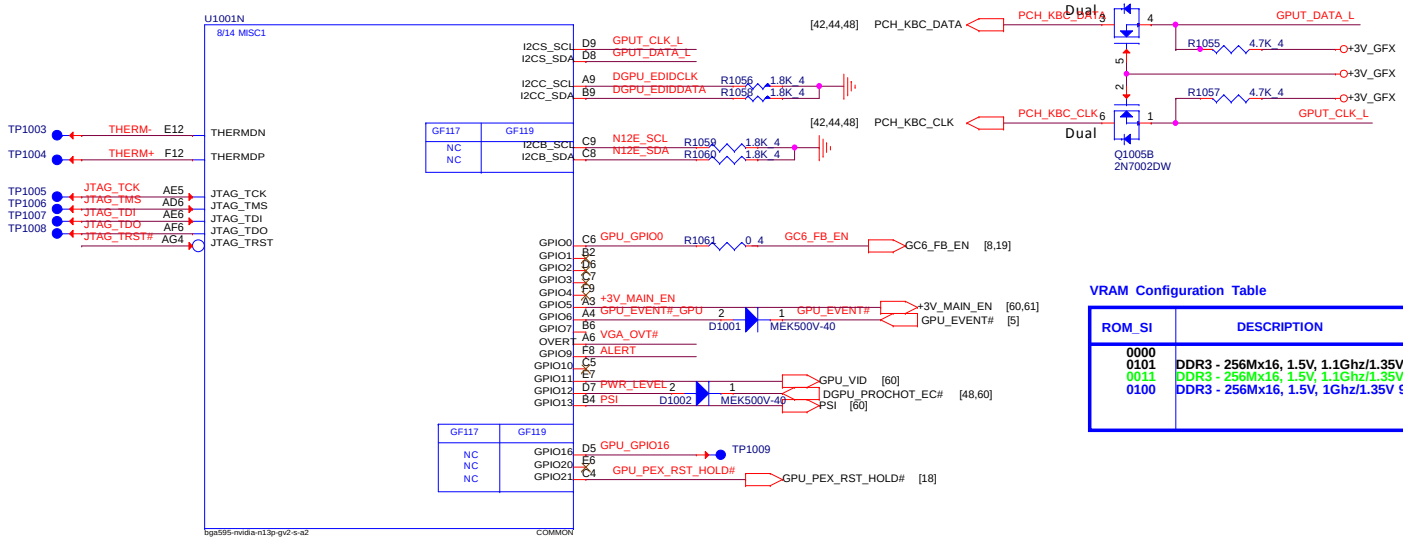




PROJECT : X63	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: N16S-GMR (DISPLAY); Rev: 1A
Date: Thursday, May 19, 2016	Sheet 20of 67







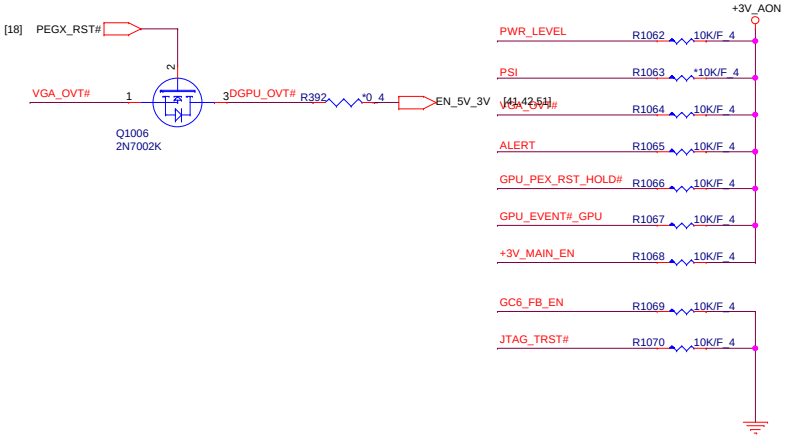


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	Straping	TOP B/S	QBC
0000						
0101	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	HYNIX	H5TC4G63CFR-N0C	0x5	AKD5PZDTW01	AKD5PZDTW02
0011	DDR3 - 256Mx16, 1.5V, 1.1Ghz/1.35V 1Ghz	Micron	MT41J256M16LY-091G:N	0x3	AKD59GSTL01	AKD59GSTL00
0100	DDR3 - 256Mx16, 1.5V, 1Ghz/1.35V 900Mhz	SAMSUNG	K4W4G1646E-BC1A	0x4	AKD5PGDT500	AKD5PGDT501

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN :AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN :AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN :AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U1004

VREFC_VMA1 M8 VREFCA
VREFD_VMA1 H1 VREFDQ

[19,23] FBA_CMD9 N3
[19,23] FBA_CMD11 P7
[19,23] FBA_CMD8 P3
[19,23] FBA_CMD25 N2
[19,23] FBA_CMD10 P8
[19,23] FBA_CMD24 P2
[19,23] FBA_CMD22 R8
[19,23] FBA_CMD7 R2
[19,23] FBA_CMD21 T8
[19,23] FBA_CMD6 R3
[19,23] FBA_CMD29 L7
[19,23] FBA_CMD23 R7
[19,23] FBA_CMD28 N7
[19,23] FBA_CMD20 T3
[19,23] FBA_CMD4 T7
[19,23] FBA_CMD14 M7

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

[19,23] FBA_CMD12 M2
[19,23] FBA_CMD27 N8
[19,23] FBA_CMD26 M3

BA0 BA1 BA2

[19] VMA_CLK0 J7
[19] VMA_CLK0# K7
[19] FBA_CMD3 K9

CK CK CKE

[19] FBA_CMD2 K1
[19] FBA_CMD0 L2
[19,23] FBA_CMD30 J3
[19,23] FBA_CMD15 K3
[19,23] FBA_CMD13 L3

ODT CS RAS CAS WE

[19] VMA_WDQS1 F3
[19] VMA_RDQS1 G3

DQSL DQSL

[19] VMA_DM1 E7
[19] VMA_DM2 D3

DML DMU

[19] VMA_WDQS2 C7
[19] VMA_RDQS2 B7

DQSU DQSU

[19,23] FBA_CMD5 T2

RESET

FBA_ZQ0 L8

GND — 243/F_4 R1072 — ZQ

[19] FBA_CMD1 L1
FBA_CMD2 J1
FBA_CMD3 J9
FBA_ZQ2 L9

GND — 243/F_4 R1124

NC#J1 NC#L1 NC#J9 NC#L9

96-BALL SDRAM_DDR3 VRAM _DDR3_HYNIX_256MX16

stuff R1124 for Hynix 8Gb DDP VRAM

DQL0 E3
DQL1 F7
DQL2 F2
DQL3 F8
DQL4 H3
DQL5 H8
DQL6 G2
DQL7 H7

VMA_DQ11 [19]
VMA_DQ14 [19]
VMA_DQ8 [19]
VMA_DQ13 [19]
VMA_DQ10 [19]
VMA_DQ12 [19]
VMA_DQ9 [19]
VMA_DQ15 [19]

DQU0 D7
DQU1 C8
DQU2 C2
DQU3 A7
DQU4 A2
DQU5 B8
DQU6 A3
DQU7

VMA_DQ17 [19]
VMA_DQ21 [19]
VMA_DQ18 [19]
VMA_DQ22 [19]
VMA_DQ19 [19]
VMA_DQ23 [19]
VMA_DQ16 [19]
VMA_DQ20 [19]

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9

+1.5V_GFX — 4.7U/6.3V_6 C1084 — 0.1U/16V_4 C1085 — 0.1U/16V_4 C1086 — GND

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

+1.5V_GFX — 4.7U/6.3V_6 C1090 — 0.1U/16V_4 C1091 — 0.1U/16V_4 C1092 — GND

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

GND

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

reserve for Hynix 8Gb DDP VRAM

SDDR3_BGA100

	0..31	32..63
CMD0	CS0*	
CMD1	CS1*	
CMD2	ODT	
CMD3	CKE	
CMD16		CS0*
CMD17		CS1*
CMD18		ODT
CMD19		CKE

SNN_FBA0_ODT1	J1	NC/ODT1
SNN_FBA0_CKE1	J9	NC/CKE1
SNN_FBA0_CS1	L1	NC/CS1
SNN_FBA0_ZQ1	L9	NC/ZQ1

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

VMA_CLK0 — R1071 162/F_4 — VMA_CLK0#

+1.5V_GFX — R1073 1.33K/F_4 — VREFC_VMA1 — R1076 1.33K/F_4 — C1096 0.01U/50V_4
+1.5V_GFX — R1074 1.33K/F_4 — VREFD_VMA1 — R1077 1.33K/F_4 — C1097 0.01U/50V_4

+1.5V_GFX — C1103 1U/6.3V_4 — C1106 1U/6.3V_4 — C1108 1U/6.3V_4 — C1111 1U/6.3V_4
+1.5V_GFX — C1104 1U/6.3V_4 — C1107 1U/6.3V_4 — C1109 1U/6.3V_4 — C1112 1U/6.3V_4

+1.5V_GFX — C1098 10U/6.3V_6 — C1099 10U/6.3V_6 — C1100 10U/6.3V_6 — C1101 0.1U/16V_4 — C1102 0.1U/16V_4 — C1105 0.1U/16V_4 — C1110 0.1U/16V_4 — C1113 0.1U/16V_4 — C1114 0.1U/16V_4

U1005

VREFC_VMA1 M8 VREFCA
VREFD_VMA1 H1 VREFDQ

FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3

BA0 BA1 BA2

VMA_CLK0 J7
VMA_CLK0# K7
FBA_CMD3 K9

CK CK CKE

FBA_CMD2 K1
FBA_CMD0 L2
FBA_CMD30 J3
FBA_CMD15 K3
FBA_CMD13 L3

ODT CS RAS CAS WE

[19] VMA_WDQS0 F3
[19] VMA_RDQS0 G3

DQSL DQSL

[19] VMA_DM0 E7
[19] VMA_DM3 D3

DML DMU

[19] VMA_WDQS3 C7
[19] VMA_RDQS3 B7

DQSU DQSU

FBA_CMD5 T2

RESET

FBA_ZQ1 L8

GND — 243/F_4 R1075 — ZQ

FBA_CMD2 J1
FBA_CMD1 L1
FBA_CMD3 J9
FBA_ZQ3 L9

GND — 243/F_4 R1125

NC#J1 NC#L1 NC#J9 NC#L9

96-BALL SDRAM_DDR3 VRAM _DDR3_HYNIX_256MX16

stuff R1125 for Hynix 8Gb DDP VRAM

DQL0 E3
DQL1 F7
DQL2 F2
DQL3 F8
DQL4 H3
DQL5 H8
DQL6 G2
DQL7 H7

VMA_DQ1 [19]
VMA_DQ4 [19]
VMA_DQ3 [19]
VMA_DQ6 [19]
VMA_DQ0 [19]
VMA_DQ7 [19]
VMA_DQ2 [19]
VMA_DQ5 [19]

DQU0 D7
DQU1 C8
DQU2 C2
DQU3 A7
DQU4 A2
DQU5 B8
DQU6 A3
DQU7

VMA_DQ25 [19]
VMA_DQ28 [19]
VMA_DQ24 [19]
VMA_DQ29 [19]
VMA_DQ26 [19]
VMA_DQ30 [19]
VMA_DQ27 [19]
VMA_DQ31 [19]

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N9
VDD#N9 R1
VDD#R1 R9
VDD#R9

+1.5V_GFX — 4.7U/6.3V_6 C1087 — 0.1U/16V_4 C1088 — 0.1U/16V_4 C1089 — GND

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

+1.5V_GFX — 4.7U/6.3V_6 C1093 — 0.1U/16V_4 C1094 — 0.1U/16V_4 C1095 — GND

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

GND

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

NB5

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L - RANK0	1A

Date: Thursday, May 19, 2016 Sheet 22of 67

Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN :AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN :AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN :AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U1006

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

[19,22] FBA_CMD9 N3
[19,22] FBA_CMD11 P7
[19,22] FBA_CMD8 P3
[19,22] FBA_CMD25 N2
[19,22] FBA_CMD10 P8
[19,22] FBA_CMD24 P2
[19,22] FBA_CMD22 R8
[19,22] FBA_CMD7 R2
[19,22] FBA_CMD21 T8
[19,22] FBA_CMD6 R3
[19,22] FBA_CMD29 L7
[19,22] FBA_CMD23 R7
[19,22] FBA_CMD28 N7
[19,22] FBA_CMD20 T3
[19,22] FBA_CMD4 T7
[19,22] FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

[19,22] FBA_CMD12 M2
[19,22] FBA_CMD27 N8
[19,22] FBA_CMD26 M3
BA0 BA1 BA2

[19] VMA_CLK1 J7
[19] VMA_CLK1# K7
[19] FBA_CMD19 K9
CK CK CKE

[19] FBA_CMD18 K1
[19] FBA_CMD16 L2
[19,22] FBA_CMD30 J3
[19,22] FBA_CMD15 K3
[19,22] FBA_CMD13 L3
ODT CS RAS CAS WE

[19] VMA_WDQS4 F3
[19] VMA_RDQS4 G3
DQSL DQSL

[19] VMA_DM4 E7
[19] VMA_DM7 D3
DML DMU

[19] VMA_WDQS7 C7
[19] VMA_RDQS7 B7
DQSU DQSU

[19,22] FBA_CMD5 T2
RESET

GND — FBA_ZQ4 — L8 ZQ — 243/F_4 R1079

[19] FBA_CMD17 J1
FBA_CMD18 L1
FBA_CMD19 J9
FBA_ZQ6 L9
NC#J1 NC#L1 NC#J9 NC#L9
GND — 243/F_4 R1126

96-BALL SDRAM_DDR3
VRAM _DDR3_HYNIX_256MX16

stuff R1124 for
Hynix 8Gb DDP VRAM

DQL0 E3 … DQL7 H7
VMA_DQ34 [19] … VMA_DQ36 [19]
DQU0 D7 … DQU7 A3
VMA_DQ57 [19] … VMA_DQ60 [19]

VDD#B2 B2 … VDD#R9 R9
+1.5V_GFX — 4.7U/6.3V_6 C1115 — 0.1U/16V_4 C1116 — 0.1U/16V_4 C1117 — GND

VDDQ#A1 A1 … VDDQ#H9 H9
+1.5V_GFX — 4.7U/6.3V_6 C1121 — 0.1U/16V_4 C1122 — 0.1U/16V_4 C1123 — GND

VSS#A9 A9 … VSS#T9 T9
GND

VSSQ#B1 B1 … VSSQ#G9 G9

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

VMA_CLK1 — R1078 162/F_4 — VMA_CLK1#

+1.5V_GFX — R1081 1.33K/F_4 — VREFC_VMA3 — R1083 1.33K/F_4 — C1127 0.01U/50V_4
+1.5V_GFX — R1082 1.33K/F_4 — VREFD_VMA3 — R1084 1.33K/F_4 — C1128 0.01U/50V_4

+1.5V_GFX — C1134 1U/6.3V_4 — C1137 1U/6.3V_4 — C1139 1U/6.3V_4 — C1142 1U/6.3V_4
+1.5V_GFX — C1135 1U/6.3V_4 — C1138 1U/6.3V_4 — C1140 1U/6.3V_4 — C1143 1U/6.3V_4

+1.5V_GFX — C1129 10U/6.3V_6 — C1130 10U/6.3V_6 — C1131 10U/6.3V_6 — C1132 0.1U/16V_4 — C1133 0.1U/16V_4 — C1136 0.1U/16V_4 — C1141 0.1U/16V_4 — C1144 0.1U/16V_4 — C1145 0.1U/16V_4

U1007

VREFC_VMA3 M8 VREFCA
VREFD_VMA3 H1 VREFDQ

FBA_CMD9 N3
FBA_CMD11 P7
FBA_CMD8 P3
FBA_CMD25 N2
FBA_CMD10 P8
FBA_CMD24 P2
FBA_CMD22 R8
FBA_CMD7 R2
FBA_CMD21 T8
FBA_CMD6 R3
FBA_CMD29 L7
FBA_CMD23 R7
FBA_CMD28 N7
FBA_CMD20 T3
FBA_CMD4 T7
FBA_CMD14 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14 A15

FBA_CMD12 M2
FBA_CMD27 N8
FBA_CMD26 M3
BA0 BA1 BA2

VMA_CLK1 J7
VMA_CLK1# K7
FBA_CMD19 K9
CK CK CKE

FBA_CMD18 K1
FBA_CMD16 L2
FBA_CMD30 J3
FBA_CMJ15 K3
FBA_CMD13 L3
ODT CS RAS CAS WE

[19] VMA_WDQS5 F3
[19] VMA_RDQS5 G3
DQSL DQSL

[19] VMA_DM5 E7
[19] VMA_DM6 D3
DML DMU

[19] VMA_WDQS6 C7
[19] VMA_RDQS6 B7
DQSU DQSU

FBA_CMD5 T2
RESET

GND — FBA_ZQ5 — L8 ZQ — 243/F_4 R1080

FBA_CMD18 J1
FBA_CMD17 L1
FBA_CMD19 J9
FBA_ZQ7 L9
NC#J1 NC#L1 NC#J9 NC#L9
GND — 243/F_4 R1127

96-BALL SDRAM_DDR3
VRAM _DDR3_HYNIX_256MX16

stuff R1124 for
Hynix 8Gb DDP VRAM

DQL0 E3 … DQL7 H7
VMA_DQ41 [19] … VMA_DQ44 [19]
DQU0 D7 … DQU7 A3
VMA_DQ51 [19] … VMA_DQ53 [19]

VDD#B2 B2 … VDD#R9 R9
+1.5V_GFX — 4.7U/6.3V_6 C1118 — 0.1U/16V_4 C1119 — 0.1U/16V_4 C1120 — GND

VDDQ#A1 A1 … VDDQ#H9 H9
+1.5V_GFX — 4.7U/6.3V_6 C1124 — 0.1U/16V_4 C1125 — 0.1U/16V_4 C1126 — GND

VSS#A9 A9 … VSS#T9 T9
GND

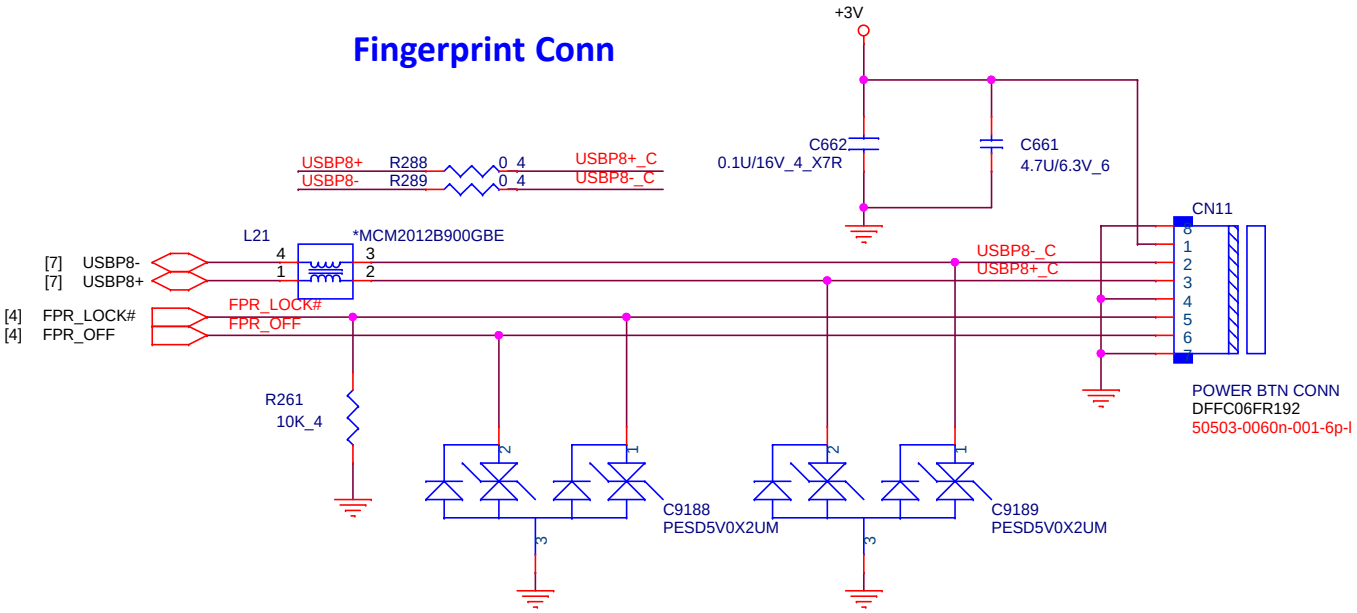
VSSQ#B1 B1 … VSSQ#G9 G9

NB5

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L - RANK0	1A
Date: Thursday, May 19, 2016	Sheet 23of 67	

Fingerprint Conn



NB5	**PROJECT : S400 Series** Quanta Computer Inc.	
Size: Custom	Document Number: **24 -- FPR**	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 24 of 67	

ALF@1119:
HP confirmed to remove the eDP to LVDS convertor.

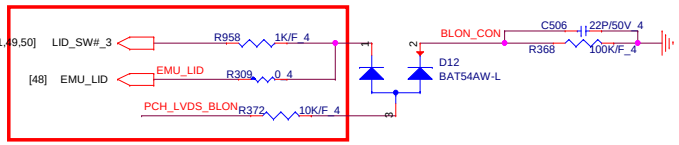
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V

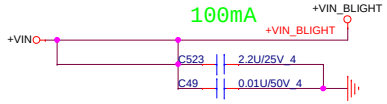
NB5

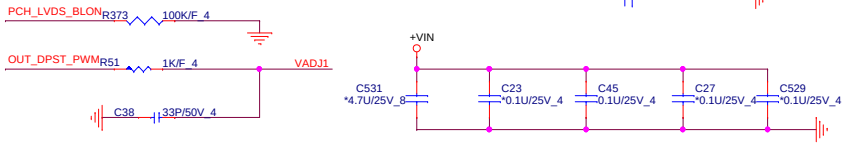
PROJECT : X63
Quanta Computer Inc.

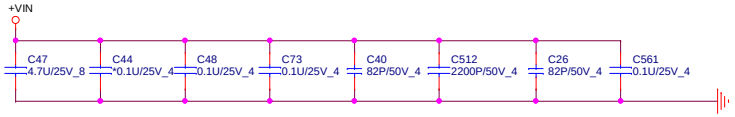
Size	Document Number	Rev
Custom	**25 -- LVDS converter RTD2136**	1A
Date: Thursday, May 19, 2016	Sheet 25 of 67	

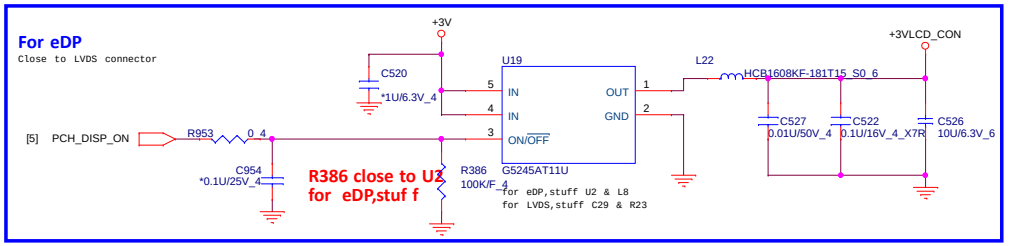
LID Switch

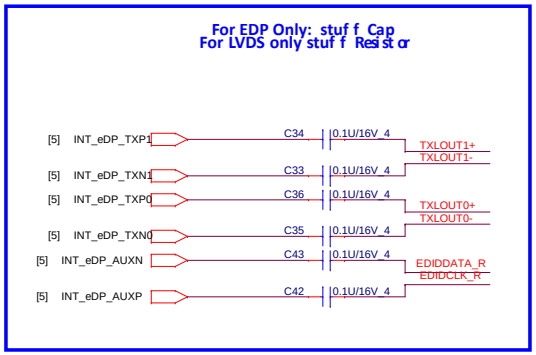


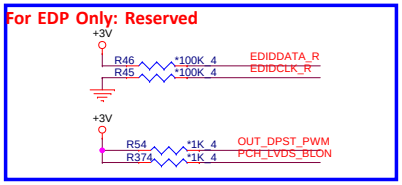


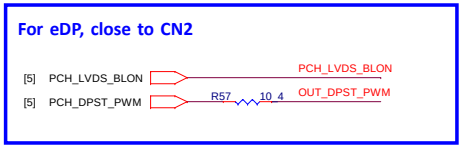


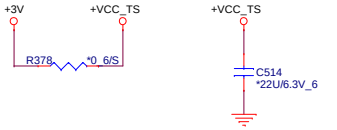




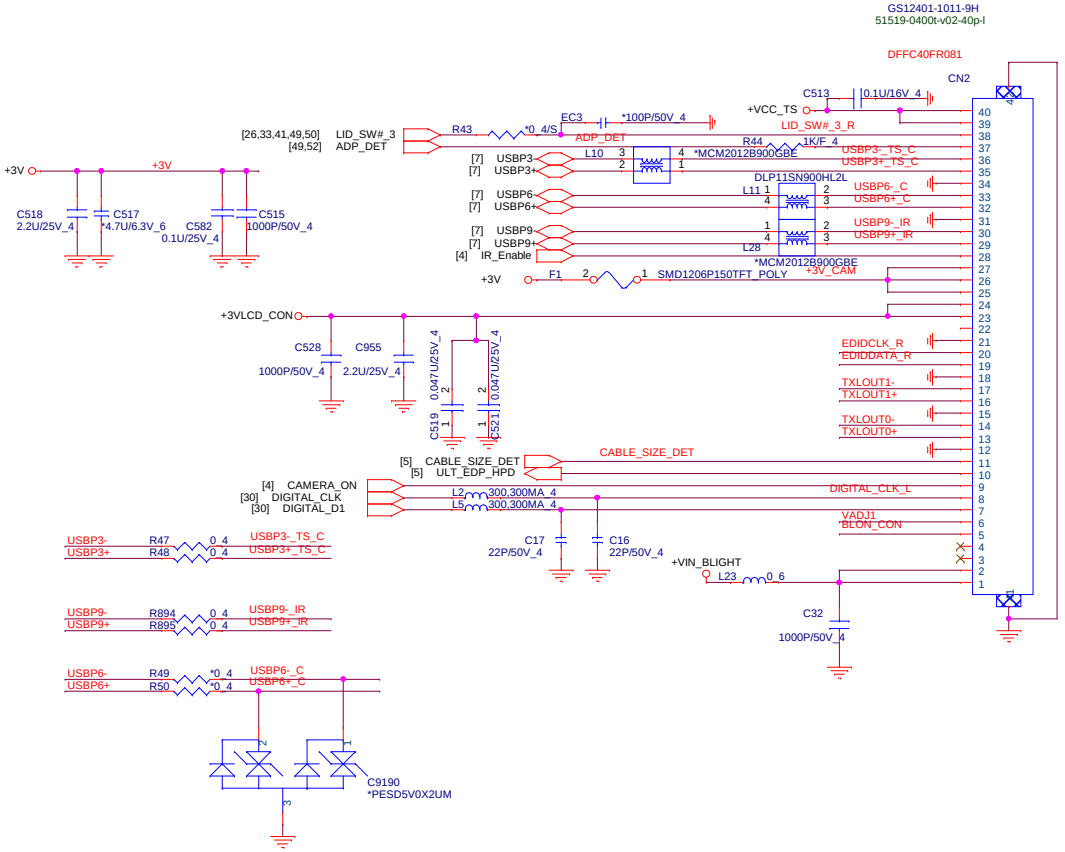








LVDS Conn.



[31,35,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67] +5VPCU
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V
[9,41,51,52,53,59,63,64,67] +3V_ALW
[8,27,29,30,40,42,43,55,59,64,67] +5V
[43,47,52,53,54,55,56,57,58,59,60,62,67] +VIN

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	26 -- LCD CONN/LID/CAM/D-MIC	1A

NB5

Date: Thursday, May 19, 2016 Sheet 26 of 67

To:
DP Switch's HPD Input Port

[5] DDI_HPD_CON

Pull down at SOC side

From:
DP Switch's Main Link
and AUXLink Port

[5] INT_DDI2_AUXP
[5] INT_DDI2_AUXN
[5] DDI2_TX0_P
[5] DDI2_TX0_N
[5] DDI2_TX1_P
[5] DDI2_TX1_N

R1530 0_4 INT_DDI1_AUXP_C
R1531 0_4 INT_DDI1_AUXN_C
R1532 *1M_4 100K_4 INT_DDI1_AUXP_C
R1533 *100K_4 *1M_4 INT_DDI1_AUXN_C

L15 PBY160808T-600Y-N(60,3A)

C596 0.1U/16V/X7R_4 RXAUXP
C598 0.1U/16V/X7R_4 RXAUXN
C595 0.1U/16V/X7R_4 VCCK_V12
C603 0.1U/16V/X7R_4 RRX0P
C606 0.1U/16V/X7R_4 RRX0N
C611 0.1U/16V/X7R_4 RRX1P
C617 0.1U/16V/X7R_4 RRX1N

U1008

RTD2166

AVCC33 AVCC_33 AUX_P AUX_N AVCC_12 LANE0_P LANE0_N LANE1_P LANE1_N
EPAD HPD EXT1.2V_CTRL SMB_SCL SMB_SDA XI LDO_RSTB PVCC_33 VCCK_12
POL2 POL1/SPI_CEB SPI_CLK SPI_SI SPI_SO VCC_33 VGA_SCL VGA_SDA
GND RED_P GREEN_P BLUE_P VDD_DAC_33 HSYNC VSYNC HVSYNC_PWR

FCH_3S_SMCLK FCH_3S_SMDATA

C293 0.1U/16V/X7R_4
C262 0.1U/25V_4
C263 2.2U/10V_4

11/10 vendor recommend change X7R to X5R

CRT_R R557 75/F_4
CRT_G R568 75/F_4
CRT_B R586 75/F_4
VDD_DAC_33 L16 PBY160808T-600Y-N(60,3A)
HSYNC R598 47_4 CRTHSYNC
VSYNC R613 47_4 CRTVSYNC

C950 0.1U/16V/X7R_4
C290 0.1U/16V/X7R_4
C278 4.7U/6.3V_4

RTD2166-CG
R887 4.7K_4
R888 4.7K_4
DDCDAT3
DDCCLK3
TP1012
TP1011 TP1010

R1543 *100K_4 SPI_SI

D9 BAV99W CRT_R1
D8 BAV99W CRT_G1
D7 BAV99W CRT_B1
D17 *BAV99W DDCCLK3
D16 *BAV99W CRTVSYNC
D15 *BAV99W CRTHSYNC
D19 *BAV99W DDCDAT3

R649 2.2K/J_4 +5VCRT2
D10 MEK500V-40 +5V_HDMIC
R625 2.2K/J_4
DDCDAT3
DDCCLK3

40 MIL
C676 0.1U/16V_4_X7R
SSM14 spec is 40V 1A

CRT_R L20 BLM15BB750SN1D(75,300MA) CRT_R1
CRT_G L19 BLM15BB750SN1D(75,300MA) CRT_G1
CRT_B L18 BLM15BB750SN1D(75,300MA) CRT_B1
+5V_HDMIC

C350 *22P/50V_4
C312 *22P/50V_4
C301 *22P/50V_4
C302 5.6P/50V_4
C319 5.6P/50V_4
C358 5.6P/50V_4

DDCDAT3 C652 *470P/50V_4
CRTHSYNC C619 *2P/50V_4
CRTVSYNC C628 *2P/50V_4
DDCCLK3 C638 *470P/50V_4

04/25 vendor recommend change 33pF to 2pF

EMI
CRT CONN
CN20

Need check footprint and PN
DFDS15FR456
dsub-10556-15002-15p

FCH_3S_SMCLK, FCH_3S_SMDATA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
ROM or EEPROM mode: connect to PCH SMBUS
IIC Protocol is used

RTD2168 Slave Address:
0x64/0x65 and 0x68/0x69

From PCH

[3,16,17,50] PCH_SMBDATA R627 0_4 FCH_3S_SMDATA
[3,16,17,50] PCH_SMBCLK R623 0_4 FCH_3S_SMCLK

NB5

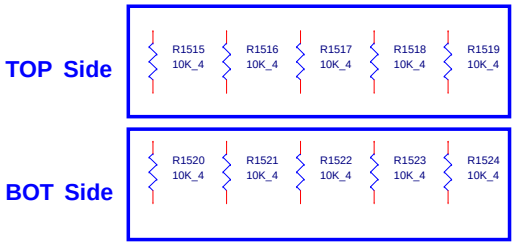
PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 -- DP2VGA_converter	1A

Date: Thursday, May 19, 2016 | Sheet 27 of 67

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB

Add Dummy ID



OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

NB5

PROJECT : X63
Quanta Computer Inc.

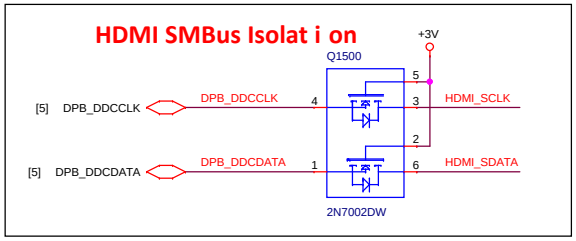
Size	Document Number	Rev
Custom	28 – REPEATER PTN3366	1A

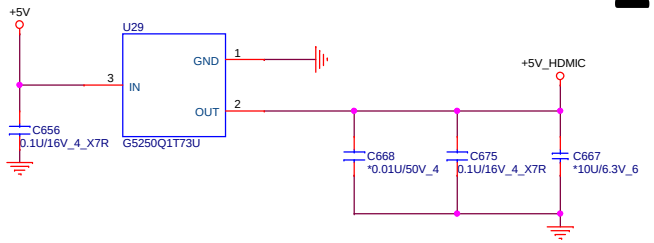
Date: Thursday, May 19, 2016 | Sheet 28 of 67

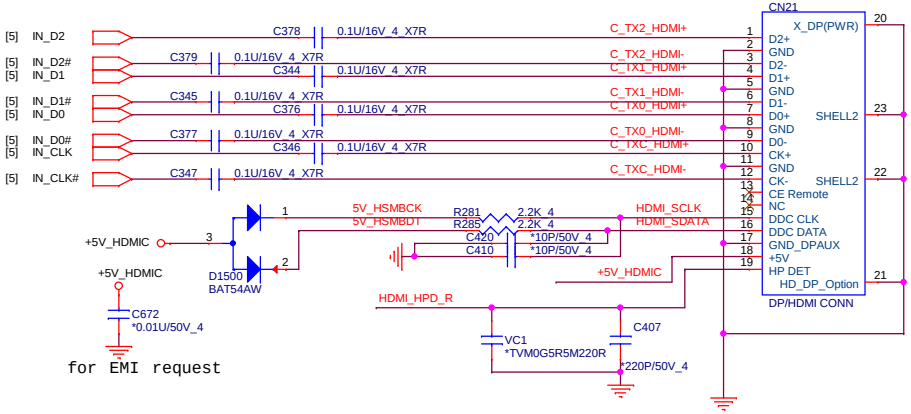
EMI Solut i on

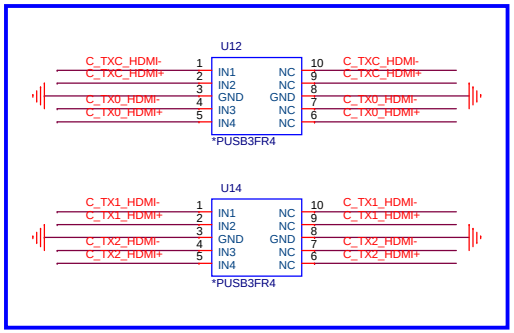
C_TX2_HDMI+	R304 150/F_4	C_TX2_HDMI-	
C_TX1_HDMI+	R291 150/F_4	C_TX1_HDMI-	
C_TX0_HDMI+	R295 150/F_4	C_TX0_HDMI-	
C_TXC_HDMI+	R299 150/F_4	C_TXC_HDMI-	

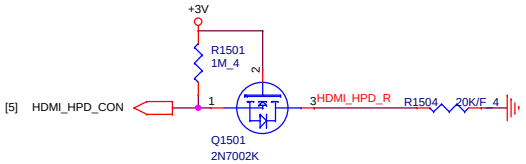
HDMI SMBus Isolat i on

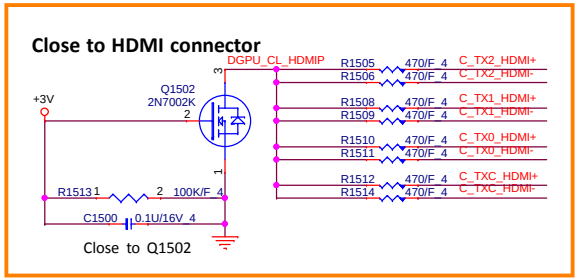






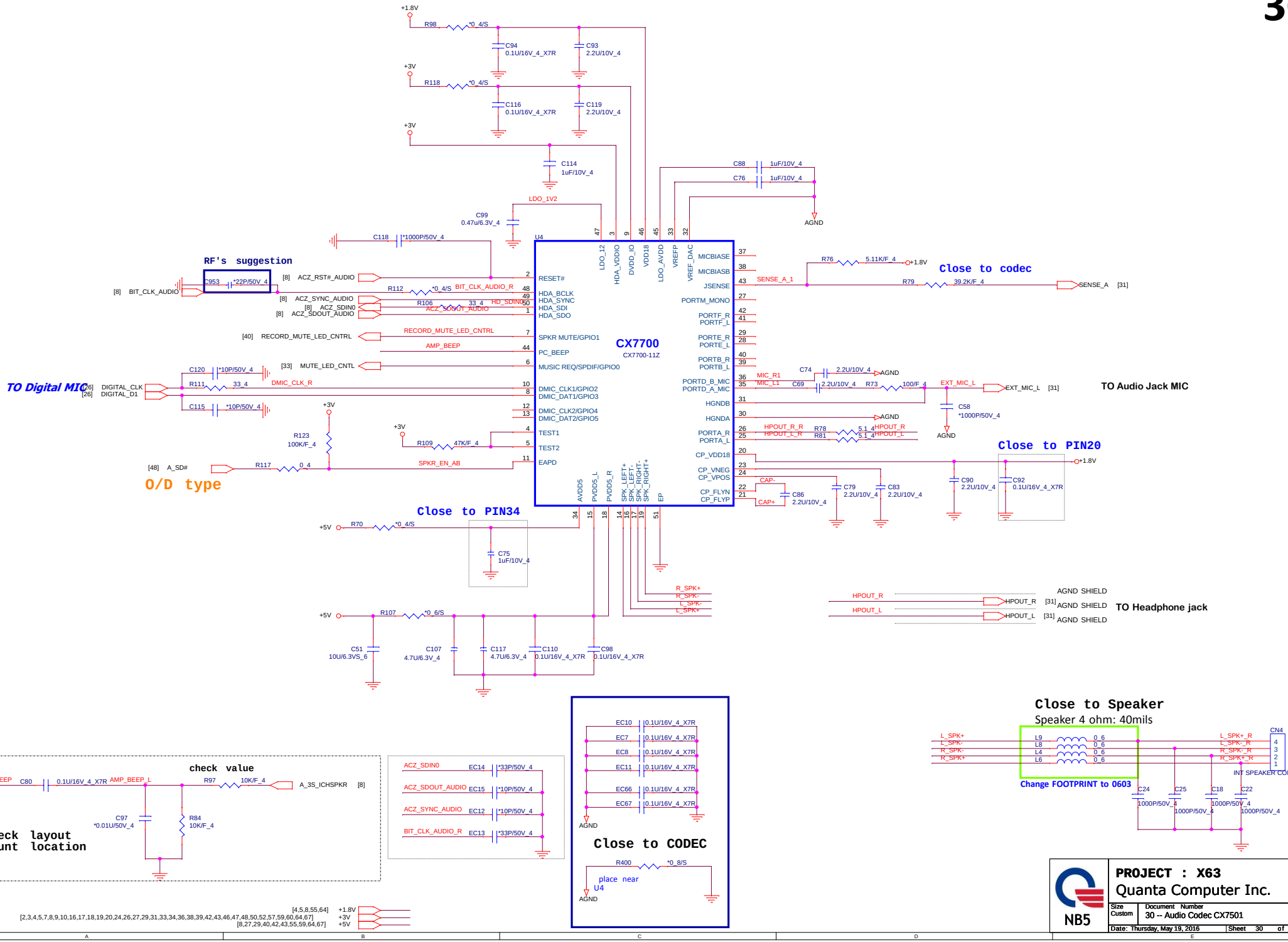






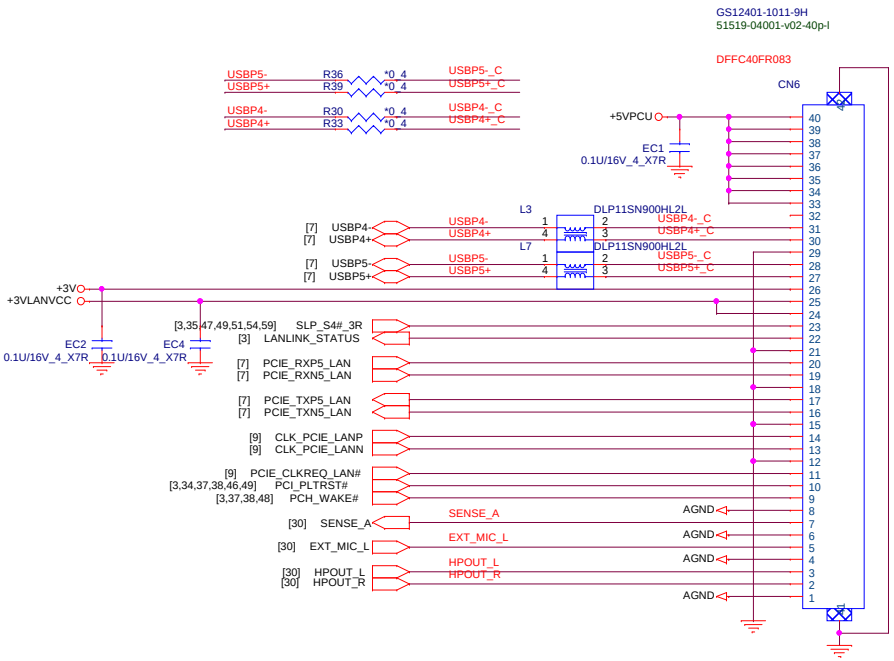
NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 29 -- HDMI CONNECTOR	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 29 of 67	

Audio Codec



NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 30 -- Audio Codec CX7501	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 30 of 67	

USB2.0 x2/LAN/Headphone_Mic Combo Jack Daugther Board Connector



NB5	**PROJECT : X63** Quanta Computer Inc.	
Size: Custom	Document Number: 31 -- DAUGTHER BOARD CONN.	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 31 of 67	

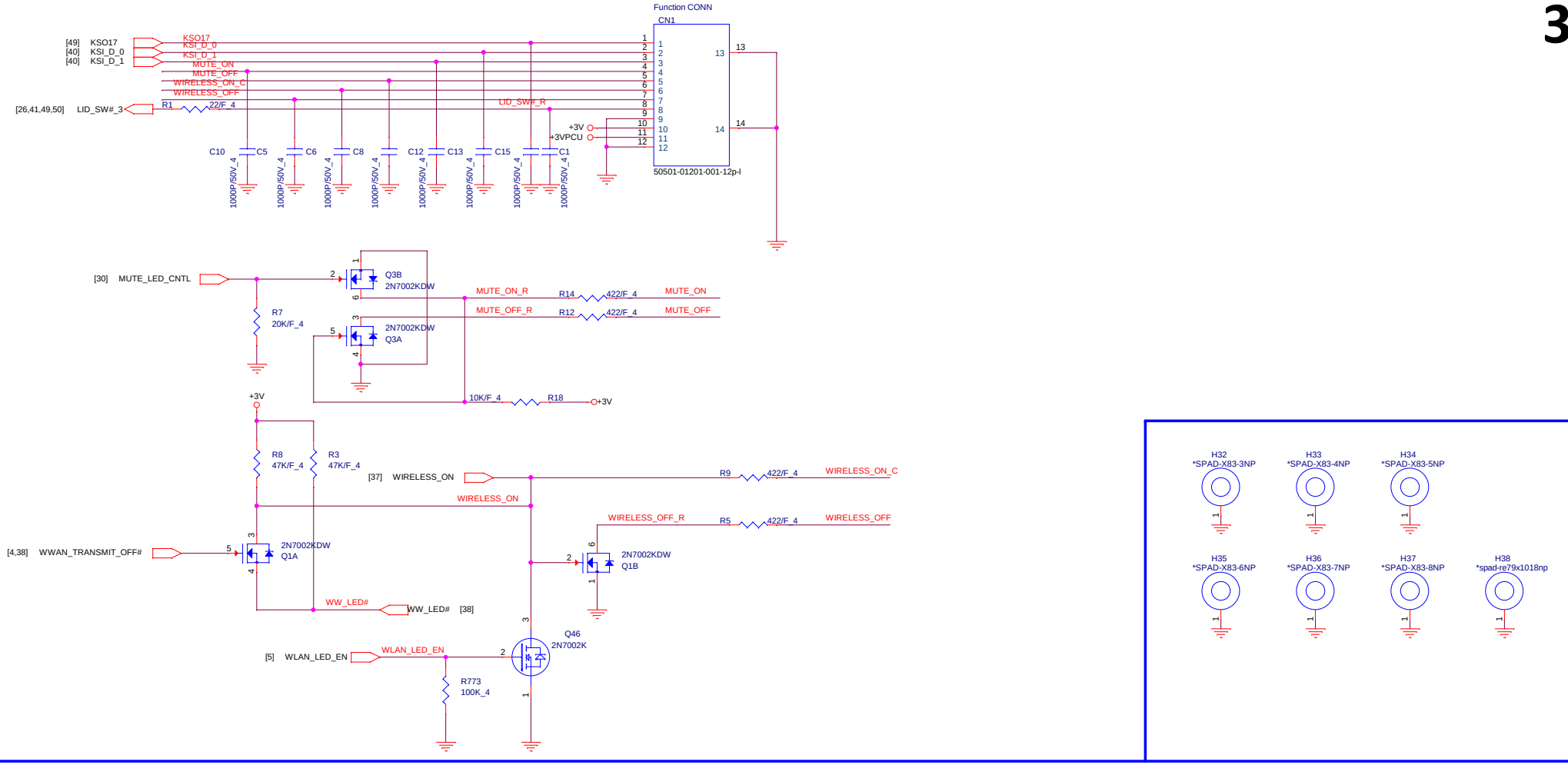
NB5

PROJECT : X63

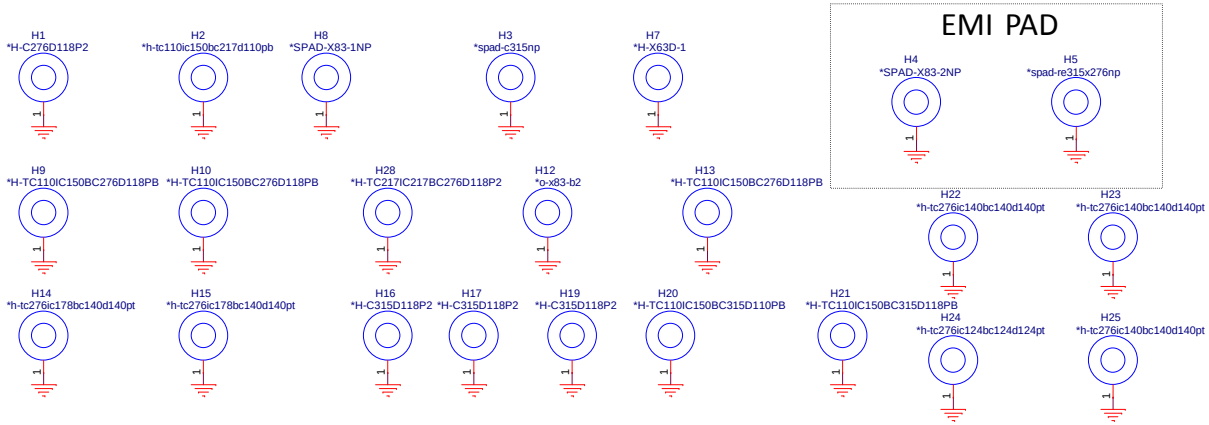
Quanta Computer Inc.

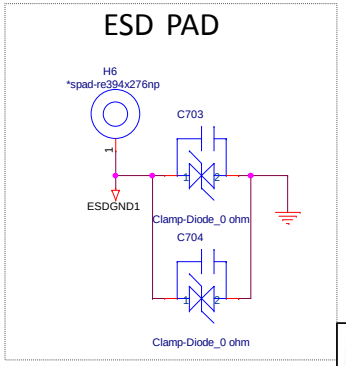
Size	Document Number	Rev
C	32 – Reserved	1A

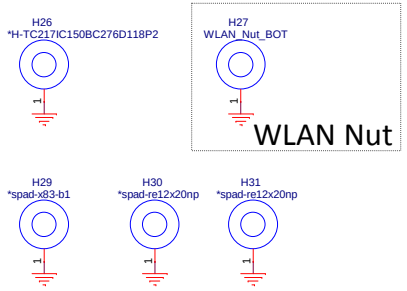
Date: Thursday, May 19, 2016 | Sheet 32 of 67



Hole







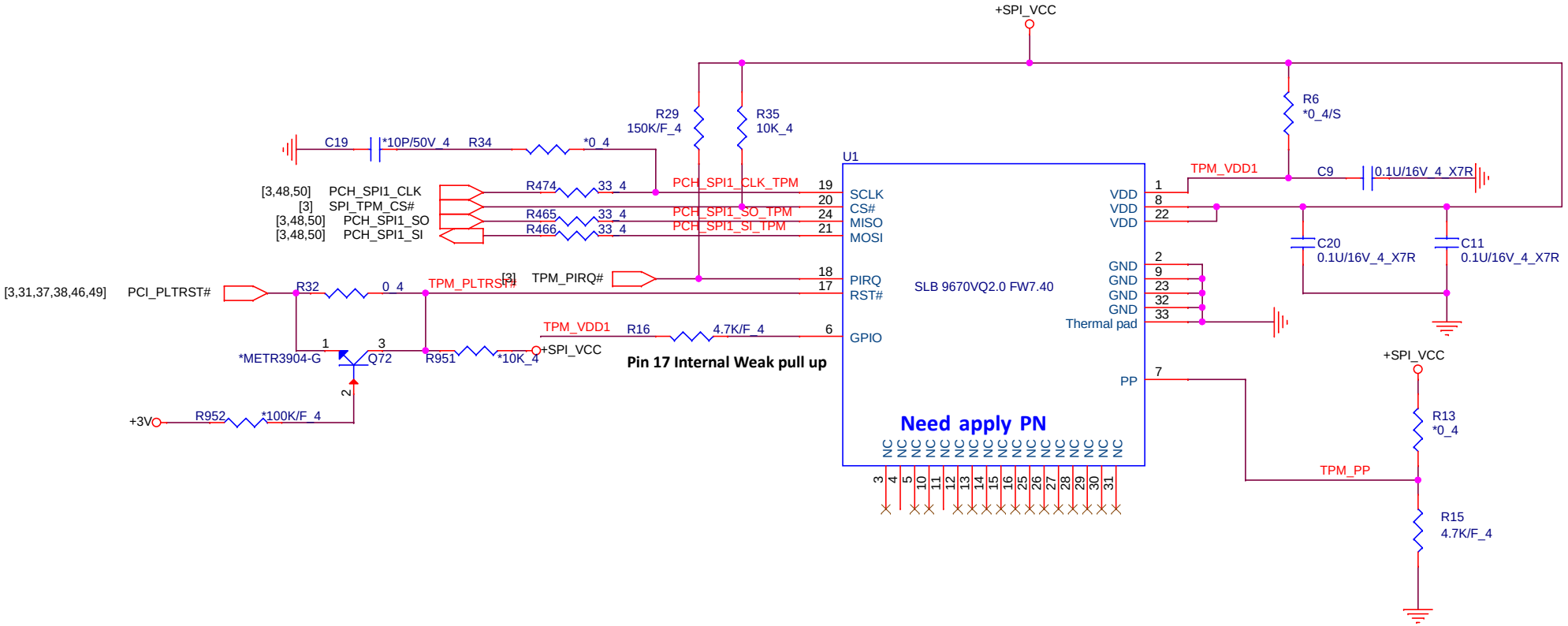
NB5

PROJECT : X63

Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- Function Conn./Hole	1A
Date: Thursday, May 19, 2016	Sheet 33 of 67	

TPM (1.2 or 2.0)



NB5

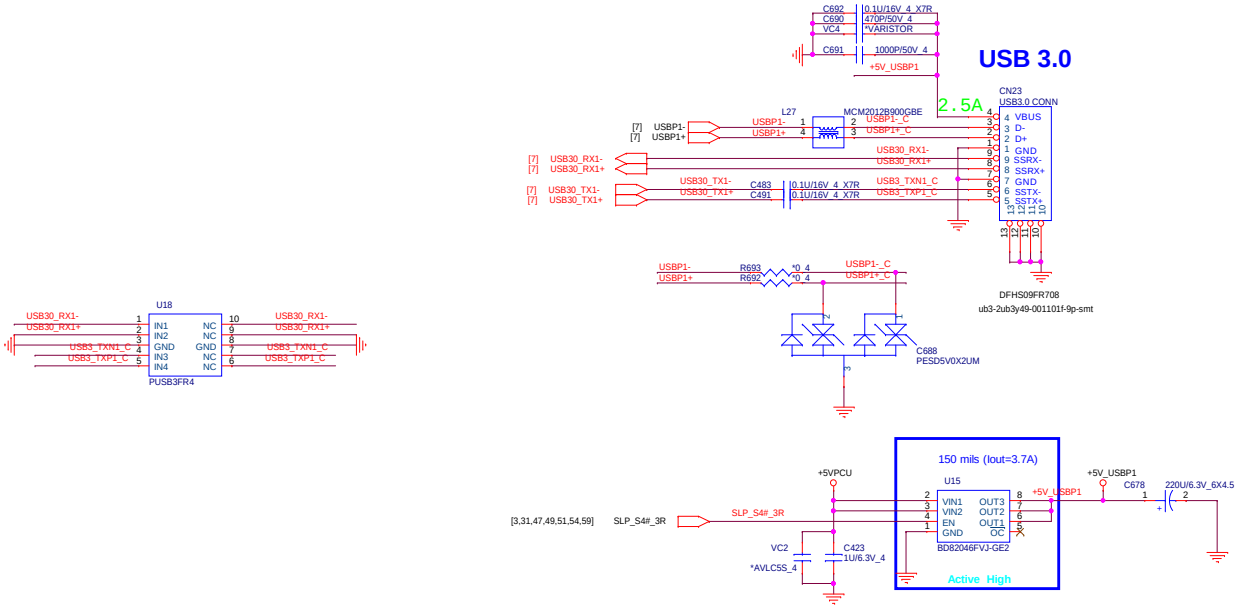
PROJECT : X63

Quanta Computer Inc.

Size	Document Number	Rev
Custom	34 -- TPM SLB9670_QFN	1A

Date: Thursday, May 19, 2016 Sheet 34 of 67

USB 2.0/3.0 Combo

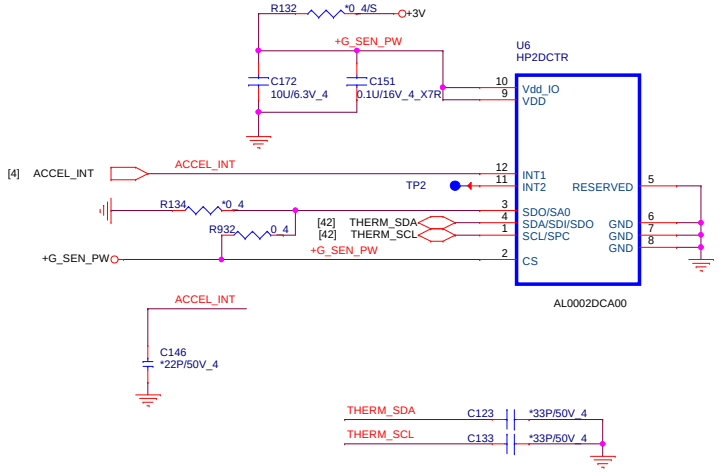


[31,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67] +5VPCU
[9,41,51,52,53,59,63,64,67] +3V_ALW

NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 35 -- USB3.0 x2	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 35 of 67	

Accelerometer Sensor

G-Sensor Power need check

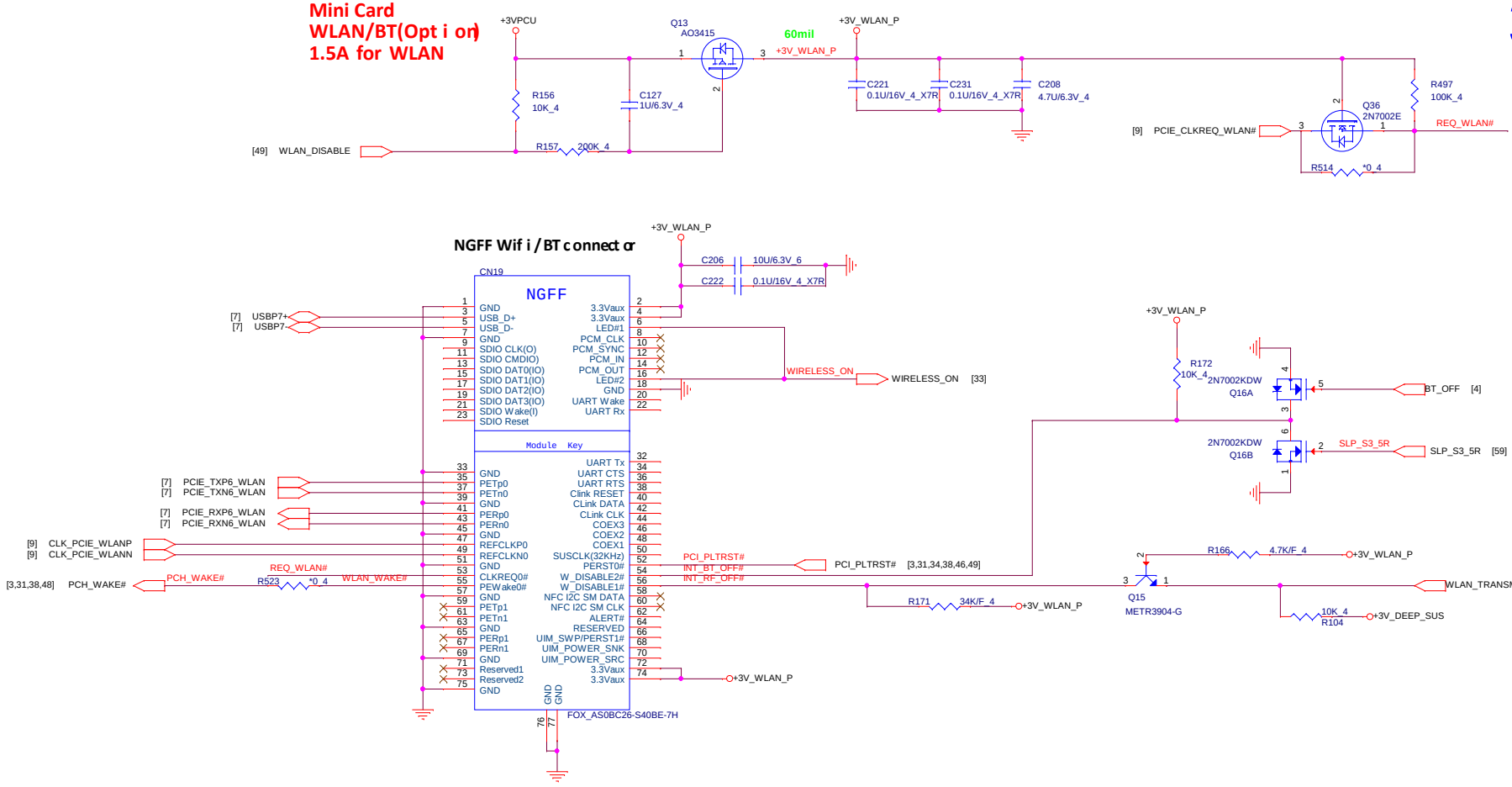


[31,35,44,45,46,47,52,53,54,55,57,58,59,60,61,62,64,67] +5VPCU
[9,41,51,52,53,59,63,64,67] +3V_ALW

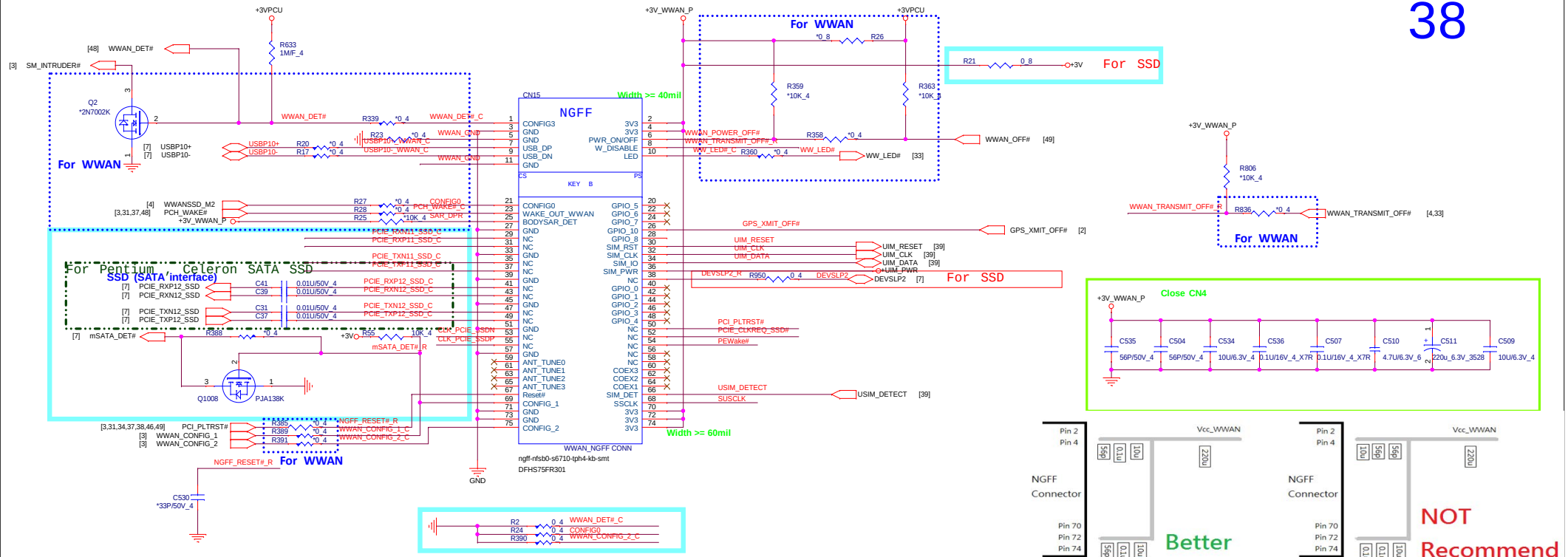
NB5	**PROJECT : X63** Quanta Computer Inc.	
Size: Custom	Document Number: **36 -- TS and Accelerometer**	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 36 of 67	

NGFF WLAN/BT

Mini Card
WLAN/BT(Opti on)
1.5A for WLAN



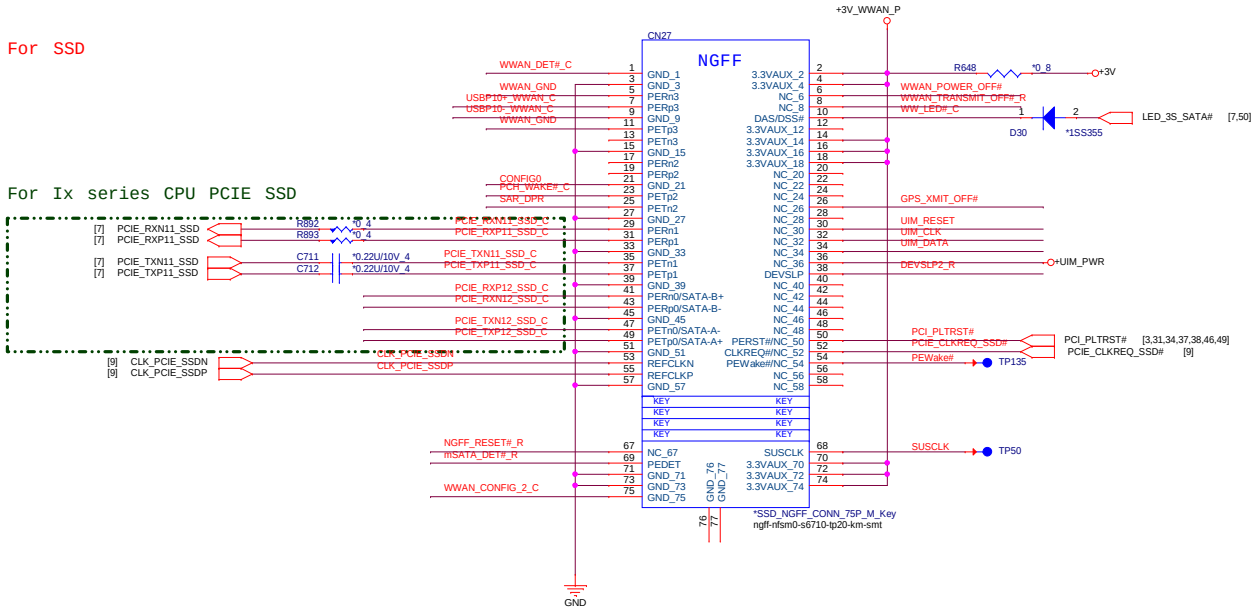
NB5	**PROJECT : X63** Quanta Computer Inc.
Size: Custom	Document Number: **37 -- NGFF WLAN/BT** — Rev: 1A
Date: Thursday, May 19, 2016	Sheet 37 of 67



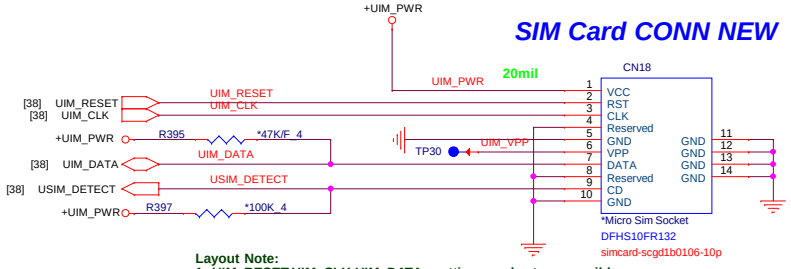
WWAN(Opt i on)
Control of power must be allowed in all S0, S3, S4 and S5 states.

	M.2 Pinout	S0	S3 – S5
WWAN 3.3V	2, 4, 70, 72, 74	On	Off

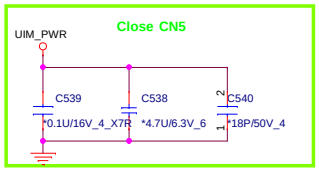
	+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0	ON	High	High	High
S3	ON	High	Low	Low
S4	ON	Low	Low	Low
S5	ON	Low	Low	Low

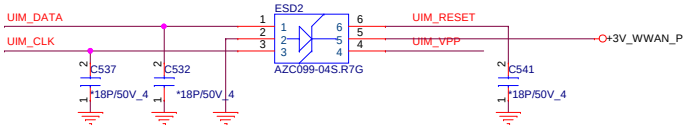


NB5	**PROJECT : X63** Quanta Computer Inc. Size: Custom Document Number: 38 -- WWAN NGFF/ SSD Rev: 1A Date: Thursday, May 19, 2016 Sheet 38 of 67



Layout Note:
1. UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible Roue into ESD then go out
2. Avoid routing the SIM_CLK and SIM_DATA lines in parallel over distances >= 2 cm
3. Position the SIM connector from the WWAN module <= 100mm if possible, NOT exceed length is 150mm.



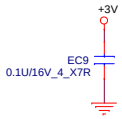


Trace Length and Routing

- Special attention should be paid to SIM traces (UIM_CLK, UIM_DATA and UIM_RST) to minimize the trace lengths between the SIM slot and the WAN NGFF slot. **Minimizing the signal lengths and traces will reduce possibility of SIM signal integrity issues.** Recommended maximum length is 100mm. Not to exceed length is 150mm.
- Minimum distance between UIM_CLK and UIM_DATA should be 20 mils. Static signals such as UIM_RST can be routed between UIM_CLK and UIM_DATA to conserve space if needed.
- It is recommended that SIM traces be isolated from other high-speed switching signals, as noise can couple into the SIM signals. Keep a minimum distance of 20 mils between UIM_CLK, UIM_DATA and any other high-speed switching signals.
- Placing the SIM card on a daughter card is also not recommended as the interconnect may impact SIM signal integrity.

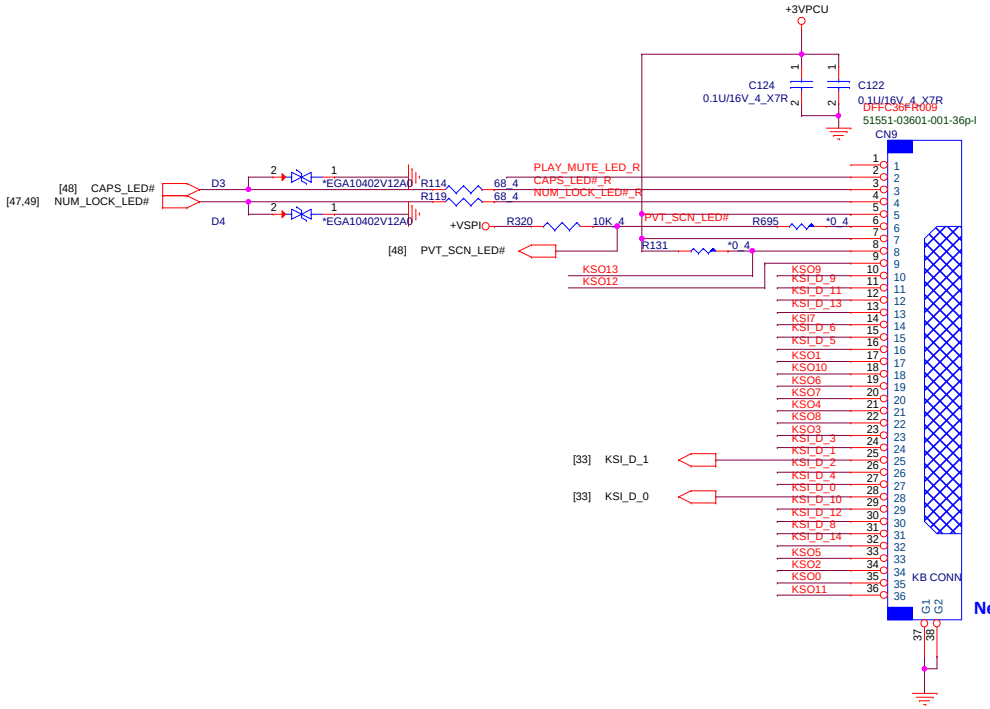
SIM Power

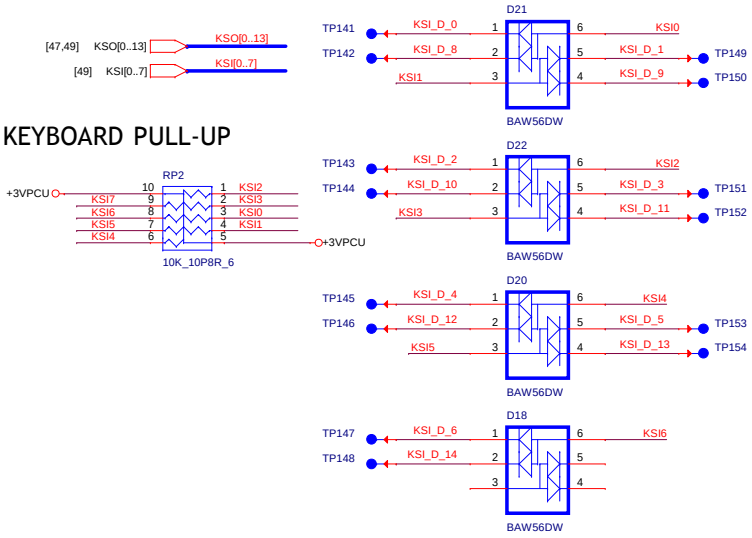
- The UIM_PWR trace width must be at least 20 mils. Sub-planar routing is recommended.
- Implement additional power filtering to SIM card power to ensure clean power is supplied to minimize any possible noise ripple effects. At a minimum, place a 0.1uF and a 4.7uF capacitor on the UIM_PWR supply and locate near the SIM connector.

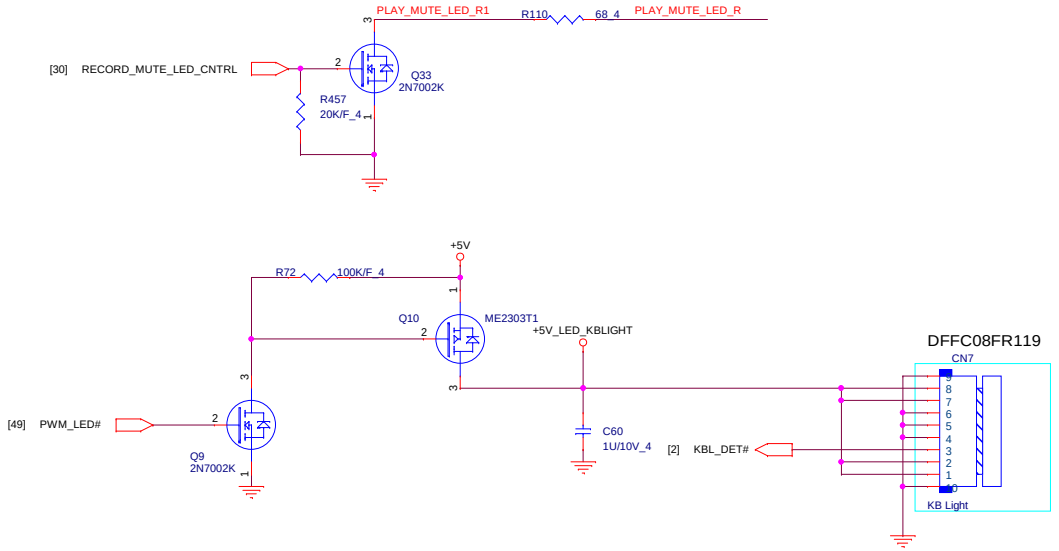


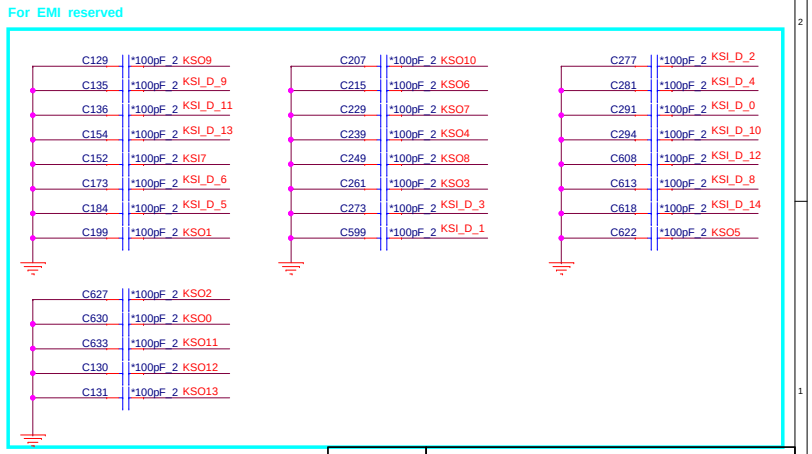
NB5	**PROJECT : X63** Quanta Computer Inc.	
Size: Custom	Document Number: 39 -- SIM CARD/ RF cap	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 39 of 67	

KEYBOARD Con.









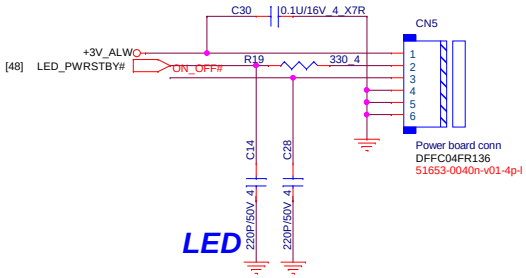
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V
[8,27,29,30,42,43,55,59,64,67] +5V
[9,41,51,52,53,59,63,64,67] +3V_ALW

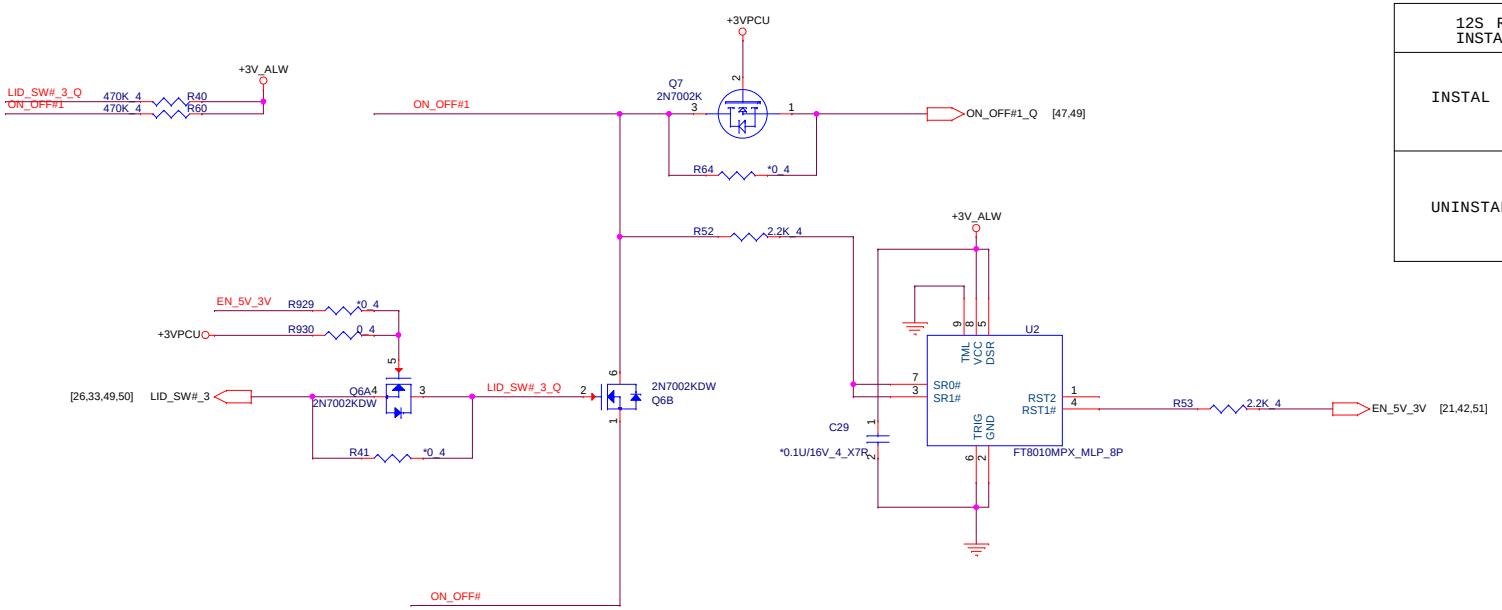
NB5

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	40 -- KB/ KB light CONN	1A
Date: Thursday, May 19, 2016	Sheet 40 of 67	

Power Bot t on Connect or





12S RESET MODE INSTAL FOR DB0	
INSTAL	R10702 R10703 R10704 R? R10701 R? U9068
UNINSTAL	R? R? Q7080 Q7081

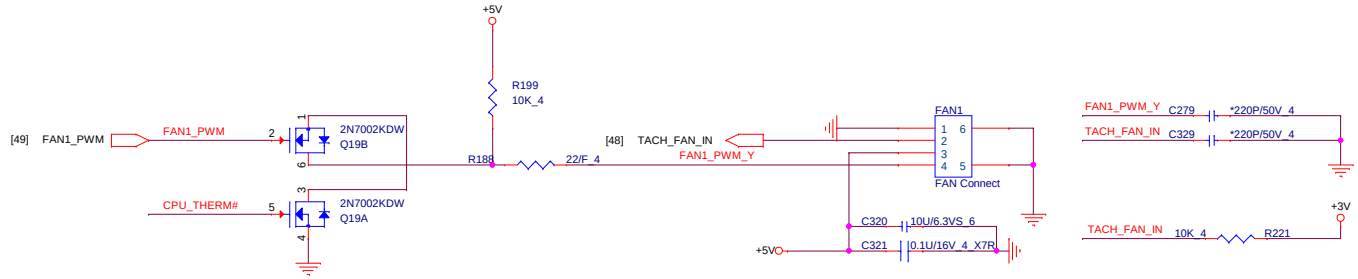
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,64,67] +3V
[8,27,29,30,40,42,43,55,59,64,67] +5V
[9,51,52,53,59,63,64,67] +3V_ALW

NB5

PROJECT : X63
Quanta Computer Inc.

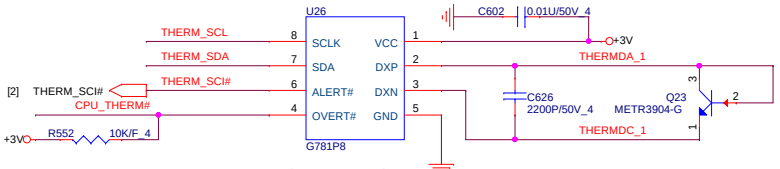
Size	Document Number	Rev
Custom	41 -- Power Button/ HW Reset	1A
Date: Thursday, May 19, 2016	Sheet 41 of 67	

FAN



Thermal sensor

CPU Thermal Sensor

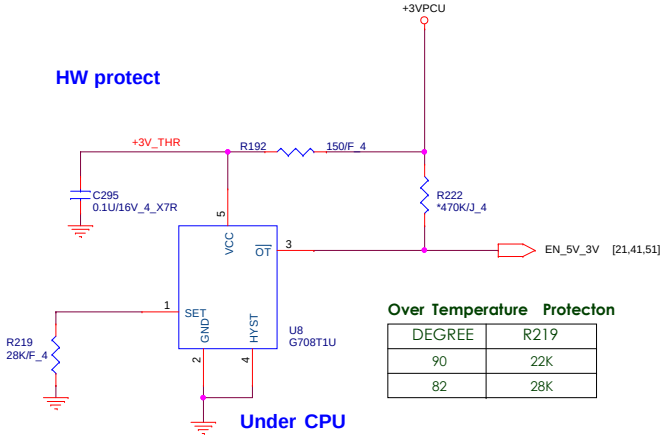


Under Heat Pipe

Main: AL000781012 G781P8(98h)

2nd:AL000431014 TMP431ADGKR

HW protect

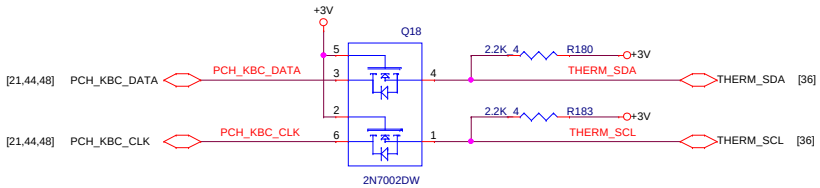


Under CPU

Over Temperature Protecton

DEGREE	R219
90	22K
82	28K

RSET (K OHM) = 0.0012T^2 - 0.9308T + 96.147



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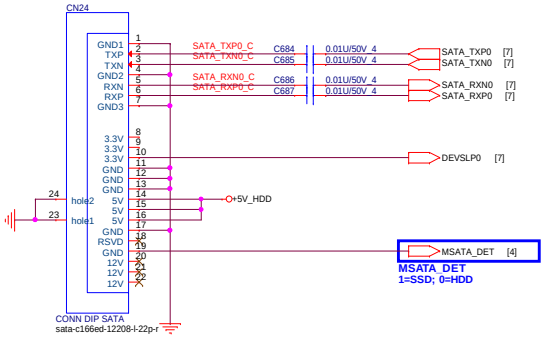
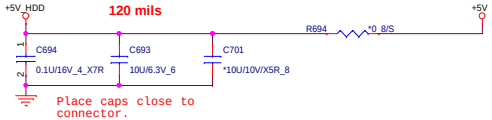
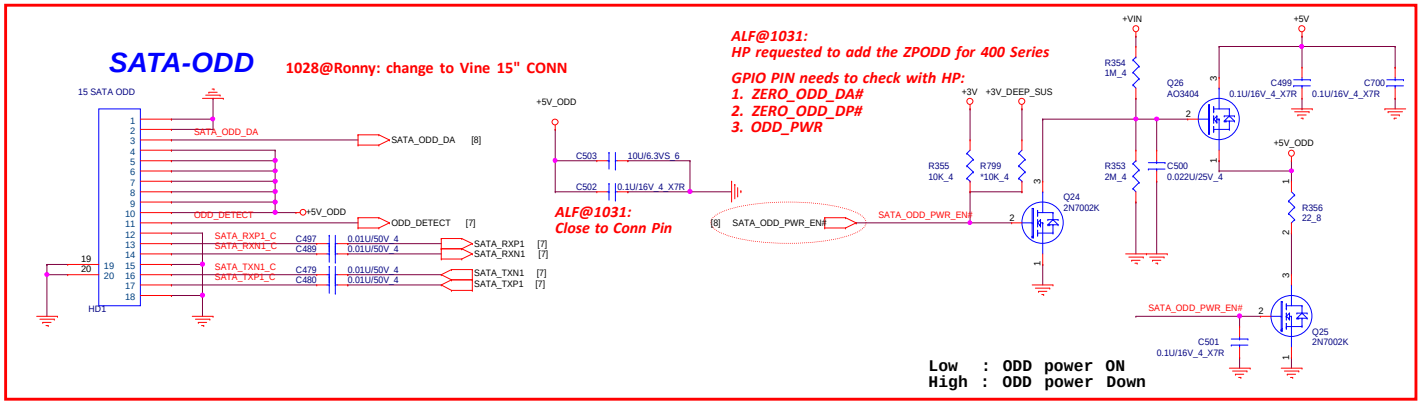
[9,41,51,52,53,59,63,64,67] +3V_ALW

NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 42-- FAN and Thermal IC	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 42 of 67	

SATA-HDD







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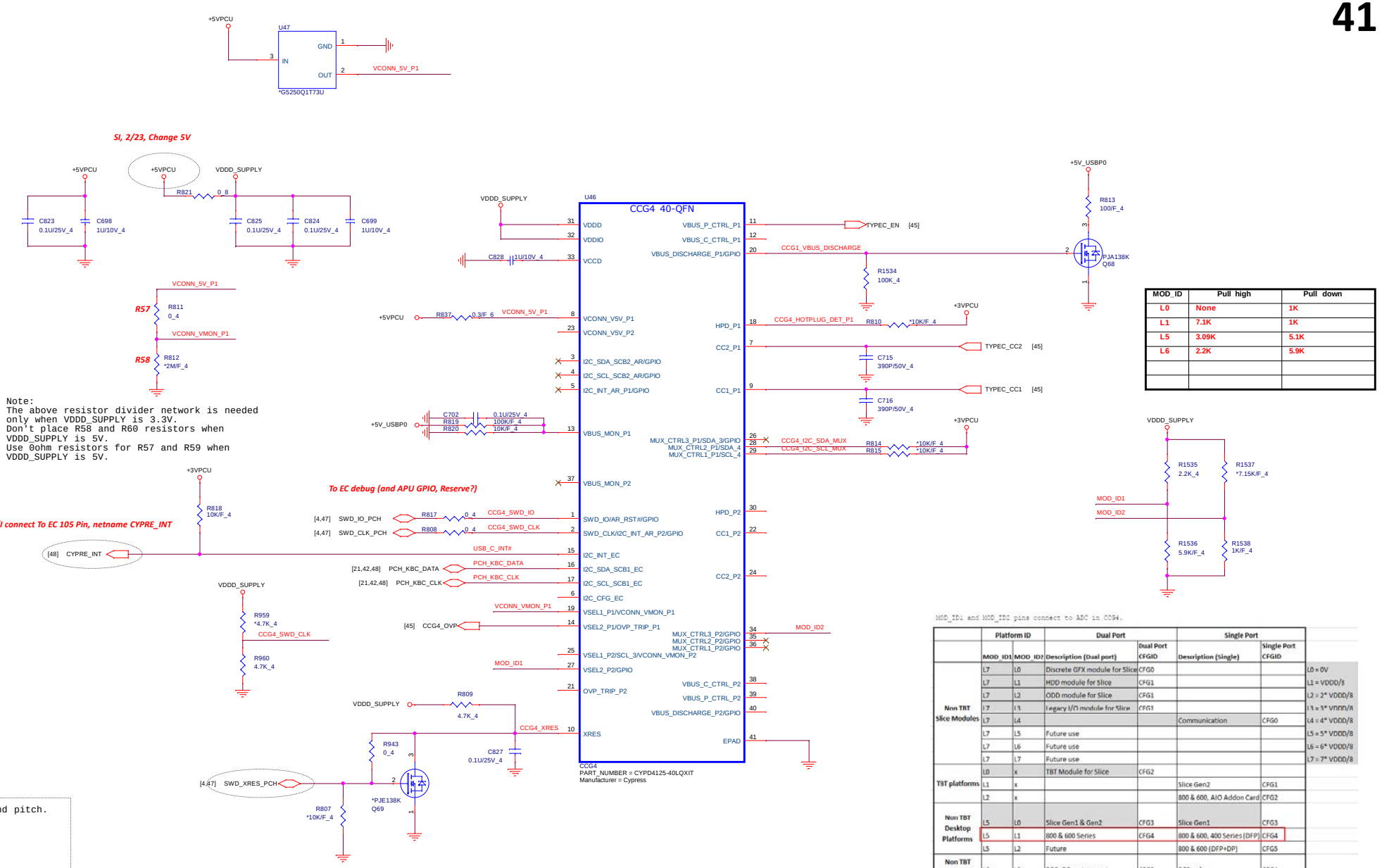
[8,27,29,30,40,42,55,59,64,67] +5V
[9,41,51,52,53,59,63,64,67] +3V_ALW

NB5	PROJECT : X63 Quanta Computer Inc.	
Size C	Document Number 43 -- HDD/ EMI cap	Rev 1A
Date: Thursday, May 19, 2016	Sheet 43 of 67	

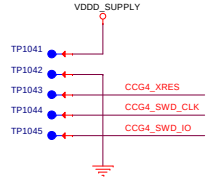


MOD_ID	Pull high	Pull down
L0	None	1K
L1	7.1K	1K
L5	3.09K	5.1K
L6	2.2K	5.9K

MOD_ID1 and MOD_ID2 pins connect to ADC in CCG4.

	Platform ID		Dual Port		Single Port		
	MOD_ID1	MOD_ID2	Description (Dual port)	Dual Port CFGID	Description (Single)	Single Port CFGID	
Non TBT Slice Modules	L7	L0	Discrete GFX module for Slice	CFG0			L0 = 0V
	L7	L1	HDD module for Slice	CFG1			L1 = VDDD/3
	L7	L2	ODD module for Slice	CFG1			L2 = 2* VDDD/8
	L7	L3	Legacy I/O module for Slice	CFG1			L3 = 3* VDDD/8
	L7	L4			Communication	CFG0	L4 = 4* VDDD/8
	L7	L5	Future use				L5 = 5* VDDD/8
	L7	L6	Future use				L6 = 6* VDDD/8
	L7	L7	Future use				L7 = 7* VDDD/8
TBT platforms	L0	x	TBT Module for Slice	CFG2			
	L1	x			Slice Gen2	CFG1	
	L2	x			800 & 600, AIO Addon Card	CFG2	
Non TBT Desktop Platforms	L5	L0	Slice Gen1 & Gen2	CFG3	Slice Gen1	CFG3	
	L5	L1	800 & 600 Series	CFG4	800 & 600, 400 Series (DFP)	CFG4	
	L5	L2	Future		800 & 600 (DFP+DP)	CFG5	
Non TBT Notebook Platforms	L6	L0	DRP+DP on two ports	CFG5	DFP only	CFG4	
	L6	L1			DFP + DP on single port	CFG5	

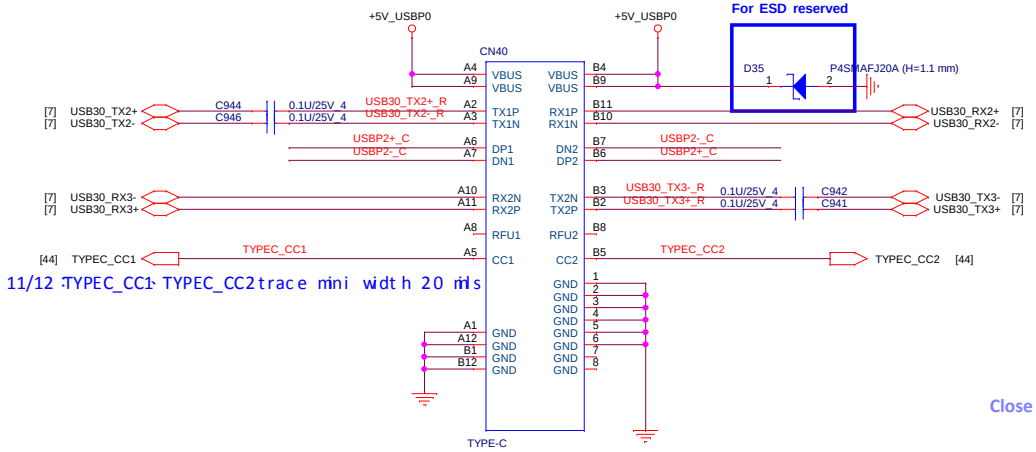
test points sequence and pitch.
(2.54mm with PHY 1.02)

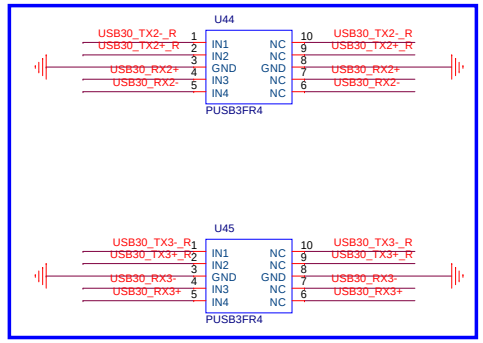


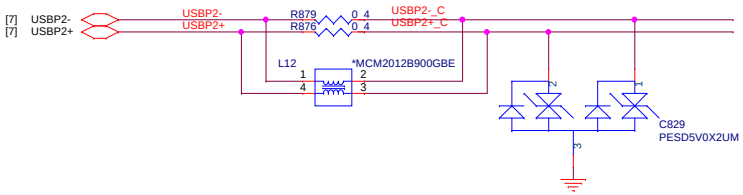
PROJECT:400 Series
Quanta Computer Inc.

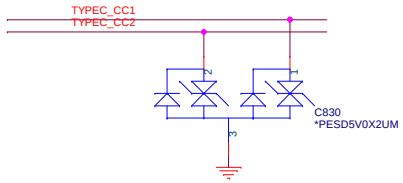
Size	Document Number	Rev
	44 -- Cypress CCG4	1A
Date: Thursday, May 19, 2016	Sheet 44 of 67	

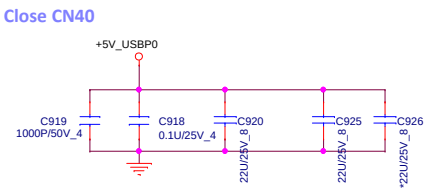
NB5

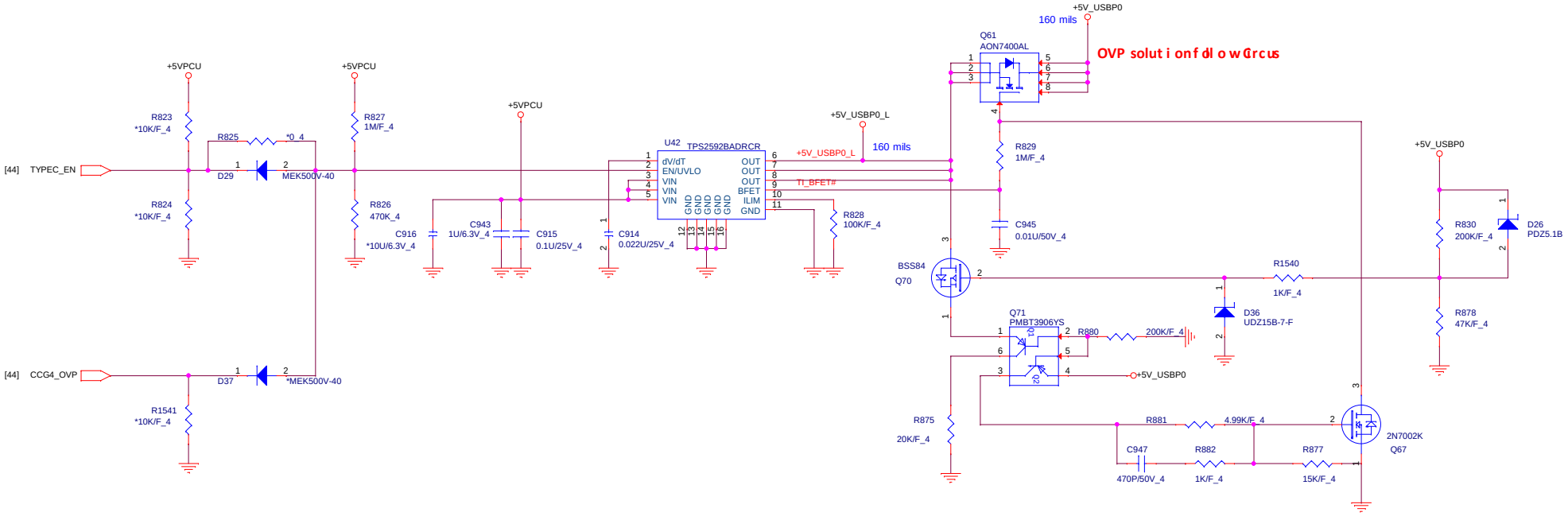




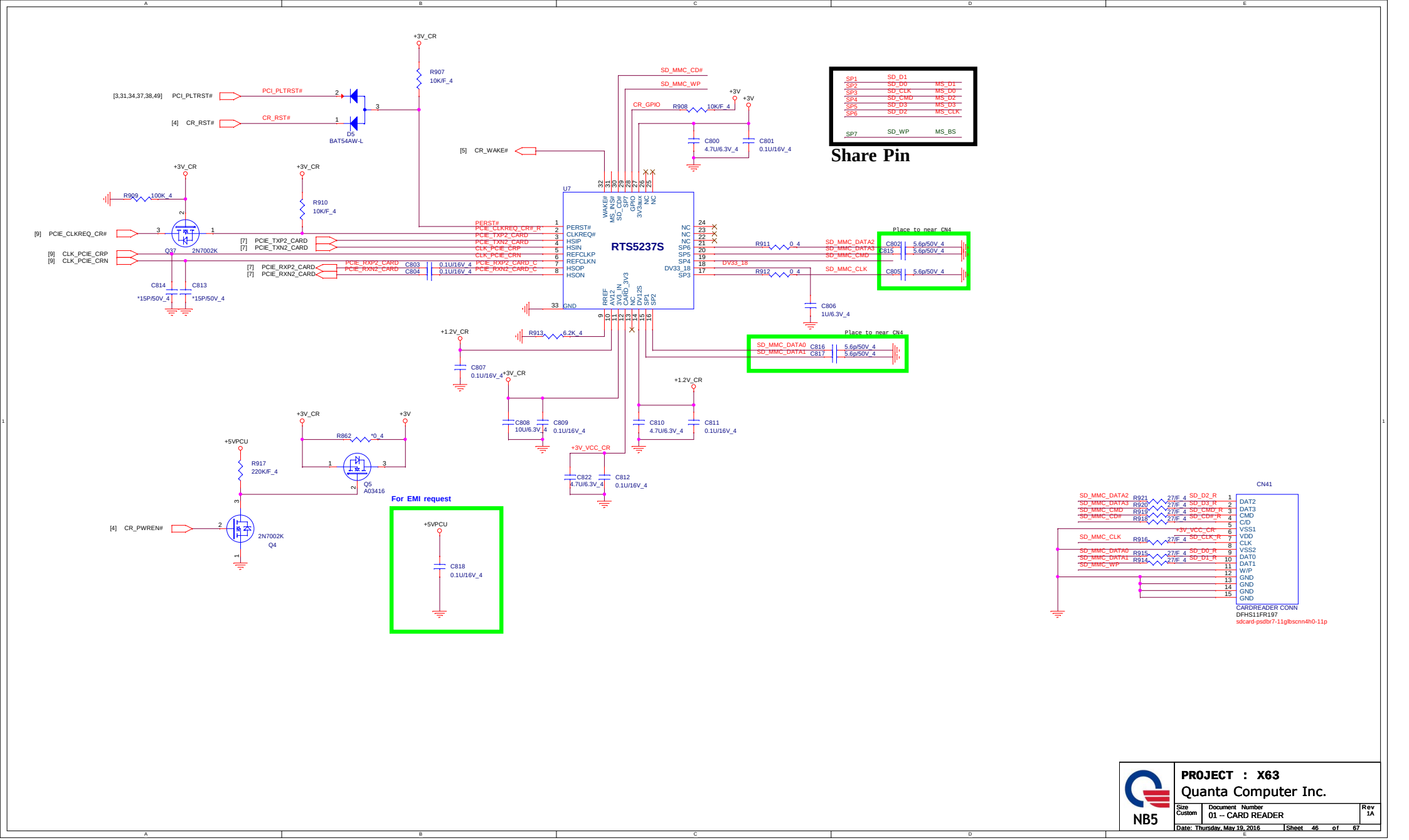








NB5	PROJECT : X63 Quanta Computer Inc.	
Size	Document Number TYPE-C	Rev 1A
Date: Thursday, May 19, 2016	Sheet 45 of 67	



PROJECT : X63

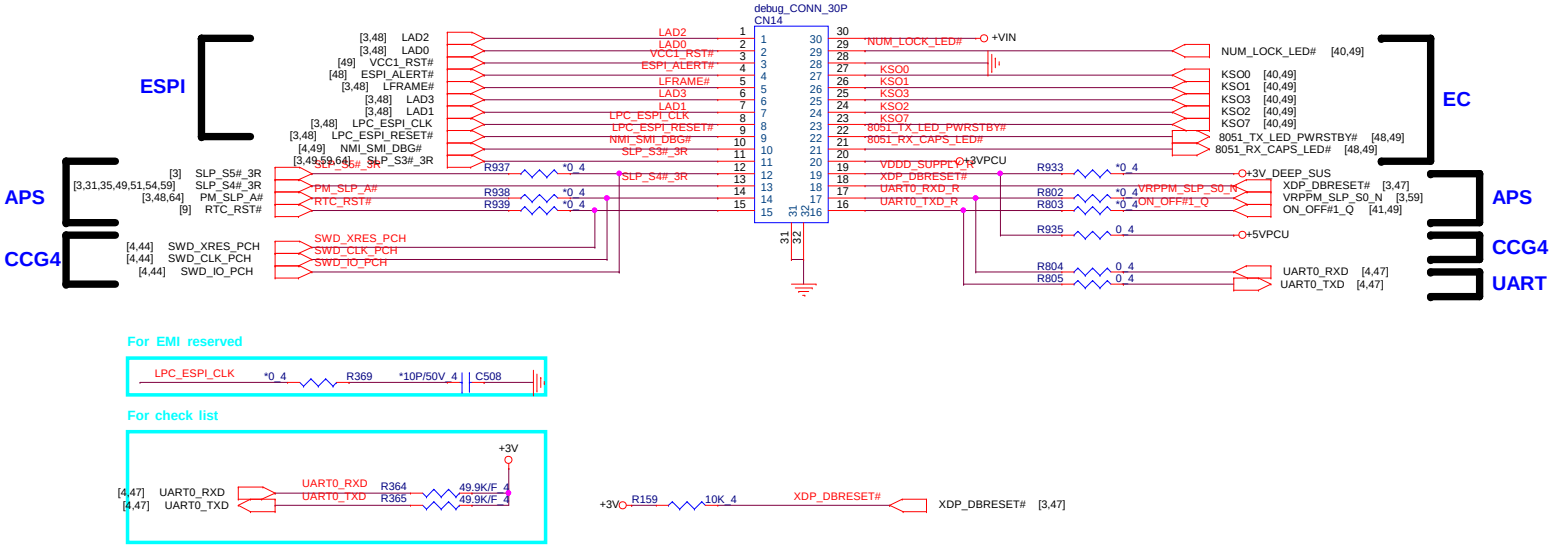
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	01 -- CARD READER	1A

Date: Thursday, May 19, 2016 | Sheet 46 of 67

ESPI+EC+APS debug conn on MB



For EMI reserved

For check list

NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 44 -- EC & eSPI/UART debug conn	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 47 of 67	

For EMI reserved

LPC_ESPI_CLK *0_4 R663 *10P/50V_4 C653

	eSPI Mode	LPC Mode
R263 R_G	Un-Install	Install
R630 R_H	Un-Install	Install
R307 R_I	Un-Install	Install
R631 R_P	Install	Un-Install

for Battery charge/charge

for Thermal IC/ G-Sensor/GPU

CPU I/O Rail Power Supply

EC

NOTE: Connect GND and AGND planes via an 0R resistor or a one-point layout connection.

NOTE: Place a 1 uF capacitor as close to the CAP pin as possible.

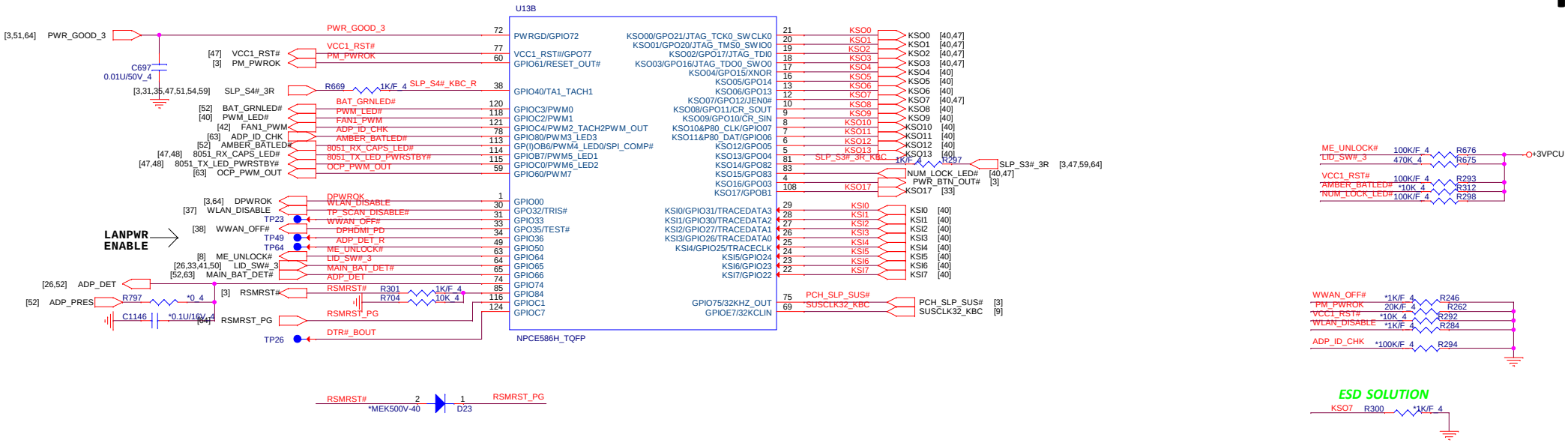
PLT_DET	PLT_DET
PD 100K	PU 10K
UMA	DIS

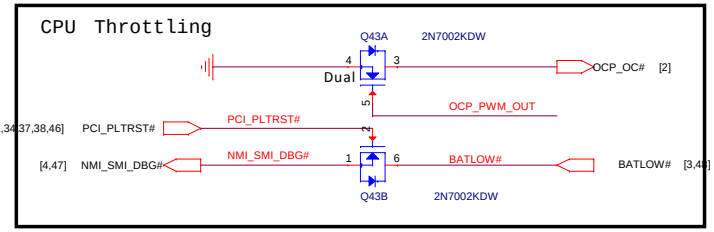
PROJECT : X63

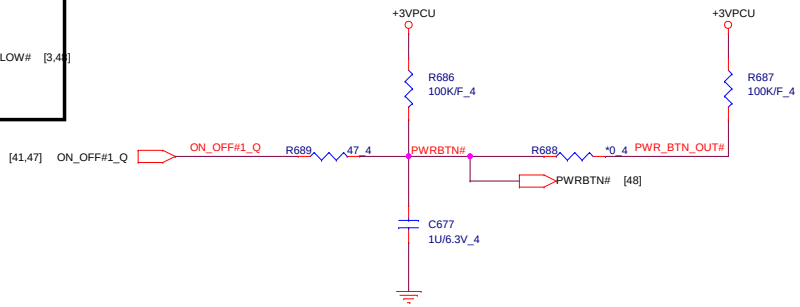
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	45 -- EC Nuvoton NPCE586H_1	1A
Date: Thursday, May 19, 2016	Sheet 48 of 67	





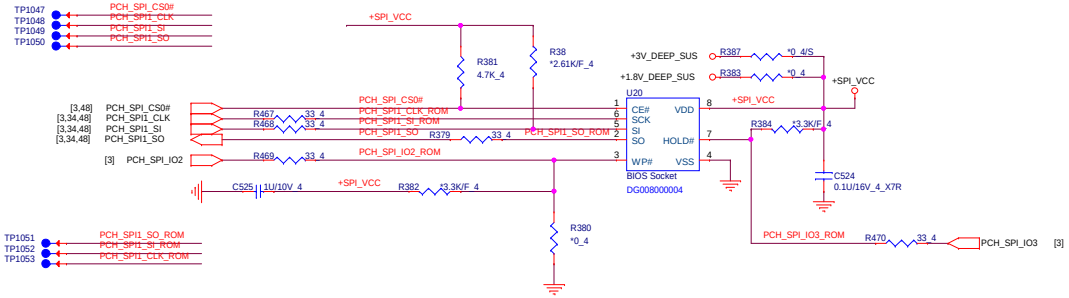


PROJECT : X63	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: 46 -- EC Nuvoton NPCE586H_2; Rev: 1A
Date: Thursday, May 19, 2016	Sheet 49 of 67

SPI ROM

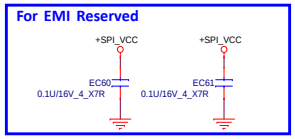
Vender	Size	P/N
Winbond	8MB	AKE3EFPKN01
Winbond	16MB	AKE3DZN0N01 SI:02/02
Socket		DFHS08FS046

PCH SPI ROM(CLG)



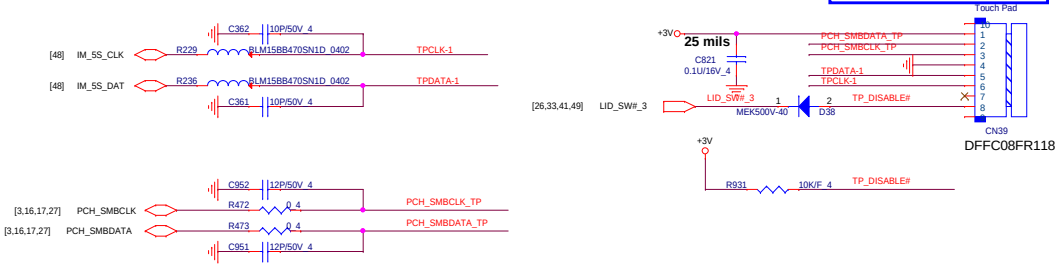
PCH 6*5mm WSON 16M SPI ROM Socket

For EMI Reserved



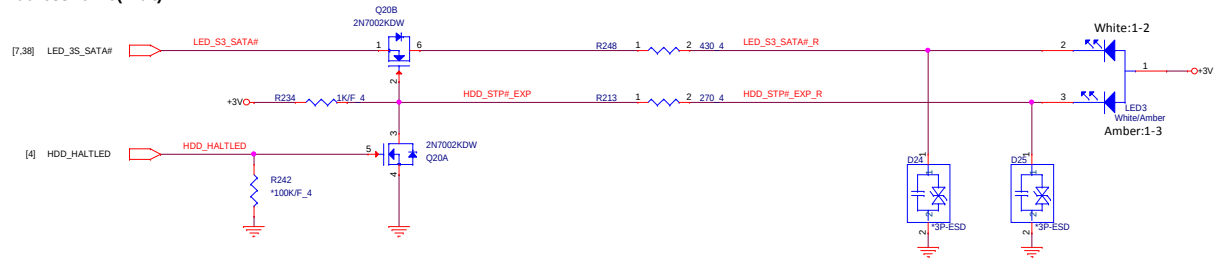
Touch pad

Forced Pad Connector



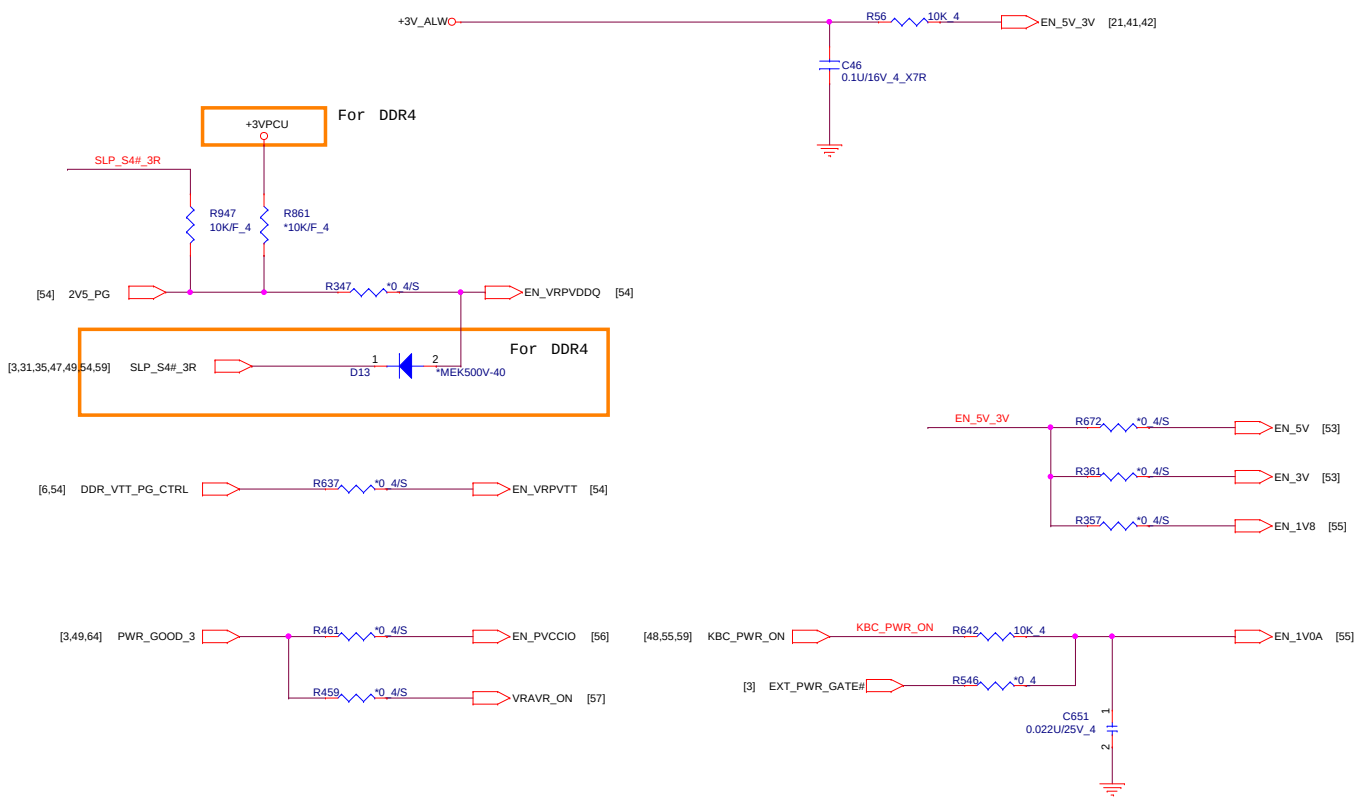
CLICK PAD
Address: 0x20(7 bit)

HDD LED



NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 47 -- Flash(KBC+PCH)/ Touch pad	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 50 of 67	

POWER TO EE NET NAME CONNECTION



NB5

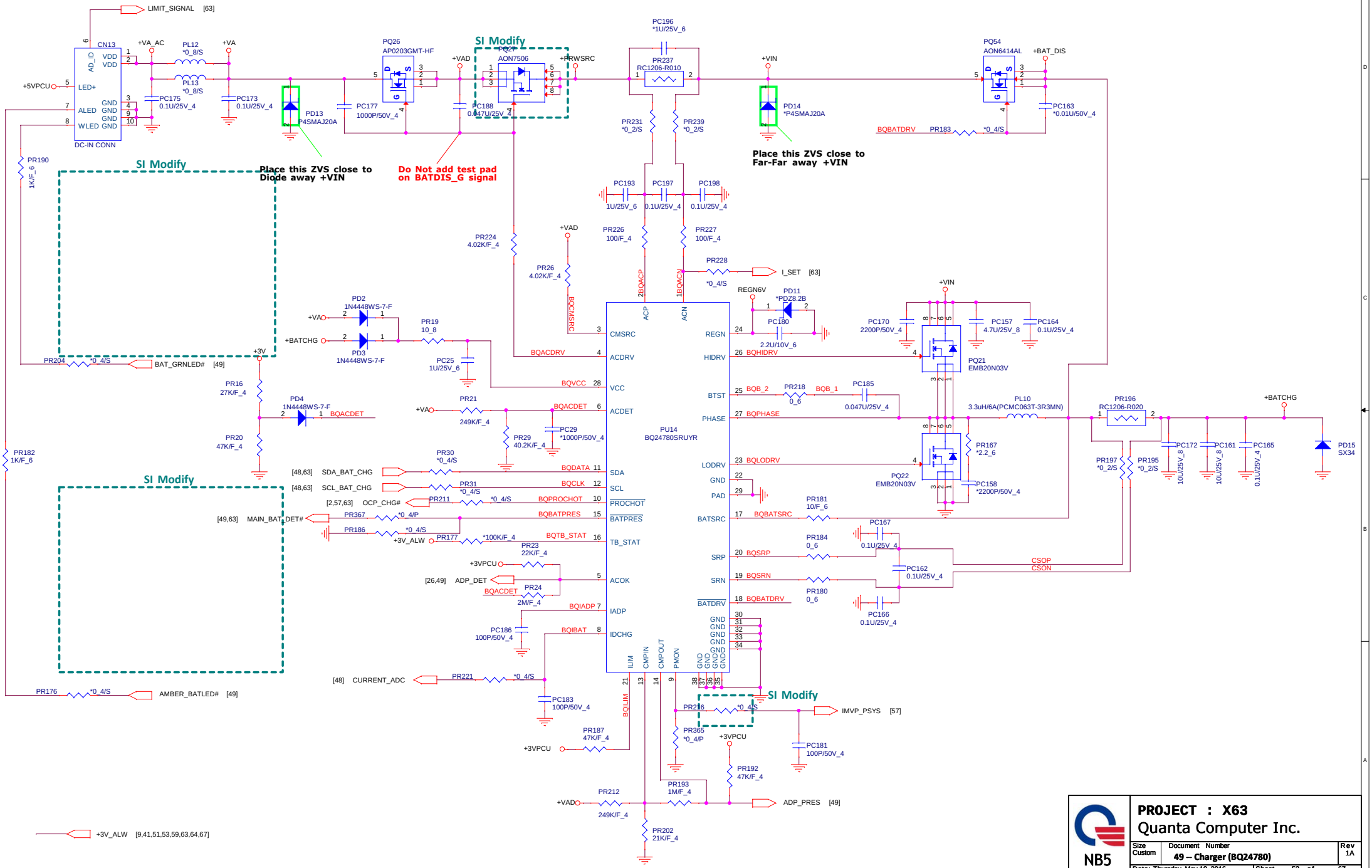
PROJECT : X63

Quanta Computer Inc.

Size	Document Number	Rev
Custom	**48 -- POWER ENABLE**	1A

Date: Thursday, May 19, 2016 | Sheet 51 of 67

90W DC_JACK



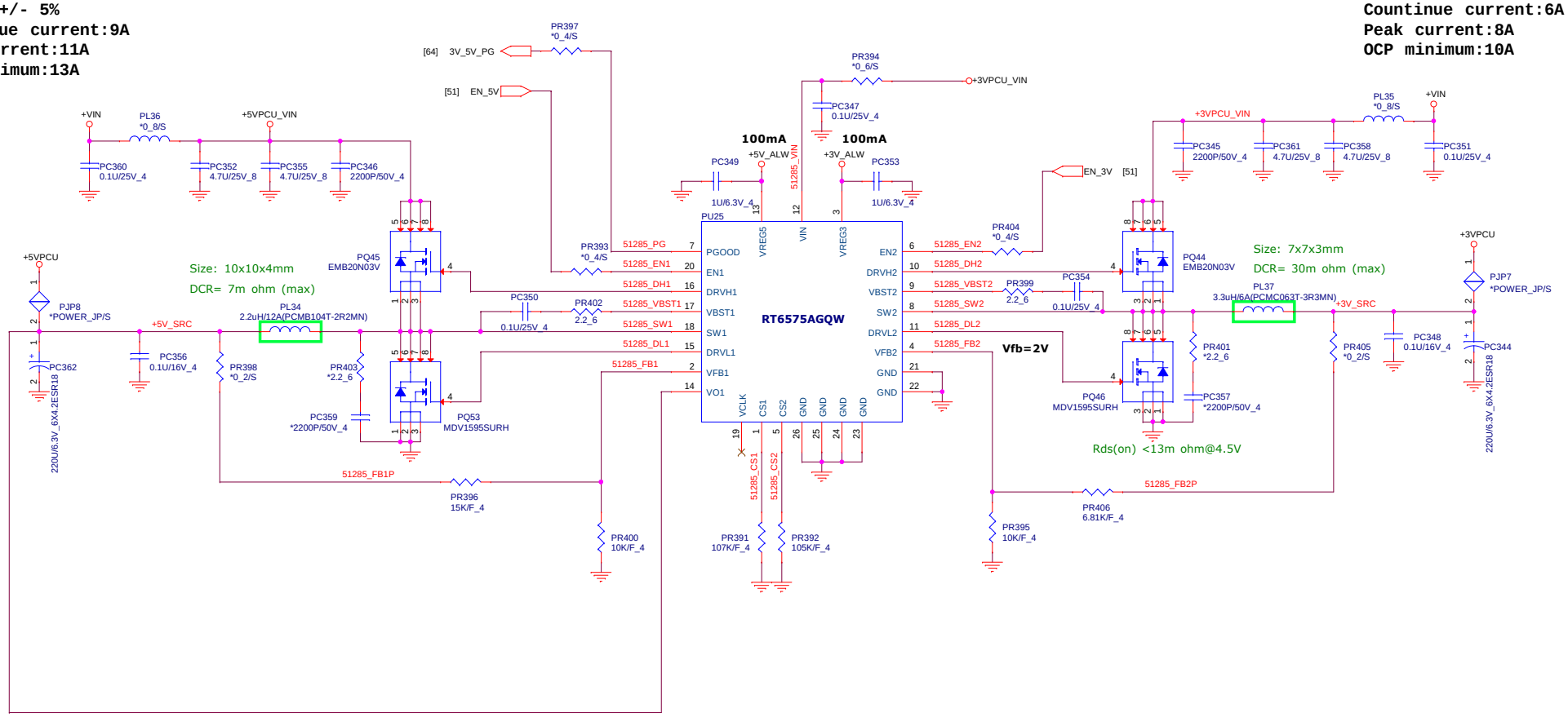
NB5	PROJECT : X63 Quanta Computer Inc.	
Size Custom	Document Number 49 – Charger (BQ24780)	Rev 1A
Date: Thursday, May 19, 2016	Sheet 52 of 67	

DC/DC +3VS5/+5VS5

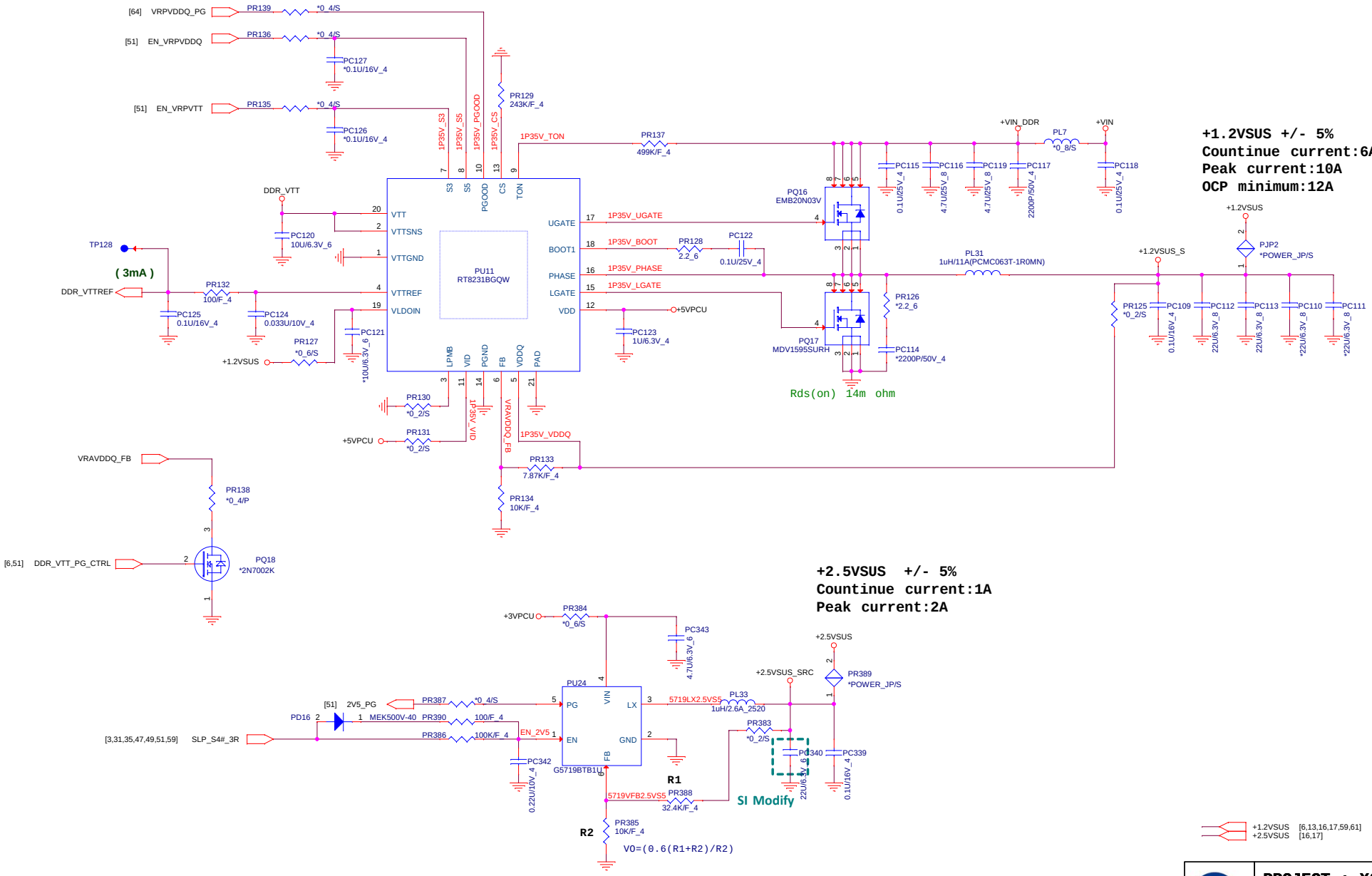
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,54,56,59,61,63,64,67]
+5VPCU [31,35,44,45,46,47,52,54,55,57,58,59,60,61,62,64,67]

+5VPCU +/- 5%
Countinue current:9A
Peak current:11A
OCP minimum:13A

+3VPCU +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:10A

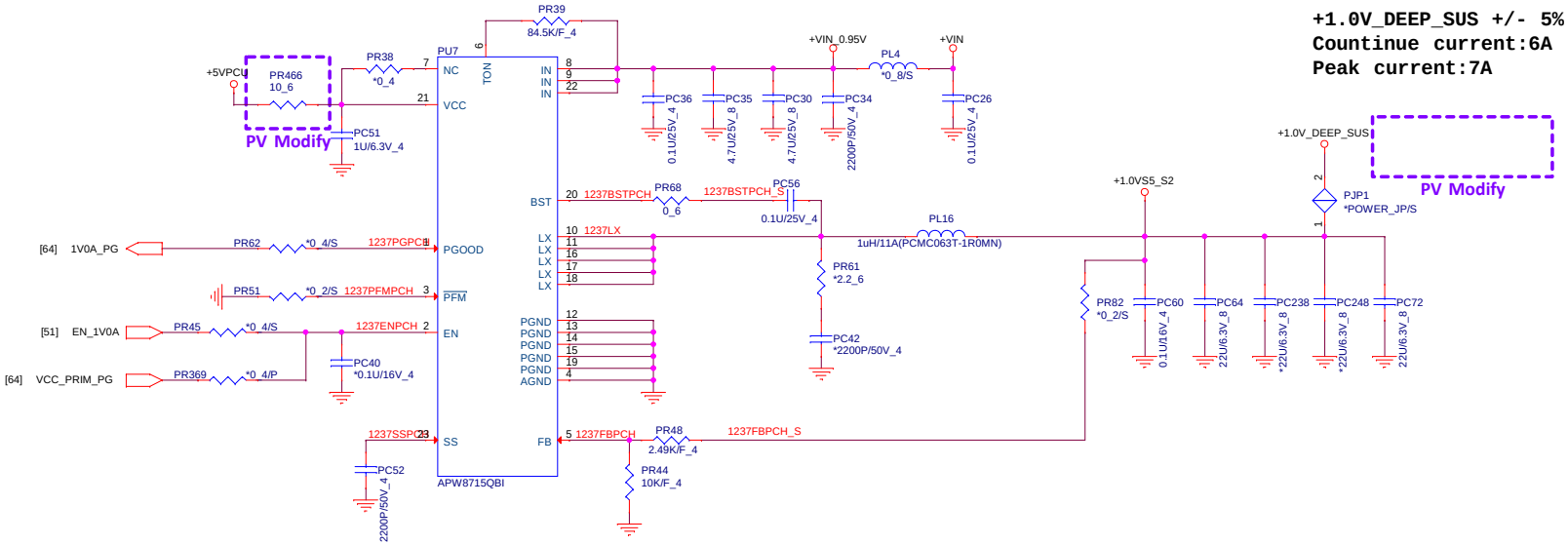


NB5	PROJECT : X63 Quanta Computer Inc.		
	Size	Document Number 50 – 3/5VS5 (SY8208B/SY8208C)	Rev 1A
	Date: Thursday, May 19, 2016	Sheet 53 of 67	

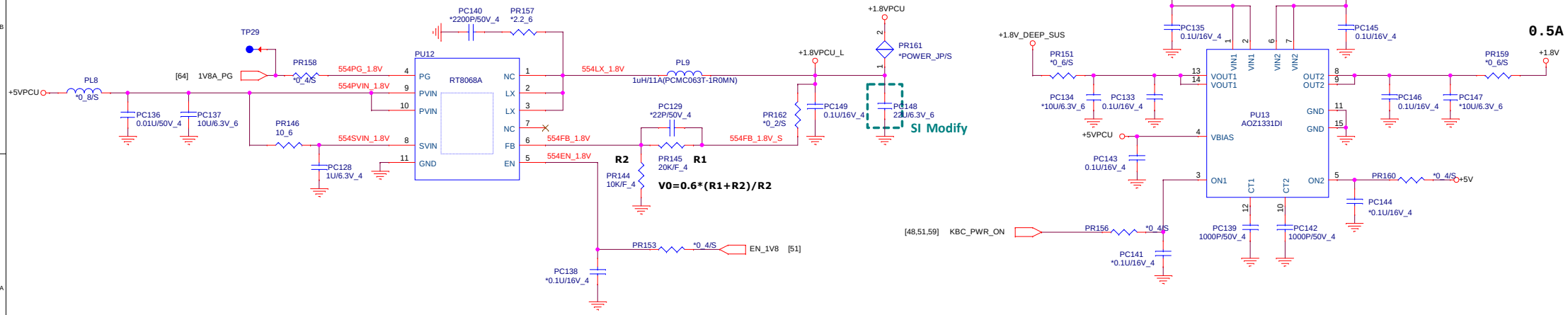


NB5	PROJECT : X63 Quanta Computer Inc.		
	Size	Document Number 51 – DDR4 (RT8231B)	Rev 1A
	Date: Thursday, May 19, 2016	Sheet 54 of 67	

+1.0V_DEEP_SUS +/- 5%
Countinue current:6A
Peak current:7A



+1.8VPCU +/- 5%
Countinue current:2A
Peak current:4A

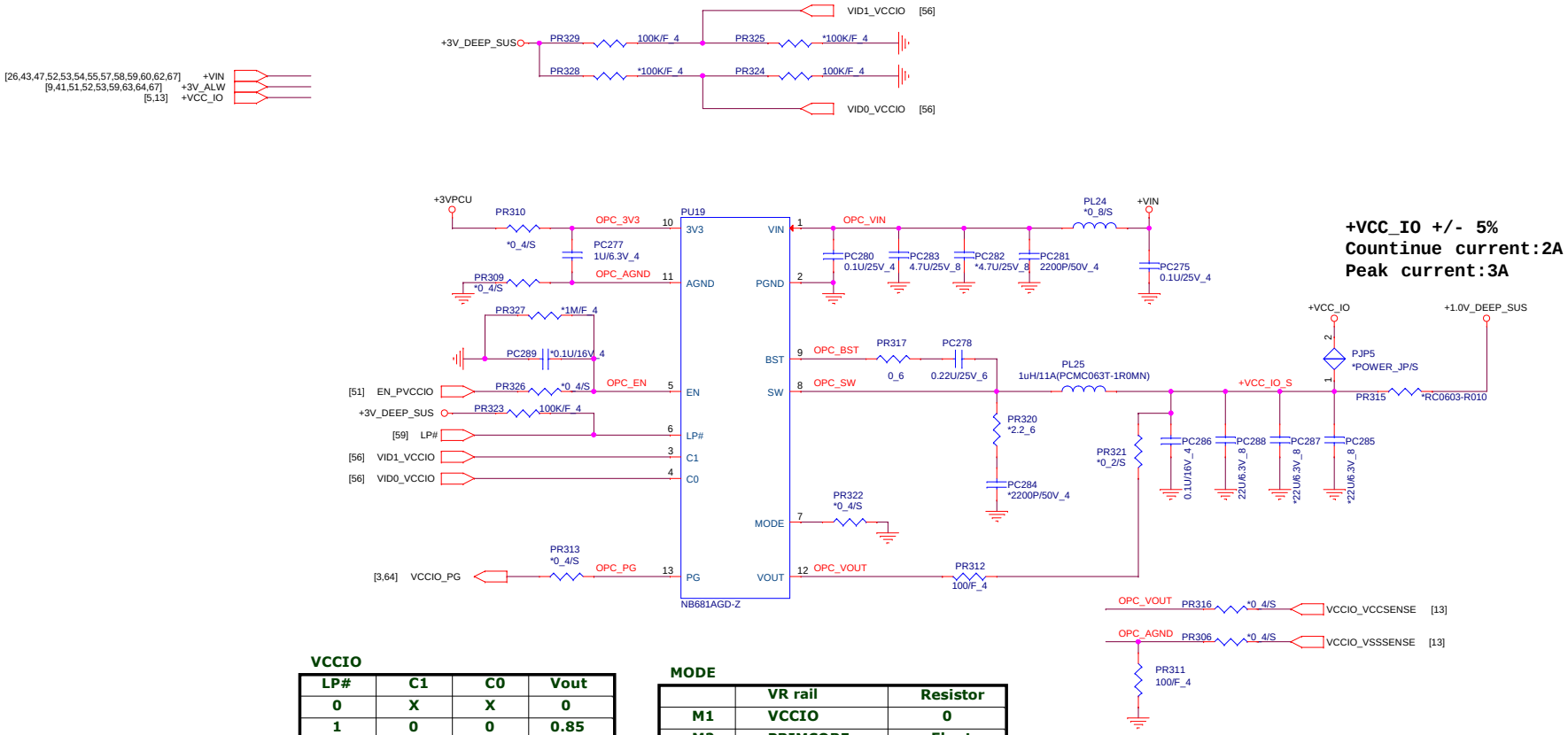


+VIN [26,43,47,52,53,54,56,57,58,59,60,62,67]
+3VPCU [3,10,33,37,38,40,41,42,44,47,48,49,51,52,53,54,56,59,61,63,64,67]
+5VPCU [31,35,44,45,46,47,52,53,54,57,58,59,60,61,62,64,67]

PROJECT : X63
Quanta Computer Inc.

NB5

Size	Document Number	Rev
	52 -- +1.0VS5/1.8VS5	1A
Date: Thursday, May 19, 2016	Sheet 55 of 67	



+VCC_IO +/- 5%
Countinue current:2A
Peak current:3A

VCCIO

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

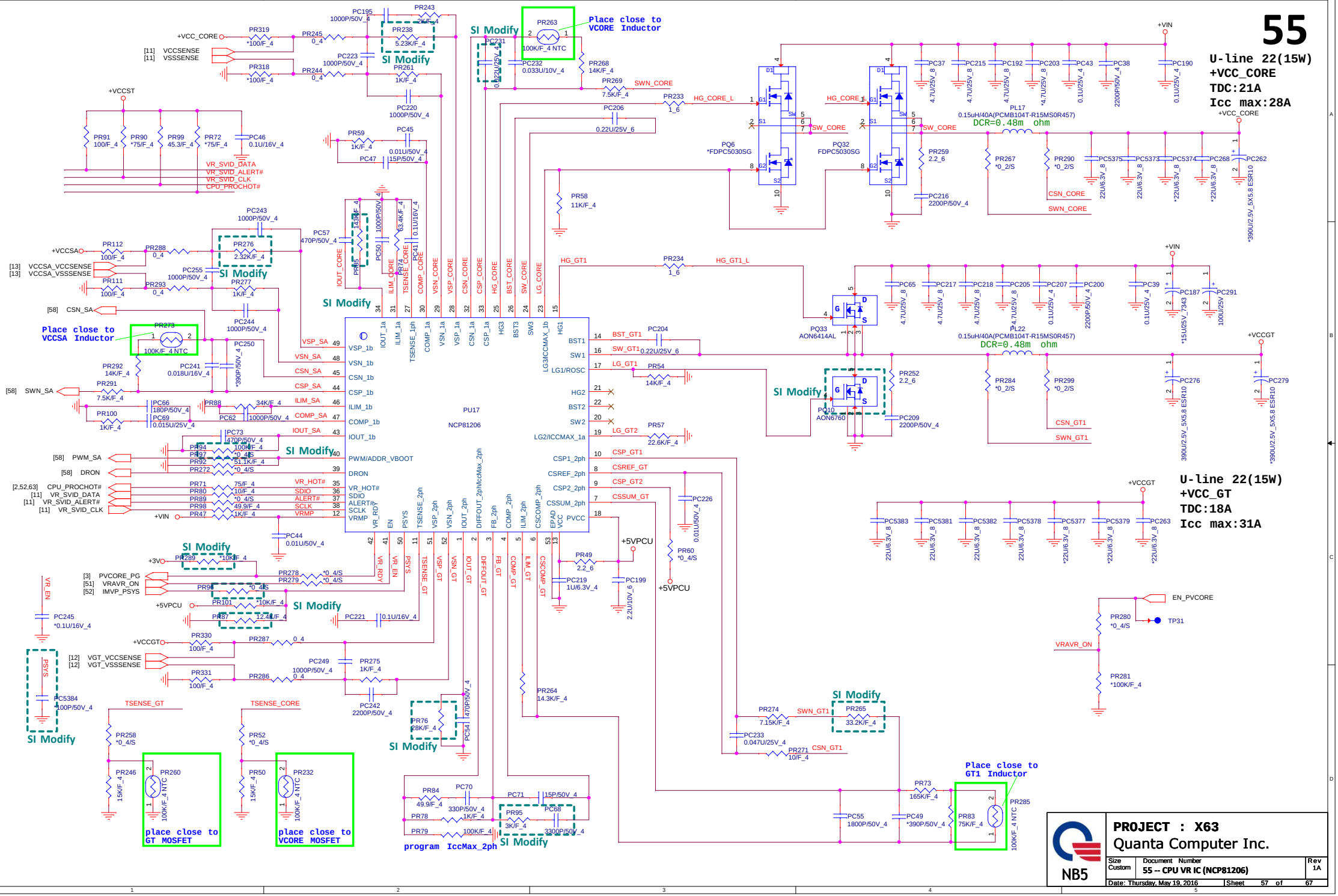
MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

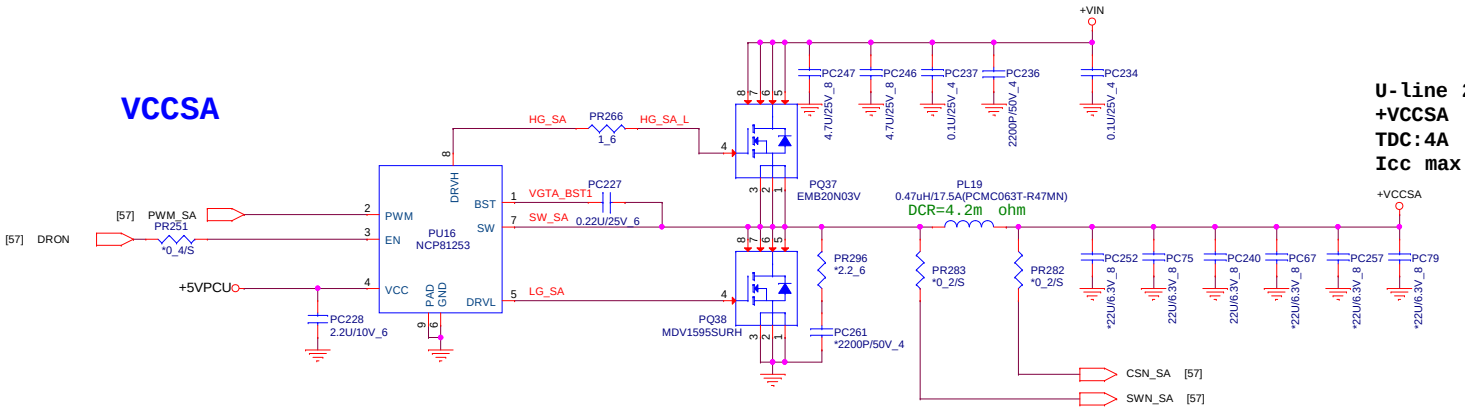
NB5

PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
	53 -- +VCC_IO (NB681)	1A
Date: Thursday, May 19, 2016	Sheet 56 of 67	

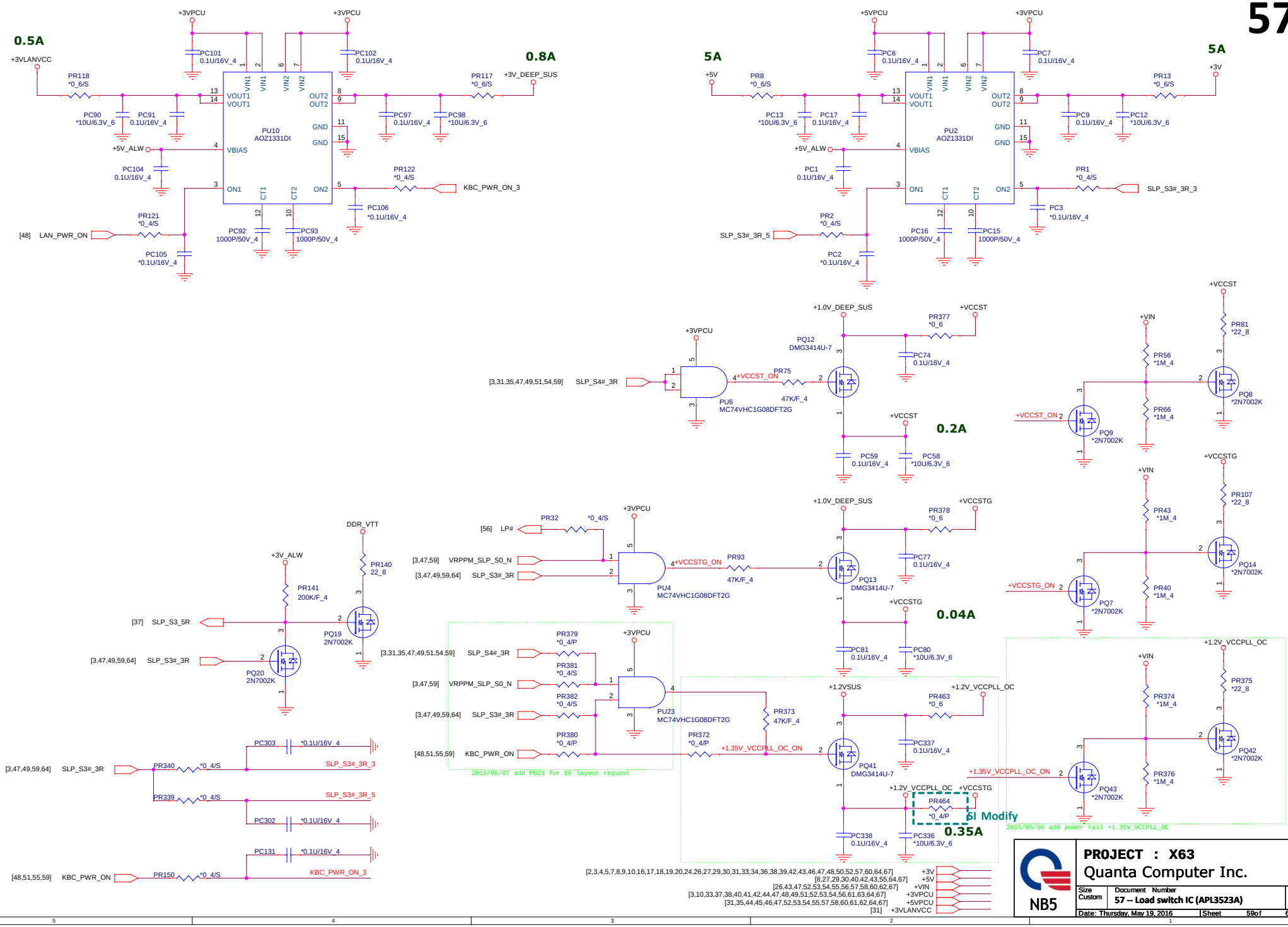

55
U-line 22(15W)
+VCC_CORE
TDC:21A
Icc max:28A
U-line 22(15W)
+VCC_GT
TDC:18A
Icc max:31A
NCP81206
PU17
SI Modify
Place close to VCORE Inductor
Place close to VCCSA Inductor
Place close to GT1 Inductor
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
PROJECT : X63
Quanta Computer Inc.
NB5
Size Custom
Document Number
55 -- CPU VR IC (NCP81206)
Rev 1A
Date: Thursday, May 19, 2016
Sheet 57 of 67

VCCSA

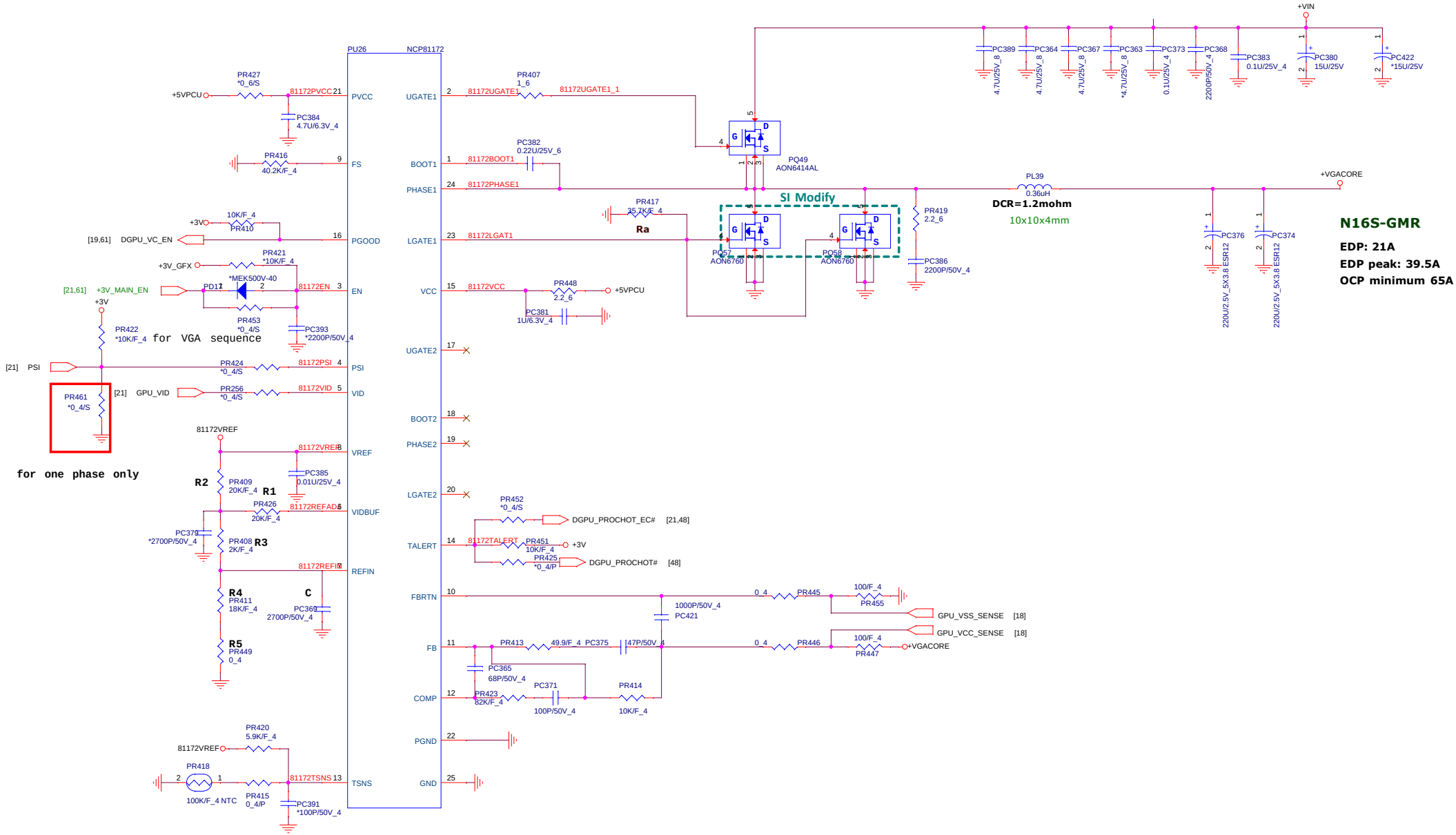


U-line 22(15W)
+VCCSA
TDC:4A
Icc max:5A

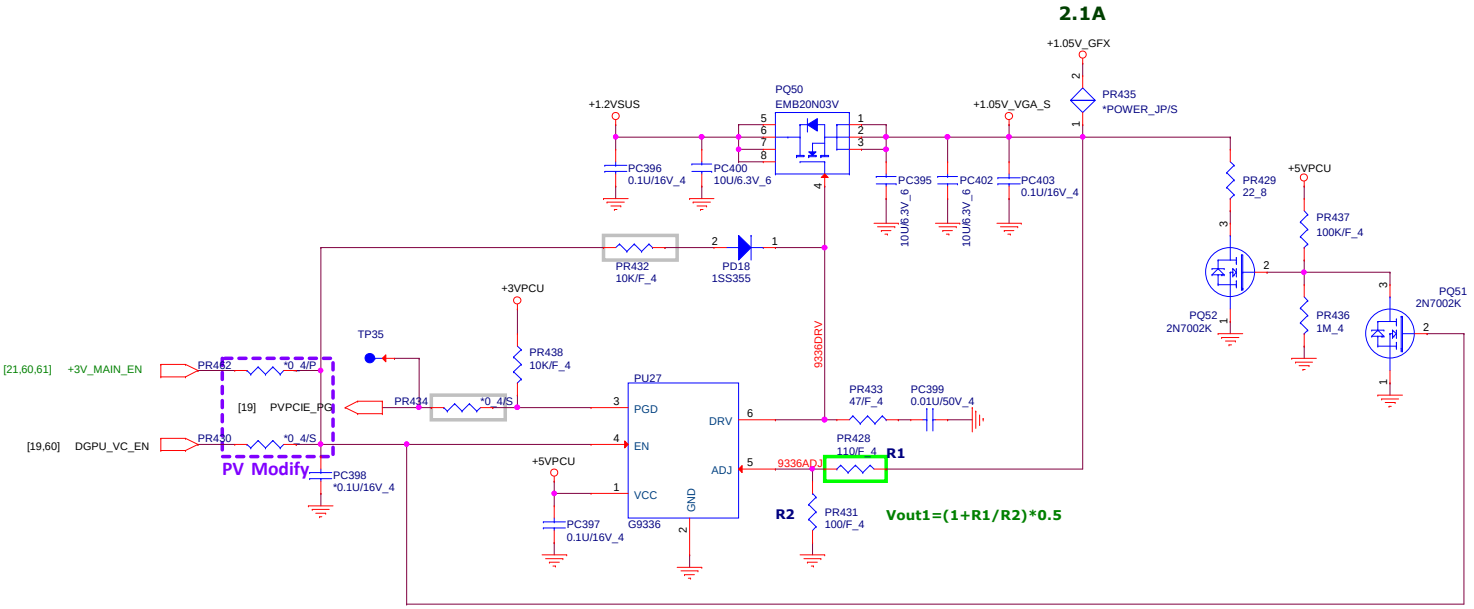
NB5	**PROJECT : X63** Quanta Computer Inc.	
Size: Custom	Document Number: **56 -- +VCCSA (NCP81253)**	Rev: 1A
Date: Thursday, May 19, 2016	Sheet 58of 67	

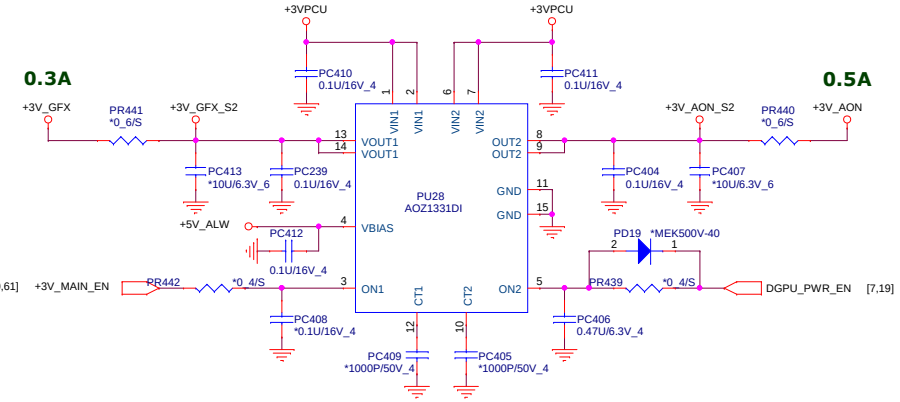


PROJECT : X63			
Quanta Computer Inc.			
NB5	Size: Custom	Document Number: 57 -- Load switch IC (APL3523A)	Rev: 1A
	Date: Thursday, May 19, 2016	Sheet: 59of 67	

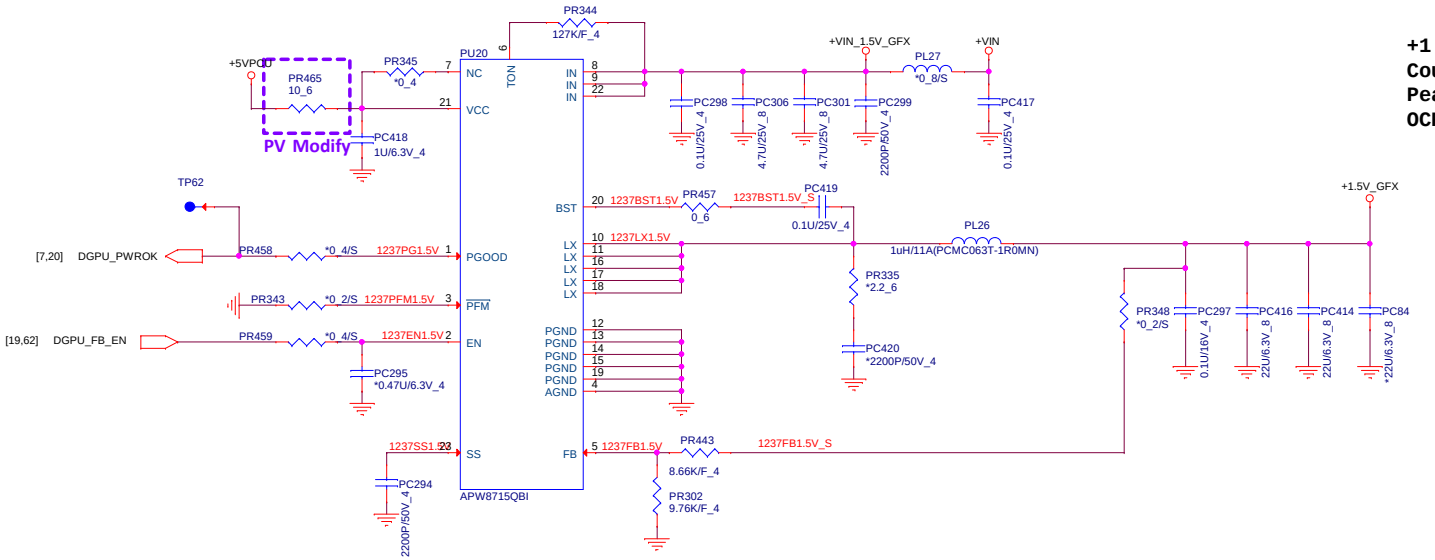


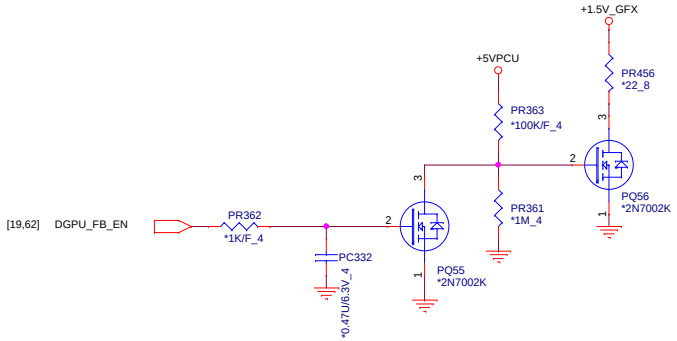
NB5	PROJECT : X63 Quanta Computer Inc.		
	Size: Custom	Document Number: 58 -- VGA Core1 (ISL62771)	Rev: 1A
	Date: Thursday, May 19, 2016	Sheet: 60of 67	





NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 60 -- +1.0V_VGA/1.8V_VGA/3V_VGA	Rev: 1A
Date: Thursday, May 19, 2016	Sheet: 61of 67	

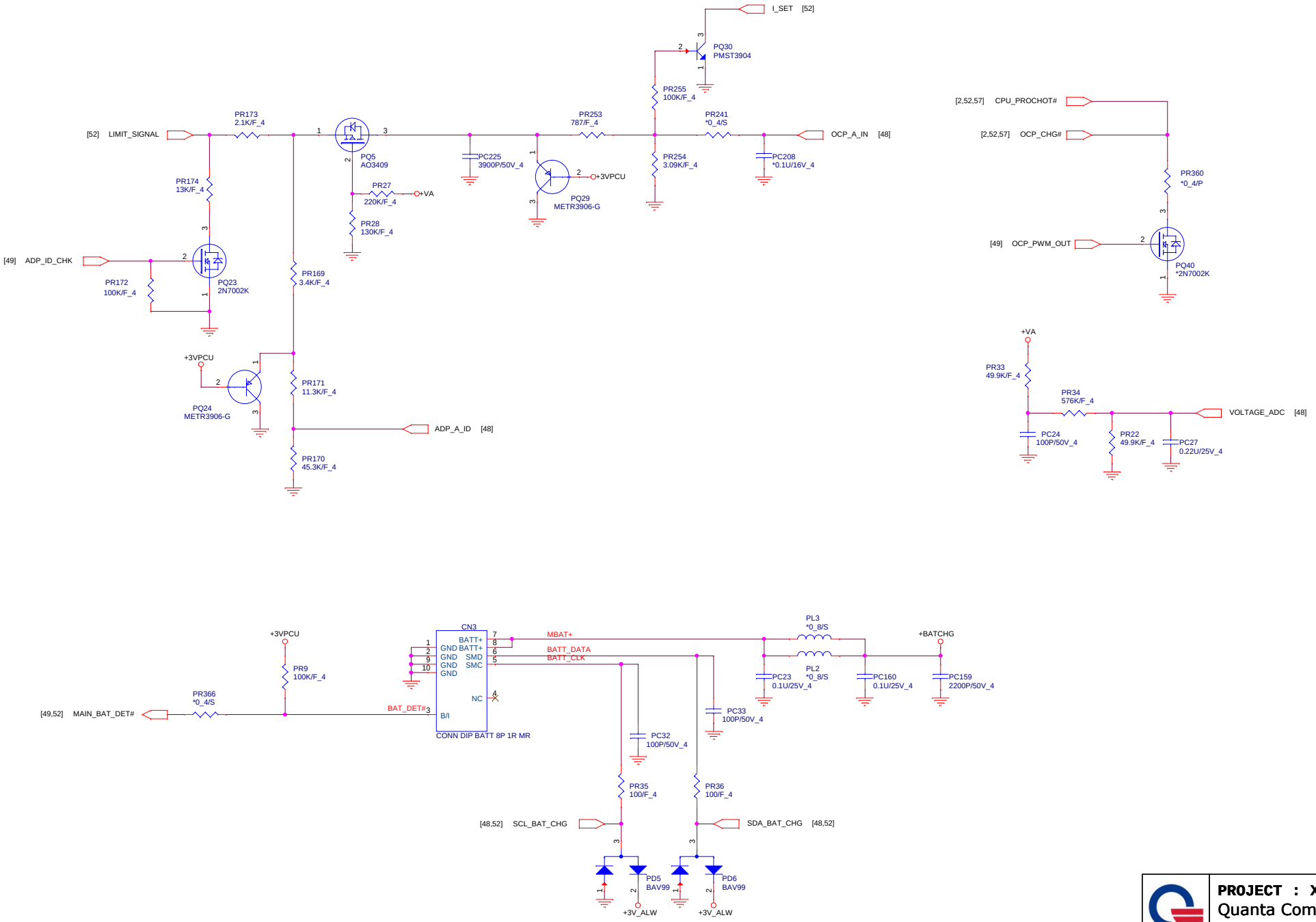




+1.5V_GFX Volt +/- 5%
Countinue current:2.4A
Peak current:4.1A
OCP minimum:8A

NB5	**PROJECT : X63** Quanta Computer Inc.	
Size: Custom	Document Number: **61 -- +1.35V_GFX (AOZ1267)**	Rev: 1A
Date: Thursday, May 19, 2016	Sheet: 62of 67	

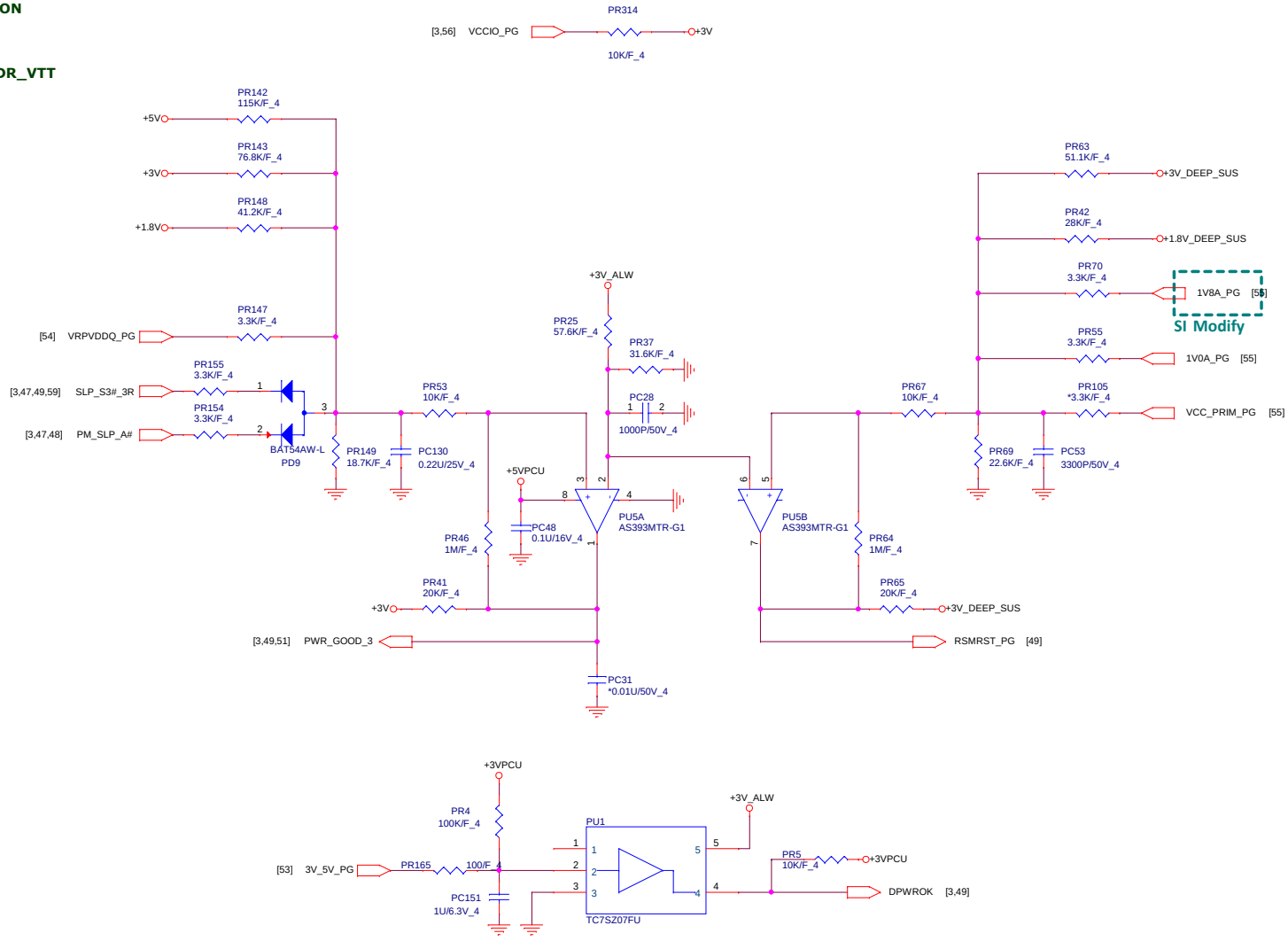
Adapter OCP



NB5	**PROJECT : X63** Quanta Computer Inc.	
Size	Document Number 62 -- CHARGER II	Rev 1A
Date: Thursday, May 19, 2016	Sheet 63 of 67	

POK CKT

PM_SLP_S4# = SUSON
PM_SLP_S3# = MAINON
+V5S = +5V
+V3S = +3V
+V0.75S =+0.75V_DDR_VTT



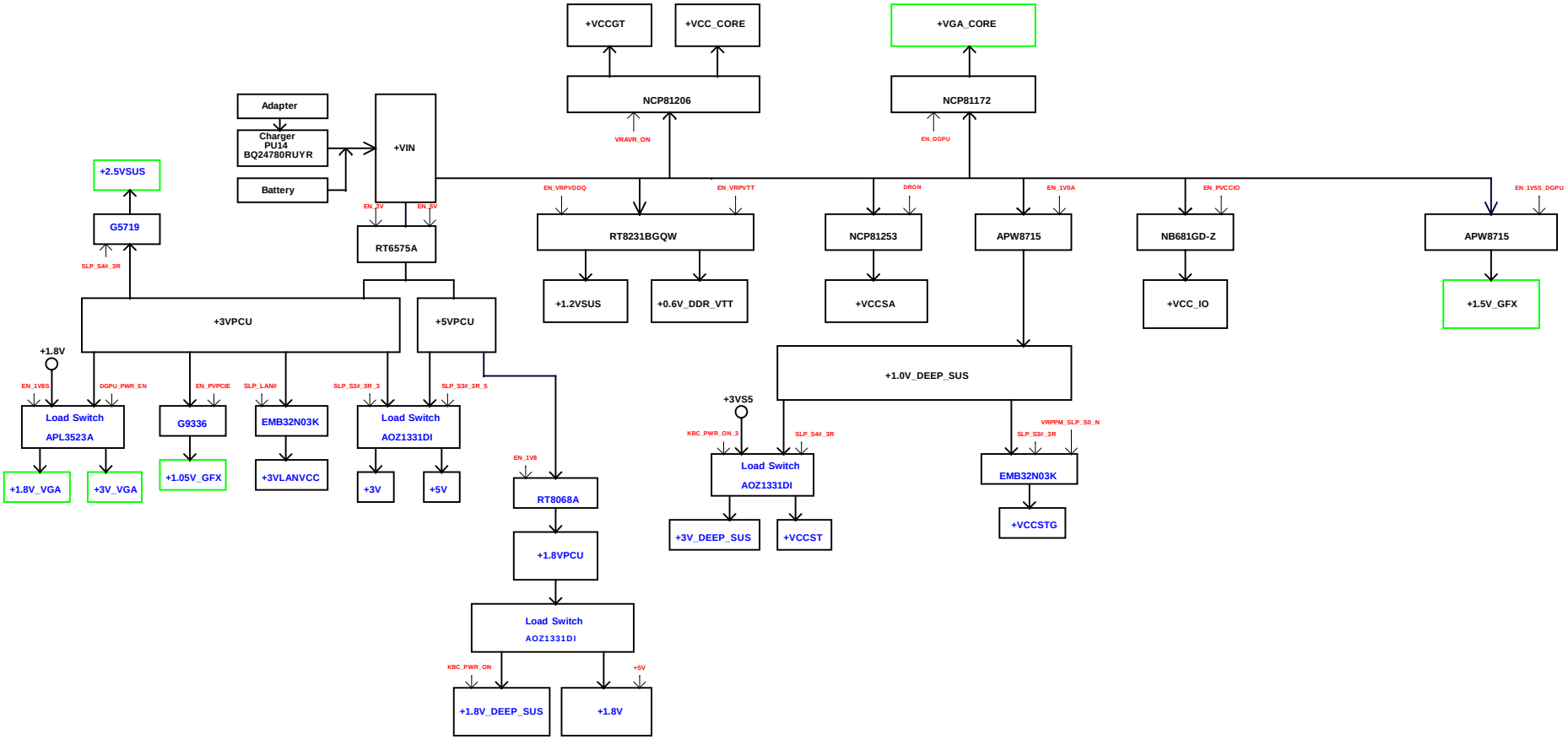
[2,3,4,5,7,8,9,10,16,17,18,19,20,24,26,27,29,30,31,33,34,36,38,39,42,43,46,47,48,50,52,57,59,60,67] +3V
[8,27,29,30,40,42,43,55,59,67] +5V
[9,41,51,52,53,59,63,67] +3V_ALW

NB5

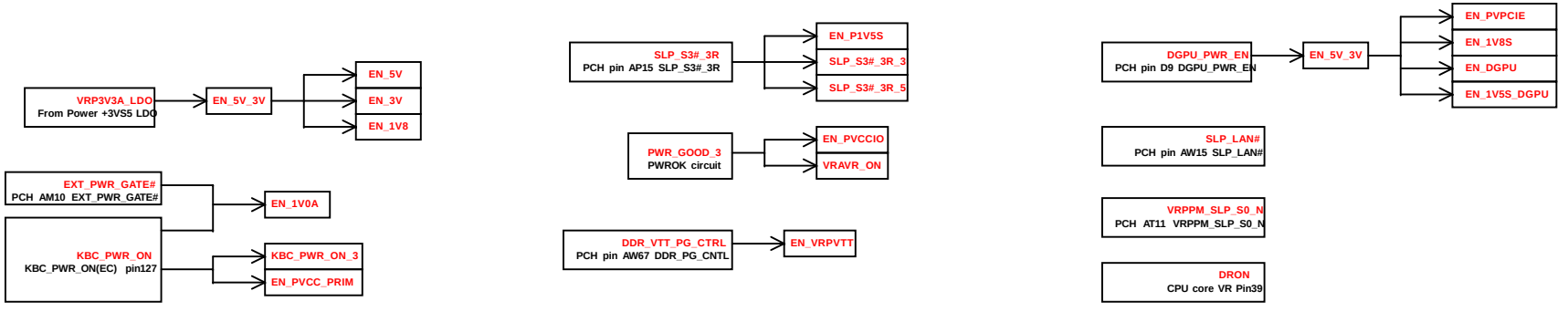
PROJECT : X63
Quanta Computer Inc.

Size	Document Number	Rev
Custom	63 -- PWROK	1A
Date: Thursday, May 19, 2016	Sheet 64 of 67	

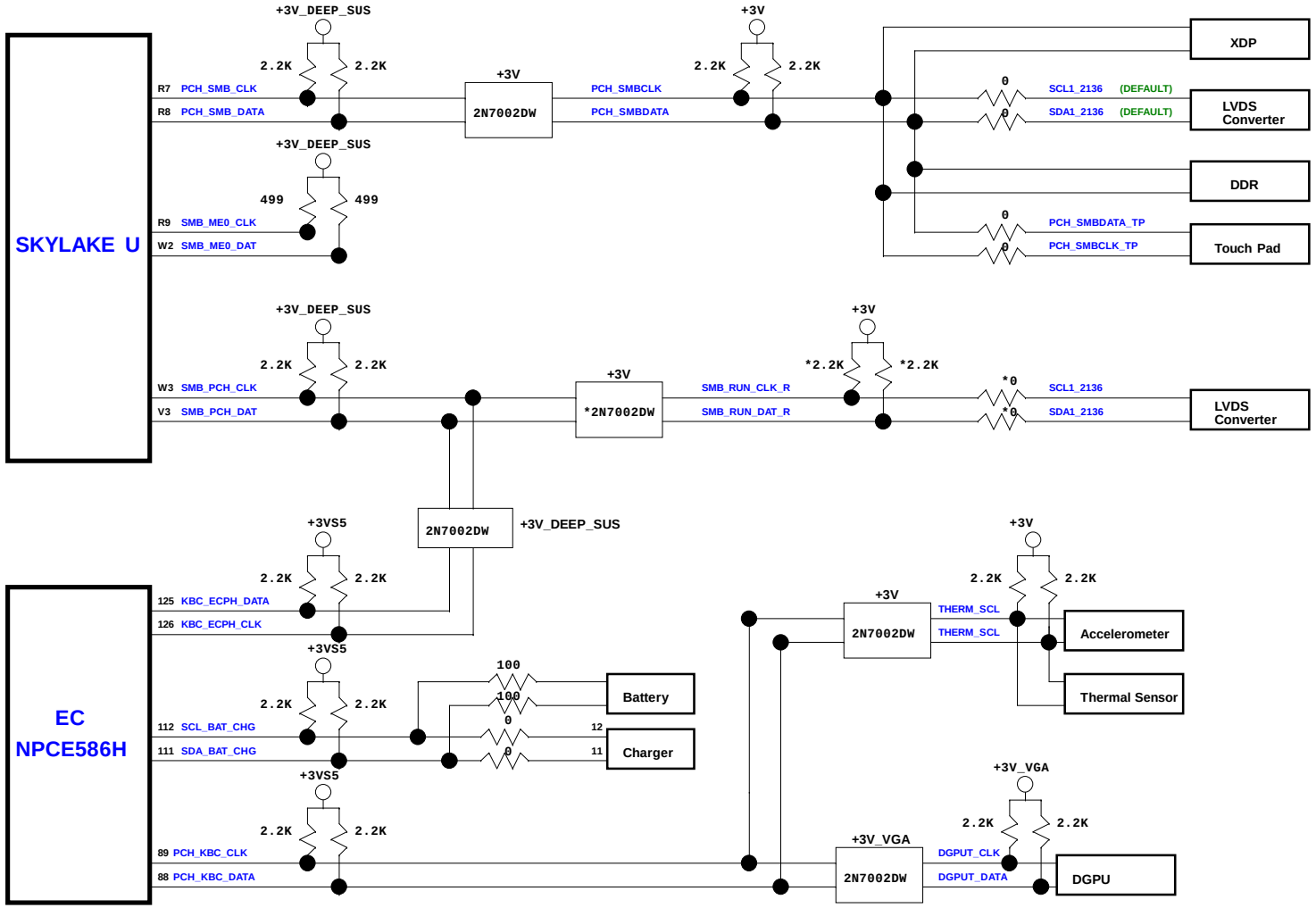
POWER BLOCK DIAGRAM



POWER ENABLE PIN



NB5	PROJECT : X63 Quanta Computer Inc.	
Size: Custom	Document Number: 64 – Power Block Diagram	Rev: 1A
Date: Thursday, May 19, 2016	Sheet: 65of 67	

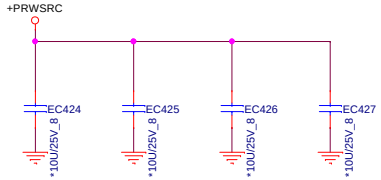


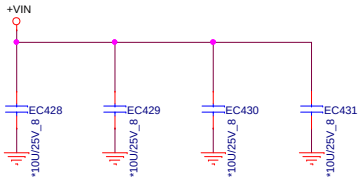
Example: *499/F_4 and *0_6/S
* means none-installed
499 means value
F means 1%
_4 means 0402 size
/S means short pad

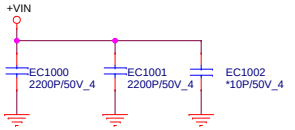
Multiplexed HSIO Lane	Port Assignment
USB3 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB3 #2 / SSIC #1	USB2.0/USB3.0 Combo Jack(Left side up)
USB3 #3 / SSIC #2	NC
USB3 #4	NC
PCIE1 / USB3 #5	dGPU
PCIE2 / USB3 #6	dGPU
PCIE3	dGPU
PCIE4	dGPU
PCIE5	LAN
PCIE6	WLAN
PCIE7 / SATA #0	HDD (SATA)
PCIE8 / SATA #1	ODD (SATA)
PCIE9	Cardreader (PCIE)
PCIE10	NC
PCIE11 / SATA #1*	NC
PCIE12 / SATA #2	SSD (SATA)

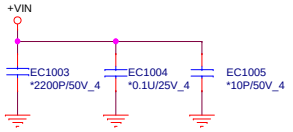
USB2.0	Port Assignment
USB2 #1	USB2.0/USB3.0 Combo Jack(Left side down)
USB2 #2	USB2.0/USB3.0 Combo Jack(Left side up)
USB2 #3	WWAN
USB2 #4	USB2.0(Right side on USB Board)
USB2 #5	USB2.0(Right side on USB Board)
USB2 #6	Touch Screen
USB2 #7	Bluetooth
USB2 #8	Finger Print
USB2 #9	Camera
USB2 #10	NC

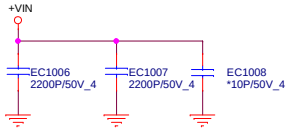
PROJECT : X63
Quanta Computer Inc.
NB5
Size: Custom | Document Number: 65 -- SMBus/Port Assignment | Rev: 1A
Date: Thursday, May 19, 2016 | Sheet 66 of 67

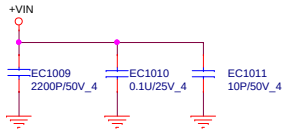


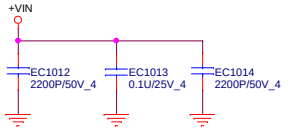


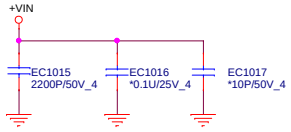












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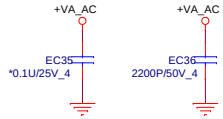

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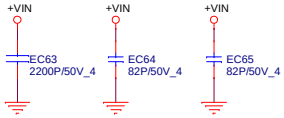

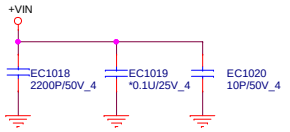

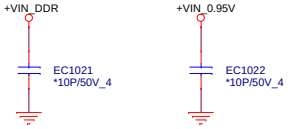

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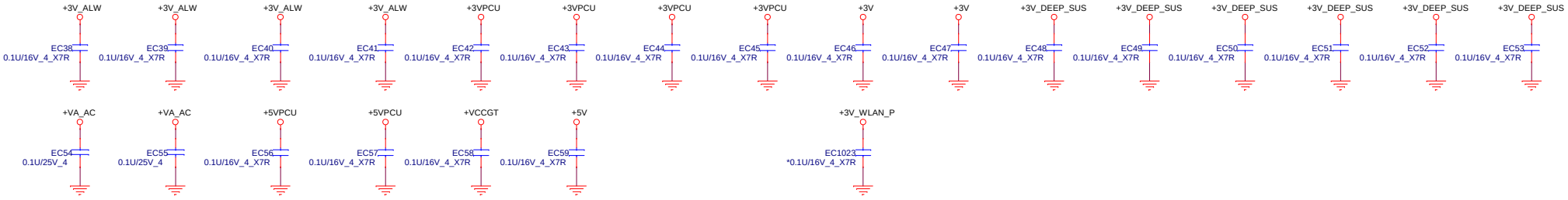

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