

Compal Confidential

JFWXX Schematics Document

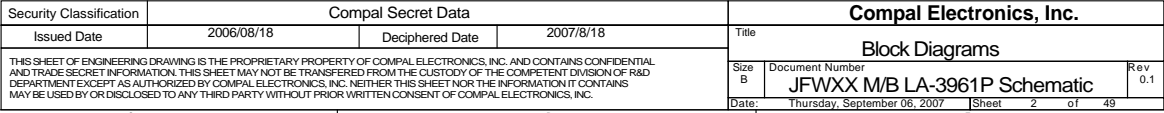
Intel Merom Processor with SiSM672MX + DDRII + SiS968 + SiS307LV

2007-09-06

REV: 0.3

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Model Name : JFWXX
File Name : LA-3961P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS (Actual +0.9V)	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PROJECT ID Table

	PROJECT_ID
14W	R424 (Pull low)
15W	NA (Internal Pull High)

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+ Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH8M SM Bus address

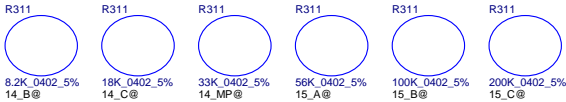
Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%
Ra	100K +/- 5%

Ra~ R312

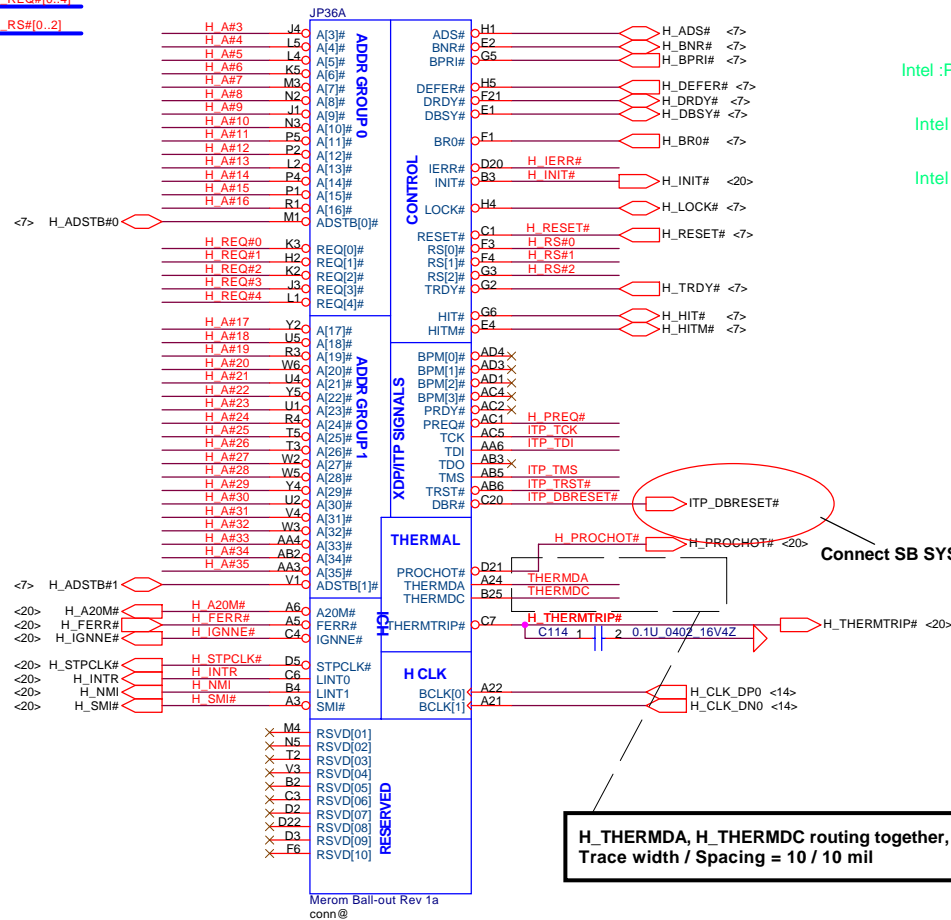
Rb~ R311



Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	Rb BOM Structure
0	0	0 V	0 V	0 V	14_A@
1	8.2K +/- 5%	0.217 V	0.250 V	0.288 V	14_B@
2	18K +/- 5%	0.439 V	0.503 V	0.575 V	14_C@ ✓
3	33K +/- 5%	0.721 V	0.819 V	0.926 V	14_MP@
4	56K +/- 5%	1.054 V	1.185 V	1.325 V	15_A@
5	100K +/- 5%	1.489 V	1.650 V	1.819 V	15_B@
6	200K +/- 5%	2.019 V	2.200 V	2.386 V	15_C@ ✓
7	NC	3.135V	3.300 V	3.465 V	15_MP@

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<7> H_A#[3..35] H_A#[3..35]
<7> H_REQ#[0..4] H_REQ#[0..4]
<7> H_RS#[0..2] H_RS#[0..2]



H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

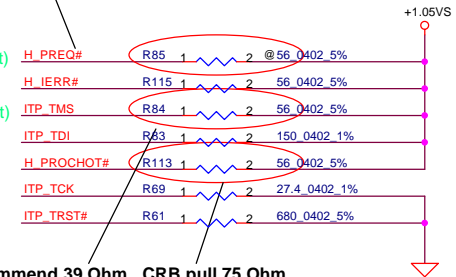
Trace length must short

Place close to CPU within 500mil

Intel :Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)

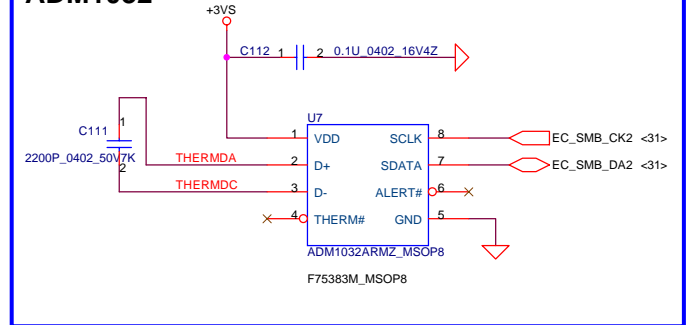
Intel :Pull-up 56ohm (Mount) SiS : Pull-up 54.9ohm (Mount)

Intel :Pull-up 56ohm (Mount) SiS : Pull-up 75ohm (Mount)

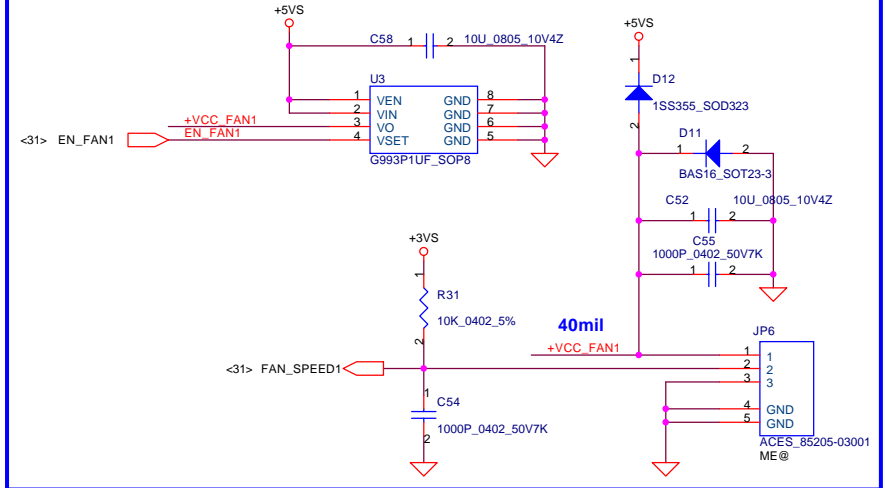


Checklist recommend 39 Ohm CRB pull 75 Ohm

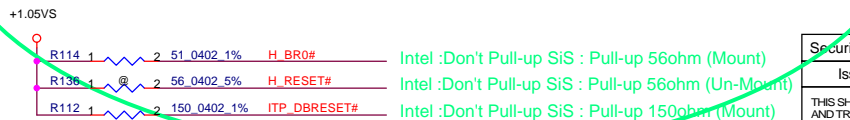
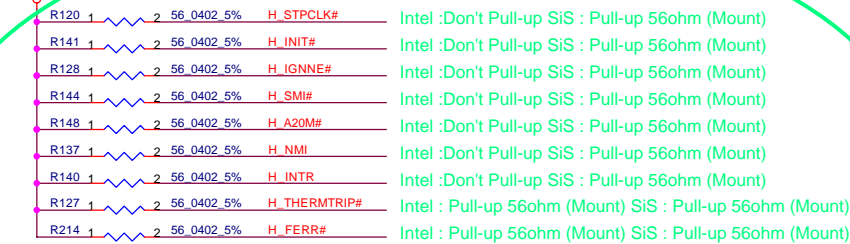
ADM1032



FAN1 Conn



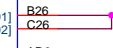
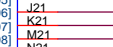
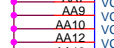
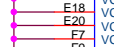
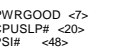
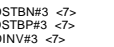
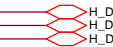
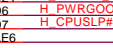
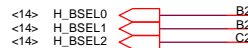
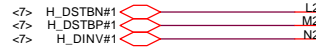
CPU to SB interface



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Close to CPU pin AD26
within 500mils.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1
200	0	1	0

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



Intel :Don't Pull-up SiS : Pull-up 56ohm (Mount)

Intel : Pull-up 56ohm (Un-Mount) SiS : Pull-up 56ohm (Mount)

Intel : Don't Pull-up (Connects to ICH) SiS : Pull-up 56ohm (Up-Mount)

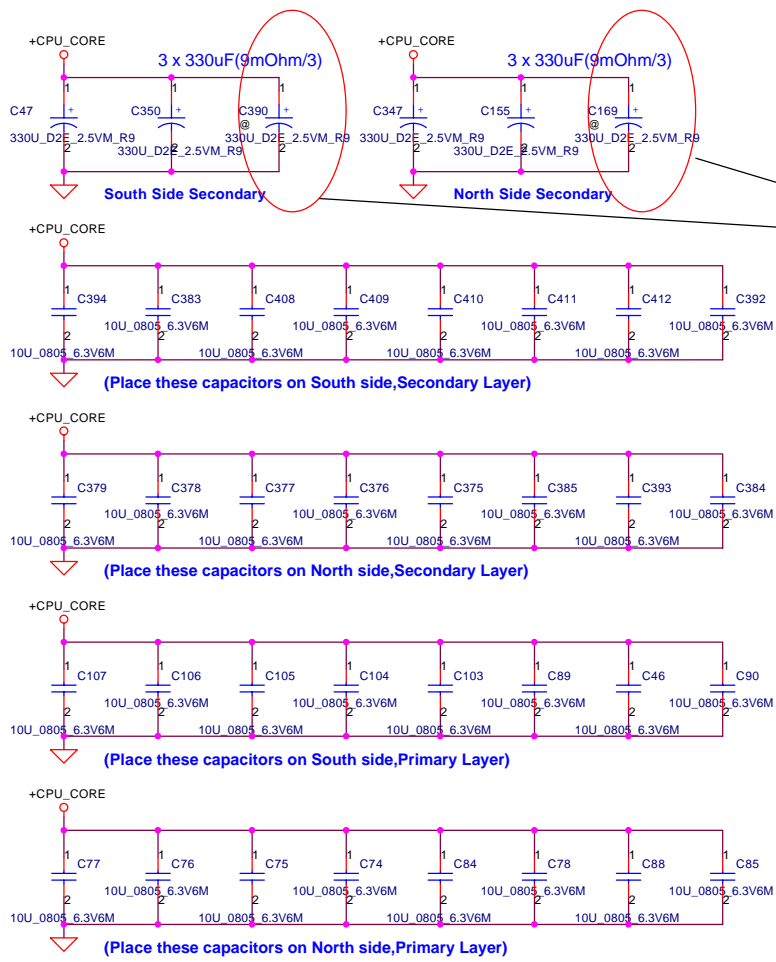
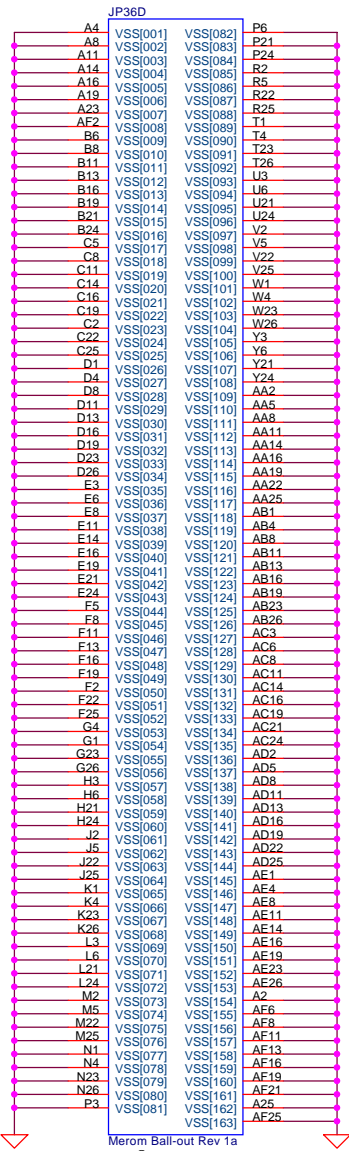
Intel : Don't Pull-up SiS : Pull-up 56ohm (1 In-Mount)

Inter: Don't Fall up Sis : Fall up soon!!! (On-mount)

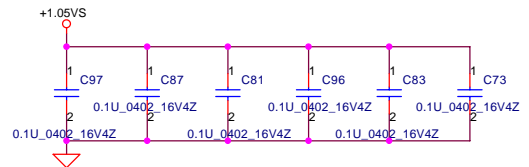
SiS Recommend

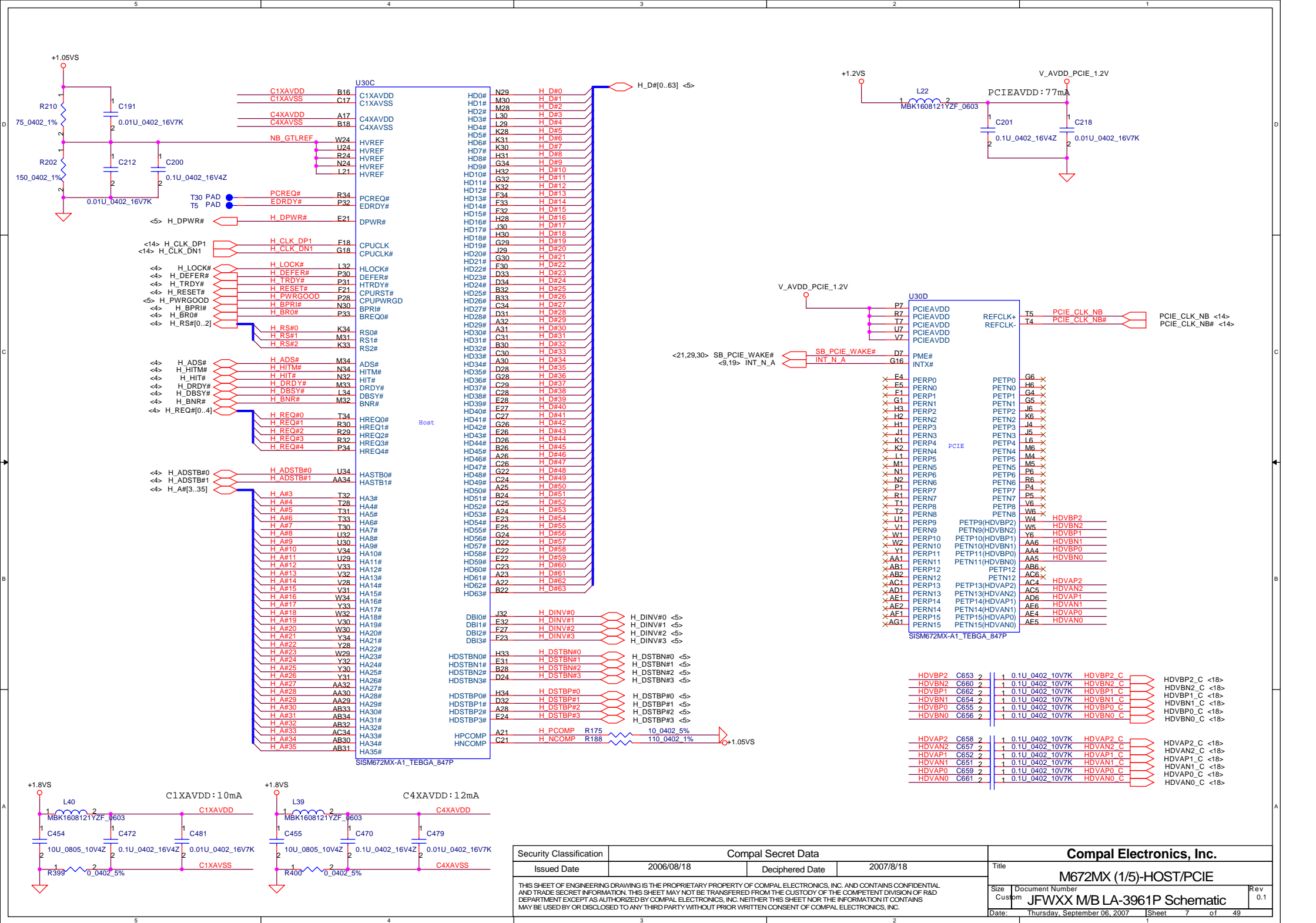
Intel :Don't Pull-down SiS :Pull-down Cap (Un-Mount)

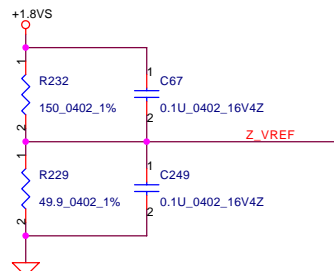
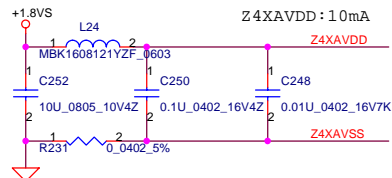
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+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

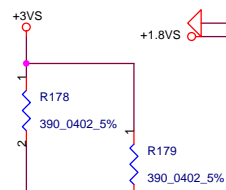




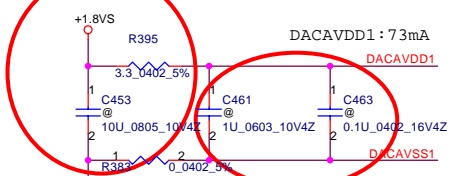
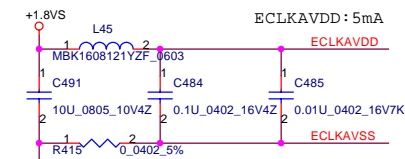
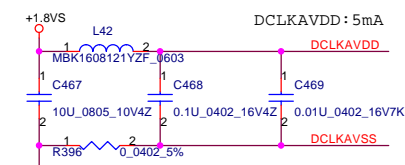


<17> VGA_CRT_HSYNC
<17> VGA_CRT_VSYNC
<17> GMCH_CRT_CLK
<17> GMCH_CRT_DATA

<19> ZAD[0..16] ZAD[0..16]



<7,19> INT_N_A
<14> REF_CLK0



DACAVDD1 Spec.
Voltage : 1.5V +/- 5%
Current : 100mA

7/30 modified to @

7/24 modified

<14> Z_CLK0
<19> ZDREQ
<19> ZUREQ
<19> ZSTB_DP0
<19> ZSTB_DN0
<19> ZSTB_DP1
<19> ZSTB_DN1

ZAD0
ZAD1
ZAD2
ZAD3
ZAD4
ZAD5
ZAD6
ZAD7
ZAD8
ZAD9
ZAD10
ZAD11
ZAD12
ZAD13
ZAD14
ZAD15
ZAD16

Z_VREF
Z_COMP_P
Z_COMP_N

Z4XAVDD
Z4XAVSS

<17> VGA_CRT_R
<17> VGA_CRT_G
<17> VGA_CRT_B

VCOMP
VVBWN
VRSET

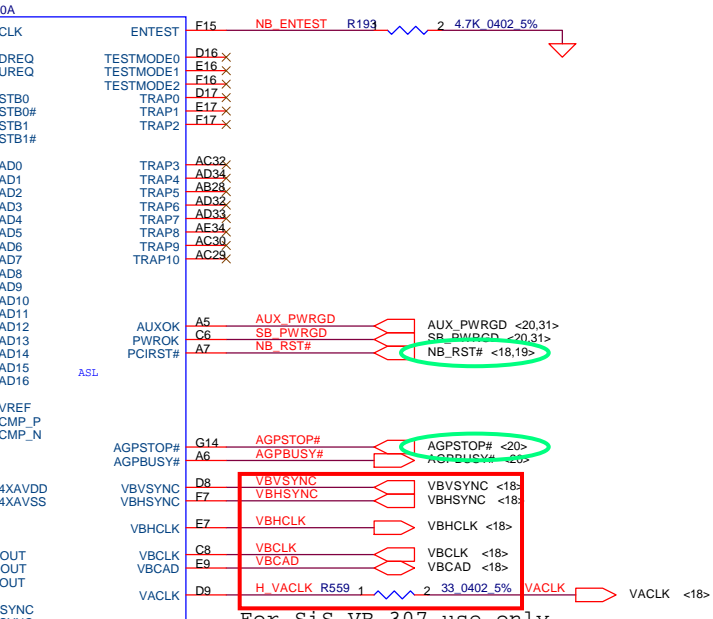
<7,19> INT_N_A
<14> REF_CLK0

DACAVIDD1
DACAVIDD2
DACAVIDD3

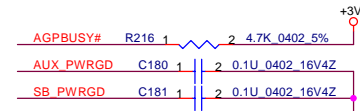
DCLKAVDD
DCLKAVSS

ECLKAVDD
ECLKAVSS

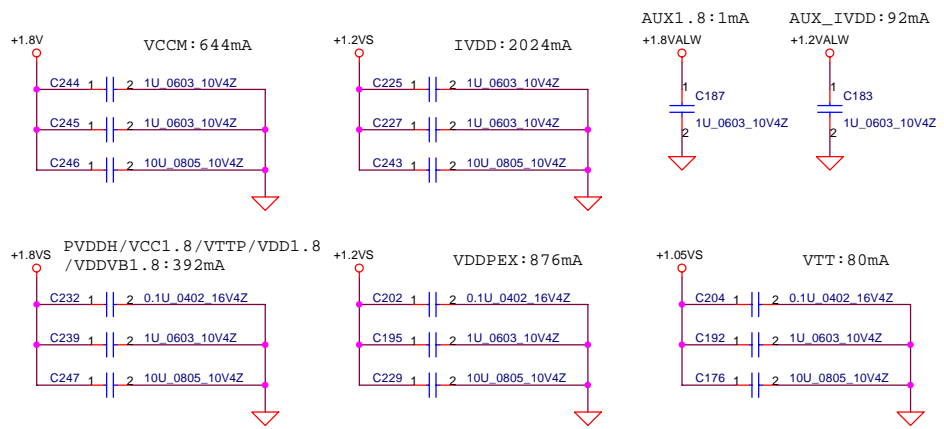
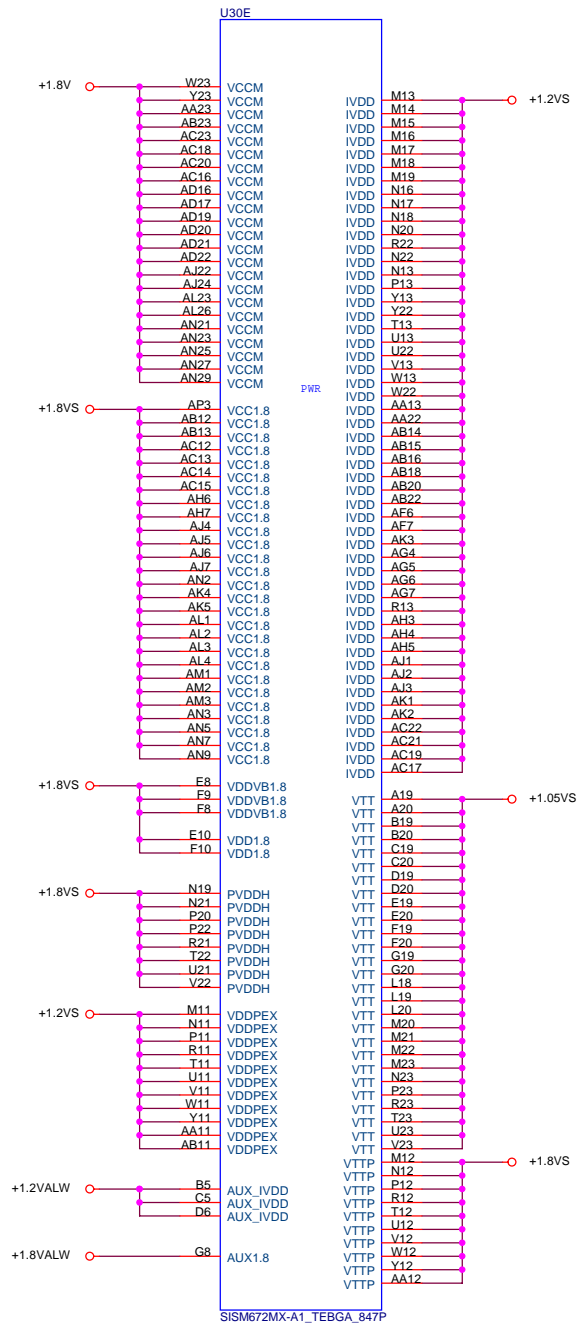
SISM672MX-A1_TEBGA_847P



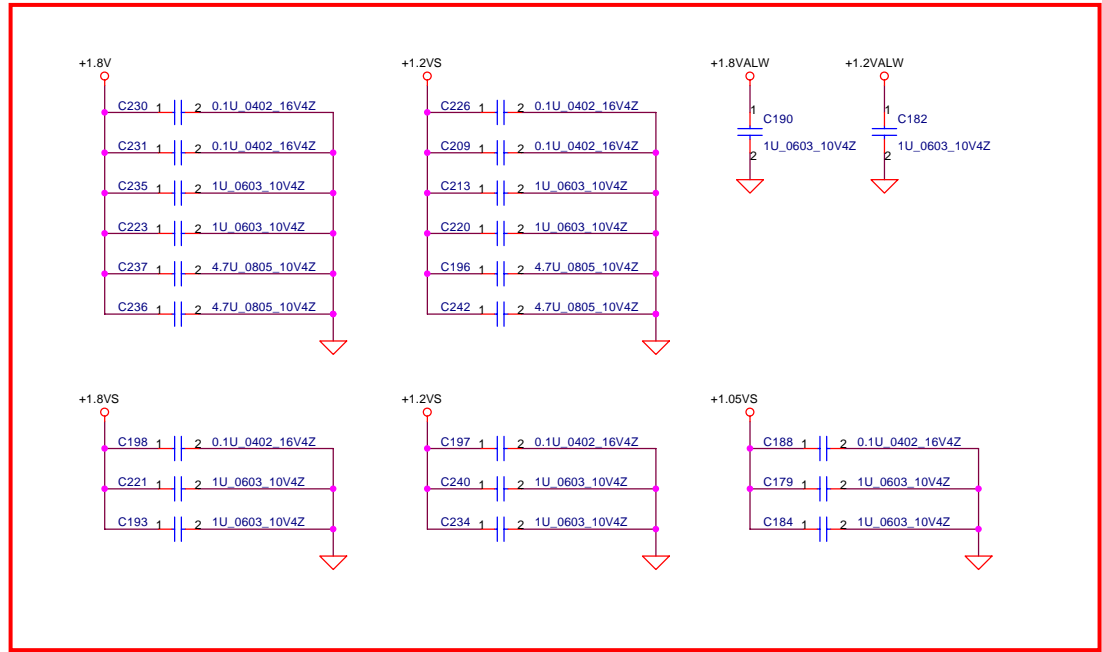
For Sis VB 307 use only



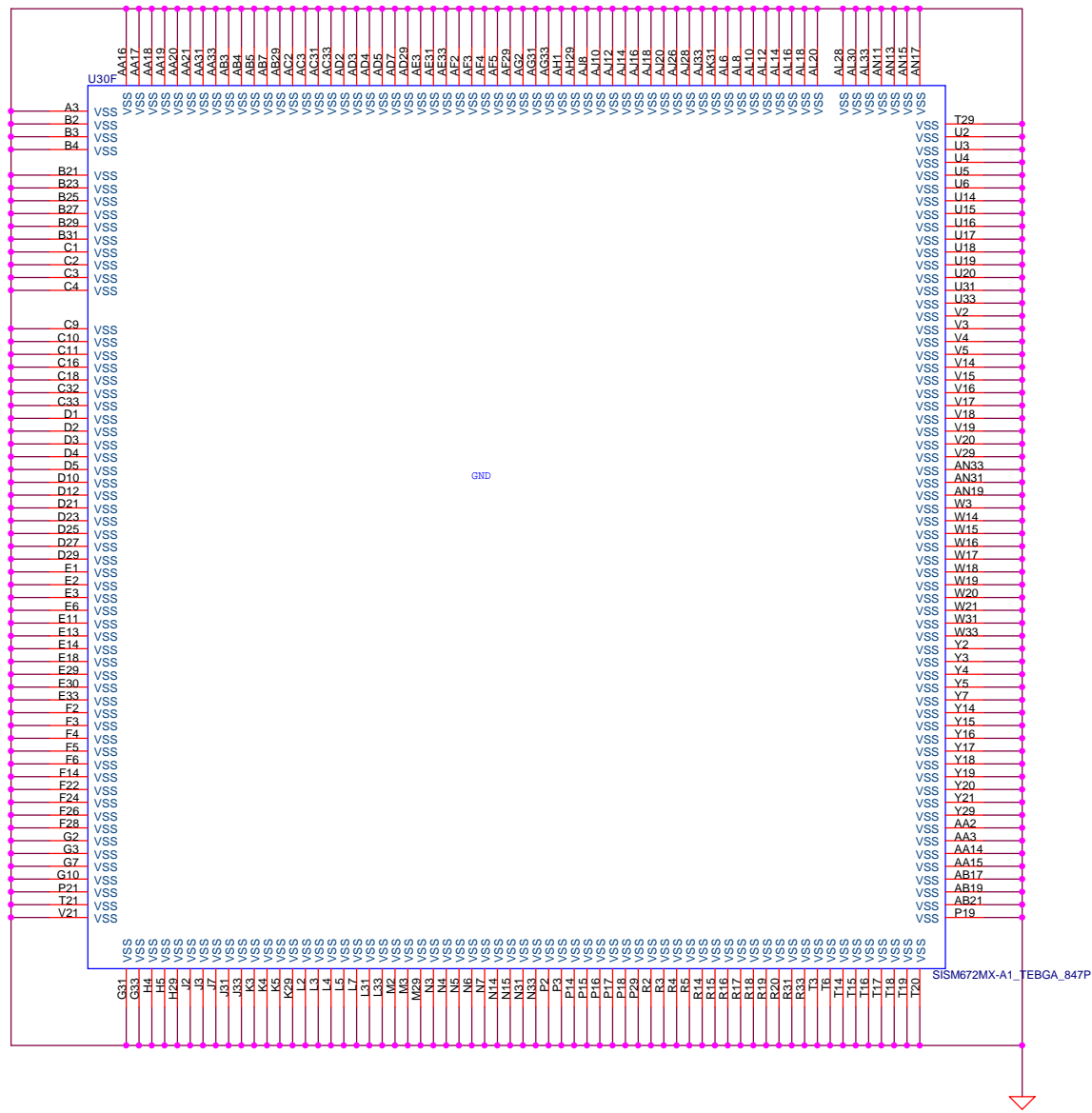
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2006/08/18				2007/8/18				M672MX (3/5)-ASL			
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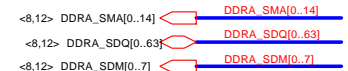
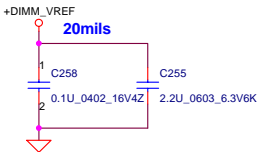
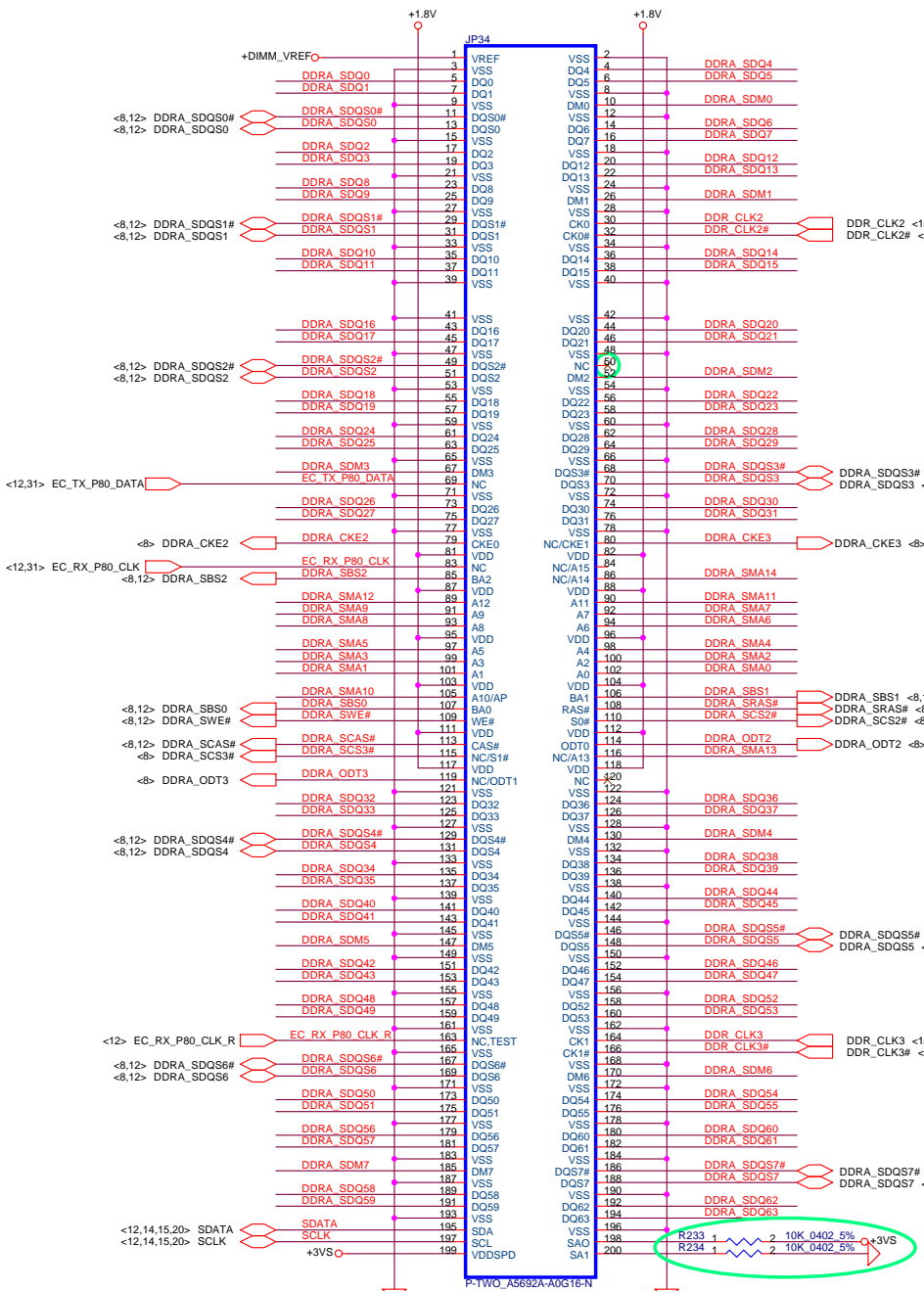
Place these Cap under M672MX solder side.



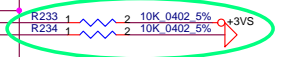
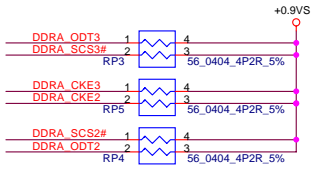
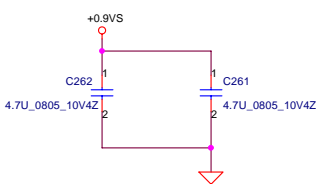
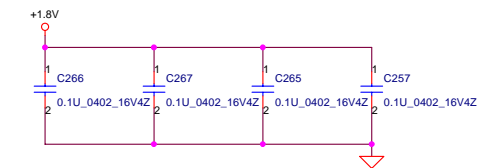
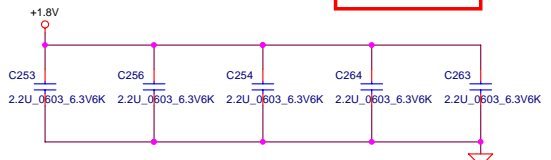
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Layout Note:
Place near JP34

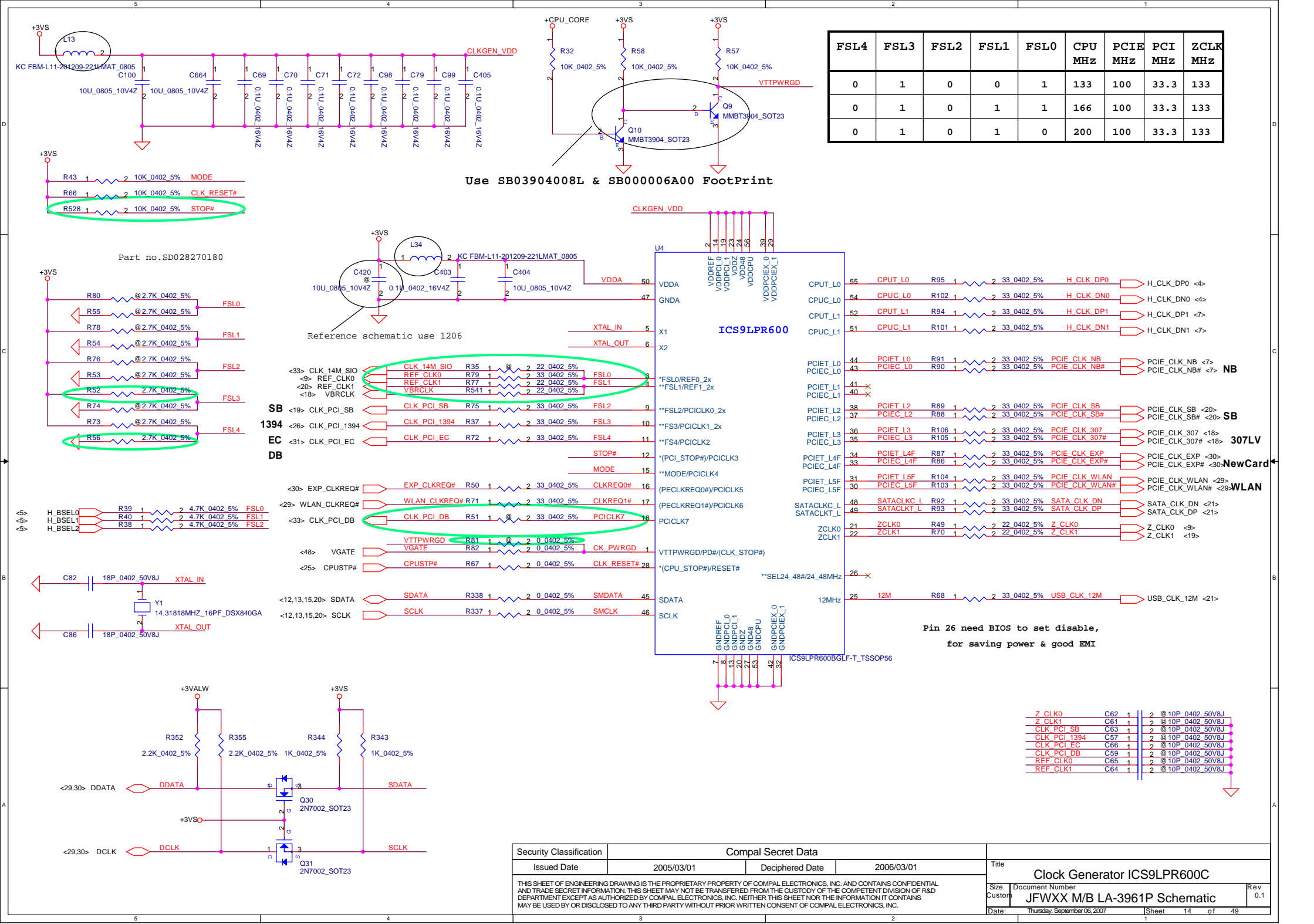


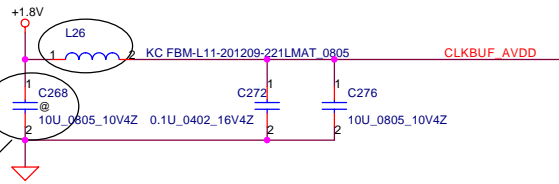
Layout Note:
Place these resistor
closely JP34,all
trace length Max=1.5"

Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

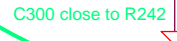
DIMM1 STD H:9.2mm (BOT)

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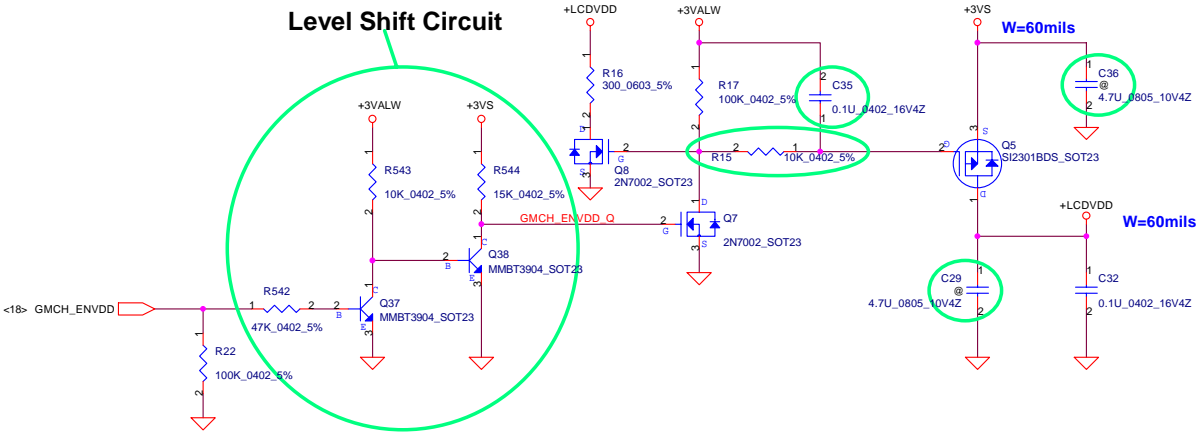


Horizontal rotate

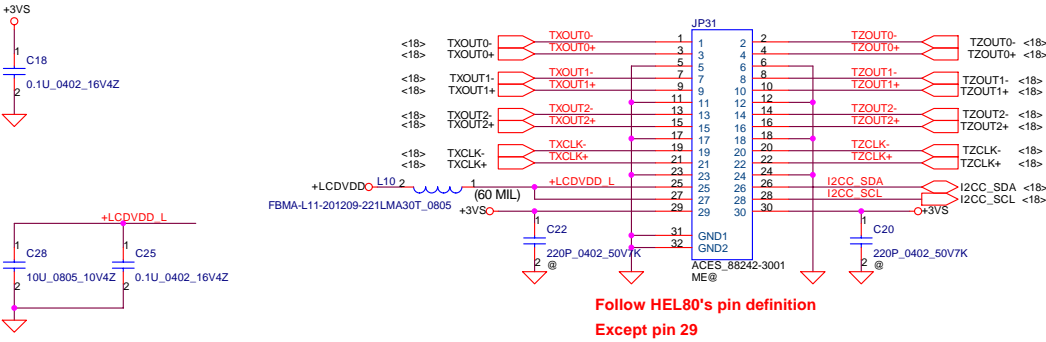


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				Size	Document Number
				Customer	JFWXX M/B LA-3961P Schematic
				Date:	Thursday, September 06, 2007
				Sheet	15 of 49

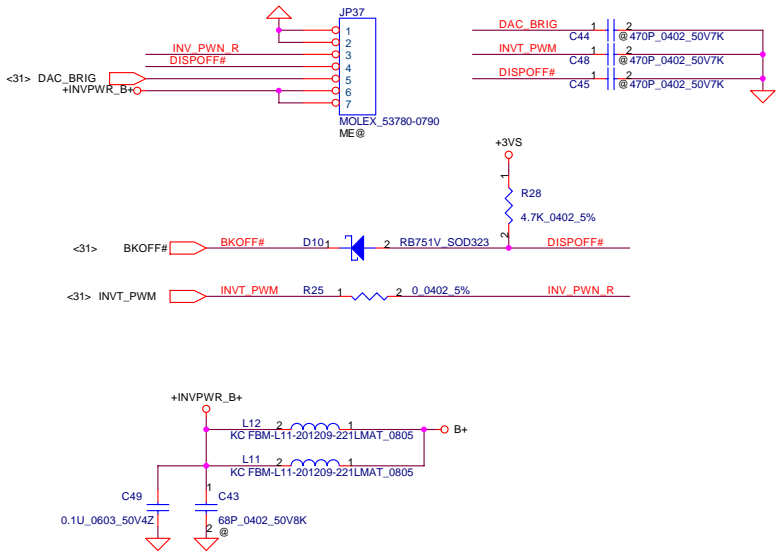
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

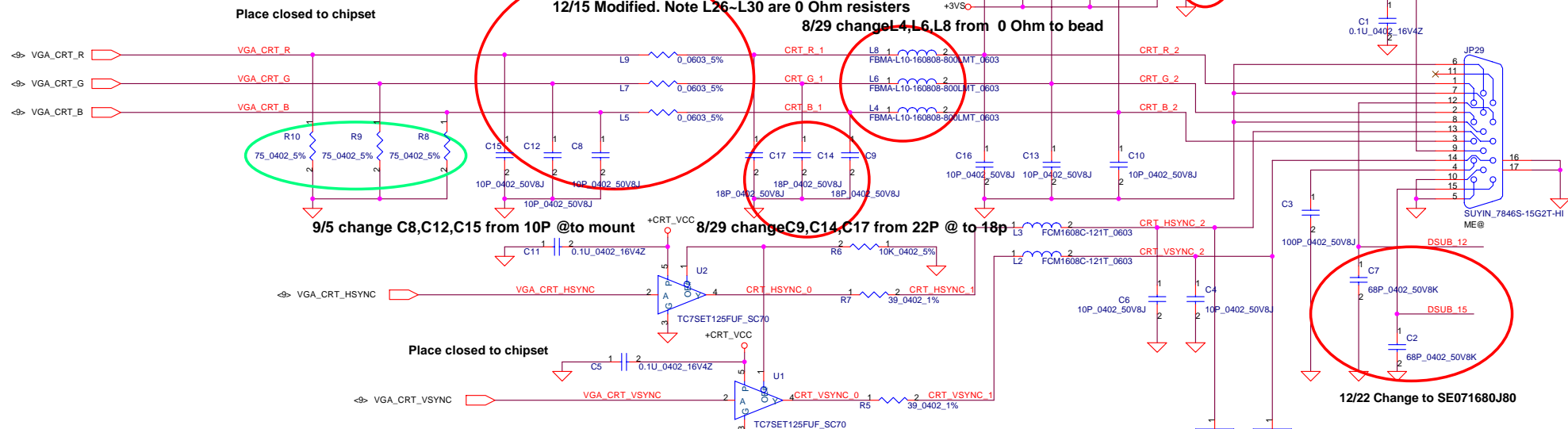


INVERTER Conn.

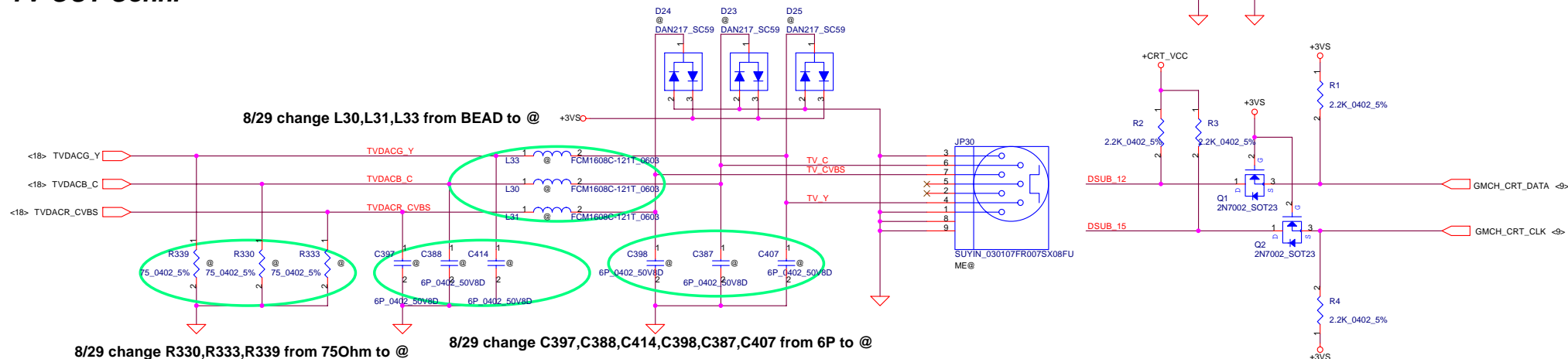


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				JFWXX M/B LA-3961P Schematic		
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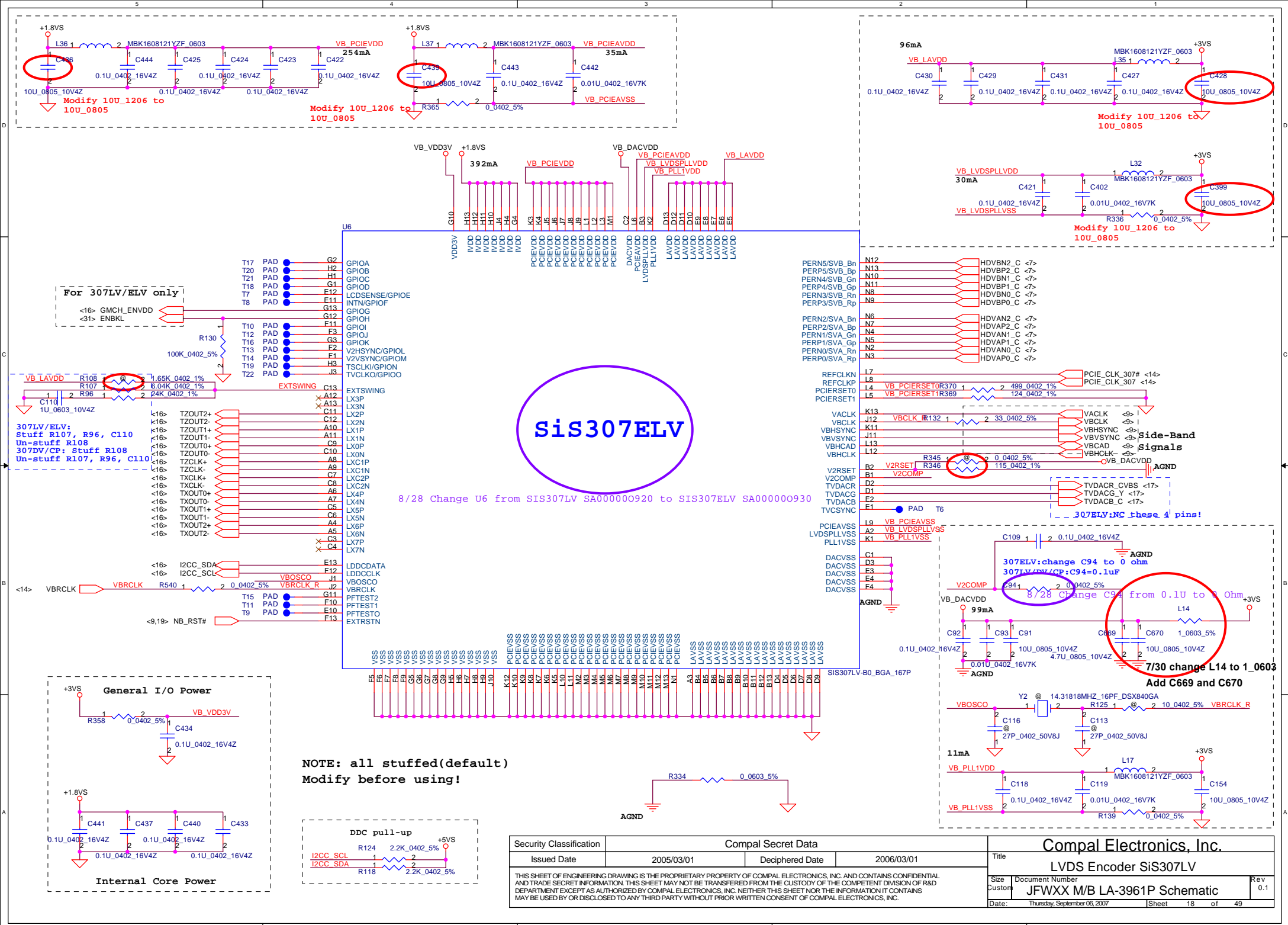
CRT Connector

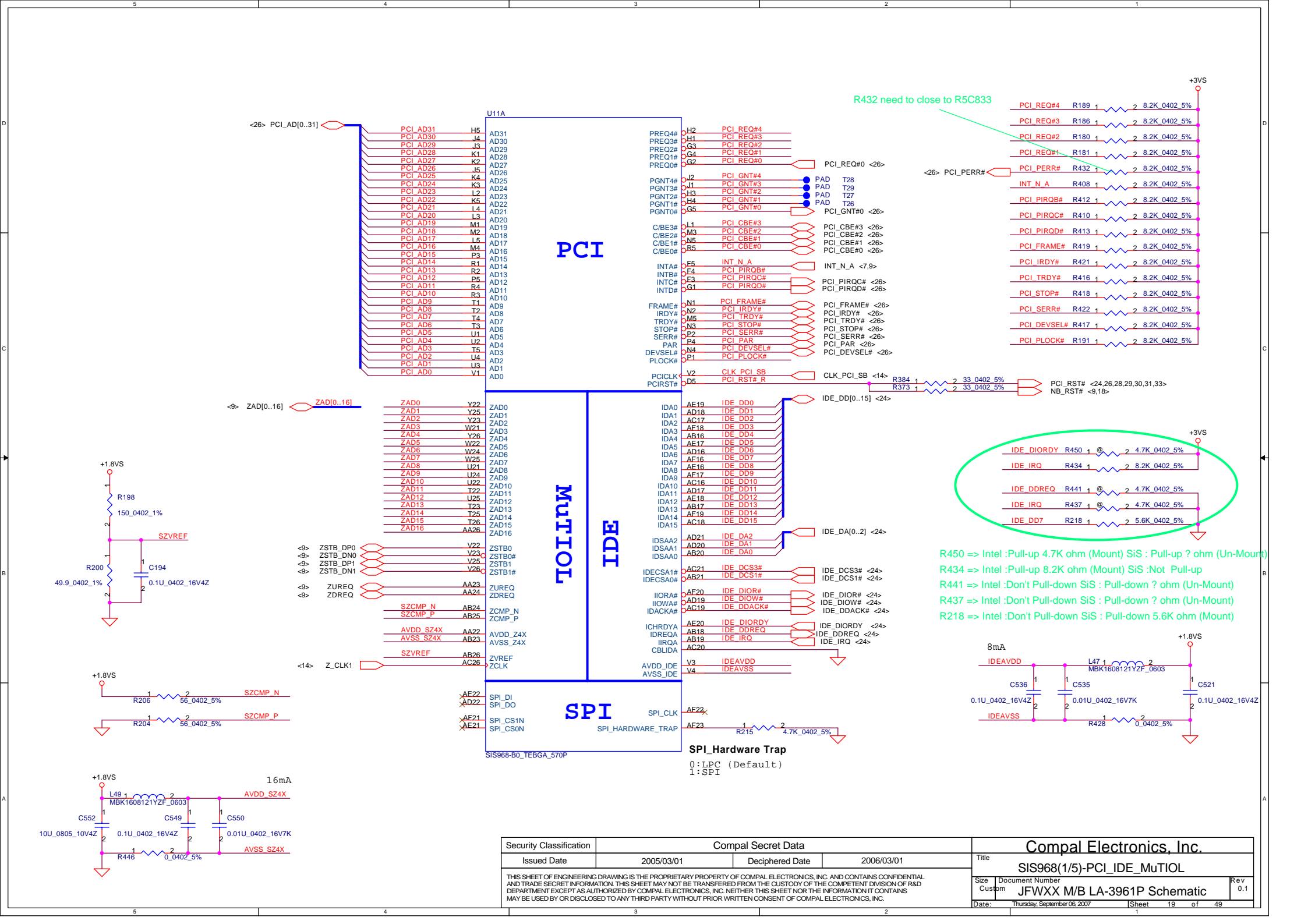


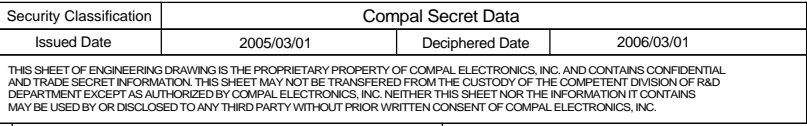
TV-OUT Conn.

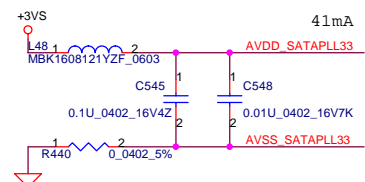
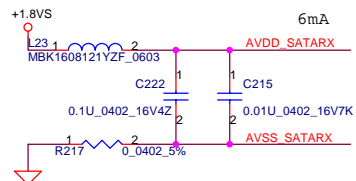
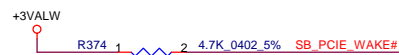
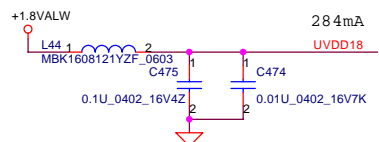
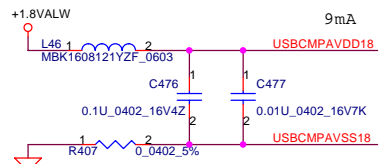
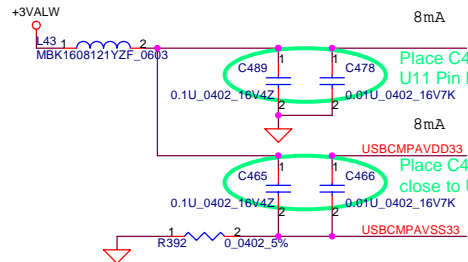
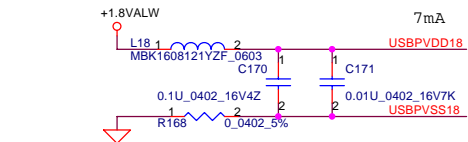


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Size B	Document Number	JFWXX M/B LA-3961P Schematic		Rev	0.1
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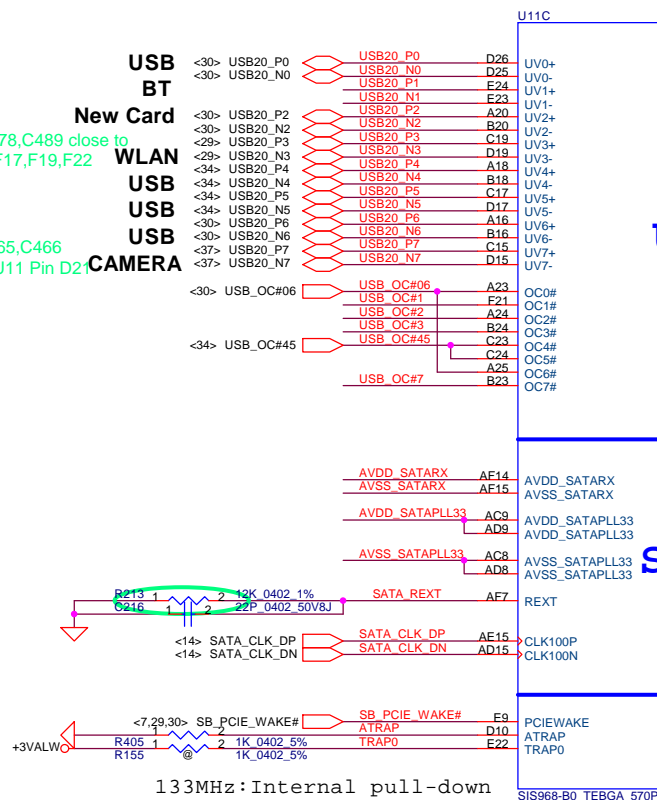




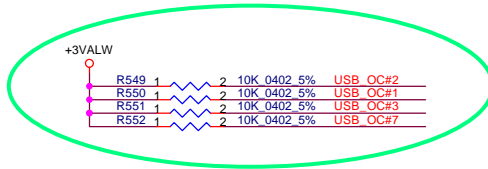
USB BT
New Card
WLAN
USB
USB
CAMERA

Place C478,C489 close to U11 Pin F17,F19,F22

Place C465,C466 close to U11 Pin D21

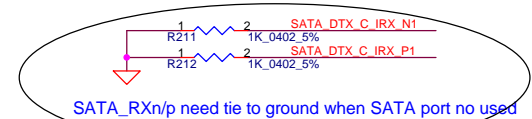
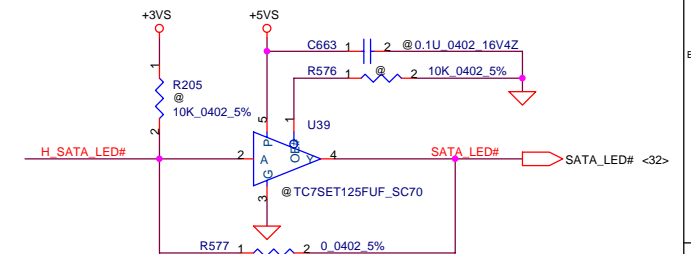


133MHz:Internal pull-down
66MHz:External pull-up



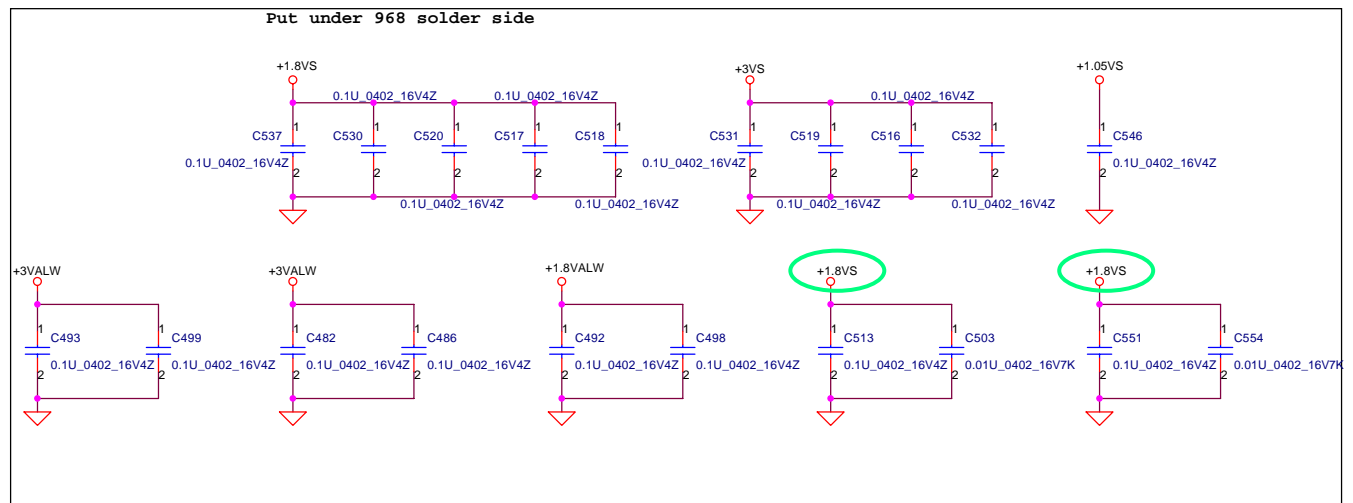
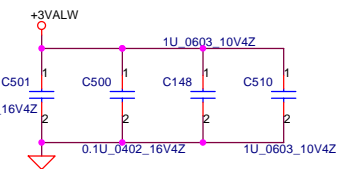
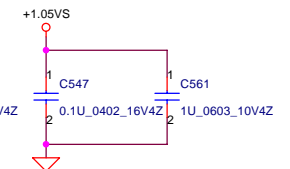
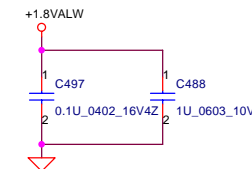
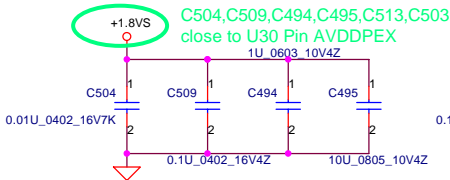
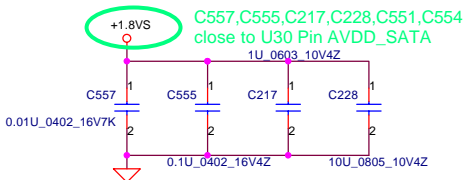
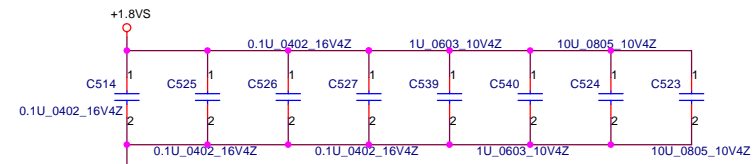
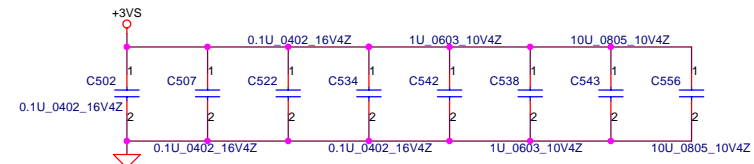
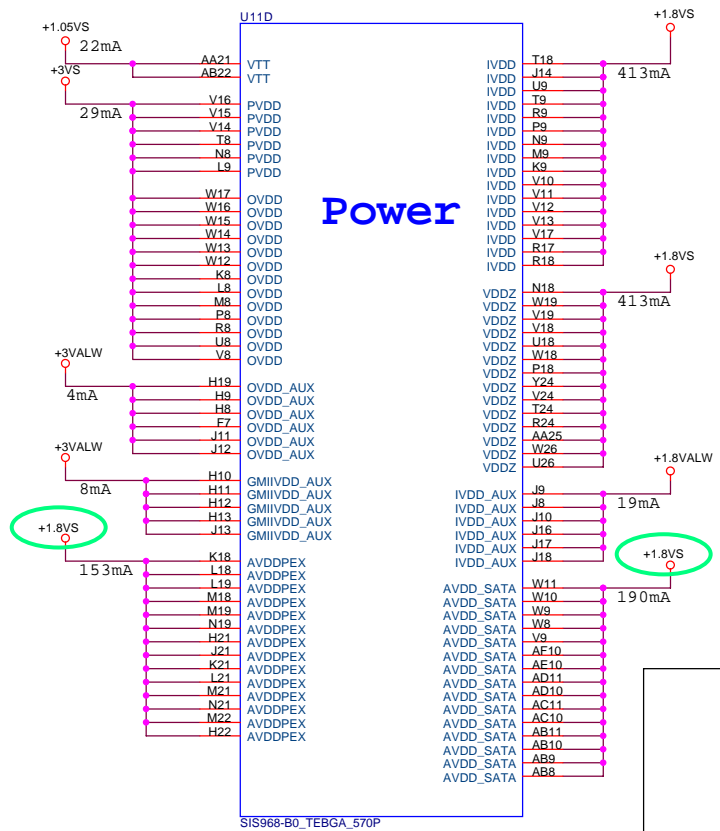
USB

SATA

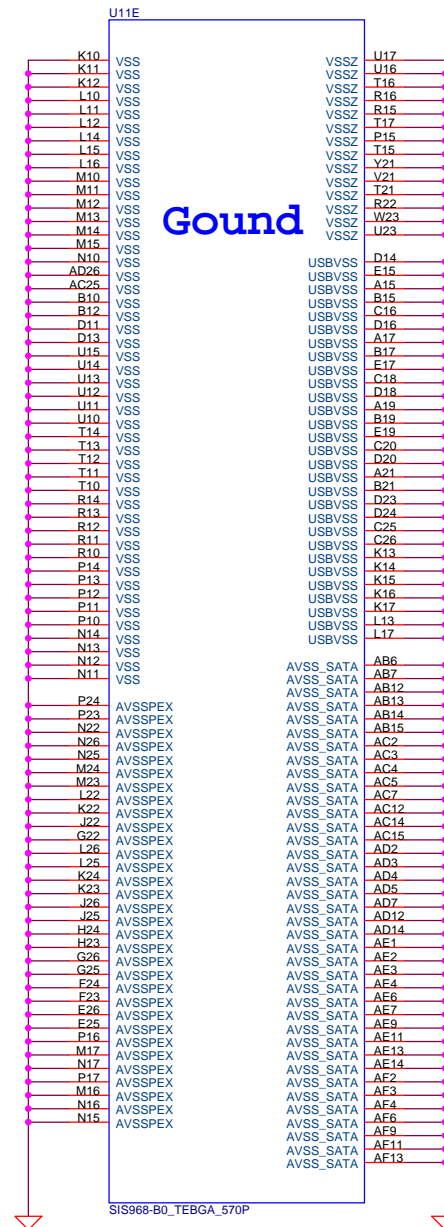


SATA_RXn/p need tie to ground when SATA port no used

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Size	Document Number	Rev		0.1	
Custom	JFWXX M/B LA-3961P Schematic	Date:		Thursday, September 06, 2007	
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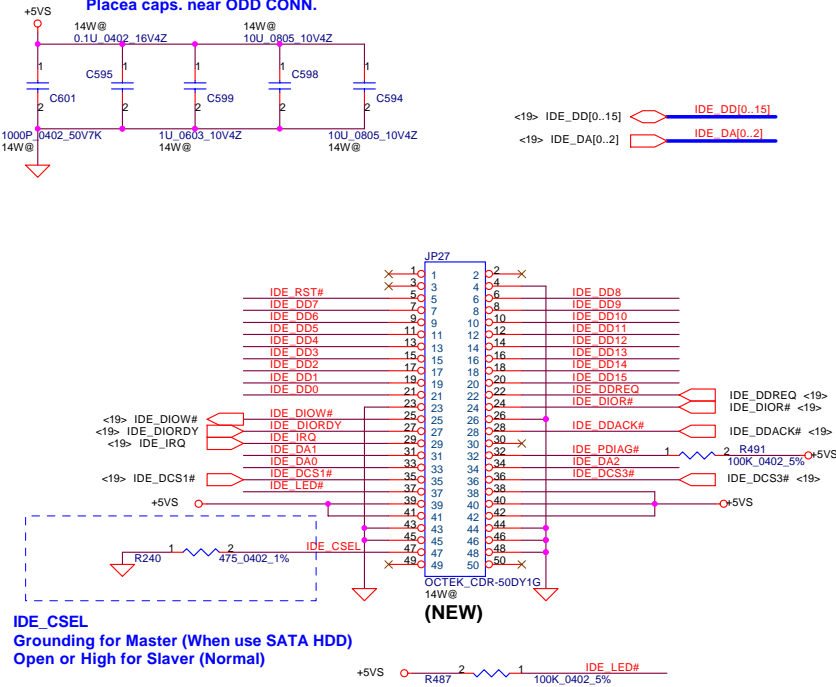
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	
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Size		Document Number		Rev	
Custom		JFWXX M/B LA-3961P Schematic		0.1	
Date:		Thursday, September 06, 2007		Sheet 22 of 49	



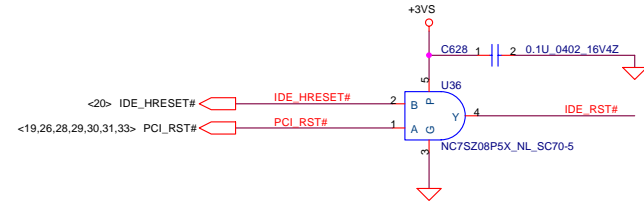
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2005/03/01	Deciphered Date	2006/03/01	Title	SIS968(5/5)-GND	
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				Custom	JFWXX M/B LA-3961P Schematic	0.1
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14W ODD Conn.

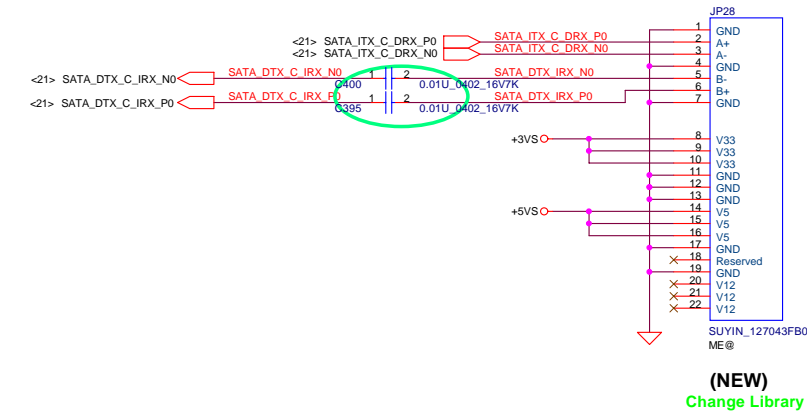
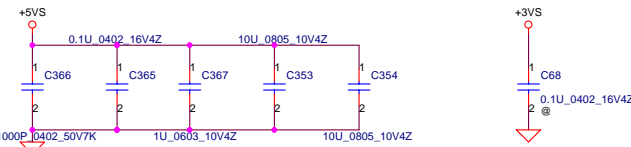
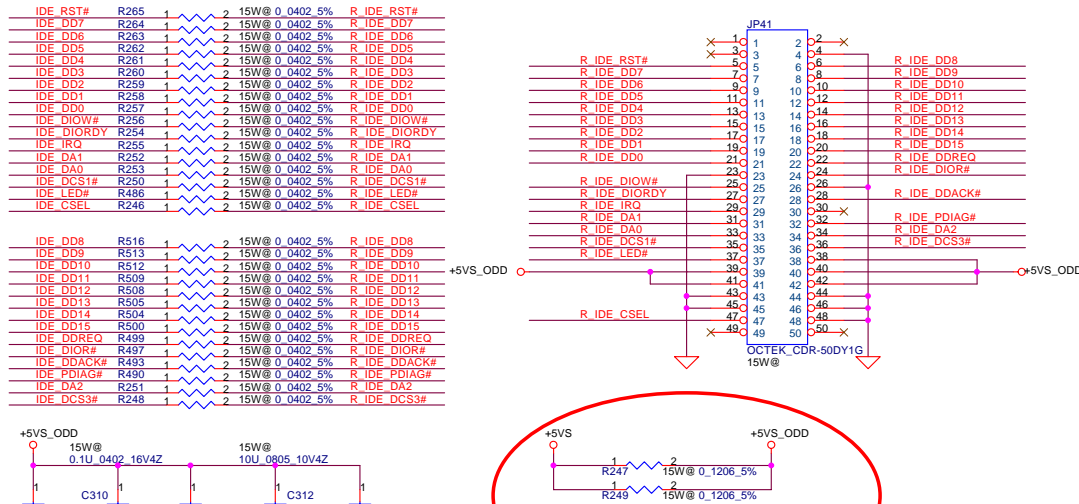
Placea caps. near ODD CONN.



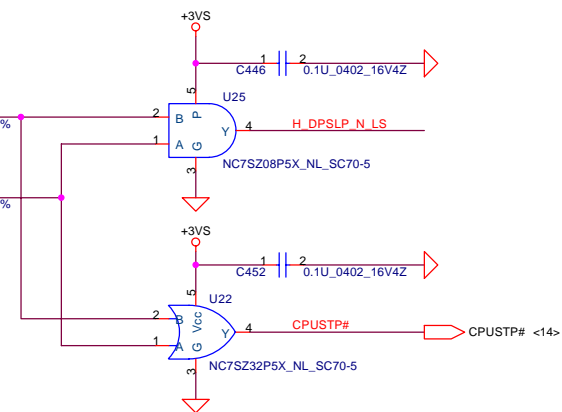
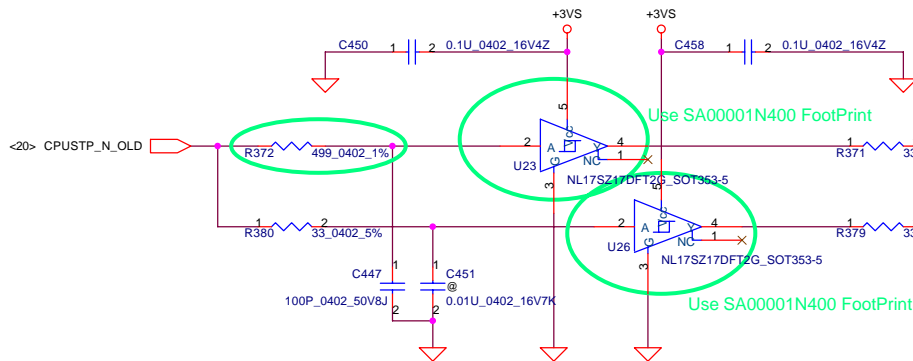
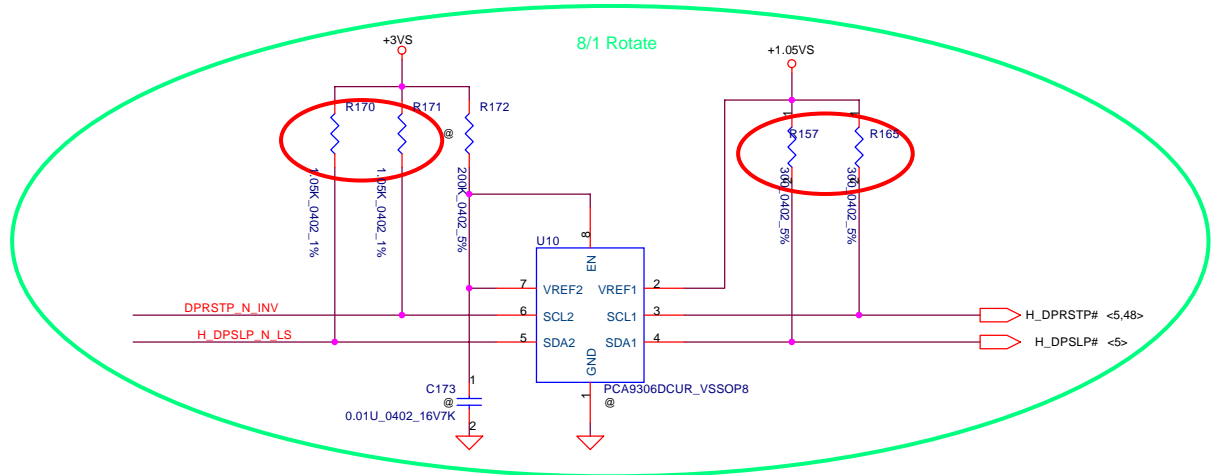
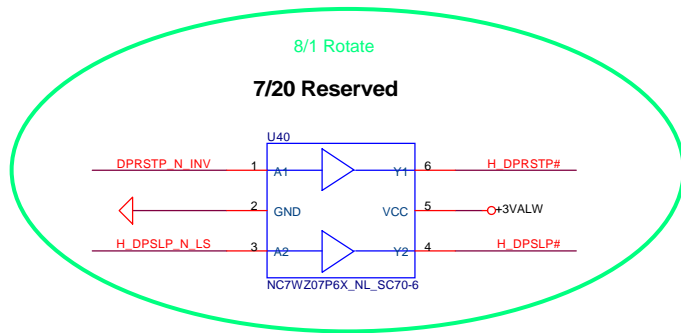
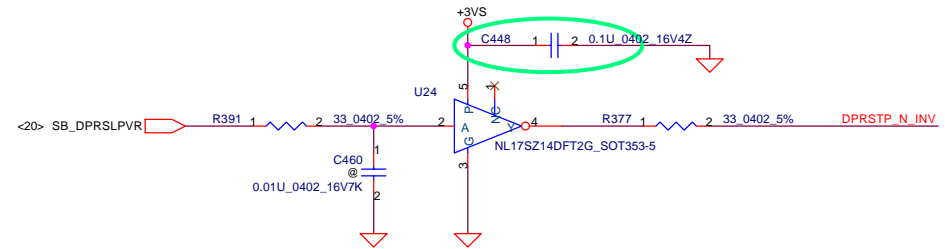
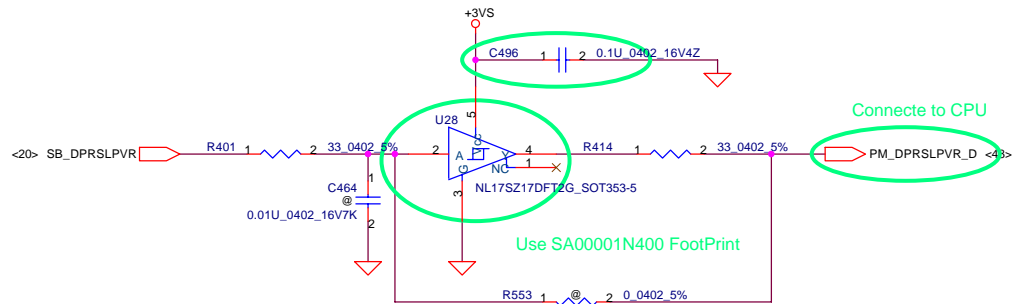
SATA HDD Conn.



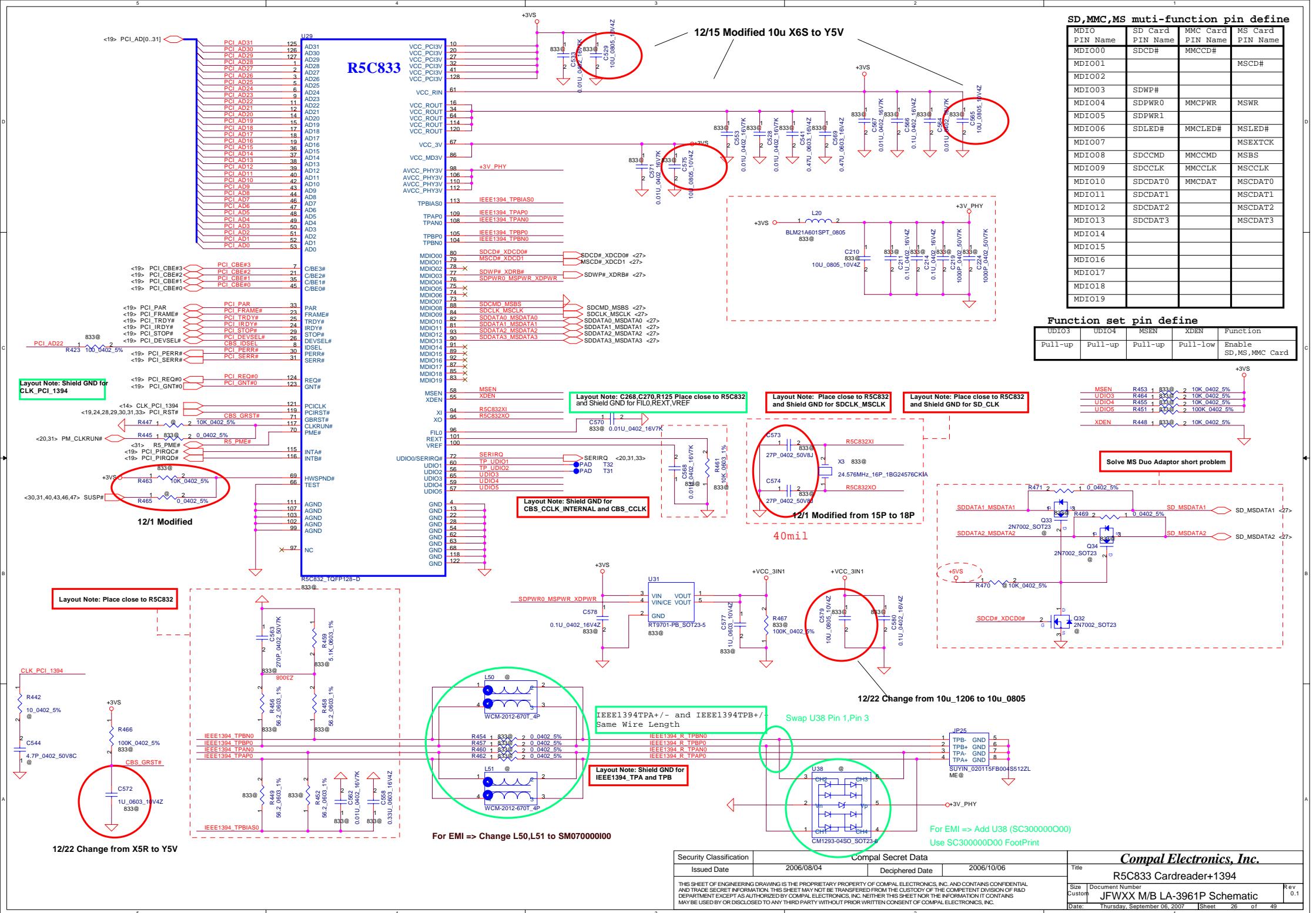
15W ODD Conn.



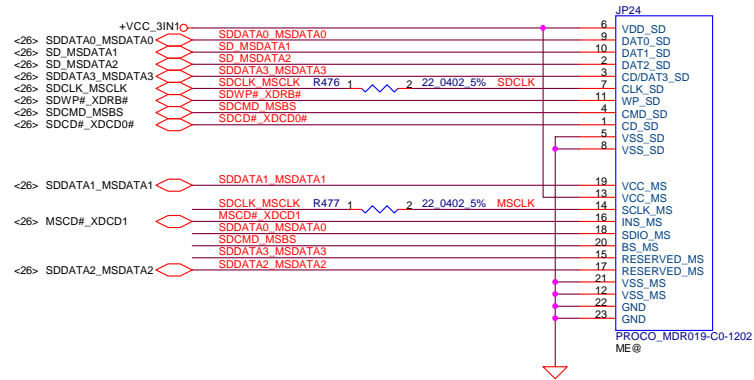
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								HDD & ODD Connector	
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				Custom Doc	Rev
				Date	Thursday, September 06, 2007
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3 in 1 Card Reader

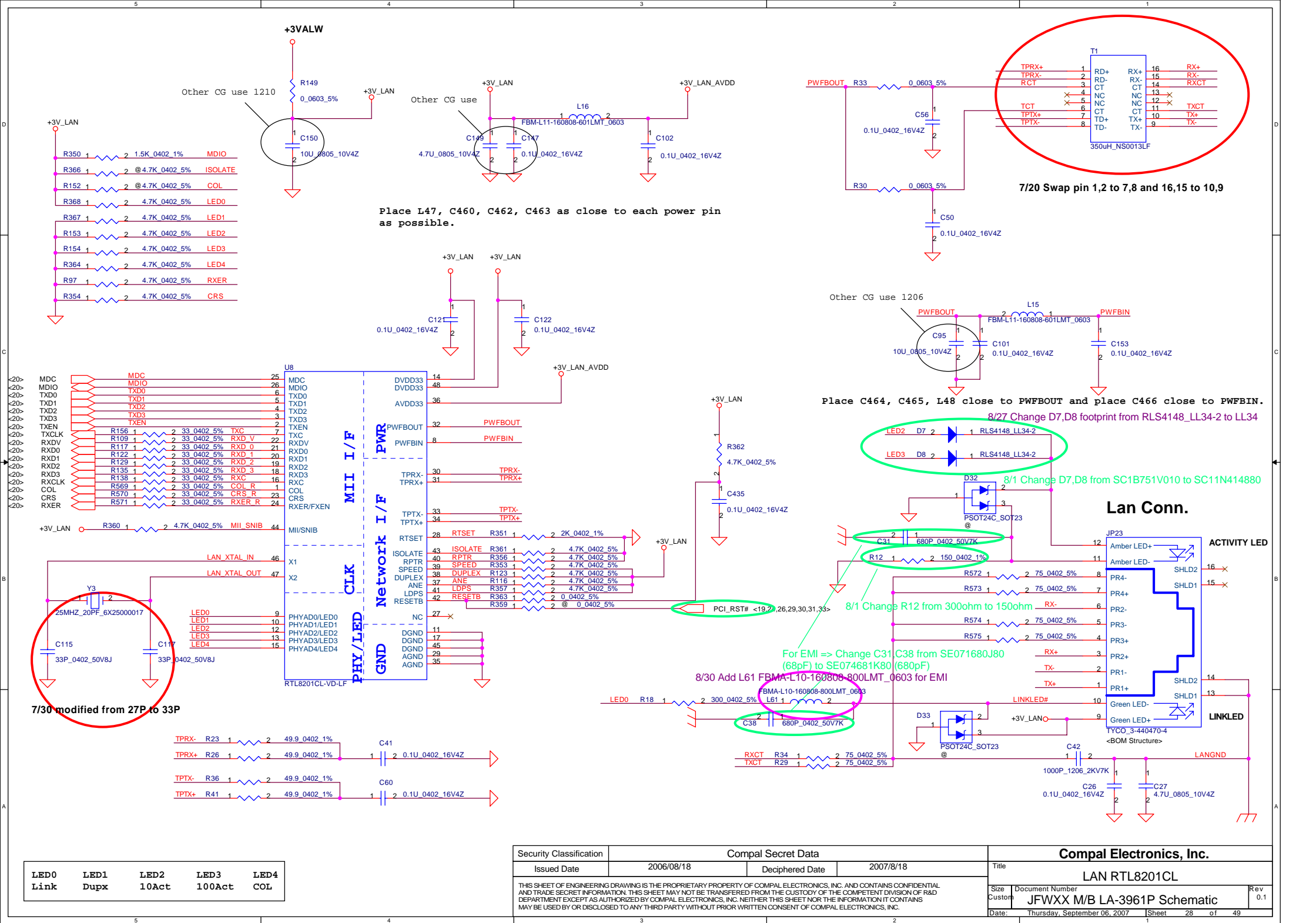


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Issued Date	2006/08/04	Deciphered Date	2006/10/06	3 IN 1 CardReader Conn.	
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Compal Electronics, Inc.

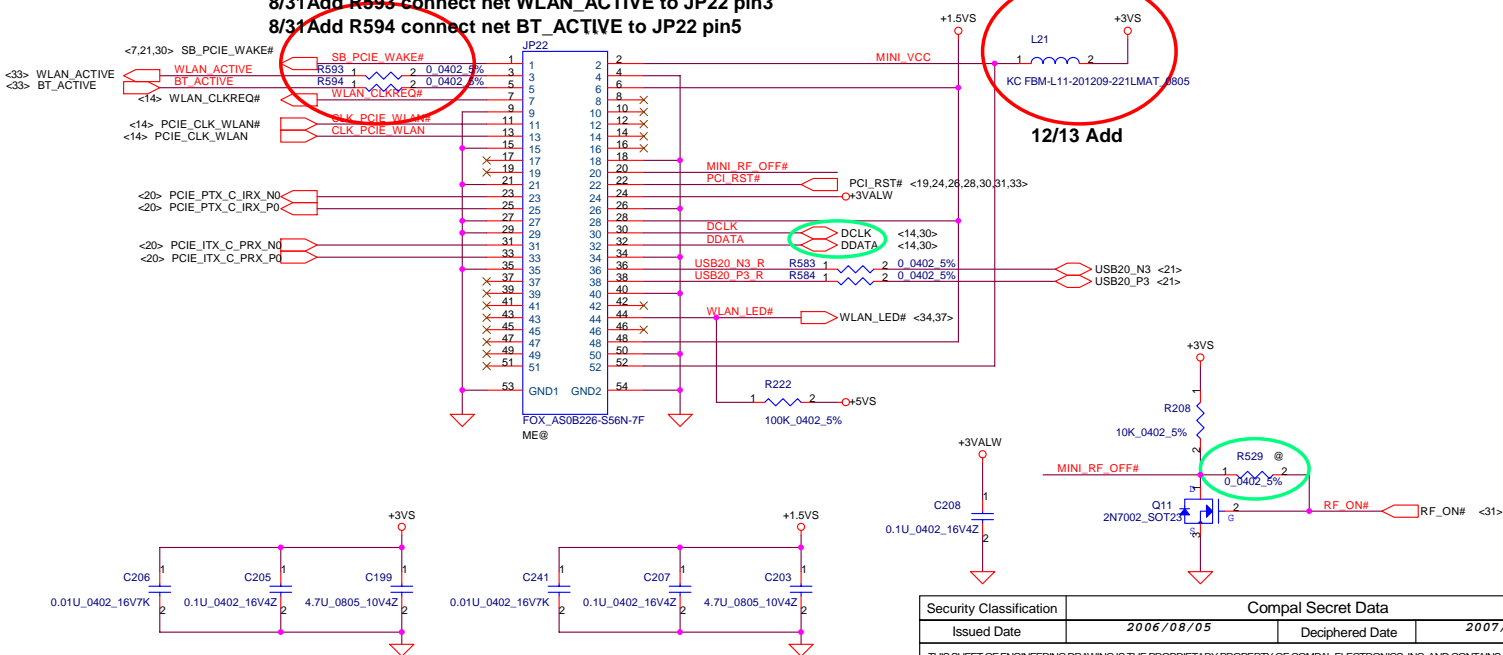
3 IN 1 CardReader Conn.

Size Custom
JFWXX M/B LA-3961P Schematic
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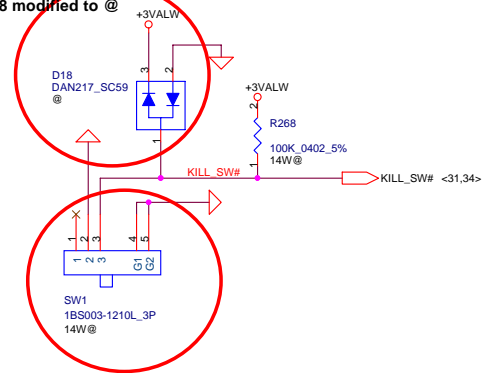
Mini-Express Card for WLAN

8/31 Add R593 connect net WLAN_ACTIVE to JP22 pin3
8/31 Add R594 connect net BT_ACTIVE to JP22 pin5



Kill SWITCH

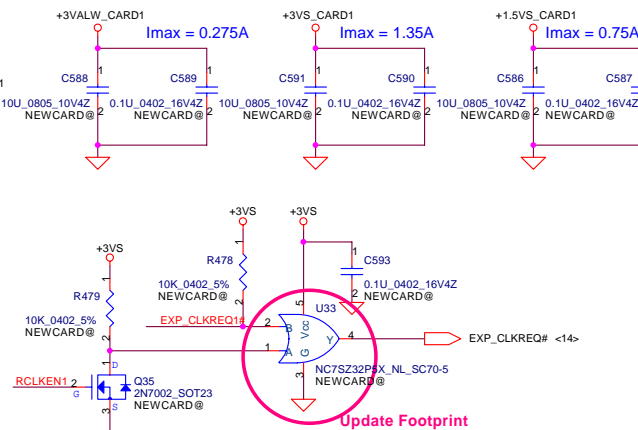
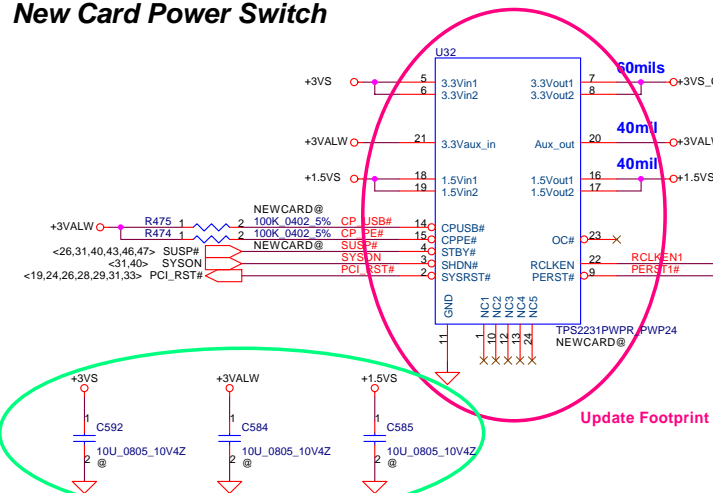
12/28 modified to @



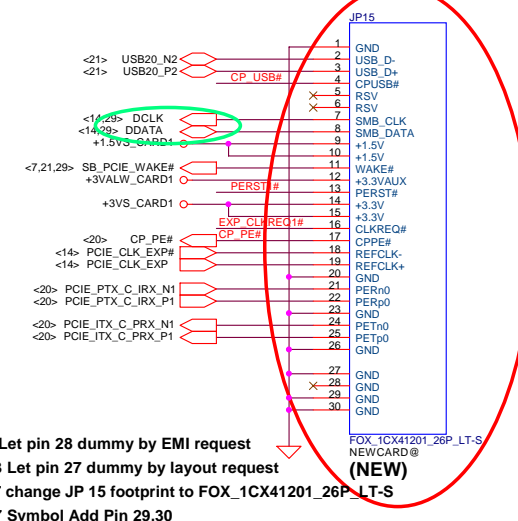
12/19 Change SW2 to correct symbol (by EMI)

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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Mini-Card/Kill SW	
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New Card Power Switch



New Card Socket (Left/TOP)



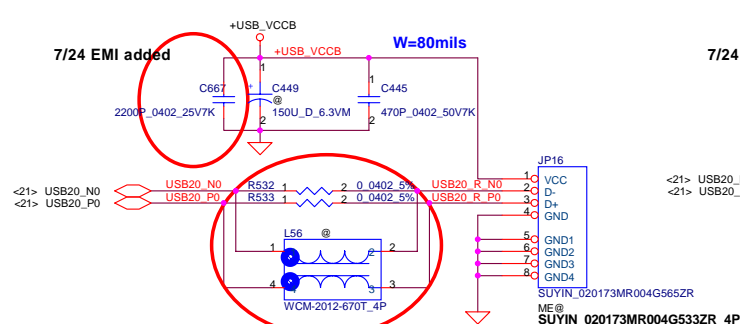
12/7 Let pin 28 dummy by EMI request

12/13 Let pin 27 dummy by layout request

12/27 change JP 15 footprint to FOX_1CX41201_26P_LT-S

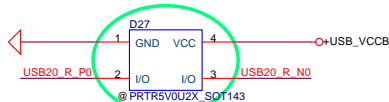
04/17 Symbol Add Pin 29,30

USB CONN. 1



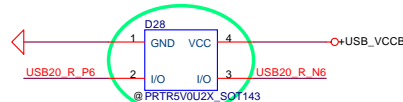
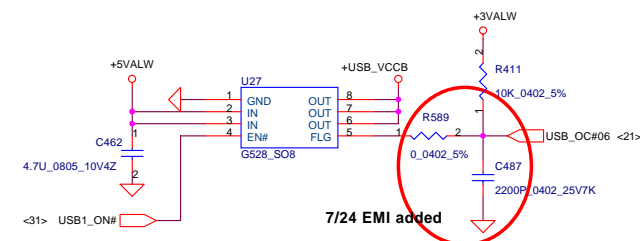
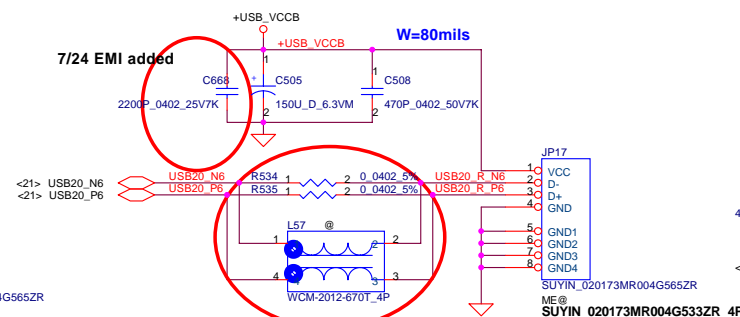
For EMI => Add R532,R533,R534,R535 (SD028000080) ,L56,L57 (SM070000I00)

7/30 change L56,57 to SM070000K00 by EMI request

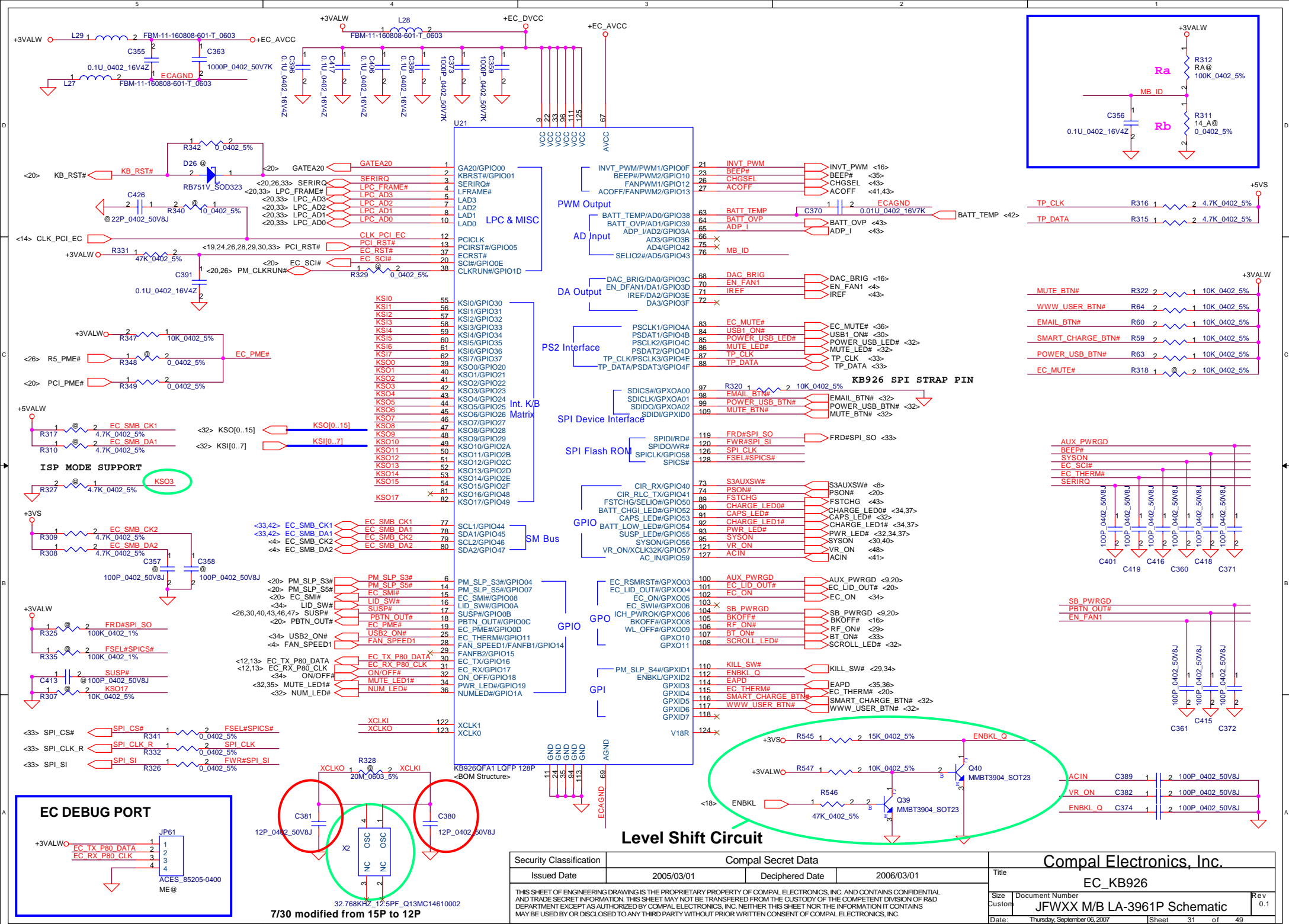


For EMI => Change D27,D28 from SC300000100 to SC300000P00

USB CONN. 2

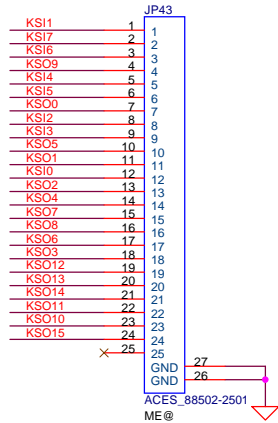


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				NewCard & USB Connector			
				Size B	Document Number	Rev. 0.	
				JFWXX M/B LA-3961P Schematic			
				Date:	Thursday, September 06, 2007	Sheet 30 of 49	

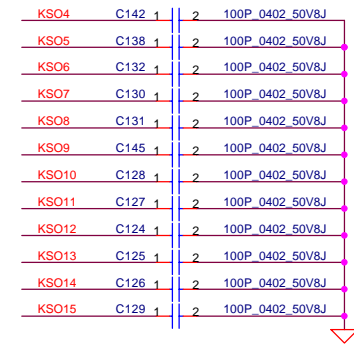
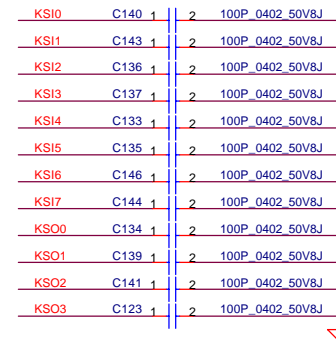
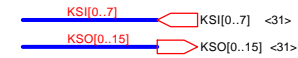
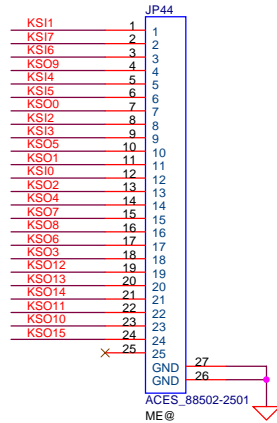


INT_KBD Conn.

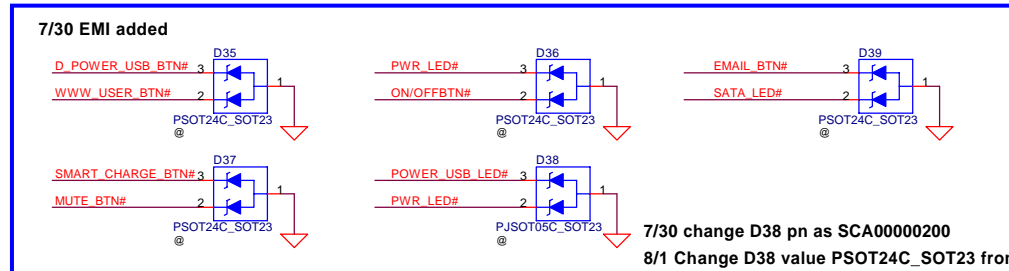
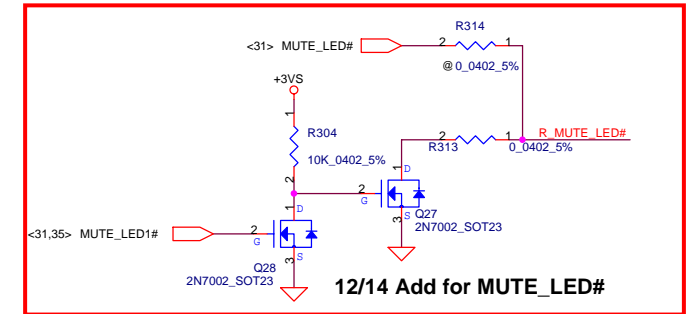
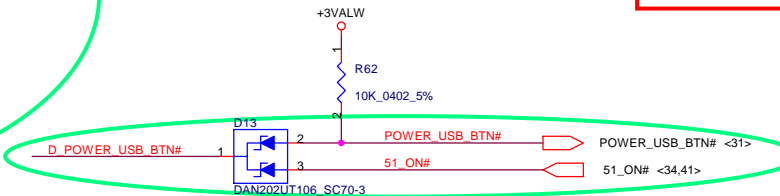
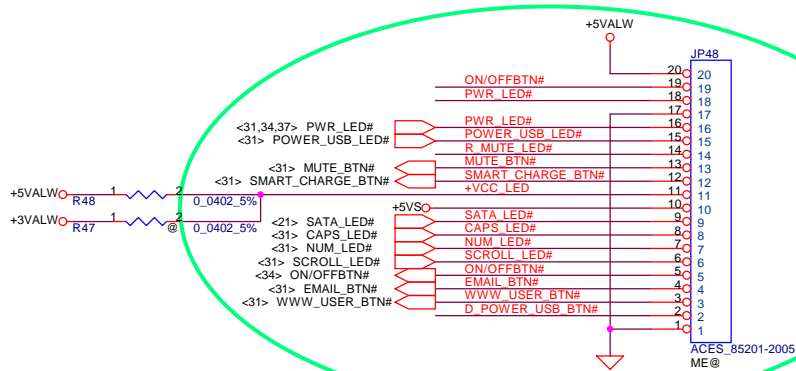
For JFW91



For JFW01



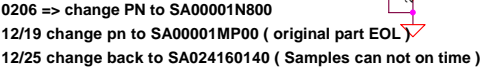
Switch Board Conn.



7/30 change D38 pn as SCA00000200

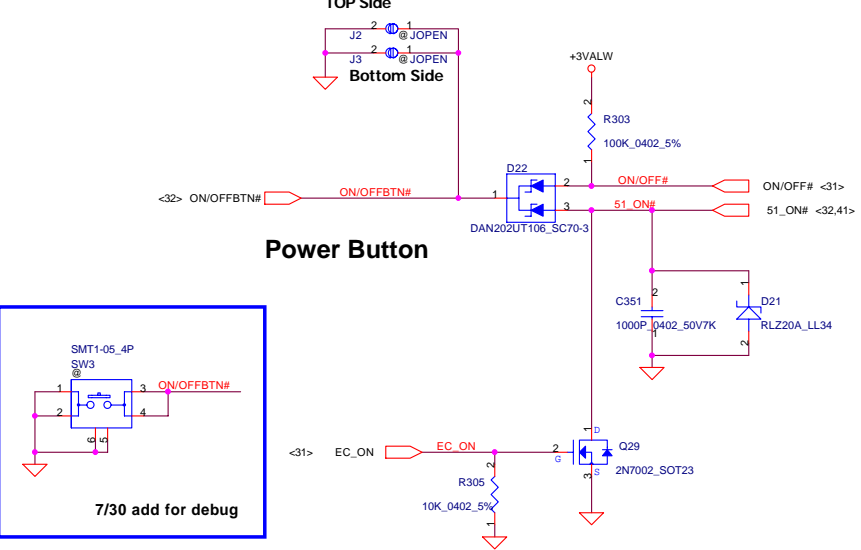
8/1 Change D38 value PSOT24C_SOT23 from to PJSOT05C_SOT23 , Add D39

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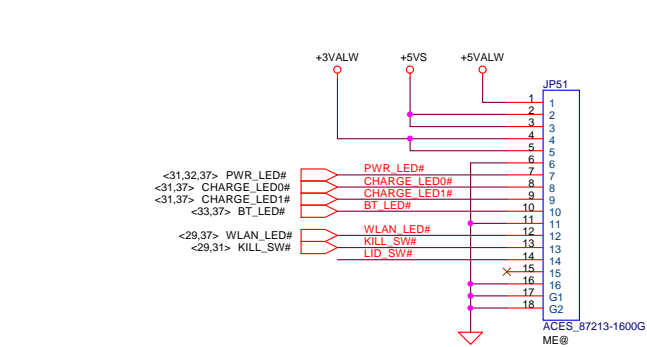


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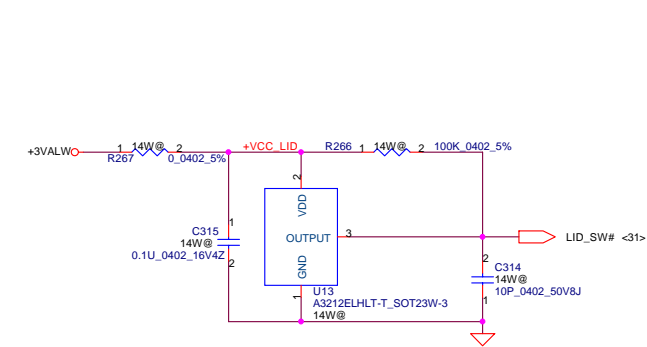
ON/OFF switch



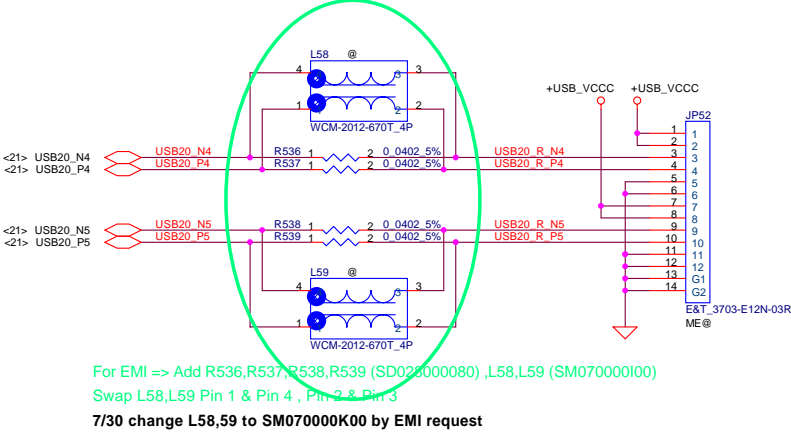
Front LED Board



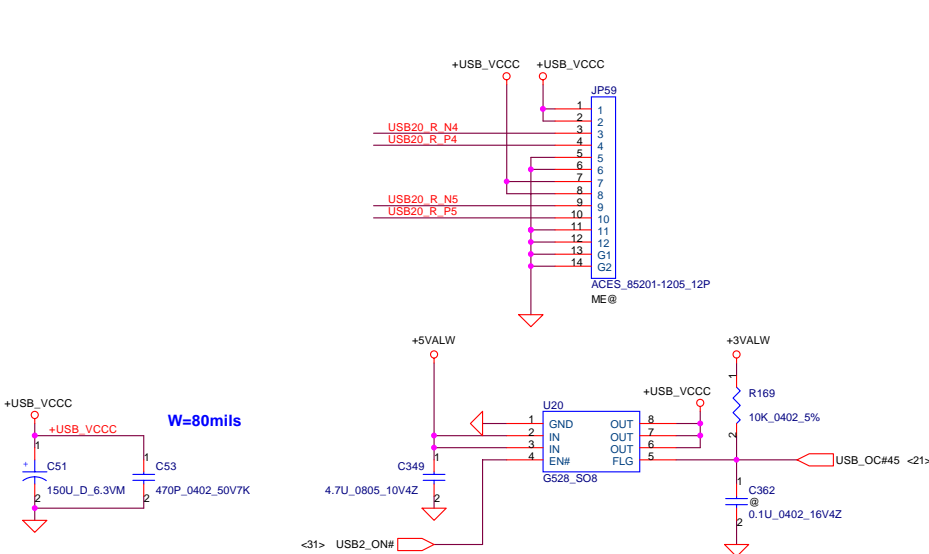
Lid Switch



For JFW01 IO Conn.

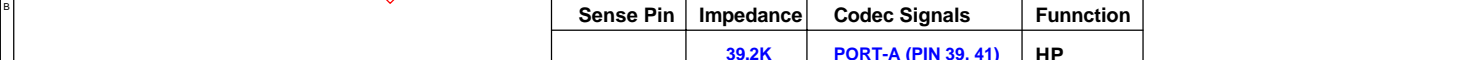


For JFW91 IO Conn.

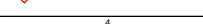


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+AVDD_AC97 +3VS_DVDD



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BEED#

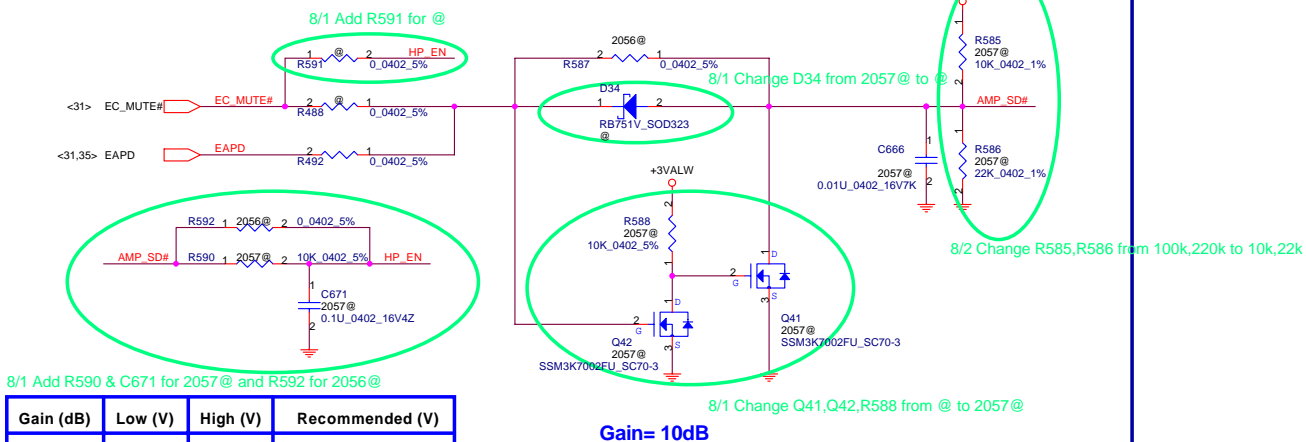
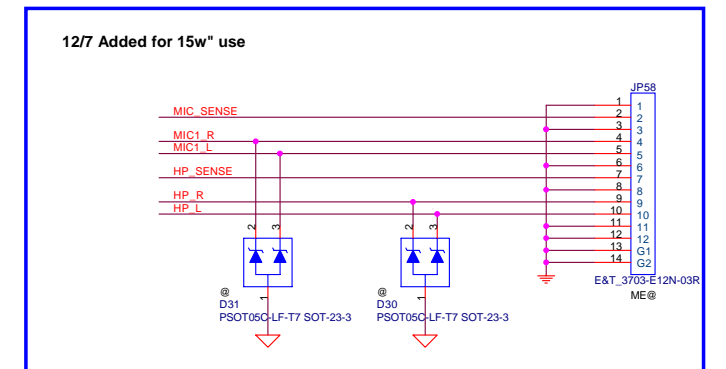
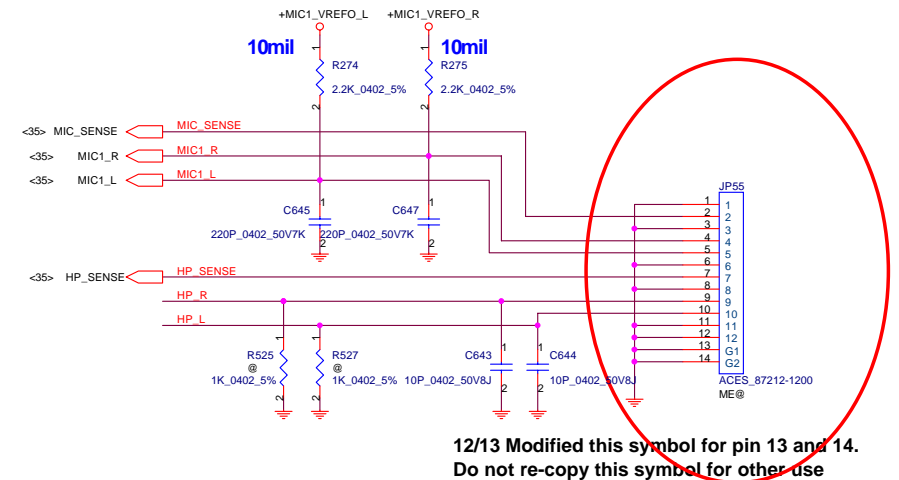
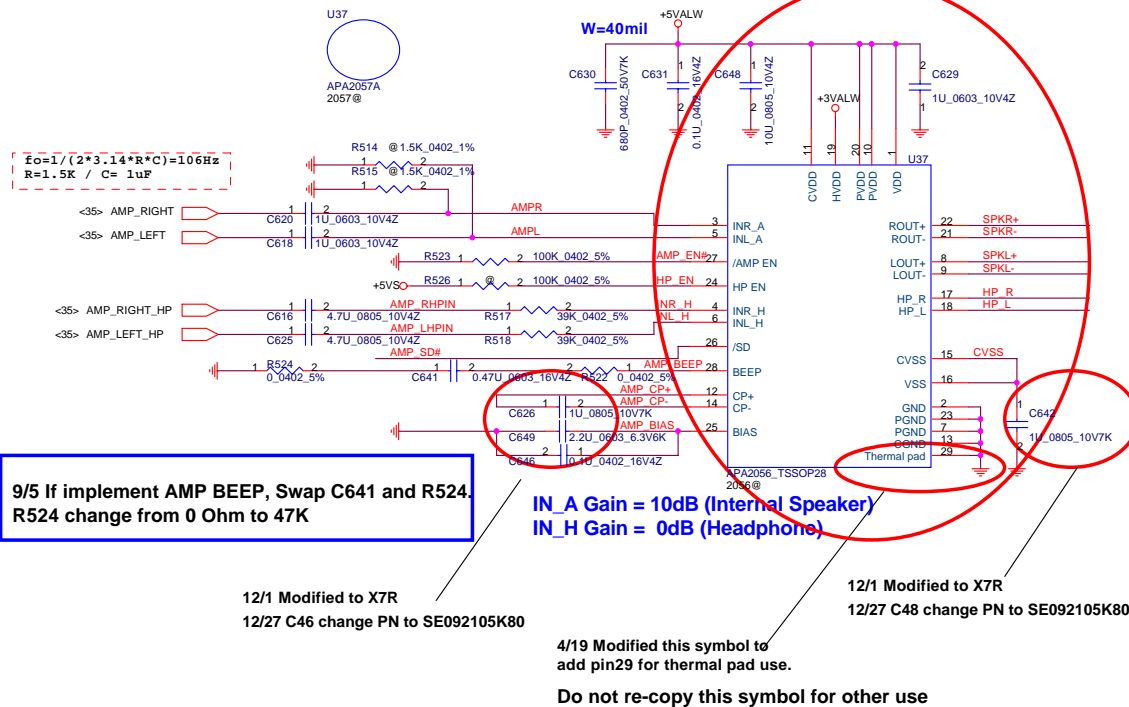
22-2515

<20> SB_SPKR 1U_0603_10V4Z 560_0402_5% B 2SC4411K SOT23 R485 3.4K 0402_5%

	3	2	1
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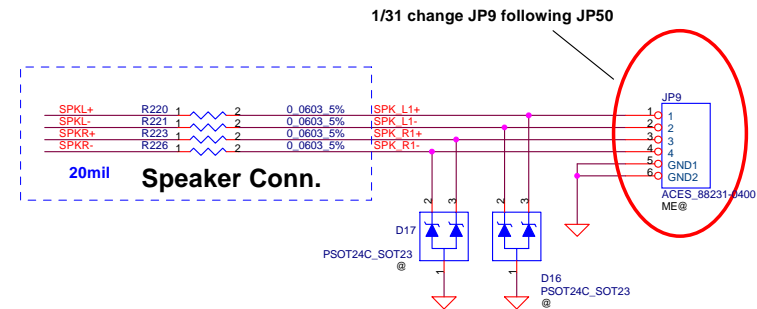
APA2056 SPK/HP Amplifier

7/20 Add U37 for APA2057A SA00001QD00



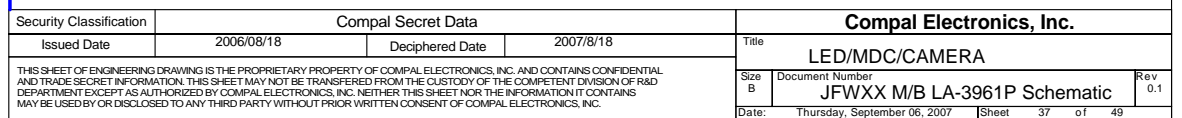
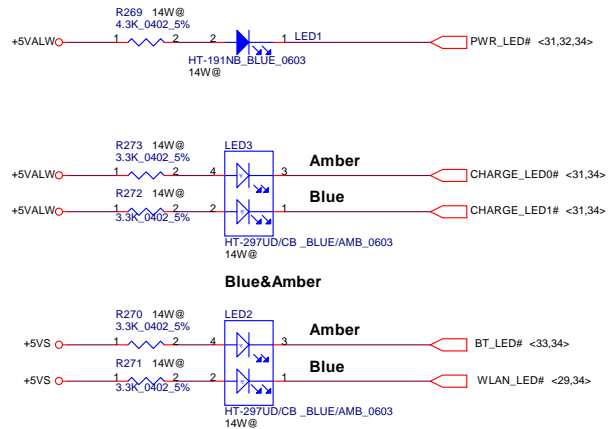
Gain (dB)	Low (V)	High (V)	Recommended (V)
10	3.45	3.51	3.48
11	3.56	3.62	3.59
12	3.68	3.73	3.70
13	3.80	3.85	3.82
15	4.02	4.07	4.05

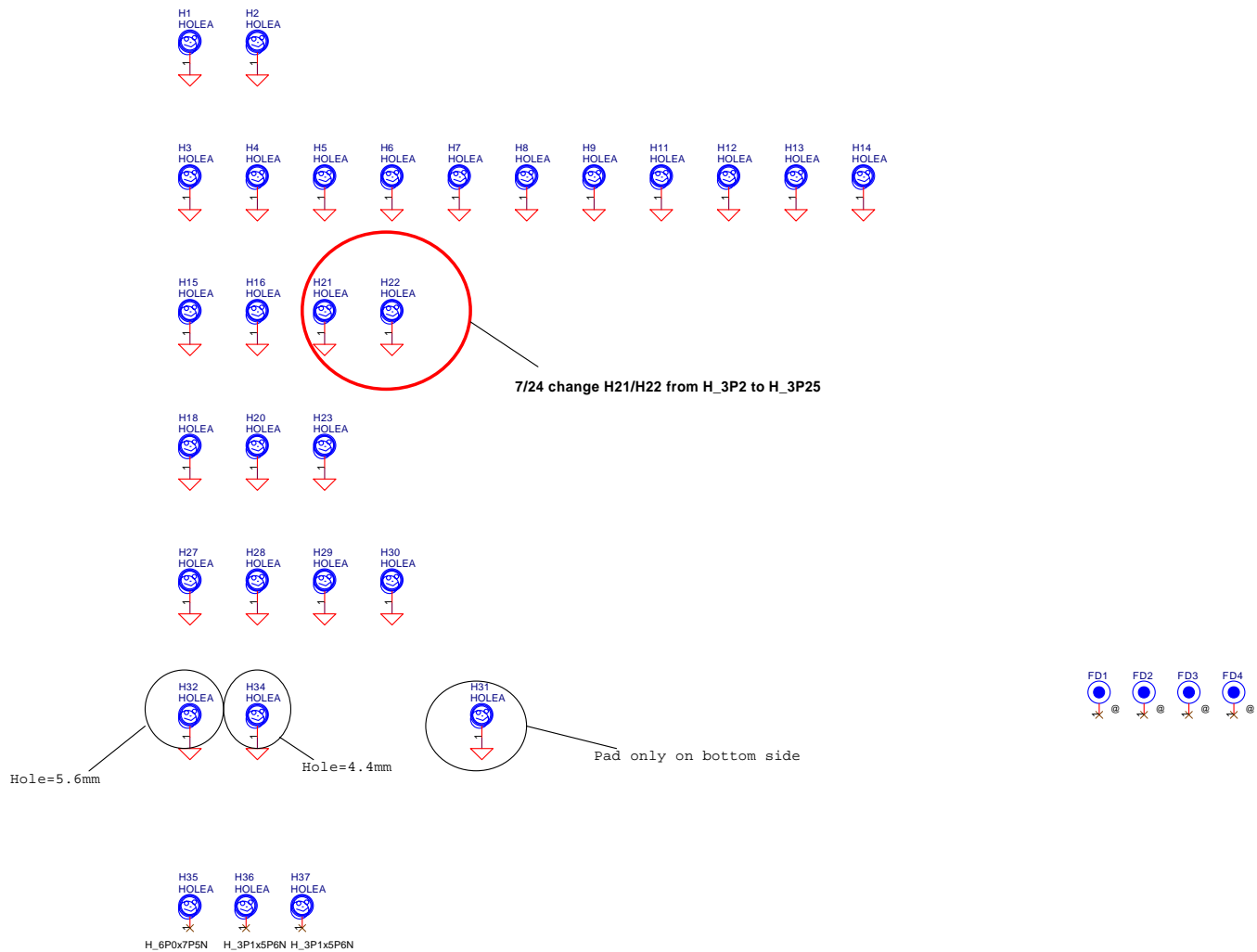
+5VALW assume equal 5.1V
10 dB ---> $5.1 \times 220 / 320 = 3.5$



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LED



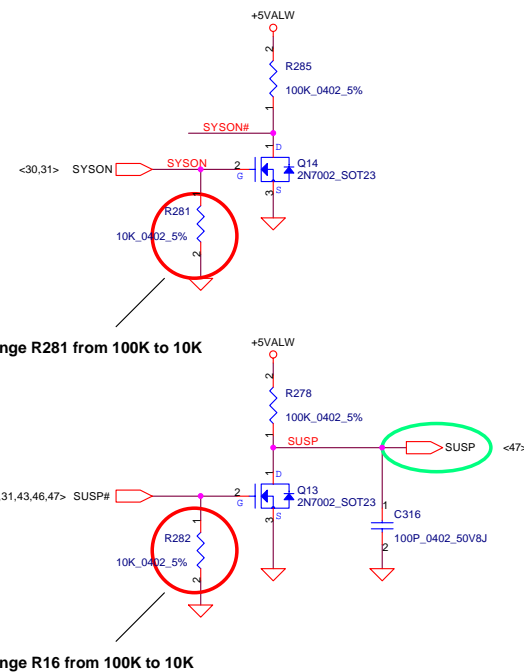
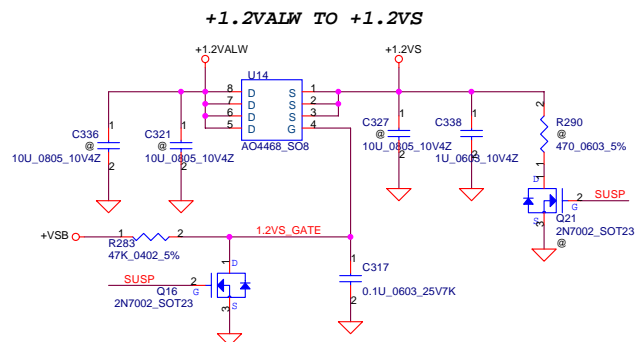
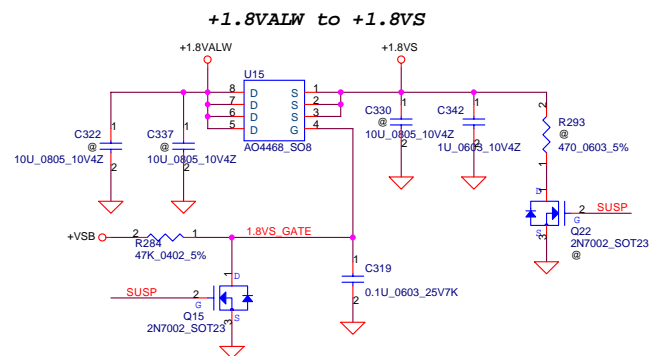


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								Size	Document Number						Rev
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High	18.764	17.901	17.063
Low	17.745	16.9	16.03

	Precharge detector		
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

	Precharge detector		
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

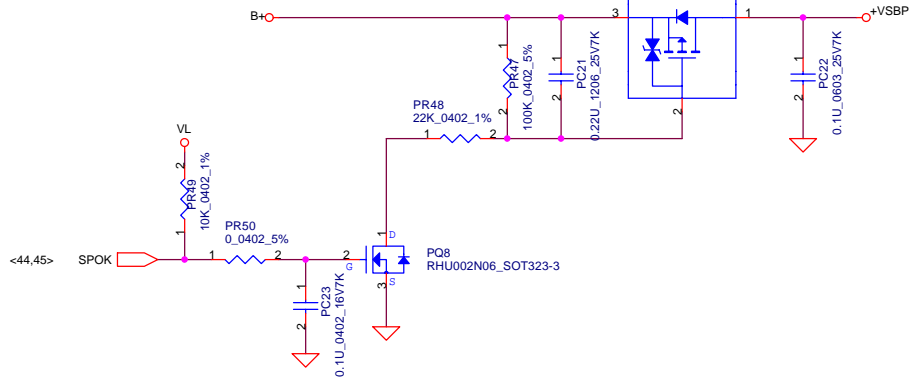
The diagrams show the following components and their connections:

- RTCTREF**: A reference point for the RTCT component.
- G920AT24U_SOT89-3**: A component with pins 1, 2, and 3. Pin 1 is connected to GND, pin 2 to IN, and pin 3 to OUT.
- PR23**: A resistor with value 560_0603_5%.
- PR24**: A resistor with value 560_0603_5%.
- PR25**: A resistor with value 200_0805_5%.
- CHGRCTCP**: A connection point for the CHGRCT component.
- CHGRCTC**: A connection point for the CHGRCT component.
- PU2**: A component with pins 1, 2, and 3. Pin 1 is connected to GND, pin 2 to IN, and pin 3 to OUT.
- PC9**: A capacitor with value 4.7U_0805_6.3V8K.
- PC8**: A capacitor with value 1U_0805_25V4Z.
- PR29**: A resistor with value 22K_04.
- 51_ON#**: A connection point for the 51_ON component.
- PJ15**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +1.5VSP and pin 2 to +1.5VS.
- PJ16**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +1.8VALWP and pin 2 to +1.8VALW.
- PJ18**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +5VALWP and pin 2 to +5VALW.
- PJ19**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +0.9VSP and pin 2 to +0.9VS.
- PJ20**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +3VALWP and pin 2 to +3VALW.
- PJ17**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +1.05VSP and pin 2 to +1.05VS.
- PJ21**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +1.2VALWP and pin 2 to +1.2VALW.
- PJ22**: A PAD-OPEN 3x3mm component with pins 1 and 2. Pin 1 is connected to +VSBP and pin 2 to +VSB.

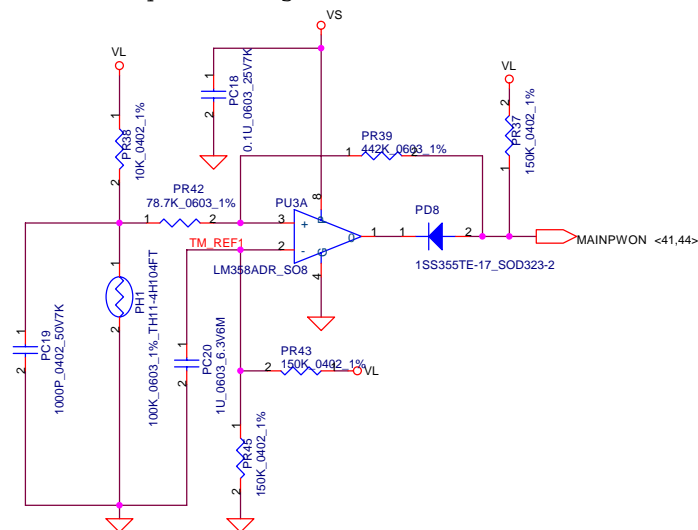
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PJP2

SUYIN



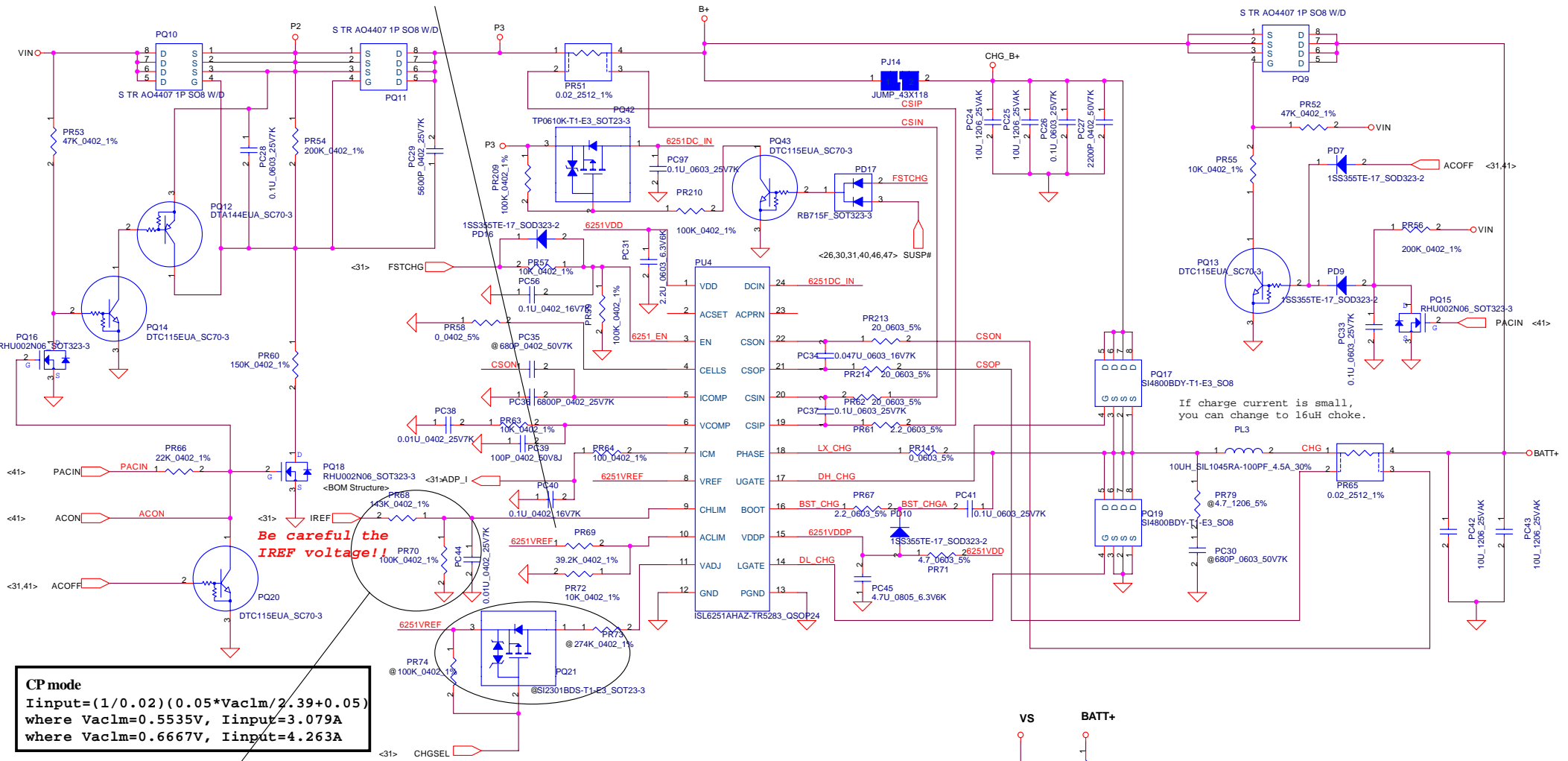
PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR74=39.2K, CP=3.079A

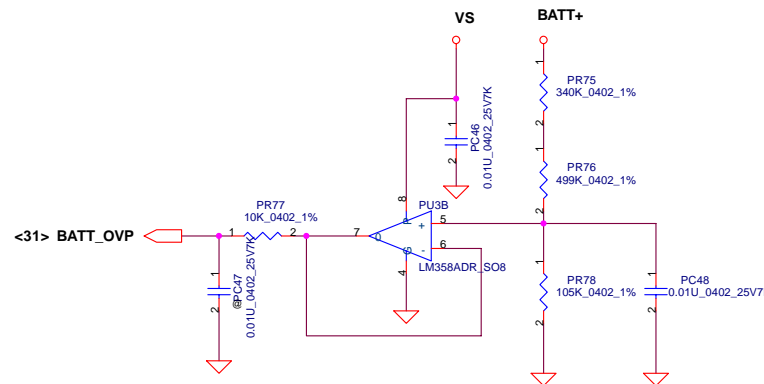
ADP_I = 19.9*Iadapter*Rsense



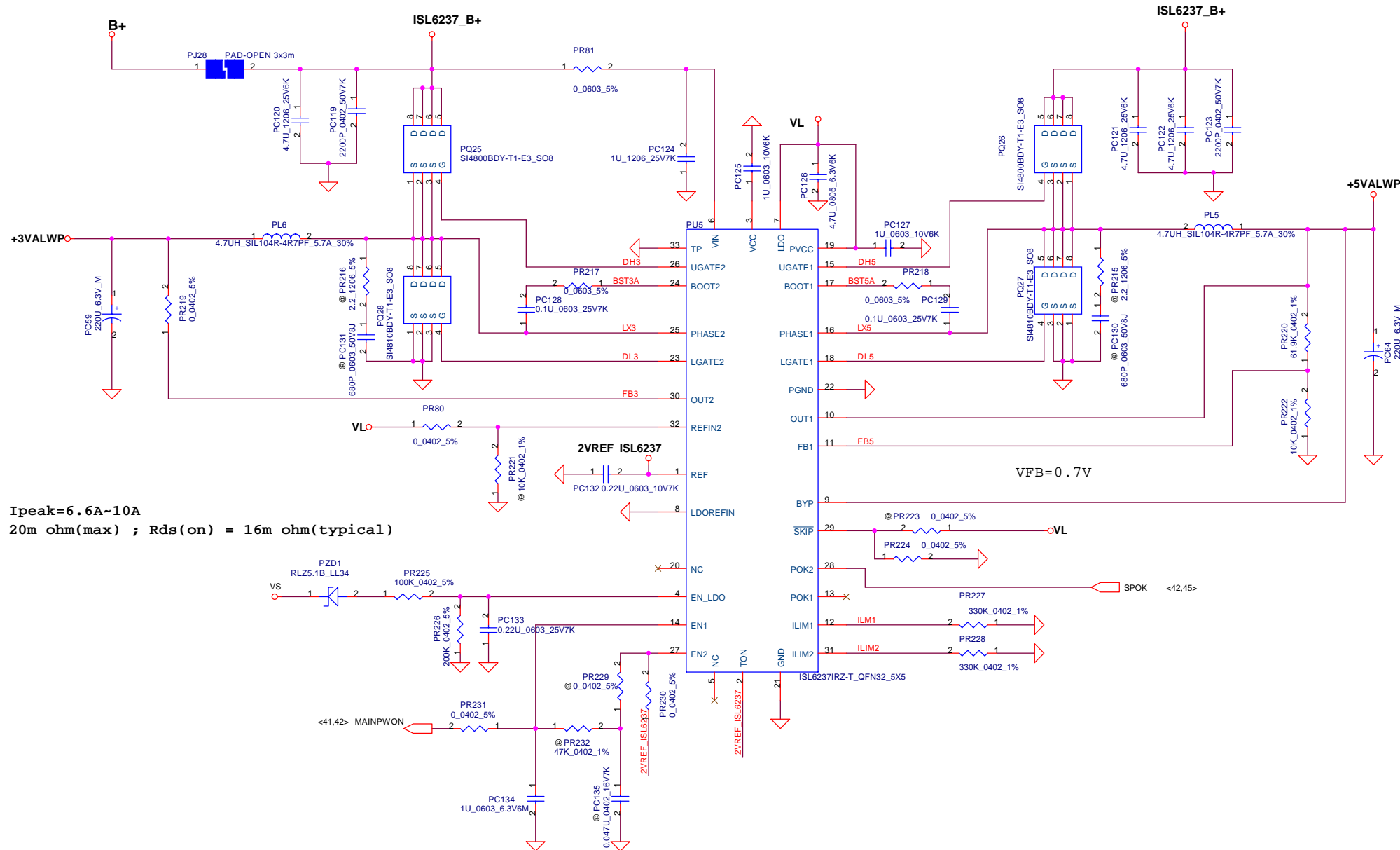
CP mode
 $I_{input} = (1/0.02)(0.05 \cdot V_{ac1m}/2.39 + 0.05)$
 where $V_{ac1m} = 0.5535V$, $I_{input} = 3.079A$
 where $V_{ac1m} = 0.6667V$, $I_{input} = 4.263A$

CC=0.6~3.4A
 $V_{CHLM} = 0.24V \sim 1.36V$
 $I_{REF} = 0.972 \cdot I_{charge}$
 $I_{REF} = 0.5832V \sim 3.3V$

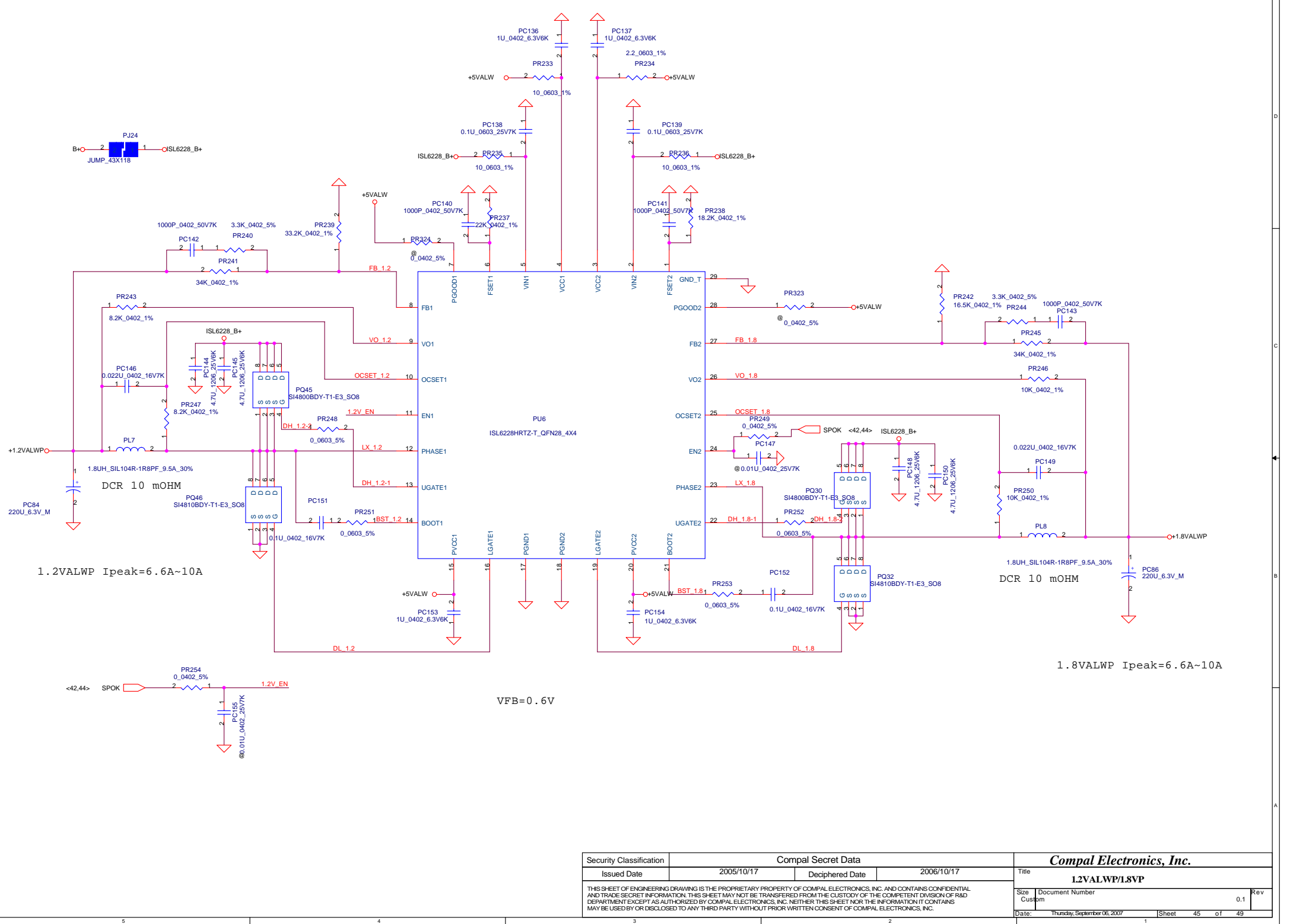
BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V



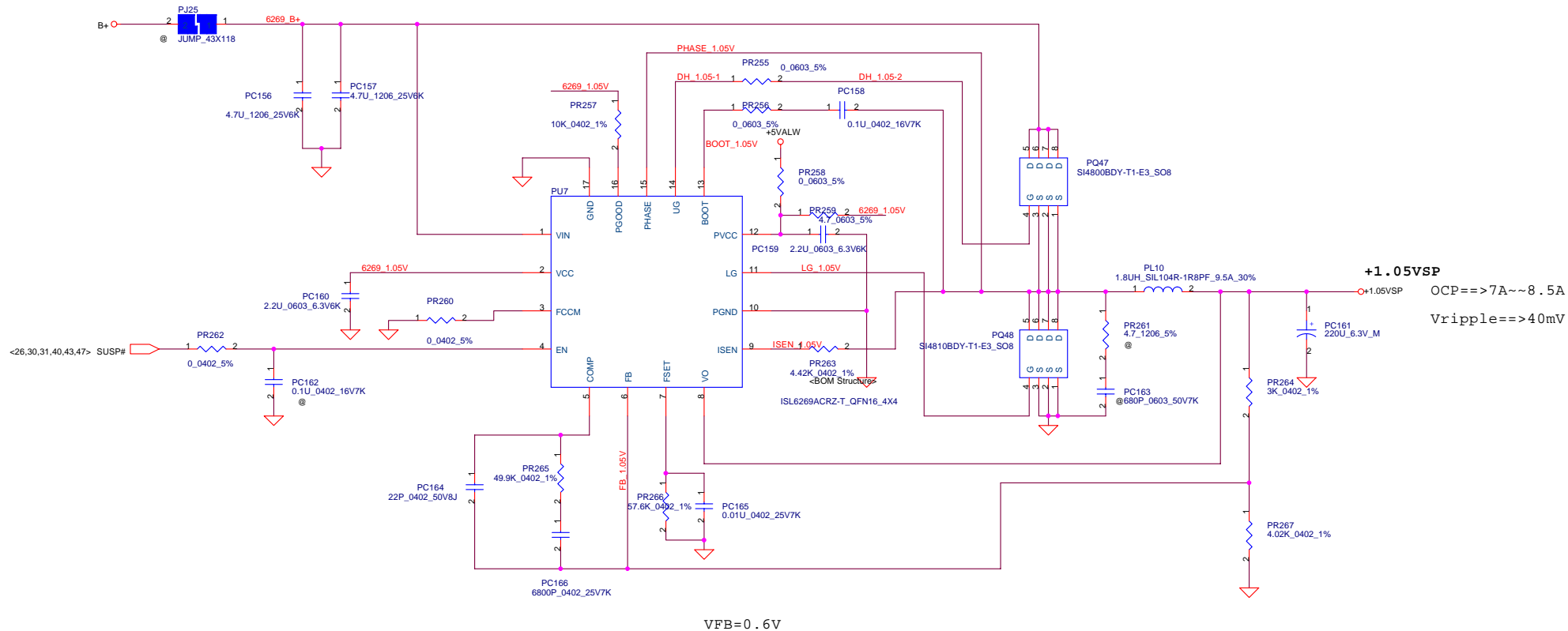
OVP voltage :
 $LI-3S : 13.50V \sim BATT-OVP = 1.5V$
 $BATT-OVP = 0.111 \cdot BATT+$



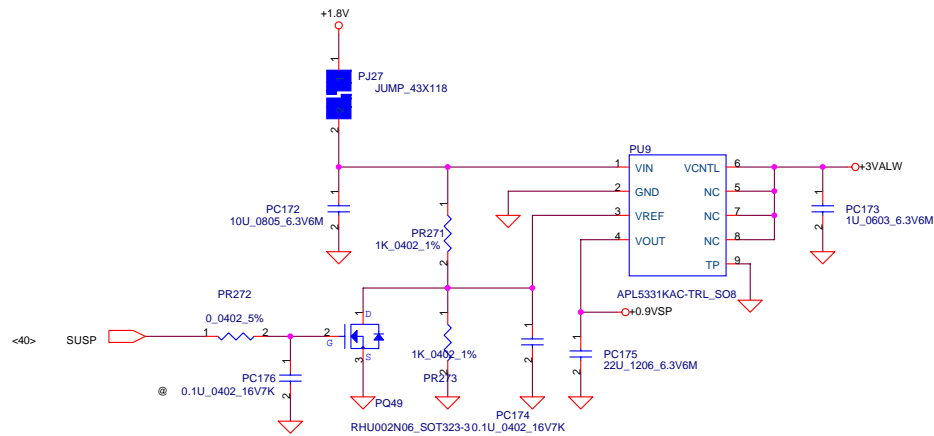
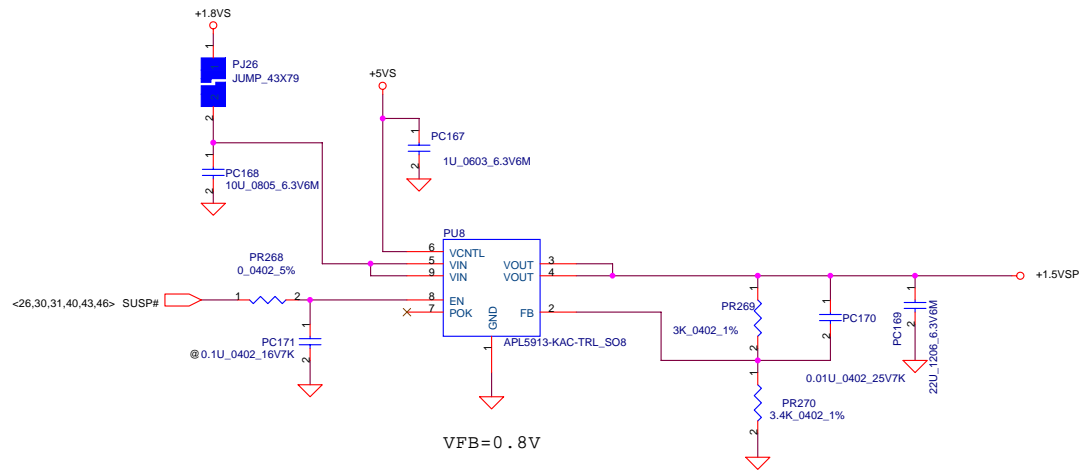
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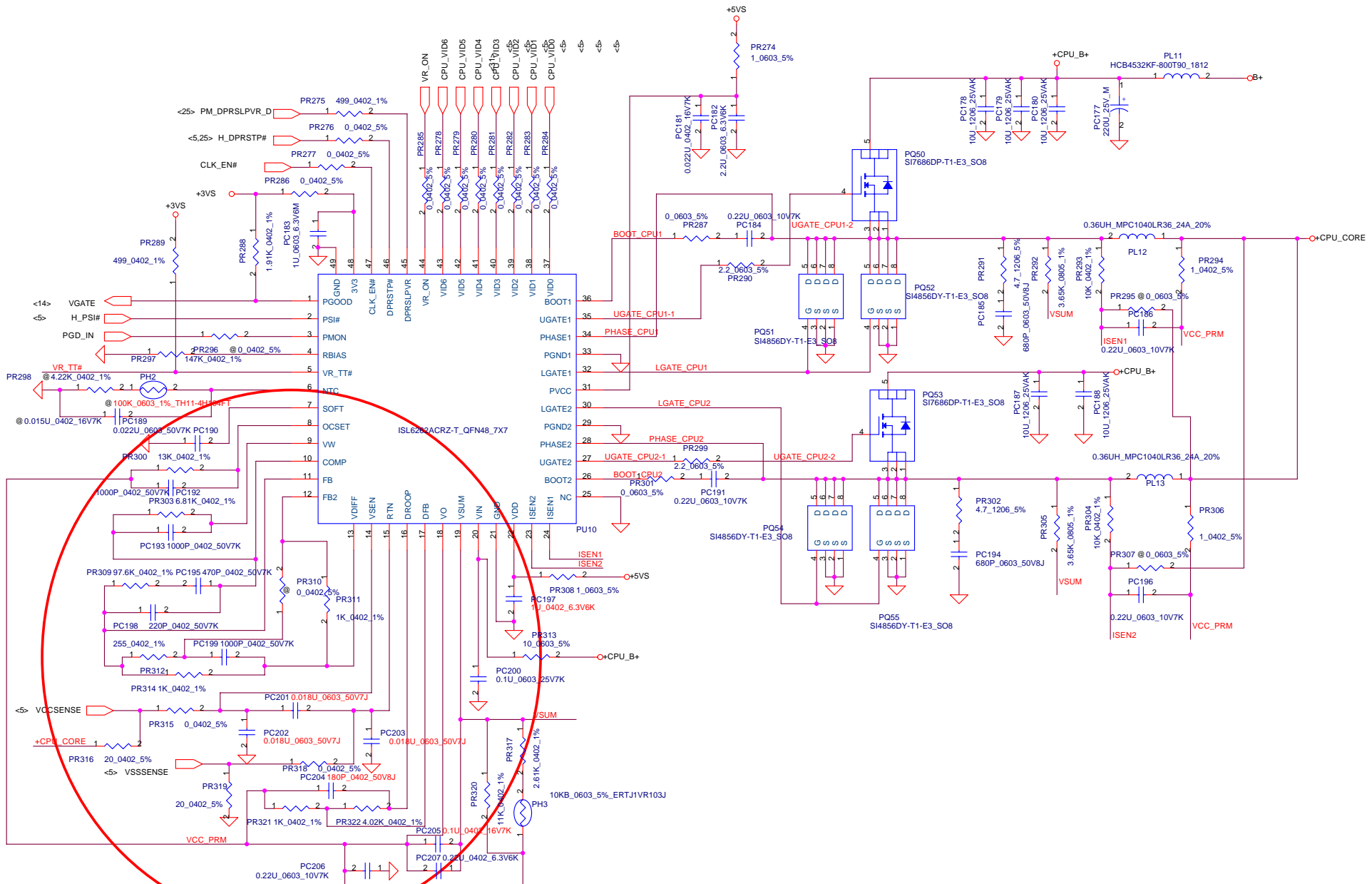
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		Size Custom					Rev 0.1
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