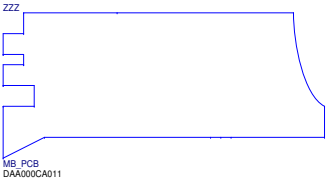


MODEL NAME : CAZ00
PCB NO : LA-D841P
BOM P/N : DAA000CA010

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Schematic Document

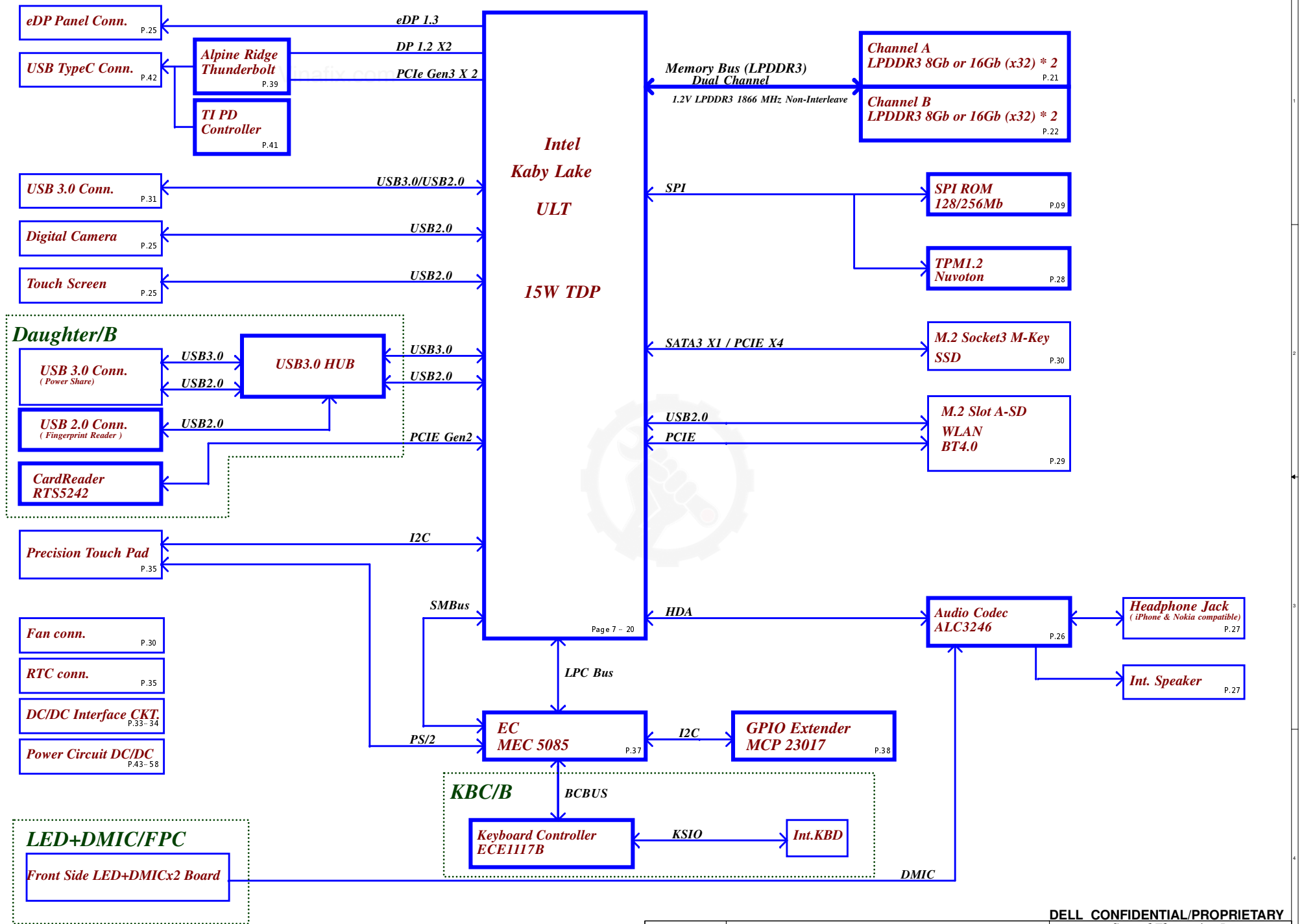
Dino2 MLK (Kaby Lake ULT)

2016-06-21

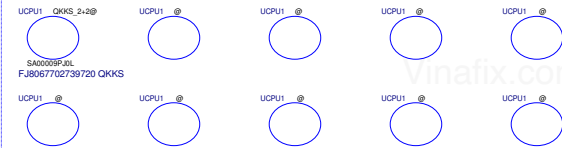
Rev: 1.0 (A00)

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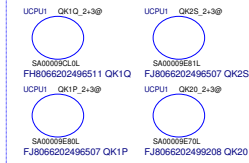
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Issued Date				2016/12/16				Compal Electronics, Inc.			
Deciphered Date				2016/12/13				Title			
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Date: Wednesday, August 31, 2016				Document Number				LA-D841P			
Sheet				1				Rev			
of				60				1.0			



2+2 CPU Option



2+3 CPU Option



AR Option



DRAM Option

DRAM Config Option

	UD19 MAG 1866@	UD20 MAG 1866@	UD21 MAG 1866@	UD22 MAG 1866@	MEM_CONFIG0 RH144 MAG 1866@	MEM_CONFIG1 RH139 MAG 1866@	MEM_CONFIG2 RH145 MAG 1866@	MEM_CONFIG3 RH151 MAG 1866@	MEM_CONFIG4 RH147 MAG 1866@
Micron 4G/1866	 SA00008PF1L EDF8132A3MA-JD-F-R A311	 SA00008PF1L EDF8132A3MA-JD-F-R A311	 SA00008PF1L EDF8132A3MA-JD-F-R A311	 SA00008PF1L EDF8132A3MA-JD-F-R A311	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%
Micron 8G/1866	 SA00008Q11L EDFA232A2MA-JD-F-R A311	 SA00008Q11L EDFA232A2MA-JD-F-R A311	 SA00008Q11L EDFA232A2MA-JD-F-R A311	 SA00008Q11L EDFA232A2MA-JD-F-R A311	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%	 SD028100280 10K_0402_5%
Hynix 4G/1866	 SA00008G61L H9CCNN8GTMLAR-NUD	 SA00008G61L H9CCNN8GTMLAR-NUD	 SA00008G61L H9CCNN8GTMLAR-NUD	 SA00008G61L H9CCNN8GTMLAR-NUD A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Hynix 8G/1866	 SA00008FJ1L H9CCNN8GTMLAR-NUD	 SA00008FJ1L H9CCNN8GTMLAR-NUD	 SA00008FJ1L H9CCNN8GTMLAR-NUD	 SA00008FJ1L H9CCNN8GTMLAR-NUD A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Samsung 4G/1866	 SA00008PO1L K4EBE304EE-EGCF A311	 SA00008PO1L K4EBE304EE-EGCF A311	 SA00008PO1L K4EBE304EE-EGCF A311	 SA00008PO1L K4EBE304EE-EGCF A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Samsung 8G/1866	 SA00008QV1L K4EBE304EE-EGCF A311	 SA00008QV1L K4EBE304EE-EGCF A311	 SA00008QV1L K4EBE304EE-EGCF A311	 SA00008QV1L K4EBE304EE-EGCF A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Micron 16G/1866	 SA00008QW1L EDFB232A1MA-JD-F-R A311	 SA00008QW1L EDFB232A1MA-JD-F-R A311	 SA00008QW1L EDFB232A1MA-JD-F-R A311	 SA00008QW1L EDFB232A1MA-JD-F-R A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Samsung 16G/2133	 SA00008VV1L K4EBE304EB-EGCG A311	 SA00008VV1L K4EBE304EB-EGCG A311	 SA00008VV1L K4EBE304EB-EGCG A311	 SA00008VV1L K4EBE304EB-EGCG A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Samsung 16G/1866	 SA00008X11L K4EBE304EB-EGCF A311	 SA00008X11L K4EBE304EB-EGCF A311	 SA00008X11L K4EBE304EB-EGCF A311	 SA00008X11L K4EBE304EB-EGCF A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D
Hynix 16G/1866	 SA00008YT1L H9CCNN8GTMLAR-NUD	 SA00008YT1L H9CCNN8GTMLAR-NUD	 SA00008YT1L H9CCNN8GTMLAR-NUD	 SA00008YT1L H9CCNN8GTMLAR-NUD A311	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D	 SD028100280 10K_0402_5%-D

Board ID Table for AD channel

RE79	CE54	REV
240K	4700p	TBD
130K	4700p	TBD
62K	4700p	A00
33K	4700p	X02
8.2K	4700p	X01
4.3K	4700p	X00
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%

	SKU	PTT	TPM2.0
Dino2 MLK	Vpro+CS	Disable	Enable
	nVpro+CS	Enable	None

SMBUS Control Table

	SOURCE	23017	BATTERY	Charger	PD	5085	XDP	Audio	Touch Pad
I2C1A_CLK I2C1A_DATA	MEC5085	V							
I2C1C_CLK I2C1C_DATA	MEC5085		V						
I2C1G_CLK I2C1G_DATA	MEC5085			V					
I2C2A_CLK I2C2A_DATA	MEC5085				V				
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH					V			
SMBCLK SMBDATA	PCH						V		
I2C0_CLK I2C0_DATA	PCH								
I2C1_CLK I2C1_DATA	PCH								V

PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	External USB3(On IOB)
	2	External USB3(On MB)
	3	NGFF CARD WLAN
	4	Touch Panel
	5	Camera
	6	
	7	
PCH USB 3.0 Port Mapping	1	External USB3(On IOB)
	2	External USB3(On MB)

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 1	Alpine Ridge
	CLKOUT_PCIE1	NGFF CARD WLAN	Lane 2	Alpine Ridge
	CLKOUT_PCIE2		Lane 3	
	CLKOUT_PCIE3	M.2 SSD / PCIe	Lane 4	
	CLKOUT_PCIE4		Lane 5	NGFF CARD WLAN
	CLKOUT_PCIE5	Card Reader	Lane 6	Card Reader
	FLEX CLK#	DESTINATION	Lane 7	
	CLKOUT_LPC_0	EC LPC	Lane 8	
	CLKOUT_LPC_1	Debug	Lane 9	M.2 SSD
			Lane 10	M.2 SSD
			Lane 11	M.2 SSD
			Lane 12 / SATA 2	M.2 SSD

SATA PORT#	DESTINATION
SATA-0	
SATA-1A	
SATA-1B	
SATA-2	M.2 SSD

Symbol Note :

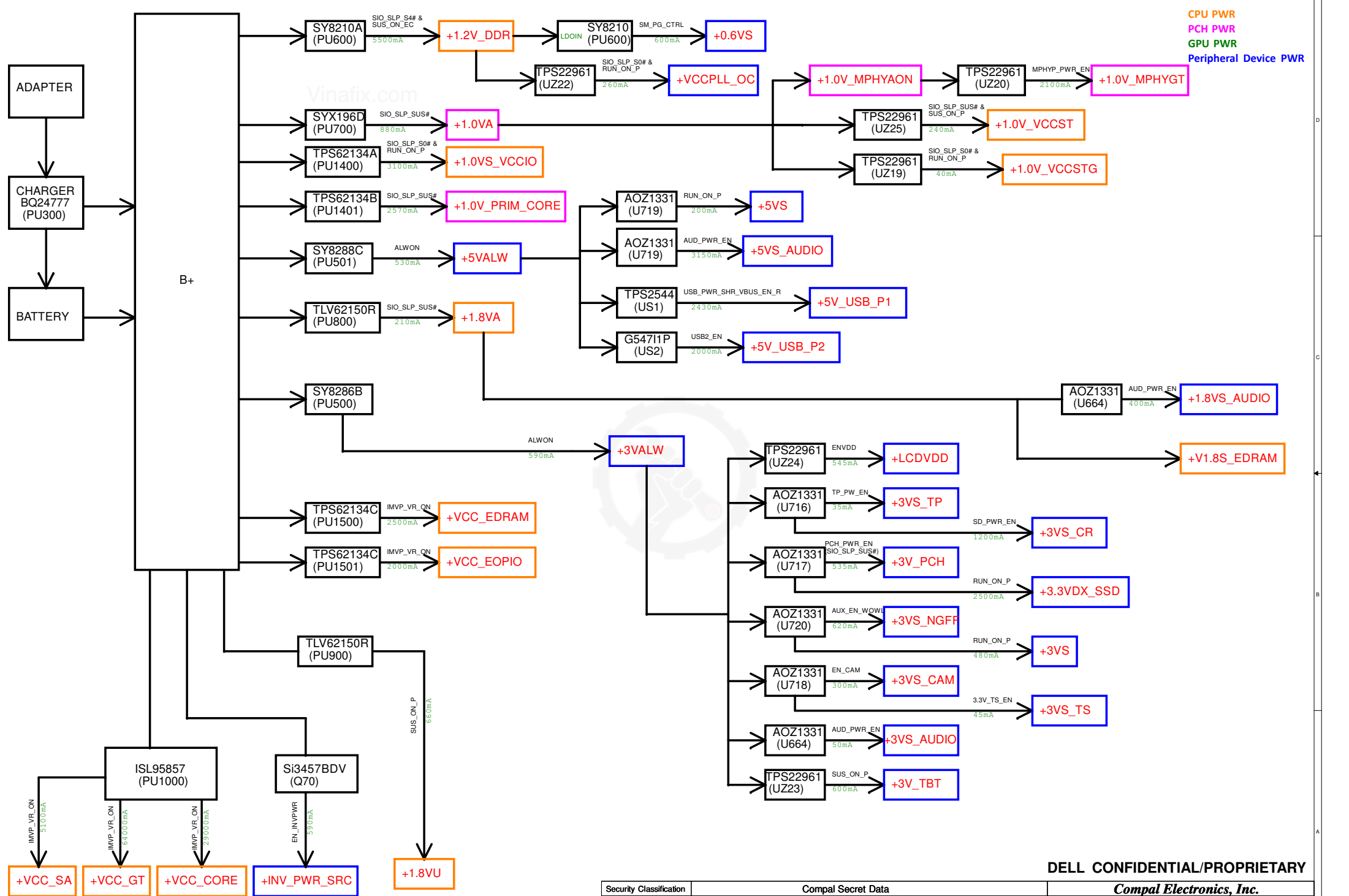


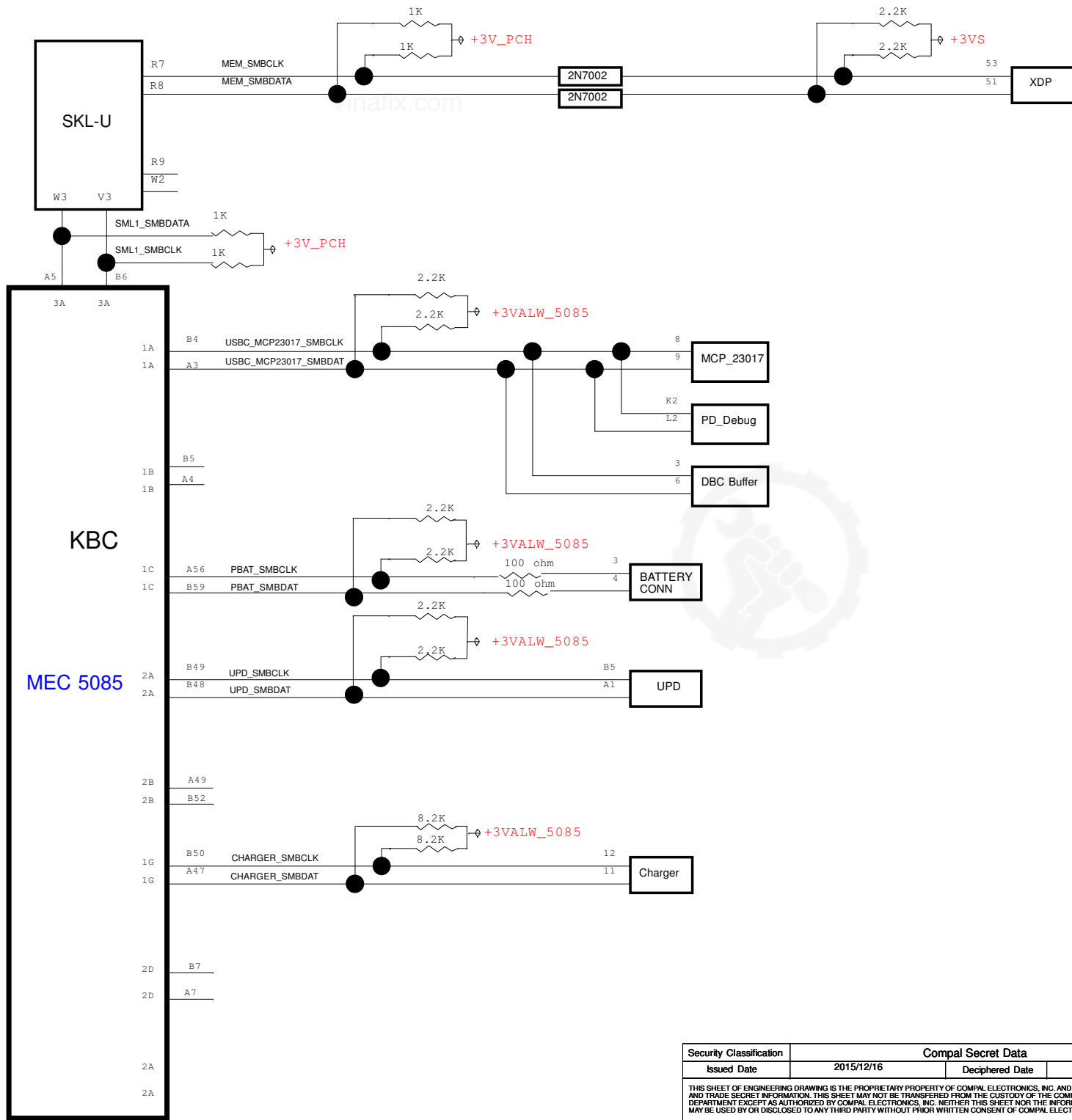
: means Digital Ground

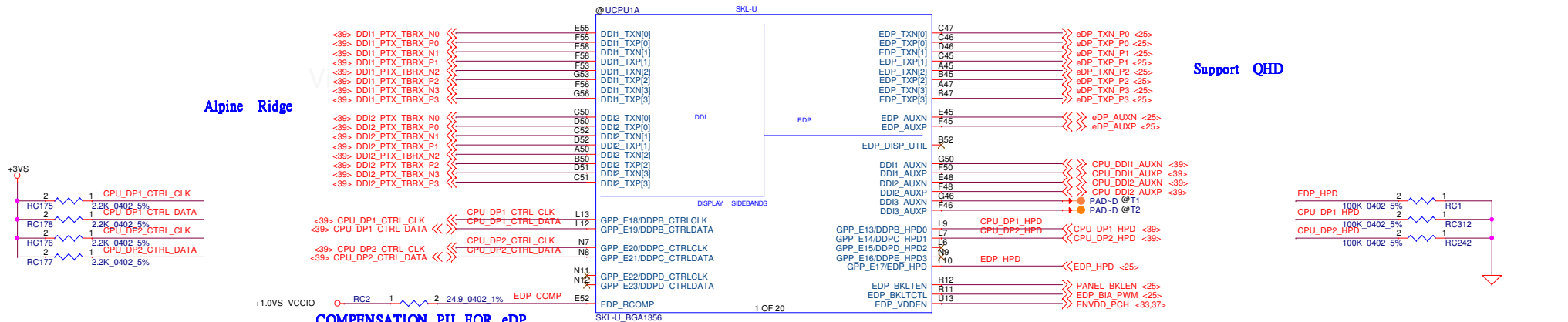


: means Analog Ground

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							P04-Notes List
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							Rev 1.0
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							Sheet 4 of 60



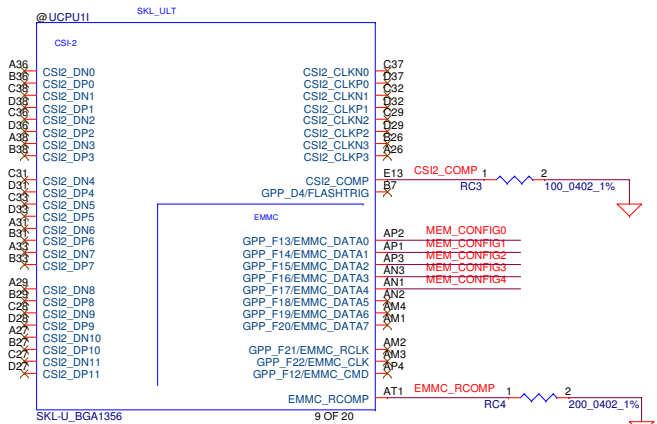




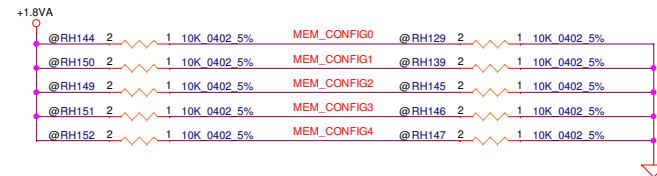
COMPENSATION PU FOR eDP

CAD Note: Trace width=20 mils, Isolation Spacing=25mil,
Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



DDR Memory Configuration Type Strap pi



GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1	0	0	1	1	0	0	1	1	0
GPP_D7	MEM_CONFIG2	0	0	0	0	1	1	0	0	0
GPP_D8	MEM_CONFIG3	0	0	0	0	0	0	0	0	1
GPP_D9	MEM_CONFIG4	0	0	0	0	0	0	0	0	0

GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	1	0	1	0	1	0	1	0	1
GPP_D6	MEM_CONFIG1	0	1	1	0	0	1	1	0	0
GPP_D7	MEM_CONFIG2	0	0	0	1	1	1	1	0	0
GPP_D8	MEM_CONFIG3	1	1	1	1	1	1	1	0	0
GPP_D9	MEM_CONFIG4	0	0	0	0	0	0	0	1	1

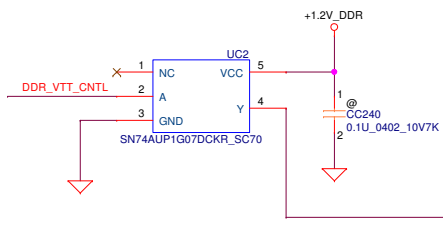
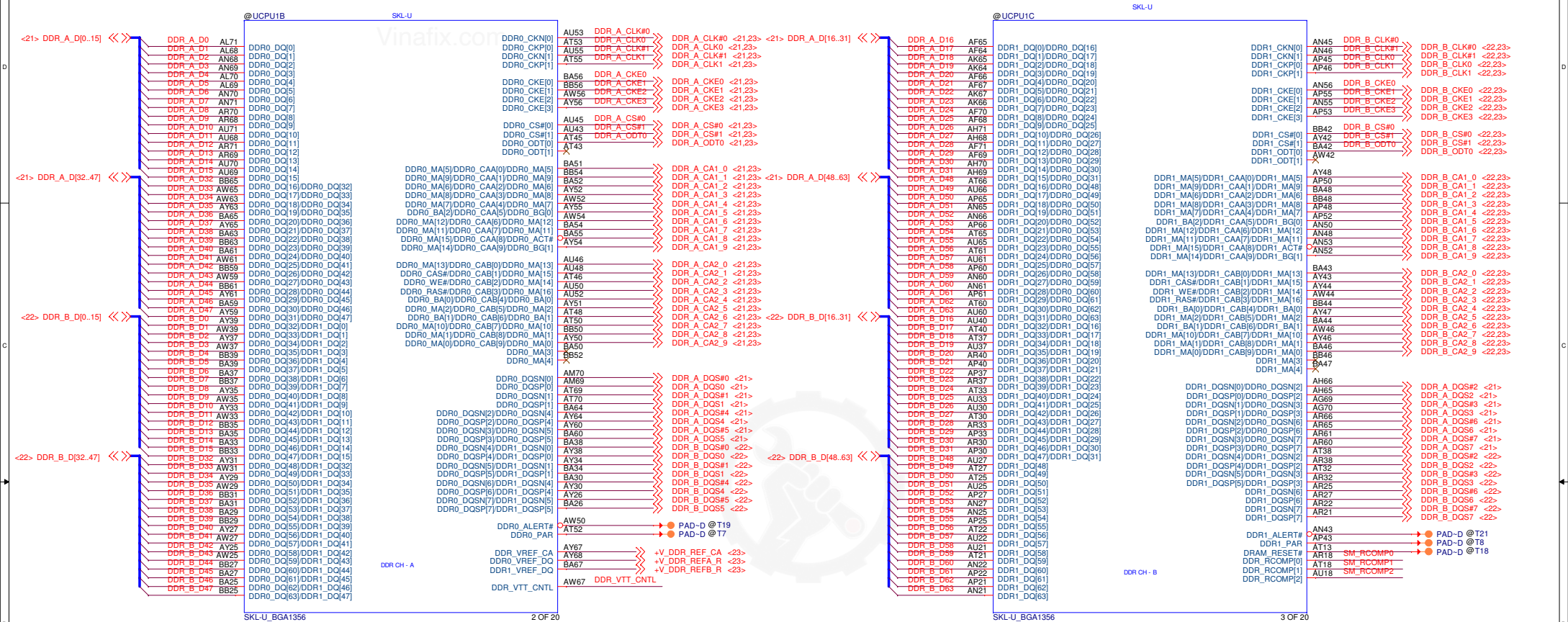
GPIO Pin	Pin Name	Micron 4G	Micron 8G	Micron 16G	Hynix 4G	Hynix 8G	Hynix 16G	Samsung 4G	Samsung 8G	Samsung 16G
GPP_D5	MEM_CONFIG0	0	1	0	1	0	1	0	1	0
GPP_D6	MEM_CONFIG1	1	1	0	0	1	1	0	0	1
GPP_D7	MEM_CONFIG2	0	0	1	1	1	1	0	0	0
GPP_D8	MEM_CONFIG3	0	0	0	0	0	0	1	1	1
GPP_D9	MEM_CONFIG4	1	1	1	1	1	1	1	1	1

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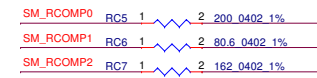
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LPDDR3, Ballout for side by side(Non-Interleave)



LPDDR3 COMPENSATION SIGNALS



CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

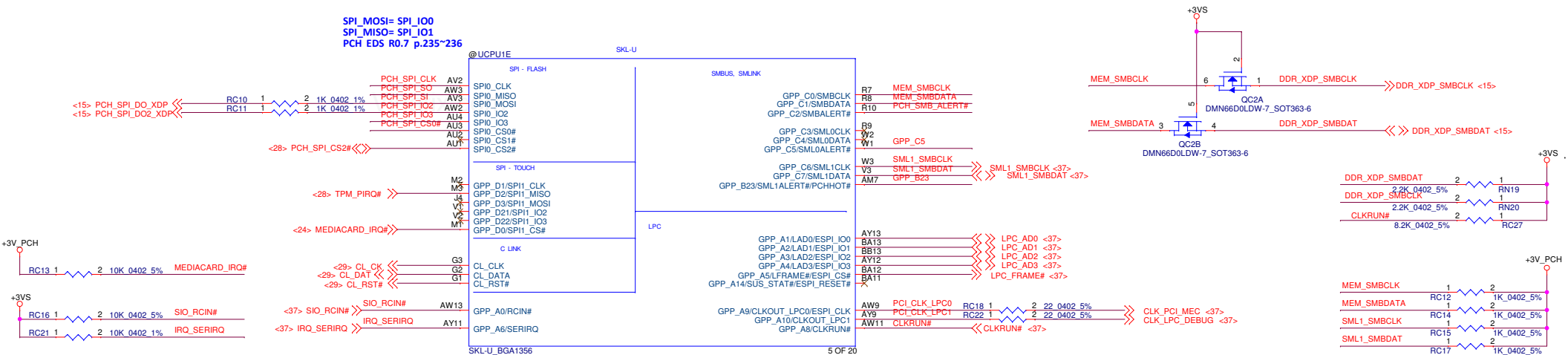
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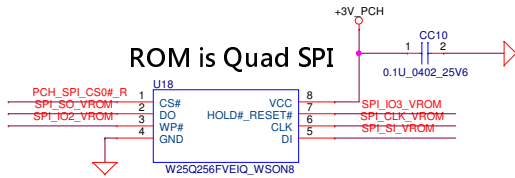
Compal Electronics, Inc.

Title			
P08-MCP(2/14)LPDDR3			
Size	Document Number		Rev
	LA-D841P		1.0
Date:	Wednesday, August 31, 2016	Sheet	8 of 60

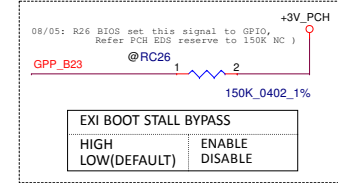
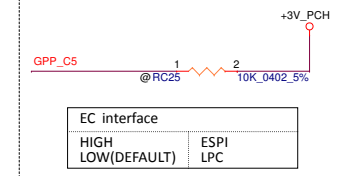
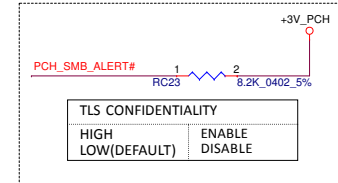
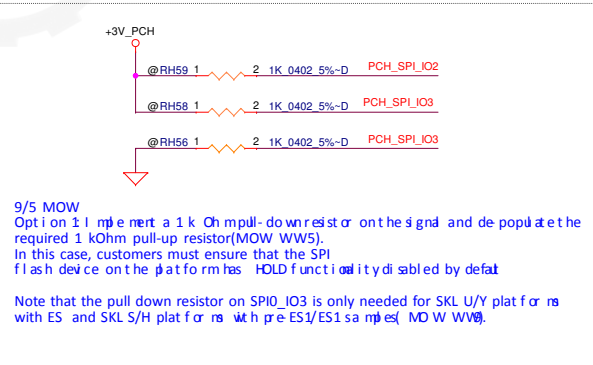
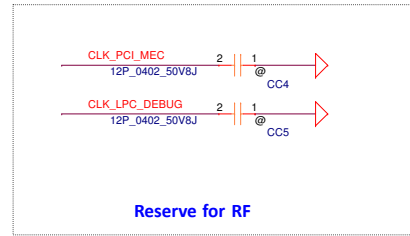
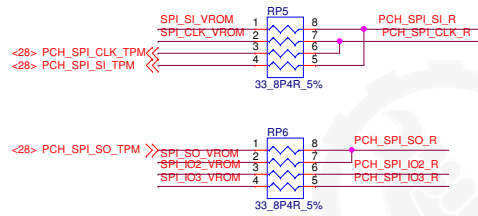
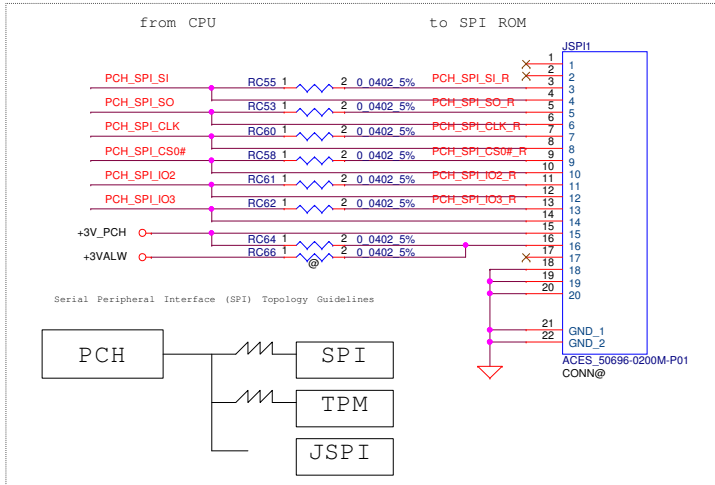
SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

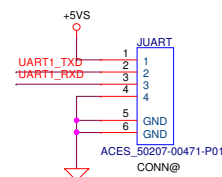
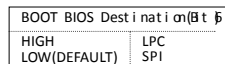


ROM is Quad SPI



SPI ROM FOR ME (32 MByte)





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				Document Number LA-D84IP
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Alpine Ridge
PCIe Gen3 x 2

<39> PCIE_PRX_TBXTX_N1
<29> PCIE_PRX_TBXTX_P1
<39> PCIE_PTX_TBRTX_N1
<39> PCIE_PTX_TBRTX_P1

<39> PCIE_PRX_TBXTX_N2
<39> PCIE_PRX_TBXTX_P2
<39> PCIE_PTX_TBRTX_N2
<39> PCIE_PTX_TBRTX_P2

WLAN
PCIe Gen2 x 1

<29> PCIE_PRX_WLANTX_N5
<29> PCIE_PRX_WLANTX_P5
<29> PCIE_PTX_WLANRX_N5
<29> PCIE_PTX_WLANRX_P5

Cardreader
PCIe Gen2 x 1

<24> PCIE_PRX_CARDTX_N6
<24> PCIE_PRX_CARDTX_P6
<24> PCIE_PTX_CARDRX_N6
<24> PCIE_PTX_CARDRX_P6

M.2 SSD
PCIe Gen3 x 4

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<30> PCIE_PRX_SSDTX_P9
<30> PCIE_PTX_SSDRX_N9
<30> PCIE_PTX_SSDRX_P9

<30> PCIE_PRX_SSDTX_N10
<30> PCIE_PRX_SSDTX_P10
<30> PCIE_PTX_SSDRX_N10
<30> PCIE_PTX_SSDRX_P10

SATA SSD

<30> PCIE_PRX_SSDTX_N11
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<30> SATA_PTX_SSDRX_N2
<30> SATA_PTX_SSDRX_P2

@UCPU1H

SKL-U

PCIe/USB3/SATA

SSIC / USB3

H13 PCIE1_RXN/USB3_5_RXN
G13 PCIE1_RXP/USB3_5_RXP
B17 PCIE1_TXN/USB3_5_TXN
A17 PCIE1_TXP/USB3_5_TXP

G11 PCIE2_RXN/USB3_6_RXN
E11 PCIE2_RXP/USB3_6_RXP
D19 PCIE2_TXN/USB3_6_TXN
C16 PCIE2_TXP/USB3_6_TXP

C18 PCIE3_RXN
D17 PCIE3_RXP
C17 PCIE3_TXN
C17 PCIE3_TXP

G15 PCIE4_RXN
B19 PCIE4_RXP
A19 PCIE4_TXN
A19 PCIE4_TXP

F16 PCIE5_RXN
E16 PCIE5_RXP
C19 PCIE5_TXN
D19 PCIE5_TXP

G18 PCIE6_RXN
F18 PCIE6_RXP
D20 PCIE6_TXN
C20 PCIE6_TXP

F20 PCIE7_RXN/SATA0_RXN
E20 PCIE7_RXP/SATA0_RXP
B21 PCIE7_TXN/SATA0_TXN
A21 PCIE7_TXP/SATA0_TXP

G21 PCIE8_RXN/SATA1A_RXN
F21 PCIE8_RXP/SATA1A_RXP
D21 PCIE8_TXN/SATA1A_TXN
C21 PCIE8_TXP/SATA1A_TXP

E22 PCIE9_RXN
D22 PCIE9_RXP
A23 PCIE9_TXN
A23 PCIE9_TXP

F25 PCIE10_RXN
E25 PCIE10_RXP
D23 PCIE10_TXN
C23 PCIE10_TXP

F5 PCIE_RCOMP_N
E5 PCIE_RCOMP_P
D56 PROC_PRDY#
D61 PROC_PREQ#
BB11 GPP_A7/PIRQA#

E28 PCIE11_RXN/SATA1B_RXN
E27 PCIE11_RXP/SATA1B_RXP
D24 PCIE11_TXN/SATA1B_TXN
C24 PCIE11_TXP/SATA1B_TXP

E30 PCIE12_RXN/SATA2_RXN
A25 PCIE12_RXP/SATA2_RXP
B25 PCIE12_TXN/SATA2_TXN
B25 PCIE12_TXP/SATA2_TXP

SKL-U_BGA1356

USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP

USB3_2_RXN/SSIC_1_RXN
USB3_2_RXP/SSIC_1_RXP
USB3_2_TXN/SSIC_1_TXN
USB3_2_TXP/SSIC_1_TXP

USB3_3_RXN/SSIC_2_RXN
USB3_3_RXP/SSIC_2_RXP
USB3_3_TXN/SSIC_2_TXN
USB3_3_TXP/SSIC_2_TXP

USB3_4_RXN
USB3_4_RXP
USB3_4_TXN
USB3_4_TXP

USB2N_1
USB2P_1

USB2N_2
USB2P_2

USB2N_3
USB2P_3

USB2N_4
USB2P_4

USB2N_5
USB2P_5

USB2N_6
USB2P_6

USB2N_7
USB2P_7

USB2N_8
USB2P_8

USB2N_9
USB2P_9

USB2N_10
USB2P_10

USB2_COMP
USB2_ID
USB2_VBUSSENSE

GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2

GPP_E0/SATA0PCIE0/SATAGP0
GPP_E1/SATA0PCIE1/SATAGP1
GPP_E2/SATA0PCIE2/SATAGP2

GPP_E8/SATA0PCIE8

8 OF 20

H8
G8
C13
D13

USB3RN1 <24>
USB3RP1 <24>
USB3TN1 <24>
USB3TP1 <24>

USB3.0 IO/B Side

J6
H6
B13
A13

USB3RN2 <31>
USB3RP2 <31>
USB3TN2 <31>
USB3TP2 <31>

USB3.0 M/B Side

J10
H10
B15
A15

E10
C10
D15
A15

AB9
AB10

USB2N_1 <24>
USB2P_1 <24>

USB2.0 IO/B Side

AD6
AD7

USB2N_2 <31>
USB2P_2 <31>

USB2.0 M/B Side

AH3
AJ3

USB2N_3 <29>
USB2P_3 <29>

NGFF (WLAN)

AD9
AD10

USB2N_4 <25>
USB2P_4 <25>

Touch Panel

AJ1
AJ2

USB2N_5 <25>
USB2P_5 <25>

Camera

AF6
AF7
AH1
AH2

AF8
AF9
AG1
AG2

AH7
AH8

AG3
AG4

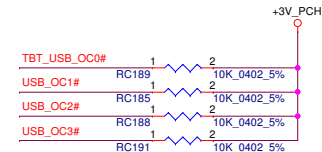
J1
J2
J3
J4
H1

USBCOMP RC44 1 2 113 0402 1%
USB2_ID RC19 1 2 0 0402 1%
VBUSSENSE RC20 1 2 1K 0402 5%

TBT_USB_OC0#
USB_OC1# <41>
USB_OC2# <24>
USB_OC3# <31>

GPP_E1
RC51 1 2 0 0201 5%

SSD_DEVSLP <30>
SSD_IFDET <30>

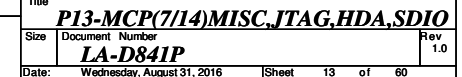


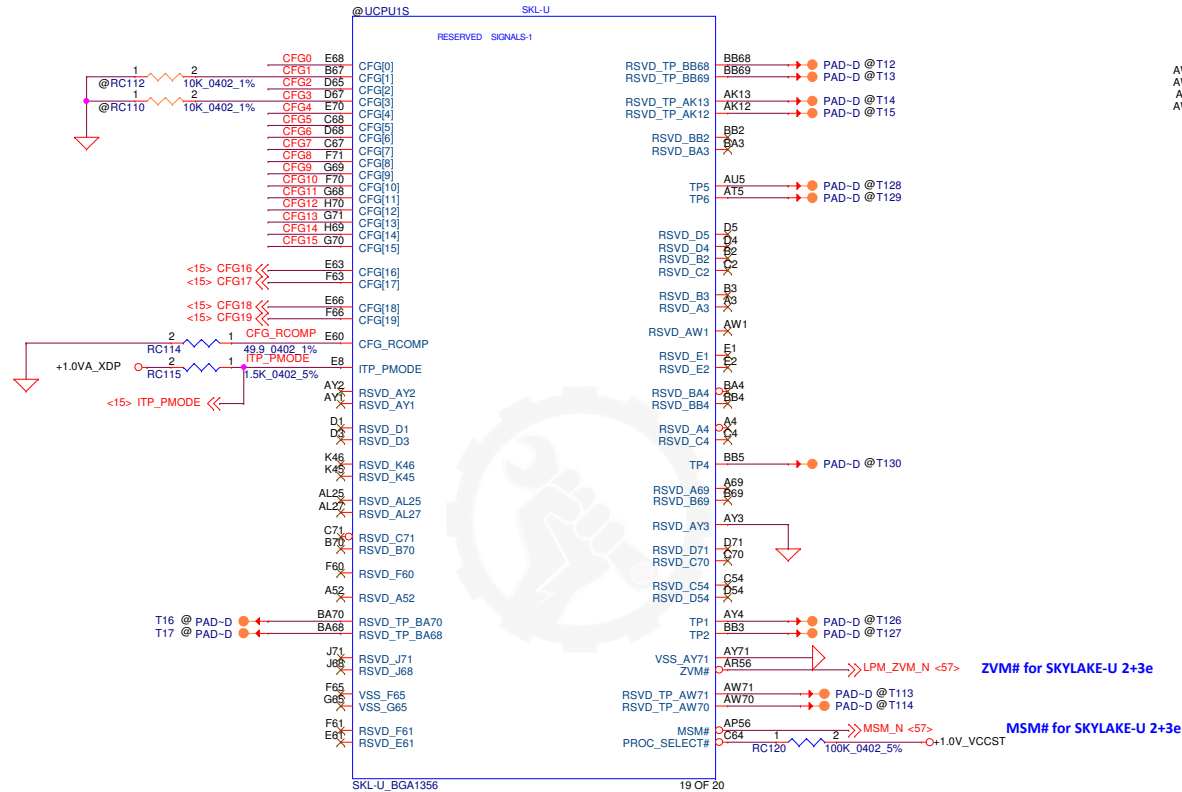
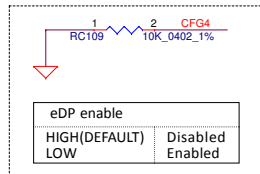
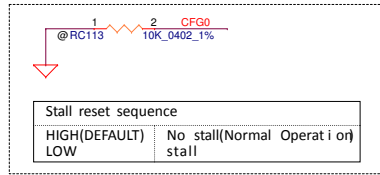
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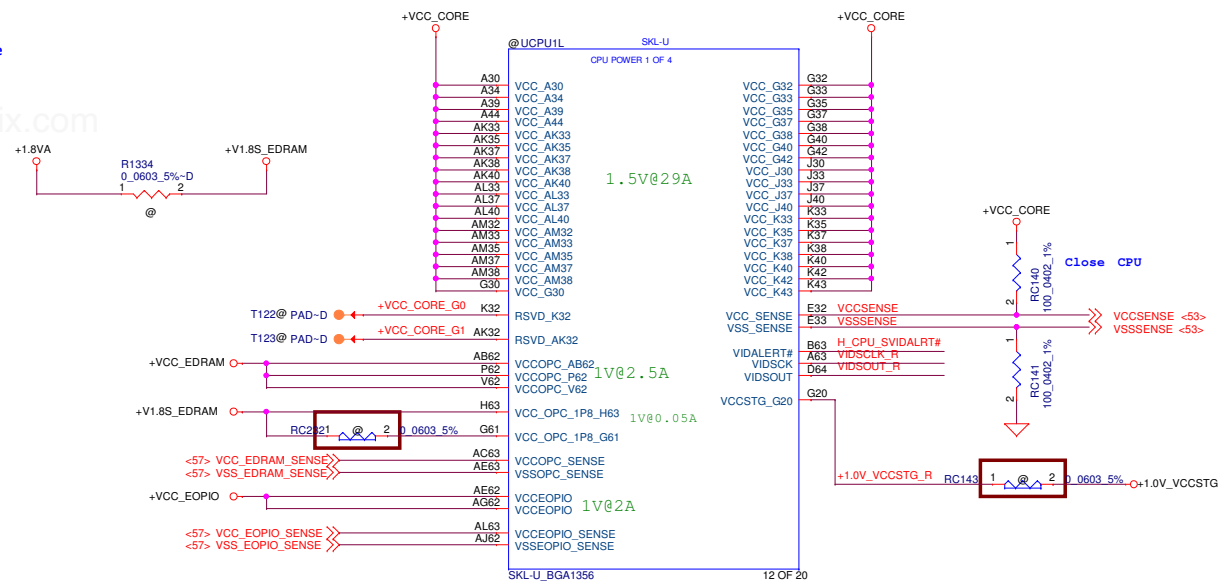
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Size	Document Number	Rev 1.0	
LA-D841P			
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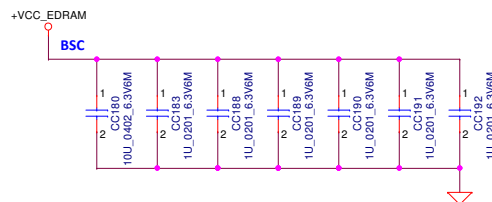


Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

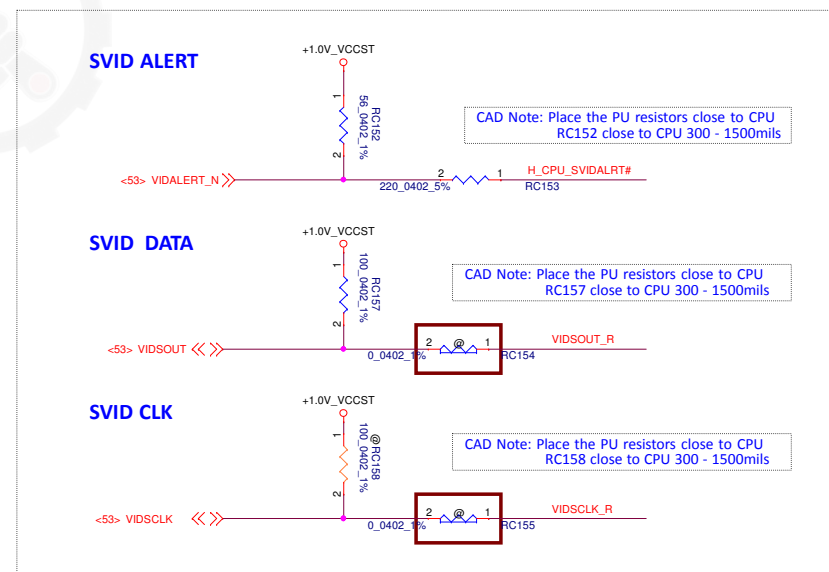
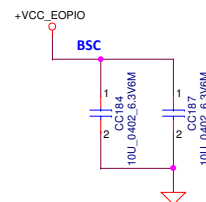
+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A
+V1.8S_EDRAM: 1.8V, 50mA
+VCC_EOPIO: 0.8~1V, 2A



+VCC_EDRAM Decoupling Requirement
Back Side (underneath the package):
10U_0402*1 pcs + 1U_0201*6 pcs



+VCC_EOPIO Decoupling Requirment
Back Side (underneath the package):
10U_0402*2 pcs

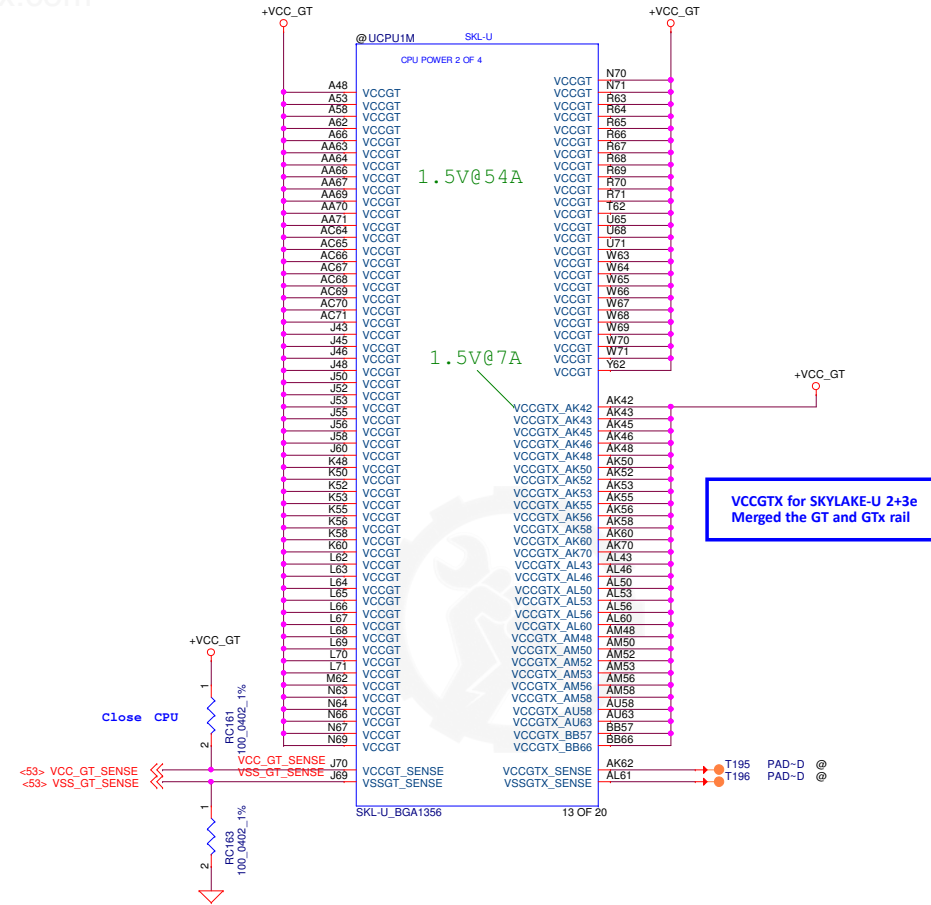


Title	P16-MCP(10/14)PWR-VCC CORE
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+VCCGT: 0.55~1.5V, 54A
+VCCGTx : 0.55~1.5V, 7A



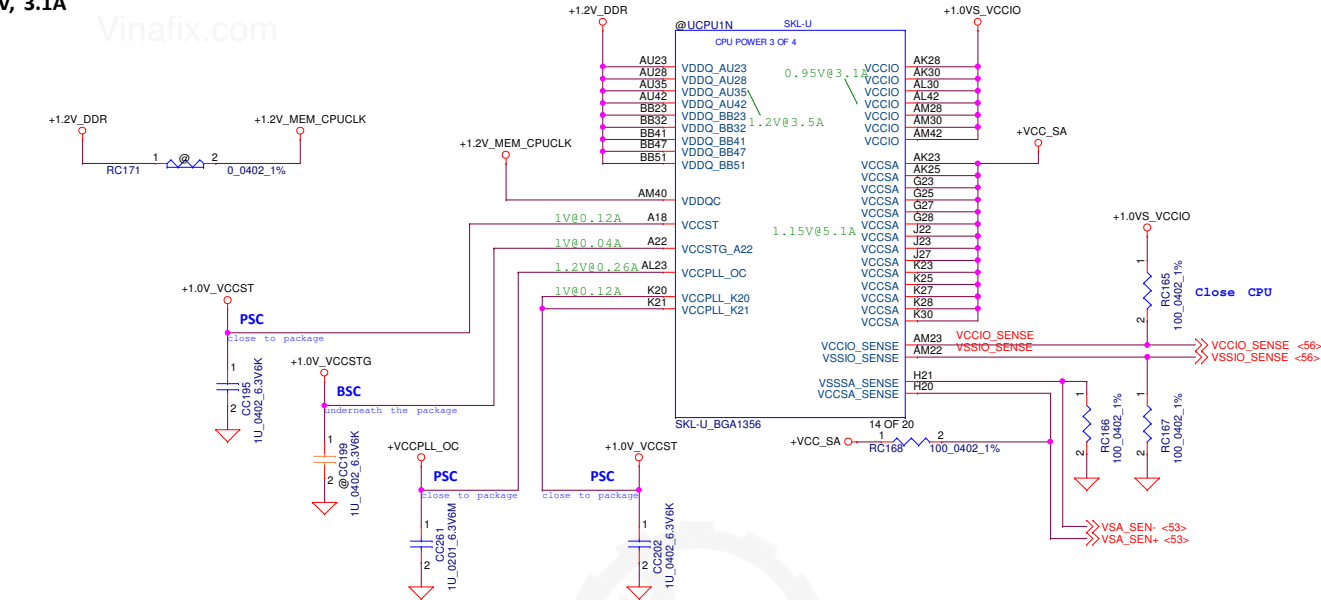
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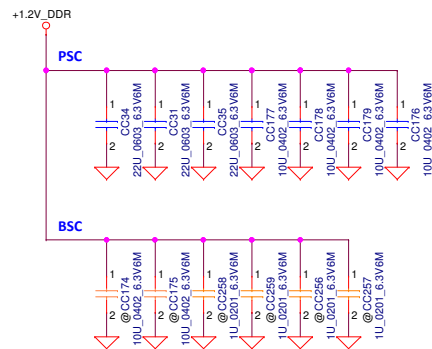
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+1.2V_DDR: 1.2V, 3.5A
 +1.0V_VCCST: 1V, 120mA; VCCPLL: 1V, 120mA
 +1.0V_VCCSTG: 1V, 40mA
 +VCCPLL_OC: 1.2V, 260mA
 +1.0VS_VCCIO: 0.85~0.95V, 3.1A
 +VCC_SA: 1.15V, 5.1A

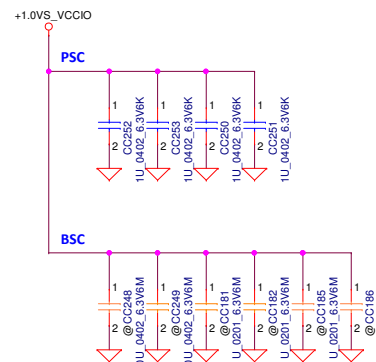
Vinafix.com



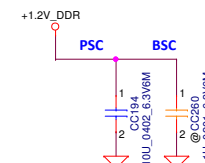
+1.2V_DDR Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (8)
 Primary Side (close to package):
 10U_0402*4 pcs + 22U_0603*3 pcs



+1.0VS_VCCIO Decoupling Requirement
 Back Side (underneath the package):
 10U_0402*2 pcs + 1U_0201*4 pcs (8)
 Primary Side (close to package):
 1U_0402*4 pcs



+1.2V_MEM_CPUCLK (VDDQC) Place on CPU
 Back Side (underneath the package):
 1U_0201*1 pcs (8)
 Primary Side (close to package):
 10U_0402 * 1 pcs



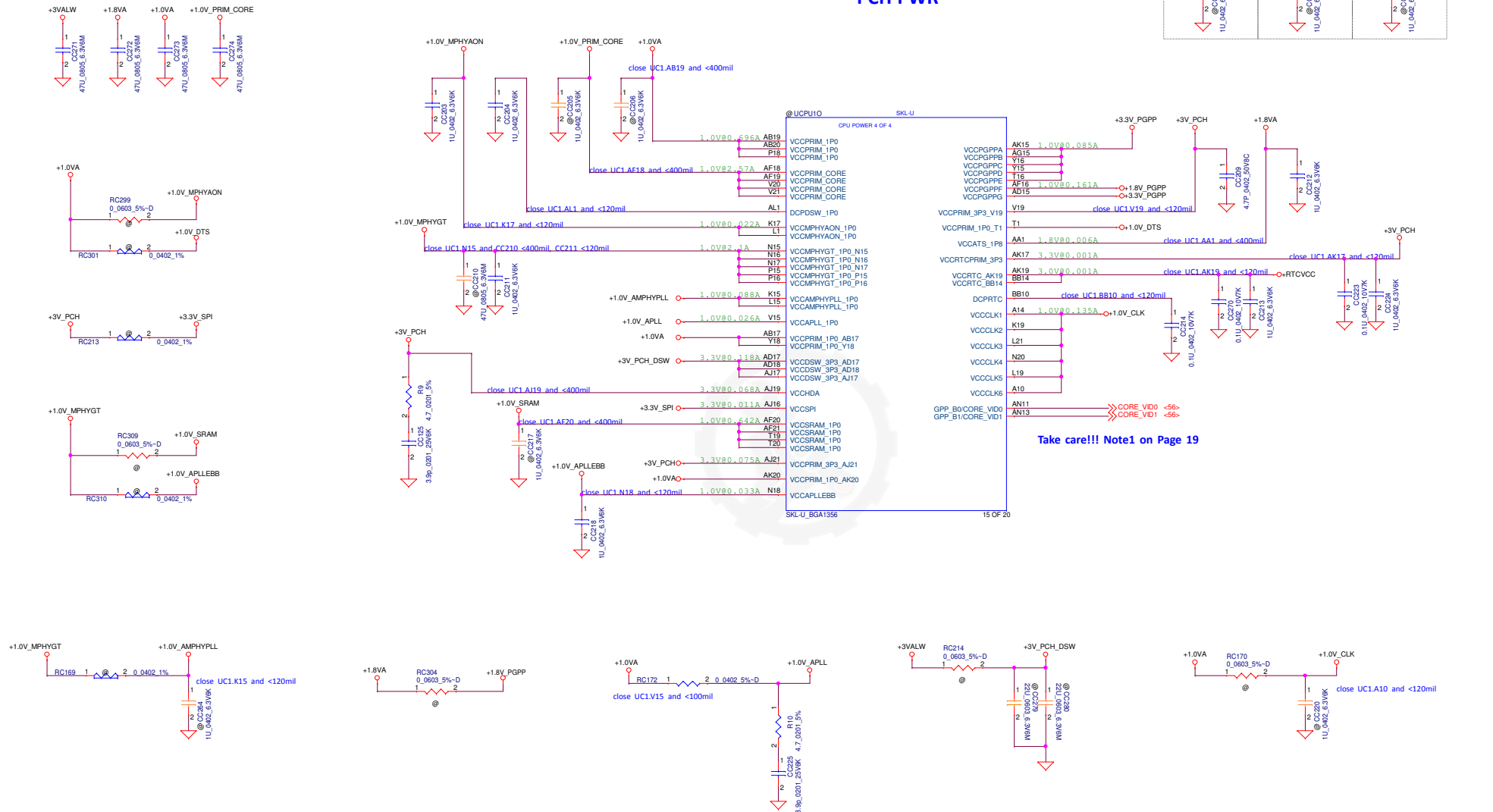
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Title	P18-MCP(12/14)PWR-VCCIO.MEM	
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PCH PWR



Take care!!! Note1 on Page 19

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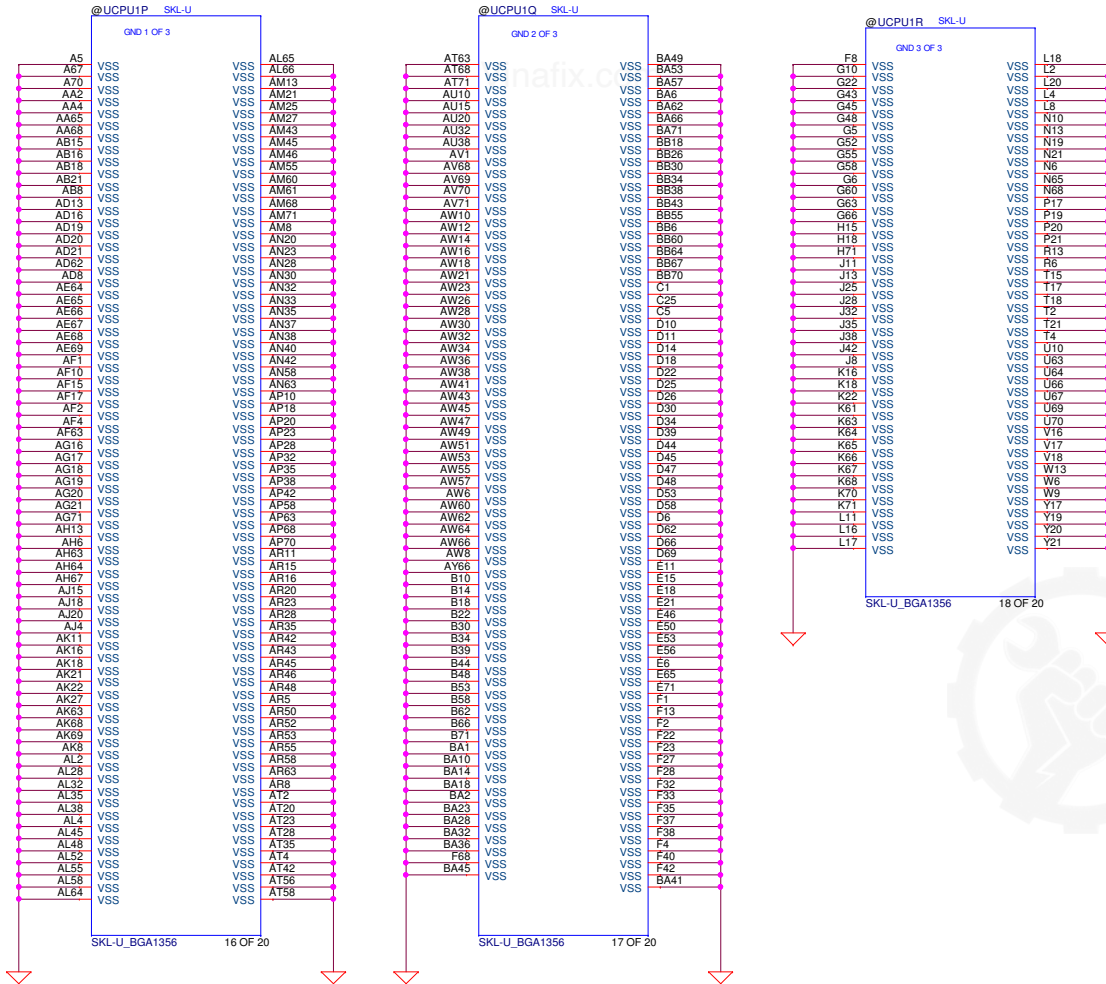
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Document Number
LA-D841P

Rev	
1.0	

Note1: VCCPRIM_CORE Implementat i on w t h PCH CORE_V D Reco mnendat i on

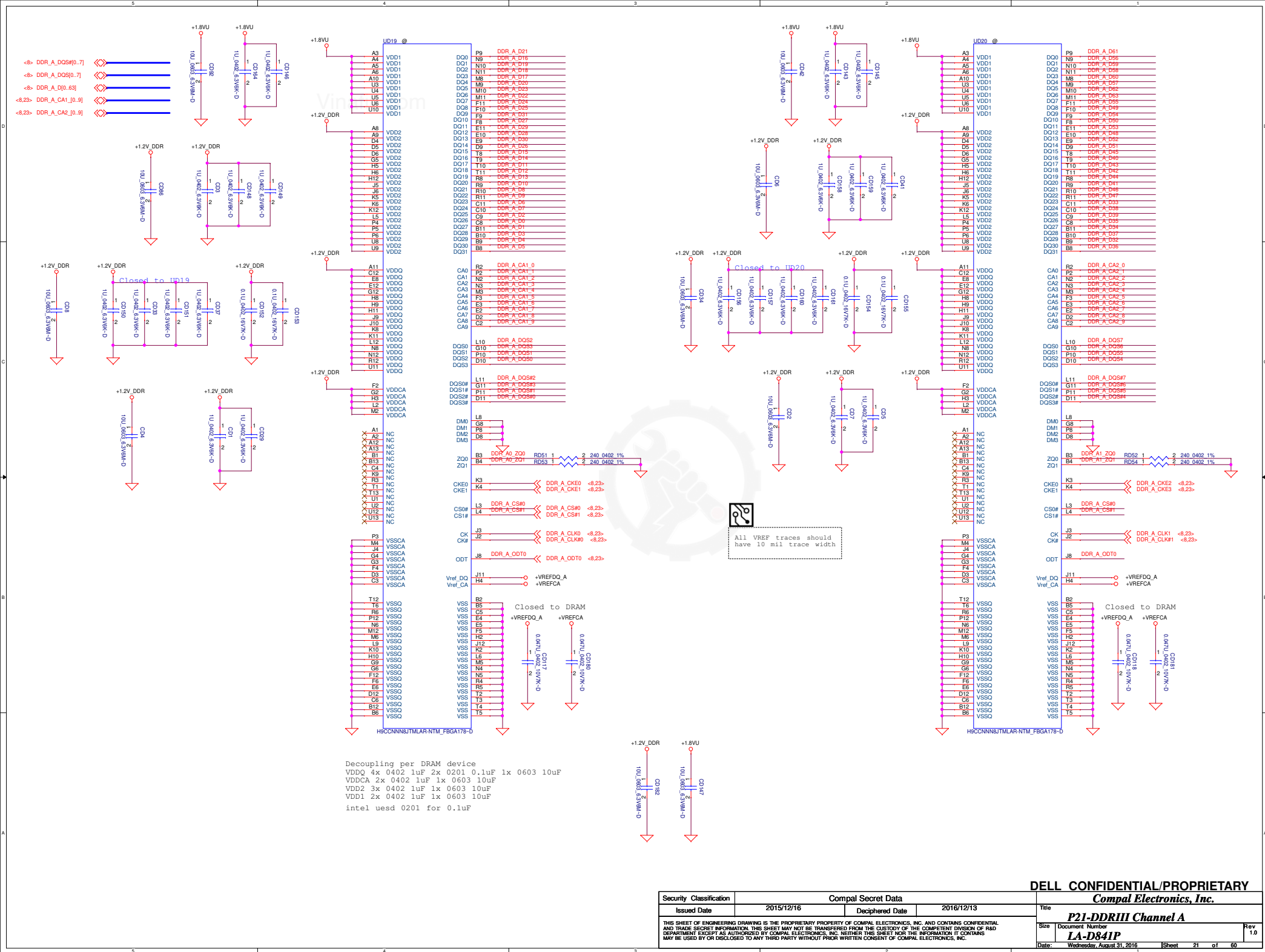
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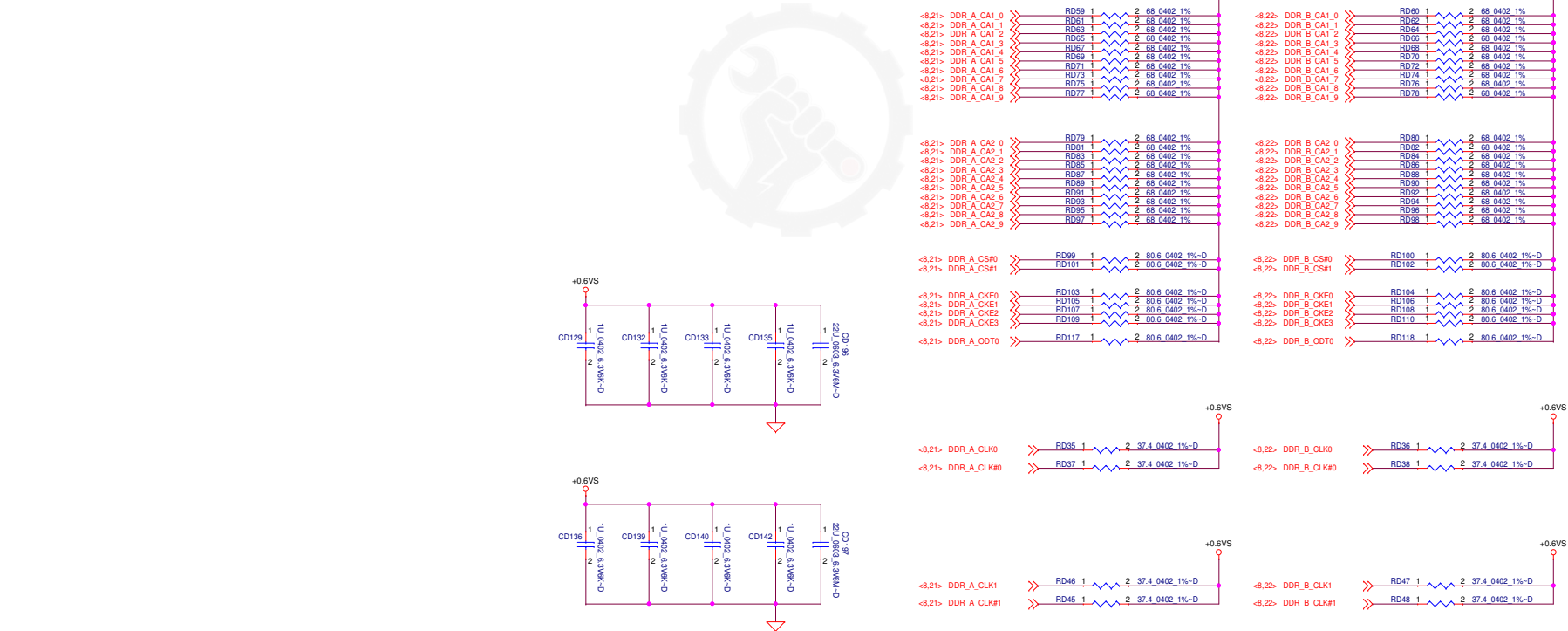
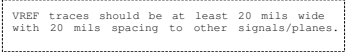


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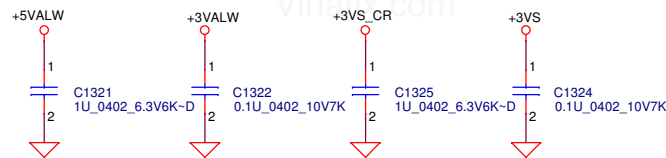
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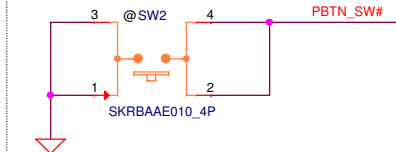




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NPI Stage Power Switch



<11> PCIE_PTX_CARDRX_P6
<11> PCIE_PTX_CARDRX_N6

CH13 1 2 0.1U 0402 10V7K-D PCIE_PTX_CARDRX_P6_C
CH14 1 2 0.1U 0402 10V7K-D PCIE_PTX_CARDRX_N6_C

<38> USB_PWR_SHR_EN_R#

<12> CLK_PCIE_MMI

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<11> USB_OC1#

<11> PCIE_PRX_CARDTX_P6

<11> PCIE_PRX_CARDTX_N6

<12> CLKREQ_PCIE#5

<11> USB20_P1

<11> USB20_N1

<12,37> PBTN_SW#

<37> USB1_DET#

<10> HOST_SD_WP#

<12,28,29,30,37,39> PCH_PLTRST#_EC

<38> USB_PWR_SHR_VBUS_EN_R

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<9> MEDIACARD_IRQ#

<37> LID_SW_IN#

+3VS_CR

+3VALW

+3VS

+5VALW

J101

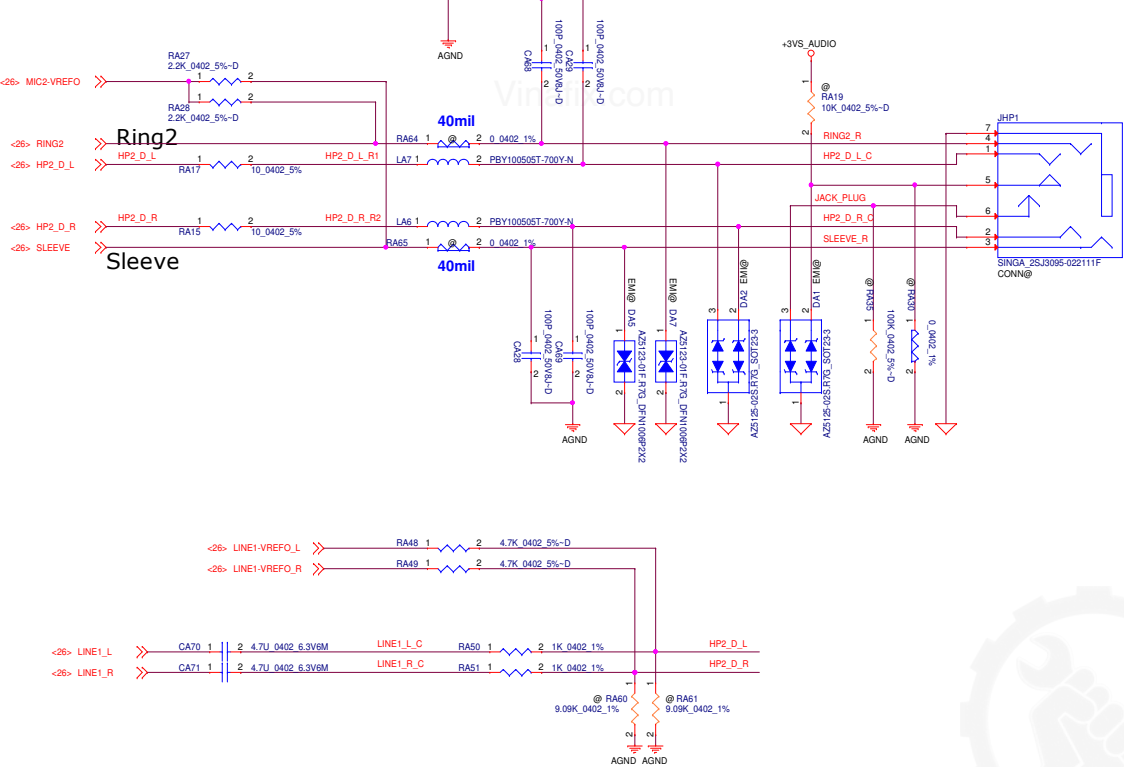
JXT_FP270H-061G1AM
CONN@

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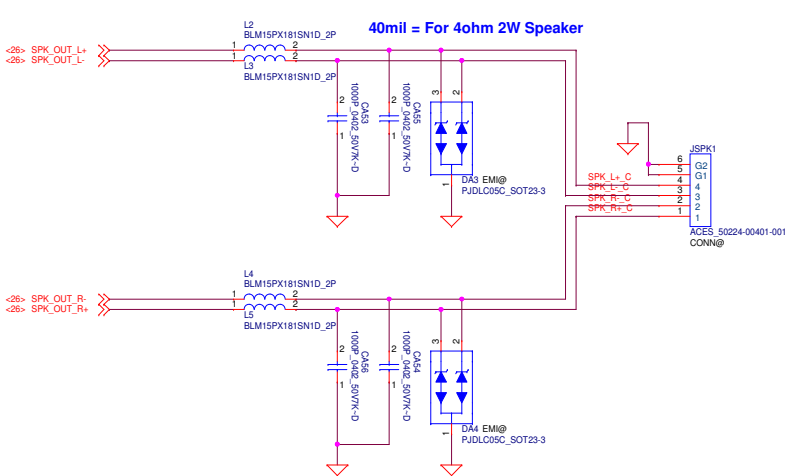
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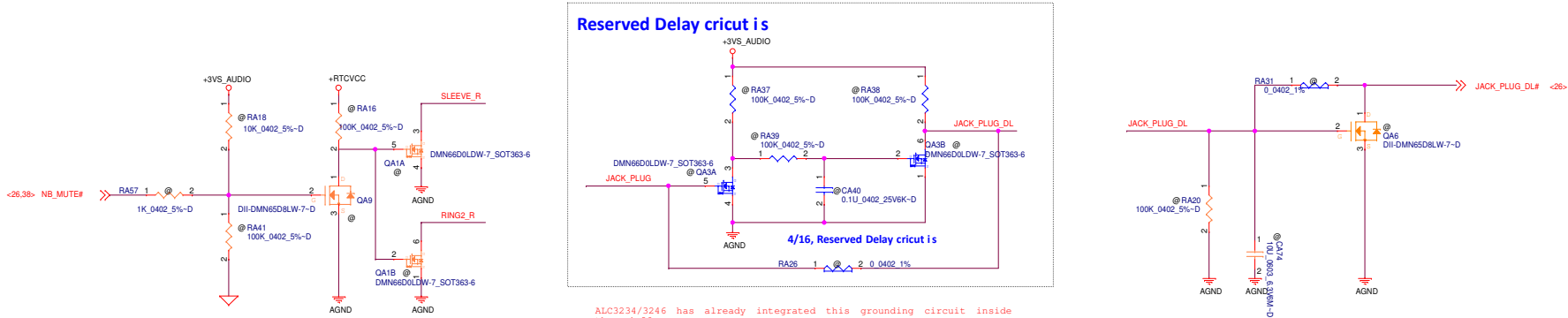
Universal Audio Jack



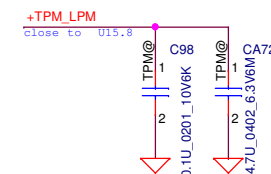
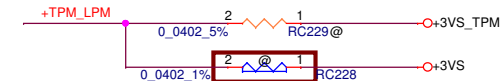
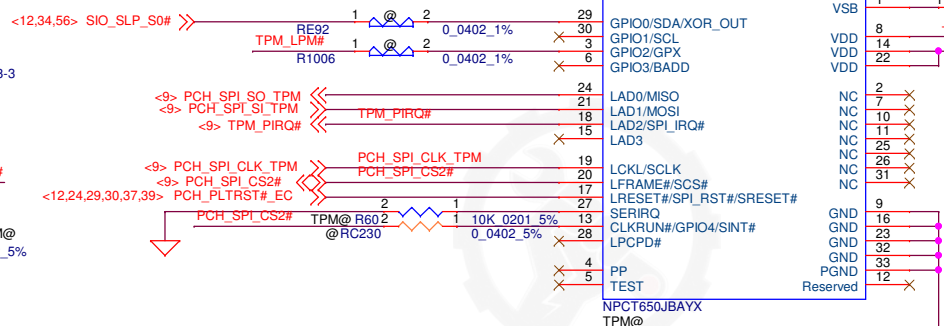
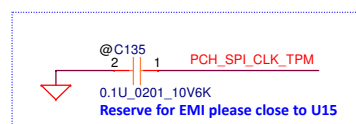
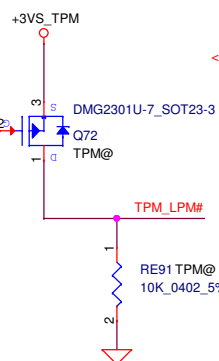
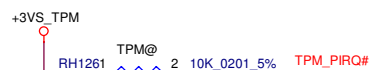
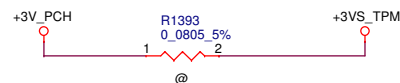
Int. Speaker Conn.



Prevent S3/S4/S5 Background Noise.



NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide

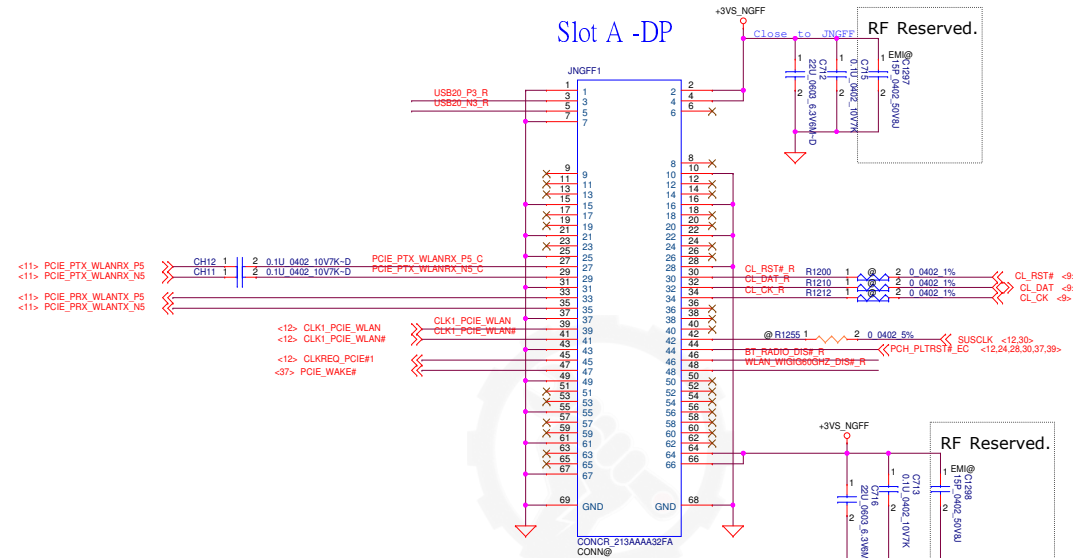
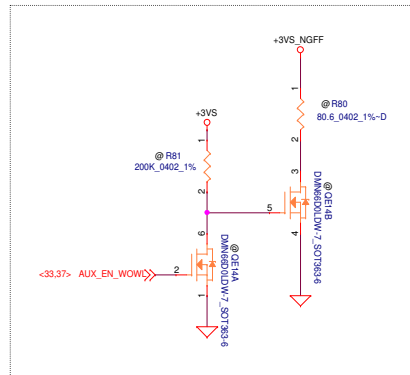
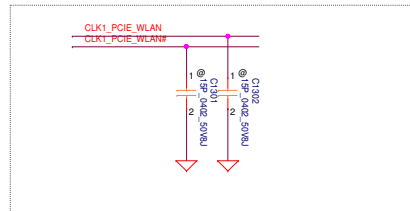
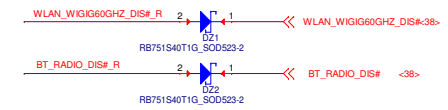
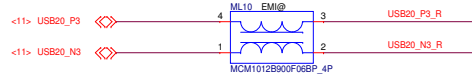


NOTE:
Place 0.1 uF capacitors as close as possible to the device power pins

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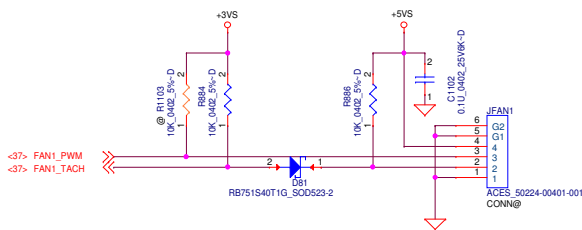
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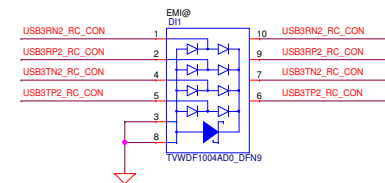
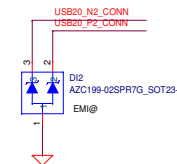
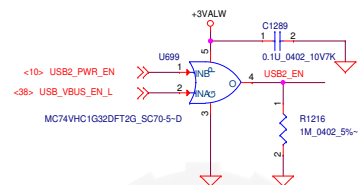
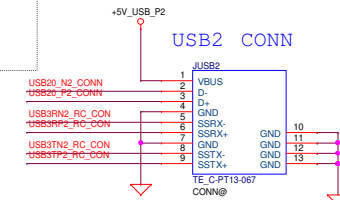
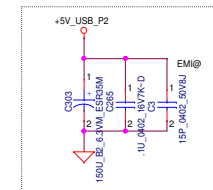
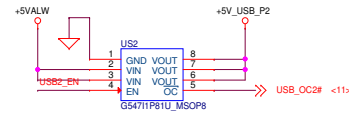
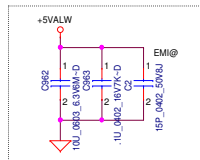
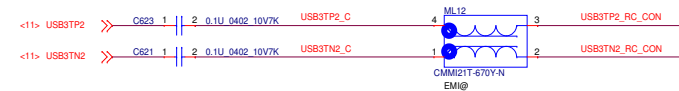
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FAN CONN

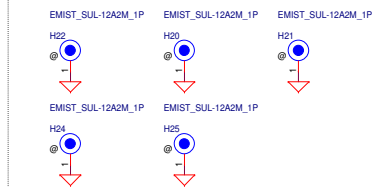


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				P30-SSD(M.2) / FAN	
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USB IO Port

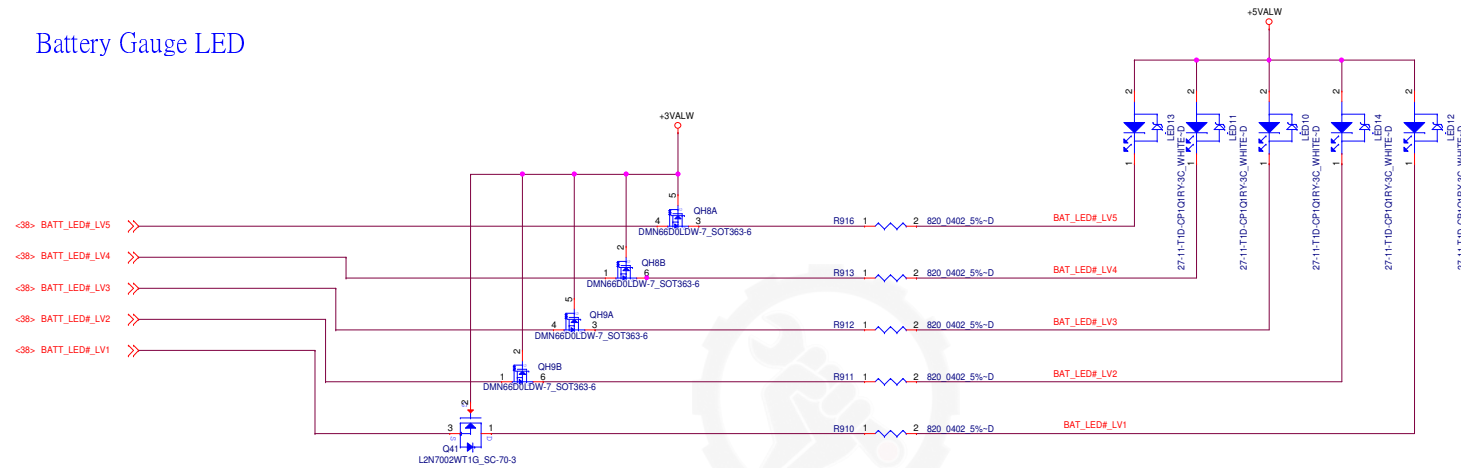


USB3.0 Shielding Clip

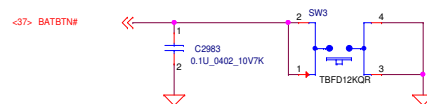


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				P31-USB 3.0 IO CONN	
				Size	Document Number
				LA-D841P	Rev 1.0
				Date:	Wednesday, August 31, 2016
				Sheet	31 of 60

Battery Gauge LED



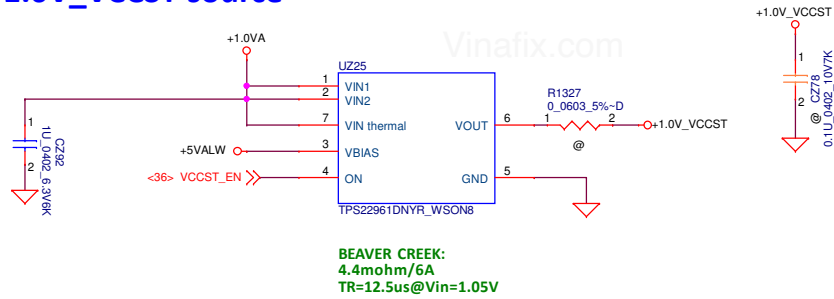
Battery Gauge Button



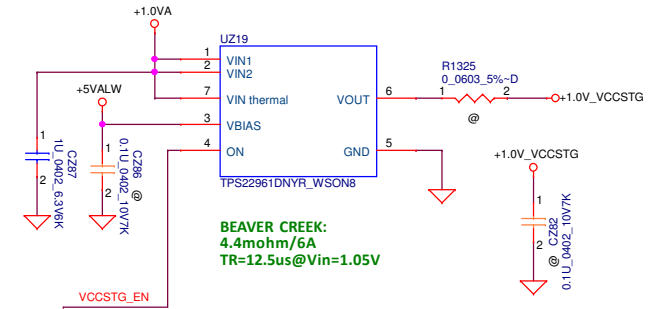
DELL CONFIDENTIAL/PROPRIETARY	
	<i>Compal Electronics, Inc.</i>

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				P32-BAT LED	
				Size	Document Number
				LA-D841P	
				Date:	Wednesday, August 31, 2016
				Sheet	32 of 60

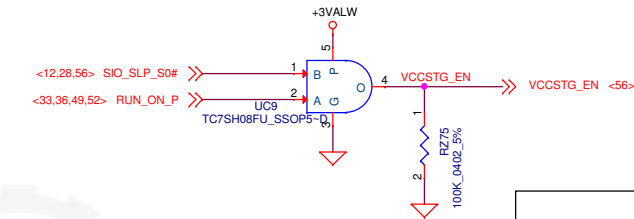
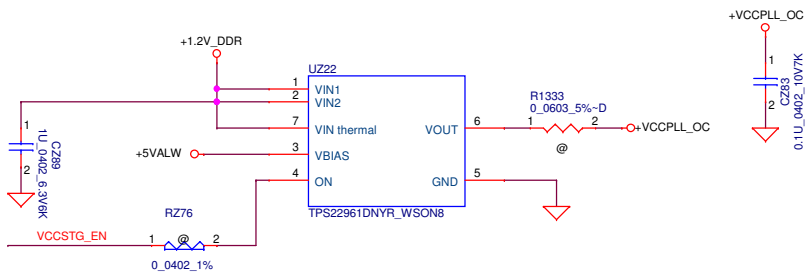
+1.0V_VCCST source



+1.0V_VCCSTG source

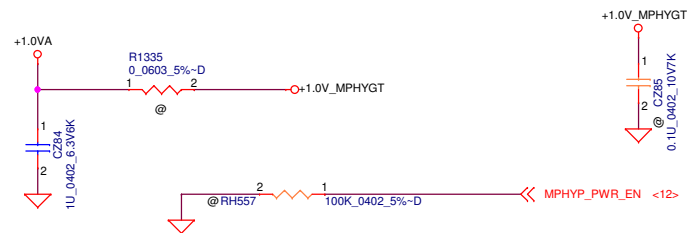


+VCCPLL_OC source

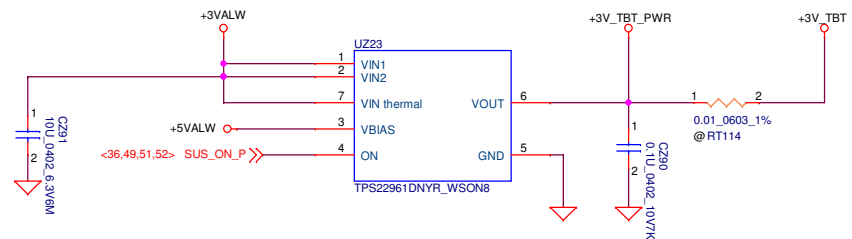


	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

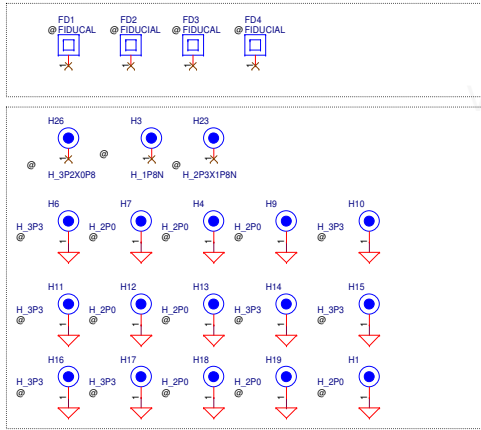
+1.0V_MPHYGT source



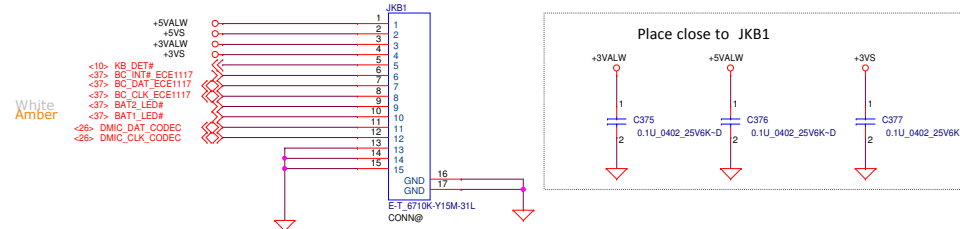
TBT Power circuits



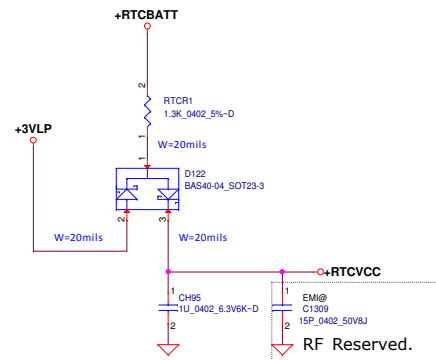
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								Document Number			
								LA-D841P			
								Date: Wednesday, August 31, 2016			
								Sheet 34 of 60			



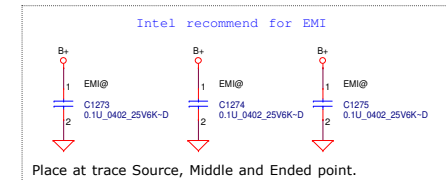
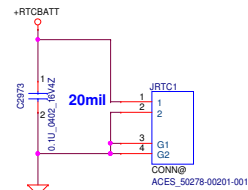
Keyboard Controller board + DMIC



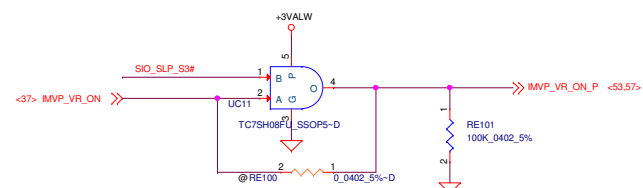
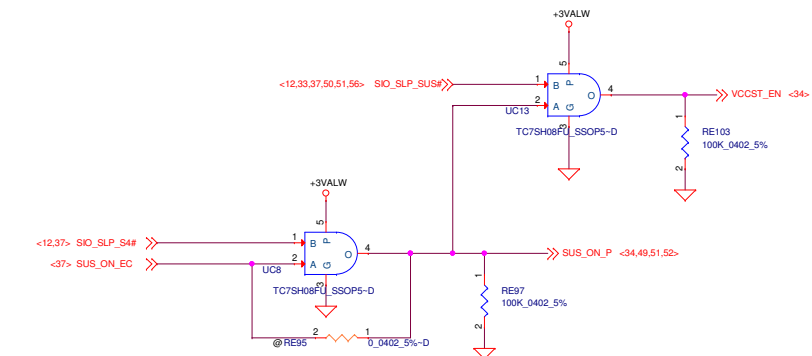
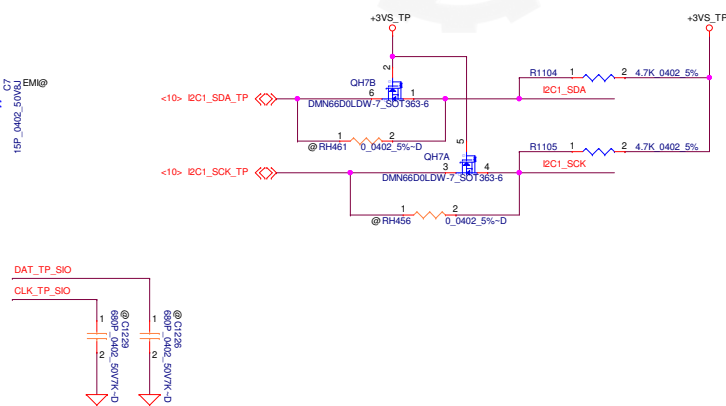
RTC Battery With Charge Function



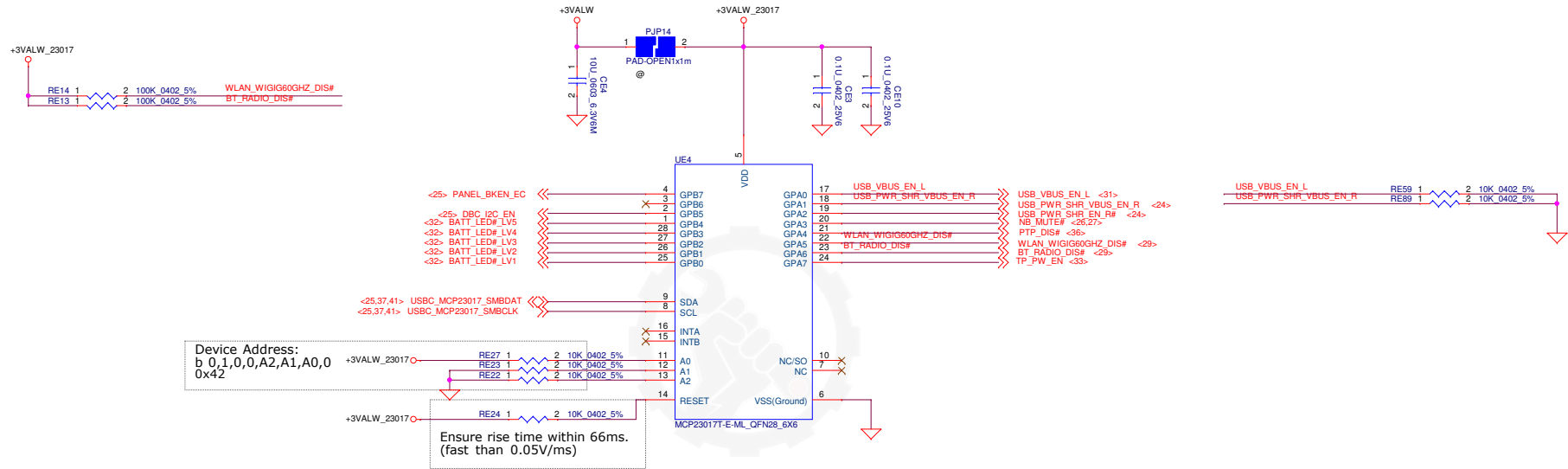
RTC Battery Conn

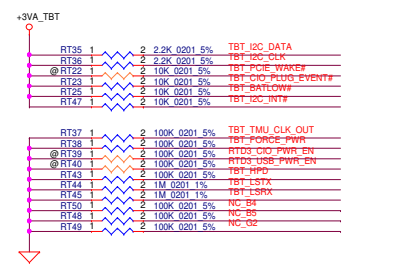
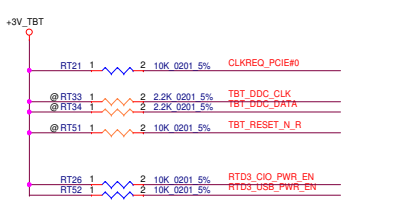
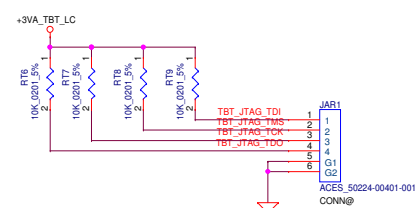


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				Size LA-D841P
				Rev 1.0
				Date: Wednesday, August 31, 2016 Sheet 35 of 60

[illegible]

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				Date:	Wednesday, August 31, 2016 Sheet 36 of 60

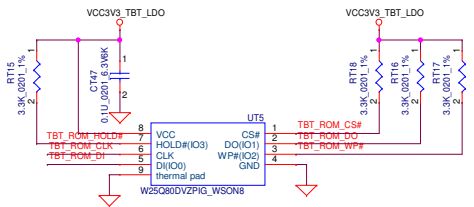
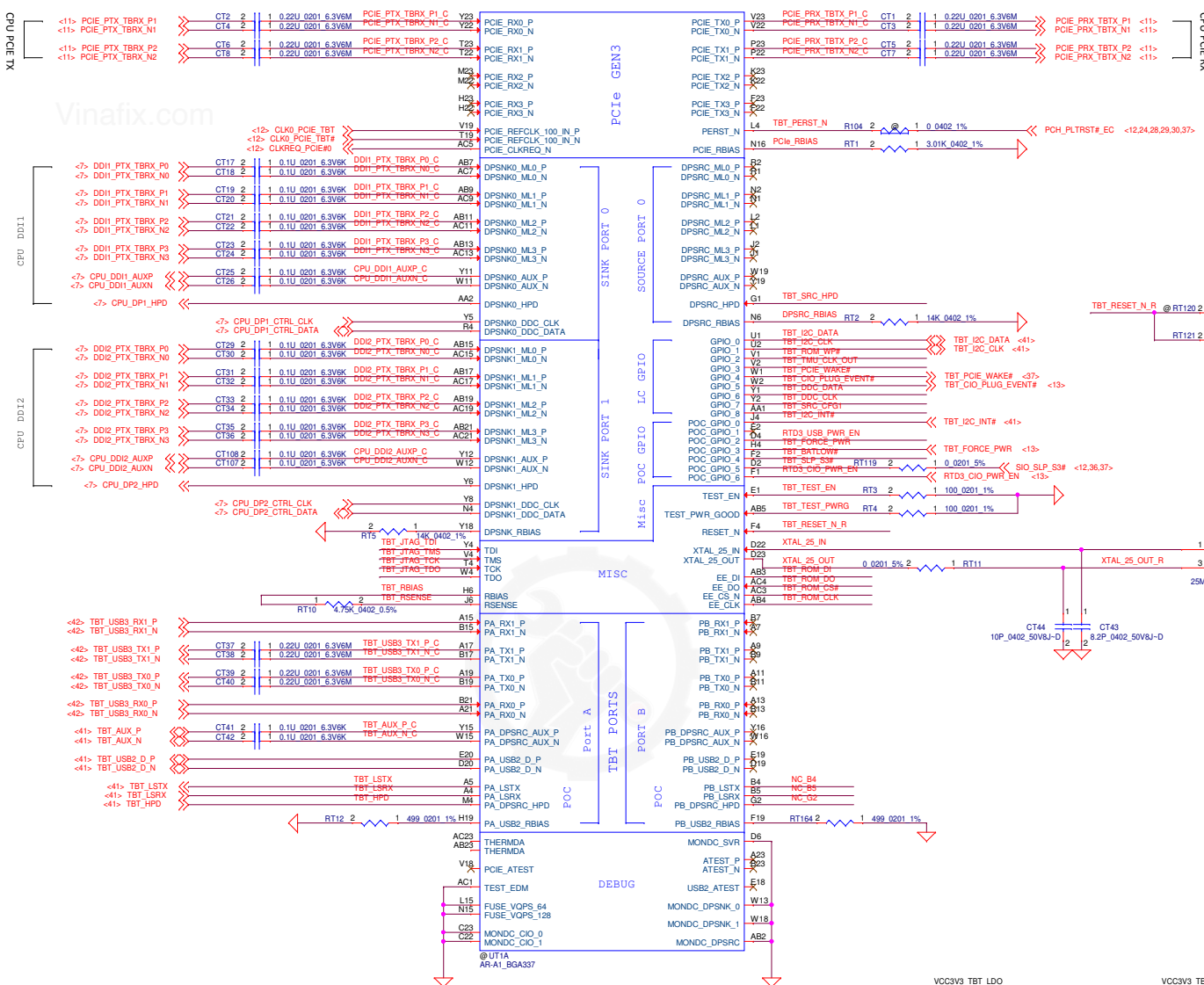




NOTE:
ASSEMBLE R297, R299 if DPSRC NOT IN USE

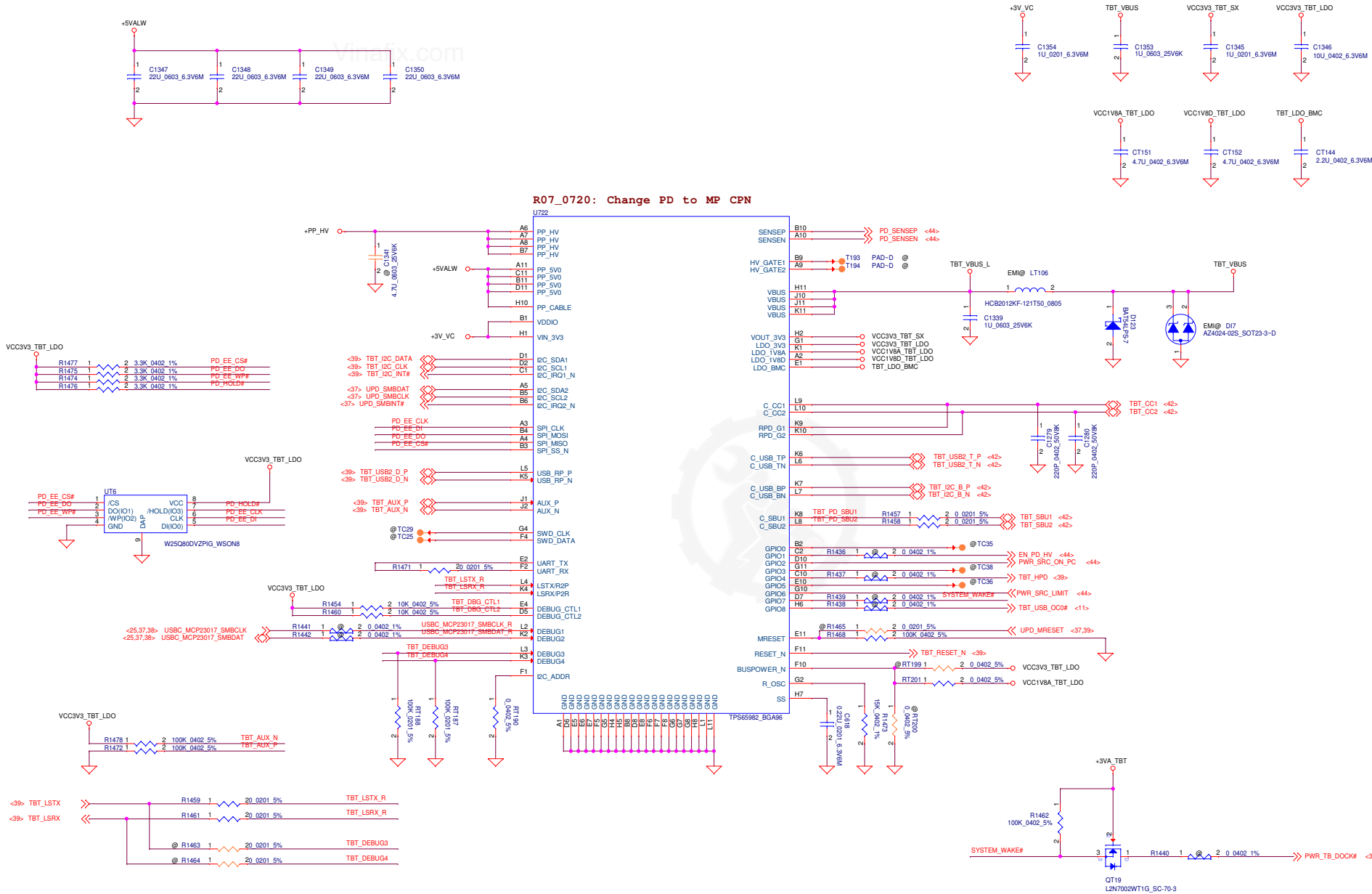
TBT_SRC_CFG1 R1403 1 2 1M 0.001 1%

TBT_SRC_HPD R1405 1 2 1M 0.001 1%

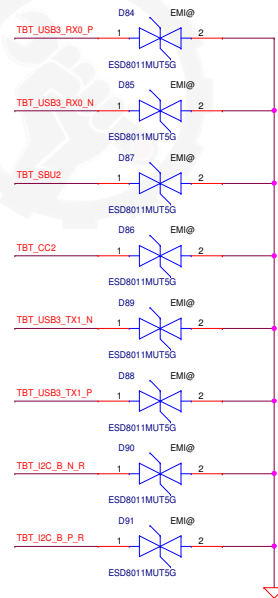
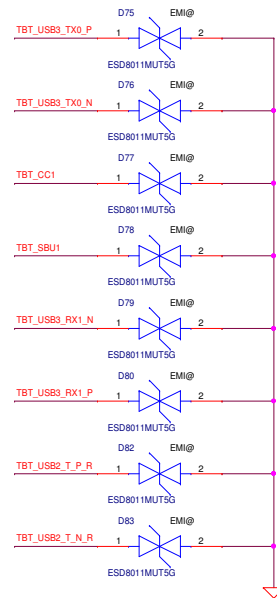
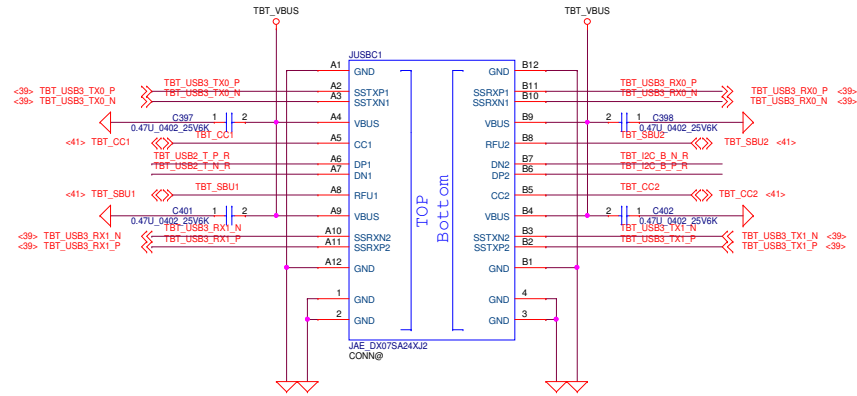
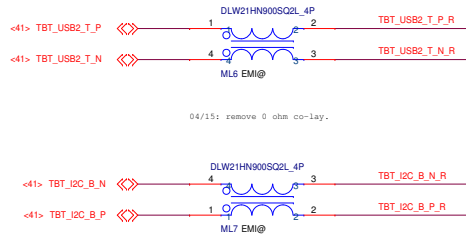


AR/PPS COMMON FLASH

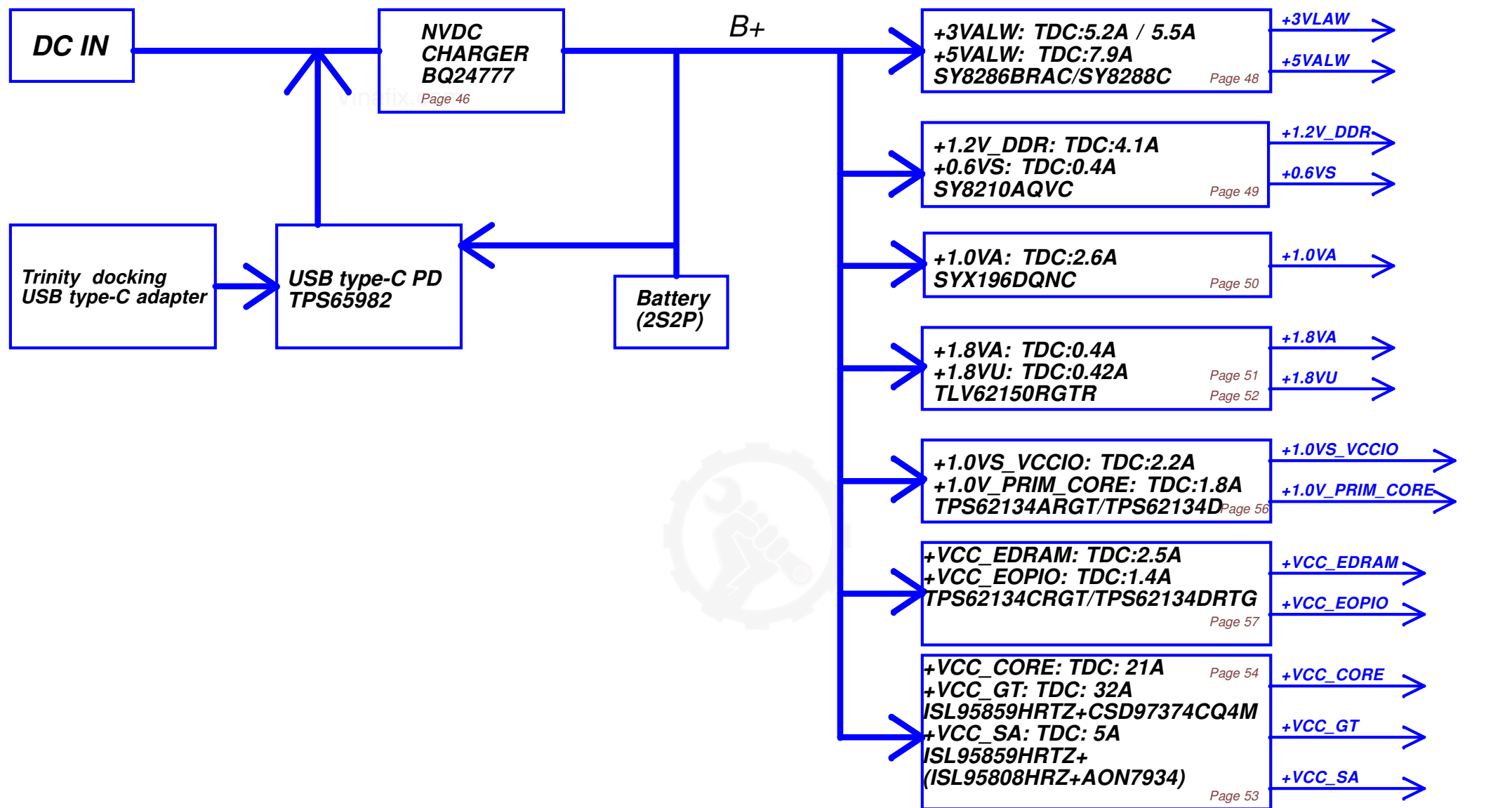
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Date:		Wednesday, August 31, 2016		Sheet	
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Vinafix.com

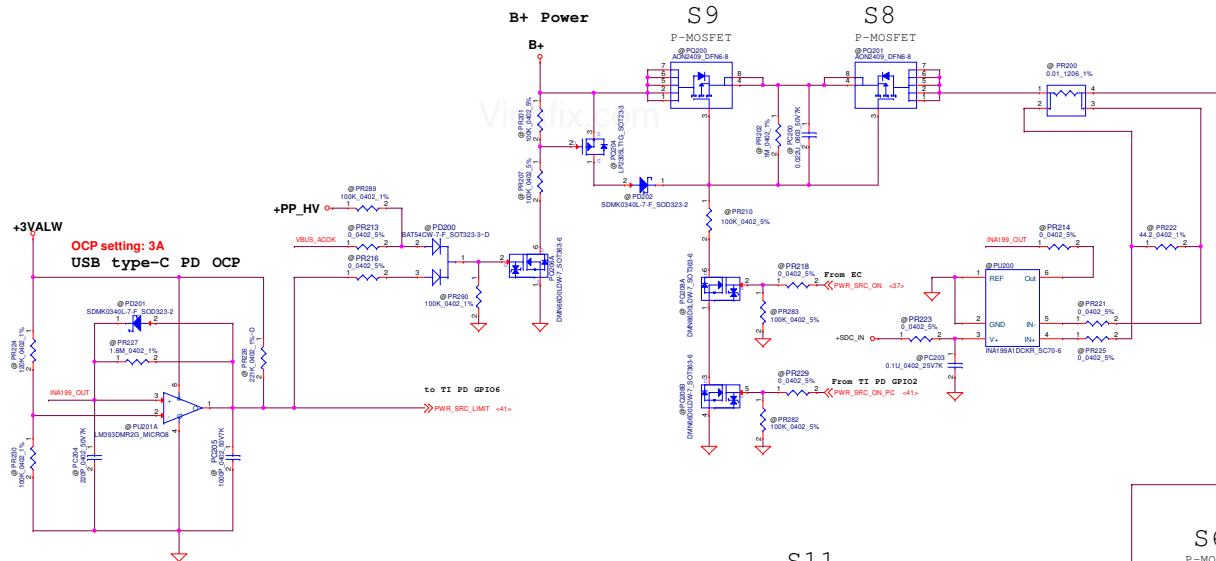


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				Document Number	
				LA-D841P	
				Rev	
				1.0	
				Date: Wednesday, August 31, 2016	
				Sheet 42 of 60	

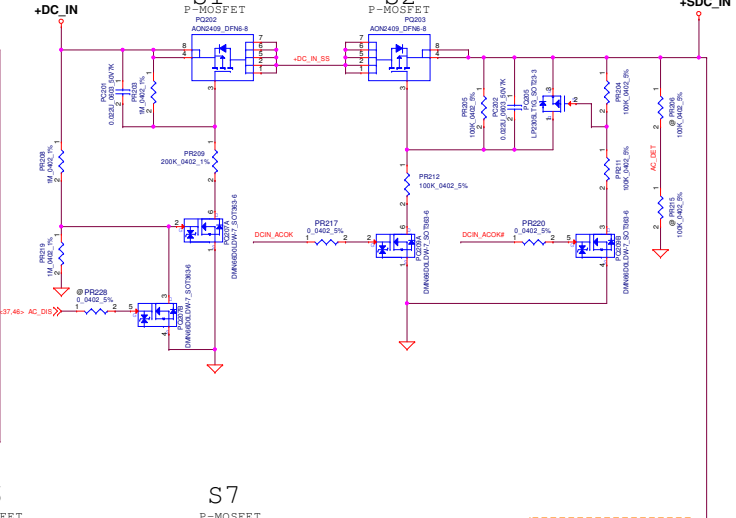


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				Size	Document Number	Rev
					LAD841P	1.0
				Date:	Wednesday, August 31, 2016	Sheet 43 of 59

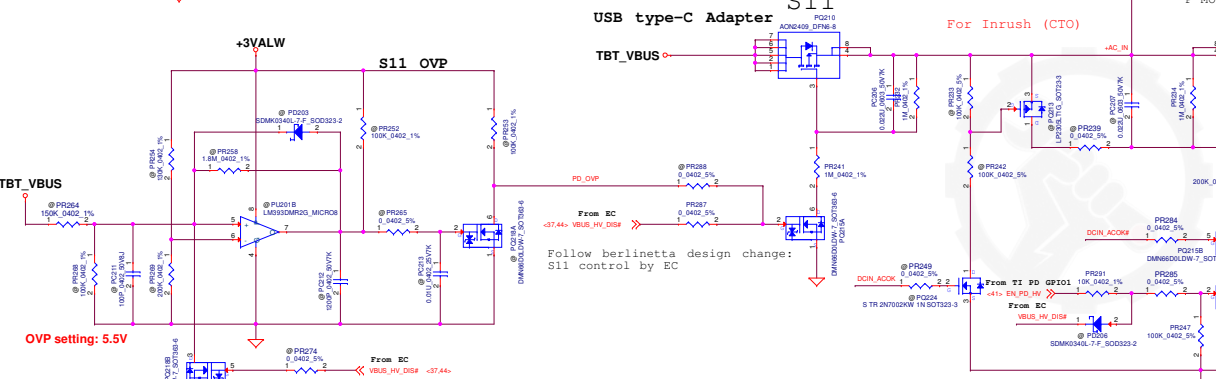
B+ Power



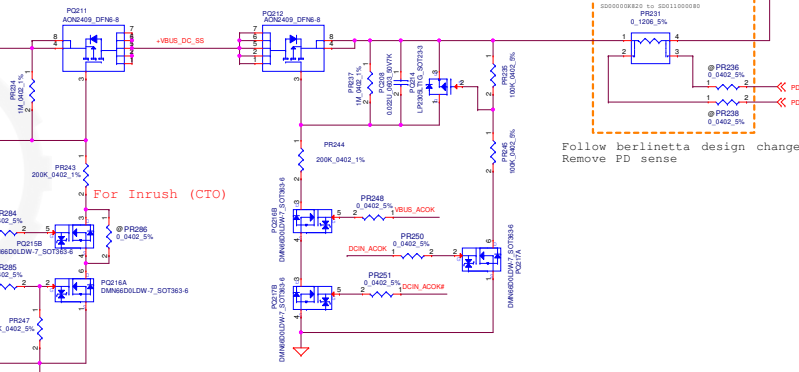
Barrel Adapter



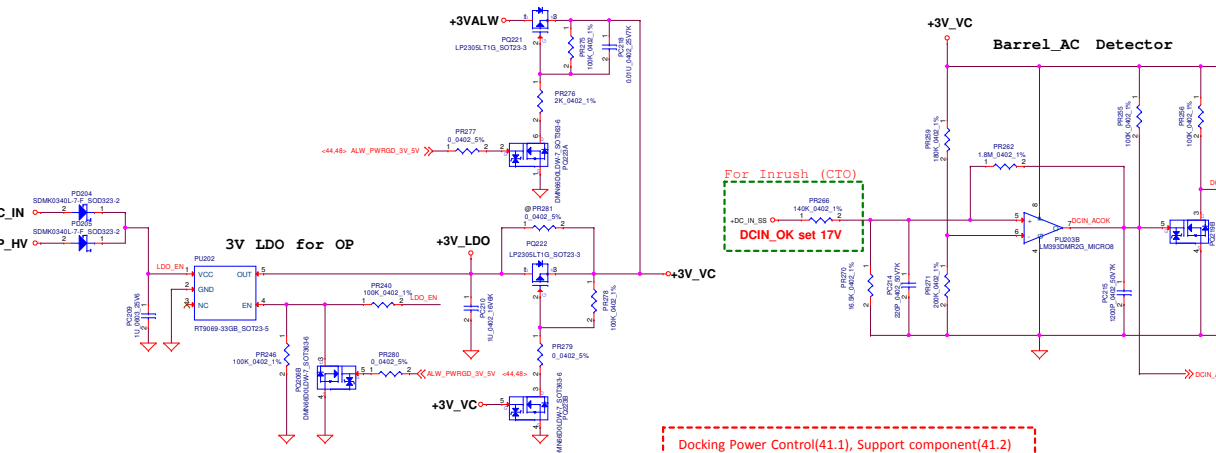
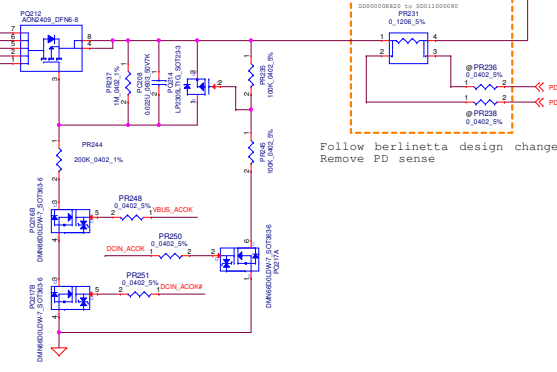
USB type-C Adapter



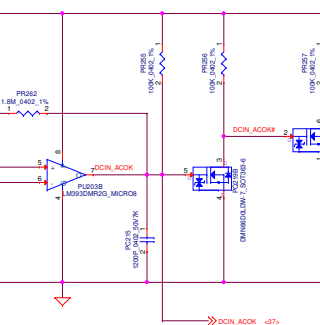
S6



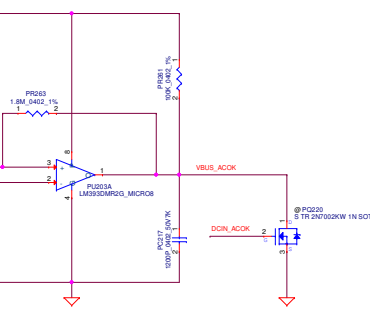
S7



Barrel AC Detector

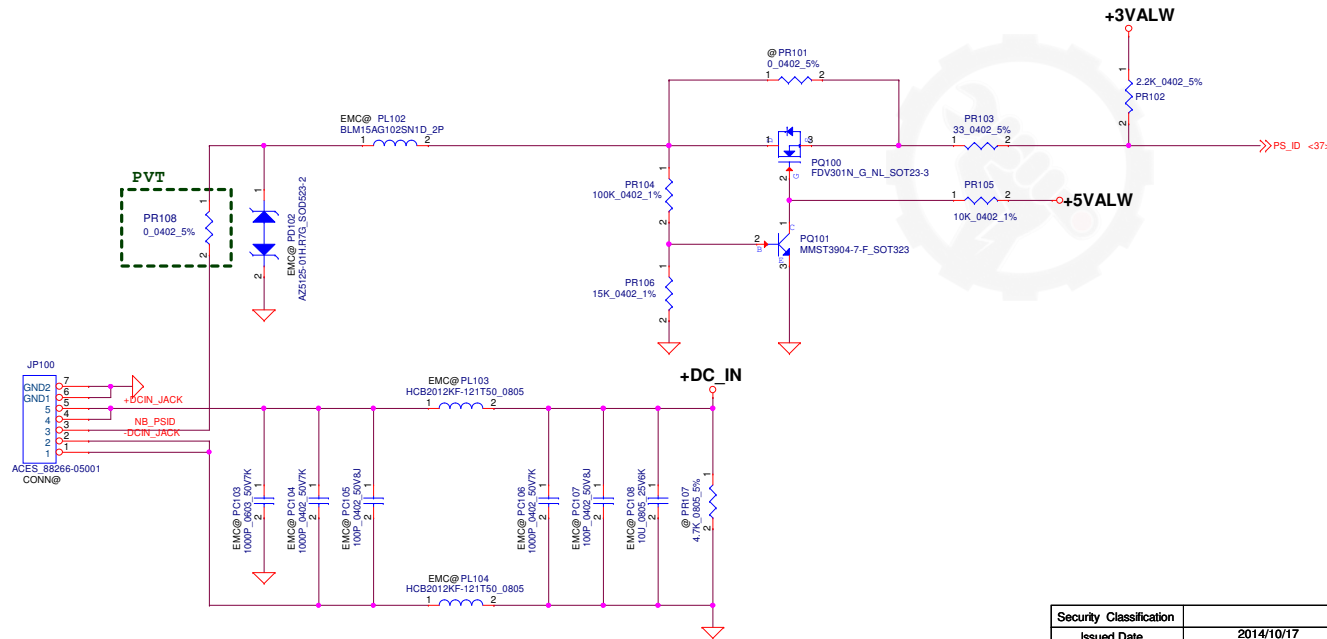
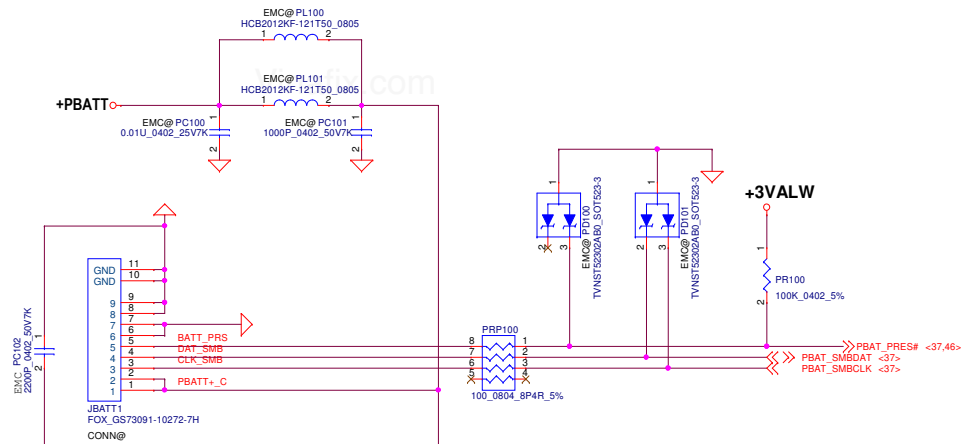


Vbus AC Detector



PBATT1 connector

SMART
Battery:
1.BATT++
2.BATT++
3.CLK_SMB
4.DAT_SMB
5.BAT_PRS
6.SYS_PRES
7.BAT_ALERT
8.GND
9.GND
10.GND
11.GND



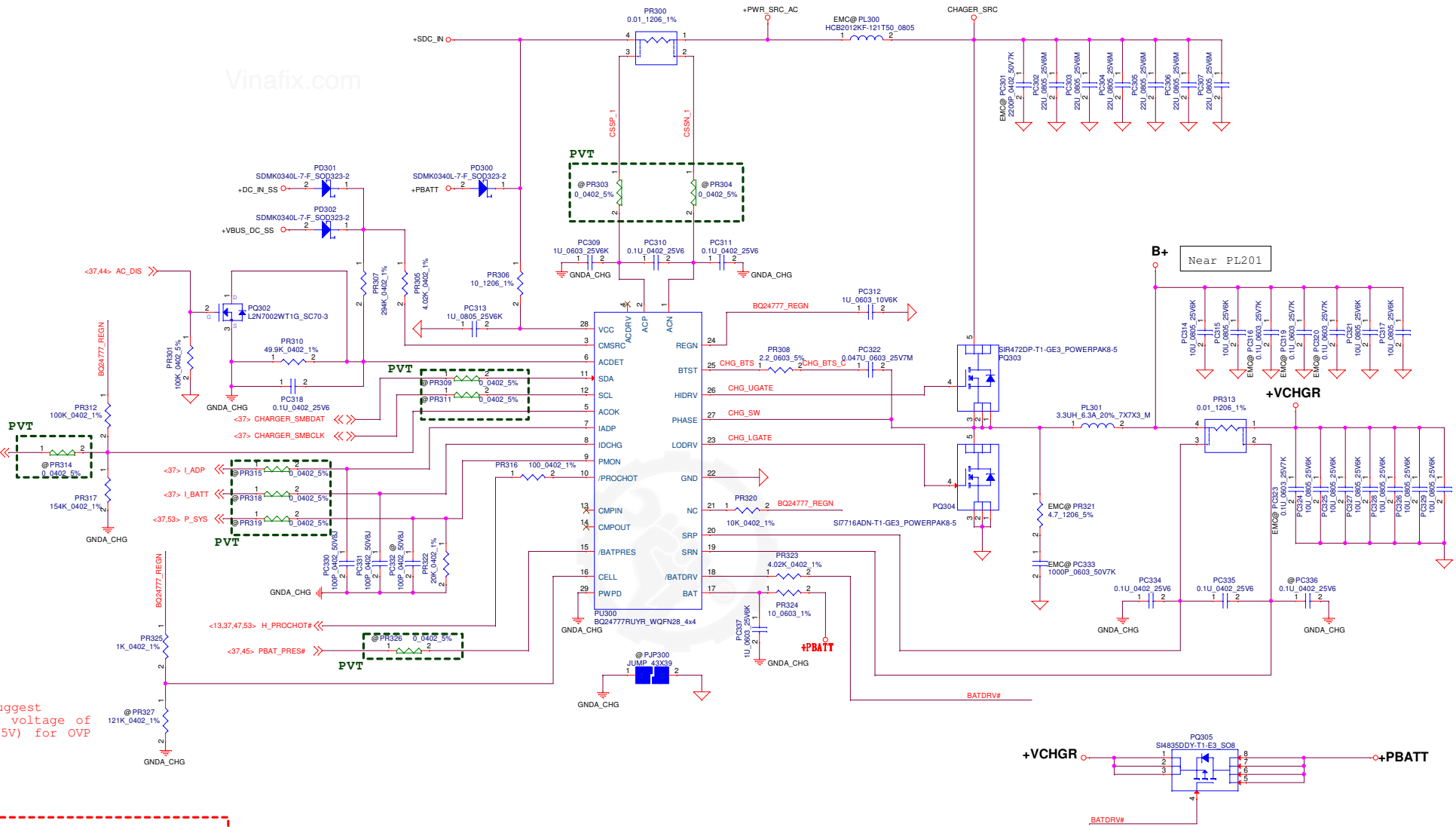
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				Part Number	LAD841P

PQ302
main:SB00000ST00
2nd:SB00000U000
3rd:SB00000Z600

CHARGER_SMBCLK
CHARGER_SMBDAT
pull up 10K in HW side

TI FAE Andrew suggest
Cell pin set the voltage of
three cell (13.5V) for OVP

Charger controller(40.1), Support component(40.2)

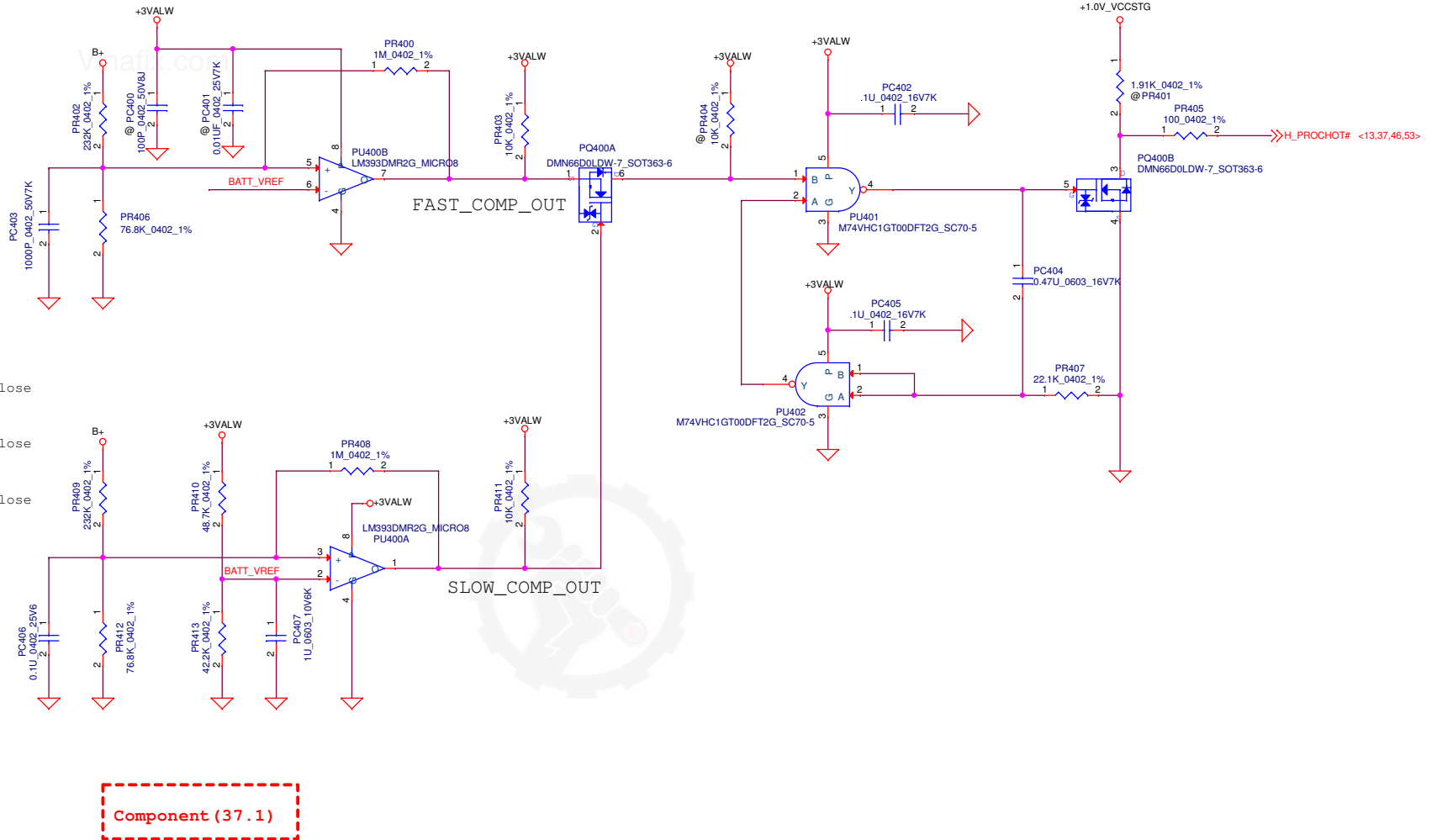


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Issued Date		2014/10/17		Title	
		Deciphered Date		2014/12/05	
				P46-PWR Charger	
				LAD841P	
				Date: Wednesday, August 31, 2016	
				Sheet 46 of 59	

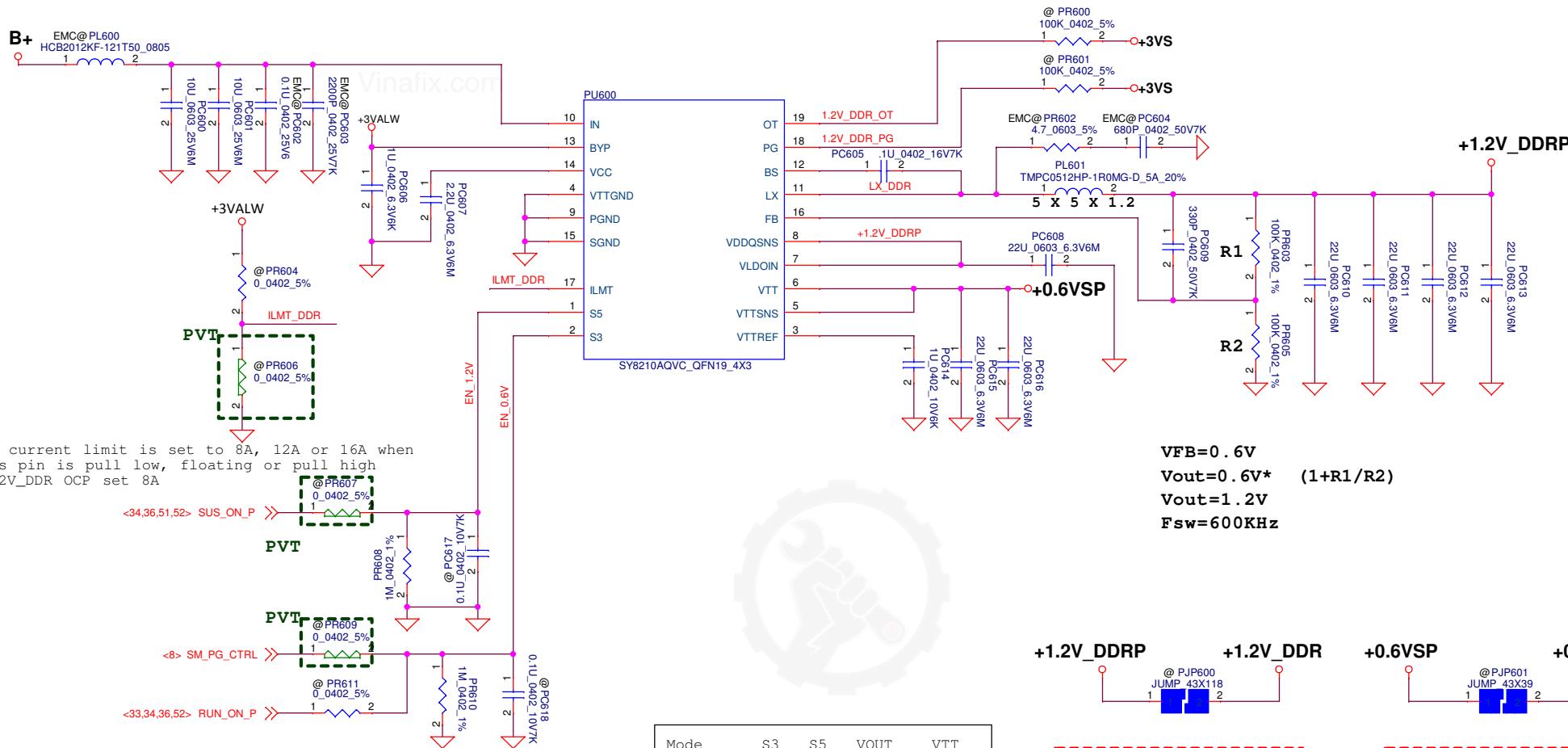
PU404_Main source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.05V PA409A close

PU404_2nd_source
PQ409A open at 3/5V_B+ below 5.72V
and 3/5V_B+ recover 6.05V PA409A close

PU404_3rd_source
PQ409A open at 3/5V_B+ below 5.73V
and 3/5V_B+ recover 6.04V PA409A close



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Issued Date		2014/10/17		Title	
		Deciphered Date		P47-PWR BATT low voltage detect	
				Size	
				Document Number	
				LAD841P	
				Date	
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				Rev	
				1.0	



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 8A

VFB=0.6V
Vout=0.6V* (1+R1/R2)
Vout=1.2V
Fsw=600KHz

DDR controller(35.3), Support component(35.4)

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDRP

+1.2V_DDR

+0.6VSP

+0.6VS

+1.2V_DDR

TDC 4.1A

Peak Current 5.8A

OCP Current 8A

0.6Volt +/- 5%

TDC 0.4A

Peak Current 0.6A

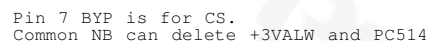
OCP Current 2A (fix)

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				Size	Document Number
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+1.0VAP **+1.0VA**

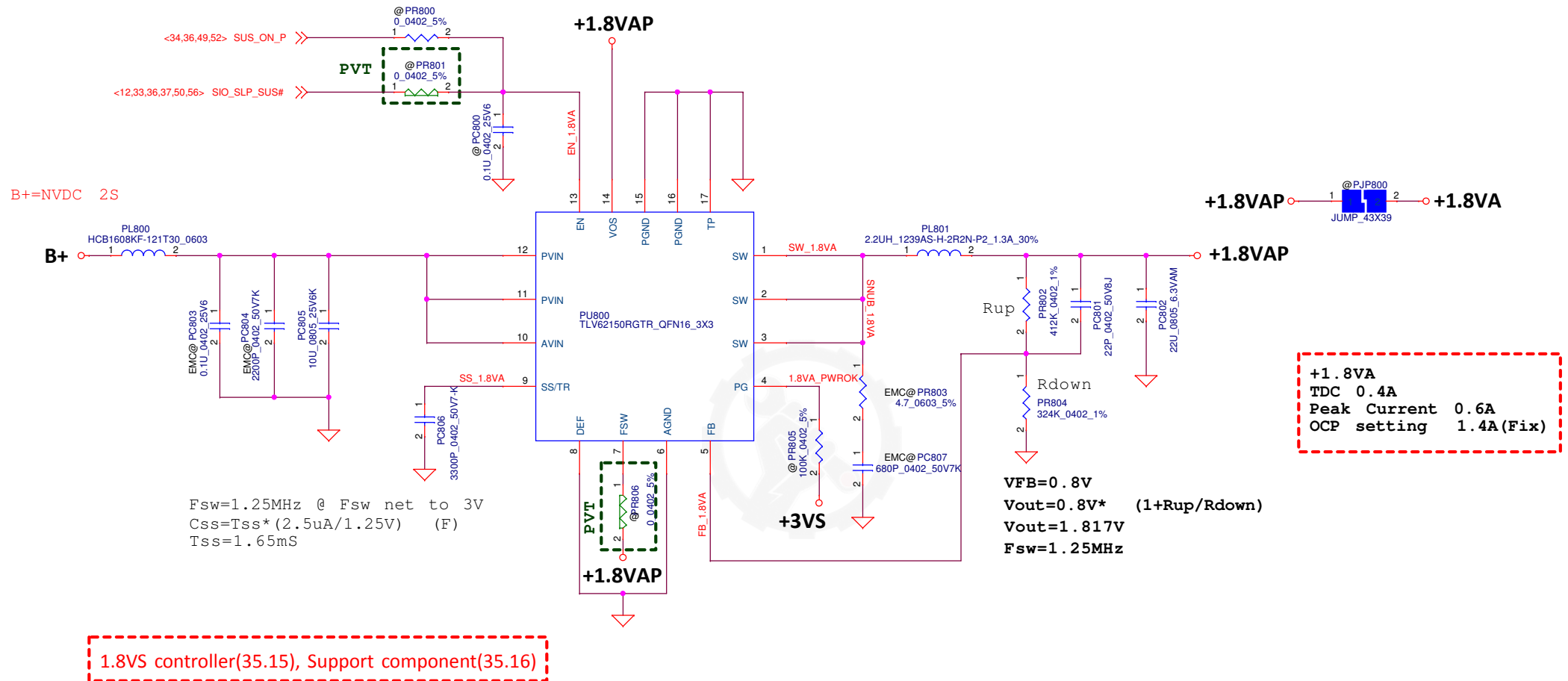
@PJP700
JUMP 43X79

1 2

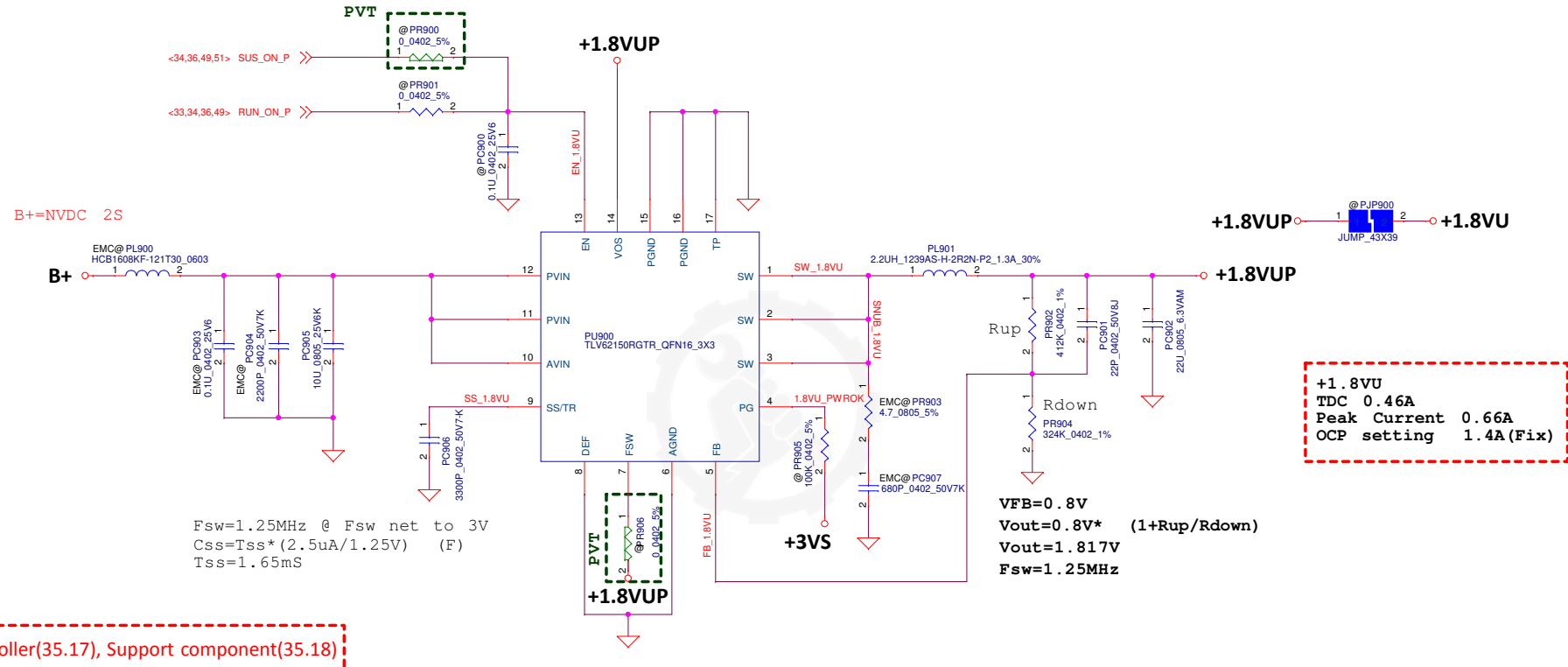


1.05V controller(35.5), Support component(35.6)

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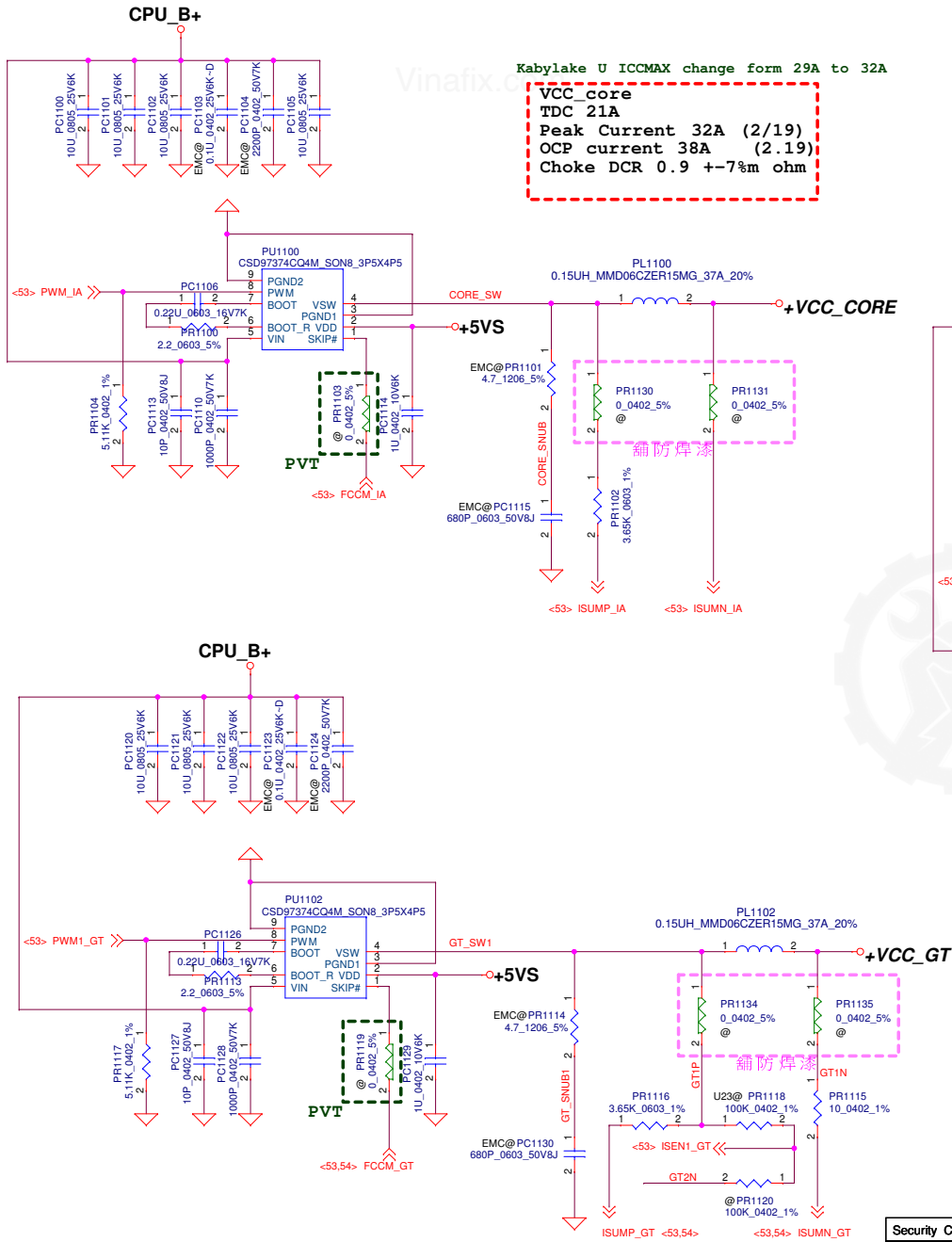


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				Size	Document Number	Rev
				LAD841P		1.0
				Date:	Wednesday, August 31, 2016	Sheet 51 of 59



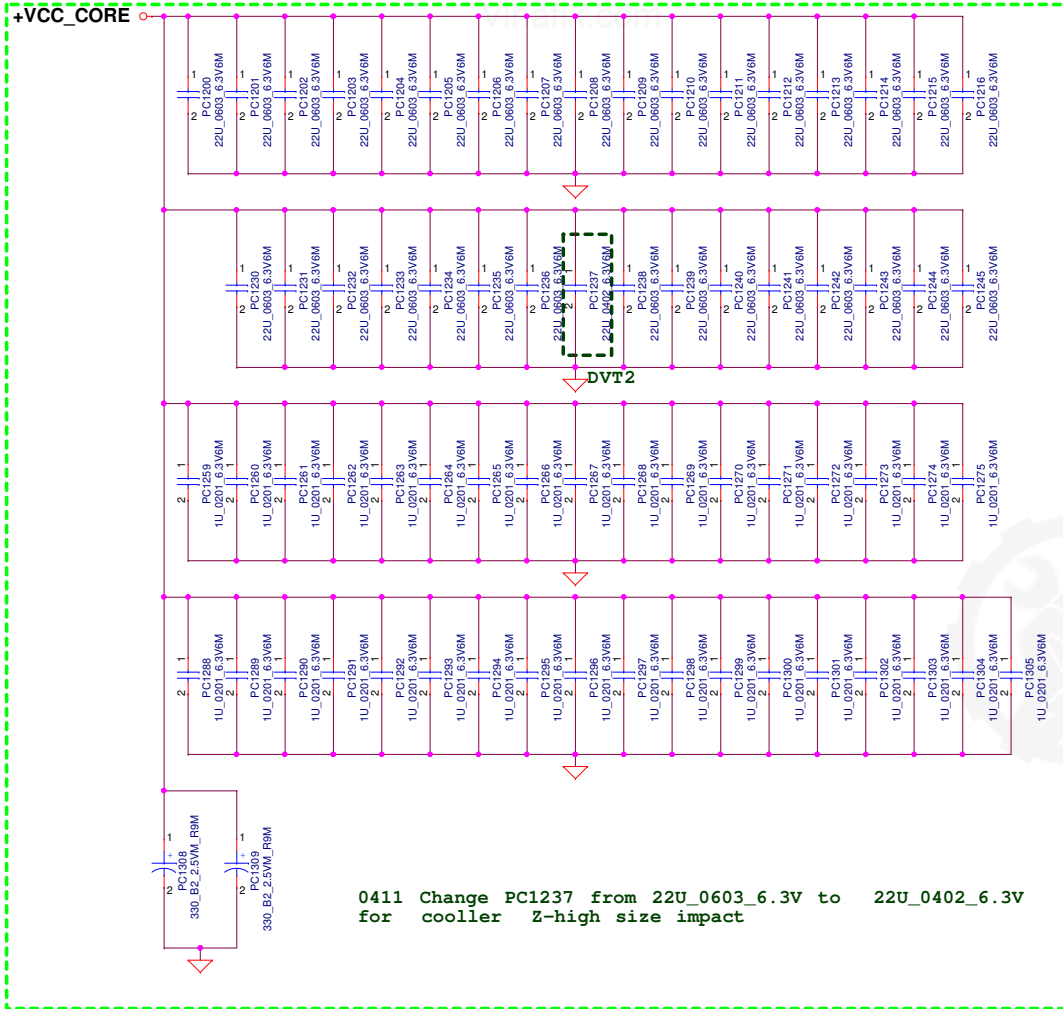


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					LAD84IP	1.0
				Date:	Wednesday, August 31, 2016	Sheet 53 of 59



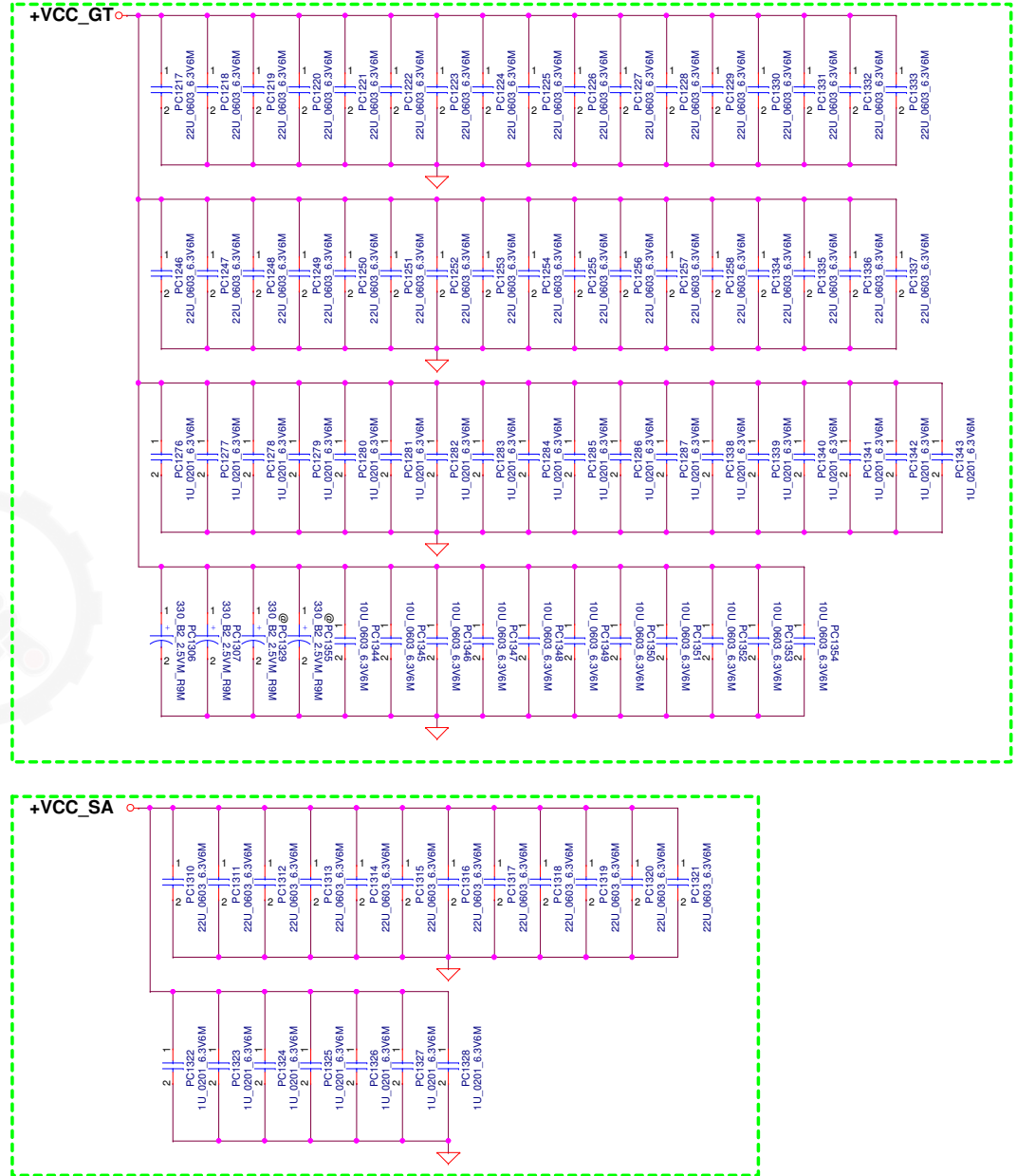
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Issued Date	2014/10/17	Deciphered Date	2014/12/05	Title	
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VCC_CORE Place on CPU
TOP Side.
22U_0603 * 26 pcs +1U_0201*33 pcs
Bottom Side.
330u_B2*2 pcs + 22U_0603 * 7 pcs + 1U_0201 *2



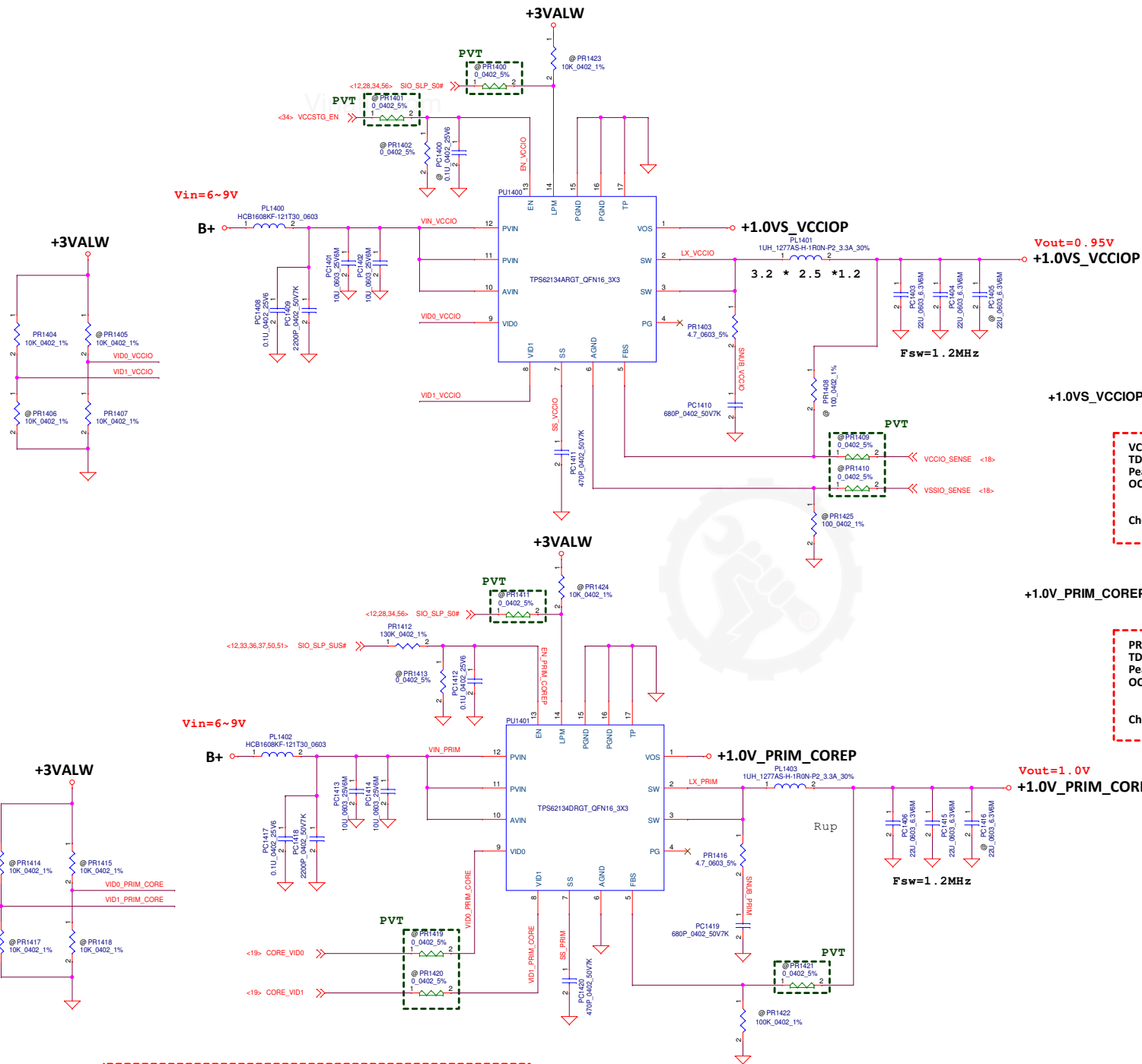
VCC_SA Place on CPU
TOP Side.
22U_0603 * 10 pcs + 1U_0201*7 pcs
Bottom Side.
22U_0603 * 2 pcs

VCC_GT Place on CPU
TOP Side.
22U_0603 * 34 pcs +10U_0603*11 pcs +1U_0201*18 pcs
Bottom Side.
330u_B2*4 pcs



VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

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				Date	Wednesday, August 31, 2016
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				Rev	1.0

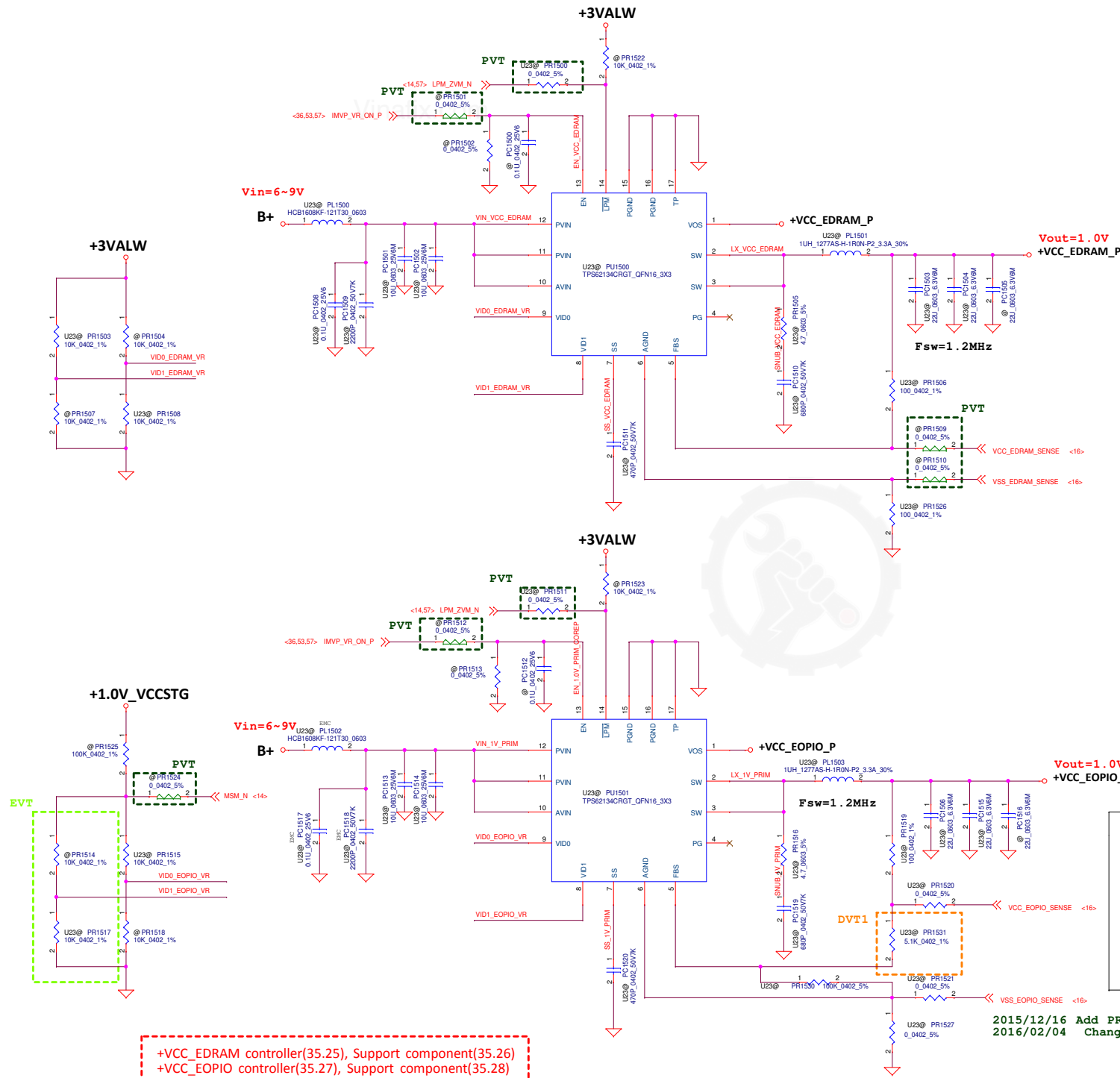


+1.0VS_VCCIO

+1.0V_PRIM_CORE

+1.0VS_VCCIO controller(35.21), Support component(35.22)
+1.0V_PRIM_CORE controller(35.23), Support component(35.24)

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				Size Document Number
				LAD841P
				Rev 1.0
				Date: Wednesday, August 31, 2016
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+VCC_EDRAM
TDC 1.75A
Peak Current 2.5 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm

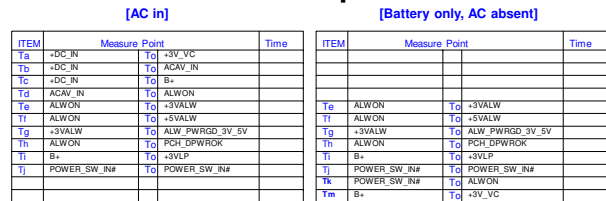
+VCC_EOPPIO
TDC 1.4A
Peak Current 2.0 A
OCP Current 4.2 A Fix by IC
MIN:3.6A
MAX:4.9A
Choke DCR 48.0mohm

	LPM	VID1	VID0	Vout
	0	X	X	0.000 (LPM)
	1	0	0	0.800+0.05 (MSM)
	1	0	1	0.950+0.05
	1	1	0	1.000+0.05
	1	1	1	1.050+0.05

2015/12/16 Add PR1530 PR1531 for Kabylake EOPPIO support to 0.85V
2016/02/04 Change PR1531 from 6.2k to 5.1k to Set 0.85V and 1 V

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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/06	Deciphered Date	2016/08/28	Title P58-PWR PIR-1	
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ITEM	Measure Point	Time
T1	+3VALW	0
T2	SIO_SLP_S0S#	1/3W_PCH
T3	SIO_SLP_S0S#	1/3W_PCH
T4	SIO_SLP_S0S#	1/10V_PRIM_CORE
T5	SIO_SLP_S0S#	1/10VA
T6	+3VALW	MPMPW_PWR_EN
T7	MPMPW_PWR_EN	1/10V_MPMPGT
T8	SIO_SLP_S0S#	1/3W_PCH
T9	+1/10VA	PCH_RSMRSt#
T10	PCH_RSMRSt#	AC_PRESENT
T11	PCH_RSMRSt#	SIO_SLP_S#
T12	SIO_SLP_S#	SIO_SLP_S#
T13	SIO_SLP_S#	SIO_SLP_WLAN#
T14	SIO_SLP_WLAN#	AUX_EN_WOVL
T15	AUX_EN_WOVL	1/3VS_NGFF
T16	SIO_SLP_S#	SIO_SLP_S#
T17	SIO_SLP_S#	1/3VS_VCGST
T18	SIO_SLP_S#	SUS_ON_EC
T19	SUS_ON_EC	1/18VU
T20	SUS_ON_EC	1/18VZ_DDR
T21	SIO_SLP_S#	1/10VZ_PWRGD
T22	SIO_SLP_S#	SIO_SLP_S#
T23	SIO_SLP_S#	RUN_ON_EC
T24	RUN_ON_EC	1/310VX_SSD
T25	RUN_ON_EC	1/10VS_VCGST2
T26	RUN_ON_EC	1/18VS_VCGD2
T27	RUN_ON_EC	1/18VU
T28	RUN_ON_EC	1/5VS
T29	+3VS	RUNPWROK
T30	+3VS	MMP_VR_ON
T31	MMP_VR_ON	VCCORE_PG (PCH_PWRCK)
T32	VCCORE_PG (PCH_PWRCK)	VCCO_3SA
T33	MMP_VR_ON	VCCO_EDRAM
T34	MMP_VR_ON	VCCO_EGPIIO
T35	MMP_VR_ON	SYS_PWRCK (RESET_OUT#)
T36	PCH_PLURSt#	1/10VZ_PWRGD
T37	PCH_PLURSt#	1/10VZ_GT