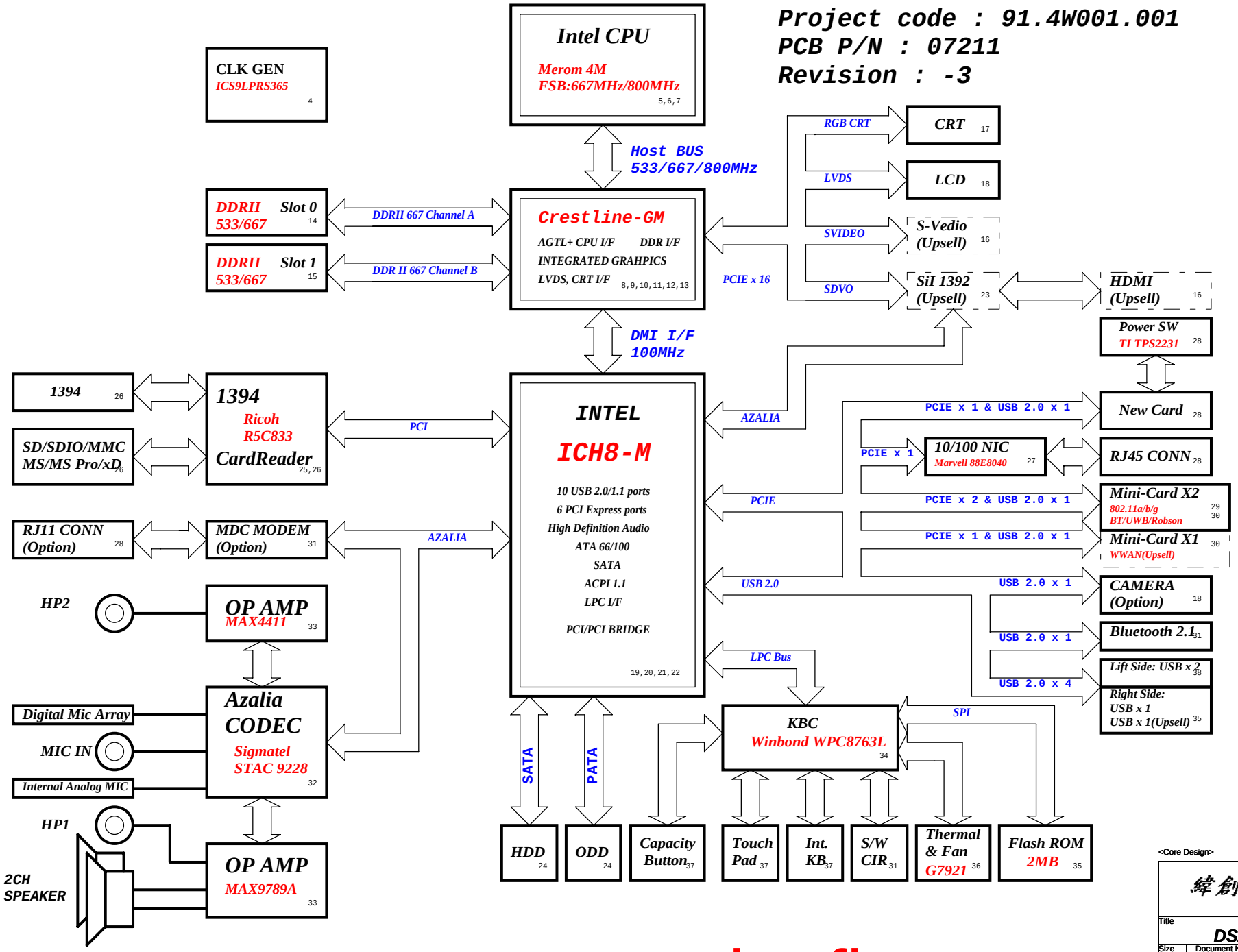
Spears Intel UMA Block Diagram 2008/02/14

Project code : 91.4W001.001
PCB P/N : 07211
Revision : -3



CPU DC/DC ISL6262A 41, 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC TPS5117 43, 44	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC TPS51120 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51100 45	
INPUTS	OUTPUTS
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

SYSTEM DC/DC LDO 45	
INPUTS	OUTPUTS
3D3V_S0	2D5V_S0
1D8V_S3	1D5V_S0
1D8V_S4	1D25V_S0

MAXIM CHARGER MAX8731A 39	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DS2 System Block Diagram

Size	Document Number	Rev
A3	Spears-Intel	-3

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CPU_CORE
ISL6262A

VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
VROK(O)
CLK_EN#(O)

Output Power
VCC_CORE_PWR(O)

VRPWRGD
CLK_EN#
VCC_CORE_S0(Imax=35A)

TI TPS51120
3D3V/5V

3V/5V_EN
DCBATOUT
DCBATOUT
5V_AUX_S5

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Input Power
VIN
V5FILT(I / 5V)

Output Signal
PGOUT1(OD / 5V)
PGOUT2(OD / 3D3V)

Output Power
5V(O)
3D3V(O)

CPUCORE_ON(Pull High 3D3V)
5V_AUX_S5
3D3V_AUX_S5
5V_S5 (6A)
3D3V_S5 (5A)

1D5V_S0

5V_S0
1D8V_S3
PM_SLP_S3#

VCNTL
VIN
EN
VOUT(O)
POK

1D5V_S0
CPUCORE_ON

G971

2D5V_S0

3D3V_S0
INPUT
OUT
2D5V_S0

G9131

1D25V_S0

5V_S0
1D8V_S3
PM_SLP_S3#

VCNTL
VIN
EN
VOUT(O)
POK

1D25V_S0
CPUCORE_ON

G966

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VIN(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN
AD+

Charger_MAX8731A

CHARGE_OFF
BAT+SENSE
BT_SCL
BT_SDA
AC_IN
AD+

Input Signal
CLS (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
PB0/MOSI/AIN0

Input Power
DCIN (I)

Output Signal
LDO (O / 5.4V)
(O)
(O)

Output Power
VCC (O)
VCC (O)

MAX8731_LDO
ACAV_IN
AC_IN#
DCBATOUT
BT+

TI TPS51100
0.9V/DDR_VREF_S3

PM_SLP_S4#
PM_SLP_S3#
5V_S5
1D8V_S3

Input Signal
S5
S3

Input Power
VCC(I)
VIN(I)

Output Power
VCC(O)
VCC(O)

DDR_VREF_S3
DDR_VREF_S0

TPS51117_1D8V_S3

PM_SLP_S4#
5V_S5
DCBATOUT

Input Signal
EN_PSV(I / 5V)

Input Power
VCC
VIN

Output Signal
PGOUT(OD / 5V)

Output Power
1D8V_PWR

CPUCORE_ON
1D8V_S3

TPS51117_1D05V

PM_SLP_S3#
5V_S5
DCBATOUT

Input Signal
EN_PSV(I / 5V)

Input Power
VCC
VIN

Output Signal
PGOUT(OD / 5V)

Output Power
1D05V_PWR

CPUCORE_ON
1D05V_S0 (15A)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 2 of 50

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD/TP3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3: low = A16 swap override enable
high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN: High=Enable Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP: High=Enable Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR: LOW = Defaule
High=No Reboot

8.2K PULL HIGH

20,22 +RTCVCC → +RTCVCC
5,6,7,8,10,11,12,20,22,34,43,47 1D05V_S0 → 1D05V_S0
8,11,22,45 1D25V_S0 → 1D25V_S0
27 1D2V_LAN_S5 → 1D2V_LAN_S5
28 1D5V_NEW_S0 → 1D5V_NEW_S0
6,11,20,21,22,28,29,30,45 1D5V_S0 → 1D5V_S0
8,11,12,14,15,44,45,46,47 1D8V_S3 → 1D8V_S3
27,28 2D5V_LAN_S5 → 2D5V_LAN_S5

20,31,34,35,36,38,39,40,47 3D3V_AUX_S5 → 3D3V_AUX_S5
27,28 3D3V_LAN_S5 → 3D3V_LAN_S5
4,8,10,11,14,15,16,17,18,19,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,40,41,43,45,46,47 3D3V_S0 → 3D3V_S0
19,21,22,27,28,31,35,36,38,40,46,47 3D3V_S5 → 3D3V_S5
18,39,40,47 5V_AUX_S5 → 5V_AUX_S5

16,17,18,22,24,33,35,36,37,41,45,46,47 5V_S0 → 5V_S0
22,24,29,30,31,35,38,40,43,44,45,46,47 5V_S5 → 5V_S5
38,39,47 AD+ → AD+
18,39,40,41,42,43,44,46,47 DCBATOUT → DCBATOUT
14,15,45,47 DDR_VREF_S0 → DDR_VREF_S0
8,14,15,45 DDR_VREF_S3 → DDR_VREF_S3

18 +LCDVDD → +LCDVDD
6,7,42 VCC_CORE_S0 → VCC_CORE_S0

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reversed	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD

<Core Design>

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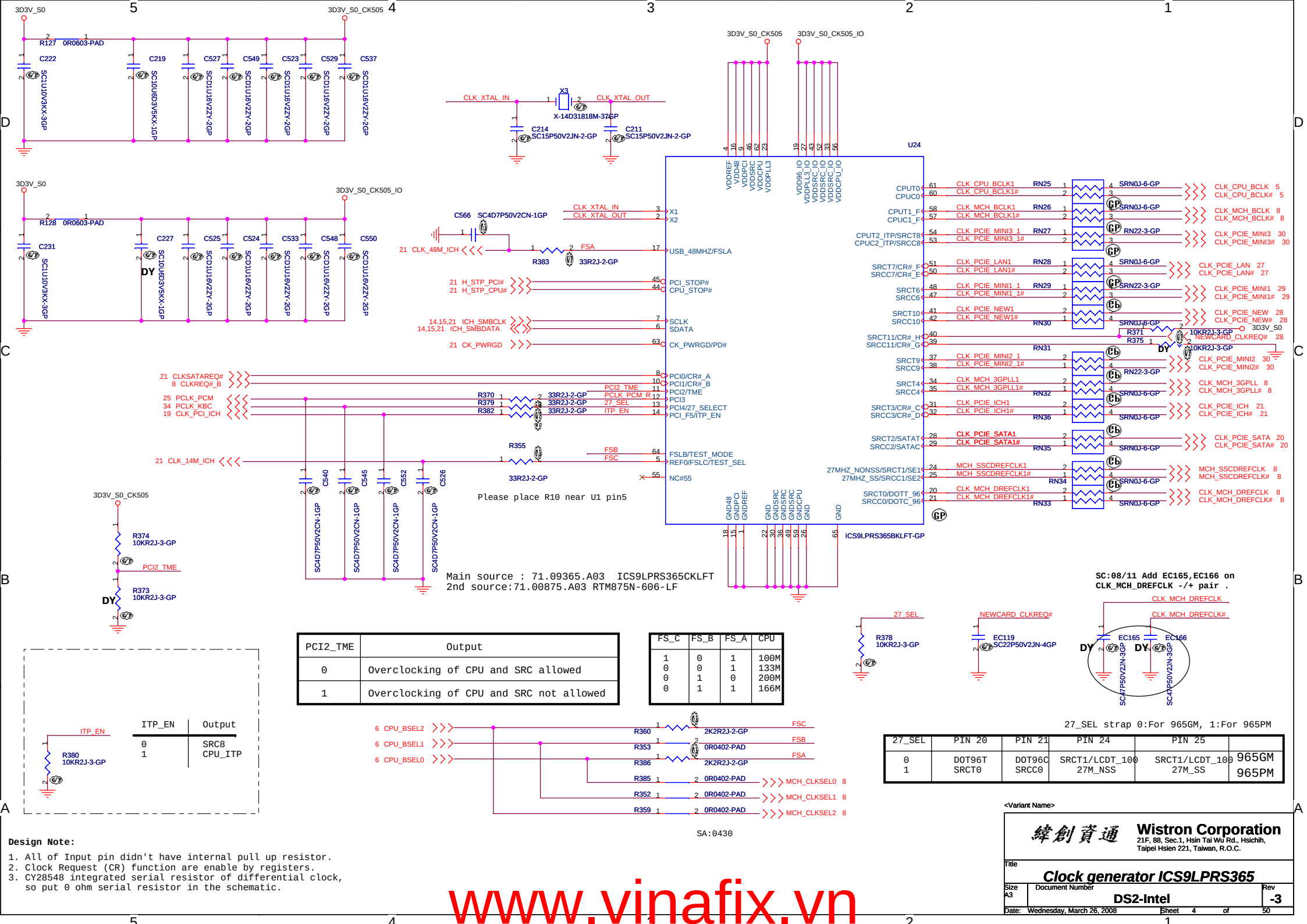

PCI2_TME	Output
0	Overclocking of CPU and SRC allowed
1	Overclocking of CPU and SRC not allowed

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

ITP_EN	Output
0	SRC8
1	CPU_ITP

27_SEL strap 0:For 965GM, 1:For 965PM

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25	
0	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100	965GM
1	SRCT0	SRCC0	27M_NSS	27M_SS	965PM

Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<variant_name>

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Title: Clock generator ICS9LPRS365

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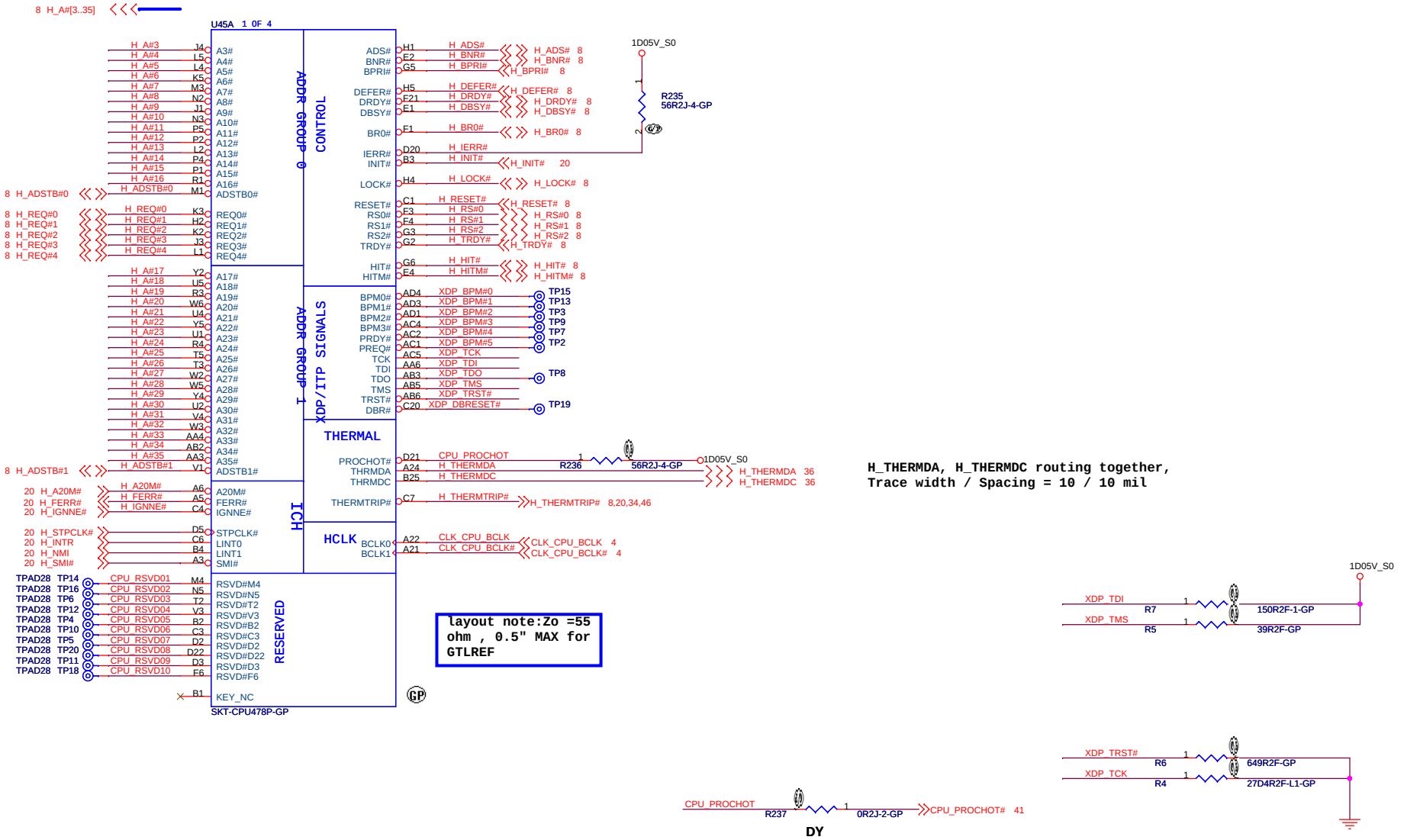

<Core Design>

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Title: Merom(1/3)-AGTL+/XDP

Size	Document Number	Rev
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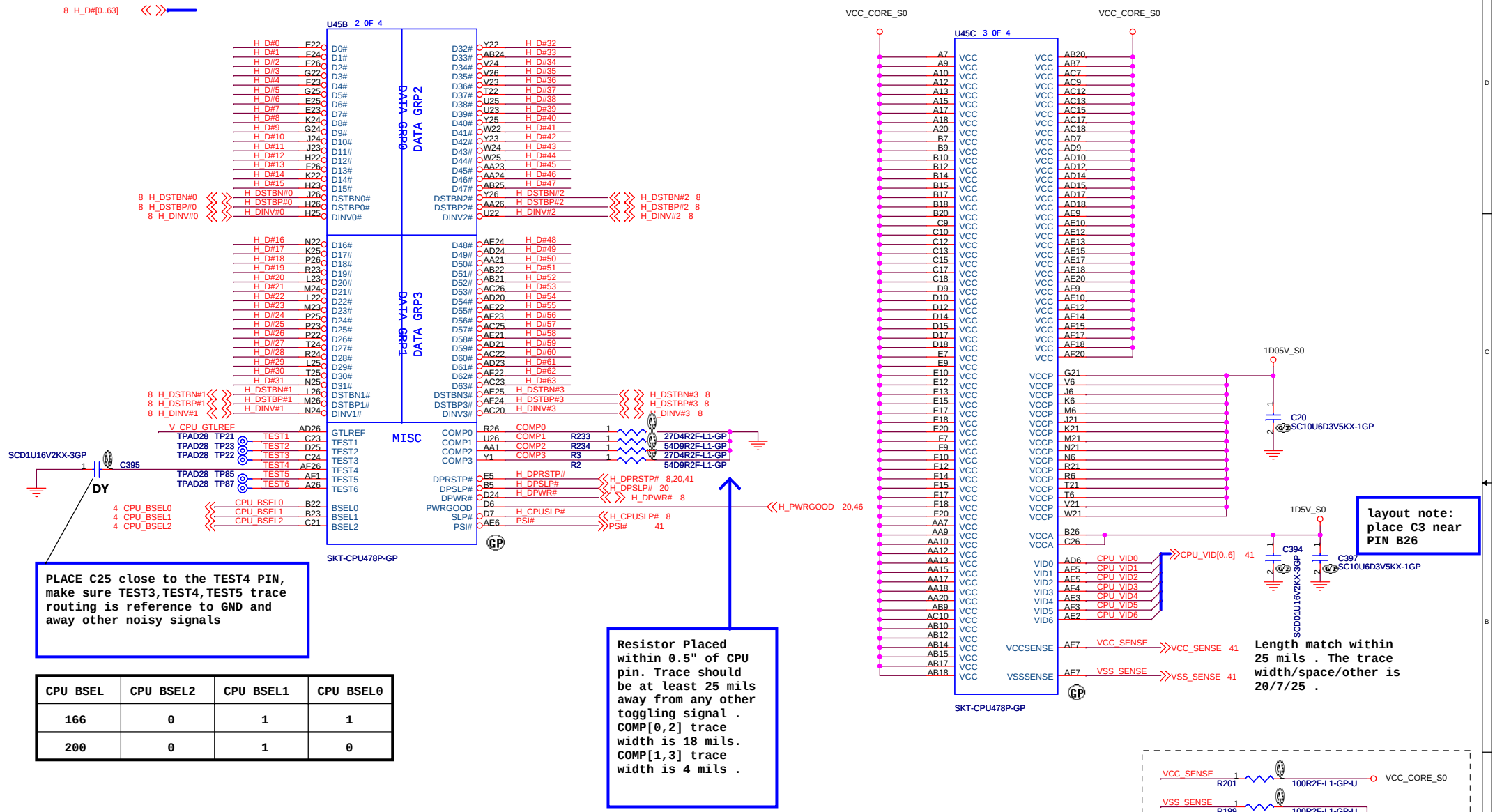

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

<Core Design>

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Title: Merom(2/3)-AGTL+/PWR

Size: A3 | Document Number: DS2-Intel | Rev: -3

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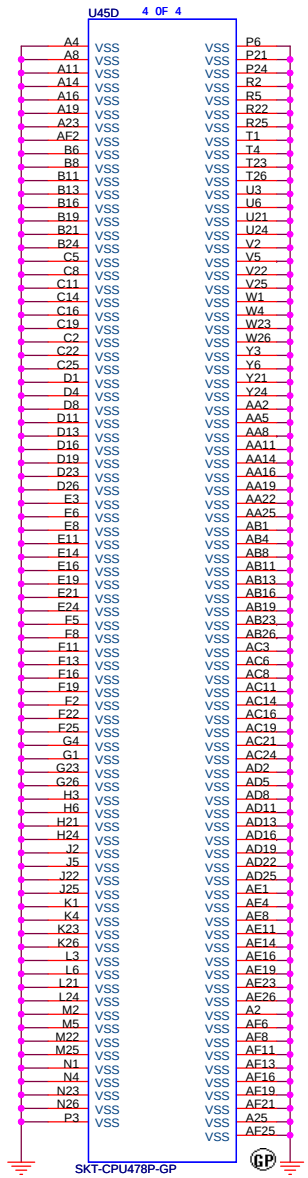

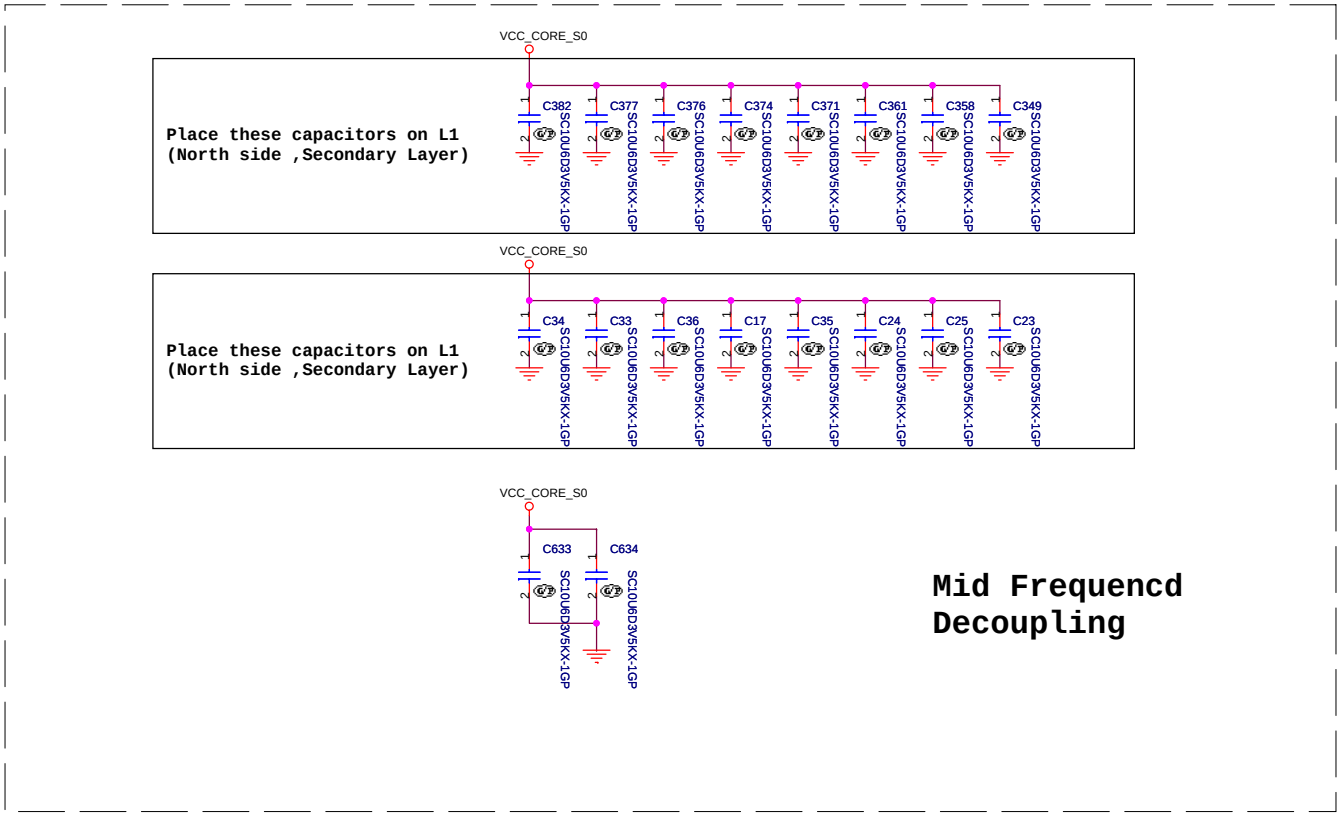

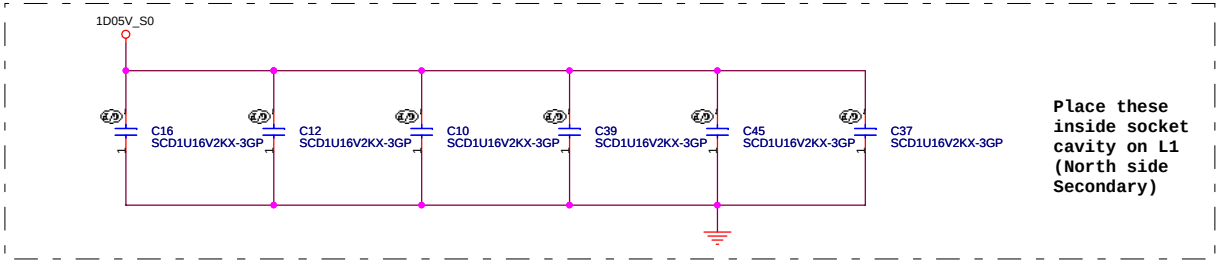

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Title: Merom(3/3)-GND&Bypass

Size: A3 | Document Number: DS2-Intel | Rev: -3

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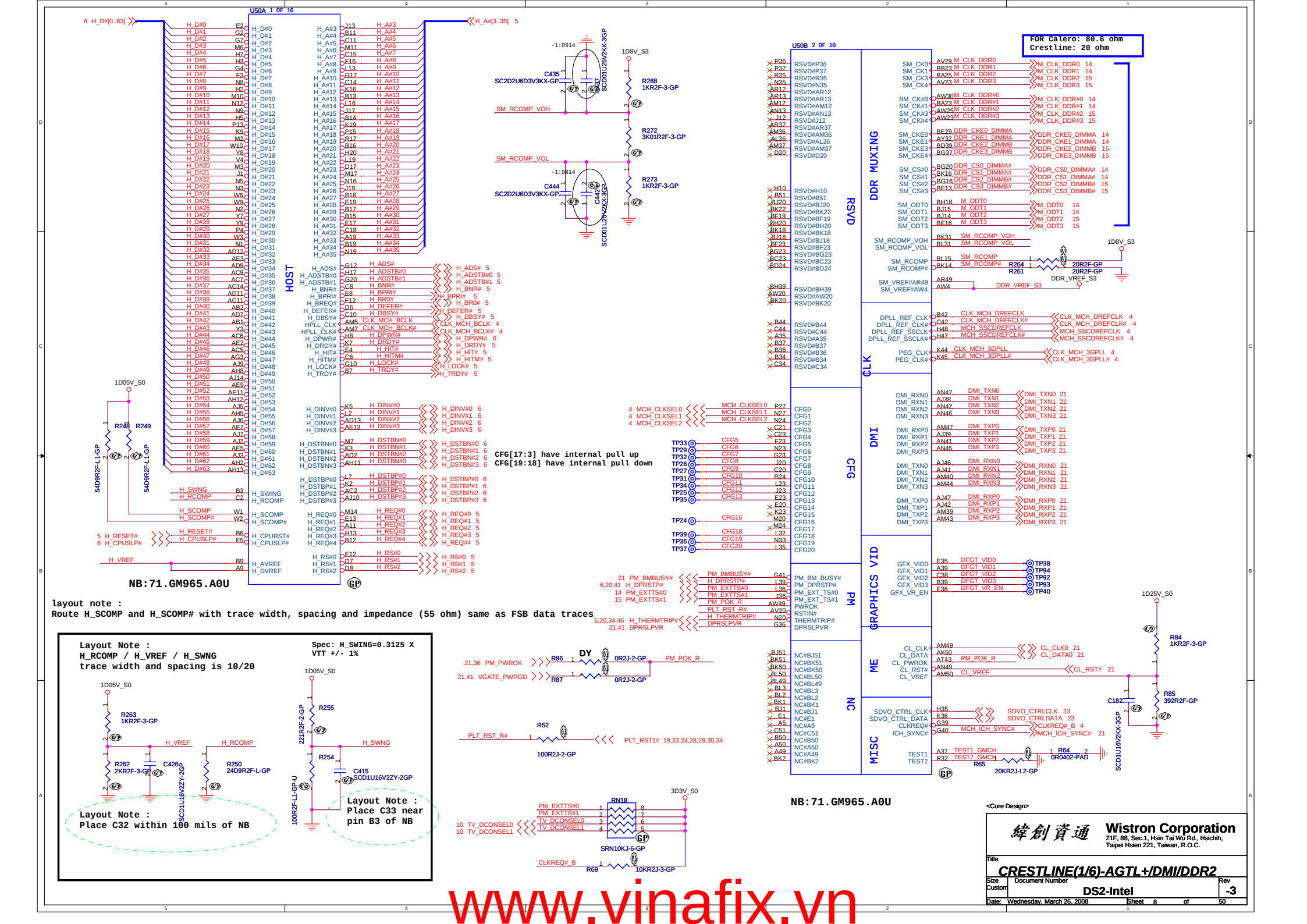

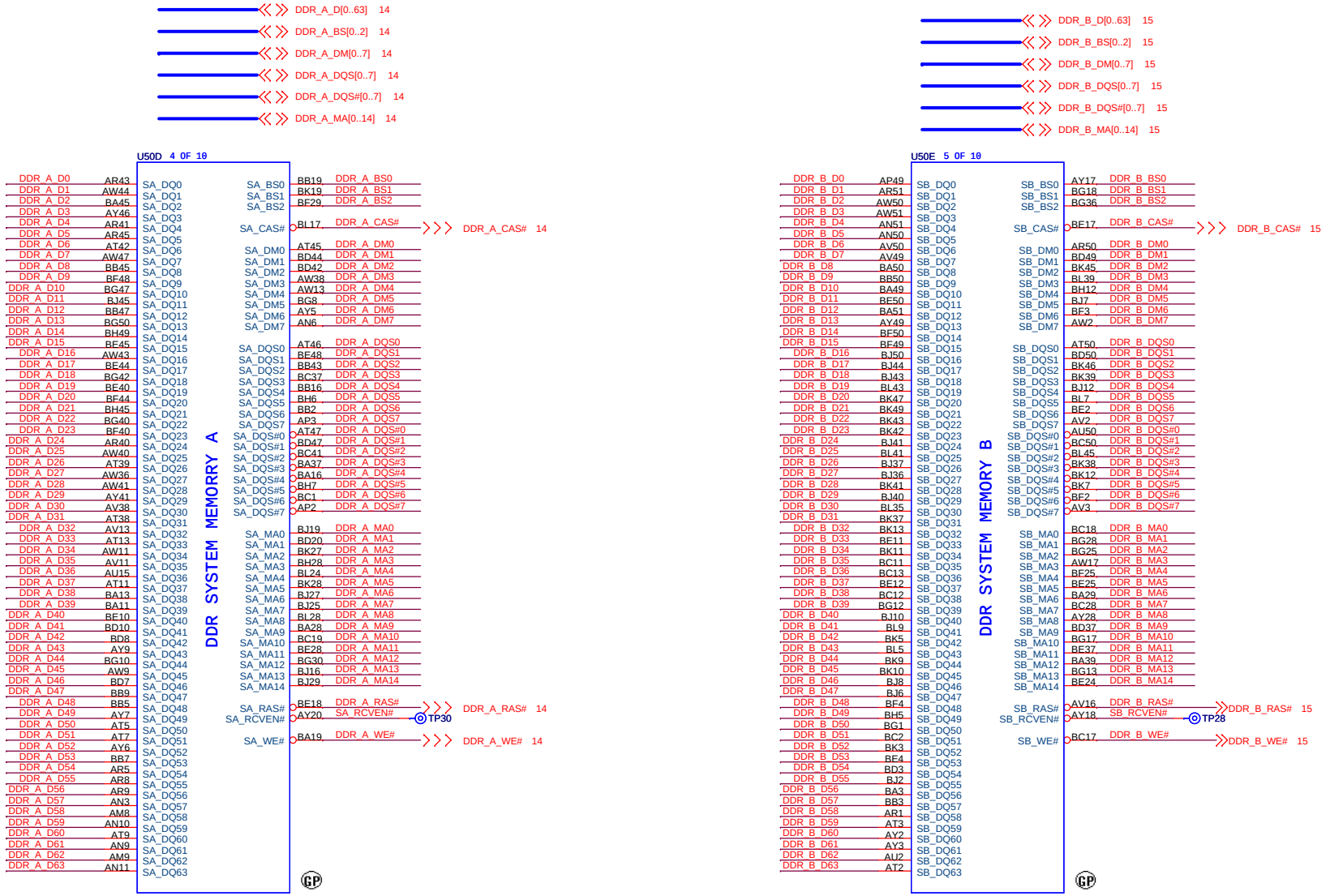

NB:71.GM965.A0U

NB:71.GM965.A0U

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Title: CRESTLINE(2/6)-DDR2 A/B CH

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For Crestline : 2.4 Kohm
For Calero : 1.5Kohm

-1:0908 Chang R68 from 64.24015.6DL to 64.33015.6DL

FOR Calero: 255 ohm
Crestline: 1.3k ohm

NB:71.GM965.A0U

PEGCOMP trace width and spacing is 20/25 mils.

Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

<Core Design>
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Title: CRESTLINE(3/6)-VGA/LVDS/TV
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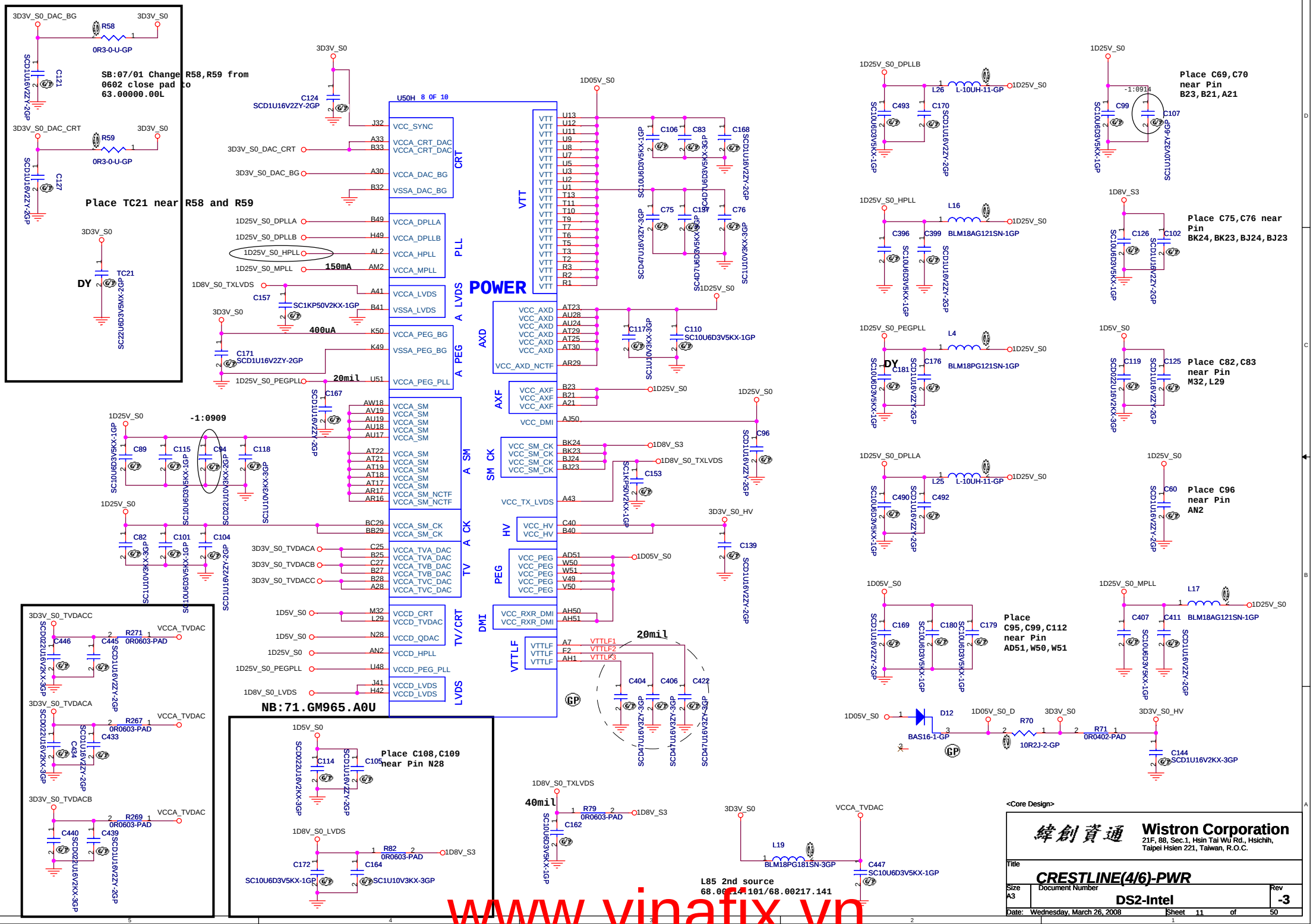
SB:07/01 Change R58,R59 from 0602 close pad to 63.00000.00L
Place TC21 near R58 and R59
POWER
U50H 8 OF 10
VCC_SYNC
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VSSA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_NCTF
VCCA_SM_CK
VCCA_TVA_DAC
VCCA_TVB_DAC
VCCA_TVC_DAC
VCCD_CRT
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
VTT
VCC_AXD
VCC_AXD_NCTF
VCC_AXF
VCC_DMI
VCC_SM_CK
VCC_TX_LVDS
VCC_HV
VCC_PEG
VCC_RXR_DMI
VTTLF
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
TV/CRT
LVDS
AXD
AXF
SM CK
HV
PEG
DMI
150mA
400uA
20mil
-1:0909
NB:71.GM965.A0U
Place C108,C109 near Pin N28
40mil
L85 2nd source
68.00814.101/68.00217.141
Place C69,C70 near Pin B23,B21,A21
Place C75,C76 near Pin BK24,BK23,BJ24,BJ23
Place C82,C83 near Pin M32,L29
Place C96 near Pin AN2
Place C95,C99,C112 near Pin AD51,W50,W51
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(4/6)-PWR
Size A3
Document Number
DS2-Intel
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Date: Wednesday, March 26, 2008
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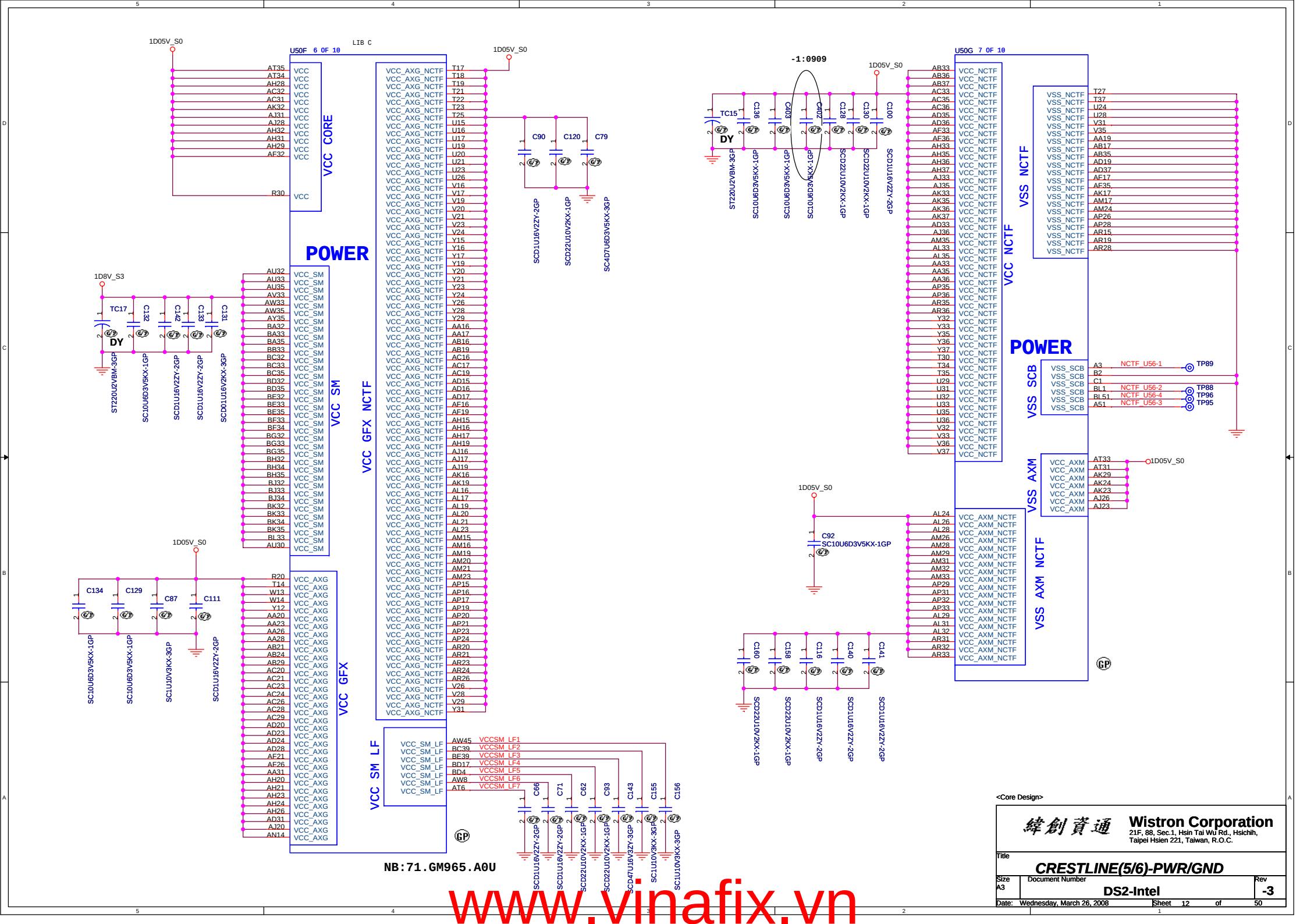
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VSS NCTF
VSS SCB
VSS AXM
VSS AXM NCTF
1D05V_S0
1D8V_S3
LIB C
U50F 6 OF 10
U50G 7 OF 10
-1:0909
NB:71.GM965.A0U
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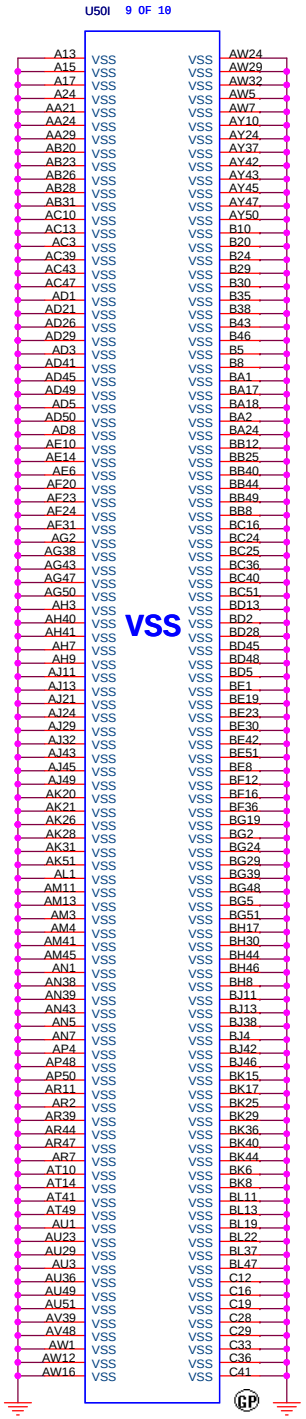
CRESTLINE(5/6)-PWR/GND
DS2-Intel
Wednesday, March 26, 2008



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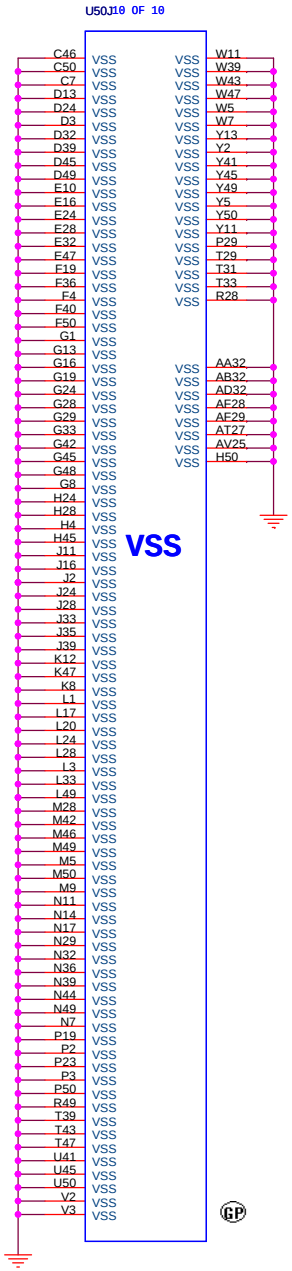

NB:71.GM965.A0U

<Core Design>

緯創資通 Wistron Corporation
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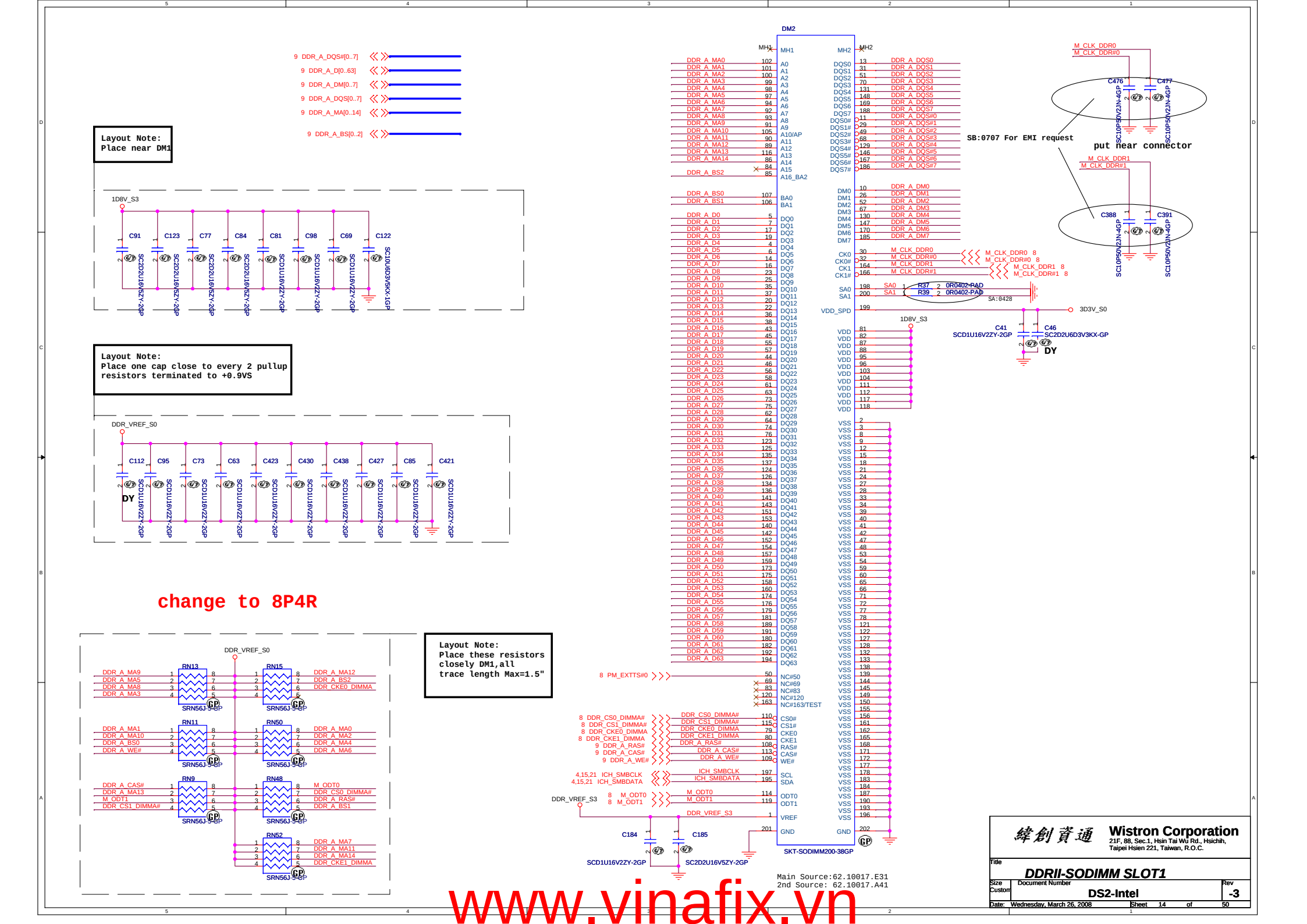
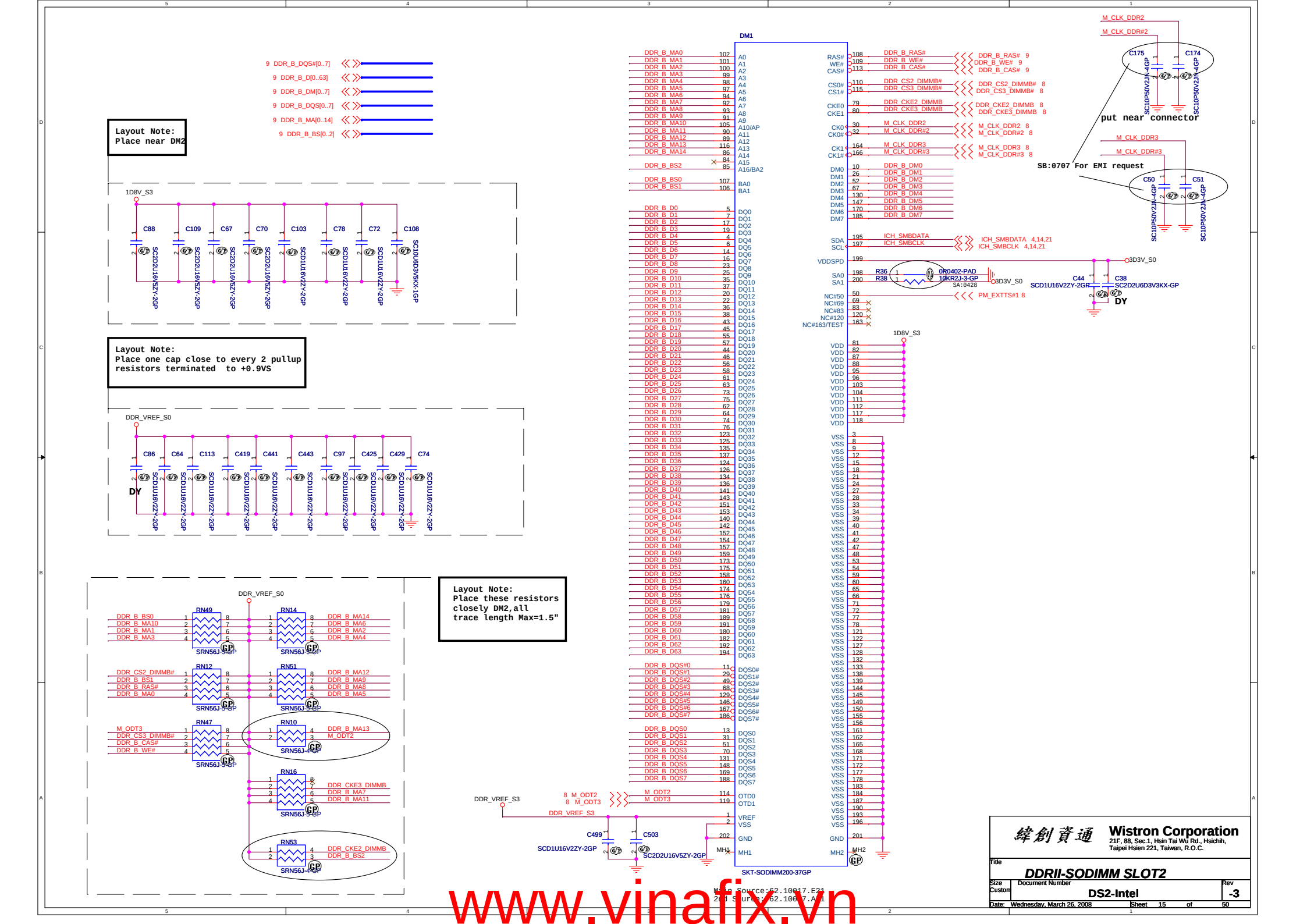
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRESTLINE(6/6)-PWR/GND

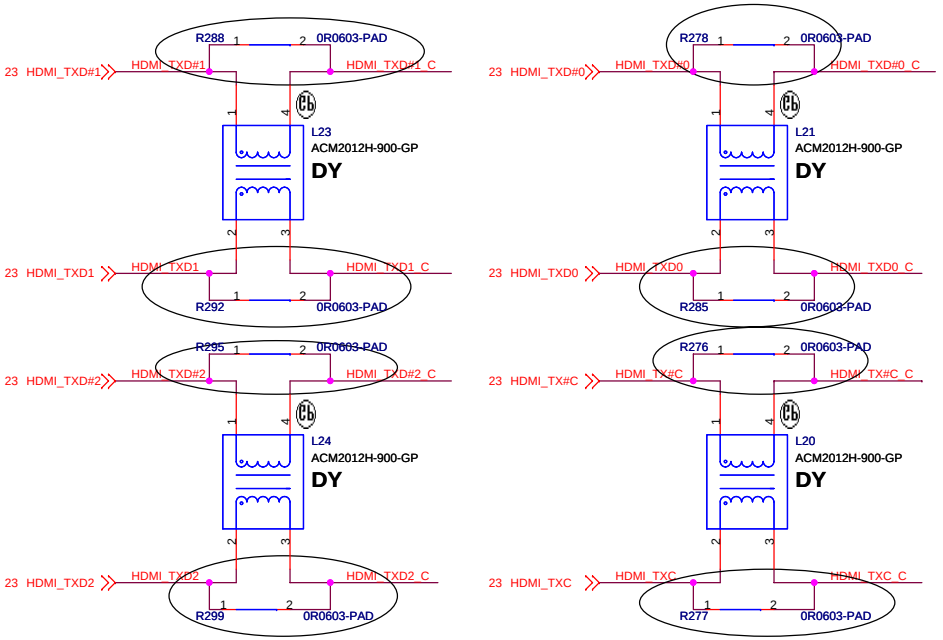
Size	Document Number	Rev
A3	DS2-Intel	-3

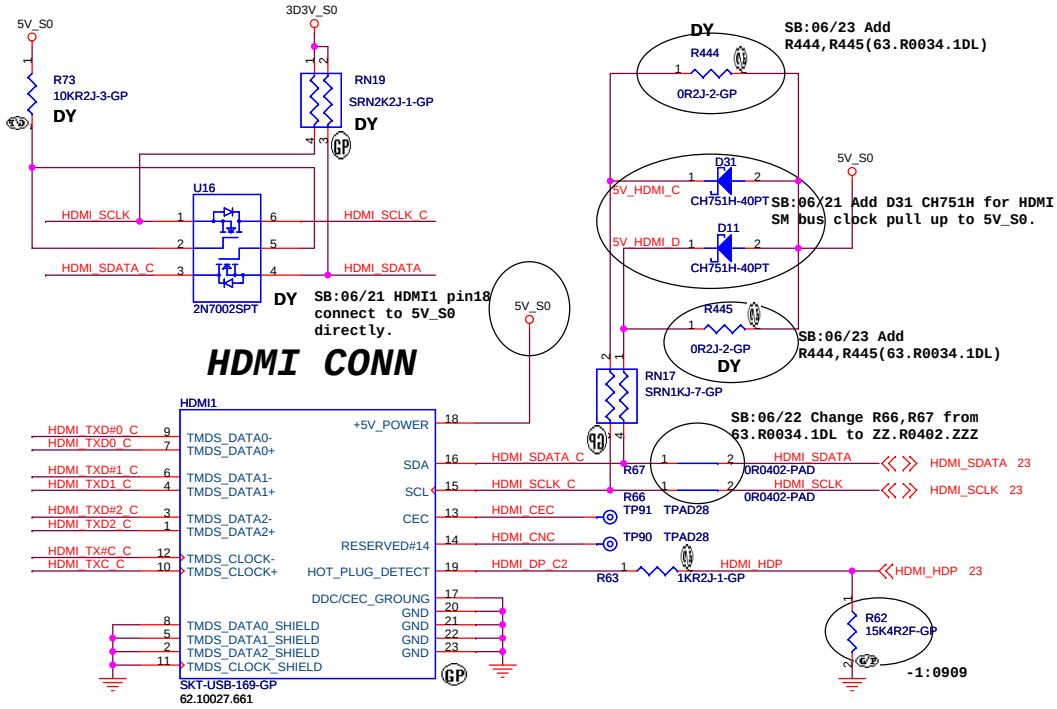
Date: Wednesday, March 26, 2008 Sheet 13 of 50




Layout Note:
Place near DM2
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS
Layout Note:
Place these resistors closely DM2,all trace length Max=1.5"
DM1
SKT-SODIMM200-37GP
put near connector
SB:0707 For EMI request
DDR_VREF_S0
DDR_VREF_S3
1D8V_S3
3D3V_S0
DY
DDR_B_DQS#[0..7]
DDR_B_D[0..63]
DDR_B_DM[0..7]
DDR_B_DQS[0..7]
DDR_B_MA[0..14]
DDR_B_BS[0..2]
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
ICH_SMBDATA 4,14,21
ICH_SMBCLK 4,14,21
PM_EXTTS#1 8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDRII-SODIMM SLOT2
DS2-Intel
-3
Wednesday, March 26, 2008
15
50
www.vinafix.vn

HDMI I/F & CONNECTOR





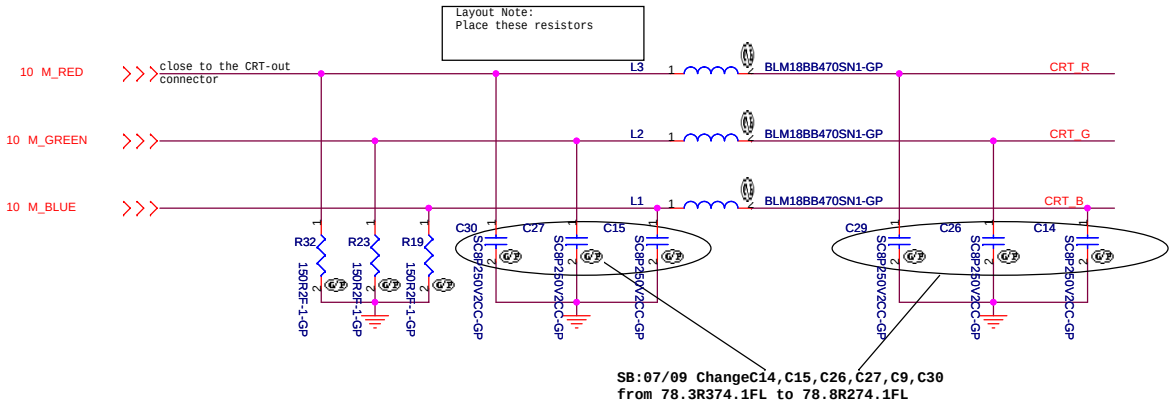
TV OUT CONN (Optional) Move to Right I/O Board

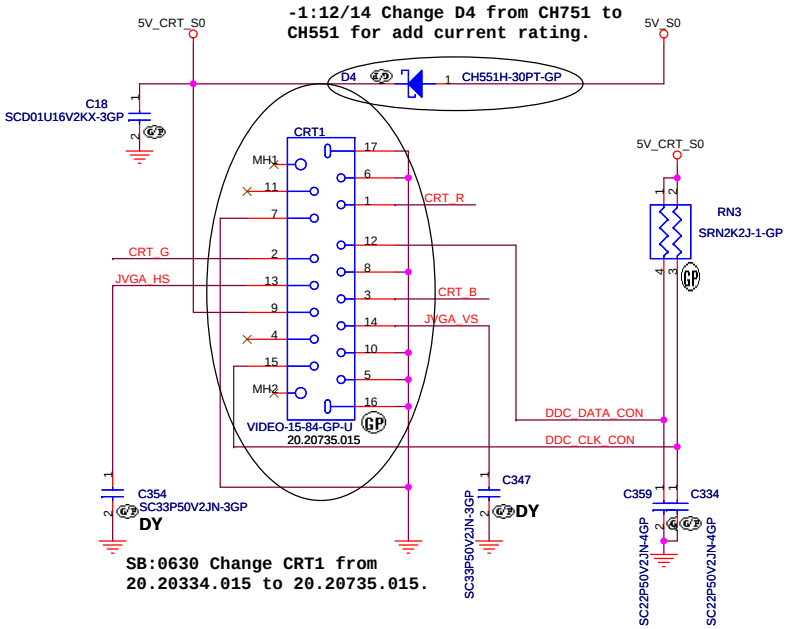
<Core Design>

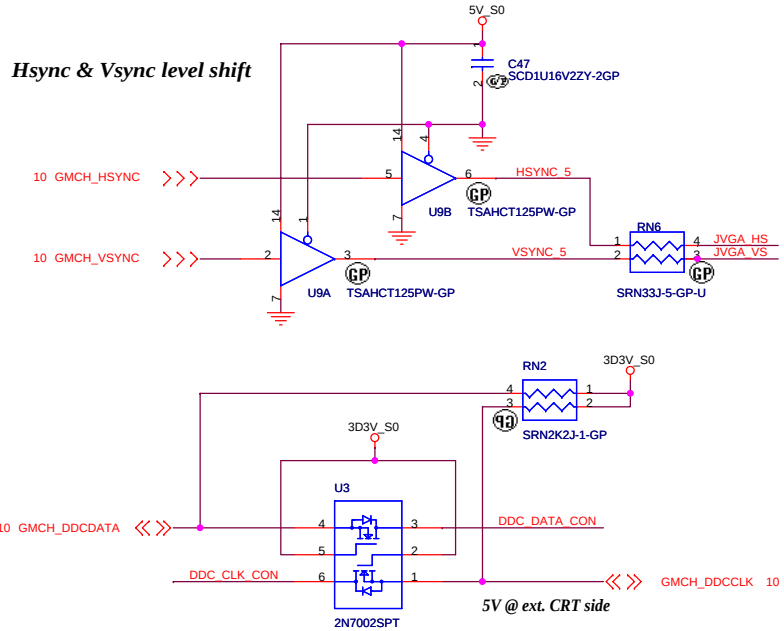
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

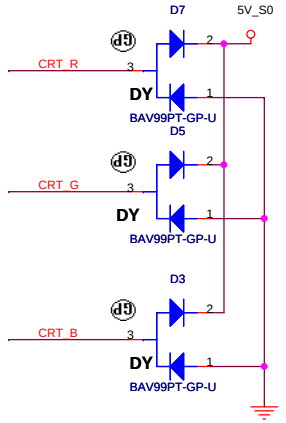
Title: HDMI/TV Connector
Size: A3
Document Number: DS2-Intel
Rev: -3
Date: Wednesday, March 26, 2008
Sheet 16 of 50

CRT I/F & CONNECTOR









<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size	Document Number	Rev
A3	DS2-Intel	-3

Date: Wednesday, March 26, 2008 Sheet 17 of 50

SC:08/09 Add LCD2 (20.F1093.040) ,please check LCD1 and LCD 2 layout overlap possibility.

SC:08/15 Rename "LCD2" to "LCD1"

SC:08/05 Change C57 from 78.10423.5FL to 78.10523.5BL

-1:08/29 Change LCD1 pin 31 from GND to NC

-1:09/02 Add R460 to prevent power short to GND via "LCD_CBL_DET#"

SC:08/09 Add EC161(78.10491.4FL) for EMI request .Default is DUMMY

SC:08/13 Add EC167,EC168(78.10034.1FL), R460,R461(63.R0034.1DL) place cross LVDS CLK A,Bpair. Default is DY.This is for RF request.

-1:08/29 Change LVDS channel A and channel B EMI solution. this is for antena team request.

SC:08/13 Add EC169,EC170,EC171, R462,R463,R464 on LVDS channel A each data pairs. This is for RF request .Default is DY.

Mic Power

600ohm 100MHz
200mA 0.5ohm DC

SC:08/09 Add EC154(78.10491.4FL) for EMI request .Default is DUMMY

CAMERA Power

SC:08/09 Add EC153(78.10491.4FL) for EMI request .Default is DUMMY

SC:08/09 Add EC151(78.22124.2FL) for EMI request .Default is DUMMY

SC:08/09 Add EC152(78.22124.2FL) for EMI request .Default is DUMMY

-1:0920

SC:08/09 Add EC157(78.33034.1FL) for EMI request .Default is DUMMY

SC:08/09 Add EC156(78.33034.1FL) for EMI request .Default is DUMMY

SC:08/09 Add EC155(78.33034.1FL) for EMI request .Default is DUMMY

-1:09/11

SC:08/13 Change L12 pin connection.pin 1 connect to "USB_PN6", pin4 connect to "USB_PP6" . This change is for layout request.

-1:09/11

INVERTER POWER

LCD POWER

SC:08/03 Add D32 ,R456 connect to U49 pin3 and delete R46 that are for LCD test function.

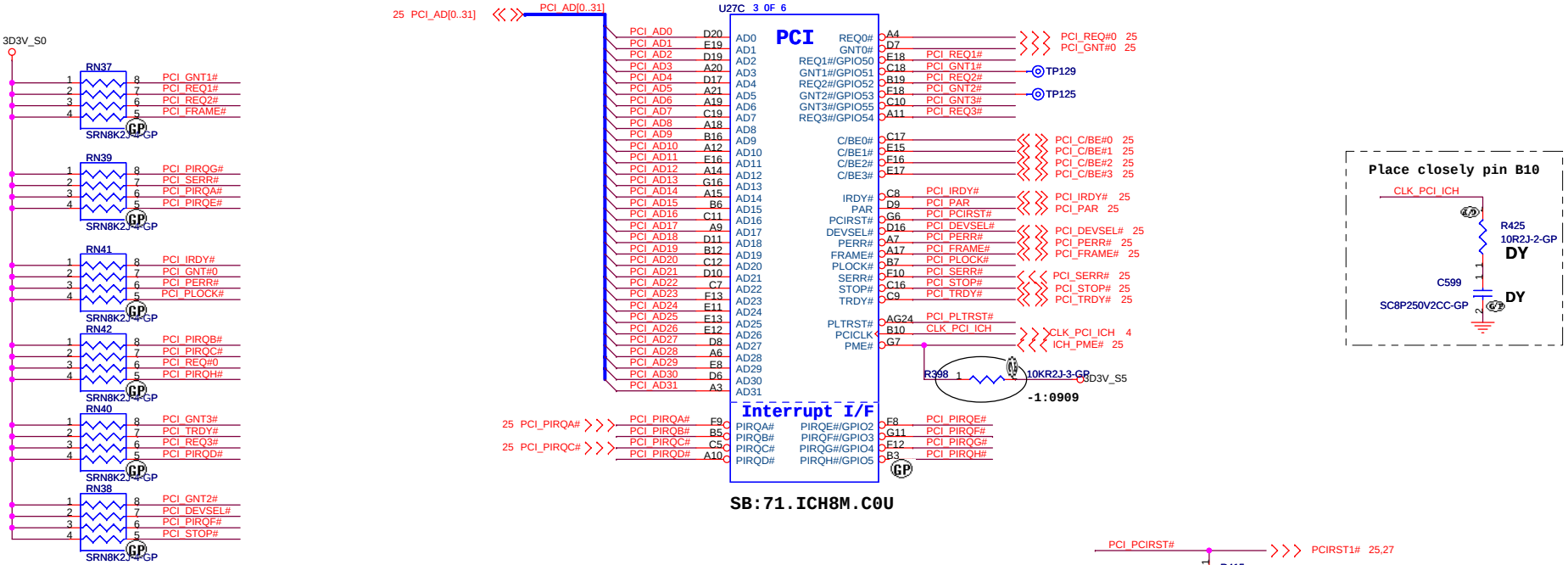
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: Custom | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 18 of 50



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *

Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 19 of 50

-1:1120 R356&R365 tolerance change from 5% to 1% for S3 resume issue.

-1:1120 R356&R365 tolerance change from 5% to 1% for S3 resume issue.

+RTCVCC

R365 330KR2F-L-GP LAN100_SLP

R364 1MR2J-1-GP SM_INTRUDER#

R356 330KR2F-L-GP ICH_INTVRMEN

+RTCVCC

R120 20KR2J-L2-GP

C205 SC1U10V3KX-3GP

G26 GAP-OPEN

U27A1 OF 6

ICH_RTCX1 AG25 RTCX1

ICH_RTCX2 AF24 RTCX2

ICH_RTCRST# AF23 RTCRST#

SM_INTRUDER# AD22 INTRUDER#

ICH_INTVRMEN AF25 INTVRMEN

LAN100_SLP AD21 LAN100_SLP

RTC

B24 GLAN_CLK

D22 LAN_RSTSYNC

C21 LAN_RXD0

B21 LAN_RXD1

C22 LAN_RXD2

D21 LAN_TXD0

E20 LAN_TXD1

C20 LAN_TXD2

AH21 GLAN_DOCK#/GPIO13

D25 GLAN_COMPI

C25 GLAN_COMPO

LAN/GLAN

1D5V_S0

R414 24D9R2F-L-GP

GLAN_COMP

-2:0920

32 ICH_AZ_CODEC_BITCLK R344 33R2J-2-GP

23,31 ICH_ACZ_MDC_BITCLK R343 33R2J-2-GP

23,31,32 ICH_AZ_CODEC_SYNC R348 33R2J-2-GP

31 ICH_AZ_MDC_RST#

23 ICH_AZ_S1392_RST#

32 ICH_AZ_CODEC_RST#

R368 R367 R366 33R2J-2-GP

HDA_BITCLK_R

HDA_SYNC

HDA_RST#

AJ16 HDA_BIT_CLK

AJ15 HDA_SYNC

AE14 HDA_RST#

31 ICH_SDIN_MDC

23 ICH_SDIN_S1392

32 ICH_SDIN_CODEC

AJ17 HDA_SDIN0

AH17 HDA_SDIN1

AH15 HDA_SDIN2

AD13 HDA_SDIN3

IHDA

23,31,32 ICH_SDOUT_CODEC R363 33R2J-2-GP

HDA_SDOUT

AE13 HDA_SDOUT

G62 GAP-OPEN

AE10 HDA_DOCK_EN#/GPIO33

AG14 HDA_DOCK_RST#/GPIO34 TP101

35 SATA_LED# AF10 SATALED#

24 SATA_RXN0_C

24 SATA_RXP0_C

C520 SC3900P50V2KX-2GP SATA_TXN0_C

C521 SC3900P50V2KX-2GP SATA_TXP0_C

24 SATA_TXN0

24 SATA_TXP0

AF6 SATA0RXN

AF5 SATA0RXP

AH5 SATA0TXN

AH6 SATA0TXP

AG3 SATA1RXN

AG4 SATA1RXP

AJ4 SATA1TXN

AJ3 SATA1TXP

AF2 SATA2RXN

AF1 SATA2RXP

AE4 SATA2TXN

AE3 SATA2TXP

SATA

4 CLK_PCIE_SATA#

4 CLK_PCIE_SATA

R119 24D9R2F-L-GP

Within 500 mils

AB7 SATA_CLKN

AC6 SATA_CLKP

AG1 SATARBIAS#

AG2 SATARBIAS

LPC_LAD[0..3] 34

FWH0/LAD0 E5 LPC_LAD0

FWH1/LAD1 E5 LPC_LAD1

FWH2/LAD2 G8 LPC_LAD2

FWH3/LAD3 F6 LPC_LAD3

FWH4/LFRAME# C4 LPC_LFRAME# LPC_LFRAME# 34

LDRQ0# G9 LPC_DRQ0# TP123

LDRQ1#/GPIO23 E6 LPC_DRQ1# TP127

LPC

A20GATE AF13 KA20GATE 34

A20M# AG26 H_A20M# H_A20M# 5

DPRSTP# AF26 H_DPRSTP# H_DPRSTP# 6,8,41

DPSLP# AE26 H_DPSLP# H_DPSLP# 6

FERR# AD24 H_FERR# H_FERR# 5

CPUPWRGD/GPIO49 AG29 H_PWRGOOD H_PWRGOOD 6,46

IGNNE# AF27 H_IGNNE# H_IGNNE# 5

INIT# AE24 H_INIT# H_INIT# 5

INTR AC20 H_INTR 5

RCIN# AH14 KBRCIN# KBRCIN# 34

NMI AD23 H_NMI H_NMI 5

SMI# AG28 H_SMI# 5

STPCLK# AA24 H_STPCLK# H_STPCLK# 5

THRMTRIP# AE27 THRMTRIP_ICH# H_THERMTRIP# 5,8,34,46

CPU

TP8 AA23

1D05V_S0

R124 56R2J-4-GP

H_FERR#

H_DPRSTP# TP105

H_DPSLP# TP108

within 2" from R184

1D05V_S0

R123 56R2J-4-GP

R122 24R2J-GP

placed within 2" from ICH8M

IDE_PDD[0..15] 24

DD0 V1 IDE_PDD0

DD1 U2 IDE_PDD1

DD2 V3 IDE_PDD2

DD3 T1 IDE_PDD3

DD4 V4 IDE_PDD4

DD5 T5 IDE_PDD5

DD6 AB2 IDE_PDD6

DD7 T6 IDE_PDD7

DD8 T3 IDE_PDD8

DD9 R2 IDE_PDD9

DD10 T4 IDE_PDD10

DD11 V6 IDE_PDD11

DD12 V5 IDE_PDD12

DD13 U1 IDE_PDD13

DD14 V2 IDE_PDD14

DD15 U6 IDE_PDD15

DA0 AA4 IDE_PDA0 24

DA1 AA1 IDE_PDA1 24

DA2 AB3 IDE_PDA2 24

DCS1# Y6 IDE_PDCS1# 24

DCS3# Y5 IDE_PDCS3# 24

DIOR# W4 IDE_PDIOR# 24

DIOW# W3 IDE_PDIOW# 24

DDACK# Y2 IDE_PDDACK# 24

IDEIRQ Y3 INT_IRQ14 24

IORDY Y1 IDE_PDIORDY 24

DDREQ W5 IDE_PDDREQ 24

IDE

SB:71.ICH8M.C0U

-1:0912

ICH_RTCX2

C203 SC12P50V2JN-3GP

CL=12.5pF

X-32D768KHZ-40GPU X1

R111 10MR2J-L-GP

C202 SC15P50V2JN-2-GP

ICH_RTCX1

-1:0920

ICH_AZ_CODEC_BITCLK

DY EC36 SC22P50V2JN-4GP

ICH_ACZ_MDC_BITCLK

C636 DY SC22P50V2JN-4GP

Please Place C636 near R454

+RTCVCC

R437 100R2J-2-GP RTCVCC_R

W=20mils W=20mils

C625 SC1U10V3ZY-6GP

U60 CH715FPT-GP

3D3V_AUX_S5

W=20mils

R438 1KR2J-1-GP BATT_R

BATT1.1

W=20mils

RTC1 BAT-CON2-U3-GP

PWR GND MH1 MH2

<Variant Name>

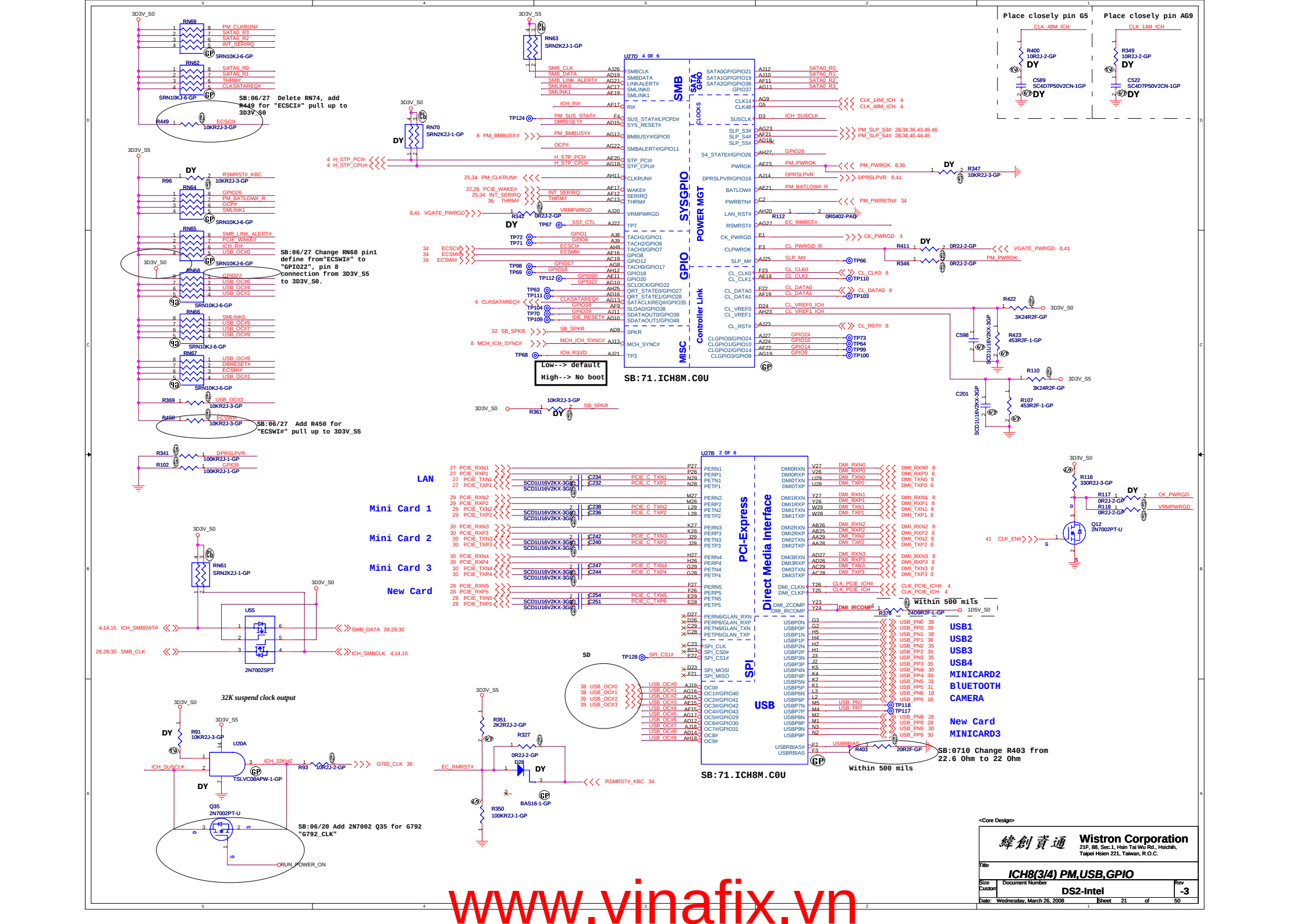
緯創資通 Wistron Corporation

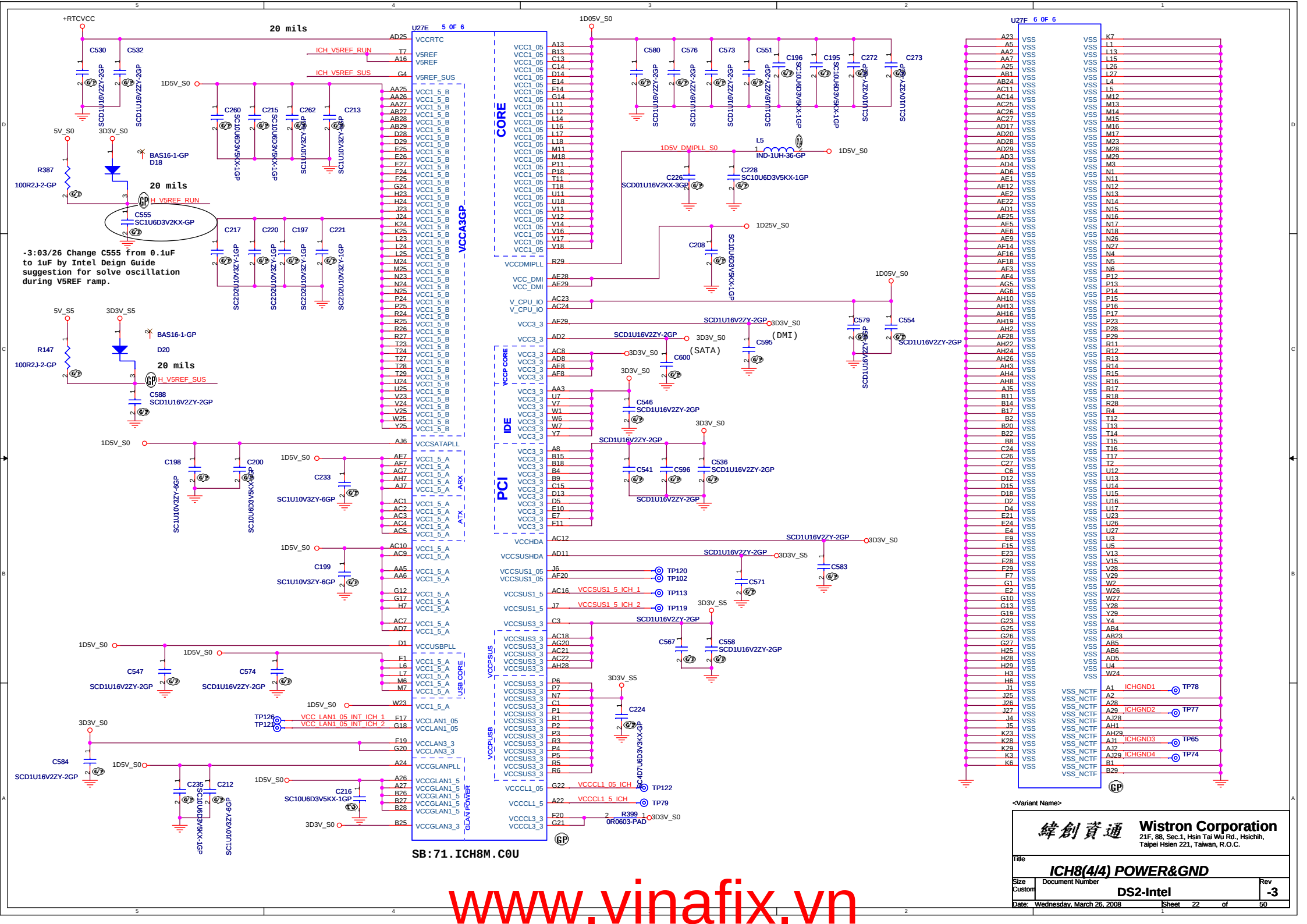
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(2/4) LAN,HD,IDE,LPC

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 20 of 50





SB:06/22 Change R279,R280,R281,R282 from 63.30134.1DL to 63.12134.1DL

SB:06/22 Change R291 from 64.75005.6DL to 64.56005.6DL

SB: 0710 Change R345 from 33 Ohm to 0 Ohm

-1:09/06 Change EC83 from ASM to DUMMY.

550mA

30mA

LAYOUT must support connectors from JAE, Molex, and Acon

<Core Design>

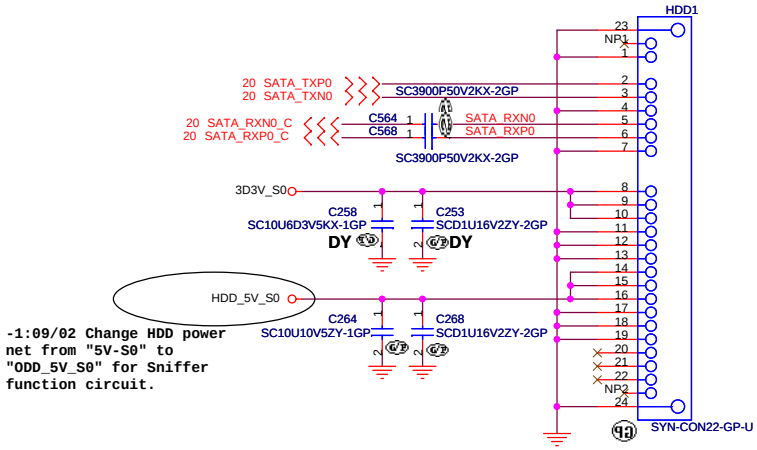
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sil 1392 HDMI

Size: A3 | Document Number: DS2-Intel | Rev: -3

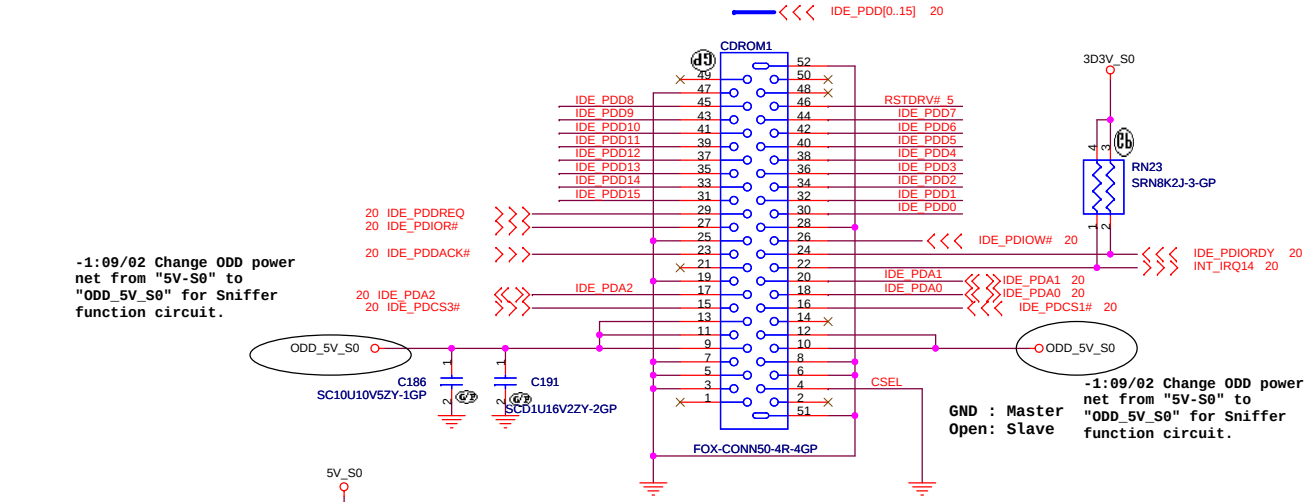
Date: Wednesday, March 26, 2008 | Sheet 23 of 50

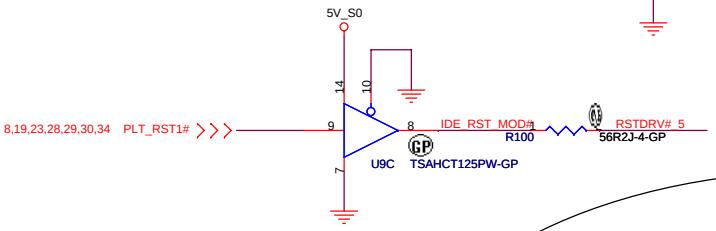
SATA HD Connector

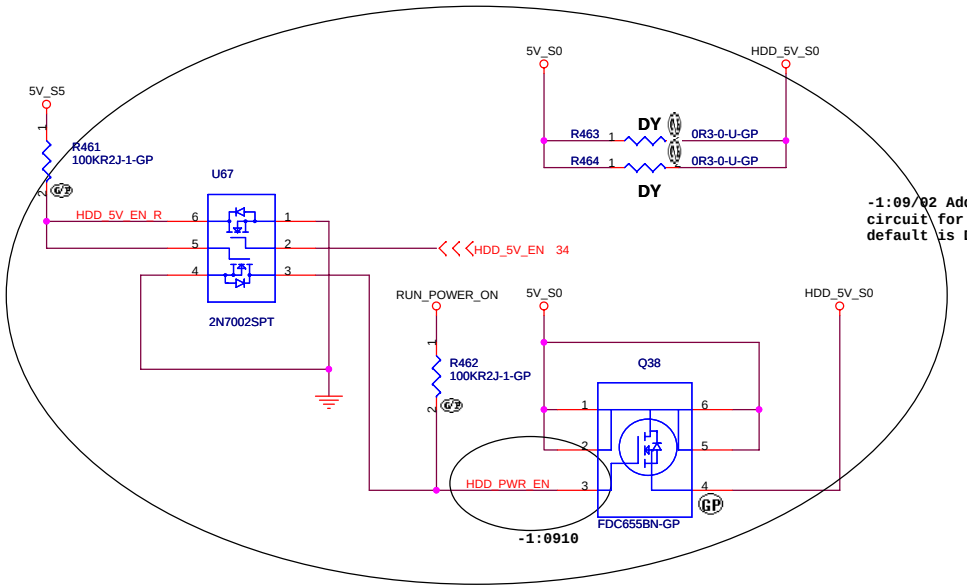


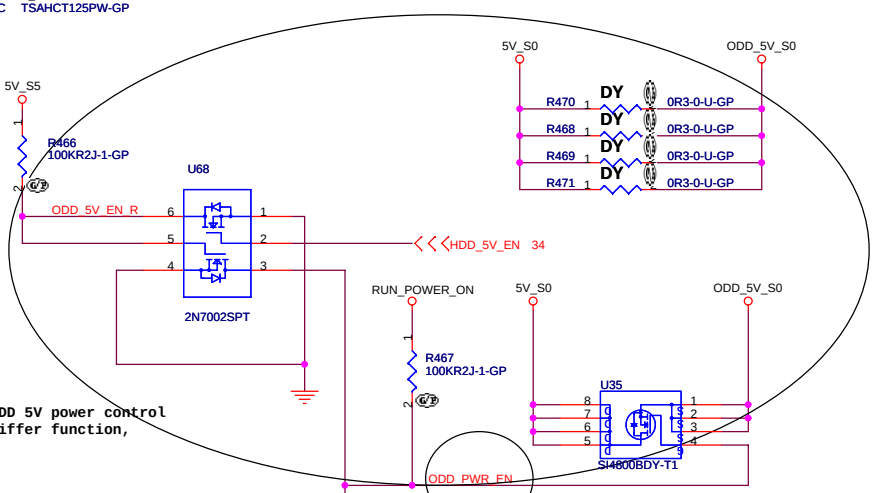
Main Source:20.80919.022

CD-ROM Connector

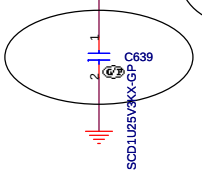








-1:0906 Add C639 for "ODD_5V_EN#".
-1:1114 The C639 change from NO-ASM to 0.1uF/25V for Sniffer issue.



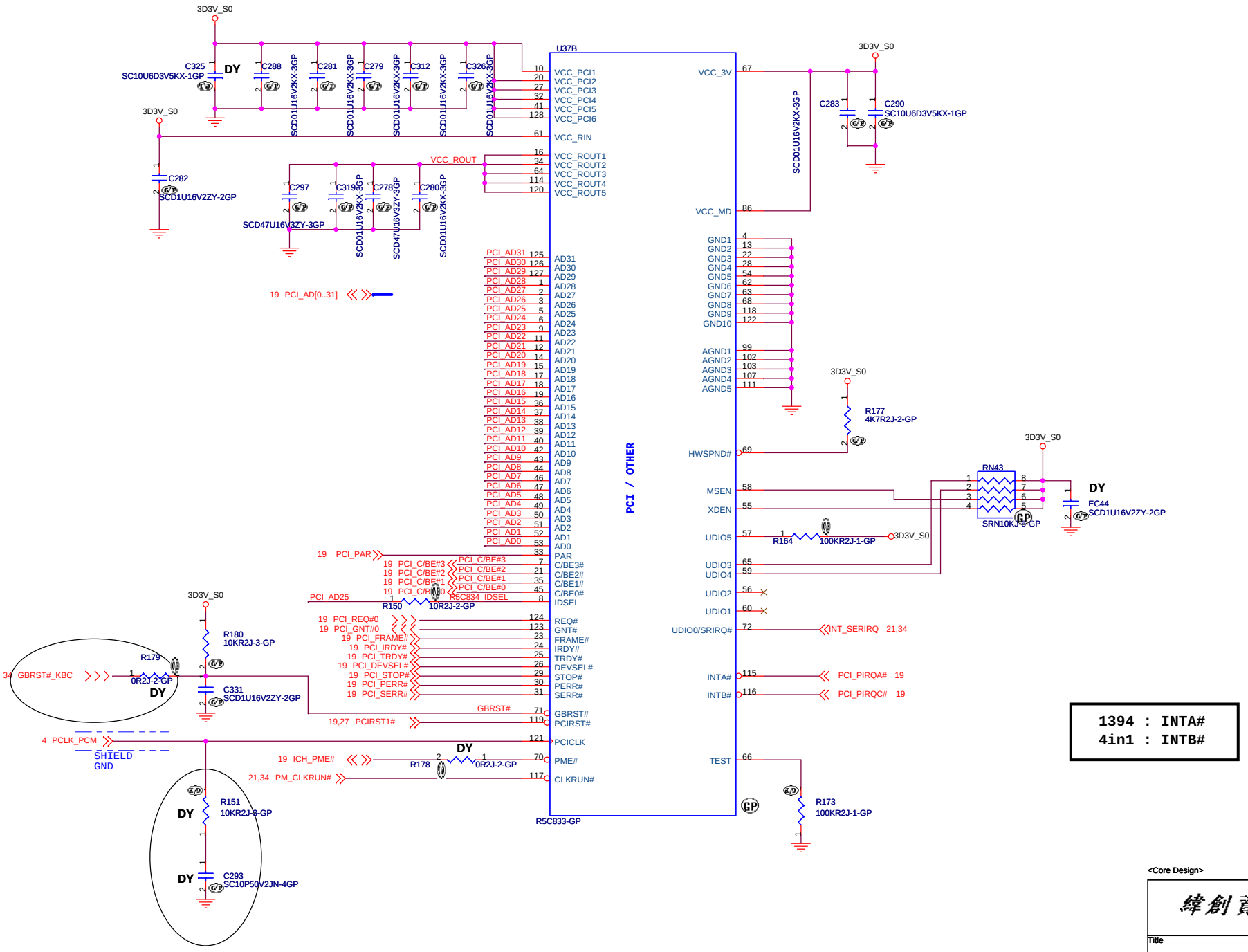
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HD/CDROM/USB

Size	Document Number	Rev
A3	DS2-Intel	-3

Date: Wednesday, March 26, 2008 Sheet 24 of 50



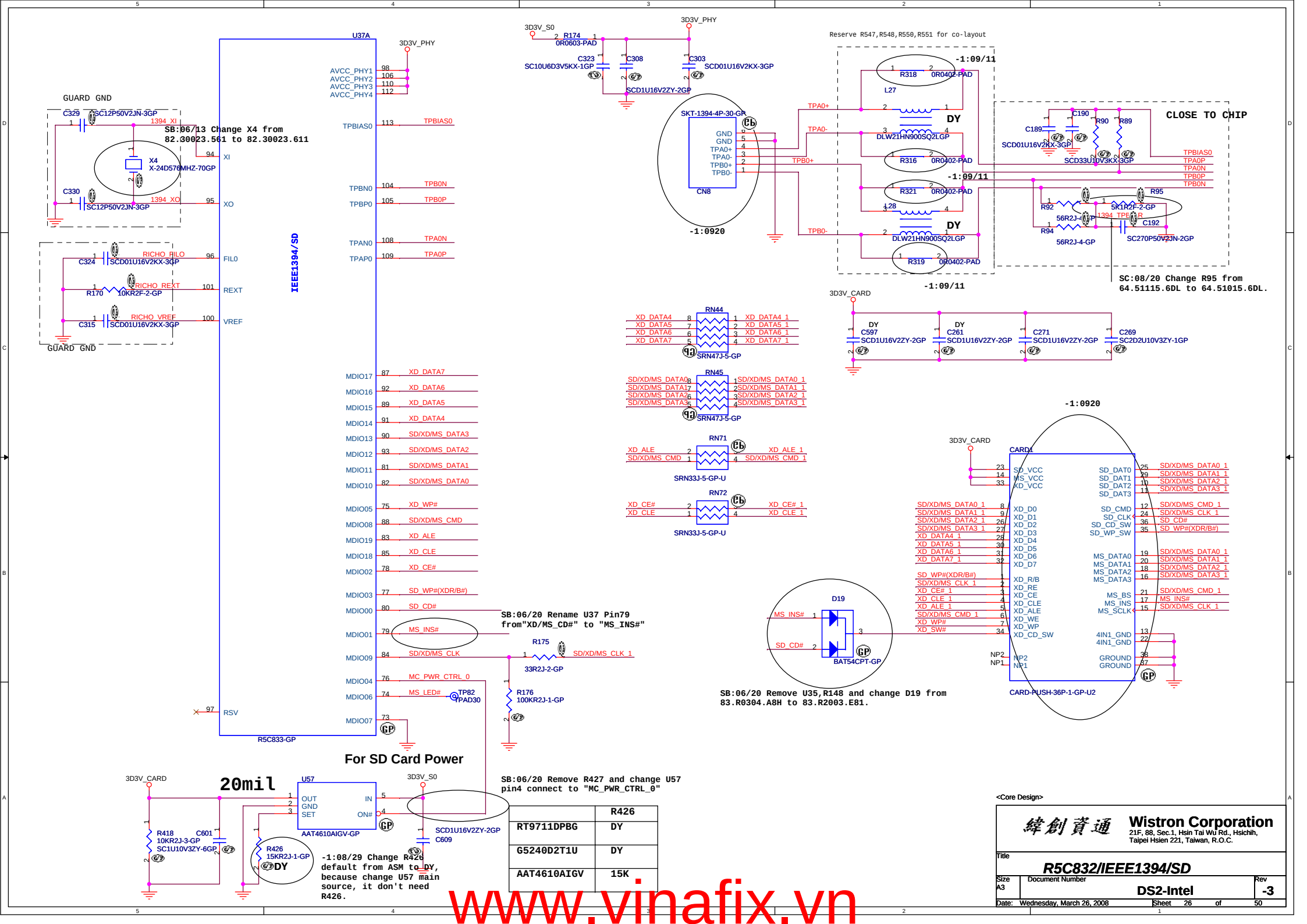
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C833/PCI

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 25 of 50



	R426
RT9711DPBG	DY
G5240D2T1U	DY
AAT4610AIGV	15K

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

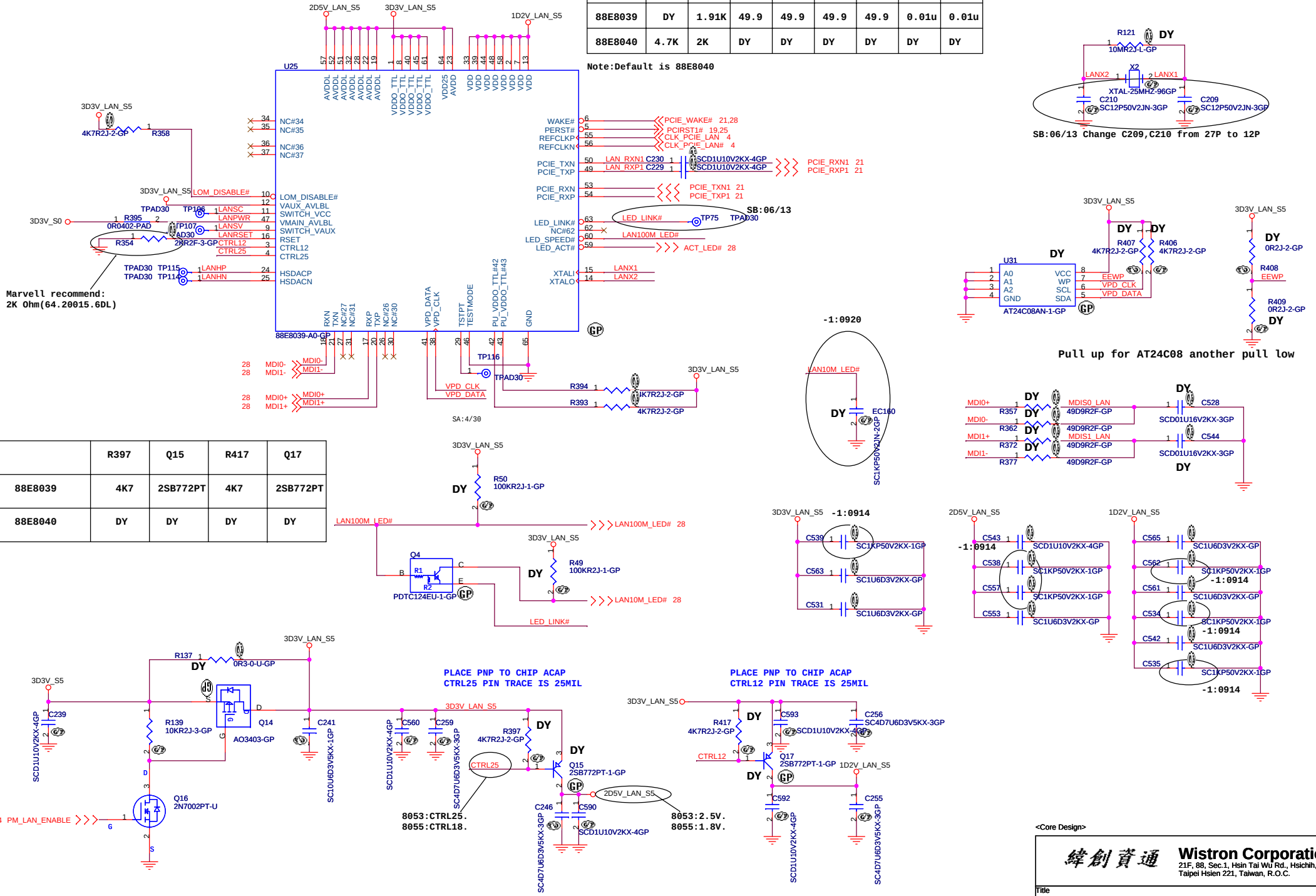
Title: R5C832/IEEE1394/SD

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 26 of 50

	R394	R354	R357	R362	R372	R377	C528	C544
88E8039	DY	1.91K	49.9	49.9	49.9	49.9	0.01u	0.01u
88E8040	4.7K	2K	DY	DY	DY	DY	DY	DY

Note:Default is 88E8040



	R397	Q15	R417	Q17
88E8039	4K7	2SB772PT	4K7	2SB772PT
88E8040	DY	DY	DY	DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

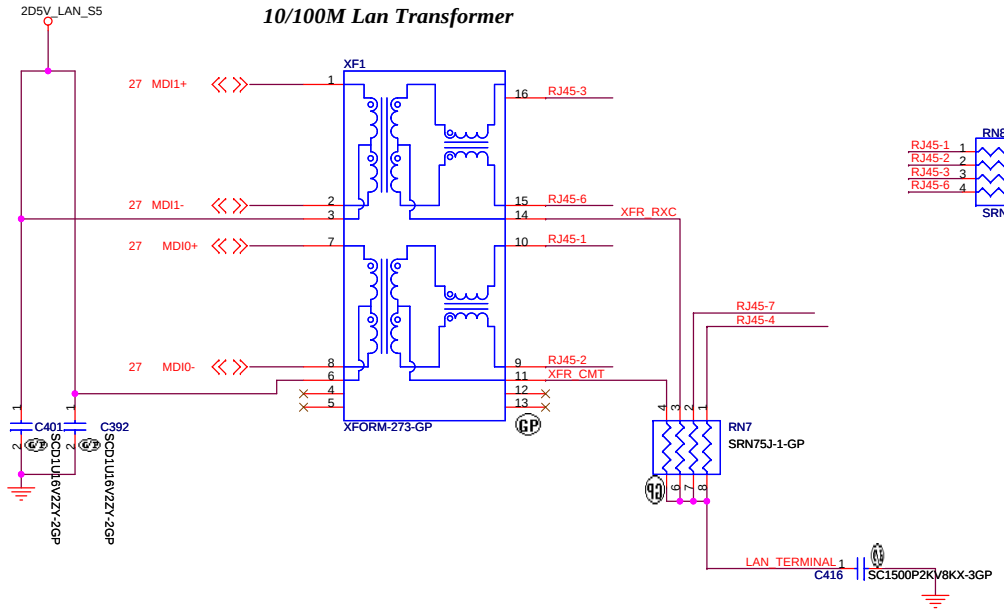
Title: LAN MARVELL

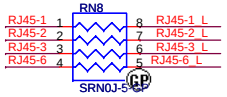
Size	Document Number	Rev
A3	DS2-Intel	-3

Date: Wednesday, March 26, 2008 Sheet 27 of 50

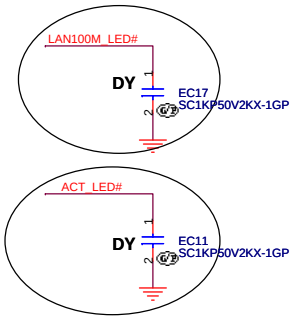
RJ45 Connector

10/100M Lan Transformer

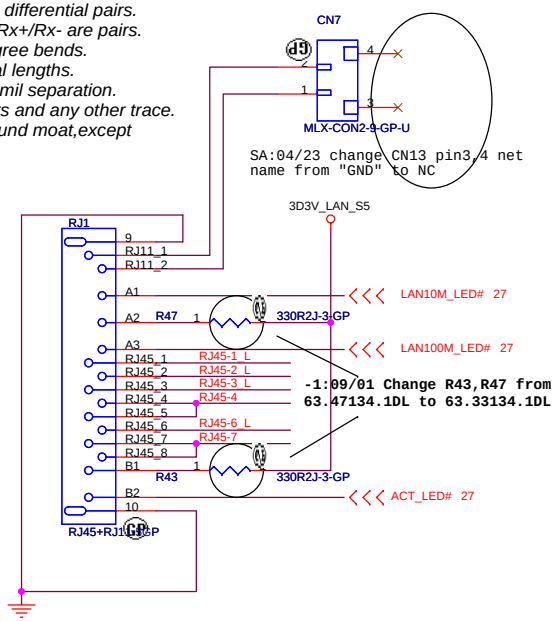




1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

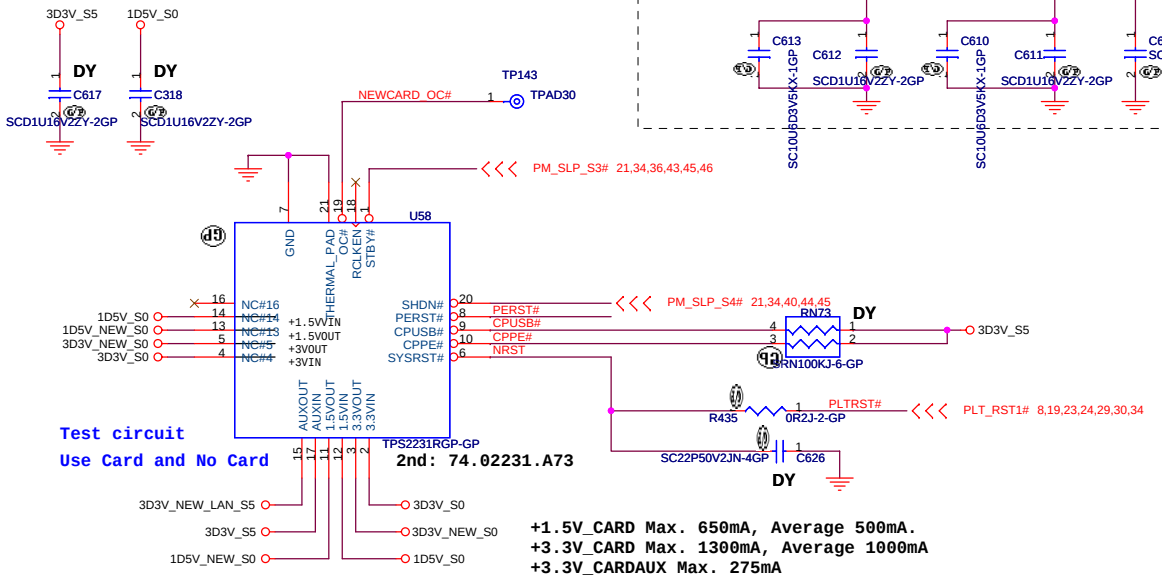


Green : Link up
Blinking : TX/RX activity

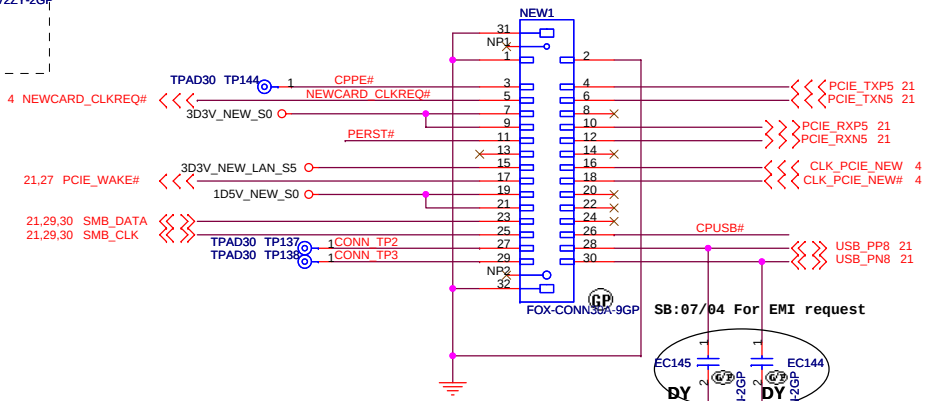


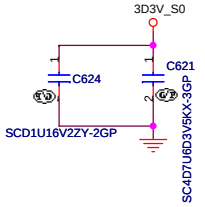
NEWCARD Connector

Place them Near to Chip



Place them Near to Connector





+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

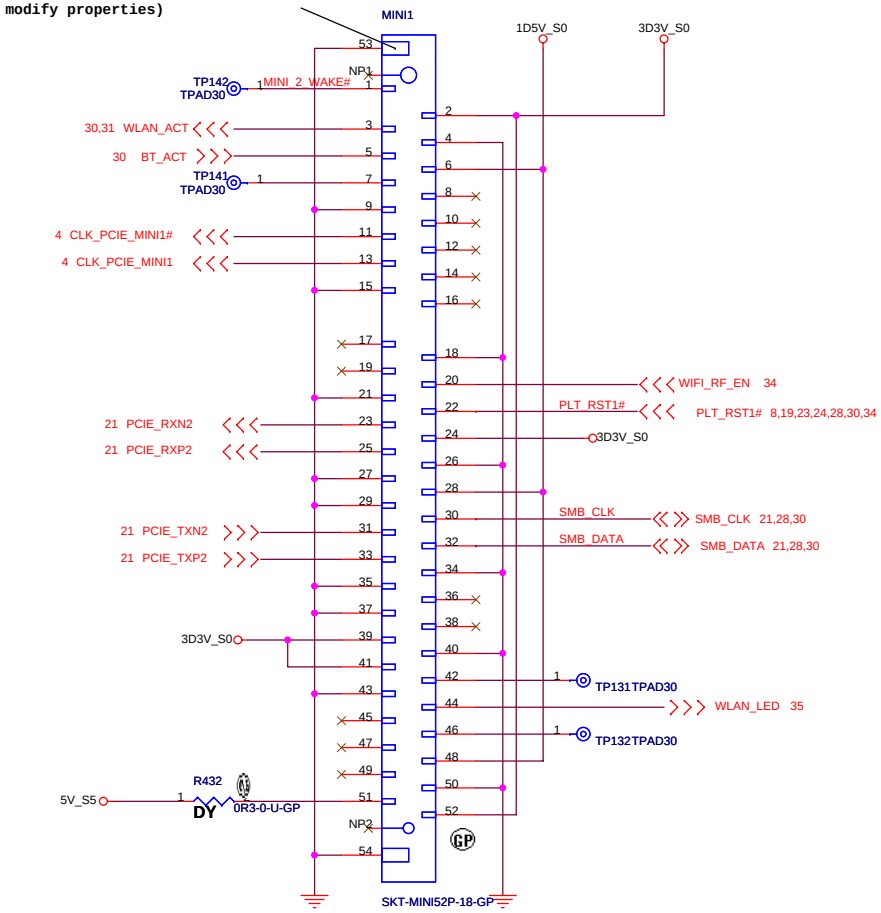
Title: *LAN connector/NEW CARD*

Size	Document Number	Rev
A3	DS2-Intel	-3

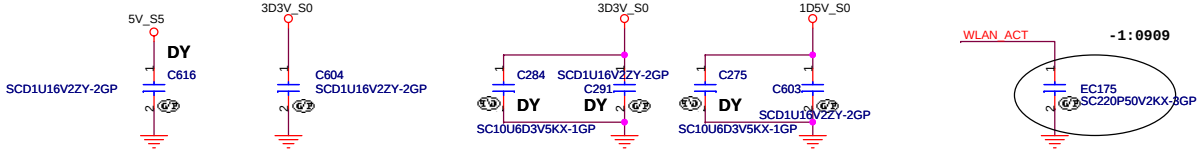
Date: Wednesday, March 26, 2008 Sheet 28 of 50

Mini Card Connector 1(802.11a/b/g)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)



Main Source:62.10043.431
2nd Source: 20.F0992.052



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

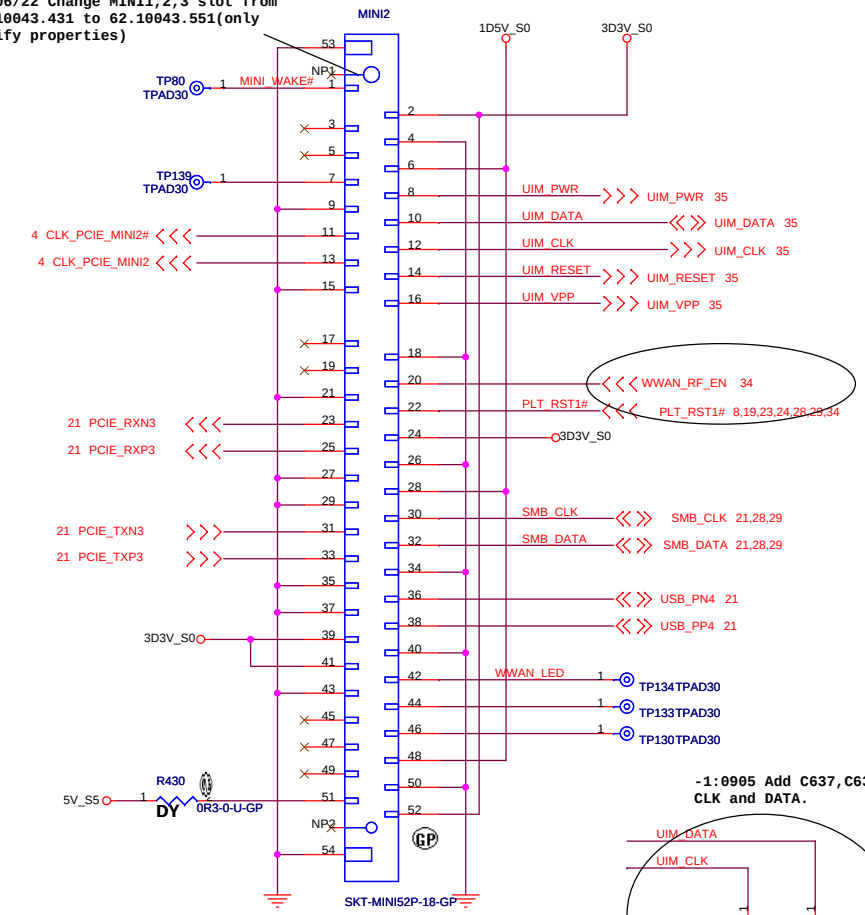
Title: MINI CARD CONN 1

Size	Document Number	Rev
A3	DS2-Intel	-3

Date: Wednesday, March 26, 2008 Sheet 29 of 50

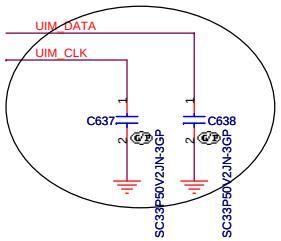
Mini Card Connector
Mini Card Connector 2(WWAN)

SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)

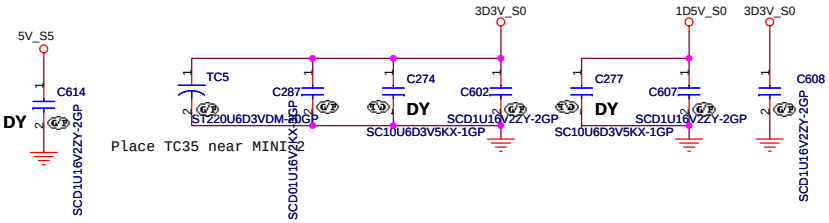


SC:07/30 Add "WWAN_RF_EN" GPIO pin connect to MINI2 pin20

-1:0905 Add C637,C638 for SIM CLK and DATA.



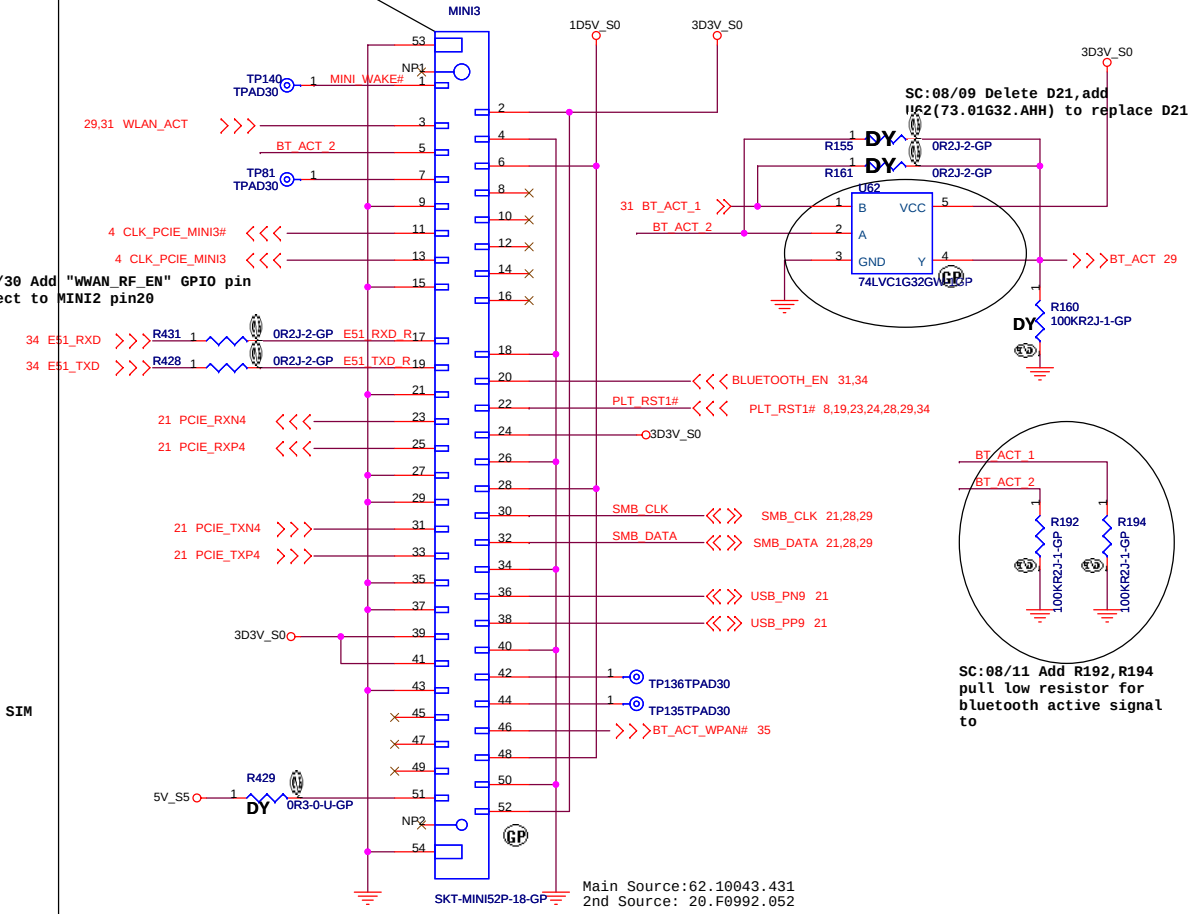
Main Source:62.10043.431
2nd Source: 20.F0992.052



Place TC35 near MINI2

Mini Card Connector 3(Robson)

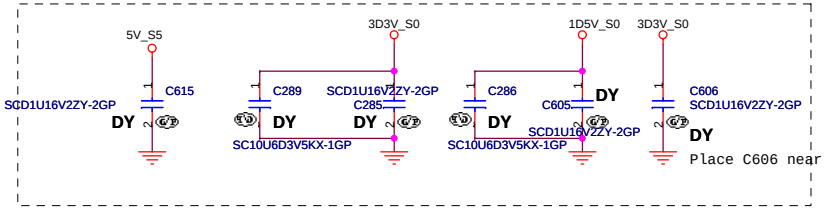
SB:06/22 Change MINI1,2,3 slot from 62.10043.431 to 62.10043.551(only modify properties)



SC:08/09 Delete D21,add U62(73.01G32.AHH) to replace D21

SC:08/11 Add R192,R194 pull low resistor for bluetooth active signal to

Main Source:62.10043.431
2nd Source: 20.F0992.052



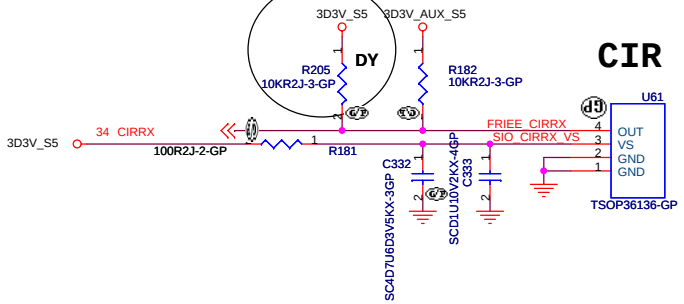
Place C606 near MINI 3 pin24

<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	MINI CARD CONN 2 & 3	
Size A3	Document Number DS2-Intel	Rev -3
Date: Wednesday, March 26, 2008	Sheet 30 of 50	

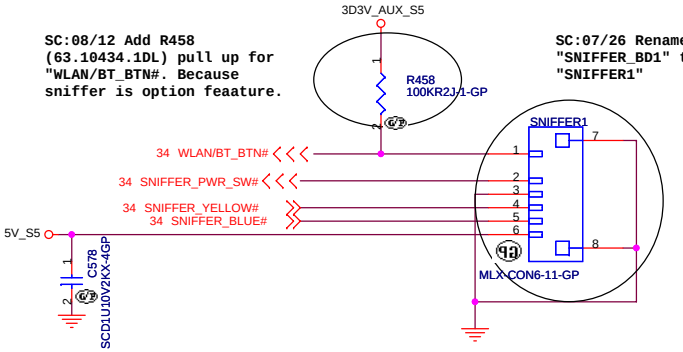
-1:0910

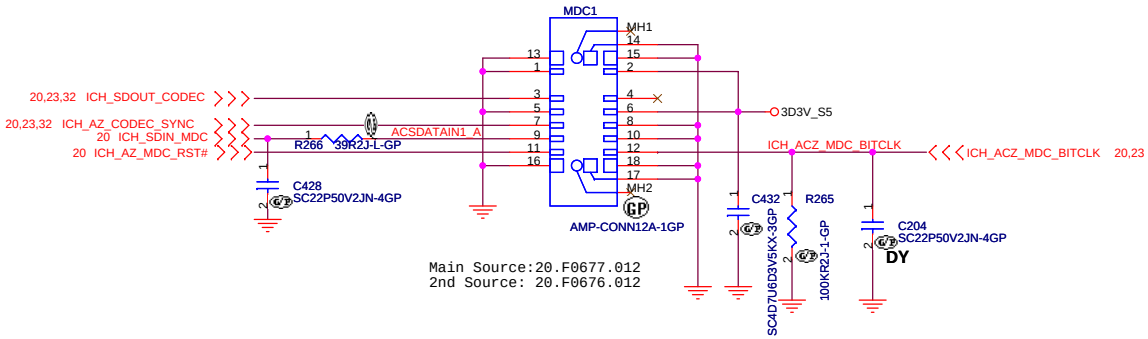
CIR



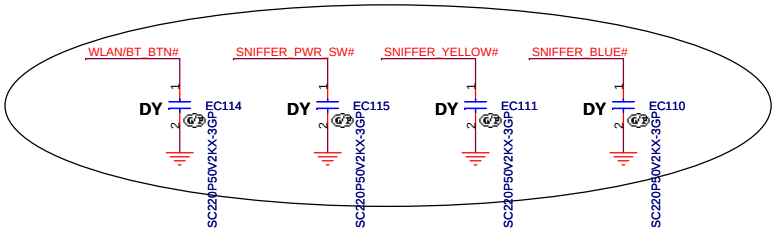
SC:08/12 Add R458 (63.10434.1DL) pull up for "WLAN/BT_BTN#. Because sniffer is option feaature.

SC:07/26 Rename "SNIFFER_BD1" to "SNIFFER1"

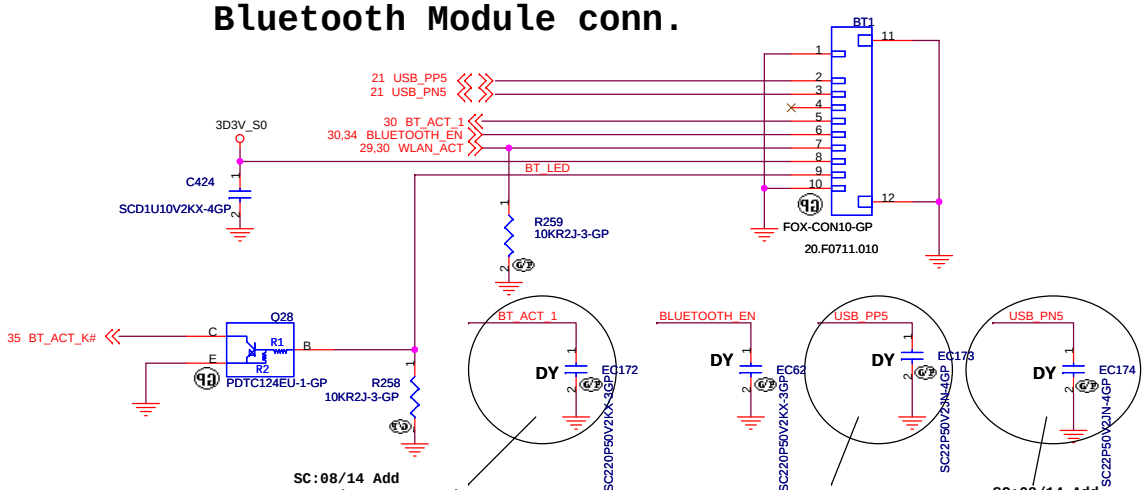




Main Source:20.F0677.012
2nd Source: 20.F0676.012



Bluetooth Module conn.



SC:08/14 Add EC172(78.22124.2FL) on "BT_ACT1" for EMI team request.

SC:08/14 Add EC173(78.22034.1FL) on "USB_PP5" for EMI team request.

SC:08/14 Add EC174(78.22034.1FL) on "USB_PN5" for EMI team request.

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MDC/CIR/Bluetooth/Sniffer Conn.***

Size	Document Number	Rev
A3	*DS2-Intel*	-3

Date: Wednesday, March 26, 2008 Sheet 31 of 50

60ohm 100MHz
3000mA 0.05ohm DC

3D3V_S0

SCD1U10V2KX-4GP C266
SCD1U10V2KX-4GP C276
SC1U6D3V2KX-GP C270

R152 100KR2J-1-GP +3V_RUN_DVDD_CORE3
C298 SC1KP50V2KX-1GP

SB:07/10 Change R344 from 33 Ohm to 0 Ohm

20 ICH_AZ_CODEC_BITCLK
20 ICH_SDIN_CODEC
20,23,31 ICH_SDOUT_CODEC
20,23,31 ICH_AZ_CODEC_SYNC
20 ICH_AZ_CODEC_RST#

ICH_AZ_CODEC_BITCLK
R146 33R2J-2-GP
SB_AZ_CODEC_SDIN0_R

3D3V_S0
U34 74LVC1G125DC-GP
18 AUD_DMIC_CLK_G
AUD_DMIC_CLK_G
R149 33R2J-2-GP
AUD_DMIC_CLK

DY

SB: Change R149 from 63.R0034.1DL to 63.33034.1DL

18 AUD_DMIC_IN0
R455 200R2F-L-GP
35 SPDIF_D
23 AUD_SPDIF_OUT
AUD_DMIC_IN0
AUD_SPDIF_OUT
AUD_DMIC_CLK

AUD_DMIC_CLK_G
EC129 SC22P50V2JN-4GP

SB:06/26 Add EC129(78.22034.1FL) by EMI request

U36 STAC9228X5TAEA2-GP 71.09228.00G

DVDD_CORE
DVDD_CORE
DVDD
BIT_CLK
SDATA_IN
SDATA_OUT
SYNC
RESET#
VOLUME UP/DMIC_0/GPIO1
VOLUME DN/DMIC_1/GPIO2
SPDIF_IN/GPIO0/DMIC_CLK
SPDIF_OUT
DVSS1
DVSS2

AVDD1
AVDD2
SENSE_A
SENSE_B
PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
VREFOUT_D
PORTE_L
PORTE_R
VREFOUT_E
PORTF_L
PORTF_R
VREFOUT_F
PORTG_L
PORTG_R
PORTH_L
PORTH_R
CD_L
CD_GND
CD_R
PC_BEEP
CAP2
VREFFILT
AVSS1
AVSS2

+VDDA
SCD1U10V2KX-4GP C320
SC1U10V3KX-3GP C296

AUD_SENSE_A
AUD_SENSE_B

TO Audio OP
AUD_HP1_OUT_L
AUD_HP1_OUT_R
AUD_HP1_OUT_L 33
AUD_HP1_OUT_R 33

C292 SC1U10V3KX-3GP INT_MIC
C294 SC1U10V3KX-3GP
R153 4K7R2J-2-GP
AUD_INT_MIC_L
AUD_INT_MIC_R
AUD_VREFOUT_B

AUD_LINE_OUT_L
AUD_LINE_OUT_R
AUD_LINE_OUT_L 33
AUD_LINE_OUT_R 33

TO Audio OP

AUD_EXT_MIC_L
AUD_EXT_MIC_R
AUD_VREFOUT_E

AUD_HP2_OUT_L 33
AUD_HP2_OUT_R 33

Port A---> HP1
Port E---> Ext Mic
Port D---> Speaker
Port F---> HP2
Port C--->Int Mic

PC BEEP
AUD_PC_BEEP
AUD_CAP2
AUD_VREFFLT
C267 SCD1U10V2KX-4GP
C299 SC1U10V5KX-2GP
C300 SC1U10V5KX-2GP
R412 10KR2J-3-GP
R141 47KR2F-GP
R413 47KR2F-GP
From SB
SB_SPKR 21
KBC_BEEP 34
From EC

SA:0428

+VDDA
R421 5K1R2F-2-GP
R420 39K2R2F-L-GP AUD_HP1_JD# 33
R154 5K1R2F-2-GP
R158 20KR2J-L2-GP AUD_HP2_JD# 33
R157 39K2R2F-L-GP EXT_MIC_JD#

Internal Microphone

Azalia I/F EMI

ICH_SDOUT_CODEC
R145 47R2J-2-GP
ICH_AZ_CODEC_SDOUT_1
C263 SCD1U10V2KX-4GP
DY

Azalia I/F EMI

-1:0921 Remove R144 and C265

MIC IN

AUD_VREFOUT_E
R162 4K7R2J-2-GP
R163 4K7R2J-2-GP
C302 SC1U10V3KX-3GP
AUD_EXT_MIC_L
AUD_EXT_MIC_R
C306 SC1U10V3KX-3GP MIC_IN_L_2
C307 SC1U10V3KX-3GP MIC_IN_R_2
R169 0R3-0-U-GP MIC_IN_L_C
R168 0R3-0-U-GP MIC_IN_R_C
EXT_MIC_JD#
EC48 SC100P50V2JN-3GP
EC49 SC100P50V2JN-3GP
MIC1
AUDIO-JK89-GP-U

SB:07/02 Change R168 from 63.R0034.1DL to 63.00000.00L

600ohm 100MHz
200mA 0.5ohm DC

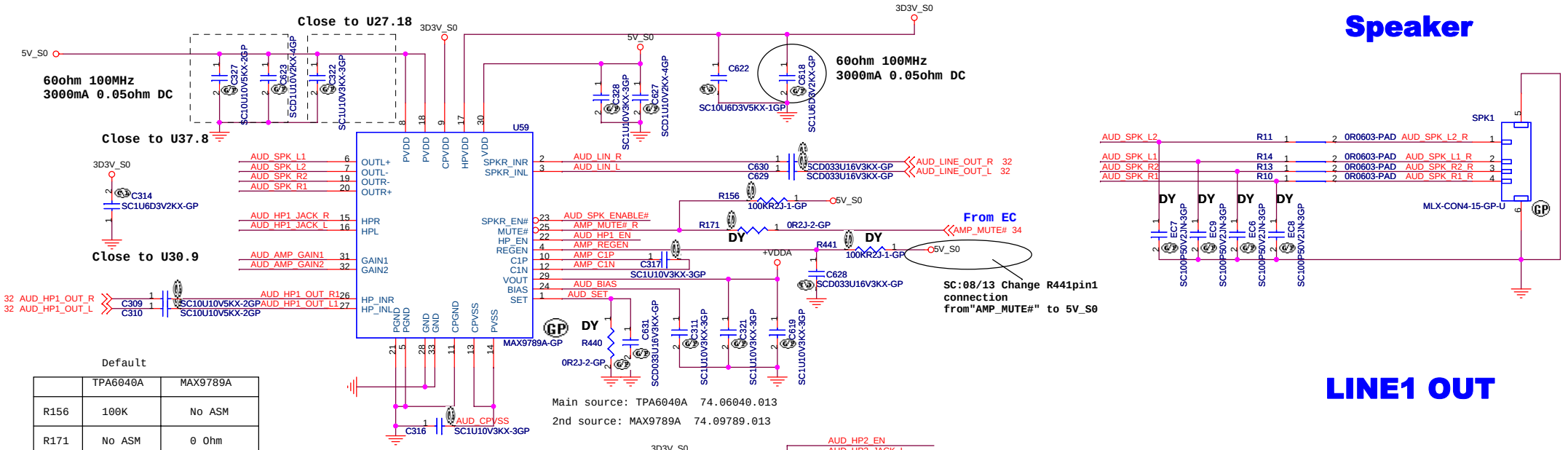
-1:0920
CN4 MICROPHONE-40-GP-U1
INT_MIC
EC52 SC1KP50V2KX-1GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC STAC9228
Size: A3 | Document Number: DS2-Intel | Rev: -3
Date: Wednesday, March 26, 2008 | Sheet 32 of 50

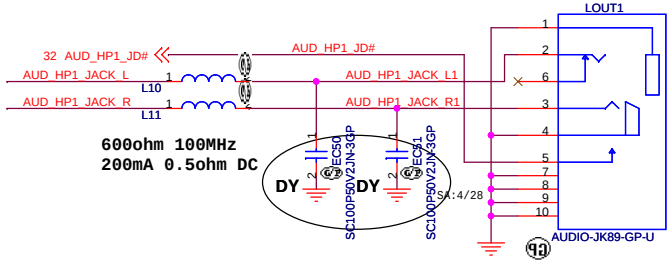
Speaker

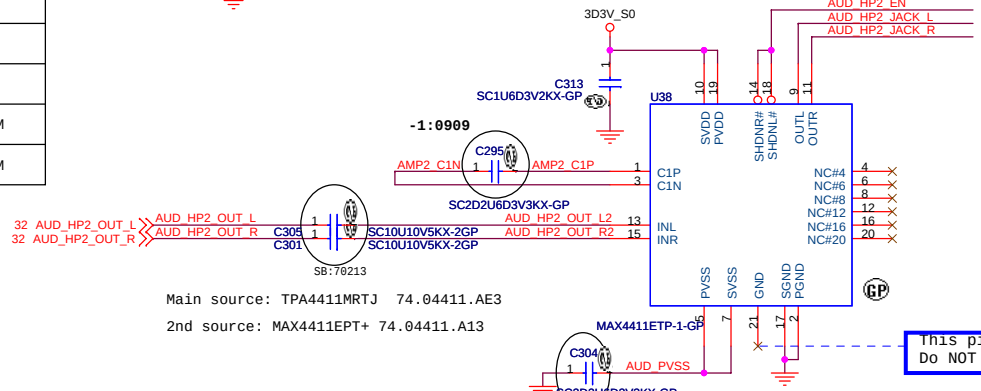


Default

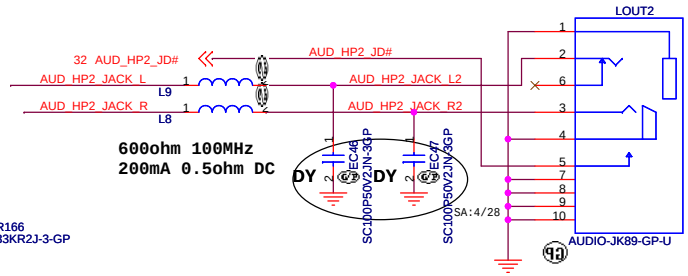
	TPA6040A	MAX9789A
R156	100K	No ASM
R171	No ASM	0 Ohm
R440	No ASM	0 Ohm
R441	No ASM	100K
C631	0.33uF	No ASM
C628	0.33uF	No ASM

LINE1 OUT

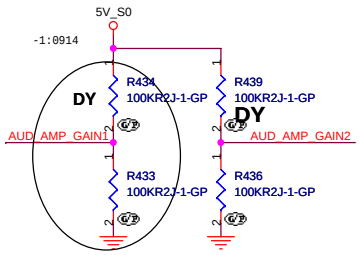




LINE2 OUT



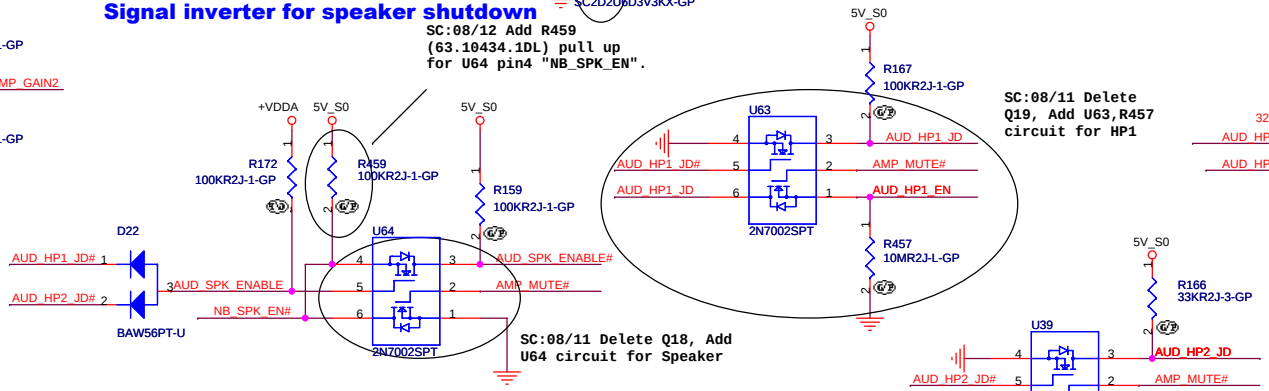
GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown

SC:08/12 Add R459 (63.10434.1DL) pull up for U64 pin4 "NB_SPK_EN".



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP/SPEAKER

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 33 of 50

WPC8763L STRAP PIN

JEN0 (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES		GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE

Forces the device to float all its output and I/O pins,if an external 10 KΩ pull-down resistor is conected.

BADDR1-0 (PIN 111, 112) I/O Base Address.
10KΩ external pull-down resistor on BADDR1: Core defined

SB:06/24 Change R104 from 63.10334.1DL to 63.47234.1DL.Base on Winbond FAE recommend to fix system will hang up after Thermal T8 shutdown

SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.

SB:06/27 Change R98 from 63.10334.1DL to 63.47234.1DL

PLACE CAP NEAR PIN80 AND PIN102

PLACE CAP NEAR PIN46,19,115,76,88,104

-1:08/30 Change Pin10 from NC to be"WWAN_RF_EN"

-1:08/30 Change Pin11 from NC to be"HDD_5V_EN"

-1: 08/29 change Pin24 from "WWAN_RF_EN" to NC, because pin24 is H/W straping pin. it has H/W concern.

SC:08/03 Change Pin27 from"BLON_OUT" to" LCD_TST_EN", delete TP45 test pad.

-1:08/29 Change U22 pin110 define from NC to"USB_PWR_EN" or USB power control.

KBC DEBUG POINT

<-----BATTERY

FOR Thermal AND Capacity Button Module

MB VERSION ID

	VER0	VER1
SA	0	0
SB	0	1
SC	1	0
-1	1	1

WPC8763L XTAL

X-32D768KHZ-40GPU

KBC CLK EMI

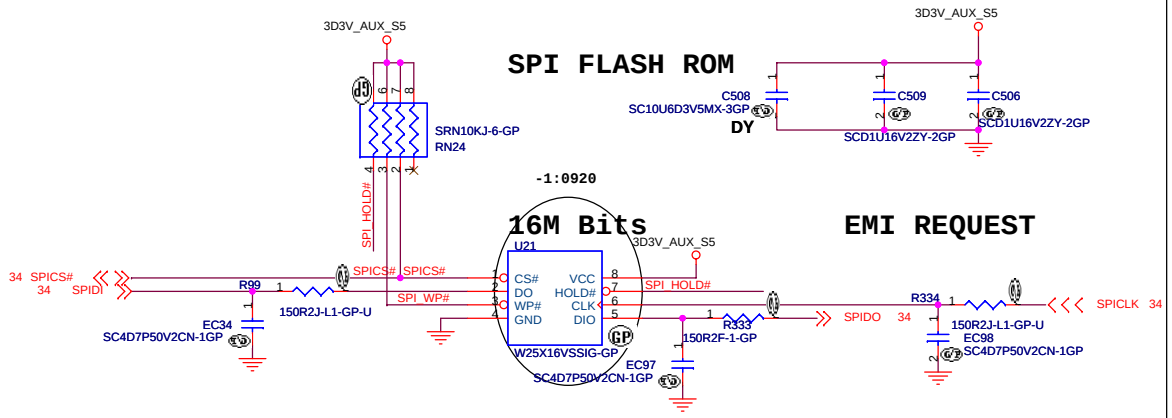
ADIA:to Charger
ACDC_ID:from Adapter Conn
KBC_PWRBTN#:from power button
BAT_IN#:from Battery Conn
DC_BATFULL#:for Battery charge LED 1
WLAN_TEST:for WKS test WLAN LED
AD_OFF:enable AC adapter power source
CHARGE_LED#:for Battery charge LED 2
WLAN/BT_BTN#:from Wlan on/off button
GMCH_BL_ON:Sense The Backlight On/Off Status from VGA Chip
WIRELESS_EN:Disable/Enable Wireless Module
BLUETOOTH_EN:Disable/Enable Bluetooth
USB_PWR_EN#:to on/off USB power switch
CCD_ON:Webcam power on/off
AC_IN#:From Charge

<Core Design>

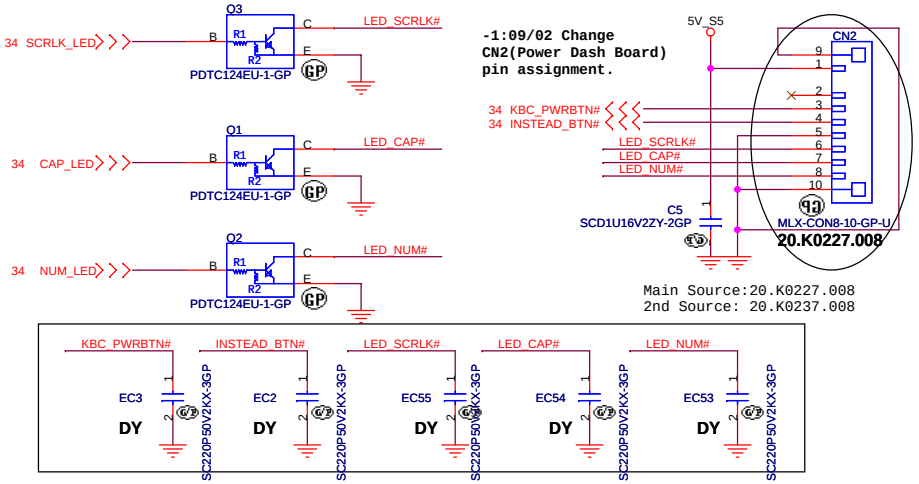
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC_Winbond WPC8763L
Size: A2 | Document Number: DS2-Intel | Rev: -3
Date: Wednesday, March 26, 2008 | Sheet 34 of 50

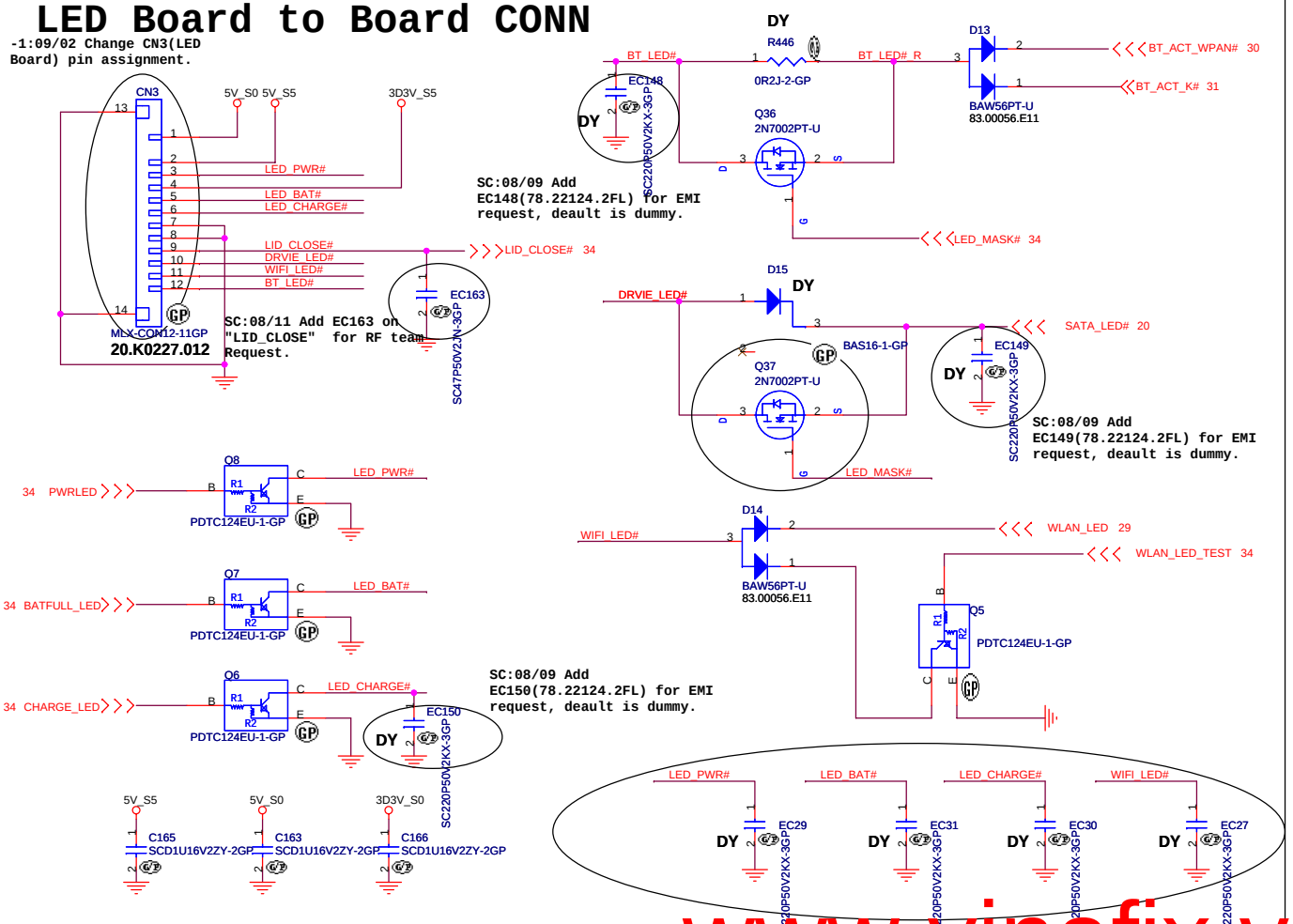
SPI



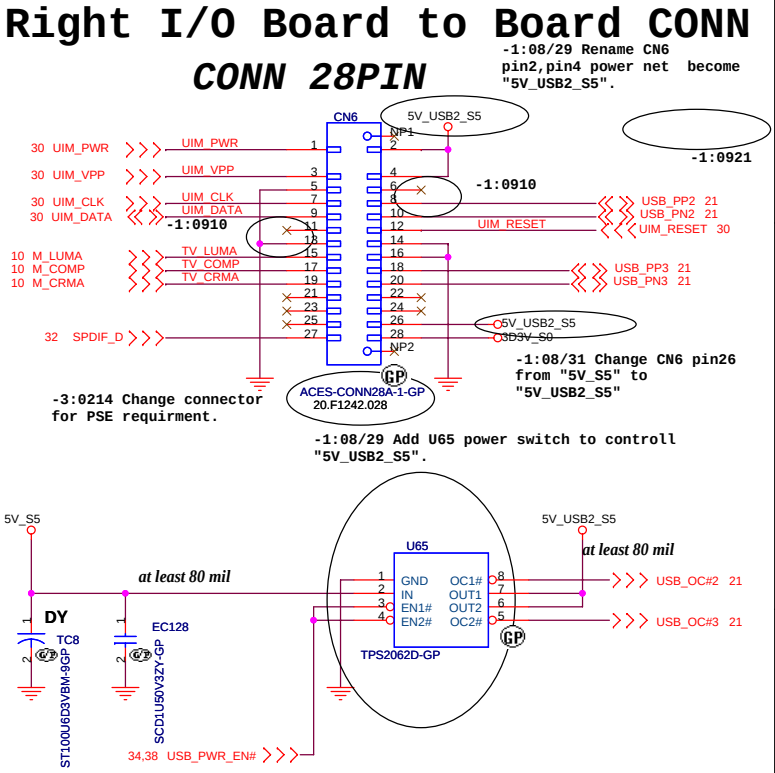
Power Dash Board to Board CONN



LED Board to Board CONN



Right I/O Board to Board CONN



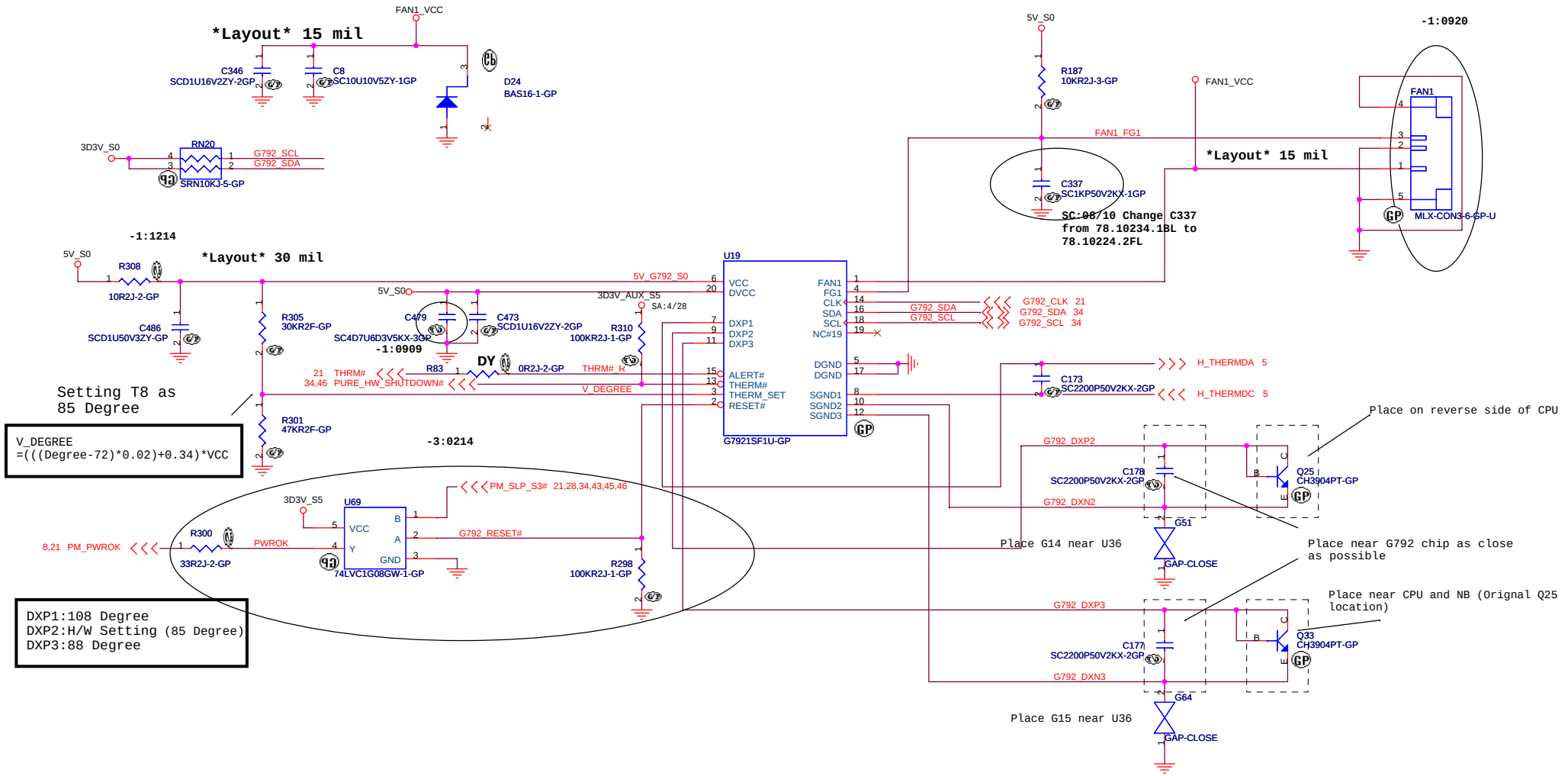
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH and Board to Board CONN

Size	Document Number	Rev
A3	DS2-Intel	-3

Date: Wednesday, March 26, 2008 Sheet 35 of 50



<Core Design>

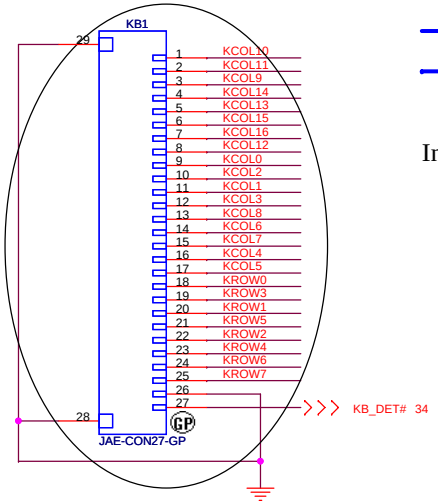
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G7921

Size	Document Number	Rev
A3	DS2-Intel	-3

Date: Wednesday, March 26, 2008 Sheet 36 of 50

SB:06/27 Change K/B connector from 20.F0694.025
to 20.K0291.027 .

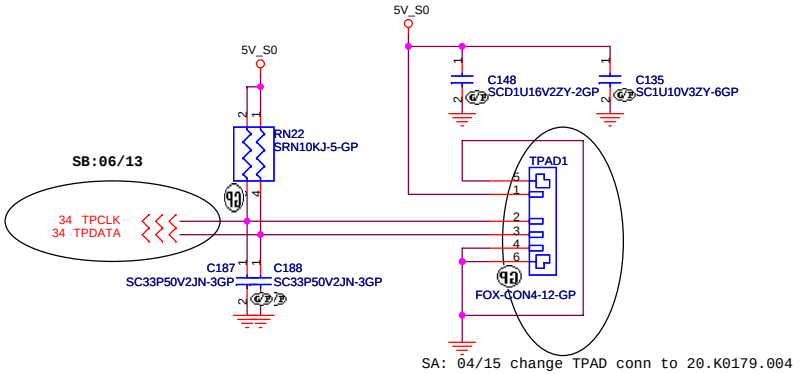


KROW[0..7] 34

KCOL[0..16] 34

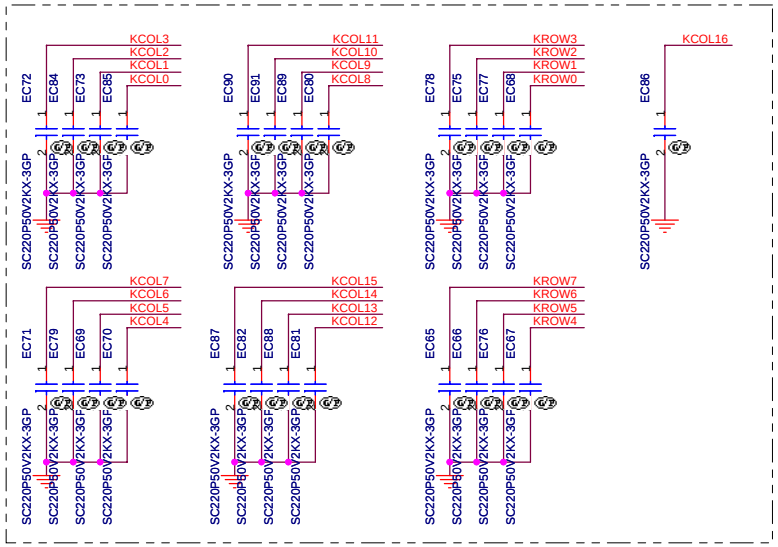
Internal KeyBoard Connector

TouchPad Connector



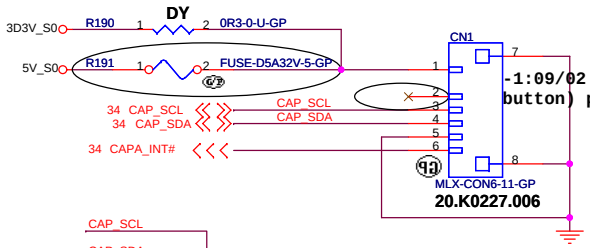
SA: 04/15 change TPAD conn to 20.K0179.004

for EMI

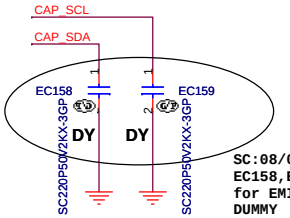


-1:12/14 Chage R191 from 0
ohm to 0.5A fuse to prevent
VCC short to GND.

CAPACITY BUTTON



-1:09/02 Change CN1(Capacity
button) pin2 from GND to NC



SC:08/09 Add
EC158,EC159(78.22124.2FL)
for EMI request .Default is
DUMMY

Main Source:20.K0227.006
2nd Source: 20.K0228.006

<Core Design>

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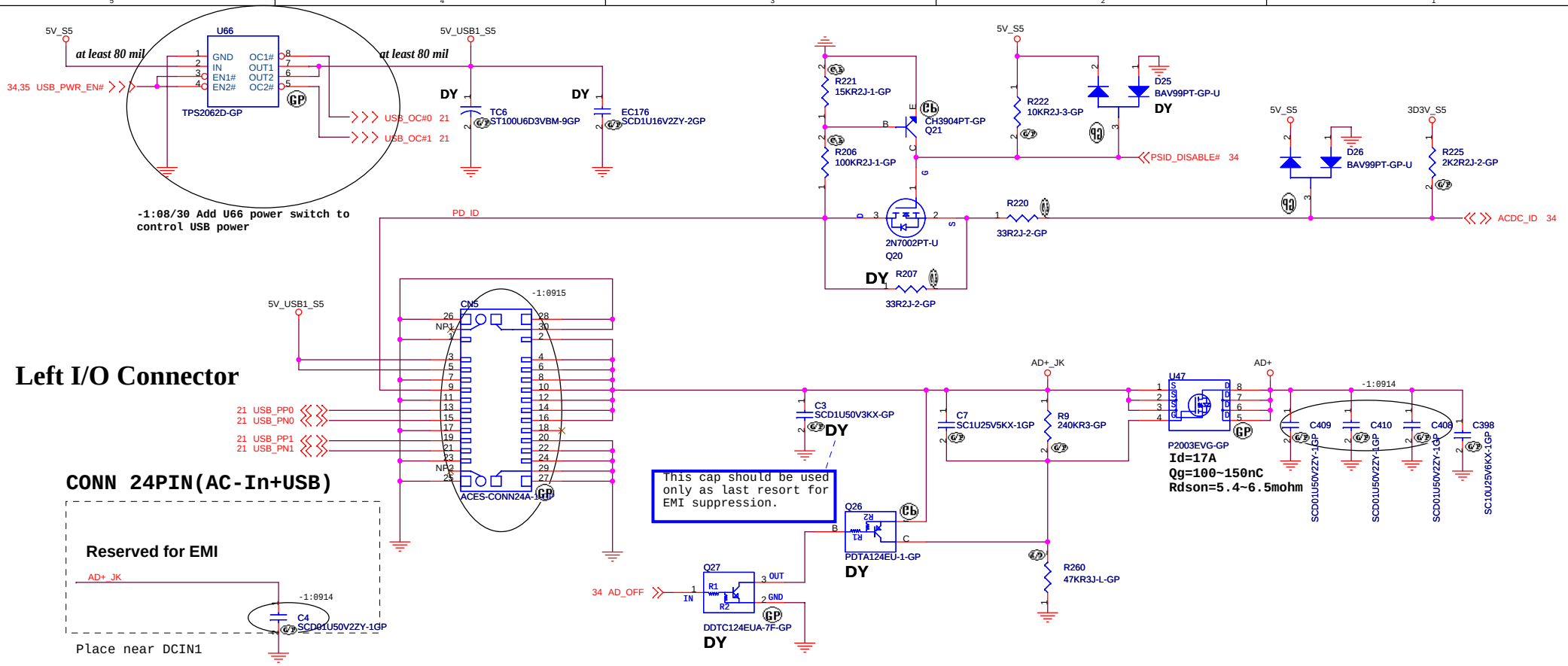
Title: KeyBoard-CONN

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 37 of 50



<Core Design>

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Title: AD/BATT CONN

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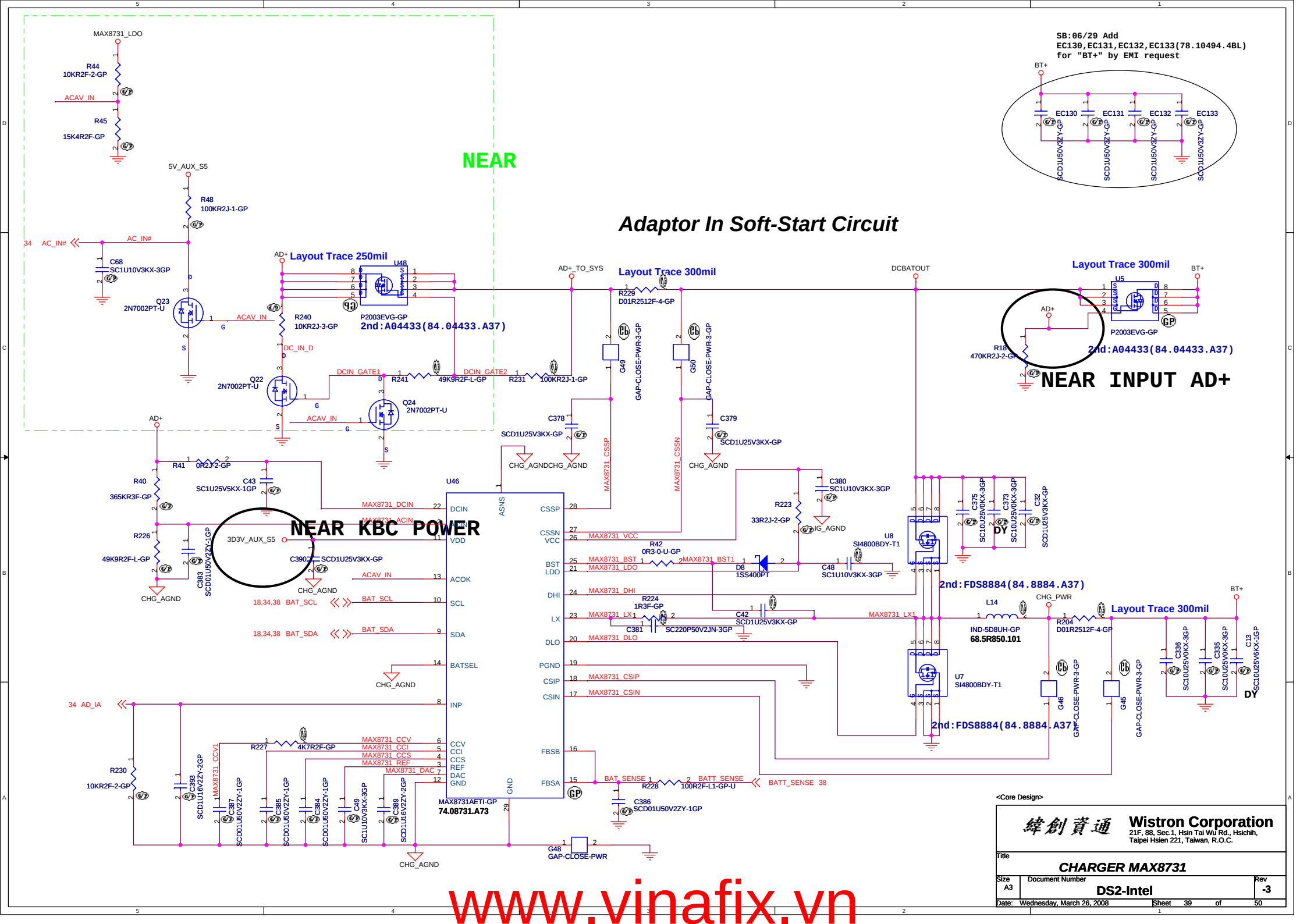

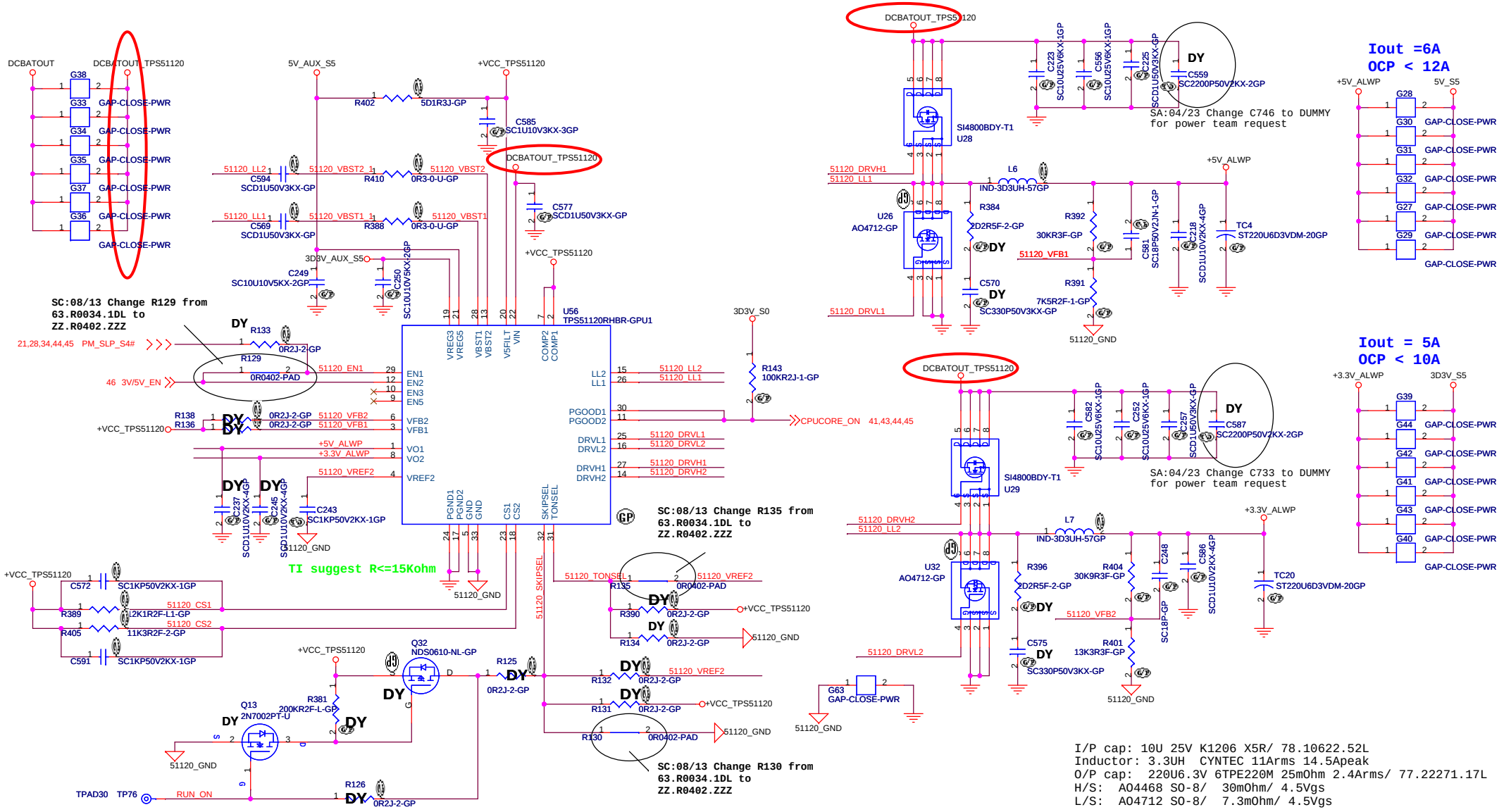

Vout=1V*(R1+R2)/R2

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

<Core Design>

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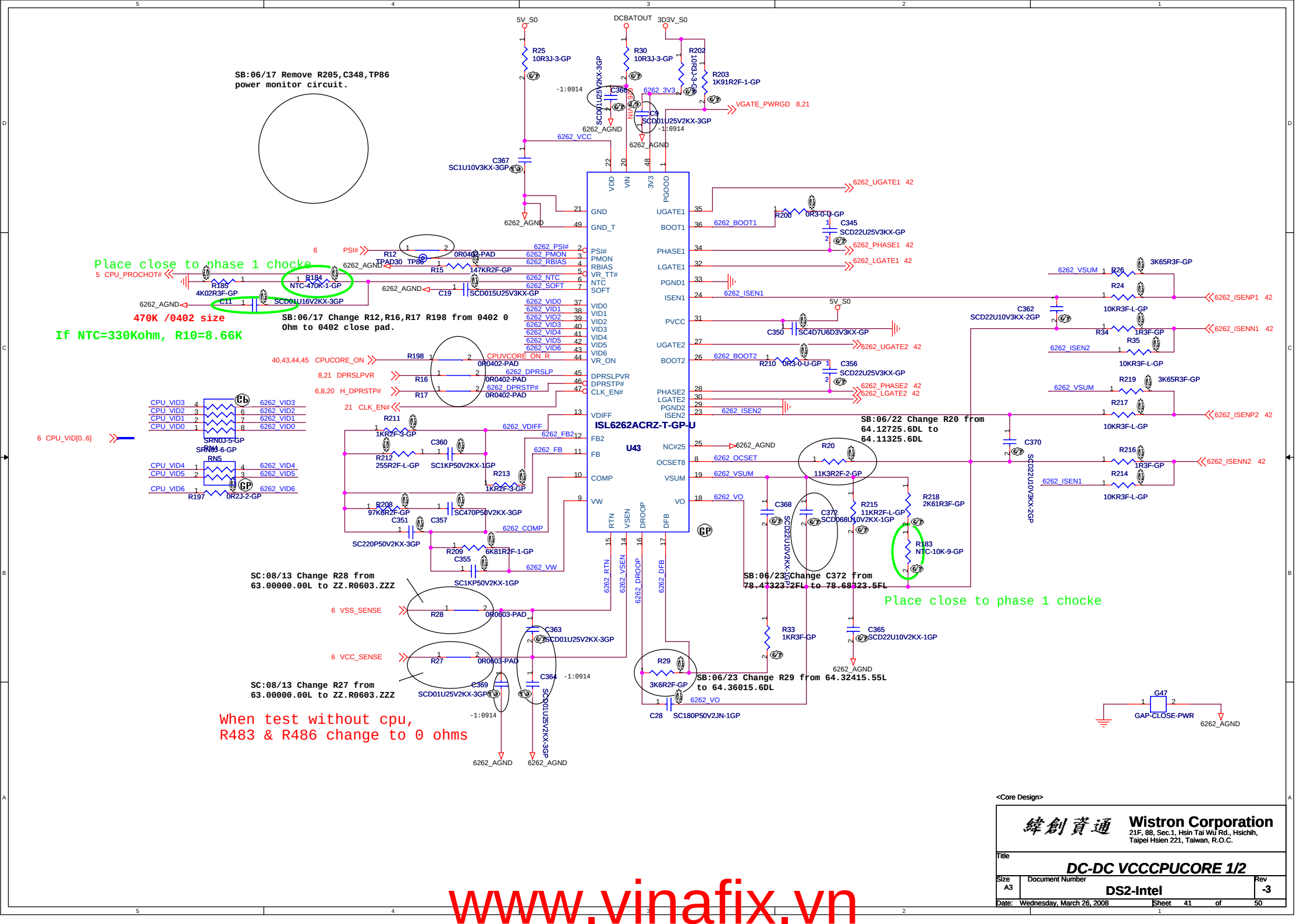
Title: DC to DC 3.3V & 5V

Size: A3 | Document Number: DS2-Intel | Rev: -3

Date: Wednesday, March 26, 2008 | Sheet 40 of 50


SB:06/17 Remove R205,C348,TP86
power monitor circuit.
Place close to phase 1 chocke
470K /0402 size
If NTC=330Kohm, R10=8.66K
SB:06/17 Change R12,R16,R17 R198 from 0402 0 Ohm to 0402 close pad.
ISL6262ACRZ-T-GP-U
U43
SB:06/22 Change R20 from 64.12725.6DL to 64.11325.6DL
SB:06/23 Change C372 from 78.47323.2FL to 78.68323.5FL
Place close to phase 1 chocke
SC:08/13 Change R28 from 63.00000.00L to ZZ.R0603.ZZZ
SC:08/13 Change R27 from 63.00000.00L to ZZ.R0603.ZZZ
SB:06/23 Change R29 from 64.32415.55L to 64.36015.6DL
When test without cpu,
R483 & R486 change to 0 ohms
<Core Design>
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DC-DC VCCCPUCORE 1/2
DS2-Intel
Wednesday, March 26, 2008
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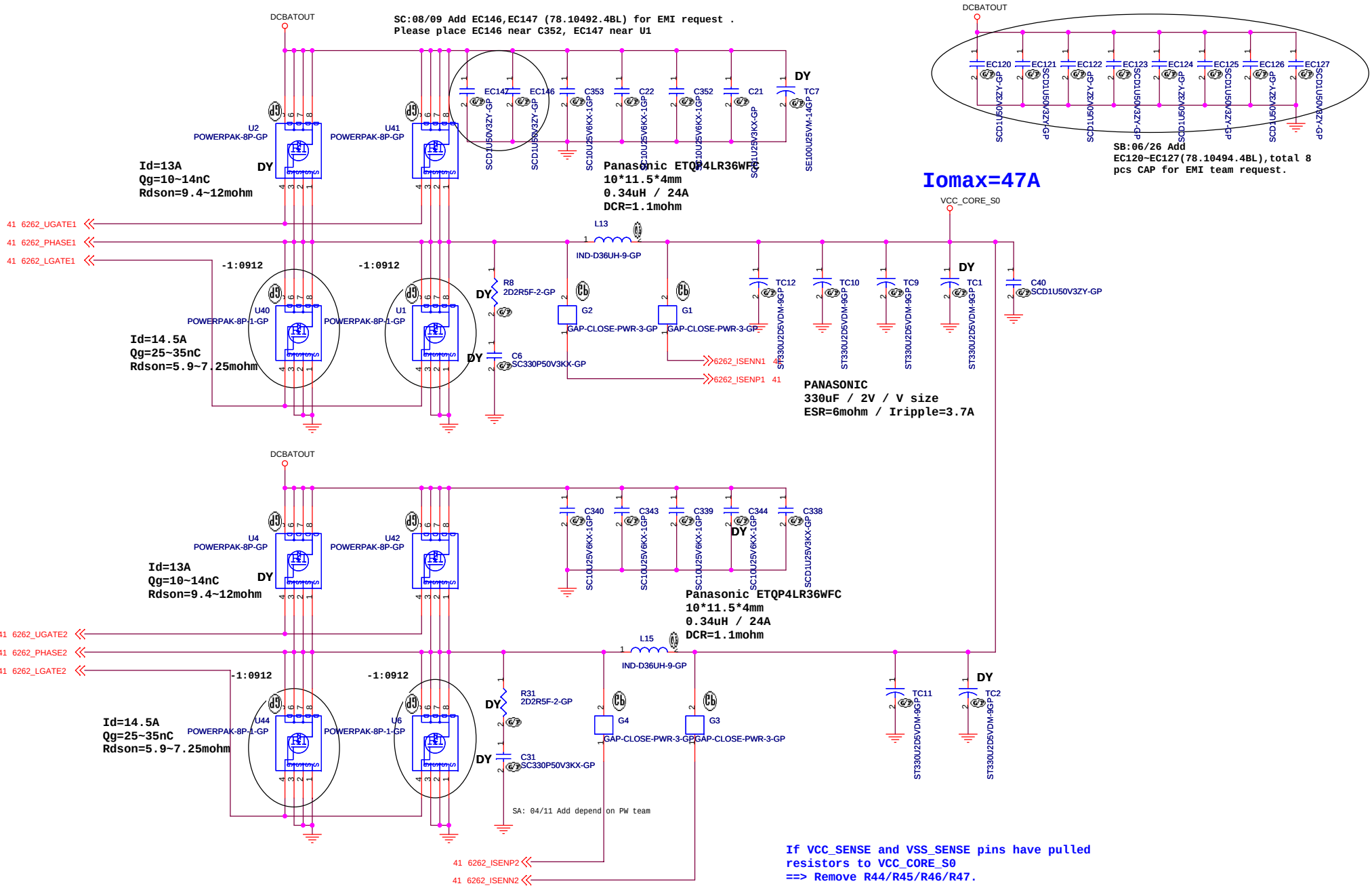

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-DC VCCCPUCORE 2/2

Size	Document Number	Rev
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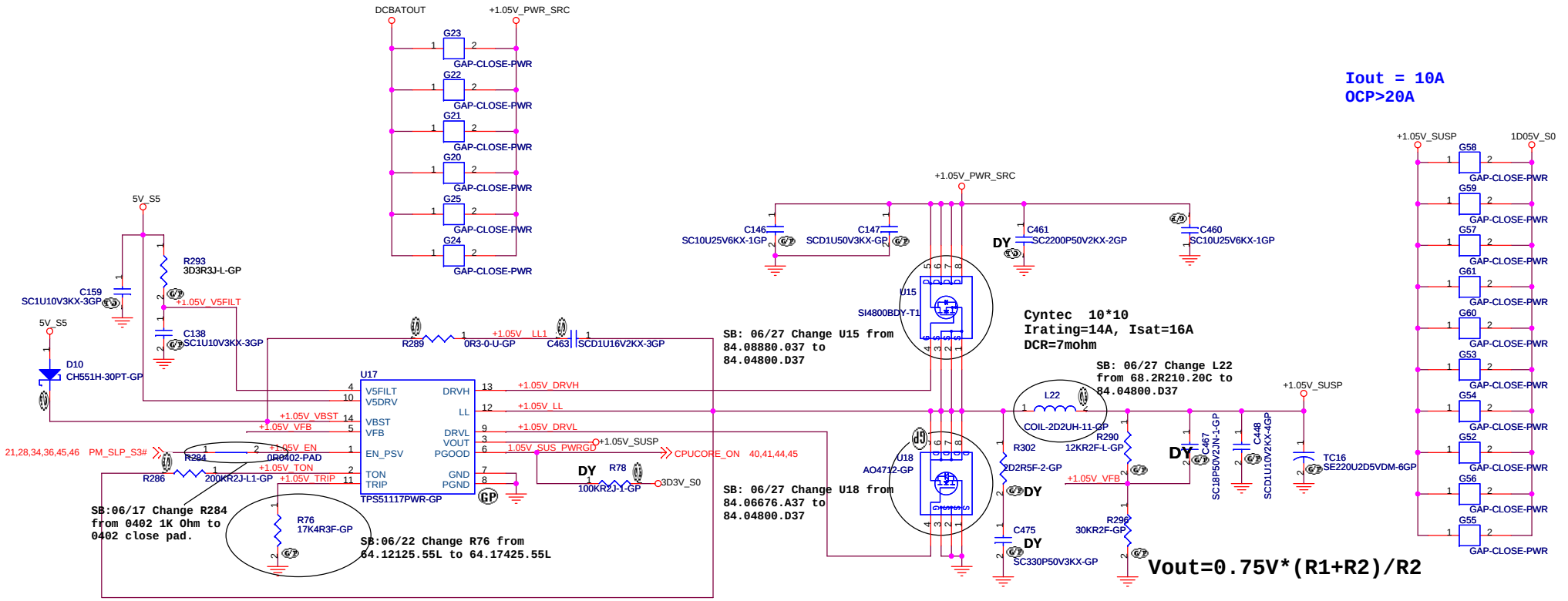

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
Ton = 200KOhm --> 330KHz

<Core Design>

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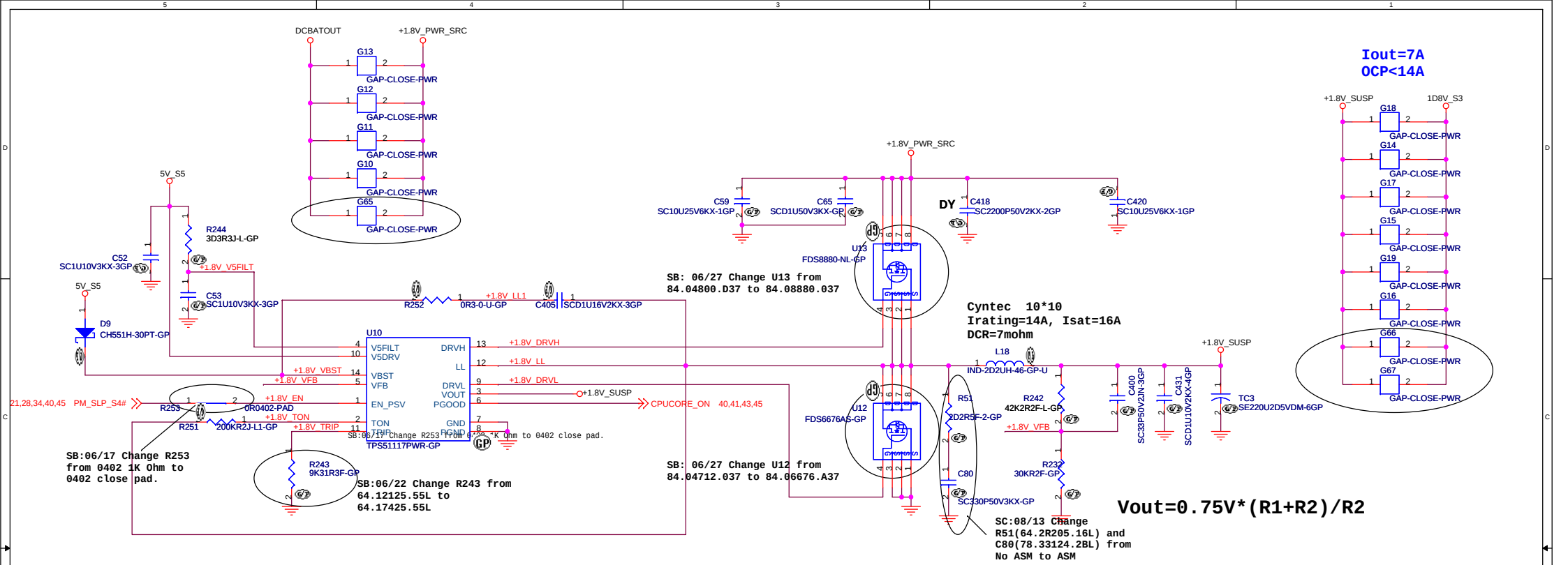
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 1.05V
Size: A3 | Document Number: DS2-Intel | Rev: -3
Date: Wednesday, March 26, 2008 | Sheet 43 of 50



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH M MPL73-1R5 Delta 9Arms 18Apeak / 68.1R510.10I
O/P cap: 220U 4V 4TPE220MF 15mOhm 3.1Arms/ 77.22271.161
H/S & L/S: FDS8884 SO-8/ 30mOhm/ 4.5Vgs/ 84.08884.037
L/S: FDS8896 SO-8/ 7.3mOhm/ 4.5Vgs/ 84.08896.037
Ton = 200KOhm --> 330KHz

<Variant Name>

緯創資通 Wistron Corporation
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Title	DC/DC 1D8V	
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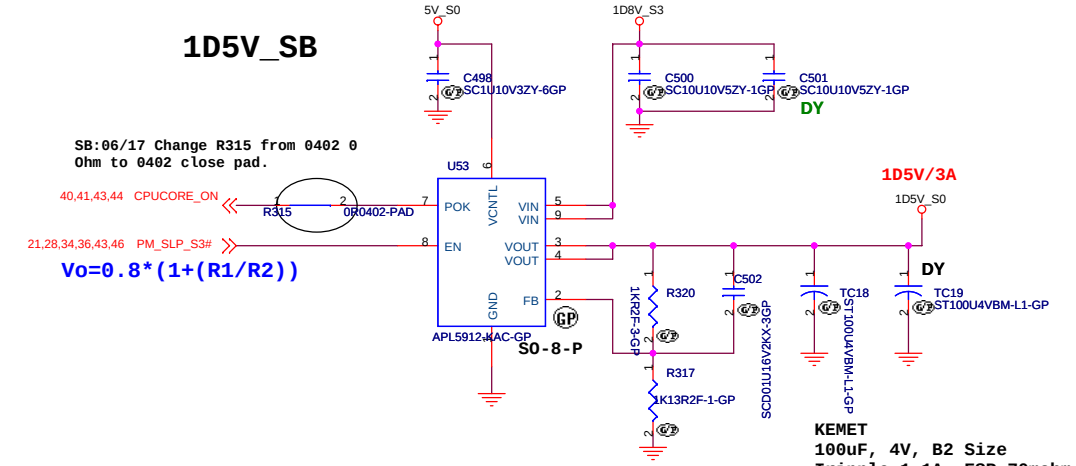
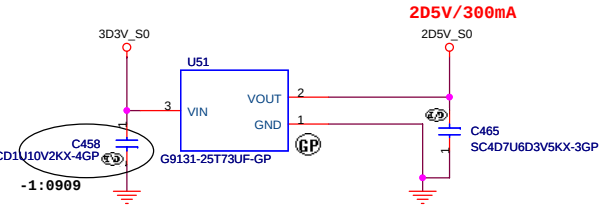
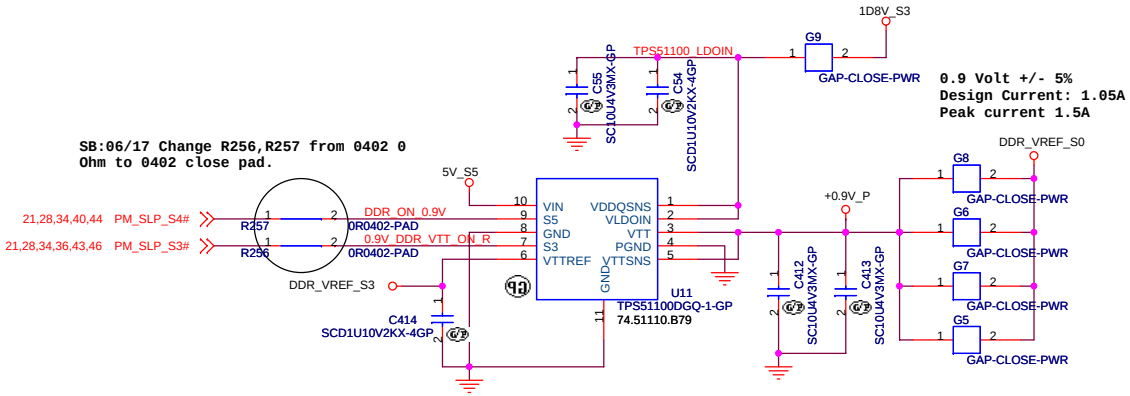
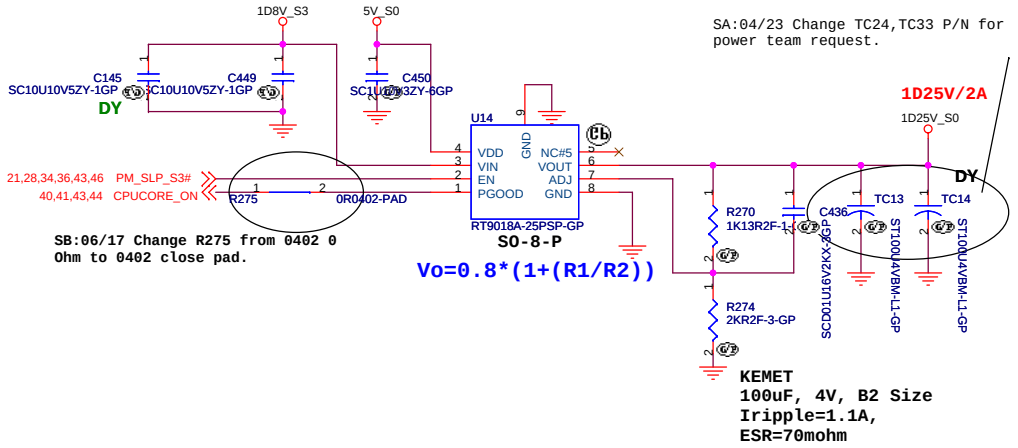
1D5V_SB





SSID = PWR.Plane.Regulator_0.9V





<variant_name>

緯創資通 **Wistron Corporation**
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Title	DC/DC 1D8V	
Size A3	Document Number DS2-Intel	Rev -3
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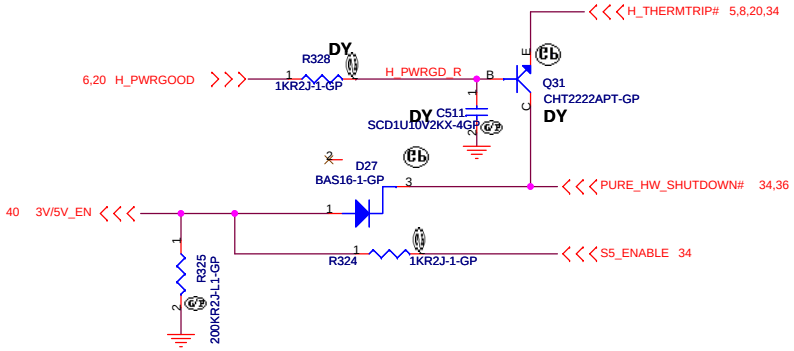
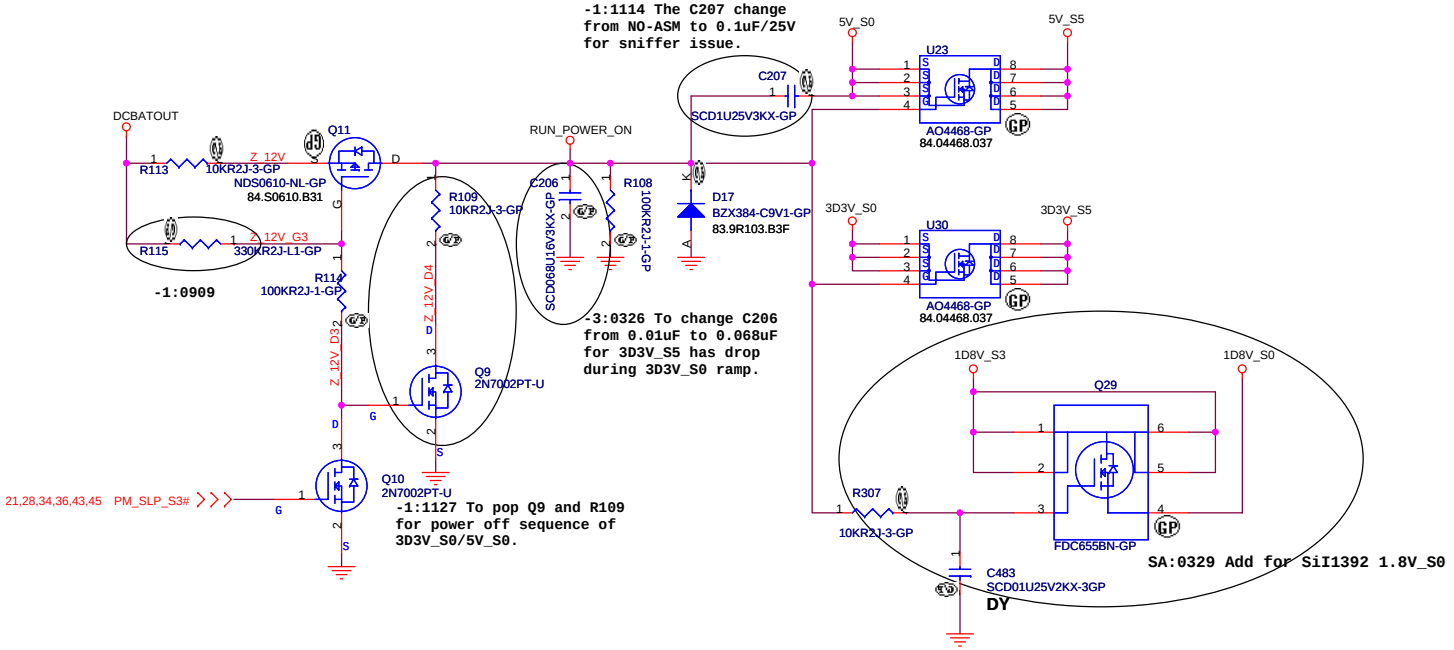


Run Power



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PWRPLANE&RESETLOGIC

Size: A3 | Document Number: DS2-Intel | Rev: -3

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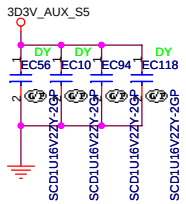
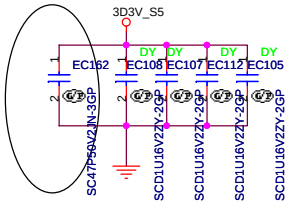
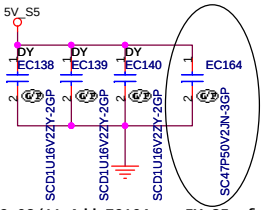


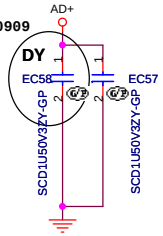


SC:08/11 Add EC162 on 3D3V_S5
for RF team Request.

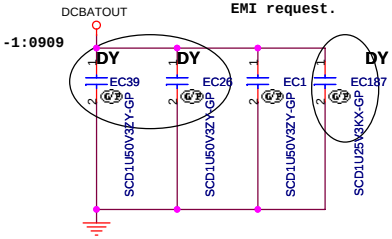


SC:08/11 Add EC164 on 5V_S5 for RF
team Request.

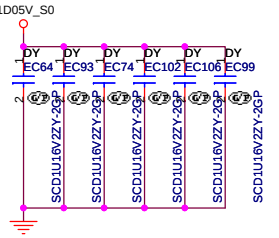
-1:0909

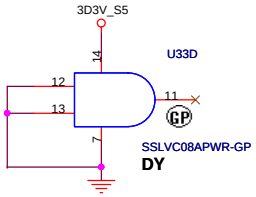


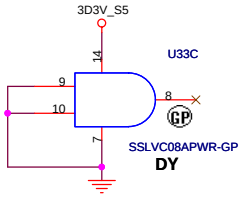
-1:0909

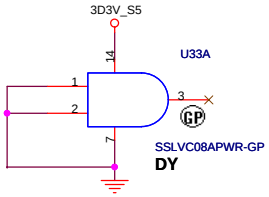


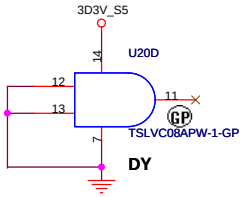
-1:0904 Add EC187(78.10422.2BL) for
DCBATOUT decoupling , this is for
EMI request.

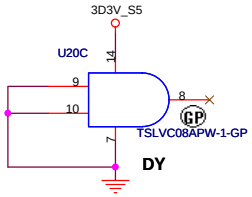


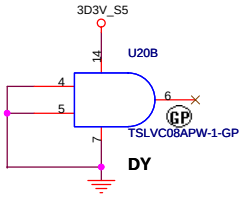


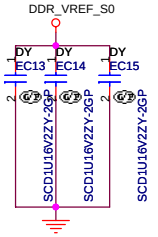


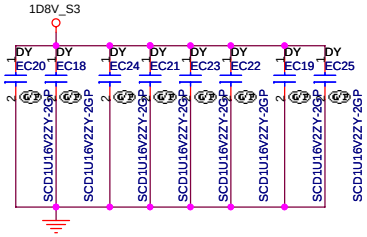


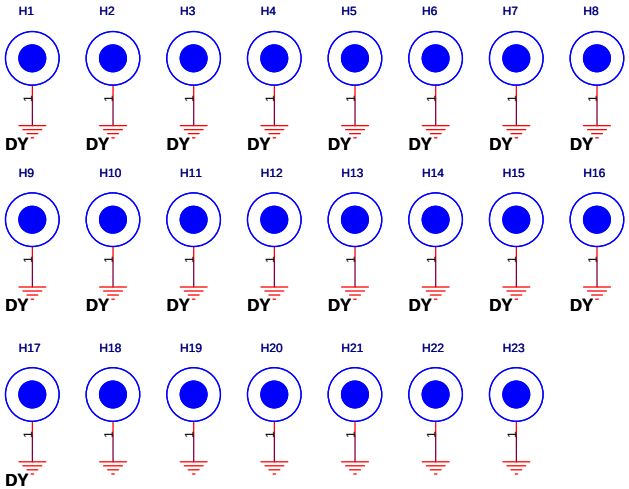


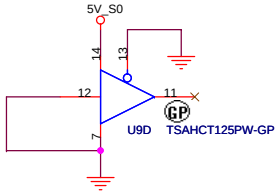




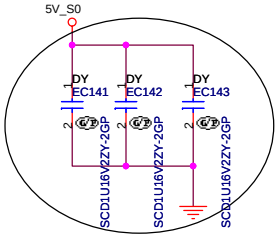




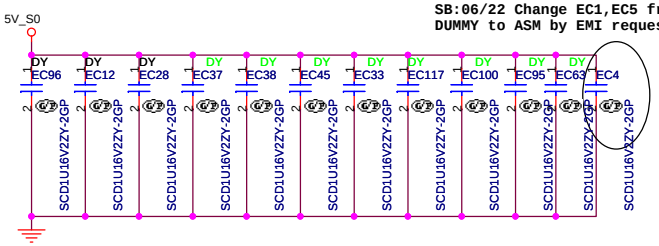




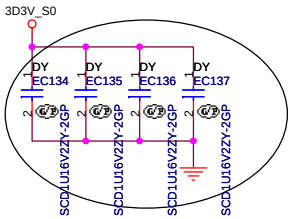
SB:06/29 Add
EC141,EC142,EC143(78.10491.4FL)
for EMI request

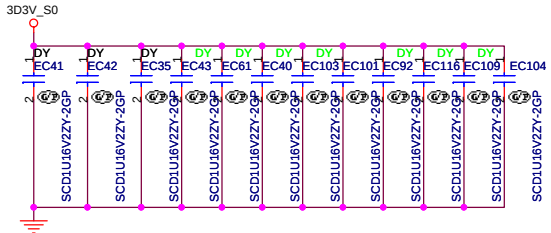


SB:06/22 Change EC1,EC5 from
DUMMY to ASM by EMI request.



SB:06/29 Add
EC134,EC135,EC136,EC137(78.10491.4FL)
for EMI request

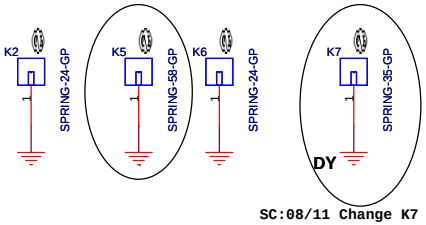


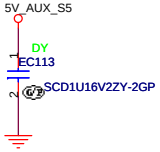


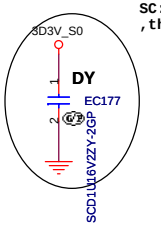
SC:08/15 Add EC177(78.10491.4FL) on 3D3V_S0
,this is for EMI request. Default is DY

Place this spring near
U40(bottom side)

-1:0920







SC:08/11 Change K7 from
34.39S07.001 to
34.41P18.001.This change is for
EMI request
-1:11/15 Remove K7 for no used.

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC

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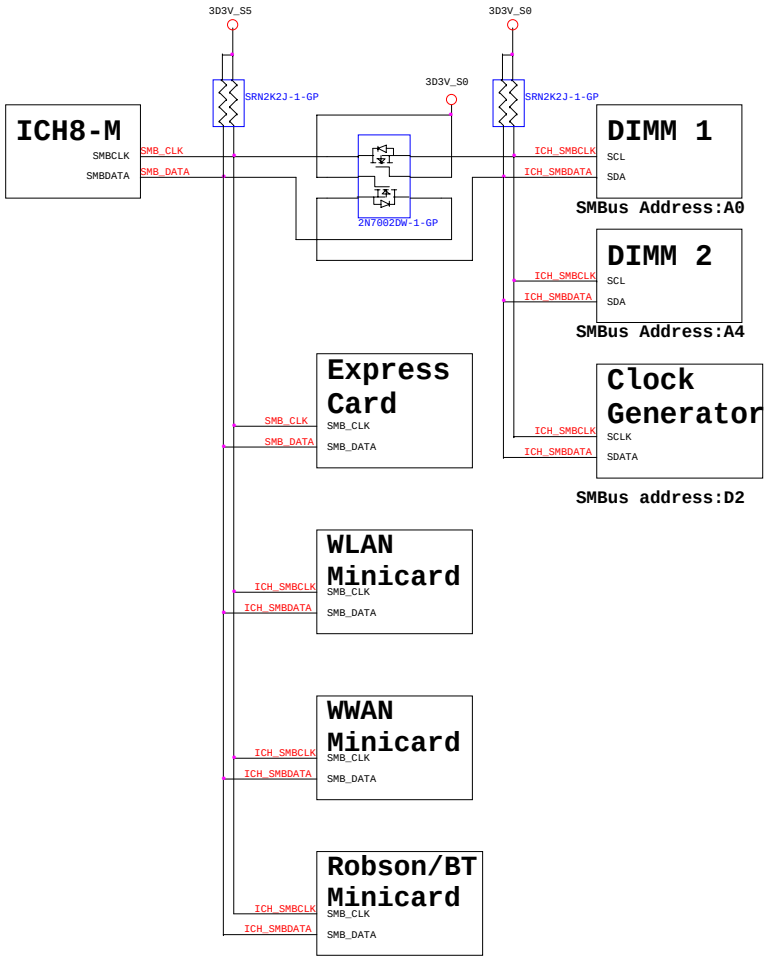
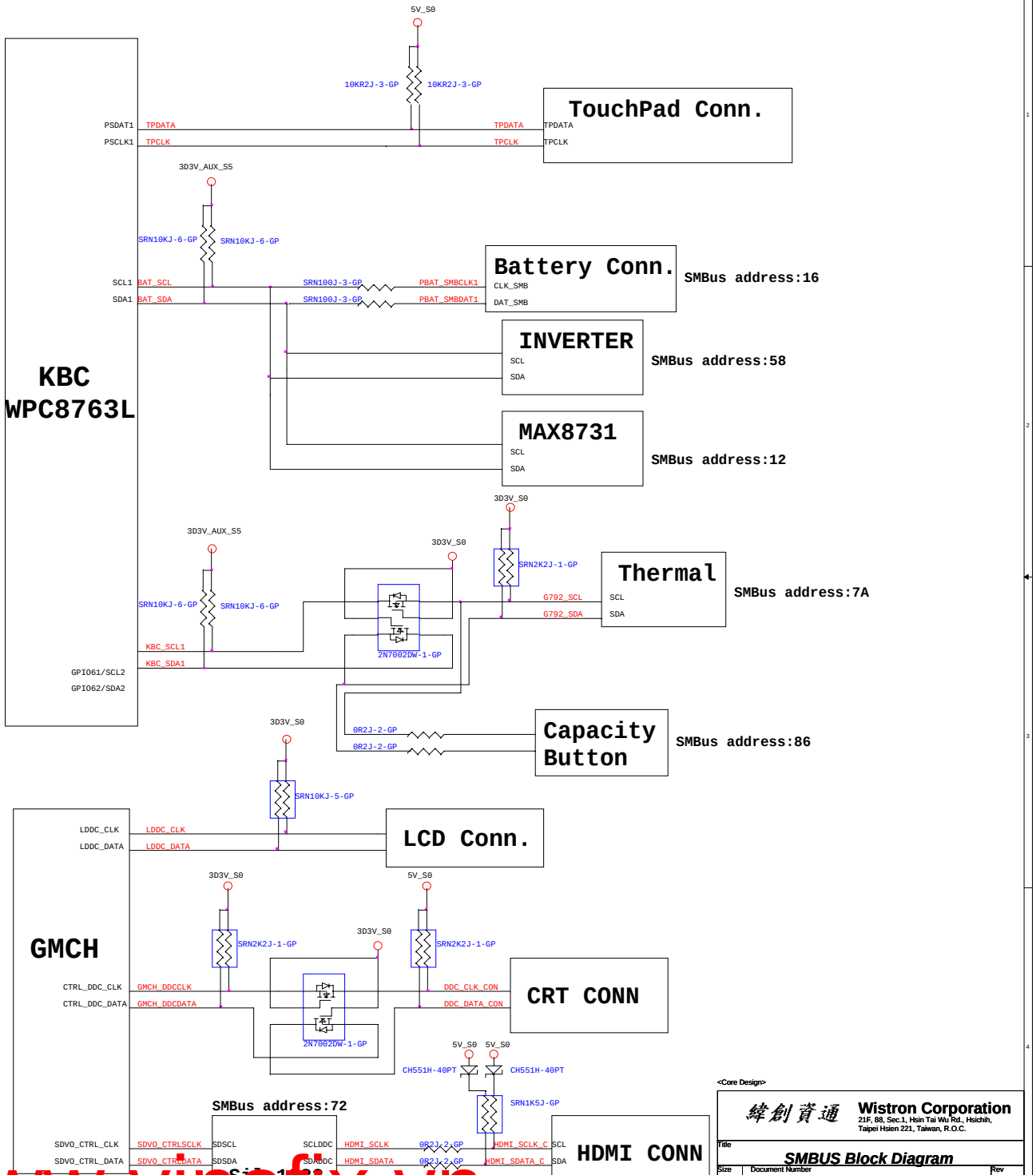
ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>
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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

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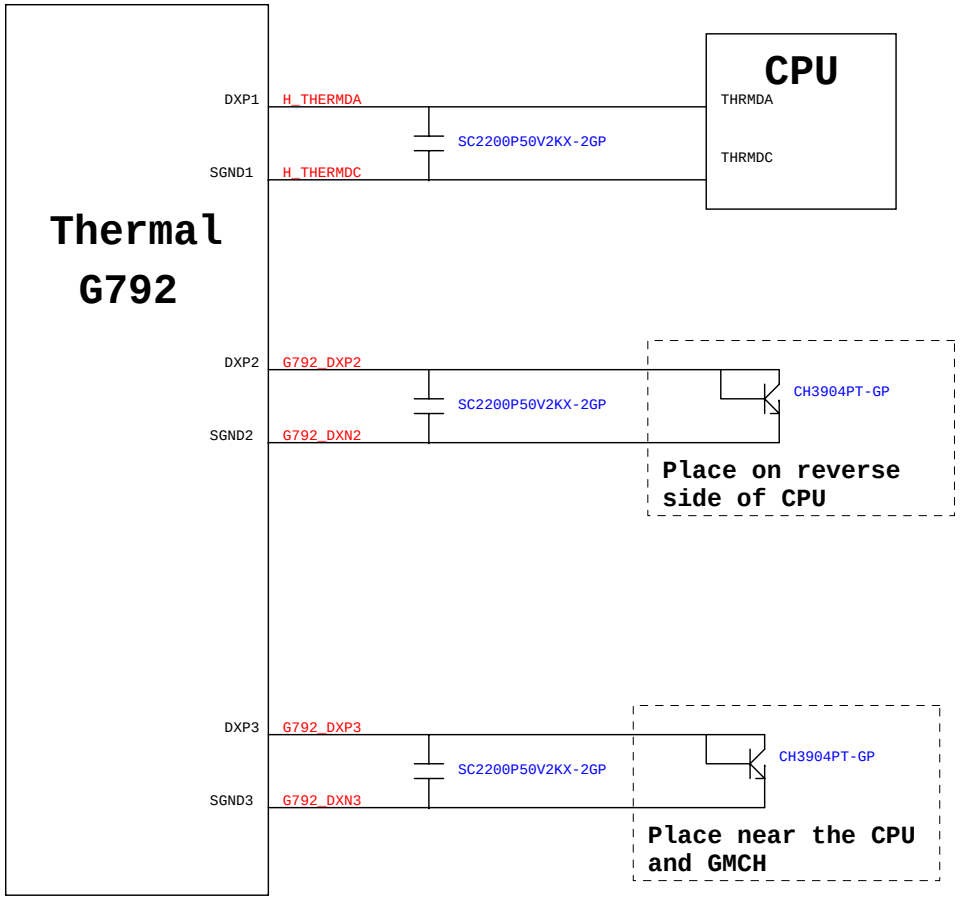
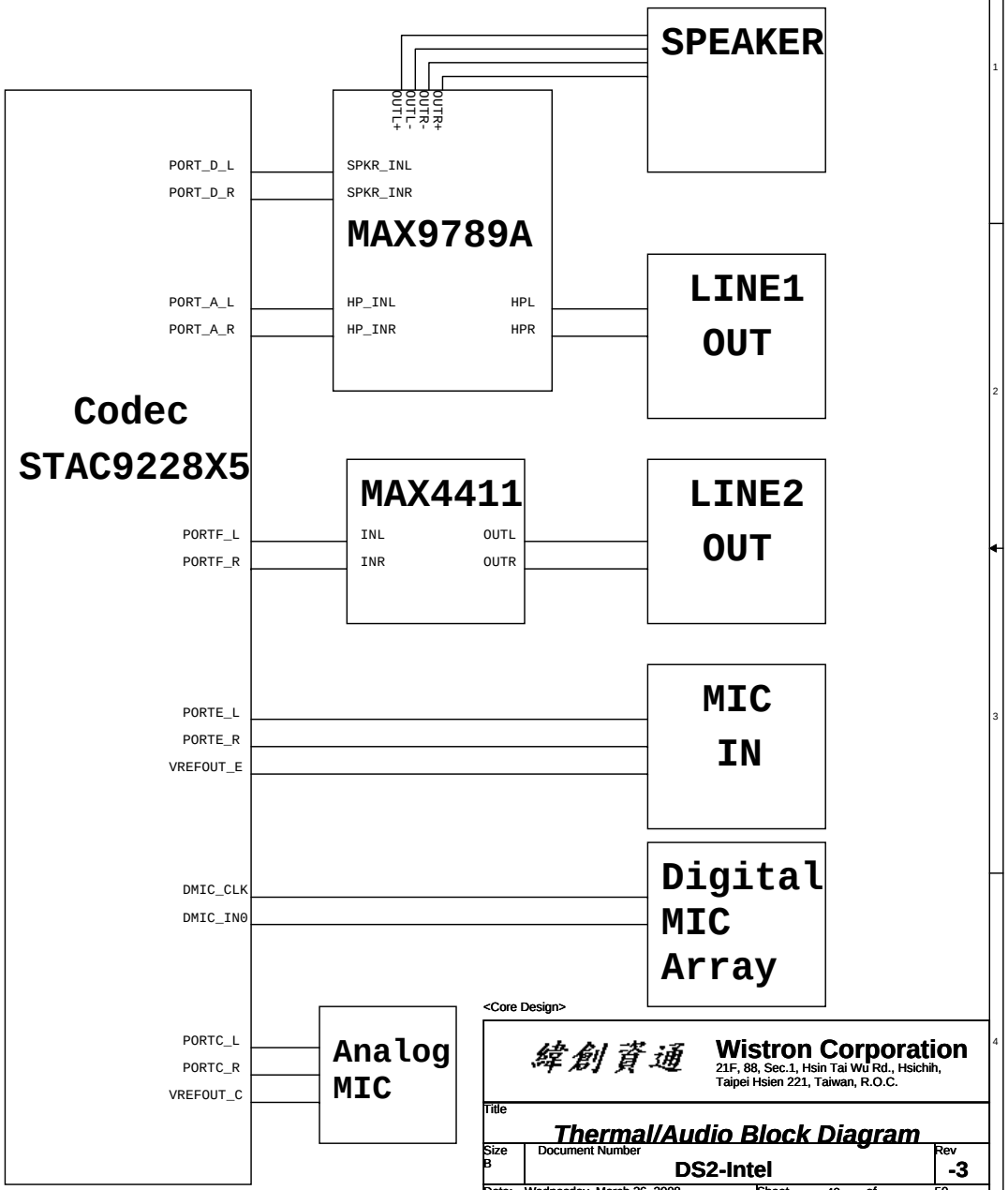
Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

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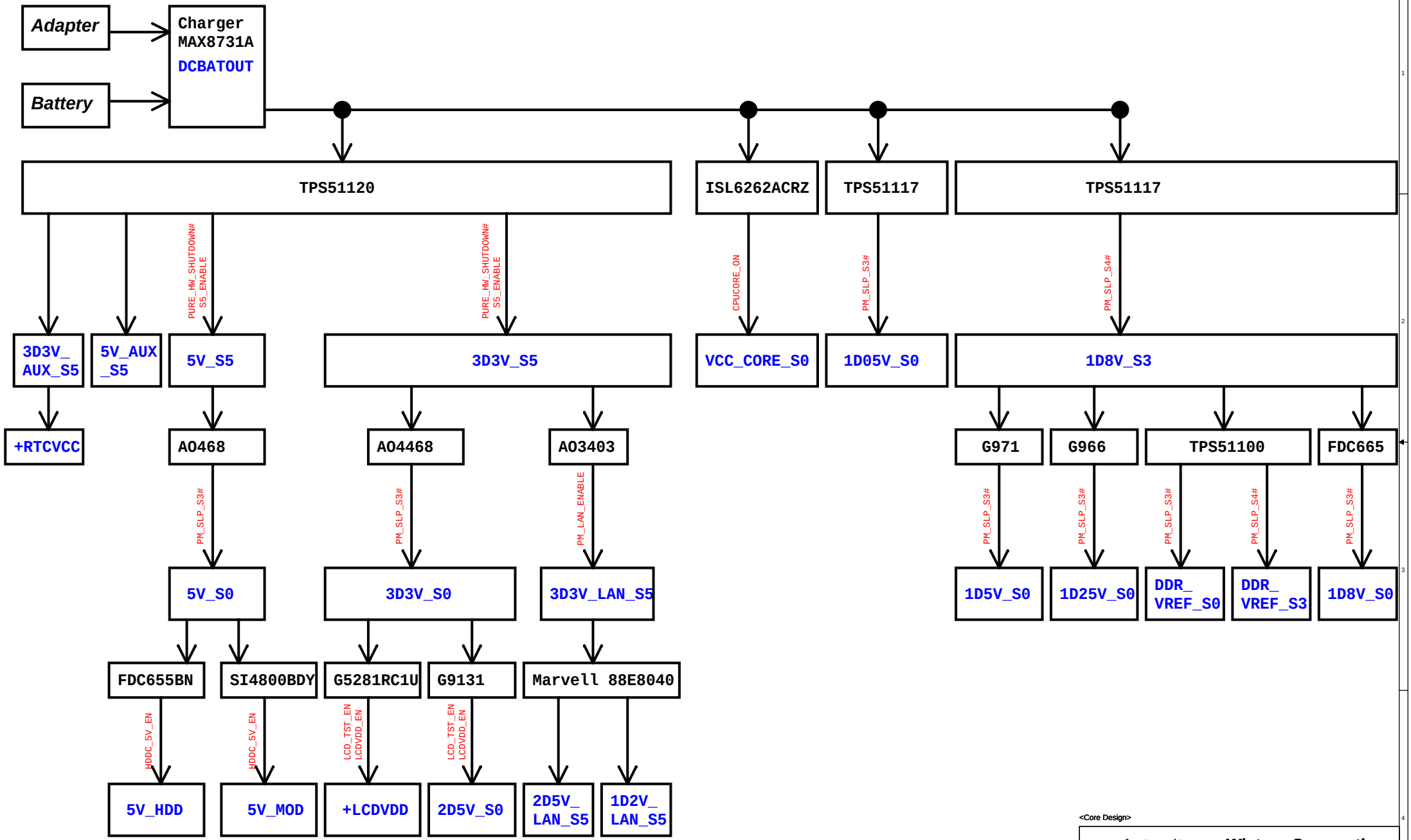

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

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