GA-78LMT-S2

Revision : 1.12

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Model Name:GA-78LMT-S2

Component value change history

Version: 1.12

P-Code: U99098-0

Date	Change Item		Reason
2012.03.12	E_BOM Release.	PCB: 0.1	Modify from 78LMT-S2P 5.02
2012.04.13	10A P_BOM Release.	PCB: 1.0	change P-BOM to 10A
2012.05.11	10B P_BOM Release.	PCB: 1.0	remove Q12 (MOS_OT BIOS OFF)
2012.07.02	11A P_BOM Release.	PCB: 1.1	Add COM port pin-header
2012.07.12	11B P_BOM Release.	PCB: 1.11	Add Erp for 0.5W Requirement
2012.08.08	11C P_BOM Release.	PCB: 1.11	DU3 change 10TA1-313933-10R

Circuit or PCB layout change for next version

Date	Version	Change Item
2012.03.11	0.1 Gerber out	change From 78LMT-S2P 5.02 (RS760=RS780L)
2012.04.13	1.0 Gerber out	1. change PCB Ver 1.0 2. Add "RB" 文字面
2012.07.02	1.1 Gerber out	Change MOS_OT pin. Add COM port pin-header
2012.07.11	1.11 Gerber out	1. Add Erp Schematic for 0.5W Requirement (P22,P27)

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Title: BOM & PCB HISTORY

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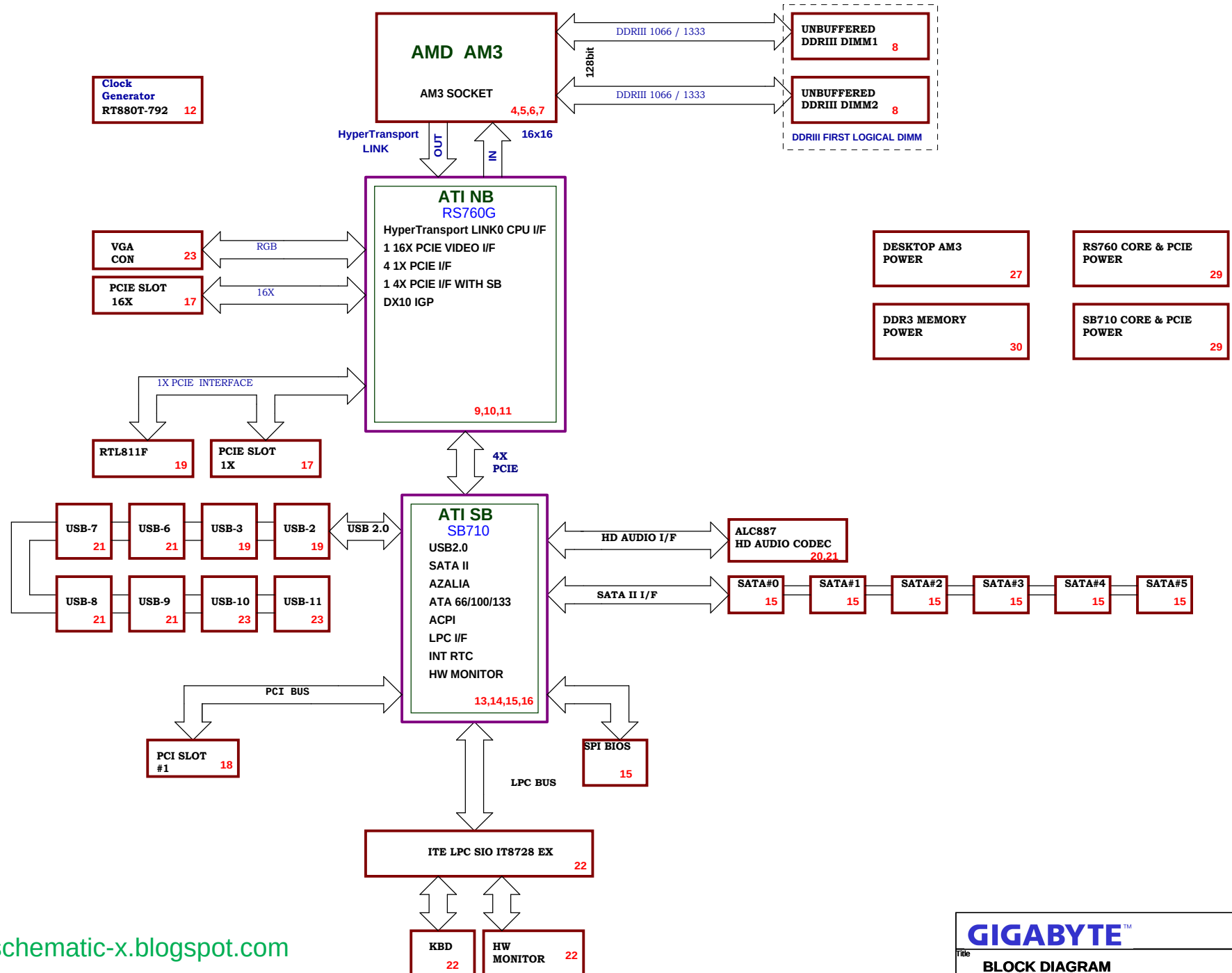
RS780L CUSTOMER DESKTOP DESIGN



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Title: BLOCK DIAGRAM		
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] <9>
L0_CADIN_H[0..15] L0_CADIN_H[0..15] <9>

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] <9>
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] <9>

M2CPUA

HYPERTRANSPORT

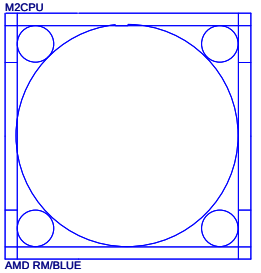
<9> L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 <9>
<9> L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 <9>
<9> L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 <9>
<9> L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 <9>
<9> L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 <9>
<9> L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 <9>
<9> L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 <9>
<9> L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 <9>
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AE5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPU



AMD RM/BLUE

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Title: CPU HYPER TRANSPORT		
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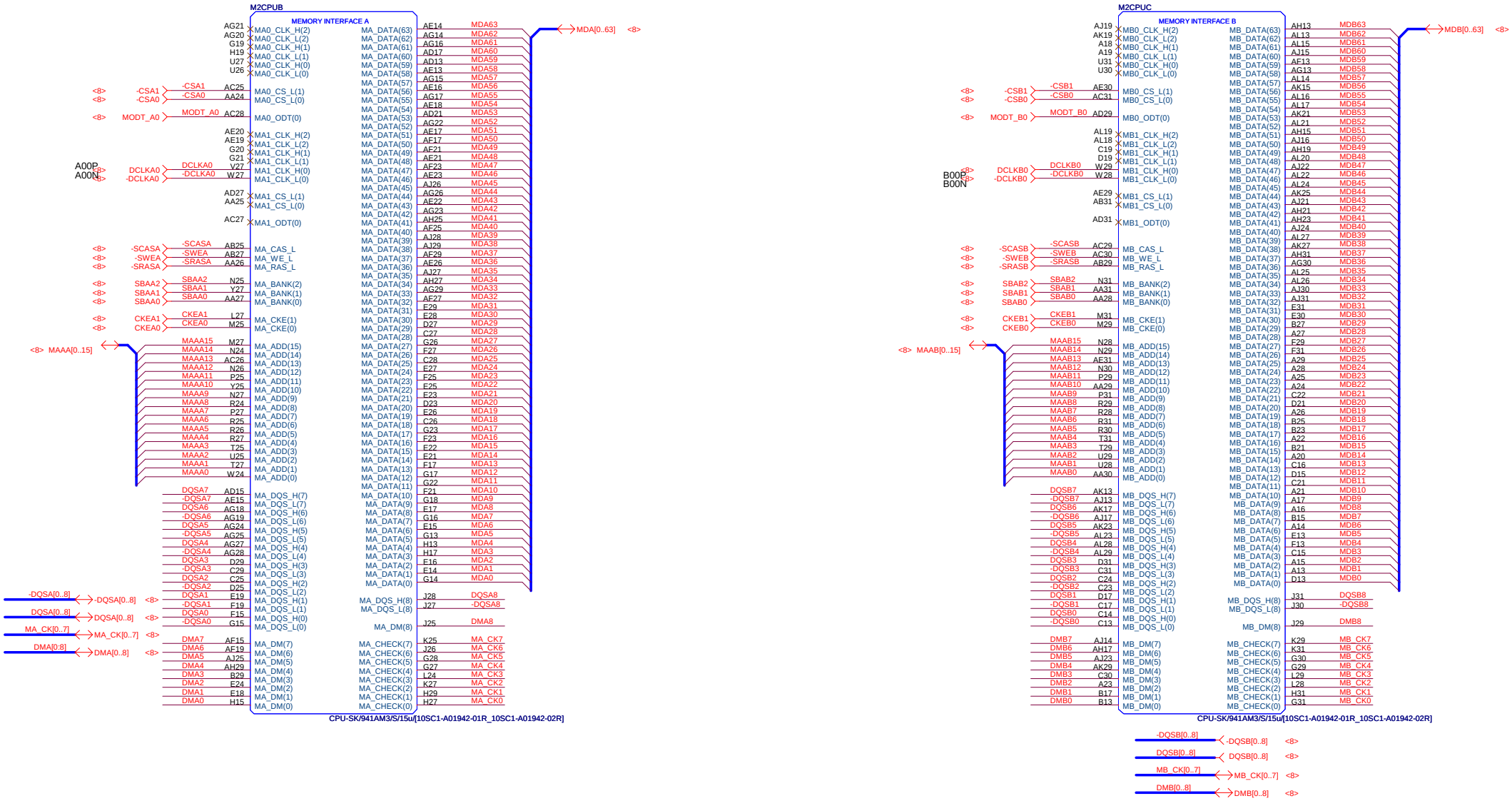

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Title: CPU DDRII MEMORY		
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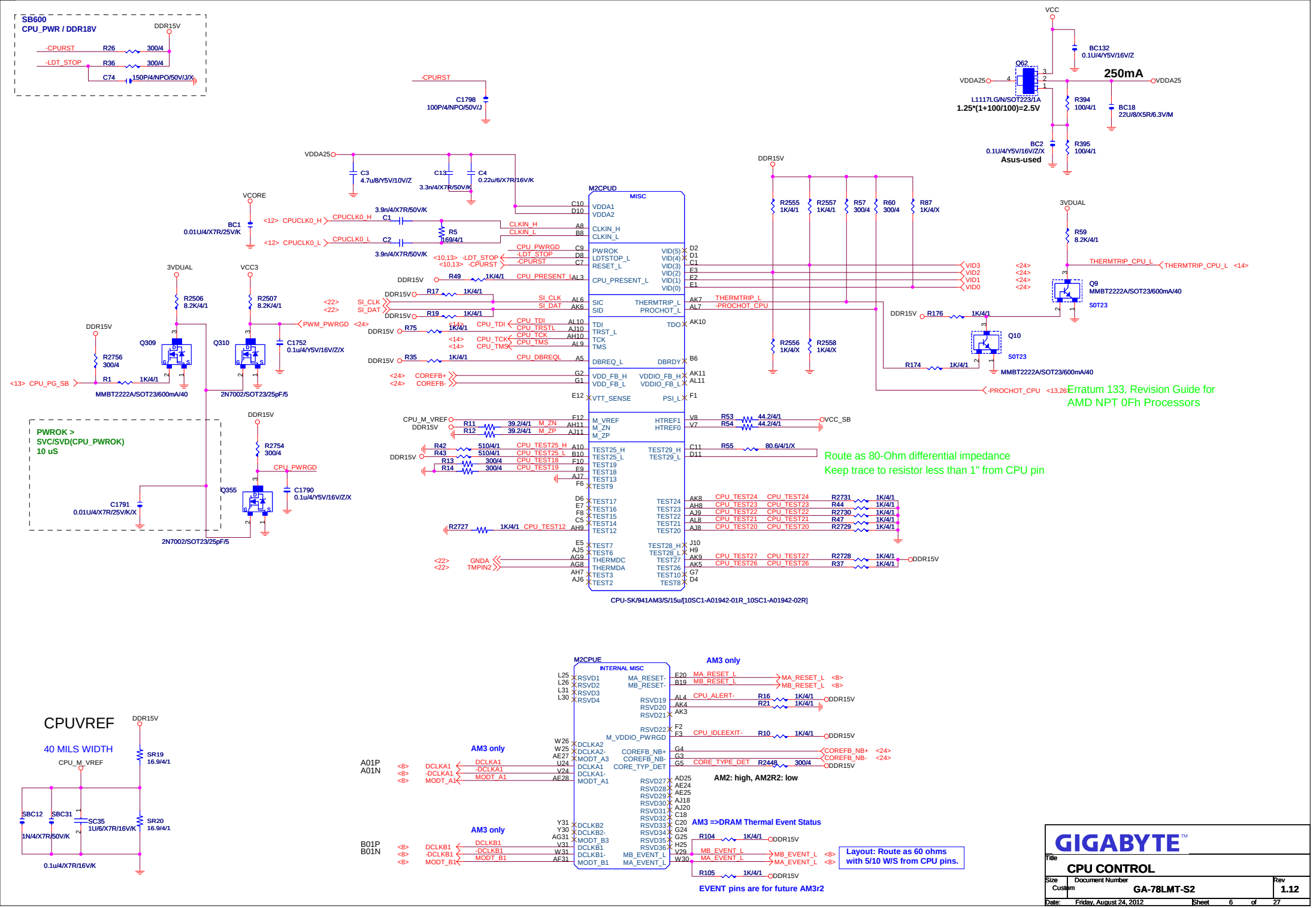
SB600
CPU_PWR / DDR18V
DDR15V
-CPURST
R26
300/4
-LDT_STOP
R36
300/4
C74
150P/4/NPO/50V/J/X
C1798
100P/4/NPO/50V/J
VCC
BC132
0.1U/4/Y5V/16V/Z
Q62
250mA
VDDA25
L1117LG/N/SOT223/1A
1.25*(1+100/100)=2.5V
R394
100/4/1
BC18
22U/8/X5R/6.3V/M
BC2
0.1U/4/Y5V/16V/Z/X
Asus-used
R395
100/4/1
VDDA25
C3
4.7u/8/Y5V/10V/Z
C13
3.3n/4/X7R/50V/K
C4
0.22u/6/X7R/16V/K
VCORE
BC1
0.01U/4/X7R/25V/K
3.9n/4/X7R/50V/K
C1
C2
3.9n/4/X7R/50V/K
R5
169/4/1
CPUCLK0_H
CPUCLK0_L
M2CPUD
MISC
VDDA1
VDDA2
CLKIN_H
CLKIN_L
PWROK
LDTSTOP_L
RESET_L
CPU_PRESENT_L
SIC
SID
TDI
TRST_L
TCK
TMS
DBREQ_L
DBRDY
VDD_FB_H
VDD_FB_L
VTT_SENSE
VDDIO_FB_H
VDDIO_FB_L
PSI_L
TDO
M_VREF
M_ZN
M_ZP
HTREF1
HTREF0
TEST25_H
TEST25_L
TEST19
TEST18
TEST13
TEST9
TEST29_H
TEST29_L
TEST17
TEST16
TEST15
TEST14
TEST12
TEST24
TEST23
TEST22
TEST21
TEST20
TEST7
TEST6
THERMDC
THERMDA
TEST3
TEST2
TEST28_H
TEST28_L
TEST27
TEST26
TEST10
TEST8
THERMTRIP_L
PROCHOT_L
VID(5)
VID(4)
VID(3)
VID(2)
VID(1)
VID(0)
CPU-SK/941AM3/S/15u/[10SC1-A01942-01R_10SC1-A01942-02R]
R2555
1K/4/1
R2557
1K/4/1
R57
300/4
R60
300/4
R87
1K/4/X
R2556
1K/4/X
R2558
1K/4/X
3VDUAL
R59
8.2K/4/1
Q9
MMBT2222A/SOT23/600mA/40
SOT23
Q10
MMBT2222A/SOT23/600mA/40
R176
1K/4/1
R174
1K/4/1
THERMTRIP_CPU_L
-PROCHOT_CPU
Erratum 133, Revision Guide for
AMD NPT 0Fh Processors
R2506
8.2K/4/1
R2507
8.2K/4/1
PWM_PWRGD
Q309
Q310
C1752
0.1u/4/Y5V/16V/Z/X
R2756
300/4
R1
1K/4/1
CPU_PG_SB
MMBT2222A/SOT23/600mA/40
2N7002/SOT23/25pF/5
PWROK >
SVC/SVD(CPU_PWROK)
10 uS
R2754
300/4
CPU_PWRGD
Q355
C1790
0.1u/4/Y5V/16V/Z/X
C1791
0.01U/4/X7R/25V/K/X
2N7002/SOT23/25pF/5
SI_CLK
SI_DAT
CPU_PRESENT_L
CPU_TDI
CPU_TRSTL
CPU_TCK
CPU_TMS
CPU_DBREQL
COREFB+
COREFB-
CPU_M_VREF
M_ZN
M_ZP
R11
39.2/4/1
R12
39.2/4/1
R53
44.2/4/1
R54
44.2/4/1
VCC_SB
R42
510/4/1
R43
510/4/1
R13
300/4
R14
300/4
CPU_TEST25_H
CPU_TEST25_L
CPU_TEST18
CPU_TEST19
CPU_TEST12
R55
80.6/4/1/X
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
CPU_TEST24
CPU_TEST23
CPU_TEST22
CPU_TEST21
CPU_TEST20
R2731
R44
R2730
R47
R2729
CPU_TEST27
CPU_TEST26
R2728
R37
GNDA
TMPIN2
M2CPUE
INTERNAL MISC
AM3 only
RSVD1
RSVD2
RSVD3
RSVD4
MA_RESET-
MB_RESET-
MA_RESET_L
MB_RESET_L
CPU_ALERT-
R16
R21
RSVD19
RSVD20
RSVD21
RSVD22
M_VDDIO_PWRGD
CPU_IDLEEXIT-
R10
DCLKA2
DCLKA2-
MODT_A3
DCLKA1
DCLKA1-
MODT_A1
COREFB_NB+
COREFB_NB-
CORE_TYP_DET
CORE_TYPE_DET
R2448
300/4
AM2: high, AM2R2: low
RSVD27
RSVD28
RSVD29
RSVD30
RSVD31
RSVD32
RSVD33
RSVD34
RSVD35
RSVD36
AM3 =>DRAM Thermal Event Status
DCLKB2
DCLKB2-
MODT_B3
DCLKB1
DCLKB1-
MODT_B1
MB_EVENT_L
MA_EVENT_L
R104
R105
Layout: Route as 60 ohms
with 5/10 W/S from CPU pins.
EVENT pins are for future AM3r2
A01P
A01N
B01P
B01N
DCLKA1
-DCLKA1
MODT_A1
DCLKB1
-DCLKB1
MODT_B1
CPUVREF
40 MILS WIDTH
CPU_M_VREF
SR19
16.9/4/1
SR20
16.9/4/1
SBC12
1N/4/X7R/50V/K
SBC31
SC35
1U/6/X7R/16V/K
0.1u/4/X7R/16V/K
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CPU CONTROL
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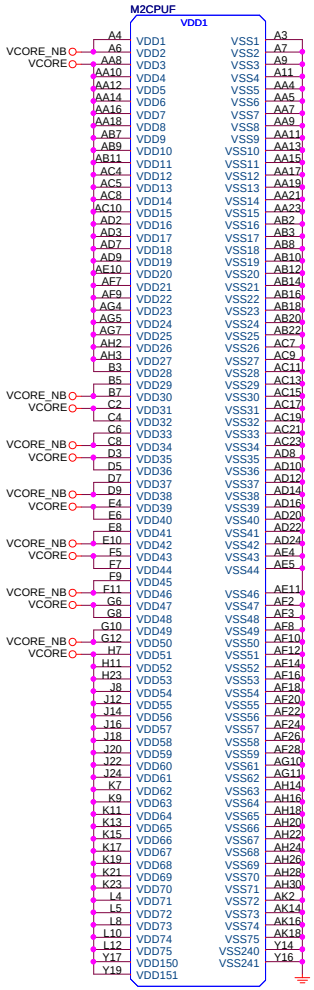
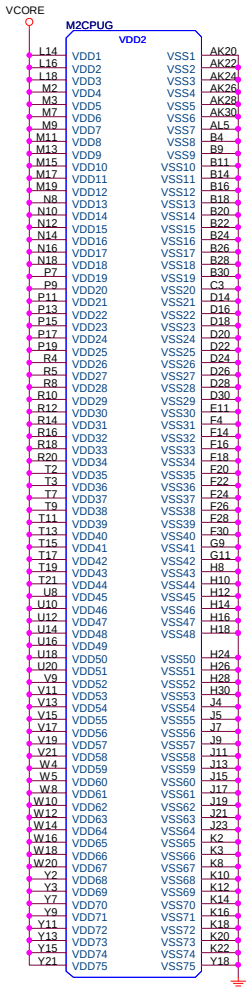
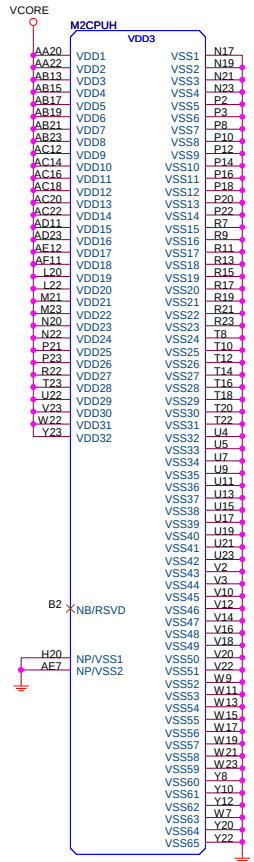
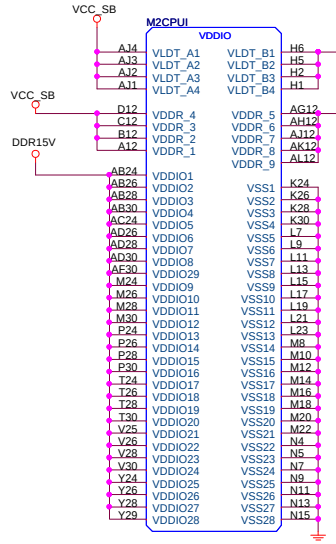
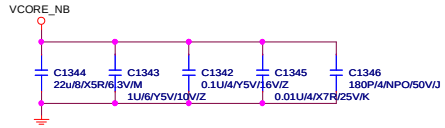
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

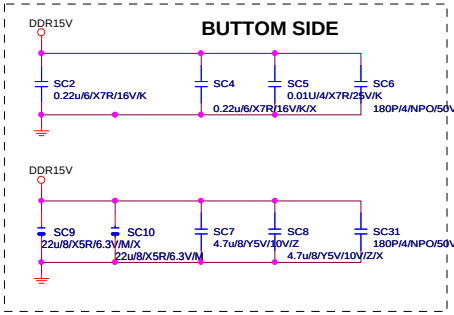


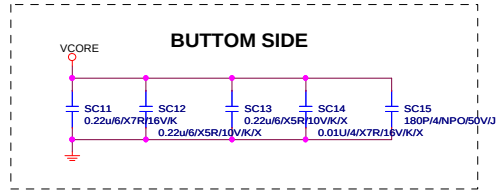


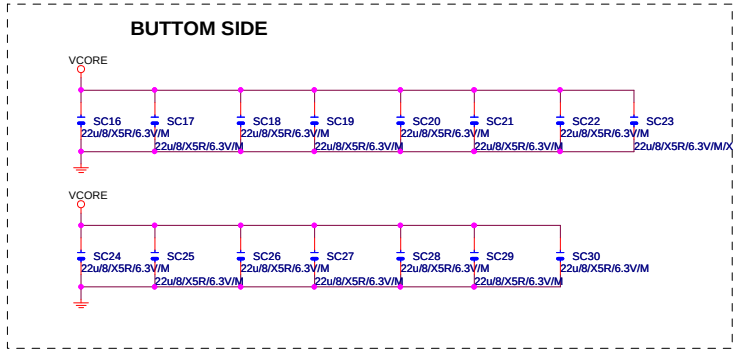


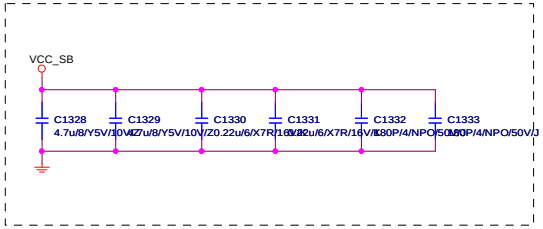


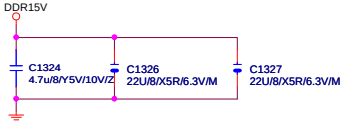


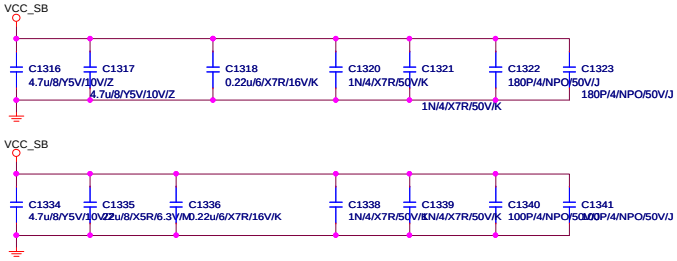


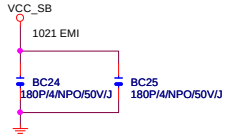












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Title: CPU POWER & GND		
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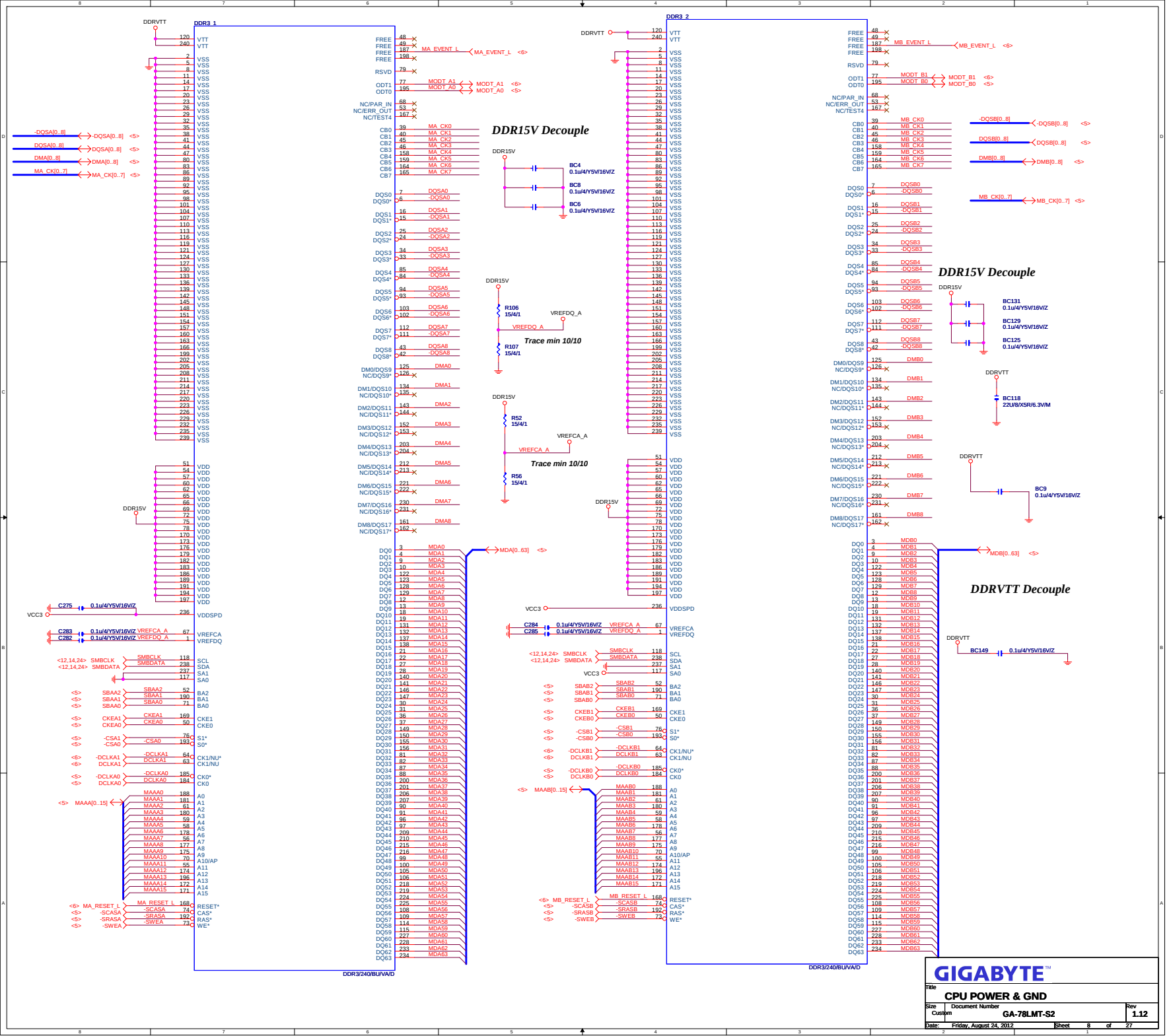

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Title	CPU POWER & GND		
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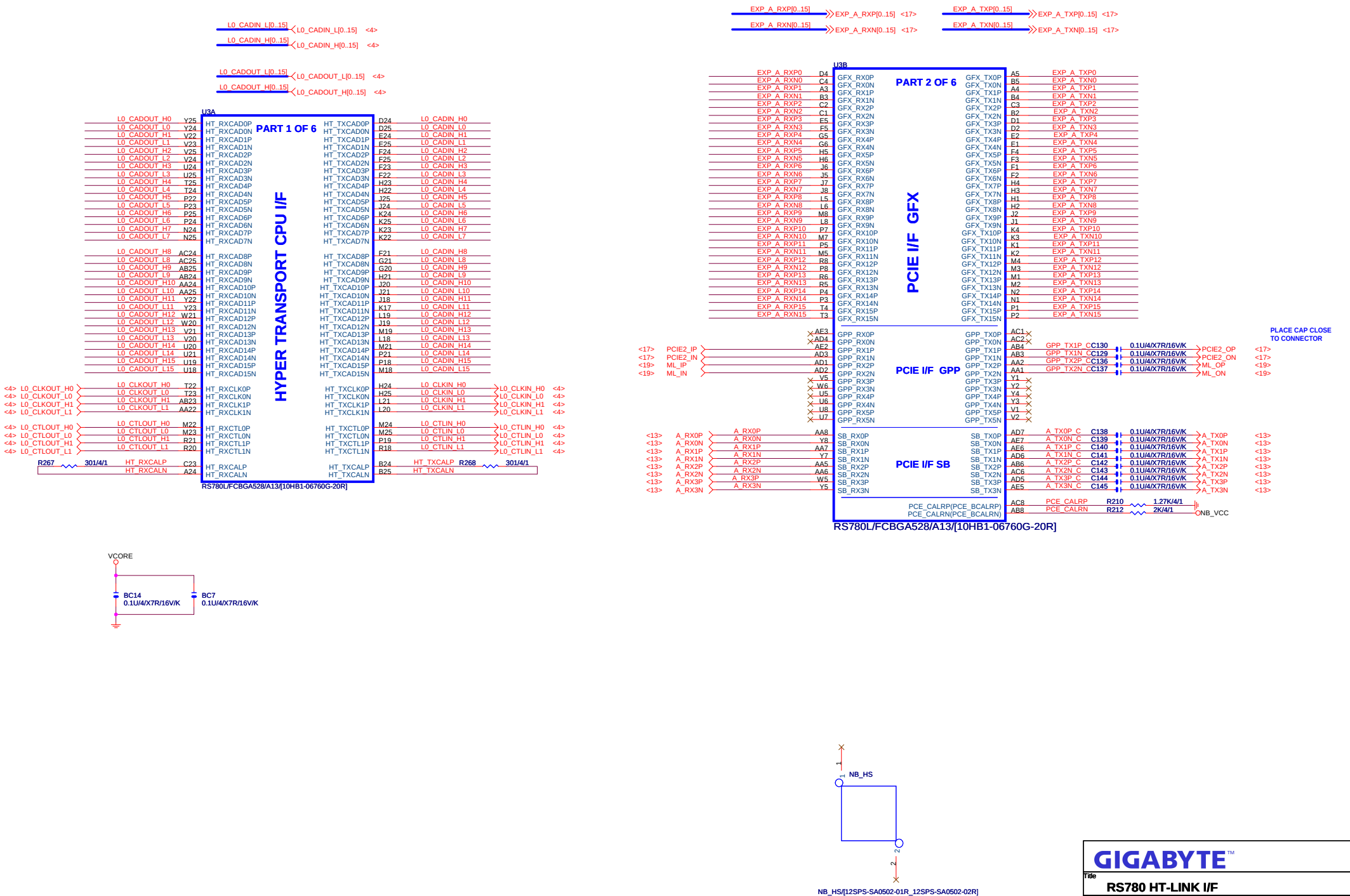
Date: Friday, August 24, 2012	Sheet 8 of 27		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L0_CADIN_L[0..15] <4>
L0_CADIN_H[0..15]
L0_CADIN_H[0..15] <4>
L0_CADOUT_L[0..15]
L0_CADOUT_L[0..15] <4>
L0_CADOUT_H[0..15]
L0_CADOUT_H[0..15] <4>
U3A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
L0_CADOUT_H0 Y25
L0_CADOUT_L0 Y24
L0_CADOUT_H1 V22
L0_CADOUT_L1 V23
L0_CADOUT_H2 V25
L0_CADOUT_L2 V24
L0_CADOUT_H3 U24
L0_CADOUT_L3 U25
L0_CADOUT_H4 T25
L0_CADOUT_L4 T24
L0_CADOUT_H5 P22
L0_CADOUT_L5 P23
L0_CADOUT_H6 P25
L0_CADOUT_L6 P24
L0_CADOUT_H7 N24
L0_CADOUT_L7 N25
L0_CADOUT_H8 AC24
L0_CADOUT_L8 AC25
L0_CADOUT_H9 AB25
L0_CADOUT_L9 AB24
L0_CADOUT_H10 AA24
L0_CADOUT_L10 AA25
L0_CADOUT_H11 Y22
L0_CADOUT_L11 Y23
L0_CADOUT_H12 W21
L0_CADOUT_L12 W20
L0_CADOUT_H13 V21
L0_CADOUT_L13 V20
L0_CADOUT_H14 U20
L0_CADOUT_L14 U21
L0_CADOUT_H15 U19
L0_CADOUT_L15 U18
HT_RXCAD0P HT_RXCAD0N HT_RXCAD1P HT_RXCAD1N HT_RXCAD2P HT_RXCAD2N HT_RXCAD3P HT_RXCAD3N HT_RXCAD4P HT_RXCAD4N HT_RXCAD5P HT_RXCAD5N HT_RXCAD6P HT_RXCAD6N HT_RXCAD7P HT_RXCAD7N
HT_RXCAD8P HT_RXCAD8N HT_RXCAD9P HT_RXCAD9N HT_RXCAD10P HT_RXCAD10N HT_RXCAD11P HT_RXCAD11N HT_RXCAD12P HT_RXCAD12N HT_RXCAD13P HT_RXCAD13N HT_RXCAD14P HT_RXCAD14N HT_RXCAD15P HT_RXCAD15N
HT_TXCAD0P HT_TXCAD0N HT_TXCAD1P HT_TXCAD1N HT_TXCAD2P HT_TXCAD2N HT_TXCAD3P HT_TXCAD3N HT_TXCAD4P HT_TXCAD4N HT_TXCAD5P HT_TXCAD5N HT_TXCAD6P HT_TXCAD6N HT_TXCAD7P HT_TXCAD7N
HT_TXCAD8P HT_TXCAD8N HT_TXCAD9P HT_TXCAD9N HT_TXCAD10P HT_TXCAD10N HT_TXCAD11P HT_TXCAD11N HT_TXCAD12P HT_TXCAD12N HT_TXCAD13P HT_TXCAD13N HT_TXCAD14P HT_TXCAD14N HT_TXCAD15P HT_TXCAD15N
D24 L0_CADIN_H0
D25 L0_CADIN_L0
E24 L0_CADIN_H1
E25 L0_CADIN_L1
F24 L0_CADIN_H2
F25 L0_CADIN_L2
F23 L0_CADIN_H3
F22 L0_CADIN_L3
H23 L0_CADIN_H4
H22 L0_CADIN_L4
J25 L0_CADIN_H5
J24 L0_CADIN_L5
K24 L0_CADIN_H6
K25 L0_CADIN_L6
K23 L0_CADIN_H7
K22 L0_CADIN_L7
F21 L0_CADIN_H8
G21 L0_CADIN_L8
G20 L0_CADIN_H9
H21 L0_CADIN_L9
J20 L0_CADIN_H10
J21 L0_CADIN_L10
J18 L0_CADIN_H11
K17 L0_CADIN_L11
L19 L0_CADIN_H12
J19 L0_CADIN_L12
M19 L0_CADIN_H13
L18 L0_CADIN_L13
M21 L0_CADIN_H14
P21 L0_CADIN_L14
P18 L0_CADIN_H15
M18 L0_CADIN_L15
<4> L0_CLKOUT_H0 L0_CLKOUT_H0 T22
<4> L0_CLKOUT_L0 L0_CLKOUT_L0 T23
<4> L0_CLKOUT_H1 L0_CLKOUT_H1 AB23
<4> L0_CLKOUT_L1 L0_CLKOUT_L1 AA22
HT_RXCLK0P HT_RXCLK0N HT_RXCLK1P HT_RXCLK1N
HT_TXCLK0P HT_TXCLK0N HT_TXCLK1P HT_TXCLK1N
H24 L0_CLKIN_H0 L0_CLKIN_H0 <4>
H25 L0_CLKIN_L0 L0_CLKIN_L0 <4>
L21 L0_CLKIN_H1 L0_CLKIN_H1 <4>
L20 L0_CLKIN_L1 L0_CLKIN_L1 <4>
<4> L0_CTLOUT_H0 L0_CTLOUT_H0 M22
<4> L0_CTLOUT_L0 L0_CTLOUT_L0 M23
<4> L0_CTLOUT_H1 L0_CTLOUT_H1 R21
<4> L0_CTLOUT_L1 L0_CTLOUT_L1 R20
HT_RXCTL0P HT_RXCTL0N HT_RXCTL1P HT_RXCTL1N
HT_TXCTL0P HT_TXCTL0N HT_TXCTL1P HT_TXCTL1N
M24 L0_CTLIN_H0 L0_CTLIN_H0 <4>
M25 L0_CTLIN_L0 L0_CTLIN_L0 <4>
P19 L0_CTLIN_H1 L0_CTLIN_H1 <4>
R18 L0_CTLIN_L1 L0_CTLIN_L1 <4>
R267 301/4/1 HT_RXCALP C23
HT_RXCALN A24
HT_RXCALP HT_RXCALN
B24 HT_TXCALP R268 301/4/1
B25 HT_TXCALN
HT_TXCALP HT_TXCALN
VCORE
BC14 0.1U/4/X7R/16V/K
BC7 0.1U/4/X7R/16V/K
EXP_A_RXP[0..15]
EXP_A_RXP[0..15] <17>
EXP_A_RXN[0..15]
EXP_A_RXN[0..15] <17>
EXP_A_TXP[0..15]
EXP_A_TXP[0..15] <17>
EXP_A_TXN[0..15]
EXP_A_TXN[0..15] <17>
U3B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
EXP_A_RXP0 D4
EXP_A_RXN0 C4
EXP_A_RXP1 A3
EXP_A_RXN1 B3
EXP_A_RXP2 C2
EXP_A_RXN2 C1
EXP_A_RXP3 E5
EXP_A_RXN3 E5
EXP_A_RXP4 G5
EXP_A_RXN4 G6
EXP_A_RXP5 H5
EXP_A_RXN5 H6
EXP_A_RXP6 J6
EXP_A_RXN6 J5
EXP_A_RXP7 J7
EXP_A_RXN7 J8
EXP_A_RXP8 L5
EXP_A_RXN8 L6
EXP_A_RXP9 M8
EXP_A_RXN9 L8
EXP_A_RXP10 P7
EXP_A_RXN10 M7
EXP_A_RXP11 P5
EXP_A_RXN11 M5
EXP_A_RXP12 P8
EXP_A_RXN12 P8
EXP_A_RXP13 R6
EXP_A_RXN13 R5
EXP_A_RXP14 P4
EXP_A_RXN14 P3
EXP_A_RXP15 T4
EXP_A_RXN15 T3
GFX_RX0P GFX_RX0N GFX_RX1P GFX_RX1N GFX_RX2P GFX_RX2N GFX_RX3P GFX_RX3N GFX_RX4P GFX_RX4N GFX_RX5P GFX_RX5N GFX_RX6P GFX_RX6N GFX_RX7P GFX_RX7N GFX_RX8P GFX_RX8N GFX_RX9P GFX_RX9N GFX_RX10P GFX_RX10N GFX_RX11P GFX_RX11N GFX_RX12P GFX_RX12N GFX_RX13P GFX_RX13N GFX_RX14P GFX_RX14N GFX_RX15P GFX_RX15N
GFX_TX0P GFX_TX0N GFX_TX1P GFX_TX1N GFX_TX2P GFX_TX2N GFX_TX3P GFX_TX3N GFX_TX4P GFX_TX4N GFX_TX5P GFX_TX5N GFX_TX6P GFX_TX6N GFX_TX7P GFX_TX7N GFX_TX8P GFX_TX8N GFX_TX9P GFX_TX9N GFX_TX10P GFX_TX10N GFX_TX11P GFX_TX11N GFX_TX12P GFX_TX12N GFX_TX13P GFX_TX13N GFX_TX14P GFX_TX14N GFX_TX15P GFX_TX15N
A5 EXP_A_TXP0
B5 EXP_A_TXN0
A4 EXP_A_TXP1
B4 EXP_A_TXN1
C3 EXP_A_TXP2
B2 EXP_A_TXN2
D1 EXP_A_TXP3
D2 EXP_A_TXN3
E2 EXP_A_TXP4
E1 EXP_A_TXN4
F4 EXP_A_TXP5
F3 EXP_A_TXN5
F1 EXP_A_TXP6
F2 EXP_A_TXN6
H4 EXP_A_TXP7
H3 EXP_A_TXN7
H1 EXP_A_TXP8
H2 EXP_A_TXN8
J2 EXP_A_TXP9
J1 EXP_A_TXN9
K4 EXP_A_TXP10
K3 EXP_A_TXN10
K1 EXP_A_TXP11
K2 EXP_A_TXN11
M4 EXP_A_TXP12
M3 EXP_A_TXN12
M1 EXP_A_TXP13
M2 EXP_A_TXN13
N2 EXP_A_TXP14
N1 EXP_A_TXN14
P1 EXP_A_TXP15
P2 EXP_A_TXN15
GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N GPP_RX4P GPP_RX4N GPP_RX5P GPP_RX5N
GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N GPP_TX4P GPP_TX4N GPP_TX5P GPP_TX5N
AE3 AD4 AE2 AD3 AD1 AD2 V5 W6 U5 U6 U8 U7
AC1 AC2 AB4 AB3 AA2 AA1 Y1 Y2 Y4 Y3 V1 V2
<17> PCIE2_IP
<17> PCIE2_IN
<19> ML_IP
<19> ML_IN
GPP_TX1P_C C130 0.1U/4/X7R/16V/K PCIE2_OP <17>
GPP_TX1N_C C129 0.1U/4/X7R/16V/K PCIE2_ON <17>
GPP_TX2P_C C136 0.1U/4/X7R/16V/K ML_OP <19>
GPP_TX2N_C C137 0.1U/4/X7R/16V/K ML_ON <19>
PLACE CAP CLOSE TO CONNECTOR
SB_RX0P SB_RX0N SB_RX1P SB_RX1N SB_RX2P SB_RX2N SB_RX3P SB_RX3N
SB_TX0P SB_TX0N SB_TX1P SB_TX1N SB_TX2P SB_TX2N SB_TX3P SB_TX3N
A_RX0P AA8
A_RX0N Y8
A_RX1P AA7
A_RX1N Y7
A_RX2P AA5
A_RX2N AA6
A_RX3P W5
A_RX3N Y5
<13> A_RX0P
<13> A_RX0N
<13> A_RX1P
<13> A_RX1N
<13> A_RX2P
<13> A_RX2N
<13> A_RX3P
<13> A_RX3N
AD7 A_TX0P_C C138 0.1U/4/X7R/16V/K A_TX0P <13>
AE7 A_TX0N_C C139 0.1U/4/X7R/16V/K A_TX0N <13>
AE6 A_TX1P_C C140 0.1U/4/X7R/16V/K A_TX1P <13>
AD6 A_TX1N_C C141 0.1U/4/X7R/16V/K A_TX1N <13>
AB6 A_TX2P_C C142 0.1U/4/X7R/16V/K A_TX2P <13>
AC6 A_TX2N_C C143 0.1U/4/X7R/16V/K A_TX2N <13>
AD5 A_TX3P_C C144 0.1U/4/X7R/16V/K A_TX3P <13>
AE5 A_TX3N_C C145 0.1U/4/X7R/16V/K A_TX3N <13>
PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)
AC8 PCE_CALRP R210 1.27K/4/1
AB8 PCE_CALRN R212 2K/4/1
NB_VCC
NB_HS
NB_HS/[12SPS-SA0502-01R_12SPS-SA0502-02R]
GIGABYTE™
Title
RS780 HT-LINK I/F
Size Custom
Document Number GA-78LMT-S2
Rev 1.12
Date: Friday, August 24, 2012
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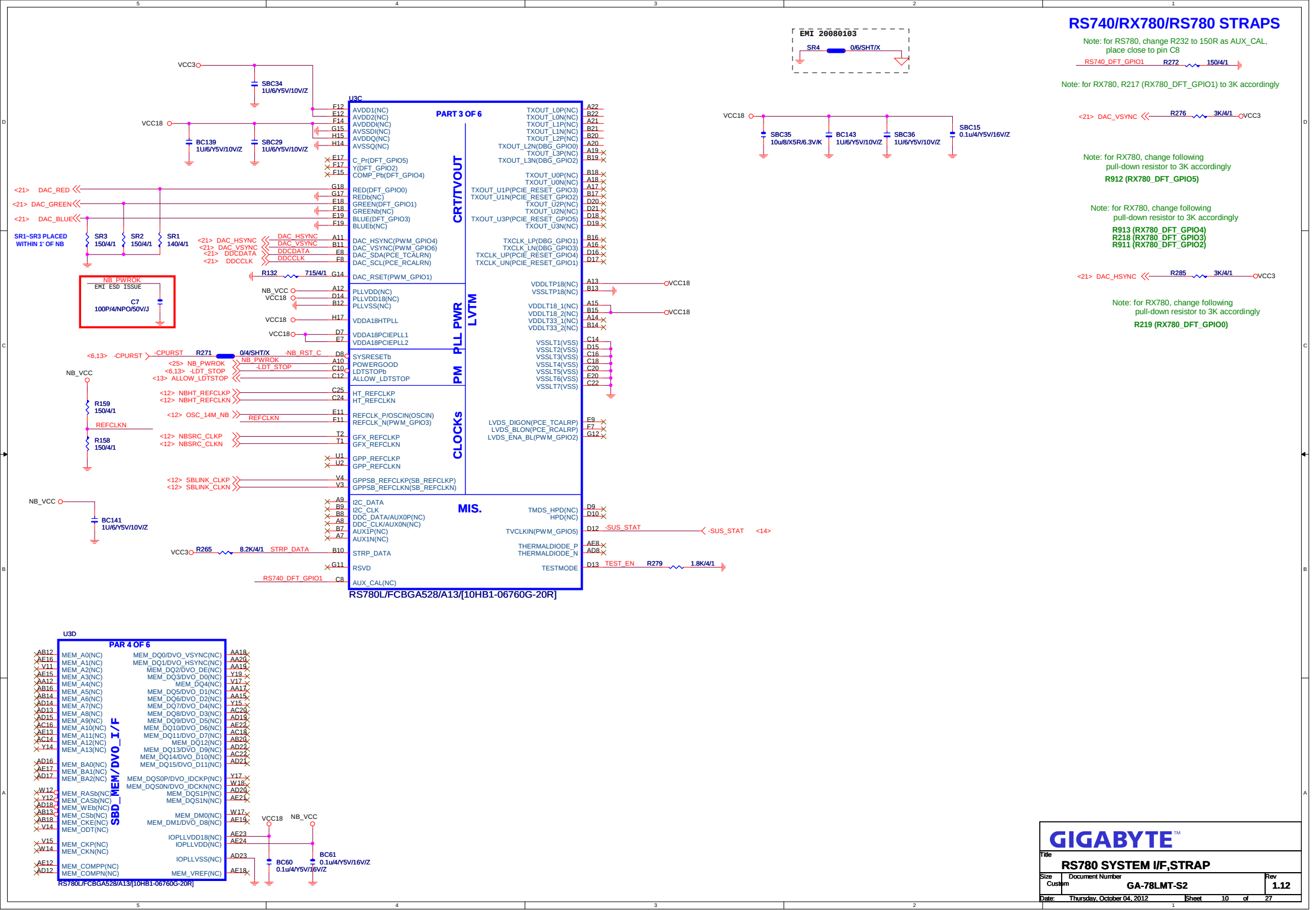

RS740/RX780/RS780 STRAPS
Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8
RS740_DFT_GPIO1 R272 150/4/1
Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly
<21> DAC_VSYNC R276 3K/4/1 VCC3
Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780_DFT_GPIO5)
Note: for RX780, change following pull-down resistor to 3K accordingly
R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)
<21> DAC_HSYNC R285 3K/4/1 VCC3
Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)
EMI 20080103
SR4 0/6/SHT/X
VCC3
SBC34 1U/6/Y5V/10V/Z
VCC18
BC139 1U/6/Y5V/10V/Z
SBC29 1U/6/Y5V/10V/Z
U3C
PART 3 OF 6
AVDD1(NC)
AVDD2(NC)
AVDDDI(NC)
AVSSDI(NC)
AVDDQ(NC)
AVSSQ(NC)
C_Pr(DFT_GPIO5)
Y(DFT_GPIO2)
COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0)
REDb(NC)
GREEN(DFT_GPIO1)
GREENb(NC)
BLUE(DFT_GPIO3)
BLUEb(NC)
DAC_HSYNC(PWM_GPIO4)
DAC_VSYNC(PWM_GPIO6)
DAC_SDA(PCE_TCALRN)
DAC_SCL(PCE_RCALRN)
DAC_RSET(PWM_GPIO1)
CRT/TVOUT
TXOUT_L0P(NC)
TXOUT_L0N(NC)
TXOUT_L1P(NC)
TXOUT_L1N(NC)
TXOUT_L2P(NC)
TXOUT_L2N(DBG_GPIO0)
TXOUT_L3P(NC)
TXOUT_L3N(DBG_GPIO2)
TXOUT_U0P(NC)
TXOUT_U0N(NC)
TXOUT_U1P(PCIE_RESET_GPIO3)
TXOUT_U1N(PCIE_RESET_GPIO2)
TXOUT_U2P(NC)
TXOUT_U2N(NC)
TXOUT_U3P(PCIE_RESET_GPIO5)
TXOUT_U3N(NC)
TXCLK_LP(DBG_GPIO1)
TXCLK_LN(DBG_GPIO3)
TXCLK_UP(PCIE_RESET_GPIO4)
TXCLK_UN(PCIE_RESET_GPIO1)
<21> DAC_RED
<21> DAC_GREEN
<21> DAC_BLUE
SR1~SR3 PLACED WITHIN 1' OF NB
SR3 150/4/1
SR2 150/4/1
SR1 140/4/1
<21> DAC_HSYNC
<21> DAC_VSYNC
<21> DDCDATA
<21> DDCCLK
R132 715/4/1
NB_PWROK
EMI ESD ISSUE
C7 100P/4/NPO/50V/J
NB_VCC
VCC18
PLL PWR
PLLVDD(NC)
PLLVDD18(NC)
PLLVSS(NC)
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
LVTM
VDDLTP18(NC)
VSSLTP18(NC)
VDDLT18_1(NC)
VDDLT18_2(NC)
VDDLT33_1(NC)
VDDLT33_2(NC)
VSSLT1(VSS)
VSSLT2(VSS)
VSSLT3(VSS)
VSSLT4(VSS)
VSSLT5(VSS)
VSSLT6(VSS)
VSSLT7(VSS)
PM
SYSRESETb
POWERGOOD
LDTSTOPb
ALLOW_LDTSTOP
<6,13> -CPURST
R271 0/4/SHT/X
-NB_RST_C
<25> NB_PWROK
-LDT_STOP
<13> ALLOW_LDTSTOP
CLOCKs
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN(OSCIN)
REFCLK_N(PWM_GPIO3)
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)
LVDS_DIGON(PCE_TCALRP)
LVDS_BLON(PCE_RCALRP)
LVDS_ENA_BL(PWM_GPIO2)
R159 150/4/1
R158 150/4/1
REFCLKN
<12> NBHT_REFCLKP
<12> NBHT_REFCLKN
<12> OSC_14M_NB
REFCLKN
<12> NBSRC_CLKP
<12> NBSRC_CLKN
<12> SBLINK_CLKP
<12> SBLINK_CLKN
MIS.
I2C_DATA
I2C_CLK
DDC_DATA/AUX0P(NC)
DDC_CLK/AUX0N(NC)
AUX1P(NC)
AUX1N(NC)
STRP_DATA
RSVD
AUX_CAL(NC)
TMDS_HPD(NC)
HPD(NC)
TVCLKIN(PWM_GPIO5)
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
-SUS_STAT
<14>
TEST_EN
R279 1.8K/4/1
R265 8.2K/4/1 STRP_DATA
RS740_DFT_GPIO1
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
SBC35 10u/8/X5R/6.3V/K
BC143 1U/6/Y5V/10V/Z
SBC36 1U/6/Y5V/10V/Z
SBC15 0.1u/4/Y5V/16V/Z
BC141 1U/6/Y5V/10V/Z
U3D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_A0(NC)
MEM_A1(NC)
MEM_A2(NC)
MEM_A3(NC)
MEM_A4(NC)
MEM_A5(NC)
MEM_A6(NC)
MEM_A7(NC)
MEM_A8(NC)
MEM_A9(NC)
MEM_A10(NC)
MEM_A11(NC)
MEM_A12(NC)
MEM_A13(NC)
MEM_BA0(NC)
MEM_BA1(NC)
MEM_BA2(NC)
MEM_RASb(NC)
MEM_CASb(NC)
MEM_WEb(NC)
MEM_CSb(NC)
MEM_CKE(NC)
MEM_ODT(NC)
MEM_CKP(NC)
MEM_CKN(NC)
MEM_COMPP(NC)
MEM_COMPN(NC)
MEM_DQ0/DVO_VSYNC(NC)
MEM_DQ1/DVO_HSYNC(NC)
MEM_DQ2/DVO_DE(NC)
MEM_DQ3/DVO_D0(NC)
MEM_DQ4(NC)
MEM_DQ5/DVO_D1(NC)
MEM_DQ6/DVO_D2(NC)
MEM_DQ7/DVO_D4(NC)
MEM_DQ8/DVO_D3(NC)
MEM_DQ9/DVO_D5(NC)
MEM_DQ10/DVO_D6(NC)
MEM_DQ11/DVO_D7(NC)
MEM_DQ12(NC)
MEM_DQ13/DVO_D9(NC)
MEM_DQ14/DVO_D10(NC)
MEM_DQ15/DVO_D11(NC)
MEM_DQS0P/DVO_IDCKP(NC)
MEM_DQS0N/DVO_IDCKN(NC)
MEM_DQS1P(NC)
MEM_DQS1N(NC)
MEM_DM0(NC)
MEM_DM1/DVO_D8(NC)
IOPLLVDD18(NC)
IOPLLVDD(NC)
IOPLLVSS(NC)
MEM_VREF(NC)
RS780L/FCBGA528/A13/[10HB1-06760G-20R]
VCC18
NB_VCC
BC60 0.1u/4/Y5V/16V/Z
BC61 0.1u/4/Y5V/16V/Z
GIGABYTE
Title
RS780 SYSTEM I/F,STRAP
Size Custom
Document Number GA-78LMT-S2
Rev 1.12
Date: Thursday, October 04, 2012
Sheet 10 of 27

RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

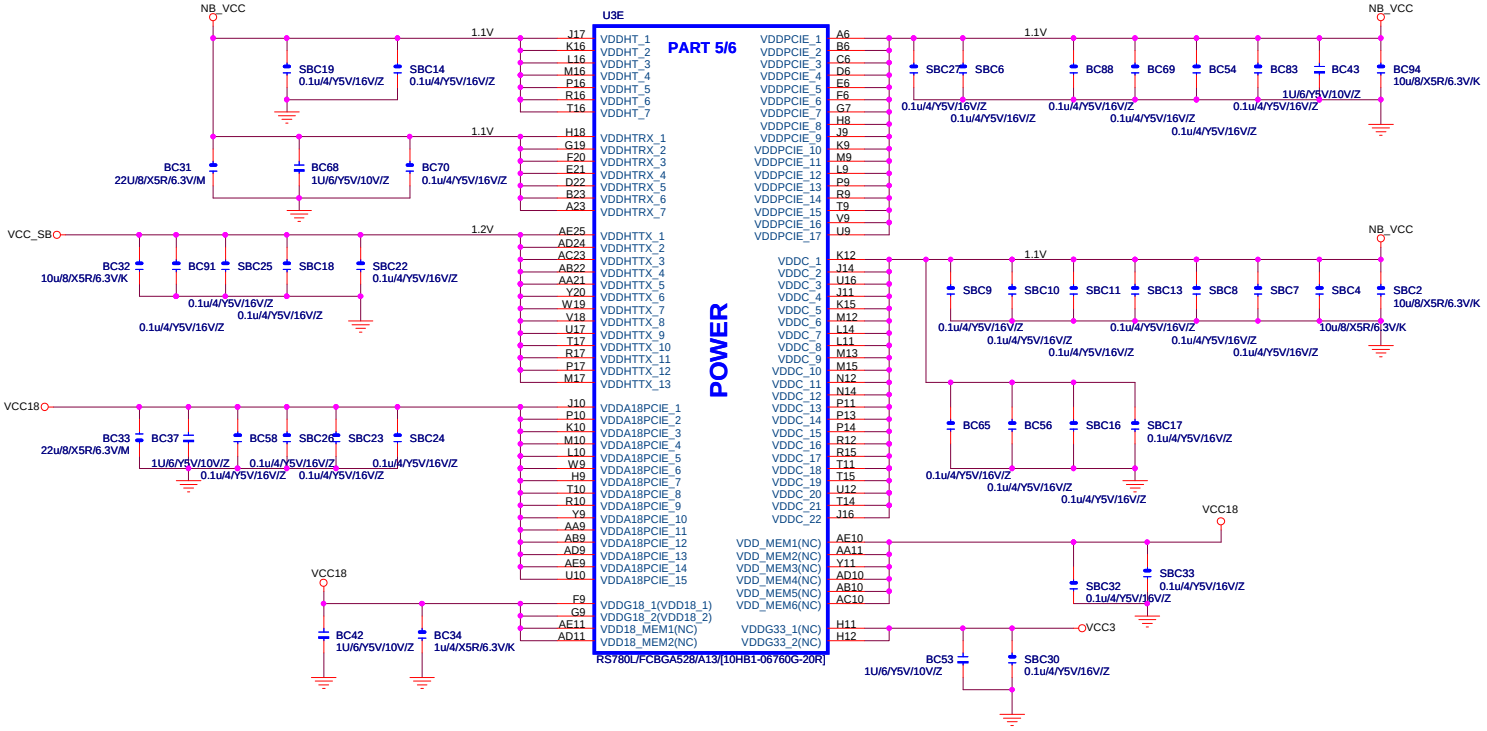
U3F — PART 6/6 — GROUND

RS780L/FCBGA528/A13/[10HB1-06760G-20R]

Please use 1mm pad size, place all ELT test pads on bottom side only

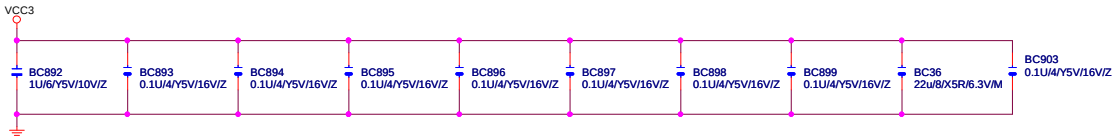
U3E — PART 5/6 — POWER

RS780L/FCBGA528/A13/[10HB1-06760G-20R]



GIGABYTE™

Title: RS780 POWER & GND		
Size: Custom	Document Number: GA-78LMT-S2	Rev: 1.12
Date: Thursday, October 04, 2012	Sheet 11 of 27	



1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

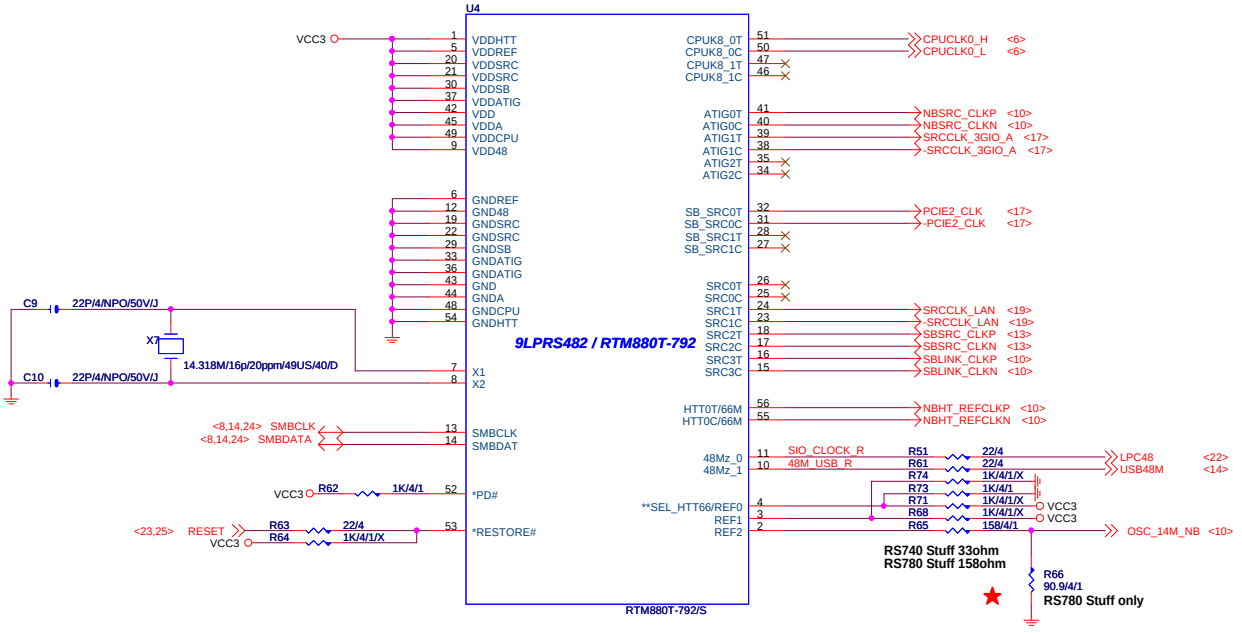
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

GIGABYTE™

Title: RTM880T-792

Size: Custom | Document Number: GA-78LMT-S2 | Rev: 1.12

Date: Friday, August 24, 2012 | Sheet 12 of 27

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-SA0301-01R_12SP2-SA0301-02R_12SP2-SA0301-03R]

U2A

SB700

Part 1 of 5

PCI EXPRESS INTERFACE

PCI CLKS

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC

CPU

RTC XTAL

SB710/FCBGA528/A14/[10HB1-06B710-11R]

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

X4 32.768K/12.5p/20ppm/TF38/35K/D

X4 SHW/D0.64*5.08*6.74

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting
EC AOD-ACC

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
	AOD Extreme	
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

BAT54C/SOT23/200mA

BAT BAT-SK/BK/P/S/D/SN

BATTERY CR2032

PH/1*2/BK/2.54/VA/D

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

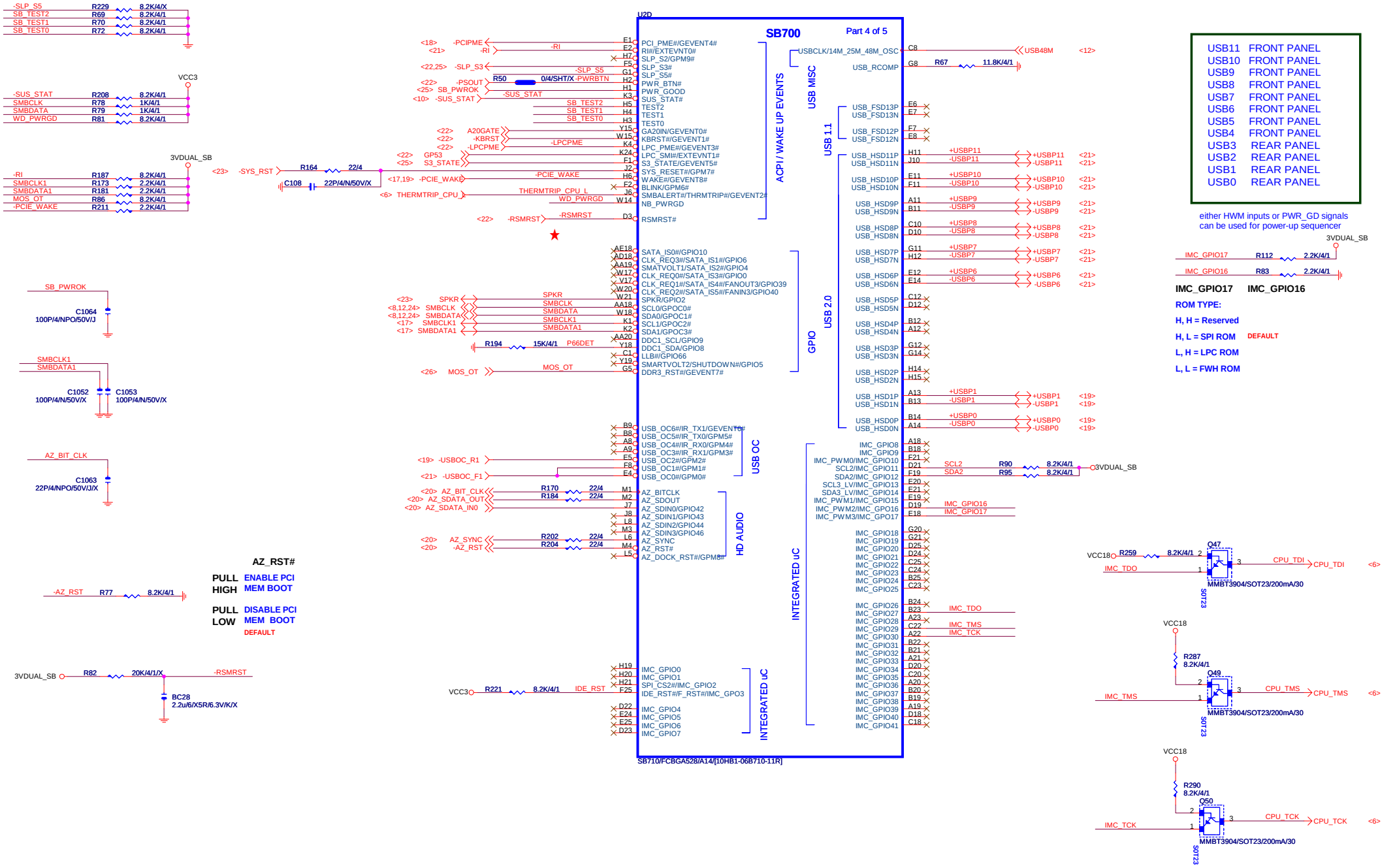
NOT ADD ICT FOR RTCVDD PIN

GIGABYTE

Title: ATI SB710 PCIE/PCI/CPU/LPC

Size: Custom | Document Number: GA-78LMT-S2 | Rev: 1.12

Date: Thursday, October 04, 2012 | Sheet 13 of 27


SB700
Part 4 of 5
U2D
SB710/FCBGA528/A14/[10HB1-06B710-11R]
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMATVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPIO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
-SLP_S5 R229 8.2K/4/X
SB_TEST2 R69 8.2K/4/1
SB_TEST1 R70 8.2K/4/1
SB_TEST0 R72 8.2K/4/1
VCC3
-SUS_STAT R208 8.2K/4/1
SMBCLK R78 1K/4/1
SMBDATA R79 1K/4/1
WD_PWRGD R81 8.2K/4/1
3VDUAL_SB
-RI R187 8.2K/4/1
SMBCLK1 R173 2.2K/4/1
SMBDATA1 R181 2.2K/4/1
MOS_OT R86 8.2K/4/1
-PCIE_WAKE R211 2.2K/4/1
-SYS_RST R164 22/4
C108 22P/4/N/50V/X
-PCIPME
-RI
-SLP_S3
-SLP_S5
R50 0/4/SHT/X -PWRBTN
-PSOUT
SB_PWROK
-SUS_STAT
SB_TEST2
SB_TEST1
SB_TEST0
A20GATE
-KBRST
-LPCPME
GP53
S3_STATE
-PCIE_WAKE
THERMTRIP_CPU_L
WD_PWRGD
-RSMRST
SPKR
SMBCLK
SMBDATA
SMBCLK1
SMBDATA1
R194 15K/4/1 P66DET
MOS_OT
-USBOC_R1
-USBOC_F1
R170 22/4
R184 22/4
AZ_BIT_CLK
AZ_SDATA_OUT
AZ_SDATA_IN0
R202 22/4
R204 22/4
AZ_SYNC
-AZ_RST
VCC3
R221 8.2K/4/1 IDE_RST
USB48M
R67 11.8K/4/1
+USBP11
-USBP11
+USBP10
-USBP10
+USBP9
-USBP9
+USBP8
-USBP8
+USBP7
-USBP7
+USBP6
-USBP6
+USBP1
-USBP1
+USBP0
-USBP0
SCL2
SDA2
R90 8.2K/4/1
R95 8.2K/4/1
3VDUAL_SB
IMC_TDO
IMC_TMS
IMC_TCK
SB_PWROK
C1064 100P/4/NPO/50V/J
SMBCLK1
SMBDATA1
C1052 100P/4/N/50V/X
C1053 100P/4/N/50V/X
AZ_BIT_CLK
C1063 22P/4/NPO/50V/J/X
-AZ_RST R77 8.2K/4/1
AZ_RST#
PULL HIGH ENABLE PCI MEM BOOT
PULL LOW DISABLE PCI MEM BOOT
DEFAULT
3VDUAL_SB R82 20K/4/1/X -RSMRST
BC28 2.2u/6/X5R/6.3V/K/X
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals can be used for power-up sequencer
3VDUAL_SB
IMC_GPIO17 R112 2.2K/4/1
IMC_GPIO16 R83 2.2K/4/1
IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
VCC18
R259 8.2K/4/1
Q47
IMC_TDO
CPU_TDI
MMBT3904/SOT23/200mA/30
SOT23
R287 8.2K/4/1
Q49
IMC_TMS
CPU_TMS
R290 8.2K/4/1
Q50
IMC_TCK
CPU_TCK
GIGABYTE
Title
ATI SB710 ACPI/USB/GPIO/AUDIO
Size Custom
Document Number GA-78LMT-S2
Rev 1.12
Date: Friday, August 24, 2012
Sheet 14 of 27

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B

SB700
Part 2 of 5

SERIAL ATA
SP_TX0P_C AD9 SATA_TX0P
SP_TX0M_C AE9 SATA_TX0N
SP_RX0M_C AB10 SATA_RX0N
SP_RX0P_C AC10 SATA_RX0P
SP_TX1P_C AE10 SATA_TX1P
SP_TX1M_C AD10 SATA_TX1N
SP_RX1M_C AD11 SATA_RX1N
SP_RX1P_C AE11 SATA_RX1P
SP_TX2P_C AB12 SATA_TX2P
SP_TX2M_C AC12 SATA_TX2N
SP_RX2M_C AE12 SATA_RX2N
SP_RX2P_C AD12 SATA_RX2P
SP_TX3P_C AD13 SATA_TX3P
SP_TX3M_C AE13 SATA_TX3N
SP_RX3M_C AB14 SATA_RX3N
SP_RX3P_C AC14 SATA_RX3P
SP_TX4P_C AE14 SATA_TX4P
SP_TX4M_C AD14 SATA_TX4N
SP_RX4M_C AD15 SATA_RX4N
SP_RX4P_C AE15 SATA_RX4P
SP_TX5P_C AB16 SATA_TX5P
SP_TX5M_C AC16 SATA_TX5N
SP_RX5M_C AE16 SATA_RX5N
SP_RX5P_C AD16 SATA_RX5P
SR6 1K/4/1 SATA_CAL V12 SATA_CAL
SATA_X1 Y12 SATA_X1
SATA_X2 AA12 SATA_X2
<23> -SATA_LED -SATA_LED W11 SATA_ACT#/GPIO67
VCC_SB AA11 PLLVDD_SATA
VCC3 W12 XTLVDD_SATA

SATA PWR

ATA 66/100/133
IDE_IORDY AA24
IDE_IRQ AA25
IDE_A0 Y22
IDE_A1 AB23
IDE_A2 Y23
IDE_DACK# AB24
IDE_DRQ AD25
IDE_IOR# AC25
IDE_IOW# AC24
IDE_CS1# Y25
IDE_CS3# Y24
IDE_D0/GPIO15 AD24
IDE_D1/GPIO16 AD23
IDE_D2/GPIO17 AE22
IDE_D3/GPIO18 AC22
IDE_D4/GPIO19 AD21
IDE_D5/GPIO20 AE20
IDE_D6/GPIO21 AB20
IDE_D7/GPIO22 AD19 PDD7 R189 8.2K/4/1
IDE_D8/GPIO23 AE19
IDE_D9/GPIO24 AC20
IDE_D10/GPIO25 AD20
IDE_D11/GPIO26 AE21
IDE_D12/GPIO27 AB22
IDE_D13/GPIO28 AD22
IDE_D14/GPIO29 AE23
IDE_D15/GPIO30 AC23

SPI ROM
SPI_DI/GPIO12 G6 SB_SPI_DI_R R101 22/4 SB_SPI_DI
SPI_DO/GPIO11 D2 SB_SPI_DO_R R102 22/4 SB_SPI_DO
SPI_CLK/GPIO47 D1 SB_SPI_CLK_R R92 22/4 SB_SPI_CLK
SPI_HOLD#/GPIO31 E4
SPI_CS1#/GPIO32 F3 SB_SPI_CS R103 22/4/X -SB_SPI_CS_ITE -SB_SPI_CS_ITE <22>
R96 22/4 SPI_CS
LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1

HW MONITOR
FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7
FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8
TEMP_COMM C6
TEMPIN0/GPIO61 B6
TEMPIN1/GPIO62 A6
TEMPIN2/GPIO63 A5
TEMPIN3/TALERT#/GPIO64 B5
VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7
AVDD F6 3VDUAL_SB
AVSS G7

BC119 0.1u/4/Y5V/16V/Z
BC117 1U/6/Y5V/10V/Z

SB710/FCBGA528/A14/[10HB1-06B710-11R]

R168 10M/4
X6
25M/20p/30ppm/49US/20/D
C115 10P/4/NPO/50V/J
C119 10P/4/NPO/50V/J

VCC3
BC112 1u/4/X5R/6.3V/K
SBC1 0.1u/4/Y5V/16V/Z
SBC3 0.1u/4/Y5V/16V/Z

Close to M_BIOS
<22> -ITE_SPI_CS R97 22/4/X SPI_CS
SB_SPI_DI
-BIOS_WP

M_BIOS
CS# VDD
SO HOLD#
WP# SCK
VSS SI
16M/SPI/SO8/200mil/S
BC203 0.1U/4/Y5V/16V/Z
-SPI_HOLD0
SB_SPI_CLK
SB_SPI_DO

<22> -ITE_SPI_CS1 -ITE_SPI_CS1
B_BIOS
16M/SPI/SO8/200mil/S/X

-SPI_HOLD0 R29 1K/4/1
SB_SPI_DO R34 1K/4/X
-BIOS_WP R38 1K/4/1
SB_SPI_DI R39 1K/4/X
SPI_CS R28 220/4
-ITE_SPI_CS1 R33 220/4/X

SATA2_0
SP_TX0P_C C1310 0.01u/4/X7R/25V/K
SP_TX0M_C C1309 0.01u/4/X7R/25V/K
SP_RX0M_C C1308 0.01u/4/X7R/25V/K
SP_RX0P_C C1302 0.01u/4/X7R/25V/K
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_1
C1307 0.01U/4/X7R/25V/K SP_RX1P_C
C1311 0.01u/4/X7R/25V/K SP_RX1M_C
C1300 0.01U/4/X7R/25V/K SP_TX1M_C
C1286 0.01U/4/X7R/25V/K SP_TX1P_C
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_2
SP_TX2P_C C1279 0.01u/4/X7R/25V/K
SP_TX2M_C C1278 0.01U/4/X7R/25V/K
SP_RX2M_C C1282 0.01U/4/X7R/25V/K
SP_RX2P_C C1283 0.01U/4/X7R/25V/K
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_3
C1284 0.01U/4/X7R/25V/K SP_RX3P_C
C1285 0.01U/4/X7R/25V/K SP_RX3M_C
C1281 0.01U/4/X7R/25V/K SP_TX3M_C
C1280 0.01U/4/X7R/25V/K SP_TX3P_C
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_4
SP_TX4P_C C1313 0.01u/4/X7R/25V/K
SP_TX4M_C C1314 0.01U/4/X7R/25V/K
SP_RX4M_C C1315 0.01U/4/X7R/25V/K
SP_RX4P_C C1303 0.01U/4/X7R/25V/K
SATA2/7/BU/H/OP/VA/D/1/B

SATA2_5
C1319 0.01U/4/X7R/25V/K SP_RX5P_C
C1312 0.01U/4/X7R/25V/K SP_RX5M_C
C1301 0.01U/4/X7R/25V/K SP_TX5M_C
C1296 0.01U/4/X7R/25V/K SP_TX5P_C
SATA2/7/BU/H/OP/VA/D/1/B

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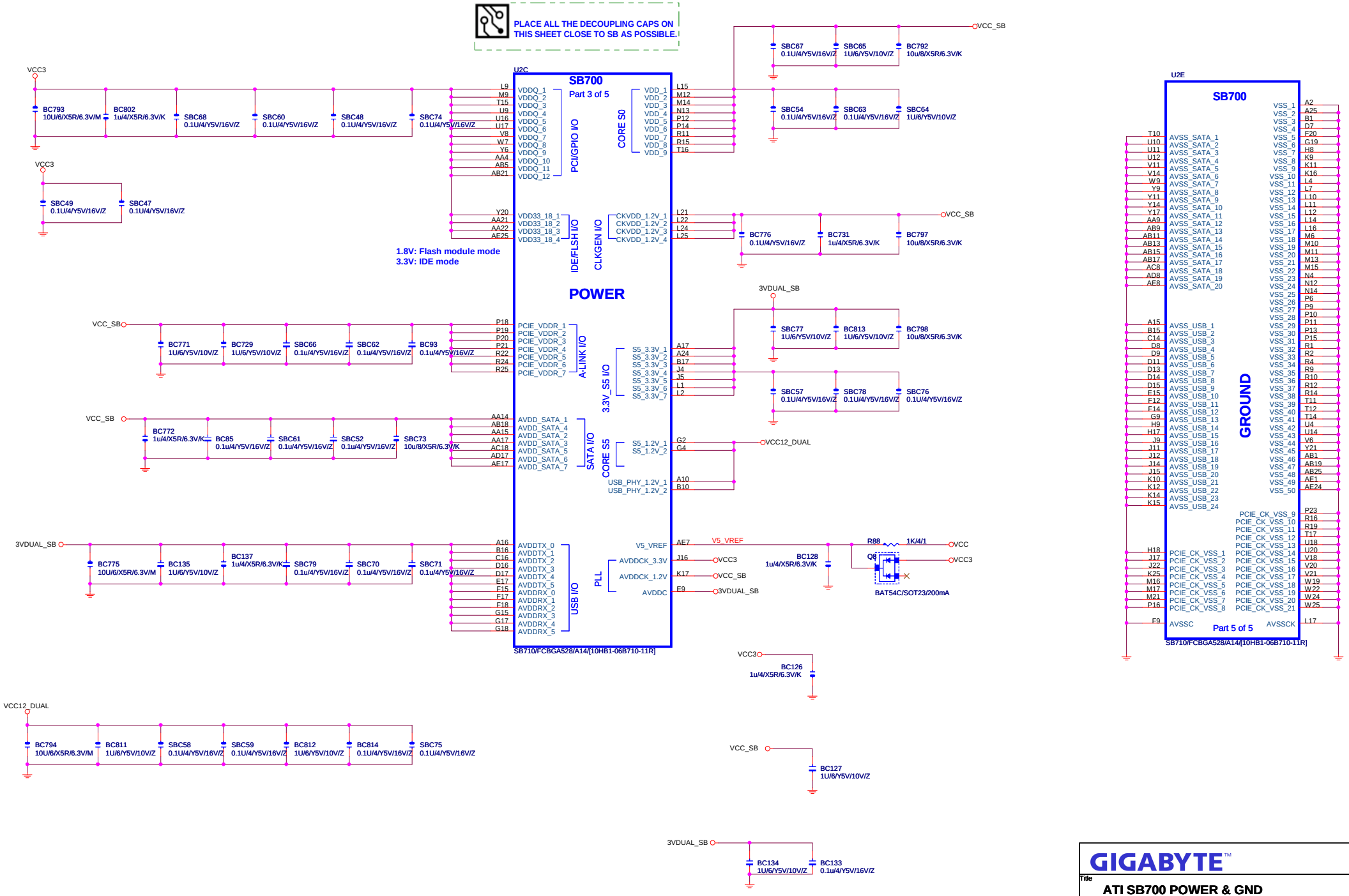
Title: ATI SB710 SATA/IDE/HWM/SPI
Size: Custom
Document Number: GA-78LMT-S2
Rev: 1.12
Date: Friday, August 24, 2012
Sheet 15 of 27


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
U2C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
1.8V: Flash module mode
3.3V: IDE mode
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
SB700/FCBGA528/A14/[10HB1-06B710-11R]
U2E
SB700
GROUND
Part 5 of 5
SB700/FCBGA528/A14/[10HB1-06B710-11R]
VCC3
VCC_SB
3VDUAL_SB
VCC12_DUAL
V5_VREF
BAT54C/SOT23/200mA
GIGABYTE
ATI SB700 POWER & GND
GA-78LMT-S2
1.12
Thursday, October 04, 2012
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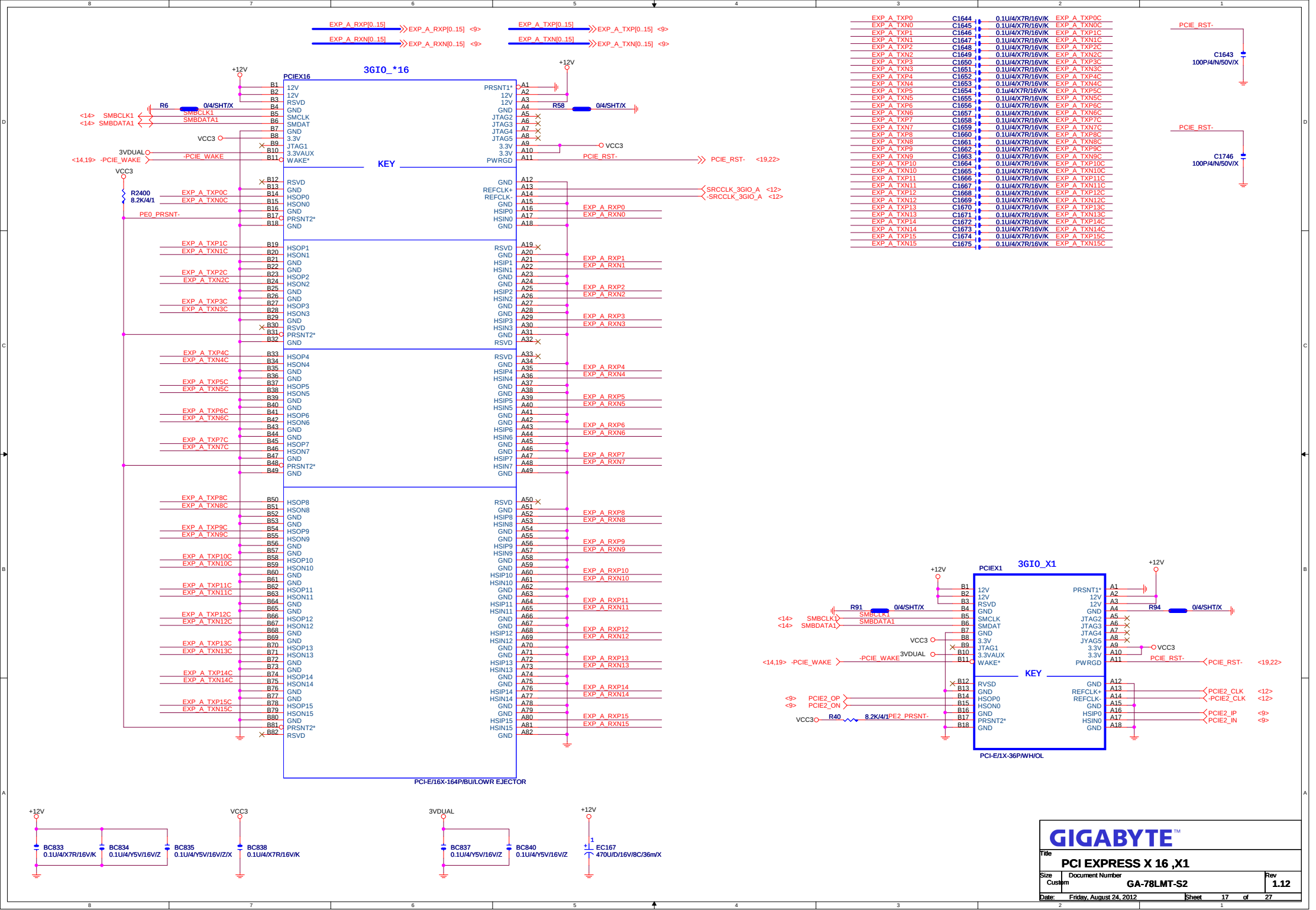
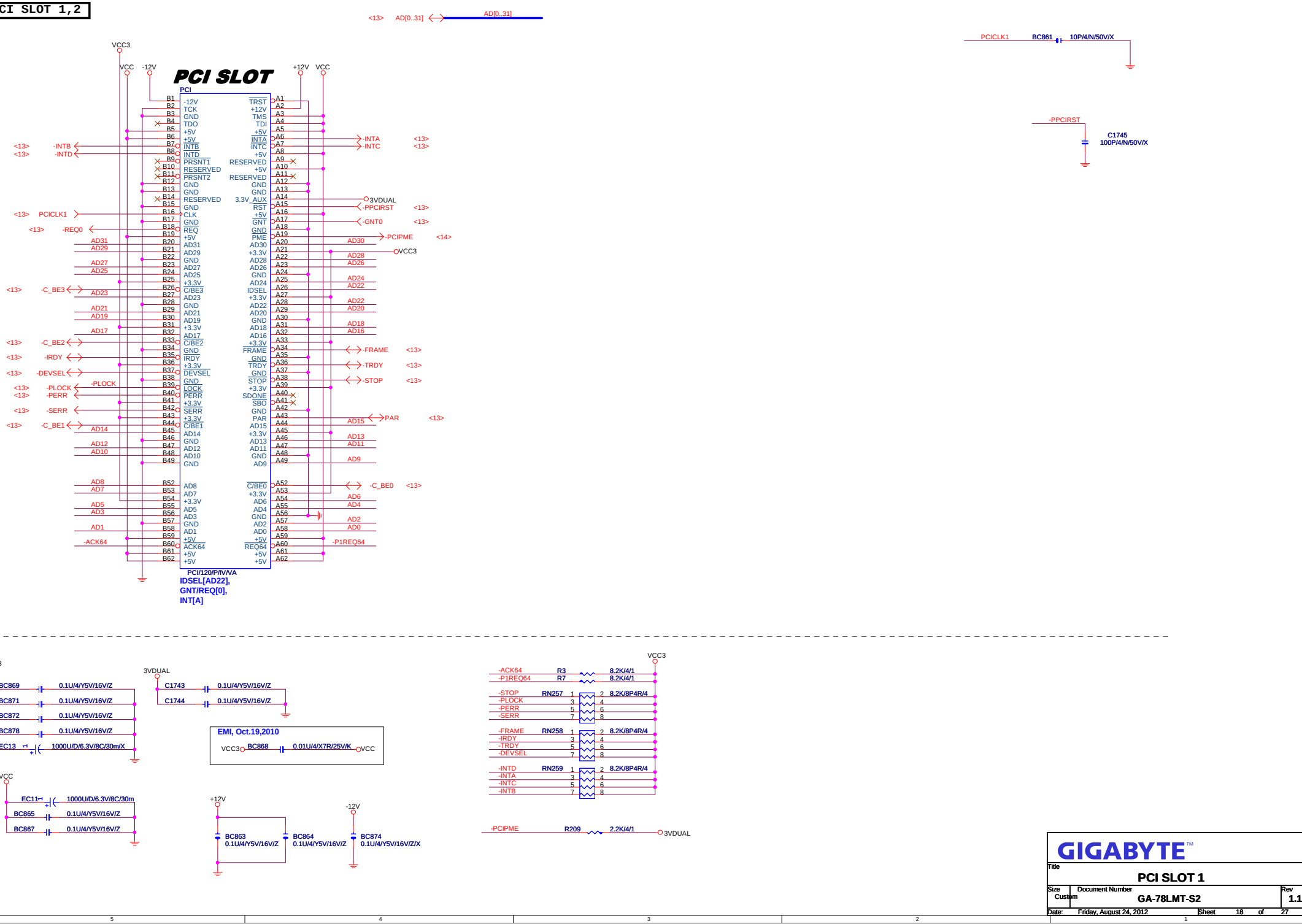

EXP_A_RXP[0..15]
EXP_A_RXN[0..15]
EXP_A_TXP[0..15]
EXP_A_TXN[0..15]
3GIO_*16
PCIEX16
KEY
PCI-E/16X-164P/BU/LOWR EJECTOR
3GIO_X1
PCIEX1
PCI-E/1X-36P/WH/OL
PCIE_RST-
SMBCLK1
SMBDATA1
-PCIE_WAKE
PE0_PRSNT-
PCIE2_OP
PCIE2_ON
PCIE2_IP
PCIE2_IN
PCIE2_CLK
-PCIE2_CLK
SRCCLK_3GIO_A
-SRCCLK_3GIO_A
PE2_PRSNT-
0.1U/4/X7R/16V/K
100P/4/N/50V/X
470U/D/16V/8C/36m/X

PCI SLOT 1,2



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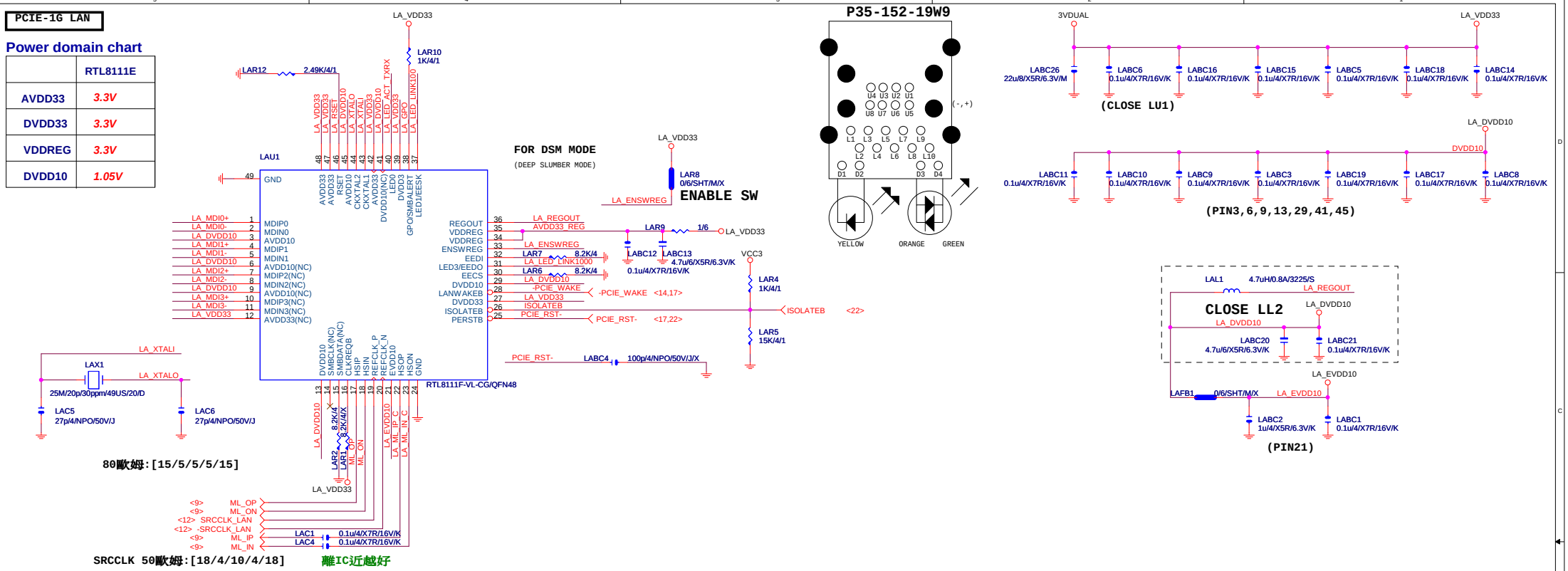
Title: PCI SLOT 1		
Size: Custom	Document Number: GA-78LMT-S2	Rev: 1.12
Date: Friday, August 24, 2012	Sheet 18 of 27	

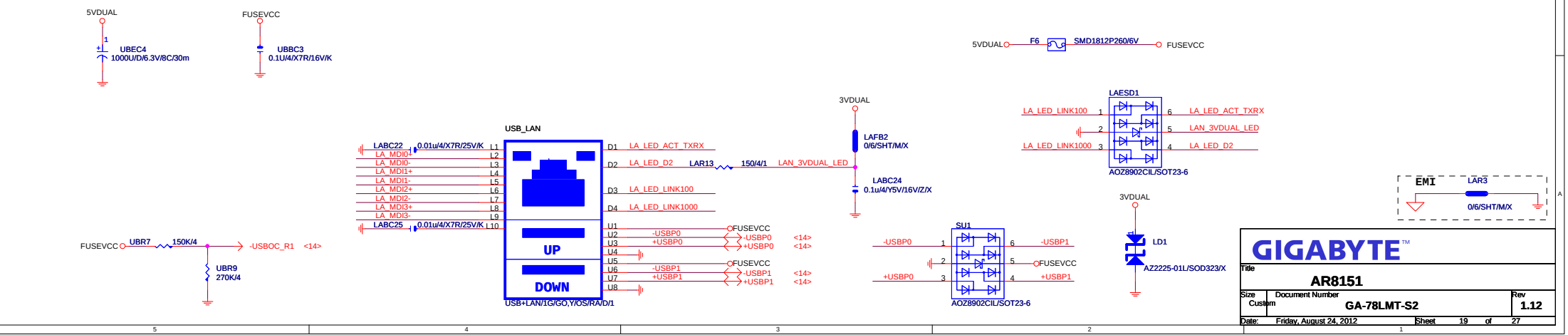
PCIE-1G LAN

Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



USB_LAN



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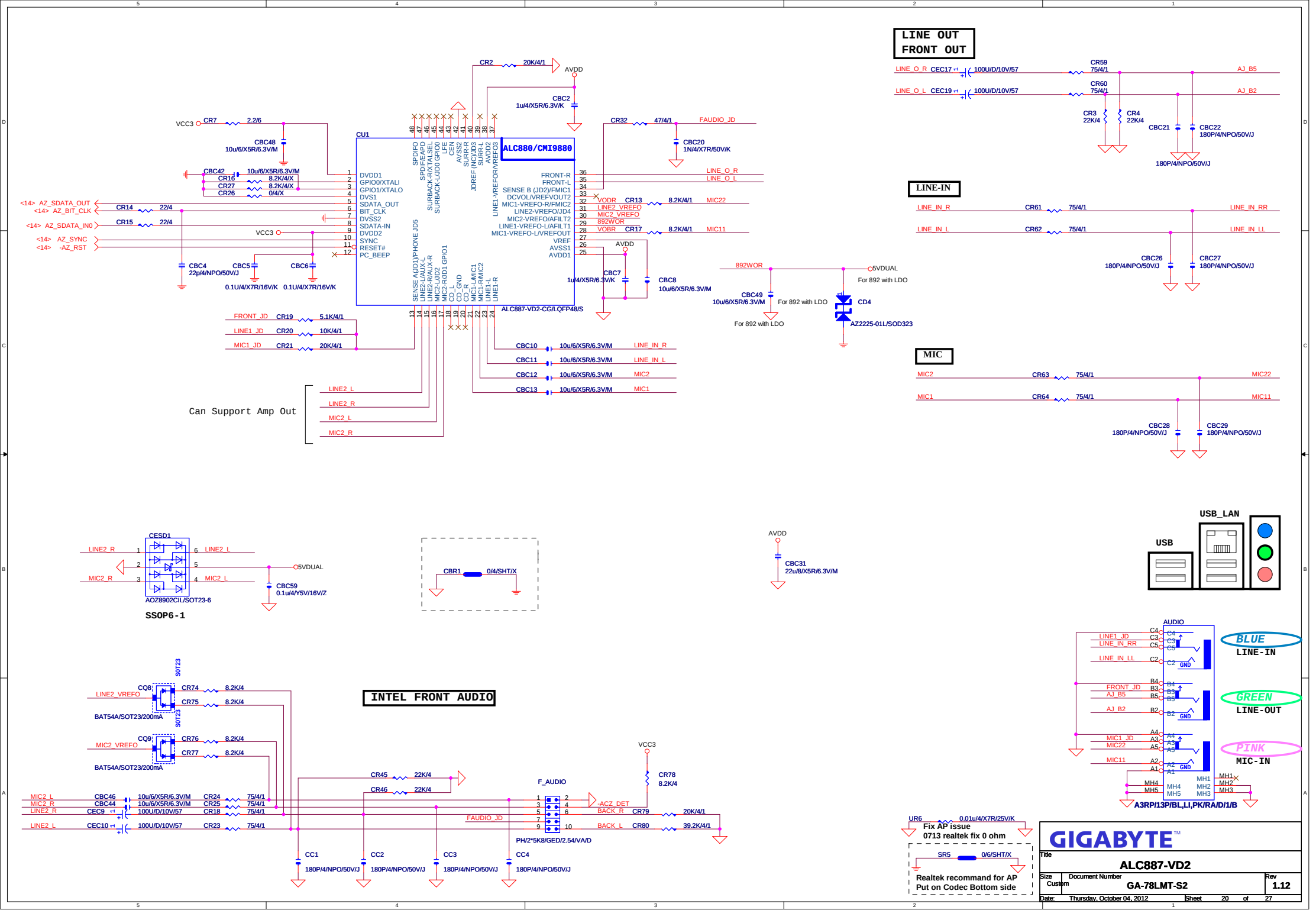
Title: AR8151

Size: Custom | Document Number: GA-78LMT-S2 | Rev: 1.12

Date: Friday, August 24, 2012 | Sheet 19 of 27


LINE OUT
FRONT OUT
LINE-IN
MIC
USB_LAN
USB
INTEL FRONT AUDIO
ALC880/CMI9880
ALC887-VD2-CG/LQFP48/S
SSOP6-1
Can Support Amp Out
Fix AP issue
0713 realtek fix 0 ohm
Realtek recommand for AP
Put on Codec Bottom side
BLUE
LINE-IN
GREEN
LINE-OUT
PINK
MIC-IN
A3RP/13P/BL,LI,PK/RA/D/1/B
GIGABYTE
ALC887-VD2
GA-78LMT-S2
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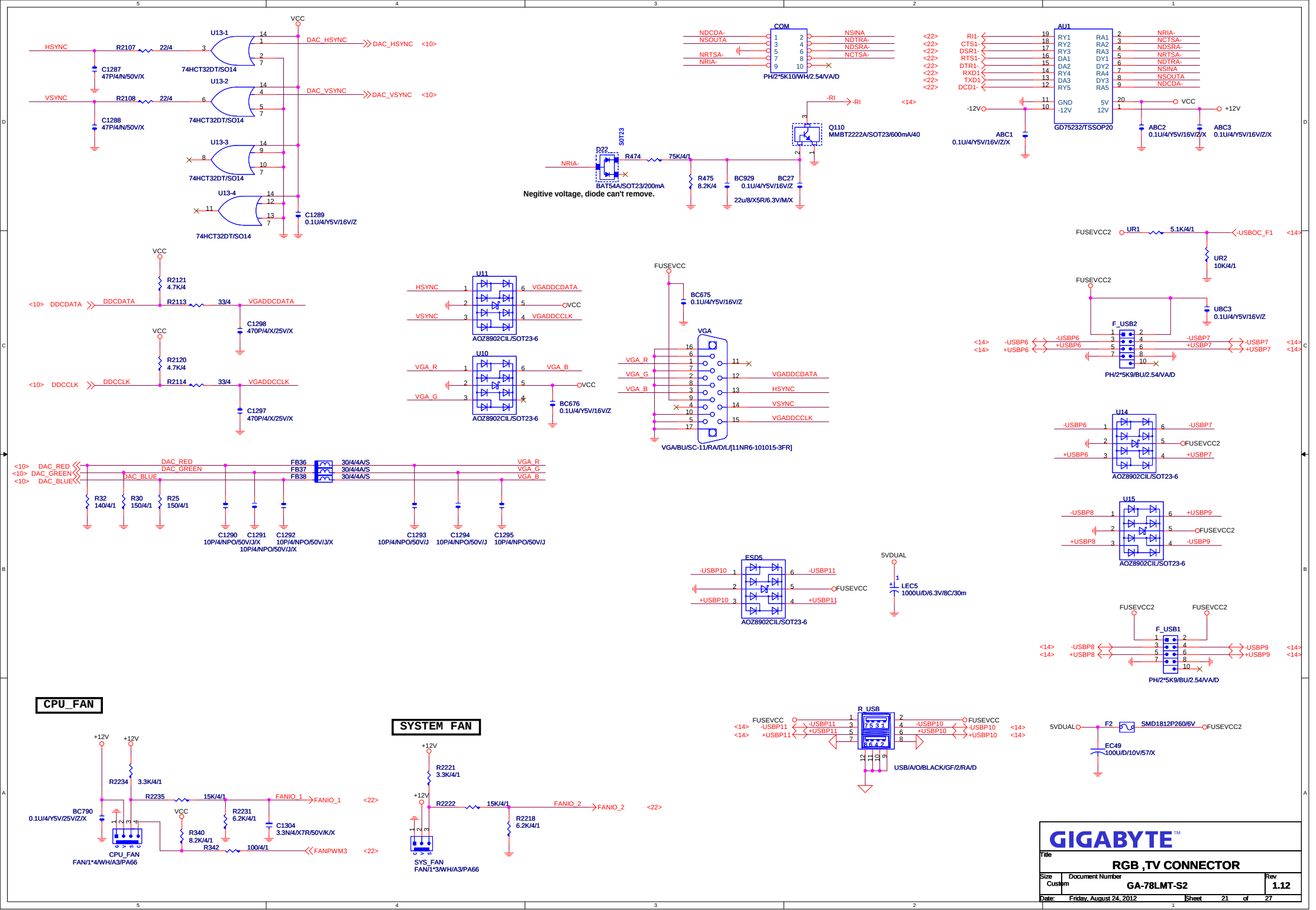
20
27



GIGABYTE™

Title: RGB ,TV CONNECTOR

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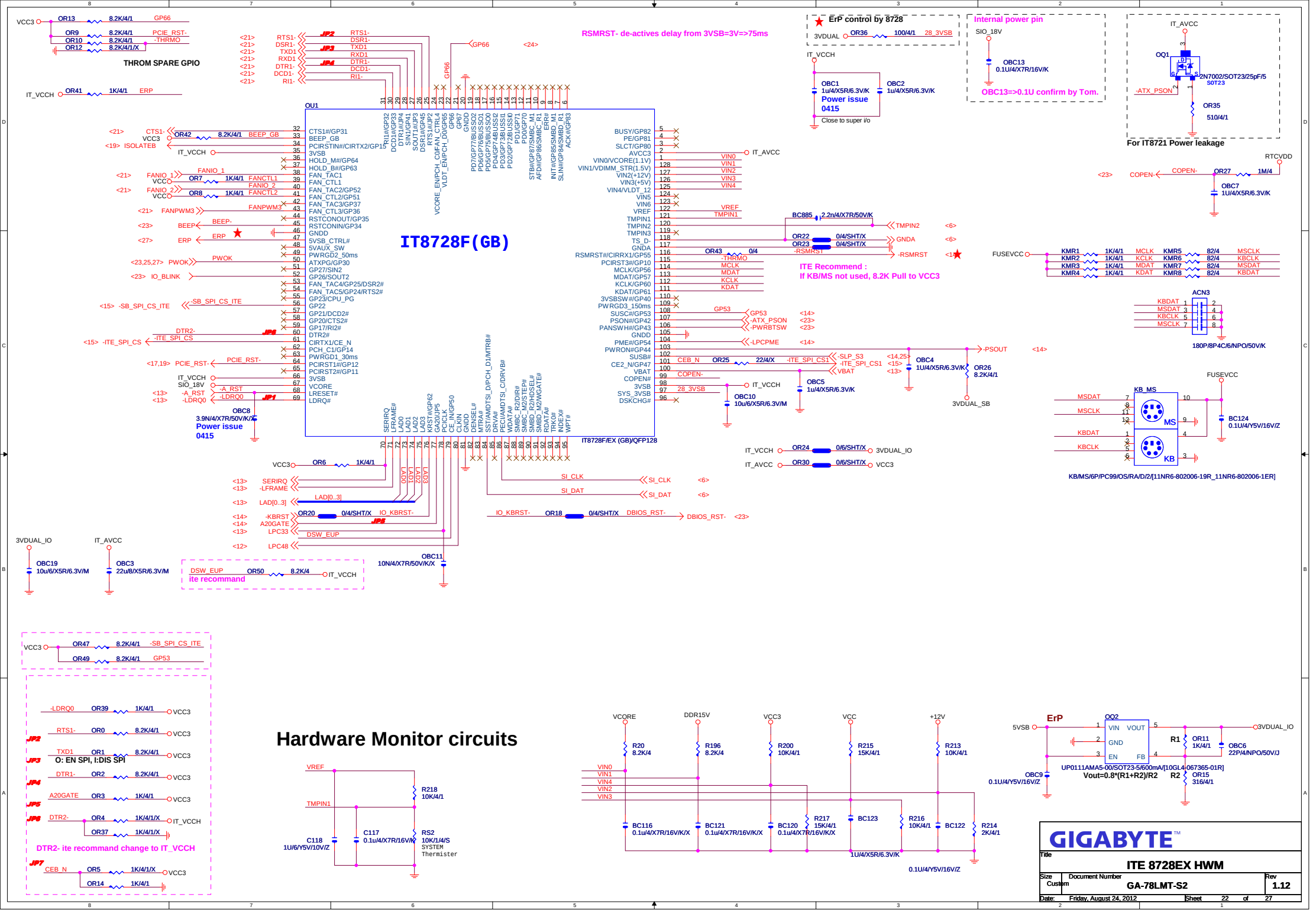
IT8728F(GB)
IT8728F/EX (GB)/QFP128
RSMRST- de-actives delay from 3VSB=3V=>75ms
ErP control by 8728
Internal power pin
THROM SPARE GPIO
ITE Recommend :
If KB/MS not used, 8.2K Pull to VCC3
Power issue
0415
OBC13=>0.1U confirm by Tom.
For IT8721 Power leakage
Close to super i/o
ite recommand
DTR2- ite recommand change to IT_VCCH
O: EN SPI, I:DIS SPI
Hardware Monitor circuits
KB/MS/6P/PC99/OS/RA/D/2/[11NR6-802006-19R_11NR6-802006-1ER]
180P/8P4C/6NPO/50V/K
Vout=0.8*(R1+R2)/R2
GIGABYTE
ITE 8728EX HWM
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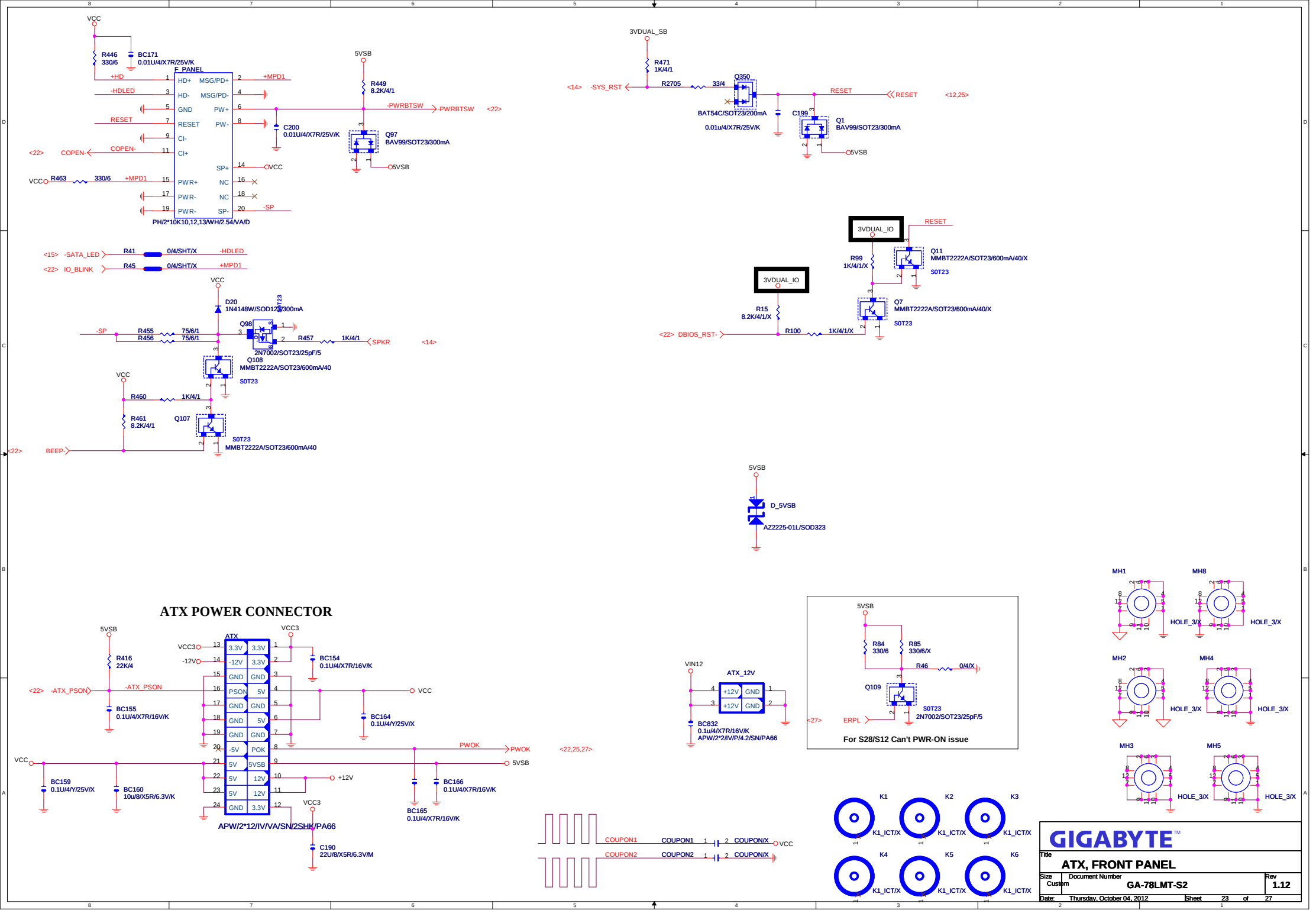
VCC
R446 330/6
BC171 0.01U/4/X7R/25V/K
F_PANEL
+HD
-HDLED
RESET
COPEN-
HD+
HD-
GND
RESET
CI-
CI+
PWR+
PWR-
PWR-
MSG/PD+
MSG/PD-
PW+
PW-
NC
NC
SP-
+MPD1
-SP
VCC
5VSB
R449 8.2K/4/1
-PWRBTSW
C200 0.01U/4/X7R/25V/K
Q97 BAV99/SOT23/300mA
R463 330/6
PH/2*10K10,12,13/WH/2.54/VA/D
3VDUAL_SB
R471 1K/4/1
R2705 33/4
Q350
BAT54C/SOT23/200mA
C199 0.01u/4/X7R/25V/K
Q1 BAV99/SOT23/300mA
RESET
<14> -SYS_RST
<12,25>
<15> -SATA_LED
<22> IO_BLINK
R41 0/4/SHT/X
R45 0/4/SHT/X
-HDLED
+MPD1
D20 1N4148W/SOD123/300mA
Q98 2N7002/SOT23/25pF/5
R455 75/6/1
R456 75/6/1
R457 1K/4/1
SPKR
Q108 MMBT2222A/SOT23/600mA/40
S0T23
R460 1K/4/1
R461 8.2K/4/1
Q107 MMBT2222A/SOT23/600mA/40
BEEP-
3VDUAL_IO
R99 1K/4/1/X
Q11 MMBT2222A/SOT23/600mA/40/X
R15 8.2K/4/1/X
R100 1K/4/1/X
Q7 MMBT2222A/SOT23/600mA/40/X
<22> DBIOS_RST-
D_5VSB
AZ2225-01L/SOD323
ATX POWER CONNECTOR
ATX
VCC3
-12V
PSON
POK
5VSB
R416 22K/4
-ATX_PSON
BC155 0.1U/4/X7R/16V/K
BC154 0.1U/4/X7R/16V/K
BC164 0.1U/4/Y25V/X
PWOK
BC159 0.1U/4/Y/25V/X
BC160 10u/8/X5R/6.3V/K
+12V
BC166 0.1U/4/X7R/16V/K
BC165 0.1U/4/X7R/16V/K
APW/2*12/IV/VA/SN/2SHK/PA66
C190 22U/8/X5R/6.3V/M
<22,25,27>
VIN12
ATX_12V
BC832 0.1u/4/X7R/16V/K APW/2*2/IV/P/4.2/SN/PA66
R84 330/6
R85 330/6/X
R46 0/4/X
Q109 2N7002/SOT23/25pF/5
ERPL
<27>
For S28/S12 Can't PWR-ON issue
COUPON1
COUPON2
COUPON/X
MH1
MH2
MH3
MH4
MH5
MH8
HOLE_3/X
K1
K2
K3
K4
K5
K6
K1_ICT/X
GIGABYTE
ATX, FRONT PANEL
Custom
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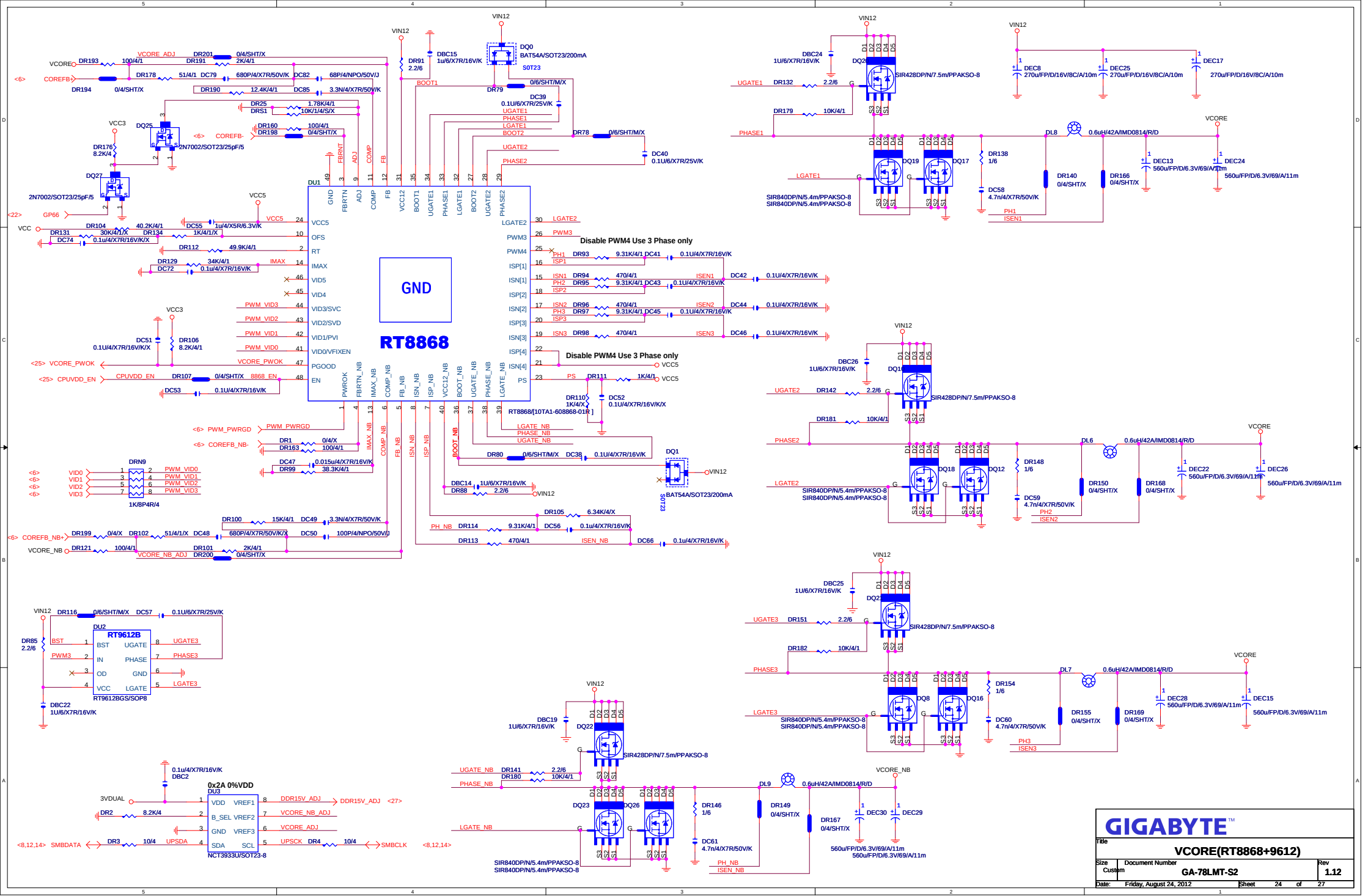
RT8868
GND
Disable PWM4 Use 3 Phase only
Disable PWM4 Use 3 Phase only
RT9612B
0x2A 0%VDD
SIR428DP/N/7.5m/PPAKSO-8
SIR840DP/N/5.4m/PPAKSO-8
BAT54A/SOT23/200mA
2N7002/SOT23/25pF/5
1K/8P4R/4
NCT3933U/SOT23-8
RT9612BGS/SOP8
RT8868/[10TA1-608868-01R]
GIGABYTE
VCORE(RT8868+9612)
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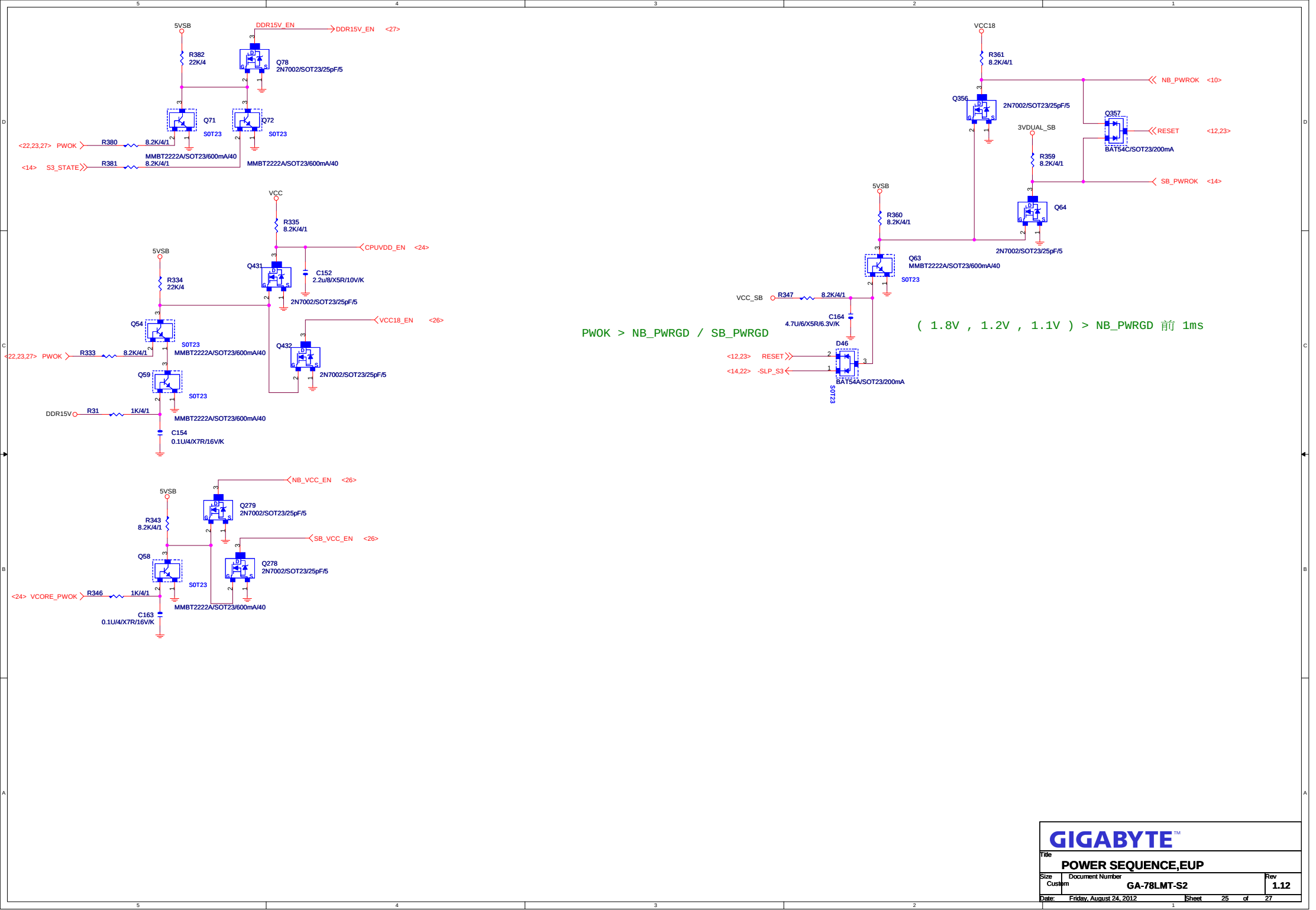

GIGABYTE™

Title: POWER SEQUENCE,EUP		
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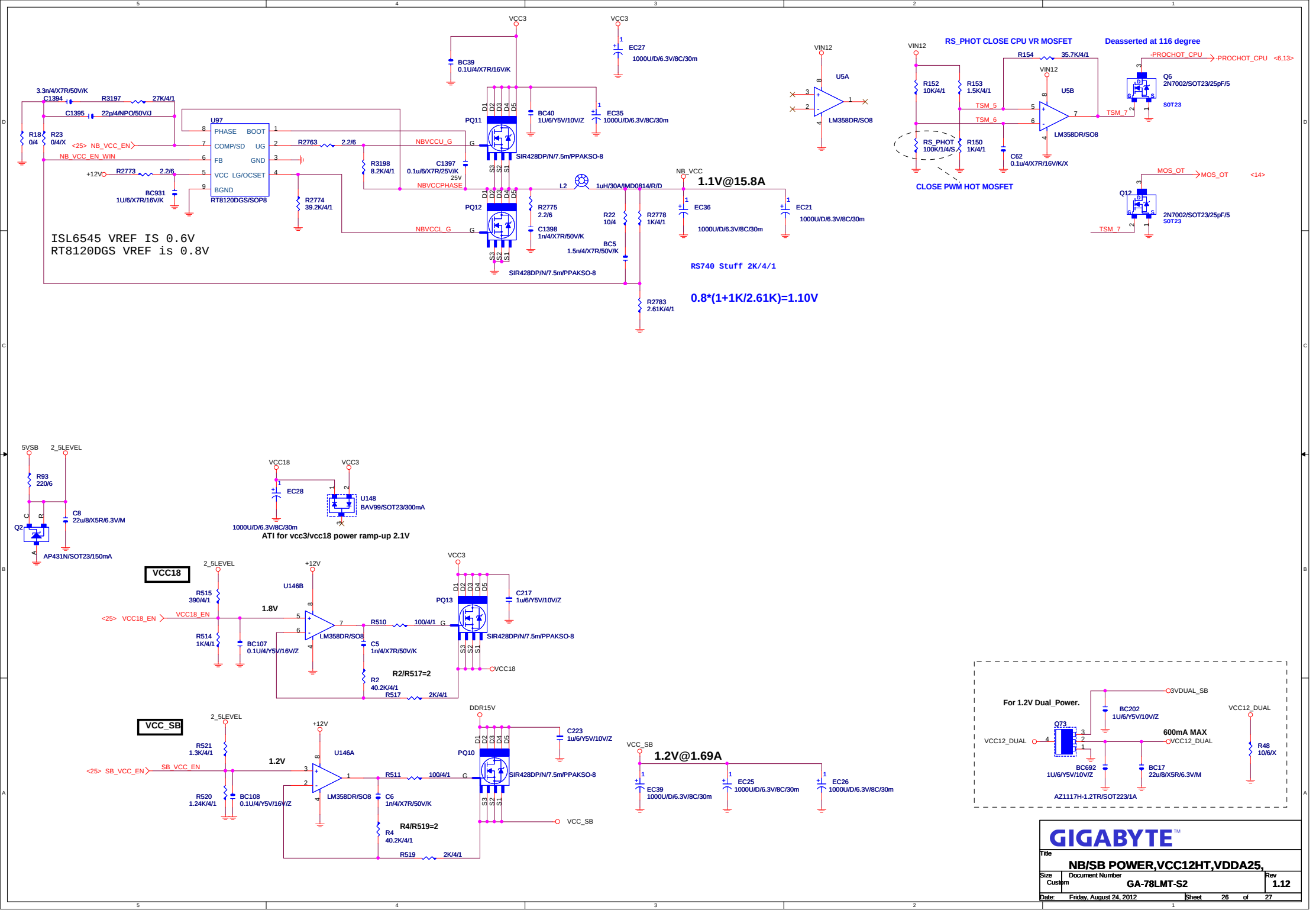

Title	NB/SB POWER,VCC12HT,VDDA25,
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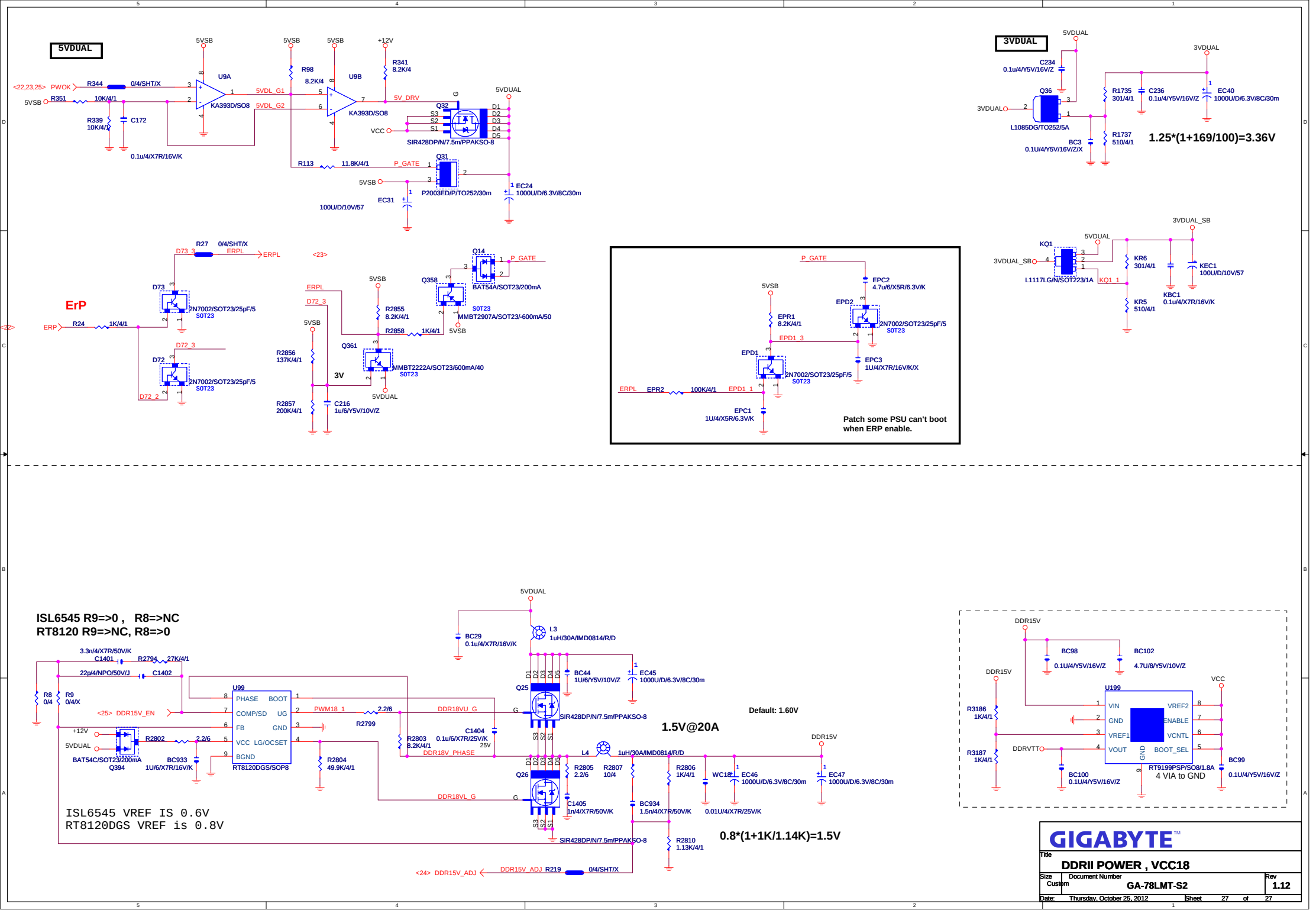
5VDUAL
U9A
U9B
KA393D/SO8
R98 8.2K/4
R341 8.2K/4
R344 0/4/SHT/X
R351 10K/4/1
R339 10K/4/1
C172
0.1u/4/X7R/16V/K
5VDL_G1
5VDL_G2
5V_DRV
Q32
SIR428DP/N/7.5m/PPAKSO-8
R113 11.8K/4/1
P_GATE
Q31
P2003ED/P/TO252/30m
EC31 100U/D/10V/57
EC24 1000U/D/6.3V/8C/30m
3VDUAL
C234 0.1u/4/Y5V/16V/Z
Q36
L1085DG/TO252/5A
R1735 301/4/1
C236 0.1u/4/Y5V/16V/Z
EC40 1000U/D/6.3V/8C/30m
R1737 510/4/1
BC3 0.1U/4/Y5V/16V/Z/X
1.25*(1+169/100)=3.36V
ErP
R27 0/4/SHT/X
R24 1K/4/1
D73
D72
2N7002/SOT23/25pF/5
S0T23
Q14
BAT54A/SOT23/200mA
Q358
MMBT2907A/SOT23/-600mA/50
R2855 8.2K/4/1
R2858 1K/4/1
Q361
MMBT2222A/SOT23/600mA/40
R2856 137K/4/1
R2857 200K/4/1
C216 1u/6/Y5V/10V/Z
3V
EPC2 4.7u/6/X5R/6.3V/K
EPR1 8.2K/4/1
EPD2
EPD1_3
EPC3 1U/4/X7R/16V/K/X
EPR2 100K/4/1
EPC1 1U/4/X5R/6.3V/K
Patch some PSU can't boot when ERP enable.
3VDUAL_SB
KQ1
L1117LG/N/SOT223/1A
KR6 301/4/1
KR5 510/4/1
KEC1 100U/D/10V/57
KBC1 0.1u/4/X7R/16V/K
ISL6545 R9=>0 , R8=>NC
RT8120 R9=>NC, R8=>0
U99
PHASE BOOT
COMP/SD UG
FB GND
VCC LG/OCSET
BGND
RT8120DGS/SOP8
BC29 0.1u/4/X7R/16V/K
L3 1uH/30A/IMD0814/R/D
BC44 1U/6/Y5V/10V/Z
EC45 1000U/D/6.3V/8C/30m
Q25
Q26
L4
R2805 2.2/6
R2807 10/4
R2806 1K/4/1
R2803 8.2K/4/1
C1404 0.1u/6/X7R/25V/K
C1405 1n/4/X7R/50V/K
BC934 1.5n/4/X7R/50V/K
WC18
EC46 1000U/D/6.3V/8C/30m
0.01U/4/X7R/25V/K
EC47 1000U/D/6.3V/8C/30m
R2810 1.13K/4/1
0.8*(1+1K/1.14K)=1.5V
Default: 1.60V
1.5V@20A
DDR18VU_G
DDR18V_PHASE
DDR18VL_G
PWM18_1
R2799 2.2/6
R2804 49.9K/4/1
C1401 3.3n/4/X7R/50V/K
R2794 27K/4/1
C1402 22p/4/NPO/50V/J
R8 0/4
R9 0/4/X
BAT54C/SOT23/200mA
Q394
R2802 2.2/6
BC933 1U/6/X7R/16V/K
ISL6545 VREF IS 0.6V
RT8120DGS VREF is 0.8V
DDR15V_ADJ R219 0/4/SHT/X
DDR15V
BC98 0.1U/4/Y5V/16V/Z
BC102 4.7U/8/Y5V/10V/Z
U199
VIN VREF2
GND ENABLE
VREF1 VCNTL
VOUT BOOT_SEL
R3186 1K/4/1
R3187 1K/4/1
BC100 0.1U/4/Y5V/16V/Z
BC99 0.1U/4/Y5V/16V/Z
RT9199PSP/SO8/1.8A
4 VIA to GND
GIGABYTE
DDRII POWER , VCC18
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