

Model Name: GA-Z170X-UD3

Rev 1.0

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B_DDR4
06	CPU_LGA1150-C
07	CPU_LGA1150-D
08	DDR4 CHANNEL A 1,2
09	DDR4 CHANNEL B 1,2
10	PCH_RGB,CLK BUFFER
11	PCH DMI,USB,PCIE
12	PCH MISC
13	PCH SATA,PCIE,SATA EXPRESS
14	PCH_PWR,GND
15	DUAL BIOS
16	ITE 8628 LPC IO
17	HMW
18	FAN CTRL--SIO
19	PCI EXPRESS X16 SLOT
20	PCI EXPRESS X4 SLOT(PCH)
21	PCI EXPRESS X1 SLOTS/SWITCH
22	M.2 X4
23	M.2 X4 (2nd)
24	SATA EXPRESSD
25	SATA EXPRESSC
26	ISL95856 PWM
27	ISL95856 MOS_VCORE-Ferrite
28	ISL95856 MOS_VCCGT-Ferrite
29	VCCSA_VCCIO_VCCPLL
30	RT8120_DDR_CHOKE

SHEET

TITLE

31	RT8120_VPP_CHOKE
32	RT8120_PCH
33	DISCRETE POWER
34	NCT3933
35	ATX POWER , A_-PROCHOT
36	KB_MS_USB
37	DVI CONN
38	PTN3356 - DP to VGA - IC
39	PTN3356 - DP to VGA - Conn
40	HDMI CONN_170
41	R_USB30
42	INTEL I219
43	USB30_LAN CONNECTOR-I219
44	Realtek ALC1150
45	REAR AUDIO JACK
46	F_USB30
47	F_USB BOX Header
48	COM,LPT,TPM ,THB,TURBO
49	F_PANEL
50	TABLE LIST
51	PCI EXPRESS X8 SLOT
52	PCI EXPRESS X16 SWITCH
53	IDT6V41510_CLK BUFFER
54	Audio Power
55	HD3SS3212&TUSB321_A
56	M.2 SWITCH
57	EMI-ESD
58	ALPINE RIDGE CIO & DP
59	ALPINE RIDGE POWER
60	NTC MAP

Gigabyte Technology


File			Cover Sheet
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Custom			
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Component value change history

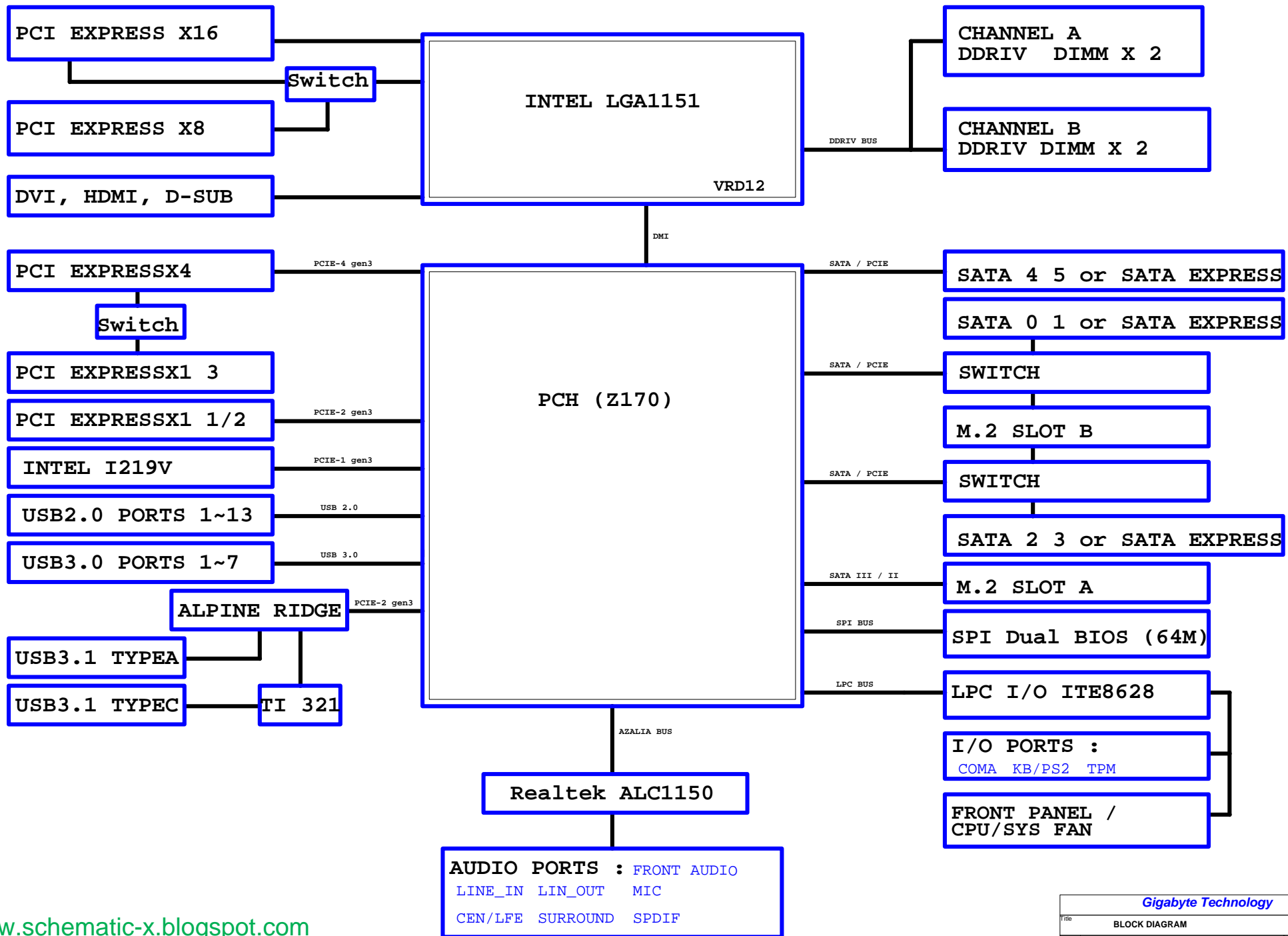
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Circuit or PCB layout change

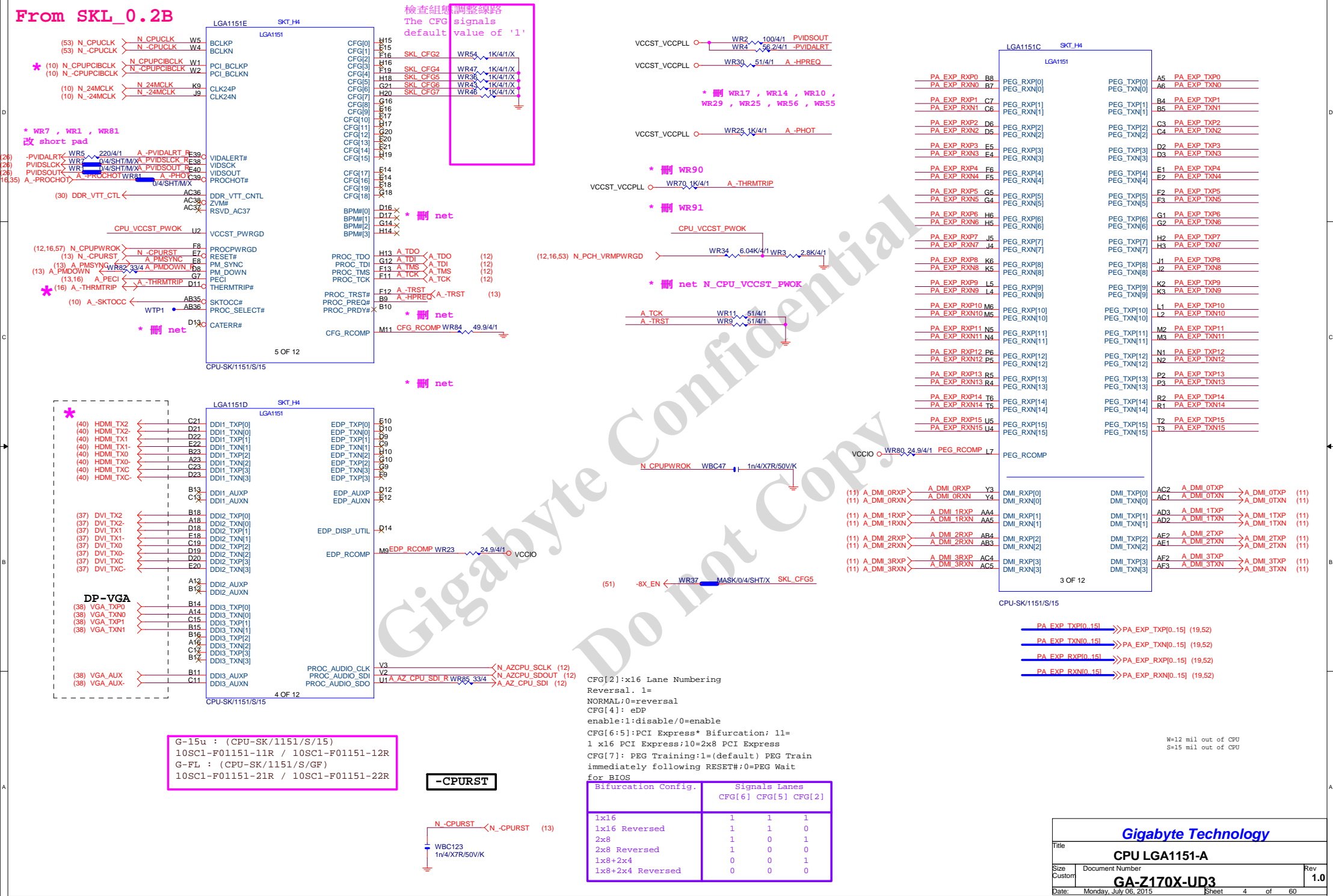
DATE	Change Item	Reason
2015/01/21	1. PCB first release 2. 線路由GA-Z1704X-SLI-02-0119B.DSN來修改 3. VCORE, VCCGT from Z1704X-UD5 TH 4. add 2nd M.2 5. add PCIE_X1_3 6. add 80port remove LPT 7. 改架高USB3 8. del turbo key 9. add 後窗裝甲 10. del PCI	REV 0.1
2015/03/24	1. update DP to VGA module (1.03 to 1.05) 2. update discrete power (0.41 to 0.51) 3. update IO module (1.04 to 1.06) 4. remove original HDMI2.0 and TYPE C 5. remove IO shield, GL850 6. add TBT circuit(USB3.1, HDMI 1.4)	REV 0.2
2015/04/02	1. rename Z170X-UD3 0.1	REV 0.1
2015/05/06	1. update TBT module (add TCAR20, THR44 change to 0402, remove THD3) 2. update DVI module(remove VD1) 3. update DP to VGA module(remove DVD1, add DVR21) 4. change PCIE_X16, X8, X4 footprint 5. update DDR VPP module(add MAC49.MAC50.MAC51.MAC52) 6. update PCIE_X4 module(SWAP PPU1 signals, slot 多一pin B48) 7. Q21 change to short pad 8. update FAN module(FNR6 change footprint to FUSE-0603-SHORT10) 9. update PCH power module(ADD NPD1.NPD2.NPR22) 10. update DDR module(Modify MR22, MR23, MR25 footprint) 11. update LAN module(add LAQ1, LAQR1)	REV 0.2
2015/06/11	1. add DVD1, VD1, THD3, NR3 2. 刪 WR100、WR101、NR302、NR303、WR102、WR103、NR300、NR301 3. U6 change location to DB_PORT 4. RN12, RN13, R199 change location to DB_PRN1, DB_PRN2(改0402 排組), DB_PR1 5. TCA(B)Q3更改為TCA(B)Q1/2 6. PCH.BA4 改接NR7 7. 修改NX1 Layout 8. THC63, THC62, THC65, THC64 9. add HDMI level shifter 10. change Etron to TI	REV 0.3
2015/06/25	1. 刪除VDDSPD 2. NPR22改0805 3. add NPC10 請放置CHOKE一出來的地方 4. WR94改0402 5. add DFC3 close to CPU 6. Add MA_DR9 close to MA_DQ2	REV 9.0

			
Title			
BOM & PCB MODIFY HISTORY			
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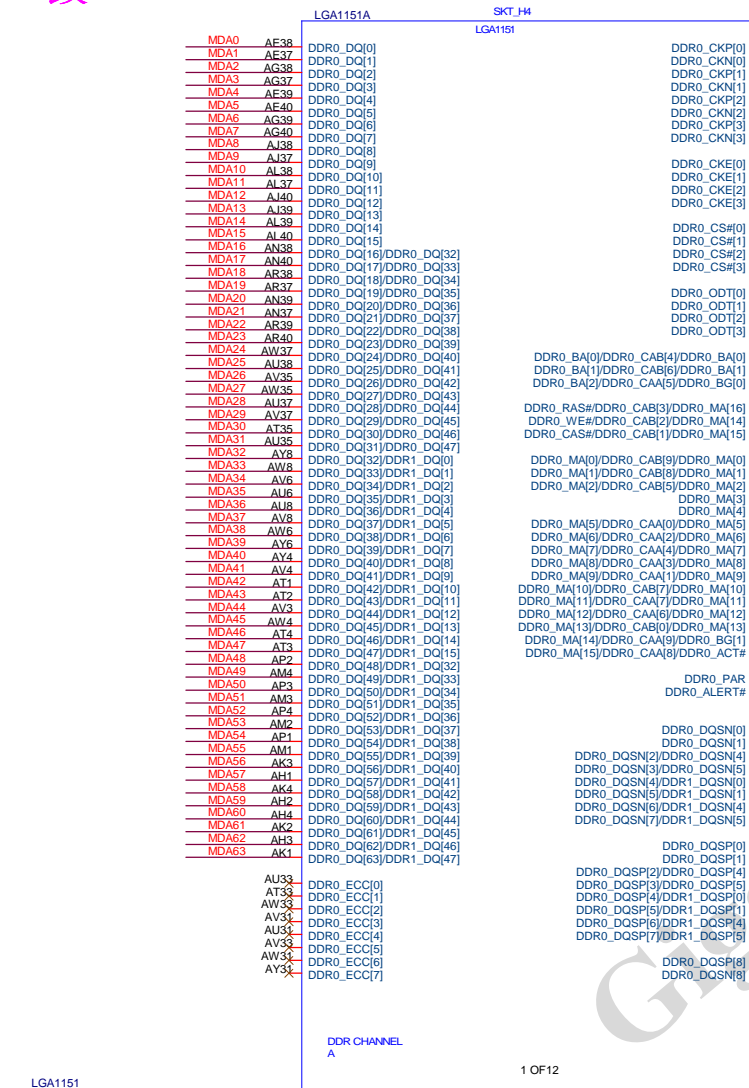
BLOCK DIAGRAM



From SKL_0.2B

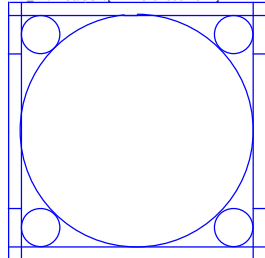


* 改DDR4 net

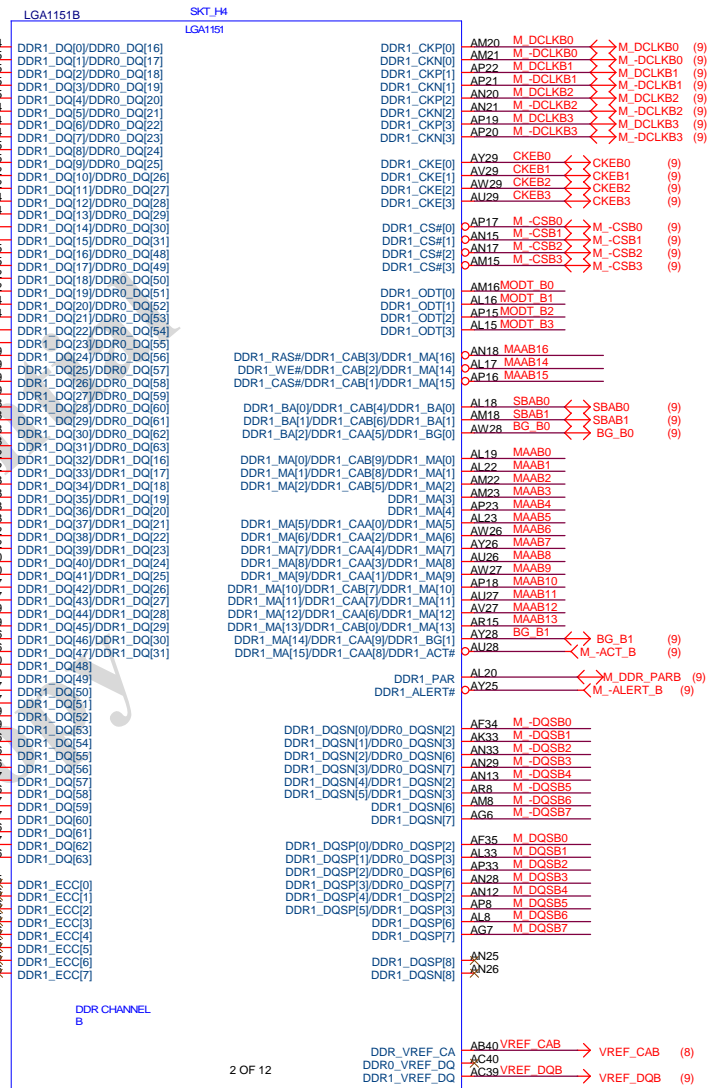


LGA1151

ILM_BP/1156/CSP/12KRC-0F0001-61R1



Need check the new CPU MB



CPU-SK1151/S/15

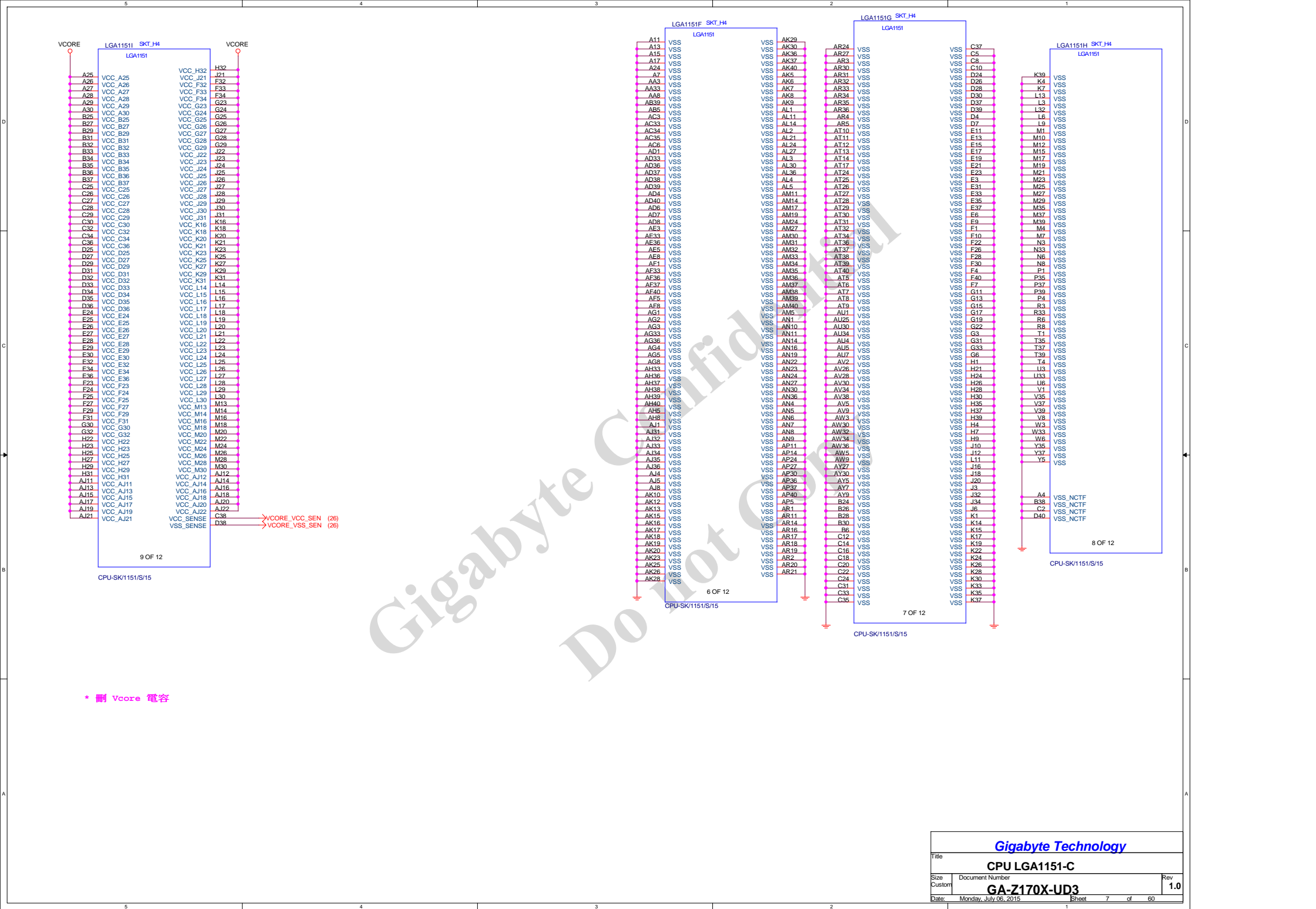
- (8) MODT_A[0..3] <=> MODT A0..31
- (9) MODT_B[0..3] <=> MODT B0..31
- (8) MDA[0..63] <=> MDA0..631
- (9) MDB[0..63] <=> MDB0..631
- (8) M_DQSA[0..7] <=> M_DQSA0..71
- (8) M_DQSA[0..7] <=> M_DQSA0..71
- (8) MAA[0..16] <=> MAA0..161
- (9) MAA[0..16] <=> MAA0..161
- (9) M_DQSB[0..7] <=> M_DQSB0..71
- (9) M_DQSB[0..7] <=> M_DQSB0..71

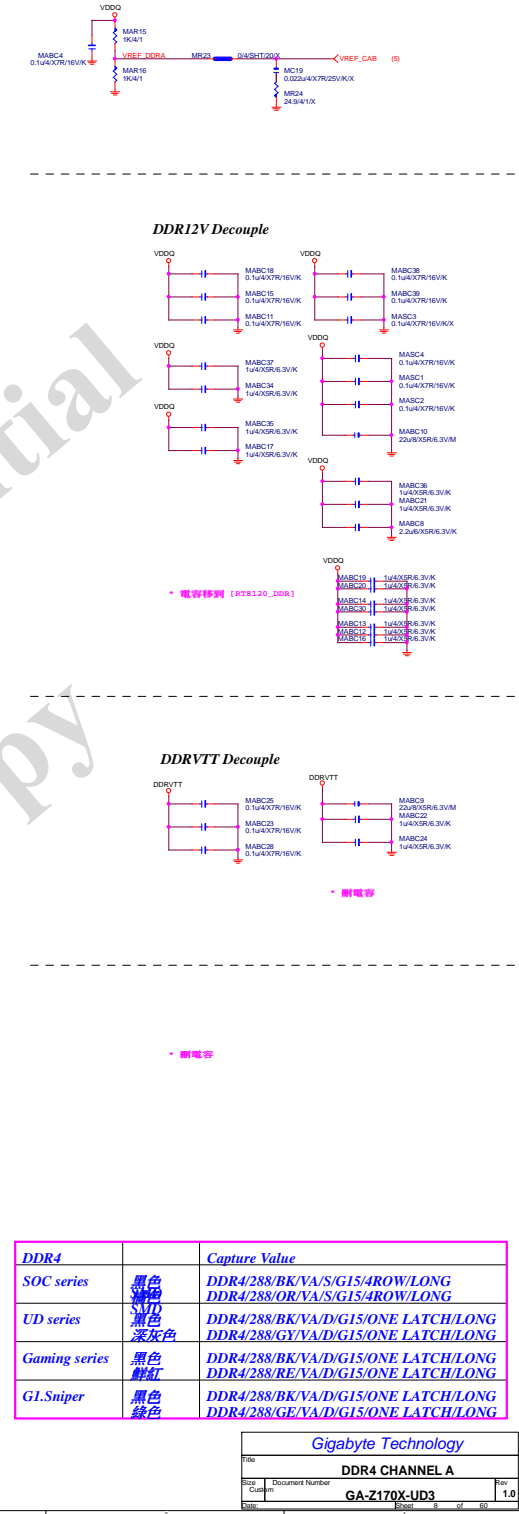
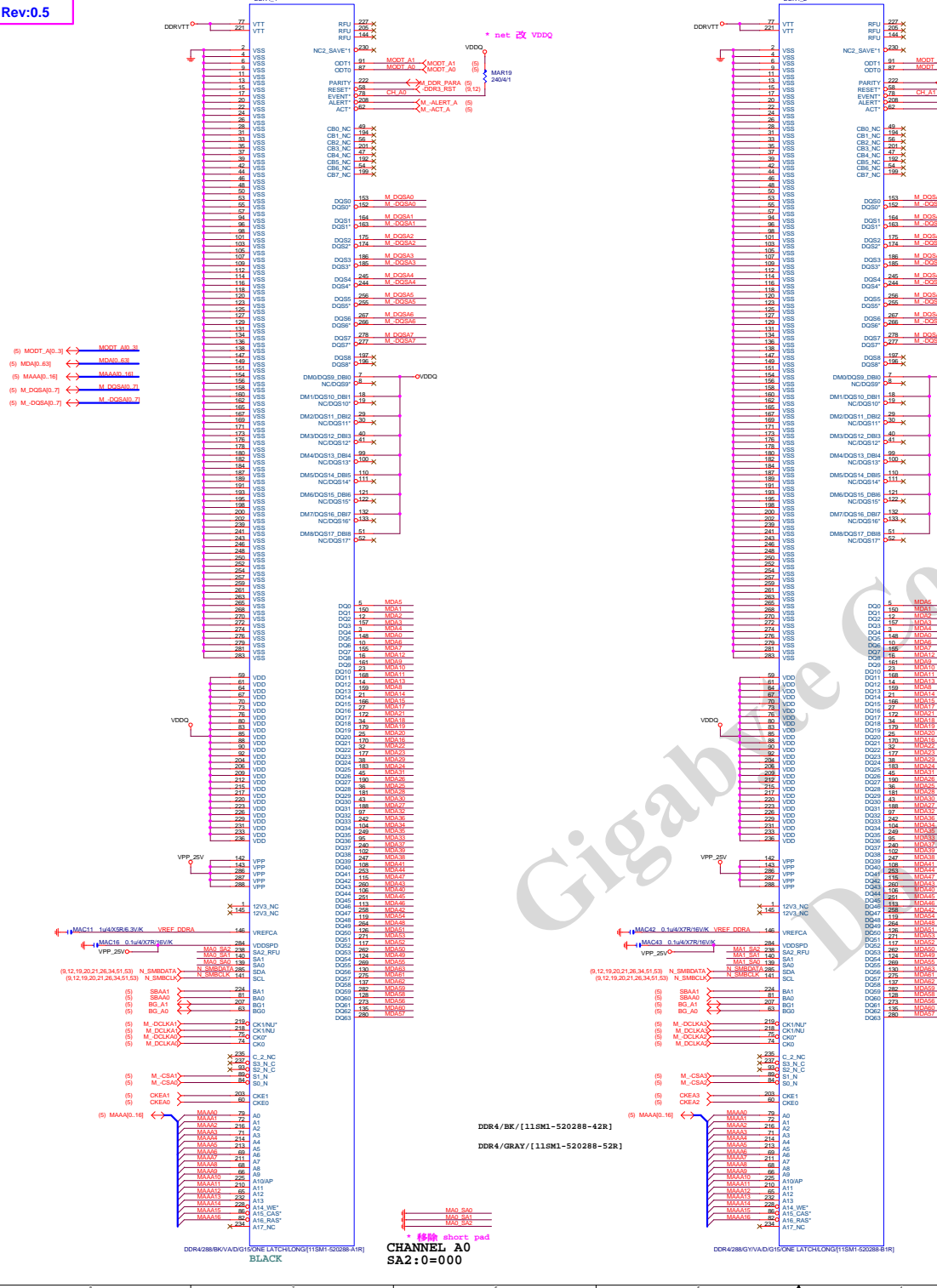
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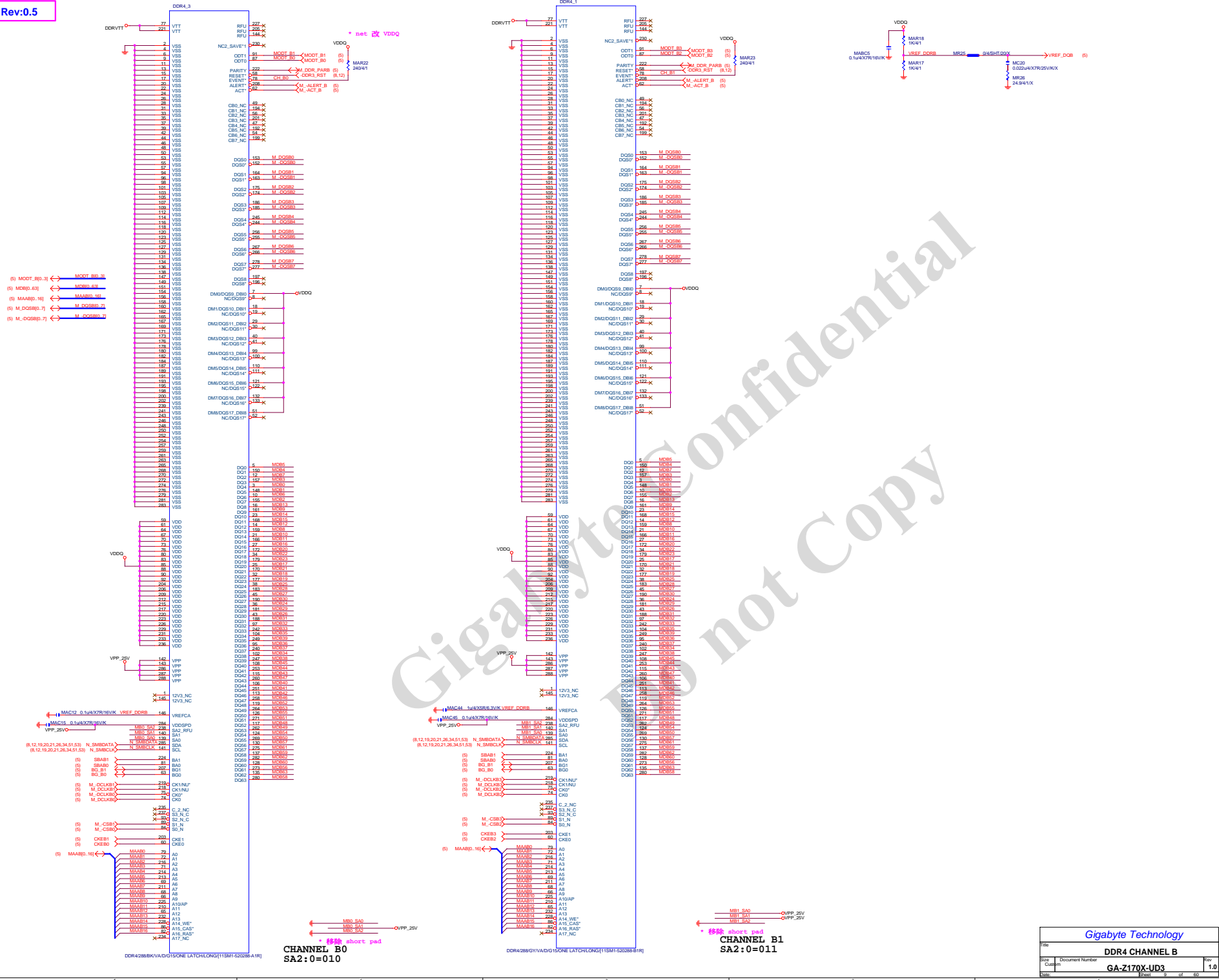
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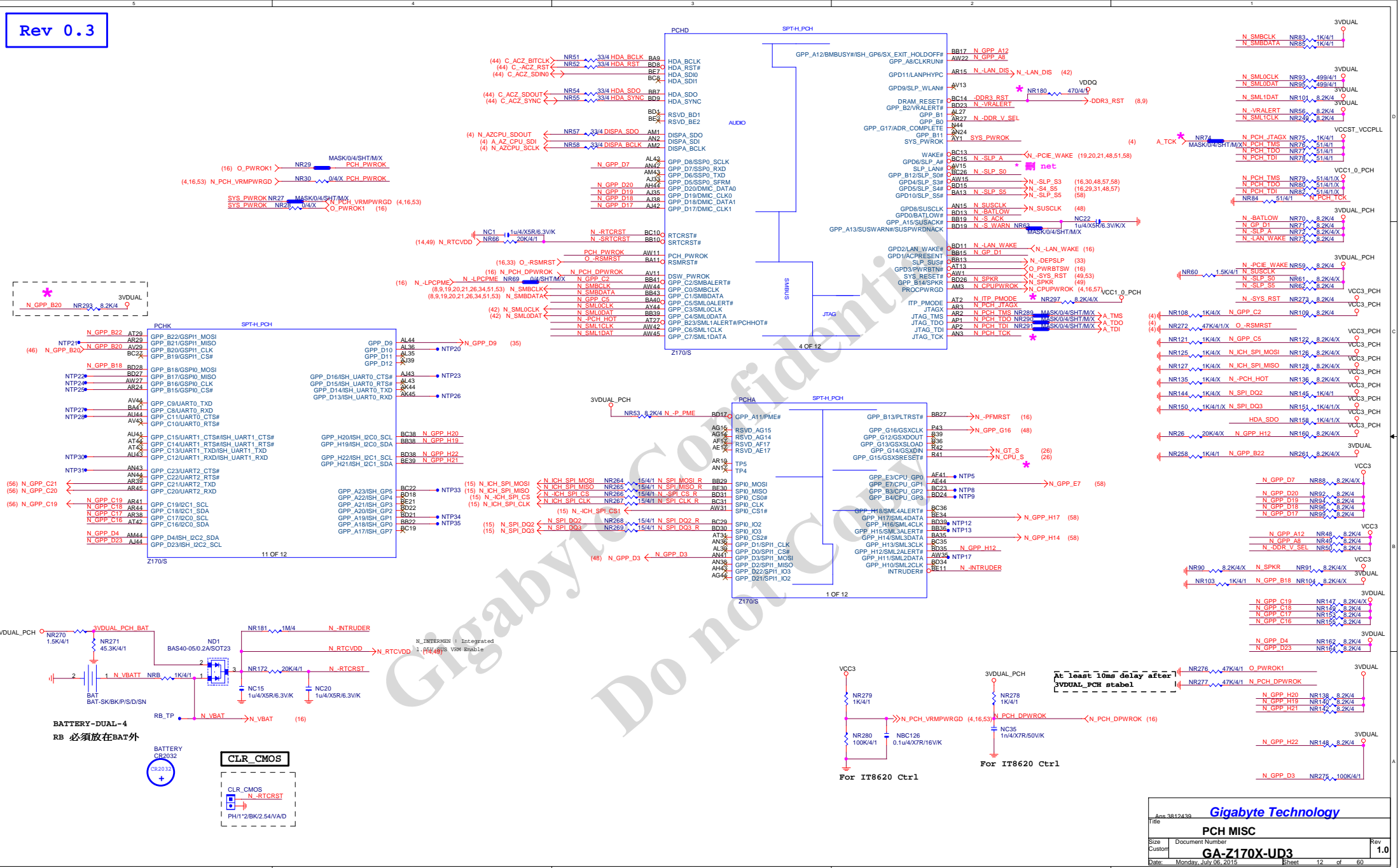
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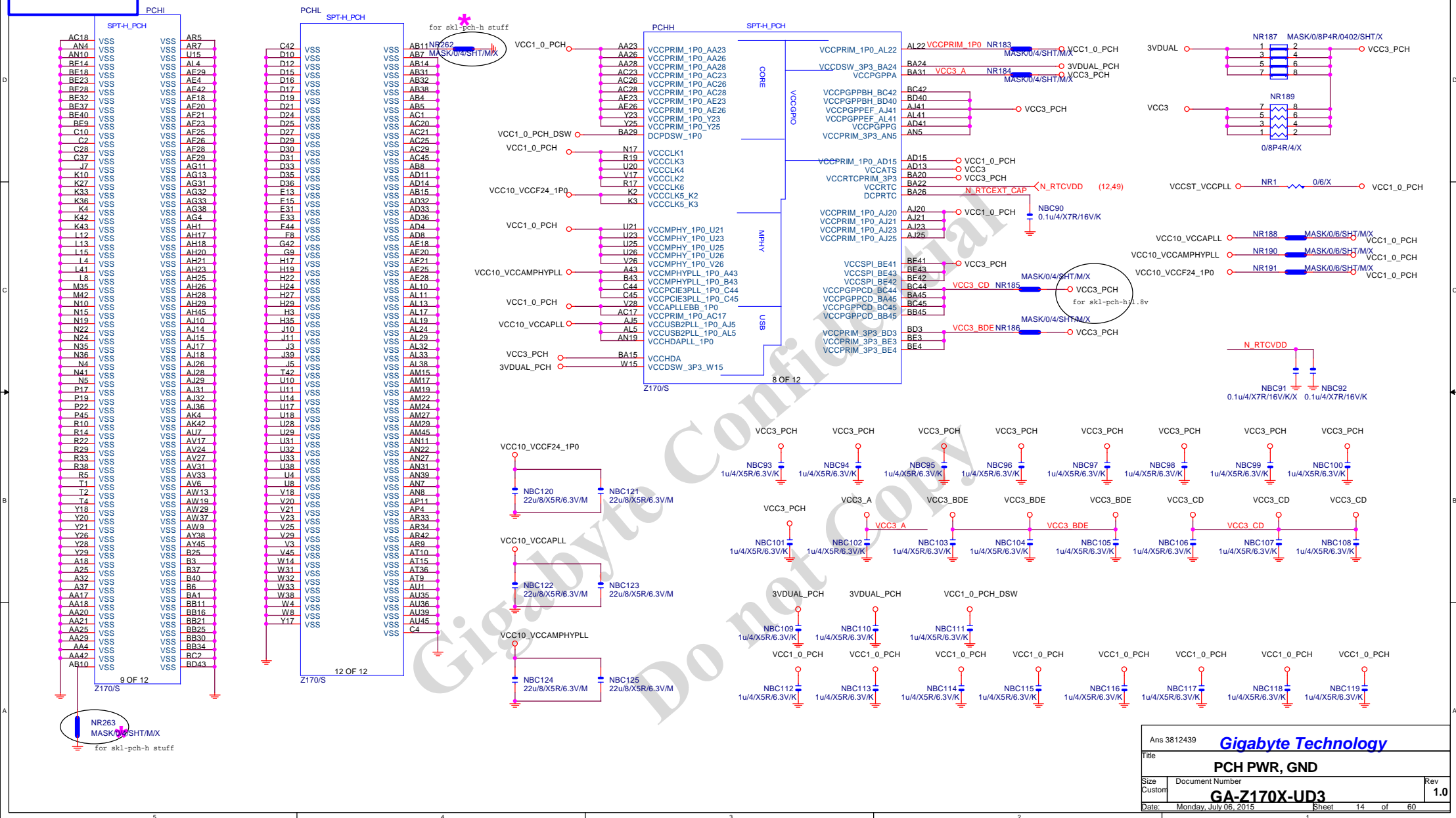
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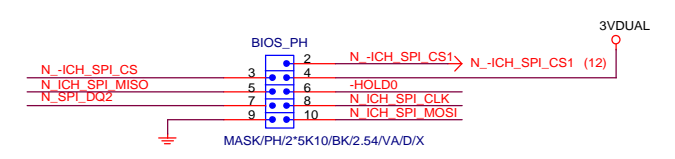
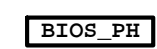
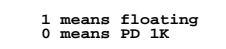


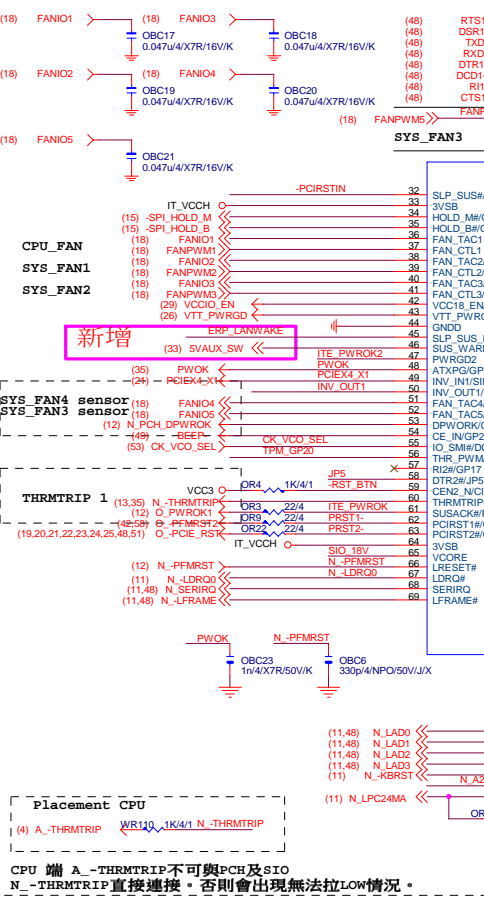






MOSI For DMI RX Termination Voltage

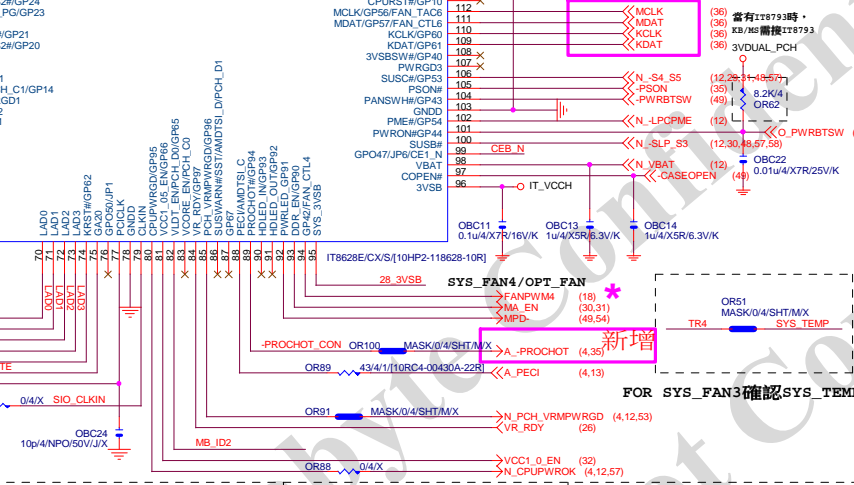




FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL4 FAN_TAC4
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL5 FAN_TAC5
OPT_FAN or SYS_FAN4	FAN_CTL2 FAN_TAC2
THRMTRIP1	YES PIN60

IT8628E GPIO問題匯整	
PIN 50	GP26-第一次接上POWER時會拉 LO
PIN 90/91	DEFAULT為HDLDE FUNCTION, GP93 BYPASS TO GP92 高運時 GP92 會被拉LO(ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用, 不然會互相干擾
PIN 22	PIN22, 需高於3V, 若低於該部分COM PORT及LPT裝置 蜂鳴器會異常動作。

IT8628E_BX



DUAL BIOS OPT STRAP

Power leakage

SIO 18V

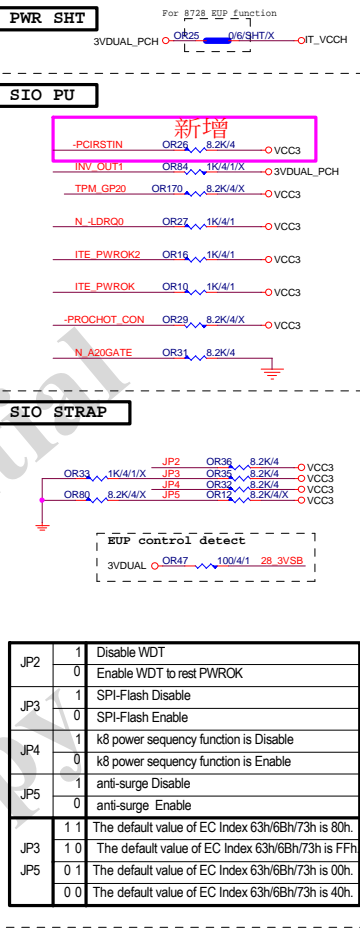
SIO CAP

IT_VCCB

IT_AVCC

3VDUAL_PCH

CLOSE SIO PIN4 VREF_25

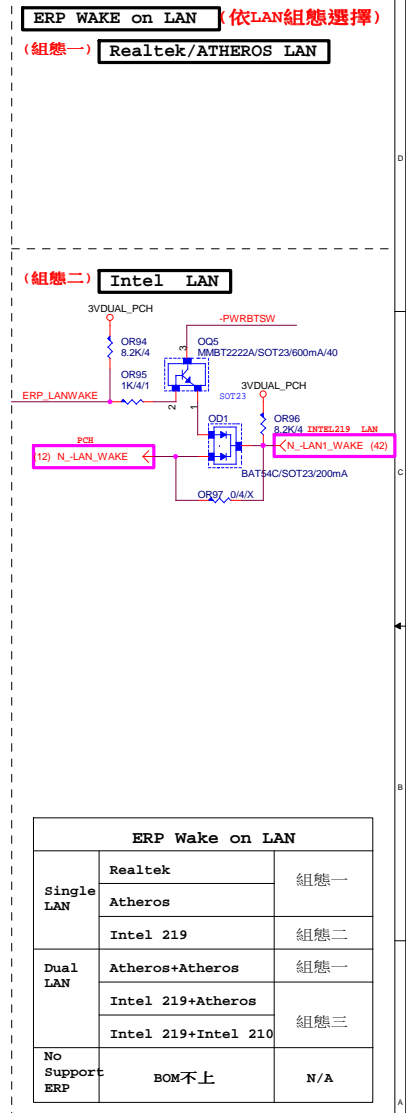


JP2	1	Disable WDT
JP2	0	Enable WDT to rest PWR0K
JP3	1	SPI-Flash Disable
JP3	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP5	1	anti-surge Disable
JP5	0	anti-surge Enable

JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

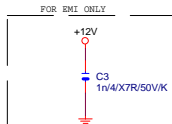
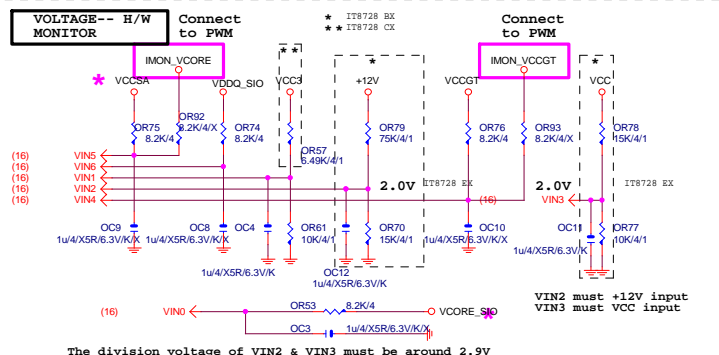
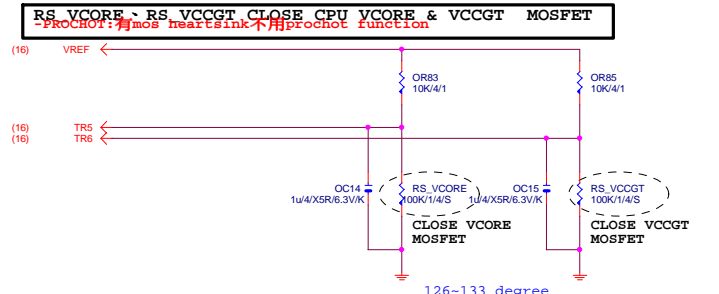
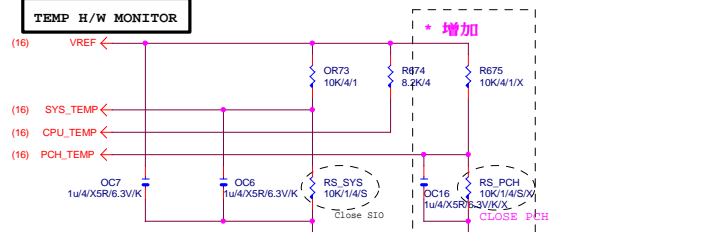
MB ID

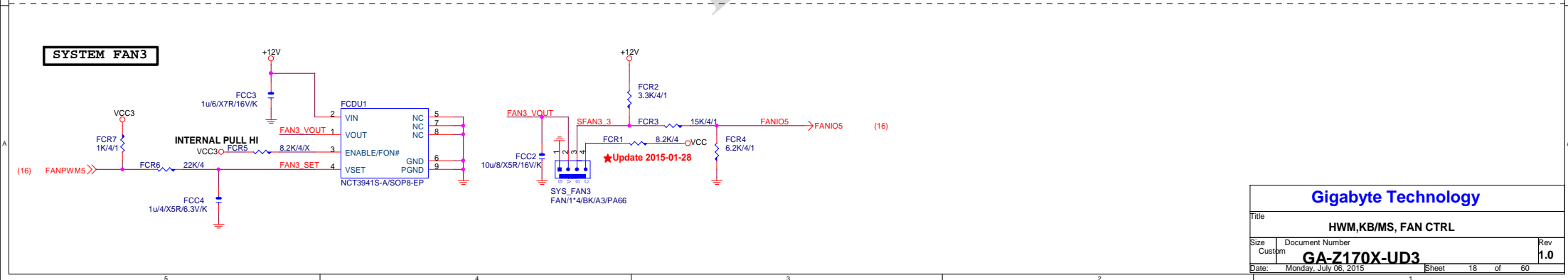
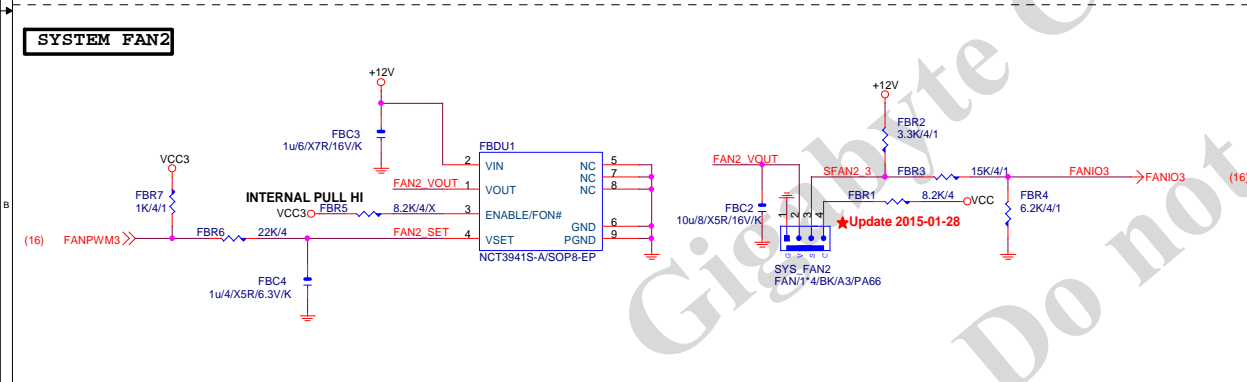
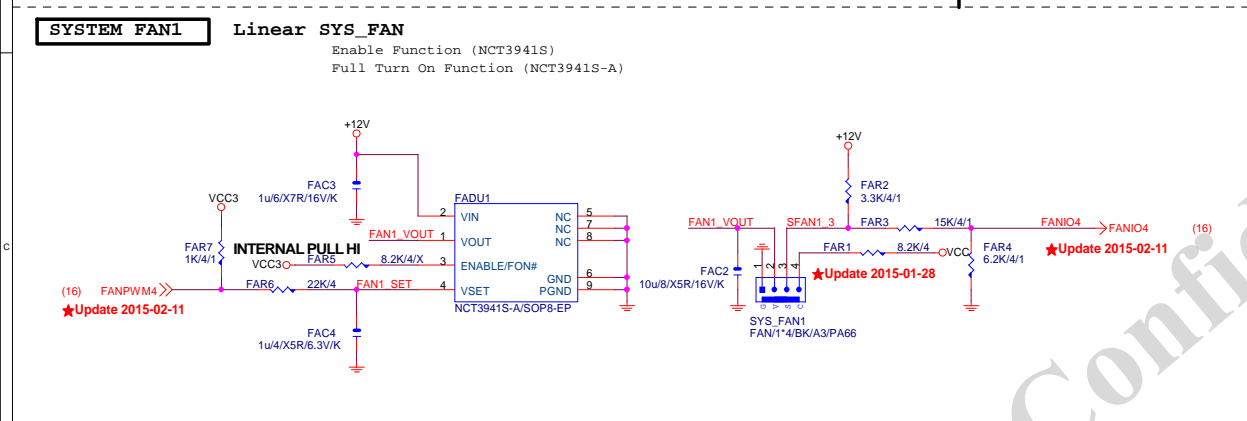
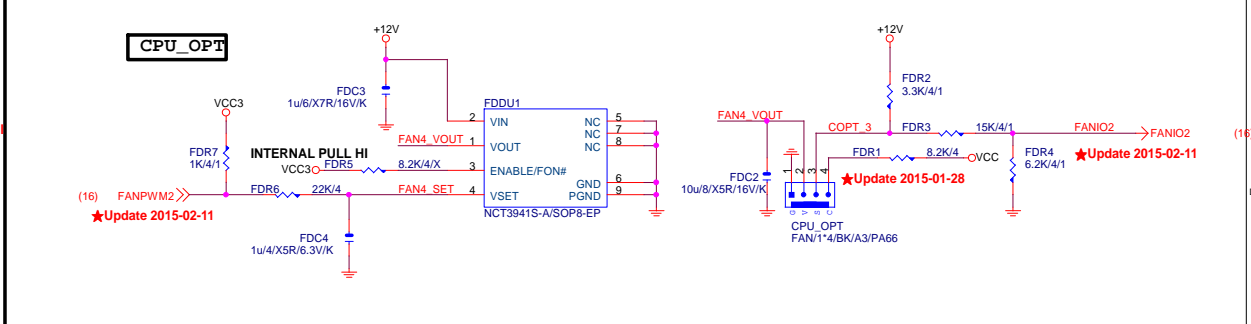
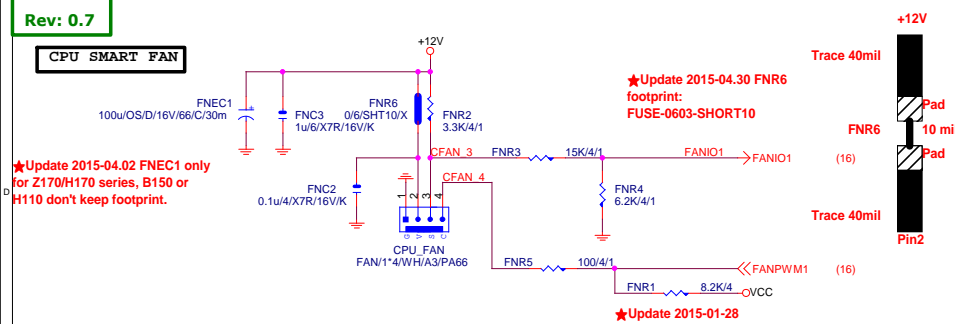
VCC3



ERP Wake on LAN		
Single LAN	Realtek	組態一
	Atheros	組態二
Dual LAN	Intel 219	組態一
	Atheros+Atheros	組態二
No Support ERP	Intel 219+Intel 210	組態三
	BOM不上	N/A

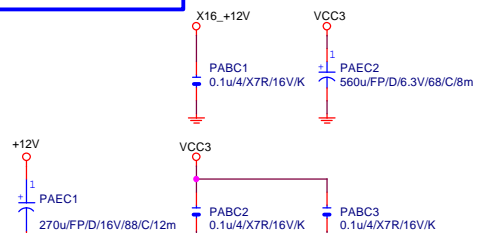
Gigabyte Technology		
ITE 8620 LPC IO		
GA-Z170X-UD3		
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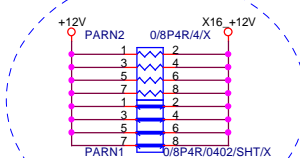
Rev 0.3

PCIEX16 CAP



PCIEX16 PROTECT SHT

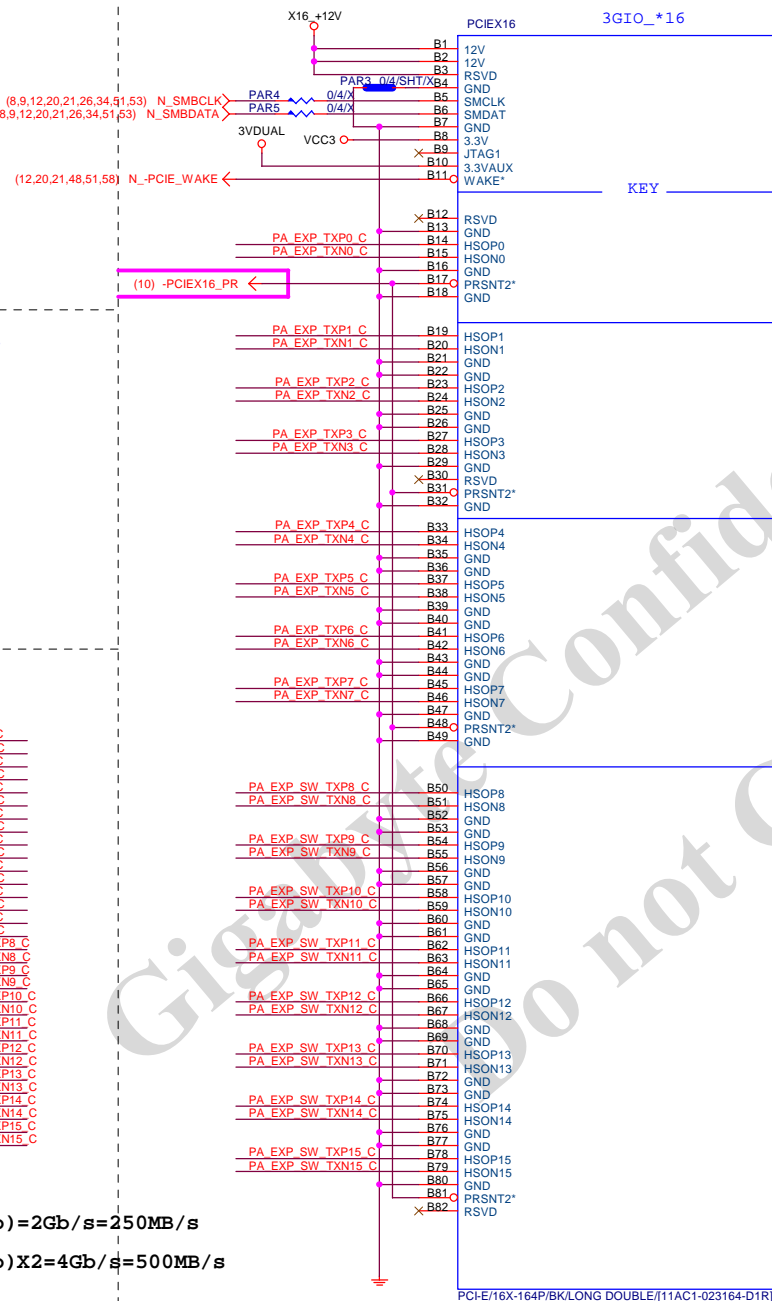
+12 protect short-wire test



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP SW TXN15 C

PCIEX16 SLOT



PCIESLOT-164DN-Q

PCIEX16 3GIO_*16

PCI-E/16X-164P/BK/LONG DOUBLE/[11AC1-023164-D1R]

PCIEX16:16/5/5/5/16

PA EXP RXP0.15] >> PA_EXP_RXP0[0..15] (4,52)

PA EXP RXN0.15] >> PA_EXP_RXN0[0..15] (4,52)

PA EXP TXP0.15] >> PA_EXP_TXP0[0..15] (4,52)

PA EXP TXN0.15] >> PA_EXP_TXN0[0..15] (4,52)

PA EXP SW RXP8.15] >> PA_EXP_SW_RXP8[8..15] (52)

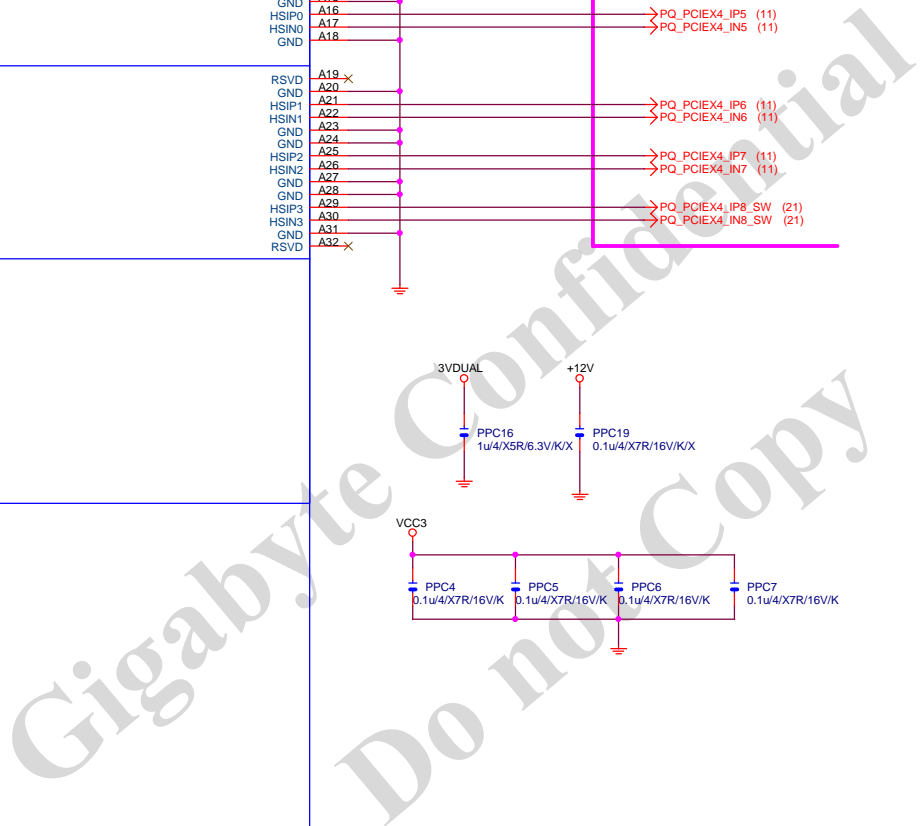
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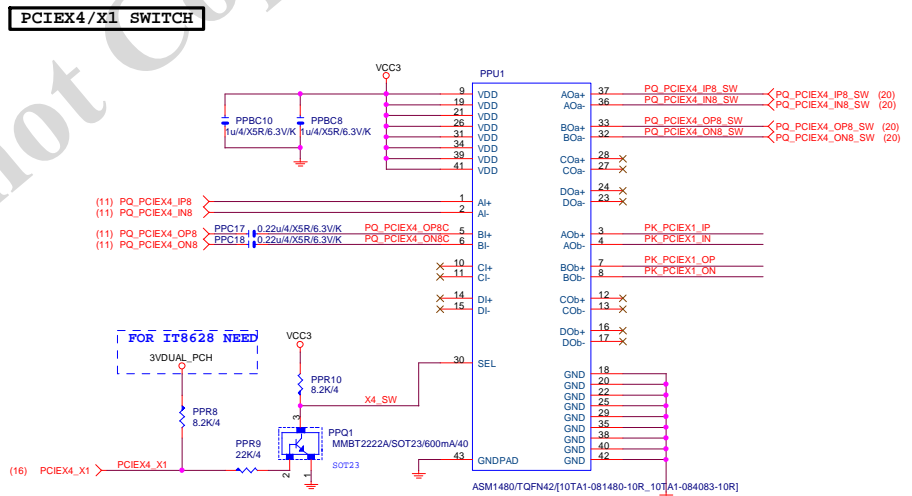
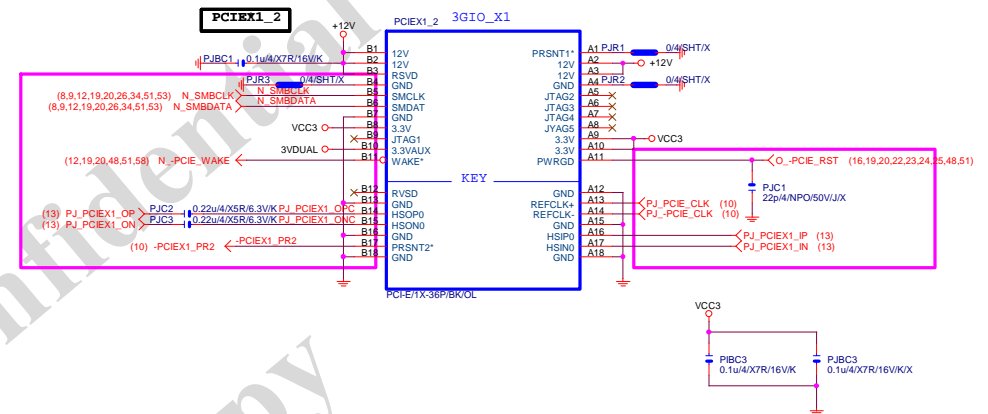
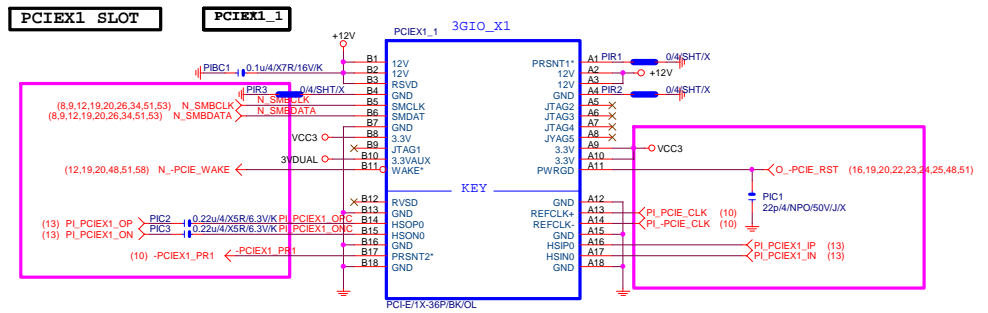
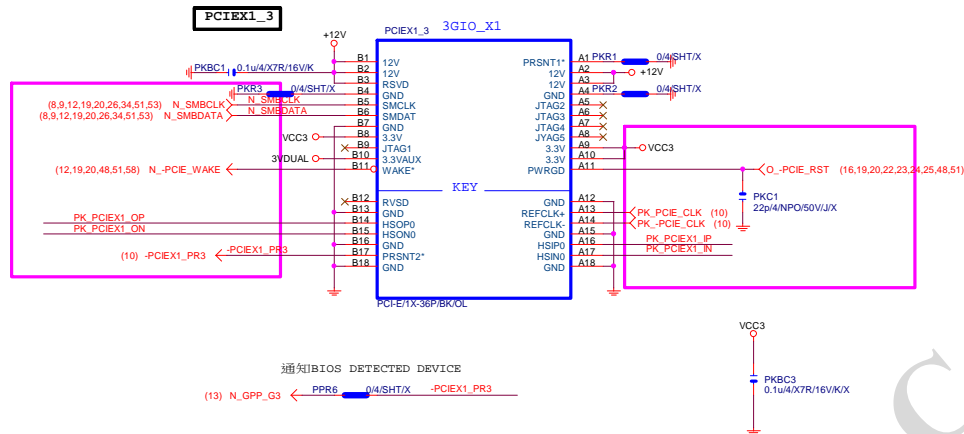
PA EXP SW TXP8.15] >> PA_EXP_SW_TXP8[8..15] (52)

PA EXP SW TXN8.15] >> PA_EXP_SW_TXN8[8..15] (52)

Gigabyte Technology

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Size	Document Number	GA-Z170X-UD3	
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	N_GPP_G3 (PCH_GPP_G3)	PCIEX4_X1 (SIO_GPIO26)
PCIEX1,PCIEX4 --> X1 (Default)	H	H
PCIEX4 No devices PCIEX4 -> X1	H	H
PCIEX4 Have devices PCIEX4 -> X4 PCIEX1 1/2 --> N/A	L	L

Function	SEL
xI--> x0a	L;PCIEX4 SLOT-->X
xI--> x0b	H;PCIEX4 SLOT-->X

M.2 Lane2 from PCH port19

(56) M2_PCIE_IN13 < 0.22u/4/X5R/6.3V/K M2DC15
(56) M2_PCIE_IP13 < 0.22u/4/X5R/6.3V/K M2DC16
(56) M2_PCIE_TP13 < M2_PCIE_TN13_C M2_PCIE_TP13_C

M.2 Lane2 from PCH port20

(56) M2_PCIE_IN14 < 0.22u/4/X5R/6.3V/K M2DC9
(56) M2_PCIE_IP14 < 0.22u/4/X5R/6.3V/K M2DC10
(56) M2_PCIE_TP14 < M2_PCIE_TN14_C M2_PCIE_TP14_C

M.2 Lane3 from PCH port21

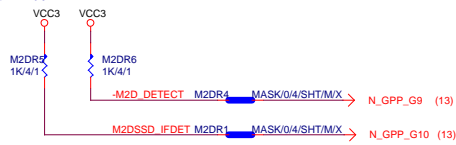
(56) M2_PCIE_IN15 < 0.22u/4/X5R/6.3V/K M2DC35
(56) M2_PCIE_IP15 < 0.22u/4/X5R/6.3V/K M2DC36
(56) M2_PCIE_TP15 < M2_PCIE_TN15_C M2_PCIE_TP15_C

M.2 Lane4 from PCH port22

(56) M2_PCIE_IP16 < 0.22u/4/X5R/6.3V/K M2DC33
(56) M2_PCIE_IP16 < 0.22u/4/X5R/6.3V/K M2DC34
(56) M2_PCIE_TP16 < M2_PCIE_TN16_C M2_PCIE_TP16_C

(10) CK_M2D_100M_DN
(10) CK_M2D_100M_DP
需與M2_-CLKREQ對應

支援SATA and M.2 function



M.2-SATA(S3)+SATA S0&S1&S2

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	H (SATA)	GPP_C21	H

M.2-SATA(S3)+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	L (S.E.)	GPP_C21	H

M.2X4

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	H	GPP_C21	H

M.2X2+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	L	GPP_C21	H

M.2X2+SATA S0&S1

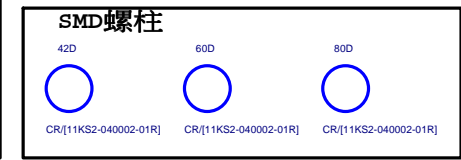
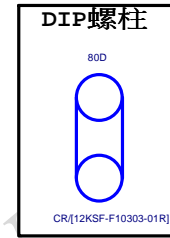
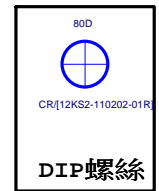
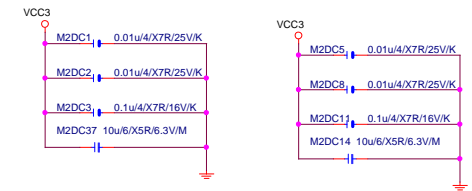
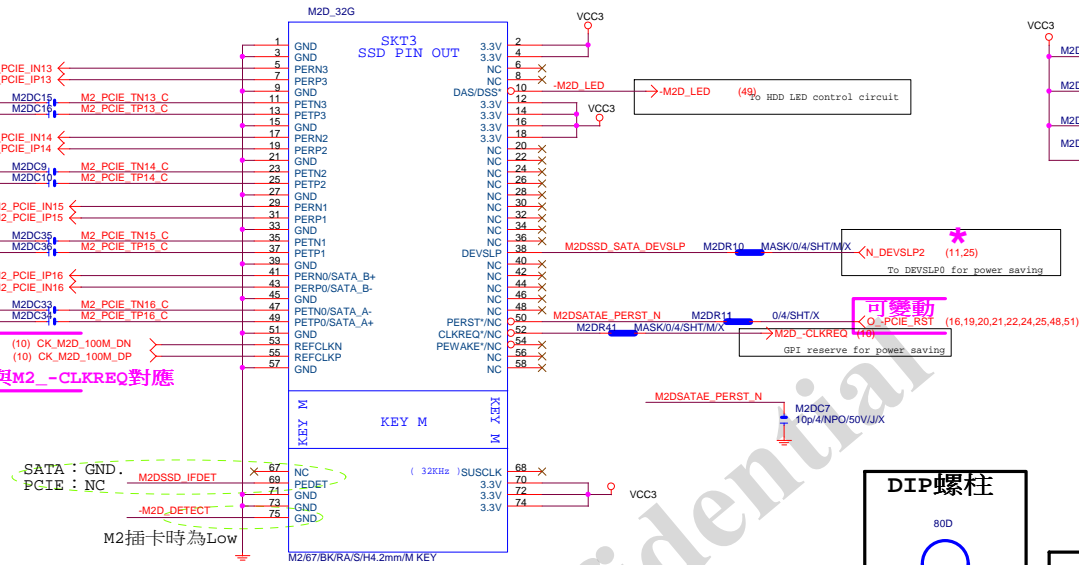
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	H	GPP_C21	H

M.2沒插卡+SATA S0~S3

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	H	GPP_C21	L

M.2沒插卡+S.E.C&S.E.D

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	L	GPP_C21	L



* check
文字面 01/23/45
NET (45/23/01)

SATA EXPRESS料號

雙層:TBD

單層+2SATA:11NR6-C10236-03R

單層:11NR6-C10118-03R

VCC3

SEDR11
1K4/1/X

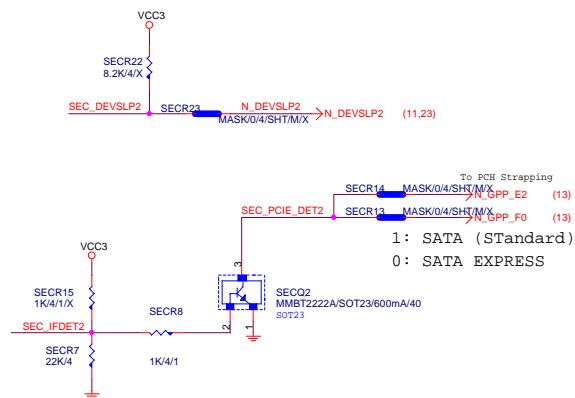
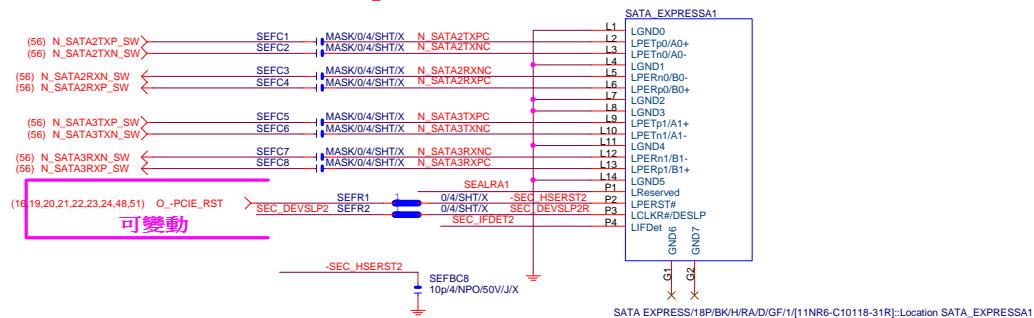
SED_IFDET4

SEDR6
22K/4

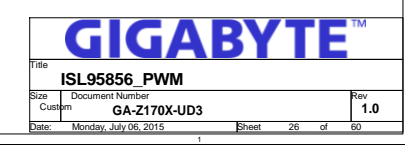
1K/4

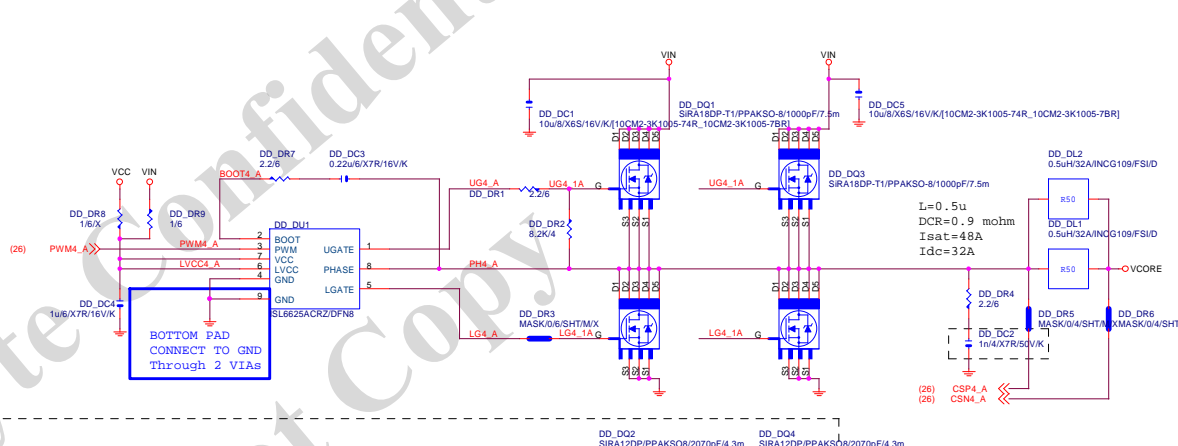
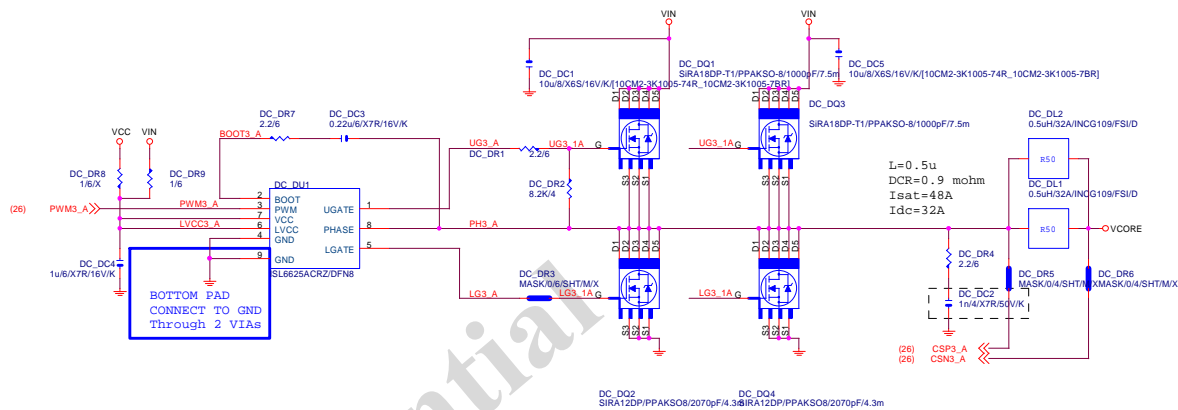
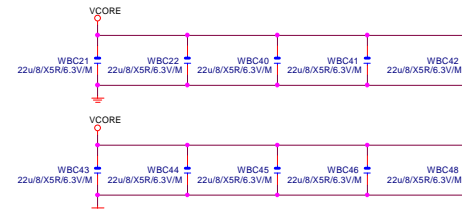
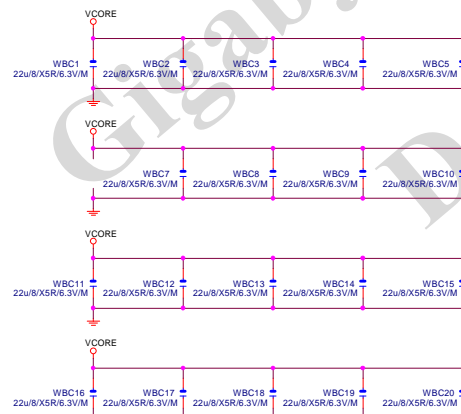
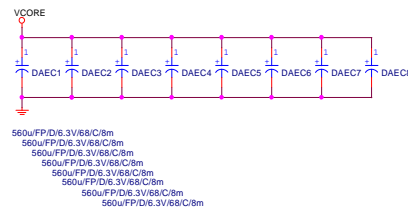
M.2 有插卡 / 沒插卡 GPP_G9	M.2插何種卡? GPP_G10	SATA Express 插何種硬碟? GPP_E0/E1/E2/F0	IO19 (S0)	IO20 (S1)	IO21 (S2)	IO22 (S3)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA	SATA	SATA	SATA (For M2)
		SATA Express (Low)	SATA	SATA	SATA	SATA (For M2)
	PCIe Mode (Hi)	SATA (Hi)	PCIe4 (For M.2)			
		SATA Express (Low)	PCIe4 (For M.2)			
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	SATA (S0)	SATA (S1)	SATA (S2)	SATA (S3)
		SATA Express (Low)	SATA Express (For S.E.0)		SATA Express (For S.E.1)	

SATA 5	(文字面寫SATA 1)
SATA 4	(文字面寫SATA 0)
SATA 3	
SATA 2	
SATA 1	(文字面寫SATA 5)
SATA 0	(文字面寫SATA 4)

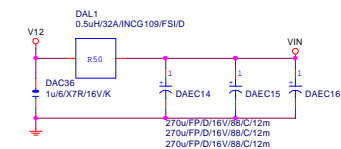
SATA EXPRESS 下層 To SATA3
port2/3

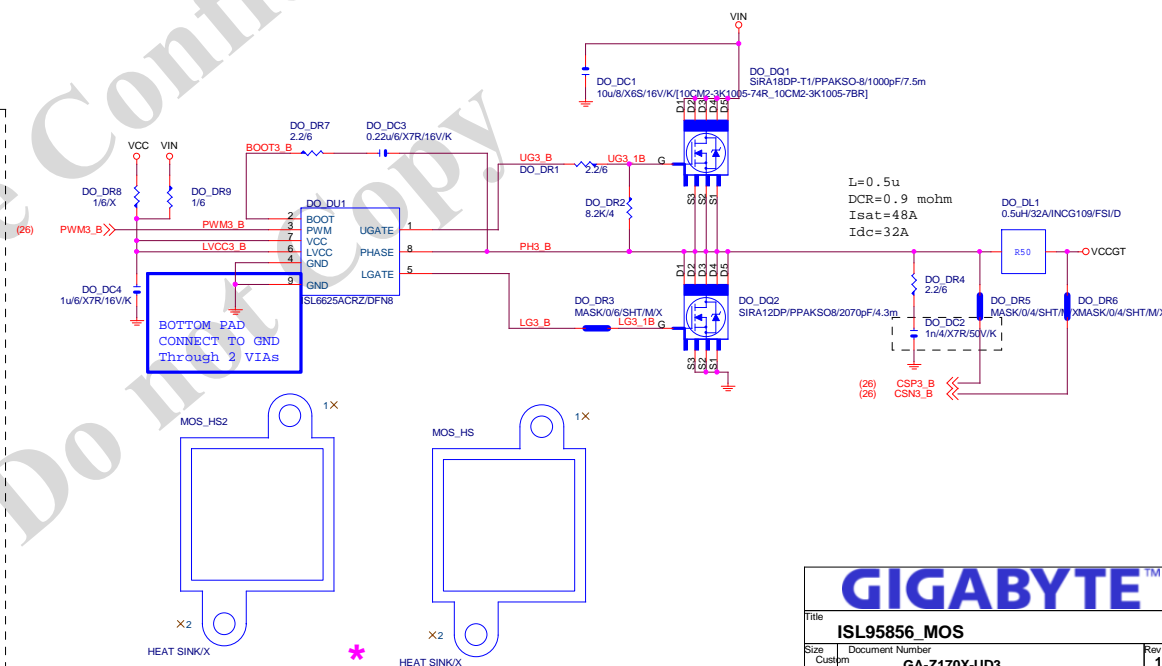
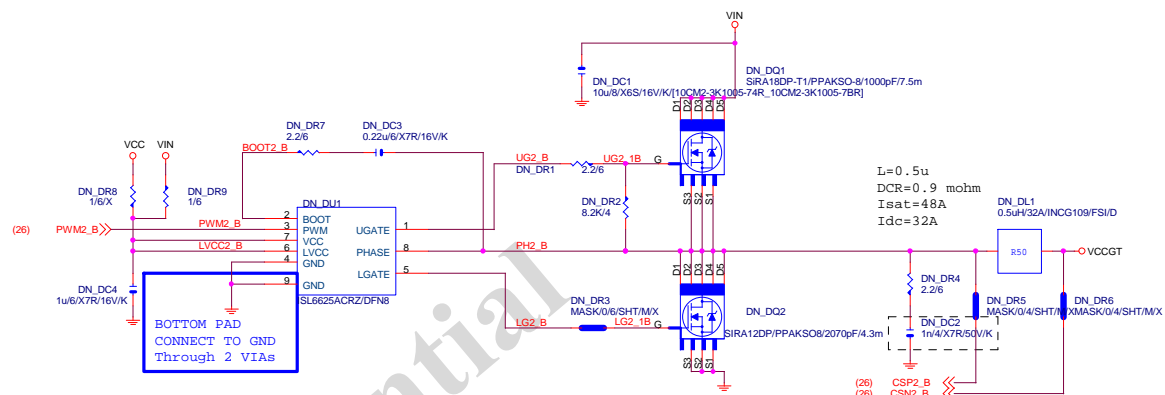
SATA 5 (文字面寫SATA 1)
SATA 4 (文字面寫SATA 0)
SATA 3
SATA 2
SATA 1 (文字面寫SATA 5)
SATA 0 (文字面寫SATA 4)



VCORE CAP 560u*8PCS
22u*29PCS

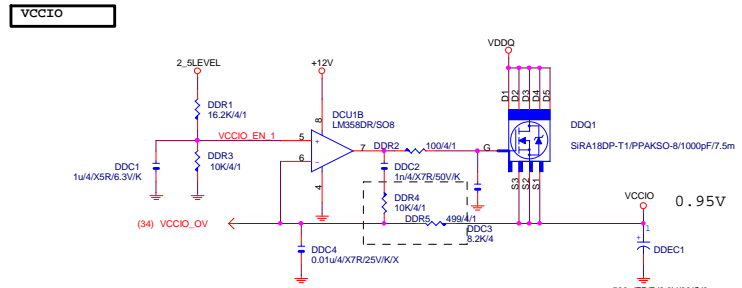
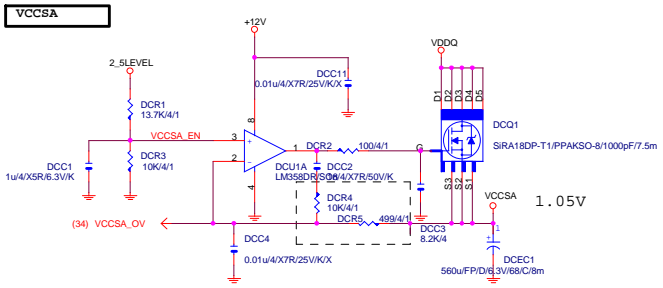
VIN CAP 270u*3PCS



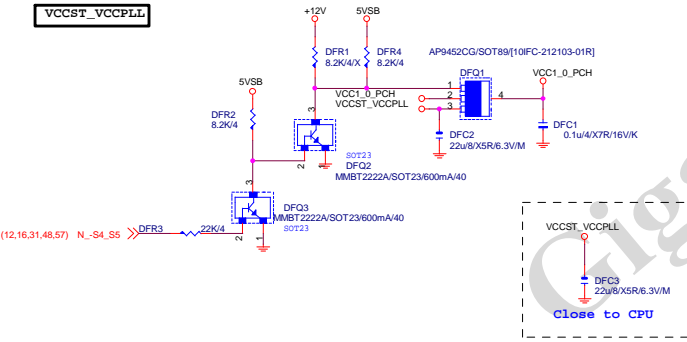
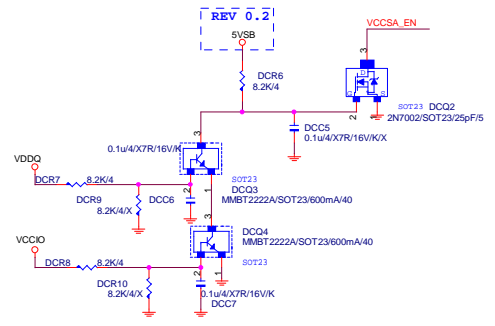
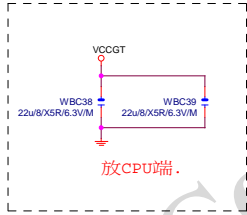


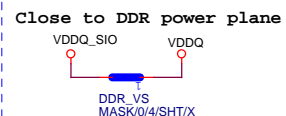
GIGABYTE

Title			
ISL95856_MOS			
Size	Document Number	Rev	
Custom	GA-Z170X-UD3	1.0	
Date:	Monday, July 06, 2015	Sheet	28 of 60

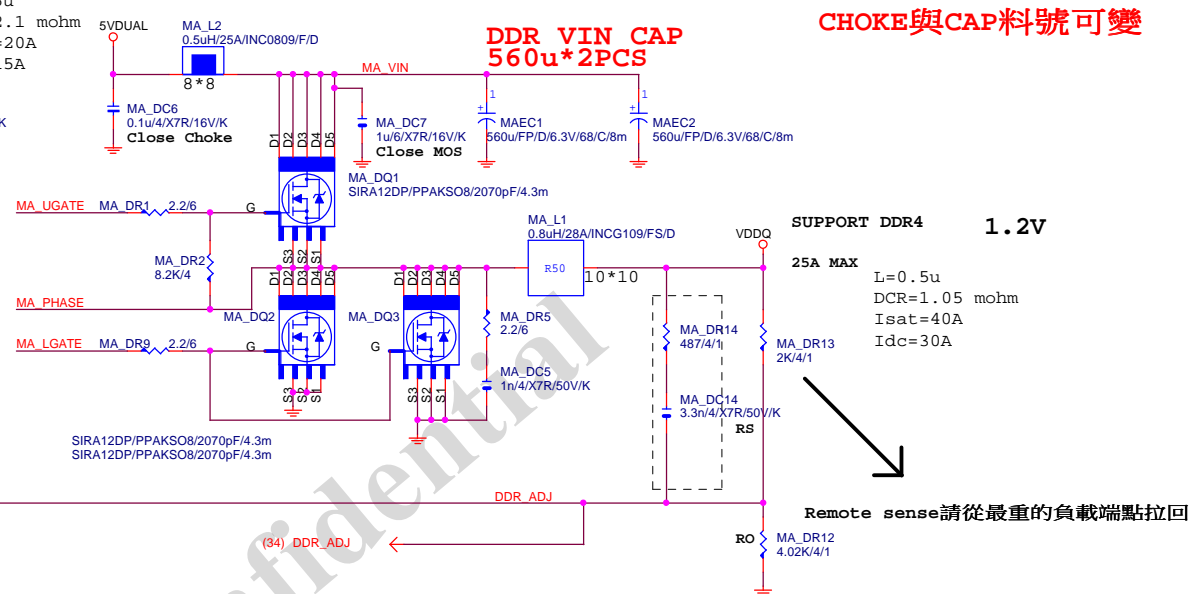


Connect to IT8620

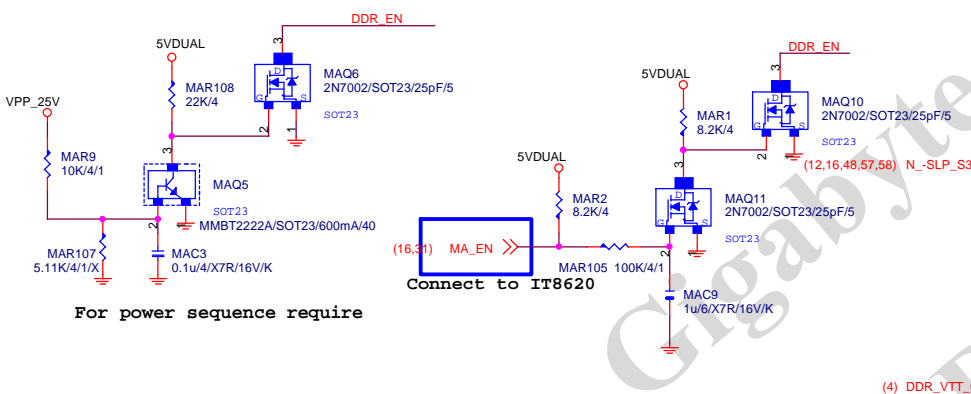




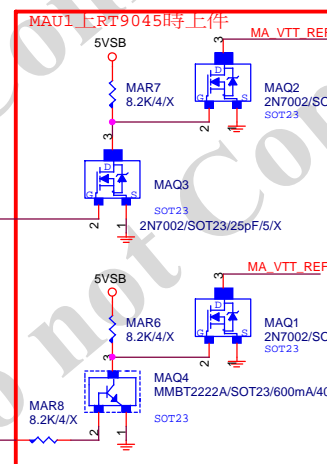
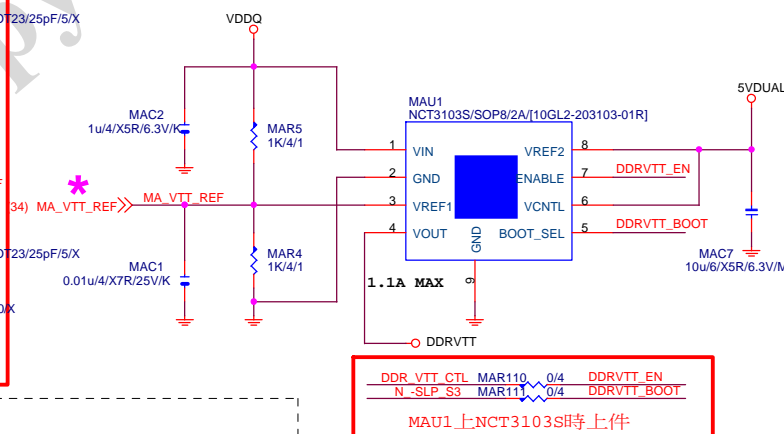
放靠近IC pin4



PWR SEQ

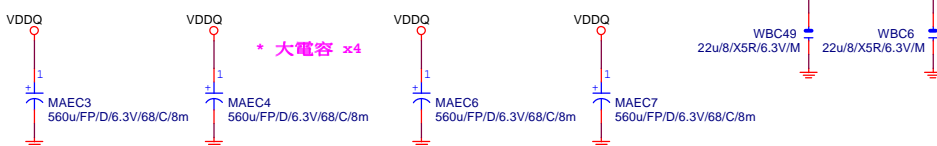


(4) DDR_VTT

**DDRVTT**

MAU1上NCT3103S時上件

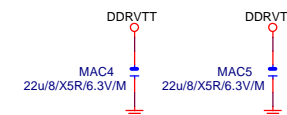
DDR CAP 560u*4PCS 22u*2PCS



* 大電容 x4

DDRVTT CAP

* 大電容 x0

**GIGABYTE™**

Title
RT8120 DDR4 POWER

Size	Document Number
Custom	GA-Z170X-UD3

Rev	1.0
-----	-----

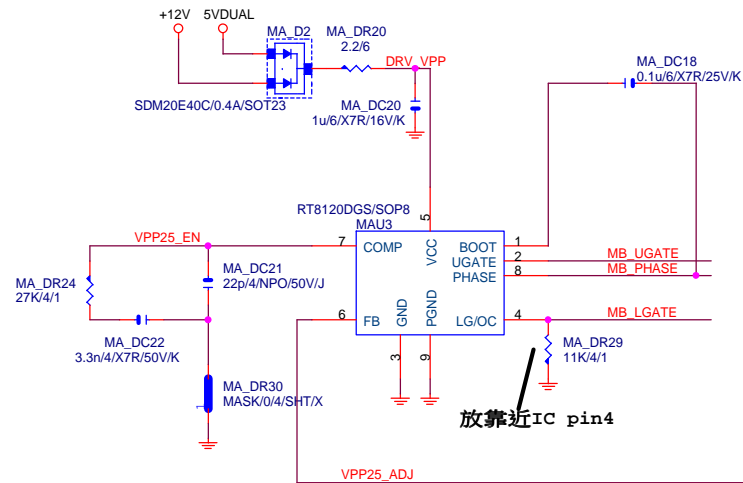
Date: Monday, July 06, 2015

Sheet

0	of	60
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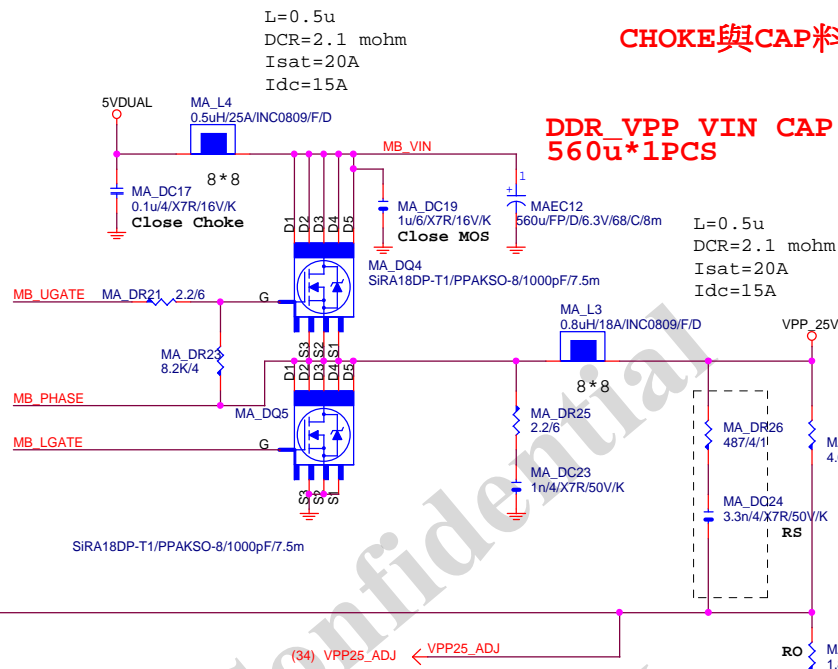
REV:0.84

VPP_25V



放靠近IC pin4

VPP25_ADJ



CHOKE與CAP料號可變

DDR_VPP VIN CAP
560u*1PCSL=0.5u
DCR=2.1 mohm
Isat=20A
Idc=15A

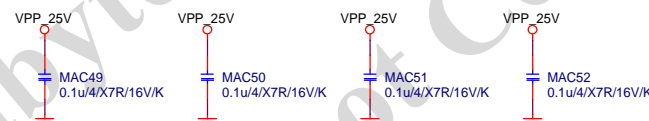
SUPPORT DDR4 2.5V

25A MAX

Remote sense請從最重的負載端點拉回

PWR_SEQ

* 刪 MA_DR32



VPP CAP 560u*1PCS

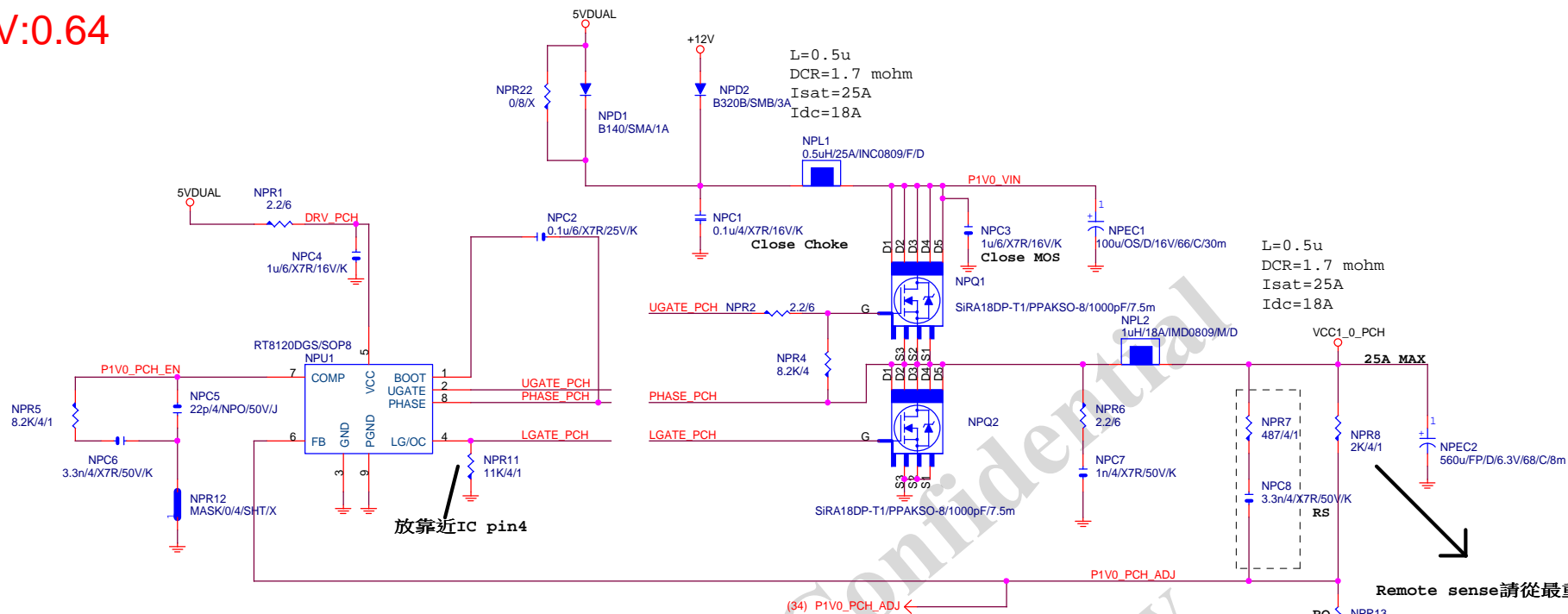
* 大電容 x1



GIGABYTE™

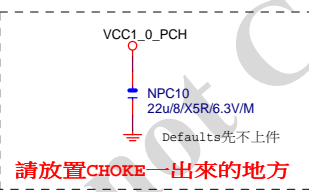
Title RT8120_VPP25 POWER		
Size Custom	Document Number GA-Z170X-UD3	Rev 1.0
Date: Monday, July 06, 2015	Sheet 31	of 60

REV:0.64



Remote sense請從最重的負載端點拉回

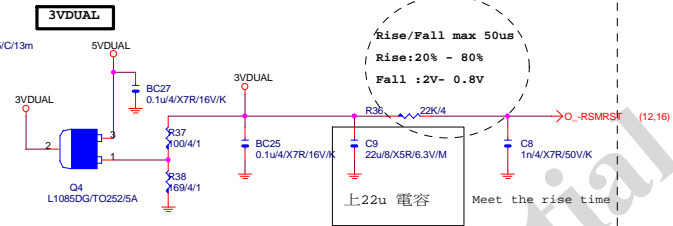
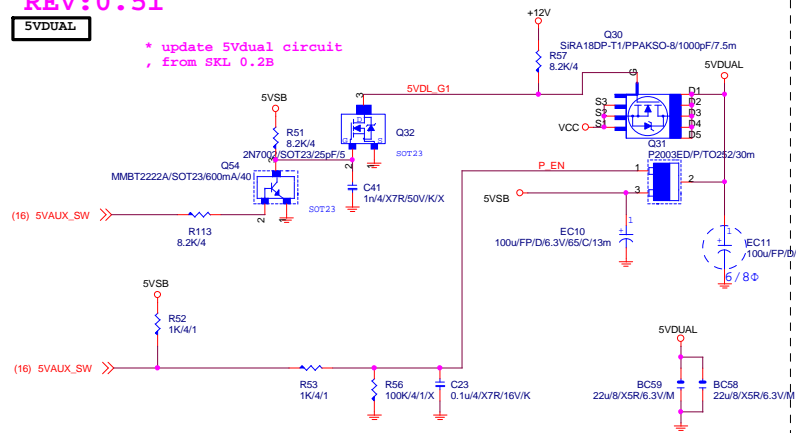
$$\begin{aligned} 0.8 * (1 + RS / RO) &= V_{out} \\ 0.8 * [1 + 2K / 8K] &= 1.0V \end{aligned}$$



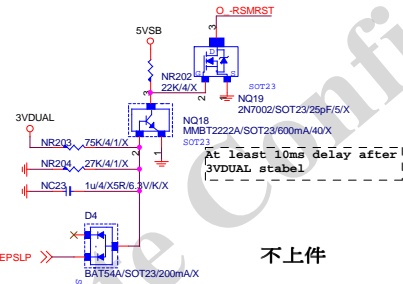
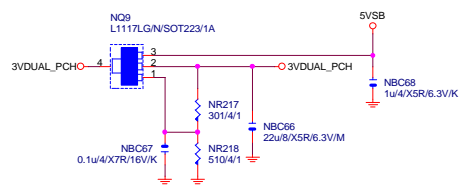
GIGABYTE™			
Title			
RT8120_PCH POWER			
Size	Document Number	Rev	
Custom	GA-Z170X-UD3	1.0	
Date:	Monday, July 06, 2015	Sheet	32 of 60

5VDUAL

```
* update 5Vdual circuit
, from SKL 0.2B
```

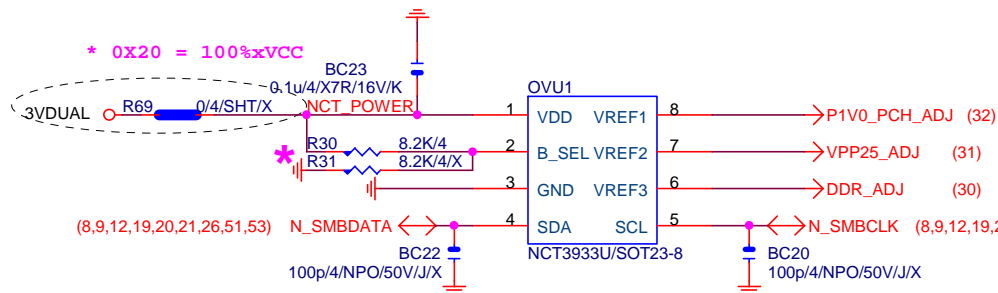


3VDUAL_PCH

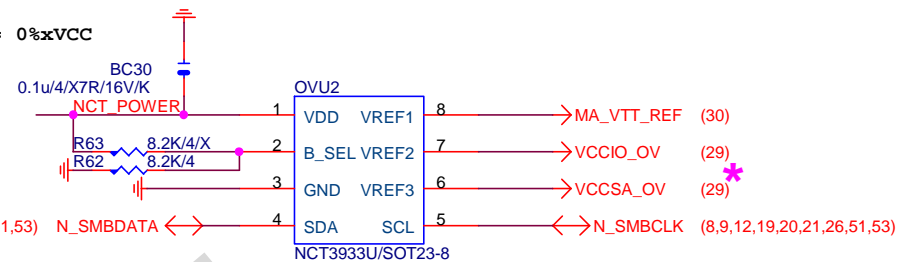


不上件

OVER VOLTAGE



0X2A = 0%xVCC



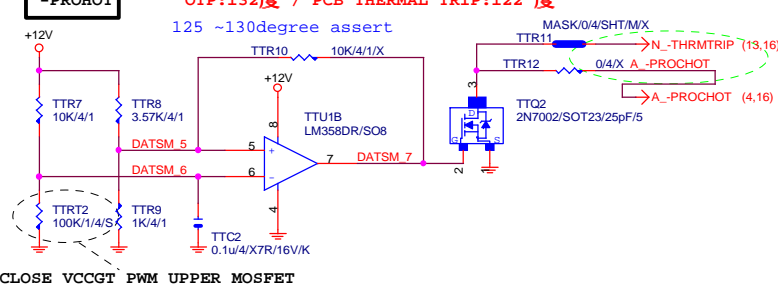
0X22 = 75%xVCC

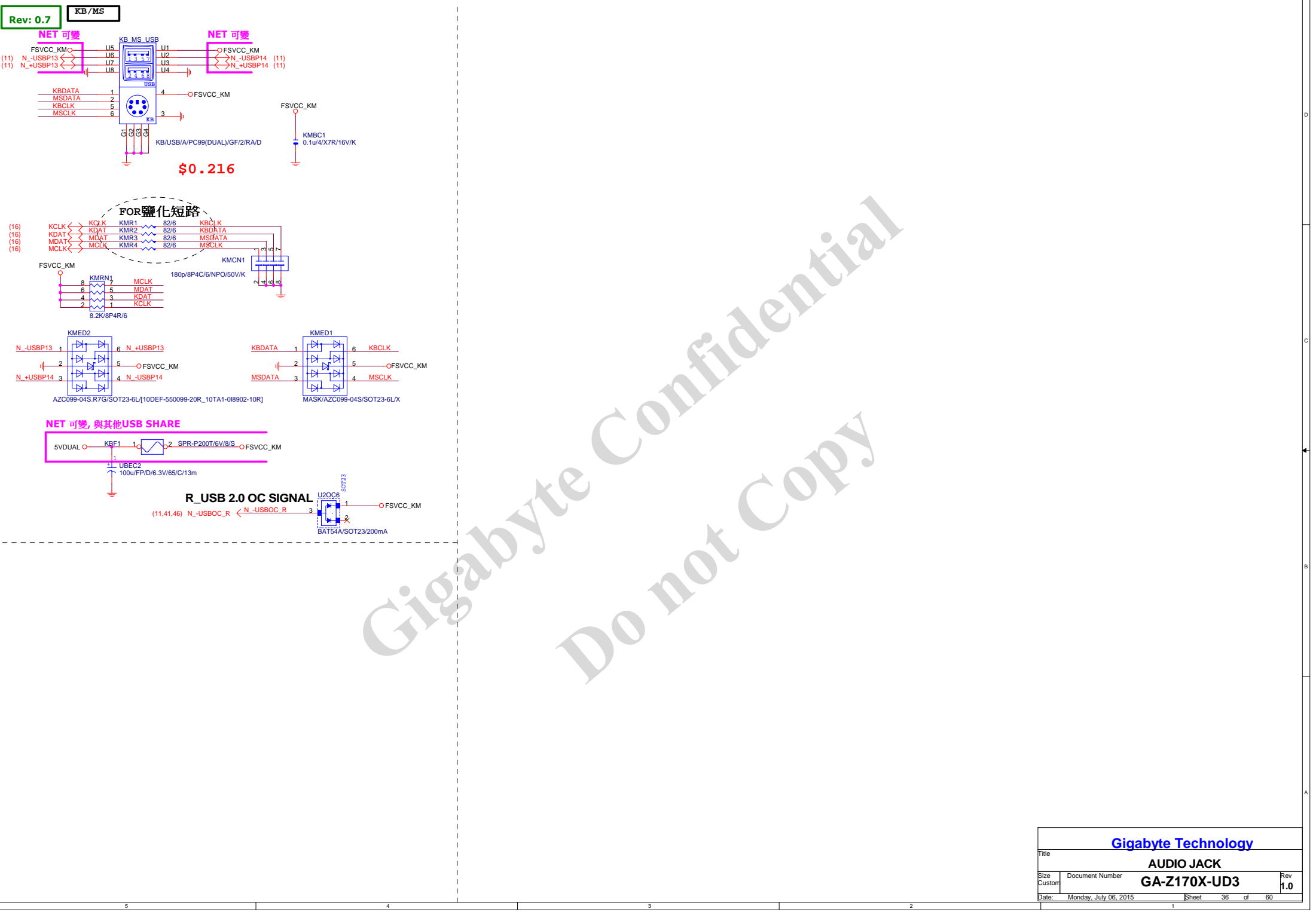
* 删除 OVU3

NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

Gigabyte Technology			
Title			
CPU CORE VR-2			
Size	Document Number	GA-Z170X-UD3	
Custom		Rev 1.0	
Date:	Monday, July 06, 2015	Sheet	34 of 60

Patch some PSU no internal
pull up resistor



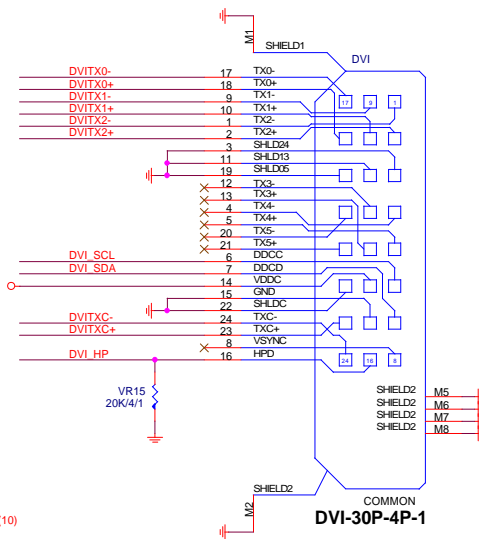
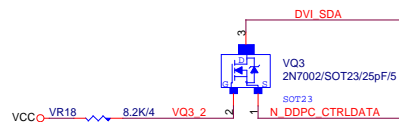
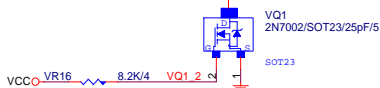
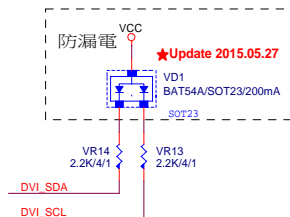


Gigabyte Confidential

Do not Copy

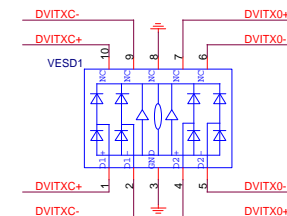
DVI CONN

NET 可變



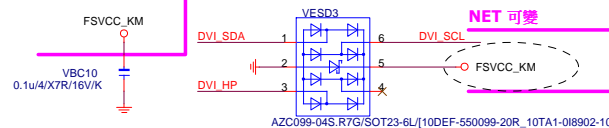
DVI-D/24P/SC/RA/D/SH/[11NR6-501024-31R]

AZ1045-04F/MSOP10



AZ1045-04F/MSOP10

NET 可變



Gigabyte Technology

Title			
FP,F_USB,USB PWR,BZ			
Size Custom	Document Number	GA-Z170X-UD3	Rev 1.0
Date:	Monday, July 06, 2015	Sheet 37 of 60	

省X'TAL COST DOWN:

1. 上件:

DVC28 [10p/4/NPO/50V/J]

DVC11 [10p/4/NPO/50V/J]~修改值

DVR10 [8.2K/4]

2. 删除:

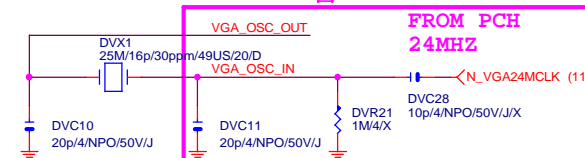
DVX1 [25M/16p/30ppm/49US/20/D]

DVC10 [20p/4/NPO/50V/J]

DVR9 [8.2K/4]

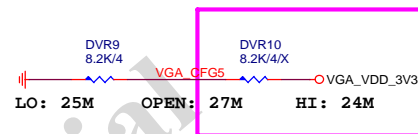
25M Crystal

省X'TAL COST DOWN

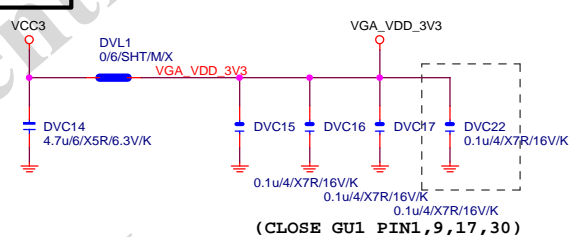


CFG5

For Crystal Less



ADAPTER POWER

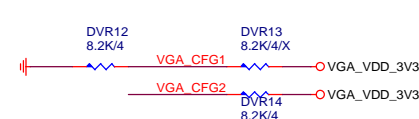
LDO MODE: DVL2, DVC23-->X
S.W MODE: DVL2, DVC23-->O

(CLOSE GU1 PIN31)

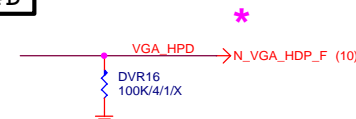
(CLOSE GU1 PIN6,27,28)

CFG1&2

Non-Compliant



HPD

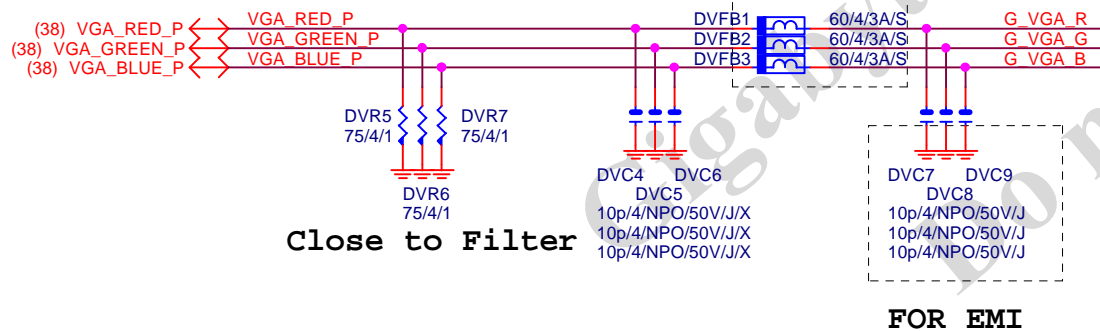
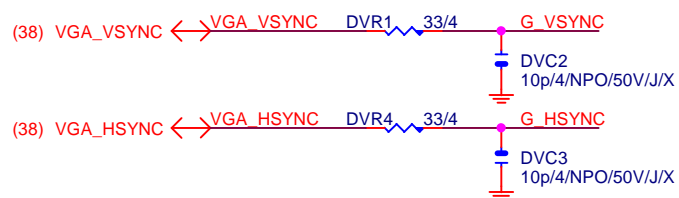
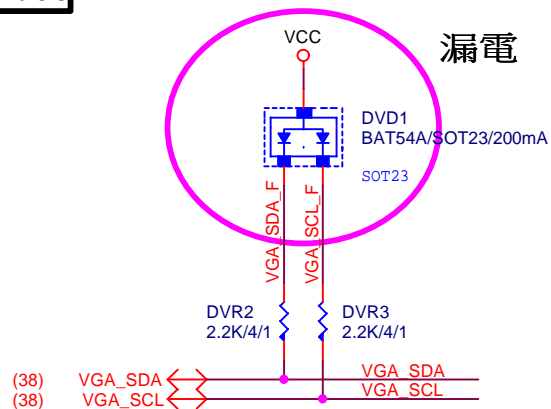


放置PCH端

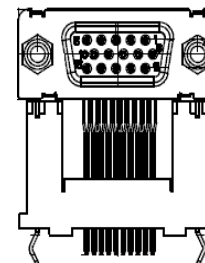
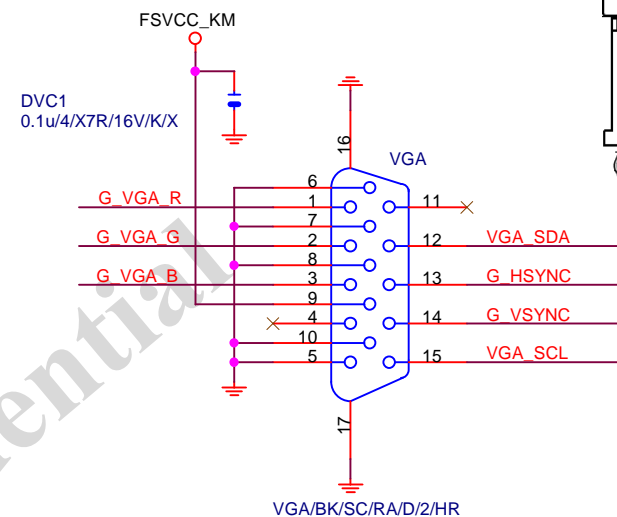
Gigabyte Technology
NXP-PTN3356

Title	Gigabyte Technology NXP-PTN3356		
Size Custom	Document Number	GA-Z170X-UD3	Rev 1.0
Date:	Monday, July 06, 2015	Sheet 38 of 60	1

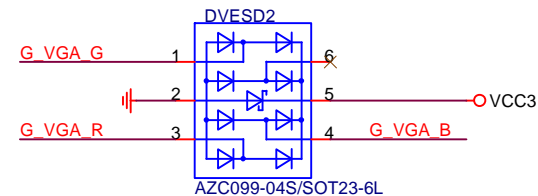
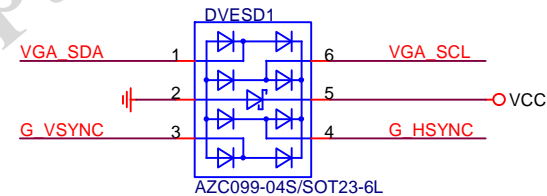
VGA SIGNAL	R1.08
------------	-------



VGA CONN. 架高型VGA (BLACK)



VGA ESD



HDMI LEVEL SHIFT

NET 可變



Port 自行調整



HDMI:20/4/6/4/20
Impedance=85 ± 17.5%

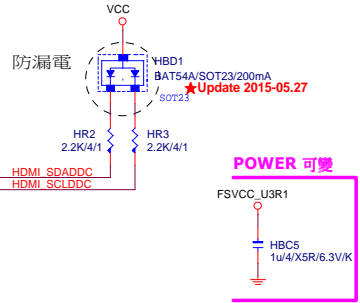
Port 自行調整



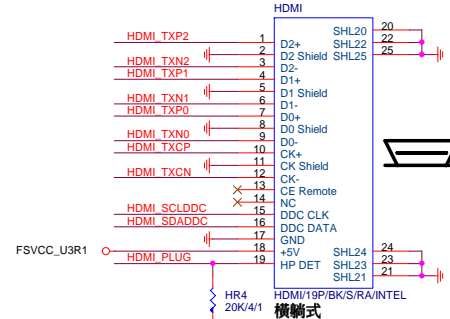
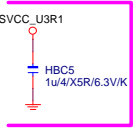
【技術通報R&D技術通報150】

HDMI eye diagram 1.4版(deep color)會fail
原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
ASM1442:紅色框要上,HR12:3.16K



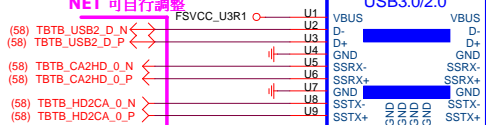
POWER 可變



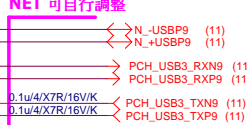
Rev: 0.7

R_USB30_1

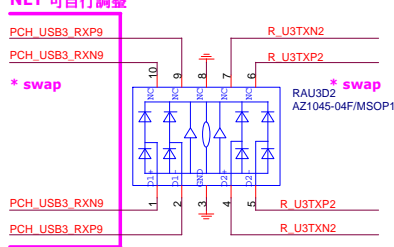
NET 可自行調整



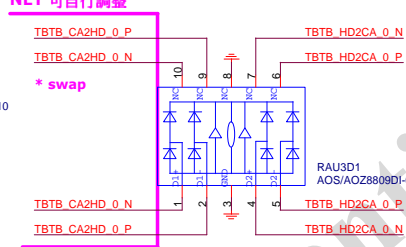
NET 可自行調整



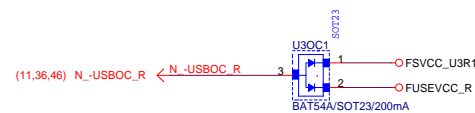
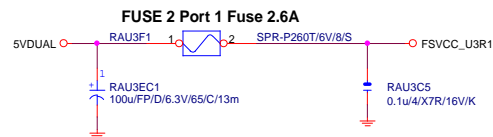
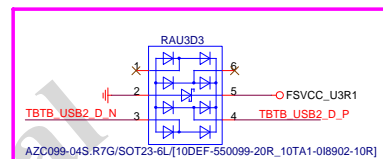
NET 可自行調整



NET 可自行調整



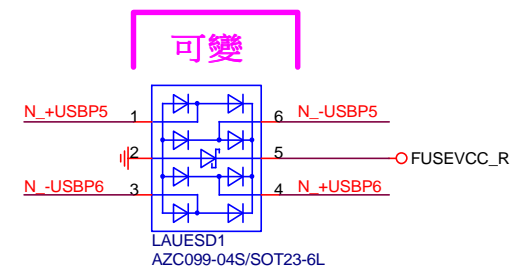
NET 可自行調整



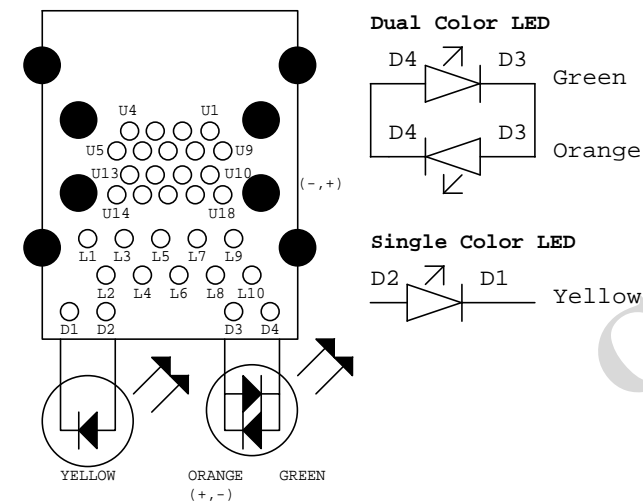
Gigabyte Technology			
Title			
R_USB30,F_USB30, USB OC			
Size	Document Number	GA-Z170X-UD3	
Custom		Rev 1.0	
Date:	Monday, July 06, 2015	Sheet	41 of 60

USB_LAN CONNECTOR R1.09

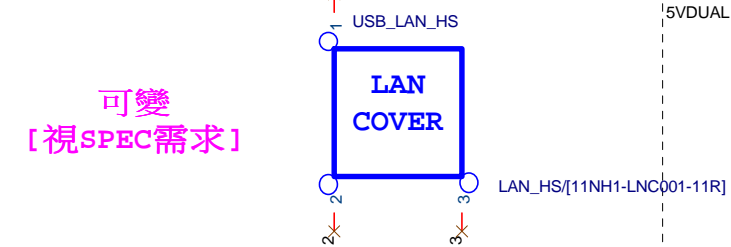
RMA ESD PROTECT note:可變更USB NAME



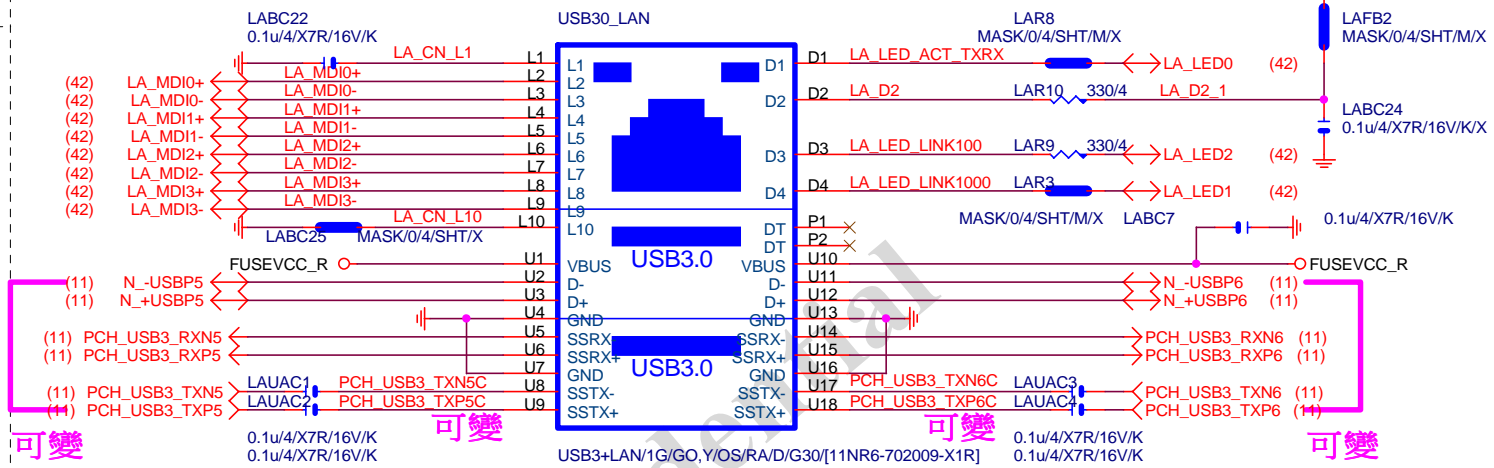
USB30 LAN LAYOUT示意圖



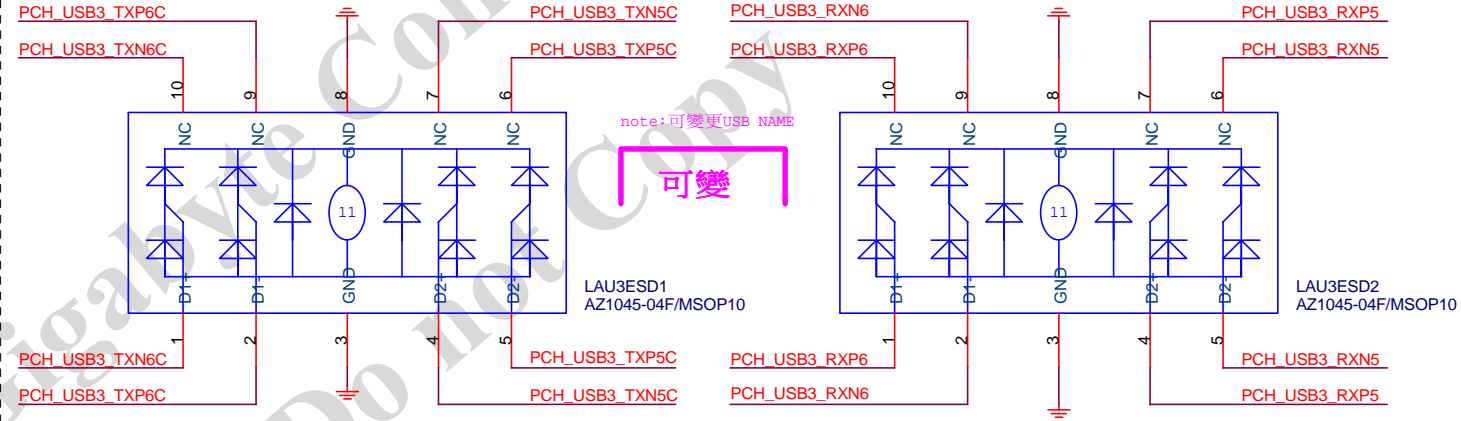
LAN COVER FOOT PRINT:LAN COVER



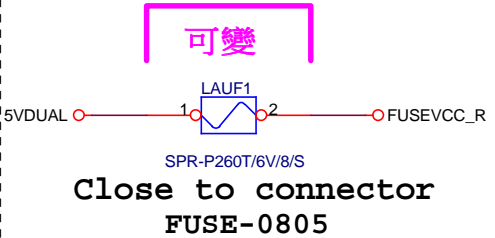
USB_LAN CONNECTOR [I219] note:可變更USB NAME



LA MDI--->100歐姆:[20/4/8/4/20]



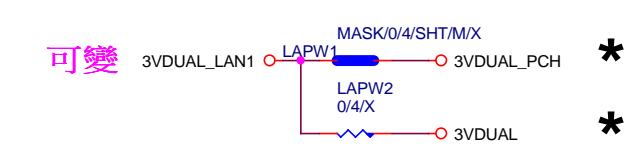
USB POWER note:可變更FUSE



EMI SHORT PAD PS:視EMI需求



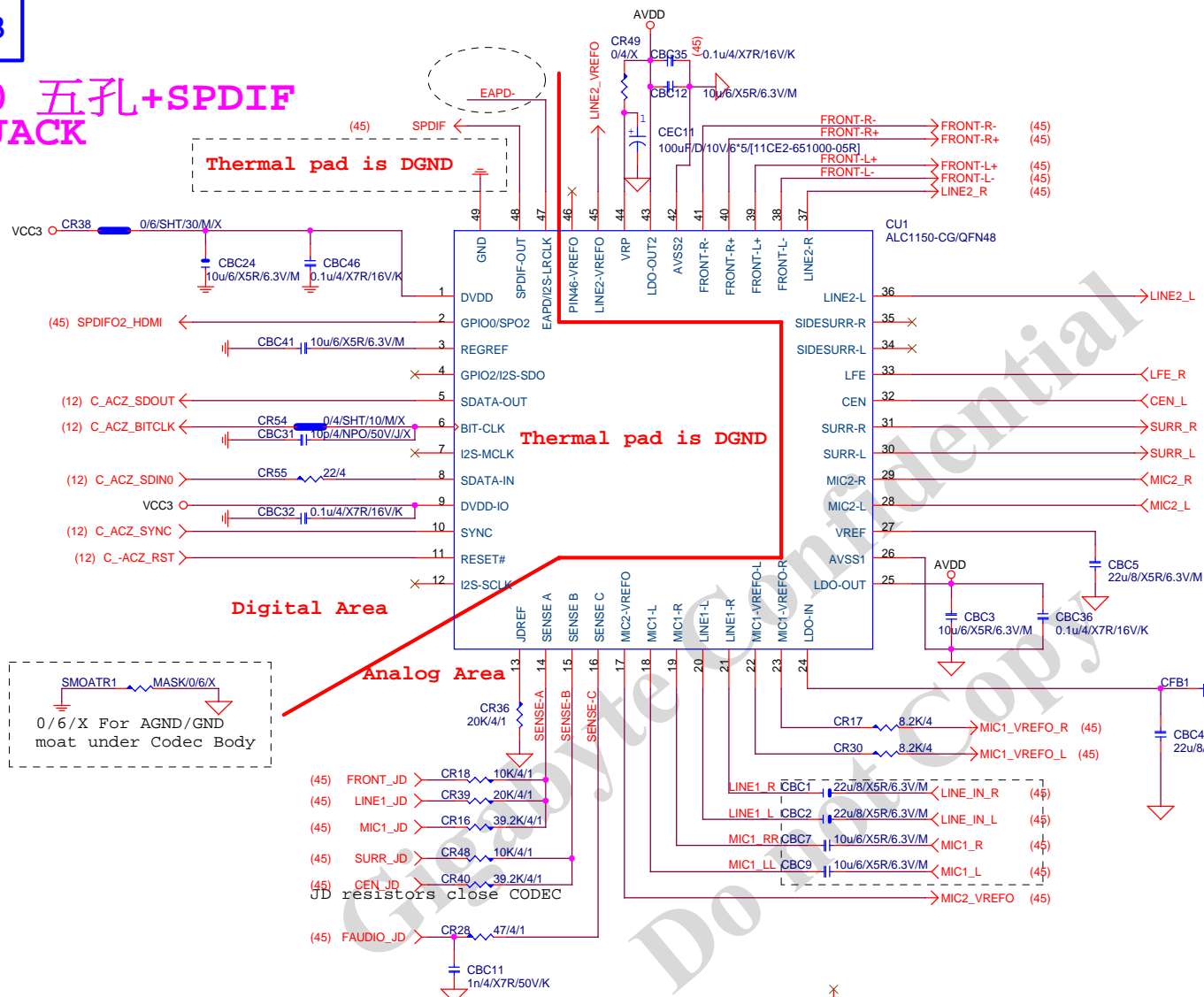
LAN POWER note: lan power連接及電流



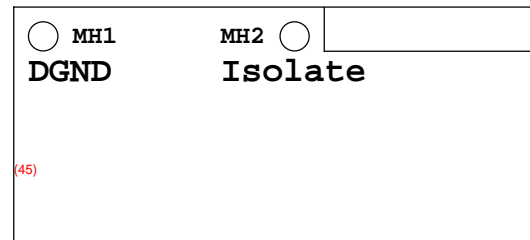
Gigabyte Technology			
LAN CONNECTOR-I219			
Title	Document Number	Rev	1.0
Size	Custom	GA-Z170X-UD3	
Date:	Monday, July 06, 2015	Sheet	43 of 60

Rev 0.93

ALC1150 五孔+SPDIF AUDIO JACK



LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
空間不夠,改為Isolate
2. MH2一律改為Isolate

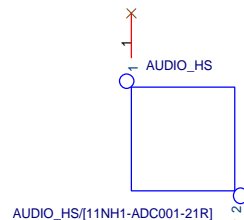
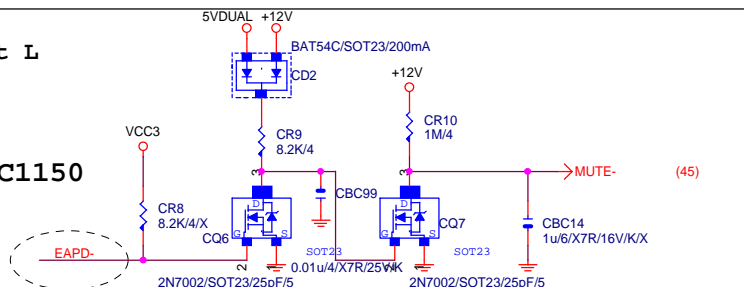


LAYOUT注意:要加
GND切割線



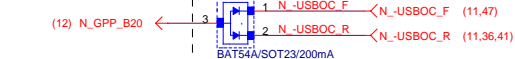
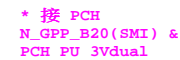
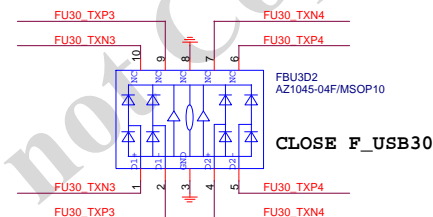
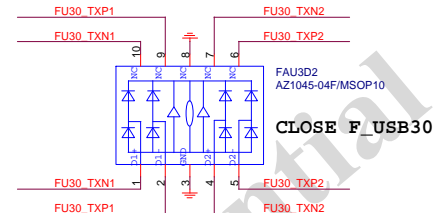
EAPD: Default L
H : ON
L : OFF

Close to ALC1150



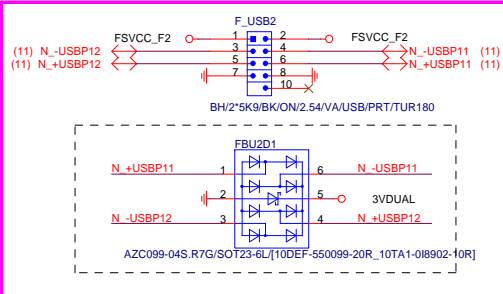
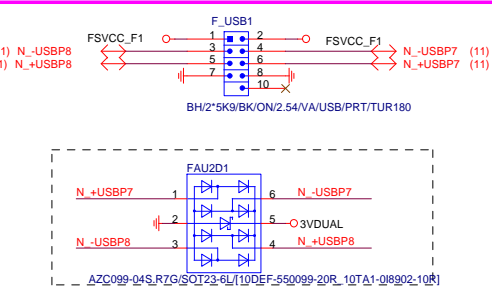
Gigabyte Technology

Title			ALC1150
Size			Document Number
Custom			GA-Z170X-UD3
Date			Monday, July 06, 2015
Sheet			44 of 60
Rev			1.0



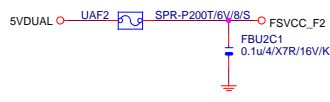
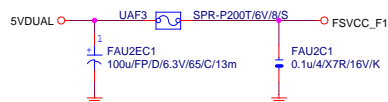
NET 可變

NET 可變

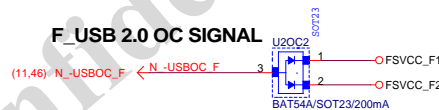


Close to connector
FUSE 2 Port 1 Fuse 2A

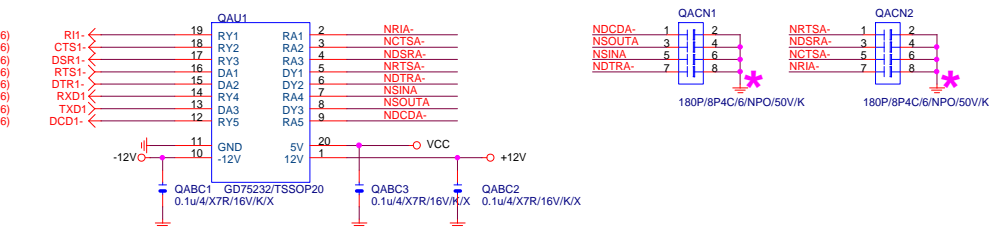
Close to connector
FUSE 2 Port 1 Fuse 2A



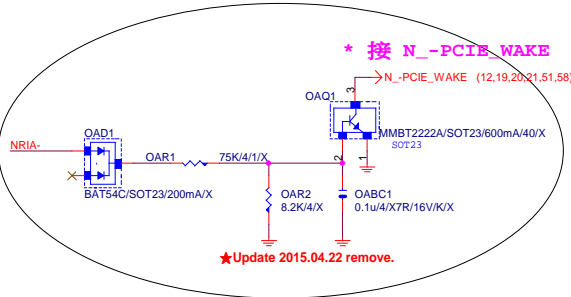
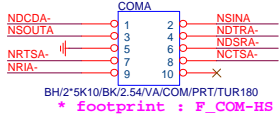
F_USB 2.0 OC SIGNAL



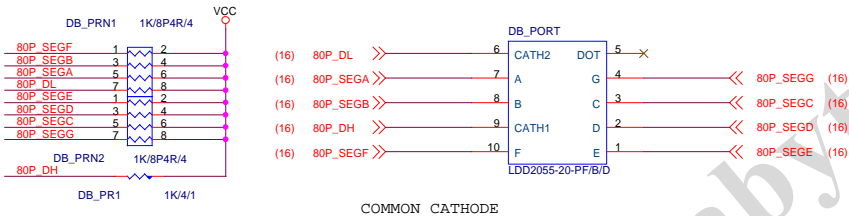
COM PORT



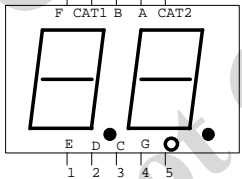
COMA



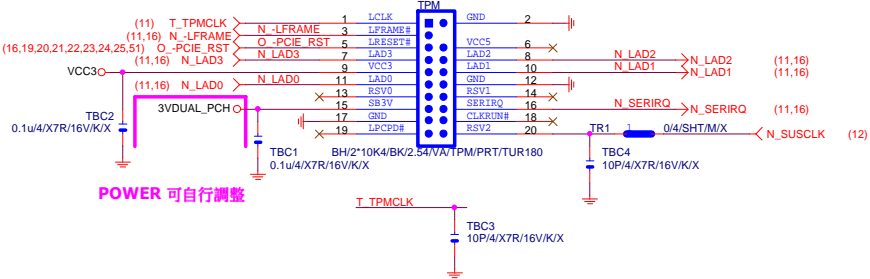
80 PORT



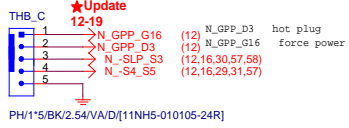
Physical Package (TOP VIEW)



TPM CONNECT

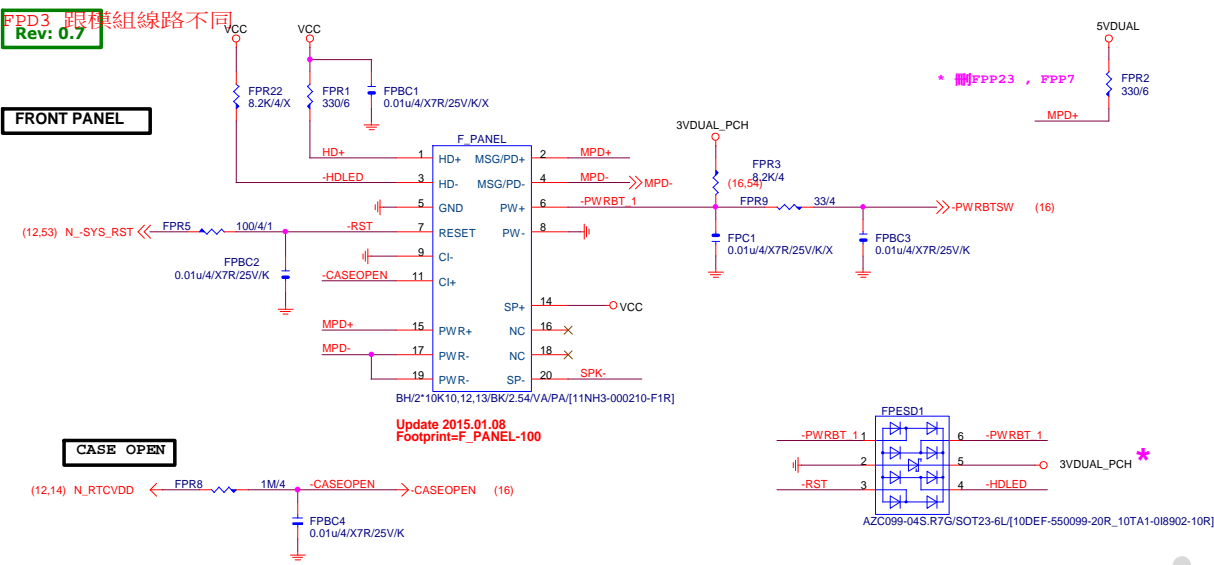


Thunderbolt

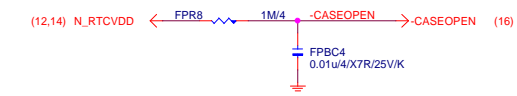


FDP3 跟模組線路不同
Rev: 0.7

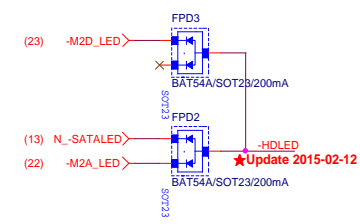
FRONT PANEL



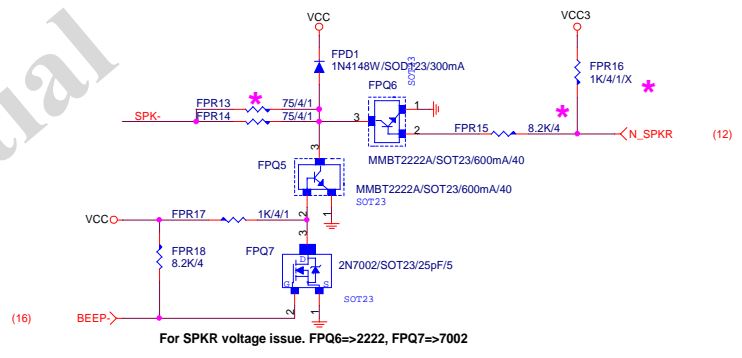
CASE OPEN



SATA LED



SPKR



Gigabyte Confidential
Do not Copy

1

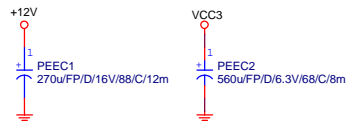
3



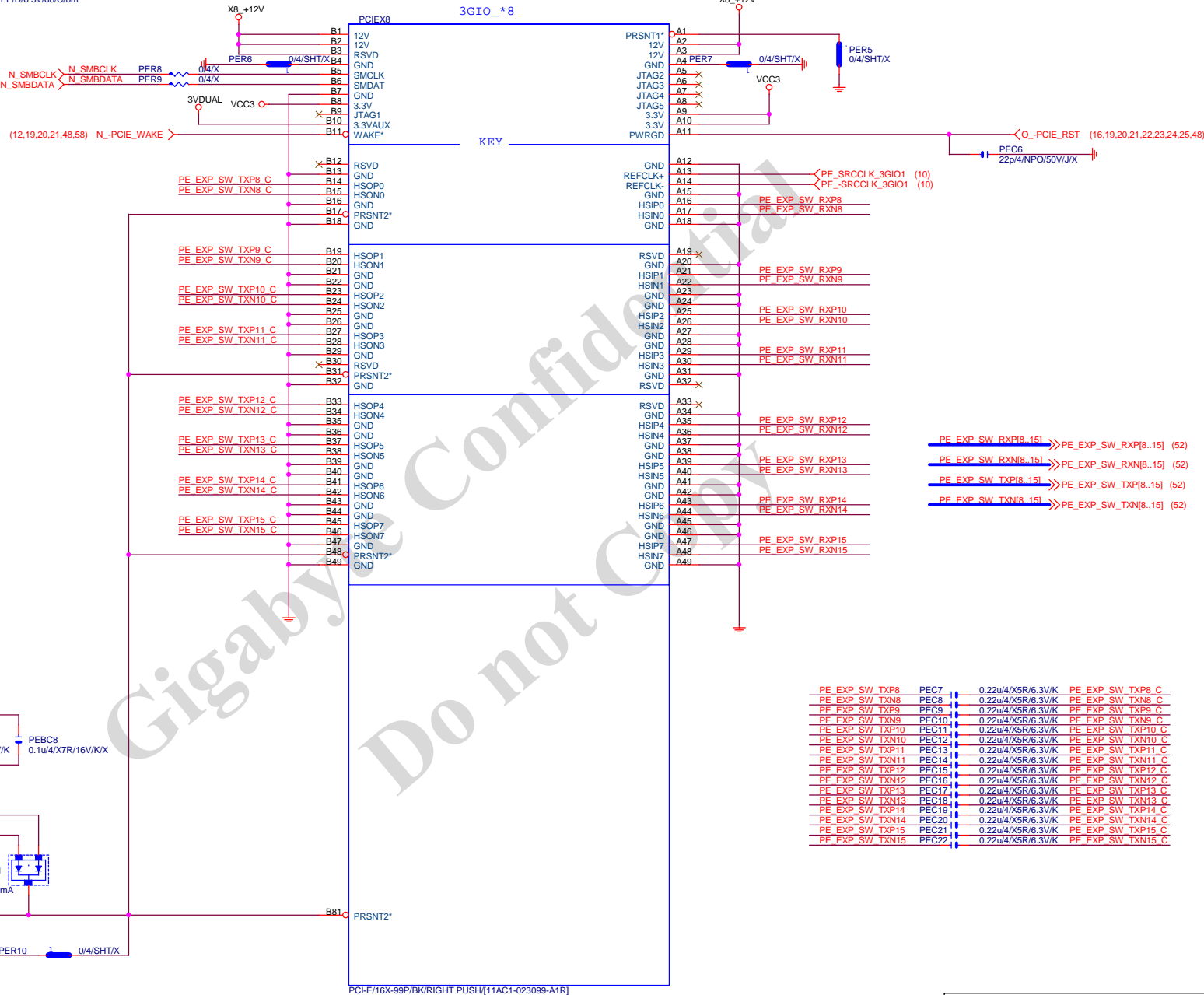
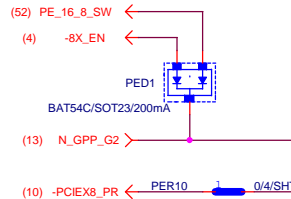
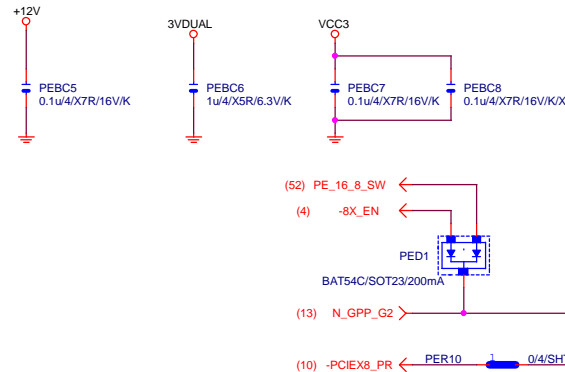
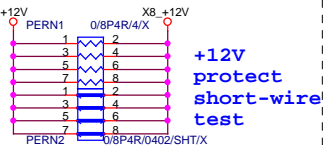
100

Rev	
1.0	

Rev 0.3



PCIEX8 PROTECT SHT



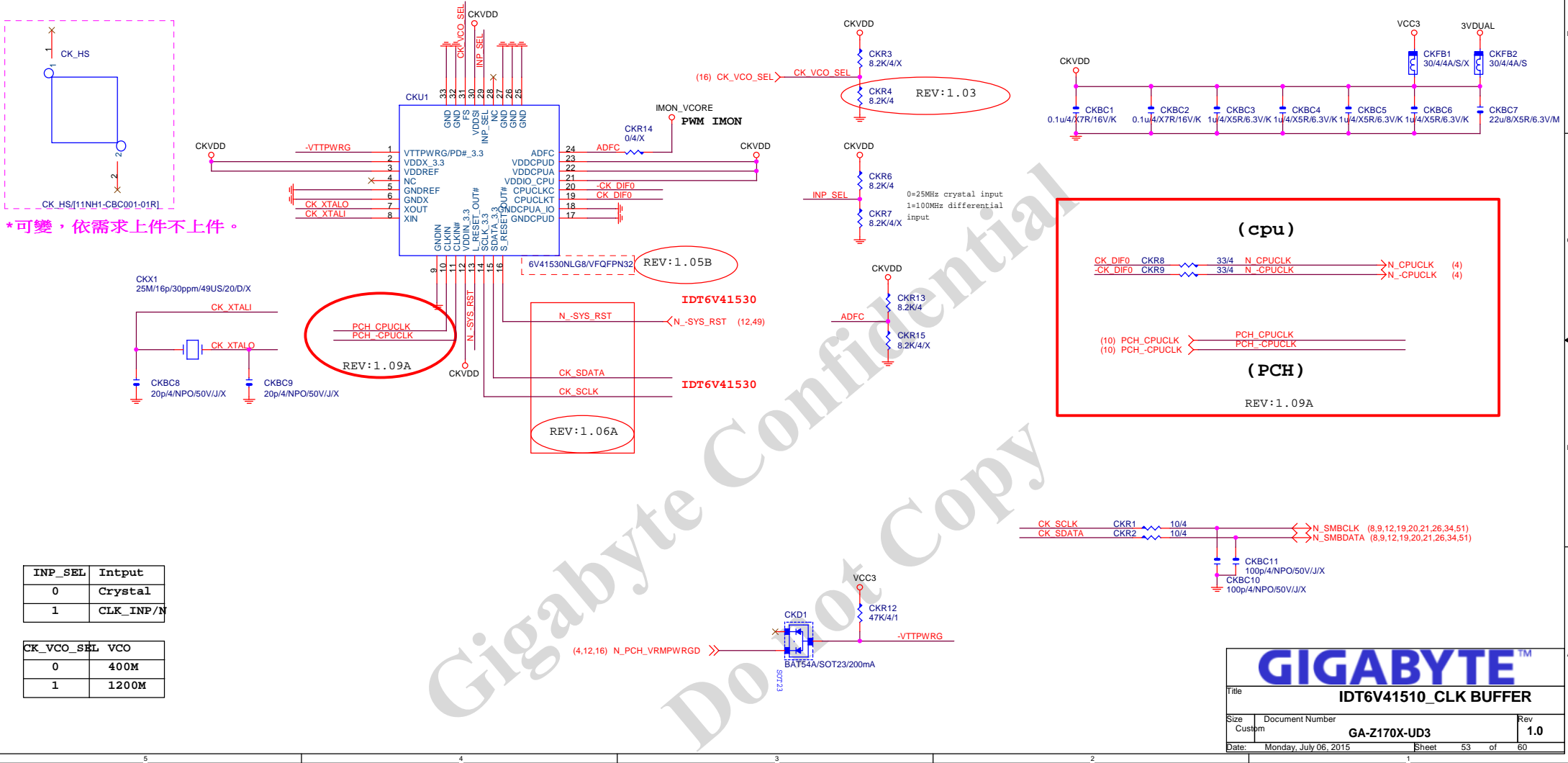
PE EXP SW TXP8	PEC7	0.22u4/X5R/6.3V/K	PE EXP SW TXP8_C
PE EXP SW TXN8	PEC8	0.22u4/X5R/6.3V/K	PE EXP SW TXN8_C
PE EXP SW TXP9	PEC9	0.22u4/X5R/6.3V/K	PE EXP SW TXP9_C
PE EXP SW TXN9	PEC10	0.22u4/X5R/6.3V/K	PE EXP SW TXN9_C
PE EXP SW TXP10	PEC11	0.22u4/X5R/6.3V/K	PE EXP SW TXP10_C
PE EXP SW TXN10	PEC12	0.22u4/X5R/6.3V/K	PE EXP SW TXN10_C
PE EXP SW TXP11	PEC13	0.22u4/X5R/6.3V/K	PE EXP SW TXP11_C
PE EXP SW TXN11	PEC14	0.22u4/X5R/6.3V/K	PE EXP SW TXN11_C
PE EXP SW TXP12	PEC15	0.22u4/X5R/6.3V/K	PE EXP SW TXP12_C
PE EXP SW TXN12	PEC16	0.22u4/X5R/6.3V/K	PE EXP SW TXN12_C
PE EXP SW TXP13	PEC17	0.22u4/X5R/6.3V/K	PE EXP SW TXP13_C
PE EXP SW TXN13	PEC18	0.22u4/X5R/6.3V/K	PE EXP SW TXN13_C
PE EXP SW TXP14	PEC19	0.22u4/X5R/6.3V/K	PE EXP SW TXP14_C
PE EXP SW TXN14	PEC20	0.22u4/X5R/6.3V/K	PE EXP SW TXN14_C
PE EXP SW TXP15	PEC21	0.22u4/X5R/6.3V/K	PE EXP SW TXP15_C
PE EXP SW TXN15	PEC22	0.22u4/X5R/6.3V/K	PE EXP SW TXN15_C

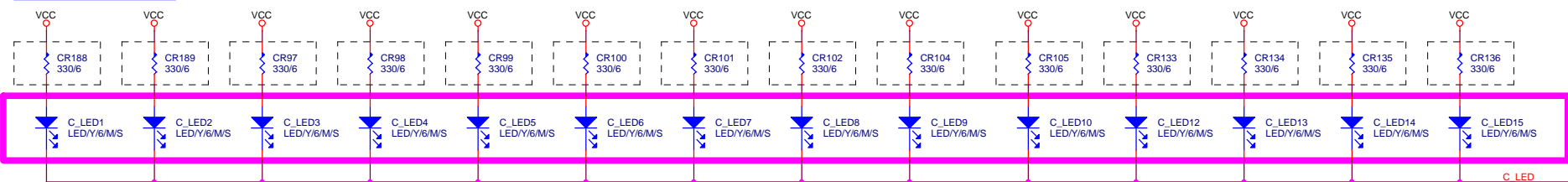
Gigabyte Technology

Title			
PCI EXPRESS X8			
Size			
Custom			
Document Number			
GA-Z170X-UD3			
Date			
Monday, July 06, 2015			
Sheet			
51			
of			
60			
Rev			
1.0			

REV:1.10A

IDT6V41530



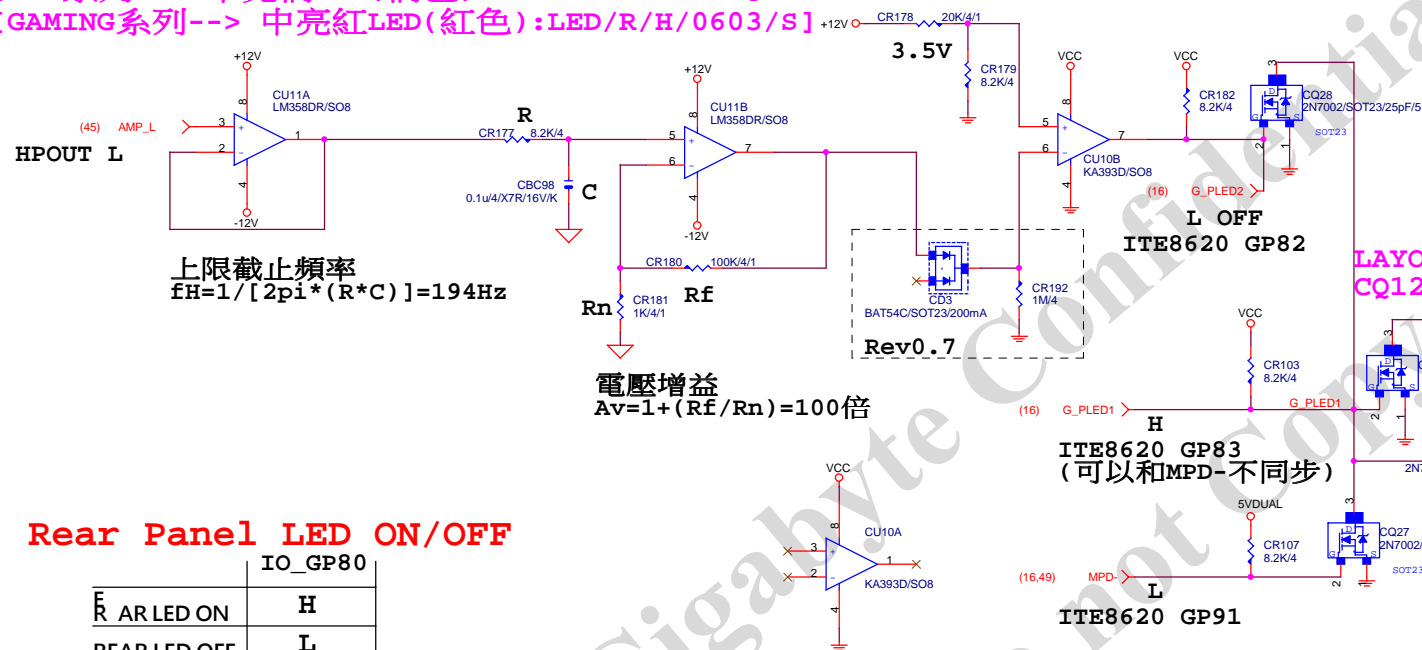


VALUE可變,LED顏色請自行修改

[UD系列--> 中亮黃LED(黃色):LED/Y/6/M/S]

[SOC系列--> 中亮橘LED(橘色):LED/O/M/0603/S]

[GAMING系列--> 中亮紅LED(紅色):LED/R/H/0603/S]



上限截止頻率
 $f_H = 1 / [2\pi * (R * C)] = 194\text{Hz}$

電壓增益
 $A_v = 1 + (R_f / R_n) = 100\text{倍}$

Rear Panel LED ON/OFF

	IO_GP80
REAR LED ON	H
REAR LED OFF	L

CLOSE TO AUDIO JACK

LAYOUT OPTION : SOC/UD7系列要LAYOUT,
其餘UD系列機種不留LAYOUT

AUDIO LED Control (沒有LPT model)

	IO_GP82	IO_GP83	IO_GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

AUDIO LED Control (有LPT model)

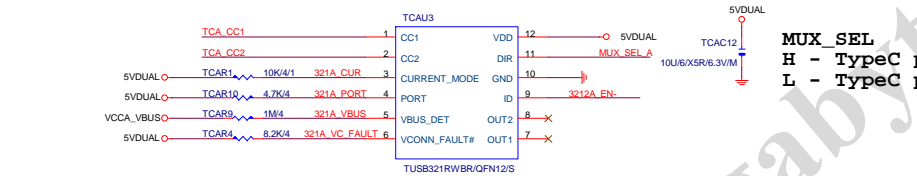
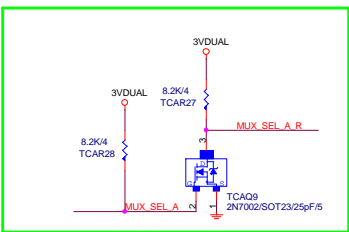
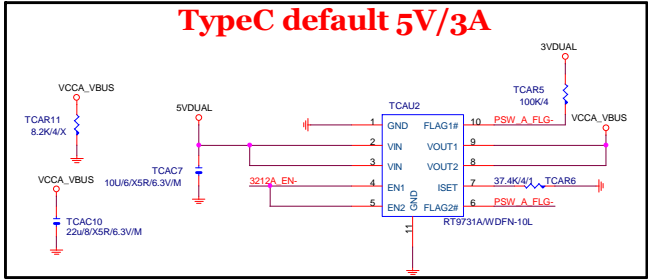
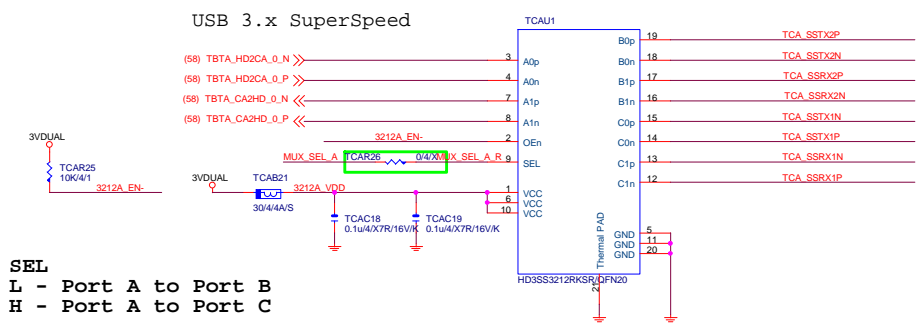
	IO_GP92	IO_GP17	IO_GP91
Still Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

LAYOUT注意:
CQ12, CQ18, CQ19必須擺放在一起

GIGABYTE™

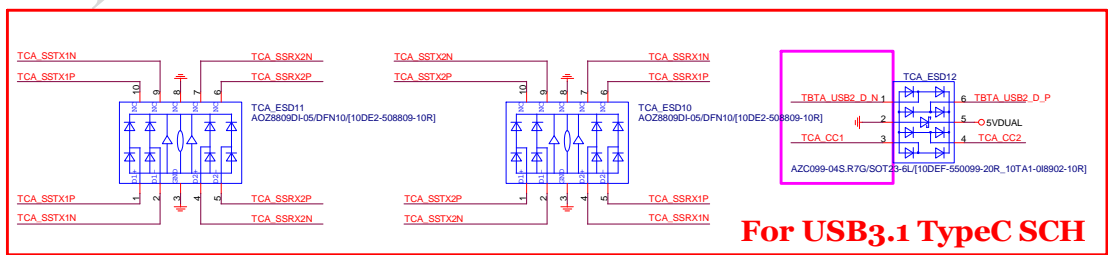
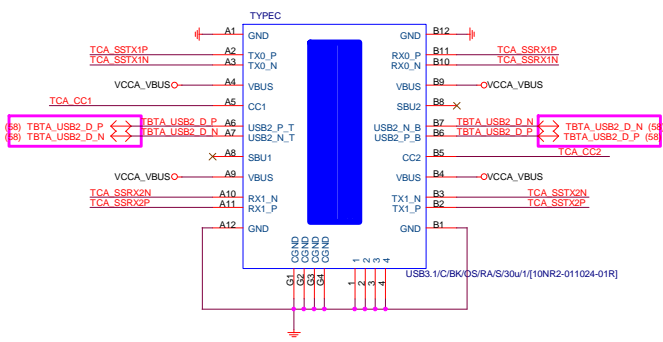
Title	AUDIO LED	
Size	Document Number	Rev
Custom	GA-Z170X-UD3	1.0
Date:	Monday, July 06, 2015	Sheet 54 of 60

INTEL AR USB31 module SCH o.61 (2015/06/15)



CURRENT MODE
L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

PORT
H - HOST
L - Device
NC - Dual Role

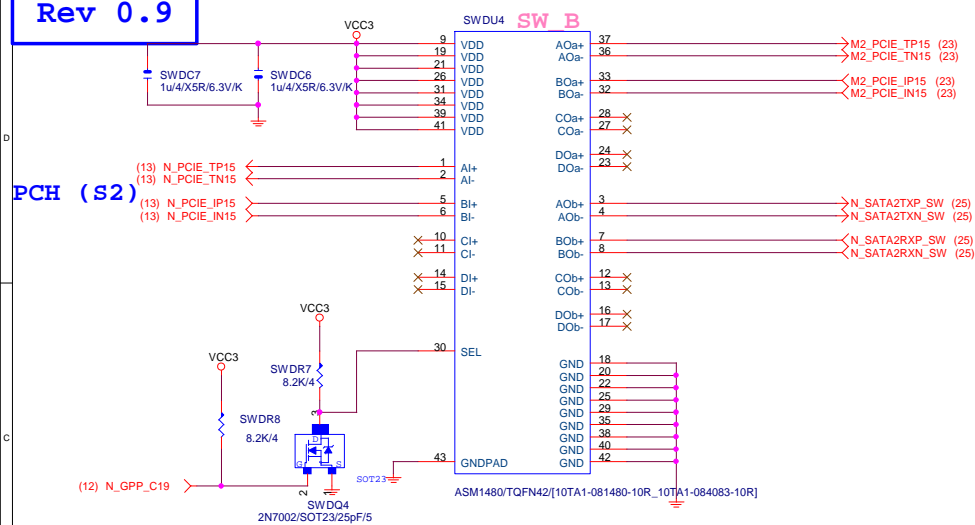


For USB3.1 TypeC SCH

USB2.o can be used the same source

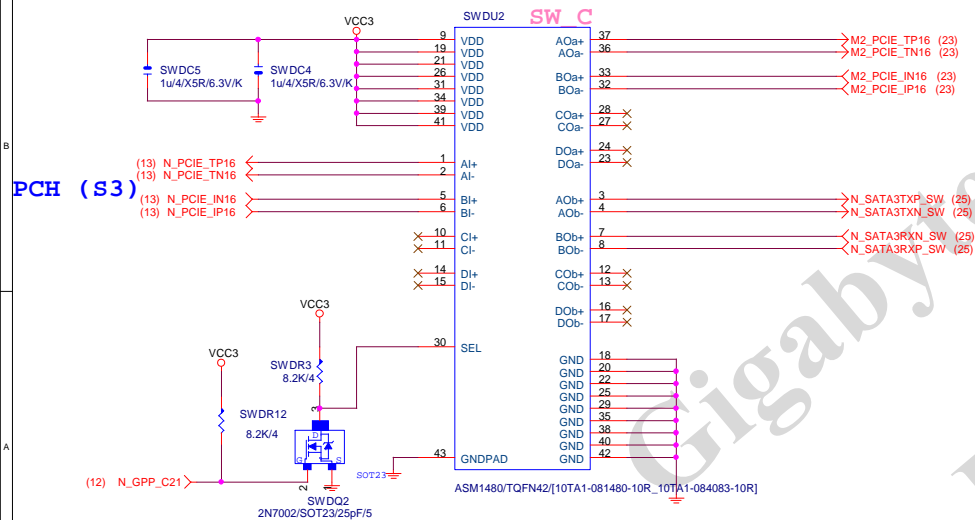
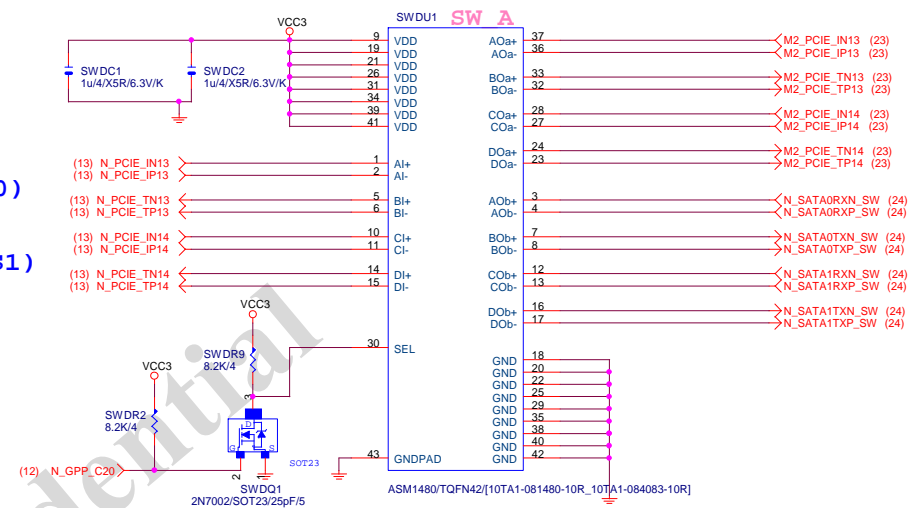
Color markers can be changed by model

GIGABYTE™		
Title		
TI TUSB321		
Size		
Document Number		
GA-Z170X-UD3		
Rev		
1.0		
Date		
Monday, July 06, 2015		
Sheet		
55 of 60		



PCH (S0)

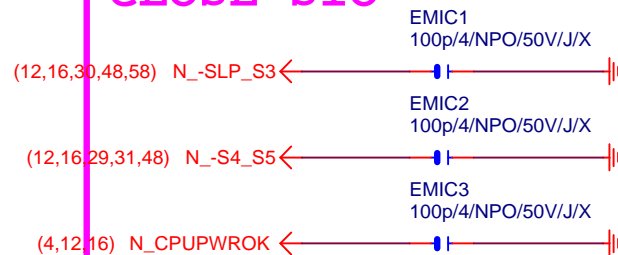
PCH (S1)

**Gigabyte Technology**
SWITCH

Title		Document Number		Rev
Size		Custom		1.0
Date		Monday, July 06, 2015		Sheet 56 of 60

EMIC5, EMIC6, EMIC7 跟模組線路不同

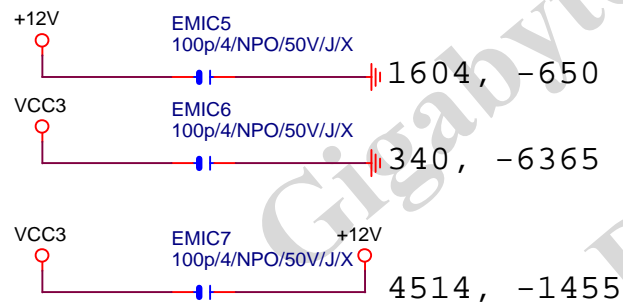
CLOSE SIO



CLOSE PCH



CLOSE AUDIO



GIGABYTE™

Title

EMI/ESD

Size
A

Document Number

GA-Z170X-UD3

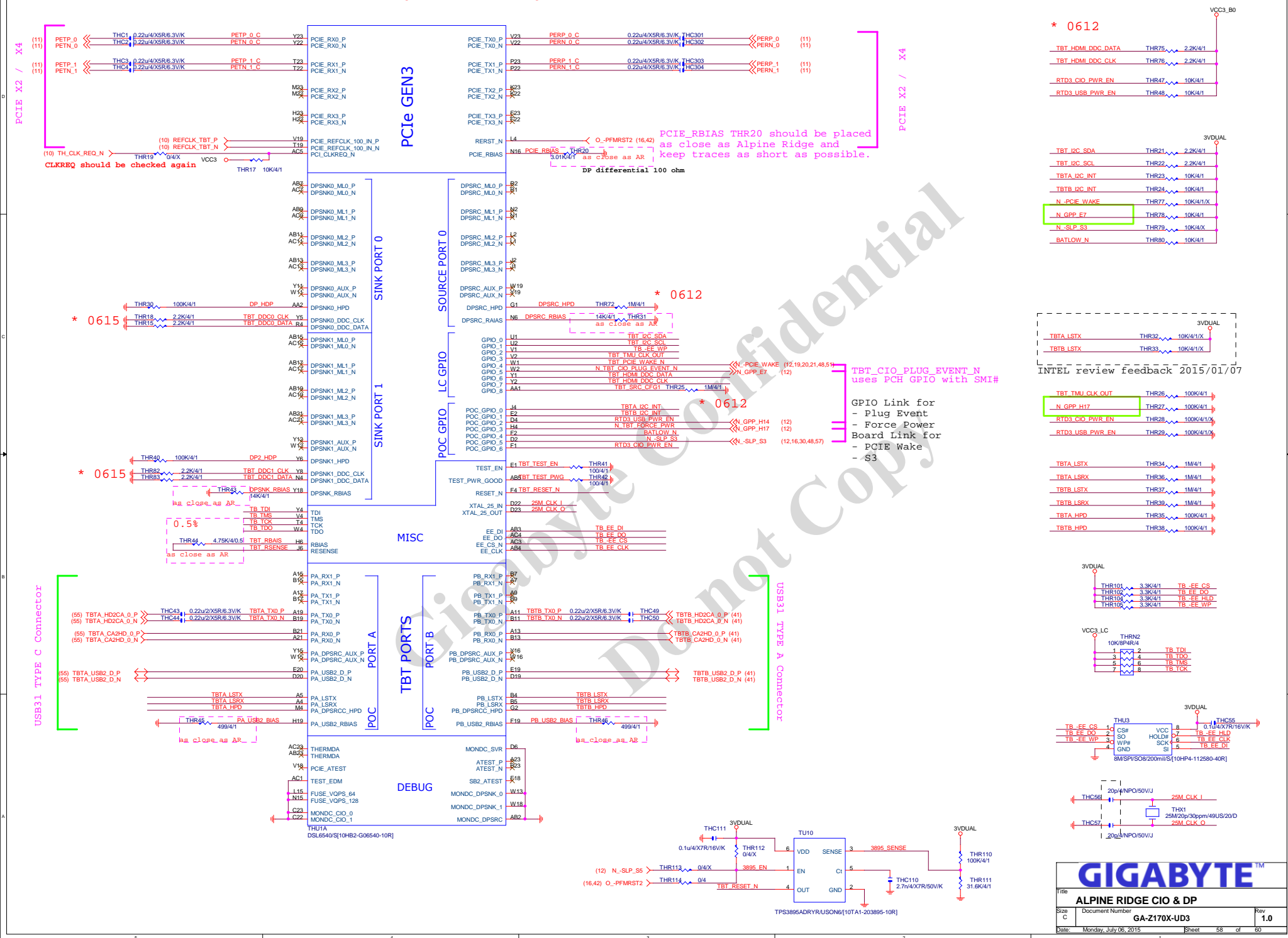
Rev

1.0

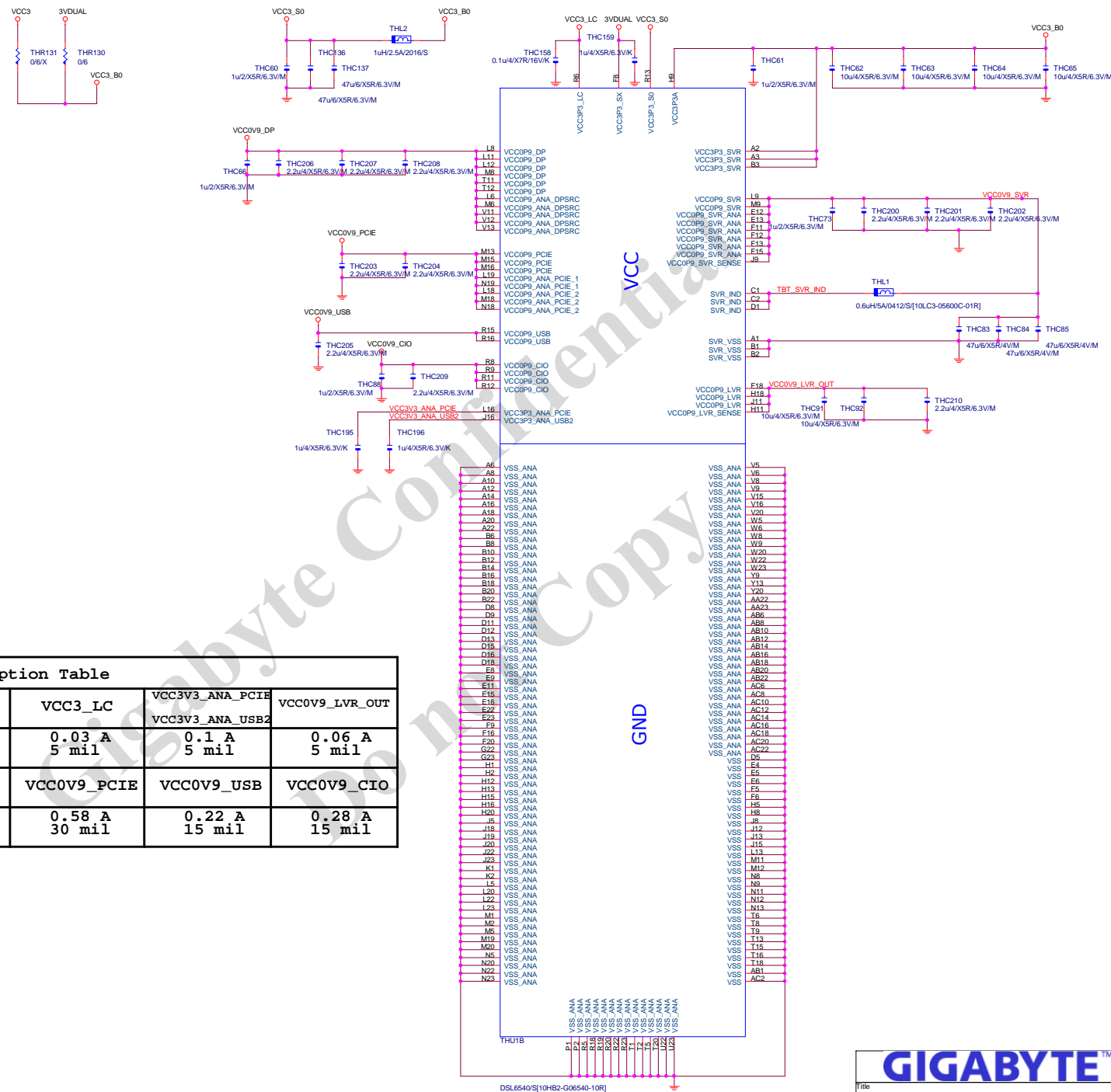
Date: Monday, July 06, 2015

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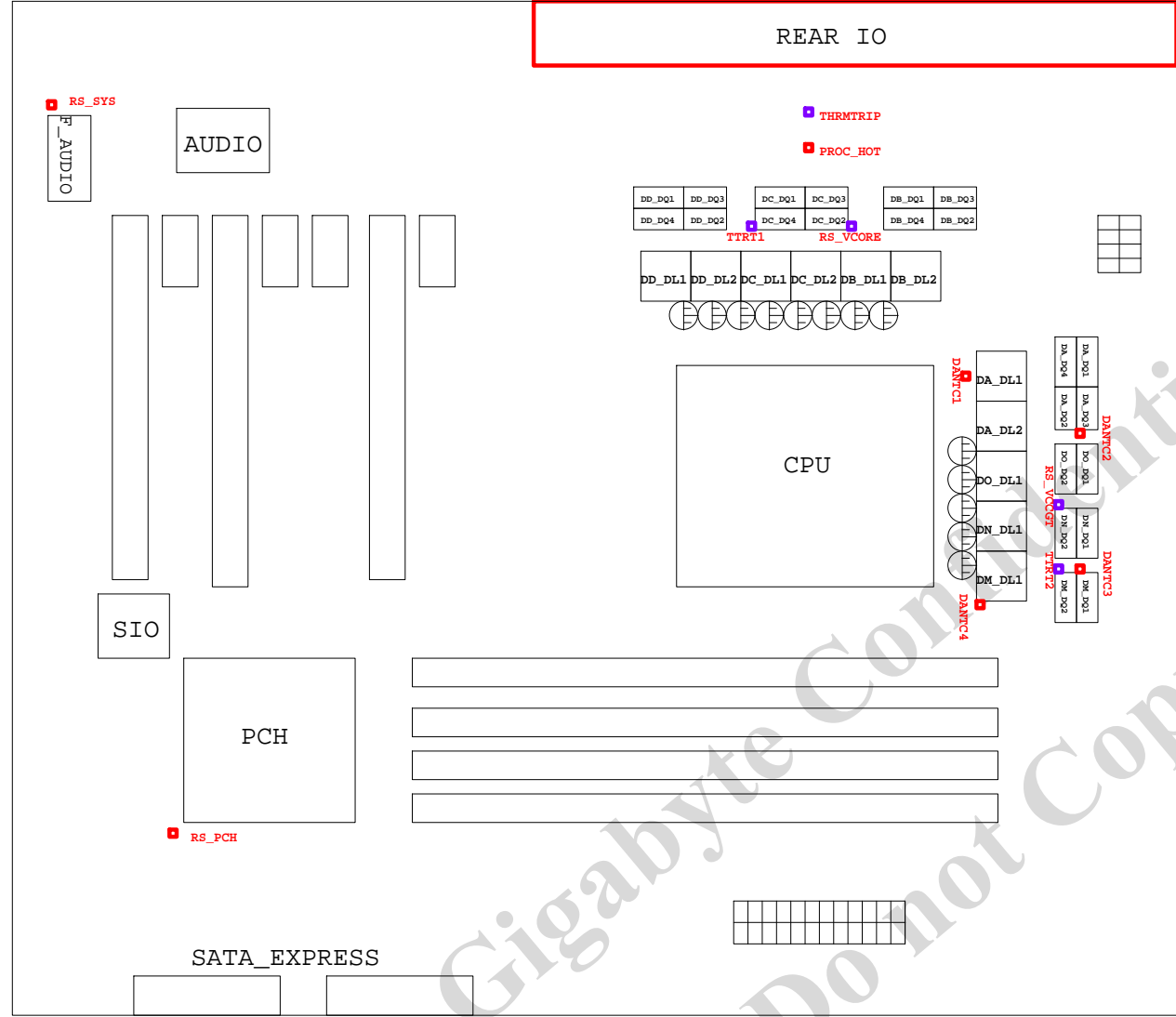
INTEL AR USB31 module SCH 0.61 (2015/06/15)



INTEL AR USB31 module SCH 0.61 (2015/06/15)



Power Consumption Table					
	VCC3	3VDUAL	VCC3_LC	VCC3V3_ANA_PCIE VCC3V3_ANA_USB2	VCC0V9_LVR_OUT
Max Current(A)	1.05 A 40 mil	0.19 A 10 mil	0.03 A 5 mil	0.1 A 5 mil	0.06 A 5 mil
	VCC0V9_SVR	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
Max Current(A)	1.83 A 80 mil	0.7 A 30 mil	0.58 A 30 mil	0.22 A 15 mil	0.28 A 15 mil



熱敏電阻	擺放靠近位置	走線方式
DANTC1	DA_DL2	Differential
DANTC2	DA_DQ3	Differential
DANTC3	DM_DQ2	Differential
DANTC4	DM_DL1	Differential
RS_VCORE	DC_DQ4	N/A
RS_VCCGT	DM_DQ2	N/A
TTRT1	DC_DQ2	N/A
TTRT2	DN_DQ2	N/A
RS_PCH	PCH	N/A
RS_SYS	F_AUDIO	N/A