1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & CSCILLATOR VALUES ARE IN HERTZ.

J78 MLB CTX

LAST_MODIFIED=Wed Feb 26 11:26:42 2014

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0002620513	ENGINEERING RELEASED	2014-02-24

DRAWING

TITLE=J17
ARRREV=DRAWING
LAST_MODIFIED=Mon Feb 24 09:56:42 2014

DRAWING TITLE: SCHEM,MLB CTO,J78

Apple Inc.

DRAWING NUMBER: 051-XXXX SIZE: D

REVISION: 5.0.0

BRANCH: proto2

PAGE: 1 OF 137

SHEET: 1 OF 115

BCM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-1468	PCBA,MLB CTO,DEV,J78	DEVELOPMENT,J78_DEVEL
639-6799	PCBA,MLB CTO 3.5G,AMETHYST,VRAM_HYNIX,4GB,J78	J78,J78_COMMON,CPU:CTO,SSD:Y,GPU:AMETHYST,FB:4G_HYNIX,EEEE:FW6K
639-6160	PCBA,MLB CTO 3.5G,AMETHYST,VRAM_ELPIDA,4GB,J78	J78,J78_COMMON,CPU:CTO,SSD:Y,GPU:AMETHYST,FB:4G_ELPIDA,EEEE:FT04
639-6860	PCBA,MLB CTO 3.6G,AMETHYST,VRAM_HYNIX,4GB,J78	J78,J78_COMMON,CPU:CTO3.6,SSD:Y,GPU:AMETHYST,FB:4G_HYNIX,EEEE:FY53
639-6859	PCBA,MLB CTO 3.6G,AMETHYST,VRAM_ELPIDA,4GB,J78	J78,J78_COMMON,CPU:CTO3.6,SSD:Y,GPU:AMETHYST,FB:4G_ELPIDA,EEEE:FY54

BOM Groups

BOM GROUP	BOM OPTIONS
J78_COMMON	COMMON,ALTERNATE,J78_COMMON1,J78_PROGPARTS,3PU_AMTH
J78_COMMON1	XDP,SPEAKERID,FBVDDQ_DFLT:1V5,RTC2ST:Y
J78_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PRCG,CIVROM:PROG,CAMROM:PROG,GFUROM:PROG
J78_DEVEL	XDP_CONN,LPCPLUS,DDRVREF_DAC,DEVEL_AUDIO,AP_ISNS:Y

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4531	1	MSM,SR1ED,FBGA,C0,3.4,84W,4+2,1.2,6M,LGA	CPU	CRITICAL	CPU:ULT
337S00003	1	CPU,MSM,QF4G,3.5,Q5,C0,4+2,84W,LGA	CPU	CRITICAL	CPU:CTO
337S00005	1	CPU,MSM,QF4D,3.6,Q8,C0,4+2,84W,LGA	CPU	CRITICAL	CPU:CTO3.6

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0080	1	SOCKET,MOLEX,LGA1150,CPU-LF	U0500	CRITICAL	

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4541	1	IC,SR1N9,1ET,LPT-D,C0,FBGA708,23X23MM	U2100	CRITICAL	
337S4562	1	IC,QEWL,LPT-D,C2,BGA,FCBGA708,23X23MM	U2100	CRITICAL	PCH_TDP
338S1247	1	IC,TBT,RR-4C,A0,FBGA,C10,SR1JC,FCBGA288	U2800	CRITICAL	
343S0616	1	IC,BCM57766A1,ENET&SD,BX8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S0032	1	IC,EFI,V0159,J78	U5210	CRITICAL	BOOTROM:PROG
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S1999	1	IC,SMC-NE,EXTERNAL,V2.21A13,P1,AM,J78	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-B1,40MHZ/500MIPS,MCU,157BGA	U5000	CRITICAL	SMC:BLANK
341S0024	1	IC,T29,EPROM,FR,V23.1,J78A	U2890	CRITICAL	TBTRON:PROG
335S0915	1	IC,SPI FLASH ROM,4MBIT,50MHZ,USON8	U2890	CRITICAL	TBTRON:BLANK
341S1912	1	IC,ENET ROM,NUMONYX,V1.15,J16/J16D/J17	U3990	CRITICAL	CIVRON:PROG
335S0854	1	1-MBIT,SPI FLASH ROM SOIC, MF	U3990	CRITICAL	CIVROM:BLANK
341S3778	1	IC,CAMERA FLASH,V7230,J16/J17	U4202	CRITICAL	CAMRON:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S0009	1	IC,ROM,GFX,V1.0,J78	U9700	CRITICAL	GPURON:PROG
335S0724	1	IC,CONF ROM,NEPT VBIOS,VTBD	U9700	CRITICAL	GPUROM:BLANK

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_FRFN	CRITICAL	EEEE:FRFN
825-7896	1	LABEL,MLB,2D	EEEE_FRFL	CRITICAL	EEEE:FRFL
825-7896	1	LABEL,MLB,2D	EEEE_FW6K	CRITICAL	EEEE:FW6K
825-7896	1	LABEL,MLB,2D	EEEE_FT04	CRITICAL	EEEE:FT04
825-7896	1	LABEL,MLB,2D	EEEE_FY54	CRITICAL	EEEE:FY54
825-7896	1	LABEL,MLB,2D	EEEE_FY53	CRITICAL	EEEE:FY53

J78 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-XXXX	1	SCH,MLB CTO,J78	SCH1	CRITICAL	J78
820-4652	1	PCBF,MLB CTO,J78	PCB1	CRITICAL	J78

J78 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB Diode Array
377S0155	377S0104		ALL	USB Diode
376S1218	376S1081		ALL	P/NCH DUAL FET
138S0803	138S0804		ALL	2.2UF CAPS SOFT
126-0161	126-0160		ALL	56UF CAPS 10X12 THD
197S0481	197S0480		Y1950	25MHZ PCH XTAL
197S0479	197S0478		ALL	12MHZ CAM/NXP XTAL
372S0186	372S0185		ALL	Alternate Temp Diode
107S0251	107S0249		R5520	Alt 2mOhm sense
107S0254	107S0241		R5410,R5480	Alt 5mOhm sense
107S0255	107S0240		R5030,R5410	Alt 1mOhm sense
341S3912	341S3913		U3990	IC,ENETROM,FDEITO,V1.15,J78
138S0681	138S0638		ALL	10uF Caps
376S1106	376S0969		ALL	N-Ch FET
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
128S0398	128S0220		ALL	3.3V INPUT CAP
335S0812	335S0807		U5210	64 MBIT SPI SER. FLASH 1/8 PLDM, SOIC8
378S0390	378S0140		ALL	DEGUG LED1
378S0391	378S0140		ALL	DEBUG LED1

GPU and VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4654	1	IC,GPU,AMD,AMETHST,256-BIT,45X45,BGA1120	U8700	CRITICAL	GPU:AMETHYST
333S0685	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9200,U9250,U9300 U9350	CRITICAL	FB:4G_HYNIX
333S0685	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9400,U9450,U9500 U9550	CRITICAL	FB:4G_HYNIX
333S0766	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9200,U9250,U9300 U9350	CRITICAL	FB:4G_ELPIDA
333S0766	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9400,U9450,U9500 U9550	CRITICAL	FB:4G_ELPIDA

SYNC_MASTER=J17 DINI SYNC_DATE=03/15/2013

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-XXXX SIZE D

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BRANCH proto2

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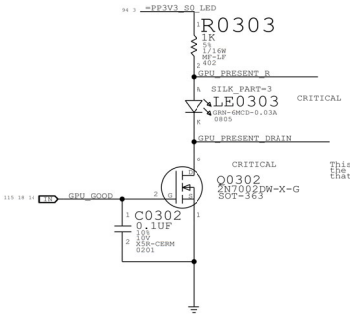
S5 Led

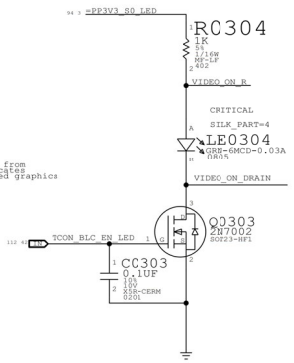
ALL_SYS_PWRGD Led

GPU GOOD Led



This LED is a GPIO driven from the southbridge that indicates that chipset has enumerated graphics

VIDEO ON Led



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-XXXX SIZE: D

REVISION: 5.0.0

BRANCH: proto2

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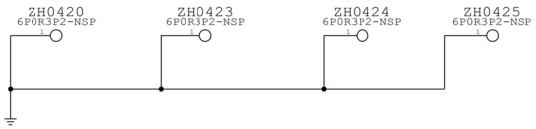
CPU Heatsink

4MM PLATED HOLES (998-4158)

GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)

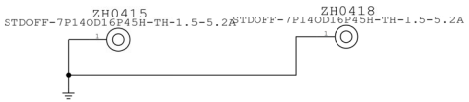


Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)

Rear Cover

860-5674 (PCB STANDOFF)

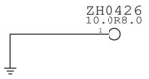


WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)

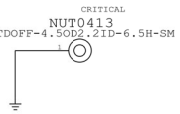
HEATPIPE MTG HOLES

998-5527 (PLATED HOLES, 8MM DIA, 10MM PAD)



SSD STANDOFF

APN: 860-1624



SYNC MASTER=J78_MLB SYNC DATE=02/21/2014

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-XXXX SIZE: D

REVISION: 5.0.0

BRANCH: proto2

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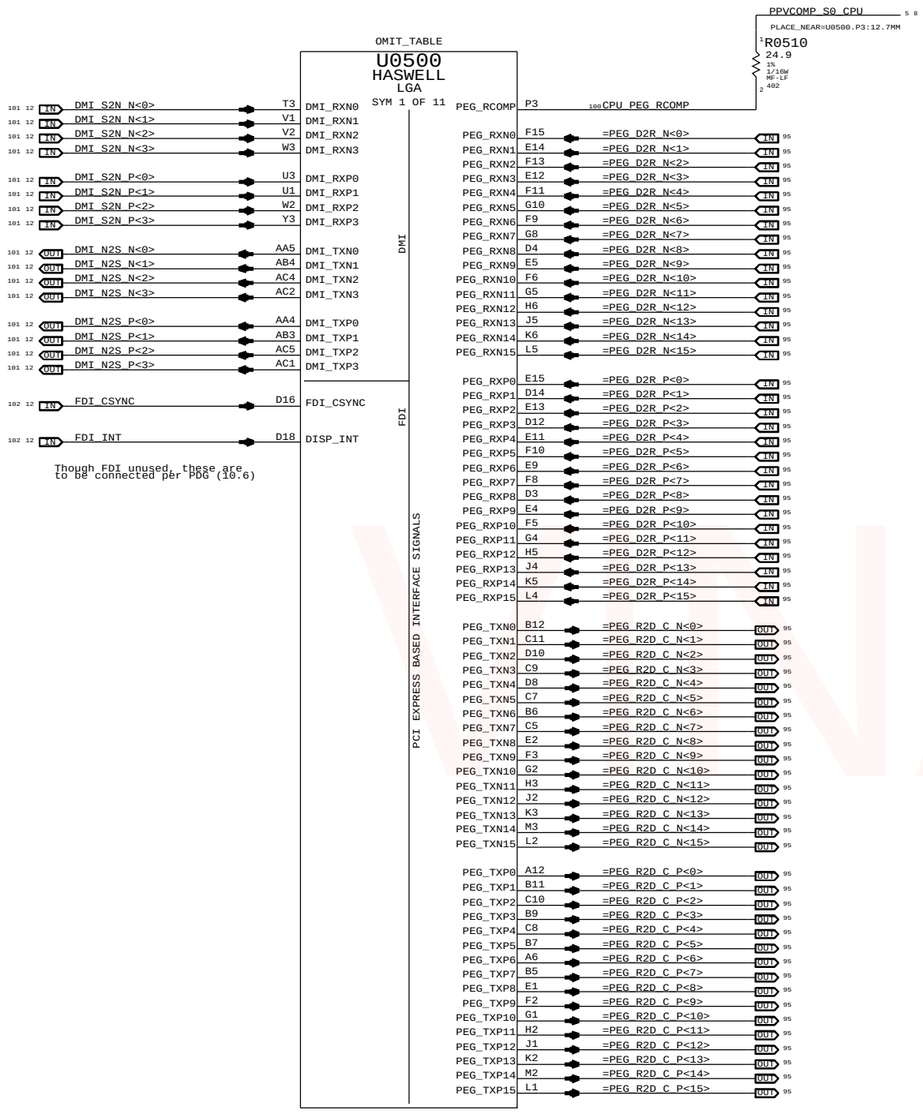

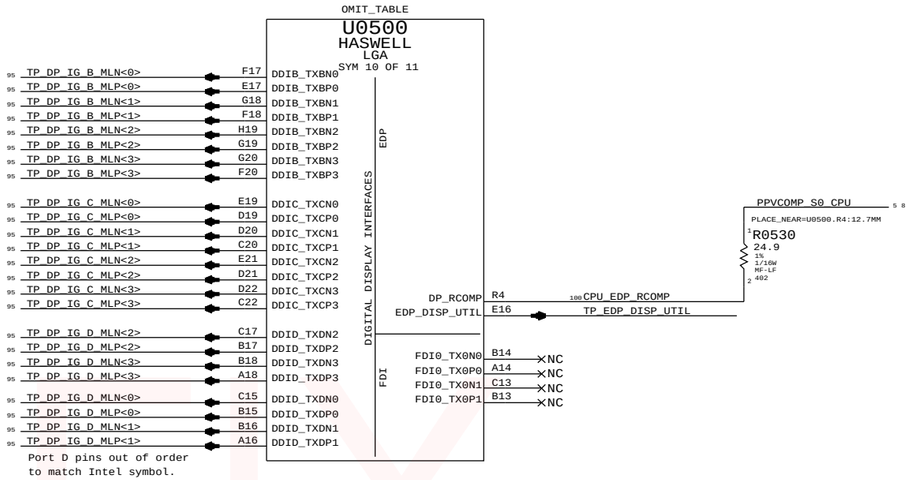

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE

CPU DMI/PEG/FDI/RSVD

Apple Inc.

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BRANCH proto2

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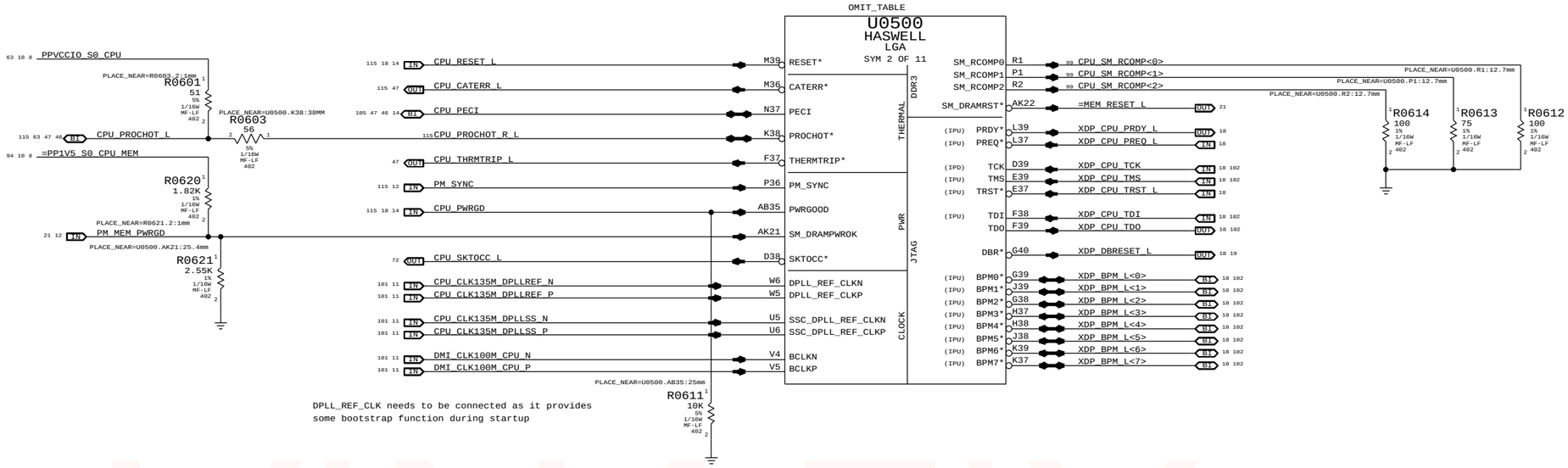

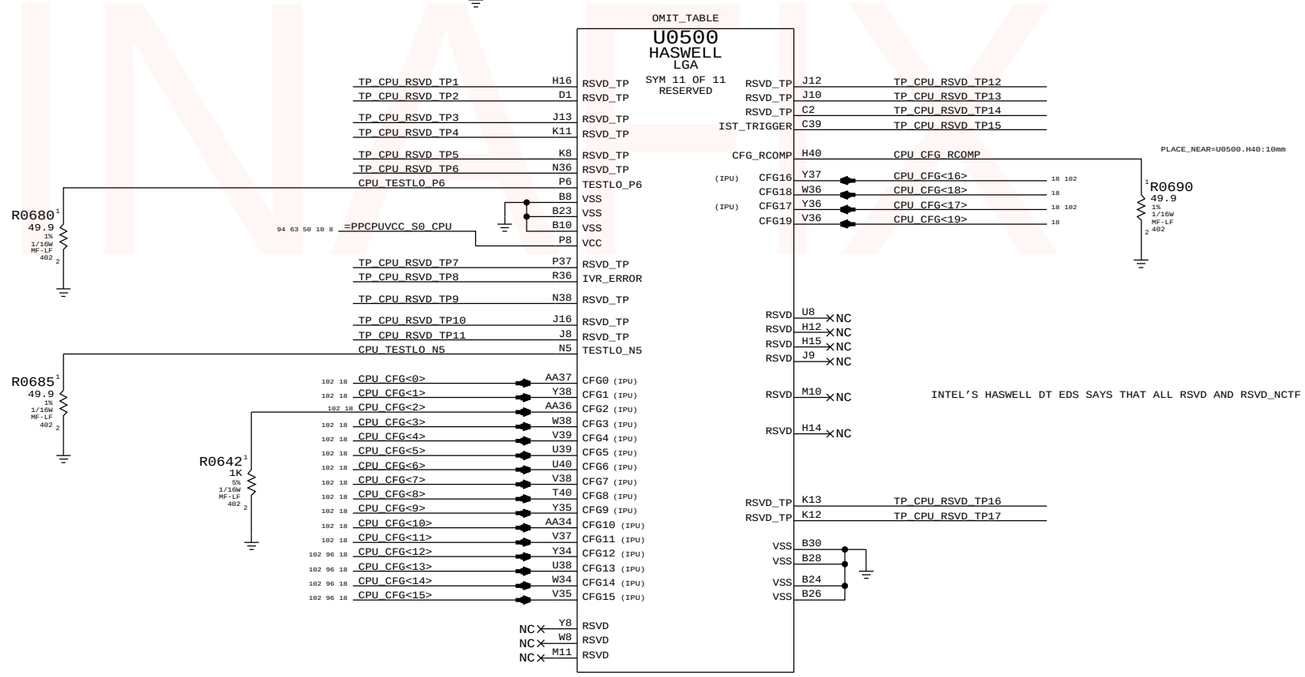

CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (default) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED(default) 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION(default) 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION(default) 0 = LANES REVERSED

SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014
PAGE TITLE: CPU Clock/Misc/JTAG/CFG
Apple Inc.
DRAWING NUMBER: 051-XXXX
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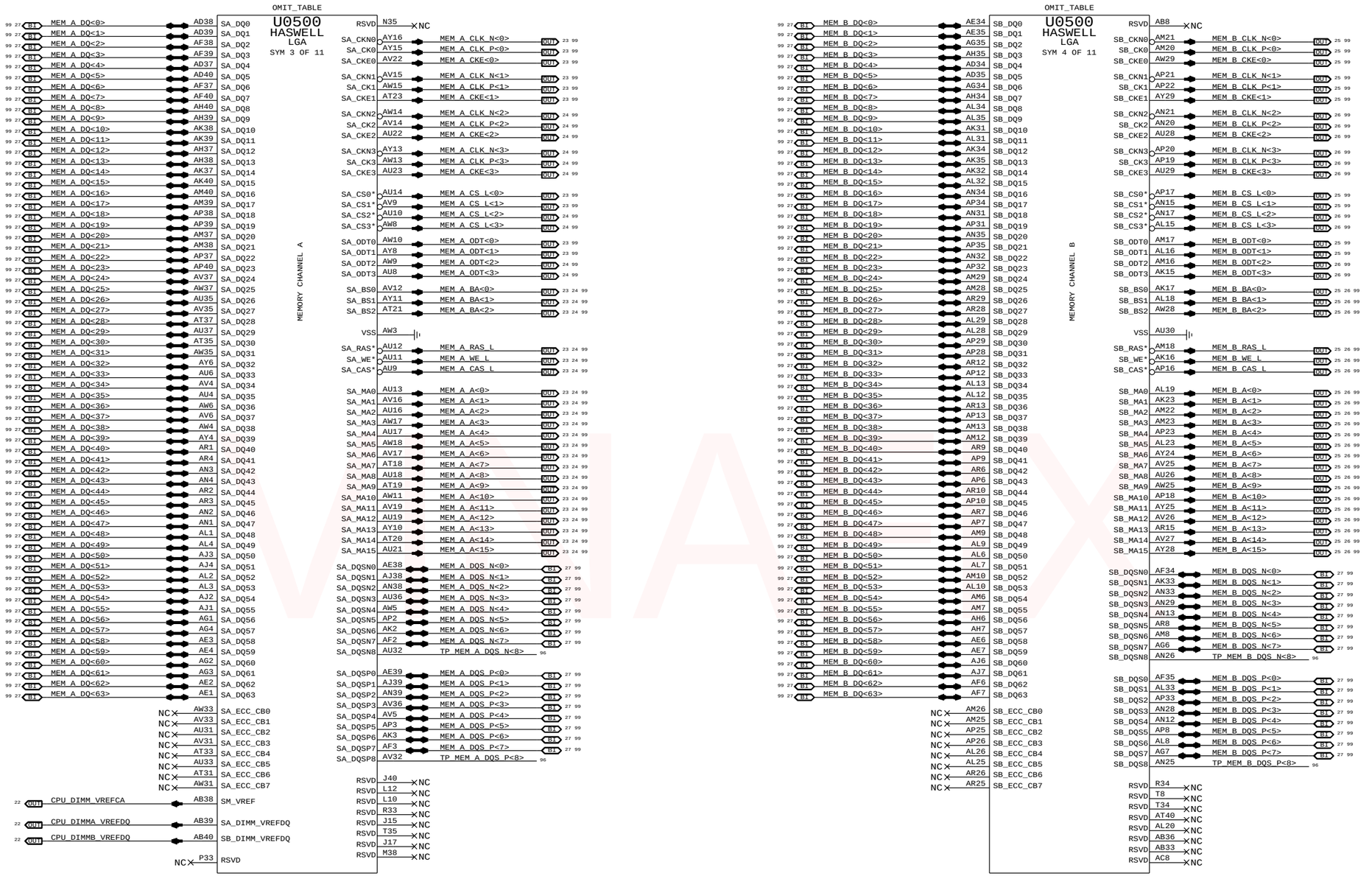

INTEL'S HASWELL DT EDS SAYS THAT ALL RSVD AND RSVD_NCTF SHOULD BE NC'D

SYNC MASTER=J78_MLB SYNC DATE=02/21/2014

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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BRANCH proto2

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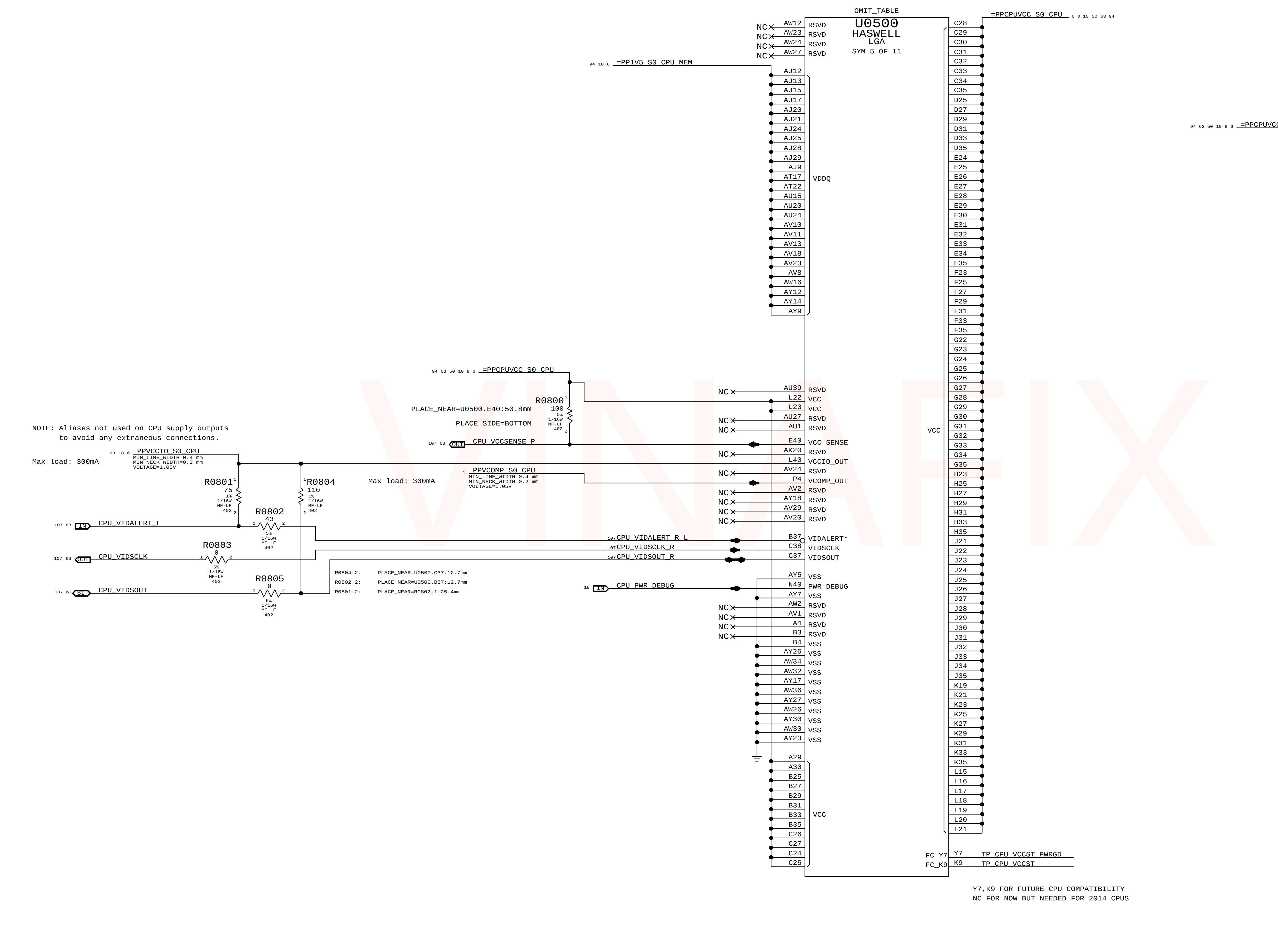

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE

CPU Power

Apple Inc.

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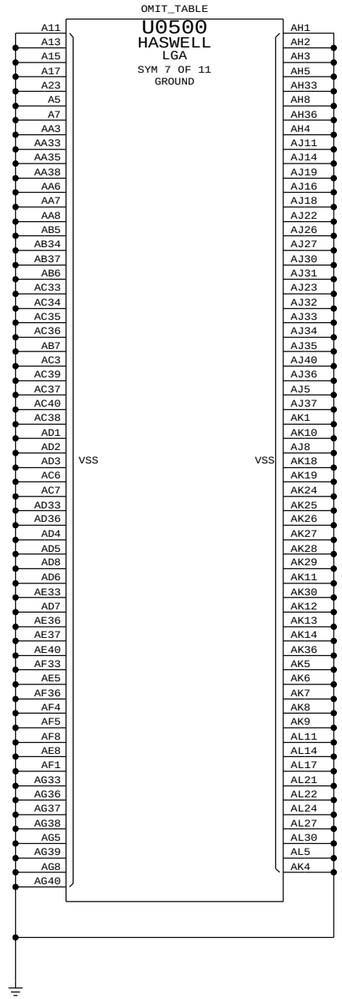
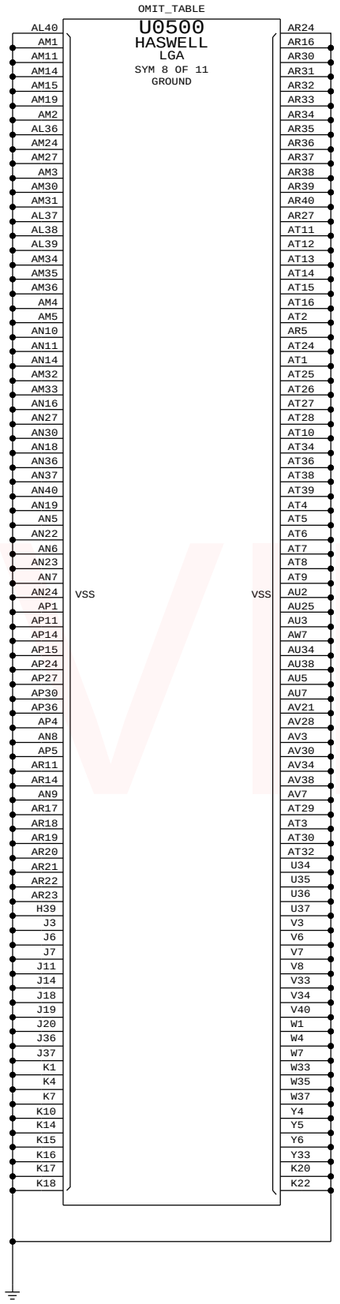
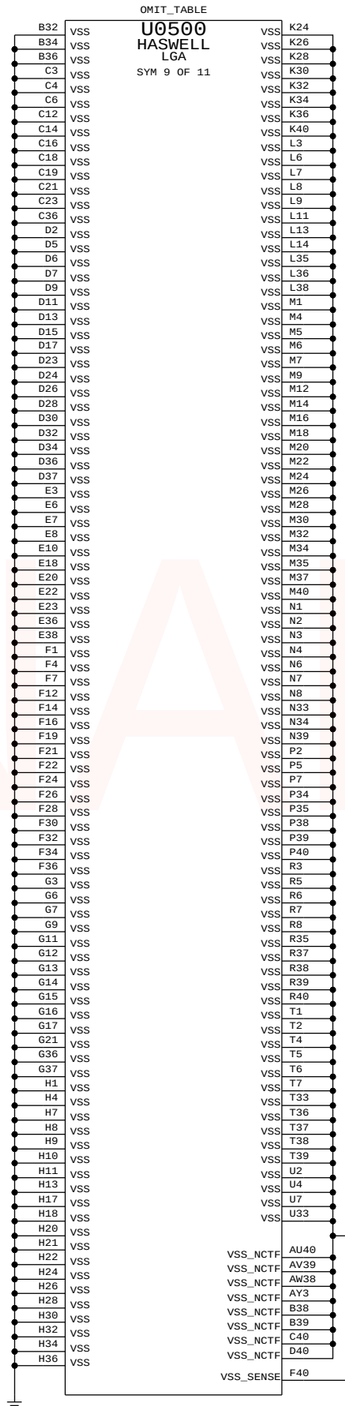
BRANCH proto2







CPU VCORE DECOUPLING

Intel Recommendation:22x 22UF 0805,topside (18 inside cavity, 4 north of processor),8x 470uF bulk caps(5 stuffed,3 no-stuffed)
Apple Implementation:28x 22UF 0603 per Harold
18x 10UF 0603 placed inside socket cavity

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71

94 63 50 8 6 =PPCPUVCC_S0_CPU

CRITICAL C1000 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1001 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1002 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1003 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1004 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1005 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1006 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1007 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1008 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1009 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1010 22UF 20% 6.3V X5R-CERM2 0603

CRITICAL C1011 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1012 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1013 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1014 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1015 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1016 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1017 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1018 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1019 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1020 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1021 22UF 20% 6.3V X5R-CERM2 0603

CRITICAL C1022 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1023 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1024 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1025 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1026 22UF 20% 6.3V X5R-CERM2 0603
CRITICAL C1027 22UF 20% 6.3V X5R-CERM2 0603

ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CRITICAL C1030 10UF 20% 6.3V X5R 603
CRITICAL C1031 10UF 20% 6.3V X5R 603
CRITICAL C1032 10UF 20% 6.3V X5R 603
CRITICAL C1033 10UF 20% 6.3V X5R 603
CRITICAL C1034 10UF 20% 6.3V X5R 603
CRITICAL C1035 10UF 20% 6.3V X5R 603
CRITICAL C1036 10UF 20% 6.3V X5R 603
CRITICAL C1037 10UF 20% 6.3V X5R 603
CRITICAL C1038 10UF 20% 6.3V X5R 603

CRITICAL C1039 10UF 20% 6.3V X5R 603
CRITICAL C1040 10UF 20% 6.3V X5R 603
CRITICAL C1041 10UF 20% 6.3V X5R 603
CRITICAL C1042 10UF 20% 6.3V X5R 603
CRITICAL C1043 10UF 20% 6.3V X5R 603
CRITICAL C1044 10UF 20% 6.3V X5R 603
CRITICAL C1045 10UF 20% 6.3V X5R 603
CRITICAL C1046 10UF 20% 6.3V X5R 603
CRITICAL C1047 10UF 20% 6.3V X5R 603

Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation:9x 22UF 0805 near CPU power pins
Apple Implementation:9x 22UF 0603 per Harold

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.

94 8 6 =PP1V5_S0_CPU_MEM

C1050 22UF 20% 6.3V X5R-CERM2 0603
C1051 22UF 20% 6.3V X5R-CERM2 0603
C1052 22UF 20% 6.3V X5R-CERM2 0603
C1053 22UF 20% 6.3V X5R-CERM2 0603
C1054 22UF 20% 6.3V X5R-CERM2 0603
C1055 22UF 20% 6.3V X5R-CERM2 0603
C1056 22UF 20% 6.3V X5R-CERM2 0603
C1057 22UF 20% 6.3V X5R-CERM2 0603
C1058 22UF 20% 6.3V X5R-CERM2 0603

NOSTUFF C1060 22UF 20% 6.3V X5R-CERM2 0603
NOSTUFF C1061 22UF 20% 6.3V X5R-CERM2 0603
NOSTUFF C1062 22UF 20% 6.3V X5R-CERM2 0603

CRITICAL C1059 470UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: CPU DECOUPLING

Apple Inc.

DRAWING NUMBER: 051-XXXX
SIZE: D
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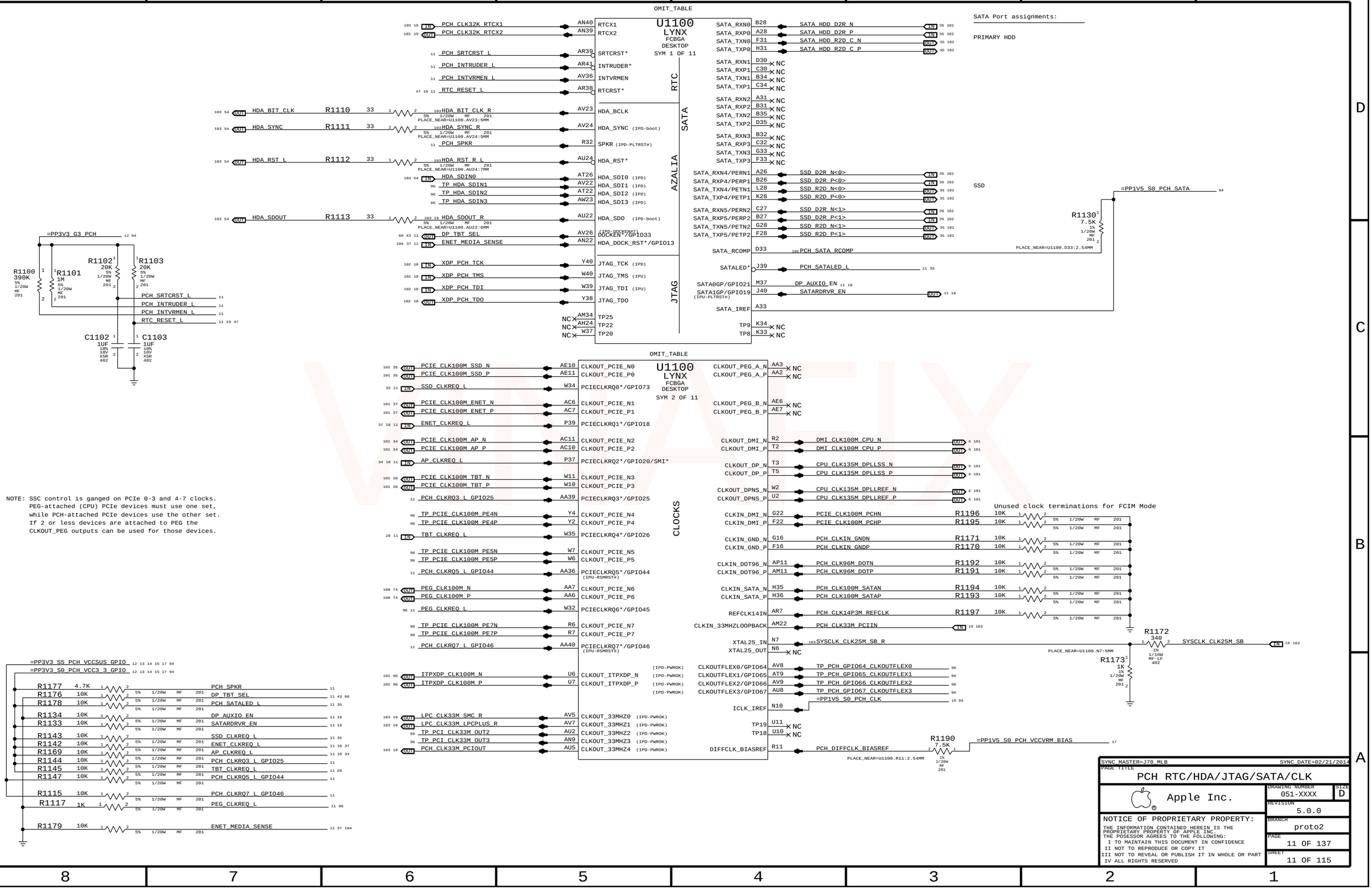
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U1100
LYNX
FCBGA
DESKTOP
SYM 1 OF 11
RTC
SATA
AZALIA
JTAG
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PCH_CLK32K_RTCX2
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
PCH_SPKR
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
DP_TBT_SEL
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_RXN4/PERN1
SATA_RXP4/PERP1
SATA_TXN4/PETN1
SATA_TXP4/PETP1
SSD_D2R_N<0>
SSD_D2R_P<0>
SSD_R2D_N<0>
SSD_R2D_P<0>
SATA_RXN5/PERN2
SATA_RXP5/PERP2
SATA_TXN5/PETN2
SATA_TXP5/PETP2
SSD_D2R_N<1>
SSD_D2R_P<1>
SSD_R2D_N<1>
SSD_R2D_P<1>
SATA_RCOMP
PCH_SATA_RCOMP
SATALED*
PCH_SATALED_L
SATA0GP/GPIO21
DP_AUXIO_EN
SATA1GP/GPIO19
SATARDRVR_EN
SATA_IREF
TP9
TP8
SATA Port assignments:
PRIMARY HDD
SSD
=PP1V5_S0_PCH_SATA
R1130 7.5K
PLACE_NEAR=U1100.D33:2.54MM
R1100 390K
R1101 1M
R1102 20K
R1103 20K
C1102 1UF
C1103 1UF
=PP3V3_G3_PCH
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 2 OF 11
CLOCKS
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
SSD_CLKREQ_L
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
ENET_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PCH_CLKRQ3_L_GPIO25
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
TBT_CLKREQ_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCH_CLKRQ5_L_GPIO44
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
TP_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P
PCH_CLKRQ7_L_GPIO46
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
TP_PCI_CLK33M_OUT2
TP_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_DPNS_N
CLKOUT_DPNS_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND_N
CLKIN_GND_P
CLKIN_DOT96_N
CLKIN_DOT96_P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_33MHZLOOPBACK
XTAL25_IN
XTAL25_OUT
PCIE_CLK100M_PCHN
PCIE_CLK100M_PCHP
PCH_CLKIN_GNDN
PCH_CLKIN_GNDP
PCH_CLK96M_DOTN
PCH_CLK96M_DOTP
PCH_CLK100M_SATAN
PCH_CLK100M_SATAP
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB_R
SYSCLK_CLK25M_SB
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
=PP1V5_S0_PCH_CLK
ICLK_IREF
DIFFCLK_BIASREF
PCH_DIFFCLK_BIASREF
=PP1V5_S0_PCH_VCCVRM_BIAS
Unused clock terminations for FCIM Mode
R1196 10K
R1195 10K
R1171 10K
R1170 10K
R1192 10K
R1191 10K
R1194 10K
R1193 10K
R1197 10K
R1172 340
R1173 1K
R1190 7.5K
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.
=PP3V3_S5_PCH_VCCSUS_GPIO
=PP3V3_S0_PCH_VCC3_3_GPIO
R1177 4.7K
R1176 10K
R1178 10K
R1134 10K
R1133 10K
R1143 10K
R1142 10K
R1169 10K
R1144 10K
R1145 10K
R1147 10K
R1115 10K
R1117 1K
R1179 10K
SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER
051-XXXX
SIZE
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REVISION
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OMIT_TABLE

U1100 LYNX FCBGA DESKTOP SYM 4 OF 11

DMI_RXN0 L24
DMI_RXN1 G24
DMI_RXN2 F26
DMI_RXN3 K26
DMI_RXP0 K24
DMI_RXP1 H24
DMI_RXP2 G26
DMI_RXP3 L26
DMI_TXN0 C20
DMI_TXN1 D21
DMI_TXN2 B22
DMI_TXN3 A24
DMI_TXP0 B20
DMI_TXP1 B21
DMI_TXP2 C22
DMI_TXP3 B24
DMI_IREF A19
TP12 L22
TP7 K22
DMI_RCOMP B19

DMI_N2S_N<0> 101 5 IN
DMI_N2S_N<1> 101 5 IN
DMI_N2S_N<2> 101 5 IN
DMI_N2S_N<3> 101 5 IN
DMI_N2S_P<0> 101 5 IN
DMI_N2S_P<1> 101 5 IN
DMI_N2S_P<2> 101 5 IN
DMI_N2S_P<3> 101 5 IN
DMI_S2N_N<0> 101 5 OUT
DMI_S2N_N<1> 101 5 OUT
DMI_S2N_N<2> 101 5 OUT
DMI_S2N_N<3> 101 5 OUT
DMI_S2N_P<0> 101 5 OUT
DMI_S2N_P<1> 101 5 OUT
DMI_S2N_P<2> 101 5 OUT
DMI_S2N_P<3> 101 5 OUT

94 13 12 =PP1V5_S0_PCH_RCOMP
R1200 1 7.5K 1% 1/20W MF 201 2
PLACE_NEAR=U1100.B19:12.7MM
101 PCH_DMI_RCOMP

DMI

FDI_RXN0 N1 NC
FDI_RXN1 P2 NC
FDI_RXP0 N2 NC
FDI_RXP1 P3 NC
TP16 R4 NC
TP5 K5 NC
TP15 P5 NC
TP10 L5 NC
FDI_CSYNC L2
FDI_INT L3
FDI_IREF N11
TP17 R12 NC
TP13 N12 NC
FDI_RCOMP K2

FDI_CSYNC FDI_CSYNC OUT 5 102
FDI_INT FDI_INT OUT 5 102
=PP1V5_S0_PCH_RCOMP 12 13 94
R1210 1 7.5K 1% 1/20W MF 201 2
PLACE_NEAR=U1100.K2:12.7MM
102 PCH_FDI_RCOMP
=PP3V3_G3_PCH 11 94
R1215 1 390K 5% 1/20W MF 201 2

FDI

SYSTEM POWER MANAGEMENT

SUSACK* (IPU) AJ37
SYS_RESET* N36
SYS_PWROK W31
PWROK AT40
APWROK AA32
DRAMPWROK (OD) AE38
RSMRST* AM40
SUSWARN*/SUSPWRNACK/GPIO30 AG41
PWRBTN* (IPU) AK41
ACPRESENT/GPIO31 (IPD-DeepSx) AM36
GPIO72 AJ40
RI* AE36
TP21 AC35
SLP_WLAN*/GPIO29 AL39

PCH_SUSACK_L
46 19 IN PM_SYSRST_L
73 47 18 IN PM_PCH_SYS_PWROK
87 73 41 20 18 IN PM_PCH_PWROK
73 IN PM_PCH_APWROK
21 6 OUT PM_MEM_PWRGD
73 18 12 IN PM_RSMRST_PCH_L
PCH_SUSWARN_L
46 18 12 IN PM_PWRBTN_L
12 PCH_GPIO31
12 PCH_GPIO72
PCH_RI_L
TP_PCH_SLP_WLAN_L

R1286 1 0 5% 1/20W MF 0201 2
94 17 15 14 13 12 11 =PP3V3_S5_PCH_VCCSUS_GPIO
R1205 1 10K 5% 1/20W MF 201 2

DSWVRMEN AM41 PCH_DSWVRMEN
DPWROK AV38 PM_RSMRST_PCH_L IN 12 18 73
WAKE* (IPD-DeepSx) AK34 PCIE_WAKE_L IN 12 20 34 38
GPIO32 N32 PCH_GPIO32 12
SUS_STAT*/GPIO61 AD37 LPC_PWRDWN_L OUT 20 46 48
SUSCLK/GPIO62 (IPU-RSMRST#) W36 PM_CLK32K_SUSCLK_R OUT 47 103
SLP_S5*/GPIO63 AA35 PM_SLP_S5_L OUT 12 34 46 72
SLP_S4* AT35 PM_SLP_S4_L OUT 12 46 72
SLP_S3* AK40 PM_SLP_S3_L OUT 12 21 38 46 47 72 73
SLP_A* AN37 TP_PM_SLP_A_L
SLP_SUS* AK38 PM_SLP_SUS_L 12
PMSYNCH F40 PM_SYNC OUT 6 115
SLP_LAN* AU36 TP_PCH_SLP_LAN_L

R1209 1 10K 5% 1/20W MF 201 2

OMIT_TABLE

U1100 LYNX FCBGA DESKTOP SYM 5 OF 11

VGA_BLUE AC3 NC
VGA_GREEN AE2 NC
VGA_RED AC2 NC
VGA_DDC_CLK AL2 NC
VGA_DDC_DATA AL3 NC
VGA_HSYNC AH3 NC
VGA_VSYNC AH2 NC
DAC_IREF AF5
VGA_IRTN AG4

CRT DISPLAY

DDPB_CTRLCLK AM1 NC
DDPB_CTRLDATA (IPD-PLTRST#) AJ5 NC
DDPC_CTRLCLK AN3 NC
DDPC_CTRLDATA (IPD-PLTRST#) AM2 NC
DDPD_CTRLCLK AN4 NC
DDPD_CTRLDATA (IPD-PLTRST#) AN2 NC
DDPB_AUXN AK6 NC
DDPC_AUXN AG7 NC
DDPD_AUXN AG11 NC
DDPB_AUXP AK8 NC
DDPC_AUXP AG6 NC
DDPD_AUXP AG10 NC
DDPB_HPD AJ2 NC
DDPC_HPD AH5 NC
DDPD_HPD AJ4 NC

VGA DAC Disabled per SB DG v1.0 (Table 11-11).

EDP_BKLTCTL AP2 NC
EDP_BKLTEN AT2 NC
EDP_VDDEN AP1 NC

EDP

94 17 15 14 13 12 11 =PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S5_PCH_VCCSUS_GPIO 11 12 13 14 15 17 94
=PP3V3_S0_PCH_VCC3_3_GPIO 11 12 13 14 15 17 94

R1260 10K 1 2 5% 1/20W MF 201 PCI_INTA_L AU29 PIRQA*
R1261 10K 1 2 5% 1/20W MF 201 PCI_INTB_L AU27 PIRQB*
R1262 10K 1 2 5% 1/20W MF 201 PCI_INTC_L AW28 PIRQC*
R1263 10K 1 2 5% 1/20W MF 201 PCI_INTD_L AV27 PIRQD*

20 12 OUT ENET_LOW_PWR_PCH AH26 GPIO50
20 12 OUT AUD_IPHS_SWITCH_EN_PCH AJ26 GPIO52
34 12 OUT BT_PWR_RST_L AW33 GPIO54

TP_PCH_STRP_BBS1 AU31 GPIO51
TP_PCH_STRP_ESI_L AV31 GPIO53
47 OUT PCH_STRP_TOPBLK_SWP_L R30 GPIO55 (IPU-PWROK&PCIRST#)

PCI

PIRQE*/GPIO2 AR30 SDCONN_OC_L IN 12 39
PIRQF*/GPIO3 AV29 AUD_IP_PERIPHERAL_DET IN 12 60
PIRQG*/GPIO4 AV28 TBT_PWR_REQ_L IN 12 29
PIRQH*/GPIO5 AT27 AUD_I2C_INT_L IN 12 58
(IPU)PME* AA31 TP_PCI_PME_L
PLTRST* AA37 PLT_RESET_L OUT 20

R1226 10K 2 1 5% 1/20W MF 201 PCH_GPIO31 12
R1240 10K 2 1 5% 1/20W MF 201 PCH_GPIO72 12
R1291 10K 1 2 5% 1/20W MF 201 PCH_GPIO32 12
R1216 10K 1 2 5% 1/20W MF 201 ENET_LOW_PWR_PCH 12 20
R1217 100K 1 2 5% 1/20W MF 201 AUD_IPHS_SWITCH_EN_PCH 12 20
R1218 10K 1 2 5% 1/20W MF 201 BT_PWR_RST_L 12 34
R1230 10K 1 2 5% 1/20W MF 201 SDCONN_OC_L 12 39
NOSTUFF Redundant to pull-up on audio page
R1214 100K 1 2 5% 1/20W MF 201 AUD_IP_PERIPHERAL_DET 12 60
R1231 10K 1 2 5% 1/20W MF 201 TBT_PWR_REQ_L 12 29
NOSTUFF Redundant to pull-up on audio page
R1233 10K 1 2 5% 1/20W MF 201 AUD_I2C_INT_L 12 58
R1225 1K 1 2 5% 1/20W MF 201 PCIE_WAKE_L 12 20 34 38

R1227 3.0K 1 2 5% 1/20W MF 201 PM_PWRBTN_L 12 18 46

R1224 100K 2 1 5% 1/20W MF 201 PM_SLP_S3_L 12 21 38 46 47 72 73
R1221 100K 2 1 5% 1/20W MF 201 PM_SLP_S4_L 12 46 72
R1222 100K 2 1 5% 1/20W MF 201 PM_SLP_S5_L 12 34 46 72
R1223 100K 2 1 5% 1/20W MF 201 PM_SLP_SUS_L 12

SYNC MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE

PCH DMI/FDI/PM/GFX/PCI

Apple Inc.

DRAWING NUMBER 051-XXXX SIZE D
REVISION 5.0.0
BRANCH proto2
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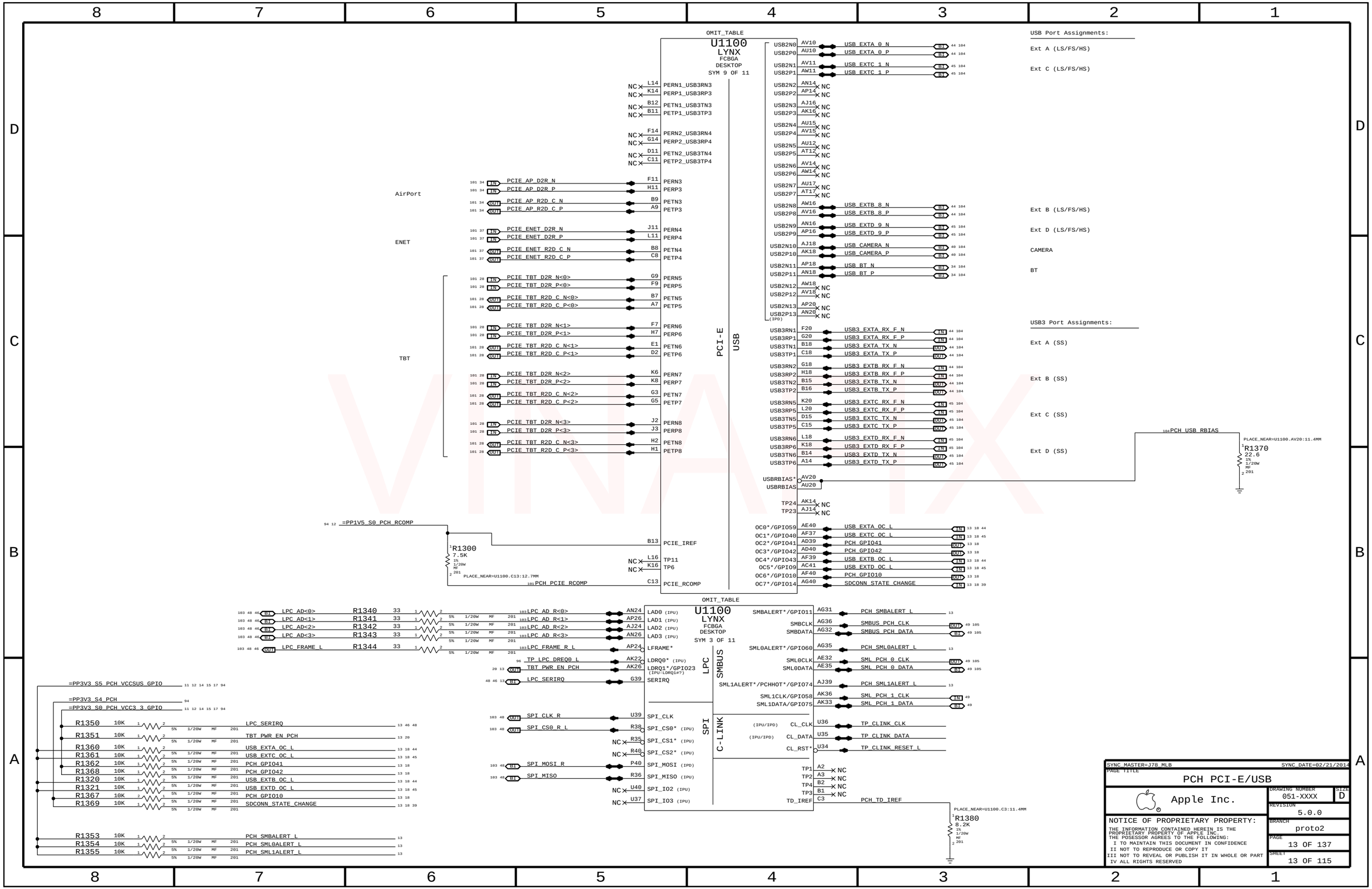
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 9 OF 11
PCI-E
USB
L14 PERN1_USB3RN3
K14 PERP1_USB3RP3
B12 PETN1_USB3TN3
B11 PETP1_USB3TP3
F14 PERN2_USB3RN4
G14 PERP2_USB3RP4
D11 PETN2_USB3TN4
C11 PETP2_USB3TP4
AirPort
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
F11 PERN3
H11 PERP3
B9 PETN3
A9 PETP3
ENET
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
J11 PERN4
L11 PERP4
B8 PETN4
C8 PETP4
TBT
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<0>
G9 PERN5
F9 PERP5
B7 PETN5
A7 PETP5
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<1>
F7 PERN6
H7 PERP6
E1 PETN6
D2 PETP6
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<2>
K6 PERN7
K8 PERP7
G3 PETN7
G5 PETP7
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
J2 PERN8
J3 PERP8
H2 PETN8
H1 PETP8
=PP1V5_S0_PCH_RCOMP
R1300 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.C13:12.7MM
PCH_PCIE_RCOMP
B13 PCIE_IREF
C13 PCIE_RCOMP
L16 TP11
K16 TP6
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
CAMERA
BT
USB2N0 AV10 USB_EXTA_0_N
USB2P0 AU10 USB_EXTA_0_P
USB2N1 AV11 USB_EXTC_1_N
USB2P1 AW11 USB_EXTC_1_P
USB2N2 AN14 NC
USB2P2 AP14 NC
USB2N3 AJ16 NC
USB2P3 AK16 NC
USB2N4 AU15 NC
USB2P4 AV15 NC
USB2N5 AU12 NC
USB2P5 AT12 NC
USB2N6 AV14 NC
USB2P6 AW14 NC
USB2N7 AU17 NC
USB2P7 AT17 NC
USB2N8 AW16 USB_EXTB_8_N
USB2P8 AV16 USB_EXTB_8_P
USB2N9 AN16 USB_EXTD_9_N
USB2P9 AP16 USB_EXTD_9_P
USB2N10 AJ18 USB_CAMERA_N
USB2P10 AK18 USB_CAMERA_P
USB2N11 AP18 USB_BT_N
USB2P11 AN18 USB_BT_P
USB2N12 AW18 NC
USB2P12 AV18 NC
USB2N13 AP20 NC
USB2P13 AN20 NC
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
USB3RN1 F20 USB3_EXTA_RX_F_N
USB3RP1 G20 USB3_EXTA_RX_F_P
USB3TN1 B18 USB3_EXTA_TX_N
USB3TP1 C18 USB3_EXTA_TX_P
USB3RN2 G18 USB3_EXTB_RX_F_N
USB3RP2 H18 USB3_EXTB_RX_F_P
USB3TN2 B15 USB3_EXTB_TX_N
USB3TP2 B16 USB3_EXTB_TX_P
USB3RN5 K20 USB3_EXTC_RX_F_N
USB3RP5 L20 USB3_EXTC_RX_F_P
USB3TN5 D15 USB3_EXTC_TX_N
USB3TP5 C15 USB3_EXTC_TX_P
USB3RN6 L18 USB3_EXTD_RX_F_N
USB3RP6 K18 USB3_EXTD_RX_F_P
USB3TN6 B14 USB3_EXTD_TX_N
USB3TP6 A14 USB3_EXTD_TX_P
PCH_USB_RBIAS
PLACE_NEAR=U1100.AV20:11.4MM
R1370 22.6 1% 1/20W MF 201
USBRBIAS*
USBRBIAS
AV20
AU20
TP24 AK14 NC
TP23 AJ14 NC
OC0*/GPIO59 AE40 USB_EXTA_OC_L
OC1*/GPIO46 AF37 USB_EXTC_OC_L
OC2*/GPIO41 AD39 PCH_GPIO41
OC3*/GPIO42 AD40 PCH_GPIO42
OC4*/GPIO43 AF39 USB_EXTB_OC_L
OC5*/GPIO9 AC41 USB_EXTD_OC_L
OC6*/GPIO16 AF40 PCH_GPIO10
OC7*/GPIO14 AG40 SDCONN_STATE_CHANGE
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 3 OF 11
LPC
SMBUS
SPI
C-LINK
LAD0 (IPU) AN24
LAD1 (IPU) AP26
LAD2 (IPU) AJ24
LAD3 (IPU) AN26
LFRAME* AP24
LDRQ0* (IPU) AK22
LDRQ1*/GPIO23 (IPU-LDRQ1#?) AK26
SERIRQ G39
LPC_AD<0> R1340 33
LPC_AD<1> R1341 33
LPC_AD<2> R1342 33
LPC_AD<3> R1343 33
LPC_FRAME_L R1344 33
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SPI_CLK U39
SPI_CS0* (IPU) R38
SPI_CS1* (IPU) R35
SPI_CS2* (IPU) R40
SPI_MOSI (IPD) P40
SPI_MISO (IPU) R36
SPI_IO2 (IPU) U40
SPI_IO3 (IPU) U37
SPI_CLK_R
SPI_CS0_R_L
SPI_MOSI_R
SPI_MISO
SMBALERT*/GPIO11 AG31 PCH_SMBALERT_L
SMBCLK AG36 SMBUS_PCH_CLK
SMBDATA AG32 SMBUS_PCH_DATA
SML0ALERT*/GPIO60 AG35 PCH_SML0ALERT_L
SML0CLK AE32 SML_PCH_0_CLK
SML0DATA AE35 SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO74 AJ39 PCH_SML1ALERT_L
SML1CLK/GPIO58 AK36 SML_PCH_1_CLK
SML1DATA/GPIO75 AK33 SML_PCH_1_DATA
CL_CLK U36 TP_CLINK_CLK
CL_DATA U35 TP_CLINK_DATA
CL_RST* U34 TP_CLINK_RESET_L
TP1 A2 NC
TP2 A3 NC
TP4 B2 NC
TP3 B1 NC
TD_IREF C3 PCH_TD_IREF
PLACE_NEAR=U1100.C3:11.4MM
R1380 8.2K 1% 1/20W MF 201
=PP3V3_S5_PCH_VCCSUS_GPIO
=PP3V3_S4_PCH
=PP3V3_S0_PCH_VCC3_3_GPIO
R1350 10K LPC_SERIRQ
R1351 10K TBT_PWR_EN_PCH
R1360 10K USB_EXTA_OC_L
R1361 10K USB_EXTC_OC_L
R1362 10K PCH_GPIO41
R1368 10K PCH_GPIO42
R1320 10K USB_EXTB_OC_L
R1321 10K USB_EXTD_OC_L
R1367 10K PCH_GPIO10
R1369 10K SDCONN_STATE_CHANGE
R1353 10K PCH_SMBALERT_L
R1354 10K PCH_SML0ALERT_L
R1355 10K PCH_SML1ALERT_L
SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
DRAWING NUMBER 051-XXXX
SIZE D
REVISION 5.0.0
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OMIT_TABLE

U1100
LYNX
FCBGA
DESKTOP
SYM 6 OF 11

GPIO

CPU/MISC

20	IN	TBT_CIO_PLUG_EVENT_ISOL
69	IN	BKLT_FAULT_INT_L
14		DPMUX_UC_IRQ
105 46 14	IN	SMC_RUNTIME_SCI_L
36 18	OUT	HDD_PWR_EN
38 14	OUT	WOL_EN
14		MEM_VDD_SEL_1V5_L
18 14	IN	PCH_GPIO16
48 14	BI	LPCPLUS_GPIO
20 14	OUT	JTAG_TBT_TMS_PCH
	NC	
105 46 14	IN	SMC_WAKE_SCI_L
22	OUT	ISOLATE_CPU_MEM_L
20	OUT	TBT_POC_RESET_L
115 18 3	OUT	GPU_GOOD
18 14	OUT	PCH_GPIO36
20 18 14	OUT	JTAG_ISP_TCK
20 14	IN	JTAG_ISP_TDO
20 14	OUT	JTAG_ISP_TDI
14		FW_PWR_EN_PCH
18 14	IN	PCH_GPIO49
103 48	BI	SPIROM_USE_MLB
41	OUT	PCH_CAM_EXT_BOOT_R_L
41	OUT	PCH_CAM_RESET_R

G38	BMBUSY*/GPIO0	
AT31	TACH1/GPIO1	
AM28	TACH2/GPIO6	
AV34	TACH3/GPIO7	
AC40	GPIO8 (IPU-RSMRST#)	
AL40	LAN_PHY_PWR_CTRL/GPIO12	
AC32	GPIO15	
M39	SATA4GP/GPIO16 (IPU-Boot/SATA4GP?)	
AP28	TACH0/GPIO17	
L38	SCLOCK/GPIO22	
AE34	GPIO24	
AU34	GPIO27 (IPU-DeepSx)	
V41	GPIO28	
N34	GPIO34	
M40	GPIO35/NMI*	
H40	SATA2GP/GPIO36 (IPD-PLTRST#)	
N41	SATA3GP/GPIO37 (IPD-PLTRST#)	
H41	SLOAD/GPIO38	
R31	SDATAOUT0/GPIO39	
L40	SDATAOUT1/GPIO48	
N40	SATA5GP/GPIO49 (IPU-Boot/SATA5GP?)	
AC36	GPIO57	
AT30	TACH4/GPIO68	
AV35	TACH5/GPIO69	
AK28	TACH6/GPIO70 (IPU-Boot?)	
AT34	TACH7/GPIO71 (IPU-Boot?)	

R1461 33.2 1% 1/20W MF 201
R1462 33.2 1% 1/20W MF 201
PLACE_NEAR=U1100.AT30:10MM
PLACE_NEAR=U1100.AV35:10MM

14		PCH_CAM_EXT_BOOT_L
14		PCH_CAM_RESET
14		TP_PCH_BLC_MCU_RESET_R
14		TP_PCH_BLC_EXT_BOOT_R

AT14	VSS	
AT15	VSS	
AT16	VSS	
AT18	VSS	

AL31	PWM0	NC
AM31	PWM1	NC
AP31	PWM2	NC
AV30	PWM3	NC
AJ31	SST	NC
N30	TP14	PCH_A20GATE (14)
G40	(IPD) PECI	PCH_PECI
K36	RCIN*	PCH_RCIN_L (14)
D40	PROCPWRGD	PCH_PROCPWRGD (115)
C40	THRMTRIP*	PM_THRMTRIP_L_R
F41	PLTRST_PROC*	CPU_RESET_L (OUT 6 18 115)
AV33	VSS	

AT20	VSS
AT21	VSS
AT23	VSS
AT24	VSS
AT28	VSS
AT29	VSS
AT33	VSS
AT36	VSS
AT38	VSS
AT41	VSS
AT7	VSS
AT8	VSS
AU1	VSS
AU3	VSS
AU39	VSS
AV1	VSS
AV12	VSS
AV17	VSS
AV2	VSS
AV21	VSS

=PP1V05_S0_PCH_V_PROC_IO (15 17 94)

NOSTUFF
R1457 1K 5% 1/16W MF-LF 402

NOSTUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI (BI 6 46 47 105)
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD (OUT 6 18 115)
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L (IN 47 115)

=PP3V3_S5_PCH_VCCSUS_GPIO (11 12 13 15 17 94)
=PP3V3_S0_PCH_VCC3_3_GPIO (11 12 13 15 17 94)

R1452	10K	5% 1/20W MF 201	TP_PCH_BLC_MCU_RESET_R	14
R1451	10K	5% 1/20W MF 201	TP_PCH_BLC_EXT_BOOT_R	14
R1411	20K	5% 1/20W MF 201	DPMUX_UC_IRQ	14
R1496	10K	5% 1/20W MF 201	SMC_RUNTIME_SCI_L	14 46 105
R1494	10K	5% 1/20W MF 201	WOL_EN	14 38
R1489	10K	5% 1/20W MF 201	MEM_VDD_SEL_1V5_L	14
R1495	10K	5% 1/20W MF 201	PCH_GPIO16	14 18
R1490	100K	5% 1/20W MF 201	LPCPLUS_GPIO	14 48
R1412	10K	5% 1/20W MF 201	JTAG_TBT_TMS_PCH	14 20
R1491	10K	5% 1/20W MF 201	SMC_WAKE_SCI_L	14 46 105
R1498	10K	5% 1/20W MF 201	PCH_GPIO36	14 18
R1413	10K	5% 1/20W MF 201	JTAG_ISP_TCK	14 18 20
R1486	10K	5% 1/20W MF 201	JTAG_ISP_TDO	14 20
R1499	10K	5% 1/20W MF 201	JTAG_ISP_TDI	14 20
R1484	10K	5% 1/20W MF 201	FW_PWR_EN_PCH	14
R1497	10K	5% 1/20W MF 201	PCH_GPIO49	14 18
R1450	10K	5% 1/20W MF 201	PCH_A20GATE	14
R1455	10K	5% 1/20W MF 201	PCH_RCIN_L	14

14 PCH_CAM_EXT_BOOT_L
14 PCH_CAM_RESET
R1422 1K 5% 1/20W MF 201
R1423 1K 5% 1/20W MF 201

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014
PAGE TITLE: PCH GPIO/MISC/NCTF
Apple Inc.
DRAWING NUMBER: 051-XXXX SIZE: D
REVISION: 5.0.0
BRANCH: proto2
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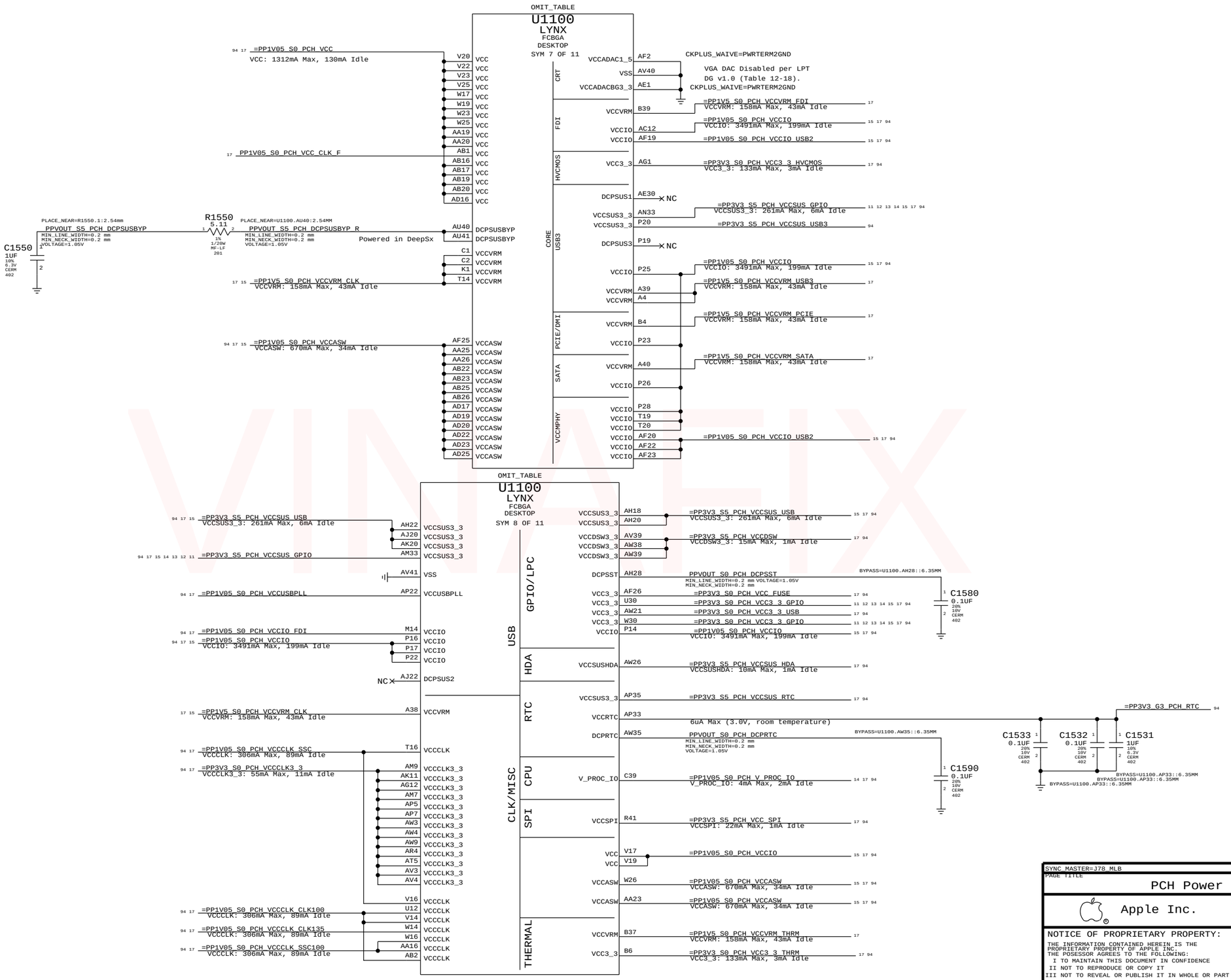
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 7 OF 11
=PP1V05_S0_PCH_VCC
VCC: 1312mA Max, 130mA Idle
V20 V22 V23 V25 W17 W19 W23 W25 AA19 AA20 AB1 AB16 AB17 AB19 AB20 AD16 VCC
=PP1V05_S0_PCH_VCC_CLK_F
PLACE_NEAR=R1550.1:2.54mm
PPVOUT_S5_PCH_DCPSUSBYP
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
C1550
1UF
10%
6.3V
CERM
402
R1550
5.11
1%
1/20W
MF-LF
201
PLACE_NEAR=U1100.AU40:2.54MM
PPVOUT_S5_PCH_DCPSUSBYP_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
Powered in DeepSx
AU40 AU41 DCPSUSBYP
C1 C2 K1 T14 VCCVRM
=PP1V5_S0_PCH_VCCVRM_CLK
VCCVRM: 158mA Max, 43mA Idle
=PP1V05_S0_PCH_VCCASW
VCCASW: 670mA Max, 34mA Idle
AF25 AA25 AA26 AB22 AB23 AB25 AB26 AD17 AD19 AD20 AD22 AD23 AD25 VCCASW
CRT
FDI
HVCMOS
CORE USB3
PCIE/DMI
SATA
VCCMPHY
VCCADAC1_5 AF2 CKPLUS_WAIVE=PWRTERM2GND
VSS AV40
VGA DAC Disabled per LPT
DG v1.0 (Table 12-18).
VCCADACBG3_3 AE1 CKPLUS_WAIVE=PWRTERM2GND
VCCVRM B39 =PP1V5_S0_PCH_VCCVRM_FDI VCCVRM: 158mA Max, 43mA Idle
VCCIO AC12 =PP1V05_S0_PCH_VCCIO VCCIO: 3491mA Max, 199mA Idle
VCCIO AF19 =PP1V05_S0_PCH_VCCIO_USB2
VCC3_3 AG1 =PP3V3_S0_PCH_VCC3_3_HVCMOS VCC3_3: 133mA Max, 3mA Idle
DCPSUS1 AE30 NC
VCCSUS3_3 AN33 =PP3V3_S5_PCH_VCCSUS_GPIO VCCSUS3_3: 261mA Max, 6mA Idle
VCCSUS3_3 P20 =PP3V3_S5_PCH_VCCSUS_USB3
DCPSUS3 P19 NC
VCCIO P25 =PP1V05_S0_PCH_VCCIO VCCIO: 3491mA Max, 199mA Idle
VCCVRM A39 A4 =PP1V5_S0_PCH_VCCVRM_USB3 VCCVRM: 158mA Max, 43mA Idle
VCCVRM B4 =PP1V5_S0_PCH_VCCVRM_PCIE VCCVRM: 158mA Max, 43mA Idle
VCCIO P23
VCCVRM A40 =PP1V5_S0_PCH_VCCVRM_SATA VCCVRM: 158mA Max, 43mA Idle
VCCIO P26
VCCIO P28 T19 T20 AF20 AF22 AF23
=PP1V05_S0_PCH_VCCIO_USB2
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 8 OF 11
=PP3V3_S5_PCH_VCCSUS_USB
VCCSUS3_3: 261mA Max, 6mA Idle
AH22 AJ20 AK20 VCCSUS3_3
=PP3V3_S5_PCH_VCCSUS_GPIO
AM33 VCCSUS3_3
VSS AV41
=PP1V05_S0_PCH_VCCUSBPLL
AP22 VCCUSBPLL
=PP1V05_S0_PCH_VCCIO_FDI
M14 VCCIO
=PP1V05_S0_PCH_VCCIO
VCCIO: 3491mA Max, 199mA Idle
P16 P17 P22 VCCIO
NC AJ22 DCPSUS2
=PP1V5_S0_PCH_VCCVRM_CLK
VCCVRM: 158mA Max, 43mA Idle
A38 VCCVRM
=PP1V05_S0_PCH_VCCCLK_SSC
VCCCLK: 306mA Max, 89mA Idle
T16 VCCCLK
=PP3V3_S0_PCH_VCCCLK3_3
VCCCLK3_3: 55mA Max, 11mA Idle
AM9 AK11 AG12 AM7 AP5 AP7 AW3 AW4 AW9 AR4 AT5 AV3 AV4 VCCCLK3_3
V16 U12 V14 W14 W16 AA16 AB2 VCCCLK
=PP1V05_S0_PCH_VCCCLK_CLK100
VCCCLK: 306mA Max, 89mA Idle
=PP1V05_S0_PCH_VCCCLK_CLK135
VCCCLK: 306mA Max, 89mA Idle
=PP1V05_S0_PCH_VCCCLK_SSC100
VCCCLK: 306mA Max, 89mA Idle
GPIO/LPC
USB
HDA
RTC
CPU
SPI
CLK/MISC
THERMAL
VCCSUS3_3 AH18 AH20 =PP3V3_S5_PCH_VCCSUS_USB VCCSUS3_3: 261mA Max, 6mA Idle
VCCDSW3_3 AV39 AW38 AW39 =PP3V3_S5_PCH_VCCDSW VCCDSW3_3: 15mA Max, 1mA Idle
DCPSST AH28 PPVOUT_S0_PCH_DCPSST
MIN_LINE_WIDTH=0.2 mm VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 mm
BYPASS=U1100.AH28::6.35MM
C1580
0.1UF
20%
10V
CERM
402
VCC3_3 AF26 =PP3V3_S0_PCH_VCC_FUSE
VCC3_3 U30 =PP3V3_S0_PCH_VCC3_3_GPIO
VCC3_3 AW21 =PP3V3_S0_PCH_VCC3_3_USB
VCC3_3 W30 =PP3V3_S0_PCH_VCC3_3_GPIO
VCCIO P14 =PP1V05_S0_PCH_VCCIO VCCIO: 3491mA Max, 199mA Idle
VCCSUSHDA AW26 =PP3V3_S5_PCH_VCCSUS_HDA VCCSUSHDA: 10mA Max, 1mA Idle
VCCSUS3_3 AP35 =PP3V3_S5_PCH_VCCSUS_RTC
=PP3V3_G3_PCH_RTC
VCCRTC AP33
6uA Max (3.0V, room temperature)
DCPRTC AW35 PPVOUT_S0_PCH_DCPRTC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
BYPASS=U1100.AW35::6.35MM
C1590
0.1UF
20%
10V
CERM
402
C1533
0.1UF
20%
10V
CERM
402
C1532
0.1UF
20%
10V
CERM
402
C1531
1UF
10%
6.3V
CERM
402
BYPASS=U1100.AP33::6.35MM
BYPASS=U1100.AP33::6.35MM
BYPASS=U1100.AP33::6.35MM
V_PROC_IO C39 =PP1V05_S0_PCH_V_PROC_IO V_PROC_IO: 4mA Max, 2mA Idle
VCCSPI R41 =PP3V3_S5_PCH_VCC_SPI VCCSPI: 22mA Max, 1mA Idle
VCC V17 V19 =PP1V05_S0_PCH_VCCIO
VCCASW W26 =PP1V05_S0_PCH_VCCASW VCCASW: 670mA Max, 34mA Idle
VCCASW AA23 =PP1V05_S0_PCH_VCCASW VCCASW: 670mA Max, 34mA Idle
VCCVRM B37 =PP1V5_S0_PCH_VCCVRM_THRM VCCVRM: 158mA Max, 43mA Idle
VCC3_3 B6 =PP3V3_S0_PCH_VCC3_3_THRM VCC3_3: 133mA Max, 3mA Idle
Current data from LPT EDS (doc #486708, Rev 1.0).
SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014
PAGE TITLE
PCH Power
Apple Inc.
DRAWING NUMBER 051-XXXX
SIZE D
REVISION 5.0.0
BRANCH proto2
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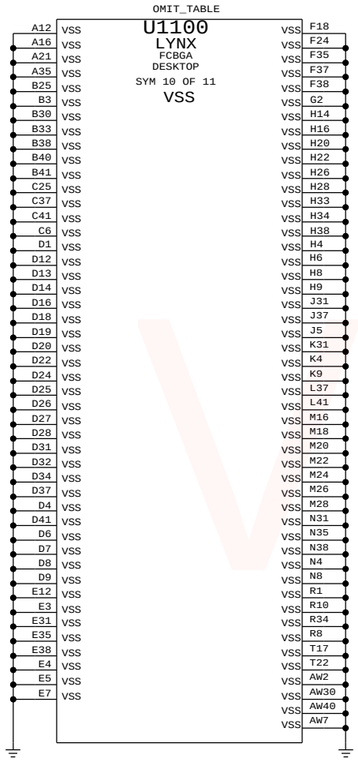

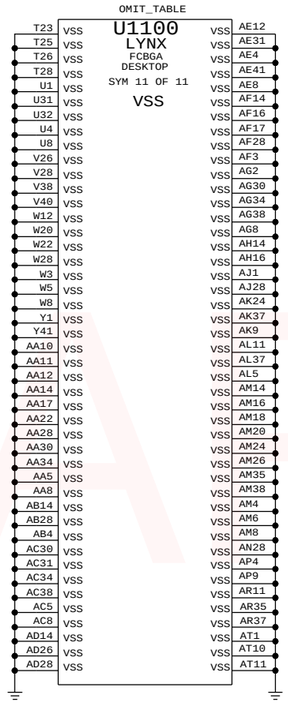

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER 051-XXXX

SIZE D

REVISION 5.0.0

BRANCH proto2

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR) INTEL:1X 0.1UF(402)
94 15 =PP3V3_S5_PCH_VCCDSW
15mA Max, 1mA Idle
C1700 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AW39::6.35MM

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR) INTEL:1X 1UF(402)
94 15 =PP3V3_S5_PCH_VCC_SPI
22mA Max, 1mA Idle
C1702 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.R41::6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR) INTEL:1X 0.1UF(402)
94 15 14 13 12 11 =PP3V3_S5_PCH_VCCSUS_GPIO
261mA Max, 6mA Idle
C1704 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AN33::6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR) INTEL:1X 0.1UF(402)
94 15 =PP3V3_S5_PCH_VCCSUS_USB
261mA Max, 6mA Idle
C1706 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AK20::6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V DSW RTC PWR) INTEL:1X 1UF(402)
94 15 =PP3V3_S5_PCH_VCCSUS_RTC
C1708 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP35::6.35MM

PCH VCCCLK3_3 BYPASS 55mA Max, 11mA Idle
(PCH 3.3V CLK PWR) INTEL:4X 1UF(402)
94 15 =PP3V3_S0_PCH_VCCCLK3_3
C1720 1 1UF 10% 6.3V CERM 402 2
C1721 1 1UF 10% 6.3V CERM 402 2
C1722 1 1UF 10% 6.3V CERM 402 2
C1723 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP5::6.35MM
BYPASS=U1100.AV4::6.35MM
BYPASS=U1100.AR4::6.35MM
BYPASS=U1100.AT5::6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR) INTEL:1X 0.1UF(402)
94 15 =PP3V3_S0_PCH_VCC3_3_HVCMOS
133mA Max, 3mA Idle
C1726 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AG1::6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR) INTEL:1X 0.1UF(402)
94 15 14 13 12 11 =PP3V3_S0_PCH_VCC3_3_GPIO
133mA Max, 3mA Idle
C1728 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.W30::6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR) INTEL:1X 1UF(402)
94 15 =PP3V3_S0_PCH_VCC3_3_USB
133mA Max, 3mA Idle
C1730 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AW21::6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR) INTEL:1X 0.1UF(402)
94 15 =PP3V3_S0_PCH_VCC3_3_THRM
133mA Max, 3mA Idle
C1732 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.B6::6.35MM

PCH VCC BYPASS
(PCH 3.3V FUSE PWR) INTEL:1X 1UF(402)
94 15 =PP3V3_S0_PCH_VCC_FUSE
133mA Max, 3mA Idle
C1734 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AF26::6.35MM

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR) INTEL:1X10UF(805), 1X1UF(402)
94 15 =PP1V05_S0_PCH_VCCASW
670mA Max, 34mA Idle
C1753 1 10UF 20% 4V X6S 0402 2
C1750 1 10UF 20% 4V X6S 0402 2
C1751 1 1UF 10% 6.3V CERM 402 2
C1752 1 1UF 10% 6.3V CERM 402 2
place_near=U1100.AD19:2.54MM
place_near=U1100.AD17:2.54MM
place_near=U1100.AD19:2.54MM
place_near=U1100.AD17:2.54MM

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
94 15 =PP1V05_S0_PCH_VCC
1312mA Max, 130mA Idle
THESE 4X1UF ARE EXTRA BYPASS
XW1701 SHORT-0201 SNS_GPU_PEX_IOVDD_P 68 106
C1761 1 1UF 10% 6.3V CERM 402 2
C1756 1 1UF 10% 6.3V CERM 402 2
C1757 1 1UF 10% 6.3V CERM 402 2
C1758 1 1UF 10% 6.3V CERM 402 2
XW1702 SHORT-0201 SNS_GPU_PEX_IOVDD_N 68 106
BYPASS=U1100.P14::6.35MM
BYPASS=U1100.V22::6.35MM
BYPASS=U1100.V25::6.35MM
BYPASS=U1100.AA19::6.35MM

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR) INTEL:2X10UF(805), 3X1UF(402)
94 15 =PP1V05_S0_PCH_VCCIO
3491mA Max, 114mA Idle
C1760 1 10UF 20% 4V X6S 0402 2
C1755 1 10UF 20% 4V X6S 0402 2
C1762 1 1UF 10% 6.3V CERM 402 2
C1763 1 1UF 10% 6.3V CERM 402 2
C1764 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.P14::12.7MM
BYPASS=U1100.P28::12.7MM
BYPASS=U1100.P16::6.35MM
BYPASS=U1100.P17::6.35MM
BYPASS=U1100.P26::6.35MM

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR) INTEL:1X 1UF(402)
94 15 =PP1V05_S0_PCH_VCCUSBPLL
C1770 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AP22::6.35MM

PCH VCCIO BYPASS INTEL:1X 1UF(402)
(PCH 1.05V FDI PWR)
94 15 =PP1V05_S0_PCH_VCCIO_FDI
3491mA Max, 114mA Idle
C1772 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.M14::6.35MM

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR) INTEL:1X 1UF(402)
94 15 =PP1V05_S0_PCH_VCCIO_USB2
3491mA Max, 114mA Idle
C1774 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AF19::6.35MM

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR) INTEL:1X1UF(603), 2X0.1UF(402)
94 15 14 =PP1V05_S0_PCH_V_PROC_IO
4mA Max, 2mA Idle
C1785 1 1UF 10% 6.3V CERM 402 2
C1786 1 0.1UF 20% 10V CERM 402 2
C1787 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.C39::12.7MM
BYPASS=U1100.C39::6.35MM
BYPASS=U1100.C39::6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR) INTEL:2X 1UF(402)
94 15 =PP1V05_S0_PCH_VCCCLK_SSC100
306mA Max, 89mA Idle
C1776 1 1UF 10% 6.3V CERM 402 2
C1777 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.AA16::6.35MM
BYPASS=U1100.W16::6.35MM

PCH VCCCLK BYPASS INTEL:2X 1UF(402)
(PCH 1.05V DIFFCLK PWR)
94 15 =PP1V05_S0_PCH_VCCCLK_CLK100
306mA Max, 89mA Idle
C1778 1 1UF 10% 6.3V CERM 402 2
C1783 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.U12::6.35MM
BYPASS=U1100.AB2::6.35MM

PCH VCCCLK BYPASS INTEL:1X 1UF(402)
(PCH 1.05V DIFFCLK135 PWR)
94 15 =PP1V05_S0_PCH_VCCCLK_CLK135
306mA Max, 89mA Idle
C1780 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.W14::6.35MM

PCH VCCCLK BYPASS INTEL:1X 1UF(402)
(PCH 1.05V SSC PWR)
94 15 =PP1V05_S0_PCH_VCCCLK_SSC
306mA Max, 89mA Idle
C1782 1 1UF 10% 6.3V CERM 402 2
BYPASS=U1100.V16::6.35MM

PCH VCCSUSHDA BYPASS
(PCH 3.3V HDA PWR) INTEL:1X 0.1UF(402)
94 15 =PP3V3_S5_PCH_VCCSUS_HDA
10mA Max, 1mA Idle
C1710 1 0.1UF 20% 10V CERM 402 2
BYPASS=U1100.AW26::6.35MM

PCH VCCVRM BYPASS INTEL:1X 0.1UF(402)
(PCH 1.5V VCCVRM PWR)
94 =PP1V5_S0_PCH_VCCVRM
158mA Max, 43mA Idle
11 =PP1V5_S0_PCH_VCCVRM_BIAS
15 =PP1V5_S0_PCH_VCCVRM_FDI
15 =PP1V5_S0_PCH_VCCVRM_USB3
15 =PP1V5_S0_PCH_VCCVRM_PCIE
15 =PP1V5_S0_PCH_VCCVRM_SATA
15 =PP1V5_S0_PCH_VCCVRM_CLK
15 =PP1V5_S0_PCH_VCCVRM_THRM
C1740 1 0.1UF 20% 16V CERM 603 2
BYPASS=U1100.T14::12.7MM

PCH_CLK_VCC_BYPASS INTEL:1X10UF(603), 1X1UF(402)
(PCH 1.05V CLK PLL PWR. NOSTUFF 10UF IF IDG NO USED)
94 =PP1V05_S0_PCH_VCC_CLK
306mA Max, 89mA Idle
L1790 5% 1/10W MF-LF 603
PP1V05_S0_PCH_VCC_CLK_F 15
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
C1790 1 NOSTUFF 10UF 20% 6.3V X5R 603 2
C1791 1 1UF 10% 10V X5R 402 2
BYPASS=U1100.AB1::12.7MM
BYPASS=U1100.AB1::6.35MM

Current data from LPT EDS (doc #486708, Rev 1.0).

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Extra BPM Testpoints

XDP_BPM_L<2>	TP-P6	TP1802
XDP_BPM_L<3>	TP-P6	TP1803
XDP_BPM_L<4>	TP-P6	TP1804
XDP_BPM_L<5>	TP-P6	TP1805
XDP_BPM_L<6>	TP-P6	TP1806
XDP_BPM_L<7>	TP-P6	TP1807

CPU Micro2-XDP

PPVCCIO_S0_CPU

=PP1V05_S0_XDP

R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM

998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_VR_READY	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
	NC	XDP_PRESENT#	

NC per Intel DPDG.

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_PRESENT_L

XDP C1804 0.1UF 20% 10V CERM 402
XDP C1800 0.1UF 20% 10V CERM 402
XDP R1831 1K 5% 1/16W MF-LF 402
XDP C1801 0.1UF 20% 10V CERM 402
XDP C1806 0.1UF 20% 10V CERM 402

R1820 51 5% 1/20W MF 201 PLACE_NEAR=J1800.51:5MM
R1823 51 5% 1/20W MF 201
R1824 51 5% 1/20W MF 201

XDP_CPU_TDO
XDP_CPU_TCK
XDP_CPU_TRST_L

TDI and TMS are terminated in CPU.

R1800 1K 5% 1/20W MF 201 PLACE_NEAR=U0500.AB35:16.5mm
CPU_PWRGD

R1802 0 5% 1/20W MF 0201
PM_PWRBTN_L

WF: SB DPDG says HOOK1 is BP_PWRGD_RST#

R1804 220 5% 1/20W MF 201
PM_PCH_SYS_PWROK

R1805 1K 5% 1/20W MF 201
CPU_RESET_L

CPU-PCH JTAG Chain Support

To link CPU and PCH JTAG pull ICT_JTAG_EN to 5V (must be in S0)

TP1845 TP-P6
ICT_JTAG_EN

Q1840 DMN5L06VK-7 SOT-563
Q1846 DMN5L06VK-7 SOT-563

XDP_CPU_TMS — XDP_CPU_PCH_TMS — XDP_PCH_TMS
PLACE_NEAR=J1800.57:5.08mm
PLACE_NEAR=J1850.57:6mm

TP1840 TP-P6

Q1840 DMN5L06VK-7 SOT-563
Q1846 DMN5L06VK-7 SOT-563

XDP_CPU_TCK — XDP_CPU_PCH_TCK — XDP_PCH_TCK
PLACE_NEAR=J1800.58:5.08mm
PLACE_NEAR=J1850.58:5.08mm

TP1841 TP-P6

Q1842 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
Q1848 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3

XDP_CPU_TDO — XDP_CPU_TDO_PCH_TDI — XDP_PCH_TDI
PLACE_NEAR=J1800.51:5.08mm
PLACE_NEAR=J1850.55:5.08mm

R1842 1M 5% 1/20W MF 201
R1841 1M 5% 1/20W MF 201
R1840 1M 5% 1/20W MF 201
R1845 1K 5% 1/20W MF 201

R1892 0 5% 1/16W MF-LF 402 NOSTUFF
=PP3V3_S5_XDP — PP3V3_S5_XDP_R
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
MAX_NECK_LENGTH=3MM

R1860 210 1% 1/20W MF 201
R1861 210 1% 1/20W MF 201
R1862 210 1% 1/20W MF 201

XDP_PCH_TDO — J1850.51:2.54mm
XDP_PCH_TDI — U1100.W39:4mm
XDP_PCH_TMS — U1100.W40:3.5mm
XDP_PCH_TCK

R1867 100 5% 1/20W MF 201 J1850.51:5mm
R1868 100 5% 1/20W MF 201 U1100.W39:21MM
R1869 100 5% 1/20W MF 201 U1100.W40:20MM
R1866 51 5% 1/20W MF 201

PCH SIGNALS

USB_EXTA_OC_L	R1890	SHORT	XDP_DA0_USB_EXTA_OC_L
USB_EXTC_OC_L	R1893	SHORT	XDP_DA1_USB_EXTC_OC_L
PCH_GPIO41	R1894	SHORT	XDP_DA2_PCH_GPIO41
PCH_GPIO42	R1895	SHORT	XDP_DA3_PCH_GPIO42
USB_EXTB_OC_L	R1880	SHORT	XDP_DB0_USB_EXTB_OC_L
USB_EXTD_OC_L	R1881	SHORT	XDP_DB1_USB_EXTD_OC_L
PCH_GPIO10	R1896	SHORT	XDP_DB2_PCH_GPIO10
SDCONN_STATE_CHANGE	R1897	SHORT	XDP_DB3_SDCONN_STATE_CHANGE_L
DP_AUXIO_EN	R1872	SHORT	XDP_DC0_DP_AUXCH_ISOL_L
SATARDRVR_EN	R1873	SHORT	XDP_DC1_SATARDRVR_EN
PCH_GPIO36	R1874	SHORT	XDP_DC2_PCH_GPIO36
JTAG_ISP_TCK	R1875	SHORT	XDP_DC3_JTAG_ISP_TCK
PCH_GPIO16	R1878	SHORT	XDP_DD0_PCH_GPIO16
PCH_GPIO49	R1879	SHORT	XDP_DD1_PCH_GPIO49
ENET_CLKREQ_L	R1882	SHORT	XDP_DD2_ENET_CLKREQ_L
AP_CLKREQ_L	R1883	SHORT	XDP_DD3_AP_CLKREQ_L
HDD_PWR_EN	R1886	SHORT	XDP_FC0_HDD_PWR_EN
GPU_GOOD	R1887	SHORT	XDP_FC1_GPU_GOOD

OMIT (All 18 R's)

XDP SIGNALS

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM

998-2516

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

OBSFN_A0	NC	OBSFN_C0	XDP_FC0_HDD_PWR_EN
OBSFN_A1	NC	OBSFN_C1	XDP_FC1_GPU_GOOD
XDP_DA0_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	XDP_DC0_DP_AUXCH_ISOL_L
XDP_DA1_USB_EXTC_OC_L	OBSDATA_A1	OBSDATA_C1	XDP_DC1_SATARDRVR_EN
XDP_DA2_PCH_GPIO41	OBSDATA_A2	OBSDATA_C2	XDP_DC2_PCH_GPIO36
XDP_DA3_PCH_GPIO42	OBSDATA_A3	OBSDATA_C3	XDP_DC3_JTAG_ISP_TCK
OBSFN_B0	NC	OBSFN_D0	NC
OBSFN_B1	NC	OBSFN_D1	NC
XDP_DB0_USB_EXTB_OC_L	OBSDATA_B0	OBSDATA_D0	XDP_DD0_PCH_GPIO16
XDP_DB1_USB_EXTD_OC_L	OBSDATA_B1	OBSDATA_D1	XDP_DD1_PCH_GPIO49
XDP_DB2_PCH_GPIO10	OBSDATA_B2	OBSDATA_D2	XDP_DD2_ENET_CLKREQ_L
XDP_DB3_SDCONN_STATE_CHANGE_L	OBSDATA_B3	OBSDATA_D3	XDP_DD3_AP_CLKREQ_L
	ITPCLK/HOOK4		
	ITPCLK#/HOOK5		
	VCC_OBS_CD		
XDP_PCH_S5_PWRGD	PWRGD/HOOK0	R1870 1K 5% 1/20W MF 201	XDP_PM_PCH_PWROK
XDP_PCH_PWRBTN_L	HOOK1		
	VCC_OBS_AB		
	HOOK2	RESET#/HOOK6	XDP_PM_PCH_PWROK
	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	TP_XDP_PCH_TRST_L
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS
	NC	XDP_PRESENT#	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP C1880 0.1UF 20% 10V CERM 402
XDP C1881 0.1UF 20% 10V CERM 402

R1830 150 5% 1/16W MF-LF 402
R1831 1K 5% 1/16W MF-LF 402

PM_RSMRST_PCH_L — R1884 1K 5% 1/20W MF 201 PLACE_NEAR=J1850.40:2.54mm
PM_PWRBTN_L — R1885 0 5% 1/20W MF 0201 PLACE_NEAR=U5000.J3:2.54mm

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

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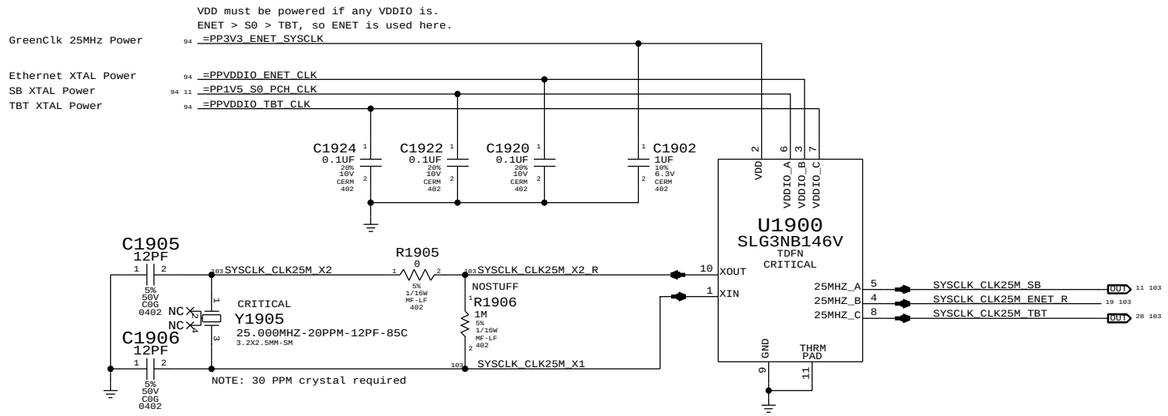
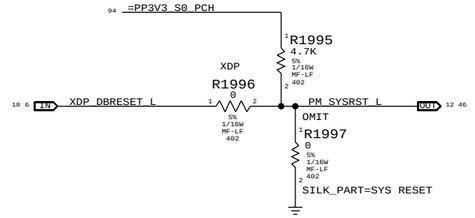
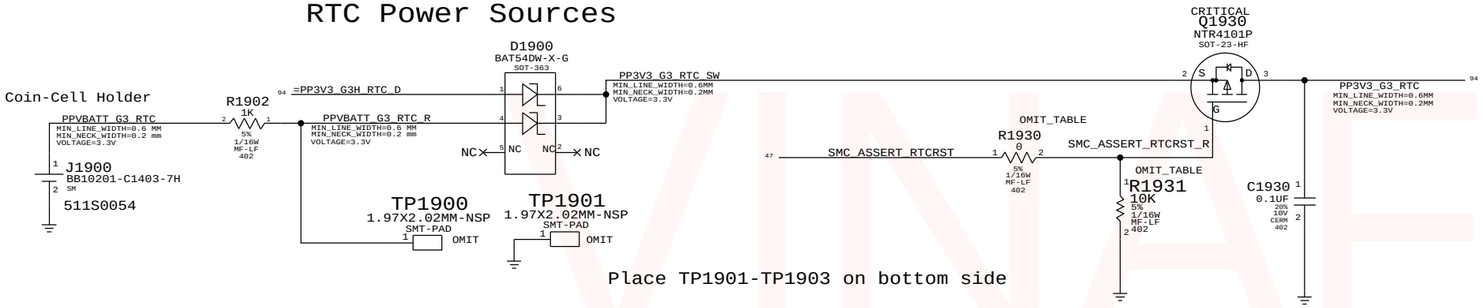
System 25MHz Clock Generator



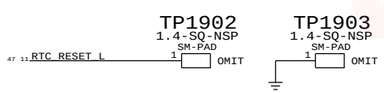
PCH Reset Button



RTC Power Sources

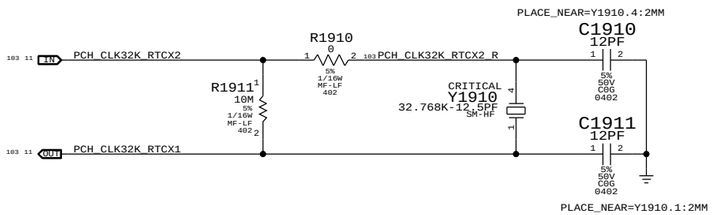


Place TP1901-TP1903 on bottom side



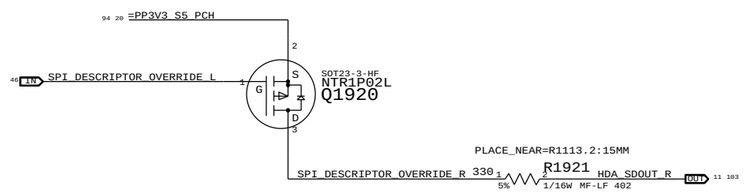
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0090	1	RES,10K OHM,402	R1930	RTCRST:Y
132S1059	1	CAP,0.1 UF,402	R1931	RTCRST:Y
116S0090	1	RES,10K OHM,402	R1931	RTCRST:N

PCH RTC Crystal

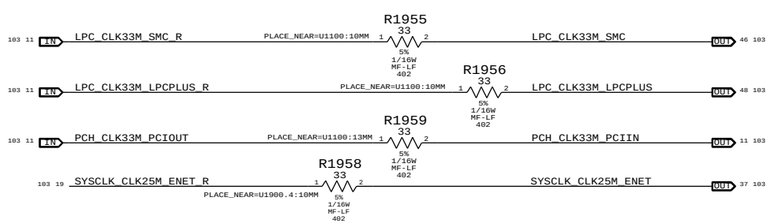


PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



Clock series termination



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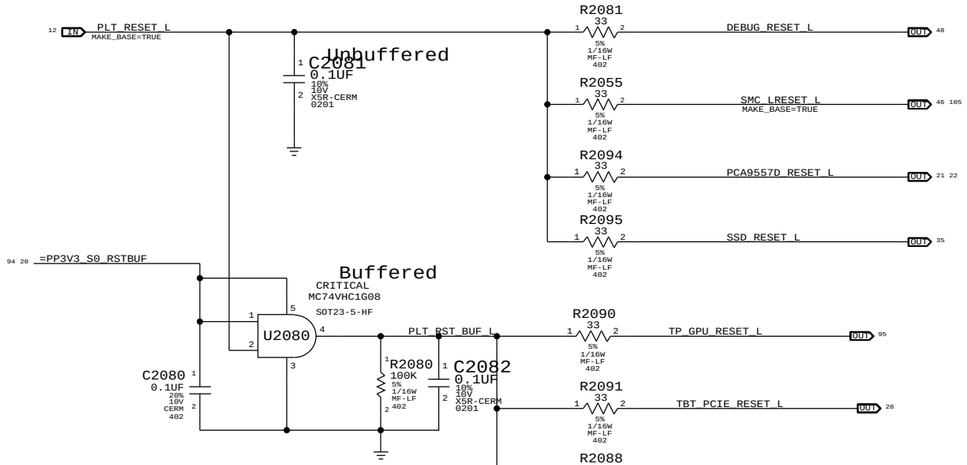
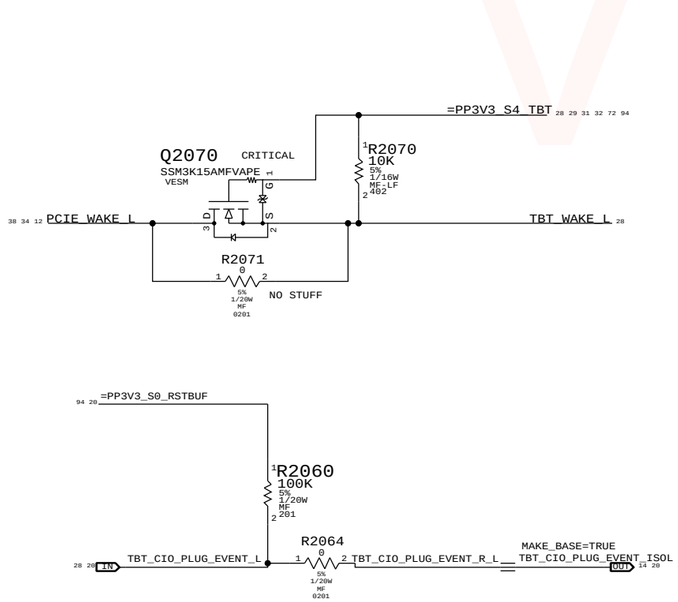
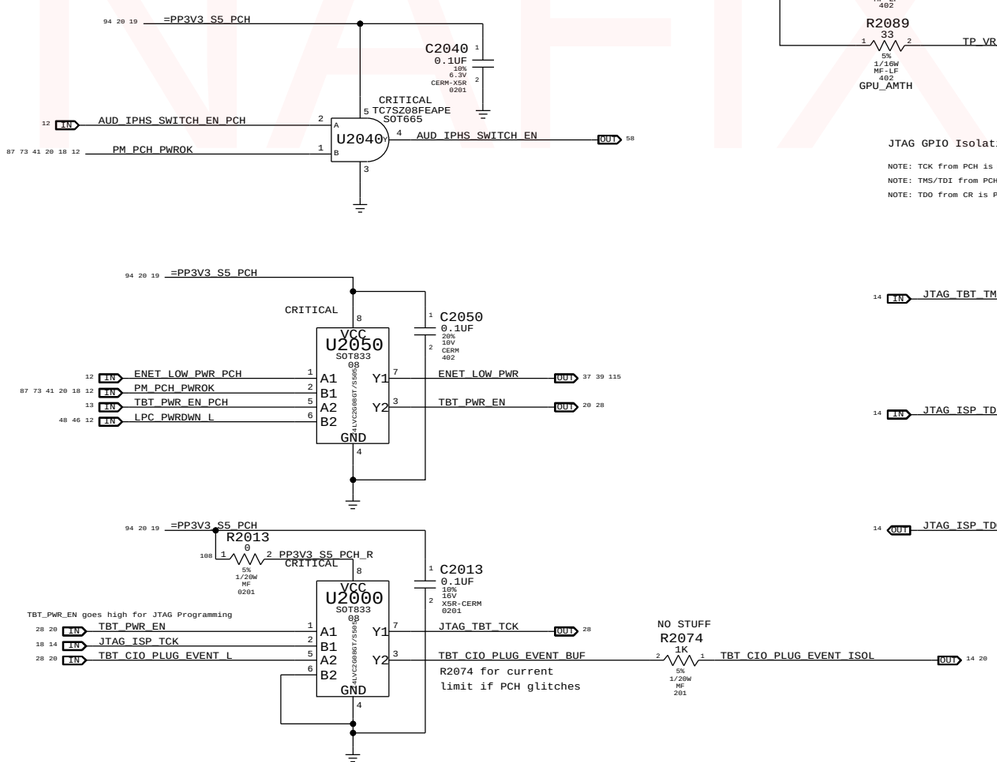
Platform Reset Connections



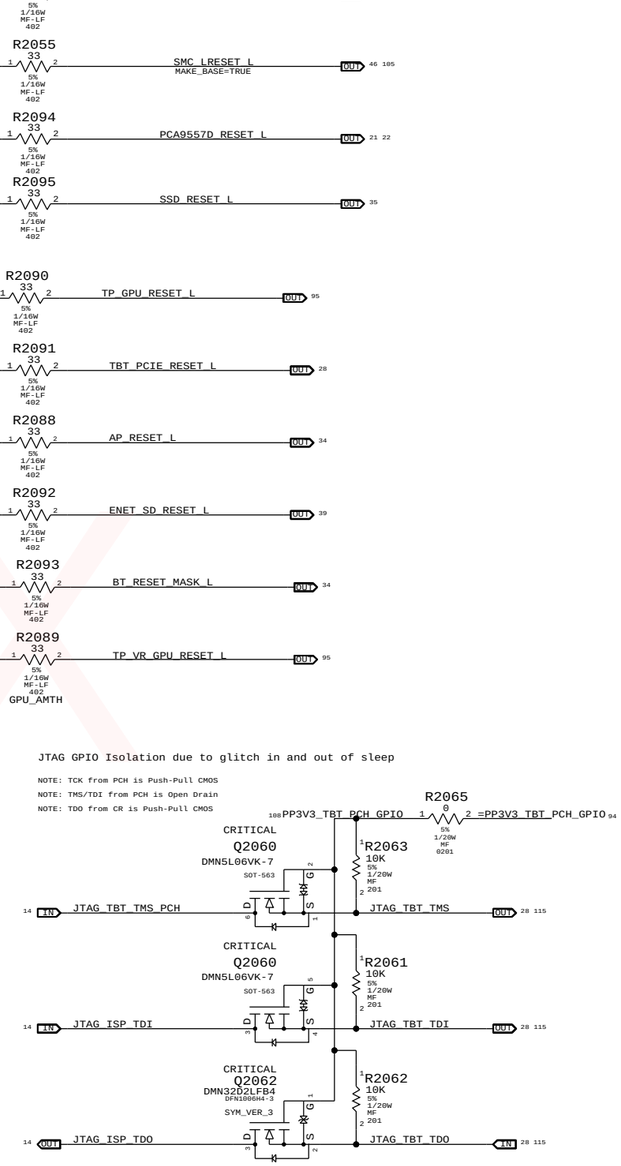
GPIO Glitch Prevention





JTAG GPIO Isolation due to glitch in and out of sleep

NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS



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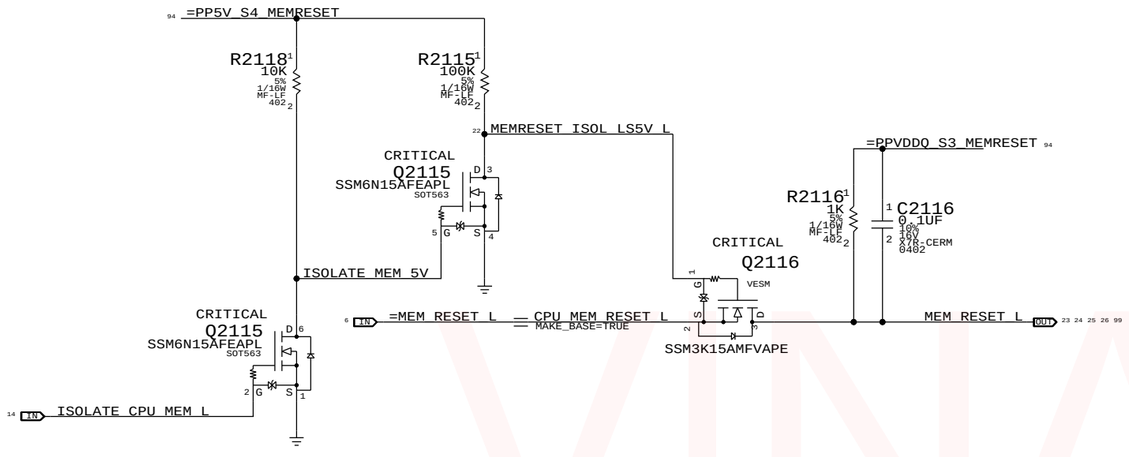
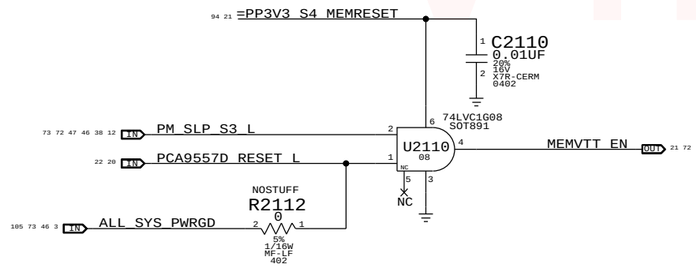
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

MEMVTT_EN = PLT_RESET_L * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L





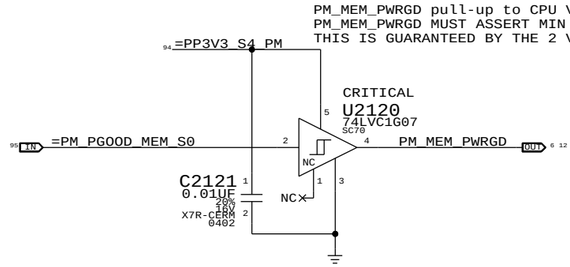
Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	1	1	1	1	CPU_MEM_RESET_L	1
1	0	1	1	1	1	1
to 2	0	0	1	1	1	0
S3 3	0	0	0	X	1	0
4	0	0	1	X	1	0
to 5	0	1	1	0 (*)	1	1
6	0	1	1	1	1	1
S0 7	1	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

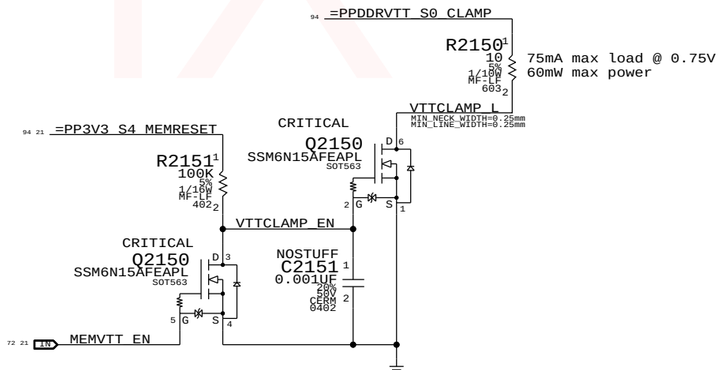
MEM S0 "PGOOD" FOR CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page
PM_MEM_PWRGD MUST ASSERT MIN 100 NS AFTER MEM_VDDQ RAMPS 80%
THIS IS GUARANTEED BY THE 2 V/MS RAMP RATE OF THE FET



MEMVTT Clamp

Ensures CKE signals are held low in S3



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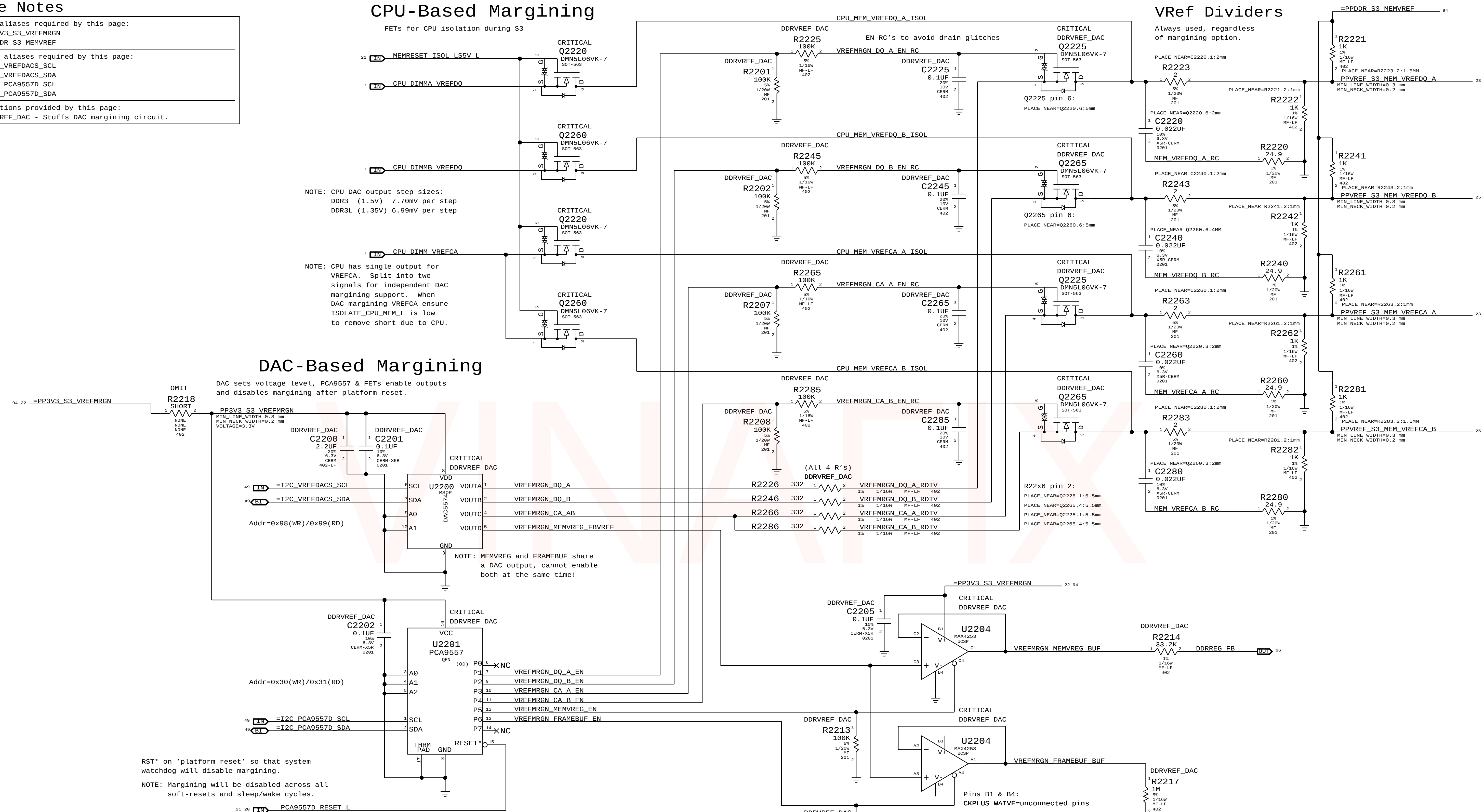
Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5

	DDR3 (1.5V)	DDR3L (1.35V)	DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)	0.675V (DAC: 0x34 = 0.670mV)	1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)	0.275V - 1.075V (+/- 400mV)	1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)	0.000V - 1.354V (0x00 - 0x69)	0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)	0.269V - 1.083V (+/- 406mV)	1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)	+811uA - -816uA (- = sourced)	+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output	7.67mV / step @ output	2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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PAGE TITLE

DDR3 VREF MARGINING

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

24 22 =PPVREF_S3_MEM_VREFDQ_A
VOLTAGE=0.75V

C2330 2.2UF 20% 6.3V CERM 402-LF
C2331 0.1UF 20% 10V CERM 402

J2300 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 1 OF 2 — CRITICAL

1	VREFDQ	2	VSS_0
3	VSS_1	4	DQ4
5	DQ0	6	DQ5
7	DQ1	8	VSS_2
9	VSS_3	10	DQS0*
11	DM0	12	DQS0
13	VSS_4	14	VSS_5
15	DQ2	16	DQ6
17	DQ3	18	DQ7
19	VSS_6	20	VSS_7
21	DQ8	22	DQ12
23	DQ9	24	DQ13
25	VSS_8	26	VSS_9
27	DQS1*	28	DM1
29	DQS1	30	RESET*
31	VSS_10	32	VSS_11
33	DQ10	34	DQ14
35	DQ11	36	DQ15
37	VSS_12	38	VSS_13
39	DQ16	40	DQ20
41	DQ17	42	DQ21
43	VSS_14	44	VSS_15
45	DQS2*	46	DM2
47	DQS2	48	VSS_16
49	VSS_17	50	DQ22
51	DQ18	52	DQ23
53	DQ19	54	VSS_18
55	VSS_19	56	DQ28
57	DQ24	58	DQ29
59	DQ25	60	VSS_20
61	VSS_21	62	DQS3*
63	DM3	64	DQS3
65	VSS_22	66	VSS_23
67	DQ26	68	DQ30
69	DQ27	70	DQ31
71	VSS_24	72	VSS_25
	KEY		
73	CKE0	74	CKE1
75	VDD_0	76	VDD_1
77	NC_0	78	A15
79	BA2	80	A14
81	VDD_2	82	VDD_3
83	A12/BC*	84	A11
85	A9	86	A7
87	VDD_4	88	VDD_5
89	A8	90	A6
91	A5	92	A4
93	VDD_6	94	VDD_7
95	A3	96	A2
97	A1	98	A0
99	VDD_8	100	VDD_9
101	CK0	102	CK1
103	CK0*	104	CK1*
105	VDD_10	106	VDD_11
107	A10_AP	108	BA1
109	BA0	110	RAS*
111	VDD_12	112	VDD_13
113	WE*	114	S0*
115	CAS*	116	ODT0
117	VDD_14	118	VDD_15
119	A13	120	ODT1
121	S1*	122	NC_1
123	VDD_16	124	VDD_17
125	TEST	126	VREFCA
127	VSS_26	128	VSS_27
129	DQ32	130	DQ36
131	DQ33	132	DQ37
133	VSS_28	134	VSS_29
135	DQS4*	136	DM4
137	DQS4	138	VSS_30
139	VSS_31	140	DQ38
141	DQ34	142	DQ39
143	DQ35	144	VSS_32
145	VSS_33	146	DQ44
147	DQ40	148	DQ45
149	DQ41	150	VSS_34
151	VSS_35	152	DQS5*
153	DM5	154	DQS5
155	VSS_36	156	VSS_37
157	DQ42	158	DQ46
159	DQ43	160	DQ47
161	VSS_38	162	VSS_39
163	DQ48	164	DQ52
165	DQ49	166	DQ53
167	VSS_40	168	VSS_41
169	DQS6*	170	DM6
171	DQS6	172	VSS_42
173	VSS_43	174	DQ54
175	DQ50	176	DQ55
177	DQ51	178	VSS_44
179	VSS_45	180	DQ60
181	DQ56	182	DQ61
183	DQ57	184	VSS_46
185	VSS_47	186	DQS7*
187	DM7	188	DQS7
189	VSS_48	190	VSS_49
191	DQ58	192	DQ62
193	DQ59	194	DQ63
195	VSS_50	196	VSS_51
197	SA0	198	EVENT*
199	VDDSPD	200	SDA
201	SA1	202	SCL
203	VTT_0	204	VTT_1

SODIMM-P0.60-D8 SYM 1 OF 2

=MEM_A_DQ<0> / =MEM_A_DQ<1>
=MEM_A_DQ<2> / =MEM_A_DQ<3>
=MEM_A_DQ<8> / =MEM_A_DQ<9>
=MEM_A_DQS_N<1> / =MEM_A_DQS_P<1>
=MEM_A_DQ<10> / =MEM_A_DQ<11>
=MEM_A_DQ<16> / =MEM_A_DQ<17>
=MEM_A_DQS_N<2> / =MEM_A_DQS_P<2>
=MEM_A_DQ<18> / =MEM_A_DQ<19>
=MEM_A_DQ<24> / =MEM_A_DQ<25>
=MEM_A_DQ<26> / =MEM_A_DQ<27>
=MEM_A_DQ<32> / =MEM_A_DQ<33>
=MEM_A_DQS_N<4> / =MEM_A_DQS_P<4>
=MEM_A_DQ<34> / =MEM_A_DQ<35>
=MEM_A_DQ<40> / =MEM_A_DQ<41>
=MEM_A_DQ<42> / =MEM_A_DQ<43>
=MEM_A_DQ<48> / =MEM_A_DQ<49>
=MEM_A_DQS_N<6> / =MEM_A_DQS_P<6>
=MEM_A_DQ<50> / =MEM_A_DQ<51>
=MEM_A_DQ<56> / =MEM_A_DQ<57>
=MEM_A_DQ<58> / =MEM_A_DQ<59>

SODIMM-P0.60-D8 SYM 2 OF 2

=MEM_A_DQ<4> / =MEM_A_DQ<5>
=MEM_A_DQS_N<0> / =MEM_A_DQS_P<0>
=MEM_A_DQ<6> / =MEM_A_DQ<7>
=MEM_A_DQ<12> / =MEM_A_DQ<13>
MEM_RESET_L
=MEM_A_DQ<14> / =MEM_A_DQ<15>
=MEM_A_DQ<20> / =MEM_A_DQ<21>
=MEM_A_DQ<22> / =MEM_A_DQ<23>
=MEM_A_DQ<28> / =MEM_A_DQ<29>
=MEM_A_DQS_N<3> / =MEM_A_DQS_P<3>
=MEM_A_DQ<30> / =MEM_A_DQ<31>
MEM_A_CKE<1>
=MEM_A_DQ<36> / =MEM_A_DQ<37>
=MEM_A_DQ<38> / =MEM_A_DQ<39>
=MEM_A_DQ<44> / =MEM_A_DQ<45>
=MEM_A_DQS_N<5> / =MEM_A_DQS_P<5>
=MEM_A_DQ<46> / =MEM_A_DQ<47>
=MEM_A_DQ<52> / =MEM_A_DQ<53>
=MEM_A_DQ<54> / =MEM_A_DQ<55>
=MEM_A_DQ<60> / =MEM_A_DQ<61>
=MEM_A_DQS_N<7> / =MEM_A_DQS_P<7>
=MEM_A_DQ<62> / =MEM_A_DQ<63>
MEM_EVENT_L
=I2C_SODIMMA_SDA
=I2C_SODIMMA_SCL

P/N: 516S1019

J2300 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 2 OF 2
MTG HOLE: 205, 206, 207, 208, 209

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

94 24 23 =PPVDDQ_S3_MEM_A
C2310 C2311 C2312 C2313 C2314 C2315 C2316 C2317 0.1UF 20% 10V CERM 402
C2300 C2301 10UF 20% 6.3V X5R 603
C2318 C2319 C2320 C2321 C2322 C2323 0.1UF 20% 10V CERM 402

=PPVDDQ_S3_MEM_A 23 24 94

23 MEM_DIMM0_SA<1>
23 MEM_DIMM0_SA<0>
94 24 23 =PP3V3_S0_MEM_A_SPD
C2340 2.2UF 20% 6.3V CERM 402-LF
R2340 10K 5% 1/16W MF-LF 402
R2341 10K 5% 1/16W MF-LF 402

94 24 23 =PPDDRVTT_S0_MEM_A

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 10V CERM 402
PPVREF_S3_MEM_VREFCA_A 22 24
VOLTAGE=0.75V

=PPDDRVTT_S0_MEM_A 23 24 94
C2350 C2351 C2352 C2353 1UF 10% 10V X5R 402

SYNC_MASTER=J78_MLB	SYNC_DATE=02/21/2012
PAGE TITLE	DDR3 SO-DIMM Connector A Slot0
Apple Inc.	DRAWING NUMBER 051-XXXX; SIZE D
	REVISION 5.0.0
	BRANCH proto2
	PAGE 23 OF 137
	SHEET 23 OF 115

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

J2400
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 1 OF 2

J2400
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2

1	VREFDQ		2	VSS_0			
3	VSS_1	CRITICAL	4	DQ4	=MEM_A_DQ<4>	BI	23 27
5	DQ0	=MEM_A_DQ<0> BI 23 27	6	DQ5	=MEM_A_DQ<5>	BI	23 27
7	DQ1	=MEM_A_DQ<1> BI 23 27	8	VSS_2			
9	VSS_3		10	DQS0*	=MEM_A_DQS_N<0>	BI	23 27
11	DM0		12	DQS0	=MEM_A_DQS_P<0>	BI	23 27
13	VSS_4		14	VSS_5			
15	DQ2	=MEM_A_DQ<2> BI 23 27	16	DQ6	=MEM_A_DQ<6>	BI	23 27
17	DQ3	=MEM_A_DQ<3> BI 23 27	18	DQ7	=MEM_A_DQ<7>	BI	23 27
19	VSS_6		20	VSS_7			
21	DQ8	=MEM_A_DQ<8> BI 23 27	22	DQ12	=MEM_A_DQ<12>	BI	23 27
23	DQ9	=MEM_A_DQ<9> BI 23 27	24	DQ13	=MEM_A_DQ<13>	BI	23 27
25	VSS_8		26	VSS_9			
27	DQS1*	=MEM_A_DQS_N<1> BI 23 27	28	DM1			
29	DQS1	=MEM_A_DQS_P<1> BI 23 27	30	RESET*	MEM_RESET_L	IN	21 23 25 26 99
31	VSS_10		32	VSS_11			
33	DQ10	=MEM_A_DQ<10> BI 23 27	34	DQ14	=MEM_A_DQ<14>	BI	23 27
35	DQ11	=MEM_A_DQ<11> BI 23 27	36	DQ15	=MEM_A_DQ<15>	BI	23 27
37	VSS_12		38	VSS_13			
39	DQ16	=MEM_A_DQ<16> BI 23 27	40	DQ20	=MEM_A_DQ<20>	BI	23 27
41	DQ17	=MEM_A_DQ<17> BI 23 27	42	DQ21	=MEM_A_DQ<21>	BI	23 27
43	VSS_14		44	VSS_15			
45	DQS2*	=MEM_A_DQS_N<2> BI 23 27	46	DM2			
47	DQS2	=MEM_A_DQS_P<2> BI 23 27	48	VSS_16			
49	VSS_17		50	DQ22	=MEM_A_DQ<22>	BI	23 27
51	DQ18	=MEM_A_DQ<18> BI 23 27	52	DQ23	=MEM_A_DQ<23>	BI	23 27
53	DQ19	=MEM_A_DQ<19> BI 23 27	54	VSS_18			
55	VSS_19		56	DQ28	=MEM_A_DQ<28>	BI	23 27
57	DQ24	=MEM_A_DQ<24> BI 23 27	58	DQ29	=MEM_A_DQ<29>	BI	23 27
59	DQ25	=MEM_A_DQ<25> BI 23 27	60	VSS_20			
61	VSS_21		62	DQS3*	=MEM_A_DQS_N<3>	BI	23 27
63	DM3		64	DQS3	=MEM_A_DQS_P<3>	BI	23 27
65	VSS_22		66	VSS_23			
67	DQ26	=MEM_A_DQ<26> BI 23 27	68	DQ30	=MEM_A_DQ<30>	BI	23 27
69	DQ27	=MEM_A_DQ<27> BI 23 27	70	DQ31	=MEM_A_DQ<31>	BI	23 27
71	VSS_24	KEY	72	VSS_25			
73	CKE0	MEM_A_CKE<2> IN 7 99	74	CKE1	MEM_A_CKE<3>	IN	7 99
75	VDD_0		76	VDD_1			
77	NC_0	NCX	78	A15	MEM_A_A<15>	IN	7 23 99
79	BA2	MEM_A_BA<2> IN 7 23 99	80	A14	MEM_A_A<14>	IN	7 23 99
81	VDD_2		82	VDD_3			
83	A12/BC*	MEM_A_A<12> IN 7 23 99	84	A11	MEM_A_A<11>	IN	7 23 99
85	A9	MEM_A_A<9> IN 7 23 99	86	A7	MEM_A_A<7>	IN	7 23 99
87	VDD_4		88	VDD_5			
89	A8	MEM_A_A<8> IN 7 23 99	90	A6	MEM_A_A<6>	IN	7 23 99
91	A5	MEM_A_A<5> IN 7 23 99	92	A4	MEM_A_A<4>	IN	7 23 99
93	VDD_6		94	VDD_7			
95	A3	MEM_A_A<3> IN 7 23 99	96	A2	MEM_A_A<2>	IN	7 23 99
97	A1	MEM_A_A<1> IN 7 23 99	98	A0	MEM_A_A<0>	IN	7 23 99
99	VDD_8		100	VDD_9			
101	CK0	MEM_A_CLK_P<2> IN 7 99	102	CK1	MEM_A_CLK_P<3>	IN	7 99
103	CK0*	MEM_A_CLK_N<2> IN 7 99	104	CK1*	MEM_A_CLK_N<3>	IN	7 99
105	VDD_10		106	VDD_11			
107	A10_AP	MEM_A_A<10> IN 7 23 99	108	BA1	MEM_A_BA<1>	IN	7 23 99
109	BA0	MEM_A_BA<0> IN 7 23 99	110	RAS*	MEM_A_RAS_L	IN	7 23 99
111	VDD_12		112	VDD_13			
113	WE*	MEM_A_WE_L IN 7 23 99	114	S0*	MEM_A_CS_L<2>	IN	7 99
115	CAS*	MEM_A_CAS_L IN 7 23 99	116	ODT0	MEM_A_ODT<2>	IN	7 99
117	VDD_14		118	VDD_15			
119	A13	MEM_A_A<13> IN 7 23 99	120	ODT1	MEM_A_ODT<3>	IN	7 99
121	S1*	MEM_A_CS_L<3> IN 7 99	122	NC_1	NCX		
123	VDD_16		124	VDD_17			
125	TEST	NCX	126	VREFCA	PPVREF_S3_MEM_VREFCA_A 22 23 VOLTAGE=0.75V		
127	VSS_26		128	VSS_27			
129	DQ32	=MEM_A_DQ<32> BI 23 27	130	DQ36	=MEM_A_DQ<36>	BI	23 27
131	DQ33	=MEM_A_DQ<33> BI 23 27	132	DQ37	=MEM_A_DQ<37>	BI	23 27
133	VSS_28		134	VSS_29			
135	DQS4*	=MEM_A_DQS_N<4> BI 23 27	136	DM4			
137	DQS4	=MEM_A_DQS_P<4> BI 23 27	138	VSS_30			
139	VSS_31		140	DQ38	=MEM_A_DQ<38>	BI	23 27
141	DQ34	=MEM_A_DQ<34> BI 23 27	142	DQ39	=MEM_A_DQ<39>	BI	23 27
143	DQ35	=MEM_A_DQ<35> BI 23 27	144	VSS_32			
145	VSS_33		146	DQ44	=MEM_A_DQ<44>	BI	23 27
147	DQ40	=MEM_A_DQ<40> BI 23 27	148	DQ45	=MEM_A_DQ<45>	BI	23 27
149	DQ41	=MEM_A_DQ<41> BI 23 27	150	VSS_34			
151	VSS_35		152	DQS5*	=MEM_A_DQS_N<5>	BI	23 27
153	DM5		154	DQS5	=MEM_A_DQS_P<5>	BI	23 27
155	VSS_36		156	VSS_37			
157	DQ42	=MEM_A_DQ<42> BI 23 27	158	DQ46	=MEM_A_DQ<46>	BI	23 27
159	DQ43	=MEM_A_DQ<43> BI 23 27	160	DQ47	=MEM_A_DQ<47>	BI	23 27
161	VSS_38		162	VSS_39			
163	DQ48	=MEM_A_DQ<48> BI 23 27	164	DQ52	=MEM_A_DQ<52>	BI	23 27
165	DQ49	=MEM_A_DQ<49> BI 23 27	166	DQ53	=MEM_A_DQ<53>	BI	23 27
167	VSS_40		168	VSS_41			
169	DQS6*	=MEM_A_DQS_N<6> BI 23 27	170	DM6			
171	DQS6	=MEM_A_DQS_P<6> BI 23 27	172	VSS_42			
173	VSS_43		174	DQ54	=MEM_A_DQ<54>	BI	23 27
175	DQ50	=MEM_A_DQ<50> BI 23 27	176	DQ55	=MEM_A_DQ<55>	BI	23 27
177	DQ51	=MEM_A_DQ<51> BI 23 27	178	VSS_44			
179	VSS_45		180	DQ60	=MEM_A_DQ<60>	BI	23 27
181	DQ56	=MEM_A_DQ<56> BI 23 27	182	DQ61	=MEM_A_DQ<61>	BI	23 27
183	DQ57	=MEM_A_DQ<57> BI 23 27	184	VSS_46			
185	VSS_47		186	DQS7*	=MEM_A_DQS_N<7>	BI	23 27
187	DM7		188	DQS7	=MEM_A_DQS_P<7>	BI	23 27
189	VSS_48		190	VSS_49			
191	DQ58	=MEM_A_DQ<58> BI 23 27	192	DQ62	=MEM_A_DQ<62>	BI	23 27
193	DQ59	=MEM_A_DQ<59> BI 23 27	194	DQ63	=MEM_A_DQ<63>	BI	23 27
195	VSS_50		196	VSS_51			
197	SA0	MEM_DIMM1_SA<0> 24	198	EVENT*	MEM_EVENT_L	OUT	23 25 26 46 47
199	VDDSPD	=PP3V3_S0_MEM_A SPD 94 24 23	200	SDA	=I2C_SODIMMA_SDA	BI	23 49
201	SA1	MEM_DIMM1_SA<1> 24	202	SCL	=I2C_SODIMMA_SCL	IN	23 49
203	VTT_0		204	VTT_1			

C2410	0.1UF	20% 10V X5R 402	C2411	0.1UF	20% 10V X5R 402	C2412	0.1UF	20% 10V X5R 402	
C2413	0.1UF	20% 10V X5R 402	C2414	0.1UF	20% 10V X5R 402	C2415	0.1UF	20% 10V X5R 402	
C2416	0.1UF	20% 10V X5R 402	C2417	0.1UF	20% 10V X5R 402				
C2400	10UF	20% 6.3V X5R 603	C2401	10UF	20% 6.3V X5R 603	C2418	0.1UF	20% 10V X5R 402	
C2419	0.1UF	20% 10V X5R 402	C2420	0.1UF	20% 10V X5R 402	C2421	0.1UF	20% 10V X5R 402	
C2422	0.1UF	20% 10V X5R 402	C2423	0.1UF	20% 10V X5R 402				
C2430	2.2UF	20% 6.3V X5R 402-LF	C2431	0.1UF	20% 10V X5R 402				
C2435	2.2UF	20% 6.3V X5R 402-LF	C2436	0.1UF	20% 10V X5R 402				
C2440	2.2UF	20% 6.3V X5R 402-LF	R2440	10K	5% 1/16W ME-LF 402	R2441	10K	5% 1/16W ME-LF 402	
C2450	1UF	10% 10V X5R 402	C2451	1UF	10% 10V X5R 402	C2452	1UF	10% 10V X5R 402	C2453 1UF 10% 10V X5R 402

94 24 23 =PPVDDQ_S3_MEM_A
=PPVDDQ_S3_MEM_A 23 24 94
94 24 23 =PP3V3_S0_MEM_A_SPD
24 MEM_DIMM1_SA<0>
24 MEM_DIMM1_SA<1>
94 24 23 =PP3V3_S0_MEM_A_SPD
94 24 23 =PPDDRVTT_S0_MEM_A
=PPDDRVTT_S0_MEM_A 23 24 94

SYNC_MASTER=J78 MLB	SYNC_DATE=02/21/2012
PAGE TITLE	DDR3 SO-DIMM Connector A Slot1
Apple Inc.	DRAWING NUMBER 051-XXXX; SIZE D
	REVISION 5.0.0
	BRANCH proto2
	PAGE 24 OF 137
	SHEET 24 OF 115

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

PPVREF_S3_MEM_VREFDQ_B
VOLTAGE=0.75V

C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 0.1UF 20% 10V CERM 402

J2500
CRITICAL
F-ANG-SM-1
SODIMM-P0.60-D8
SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
NCX 77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	2 NC	124
NCX 125	TEST	VDD_17	126
127	VSS_26	VREFCA	128
129	DQ32	VSS_27	130
131	DQ33	DQ36	132
133	VSS_28	DQ37	134
135	DQS4*	VSS_29	136
137	DQS4	DM4	138
139	VSS_31	VSS_30	140
141	DQ34	DQ38	142
143	DQ35	DQ39	144
145	VSS_33	VSS_32	146
147	DQ40	DQ44	148
149	DQ41	DQ45	150
151	VSS_35	VSS_34	152
153	DM5	DQS5*	154
155	VSS_36	DQS5	156
157	DQ42	VSS_37	158
159	DQ43	DQ46	160
161	VSS_38	DQ47	162
163	DQ48	VSS_39	164
165	DQ49	DQ52	166
167	VSS_40	DQ53	168
169	DQS6*	VSS_41	170
171	DQS6	DM6	172
173	VSS_43	VSS_42	174
175	DQ50	DQ54	176
177	DQ51	DQ55	178
179	VSS_45	VSS_44	180
181	DQ56	DQ60	182
183	DQ57	DQ61	184
185	VSS_47	VSS_46	186
187	DM7	DQS7*	188
189	VSS_48	DQS7	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

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SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402
C2514 0.1UF 20% 10V CERM 402
C2515 0.1UF 20% 10V CERM 402
C2516 0.1UF 20% 10V CERM 402
C2517 0.1UF 20% 10V CERM 402
C2500 10UF 20% 6.3V X5R 603
C2501 10UF 20% 6.3V X5R 603
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402
C2520 0.1UF 20% 10V CERM 402
C2521 0.1UF 20% 10V CERM 402
C2522 0.1UF 20% 10V CERM 402
C2523 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD
R2541 10K 5% 1/16W MF-LF 402
MEM_DIMM2_SA<1>
MEM_DIMM2_SA<0>
=PP3V3_S0_MEM_B_SPD
C2540 2.2UF 20% 6.3V CERM 402-LF
R2540 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_B
C2550 1UF 10% 10V X5R 402
C2551 1UF 10% 10V X5R 402
C2552 1UF 10% 10V X5R 402
C2553 1UF 10% 10V X5R 402

PPVREF_S3_MEM_VREFCA_B
VOLTAGE=0.75V
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 0.1UF 20% 10V CERM 402

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=MEM_B_DQ<62>	=MEM_B_DQ<63>
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=I2C_SODIMMB_SDA	
=I2C_SODIMMB_SCL	

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MEM_B_A<12>	MEM_B_A<11>
MEM_B_A<9>	MEM_B_A<7>
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MEM_B_CLK_N<0>	MEM_B_CLK_N<1>
MEM_B_A<10>	MEM_B_BA<1>
MEM_B_BA<0>	MEM_B_RAS_L
MEM_B_WE_L	MEM_B_CS_L<0>
MEM_B_CAS_L	MEM_B_ODT<0>
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MEM_B_CS_L<1>	

=PPVDDQ_S3_MEM_B	=PPVDDQ_S3_MEM_B
=PPDDRVTT_S0_MEM_B	=PPDDRVTT_S0_MEM_B

SYNC_MASTER=J78_MLB	SYNC_DATE=02/21/2014
PAGE TITLE	DDR3 SO-DIMM CONNECTOR B SLOT0
Apple Inc.	DRAWING NUMBER 051-XXXX; SIZE D
	REVISION 5.0.0
	BRANCH proto2
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	SHEET 25 OF 115

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

PPVREF_S3_MEM_VREFDQ_B
VOLTAGE=0.75V

C2630 2.2UF 20% 6.3V CERM 402-LF
C2631 0.1UF 20% 10V CERM 402

=PPVDDQ_S3_MEM_B

C2610 0.1UF 20% 10V CERM 402
C2611 0.1UF 20% 10V CERM 402
C2612 0.1UF 20% 10V CERM 402
C2613 0.1UF 20% 10V CERM 402
C2614 0.1UF 20% 10V CERM 402
C2615 0.1UF 20% 10V CERM 402
C2616 0.1UF 20% 10V CERM 402
C2617 0.1UF 20% 10V CERM 402

C2600 10UF 20% 6.3V X6S 603
C2601 10UF 20% 6.3V X6S 603
C2618 0.1UF 20% 10V CERM 402
C2619 0.1UF 20% 10V CERM 402
C2620 0.1UF 20% 10V CERM 402
C2621 0.1UF 20% 10V CERM 402
C2622 0.1UF 20% 10V CERM 402
C2623 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD

R2641 10K 5% 1/16W 0402-LF 402
R2640 10K 5% 1/16W 0402-LF 402

MEM_DIMM3_SA<1>
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=PP3V3_S0_MEM_B_SPD

C2640 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVTT_S0_MEM_B

J2600
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 1 OF 2
CRITICAL

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
NCX 77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1 2XNC	122
123	VDD_16	VDD_17	124
NCX 125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
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133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

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MEM_EVENT_L
=I2C_SODIMMB_SDA
=I2C_SODIMMB_SCL

=PPVDDQ_S3_MEM_B

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SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

PPVREF_S3_MEM_VREFCA_B
VOLTAGE=0.75V

C2635 2.2UF 20% 6.3V CERM 402-LF
C2636 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B

C2650 1UF 10% 10V X5R 402
C2651 1UF 10% 10V X5R 402
C2652 1UF 10% 10V X5R 402
C2653 1UF 10% 10V X5R 402

SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B SLOT1

Apple Inc.

DRAWING NUMBER 051-XXXX
SIZE D
REVISION 5.0.0
BRANCH proto2
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THERE ARE NO PIN SWAPS

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MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	MEM_B_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	MEM_B_DQS_P<5>
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	MEM_B_DQ<47>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	MEM_B_DQ<46>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	MEM_B_DQ<45>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	MEM_B_DQ<44>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	MEM_B_DQ<43>
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	MEM_B_DQ<42>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	MEM_B_DQ<41>
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	MEM_B_DQ<40>
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	MEM_B_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	MEM_B_DQS_P<6>
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	MEM_B_DQ<55>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	MEM_B_DQ<54>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	MEM_B_DQ<53>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	MEM_B_DQ<52>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	MEM_B_DQ<51>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	MEM_B_DQ<50>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	MEM_B_DQ<49>
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	MEM_B_DQ<48>
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	MEM_B_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	MEM_B_DQS_P<7>
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	MEM_B_DQ<63>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	MEM_B_DQ<62>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	MEM_B_DQ<61>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	MEM_B_DQ<60>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	MEM_B_DQ<59>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	MEM_B_DQ<58>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	MEM_B_DQ<57>
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	MEM_B_DQ<56>

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DDR3 ALIASES AND BITSWAPS

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CRITICAL
OMIT_TABLE

U2800
REDWOOD-RIDGE
FCBGA
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PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9	PERP_0	PETP_0	AD5 PCIE_TBT_D2R_C_P<0> C2840 0.1UF PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10	PERN_0	PETN_0	AD7 PCIE_TBT_D2R_C_N<0> C2841 0.1UF PCIE_TBT_D2R_N<0>
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12	PERP_1	PETP_1	AD9 PCIE_TBT_D2R_C_P<1> C2842 0.1UF PCIE_TBT_D2R_P<1>
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13	PERN_1	PETN_1	AD11 PCIE_TBT_D2R_C_N<1> C2843 0.1UF PCIE_TBT_D2R_N<1>
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15	PERP_2	PETP_2	AD13 PCIE_TBT_D2R_C_P<2> C2844 0.1UF PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16	PERN_2	PETN_2	AD15 PCIE_TBT_D2R_C_N<2> C2845 0.1UF PCIE_TBT_D2R_N<2>
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18	PERP_3	PETP_3	AD17 PCIE_TBT_D2R_C_P<3> C2846 0.1UF PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19	PERN_3	PETN_3	AD19 PCIE_TBT_D2R_C_N<3> C2847 0.1UF PCIE_TBT_D2R_N<3>

TBT_PCIE_RESET_L	P5	PERST_OD_N
TBT_PWR_ON_POC_RST_L	R4	PWR_ON_POC_RSTN

MISC

TP_TBT_MONDC0	AD23	MONDC0	
TP_TBT_MONDC1	AC24	MONDC1	
DEBUG: For monitoring current/voltage			
TBT_MONOBSP	W18	MONOBSP	
TBT_MONOBSN	W16	MONOBSN	
DEBUG: For monitoring clock			
TP_TBT_THERM_DP (Use AA8 GND ball for THERM_DN)	AB7	THERMDA	
TBT_SPI_MOSI	AA2	EE_DI	
TBT_SPI_MISO	Y3	EE_DO	
TBT_SPI_CS_L	T5	EE_CS_N	
TBT_SPI_CLK	U8	EE_CLK	
JTAG_TBT_TDI	W2	TDI	
JTAG_TBT_TMS	AB1	TMS	
JTAG_TBT_TCK	AA6	TCK	
JTAG_TBT_TDO	U6	TDO	
TBT_TEST_EN	R6	TEST_EN	
TBT_TEST_PWR_GOOD	W8	TEST_PWR_GOOD	

RSENSE	U20	TBT_RSENSE
RBIAS	W20	TBT_RBIAS
RSVD	AD1, L8	

R2855 1K 1% 1/20W MF 201

Used for straps in host mode

PCIE_RST_0_N	W6	TP_TBT_PCIE_RESET0_L
PCIE_RST_1_N	AB3	TBT_DFT_STRAP_1
PCIE_RST_2_N	AD3	TBT_ROM_SECURITY_XOR
PCIE_RST_3_N	V1	TBT_DFT_STRAP_3
PCIE_CLKREQ_OD_N	V3	TBT_CLKREQ_L
REFCLK_100_IN_P	AB21	PCIE_CLK100M_TBT_P
REFCLK_100_IN_N	AD21	PCIE_CLK100M_TBT_N
XTAL_25_IN	AA24	SYSCLK_CLK25M_TBT_R
XTAL_25_OUT	AB23	TP_TBT_XTAL25OUT
TMU_CLK_OUT	AA4	TBT_TMU_CLK_OUT

DISPLAY PORTS

DP_TBTSNK0_ML_P<3>	E14	DPSNK0_3_P
DP_TBTSNK0_ML_N<3>	D13	DPSNK0_3_N
DP_TBTSNK0_ML_P<2>	E16	DPSNK0_2_P
DP_TBTSNK0_ML_N<2>	D15	DPSNK0_2_N
DP_TBTSNK0_ML_P<1>	E18	DPSNK0_1_P
DP_TBTSNK0_ML_N<1>	D17	DPSNK0_1_N
DP_TBTSNK0_ML_P<0>	E20	DPSNK0_0_P
DP_TBTSNK0_ML_N<0>	D19	DPSNK0_0_N
DP_TBTSNK0_AUXCH_P	G4	DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N	G2	DPSNK0_AUX_N
DP_TBTSNK0_HPD	AB5	DPSNK0_HPD
DP_TBTSNK1_ML_P<3>	E6	DPSNK1_3_P
DP_TBTSNK1_ML_N<3>	D5	DPSNK1_3_N
DP_TBTSNK1_ML_P<2>	E8	DPSNK1_2_P
DP_TBTSNK1_ML_N<2>	D7	DPSNK1_2_N
DP_TBTSNK1_ML_P<1>	E10	DPSNK1_1_P
DP_TBTSNK1_ML_N<1>	D9	DPSNK1_1_N
DP_TBTSNK1_ML_P<0>	E12	DPSNK1_0_P
DP_TBTSNK1_ML_N<0>	D11	DPSNK1_0_N
DP_TBTSNK1_AUXCH_P	H3	DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N	H1	DPSNK1_AUX_N
DP_TBTSNK1_HPD	U4	DPSNK1_HPD

TBT_A_R2D_C_P<0>	G24	PA_CIO0_TX_P/DPSRC_0_P	PB_CIO2_TX_P/DPSRC_0_P
TBT_A_R2D_C_N<0>	E24	PA_CIO0_TX_N/DPSRC_0_N	PB_CIO2_TX_N/DPSRC_0_N
TBT_A_D2R_P<0>	G22	PA_CIO0_RX_P	PB_CIO2_RX_P
TBT_A_D2R_N<0>	E22	PA_CIO0_RX_N	PB_CIO2_RX_N
TBT_A_CONFIG1_BUF	P1	PA_CONFIG1/CIO_0_LSEO	PB_CONFIG1/CIO_2_LSEO
TBT_A_CONFIG2_RC	K5	PA_CONFIG2/CIO_0_LSOE	PB_CONFIG2/CIO_2_LSOE
TBT_A_R2D_C_P<1>	L24	PA_CIO1_TX_P/DPSRC_2_P	PB_CIO3_TX_P/DPSRC_2_P
TBT_A_R2D_C_N<1>	J24	PA_CIO1_TX_N/DPSRC_2_N	PB_CIO3_TX_N/DPSRC_2_N
TBT_A_D2R_P<1>	L22	PA_CIO1_RX_P	PB_CIO3_RX_P
TBT_A_D2R_N<1>	J22	PA_CIO1_RX_N	PB_CIO3_RX_N
TBT_A_LSTX	N8	PA_LSTX/CIO_1_LSEO	PB_LSTX/CIO_3_LSEO
TBT_A_LSRX	J6	PA_LSRX/CIO_1_LSOE	PB_LSRX/CIO_3_LSOE
TBTPA_ML_C_P<1>	A16	PA_DPSRC_1_P	PB_DPSRC_1_P
TBTPA_ML_C_N<1>	B17	PA_DPSRC_1_N	PB_DPSRC_1_N
TBTPA_ML_C_P<3>	A18	PA_DPSRC_3_P	PB_DPSRC_3_P
TBTPA_ML_C_N<3>	B19	PA_DPSRC_3_N	PB_DPSRC_3_N
TBTPA_AUXCH_C_P	L4	PA_AUX_P	PB_AUX_P
TBTPA_AUXCH_C_N	L2	PA_AUX_N	PB_AUX_N
TBTPA_HPD	M3	PA_DPSRC_HPD	PB_DPSRC_HPD
TBT_A_HV_EN	R8	GPIO_0/PA_HV_EN/BYP0	GPIO_1/PB_HV_EN/BYP0
TBT_A_CIO_SEL	N2	GPIO_10/PA_CIO_SEL/BYP1	GPIO_11/PB_CIO_SEL/BYP1
TBT_A_DP_PWRDN	P3	GPIO_12/PA_DP_PWRDN/BYP2	GPIO_13/PB_DP_PWRDN/BYP2

DP_TBTSRC_ML_CP<3>	A14	DPSRC_3_P
DP_TBTSRC_ML_CN<3>	B15	DPSRC_3_N
DP_TBTSRC_ML_CP<2>	A12	DPSRC_2_P
DP_TBTSRC_ML_CN<2>	B13	DPSRC_2_N
DP_TBTSRC_ML_CP<1>	A10	DPSRC_1_P
DP_TBTSRC_ML_CN<1>	B11	DPSRC_1_N
DP_TBTSRC_ML_CP<0>	A8	DPSRC_0_P
DP_TBTSRC_ML_CN<0>	B9	DPSRC_0_N
DP_TBTSRC_AUXCH_CP	J4	DPSRC_AUX_P
DP_TBTSRC_AUXCH_CN	J2	DPSRC_AUX_N
DP_TBTSRC_HPD	AC2	DPSRC_HPD_OD

TBT_GPIO2	U2	GPIO_2/TMU_CLK_IN/AC_PRESENT
TBT_PWR_EN	L6	GPIO_3/FORCE_PWR
TBT_WAKE_L	H5	GPIO_4/WAKE_OD_N
TBT_CIO_PLUG_EVENT_L	Y7	GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD
HDMITBTMUX_SEL_TBT	Y1	GPIO_6_OD/CIO_SDA_OD
TBT_GPIO7	T7	GPIO_7_OD/CIO_SCL_OD
TBT_EN_CIO_PWR_L	V7	GPIO_8/EN_CIO_PWR_OD*
=TBT_BATLOW_L	M7	GPIO_9/SX_CTRL_OD*
TBTDP_AUXIO_EN	T1	GPIO_14
TBT_DDC_XBAR_EN_L	T3	GPIO_15

TBT_B_R2D_C_P<0>	R24	PB_CIO2_TX_P/DPSRC_0_P
TBT_B_R2D_C_N<0>	N24	PB_CIO2_TX_N/DPSRC_0_N
TBT_B_D2R_P<0>	R22	PB_CIO2_RX_P
TBT_B_D2R_N<0>	N22	PB_CIO2_RX_N
TBT_B_CONFIG1_BUF	D3	PB_CONFIG1/CIO_2_LSEO
TBT_B_CONFIG2_RC	M1	PB_CONFIG2/CIO_2_LSOE
TBT_B_R2D_C_P<1>	W24	PB_CIO3_TX_P/DPSRC_2_P
TBT_B_R2D_C_N<1>	U24	PB_CIO3_TX_N/DPSRC_2_N
TBT_B_D2R_P<1>	W22	PB_CIO3_RX_P
TBT_B_D2R_N<1>	U22	PB_CIO3_RX_N
TBT_B_LSTX	M5	PB_LSTX/CIO_3_LSEO
TBT_B_LSRX	P7	PB_LSRX/CIO_3_LSOE
DP_TBTPB_ML_C_P<1>	A20	PB_DPSRC_1_P
DP_TBTPB_ML_C_N<1>	B21	PB_DPSRC_1_N
DP_TBTPB_ML_C_P<3>	A22	PB_DPSRC_3_P
DP_TBTPB_ML_C_N<3>	B23	PB_DPSRC_3_N
DP_TBTPB_AUXCH_C_P	K3	PB_AUX_P
DP_TBTPB_AUXCH_C_N	K1	PB_AUX_N
DP_TBTPB_HPD	N6	PB_DPSRC_HPD
TBT_B_HV_EN	F1	GPIO_1/PB_HV_EN/BYP0
TBT_B_CIO_SEL	R2	GPIO_11/PB_CIO_SEL/BYP1
TBT_B_DP_PWRDN	F3	GPIO_13/PB_DP_PWRDN/BYP2

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

PP3V3_TBTLC

R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
C2890 1UF 10% 6.3V CERM 402 (BYPASS=U2890::2mm)
R2892 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U2890 4MBIT W25X40CLXIG USON

(TBT_SPI_MOSI)	5	DI/IO0
(TBT_SPI_CLK)	6	CLK
(TBT_SPI_CS_L)	1	CS*
TBTROM_WP_L	3	WP*
TBTROM_HOLD_L	7	HOLD*
(TBT_SPI_MISO)	2	DO/IO1
	4	GND
	8	VCC
	9	THRM_PAD

OMIT
R2815 NOSTUFF NONE NONE NONE 0201

R2829 10K 5% 1/20W MF 201
R2825 100 5% 1/20W MF 201

R2830 100K 5% 1/20W MF 201
R2831 100K 5% 1/20W MF 201

R2895 806 1% 1/20W MF 201
R2896 1K 5% 1/20W MF 201
R2899 NO STUFF 10K 5% 1/20W MF 201

R2878 100K 5% 1/20W MF 201
R2879 100K 5% 1/20W MF 201

R2881 100K 5% 1/20W MF 201
R2880 100K 5% 1/20W MF 201
R2882 100K 5% 1/20W MF 201

R2884 100K 5% 1/20W MF 201
R2885 10K 5% 1/20W MF 201
R2886 NO STUFF 10K 5% 1/20W MF 201

R2832 100K 5% 1/20W MF 201
R2883 100K 5% 1/20W MF 201

R2888 10K 5% 1/20W MF 201
R2887 10K 5% 1/20W MF 201

R2867 NO STUFF 10K 5% 1/20W MF 201
R2861 10K 5% 1/20W MF 201
R2862 10K 5% 1/20W MF 201
R2863 10K 5% 1/20W MF 201

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

Divides 3.3V to 1.8V

PP3V3_TBTLC
SYSCLK_CLK25M_TBT
=PP3V3_S4_TBT
TBT_EN_CIO_PWR_L
TBT_DDC_XBAR_EN_L
HDMITBTMUX_SEL_TBT
TBTDP_AUXIO_EN
DP_TBTSRC_HPD
=TBT_BATLOW_L
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N

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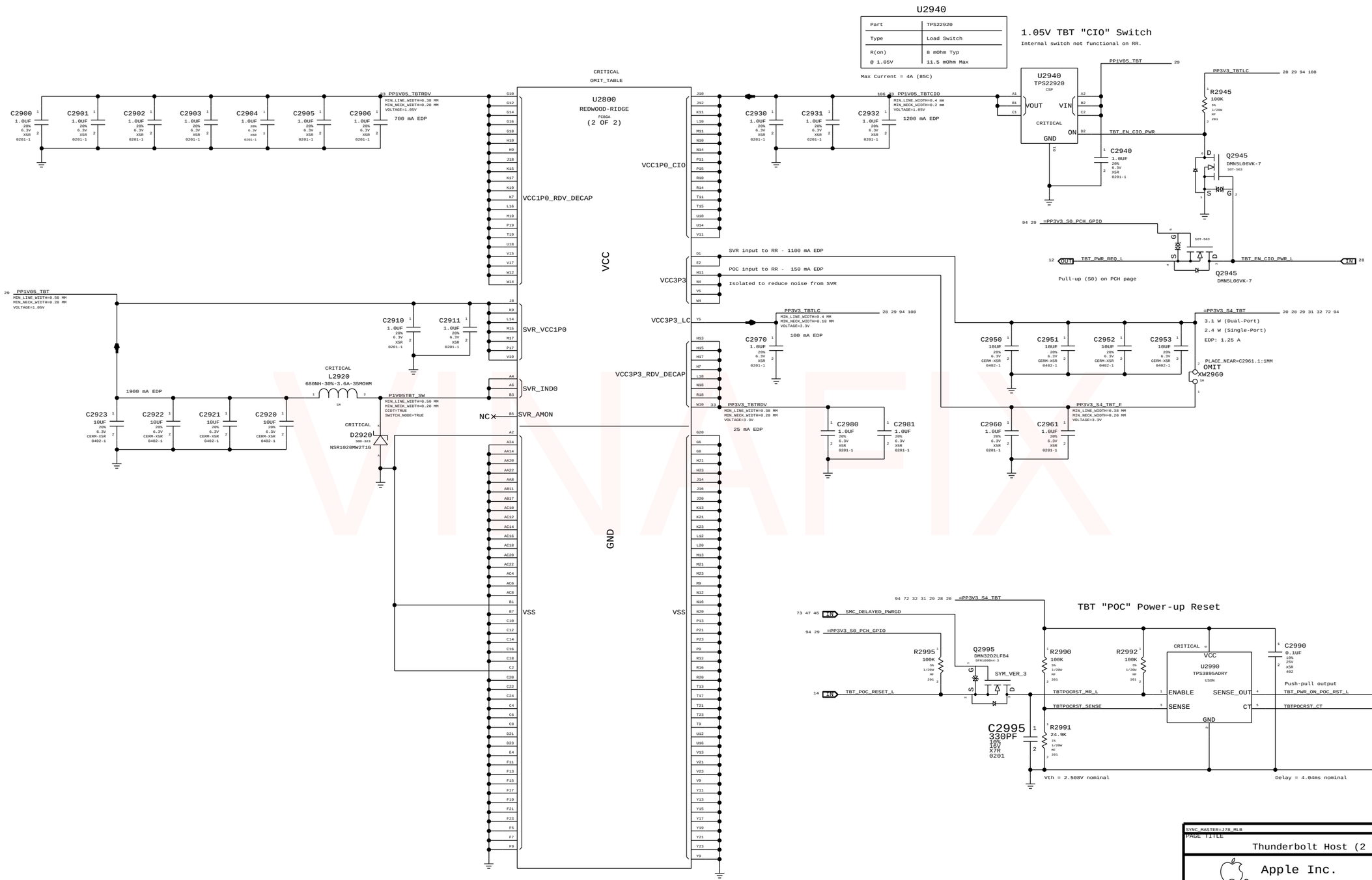

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

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Thunderbolt Power Support

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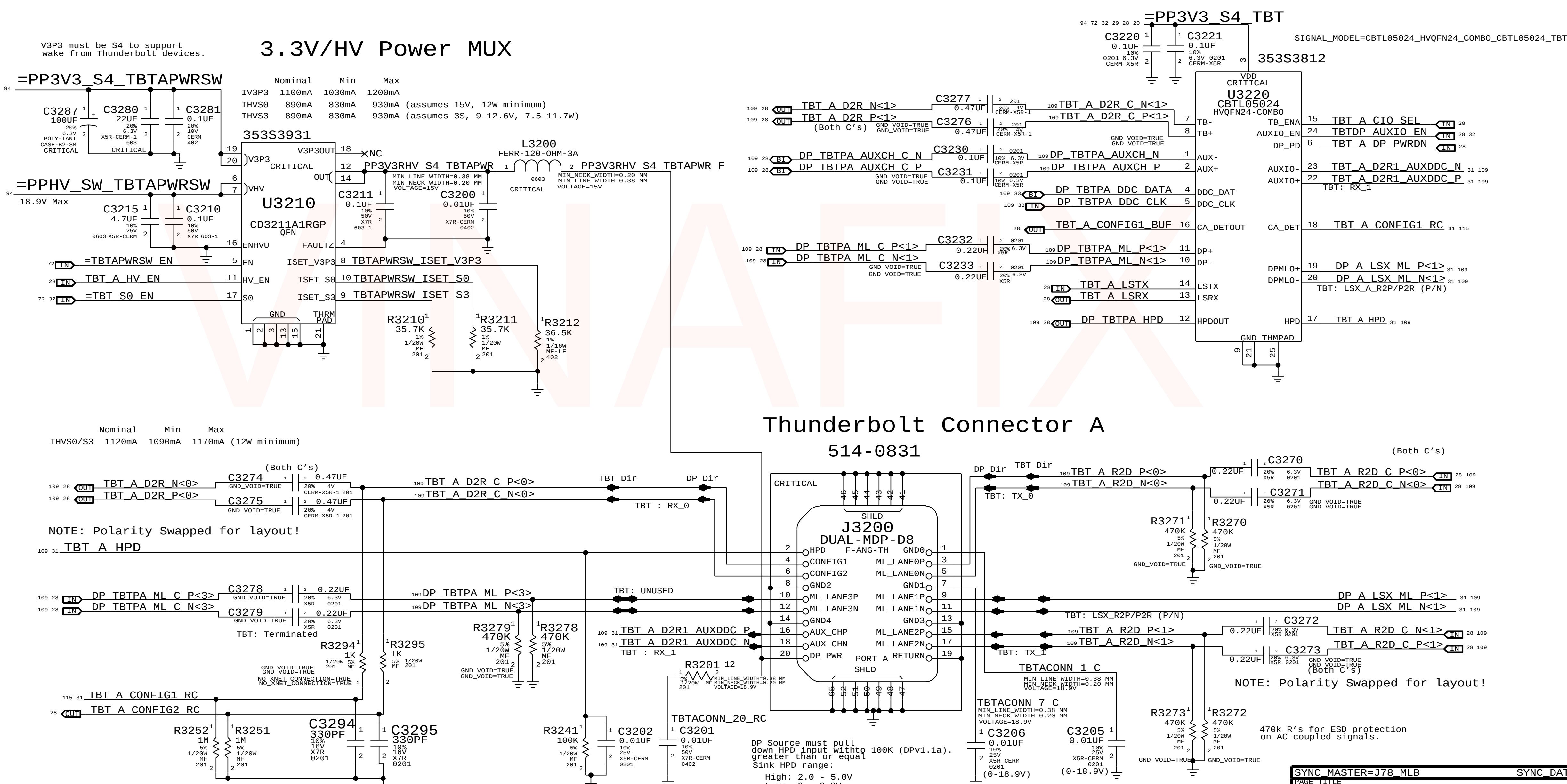
3.3V/HV Power MUX
V3P3 must be S4 to support wake from Thunderbolt devices.
=PP3V3_S4_TBTAPWRSW
=PPHV_SW_TBTAPWRSW
18.9V Max
Nominal Min Max
IV3P3 1100mA 1030mA 1200mA
IHVS0 890mA 830mA 930mA (assumes 15V, 12W minimum)
IHVS3 890mA 830mA 930mA (assumes 3S, 9-12.6V, 7.5-11.7W)
353S3931
U3210
CD3211A1RGP
QFN
CRITICAL
C3287 100UF
C3280 22UF
C3281 0.1UF
C3215 4.7UF
C3210 0.1UF
C3211 0.1UF
C3200 0.01UF
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
PP3V3RHV_S4_TBTAPWR
L3200
FERR-120-OHM-3A
PP3V3RHV_S4_TBTAPWR_F
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
R3210 35.7K
R3211 35.7K
R3212 36.5K
=PP3V3_S4_TBT
C3220 0.1UF
C3221 0.1UF
353S3812
U3220
CBTL05024
HVQFN24-COMBO
SIGNAL_MODEL=CBTL05024_HVQFN24_COMBO_CBTL05024_TBT
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
C3277 0.47UF
C3276 0.47UF
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C3230 0.1UF
C3231 0.1UF
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C3232 0.22UF
C3233 0.22UF
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
Thunderbolt Connector A
514-0831
J3200
DUAL-MDP-D8
F-ANG-TH
CRITICAL
Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
C3274 0.47UF
C3275 0.47UF
(Both C's)
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT Dir
DP Dir
TBT : RX_0
NOTE: Polarity Swapped for layout!
TBT_A_HPD
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C3278 0.22UF
C3279 0.22UF
TBT: Terminated
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: UNUSED
R3279 470K
R3278 470K
R3294 1K
R3295 1K
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT : RX_1
R3201
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252 1M
R3251 1M
C3294 330PF
C3295 330PF
R3241 100K
C3202 0.01UF
TBTACONN_20_RC
C3201 0.01UF
DP Source must pull down HPD input with to 100K (DPv1.1a). greater than or equal
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C3270 0.22UF
C3271 0.22UF
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R3271 470K
R3270 470K
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1
C3272 0.22UF
C3273 0.22UF
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
NOTE: Polarity Swapped for layout!
TBTACONN_1_C
TBTACONN_7_C
C3206 0.01UF
C3205 0.01UF
(0-18.9V)
R3273 470K
R3272 470K
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER	051-1635
SIZE	D
REVISION	5.0.0
BRANCH	proto2
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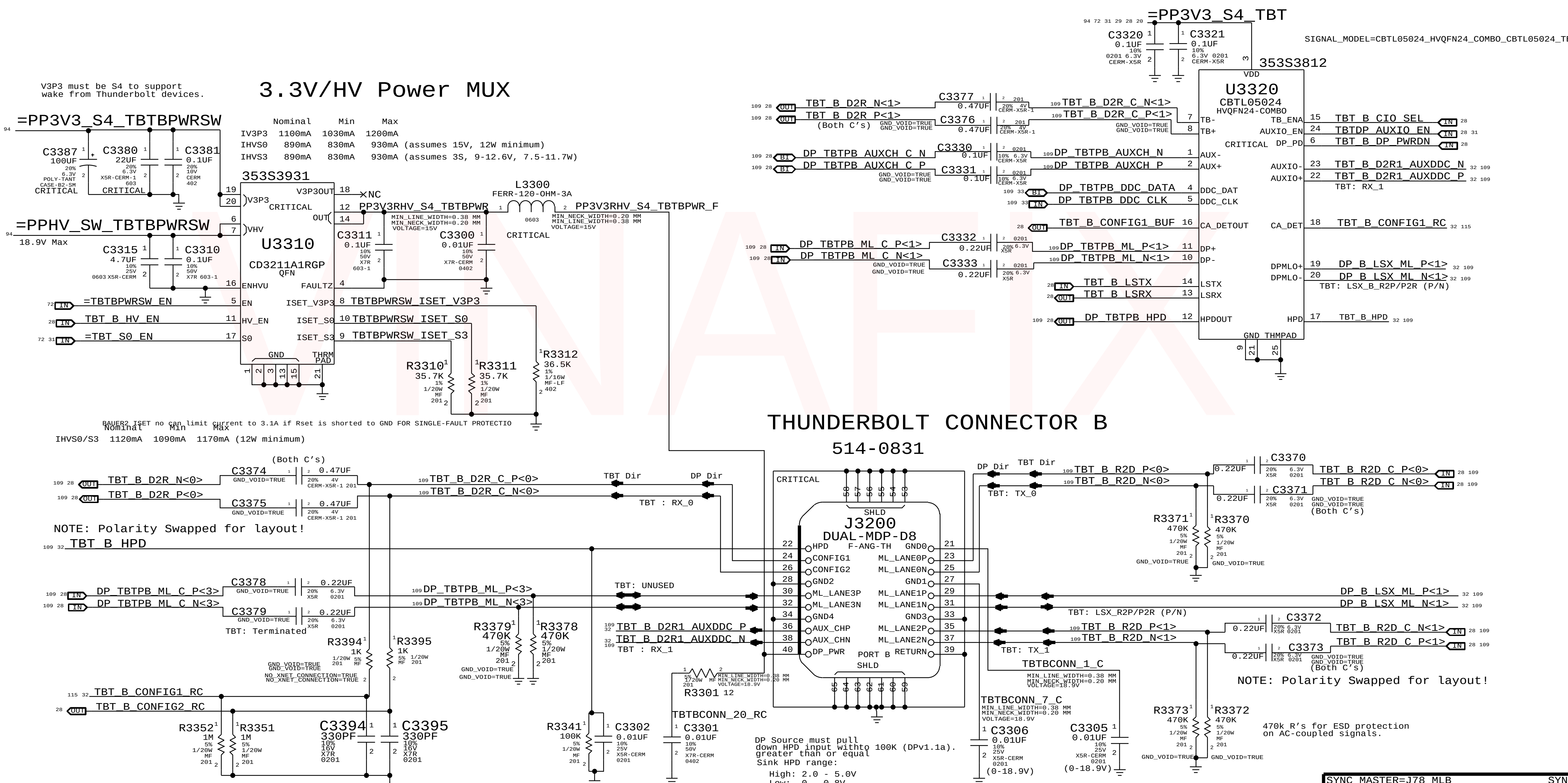
SHEET	31 OF 115



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D

REVISION: 5.0.0

BRANCH: proto2

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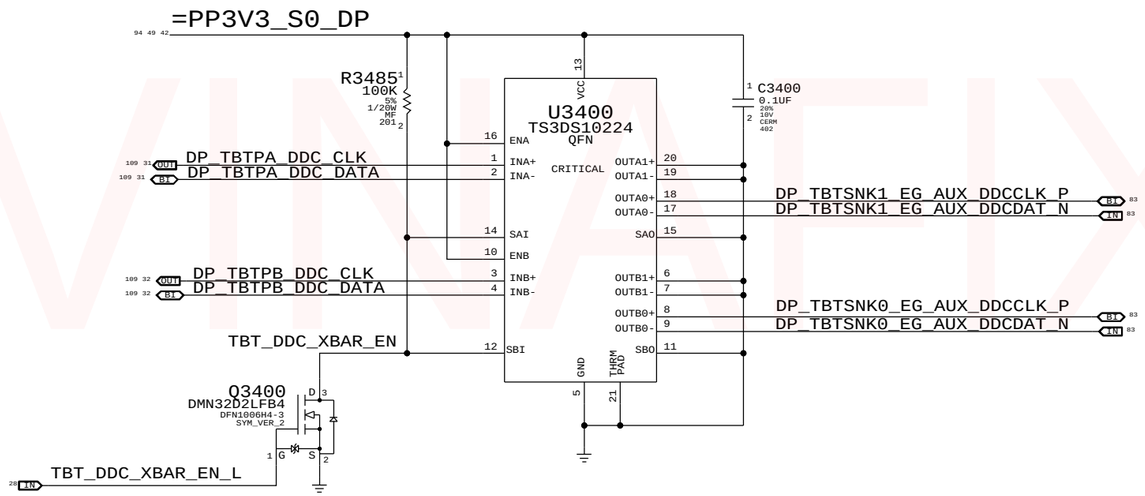
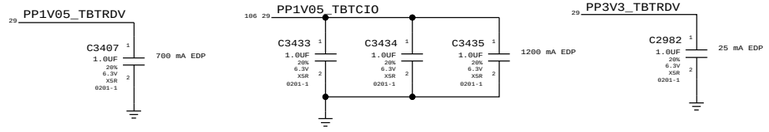
Dual-Port Host DDC Crossbar



28 =TBT_BATLOW_L — TBT_BATLOW_L
MAKE_BASE=TRUE



Additional DeCaps added for CSA-29 (csa-29 is syncing from J44)

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: TBT DDC Crossbar

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D

REVISION: 5.0.0

BRANCH: proto2

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AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)

94 47 34 =PP3V3_S4_AP

U3510 TPS22924 CSP
A2 B2 VIN VOUT A1 B1
CRITICAL
C2 ON GND C1

47 34 IN AP_PWR_EN

47 PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

CRITICAL L3502
FERR-220-OHM-2.5A
0603

34 PP3V3_S4_AP_FLT

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603

514S0335 CRITICAL
J3500 SSD-K99 F-RT-SM1

47 46 BI AP_EVENT_L
101 13 IN PCIE_AP_R2D_C_N
101 13 IN PCIE_AP_R2D_C_P

C3505 0.1UF 10% 16V X7R-CERM-X5R 0201
PLACE_NEAR=J3500.4:7mm
C3506 0.1UF 10% 16V X7R-CERM-X5R 0201
PLACE_NEAR=J3500.5:7mm

101 PCIE_AP_R2D_N
101 PCIE_AP_R2D_P
101 11 IN PCIE_CLK100M_AP_N
101 11 IN PCIE_CLK100M_AP_P
101 13 OUT PCIE_AP_D2R_P
101 13 OUT PCIE_AP_D2R_N

34 AP_WAKE_L
34 AP_RESET_CONN_L
34 AP_CLKREQ_Q_L
104 34 USB_BT_MUX_N
104 34 USB_BT_MUX_P

94 34 =PP3V3_G3H_BT

CRITICAL
U3540 TPS22924B CSP
A2 B2 VIN VOUT A1 B1
C2 ON GND C1

PP3V3_G3H_BT_FET
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

CRITICAL L3501
FERR-220-OHM-2.5A
0603

PP3V3_G3H_BT_FLT
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603

20 BT_RESET_MASK_L

BT_RESET_MASK_L GATES BT_PWR_RST_L
until after S0 GPIO is guranteed stable

47 46 SMC_G3_WAKESRC_EN

R3542 10K 5% 1/16W MF-LF 402

CRITICAL
Q3540 DMC2400UV SOT563
P-CHN
3 D S 4
G
5

12 IN BT_PWR_RST_L

BT_PWR_EN

6 D
Q3540 DMC2400UV SOT563 P-CHN
G S
1

BT_PWR_RST

R3543 10K 5% 1/16W MF-LF 402
C3541 0.01UF 20% 16V CERM 402

Wake from BT in G3H circuit

47 46 OUT SMC_PME_S4_WAKE_L

CRITICAL
Q3501 SSM3K15AMFVAPE VESM
3 D
S G
2 1

94 34 =PP3V3_G3H_BT

C3500 0.1UF 10% 16V X5R-CERM 0201

U3501 USB3740 DFN
VDD
104 13 BI USB_BT_N DP_2
104 13 BI USB_BT_P DM_2
USB_BT_WAKEN DP_1
NC DM_1
OE*
72 46 12 IN PM_SLP_S5_L S
GND

DP 10 USB_BT_MUX_N 34 104
DM 9 USB_BT_MUX_P 34 104

SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

R3501 15K 1% 1/20W MF 201

Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%

PP3V3_S4_AP_FLT 34
=PP3V3_S4_AP 34 47 94

R3530 100K 1% 1/16W MF-LF 402
R3531 232K 1% 1/16W MF-LF 402
P3V3AP_VMON

CRITICAL
U3530 SLG4AP041V TDFN
VDD
SENSE VREF
DLY
RESET* MR*
EN
IN OUT (OD)
THRM PAD GND

C3530 0.1UF 20% 16V CERM 402

34 AP_RESET_CONN_L
34 AP_CLKREQ_Q_L

AP_RESET_L IN 20
AP_PWR_EN IN 34 47
AP_CLKREQ_L OUT 11 18

R3532 100K 1% 1/16W MF-LF 402

PP3V3_S4_AP_FLT 34

Q3570 SSM3K15AMFVAPE VESM CRITICAL
D G S

R3570 10K 5% 1/16W MF-LF 402

38 20 12 PCIE_WAKE_L
AP_WAKE_L 34

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: AIRPORT/BT

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D
REVISION: 5.0.0
BRANCH: proto2
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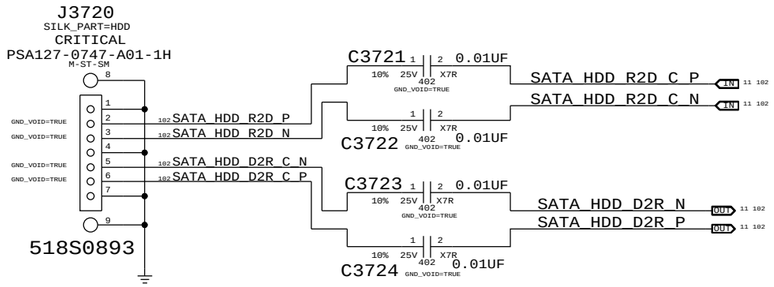
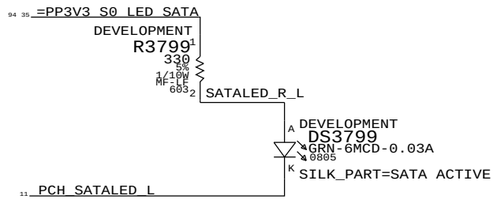
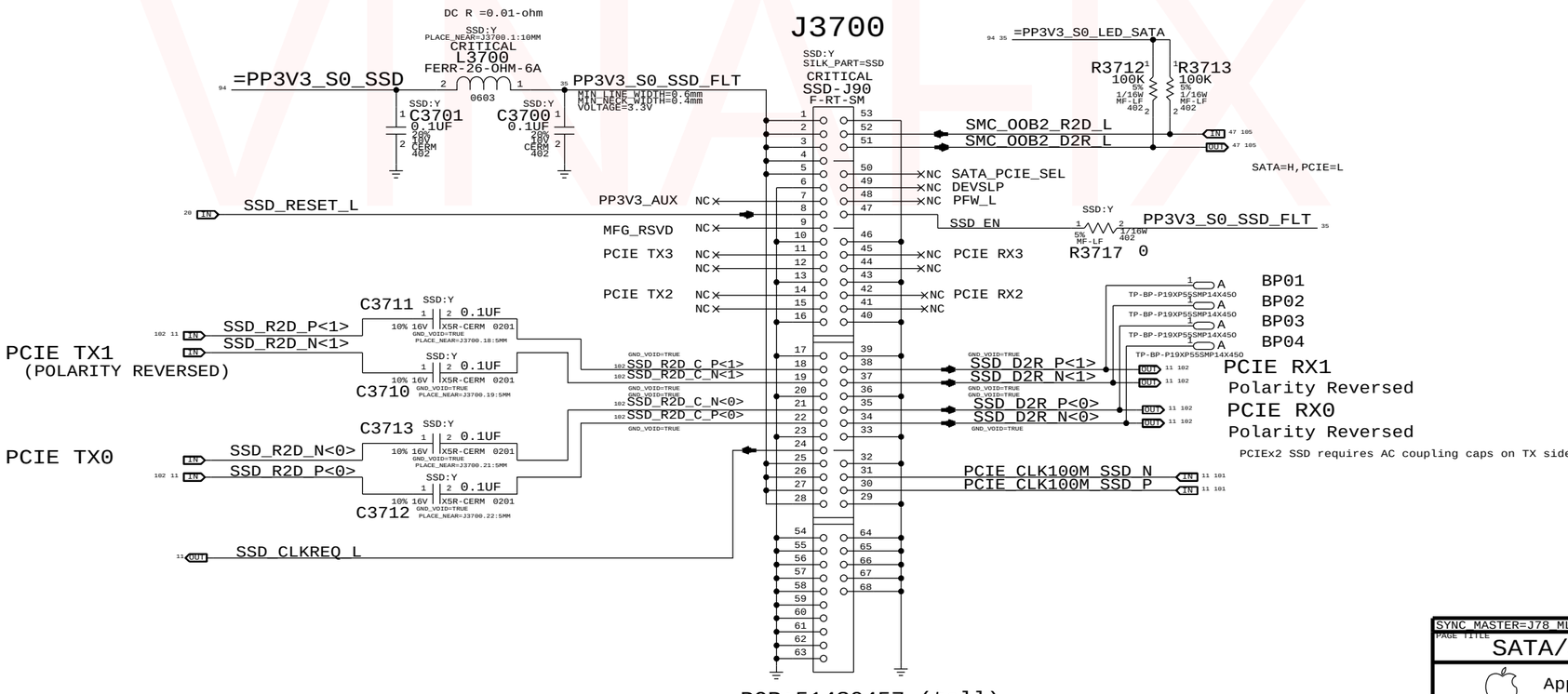
HDD SIGNAL CONNECTOR



SATA Activity LED



GS3 SSD



SYNC_MASTER=J78_MLB	SYNC_DATE=02/21/2014
PAGE TITLE	SATA/SSD Connectors
Apple Inc.	DRAWING NUMBER 051-1635 · SIZE D
	REVISION 5.0.0
	BRANCH proto2
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HDD POWER

HDD OOB TEMP SENSING

=PP5V_S0_HDD_PWR
=PP12V_S0_HDD_PWR
J3830
78047-0773
M-ST-SM-1
SILK_PART=PWR
CRITICAL
518S0865
C3831 10UF 10% 25V X5R 1206-1
C3832 10UF 20% 16V X5R 603
SMC_OOB1_RX_CN
FERR-220-OHM
L3830
SMC_OOB1_RX_FILT
=PP3V3_S0_SENSE
R3802 180K 5% 1/16W MF-LF 402
R3800 232K 1% 1/16W MF-LF 402
Trip is 1.0V
HDD_OOB_1V00_REF
R3801 100K 1% 1/16W MF-LF 402
C3801 0.1UF 10% 16V X7R-CERM 0402
C3800 0.1UF 10% 16V X7R-CERM 0402
R3805 1K 5% 1/16W MF-LF 402
IDLE IS AT 1.5V
From drive:
Low: 0.0V to 0.3V
High: 1.2V to 2.0V
R3821 10K 5% MF-LF 1/16W 402
HDD_PWR_EN_L
Q3820 SSM6N15AFEAPL SOT563 CRITICAL
Q3820 SSM6N15AFEAPL SOT563 CRITICAL
R3803 3.3K 5% 1/16W MF-LF 402
SMC_OOB1_D2R_R
R3804 150K 5% 1/16W MF-LF 402
U3800 LMV331 SC70-5 CRITICAL
VCC
GND
SMC_OOB1_D2R_L
Notes:
Drive active: Valid signal protocol
Drive asleep: HDD drives HDD_OOB_TEMP low
Drive disconnected: Pulled high

HDD 12V_S0 FET
(max 2.8A,ave 0.6A)

=PP12V_S0_HDD
Q3810 IRFH3702TRPBF
PP12V_S0_HDD_FET
R3810 100 5% 1/10W MF-LF 603
FET_HDD_SLGSW
C3810 1UF 10% 16V X5R 603
U3810 SLG5AP026 TDFN CRITICAL
VCC
ON
NC
NC
D1
D2
G
PG
GND
THRM PAD
VIH: 2.4V TO 5.5V
HDD_12V_S0_GATE
NC
PQFN CRITICAL 376S0910 12mOhm
353S3098
=PP3V3_S0_SENSE
R3813 IS NO STUFF for Test Only
NOSTUFF R3813 100K 1/16W MF-LF 1% 402
R3812 0 5% 1/16W MF-LF 402
HDD_PWR_EN
HDD_PWR_EN_R
(PULL UP TO 3V3_S5 INSIDE PCH)

HDD 5V_S0 FET (max 0.7A,ave 0.3A)

=PP5V_S0_HDD
C3820 0.1UF 20% 16V CERM 603
U3820 SLG5AP304V TDFN CRITICAL
VDD
CAP
ON
GND
HDD5V_RAMP_CAP
C3821 0.0047UF 10% 25V CERM 0402
4nF = 2.3V/ms Ramp Rate
PP5V_S0_HDD_FET
353S3672
4AMP,

REMOVE R3813 AND SHORT R3812 AFTER HDD_PWR_EN WORKS

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
HDD/SSD Temp Sense

Apple Inc.

DRAWING NUMBER 051-1635 SIZE D
REVISION 5.0.0
BRANCH proto2
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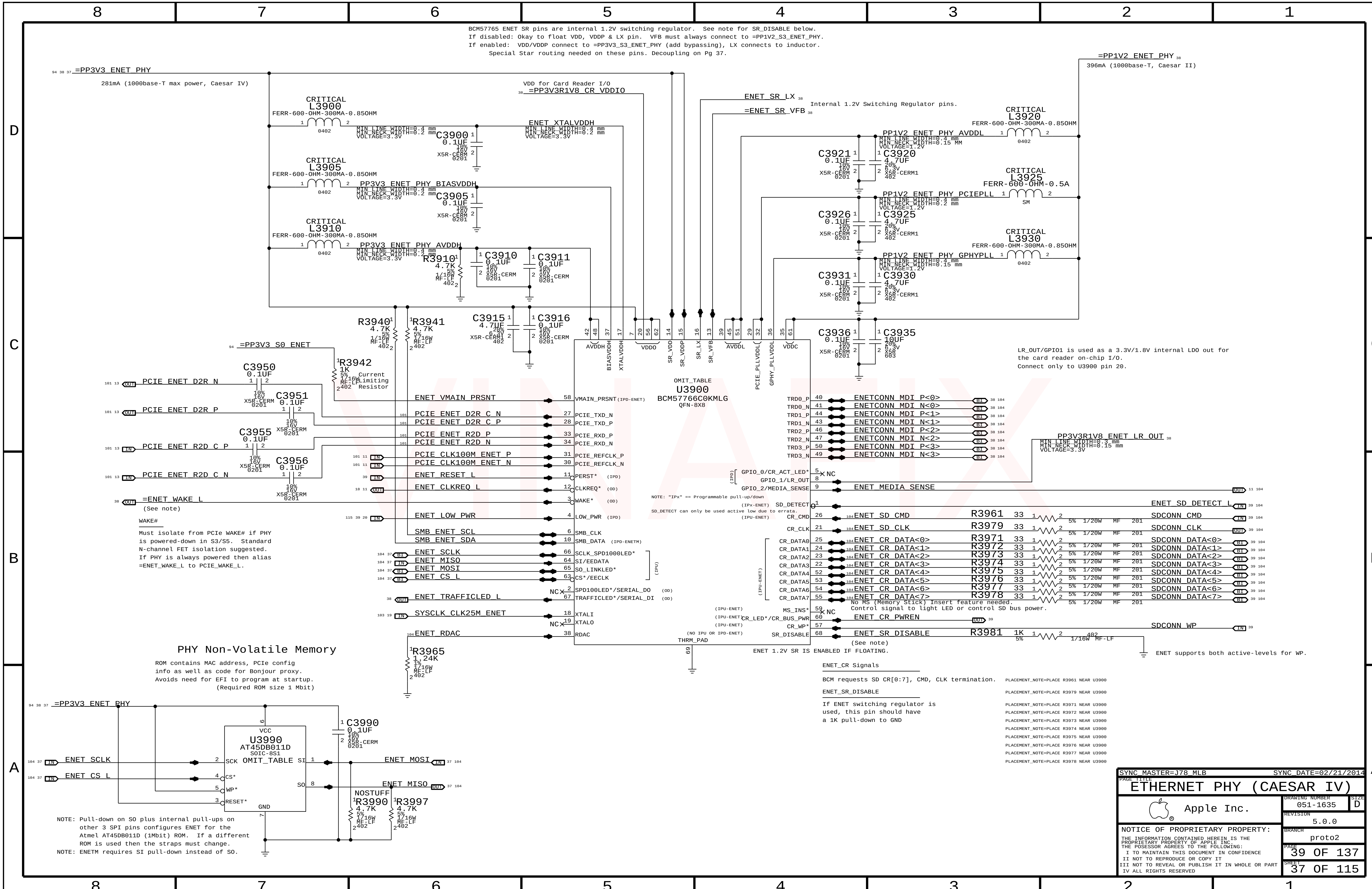
BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.
=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)
=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)
VDD for Card Reader I/O
=PP3V3R1V8_CR_VDDIO
ENET_SR_LX
=ENET_SR_VFB
Internal 1.2V Switching Regulator pins.
CRITICAL
L3900
FERR-600-OHM-300MA-0.85OHM
ENET_XTALVDDH
C3900
0.1UF
L3905
PP3V3_ENET_PHY_BIASVDDH
C3905
L3910
PP3V3_ENET_PHY_AVDDH
R3910
4.7K
C3910
C3911
L3920
PP1V2_ENET_PHY_AVDDL
C3921
C3920
4.7UF
L3925
FERR-600-OHM-0.5A
PP1V2_ENET_PHY_PCIEPLL
C3926
C3925
L3930
PP1V2_ENET_PHY_GPHYPLL
C3931
C3930
C3936
C3935
10UF
C3915
C3916
R3940
R3941
=PP3V3_S0_ENET
R3942
1K
Current Limiting Resistor
C3950
C3951
C3955
C3956
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
=ENET_WAKE_L
(See note)
WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.
ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
ENET_TRAFFICLED_L
SYSCLK_CLK25M_ENET
ENET_RDAC
OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8
NOTE: "IPx" == Programmable pull-up/down
SD_DETECT can only be used active low due to errata.
ENETCONN_MDI_P<0>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<2>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
PP3V3R1V8_ENET_LR_OUT
LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O. Connect only to U3900 pin 20.
ENET_MEDIA_SENSE
ENET_SD_DETECT_L
ENET_SD_CMD
ENET_SD_CLK
ENET_CR_DATA<0> … ENET_CR_DATA<7>
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0> … SDCONN_DATA<7>
R3961 R3979 R3971 R3972 R3973 R3974 R3975 R3976 R3977 R3978
No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.
ENET_CR_PWREN
SDCONN_WP
ENET_SR_DISABLE
R3981
1K
(See note)
ENET 1.2V SR IS ENABLED IF FLOATING.
ENET supports both active-levels for WP.
ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.
ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND
PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900
R3965
1.24K
PHY Non-Volatile Memory
ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup. (Required ROM size 1 Mbit)
=PP3V3_ENET_PHY
U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE
C3990
0.1UF
ENET_SCLK
ENET_CS_L
ENET_MOSI
ENET_MISO
NOSTUFF
R3990
R3997
4.7K
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.
SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014
ETHERNET PHY (CAESAR IV)
Apple Inc.
DRAWING NUMBER 051-1635
SIZE D
REVISION 5.0.0
BRANCH proto2
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CAESAR IV 1.2V INT.VR CMPTS

94 38 37 =PP3V3_ENET_PHY

Power decoupling

C4010 4.7UF 20% 6.3V X5R-CERM1 402

C4011 0.1UF 10% 16V X7R-CERM 0402

37 ENET_SR_LX

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
L4010 4.7UH-0.8A
PCAA031B-SM

C4012 10UF 20% 6.3V X5R 603

C4013 0.1UF 10% 16V X7R-CERM 0402

PP1V2_ENET_INTREG 38

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V

Feedback loop

38 PP1V2_ENET_INTREG

MAKE_BASE=TRUE

=PP1V2_ENET_PHY 37

=ENET_SR_VFB 37

3.3V ENET FET

ENET Enable Generation

"ENET" = "S0" || ("S4" && "WOL_EN")

94 =PP3V3_S4_FET_ENET

R4020 10K 5% 1/16W MF-LF 402

C4020 0.033UF 10% 16V X5R 402

CRITICAL
Q4020 NTR4101P SOT-23-HF

PP3V3_ENET_FET 94

R4021 100K 5% 1/16W MF-LF 402

P3V3ENET_SS

C4021 0.01UF 10% 50V X7R-CERM 0402

PM_EN_ENET_L

CRITICAL
Q4021 2N7002DW-X-G SOT-363

14 WOL_EN

CRITICAL
Q4021 2N7002DW-X-G SOT-363

73 72 47 46 21 12 PM_SLP_S3_L

CAESAR IV ACTIVITY LED

94 38 37 =PP3V3_ENET_PHY

DEVELOPMENT
R4050 330 5% 1/16W MF-LF 402

ENET_ACT

DEVELOPMENT
LED4050 GRN-6MCD-0.03A 0805
SILKSCREEN:ENET ACT

37 ENET_TRAFFICLED_L

CAESAR IV WAKE# ISOLATION

=PP3V3_ENET_PHY 37 38 94

Q4070 SSM3K15AMFVAPE VESM

R4070 10K 5% 1/16W MF-LF 402

34 20 12 PCIE_WAKE_L

ENET_WAKE_L

MAKE_BASE=TRUE

=ENET_WAKE_L 37

157S0058
CRITICAL
T4000 SM

104 37 BI ENETCONN_MDI_N<1>

104 37 BI ENETCONN_MDI_P<1>

ENETCONN_MCT1

ENETCONN_MDI_T_N<1> BI 38 104

ENETCONN_MDI_T_P<1> BI 38 104

TX →
LFE8904CF
← RX

104 37 BI ENETCONN_MDI_N<0>

104 37 BI ENETCONN_MDI_P<0>

ENETCONN_MCT3

ENETCONN_MDI_T_N<0> BI 38 104

ENETCONN_MDI_T_P<0> BI 38 104

CRITICAL
T4010 SM

104 37 BI ENETCONN_MDI_N<2>

104 37 BI ENETCONN_MDI_P<2>

ENETCONN_MCT2

ENETCONN_MDI_T_N<2> BI 38 104

ENETCONN_MDI_T_P<2> BI 38 104

TX →
LFE8904CF
← RX

104 37 BI ENETCONN_MDI_P<3>

104 37 BI ENETCONN_MDI_N<3>

ENETCONN_MCT0

ENETCONN_MDI_T_P<3> BI 38 104

ENETCONN_MDI_T_N<3> BI 38 104

ENETCONN_TCT

C4001 0.1UF 20% 10V CERM 402

C4002 0.1UF 20% 10V CERM 402

C4003 0.1UF 20% 10V CERM 402

C4004 0.1UF 20% 10V CERM 402

R4000 75 5% 1/16W MF-LF 402

R4001 75 5% 1/16W MF-LF 402

R4002 75 5% 1/16W MF-LF 402

R4003 75 5% 1/16W MF-LF 402

104 ENETCONN_MCT_BS

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM

NOSTUFF
C4000 1000PF 10% 2KV CERM 1206

514-0822
CRITICAL
J4000 RCPT-RJ45-D8 F-ANG-TH

ENET_MDI

104 38 BI ENETCONN_MDI_T_N<3> 8 ENET_MDI_TRAN3-

104 38 BI ENETCONN_MDI_T_P<3> 7 ENET_MDI_TRAN3+

104 38 BI ENETCONN_MDI_T_N<1> 6 ENET_MDI_TRAN1-

104 38 BI ENETCONN_MDI_T_N<2> 5 ENET_MDI_TRAN2-

104 38 BI ENETCONN_MDI_T_P<2> 4 ENET_MDI_TRAN2+

104 38 BI ENETCONN_MDI_T_P<1> 3 ENET_MDI_TRAN1+

104 38 BI ENETCONN_MDI_T_N<0> 2 ENET_MDI_TRAN0-

104 38 BI ENETCONN_MDI_T_P<0> 1 ENET_MDI_TRAN0+

9 10 11 12 13 14 SHIELD PINS

37 PP3V3R1V8_ENET_LR_OUT

MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.15 mm

=PP3V3R1V8_CR_VDDIO 37

C4030 4.7UF 20% 6.3V X5R-CERM1 402

C4031 0.1UF 10% 16V X5R-CERM 0201

C4032 0.1UF 10% 16V X5R-CERM 0201

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

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Ethernet Support & Connector

Apple Inc.

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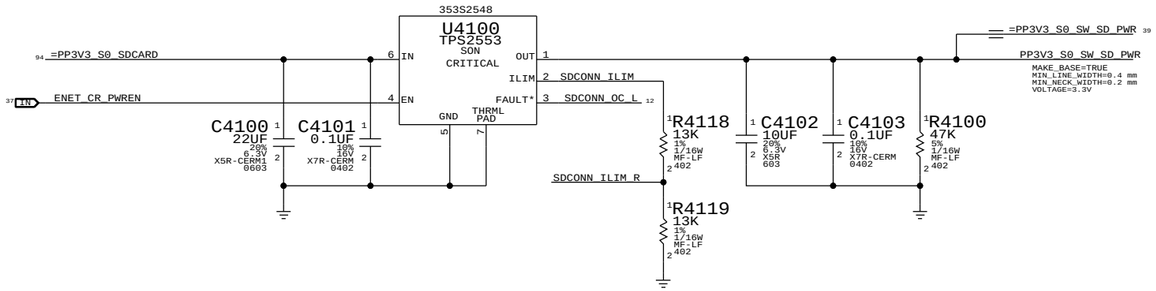
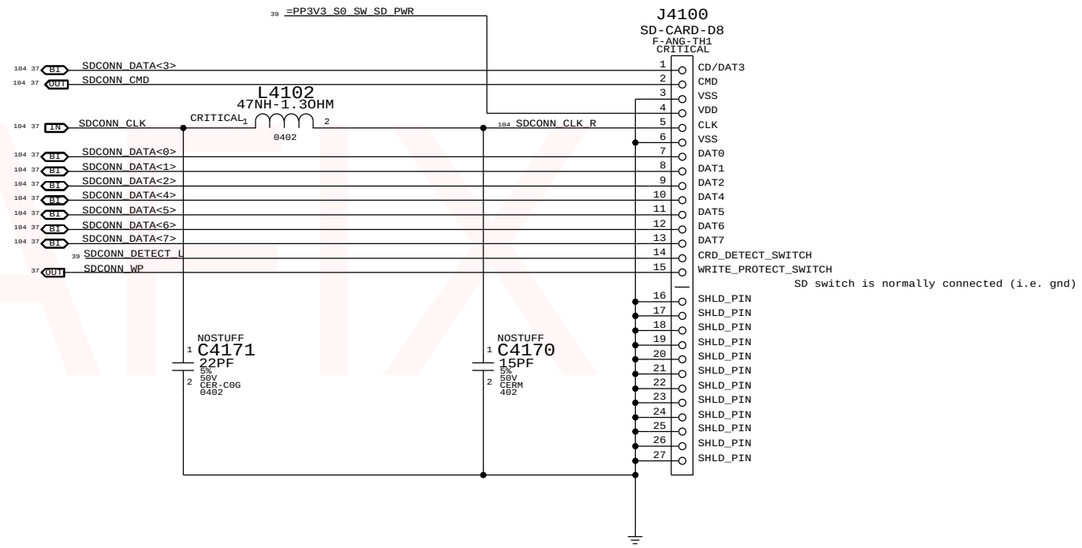
SD CARD 3.3V OVERCURRENT PROTECTION CHIP

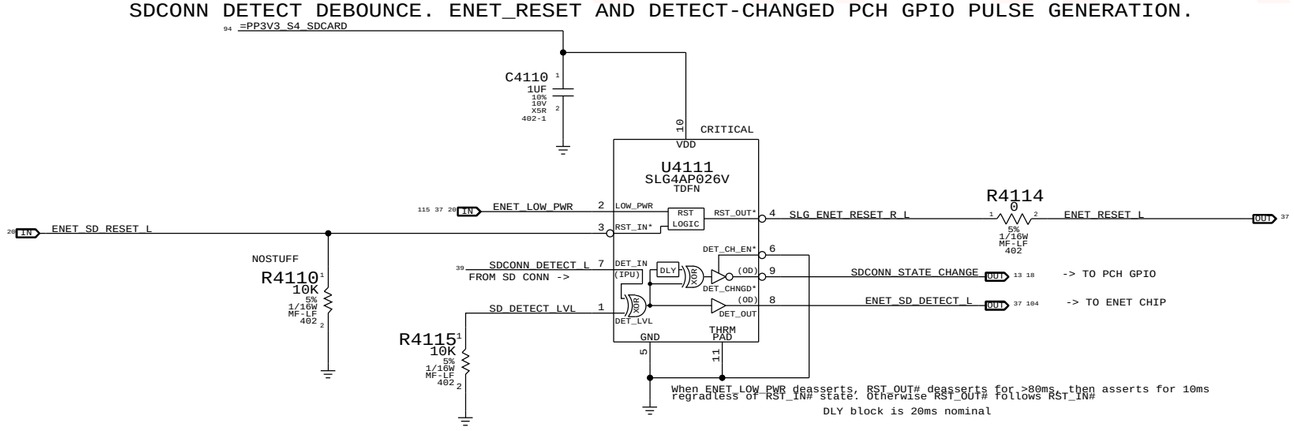


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=J78 MLB SYNC_DATE=02/21/2014

PAGE TITLE

SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-1635 SIZE D

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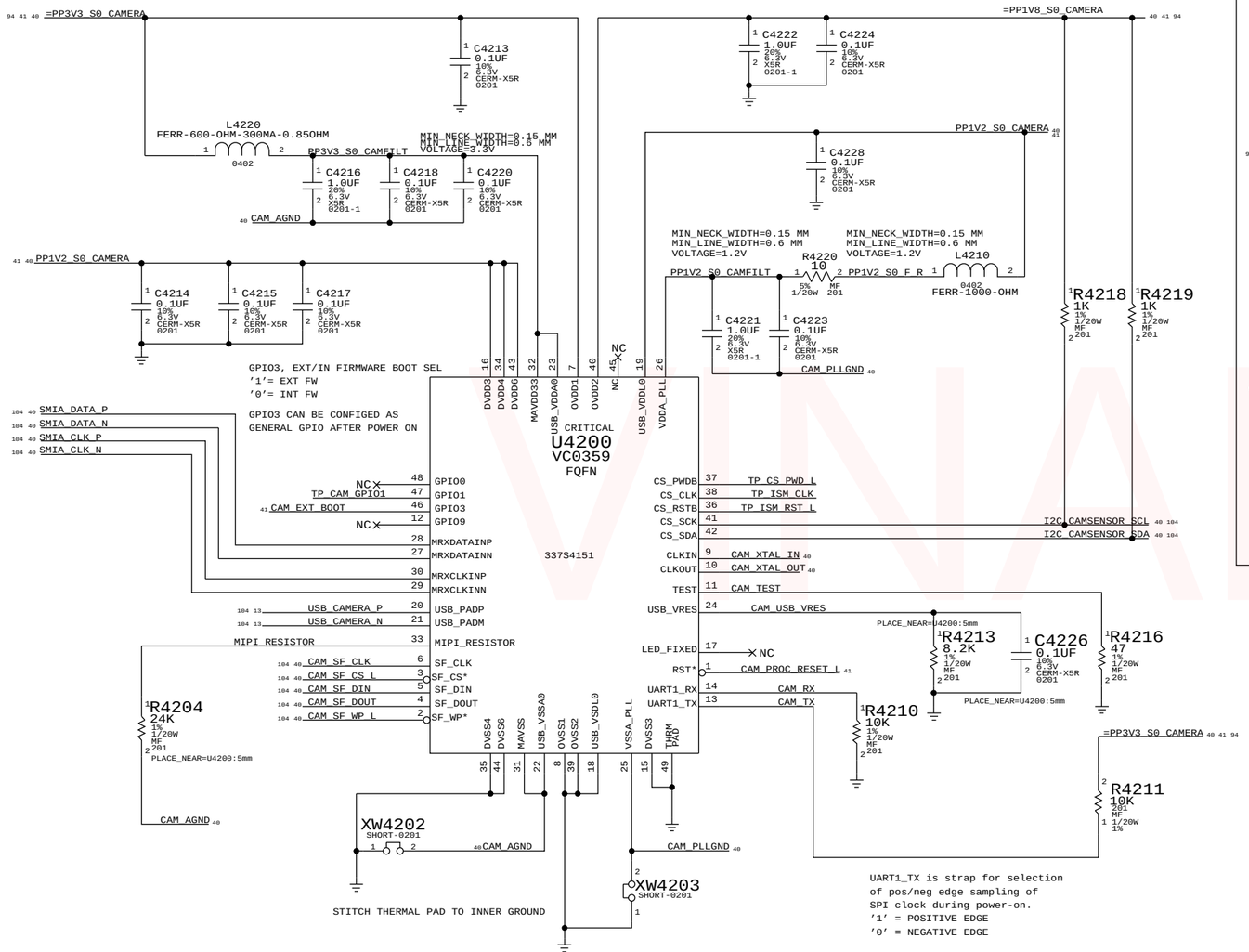
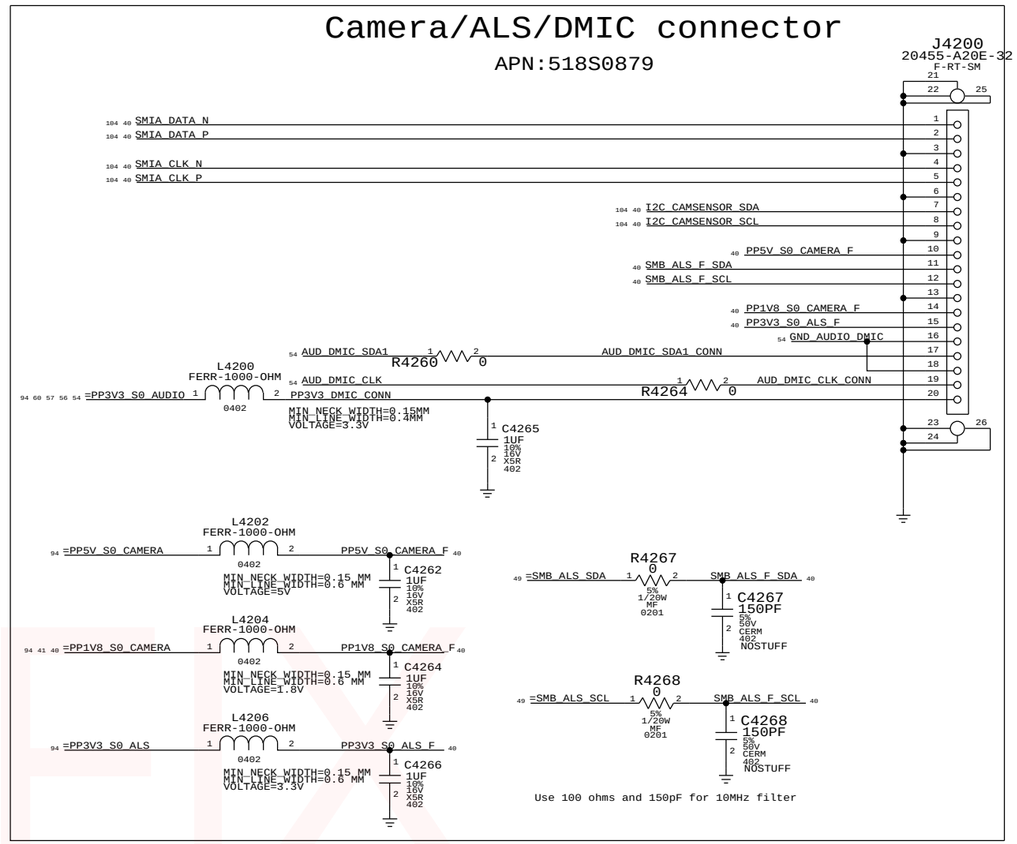
USB CAMERA CONTROLLER

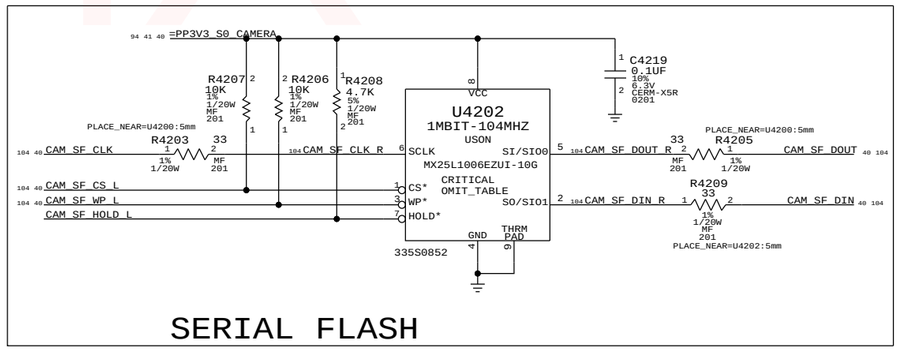


Camera/ALS/DMIC connector

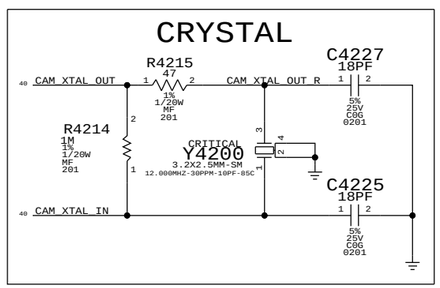
APN:518S0879



SERIAL FLASH



CRYSTAL



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

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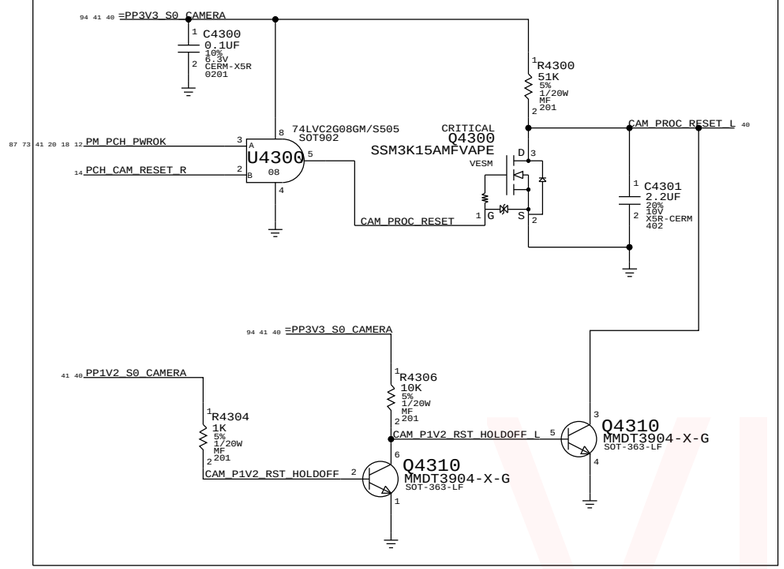
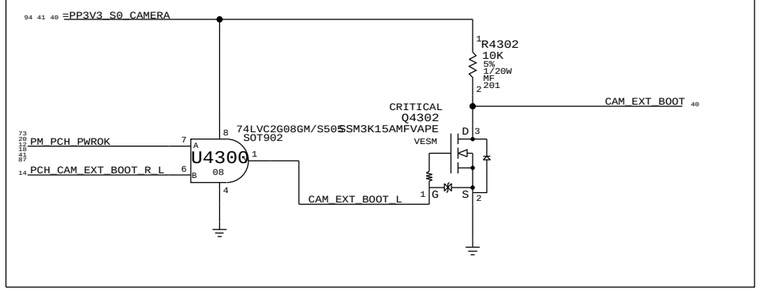
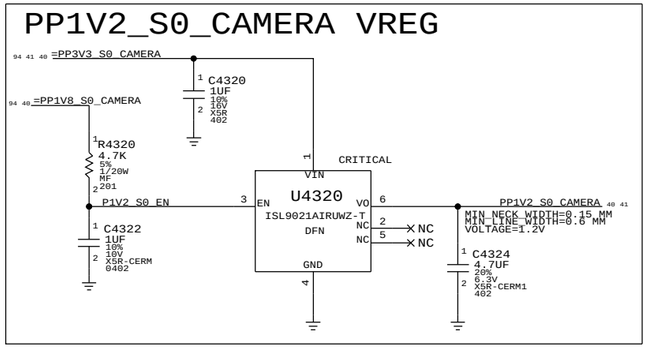
Camera Processor Reset



Camera Processor ExtBoot Cntl



PP1V2_S0_CAMERA VREG



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

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Camera Controller Support

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INTERNAL DP(STRAIGHT)

518S0886
CRITICAL

J4400
20525-160E-01
F-RT-SM

94 =PP12V_S0_LCD → F4400 2AMP-32V (0603) → PP12V_LCD_F (VOLTAGE=12V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.1 mm) → L4400 FERR-120-OHM-3A (0603, 155S0367) → PP12V_LCD (VOLTAGE=12V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.1 mm)

- C4420 10UF 10% 16V X5R-CERM 0805
- C4401 0.001UF 20% 50V CERM 0402
- C4421 0.1UF 10% 16V X7R-CERM 0402

Display TCon Master (Not used)

105 49	BI	SMB_DP_TCON_SDA
105 49	OUT	SMB_DP_TCON_SCL

Display TCon Slave (connect to SMC)

49	IN	SMB_DP_TCON_SLA_SDA
49	BI	SMB_DP_TCON_SLA_SCL
112 69 43	OUT	DP_INTPNL_ML_HPD
112 84 42	OUT	DP_INT_EG_SL_HPD
109 43	BI	DP_INTPNL_ML_AUX_C_P
109 43	BI	DP_INTPNL_ML_AUX_C_N
109 43	IN	DP_INTPNL_ML_C_P<0>
109 43	IN	DP_INTPNL_ML_C_N<0>
109 43	IN	DP_INTPNL_ML_C_P<1>
109 43	IN	DP_INTPNL_ML_C_N<1>
109 43	IN	DP_INTPNL_ML_C_P<2>
109 43	IN	DP_INTPNL_ML_C_N<2>
109 43	IN	DP_INTPNL_ML_C_P<3>
109 43	IN	DP_INTPNL_ML_C_N<3>
109 42	IN	DP_INT_EG_SL_C_P<0>
109 42	IN	DP_INT_EG_SL_C_N<0>
109 42	IN	DP_INT_EG_SL_C_P<1>
109 42	IN	DP_INT_EG_SL_C_N<1>
109 42	IN	DP_INT_EG_SL_C_P<2>
109 42	IN	DP_INT_EG_SL_C_N<2>
109 42	IN	DP_INT_EG_SL_C_P<3>
109 42	IN	DP_INT_EG_SL_C_N<3>
109 42	BI	DP_INT_EG_SL_AUX_C_P
109 42	BI	DP_INT_EG_SL_AUX_C_N
109 96	OUT	AUDIO_SCLK
109 96	OUT	AUDIO_WS
109 54	OUT	DP_INT_SPDIF_AUDIO
109 96	OUT	AUDIO_MUTE_L
112 69	OUT	BLC_VSYNC
112 69	OUT	BLC_LSYNC
112 42		BLC_EN

109 83 IN DP_INT_EG_SL_AUX_P → C4458 0.22UF (20% 6.3V XSR 0201) → DP_INT_EG_SL_AUX_C_P → 42 109
109 83 IN DP_INT_EG_SL_AUX_N → C4459 0.22UF (20% 6.3V XSR 0201) → DP_INT_EG_SL_AUX_C_N → 42 109

- R4406 100K 5% 1/20W MF 201
- R4407 100K 5% 1/20W MF 201 → =PP3V3_S0_INTDPMUX (43 94)

109 83	IN	DP_INT_EG_SL_P<0>	C4450 0.22UF → DP_INT_EG_SL_C_P<0> (42 109)
109 83	IN	DP_INT_EG_SL_N<0>	C4451 0.22UF → DP_INT_EG_SL_C_N<0> (42 109)
109 83	IN	DP_INT_EG_SL_P<1>	C4452 0.22UF → DP_INT_EG_SL_C_P<1> (42 109)
109 83	IN	DP_INT_EG_SL_N<1>	C4453 0.22UF → DP_INT_EG_SL_C_N<1> (42 109)
109 83	IN	DP_INT_EG_SL_P<2>	C4454 0.22UF → DP_INT_EG_SL_C_P<2> (42 109)
109 83	IN	DP_INT_EG_SL_N<2>	C4455 0.22UF → DP_INT_EG_SL_C_N<2> (42 109)
109 83	IN	DP_INT_EG_SL_P<3>	C4456 0.22UF → DP_INT_EG_SL_C_P<3> (42 109)
109 83	IN	DP_INT_EG_SL_N<3>	C4457 0.22UF → DP_INT_EG_SL_C_N<3> (42 109)

(20% 6.3V XSR 0201)

DP_INT_EG_SL_HPD (42 84 112)

- R4400 100K 5% 1/20W MF 201
- 94 49 42 33 =PP3V3_S0_DP
- NOSTUFF R4416 100K 5% 1/20W MF 201
- 112 69 TCON_BLC_EN
- R4415 0 1/16W 402 5% → BLC_EN (42 112)
- NOSTUFF C4410 15UF 20% 6.3V CERM 0402
- 94 49 42 33 =PP3V3_S0_DP
- C4400 0.1UF 10% 6.3V CERM-XSR 0201
- CRITICAL TC7SZ08FEAPE SOT665 U4400
- 112 3 TCON_BLC_EN_LED

Current setting is Workaround for BLC_EN issue ON T-CON (POC)

Note: Make the following stuffing change if problem fixed on T-Con
NOSTUFF R4416
STUFF R4415
STUFF R8105, on BLC page 81

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TP to DP aliases

28 IN TP_DP_TBTSRC_ML_CP<0> = DP_TBTSRC_ML_P<0> 43 109
28 IN TP_DP_TBTSRC_ML_CN<0> = DP_TBTSRC_ML_N<0> 43 109
MAKE_BASE=TRUE

28 IN TP_DP_TBTSRC_ML_CP<1> = DP_TBTSRC_ML_P<1> 43 109
28 IN TP_DP_TBTSRC_ML_CN<1> = DP_TBTSRC_ML_N<1> 43 109
MAKE_BASE=TRUE

28 IN TP_DP_TBTSRC_ML_CP<2> = DP_TBTSRC_ML_P<2> 43 109
28 IN TP_DP_TBTSRC_ML_CN<2> = DP_TBTSRC_ML_N<2> 43 109
MAKE_BASE=TRUE

28 IN TP_DP_TBTSRC_ML_CP<3> = DP_TBTSRC_ML_P<3> 43 109
28 IN TP_DP_TBTSRC_ML_CN<3> = DP_TBTSRC_ML_N<3> 43 109
MAKE_BASE=TRUE

28 BI TP_DP_TBTSRC_AUXCH_CP = DP_TBTSRC_AUXCH_P 43 109
28 BI TP_DP_TBTSRC_AUXCH_CN = DP_TBTSRC_AUXCH_N 43 109
MAKE_BASE=TRUE

94 43 =PP1V5_S0_DP

R4510 470K 5% 1/20W MF 201
R4511 470K 5% 1/20W MF 201

109 83 BI DP_INT_EG_ML_AUX_P — C4508 0.22UF 20% X5R 6.3V — 109 DP_INT_EG_ML_AUX_C_P
109 83 BI DP_INT_EG_ML_AUX_N — C4509 0.22UF 20% X5R 6.3V — 109 DP_INT_EG_ML_AUX_C_N

94 43 =PP1V5_S0_DP

R4512 470K 5% 1/20W MF 201
R4513 470K 5% 1/20W MF 201

109 43 BI DP_TBTSRC_AUXCH_P — C4510 0.22UF 20% X5R 6.3V — 109 DP_TBTSRC_AUX_C_P
109 42 BI DP_TBTSRC_AUXCH_N — C4511 0.22UF 20% X5R 6.3V — 109 DP_TBTSRC_AUX_C_N

112 84 OUT DP_INT_EG_ML_HPD

R4500 100K 5% 1/20W MF 201

94 43 42 =PP3V3_S0_INTDPMUX

R4504 10K 5% 1/20W MF 201

60 14 IN DP_TBT_SEL

NOSTUFF
R4501 10K 5% 1/20W MF 201
U4500.A1:8MM

DP_GPU_MUX_EN

109 83 IN DP_INT_EG_ML_P<0> — B4 DIN1_0+
109 83 IN DP_INT_EG_ML_N<0> — A4 DIN1_0-
109 83 IN DP_INT_EG_ML_P<1> — B5 DIN1_1+
109 83 IN DP_INT_EG_ML_N<1> — A5 DIN1_1-
109 83 IN DP_INT_EG_ML_P<2> — B6 DIN1_2+
109 83 IN DP_INT_EG_ML_N<2> — A6 DIN1_2-
109 83 IN DP_INT_EG_ML_P<3> — A8 DIN1_3+
109 83 IN DP_INT_EG_ML_N<3> — A9 DIN1_3-
109 DP_INT_EG_ML_AUX_C_P — H9 DAUX1+
109 DP_INT_EG_ML_AUX_C_N — J9 DAUX1-
NC — H8 DDC_CLK1
NC — J8 DDC_DAT1
J2 HPD_1

43 IN DP_TBTSRC_ML_C_P<0> — B8 DIN2_0+
43 IN DP_TBTSRC_ML_C_N<0> — B9 DIN2_0-
43 IN DP_TBTSRC_ML_C_P<1> — D8 DIN2_1+
43 IN DP_TBTSRC_ML_C_N<1> — D9 DIN2_1-
43 IN DP_TBTSRC_ML_C_P<2> — E8 DIN2_2+
43 IN DP_TBTSRC_ML_C_N<2> — E9 DIN2_2-
43 IN DP_TBTSRC_ML_C_P<3> — F8 DIN2_3+
43 IN DP_TBTSRC_ML_C_N<3> — F9 DIN2_3-
109 DP_TBTSRC_AUX_C_P — H6 DAUX2+
109 DP_TBTSRC_AUX_C_N — J6 DAUX2-
NC — H5 DDC_CLK2
NC — J5 DDC_DAT2
109 28 OUT DP_TBTSRC_HPD — H3 HPD_2
PD is on the LR page

VDD A2 J4
GND B3 C8 G8 H4 H7 G2

U4500
CBTL06142EEE
TFBGA
CRITICAL

DDC_AUX_SEL C2
XSD* B7
GPU_SEL A1

=PP3V3_S0_INTDPMUX 42 43 94

C4568 0.1UF 10% 6.3V CERM-X5R 0201
C4569 0.1UF 10% 6.3V CERM-X5R 0201

DOUT_0+ B2 — 109 DP_INTPNL_ML_P<0> — C4500 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_P<0> OUT 42 109
DOUT_0- B1 — 109 DP_INTPNL_ML_N<0> — C4501 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_N<0> OUT 42 109
DOUT_1+ D2 — 109 DP_INTPNL_ML_P<1> — C4502 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_P<1> OUT 42 109
DOUT_1- D1 — 109 DP_INTPNL_ML_N<1> — C4503 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_N<1> OUT 42 109
DOUT_2+ E2 — 109 DP_INTPNL_ML_P<2> — C4504 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_P<2> OUT 42 109
DOUT_2- E1 — 109 DP_INTPNL_ML_N<2> — C4505 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_N<2> OUT 42 109
DOUT_3+ F2 — 109 DP_INTPNL_ML_P<3> — C4506 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_P<3> OUT 42 109
DOUT_3- F1 — 109 DP_INTPNL_ML_N<3> — C4507 0.22UF 0201 20% X5R 6.3V — DP_INTPNL_ML_C_N<3> OUT 42 109

AUX+ H2 — 109 DP_INTPNL_ML_AUX_P — R4558 0 5% 1/20W MF 0201 — DP_INTPNL_ML_AUX_C_P BI 42 109
AUX- H1 — 109 DP_INTPNL_ML_AUX_N — R4559 0 5% 1/20W MF 0201 — DP_INTPNL_ML_AUX_C_N BI 42 109

HPDIN J1 — DP_INTPNL_ML_HPD IN 42 69 112

R4502 100K 5% 1/20W MF 201
R4503 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX 42 43 94

109 43 IN DP_TBTSRC_ML_P<0> = DP_TBTSRC_ML_C_P<0> 43
109 43 IN DP_TBTSRC_ML_N<0> = DP_TBTSRC_ML_C_N<0> 43
MAKE_BASE=TRUE

109 43 IN DP_TBTSRC_ML_P<1> = DP_TBTSRC_ML_C_P<1> 43
109 43 IN DP_TBTSRC_ML_N<1> = DP_TBTSRC_ML_C_N<1> 43
MAKE_BASE=TRUE

109 43 IN DP_TBTSRC_ML_P<2> = DP_TBTSRC_ML_C_P<2> 43
109 43 IN DP_TBTSRC_ML_N<2> = DP_TBTSRC_ML_C_N<2> 43
MAKE_BASE=TRUE

109 43 IN DP_TBTSRC_ML_P<3> = DP_TBTSRC_ML_C_P<3> 43
109 43 IN DP_TBTSRC_ML_N<3> = DP_TBTSRC_ML_C_N<3> 43
MAKE_BASE=TRUE

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

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Internal DP MUXing

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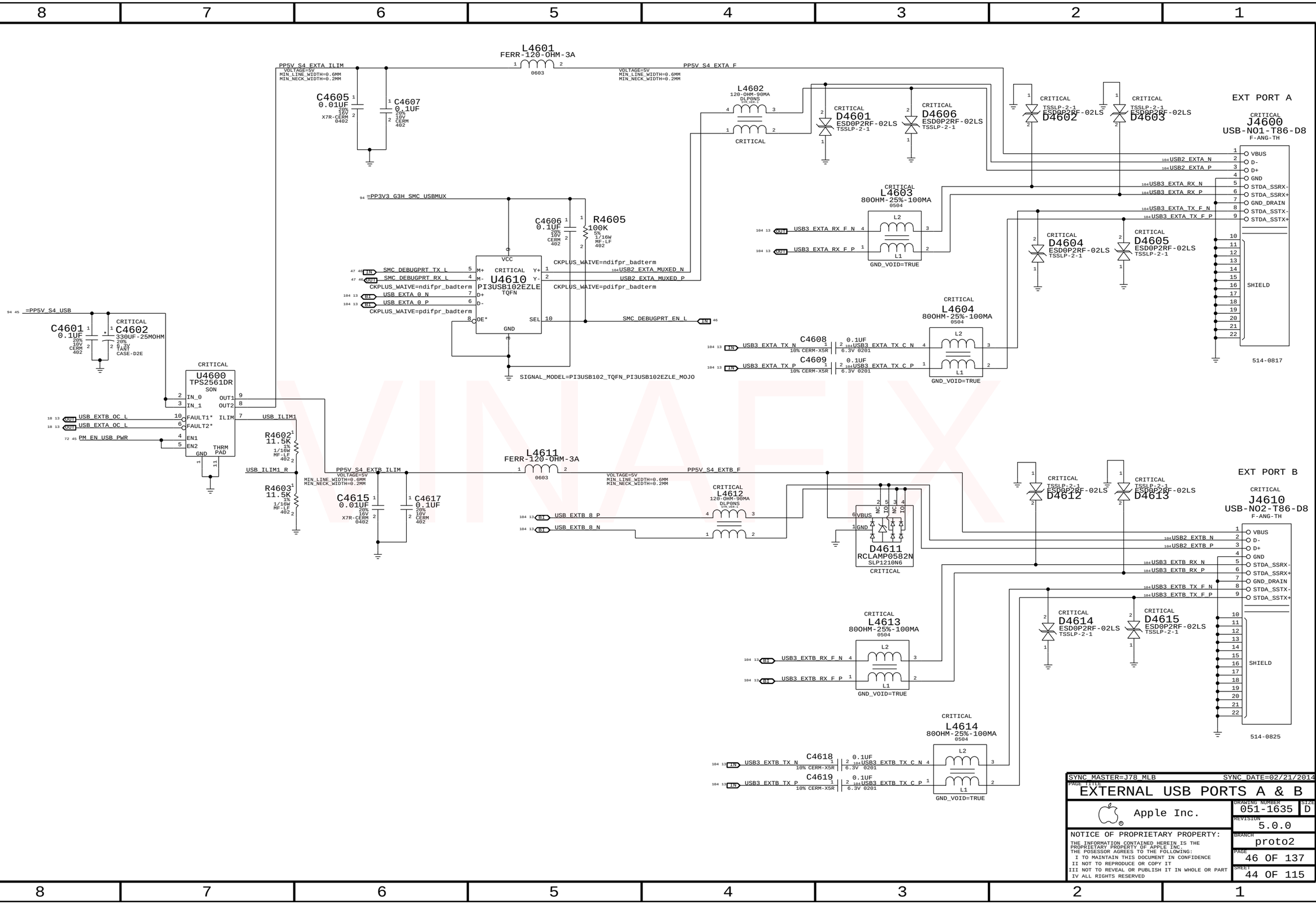
L4601
FERR-120-OHM-3A
0603
PP5V_S4_EXTA_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
C4605
0.01UF
20%
16V
X7R-CERM
0402
C4607
0.1UF
20%
10V
CERM
402
PP5V_S4_EXTA_F
L4602
120-OHM-90MA
DLP0NS
CRITICAL
D4601
ESD0P2RF-02LS
TSSLP-2-1
D4606
ESD0P2RF-02LS
TSSLP-2-1
D4602
ESD0P2RF-02LS
TSSLP-2-1
D4603
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT A
J4600
USB-NO1-T86-D8
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-0817
USB2_EXTA_N
USB2_EXTA_P
USB3_EXTA_RX_N
USB3_EXTA_RX_P
USB3_EXTA_TX_F_N
USB3_EXTA_TX_F_P
L4603
80OHM-25%-100MA
0504
L2
L1
GND_VOID=TRUE
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
D4604
ESD0P2RF-02LS
TSSLP-2-1
D4605
ESD0P2RF-02LS
TSSLP-2-1
=PP3V3_G3H_SMC_USBMUX
C4606
0.1UF
20%
10V
CERM
402
R4605
100K
5%
1/16W
MF-LF
402
U4610
PI3USB102EZLE
TQFN
VCC
GND
SEL
OE*
M+
M-
D+
D-
Y+
Y-
CKPLUS_WAIVE=ndifpr_badterm
CKPLUS_WAIVE=pdifpr_badterm
SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L
USB_EXTA_0_N
USB_EXTA_0_P
USB2_EXTA_MUXED_N
USB2_EXTA_MUXED_P
SMC_DEBUGPRT_EN_L
SIGNAL_MODEL=PI3USB102_TQFN_PI3USB102EZLE_MOJO
=PP5V_S4_USB
C4601
0.1UF
C4602
330UF-25MOHM
6.3V
TANT
CASE-D2E
U4600
TPS2561DR
SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
ILIM
OUT1
OUT2
GND
THRM PAD
USB_EXTB_OC_L
USB_EXTA_OC_L
PM_EN_USB_PWR
USB_ILIM1
R4602
11.5K
1%
1/16W
MF-LF
402
USB_ILIM1_R
R4603
11.5K
C4615
0.01UF
C4617
0.1UF
L4604
80OHM-25%-100MA
0504
C4608
0.1UF
10% CERM-X5R
6.3V 0201
C4609
0.1UF
USB3_EXTA_TX_N
USB3_EXTA_TX_P
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
L4611
FERR-120-OHM-3A
0603
PP5V_S4_EXTB_ILIM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
PP5V_S4_EXTB_F
C4615
0.01UF
20%
16V
X7R-CERM
0402
C4617
0.1UF
20%
10V
CERM
402
L4612
120-OHM-90MA
DLP0NS
CRITICAL
USB_EXTB_8_P
USB_EXTB_8_N
D4611
RCLAMP0582N
SLP1210N6
VBUS
GND
NC
IO
D4612
ESD0P2RF-02LS
TSSLP-2-1
D4613
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT B
J4610
USB-NO2-T86-D8
F-ANG-TH
USB2_EXTB_N
USB2_EXTB_P
USB3_EXTB_RX_N
USB3_EXTB_RX_P
USB3_EXTB_TX_F_N
USB3_EXTB_TX_F_P
SHIELD
514-0825
L4613
80OHM-25%-100MA
0504
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
D4614
ESD0P2RF-02LS
TSSLP-2-1
D4615
ESD0P2RF-02LS
TSSLP-2-1
L4614
80OHM-25%-100MA
0504
C4618
0.1UF
C4619
0.1UF
USB3_EXTB_TX_N
USB3_EXTB_TX_P
USB3_EXTB_TX_C_N
USB3_EXTB_TX_C_P
SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014
PAGE TITLE
EXTERNAL USB PORTS A & B
Apple Inc.
DRAWING NUMBER
051-1635
SIZE
D
REVISION
5.0.0
BRANCH
proto2
PAGE
46 OF 137
SHEET
44 OF 115
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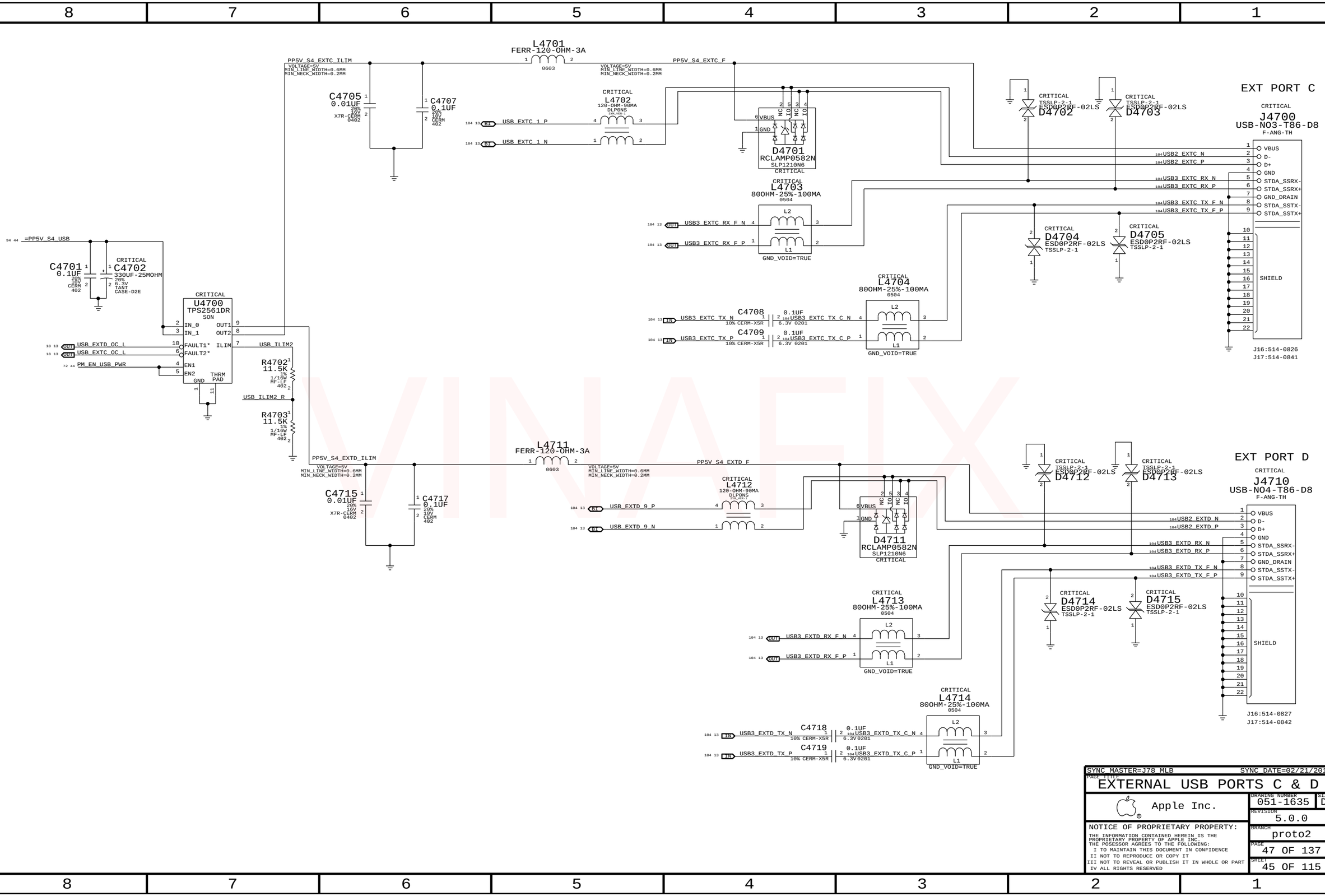

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE

EXTERNAL USB PORTS C & D

Apple Inc.

DRAWING NUMBER 051-1635 SIZE D

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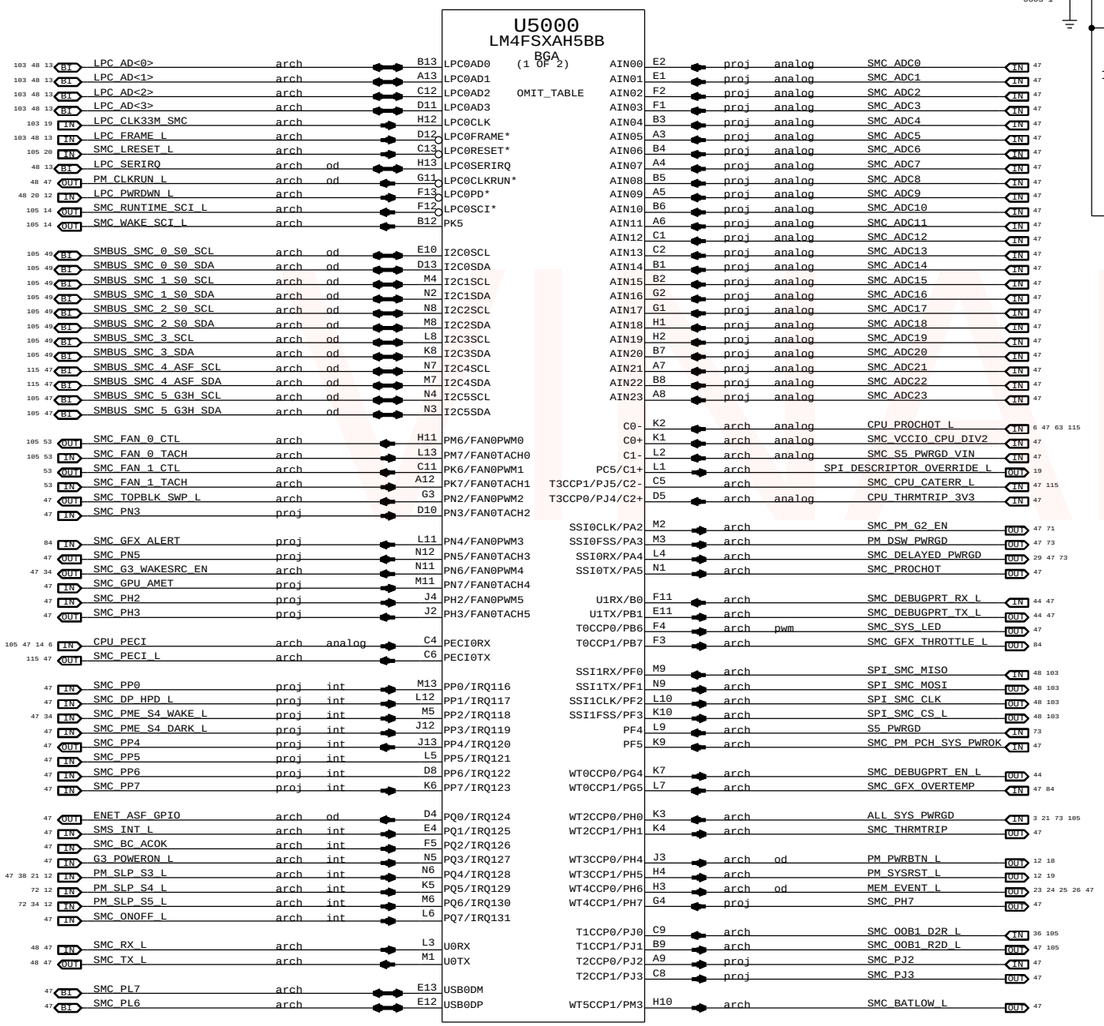
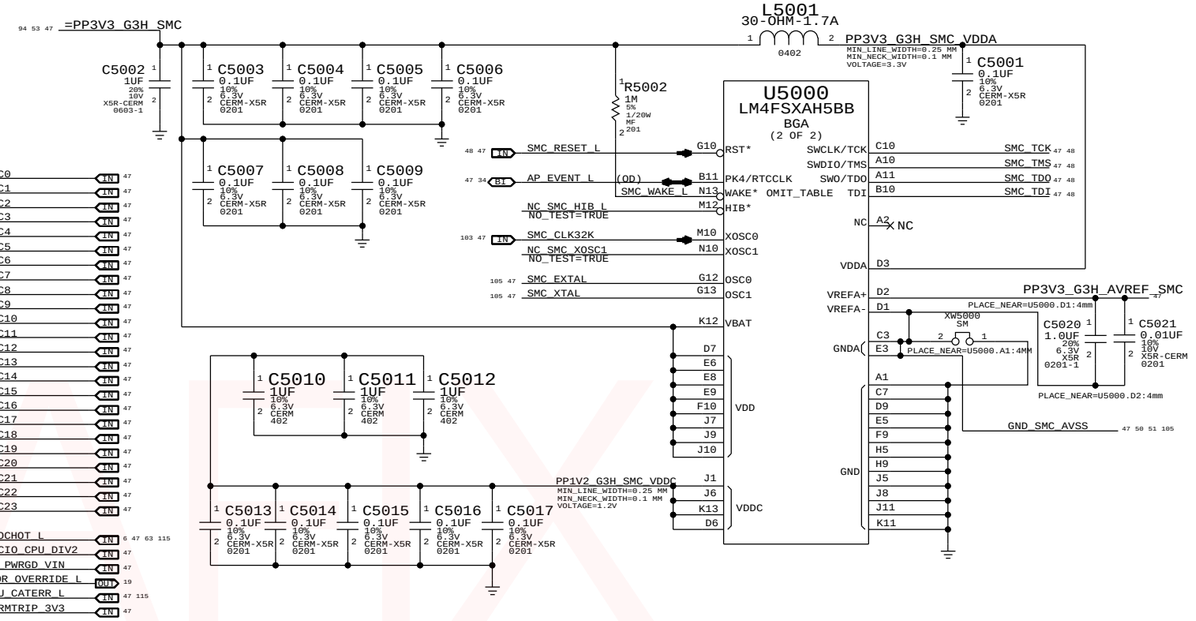
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.





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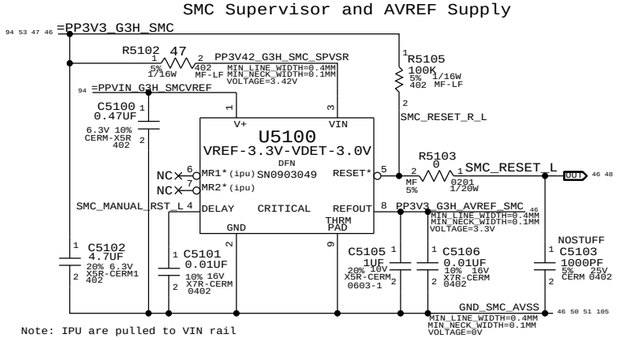
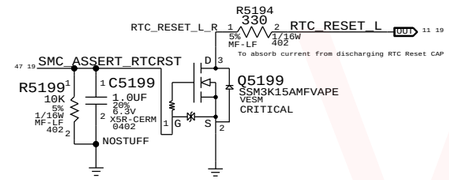
SMC Supervisor and AVREF Supply

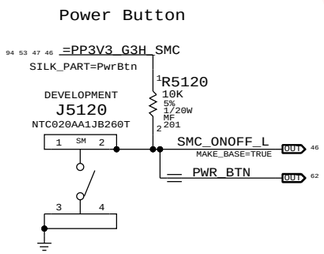


Note: IPU are pulled to VIN rail

SMC Controlled RTC Reset

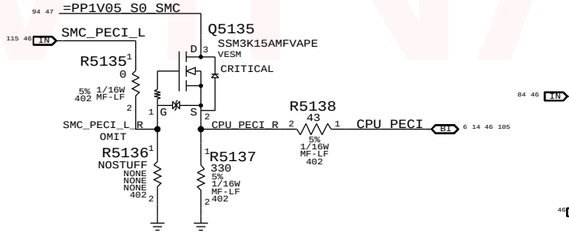


Power Button

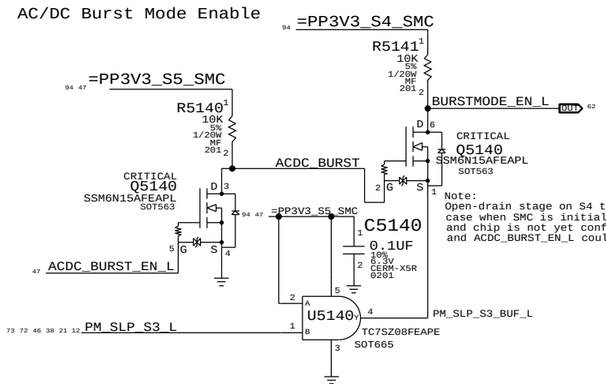


PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections



AC/DC Burst Mode Enable



Note:
Open-drain stage on S4 to account
case when SMC is initializing in S5,
and chip is not yet configured.
and ACDC_BURST_EN_L could be floating.

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE	50 105
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE	50 105
SMC_ADC2	VSNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	50 105
SMC_ADC3	ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	50 105
SMC_ADC4	VSNS_P1V5S0	MAKE_BASE=TRUE	51 105
SMC_ADC5	ISNS_P1V5S0	MAKE_BASE=TRUE	51 105
SMC_ADC6	VSNS_VDDQS3_DDR	MAKE_BASE=TRUE	51 105
SMC_ADC7	ISNS_VDDQS3_DDR	MAKE_BASE=TRUE	51 105
SMC_ADC8	VSNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	50 105
SMC_ADC9	ISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	50 105
SMC_ADC10	VSNS_CPUVCC	MAKE_BASE=TRUE	50 105
SMC_ADC11	ISNS_CPUVCC	MAKE_BASE=TRUE	50 105
SMC_ADC12	VSNS_GPUCORE_ALT	MAKE_BASE=TRUE	50 105
SMC_ADC13	ISNS_GPUCORE_ALT	MAKE_BASE=TRUE	50 105
SMC_ADC14	VSNS_HDDS0	MAKE_BASE=TRUE	50 105
SMC_ADC15	ISNS_HDDS0	MAKE_BASE=TRUE	50 105
Proto-1 SMC_ADC16	ISNS_P3V3S4_AP	MAKE_BASE=TRUE	50 105
SMC_ADC17	ISNS_P12VS0_HDD	MAKE_BASE=TRUE	50 105
SMC_ADC18	VSNS_P1V05S0_PCH	MAKE_BASE=TRUE	50 105
Proto-1 SMC_ADC19	ISNS_P12VS0_GPU_AUX	MAKE_BASE=TRUE	50 105
Proto-1 SMC_ADC20	VSNS_P3V3S5	MAKE_BASE=TRUE	51 105
Proto-1 SMC_ADC21	ISNS_SSDS0	MAKE_BASE=TRUE	51 105
Proto-1 SMC_ADC22	VSNS_GPU_VDDCI	MAKE_BASE=TRUE	51 105
Proto-1 SMC_ADC23	ISNS_GPU_VDDCI	MAKE_BASE=TRUE	51

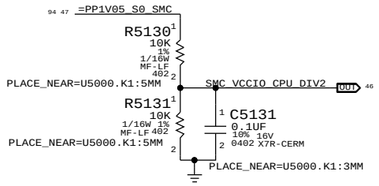
Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE	47
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE	35 105
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE	35 105
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE	62
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE	19 47
SMC_PL6	SMC_WIFI_PWR_EN	MAKE_BASE=TRUE	47

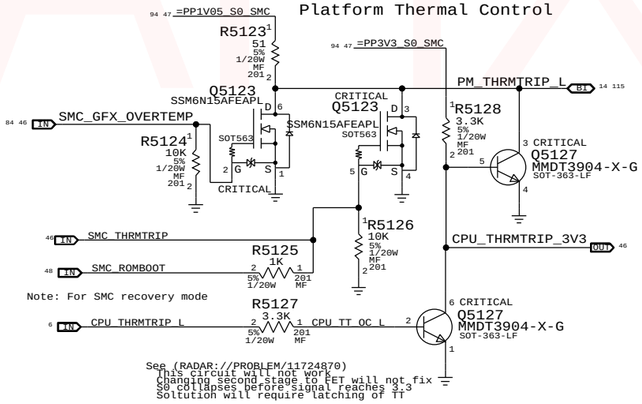
Unused Project-specific

SMC_PL7	NC_SMC_PL7	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE	NO_TEST=TRUE
TP for access if ZPB re-intstated			
115 46 SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE	NO_TEST=TRUE
115 46 SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE	NO_TEST=TRUE
105 46 SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE	NO_TEST=TRUE
105 46 SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	MAKE_BASE=TRUE	NO_TEST=TRUE
105 46 SMC_OOB1_R2D_L	NC_SMC_OOB1_R2D_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_BATLOW_L	NC_SMC_BATLOW_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PH3	NC_SMC_PH3	MAKE_BASE=TRUE	NO_TEST=TRUE

Comparator Reference



Platform Thermal Control

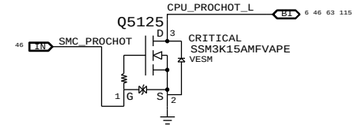


Note: For SMC recovery mode

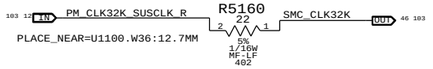
See (RADAR://PROBLEM/11724870)
This circuit will not work
Changing second stage to FET will not fix
50:c0 elapses before signal reaches 3.3
Solution will require latching of TT

PROCHOT Support

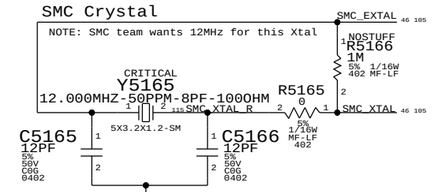
Level-shifter that allows SMC to drive PROCHOT



SMC 32KHz Clock



SMC Crystal



Arch Pull Up/Down

46 26 25 24 23 MEM_EVENT_L	R5170	10K	1	2 5% MF	1/20W 201
48 46 PM_CLKRUN_L	R5171	10K	1	2 5% MF	1/20W 201

46 ENET_ASF_GPIO	R5175	10K	1	2 5% MF	1/20W 201
46 G3_POWERON_L	R5176	10K	1	2 5% MF	1/20W 201
46 SMC_BC_ACOK	R5178	100K	1	2 5% MF	1/20W 201
46 SMC_SYS_LED	R5179	100K	1	2 5% MF	1/20W 201
46 SMS_INT_L	R5180	100K	1	2 5% MF	1/20W 201
46 34 SMC_PME_S4_WAKE_L	R5181	10K	1	2 5% MF	1/20W 201

46 34 AP_EVENT_L	R5185	10K	1	2 5% MF	1/20W 201
46 34 SMC_G3_WAKESRC_EN	R5118	100K	1	2 5% MF	1/20W 201
73 46 29 SMC_DELAYED_PWRGD	R5186	100K	1	2 5% MF-LF	1/16W 402
73 46 PM_DSW_PWRGD	R5184	100K	1	2 5% MF-LF	1/16W 402
71 46 SMC_PM_G2_EN	R5187	100K	1	2 5% MF	1/20W 201

Note:

Serial/JTAG Interface Pull-ups

48 46 SMC_TX_L	R5190	10K	1	2 5% MF	1/20W 201
48 46 SMC_RX_L	R5191	100K	1	2 5% MF	1/20W 201
48 46 SMC_TCK	R5195	10K	1	2 5% MF	1/20W 201
48 46 SMC_TDI	R5196	10K	1	2 5% MF	1/20W 201
48 46 SMC_TDO	R5197	10K	1	2 5% MF	1/20W 201
48 46 SMC_TMS	R5198	10K	1	2 5% MF	1/20W 201

46 44 SMC_DEBUGPRT_TX_L	R5192	20K	1	2 5% MF	1/20W 201
46 44 SMC_DEBUGPRT_RX_L	R5193	20K	1	2 5% MF	1/20W 201

Arch Pull Up/Down

73 18 12 PM_PCH_SYS_PWROK	R5148 0	5% MF	1/20W 0201	PM_PCH_SYS_PWROK	46
115 6 CPU_CATERR_L	R5149 0	5% MF	1/20W 0201	SMC_CPU_CATERR_L	46 115
46 SMC_TOPBLK_SWP_L	R5154 1K	5% MF	1/20W 201	PCH_STRP_TOPBLK_SWP_L	12

46 26 25 24 23 MEM_EVENT_L	R5170	10K	1	2 5% MF	1/20W 201
48 46 PM_CLKRUN_L	R5171	10K	1	2 5% MF	1/20W 201

46 ENET_ASF_GPIO	R5175	10K	1	2 5% MF	1/20W 201
46 G3_POWERON_L	R5176	10K	1	2 5% MF	1/20W 201
46 SMC_BC_ACOK	R5178	100K	1	2 5% MF	1/20W 201
46 SMC_SYS_LED	R5179	100K	1	2 5% MF	1/20W 201
46 SMS_INT_L	R5180	100K	1	2 5% MF	1/20W 201
46 34 SMC_PME_S4_WAKE_L	R5181	10K	1	2 5% MF	1/20W 201

46 34 AP_EVENT_L	R5185	10K	1	2 5% MF	1/20W 201
46 34 SMC_G3_WAKESRC_EN	R5118	100K	1	2 5% MF	1/20W 201
73 46 29 SMC_DELAYED_PWRGD	R5186	100K	1	2 5% MF-LF	1/16W 402
73 46 PM_DSW_PWRGD	R5184	100K	1	2 5% MF-LF	1/16W 402
71 46 SMC_PM_G2_EN	R5187	100K	1	2 5% MF	1/20W 201

48 46 SMC_TX_L	R5190	10K	1	2 5% MF	1/20W 201
48 46 SMC_RX_L	R5191	100K	1	2 5% MF	1/20W 201
48 46 SMC_TCK	R5195	10K	1	2 5% MF	1/20W 201
48 46 SMC_TDI	R5196	10K	1	2 5% MF	1/20W 201
48 46 SMC_TDO	R5197	10K	1	2 5% MF	1/20W 201
48 46 SMC_TMS	R5198	10K	1	2 5% MF	1/20W 201

46 44 SMC_DEBUGPRT_TX_L	R5192	20K	1	2 5% MF	1/20W 201
46 44 SMC_DEBUGPRT_RX_L	R5193	20K	1	2 5% MF	1/20W 201

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: SMC Support

Apple Inc.

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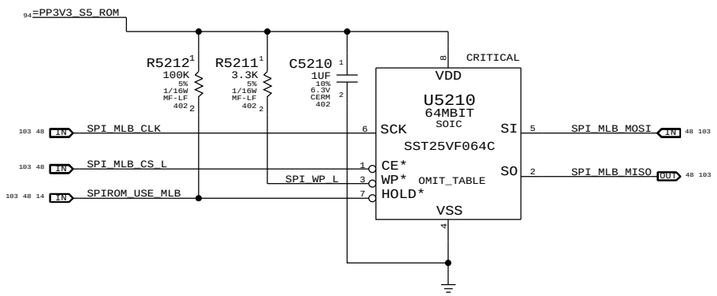
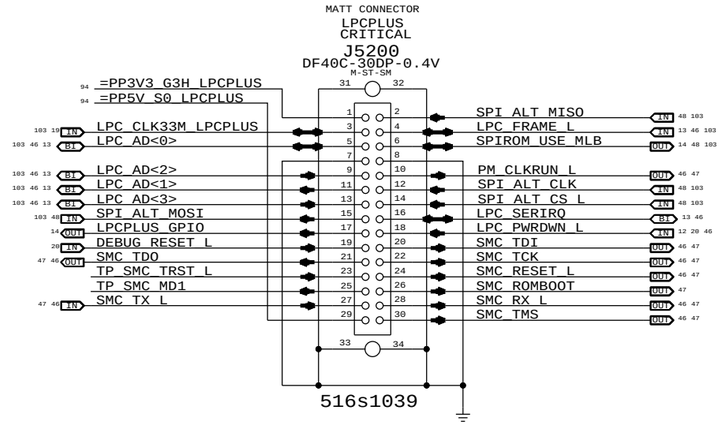
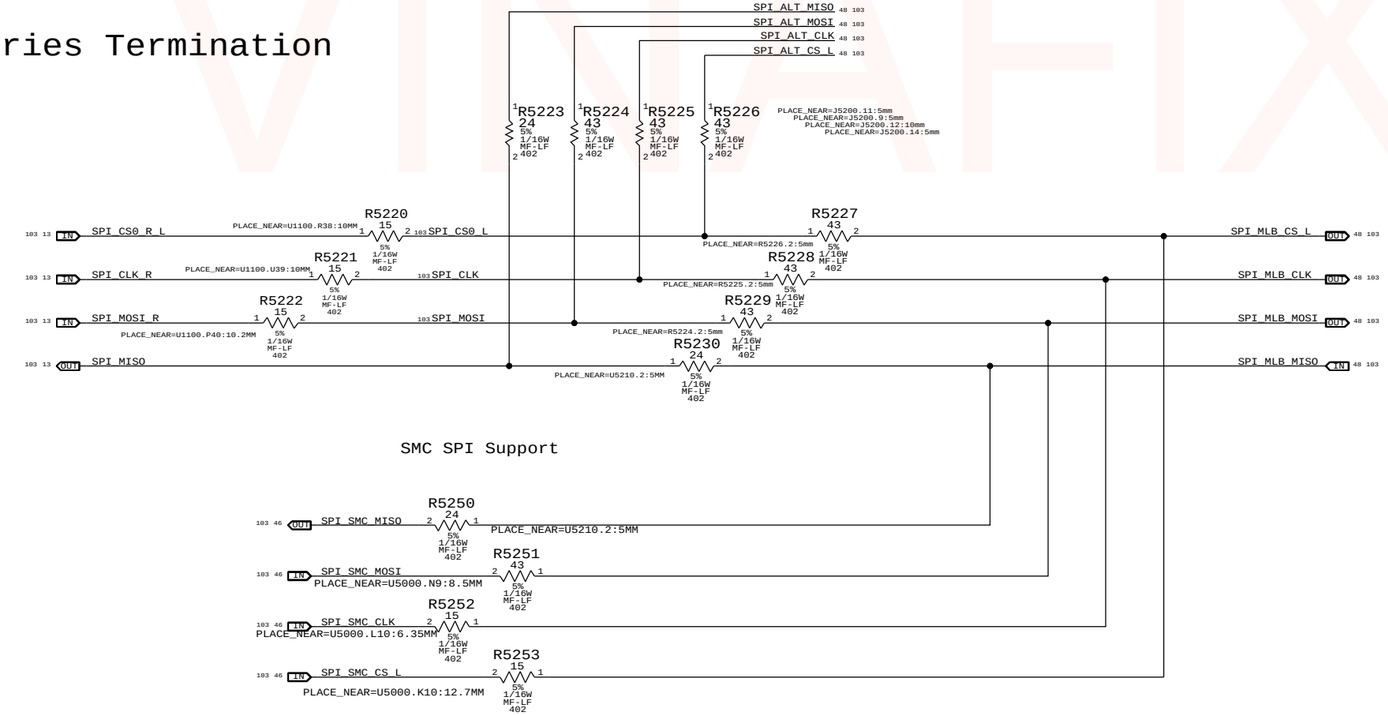
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
SPI and Debug Connector

Apple Inc.

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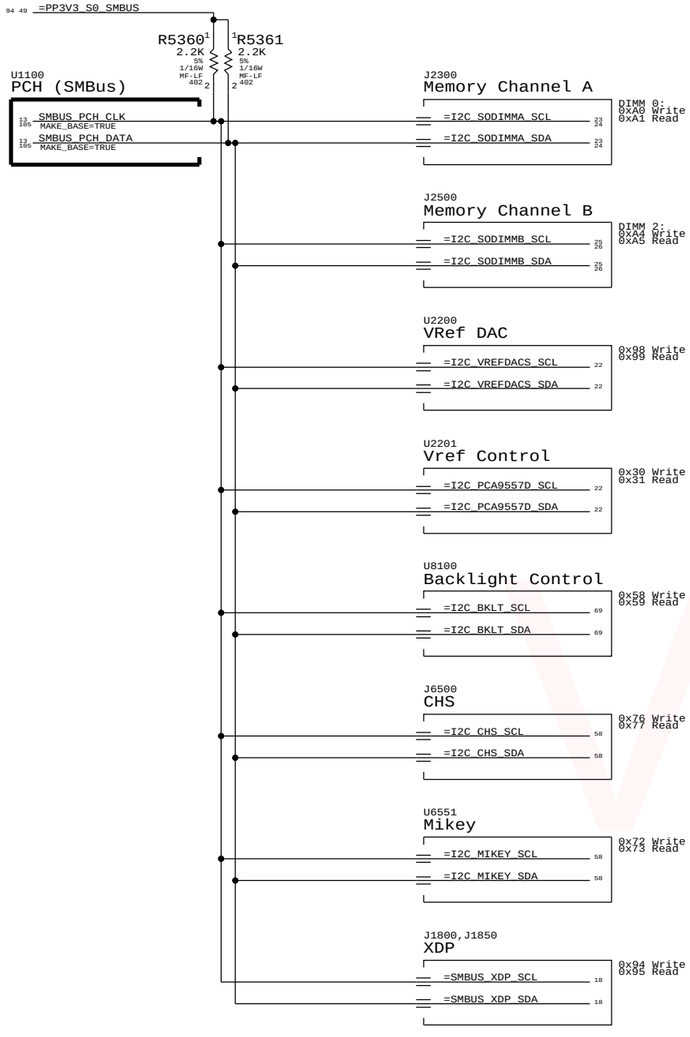

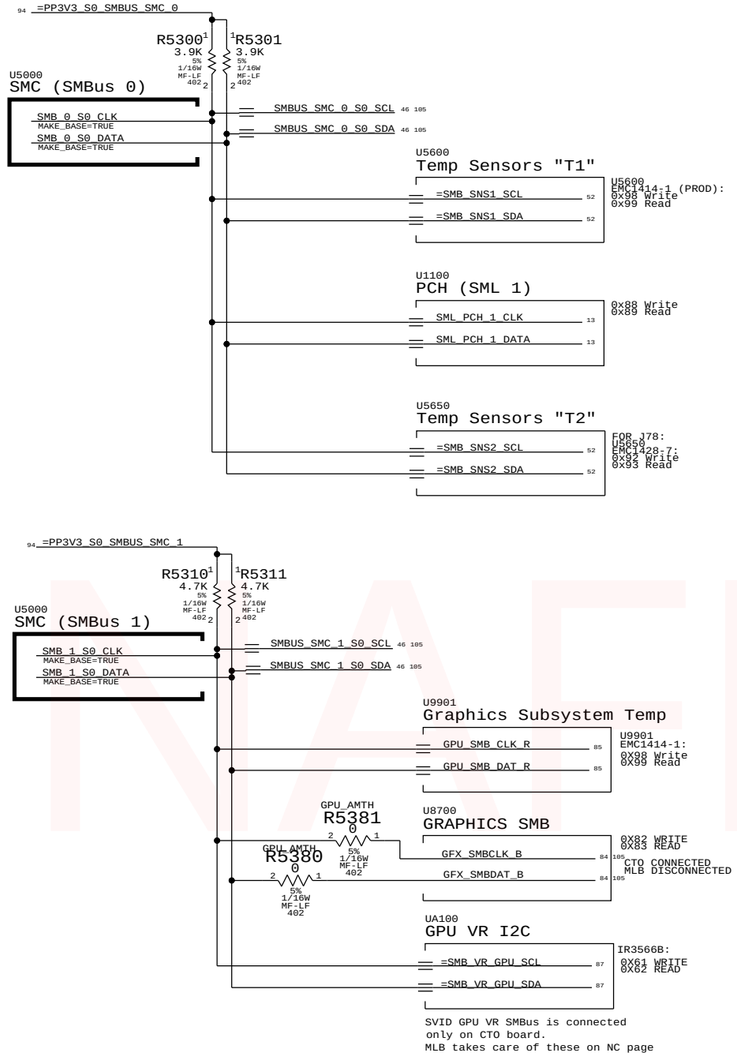

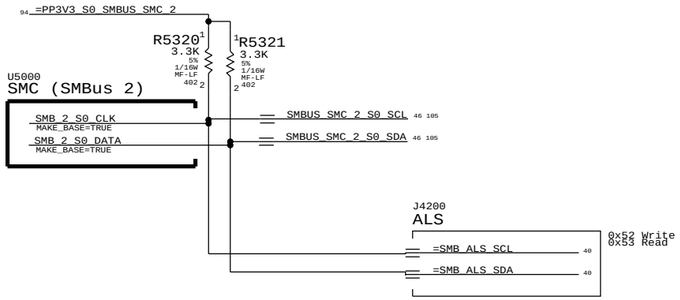

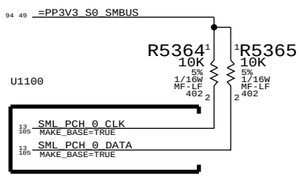

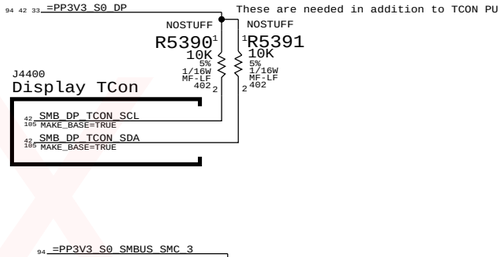

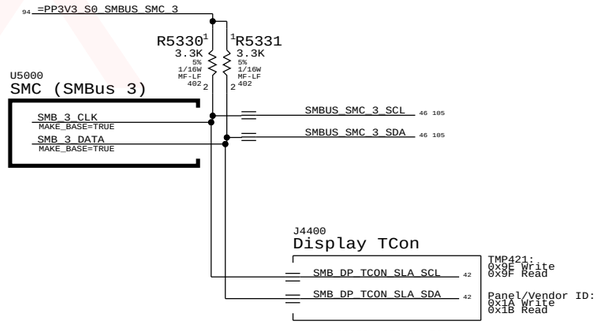

Line Legend
- Master
- Slave
- Mux

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

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SMBus Connections

Apple Inc.

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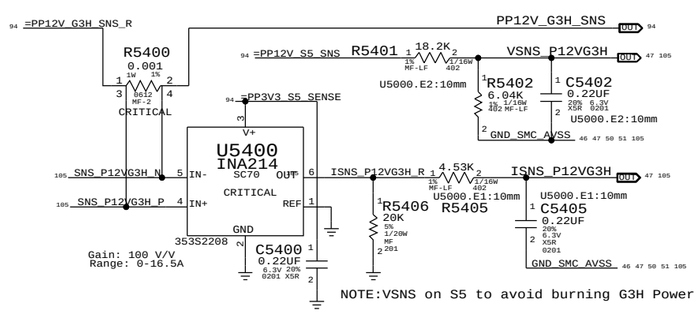
12V G3H (VD2R:ADC0/ID2R:ADC1)

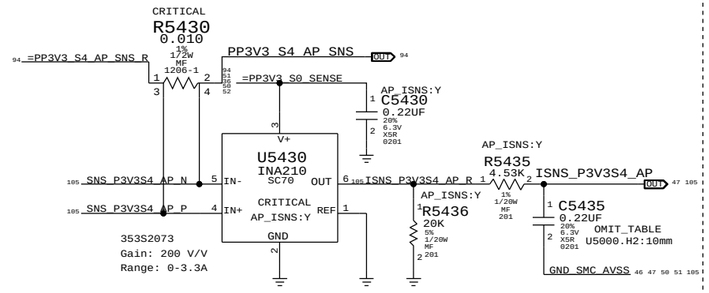
AC/DC lowside sense (System total)



NOTE:VSNS on S5 to avoid burning G3H Power

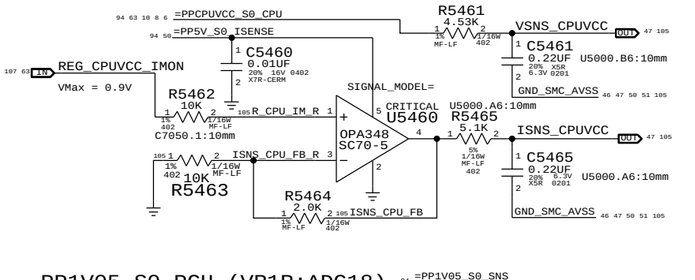
PP3V3_S4_AP (IW0R:ADC16)

Airport supply current sense



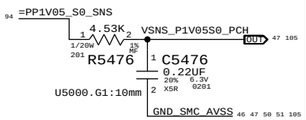
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22UF,201	C5435	AP_ISNS:Y
117S0201	1	RES,0 OHM,201	C5435	AP_ISNS:N

CPU Core (VC0C:ADC10/IC0C:ADC11)



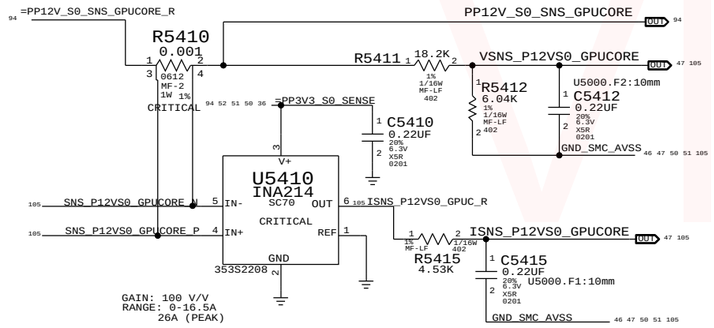
PP1V05_S0_PCH (VR1R:ADC18)

I/V-sense for PP1V05_S0_PCH
Since PP1V05 Vreg feedback is coming
from near GPU, place this sensor near PCH.



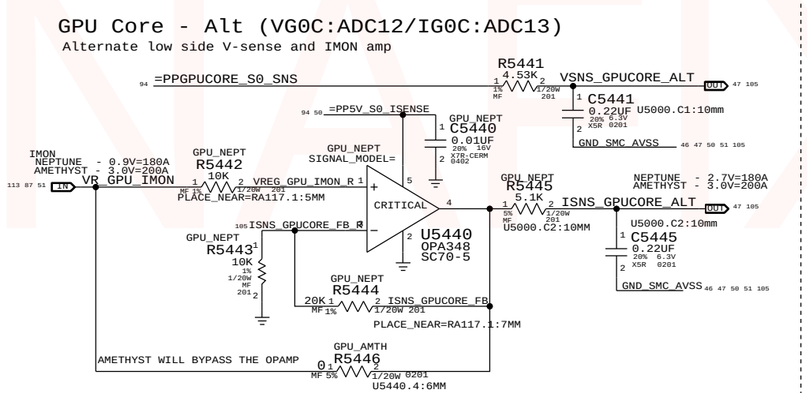
GPU Core (VG1C:ADC2/IG1C:ADC3)

GPU highside sense for GPU Core Regulator



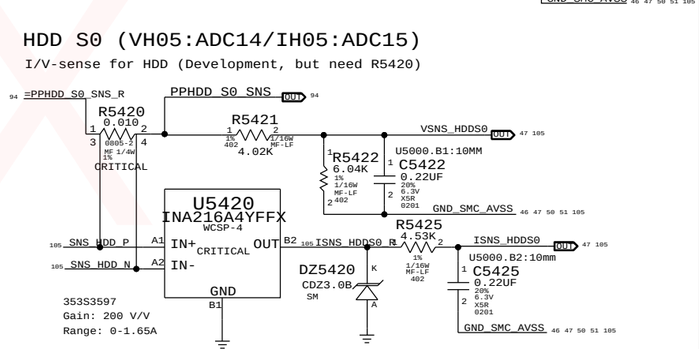
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp



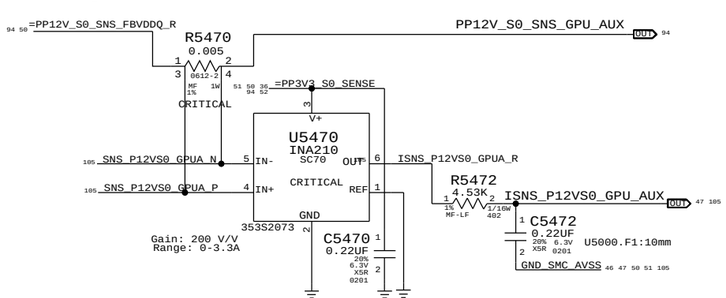
HDD S0 (VH05:ADC14/IH05:ADC15)

I/V-sense for HDD (Development, but need R5420)



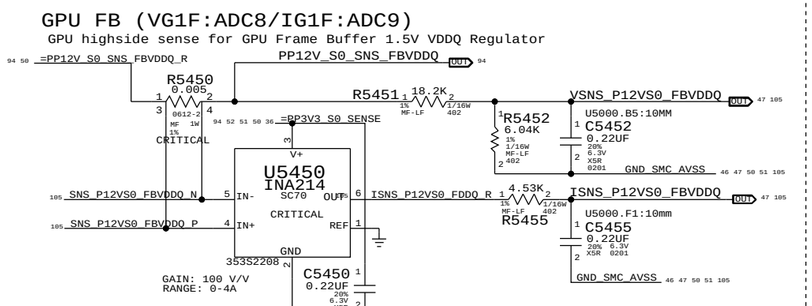
GPU AUX RAILS (IG1A:ADC19)

GPU highside sense for GPU 0.9V & 1.8V VR



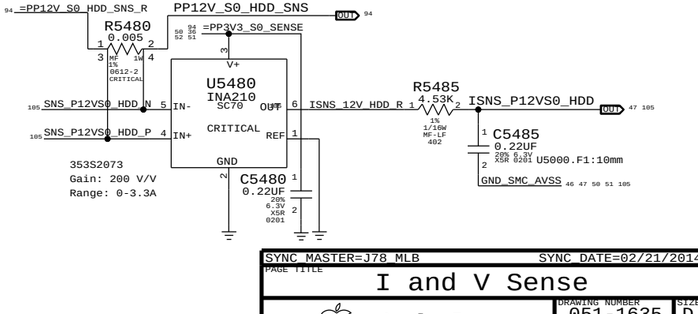
GPU FB (VG1F:ADC8/IG1F:ADC9)

GPU highside sense for GPU Frame Buffer 1.5V VDDQ Regulator



PP12V_S0_HDD (IH02:ADC17)

HDD 12V CURRENT SENSE



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: I and V Sense

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D

REVISION: 5.0.0

BRANCH: proto2

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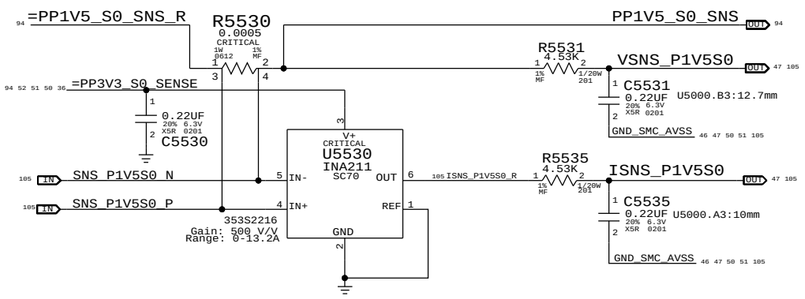
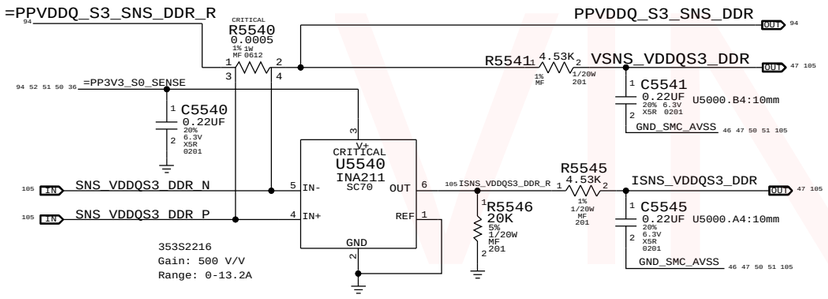
PP1V5_S0 (VC0M:ADC4/ IC0M:ADC5)

lowside sense for VCCVRM,PCH,CPU mem, audio



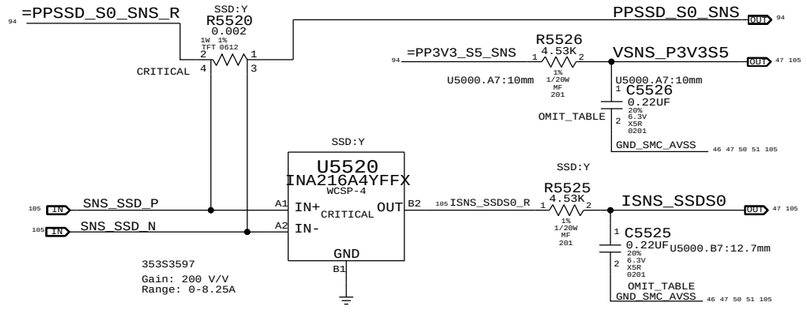
VDDQ S3 (VM0R:ADC6/ IM0R:ADC7)

VDDQ lowside sense for SO-DIMM modules



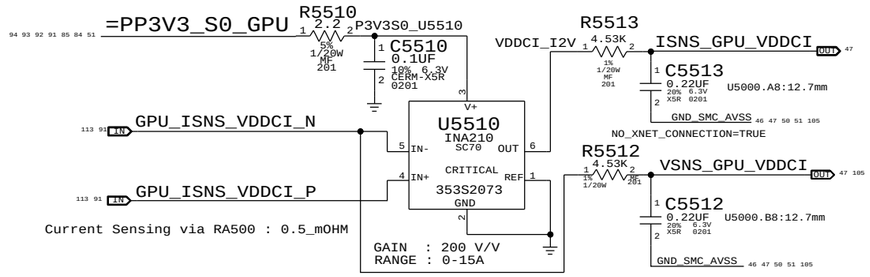
SSD S0 (VR3R:ADC20 / IH1R:ADC21)

I-sense for SSD / V-sense for PP3V3_S5)

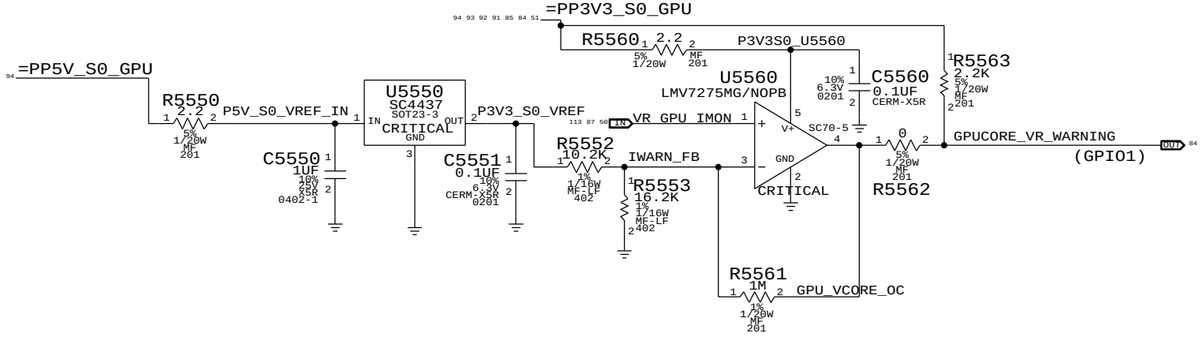


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0201	2	RES,0 OHM,201	C5525,C5526	SSD:N

GPU_VDDCI S0 (VG0S:ADC22 /IG0S: ADC23)



GPU VR OVER CURRENT WARNING



SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013

PAGE TITLE: I and V Sense(Continued)

Apple Inc.

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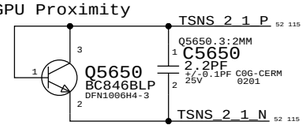
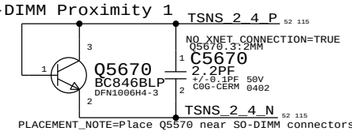
GPU Proximity



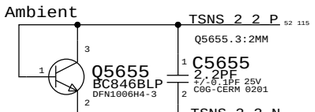
PLACEMENT_NOTE=Place Q5550 near GPU and GDDR5

SO-DIMM Proximity 1



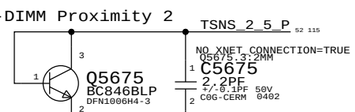
PLACEMENT_NOTE=Place Q5570 near SO-DIMM connectors (top left)

Ambient



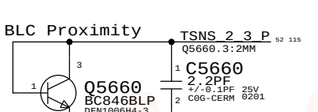
PLACEMENT_NOTE=Place Q5555 near bottom of board

SO-DIMM Proximity 2



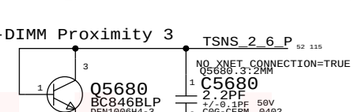
PLACEMENT_NOTE=Place Q5575 near SO-DIMM connectors (top right)

BLC Proximity



PLACEMENT_NOTE=Place Q5560 near BLC VR

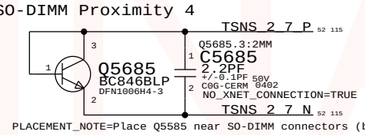
SO-DIMM Proximity 3



PLACEMENT_NOTE=Place Q5580 near SO-DIMM connectors (bottom left)

NEED TO FIND LOCATION

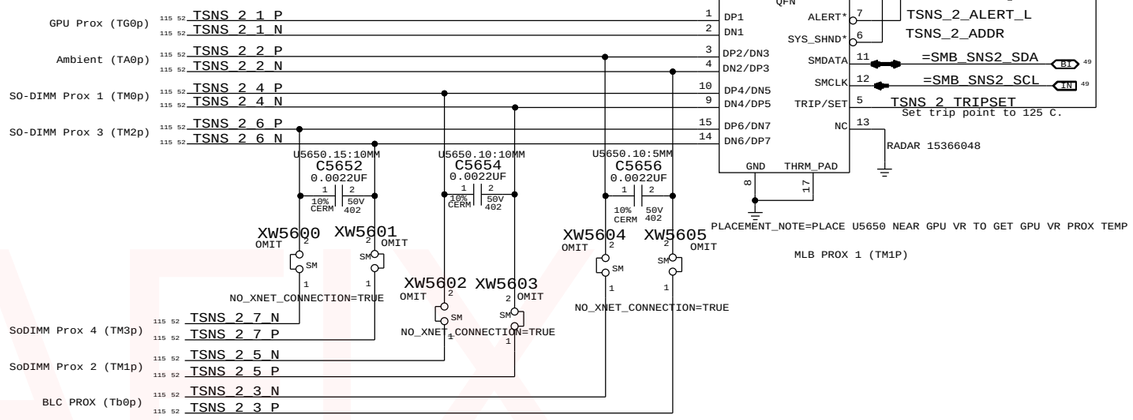
SO-DIMM Proximity 4



PLACEMENT_NOTE=Place Q5585 near SO-DIMM connectors (bottom right)

TEMP SENSOR T2 EMC1428: NEAR GPU VR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode



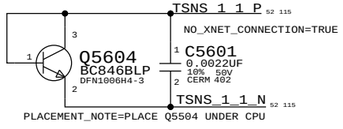
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

SNS T2: TEMP SENSOR IC

PLACEMENT_NOTE=PLACE U5650 NEAR GPU VR TO GET GPU VR PROX TEMP

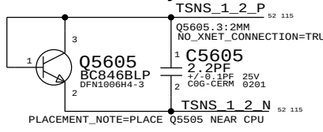
MLB PROX 1 (TM1P)

MLB Proximity



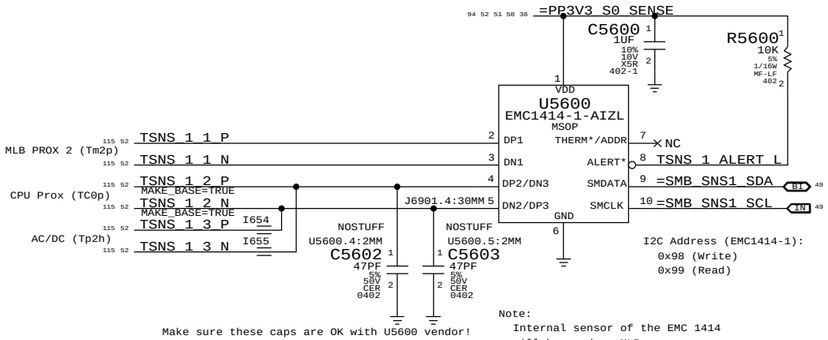
PLACEMENT_NOTE=PLACE Q5504 UNDER CPU

CPU Proximity



PLACEMENT_NOTE=PLACE Q5505 NEAR CPU

Temperature Sensor T1 EMC1414: Near PSU Conn



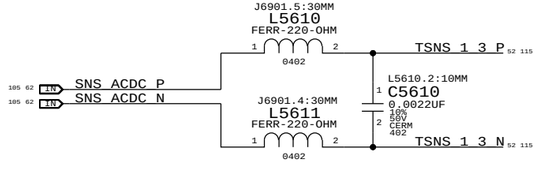
Make sure these caps are OK with U5600 vendor!

PLACEMENT_NOTE=PLACE U5600 NEAR PSU CONNECTOR

I2C Address (EMC1414-1):
0x98 (Write)
0x99 (Read)

Note:
Internal sensor of the EMC 1414 will be used as MLB sensor.
MLB PROX 0 (Tm0p)

AC/DC Via connector to diode inside PSU



SYNC_MASTER=J78_MLB	SYNC_DATE=02/21/2014
PAGE TITLE	Temperature Sensors
Apple Inc.	DRAWING NUMBER: 051-1635 SIZE: D
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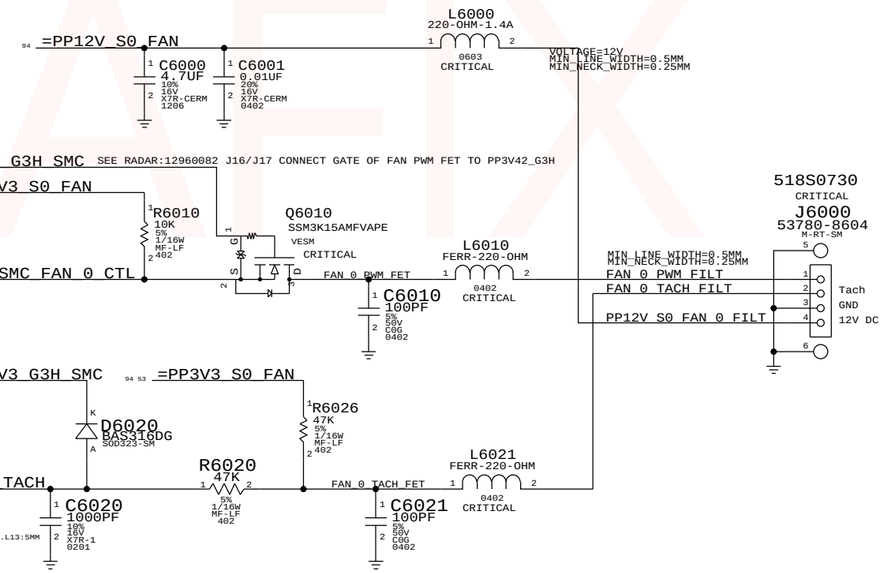
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

46 IN SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
MAKE_BASE=TRUE NO_TEST=TRUE

46 OUT SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
System Fan

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6100 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6101 4.7UF 20% 4V X5R-1 402

C6100 0.47UF 10% 10V X5R 0402

GND_AUDIO_CODEC

PP4V5_AUDIO_ANALOG

R6100 2.67K 1% 1/16W MF-LF 402

C6109 2.2UF 20% 6.3V CERM 402-LF

C6110 2.2UF 20% 6.3V CERM 402-LF

C6108 10UF 20% 16V POLY-TANT CASE-B2-SM

VBIAS_DAC

CS4206_FP

CS4206_FN

U6101 CS4206B QFN

C6102 0.47UF 10% 10V X5R 0402

C6103 10UF 20% 16V POLY-TANT CASE-B2-SM

C6105 1UF 10% 10V X5R 402-1

C6104 0.47UF 10% 10V X5R 0402

C6106 0.47UF 10% 10V X5R 0402

C6107 CRITICAL 10UF 10% 10V X5R-CERM 0402-1

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_CODEC

R6105 0 5% 1/16W MF-LF 402

TP_AUD_HP_L NC

TP_AUD_HP_R NC

CS4206_HPREF

DMICS 1 & 2 — AUD_DMIC_SDA1

NC — TP_AUD_GPIO_1

HP AMP CNTRL — AUD_GPIO_2

MAC SPKR AMP CNTRL — AUD_CODEC_MICBIAS

D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL — AUD_GPIO_3

AUD_SENSE_A

R6106 100K 1% 1/16W MF-LF 402

C6111 2.2UF 20% 6.3V CERM 402-LF

C6112 2.2UF 20% 6.3V CERM 402-LF

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

/SPDIF_OUT2

HPOUT_L — MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM — TP_AUD_HP_L NC

HPOUT_R — MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM — TP_AUD_HP_R NC

HPREF — MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM — CS4206_HPREF

LINEOUT_L1+ — AUD_LO1_L_P

LINEOUT_L1- — AUD_LO1_L_N

LINEOUT_R1+ — AUD_LO1_R_P

LINEOUT_R1- — AUD_LO1_R_N

HP AMP/LINE OUT

TWEETERS

RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

LINEOUT_L2+ — AUD_LO2_L_P

LINEOUT_L2- — AUD_LO2_L_N

LINEOUT_R2+ — AUD_LO2_R_P

LINEOUT_R2- — AUD_LO2_R_N

WOOFERS

MICBIAS — AUD_CODEC_MICBIAS

VCOM — CS4206_VCOM — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

LINEIN_L+ — NO_TEST=TRUE — AUD_LI_P_L NC

LINEIN_C- — NO_TEST=TRUE — AUD_LI_COM NC

LINEIN_R+ — NO_TEST=TRUE — AUD_LI_P_R NC

MICIN_L+ — AUD_MIC_INL_P

MICIN_L- — AUD_MIC_INL_N

MICIN_R+ — NO_TEST=TRUE — AUD_MIC_INP_R NC

MICIN_R- — NO_TEST=TRUE — AUD_MIC_INN_R NC

VREF+_ADC — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM — CS4206_VREF_ADC NC

DMIC_SCL — CS4206_DMIC_SCL — R6104 22 5% 1/16W MF-LF 402 — AUD_DMIC_CLK

DGND THRM PAD AGND

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK — BITCLK

HDA_SYNC — SYNC

HDA_SDIN0 — R6101 22 5% 1/16W MF-LF 402 — AUD_SDI_R — SDI

HDA_SDOUT — SDO

HDA_RST_L — RESET*

DP_INT_SPDIF_AUDIO — SPDIF_IN

AUD_SPDIF_CHIP — R6102 22 5% 1/16W MF-LF 402 — SPDIF_OUT

AUD_SPDIF_OUT

R6103 100K 1% 1/16W MF-LF 402

VL_HD

VL_IF

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

GND_AUDIO_DMIC — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=0V — XW6100 SM

C6113 CRITICAL 1UF 10% 25V TANT CASE-P3-HF

C6114 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM

C6115 0.47UF 10% 10V X5R 0402

R6107 100K 1% 1/16W MF-LF 402

R6108 100K 1% 1/16W MF-LF 402

R6109 100K 1% 1/16W MF-LF 402

R6110 100K 1% 1/16W MF-LF 402

R6111 100K 1% 1/16W MF-LF 402

GND_AUDIO_CODEC

Q6170 P S — DEVEL_AUDIO CRITICAL — Q6170 DMC2400UV SOT563 — Q6170 P G — R6170 0 5% 1/16W MF-LF 402

Q6170 N S — DEVEL_AUDIO CRITICAL — Q6170 DMC2400UV SOT563 — Q6170 N G — R6171 0 5% 1/16W MF-LF 402

Q6171 P S — DEVEL_AUDIO CRITICAL — Q6171 DMC2400UV SOT563 — Q6171 P G — R6172 0 5% 1/16W MF-LF 402

Q6171 N S — DEVEL_AUDIO CRITICAL — Q6171 DMC2400UV SOT563 — Q6171 N G — R6173 0 5% 1/16W MF-LF 402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=5V — PP5V_AUDIO_HPAMP

L6110 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=5V — =PP5V_S0_AUDIO

VR6101 TPS71745 CRITICAL — 4V5_REG_IN — 4V5_REG_EN — GND — NC — NR/FB — 4V5_NR — PP4V5_AUDIO_ANALOG MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.15MM VOLTAGE=4.5V

R6120 0 5% 1/16W MF-LF 402 — =PP3V3_S0_AUDIO

C6122 1UF 10% 10V X5R 402-1

XW6110 SM

C6123 0.1UF 10% 16V X7R-CERM 0402

C6124 1UF 10% 10V X5R 402-1 — MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

GND_AUDIO_CODEC — MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW6111 SM — GND_AUDIO_HPAMP MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

SYNC_MASTER=J78_MLB — SYNC_DATE=02/21/2014

PAGE TITLE: AUDIO: CODEC/REGULATORS

Apple Inc.

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R & L CHANNELS SWAPPED TO MAKE LAYOUT MORE LOGICAL

NO_XNET_CONNECTION=TRUE
C6262 100PF 5% 50V C0G 0402
R6262 19.6K 1% 1/16W MF-LF 402
MAX97220 OUTR

CRITICAL
C6261 33UF 20% 6.3V TANT CASE-A
AUD_LO1_R_N
R6261 26.1K 1% 1/16W MF-LF 402
MAX97220 INR_N

CRITICAL
C6263 33UF 20% 6.3V TANT CASE-A
AUD_LO1_R_P
R6263 26.1K 1% 1/16W MF-LF 402
MAX97220 INR_P

NO_XNET_CONNECTION=TRUE
R6264 19.6K 1% 1/16W MF-LF 402
C6264 100PF 5% 50V C0G 0402
AUD_HP_PORT_REF

NO_XNET_CONNECTION=TRUE
R6274 19.6K 1% 1/16W MF-LF 402
C6274 100PF 5% 50V C0G 0402

CRITICAL
C6273 33UF 20% 6.3V TANT CASE-A
AUD_LO1_L_P
R6273 26.1K 1% 1/16W MF-LF 402
MAX97220 INL_P

CRITICAL
C6271 33UF 20% 6.3V TANT CASE-A
AUD_LO1_L_N
R6271 26.1K 1% 1/16W MF-LF 402
MAX97220 INL_N

NO_XNET_CONNECTION=TRUE
R6272 19.6K 1% 1/16W MF-LF 402
MAX97220 OUTL
C6272 100PF 5% 50V C0G 0402
NO_XNET_CONNECTION=TRUE

PP5V_AUDIO_HPAMP
C6250 0.1UF 10% 16V X7R-CERM 0402
C6251 10UF 20% 10V X5R-CERM 0402-1
C6252 1UF 10% 10V X5R 402-1
C6253 1UF 10% 10V X5R 402-1
GND_AUDIO_HPAMP

R & L CHANNELS SWAPPED TO MAKE LAYOUT MORE LOGICAL

CRITICAL
U6250 MAX97220AETE TQFN
PVDD SVDD SVDD2 PGND SGND PVSS THM_PAD
MAX97220_INR_N
MAX97220_INR_P
MAX97220_INL_P
MAX97220_INL_N
MAX97220_SHDN_L
INL- INL+ INR+ INR- SHDN*
OUTL OUTR BIAS C1P C1N

MAX97220_BIAS
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
MAX97220_C1P
C6255 2.2UF 20% 25V X5R-CERM 0402-1
C6256 1UF 10% 10V X5R 402-1
MAX97220_C1N
MAX97220_PVSS
MIN_LINE_WIDTH=0.5MM
VOLTAGE=0V
C6254 2.2UF 20% 25V X5R-CERM 0402-1
GND_AUDIO_HPAMP

MAX97220_OUTR
MAX97220_OUTL
C6257 0.1UF 10% 16V X7R-CERM 0402
C6258 0.1UF 10% 10V X7R-CERM 0402
MAX97220_OUTL_ZOBEL
MAX97220_OUTR_ZOBEL
R6251 33 5% 1/16W MF-LF 402
R6252 33 5% 1/16W MF-LF 402
R6253 2.0K 5% 1/16W MF-LF 402
R6254 2.0K 5% 1/16W MF-LF 402
NOSTUFF Q6250 DMN2015UFDE UDFN
NOSTUFF Q6251 DMN2015UFDE UDFN

PP5V_AUDIO_HPAMP
NOSTUFF R6257 100K 5% 1/16W MF-LF 402
MUTE_SWITCH
NOSTUFF Q6252 SSM6N15AFEAPL SOT563
NC
NOSTUFF Q6252 SSM6N15AFEAPL SOT563
NOSTUFF R6255 0 5% 1/16W MF-LF 402
MAX97220_SHDN_L
MUTE_CONTROL
Q6252_GATE
NOSTUFF R6258 100K 5% 1/16W MF-LF 402
NOSTUFF R6259 100K 5% 1/16W MF-LF 402
NOSTUFF R6256 0 5% 1/16W MF-LF 402
GND_AUDIO_HPAMP

L6250 FERR-220-OHM 0402
AUD_GPIO_2
MAX97220_SHDN_L
R6250 100K 5% 1/16W MF-LF 402

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
AUDIO: HEADPHONE AMP

Apple Inc.

DRAWING NUMBER 051-1635 SIZE D
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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

94 57 IN =PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 10% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 220UF 20% 16V ELEC SM-CASE-C1-HF
CRITICAL C6307 220UF 20% 16V ELEC SM-CASE-C1-HF

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6300 FERR-1000-OHM 0402
L6301 FERR-1000-OHM 0402
L6302 FERR-1000-OHM 0402
L6303 FERR-1000-OHM 0402

61 54 IN AUD_LO2_L_N → C6308 1UF 10% 25V X5R 0402 → AUD_LAMP_RINC_P → AUD_LAMP_RIN_P
61 54 IN AUD_LO2_L_P → C6309 1UF 10% 25V X5R 0402 → AUD_LAMP_RINC_N → AUD_LAMP_RIN_N
61 55 54 IN AUD_LO1_L_P → C6310 4700PF 5% 50V NPO-C0G-CERM 0805 → AUD_LAMP_LINC_P → AUD_LAMP_LIN_P
61 55 54 IN AUD_LO1_L_N → C6311 4700PF 5% 50V NPO-C0G-CERM 0805 → AUD_LAMP_LINC_N → AUD_LAMP_LIN_N

34 35 36 37 PVDD

CRITICAL U6300 SSM3302 LFCSP

20	INR+		
19	INR-		
22	SDNR*	ONLY WOOFERS ON UNDER WINDOWS	57 56 IN AUD_SPKRAMP_WIN_SHDN_L
16	MONO	56 AUD_LAMP_MONO	
9	SDNL*	WOOFERS & TWEETERS ON UNDER MAC OS	57 56 IN AUD_SPKRAMP_MAC_SHDN_L
11	INL+		
12	INL-		
21	GAIN	56 AUD_LAMP_GAIN	
8	VREG/AVDD	56 AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)	
23	REGEN	94 60 57 54 48 =PP3V3_S0_AUDIO	
7 24 41	AGND	THERM_PAD	
31 32 33 38 39 40	PGND		
17	THERM	TP_AUD_LAMP_THERM NC	
30	BOOTR+	AUD_LAMP_BOOTRP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) → C6313 0.22UF 20% 25V X5R 603	
28 29	OUTR+		
26 27	OUTR-		
25	BOOTR-	AUD_LAMP_BOOTRN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) → C6314 0.22UF 20% 25V X5R 603	
10	EDGE	AUD_LAMP_EDGE 56	
1	BOOTL+	AUD_LAMP_BOOTLP (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) → C6315 0.22UF 20% 25V X5R 603	
2 3	OUTL+		
4 5	OUTL-		
6	BOOTL-	AUD_LAMP_BOOTLN (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM) → C6316 0.22UF 20% 25V X5R 603	
18	NC	NC	
13	NC	NC	
14	TEST		
15	TEST		

C6317 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

NO_XNET_CONNECTION=TRUE
CRITICAL L6305 110-OHM-3A DLY5ATN111SQ2 SM_VSS-1
AUD_LAMP_OUTPR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) 56 → AUD_LAMP_OUTNR 56
AUD_LAMP_OUTPR 56 → AUD_LAMP_OUTNR (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM) 56
AUD_SPKR_LWFR_OUT_P → OUT 59 61
NO_XNET_CONNECTION=TRUE
CRITICAL C6323 1000PF 5% 25V CERM 0402
AUD_SPKR_LWFR_OUT_N → OUT 59 61

NO_XNET_CONNECTION=TRUE
CRITICAL L6307 110-OHM-3A DLY5ATN111SQ2 SM_VSS-1
AUD_LAMP_OUTPL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
AUD_LAMP_OUTNL (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM)
AUD_SPKR_LTWT_OUT_P → OUT 59 61
NO_XNET_CONNECTION=TRUE
CRITICAL C6324 1000PF 5% 25V CERM 0402
AUD_SPKR_LTWT_OUT_N → OUT 59 61

NO_XNET_CONNECTION=TRUE
CRITICAL C6320 1000PF 5% 25V CERM 0402
CRITICAL C6322 1000PF 5% 25V CERM 0402
NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE
CRITICAL C6319 1000PF 5% 25V CERM 0402
CRITICAL C6321 1000PF 5% 25V CERM 0402
NO_XNET_CONNECTION=TRUE

L6308 FERR-1000-OHM 0402
54 IN AUD_CODEC_MICBIAS → AUD_SPKRAMP_MAC_SHDN_L OUT 56 57
R6301 100K 5% 1/16W MF-LF 402
NOSTUFF C6312 100PF 5% 50V C0G 0402

R6308 0 5% 1/16W MF-LF 402
54 IN AUD_GPIO_3 → AUD_SPKRAMP_WIN_SHDN_L OUT 56 57
R6309 100K 5% 1/16W MF-LF 402
NOSTUFF C6318 100PF 5% 50V C0G 0402

EDGE RATE CONTROL

	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

56 AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402
NOSTUFF R6305 0 5% 1/16W MF-LF 402
AUD_LAMP_EDGE 56
AUD_LAMP_MONO 56
NOSTUFF R6306 0 5% 1/16W MF-LF 402
AUD_LAMP_GAIN 56
R6303 0 5% 1/16W MF-LF 402
R6307 47K 5% 1/16W MF-LF 402

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014
PAGE TITLE: AUDIO: LEFT SPKR AMP
Apple Inc.
DRAWING NUMBER 051-1635 SIZE D
REVISION 5.0.0
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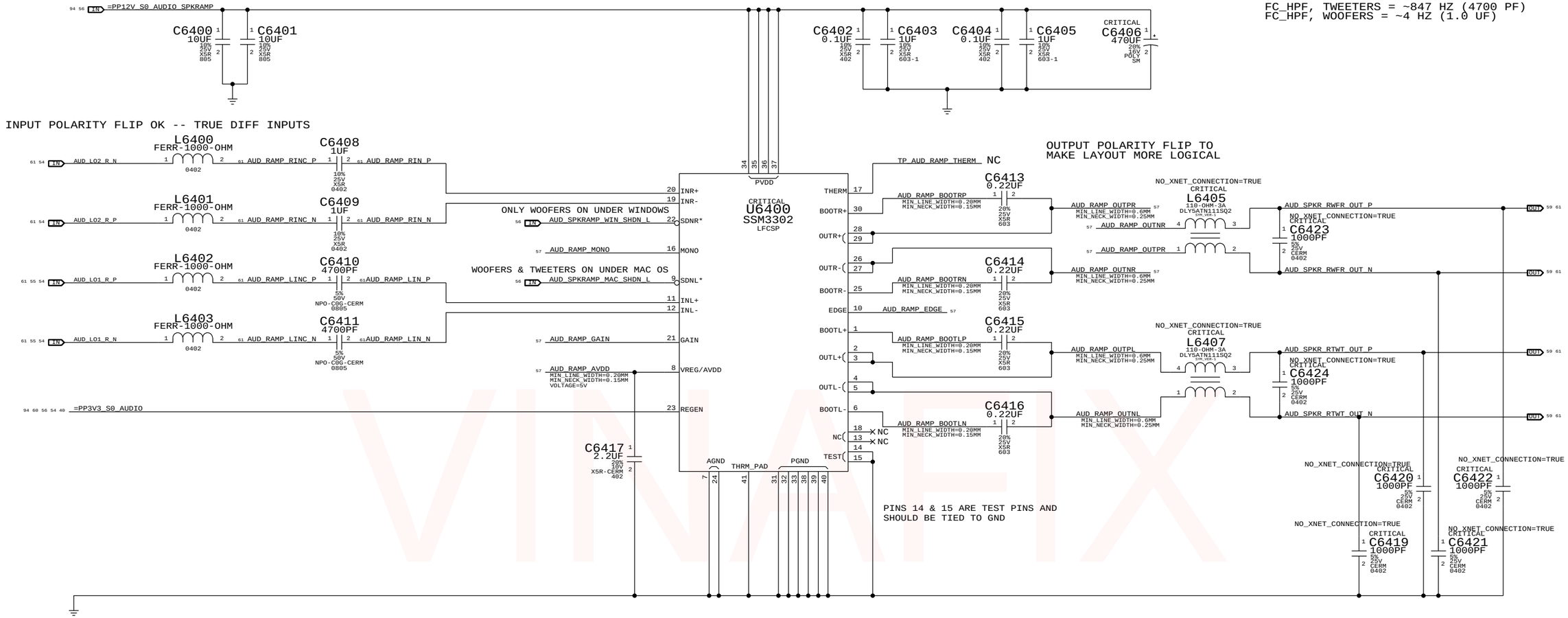
RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

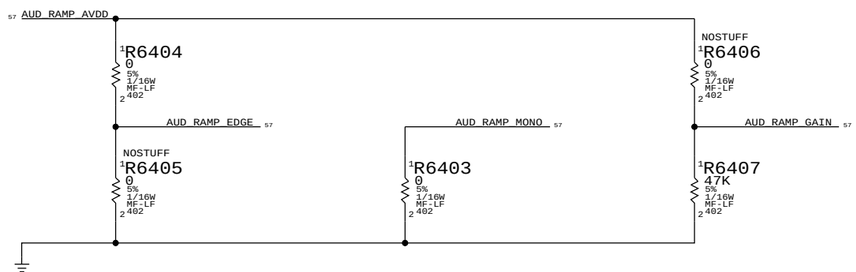


EDGE RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
AUDIO: RIGHT SPKR AMP

Apple Inc.

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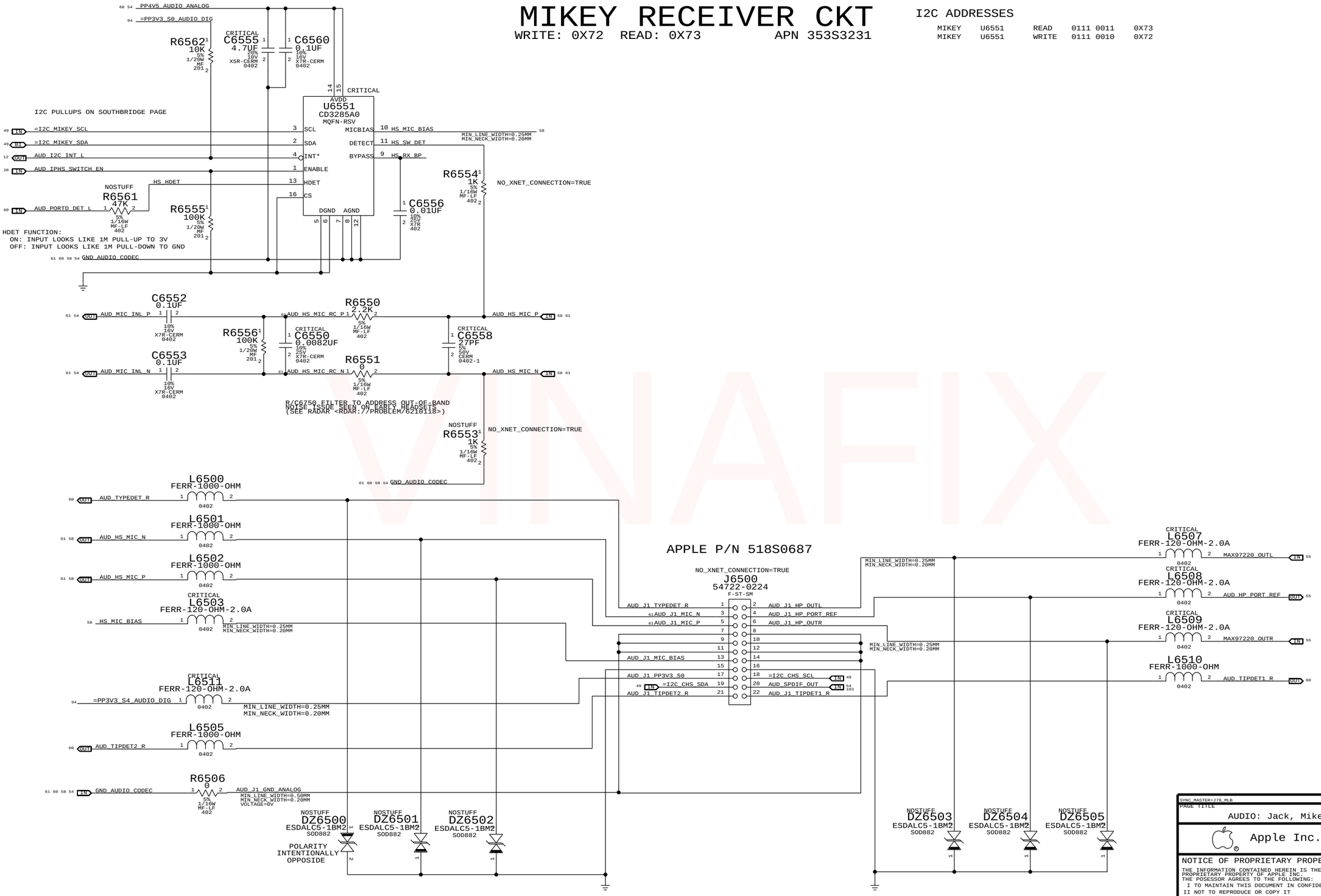
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2012

PAGE TITLE: AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

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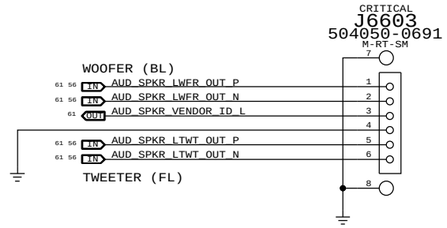
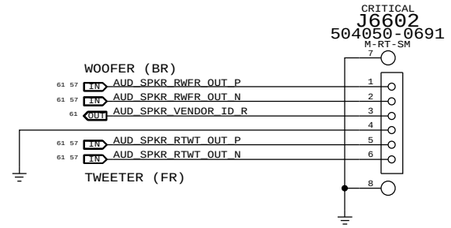
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862





SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
Audio: Spkr/Mic Conn.

Apple Inc.

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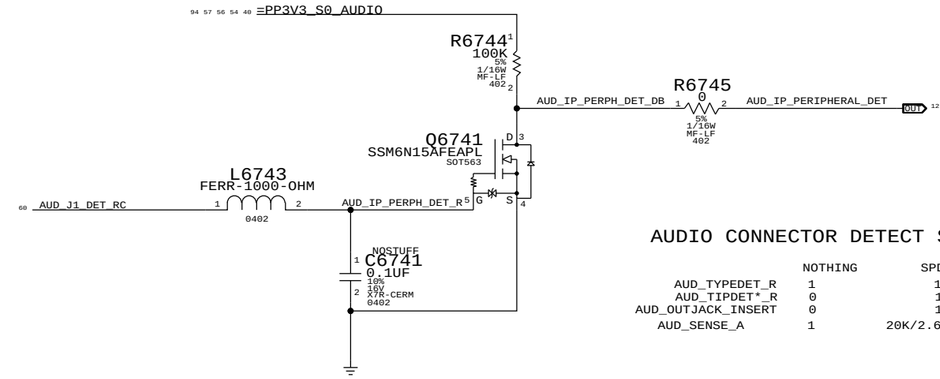
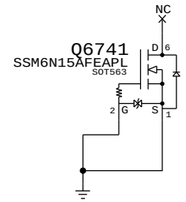
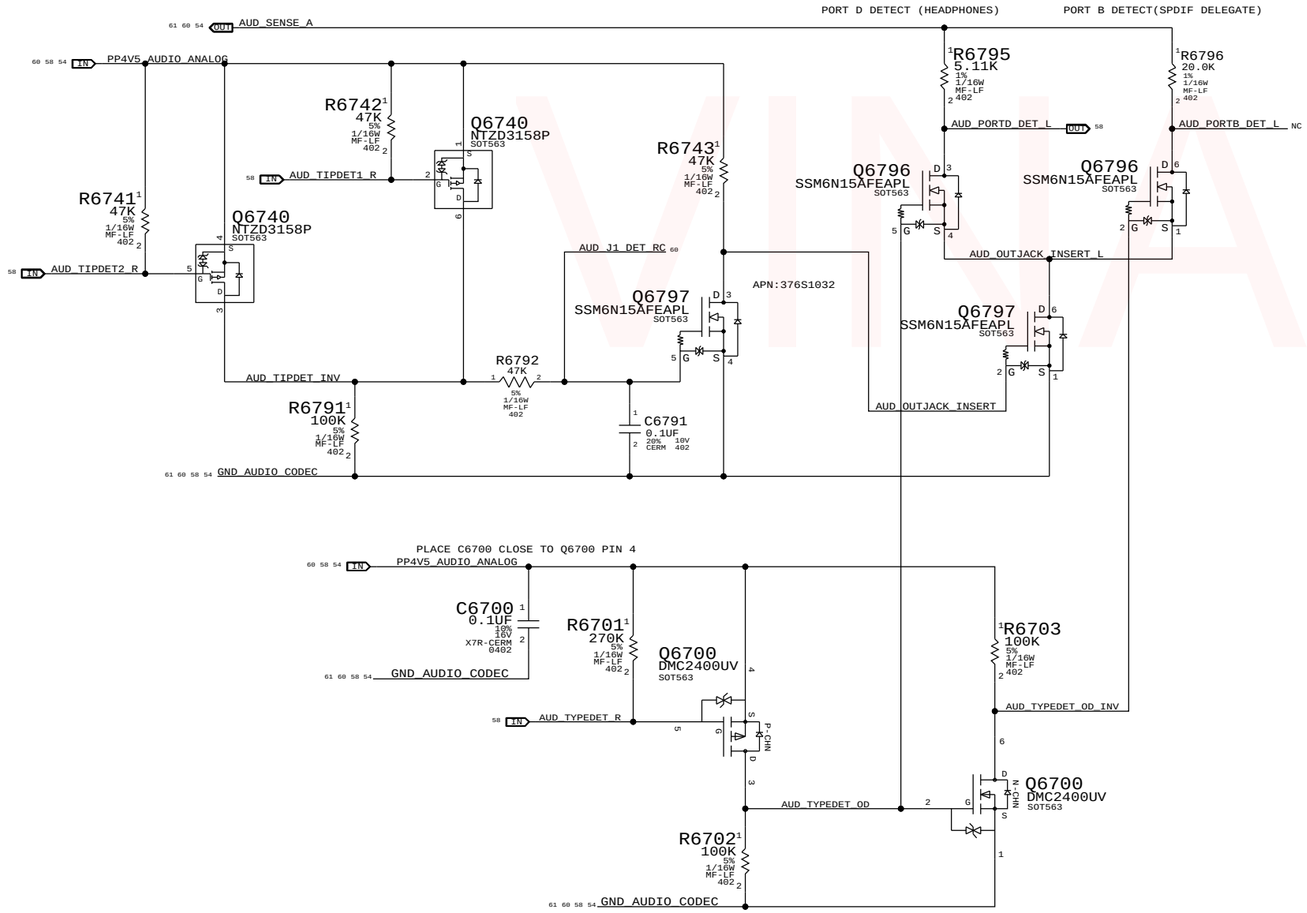
IPHS HS Detect Debounce CKT



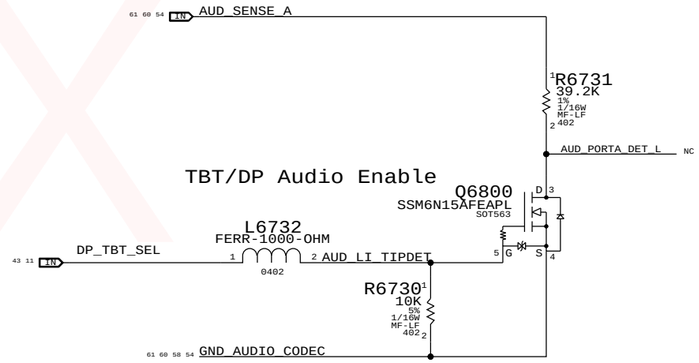
AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





Target Display Mode Detect



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

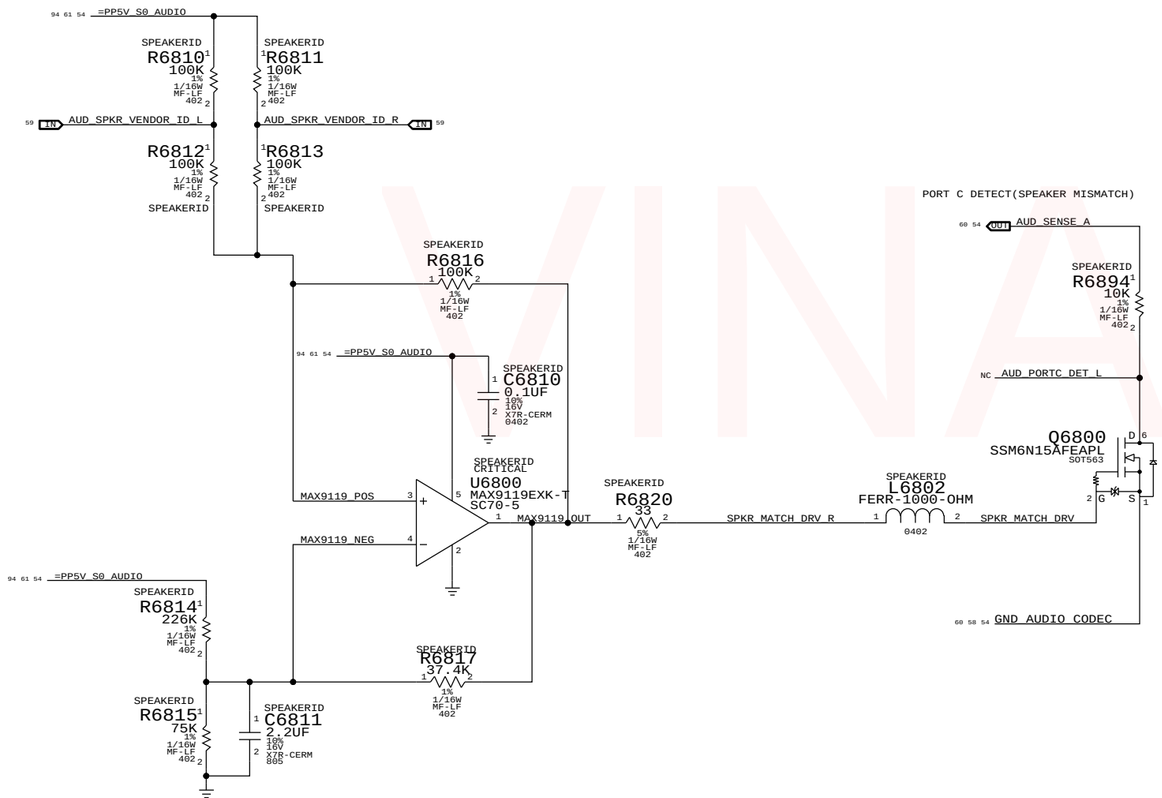
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
1535 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	54 55 56
1536 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	54 55 56
1537 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	55
1538 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	55
1539 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	54 55 57
1540 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	54 55 57
1541 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	55
1542 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	55
1543 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	54 56
1544 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	54 56
1545 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	54 57
1546 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	54 57
1547 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	57
1548 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	57
1549 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	57
1550 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	57
1551 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	57
1552 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	57
1553 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	57
1554 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	57
1555 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	56
1556 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	56
1557 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	56
1558 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	56
1559 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	56
1560 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	56
1561 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	56
1562 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	56
1563 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_P	55
1564 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_N	55
1565 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_P	55
1566 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_N	55
1567 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	57 59
1568 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	57 59
1569 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	57 59
1570 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	57 59
1571 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	56 59
1572 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	56 59
1573 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	56 59
1574 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	56 59
1575 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	54 58
1576 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	54 58
1577 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	58
1578 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	58
1579 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	58
1580 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	58
1581 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	58
1582 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	58

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: AUDIO: Speaker ID

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D
REVISION: 5.0.0
BRANCH: proto2
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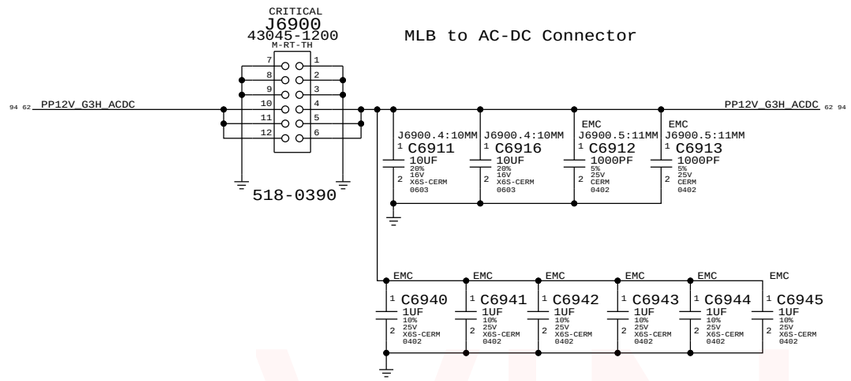
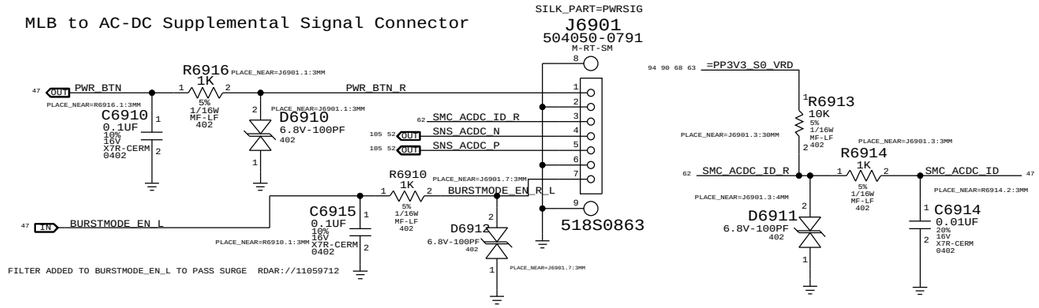
SHEET: 61 OF 115

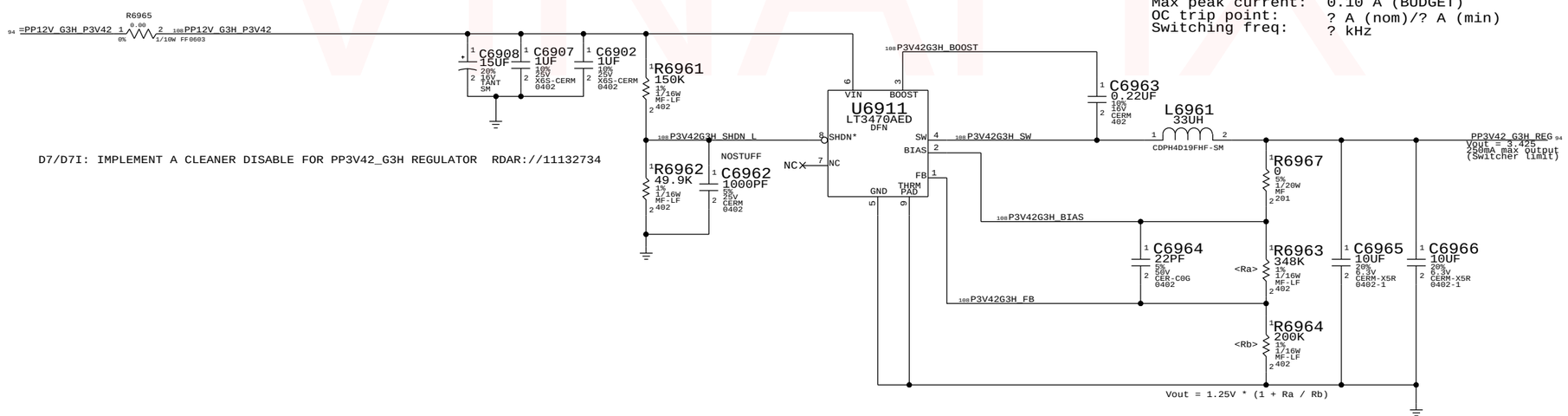




D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734

SYNC_MASTER=J78 MLB SYNC_DATE=02/21/2014

PAGE TITLE
Power Connectors / VReg G3Hot

Apple Inc.

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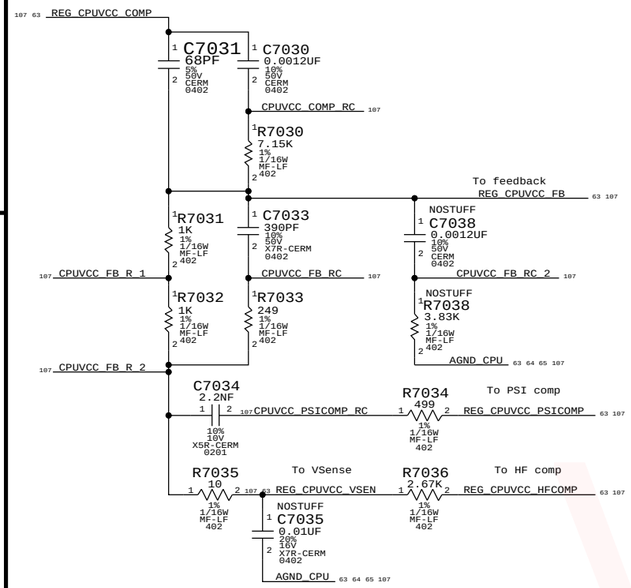
CPU VCC S0 Regulator

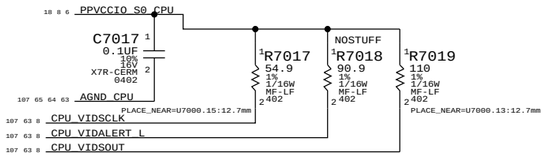
OC trip point: 114 A

Switching freq: 403 kHz = 5 E10 / R7003

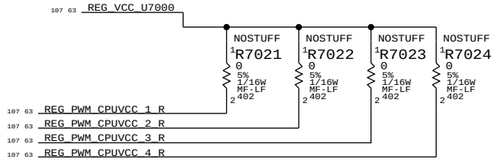
Compensation and feedback

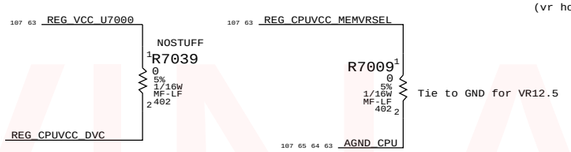


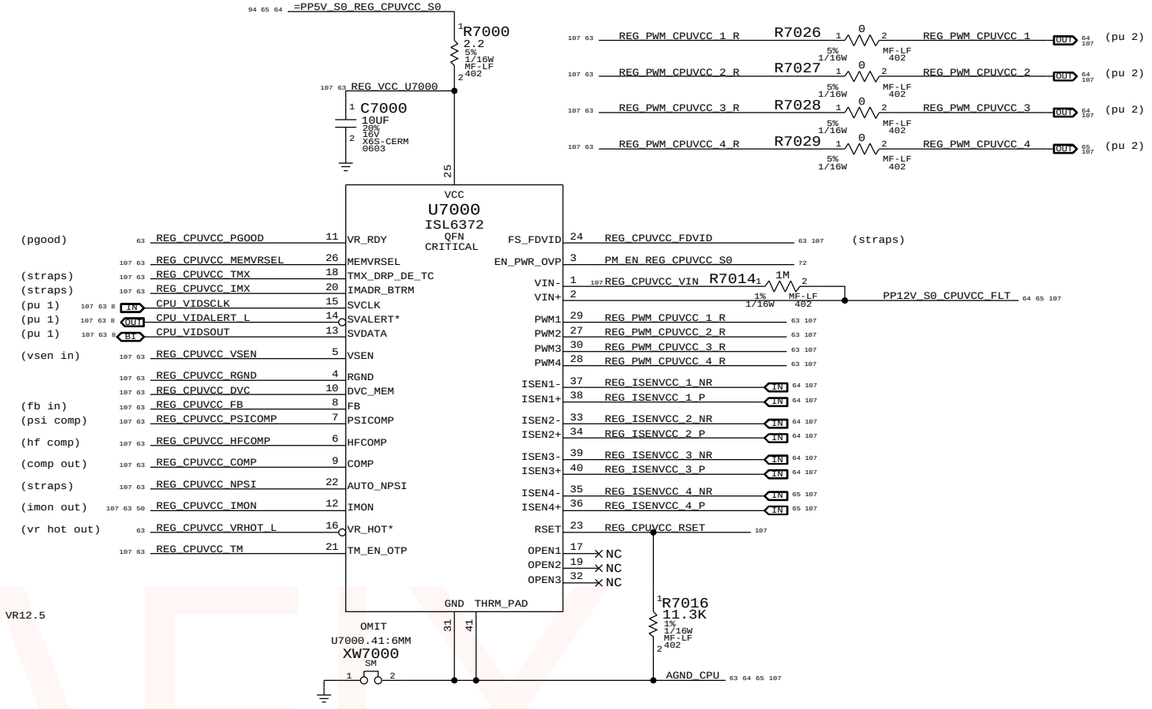
Pull-ups 1



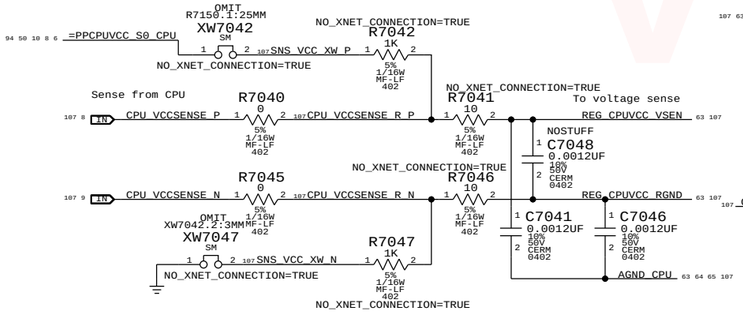
Pull-ups 2



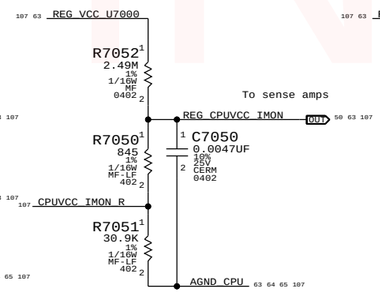




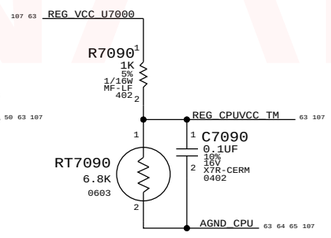
Voltage sense input



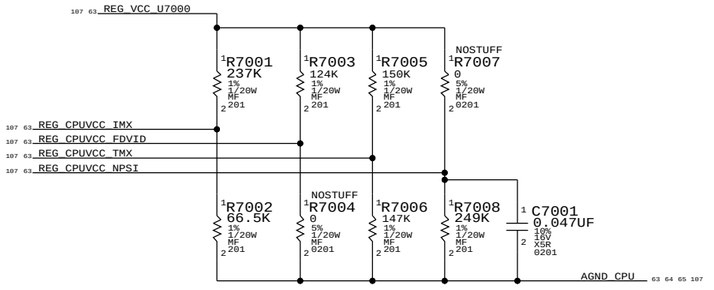
IMON output



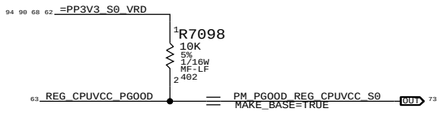
Temp measurement



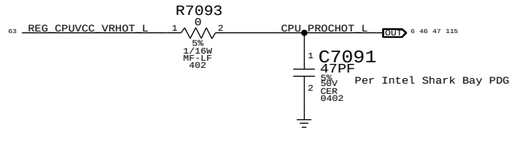
Straps



Power goods



VRHot to ProcHot



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: VReg CPU VCC Cntl

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D

REVISION: 5.0.0

BRANCH: proto2

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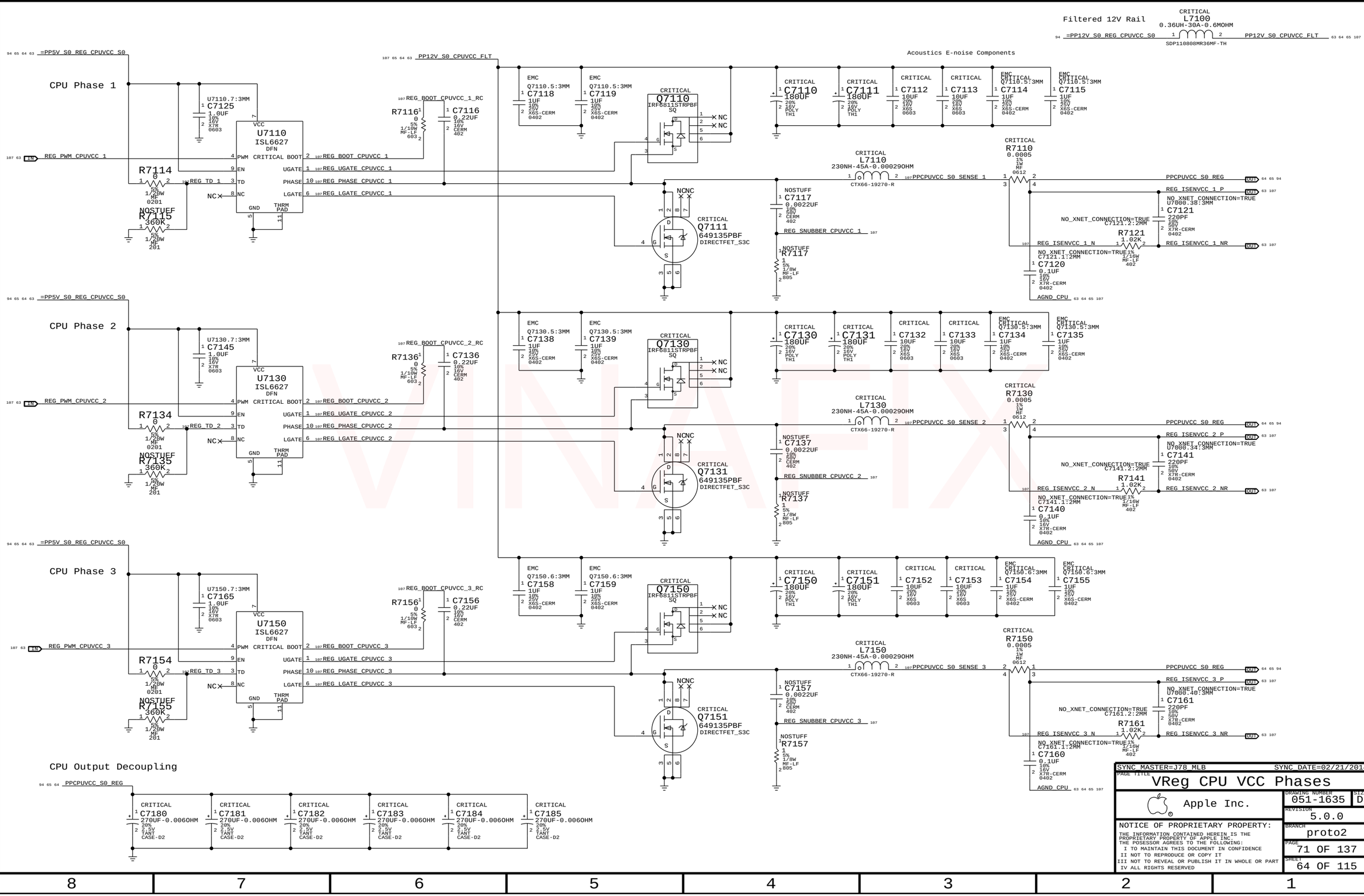
Filtered 12V Rail
CRITICAL L7100 0.36UH-30A-0.6MOHM SDP110808MR36MF-TH
=PP12V_S0_REG_CPUVCC_S0
PP12V_S0_CPUVCC_FLT
Acoustics E-noise Components
CPU Phase 1
U7110 ISL6627 DFN
REG_PWM_CPUVCC_1
REG_BOOT_CPUVCC_1
REG_UGATE_CPUVCC_1
REG_PHASE_CPUVCC_1
REG_LGATE_CPUVCC_1
REG_TD_1
Q7110 IRF6811STRPBF SQ
Q7111 649135PBF DIRECTFET_S3C
L7110 230NH-45A-0.00029OHM CTX66-19270-R
PPCPUVCC_S0_SENSE_1
REG_SNUBBER_CPUVCC_1
PPCPUVCC_S0_REG
REG_ISENVCC_1_P
REG_ISENVCC_1_N
REG_ISENVCC_1_NR
CPU Phase 2
U7130 ISL6627 DFN
REG_PWM_CPUVCC_2
REG_BOOT_CPUVCC_2
REG_UGATE_CPUVCC_2
REG_PHASE_CPUVCC_2
REG_LGATE_CPUVCC_2
REG_TD_2
Q7130 IRF6811STRPBF SQ
Q7131 649135PBF DIRECTFET_S3C
L7130 230NH-45A-0.00029OHM CTX66-19270-R
PPCPUVCC_S0_SENSE_2
REG_SNUBBER_CPUVCC_2
PPCPUVCC_S0_REG
REG_ISENVCC_2_P
REG_ISENVCC_2_N
REG_ISENVCC_2_NR
CPU Phase 3
U7150 ISL6627 DFN
REG_PWM_CPUVCC_3
REG_BOOT_CPUVCC_3
REG_UGATE_CPUVCC_3
REG_PHASE_CPUVCC_3
REG_LGATE_CPUVCC_3
REG_TD_3
Q7150 IRF6811STRPBF SQ
Q7151 649135PBF DIRECTFET_S3C
L7150 230NH-45A-0.00029OHM CTX66-19270-R
PPCPUVCC_S0_SENSE_3
REG_SNUBBER_CPUVCC_3
PPCPUVCC_S0_REG
REG_ISENVCC_3_P
REG_ISENVCC_3_N
REG_ISENVCC_3_NR
CPU Output Decoupling
PPCPUVCC_S0_REG
C7180 270UF-0.006OHM
C7181 270UF-0.006OHM
C7182 270UF-0.006OHM
C7183 270UF-0.006OHM
C7184 270UF-0.006OHM
C7185 270UF-0.006OHM
SYNC_MASTER=J78_MLB
SYNC_DATE=02/21/2014
PAGE TITLE
VReg CPU VCC Phases
Apple Inc.
DRAWING NUMBER 051-1635
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REVISION 5.0.0
BRANCH proto2
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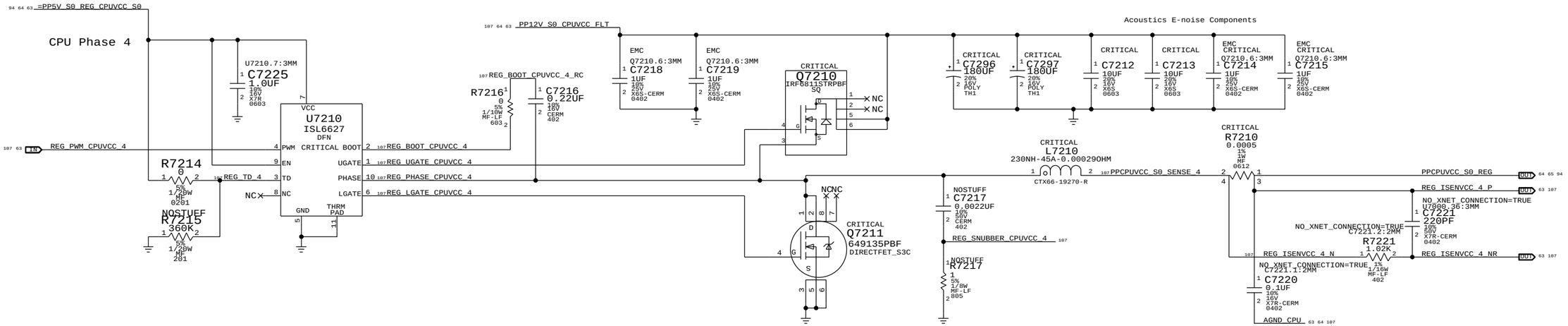

CPU Output Decoupling

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: VReg CPU VCC Phase 4

Apple Inc.

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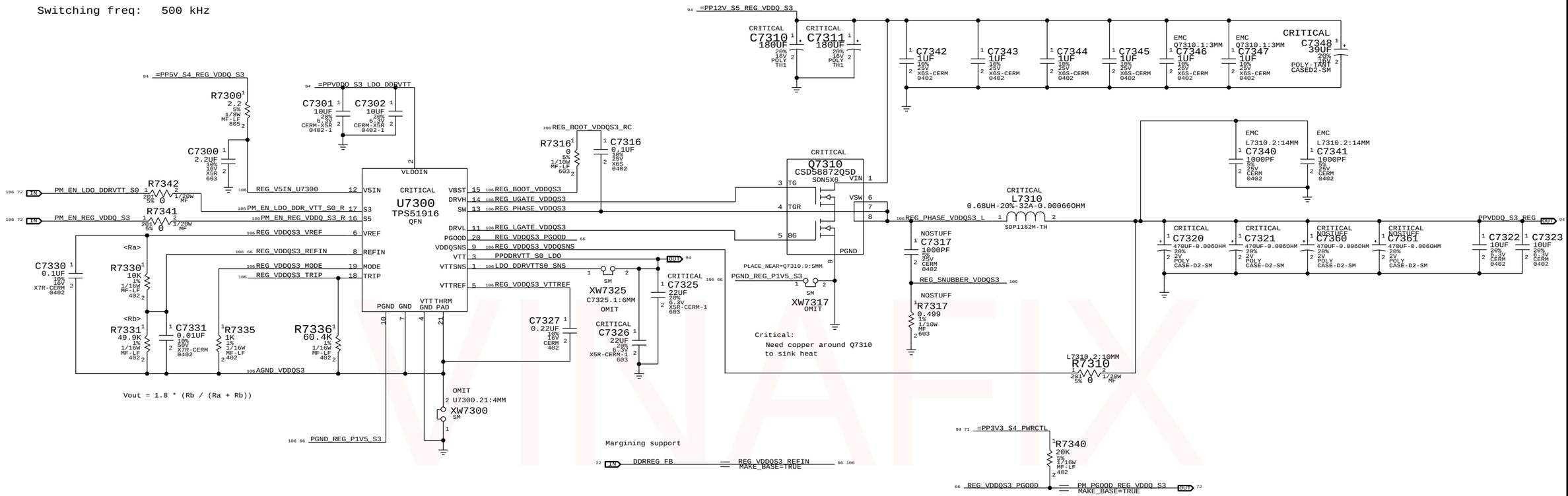
VDDQ (1.5V) S3 REGULATOR

OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5\ *\ Rds(Q7310)} + \frac{0.65625}{L7310\ *\ f(switch)}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: VReg VDDQ S3

Apple Inc.

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3.3V S5 Regulator

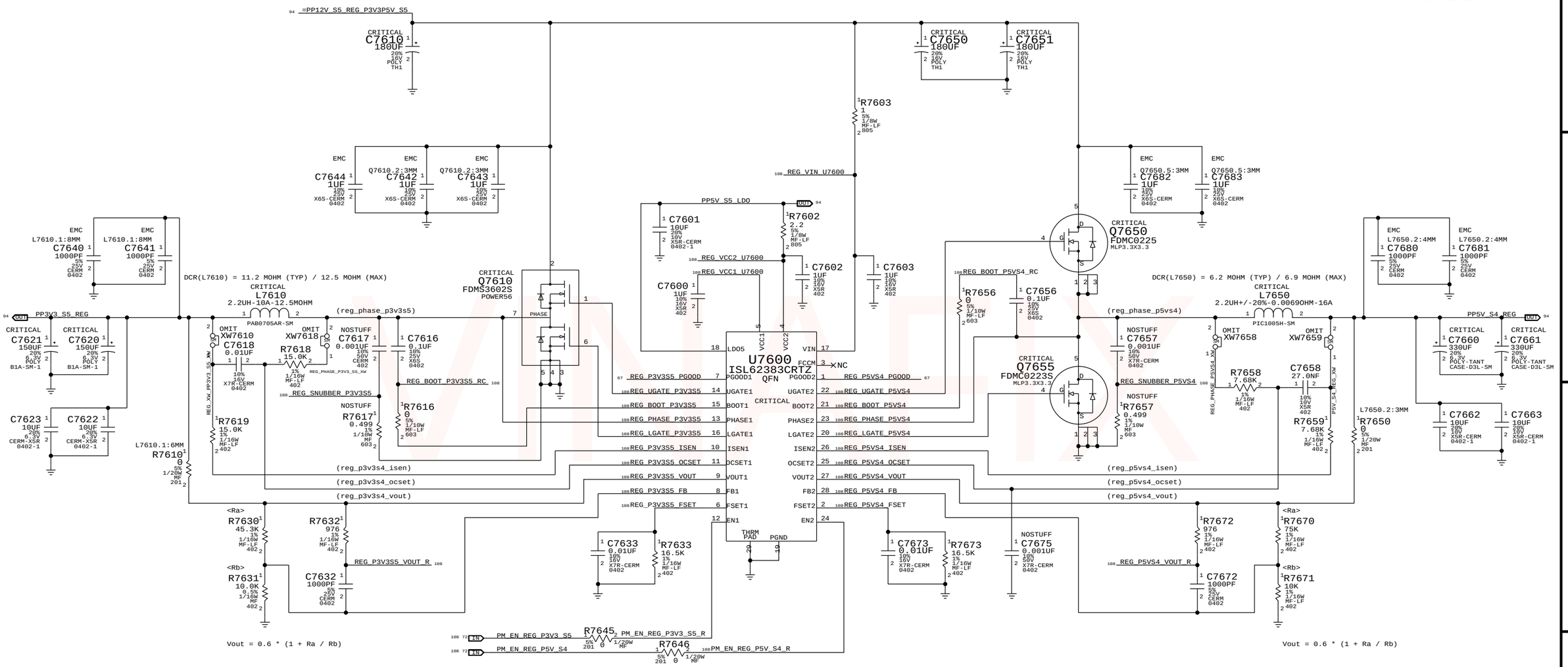
OC trip point: 12.5 A = $\frac{\text{R7618 * 10 E-6}}{\text{DCR(L7610)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7633}}$

5V S4 Regulator

OC trip point: 14.1 A = $\frac{\text{R7658 * 10 E-6}}{\text{DCR(L7650)}}$

Switching freq: 356 kHz = $\frac{1}{\text{170 E-12 * R7673}}$



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: VReg 3.3V S5/5V S4

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D

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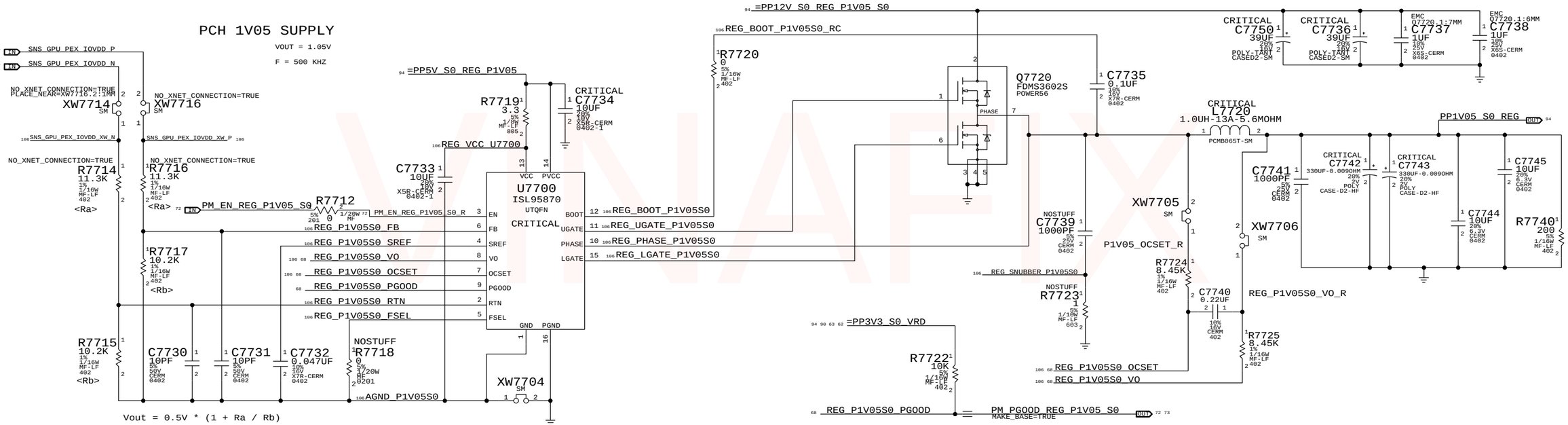
PCH 1V05 SUPPLY

VOUT = 1.05V

F = 500 KHZ



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE

1V05 PCH VREG

Apple Inc.

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND,PWR,33UH,20%,10A,35MOHM	L8100	CRITICAL	
353S00037	1	IC,PLP8565A13,LED BCKLGHT CTRL,7X7 QFN56	U8100	CRITICAL	

OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152S1668 (Cyntec) directly for next program

OMIT_TABLE

L8100 33UH-20%-10A-0.03510HM IHLP6767GZ-IHLP4040DZ11-SM

D8101 VS-8TQ100SPBF TO263

PP12V_S0_BKLT_PWR — D8103 SBR130S3 SOD-323 — C8140 1000PF 5% 25V CERM 0402 — C8141 1000PF 5% 25V CERM 0402 — CRITICAL C8102 10UF 10% 25V X7R-CERM 1206-1 — CRITICAL C8103 10UF 10% 25V X7R-CERM 1206-1 — CRITICAL C8114 100UF 20% 35V ELEC 0.3X11-TH

PLACE C8114 NEAR HIGHER FREQUENCY CAPS

GND

BKLT_BOOST — C8119 100PF 5% 100V C0G-CERM 0603 — CRITICAL C8106 2.2UF 10% 100V X7R 1206-2 — CRITICAL C8108 2.2UF 10% 100V X7R 1206-2 — CRITICAL C8109 15UF 20% 100V ELEC TH-COMBO — CRITICAL C8118 15UF 20% 100V ELEC TH-COMBO — C8120 100PF 5% 100V C0G-CERM 0603

GND

NOSTUFF R8123 4.7 5% 1/10W MF-LF 603 — BKLT_SNUBBER — NOSTUFF C8113 100PF 5% 100V C0G-CERM 0603

GND

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0810	138S0839		C8106, C8108	BLC OUTPUT CAPS
371S0748	371S0731		D8103	INPUT DIODE
371S0783	371S0782		D8101	OUTPUT DIODE
126-0226	126-0190		C8109, C8118	OUTPUT POLYMER CAPS
376S0845	376S1067		Q8119	POWERLINE FET
126-0312	126-0306		C8114	INPUT ECAP
152S1668	152S1970		L8100	BOOST INDUCTOR
376S1204	376S1106		Q8211 TO Q8216	LED SINK FET
740S0145	740S0146		F8100	FUSE FOR BLC
107S0359	107S0229		R8102	BOOST SENSE RESISTOR

PP3V3_S0_BKLT_VDDIO — PP5V_S0_BKLT_VDDD — PP5V_S0_BKLT_VDDA

PP12V_S0_BKLT_FILT

OMIT_TABLE

BKLT_GATE_R — Q8120 FDMC86102LZ MLP-3.3X3.3-PWRPK-12128-COMBO — R8119 0.005 1% 1/8W MF-LF 805 — BKLT_SNSP_R — R8102 0.03 1% 2W MF 2512-LF — BKLT_SNSN_R

R8114 20 5% 1/8W MF-LF 805 — BKLT_BST_FB_R — R8113 887K 1% 1/10W MF-LF 402 — R8112 330K 1% 1/8W MF 0402 — XW8109 SHORT-1206 — BKLT_SNSN_R

R8104 887K 1% 1/10W MF-LF 402 — R8103 330K 1% 1/8W MF 0402

BKLT_PHASE — Q8121 IRF6645PBF DIRECTFET-SJ — BKLT_GATE_R — C8111 1000PF 10% 100V X7R-CERM 0603 — BKLT_SNSP_R

U8100 LP8565 QFN

VDDIO 4	VDDD 5	VDDA 42	
BST_GD	36	BKLT_GATE	
BST_ISENSE_P	34	BKLT_SNSP	69 112
BST_ISENSE_N	33	BKLT_SNSN	69 112
BST_FB	31	BKLT_BST_FB	
BST_SHORT_FB	30	BKLT_BST_SHORT_FB	
LED1_HDR	14	BKLT_VSEN1	IN 70
LED1_GD	15	BKLT_GD1	OUT 70 112
LED1_R	16	BKLT_ISEN1	IN 70 112
LED2_HDR	17	BKLT_VSEN2	IN 70
LED2_GD	18	BKLT_GD2	OUT 70 112
LED2_R	19	BKLT_ISEN2	IN 70 112
LED3_HDR	20	BKLT_VSEN3	IN 70
LED3_GD	21	BKLT_GD3	OUT 70 112
LED3_R	22	BKLT_ISEN3	IN 70 112
LED4_HDR	24	BKLT_VSEN4	IN 70
LED4_GD	25	BKLT_GD4	OUT 70 112
LED4_R	26	BKLT_ISEN4	IN 70 112
LED5_HDR	29	BKLT_VSEN5	IN 70
LED5_GD	27	BKLT_GD5	OUT 70 112
LED5_R	28	BKLT_ISEN5	IN 70 112
LED6_HDR	44	BKLT_VSEN6	IN 70
LED6_GD	45	BKLT_GD6	OUT 70 112
LED6_R	46	BKLT_ISEN6	IN 70 112
LED7_HDR	47	BKLT_VSEN7	IN 70
LED7_GD	48	BKLT_GD7	OUT 70 112
LED7_R	49	BKLT_ISEN7	IN 70 112
LED8_HDR	51	BKLT_VSEN8	IN 70
LED8_GD	52	BKLT_GD8	OUT 70 112
LED8_R	53	BKLT_ISEN8	IN 70 112
LED9_HDR	54	BKLT_VSEN9	IN 70
LED9_GD	55	BKLT_GD9	OUT 70 112
LED9_R	56	BKLT_ISEN9	IN 70 112
GNDA 41	GNDD 6	LED_GND1 23	LED_GND2 50
GND_BST_GD 35	THRM PAD 57		

BKLT_PLL_FILT — R8111 270K 5% 1/16W MF-LF 402 — NOSTUFF D8102 SOD-523 BAT54XV2T1 — C8115 330PF 5% 50V C0G 402 — BKLT_PLL_FILT_R — C8116 4700PF 10% 50V X7R-CERM 0402 — BKLT_GNDA

BKLT_GD_RAIL — C8145 0.1UF 10% 25V X6S 0402 NOSTUFF — C8117 0.1UF 10% 25V X6S 0402 — BKLT_GND_BST_GD

R8140 0 MF-LF1/16W NOSTUFF 5% 402 — BKLT_GD_RAIL

R8138 1 5% 1/16W MF-LF 402 — PP12V_S0_BKLT_PWR — PP12V_S0_BKLT_PWR_R — C8142 1UF 10% 25V X7R 0603 — C8143 0.01UF 10% 16V X7R-CERM 0402 — C8144 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GND_BST_GD

XW8105 BKLT_GNDA — XW8106 BKLT_GNDD

R8137 1 5% 1/16W MF-LF 402 — =PP5V_S0_BKLT — PP5V_S0_BKLT_VDDA — C8137 22UF 20% 10V X5R-CERM 0603 — C8138 0.01UF 10% 16V X7R-CERM 0402 — C8139 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GNDA

XW8108

R8131 1 5% 1/16W MF-LF 402 — =PP5V_S0_BKLT — PP5V_S0_BKLT_VDDD — C8131 22UF 20% 10V X5R-CERM 0603 — C8132 0.01UF 10% 16V X7R-CERM 0402 — C8133 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GNDD

R8134 1 5% 1/16W MF-LF 402 — =PP3V3_S0_BKLT — PP3V3_S0_BKLT_VDDIO — C8134 1UF 10% 25V X7R 0603 — C8135 0.01UF 10% 16V X7R-CERM 0402 — C8136 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GNDD

R8172 0 5% 1/16W MF-LF 402 — BKLT_FAULT_INT_R_L

=PP3V3_S0_BKLT — R8124 4.7K MF 1/20W 201 5% — BKLT_FAULT_INT_L

R8106 100K MF 1/20W 201 5% — DP_INTPNL_ML_HPD_R

R8105 100K MF 1/20W 201 5% — TCON_BLC_EN

R8107 10K MF 1/20W 201 5% — BKLT_PWM_IN

R8121 10K MF 1/20W 201 5% NOSTUFF — BLC_VSYNC_R

R8120 10K MF 1/20W 201 5% NOSTUFF — BLC_LSYNC_R

BKLT_GNDD

R8180 10K MF 1/20W 201 5% — BKLT_ANG_TEST

R8181 10K MF 1/20W 201 5% — BKLT_DIG_TEST

R8182 10K MF 1/20W 201 5% — BKLT_NC_TEST

BKLT_GNDA

R8173 0 MF-LF1/16W 5% 402 — DP_INTPNL_ML_HPD

R8170 0 MF-LF1/16W 5% 402 — BLC_VSYNC

R8139 0 MF-LF1/16W 5% 402 NOSTUFF

R8171 0 MF-LF1/16W 5% 402 — BLC_LSYNC

F8100 6AMP-32V 0603-1 — R8132 0.005 1% 1/4W MF 1206 — PP12V_BKLT_SNS — PP12V_BKLT_FUSED

CRITICAL FB8108 160-OHM-6A 1206 — PP12V_S0_BKLT_FILT

Q8119 FDMS6681Z POWER56 — PP12V_S0_BKLT_PWR

NOSTUFF C8171 0.1UF 10% 25V X6S 0402 — NOSTUFF R8101 330K 1% 1/8W MF 0402 — BKLT_EN_DIV

NOSTUFF R8133 147K 1% 1/10W MF-LF 402 — BKLT_EN_L — R8122 0 5% 1/16W MF-LF 402 — BKLT_SHUTDOWN

NOSTUFF Q8101 SSM3K15AMFVAPE VESM — TCON_BLC_EN — GND

BKLT_BOOST — C8121 470PF 5% 100V CER-C0G 0603 — C8122 470PF 5% 100V CER-C0G 0603 — C8123 470PF 5% 100V CER-C0G 0603 — C8124 470PF 5% 100V CER-C0G 0603 — C8125 470PF 5% 100V CER-C0G 0603 — C8126 470PF 5% 100V CER-C0G 0603 — C8127 470PF 5% 100V CER-C0G 0603 — C8128 470PF 5% 100V CER-C0G 0603 — C8129 470PF 5% 100V CER-C0G 0603

LED_RETURN_1_FB
LED_RETURN_2_FB
LED_RETURN_3_FB
LED_RETURN_4_FB
LED_RETURN_5_FB
LED_RETURN_6_FB
LED_RETURN_7_FB
LED_RETURN_8_FB
LED_RETURN_9_FB

BKLT_SNSP — R8125 0 5% 1/16W MF-LF 402 — BKLT_SNSP_R — C8130 1000PF 5% 100V X7R 603 NOSTUFF

BKLT_SNSN — R8191 0 5% 1/16W MF-LF 402 — BKLT_SNSN_R

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: LCD Backlight Driver (LP8565)

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D
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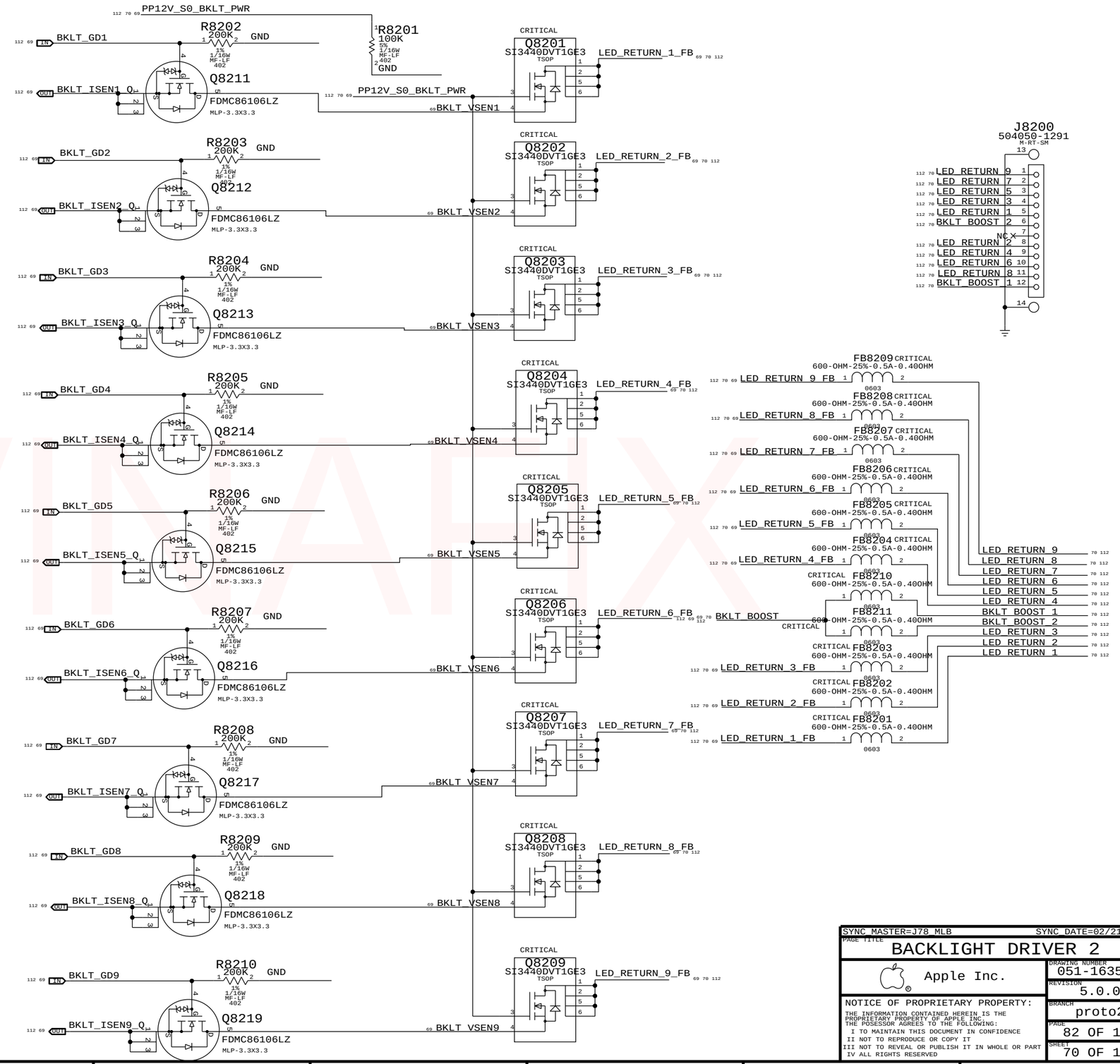
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1073	376S1256		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE

BACKLIGHT DRIVER 2

Apple Inc.

DRAWING NUMBER 051-1635 SIZE D

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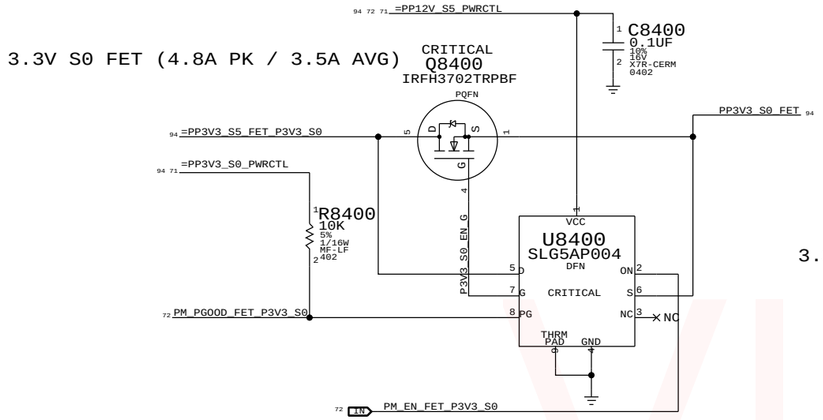
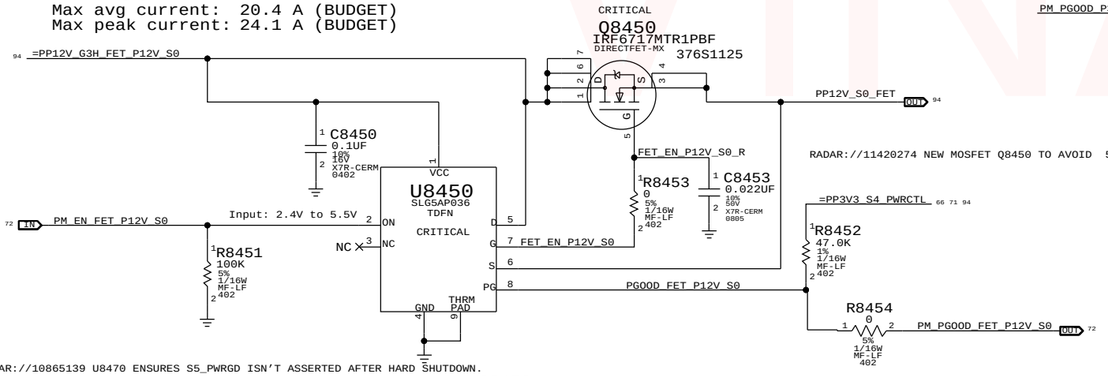
3.3V S0 FET (4.8A PK / 3.5A AVG)



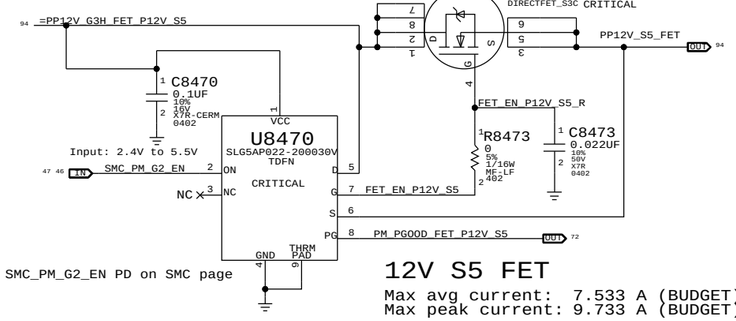
12V S0 FET

Max avg current: 20.4 A (BUDGET)
Max peak current: 24.1 A (BUDGET)



RADAR://11420274 NEW MOSFET Q8450 TO AVOID 50A 100US PULSE ON 12V S0.

RADAR://10865139 U8470 ENSURES S5_PWRGD ISN'T ASSERTED AFTER HARD SHUTDOWN.

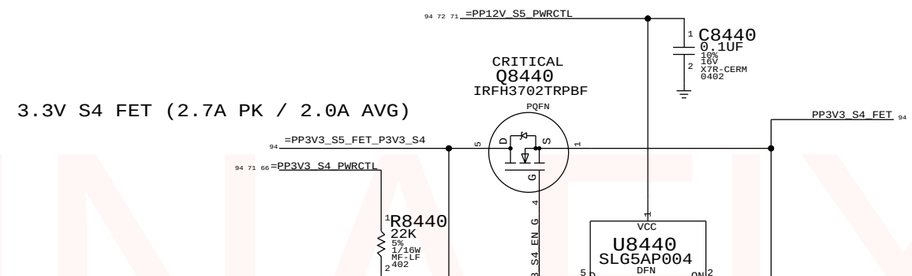


SMC_PM_G2_EN PD on SMC page

12V S5 FET

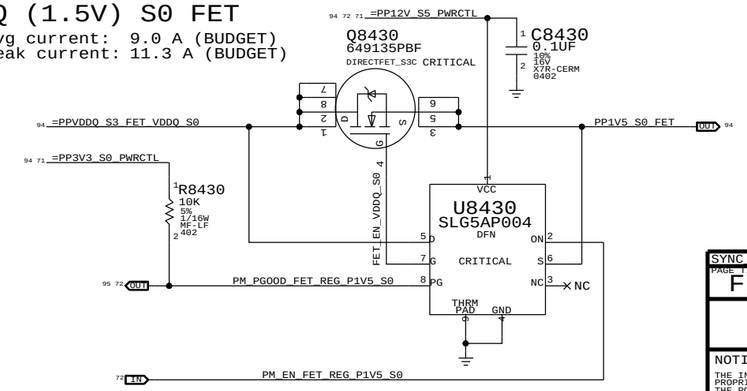
Max avg current: 7.533 A (BUDGET)
Max peak current: 9.733 A (BUDGET)

3.3V S4 FET (2.7A PK / 2.0A AVG)



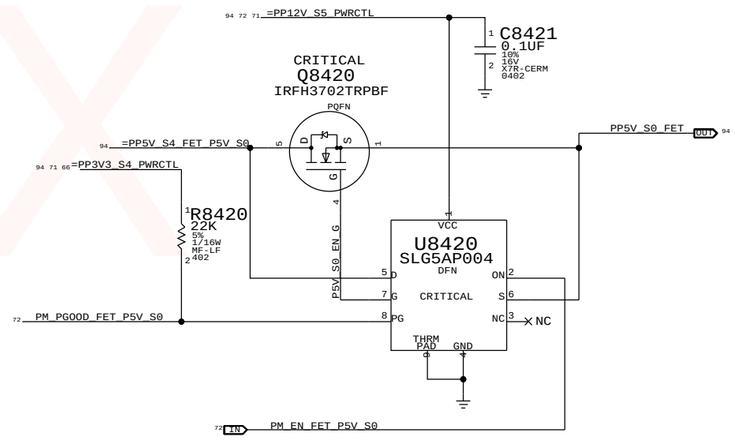
VDDQ (1.5V) S0 FET

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)



5V S0 FET

Max avg current: 2.7 A (BUDGET)
Max peak current: 3.9 A (BUDGET)



SYNC_MASTER=J78_MLB	SYNC_DATE=02/21/2014
PAGE TITLE	FET-Controlled S0 and S4
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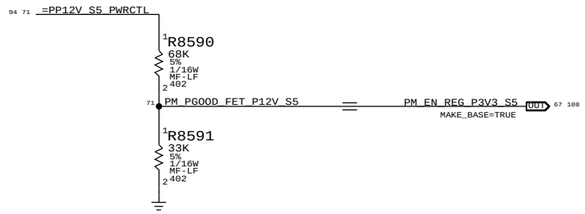
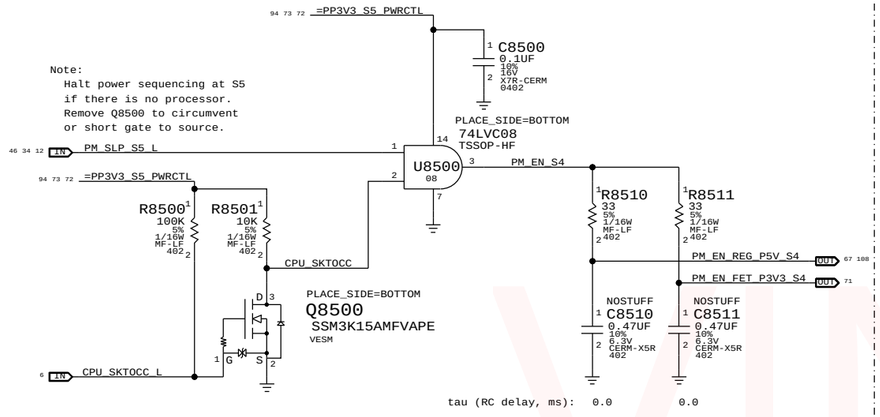
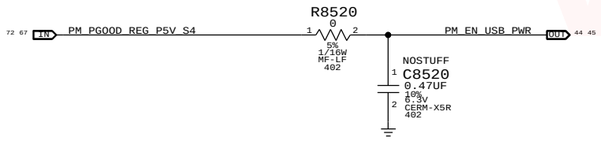
S5 Enable



S4 Enables

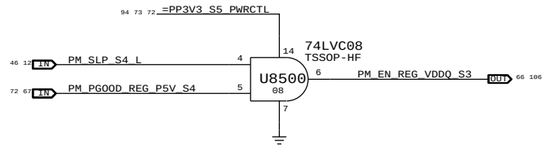


S4 USB Enable

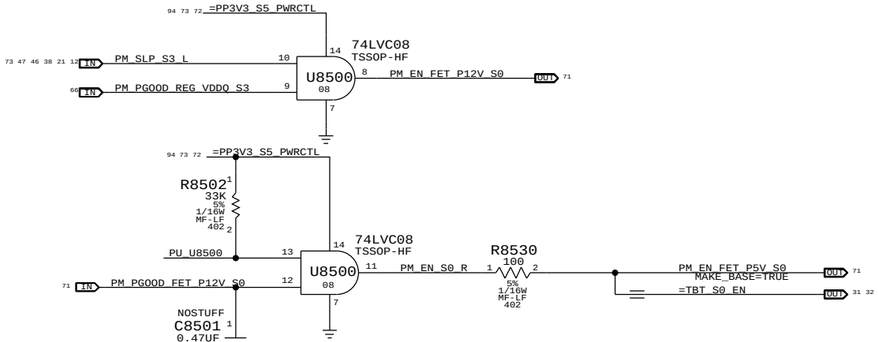


S4 TBT S4 Port Enable

S3 VDDQ Enable

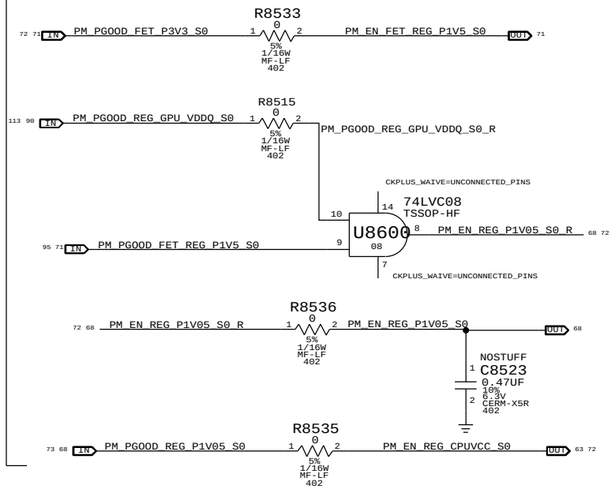


S0 Enables



S0 GPU SEQUENCING

S0 PCH Sequencing



Rail definitions

Platform: ALL PROCESSOR NON-CORE AND NON-GRAPHICS (5 V, 3.3 V, 1.5 V, 1.05V FOR PCH/TBT)
Uncore: VDDQ

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

AMD GPU:
1. 5V_S0 -> 3V3_S0 -> 0V95 -> 1V8 (VDD_CT) -> GPUCORE (VDDC) -> VDDCI -> MVDD

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PAGE TITLE
PM Regulator Enables

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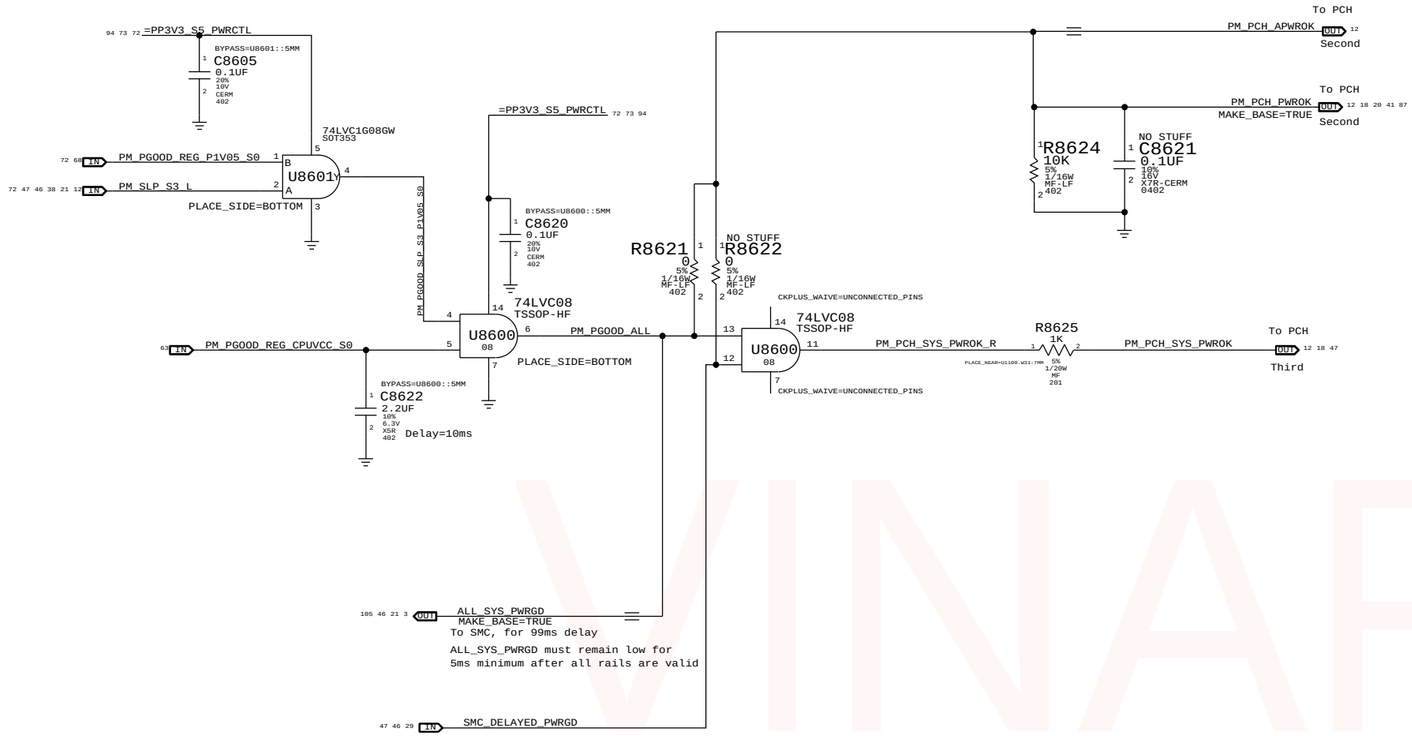
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



Resume Reset

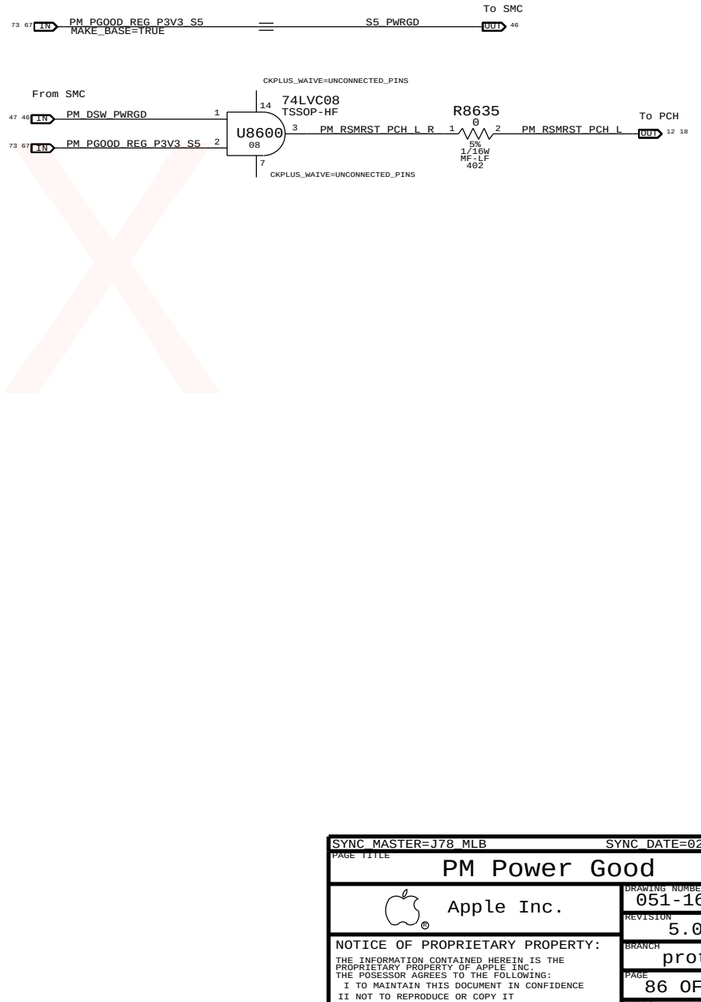
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
THE IMAC J78 DESIGNS DOES NOT SUPPORT DEEP SX MODES SO BOTH DPWROK AND RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE
PM Power Good

Apple Inc.

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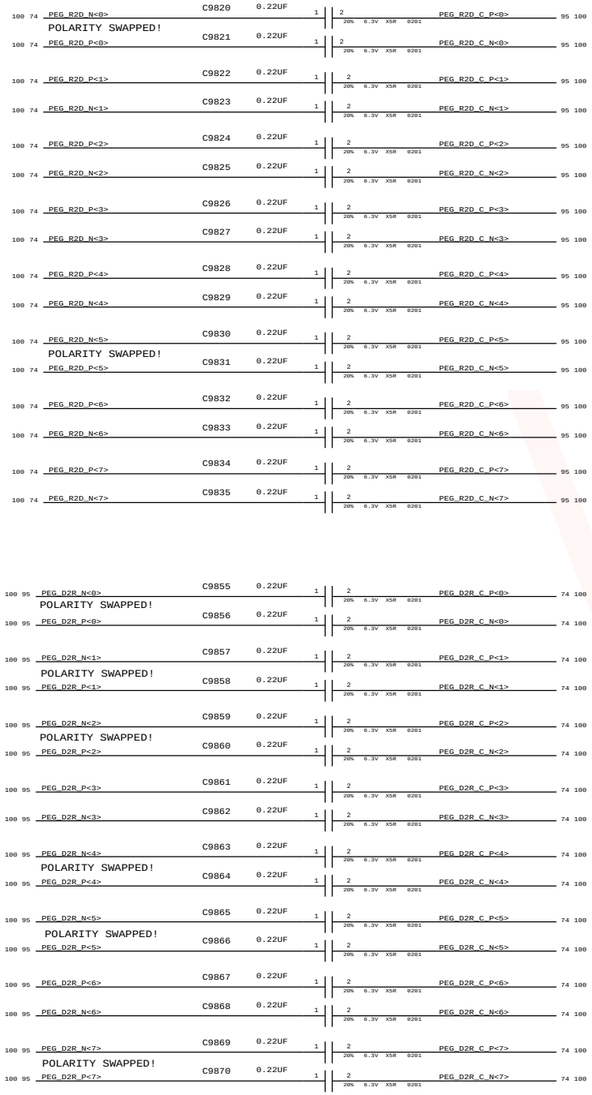
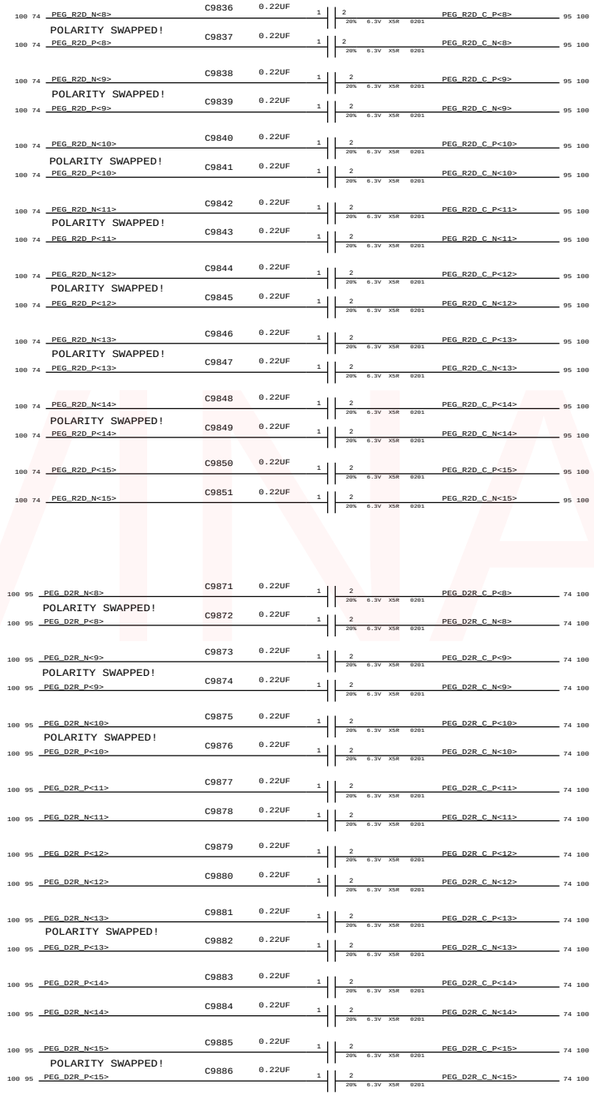
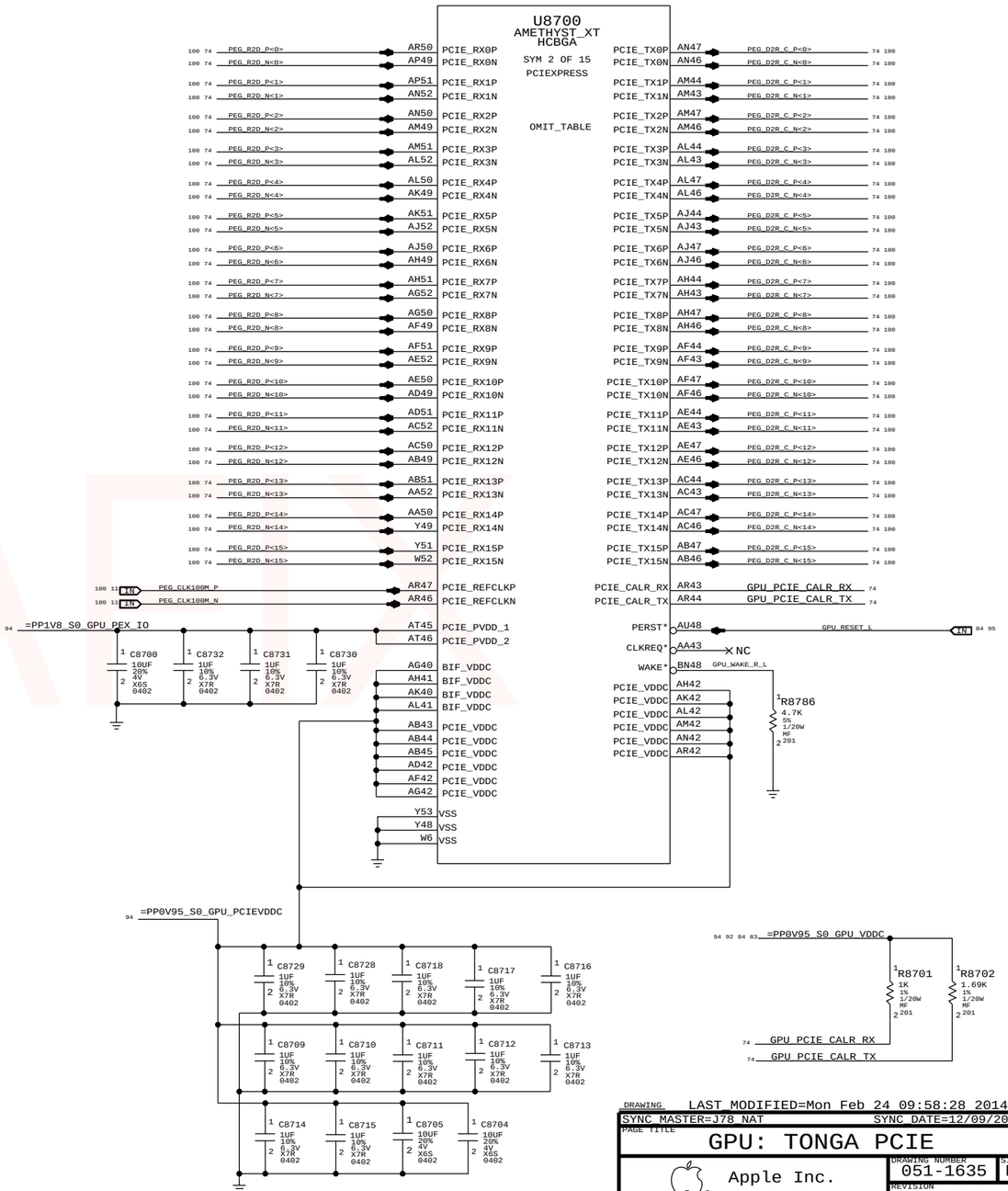
POLARITY SWAPS INTENDED ON LANES,SEE NOTES AT DIFF PAIRS.
ALL LANES ARE ALSO REVERSED, SEE ALIASES ON CSA 102

NOTE:
TONGA DOES NOT GENERATE PCIE CLKREQ.







DRAWING LAST_MODIFIED=Mon Feb 24 09:58:28 2014
SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013
PAGE TITLE
GPU: TONGA PCIE

Apple Inc.

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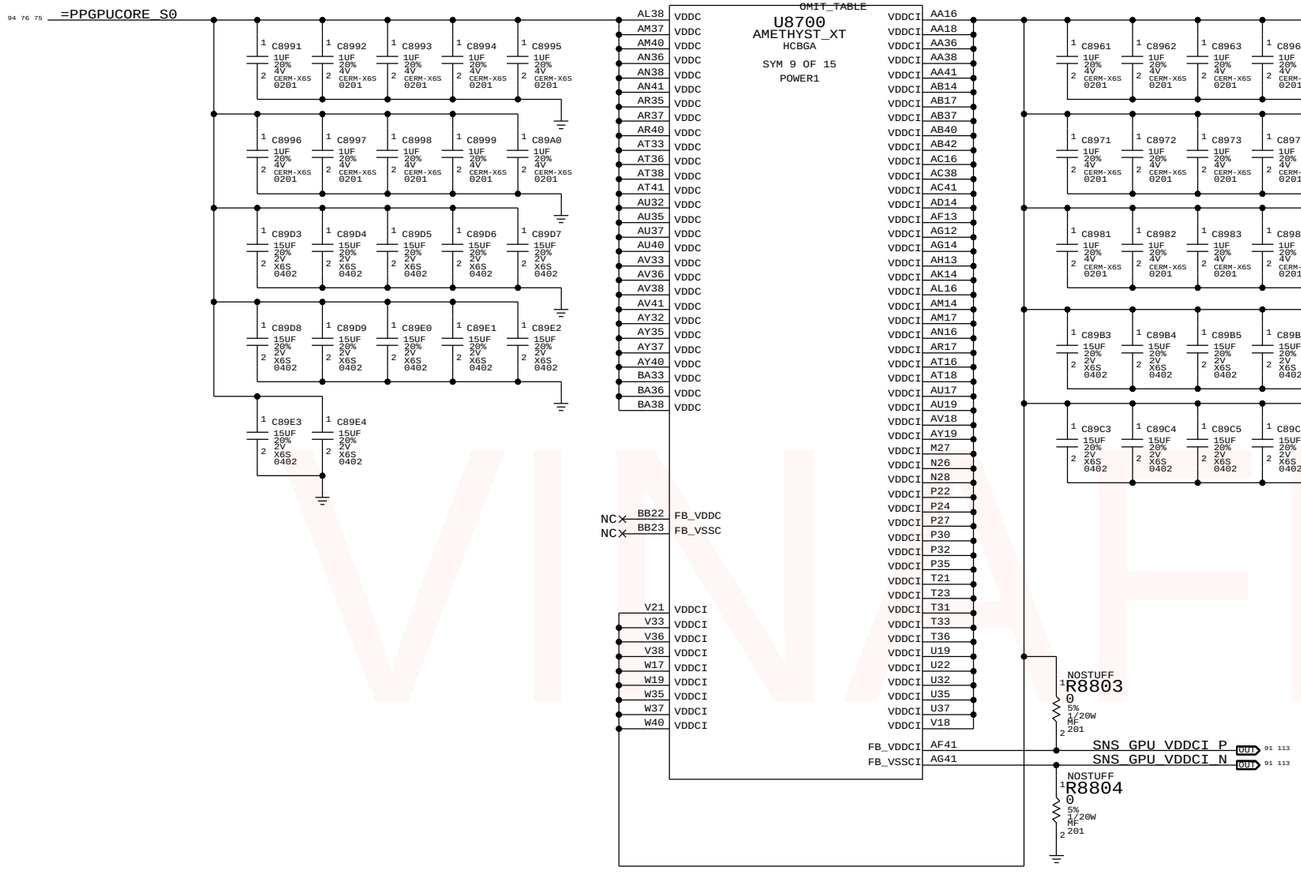
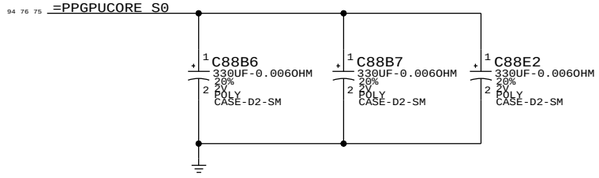
GPU VDDC/VDDCI DECOUPLING

PLACE ALL CAPS UNDER GPU



PLACE CLOSE TO GPU



DRAWING LAST_MODIFIED=Mon Feb 24 09:58:28 2014
SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013
PAGE TITLE: GPU: CORE VDDC/VDDCI
Apple Inc.
DRAWING NUMBER 051-1635 SIZE D
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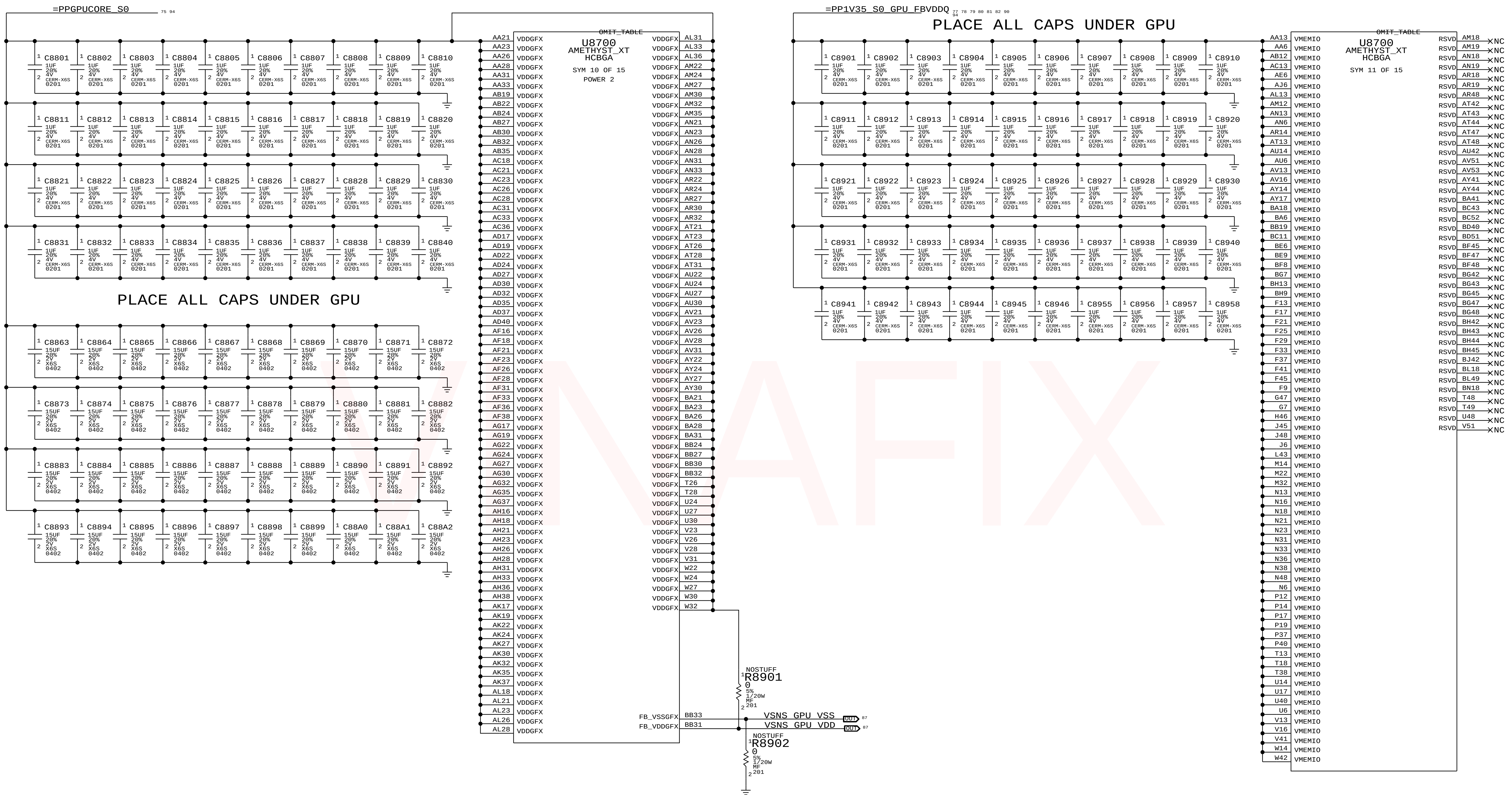
GPU MVDD/VDDGFX DECOUPLING



LAST_MODIFIED=Mon Feb 24 09:58:29 2014

SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013

PAGE TITLE: GPU: MVDD/VDDGFX

Apple Inc.

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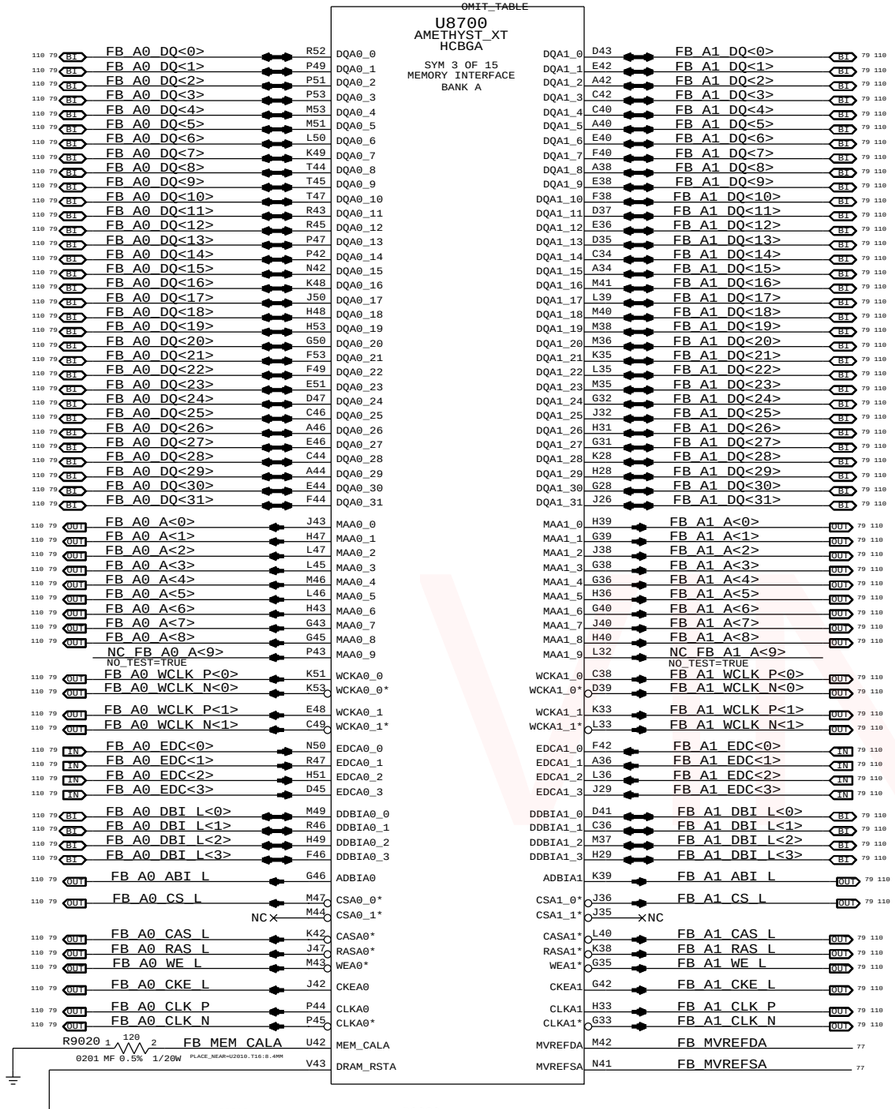

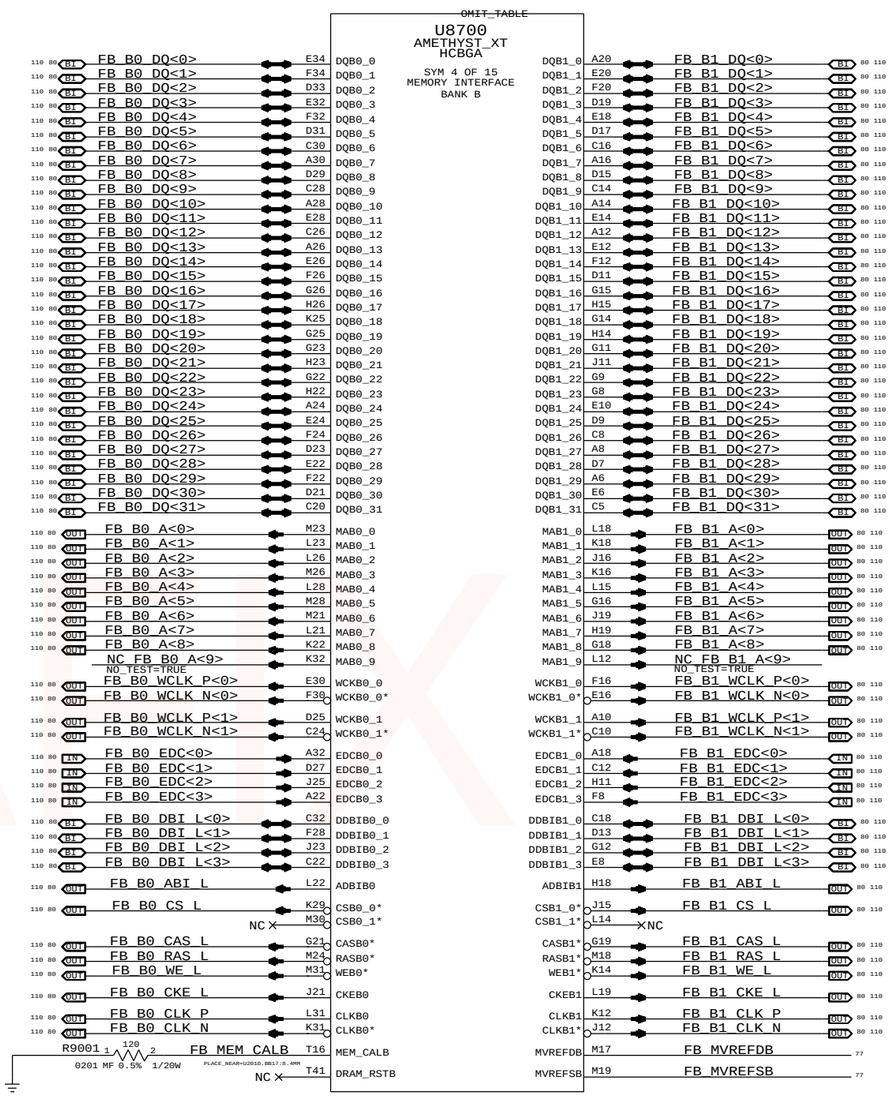

DRAWING	LAST_MODIFIED=Mon Feb 24 09:58:29 2014
SYNC_MASTER=J78_PETER	SYNC_DATE=12/04/2013
PAGE TITLE	GPU: FRAME BUFFER A/B
	Apple Inc.
DRAWING NUMBER	051-1635
SIZE	D
REVISION	5.0.0
BRANCH	proto2
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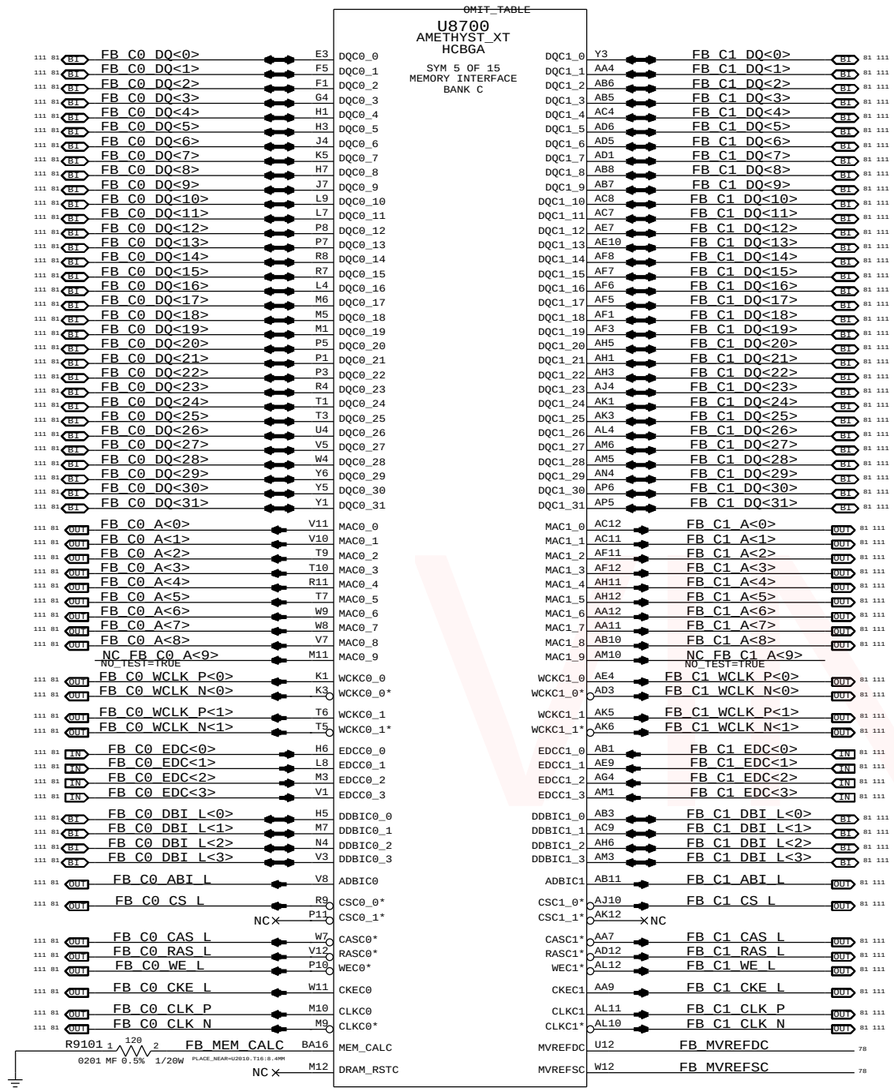

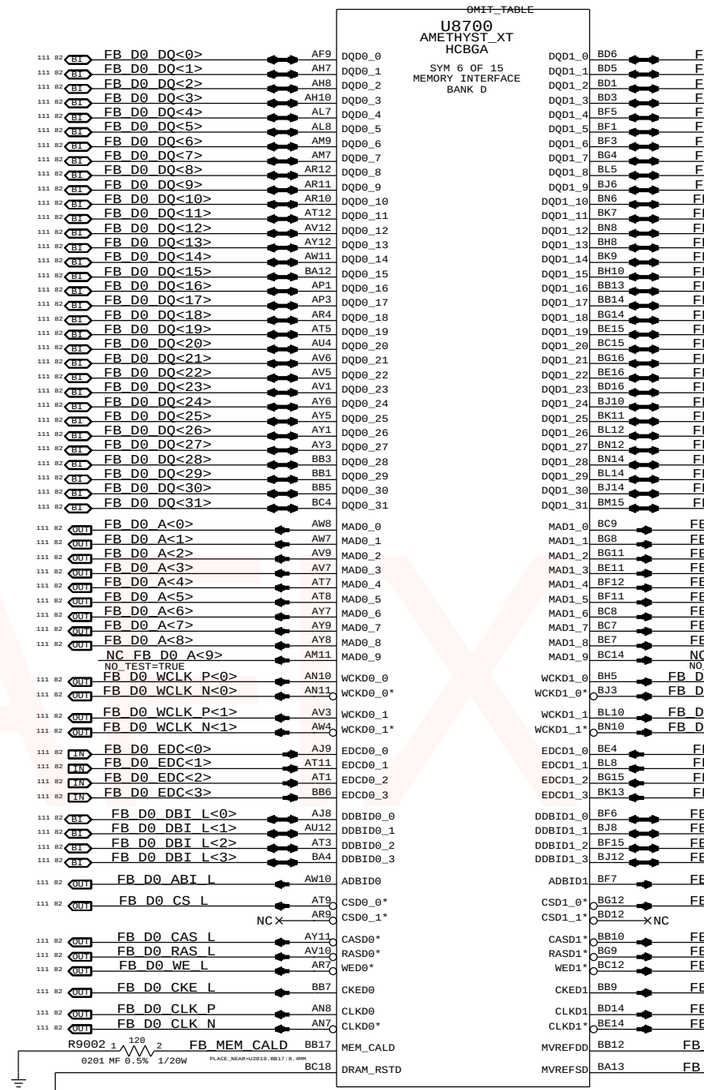

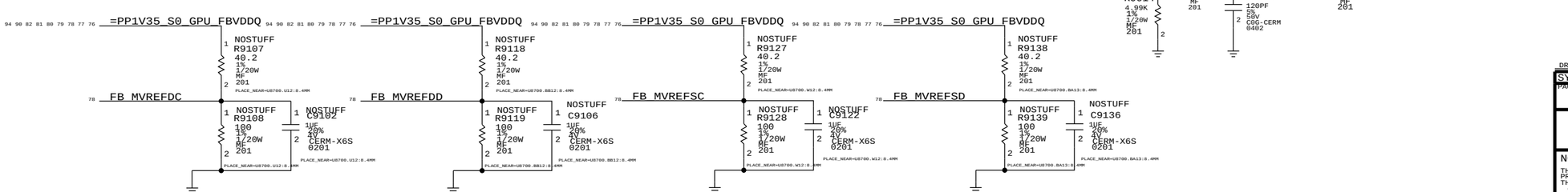

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SYNC_MASTER=J78 PETER SYNC_DATE=12/04/2013
PAGE TITLE
GPU: FRAME BUFFER C/D

Apple Inc.

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BRANCH proto2
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

NORMAL

U9200
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

MIRRORED

U9250
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

U9200
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

U9250
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

SYNC_MASTER=J78_MLB	SYNC_DATE=02/21/2014
PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-1635 SIZE D
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NORMAL

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

MIRRORED

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

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PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-1635 SIZE D
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NORMAL

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BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

MIRRORED

U9450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

U9400
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

U9450
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

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PAGE TITLE	GDDR5 FRAME BUFFER C
Apple Inc.	DRAWING NUMBER 051-1635 SIZE D
	REVISION 5.0.0
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

NORMAL

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32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

MIRRORED

U9550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

U9500
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

U9550
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

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PAGE TITLE	GDDR5 FRAME BUFFER D
Apple Inc.	DRAWING NUMBER 051-1635 SIZE D
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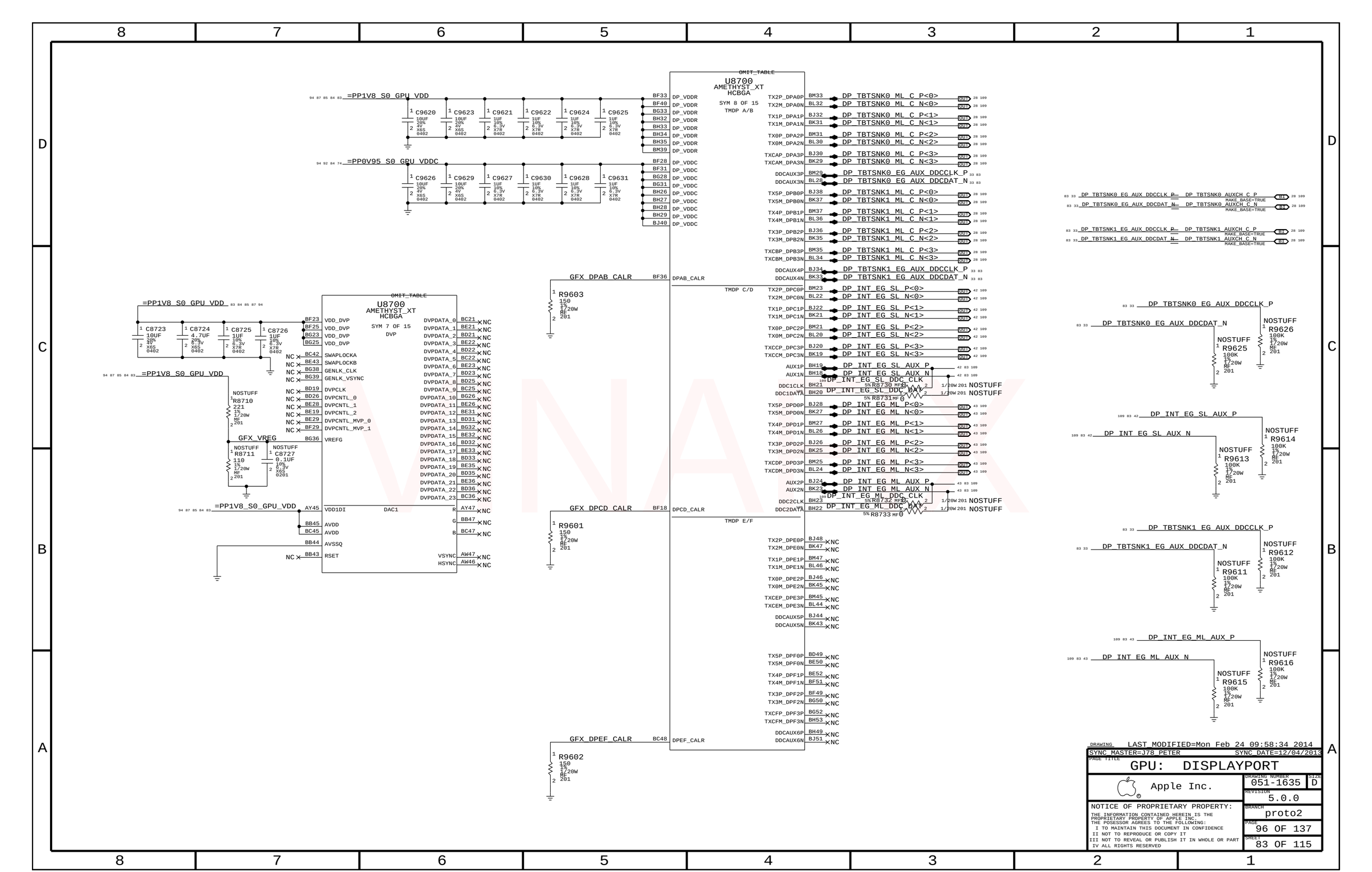
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C9623 10UF 20% 4V X6S 0402
C9621 1UF 10% 6.3V X7R 0402
C9622 1UF 10% 6.3V X7R 0402
C9624 1UF 10% 6.3V X7R 0402
C9625 1UF 10% 6.3V X7R 0402
=PP0V95_S0_GPU_VDDC
C9626 10UF 20% 4V X6S 0402
C9629 10UF 20% 4V X6S 0402
C9627 1UF 10% 6.3V X7R 0402
C9630 1UF 10% 6.3V X7R 0402
C9628 1UF 10% 6.3V X7R 0402
C9631 1UF 10% 6.3V X7R 0402
OMIT_TABLE
U8700
AMETHYST_XT
HCBGA
SYM 8 OF 15
TMDP A/B
DP_VDDR
DP_VDDC
TX2P_DPA0P
TX2M_DPA0N
TX1P_DPA1P
TX1M_DPA1N
TX0P_DPA2P
TX0M_DPA2N
TXCAP_DPA3P
TXCAM_DPA3N
DDCAUX3P
DDCAUX3N
TX5P_DPB0P
TX5M_DPB0N
TX4P_DPB1P
TX4M_DPB1N
TX3P_DPB2P
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TXCBP_DPB3P
TXCBM_DPB3N
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DDCAUX4N
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GFX_DPAB_CALR
R9603 150 1% 1/20W MF 201
DPAB_CALR
TMDP C/D
TX2P_DPC0P
TX2M_DPC0N
TX1P_DPC1P
TX1M_DPC1N
TX0P_DPC2P
TX0M_DPC2N
TXCCP_DPC3P
TXCCM_DPC3N
AUX1P
AUX1N
DDC1CLK
DDC1DATA
TX5P_DPD0P
TX5M_DPD0N
TX4P_DPD1P
TX4M_DPD1N
TX3P_DPD2P
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TXCDP_DPD3P
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AUX2N
DDC2CLK
DDC2DATA
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DP_INT_EG_SL_DDC_DAT
R8730 0 5% MF
R8731 0 5% MF
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DP_INT_EG_ML_AUX_P
DP_INT_EG_ML_AUX_N
DP_INT_EG_ML_DDC_CLK
DP_INT_EG_ML_DDC_DAT
R8732 0 5% MF
R8733 0 5% MF
1/20W 201 NOSTUFF
GFX_DPCD_CALR
R9601 150 1% 1/20W MF 201
DPCD_CALR
GFX_DPEF_CALR
R9602 150 1% 1/20W MF 201
DPEF_CALR
NC
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DP_TBTSNK0_EG_AUX_DDCDAT_N
DP_TBTSNK0_AUXCH_C_P
DP_TBTSNK0_AUXCH_C_N
DP_TBTSNK1_EG_AUX_DDCCLK_P
DP_TBTSNK1_EG_AUX_DDCDAT_N
DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N
MAKE_BASE=TRUE
NOSTUFF R9626 100K 1% 1/20W MF 201
NOSTUFF R9625 100K 1% 1/20W MF 201
DP_INT_EG_SL_AUX_P
DP_INT_EG_SL_AUX_N
NOSTUFF R9614 100K 1% 1/20W MF 201
NOSTUFF R9613 100K 1% 1/20W MF 201
NOSTUFF R9612 100K 1% 1/20W MF 201
NOSTUFF R9611 100K 1% 1/20W MF 201
DP_INT_EG_ML_AUX_P
DP_INT_EG_ML_AUX_N
NOSTUFF R9616 100K 1% 1/20W MF 201
NOSTUFF R9615 100K 1% 1/20W MF 201
C8723 10UF 20% 4V X6S 0402
C8724 4.7UF 20% 6.3V X6S 0402
C8725 1UF 10% 6.3V X7R 0402
C8726 1UF 10% 6.3V X7R 0402
=PP1V8_S0_GPU_VDD
NOSTUFF R8710 221 1% 1/20W MF 201
GFX_VREG
NOSTUFF R8711 110 1% 1/20W MF 201
NOSTUFF C8727 0.1UF 10% 6.3V X6S 0201
=PP1V8_S0_GPU_VDD
OMIT_TABLE
U8700
AMETHYST_XT
HCBGA
SYM 7 OF 15
DVP
VDD_DVP
SWAPLOCKA
SWAPLOCKB
GENLK_CLK
GENLK_VSYNC
DVPCLK
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCNTL_MVP_0
DVPCNTL_MVP_1
VREFG
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23
=PP1V8_S0_GPU_VDD
VDD1DI
DAC1
AVDD
AVSSQ
RSET
R
G
B
VSYNC
HSYNC
DRAWING
LAST MODIFIED=Mon Feb 24 09:58:34 2014
SYNC_MASTER=J78 PETER
SYNC_DATE=12/04/2013
PAGE TITLE
GPU: DISPLAYPORT
Apple Inc.
DRAWING NUMBER 051-1635
SIZE D
REVISION 5.0.0
BRANCH proto2
PAGE 96 OF 137
SHEET 83 OF 115
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GPU overtemp masking

=PP3V3_S0_GPU
C9779 0.1UF 10% 6.3V CERM-X5R 0201
U9701 74LVC1G08 SOT891
GPU_RESET_L
GPU_OVERTEMP
SMC_GFX_OVERTEMP
R9779 10K 5% 1/20W MF 201
R9792 10K 5% 1/20W MF 201
NC

=PP3V3_S0_GPU
R9781 10K 5% 1/20W MF 201
R9704 10K 5% 1/20W MF 201
R9785 10K 5% 1/20W MF 201
SMC_GFX_THROTTLE_R_L
TP_GPU_BP_0
TP_GPU_BP_1

=PP1V8_S0_GPU_VDD
L9703 0402 FERR-120-OHM-1.5A DCR:0.095OHM
C9722 0.1UF 10% 6.3V X6S 0201
C9760 10UF 20% 4V X6S 0402
C9724 1UF 10% 6.3V X7R 0402
C9725 0.1UF 10% 6.3V X6S 0201

=PP0V95_S0_GPU_VDDC
L9704 0402 FERR-120-OHM-1.5A DCR:0.095OHM
C9719 0.1UF 10% 6.3V X6S 0201
C9707 4.7UF 20% 6.3V X6S 0402
C9720 1UF 10% 6.3V X7R 0402
C9721 0.1UF 10% 6.3V X6S 0201

=PP1V8_S0_GPU_VDD
L9705 0603 FERR-220-OHM-2A DCR:0.050HM
C9733 0.1UF 10% 6.3V X6S 0201
C9717 10UF 20% 4V X6S 0402 NOSTUFF
C9714 4.7UF 20% 6.3V X6S 0402
C9713 4.7UF 20% 6.3V X6S 0402
C9712 1UF 10% 6.3V X7R 0402
C9711 0.1UF 10% 6.3V X6S 0201

=PP1V8_S0_GPU_VDD
L9901 0402 FERR-120-OHM-1.5A
C9901 0.1UF 10% 6.3V X6S 0201
C9902 0.1UF 10% 6.3V X6S 0201
C9903 1UF 10% 6.3V X7R 0402

=PP1V8_S0_GPU_VDD
C9732 1UF 0402 10% 6.3V X7R
=PP3V3_S0_GPU
C9730 1UF 0402 10% 6.3V X7R

VDD_GPIO18: BB35, BB36, BB37, BC35
VDD_GPIO33: BB38, BB40, BC38, BC39

GFX_PS_0 → PS_0 BJ16
GFX_PS_1 → PS_1 BH16
GFX_PS_2 → PS_2 BH17
GFX_PS_3 → PS_3 BG18
GFX_PS_4 → PS_4 BG19
GFX_SMBCLK_B → SMBCLK AV42
GFX_SMBDAT_B → SMBDAT AY42

SERIAL VID INTERFACE
NC → SCL V47
NC → SDA V46
VR_GPU_SVC → GPIO_SVC BF22
VR_GPU_SVD → GPIO_SVD BG22
VR_GPU_SVT → GPIO_SVT BG21
NC → DDCVGACLK U50
NC → DDCVGADATA U52
GPU_TEST_PG → TEST_PG AV47
GPU_TEST6 → TEST6 AW44
R9641 10K 5% 1/20W MF 201
R9787 0 5% 1/20W MF 201

TP_GPU_CB_REFCKP_OUT0 → CLKBUF_REFCLKP_OUT0 AN44
TP_GPU_CB_REFCKN_OUT0 → CLKBUF_REFCLKN_OUT0 AN43
TP_GPU_CB_REFCKP_OUT1 → CLKBUF_REFCLKP_OUT1 AT51
TP_GPU_CB_REFCKN_OUT1 → CLKBUF_REFCLKN_OUT1 AR52
TP_GPU_BP_0 → BP_0 BD42
TP_GPU_BP_1 → BP_1 BE42
PP1V8_SPLL_PVDD_FLT → SPLL_PVDD BC29
PP0V95_DPLL_VDDC_FLT → SPLL_VDDC BC26
PP1V8_MPLL_PVDD_FLT → MPLL_PVDD H8, J9, L11
PP1V8_TSVDD_FLT → TSVDD AY53
TP_TS_A → TS_A AA47

OMIT_TABLE
U8700 AMETHYST_XT HCBGA
SYM 1 OF 15
JTAG
PLLS XTAL
GPIO
TSS FDO

JTAG_TDO AW43 — TP_GPU_JTAG_TDO — TP9700
JTAG_TDI BA42 — TP_GPU_JTAG_TDI — TP9701
JTAG_TMS AY43 — TP_GPU_JTAG_TMS — TP9702
JTAG_TCK BB42 — TP_GPU_JTAG_TCK — TP9703
TESTEN AW48 — TP_GPU_JTAG_TESTEN — TP9704
JTAG_TRST* BB41 — TP_GPU_JTAG_TRST_L — TP9705

GPIO_0 V49 — NC
GPIO_1 BF39 — GPUCORE_VR_WARNING (IN 51)
GPIO_2 BD28 — NC
GPIO_5_REG_HOT_AC_BATT BD39 — SMC_GFX_THROTTLE_R_L — R9757 0 — SMC_GFX_THROTTLE_L (IN 46)
GPIO_6_TACH V48 — VR_GPU_VRDHOT_L (IN 87)
GPIO_8_ROMSO BE46 — GPU_ROM_SO (85 115)
GPIO_9_ROMSI BF46 — GPU_ROM_SI — R9722 33 — GPU_ROM_SI_R (85 115)
GPIO_10_ROMSCK BG46 — GPU_ROM_SCK — R9726 33 — GPU_ROM_SCK_R (85)
GPIO_11 AA44 — NC
GPIO_12 BA50 — NC
GPIO_13 BA52 — NC
GPIO_14_HPD2 AV45 — DP_INT_EG_ML_HPD (IN 43 112)
GPIO_15 W44 — NC
GPIO_16_8P_DETECT V45 — GPU_VDDCI_ALTV (OUT 91 114)
GPIO_17_THERMAL_INT AA45 — SMC_GFX_ALERT (46 84)
GPIO_18_HPD3 AV44 — DP_TBTSNK0_HPD (IN 28 109)
GPIO_19_CTF W43 — GPU_OVERTEMP_R — R9758 0 — GPU_OVERTEMP (84)
GPIO_20 W45 — GPU_FBVDDQ_ALTV (OUT 90 113)
GPIO_21 BF38 — NC
GPIO_22_ROMCSB BE47 — GPU_ROM_CS_L — R9727 33 — GPU_ROM_CS_L_R (85 115)
GPIO_29 BF43 — NC
GPIO_30 BE40 — NC
GENERICA BH41 — NC
GENERICB BE38 — NC
GENERICC BE39 — NC
GENERICD BG29 — NC
GENERICE_HPD4 BC31 — DP_TBTSNK1_HPD (IN 28 109)
GENERICF_HPD5 BC32 — NC
GENERICG_HPD6 BA48 — NC
HPD1 BE45 — DP_INT_EG_SL_HPD (IN 42 112)
PX_EN T51 — NC — BACO MODE

XO_IN2 BM41 — PD_GFX_CLK_100M — R9707 NOSTUFF 4.99K
XO_IN BK41 — PD_GFX_CLK_27M — R9708 NOSTUFF 4.99K
XTALIN BN40 — GFX_XTAL_IN_27M (110) — R9701 0 — GPU_OSC_27M_XTAL_IN (110)
XTALOUT BL40 — GFX_XTAL_OUT_27M (110) — R9702 0 — GPU_OSC_27M_XTAL_OUT (110)
CLKTESTA BM17 — CLKTESTA — C9709 NOSTUFF 0.1UF — CLKTESTA_C
CLKTESTB BK17 — CLKTESTB — C9710 NOSTUFF 0.1UF — CLKTESTB_C
PLL_ANALOG_IN AV48 — TP_GPU_PLL_ANALOG_IN
PLL_ANALOG_OUT AV49 — GPU_PLL_ANALOG_OUT (84)
DPLUS W47 — GPU_TDIODE_P (IN 85 105)
DMINUS W46 — GPU_TDIODE_N (IN 85 105)
GPIO_28_FDO AA46 — GPU_MLPS_EN_L (84)

GPIO_28 SHOULD BE LOW AT POWER-UP TO ENABLE MULTI-LEVEL PIN STRAPS

=PP3V3_S0_GPU
R8704 1K 5% 1/20W MF 201
R8714 1K 5% 1/20W MF 201
R8706 1K 5% 1/20W MF 201
NOSTUFF R8703 1K 5% 1/20W MF 201
R8707 1K 5% 1/20W MF 201
NOSTUFF R8708 1K 5% 1/20W MF 201
R8709 1K 5% 1/20W MF 201

GPU_MLPS_EN_L (84) — R9784 10K 5% 1/20W MF 201

SMC_GFX_ALERT (84 46) — R9782 10K 5% 1/20W MF 201
GPU_PLL_ANALOG_OUT (84) — NOSTUFF R9747 16.2K 1% 1/20W MF 201

R9710 NOSTUFF 51.1 1% 1/20W MF 201
R9709 NOSTUFF 51.1 1% 1/20W MF 201

Y9701 197S0499 2.5X2.00MM-SM 27MHZ-30PPM-12PF-40OHM
C9702 18PF 5% 25V C0G 0201
C9703 18PF 5% 25V C0G 0201
C = 2*CL - (CPIN+CP)

DRAWING	LAST MODIFIED=Mon Feb 24 09:58:34 2014
SYNC_MASTER=J78_PETER	SYNC_DATE=11/13/2013
PAGE TITLE	GPU: GPIOS/PLLS/STRAPS
	Apple Inc.
DRAWING NUMBER	051-1635
SIZE	D
REVISION	5.0.0
BRANCH	proto2
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CONFIG STRAPS - MLS

STRAPS SET TO BOOT FROM EFI ROM.

=PP1V8_S0_GPU_VDD1 (94 87 84 83)

R9731 8.45K 1% 1/20W MF 201 — GFX_PS_0 (84)
- R9732 2K 1% 1/20W MF 201 — PLACE_NEAR=U8700.BJ16:15MM
- C9737 0.082UF 10% 10V CERM-X7R 402 — PLACE_NEAR=U8700.BJ16:15MM
- PLACE_NEAR=U8700.BJ16:15MM

R9733 8.45K 1% 1/20W MF 201 — GFX_PS_1 (84)
- R9734 2K 1% 1/20W MF 201 — PLACE_NEAR=U8700.BH16:15MM
- NOSTUFF C9734 0.68UF 5% 6.3V X6S 0402 — PLACE_NEAR=U8700.BH16:15MM
- PLACE_NEAR=U8700.BH16:15MM

NOSTUFF R9735 4.53K 1% 1/20W MF 201 — GFX_PS_2 (84)
- R9736 4.75K 1% 1/20W MF 201 — PLACE_NEAR=U8700.BH17:15MM
- C9735 0.68UF 5% 6.3V X6S 0402 — PLACE_NEAR=U8700.BH17:15MM
- PLACE_NEAR=U8700.BH17:15MM

NOSTUFF R9737 4.53K 1% 1/20W MF 201 — GFX_PS_3 (84)
- R9738 4.75K 1% 1/20W MF 201 — PLACE_NEAR=U8700.BG18:15MM
- C9736 0.68UF 5% 6.3V X6S 0402 — PLACE_NEAR=U8700.BG18:15MM
- PLACE_NEAR=U8700.BG18:15MM

R9809 4.53K 1% 1/20W MF 201 — GFX_PS_4 (84)
- R9810 2K 1% 1/20W MF 201 — PLACE_NEAR=U8700.BG19:15MM
- NOSTUFF C9805 0.68UF 5% 6.3V X6S 0402 — PLACE_NEAR=U8700.BG19:15MM
- PLACE_NEAR=U8700.BG19:15MM

SMC KEY

GFXA

GPU DIE TEMP	TG0P
GPU VRAM PROX TEMP	TG1P
GPU VR PROX TEMP	TG2P

=PP3V3_S0_GPU (51 84 85 91 92 93 94)

R9901 10K 5% 1/20W MF 201 — GFX_SMBADDR (7)

NOSTUFF R9912 10K 5% 1/20W MF 201 — GFX_SMBALT_L (8)

C9905 1.0UF 20% 6.3V X5R 0201-1

C9906 0.0022UF 10% 50V CERM 402 — PLACE_NEAR=U9901.2:3MM

NO_XNET_CONNECTION=TRUE
C9907 0.0022UF 10% 50V CERM 402 — PLACE_NEAR=U9901.4:3MM

U9901 EMC1414-1-AIZL MSOP

VDD	1	
THERM*/ADDR	7	GFX_SMBADDR
ALERT*	8	GFX_SMBALT_L
SMDATA	9	GPU_SMB_DAT
SMCLK	10	GPU_SMB_CLK
GND	6	
DP1	2	GPU_TDIODE_P (84 105)
DN1	3	GPU_TDIODE_N (84 105)
DP2/DN3	4	GFX_THM_DP2 (105)
DN2/DP3	5	GFX_THM_DN2 (105)

GPU_SMB_DAT_R (49 [B]) — R9954 0 5% 1/20W MF 0201 — GPU_SMB_DAT
GPU_SMB_CLK_R (49 [B]) — R9955 0 5% 1/20W MF 0201 — GPU_SMB_CLK

Q9901 BC846BMXXH SOT732-3 — GDDR5 TEMP SENSOR

NO_XNET_CONNECTION=TRUE
XW9901 SM — GFX_THM_DP3 (105)

Q9902 BC846BMXXH SOT732-3

NO_XNET_CONNECTION=TRUE
XW9902 SM — GFX_THM_DN3 (105)

PWR VR TEMP SENSOR

GPU BOOT ROM

=PP3V3_S0_GPU (94 93 92 91 85 84 51)

R9724 10K 5% 1/20W MF 201
R9725 10K 5% 1/20W MF 201
R9729 10K 5% 1/20W MF 201
C9704 0.1UF 10% 6.3V CERM-XSR 0201

U9700 M25P10A UFDFPN8 OMIT_TABLE

VCC	8	
D	5	GPU_ROM_SI_R (115 84)
C	6	GPU_ROM_SCK_R (84)
S*	1	GPU_ROM_CS_L_R (115 84)
W*	3	GPU_ROM_WP_L (115)
HOLD*	7	GPU_ROM_HOLD_L
Q	2	GPU_ROM_SO_R (115)
VSS	4	
THRM PAD	9	

R9723 33 1/20W MF 5% 201 — GPU_ROM_SO (84 115) — PLACE_NEAR=U9700.2:8MM

R9728 0 5% 1/20W MF 201

Page Notes

Power aliases required by this page:
- +PP1V05_S0_GPU_PCH_SDVDD
- +PP3V3_S0_GPU
- +PP1V05_S0_GPU_PCH_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=J78_PETER SYNC_DATE=11/13/2017

PAGE TITLE: GPU: STRAPS,SENSORS,ROM

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D
REVISION: 5.0.0
BRANCH: proto2
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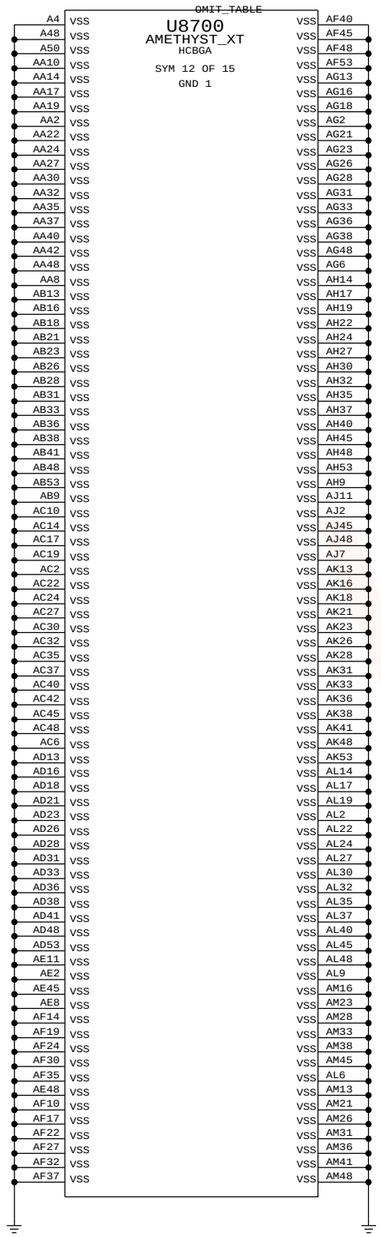

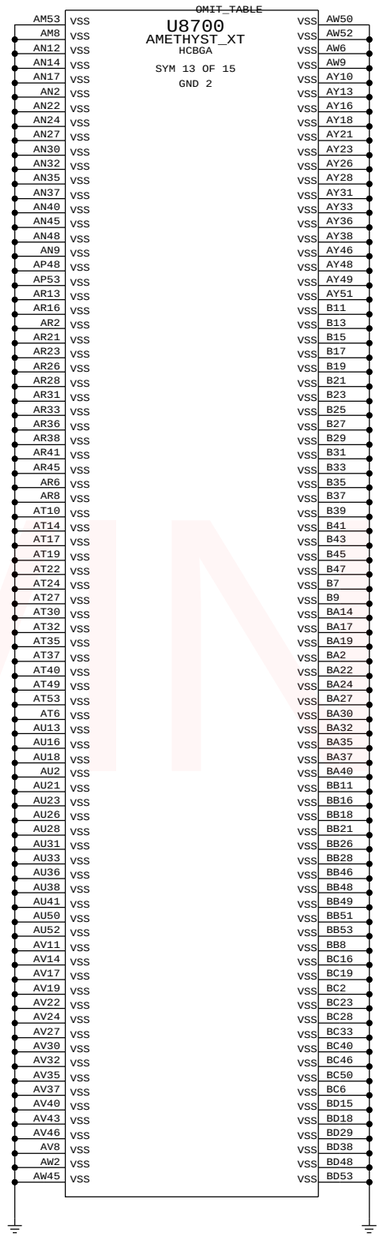

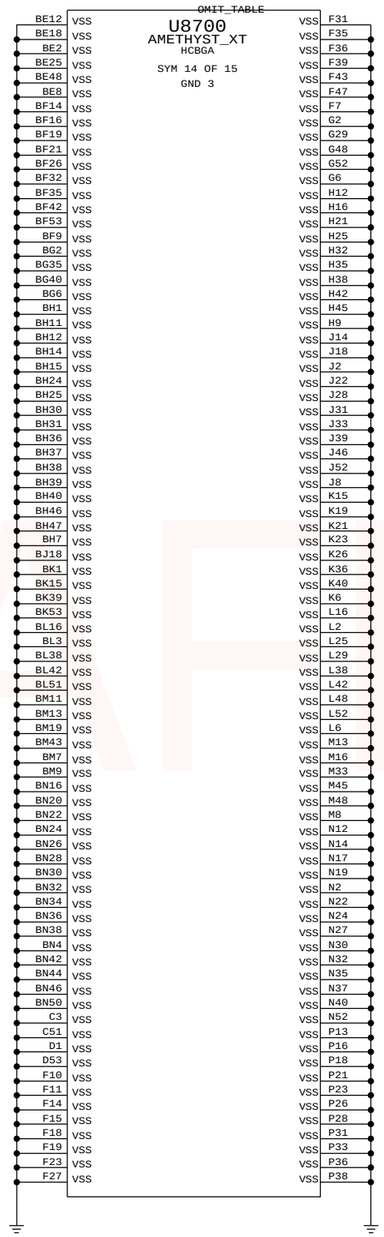

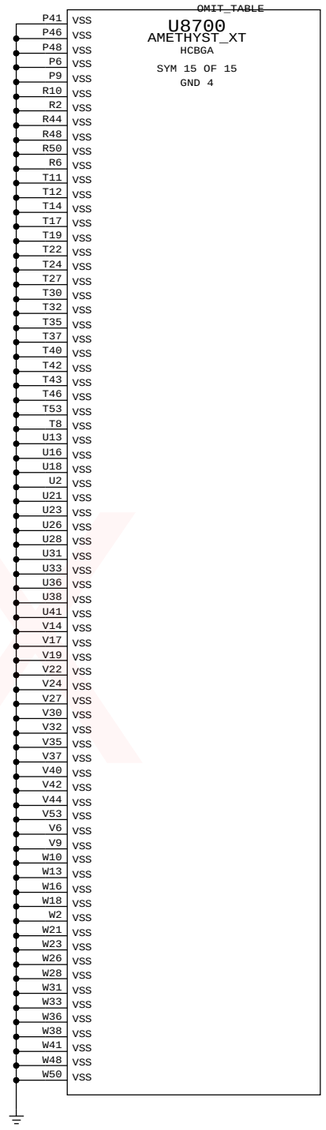

DRAWING LAST_MODIFIED=Mon Feb 24 09:58:35 2014

SYNC_MASTER=J78_PETER SYNC_DATE=11/13/2013

PAGE TITLE

GPU: GNDS & UNUSED

Apple Inc.

DRAWING NUMBER 051-1635 SIZE D

REVISION 5.0.0

BRANCH proto2

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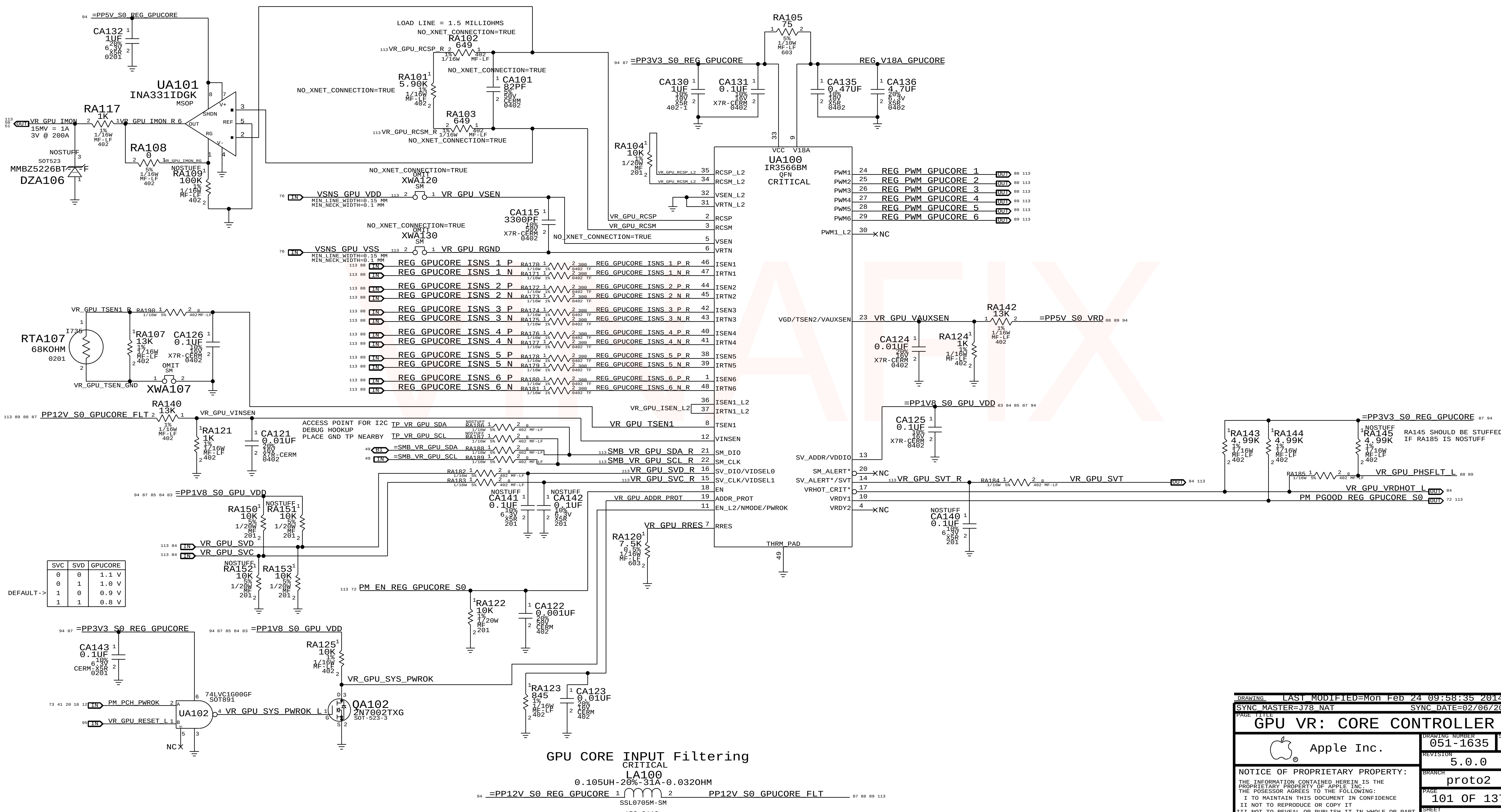
O/P= PPGPUCORE_S0_REG

GPUCORE
VOUT = VCORE
PEAK = 180A
AVG = 150A



=PP5V_S0_REG_GPUCORE
CA132 1UF 20% 6.3V X5R 0201
UA101 INA331IDGK MSOP
RA117 1K 1% 1/16W MF-LF 402
VR_GPU_IMON
15MV = 1A
3V @ 200A
VR_GPU_IMON_R
RA108 0 5% 1/16W MF-LF 402
NOSTUFF
MMBZ5226BT-F SOT523
DZA106
RA109 100K 1% 1/16W MF-LF 402
LOAD LINE = 1.5 MILLIOHMS
NO_XNET_CONNECTION=TRUE
RA102 649 1% 1/16W MF-LF 402
VR_GPU_RCSP_R
RA101 5.90K 1% 1/16W MF-LF 402
CA101 82PF 5% 50V CERM 0402
RA103 649 1% 1/16W MF-LF 402
VR_GPU_RCSM_R
VSNS_GPU_VDD
MIN_LINE_WIDTH=0.15 MM
MIN_NECK_WIDTH=0.1 MM
XWA120 SM
VR_GPU_VSEN
CA115 3300PF 10% 16V X7R-CERM 0402
VSNS_GPU_VSS
XWA130 SM
VR_GPU_RGND
RA105 75 5% 1/10W MF-LF 603
=PP3V3_S0_REG_GPUCORE
REG_V18A_GPUCORE
CA130 1UF 10% 16V X5R 402-1
CA131 0.1UF 10% 16V X7R-CERM 0402
CA135 0.47UF 10% 16V X5R 0402
CA136 4.7UF 20% 6.3V X5R 0402
RA104 10K 1% 1/20W MF 201
UA100 IR3566BM QFN CRITICAL
VCC V18A
RCSP_L2 RCSM_L2 VSEN_L2 VRTN_L2 RCSP RCSM VSEN VRTN
ISEN1 IRTN1 ISEN2 IRTN2 ISEN3 IRTN3 ISEN4 IRTN4 ISEN5 IRTN5 ISEN6 IRTN6
ISEN1_L2 IRTN1_L2 TSEN1 VINSEN SM_DIO SM_CLK
SV_DIO/VIDSEL0 SV_CLK/VIDSEL1 EN ADDR_PROT EN_L2/NMODE/PWRGK RRES THRM_PAD
PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 PWM1_L2
VGD/TSEN2/VAUXSEN SV_ADDR/VDDIO SM_ALERT* SV_ALERT*/SVT VRHOT_CRIT* VRDY1 VRDY2
REG_PWM_GPUCORE_1
REG_PWM_GPUCORE_2
REG_PWM_GPUCORE_3
REG_PWM_GPUCORE_4
REG_PWM_GPUCORE_5
REG_PWM_GPUCORE_6
REG_GPUCORE_ISNS_1_P
REG_GPUCORE_ISNS_1_N
REG_GPUCORE_ISNS_2_P
REG_GPUCORE_ISNS_2_N
REG_GPUCORE_ISNS_3_P
REG_GPUCORE_ISNS_3_N
REG_GPUCORE_ISNS_4_P
REG_GPUCORE_ISNS_4_N
REG_GPUCORE_ISNS_5_P
REG_GPUCORE_ISNS_5_N
REG_GPUCORE_ISNS_6_P
REG_GPUCORE_ISNS_6_N
VR_GPU_ISEN_L2
VR_GPU_TSEN1_R
RTA107 68KOHM 0201
RA107 13K 1% 1/16W MF-LF 402
CA126 0.1UF 10% 16V X7R-CERM 0402
VR_GPU_TSEN_GND
XWA107 OMIT SM
PP12V_S0_GPUCORE_FLT
RA140 13K 1% 1/16W MF-LF 402
VR_GPU_VINSEN
RA121 1K 1% 1/16W MF-LF 402
CA121 0.01UF 20% 16V X7R-CERM 0402
ACCESS POINT FOR I2C
DEBUG HOOKUP
PLACE GND TP NEARBY
TP_VR_GPU_SDA
TP_VR_GPU_SCL
=SMB_VR_GPU_SDA
=SMB_VR_GPU_SCL
SMB_VR_GPU_SDA_R
SMB_VR_GPU_SCL_R
VR_GPU_SVD_R
VR_GPU_SVC_R
VR_GPU_ADDR_PROT
VR_GPU_RRES
CA141 0.1UF 10% 6.3V X5R 201
CA142 0.1UF 10% 6.3V X5R 201
=PP1V8_S0_GPU_VDD
RA150 10K 5% 1/20W MF 201
RA151 10K 5% 1/20W MF 201
VR_GPU_SVD
VR_GPU_SVC
RA152 10K 5% 1/20W MF 201
RA153 10K 5% 1/20W MF 201
RA120 7.5K 0.5% 1/16W MF-LF 603
RA142 13K 1% 1/16W MF-LF 402
=PP5V_S0_VRD
VR_GPU_VAUXSEN
CA124 0.01UF 20% 16V X7R-CERM 0402
RA124 1K 1% 1/16W MF-LF 402
=PP1V8_S0_GPU_VDD
CA125 0.1UF 10% 16V X7R-CERM 0402
=PP3V3_S0_REG_GPUCORE
RA143 4.99K 1% 1/16W MF-LF 402
RA144 4.99K 1% 1/16W MF-LF 402
RA145 4.99K 1% 1/16W MF-LF 402
RA145 SHOULD BE STUFFED
IF RA185 IS NOSTUFF
VR_GPU_SVT_R
RA184 VR_GPU_SVT
RA185 VR_GPU_PHSFLT_L
VR_GPU_VRDHOT_L
PM_PGOOD_REG_GPUCORE_S0
CA140 0.1UF 10% 6.3V X5R 201
PM_EN_REG_GPUCORE_S0
RA122 10K 1% 1/20W MF 201
CA122 0.001UF 20% 50V CERM 402
=PP3V3_S0_REG_GPUCORE
CA143 0.1UF 10% 6.3V CERM-X5R 0201
=PP1V8_S0_GPU_VDD
RA125 10K 1% 1/16W MF-LF 402
VR_GPU_SYS_PWROK
74LVC1G00GF SOT891
UA102
PM_PCH_PWROK
VR_GPU_RESET_L
VR_GPU_SYS_PWROK_L
QA102 2N7002TXG SOT-523-3
RA123 845 1% 1/16W MF-LF 402
CA123 0.01UF 20% 16V CERM 402
GPU CORE INPUT Filtering
CRITICAL
LA100
0.105UH-20%-31A-0.032OHM
=PP12V_S0_REG_GPUCORE
PP12V_S0_GPUCORE_FLT
SSL0705M-SM
152-0110

SVC	SVD	GPUCORE
0	0	1.1 V
0	1	1.0 V
1	0	0.9 V
1	1	0.8 V

DEFAULT-> (1, 0, 0.9 V)

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GPU VR: CORE CONTROLLER
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PP12V_S0_GPUCORE_FLT

=PP5V_S0_VRD

GPU Phase 1

UA210 IR3575M PQFN

REG_PWM_GPUCORE_1

VR_GPU_PHSFLT_L

REG_PHSFLT_GPUCORE_1_L

REG_BOOST_GPUCORE_1

REG_BOOST_GPUCORE_1_RC

VR_PHASE_GPUCORE_1

LA210 230NH-45A-0.000290HM CTX66-19270-R

PPGPUCORE_S0_SENSE_1

PPGPUCORE_S0_REG

REG_SNUBBER_GPUCORE_1

REG_GPUCORE_ISNS_1_N

REG_GPUCORE_ISNS_1_P

GPU PHASE 2

UA230 IR3575M PQFN

REG_PWM_GPUCORE_2

REG_PHSFLT_GPUCORE_2_L

REG_BOOST_GPUCORE_2

REG_BOOST_GPUCORE_2_RC

VR_PHASE_GPUCORE_2

LA230 230NH-45A-0.000290HM CTX66-19270-R

PPGPUCORE_S0_SENSE_2

PPGPUCORE_S0_REG

REG_SNUBBER_GPUCORE_2

REG_GPUCORE_ISNS_2_N

REG_GPUCORE_ISNS_2_P

GPU PHASE 3

UA250 IR3575M PQFN

REG_PWM_GPUCORE_3

REG_PHSFLT_GPUCORE_3_L

REG_BOOST_GPUCORE_3

REG_BOOST_GPUCORE_3_RC

VR_PHASE_GPUCORE_3

LA250 230NH-45A-0.000290HM CTX66-19270-R

PPGPUCORE_S0_SENSE_3

PPGPUCORE_S0_REG

REG_SNUBBER_GPUCORE_3

REG_GPUCORE_ISNS_3_N

REG_GPUCORE_ISNS_3_P

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GPU VR: CORE PHASES 1-3

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GPU PHASE 4

PP12V_S0_GPUCORE_FLT
=PP5V_S0_VRD
CRITICAL CA325 10UF 20% 16V X5R-CERM 0402-1
UA310 IR3575M PQFN
REG_BOOST_GPUCORE_4_RC
RA316 0 5% 1/10W MF-LF 603
CA316 0.22UF 10% 16V CERM 402
REG_BOOST_GPUCORE_4
REG_PWM_GPUCORE_4
RA329 0 5% 1/20W MF 201
VR_GPU_PHSELT_L
REG_PHSFLT_GPUCORE_4_L
NC
VR_PHASE_GPUCORE_4
CRITICAL CA364 39UF 20% 16V POLY-TANT CASED2-SM
CRITICAL CA350 180UF 20% 16V POLY THI
CRITICAL CA352 1UF 10% 25V X6S-CERM 0402
CRITICAL CA353 1UF 10% 25V X6S-CERM 0402
CRITICAL CA358 1UF 10% 25V X6S-CERM 0402
CRITICAL CA359 1UF 10% 25V X6S-CERM 0402
CRITICAL CA360 1UF 10% 25V X6S-CERM 0402
CRITICAL CA361 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL CA354 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL CA355 1UF 10% 25V X6S-CERM 0402
CRITICAL LA310 230NH-45A-0.000290HM CTX66-19270-R
PPGPUCORE_S0_SENSE_4
CRITICAL RA310 0.0005 1% 1W MF 0612-1
PPGPUCORE_S0_REG
CA322 10UF 20% 4V X6S-CERM 0402-1
CA323 10UF 20% 4V X6S-CERM 0402-1
NOSTUFF CA317 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_GPUCORE_4
NOSTUFF RA317 2.2 5% 1/8W MF-LF 805
REG_GPUCORE_ISNS_4_N
REG_GPUCORE_ISNS_4_P

GPU PHASE 5

=PP5V_S0_VRD
CRITICAL CA345 10UF 20% 16V X5R-CERM 0402-1
UA330 IR3575M PQFN
REG_BOOST_GPUCORE_5_RC
RA336 0 5% 1/10W MF-LF 603
CA336 0.22UF 10% 16V CERM 402
REG_BOOST_GPUCORE_5
REG_PWM_GPUCORE_5
RA349 0 5% 1/20W MF 201
REG_PHSFLT_GPUCORE_5_L
NC
VR_PHASE_GPUCORE_5
CRITICAL CA344 39UF 20% 16V POLY-TANT CASED2-SM
CRITICAL CA330 180UF 20% 16V POLY THI
CRITICAL CA332 1UF 10% 25V X6S-CERM 0402
CRITICAL CA333 1UF 10% 25V X6S-CERM 0402
CRITICAL CA338 1UF 10% 25V X6S-CERM 0402
CRITICAL CA339 1UF 10% 25V X6S-CERM 0402
CRITICAL CA340 1UF 10% 25V X6S-CERM 0402
CRITICAL CA341 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL CA335 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL CA334 1UF 10% 25V X6S-CERM 0402
CRITICAL LA330 230NH-45A-0.000290HM CTX66-19270-R
PPGPUCORE_S0_SENSE_5
CRITICAL RA330 0.0005 1% 1W MF 0612-1
PPGPUCORE_S0_REG
CA342 10UF 20% 4V X6S-CERM 0402-1
CA343 10UF 20% 4V X6S-CERM 0402-1
NOSTUFF CA337 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_GPUCORE_5
NOSTUFF RA337 2.2 5% 1/8W MF-LF 805
REG_GPUCORE_ISNS_5_N
REG_GPUCORE_ISNS_5_P

GPU PHASE 6

=PP5V_S0_VRD
CRITICAL CA365 10UF 20% 16V X5R-CERM 0402-1
UA350 IR3575M PQFN
REG_BOOST_GPUCORE_6_RC
RA356 0 5% 1/10W MF-LF 603
CA356 0.22UF 10% 16V CERM 402
REG_BOOST_GPUCORE_6
REG_PWM_GPUCORE_6
RA369 0 5% 1/20W MF 201
REG_PHSFLT_GPUCORE_6_L
NC
VR_PHASE_GPUCORE_6
CRITICAL CA324 39UF 20% 16V POLY-TANT CASED2-SM
CRITICAL CA310 180UF 20% 16V POLY THI
CRITICAL CA312 1UF 10% 25V X6S-CERM 0402
CRITICAL CA313 1UF 10% 25V X6S-CERM 0402
CRITICAL CA318 1UF 10% 25V X6S-CERM 0402
CRITICAL CA319 1UF 10% 25V X6S-CERM 0402
CRITICAL CA320 1UF 10% 25V X6S-CERM 0402
CRITICAL CA321 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL CA315 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL CA314 1UF 10% 25V X6S-CERM 0402
CRITICAL LA350 230NH-45A-0.000290HM CTX66-19270-R
PPGPUCORE_S0_SENSE_6
CRITICAL RA350 0.0005 1% 1W MF 0612-1
PPGPUCORE_S0_REG
CA362 10UF 20% 4V X6S-CERM 0402-1
CA363 10UF 20% 4V X6S-CERM 0402-1
NOSTUFF CA357 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_GPUCORE_6
NOSTUFF RA357 2.2 5% 1/8W MF-LF 805
REG_GPUCORE_ISNS_6_N
REG_GPUCORE_ISNS_6_P

GPU OUTPUT DECOUPLING

PPGPUCORE_S0_REG
CRITICAL CA380 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL CA381 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL CA382 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL CA383 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL CA384 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL CA385 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
CRITICAL CA386 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

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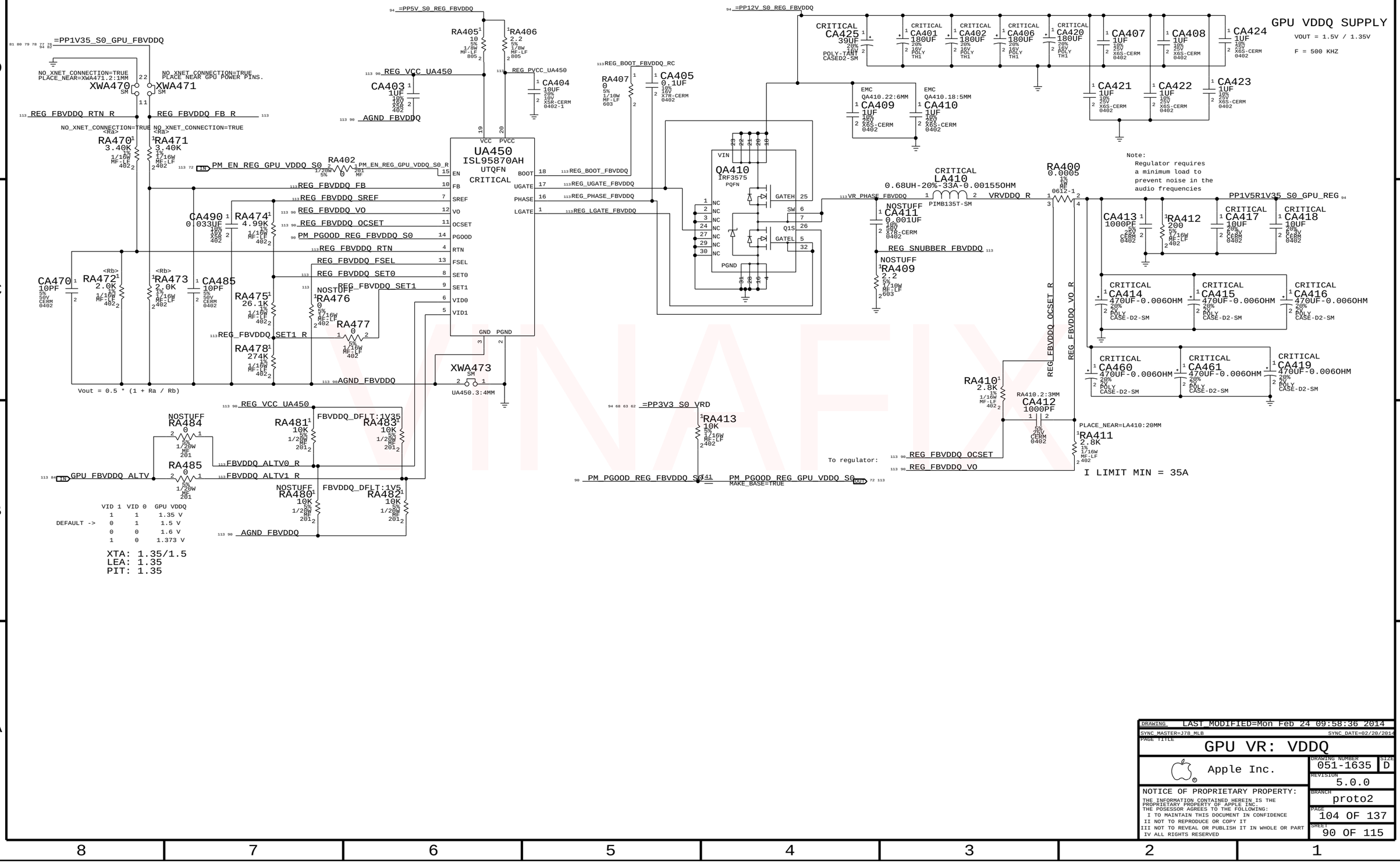

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GPU VR: VDDQ
Apple Inc.
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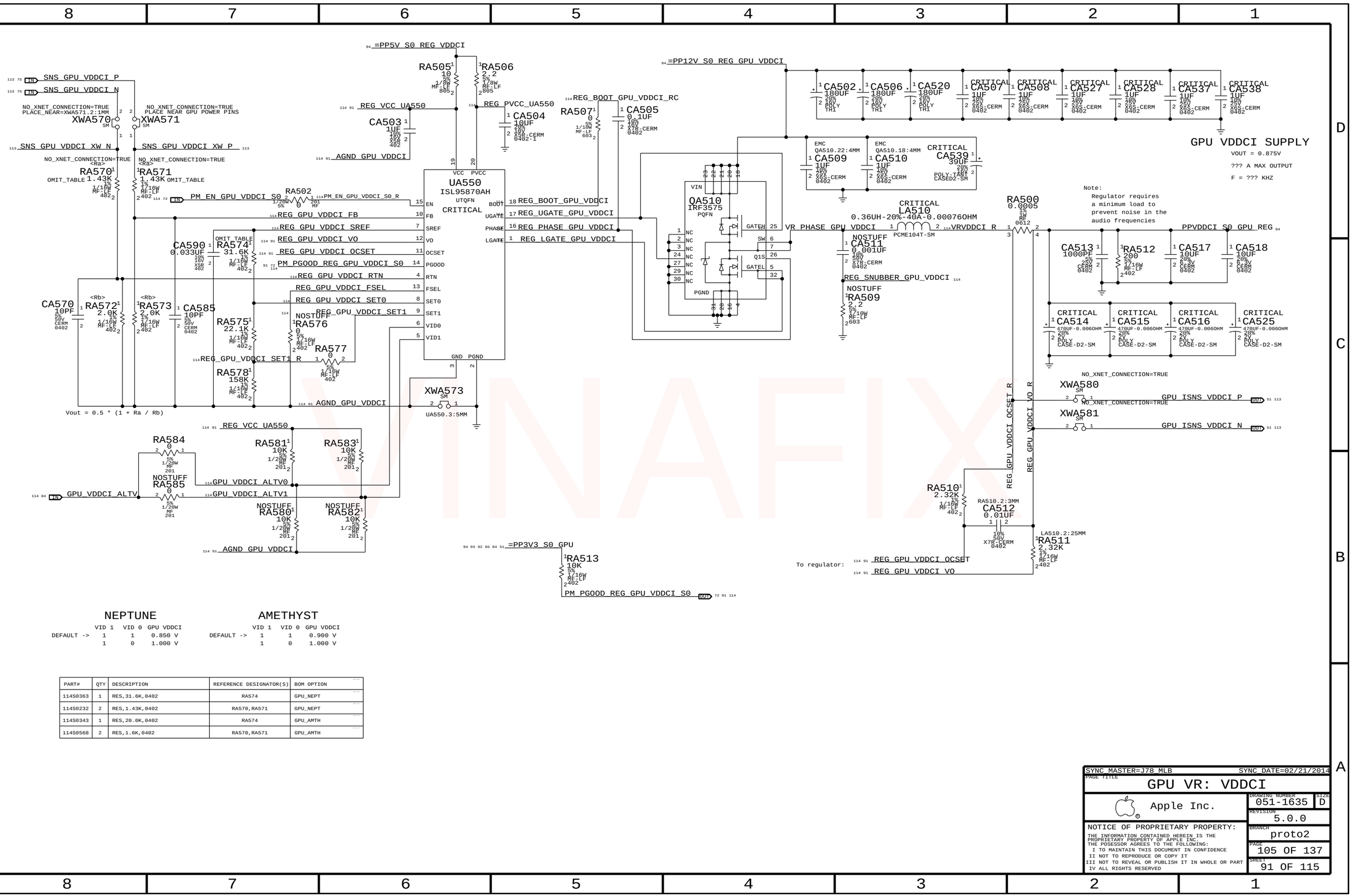

NEPTUNE

	VID 1	VID 0	GPU VDDCI
DEFAULT ->	1	1	0.850 V
	1	0	1.000 V

AMETHYST

	VID 1	VID 0	GPU VDDCI
DEFAULT ->	1	1	0.900 V
	1	0	1.000 V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0363	1	RES,31.6K,0402	RA574	GPU_NEPT
114S0232	2	RES,1.43K,0402	RA570,RA571	GPU_NEPT
114S0343	1	RES,20.0K,0402	RA574	GPU_AMTH
114S0568	2	RES,1.6K,0402	RA570,RA571	GPU_AMTH

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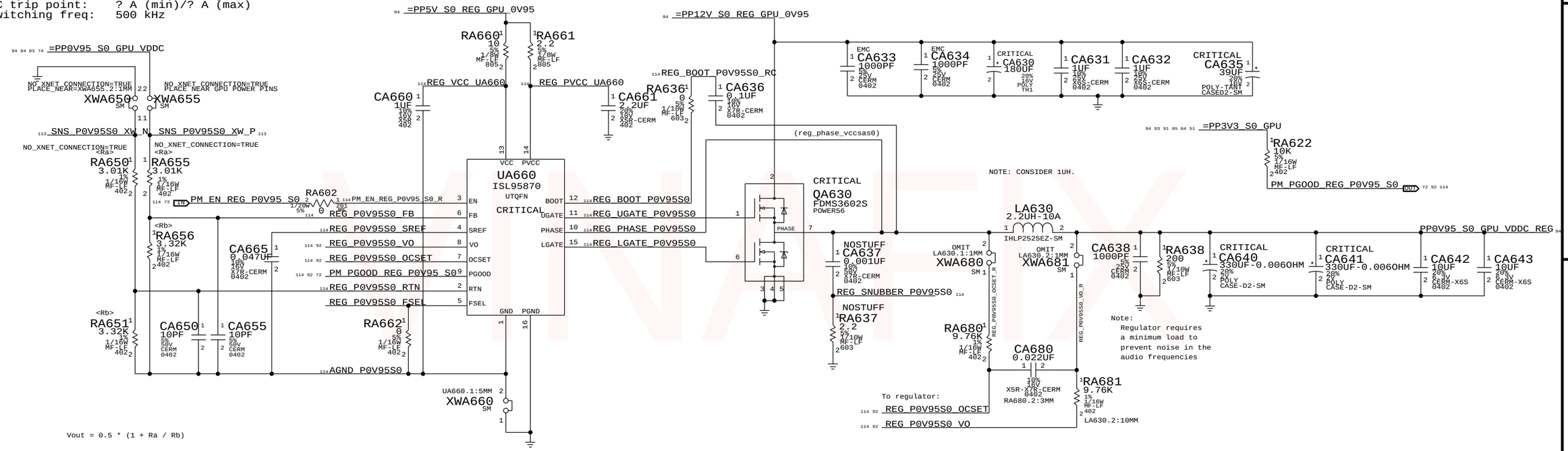
GPU VDDC (0.95V) S0 REGULATOR

Max avg current: 8.10 A (BUDGET)
Max peak current: 8.50 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



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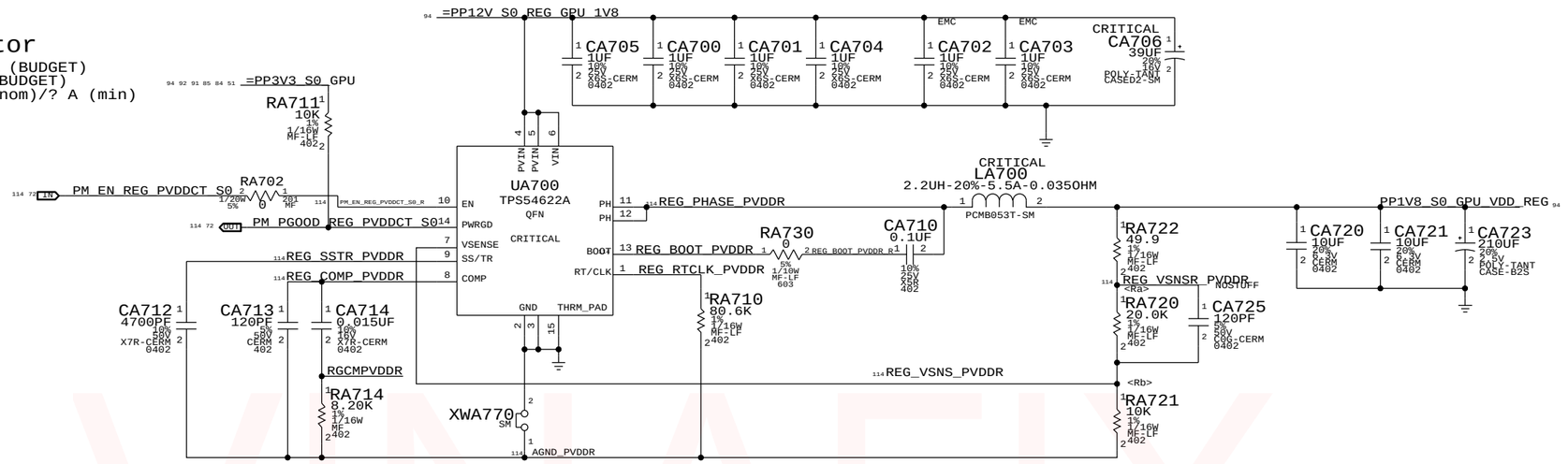
1.8V S0 Regulator

Max avg current: 2.4 A (BUDGET)
Max peak current: 3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



VOUT = 0.6 * (1 + RA / RB)

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G3 Rails

Always on: Keeps the PCH RTC alive

108 PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC — 19
- =PP3V3_G3_PCH_RTC — 15
- =PP3V3_G3_PCH — 11 12

G3H Rails

On with AC/DC plugged in

108 PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC — 62
- =PP12V_G3H_SNS_R — 50

108 PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS — 50
- =PP12V_G3H_P3V42 — 62
- =PP12V_G3H_FET_P12V_S0 — 71
- =PP12V_G3H_FET_P12V_S5 — 71

108 PP3V42_G3H (MAKE_BASE=TRUE)
- PP3V42_G3H_REG — 62
- =PP3V3_G3H_BT — 34
- =PP3V3_G3H_RTC_D — 19
- =PP3V3_G3H_SMC — 46 47 53
- =PP3V3_G3H_SMC_USBMUX — 44
- =PPVIN_G3H_SMCVREF — 47
- =PP3V3_G3H_LPCPLUS — 48

Ground/Common

GND (MAKE_BASE=TRUE)

S5 Rails

On when in S5

108 PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET — 71
- =PP12V_S5_REG_P3V3P5V_S5 — 67
- =PP12V_S5_REG_VDDQ_S3 — 66
- =PP12V_S5_PWRCTL — 71 72
- =PPHV_SW_TBTAPWRSW — 31
- =PPHV_SW_TBTBPWRSW — 32
- =PP12V_S5_SNS — 50

108 PP5V_S5 (MAKE_BASE=TRUE)
- PP5V_S5_LDO — 67

108 PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_REG — 67
- =PP3V3_S5_FET_P3V3_S0 — 71
- =PP3V3_S5_FET_P3V3_S4 — 71
- =PP3V3_S5_SMC — 47
- =PP3V3_S5_LED — 3
- =PP3V3_S5_PCH_VCCSUS_GPIO — 11 12 13 14 15 17
- =PP3V3_S5_PCH_VCCDSW — 15 17
- =PP3V3_S5_PCH_VCC_SPI — 15 17
- =PP3V3_S5_PCH_VCCSUS_HDA — 15 17
- =PP3V3_S5_PCH_VCCSUS_USB — 15 17
- =PP3V3_S5_PCH_VCCSUS_RTC — 15 17
- =PP3V3_S5_PCH_VCCSUS_USB3 — 15
- =PP3V3_S5_PCH — 19 20
- =PP3V3_S5_PWRCTL — 72 73
- =PP3V3_S5_ROM — 48
- =PP3V3_S5_VRD — 67
- =PP3V3_S5_XDP — 18
- =PP3V3_S5_SENSE — 50
- =PP3V3_S5_SNS — 51

S4 Rails

Enabled when system has AC and is in run or sleep

108 PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_REG — 67
- =PP5V_S4_REG_VDDQ_S3 — 66
- =PP5V_S4_FET_P5V_S0 — 71
- =PP5V_S4_MEMRESET — 21
- =PP5V_S4_USB — 44 45

108 PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET — 71
- =PP3V3_S4_FET_ENET — 38
- =PP3V3_S4_PWRCTL — 66 71
- =PP3V3_S4_LED — 3
- =PP3V3_S4_MEMRESET — 21
- =PP3V3_S4_PCH — 13
- =PP3V3_S4_PM — 21
- =PP3V3_S4_SDCARD — 39
- =PP3V3_S4_SMC — 47
- =PP3V3_S4_TBT — 20 28 29 31 32 72
- =PP3V3_S4_AUDIO_DIG — 58
- =PP3V3_S4_AP_SNS_R — 50
- =PP3V3_S3_VREFMRGN — 22
- =PP3V3_S4_TBTAPWRSW — 31
- =PP3V3_S4_TBTBPWRSW — 32

108 PP3V3_S4_AP (MAKE_BASE=TRUE)
- PP3V3_S4_AP_SNS — 50
- =PP3V3_S4_AP — 34 47

S3 Rails

Enabled when system is in run or sleep

108 PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET — 38
- =PP3V3_ENET_PHY — 37 38
- =PP3V3_ENET_SYSCLK — 19
- =PPVDDIO_ENET_CLK — 19

106 PPVDDQ_S3 (MAKE_BASE=TRUE)
- PPVDDQ_S3_REG — 66
- =PPVDDQ_S3_SNS_DDR_R — 51
- =PPVDDQ_S3_FET_VDDQ_S0 — 71

THIS IS 1.5V RAIL

106 PPVDDQ_S3_DDR (MAKE_BASE=TRUE)
- PPVDDQ_S3_SNS_DDR — 51
- =PPDDR_S3_MEMVREF — 22
- =PPVDDQ_S3_MEM_A — 23 24
- =PPVDDQ_S3_MEM_B — 25 26
- =PPVDDQ_S3_MEMRESET — 21
- =PPVDDQ_S3_LDO_DDRVTT — 66

THIS IS 1.5V RAIL

S0 Rails

Enabled when system is in run

108 PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET — 71
- =PP12V_S0_AUDIO_SPKRAMP — 56 57
- =PP12V_S0_FAN — 53
- =PP12V_S0_SNS_GPUCORE_R — 50
- =PP12V_S0_LCD — 42
- =PP12V_S0_REG_CPUVCC_S0 — 64
- =PP12V_S0_REG_P1V05_S0 — 68
- =PP12V_S0_SNS_FBVDDQ_R — 50
- =PP12V_S0_HDD — 36
- =PP12V_S0_BKLT — 69

108 PP12V_S0_GPU_AUX (MAKE_BASE=TRUE)
- PP12V_S0_SNS_GPU_AUX — 50
- =PP12V_S0_REG_GPU_0V95 — 92
- =PP12V_S0_REG_GPU_1V8 — 93

108 PP12V_S0_GPUCORE (MAKE_BASE=TRUE)
- PP12V_S0_SNS_GPUCORE — 50
- =PP12V_S0_REG_GPUCORE — 87
- =PP12V_S0_REG_GPU_VDDCI — 91

108 PPHDD12_S0 (MAKE_BASE=TRUE)
- PP12V_S0_HDD_FET — 36
- =PP12V_S0_HDD_SNS_R — 50

108 PP12V_S0_HDD (MAKE_BASE=TRUE)
- PP12V_S0_HDD_SNS — 50
- =PP12V_S0_HDD_PWR — 36

109 PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)
- PP12V_S0_SNS_FBVDDQ — 50
- =PP12V_S0_REG_FBVDDQ — 90

108 PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET — 71
- =PP5V_S0_AUDIO — 54 61
- =PP5V_S0_BKLT — 69
- =PP5V_S0_ISENSE — 50
- =PP5V_S0_LPCPLUS — 48
- =PP5V_S0_REG_CPUVCC_S0 — 63 64 65
- =PP5V_S0_REG_FBVDDQ — 90
- =PP5V_S0_REG_P1V05 — 68
- =PP5V_S0_HDD — 36
- =PP5V_S0_VRD — 87 88 89
- =PP5V_S0_GPU — 51
- =PP5V_S0_REG_VDDCI — 91
- =PP5V_S0_REG_GPU_0V95 — 92
- =PP5V_S0_CAMERA — 40
- =PP5V_S0_REG_GPUCORE — 87

108 PPHDD_S0 (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET — 36
- =PPHDD_S0_SNS_R — 50

108 PP5V_S0_HDD (MAKE_BASE=TRUE)
- PPHDD_S0_SNS — 50
- =PP5V_S0_HDD_PWR — 36

108 PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET — 71
- =PP3V3_S0_AUDIO — 40 54 56 57 60
- =PP3V3_S0_AUDIO_DIG — 58
- =PP3V3_S0_BKLT — 69
- =PP3V3_S0_DP — 33 42 49
- =PP3V3_S0_ENET — 37
- =PP3V3_S0_FAN — 53
- =PP3V3_S0_GPU — 51 84 85 91 92 93
- =PP3V3_S0_INTDPMUX — 42 43
- =PP3V3_S0_LED — 3
- =PP3V3_S0_LED_SATA — 35
- =PP3V3_S0_MEM_A_SPD — 23 24
- =PP3V3_S0_MEM_B_SPD — 25 26
- =PP3V3_S0_PCH — 19
- =PP3V3_S0_PCH_VCC3_3_GPIO — 11 12 13 14 15 17
- =PP3V3_S0_PCH_VCC3_3_THRM — 15 17
- =PP3V3_S0_PCH_VCCCLK3_3 — 15 17
- =PP3V3_S0_PCH_VCC3_3_HVCMOS — 15 17
- =PP3V3_S0_PCH_VCC_FUSE — 15 17
- =PP3V3_S0_PWRCTL — 71
- =PP3V3_S0_RSTBUF — 20
- =PP3V3_S0_SDCARD — 39
- =PP3V3_S0_SENSE — 36 50 51 52
- =PP3V3_S0_SMBUS — 49
- =PP3V3_S0_SMBUS_SMC_0 — 49
- =PP3V3_S0_SMBUS_SMC_1 — 49
- =PP3V3_S0_SMBUS_SMC_3 — 49
- =PP3V3_S0_SMC — 47
- =PP3V3_S0_VRD — 62 63 68 90
- =PP3V3_S0_PCH_GPIO — 29
- =PP3V3_S0_PCH_VCC3_3_USB — 15 17
- =PPSSD_S0_SNS_R — 51
- =PP3V3_TBT_PCH_GPIO — 20
- =PP3V3_S0_CAMERA — 40 41
- =PP3V3_S0_ALS — 40
- =PP3V3_S0_SMBUS_SMC_2 — 49
- =PP3V3_S0_REG_GPUCORE — 87

108 PPSSD_S0 (MAKE_BASE=TRUE)
- PPSSD_S0_SNS — 51
- =PP3V3_S0_SSD — 35

106 PP1V5_S0 (MAKE_BASE=TRUE)
- PP1V5_S0_FET — 71
- =PP1V5_S0_SNS_R — 51

106 PP1V5_S0_PCH (MAKE_BASE=TRUE)
- PP1V5_S0_SNS — 51
- =PP1V5_S0_CPU_MEM — 6 8 10
- =PP1V5_S0_AUD_DIG — 54
- =PP1V5_S0_PCH_VCCVRM — 17
- =PP1V5_S0_PCH_RCOMP — 12 13
- =PP1V5_S0_PCH_SATA — 11
- =PP1V5_S0_PCH_CLK — 11 19
- =PP1V5_S0_DP — 43

106 PPDDRVTT_S0 (MAKE_BASE=TRUE)
- PPDDRVTT_S0_LDO — 66
- =PPDDRVTT_S0_CLAMP — 21
- =PPDDRVTT_S0_MEM_A — 23 24
- =PPDDRVTT_S0_MEM_B — 25 26

107 PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)
- PPCPUVCC_S0_REG — 64 65
- =PPCPUVCC_S0_CPU — 6 8 10 50 63

GPU Rails (S0)

Enabled when system is in run

113 PPGPUCORE_S0 (MAKE_BASE=TRUE)
- PPGPUCORE_S0_REG — 88 89
- =PPGPUCORE_S0 — 75 76
- =PPGPUCORE_S0_SNS — 50

113 PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)
- PP1V5R1V35_S0_GPU_REG — 90
- =PP1V35_S0_GPU_FBVDDQ — 76 77 78 79 80 81 82 90

106 PP1V05_S0 (MAKE_BASE=TRUE)
- PP1V05_S0_REG — 68
- =PP1V05_S0_PCH_VCC — 15 17
- =PP1V05_S0_PCH_VCCCLK_CLK100 — 15 17
- =PP1V05_S0_PCH_VCCASW — 15 17
- =PP1V05_S0_PCH_VCC_CLK — 17
- =PP1V05_S0_PCH_VCCIO_FDI — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC — 15 17
- =PP1V05_S0_PCH_VCCUSBPLL — 15 17
- =PP1V05_S0_PCH_VCCIO — 15 17
- =PP1V05_S0_PCH_VCCCLK_SSC100 — 15 17
- =PP1V05_S0_PCH_VCCCLK_CLK135 — 15 17
- =PP1V05_S0_PCH_VCCIO_USB2 — 15 17
- =PP1V05_S0_PCH_V_PROC_IO — 14 15 17
- =PP1V05_S0_SNS — 50
- =PP1V05_S0_SMC — 47
- =PP1V05_S0_XDP — 18

109 PPVDDCI_S0_GPU (MAKE_BASE=TRUE)
- PPVDDCI_S0_GPU_REG — 91
- =PPVDDCI_S0_GPU — 75

108 PP0V95_S0_GPU_VDDC (MAKE_BASE=TRUE)
- PP0V95_S0_GPU_VDDC_REG — 92
- =PP0V95_S0_GPU_VDDC — 74 83 84 92
- =PP0V95_S0_GPU_PCIEVDDC — 74

108 PP1V8_S0_GPU_VDD (MAKE_BASE=TRUE)
- PP1V8_S0_GPU_VDD_REG — 93
- =PP1V8_S0_GPU_VDD — 83 84 85 87
- =PP1V8_S0_CAMERA — 40 41
- =PP1V8_S0_GPU_PEX_IO — 74

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

108 29 28 PP3V3_TBTLC (MAKE_BASE=TRUE)
- =PPVDDIO_TBT_CLK — 19

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PEG aliases

100 74 PEG_D2R_N<0..15> ⟷ =PEG_D2R_N<15..0> 5
MAKE_BASE=TRUE

100 74 PEG_D2R_P<0..15> ⟷ =PEG_D2R_P<15..0> 5
MAKE_BASE=TRUE

100 74 PEG_R2D_C_N<0..15> ⟷ =PEG_R2D_C_N<15..0> 5
MAKE_BASE=TRUE

100 74 PEG_R2D_C_P<0..15> ⟷ =PEG_R2D_C_P<15..0> 5
MAKE_BASE=TRUE

DDI/FDI ALIASES

5 TP_DP_IG_B_MLN<0..3> I64 NO_TEST=TRUE NC_DP_IG_B_MLN<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_B_MLP<0..3> NO_TEST=TRUE NC_DP_IG_B_MLP<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_C_MLN<0..3> NO_TEST=TRUE NC_DP_IG_C_MLN<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_C_MLP<0..3> NO_TEST=TRUE NC_DP_IG_C_MLP<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_D_MLN<0..3> NO_TEST=TRUE NC_DP_IG_D_MLN<0..3>
MAKE_BASE=TRUE

5 TP_DP_IG_D_MLP<0..3> NO_TEST=TRUE NC_DP_IG_D_MLP<0..3>
MAKE_BASE=TRUE

GPU ALIASES

84 74 GPU_RESET_L ⟷ TP_GPU_RESET_L 20
MAKE_BASE=TRUE

87 VR_GPU_RESET_L ⟷ TP_VR_GPU_RESET_L 20
MAKE_BASE=TRUE

MEMORY PGOOD

21 =PM_PGOOD_MEM_S0 ⟷ PM_PGOOD_FET_REG_P1V5_S0 71 72
MAKE_BASE=TRUE

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Signal Aliases

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CPU Reserved

102 18 6 TP_CPU_CFG<15..12> — NC_CPU_CFG<15..12>
MAKE_BASE=TRUE

CPU Memory

7 TP_MEM_A_DQS_N<8> — NC_MEM_A_DQSNX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_A_DQS_P<8> — NC_MEM_A_DQSPX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_B_DQS_N<8> — NC_MEM_B_DQSNX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_B_DQS_P<8> — NC_MEM_B_DQSPX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCIe

11 TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4PX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE5N — NC_PCIE_CLK100M_PE5NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE5P — NC_PCIE_CLK100M_PE5PX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE7N — NC_PCIE_CLK100M_PE7NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE7P — NC_PCIE_CLK100M_PE7PX
MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

11 TP_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3
MAKE_BASE=TRUE NO_TEST=TRUE

TP_ITPXDP_CLK100MP — ITPXDP_CLK100M_P 11 102
MAKE_BASE=TRUE NO_TEST=TRUE

TP_ITPXDP_CLK100MN — ITPXDP_CLK100M_N 11 102
MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

13 TP_LPC_DREQ0_L — NC_LPC_DREQ0_L
MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

11 TP_HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_HDA_SDIN2 — NC_HDA_SDIN2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_HDA_SDIN3 — NC_HDA_SDIN3
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCI_CLK33M_OUT2 — NC_PCI_CLK33M_OUT2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3
MAKE_BASE=TRUE NO_TEST=TRUE

11 PEG_CLKREQ_L — NC_PEG_CLKREQ_L
MAKE_BASE=TRUE NO_TEST=TRUE

AUDIO MISC

109 42 AUDIO_MUTE_L — NC_AUDIO_MUTE_L
MAKE_BASE=TRUE NO_TEST=TRUE

109 42 AUDIO_SCLK — NC_AUDIO_SCLK
MAKE_BASE=TRUE NO_TEST=TRUE

109 42 AUDIO_WS — NC_AUDIO_WS
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=J78_MLB SYNC_DATE=12/05/2013

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Unused Signal Aliases

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Functional / ICT Test

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J17 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT,BGA_VRAM	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	0.070 MM	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 MM	
2	Plane	1 oz	
	Core	0.101 MM	
3	Signal	0.5 oz	
	Prepreg	0.115 MM	
4	Plane	1 oz	
	Core	0.076 MM	
5	Signal	0.5 oz	
	Prepreg	0.380 MM	
6	Plane	1 oz	
	Core	0.076 MM	
7	Plane	1 oz	
	Prepreg	0.380 MM	
8	Signal	0.5 oz	
	Core	0.076 MM	
9	Plane	1 oz	
	Prepreg	0.115 MM	
10	Signal	0.5 oz	
	Core	0.101 MM	
11	Plane	1 oz	
	Prepreg	0.071 MM	
Btm	Signal	0.5 oz (Cu plated)	

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.381 MM	?

Main Segment Min Spacing Rules (mils) (Shark Bay PDG, Intel Doc# 486712)

Table	Trace	Design	Iso	Design	Comments
4-2	4	(diff)	15	19.69	CLK trace spacing controlled by =68_OHM_DIFF
4-3	8	9.84	12	13.78	
4-4	6	7.87	12	13.78	
4-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	7 23
DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	7 23
DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	7 24
DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	7 24
DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	7 23
DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	7 23
DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	7 23
DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	7 24
DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	7 24
DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	7 24
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	7 23 24
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	7 23 24
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	7 23 24
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	7 23 24
DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	7 23 24
DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	7 27
DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	7 27
DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	7 27
DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	7 27
DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	7 27
DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	7 27
DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	7 27
DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	7 27
DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	7 27
DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	7 27
DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	7 27
DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	7 27
DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	7 27
DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	7 27
DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	7 27
DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	7 27
DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	7 27
DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	7 27
DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	7 27
DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	7 27
DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	7 27
DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	7 27
DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	7 27
DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	7 27
Channel B				
DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	7 25
DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	7 25
DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	7 26
DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	7 26
DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	7 25
DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	7 25
DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	7 25
DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	7 26
DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	7 26
DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	7 26
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	7 25 26
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	7 25 26
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	7 25 26
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	7 25 26
DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	7 25 26
DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	7 27
DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	7 27
DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	7 27
DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	7 27
DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	7 27
DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	7 27
DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	7 27
DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	7 27
DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	7 27
DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	7 27
DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	7 27
DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	7 27
DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	7 27
DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	7 27
DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	7 27
DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	7 27
DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	7 27
DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	7 27
DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	7 27
DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	7 27
DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	7 27
DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	7 27
DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	7 27
DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	7 27
Reset				
DDR_50S			MEM_RESET_L	21 23 24 25 26
SM COMP				
DDR_COMP_PHY		DDR_COMP	CPU_SM_RCOMP<0..2>	6

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: DDR3 Constraints

Apple Inc.

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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_R2D_80D	*	=80_OHM_DIFF	0.12 MM	=80_OHM_DIFF	=80_OHM_DIFF	0.12 MM	=80_OHM_DIFF
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE3_PHY	*	PCIE_80D
PCIE3_R2D_PHY	*	PCIE_R2D_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
PEG_R2D	PEG_R2D	*	PEG_SAME_DIR
PEG_D2R	PEG_D2R	*	PEG_SAME_DIR
PEG_D2R	PEG_R2D	*	PEG_ALT_DIR
PEG_D2R	POWER	*	PEG2PWR_ISO
PEG_R2D	POWER	*	PEG2PWR_ISO
PEG_D2R	VR_SWITCH	*	PEG2VR_ISO
PEG_R2D	VR_SWITCH	*	PEG2VR_ISO
PEG_D2R	*	*	PEG_ISO
PEG_R2D	*	*	PEG_ISO

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG*	GDDR*	*	PEG_GDDR_ISO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PEG_SAME_DIR	*	=3.5X_DIELECTRIC	?
PEG_ALT_DIR	*	=7X_DIELECTRIC	?
PEG2PWR_ISO	*	1 MM	?
PEG2VR_ISO	*	1 MM	?
PEG_ISO	*	=4:1_SPACING	?
PEG_GDDR_ISO	*	=5.6X_DIELECTRIC	?

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
144D PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<15>	74
144J PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<15>	74
144F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<15>	74 95
144L	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<15>	74 95
144C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<15>	74 95
144A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<15>	74 95
144H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<15>	74
144E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<15>	74
144B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<14>	74
144K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<14>	74
145D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<14>	74 95
145J	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<14>	74 95
145C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<14>	74 95
145A PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<14>	74 95
145H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<14>	74
145E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<14>	74
145B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<13>	74
145K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<13>	74
146D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<13>	74 95
146J	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<13>	74 95
145C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<13>	74 95
146A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<13>	74 95
146H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<13>	74
146E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<13>	74
146B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<12>	74
146K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<12>	74
147D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<12>	74 95
146F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<12>	74 95
146C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<12>	74 95
147A PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<12>	74 95
146G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<12>	74
147J	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<12>	74
147B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<11>	74
147K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<11>	74
147D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<11>	74 95
147F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<11>	74 95
147C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<11>	74 95
147A PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<11>	74 95
147G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<11>	74
147E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<11>	74
148B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<10>	74
148K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<10>	74
148D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<10>	74 95
148J	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<10>	74 95
148C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<10>	74 95
148A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<10>	74 95
148H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<10>	74
148E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<10>	74
149B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<9>	74
149K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<9>	74
149D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<9>	74 95
149F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<9>	74 95
149C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<9>	74 95
149A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<9>	74 95
149G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<9>	74
149E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<9>	74
149B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<8>	74
149K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<8>	74
149D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<8>	74 95
149F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<8>	74 95
149C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<8>	74 95
149A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<8>	74 95
149G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<8>	74
149E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<8>	74

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
160D PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<7>	74
160J PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<7>	74
160F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<7>	74 95
160L	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<7>	74 95
160C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<7>	74 95
160A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<7>	74 95
161H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<7>	74
161E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<7>	74
161B PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<6>	74
161K PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<6>	74
161D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<6>	74 95
161F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<6>	74 95
161C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<6>	74 95
161A PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<6>	74 95
161G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<6>	74
161E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<6>	74
152B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<5>	74
152K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<5>	74
152D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<5>	74 95
152F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<5>	74 95
152C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<5>	74 95
152A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<5>	74 95
162H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<5>	74
162E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<5>	74
152B PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<4>	74
152K PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<4>	74
153D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<4>	74 95
153F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<4>	74 95
153C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<4>	74 95
153A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<4>	74 95
153G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<4>	74
153E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<4>	74
163B PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<3>	74
163K PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<3>	74
163D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<3>	74 95
163F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<3>	74 95
163C PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<3>	74 95
163A PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<3>	74 95
154H	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<3>	74
154E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<3>	74
154B PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<2>	74
154K PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<2>	74
154D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<2>	74 95
154F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<2>	74 95
154C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<2>	74 95
154A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<2>	74 95
154G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<2>	74
154E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<2>	74
164B PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<1>	74
164K PCIE_GEN3_R2D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<1>	74
164D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<1>	74 95
164F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<1>	74 95
164C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<1>	74 95
164A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<1>	74 95
164G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<1>	74
164E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<1>	74
165B PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_P<0>	74
165K PCIE_GEN3_R2D_RVSD	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_N<0>	74
165D	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_P<0>	74 95
165F	PCIE3_R2D_PHY	PEG_R2D	PEG_R2D_C_N<0>	74 95
165C PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<0>	74 95
165A PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<0>	74 95
165G	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<0>	74
165E	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<0>	74
CPU PCIe Clocks				
166D PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P	11 74
166C PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N	11 74
CPU PCIe Compensation				
167A	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_RCOMP	5
CPU eDP Compensation				
157A	COMP_PCIE_PHY	COMP_PCIE	CPU_EDP_RCOMP	5

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	DMI_COMP

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?
DMI2PWR_ISO	*	0.5 MM	?
DMI2VR_ISO	*	1 MM	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	POWER	*	DMI2PWR_ISO
DMI_S2N	POWER	*	DMI2PWR_ISO
DMI_N2S	VR_SWITCH	*	DMI2VR_ISO
DMI_S2N	VR_SWITCH	*	DMI2VR_ISO
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_COMP	*	Y	0.2032 MM	0.2032 MM	3 MM	=STANDARD	=STANDARD

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3..0>	28
PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3..0>	28
	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3..0>	13 28
	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3..0>	13 28
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3..0>	13 28
PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3..0>	13 28
	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3..0>	28
	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3..0>	28
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
x1 AirPort				
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	34
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	34
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	13 34
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	13 34
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	13 34
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	13 34
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
x1 Caesar IV				
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	37
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	37
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	13 37
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	13 37
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	13 37
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	13 37
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	37
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	11 37
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	11 37
x2 SSD				
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35
PCH PCIE Compensation				
	COMP_DMI_PHY	COMP_PCIE	PCH_PCIE_RCOMP	13

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_P<3..0>	5 12
DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_N<3..0>	5 12
DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_P<3..0>	5 12
DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_N<3..0>	5 12
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	6 11
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	6 11
DMI Compensation				
	COMP_DMI_PHY	COMP_PCIE	PCH_DMI_RCOMP	12

CPU DP REF CLK

Electrical Contraint Set	Physical	Spacing		
CPU DP REF CLK				
CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	SATA_50S
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
SATA2PWR_ISO	*	0.5 MM	?
SATA2VR_ISO	*	1 MM	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
SATA	POWER	*	SATA2PWR_ISO
SATA	VR_SWITCH	*	SATA2VR_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
I90 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_P NO_TEST=TRUE	35
I92 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_N NO_TEST=TRUE	35
I89	SATA_PHY_90	SATA	SATA_HDD_R2D_C_P	11 35
I91	SATA_PHY_90	SATA	SATA_HDD_R2D_C_N	11 35
I84 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_P	11 35
I85 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_N	11 35
I81	SATA_PHY_90	SATA	SATA_HDD_D2R_C_P NO_TEST=TRUE	35
I83	SATA_PHY_90	SATA	SATA_HDD_D2R_C_N NO_TEST=TRUE	35
PCH SATA Port 1 (SSD)				
I96 SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_P<0..1>	11 35
I98 SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_N<0..1>	11 35
I115 SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_P<0..1>	35
I114 SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_N<0..1>	35
I109 SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_P<0..1>	11 35
I107 SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_N<0..1>	11 35
PCH SATA Compensation				
I105	COMP_SATA_PHY	COMP_SATA	PCH_SATA_RCOMP	11

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
I37	XDP_PHY	XDP	XDP_BPM_L<7..0>	6 18
I38	XDP_PHY	XDP	CPU_CFG<17..0>	6 18 96
I39 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	
I40 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	
I41 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	11 96
I43 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	11 96
I42	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	
I44	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	
I45	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	6 18
I46	XDP_PHY	XDP	XDP_CPU_TMS	6 18
I47	XDP_PHY	XDP	XDP_CPU_TDI	6 18
I48	XDP_PHY	XDP	XDP_CPU_TDO	6 18
PCH XDP				
I49	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	11 18
I50	XDP_PHY	XDP	XDP_PCH_TMS	11 18
I51	XDP_PHY	XDP	XDP_PCH_TDI	11 18
I52	XDP_PHY	XDP	XDP_PCH_TDO	11 18

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Imp	Design	Iso	Design	Comments
6-1/6-2	85	85	12	11.81	FDI main length

FDI Compensation Rules (mils)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

FDI

Electrical Contraint Set	Physical	Spacing		
FDI				
I112	FDI_SE_PHY	FDI	FDI_CSYNC	5 12
I113	FDI_SE_PHY	FDI	FDI_INT	5 12
FDI Compensation				
I110	COMP_FDI_PHY	COMP_FDI	PCH_FDI_RCOMP	12

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
J33	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	11 19
J32	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	11 19

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
H30	LPC_55S	LPC	LPC_AD<3..0>	13 46 48
H33	LPC_55S	LPC	LPC_AD_R<3..0>	13
H31	LPC_55S	LPC	LPC_FRAME_L	13 46 48
H37	LPC_55S	LPC	LPC_FRAME_R_L	13
LPC Clocks				
H36	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 48
H44	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
H34	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	19 46
H42	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	11 19

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
H38	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	11 19
H40	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB_R	11
PCH RTC 32K				
H43	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	11 19
H41	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	11 19
H35	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	19
SMC 32K				
H39	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	12 47
H45	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	46 47

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
H27	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	19
H29	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	19
H28	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	19
25M Reference Clocks				
H46	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	19 37
H48	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	19
H49	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	19 28
H50	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	28

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
H55	HDA_55S	HDA	HDA_BIT_CLK	11 54
H61	HDA_55S	HDA	HDA_BIT_CLK_R	11
H56	HDA_55S	HDA	HDA_RST_L	11 54
H62	HDA_55S	HDA	HDA_RST_R_L	11
H65	HDA_55S	HDA	HDA_SDOUT	11 54
H67	HDA_55S	HDA	HDA_SDOUT_R	11 19
H66	HDA_55S	HDA	HDA_SYNC	11 54
H68	HDA_55S	HDA	HDA_SYNC_R	11
H64	HDA_55S	HDA	HDA_SDIN0	11 54
H69	HDA_55S	HDA	AUD_SDI_R	54
SPDIF				
H47		HDA	AUD_SPDIF_CHIP	54
H71		HDA	AUD_SPDIF_OUT	54 58

SPI Bootrom

Electrical Contraint Set	Physical	Spacing			
SPI ROM					
H91		SPI_50S	SPI	SPI_CLK_R	13 48
H92	SPI_CLK	SPI_50S	SPI	SPI_CLK	48
H93		SPI_50S	SPI	SPI_ALT_CLK	48
H40		SPI_50S	SPI	SPI_SMC_CLK	46 48
H40		SPI_50S	SPI	SPI_MLB_CLK	48
H95		SPI_50S	SPI	SPI_CS0_R_L	13 48
H90	SPI_CS_L	SPI_50S	SPI	SPI_CS0_L	48
H96		SPI_50S	SPI	SPI_ALT_CS_L	48
H40		SPI_50S	SPI	SPI_SMC_CS_L	46 48
H97		SPI_50S	SPI	SPI_MLB_CS_L	48
H98		SPI_50S	SPI	SPI_MOSI_R	13 48
H46	SPI_MOSI	SPI_50S	SPI	SPI_MOSI	48
H41		SPI_50S	SPI	SPI_ALT_MOSI	48
H43		SPI_50S	SPI	SPI_SMC_MOSI	46 48
H43		SPI_50S	SPI	SPI_MLB_MOSI	48
H40	SPI_MISO	SPI_50S	SPI	SPI_MISO	13 48
H40		SPI_50S	SPI	SPI_ALT_MISO	48
H43		SPI_50S	SPI	SPI_SMC_MISO	46 48
H43		SPI_50S	SPI	SPI_MLB_MISO	48
H40		SPI_50S	SPI	SPIROM_USE_MLB	14 48

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?
USB32PWR_ISO	*	0.5 MM	?
USB32VR_ISO	*	1 MM	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO
USB3	POWER	*	USB32PWR_ISO
USB3	VR_SWITCH	*	USB32VR_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

Constraints Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
J42C USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	44
J42A USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	44
J42B	USB3_PHY	USB3	USB3_EXTA_RX_F_P	13 44
J42D	USB3_PHY	USB3	USB3_EXTA_RX_F_N	13 44
J41A USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	13 44
J41C USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	13 44
J41B	USB3_PHY	USB3	USB3_EXTA_TX_F_P	44
J41D	USB3_PHY	USB3	USB3_EXTA_TX_F_N	44
J49A	USB3_PHY	USB3	USB3_EXTA_TX_C_P	44
J49C	USB3_PHY	USB3	USB3_EXTA_TX_C_N	44
J41E USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_P	13 44
J41D USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_N	13 44
J41C	USB2_PHY	USB2	USB2_EXTA_MUXED_P	44
J42C	USB2_PHY	USB2	USB2_EXTA_MUXED_N	44
J49A	USB2_PHY	USB2	USB2_EXTA_P	44
J49C	USB2_PHY	USB2	USB2_EXTA_N	44
External Port B (J4610)				
J42E USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	44
J42C USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	44
J42F	USB3_PHY	USB3	USB3_EXTB_RX_F_P	13 44
J42H	USB3_PHY	USB3	USB3_EXTB_RX_F_N	13 44
J42G USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	13 44
J42J USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	13 44
J42K	USB3_PHY	USB3	USB3_EXTB_TX_F_P	44
J42M	USB3_PHY	USB3	USB3_EXTB_TX_F_N	44
J49E	USB3_PHY	USB3	USB3_EXTB_TX_C_P	44
J49C	USB3_PHY	USB3	USB3_EXTB_TX_C_N	44
J43C USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_P	13 44
J43D USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_N	13 44
J43A	USB2_PHY	USB2	USB2_EXTB_P	44
J43B	USB2_PHY	USB2	USB2_EXTB_N	44
External Port C (J4700)				
J43F USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	45
J43H USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	45
J43K	USB3_PHY	USB3	USB3_EXTC_RX_F_P	13 45
J44C	USB3_PHY	USB3	USB3_EXTC_RX_F_N	13 45
J44A USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	13 45
J44J USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	13 45
J44E	USB3_PHY	USB3	USB3_EXTC_TX_F_P	45
J44G	USB3_PHY	USB3	USB3_EXTC_TX_F_N	45
J49D	USB3_PHY	USB3	USB3_EXTC_TX_C_P	45
J49F	USB3_PHY	USB3	USB3_EXTC_TX_C_N	45
J44B USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_P	13 45
J44D USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_N	13 45
J45C	USB2_PHY	USB2	USB2_EXTC_P	45
J45D	USB2_PHY	USB2	USB2_EXTC_N	45
External Port D (J4710)				
J45E USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	45
J45G USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	45
J45K	USB3_PHY	USB3	USB3_EXTD_RX_F_P	13 45
J46C	USB3_PHY	USB3	USB3_EXTD_RX_F_N	13 45
J45F USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	13 45
J45H USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	13 45
J46E	USB3_PHY	USB3	USB3_EXTD_TX_F_P	45
J46G	USB3_PHY	USB3	USB3_EXTD_TX_F_N	45
J49B	USB3_PHY	USB3	USB3_EXTD_TX_C_P	45
J49D	USB3_PHY	USB3	USB3_EXTD_TX_C_N	45
J46F USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_P	13 45
J46H USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_N	13 45
J46B	USB2_PHY	USB2	USB2_EXTD_P	45
J46D	USB2_PHY	USB2	USB2_EXTD_N	45
Camera (J3510)				
H4K USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_P	13 40
H5K USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_N	13 40
PCH USB Compensation				
J48E	PCH_55S	COMP_PCH	PCH_USB_RBIAS	13

RMH Love

Electrical Contraint Set	Physical	Spacing		
J49E USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_P	13 34
J41E USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_N	13 34
J50D USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_P	34
J50C USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_N	34

Et tu Brute?

Electrical Contraint Set	Physical	Spacing		
Ethernet				
J47C ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	37 38
J47D ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	37 38
J47G	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	38
J47F	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	38
J51C		ENET_TRANS	ENETCONN_MCT0	38
J52C		ENET_TRANS	ENETCONN_MCT1	38
J52A		ENET_TRANS	ENETCONN_MCT2	38
J52J		ENET_TRANS	ENETCONN_MCT3	38
J52E		ENET_TRANS	ENETCONN_MCT_BS	38
J47C	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	37
SD				
J47A SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0>	37
J48C	SD_PHY	SD	SDCONN_DATA<7..0>	37 39
J51A	SD_PHY	SD	SDCONN_DATA_R <7..0>	
J48E SD_CMD	SD_PHY	SD	ENET_SD_CMD	37
J48D	SD_PHY	SD	SDCONN_CMD	37 39
J51C	SD_PHY	SD	SDCONN_CMD_R	
J48G SD_CLK	SD_PHY	SD	ENET_SD_CLK	37
J48F	SD_PHY	SD	SDCONN_CLK	37 39
J48B	SD_PHY	SD	SDCONN_CLK_R	39
J48H	SD_PHY	SD	ENET_MEDIA_SENSE	11 37
J48H	SD_PHY	SD	ENET_SD_DETECT_L	37 39
CIV SPI				
J49B	CIV_SPI	SPI	ENET_SCLK	37
J48B	CIV_SPI	SPI	ENET_MISO	37
J49J	CIV_SPI	SPI	ENET_MOSI	37
J49H	CIV_SPI	SPI	ENET_CS_L	37

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing		
H59J SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	40
H59K SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	40
H58A SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	40
H58B SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	40
H66F	SPI_50S	SPI	CAM_SF_CLK	40
H66G	SPI_50S	SPI	CAM_SF_CLK_R	40
H66D	SPI_50S	SPI	CAM_SF_DIN	40
H61C	SPI_50S	SPI	CAM_SF_DIN_R	40
H61A	SPI_50S	SPI	CAM_SF_CS_L	40
H61B	SPI_50S	SPI	CAM_SF_WP_L	40
H61E	SPI_50S	SPI	CAM_SF_DOUT	40
H61D	SPI_50S	SPI	CAM_SF_DOUT_R	40
H61F	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	40
H61H	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	40

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
SNS_DIFF_J90	*	Y	0.200 MM	0.100 MM	200 MM	0.150 MM	0.100 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=1.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMC Generic Control Line Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMC_ISO	*	=1:1_SPACING	?
SMC_3xISO	*	=3:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO
SMC_3XCTRL	*	*	SMC_3xISO

SMC Generic Control Line Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMC_GEN	*	SMC_50S

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
I3		SENSE	GND_SMC_AVSS	46 47 50 51
12V S5 (System Total)				
I4 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	50
I5 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	50
I6		SENSE	ISNS_P12VG3H_R	50
I7		SENSE	ISNS_P12VG3H	47 50
I8		SENSE	VSNS_P12VG3H	47 50
12V S0 (GPU Core)				
I22 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_P	50
I23 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_N	50
I24		SENSE	ISNS_P12VS0_GPUC_R	50
I25		SENSE	ISNS_P12VS0_GPUCORE	47 50
I26		SENSE	VSNS_P12VS0_GPUCORE	47 50
I143 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUA_P	50
I144 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUA_N	50
HDD				
I80 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_P	50
I82 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_N	50
I83		SENSE	ISNS_HDDS0_R	50
I85		SENSE	ISNS_HDDS0	47 50
I84		SENSE	VSNS_HDDS0	47 50
I126 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_HDD_P	50
I128 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_HDD_N	50
I127		SENSE	ISNS_12V_HDD_R	50
I129		SENSE	ISNS_P12VS0_HDD	47 50
SSD				
I105 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	51
I107 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	51
I106		SENSE	ISNS_SSDS0_R	51
I108		SENSE	ISNS_SSDS0	47 51
I109		SENSE	VSNS_P3V3S5	47 51
GPU Core (alternate low side sense)				
I110		SENSE	ISNS_GPUCORE_ALT	47 50
I129		SENSE	ISNS_GPUCORE_FB	50
I145		SENSE	ISNS_GPUCORE_FB_R	50
I125		SENSE	VSNS_GPUCORE_ALT	47 50
I146		SENSE	VREG_GPU_IMON_R	50
GPU VDDCI				
I137		SENSE	VSNS_GPU_VDDCI	47 51
GPU AUX				
I141		SENSE	ISNS_P12VS0_GPU_AUX	47 50
I147		SENSE	ISNS_P12VS0_GPUA_R	50
VDDQ S3 (DDR)				
I31 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_P	51
I32 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_N	51
I35		SENSE	ISNS_VDDQS3_DDR_R	51
I24		SENSE	ISNS_VDDQS3_DDR	47 51
I38		SENSE	VSNS_VDDQS3_DDR	47 51
VDDQ S0 (GPU FBVDDQ)				
I37 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_P	50
I38 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_N	50
I39		SENSE	ISNS_P12VS0_FDDQ_R	50
I40		SENSE	ISNS_P12VS0_FBVDDQ	47 50
I142		SENSE	VSNS_P12VS0_FBVDDQ	47 50
CPU Core				
I42		SENSE	R_CPU_IM_R	50
I43		SENSE	ISNS_CPU_FB_R	50
I44		SENSE	ISNS_CPU_FB	50
I45		SENSE	ISNS_CPUVCC	47 50
I46		SENSE	VSNS_CPUVCC	47 50
PP1V05_S0_PCH				
I119		SENSE	VSNS_P1V05S0_PCH	47 50
PP1V5_S0				
I111 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_P	51
I113 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_N	51
I112		SENSE	ISNS_P1V5S0_R	51
I114		SENSE	ISNS_P1V5S0	47 51
I115		SENSE	VSNS_P1V5S0	47 51
Airport				
I101 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_P	50
I103 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_N	50
I104		SENSE	ISNS_P3V3S4_AP_R	50
I100		SENSE	ISNS_P3V3S4_AP	47 50

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
I61	CLK_XTAL	XTAL	SMC_XTAL	46 47
I62	CLK_XTAL	XTAL	SMC_EXTAL	46 47
I91	SMC_GEN	SMC_CTRL	SMC_LRESET_L	20 46
I90	SMC_GEN	SMC_CTRL	SMC_RUNTIME_SCI_L	14 46
I92	SMC_GEN	SMC_CTRL	SMC_WAKE_SCI_L	14 46
I93	SMC_GEN	SMC_CTRL	SMC_FAN_0_CTL	46 53
I94	SMC_GEN	SMC_CTRL	SMC_FAN_0_TACH	46 53
I96	SMC_GEN	SMC_3XCTRL	CPU_PECI	6 14 46 47
I130	SMC_GEN	SMC_3XCTRL	ALL_SYS_PWRGD	3 21 46 73

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
I10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	46 49
I9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	46 49
I11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	46 49
I12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	46 49
I13	SMB_PHY	SMB	SMBUS_SMC_2_S0_SCL	46 49
I14	SMB_PHY	SMB	SMBUS_SMC_2_S0_SDA	46 49
I15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	46 49
I16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	46 49
I19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	46 47
I20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	46 47
GPU				
I135	SMB_PHY	SMB	GFX_SMBDAT_B	49 84
I136	SMB_PHY	SMB	GFX_SMBCLK_B	49 84
PCH				
I21	SMB_PHY	SMB	SMBUS_PCH_CLK	13 49
I22	SMB_PHY	SMB	SMBUS_PCH_DATA	13 49
I53	SMB_PHY	SMB	SML_PCH_0_CLK	13 49
I54	SMB_PHY	SMB	SML_PCH_0_DATA	13 49
Display TCon				
I55	SMB_PHY	SMB	SMB_DP_TCON_SCL	42 49
I56	SMB_PHY	SMB	SMB_DP_TCON_SDA	42 49

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
I65 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	52 62
I66 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	52 62
HDD Out-of-Band				
I117		SENSE	SMC_OOB1_D2R_L	36 46
I118		SENSE	SMC_OOB1_R2D_L	46 47
I116		SENSE	SMC_OOB1_D2R_R	36
SSD Out-of-Band				
I27		SENSE	SMC_OOB2_R2D_L	35 47
I28		SENSE	SMC_OOB2_D2R_L	35 47
GPU PCIE				
I131 SNS_TEMP	SNS_DIFF_PHY	SENSE	GPU_TDIODE_P	84 85
I132 SNS_TEMP	SNS_DIFF_PHY	SENSE	GPU_TDIODE_N	84 85
I140 SNS_TEMP	SNS_DIFF_PHY	SENSE	GFX_THM_DP2	85
I139 SNS_TEMP	SNS_DIFF_PHY	SENSE	GFX_THM_DN3	85
I138 SNS_TEMP	SNS_DIFF_PHY	SENSE	GFX_THM_DP3	85
I137 SNS_TEMP	SNS_DIFF_PHY	SENSE	GFX_THM_DN2	85

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
VR_SENSE	*	Y	0.300 MM	0.200 MM	25 MM	0.400 MM	0.200 MM
POWER_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
GPU_VSEN_PHY	*	Y	0.150 MM	0.100 MM	25 MM	0.400 MM	0.200 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S
VR_SVID_PHY	*	POWER_55S
VR_GPU_VSEN	*	GPU_VSEN_PHY

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?
VR_SVID_ISO	*	=2.6:1_SPACING	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO
VR_SVID	*	*	VR_SVID_ISO

PCH/GPU/TBT 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I1	POWER	POWER	5V			REG_VCC_U7700 68
Local Ground						
I3	GND	GND	0V			AGND_P1V05S0 68
1.05V S0						
I5	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0 68
I4	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L 68
I7	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0 68
I6	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC 68
I8	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0 68
I10	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0 68
I12	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0 68
I11	VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET 68
I14	VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO 68
I72	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_P 17 68
I73	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_N 17 68
I16	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_XW_P 68
I17	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE			SNS_GPU_PEX_IOVDD_XW_N 68
I19			SENSE			REG_P1V05S0_FB 68
I18			SENSE			REG_P1V05S0_RTN 68
I21	VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF 68
I20	VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL 68
Output Bus						
I22	POWER	POWER	1.05V			PP1V05_S0 94
FET Switched						
I66	POWER	POWER	1.05V			PP1V05_TBTCIO 29 33

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I43	POWER	POWER	5V			REG_V5IN_U7300 66
Local Ground						
I44	GND	GND	0V			AGND_VDDQS3 66
I74	GND	GND	0V			PGND_REG_P1V5_S3 66
VDDQ S3						
I45	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3 66
I47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L 66
I46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3 66
I48	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC 66
I49	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3 66
I52	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQS3 66
I51	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3 66
I53	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS 66
I55	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF 66
I56	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN 66
I57	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE 66
I58	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP 66
I59	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS 66
I61	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VTTREF 66
I70	VR_CTL_PHY	VR_CTL				PM_EN_REG_VDDQ_S3 66 72
I71	VR_CTL_PHY	VR_CTL				PM_EN_REG_VDDQ_S3_R 66
I68	VR_CTL_PHY	VR_CTL				PM_EN_LDO_DDRVTT_S0 66 72
I69	VR_CTL_PHY	VR_CTL				PM_EN_LDO_DDR_VTT_S0_R 66
Output Bus						
I60	POWER	POWER	1.5V			PPVDDQ_S3 94
I62	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S0 94
FET Switched						
I63	POWER	POWER	1.5V			PP1V5_S0 94
Sensed						
I64	POWER	POWER	1.5V			PPVDDQ_S3_DDR 94
I67	POWER	POWER	1.5V			PP1V5_S0_PCH 94

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CPU VCC Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H80	POWER	POWER	12V			PP12V_S0_CPUVCC_FLT 63 64 65
H81	POWER	POWER	5V			REG_VCC_U7000 63
Local Ground						
H82	GND	GND	0V			AGND_CPU 63 64 65
Phase 1						
H83	VR_CTL_PHY	VR_CTL				REG_TD_1 64
H84	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1 63 64
H85	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1_R 63
H87	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_1 64
H88	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1 64
H89	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_1_RC 64
H90	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_1 64
H91	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_1 64
H92	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_1 64
H93	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1 64
H94 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_P 63 64
H95 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_N 64
H96		SENSE				REG_ISENVCC_1_NR 63 64
Phase 2						
H113	VR_CTL_PHY	VR_CTL				REG_TD_2 64
H114	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2 63 64
H115	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2_R 63
H117	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_2 64
H118	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2 64
H119	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_2_RC 64
H120	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_2 64
H121	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_2 64
H122	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_2 64
H123	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2 64
H124 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_P 63 64
H125 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_N 64
H126		SENSE				REG_ISENVCC_2_NR 63 64
Phase 3						
H135	VR_CTL_PHY	VR_CTL				REG_TD_3 64
H136	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3 63 64
H138	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3_R 63
H139	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_3 64
H140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_3 64
H141	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_3_RC 64
H142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_3 64
H143	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_3 64
H144	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_3 64
H145	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_3 64
H146 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_P 63 64
H147 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_N 64
H148		SENSE				REG_ISENVCC_3_NR 63 64
Phase 4						
H162	VR_CTL_PHY	VR_CTL				REG_TD_4 65
H163	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_4 63 65
H164	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_4_R 63
H166	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_4 65
H167	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_4 65
H168	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_4_RC 65
H169	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_4 65
H170	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_4 65
H171	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_4 65
H172	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_4 65
H173 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_4_P 63 65
H174 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_4_N 65
H175		SENSE				REG_ISENVCC_4_NR 63 65

CPU VCC Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL6372						
H182	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DVC 63
H183	VR_CTL_PHY	VR_CTL				CPUVCC_DVC_RC
H184	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC_2 63
H185	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP 63
H186	VR_CTL_PHY	VR_CTL				CPUVCC_COMP_RC 63
H187	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB 63
H188	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC 63
H189	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_1 63
H190	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_2 63
H191	VR_CTL_PHY	VR_CTL				CPUVCC_PSICOMP_RC 63
H192	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PSICOMP 63
H193	VR_CTL_PHY	VR_CTL				REG_CPUVCC_HFCOMP 63
H194 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_P 8 63
H195 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_N 9 63
H196	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_P 63
H197	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_N 63
H198 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_VCC_XW_P 63
H199 VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_VCC_XW_N 63
H200		SENSE				REG_CPUVCC_VSEN 63
H201		SENSE				REG_CPUVCC_RGND 63
H202		SENSE				REG_CPUVCC_VIN 63
H203	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMON 50 63
H204	VR_CTL_PHY	VR_CTL				CPUVCC_IMON_R 63
H205	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TM 63
H206	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMX 63
H207	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NPSI 63
H208	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FDVID 63
H209	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TMX 63
H210	VR_CTL_PHY	VR_CTL				REG_CPUVCC_MEMVRSEL 63
H211	VR_CTL_PHY	VR_CTL				REG_CPUVCC_RSET 63
H212 CPU_VIDSCLK	VR_VID_PHY	VR_VID				CPU_VIDSCLK 8 63
H213	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R 8
H214 CPU_VIDALERT_L	VR_VID_PHY	VR_VID				CPU_VIDALERT_L 8 63
H215	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L 8
H216 CPU_VIDSOUT	VR_VID_PHY	VR_VID				CPU_VIDSOUT 8 63
H217	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R 8
Output Bus						
H218	POWER	POWER	1.8V			PPCPUVCC_S0_CPU 94

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3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H843	POWER	POWER	12V			REG_VIN_U7600	67
H125	POWER	POWER	5V			REG_VCC1_U7600	67
H122	POWER	POWER	5V			REG_VCC2_U7600	67
3.3V S5							
H849	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	67
H847	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	67
H851	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC	67
H84D	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	67
H850	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5	67
H852	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	67
H107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	67
H107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	67
H113	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	67
H108	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	67
H107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	67
H107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	67
H150	VR_CTL_PHY	VR_CTL				PM_EN_REG_P3V3_S5	67 72
H150	VR_CTL_PHY	VR_CTL				PM_EN_REG_P3V3_S5_R	67
5V S3							
H113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	67
H113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	67
H113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC	67
H114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	67
H114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4	67
H114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	67
H114	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	67
H114	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	67
H114	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	67
H114	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	67
H114	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	67
H114	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	67
H150	VR_CTL_PHY	VR_CTL				PM_EN_REG_P5V_S4	67 72
H150	VR_CTL_PHY	VR_CTL				PM_EN_REG_P5V_S4_R	67
Output Bus							
H115	POWER	POWER	5V			PP5V_S5	94
H112	POWER	POWER	5V			PP5V_S4	94
H114	POWER	POWER	3.3V			PP3V3_S5	94
H151	POWER	POWER	3.3V			PP3V3_S5_PCH_R	20
FET Switched							
H123	POWER	POWER	5V			PP5V_S0	94
H124	POWER	POWER	3.3V			PP3V3_S4	94
H121	POWER	POWER	3.3V			PP3V3_S0	94
H150	POWER	POWER	3.3V			PP3V3_TBT_PCH_GPIO	20
H121	POWER	POWER	3.3V			PP3V3_ENET	94
H138	POWER	POWER	3.3V			PP3V3_TBTLC	28 29 94
Sensed							
H145	POWER	POWER	3.3V			PPSSD_S0	94
H147	POWER	POWER	3.3V			PP3V3_S4_AP	94

J90 GPU VREG POWER NETS

	Physical	Spacing	Voltage	DIDT	NO_TEST		
H148	POWER	POWER	1.8V			PP1V8_S0_GPU_VDD	94
H148	POWER	POWER	0.95V			PP0V95_S0_GPU_VDDC	94
H148	POWER	POWER	0.85V			PPVDDCI_S0_GPU	94
H149	POWER	POWER	1.8V			PP1V8_TSVDD_FLT	84
H149	POWER	POWER	1.8V			PP1V8_SPLL_PVDD_FLT	84
H149	POWER	POWER	1.8V			PP1V8_AVDD_FLT	
H149	POWER	POWER	1.8V			PP1V8_VDD1DI_FLT	
H149	POWER	POWER	1.8V			PP1V8_XTAL_VDDR_FLT	
H149	POWER	POWER	1.8V			PP1V8_MPLL_PVDD_FLT	84
H149	POWER	POWER	1.8V			PP1V8_DPLL_PVDD_FLT	
H149	POWER	POWER	0.95V			PP0V95_SPLL_VDDC_FLT	
H149	POWER	POWER	0.95V			PP0V95_DPLL_VDDC_FLT	84

3.42V G3H

	Physical	Spacing	Voltage	DIDT	NO_TEST		
3.42V G3H							
H146	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_BOOST	62
H146	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_BOOST_R	
H146	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_SW	62
H146	VR_CTL_PHY	VR_CTL				P3V42G3H_FB	62
H146	VR_CTL_PHY	VR_CTL				P3V42G3H_BIAS	62
H146	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	62
Output Bus							
H146	POWER	POWER	3.425V			PP3V42_G3H	94

3.3V G3

	Physical	Spacing	Voltage	DIDT	NO_TEST		
H147	POWER	POWER	3.3V			PP3V3_G3	94

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
FET Switched							
H150	POWER	POWER	5V			PPHDD_S0	94
Sensed							
H146	POWER	POWER	5V			PP5V_S0_HDD	94

12V

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H146	POWER	POWER	12V			PP12V_ACDC	94
FET Switched							
H146	POWER	POWER	12V			PP12V_S5	94
H145	POWER	POWER	12V			PP12V_S0	94
H148	POWER	POWER	12V			PPHDD12_S0	94
Sensed							
H146	POWER	POWER	12V			PP12V_G3H	94
H147	POWER	POWER	12V			PP12V_G3H_P3V42	62
H148	POWER	POWER	12V			PP12V_S0_GPUCORE	94
H145	POWER	POWER	12V			PP12V_S0_FBVDDQ	94
H147	POWER	POWER	12V			PP12V_S0_HDD	94
H150	POWER	POWER	12V			PP12V_S0_GPU_AUX	94

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Common							
H838	GND	GND	0V			GND	

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

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Platform VReg Constraints

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
TBT_MISC_55S	*	=55_OHM_SE	=55_OHM_SE	0.070 MM	=55_OHM_SE	=STANDARD	=STANDARD

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
TBT2PWR_ISO	*	0.5 MM	?
BGA_TBT_AREA	*	0.075MM	?
TBT_MISC	*	=3:1_SPACING	?
TBT2VR_ISO	*	1 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_TBT	BGA_TBT_AREA
TBTDP	*	*	TBTDP_ISO
TBTDP	POWER	*	TBT2PWR_ISO
TBTDP	VR_SWITCH	*	TBT2VR_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP2DP_ISO	*	=4X_DIELECTRIC	?
DP2DP_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
DP_ISO	*	=5X_DIELECTRIC	?
DP_ISO	TOP,BOTTOM	=7X_DIELECTRIC	?
DP2PWR_ISO	*	0.5 MM	?
DP2VR_ISO	*	1 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	DISPLAYPORT	*	DP2DP_ISO
DISPLAYPORT	POWER	*	DP2PWR_ISO
DISPLAYPORT	VR_SWITCH	*	DP2VR_ISO
DISPLAYPORT	*	*	DP_ISO

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	NO_TEST=TRUE 28 83
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	NO_TEST=TRUE 28 83
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	NO_TEST=TRUE 28
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	NO_TEST=TRUE 28
	TBTDP_90D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	28 83
	TBTDP_90D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	28 83
DP_TBTSNK0_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	28
DP_TBTSNK0_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	28
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	NO_TEST=TRUE 28 83
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	NO_TEST=TRUE 28 83
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	NO_TEST=TRUE 28
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	NO_TEST=TRUE 28
	TBTDP_90D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	28 83
	TBTDP_90D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	28 83
DP_TBTSNK1_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	28
DP_TBTSNK1_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	28
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	NO_TEST=TRUE 43
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	NO_TEST=TRUE 43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	43
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	28
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	28
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	28
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	28
	TBT_MISC_55S	TBT_MISC	DP_TBTSNK0_HPD	28 84
	TBT_MISC_55S	TBT_MISC	DP_TBTSNK1_HPD	28 84
	TBT_MISC_55S	TBT_MISC	DP_TBTSRC_HPD	28 43
	TBT_MISC_55S	TBT_MISC	DP_TBTPA_HPD	28 31
	TBT_MISC_55S	TBT_MISC	DP_TBTPB_HPD	28 32
	TBT_MISC_55S	TBT_MISC	TBT_A_HPD	31
	TBT_MISC_55S	TBT_MISC	TBT_B_HPD	32

*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Contraint Set	Physical	Spacing		
SLAVE NETS - GPU/PANEL				
DP_INTPNL_SL_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_SL_AUX_P	42 83
DP_INTPNL_SL_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_SL_AUX_N	42 83
DP_INTPNL_SL_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_SL_AUX_C_P	42
DP_INTPNL_SL_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_SL_AUX_C_N	42
DP_INTPNL_SL	DP_85D	DISPLAYPORT	DP_INT_EG_SL_P<3..0>	NO_TEST=TRUE 42 83
DP_INTPNL_SL	DP_85D	DISPLAYPORT	DP_INT_EG_SL_N<3..0>	NO_TEST=TRUE 42 83
DP_INTPNL_SL	DP_85D	DISPLAYPORT	DP_INT_EG_SL_C_P<3..0>	NO_TEST=TRUE 42
DP_INTPNL_SL	DP_85D	DISPLAYPORT	DP_INT_EG_SL_C_N<3..0>	NO_TEST=TRUE 42
	TBTDP_90D	DISPLAYPORT	DP_INT_EG_SL_DDC_CLK	83
	TBTDP_90D	DISPLAYPORT	DP_INT_EG_SL_DDC_DAT	83
MASTER NETS - GPU-MUX				
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	NO_TEST=TRUE 43 83
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	NO_TEST=TRUE 43 83
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_ML_AUX_P	43 83
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_ML_AUX_N	43 83
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_ML_AUX_C_P	43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INT_EG_ML_AUX_C_N	43
	TBTDP_90D	DISPLAYPORT	DP_INT_EG_ML_DDC_CLK	83
	TBTDP_90D	DISPLAYPORT	DP_INT_EG_ML_DDC_DAT	83
MASTER NETS - MUX-PANEL				
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	NO_TEST=TRUE 43
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	NO_TEST=TRUE 43
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	NO_TEST=TRUE 42 43
DP_INTPNL_ML	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	NO_TEST=TRUE 42 43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INTPNL_ML_AUX_P	43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INTPNL_ML_AUX_N	43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INTPNL_ML_AUX_C_P	42 43
DP_INTPNL_ML_AUX	TBTDP_90D	DISPLAYPORT	DP_INTPNL_ML_AUX_C_N	42 43
INTERNAL DP AUDIO				
		HDA	AUDIO_SCLK	42 96
		HDA	AUDIO_WS	42 96
		HDA	DP_INT_SPDIF_AUDIO	42 54
		HDA	AUDIO_MUTE_L	42 96

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	NO_TEST=TRUE 28 31
TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	NO_TEST=TRUE 28 31
TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	NO_TEST=TRUE 28 31
TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	NO_TEST=TRUE 28 31
	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	NO_TEST=TRUE 31
	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	NO_TEST=TRUE 31
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	NO_TEST=TRUE 28 31
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	NO_TEST=TRUE 28 31
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	NO_TEST=TRUE 28 31
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	NO_TEST=TRUE 28 31
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	NO_TEST=TRUE 31
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	NO_TEST=TRUE 31
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	NO_TEST=TRUE 31
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	NO_TEST=TRUE 31
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	NO_TEST=TRUE 31
	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	NO_TEST=TRUE 31
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	NO_TEST=TRUE 28 31
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	NO_TEST=TRUE 28 31
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	NO_TEST=TRUE 28 31
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	NO_TEST=TRUE 28 31
TBT_A_D2R1	TBTDP_90D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	28 31
TBT_A_D2R1	TBTDP_90D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	28 31
	TBTDP_90D	DISPLAYPORT	DP_TBTPA_AUXCH_P	31
	TBTDP_90D	DISPLAYPORT	DP_TBTPA_AUXCH_N	31
DP_A_AUXCH_DDC	TBTDP_90D	DISPLAYPORT	DP_A_AUXCH_DDC_P	
DP_A_AUXCH_DDC	TBTDP_90D	DISPLAYPORT	DP_A_AUXCH_DDC_N	
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	31
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	31
TBTPA_DDC_I2C	TBTDP_90D	TBT_I2C	DP_TBTPA_DDC_CLK	31 33
TBTPA_DDC_I2C	TBTDP_90D	TBT_I2C	DP_TBTPA_DDC_DATA	31 33
Port B				
TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	NO_TEST=TRUE 28 32
TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	NO_TEST=TRUE 28 32
TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	NO_TEST=TRUE 28 32
TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	NO_TEST=TRUE 28 32
	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	NO_TEST=TRUE 32
	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	NO_TEST=TRUE 32
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	NO_TEST=TRUE 28 32
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	NO_TEST=TRUE 28 32
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	NO_TEST=TRUE 28 32
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	NO_TEST=TRUE 28 32
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	NO_TEST=TRUE 32
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	NO_TEST=TRUE 32
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	NO_TEST=TRUE 32
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	NO_TEST=TRUE 32
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	NO_TEST=TRUE 32
	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	NO_TEST=TRUE 32
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	NO_TEST=TRUE 28 32
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	NO_TEST=TRUE 28 32
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	NO_TEST=TRUE 28 32
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	NO_TEST=TRUE 28 32
TBT_B_D2R1	TBTDP_90D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	28 32
TBT_B_D2R1	TBTDP_90D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	28 32
	TBTDP_90D	DISPLAYPORT	DP_TBTPB_AUXCH_P	32
	TBTDP_90D	DISPLAYPORT	DP_TBTPB_AUXCH_N	32
DP_B_AUXCH_DDC	TBTDP_90D	DISPLAYPORT	DP_B_AUXCH_DDC_P	
DP_B_AUXCH_DDC	TBTDP_90D	DISPLAYPORT	DP_B_AUXCH_DDC_N	
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	32
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	32
TBTPB_DDC_I2C	TBTDP_90D	TBT_I2C	DP_TBTPB_DDC_CLK	32 33
TBTPB_DDC_I2C	TBTDP_90D	TBT_I2C	DP_TBTPB_DDC_DATA	32 33

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	100 MM	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	100 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
GDDR_BGA7MM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	7 MM	=STANDARD	=STANDARD
GDDR_BGA5MM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	5 MM	=STANDARD	=STANDARD
GDDR_BGA4MM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	4.9 MM	=STANDARD	=STANDARD
GDDR_BGA5MM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	4.9 MM	=80_OHM_DIFF	=80_OHM_DIFF
GDDR_BGA3MM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	3 MM	=STANDARD	=STANDARD
GDDR_BGA4MM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	4 MM	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	BGA	GDDR_BGA7MM_45S
GDDR_ADBI_PHY	BGA	GDDR_BGA4MM_45S
GDDR_CTRL_PHY	BGA	GDDR_BGA7MM_45S
GDDR_CLK_PHY	BGA	GDDR_BGA5MM_80D
GDDR_DQ_PHY	BGA	GDDR_BGA7MM_45S
GDDR_EDC_PHY	BGA	GDDR_BGA4MM_45S
GDDR_DBI_PHY	BGA	GDDR_BGA4MM_45S
GDDR_WCK_PHY	BGA	GDDR_BGA5MM_80D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	BGA_VRAM	GDDR_BGA3MM_45S
GDDR_ADBI_PHY	BGA_VRAM	GDDR_BGA3MM_45S
GDDR_CTRL_PHY	BGA_VRAM	GDDR_BGA3MM_45S
GDDR_CLK_PHY	BGA_VRAM	GDDR_BGA4MM_80D
GDDR_WCK_PHY	BGA_VRAM	GDDR_BGA4MM_80D

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=5X_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=7X_DIELECTRIC	?
GDDR_MA2MA	*	=3X_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=5X_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=7X_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=3X_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_CLK2CLK	*	=5X_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3X_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_EDC_ISO	*	=7X_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=10X_DIELECTRIC	?
GDDR_EDC2EDC	*	=7X_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=10X_DIELECTRIC	?
GDDR_DBI2DBI	*	=5X_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=7X_DIELECTRIC	?
GDDR_WCK2WCK	*	=5X_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=7X_DIELECTRIC	?
GDDR_BGA_ISO	*	=1.3X_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*	*	BGA	GDDR_BGA_ISO
GDDR_*	*	BGA_VRAM	GDDR_BGA_ISO

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_GPU_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing		
Memory Address				
GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	NO_TEST=TRUE 77 79
GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	NO_TEST=TRUE 77 79
Address Dynamic Bus Inv				
GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	NO_TEST=TRUE 77 79
GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	NO_TEST=TRUE 77 79
Control				
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	NO_TEST=TRUE 77 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	NO_TEST=TRUE 77 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	NO_TEST=TRUE 77 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	NO_TEST=TRUE 77 79
GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	NO_TEST=TRUE 77 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	NO_TEST=TRUE 77 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	NO_TEST=TRUE 77 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	NO_TEST=TRUE 77 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	NO_TEST=TRUE 77 79
GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	NO_TEST=TRUE 77 79
Clock				
GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	NO_TEST=TRUE 77 79
GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	NO_TEST=TRUE 77 79
GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	NO_TEST=TRUE 77 79
GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	NO_TEST=TRUE 77 79
Data				
GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	NO_TEST=TRUE 77 79
GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	NO_TEST=TRUE 77 79
GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	NO_TEST=TRUE 77 79
GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	NO_TEST=TRUE 77 79
GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	NO_TEST=TRUE 77 79
GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	NO_TEST=TRUE 77 79
GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	NO_TEST=TRUE 77 79
GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	NO_TEST=TRUE 77 79
Error Detection				
GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	NO_TEST=TRUE 77 79
GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	NO_TEST=TRUE 77 79
GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	NO_TEST=TRUE 77 79
GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	NO_TEST=TRUE 77 79
GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	NO_TEST=TRUE 77 79
GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	NO_TEST=TRUE 77 79
GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	NO_TEST=TRUE 77 79
GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	NO_TEST=TRUE 77 79
Data Dynamic Bus Inv				
GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	NO_TEST=TRUE 77 79
GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	NO_TEST=TRUE 77 79
GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	NO_TEST=TRUE 77 79
GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	NO_TEST=TRUE 77 79
GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	NO_TEST=TRUE 77 79
GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	NO_TEST=TRUE 77 79
GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	NO_TEST=TRUE 77 79
GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	NO_TEST=TRUE 77 79
Forwarded Clock				
GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	NO_TEST=TRUE 77 79
GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	NO_TEST=TRUE 77 79
GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	NO_TEST=TRUE 77 79
GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	NO_TEST=TRUE 77 79
GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	NO_TEST=TRUE 77 79
GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	NO_TEST=TRUE 77 79
GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	NO_TEST=TRUE 77 79
GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	NO_TEST=TRUE 77 79

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing		
Memory Address				
GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	NO_TEST=TRUE 77 80
GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	NO_TEST=TRUE 77 80
Address Dynamic Bus Inv				
GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	NO_TEST=TRUE 77 80
GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	NO_TEST=TRUE 77 80
Control				
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	NO_TEST=TRUE 77 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	NO_TEST=TRUE 77 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	NO_TEST=TRUE 77 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	NO_TEST=TRUE 77 80
GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	NO_TEST=TRUE 77 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	NO_TEST=TRUE 77 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	NO_TEST=TRUE 77 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	NO_TEST=TRUE 77 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	NO_TEST=TRUE 77 80
GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	NO_TEST=TRUE 77 80
Clock				
GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	NO_TEST=TRUE 77 80
GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	NO_TEST=TRUE 77 80
GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	NO_TEST=TRUE 77 80
GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	NO_TEST=TRUE 77 80
Data				
GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	NO_TEST=TRUE 77 80
GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	NO_TEST=TRUE 77 80
GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	NO_TEST=TRUE 77 80
GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	NO_TEST=TRUE 77 80
GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	NO_TEST=TRUE 77 80
GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	NO_TEST=TRUE 77 80
GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	NO_TEST=TRUE 77 80
GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	NO_TEST=TRUE 77 80
Error Detection				
GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	NO_TEST=TRUE 77 80
GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	NO_TEST=TRUE 77 80
GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	NO_TEST=TRUE 77 80
GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	NO_TEST=TRUE 77 80
GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	NO_TEST=TRUE 77 80
GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	NO_TEST=TRUE 77 80
GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	NO_TEST=TRUE 77 80
GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	NO_TEST=TRUE 77 80
Data Dynamic Bus Inv				
GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	NO_TEST=TRUE 77 80
GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	NO_TEST=TRUE 77 80
GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	NO_TEST=TRUE 77 80
GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	NO_TEST=TRUE 77 80
GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	NO_TEST=TRUE 77 80
GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	NO_TEST=TRUE 77 80
GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	NO_TEST=TRUE 77 80
GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	NO_TEST=TRUE 77 80
Forwarded Clock				
GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	NO_TEST=TRUE 77 80
GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	NO_TEST=TRUE 77 80
GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	NO_TEST=TRUE 77 80
GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	NO_TEST=TRUE 77 80
GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	NO_TEST=TRUE 77 80
GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	NO_TEST=TRUE 77 80
GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	NO_TEST=TRUE 77 80
GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	NO_TEST=TRUE 77 80

GPU

Electrical Contraint Set	Physical	Spacing		
Clocks				
	CLK_GPU_55S	CLK_GPU	TEST_GFX_JTAG_TCK	
	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_IN	84
	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_OUT	84
	CLK_GPU_55S	CLK_GPU	GFX_XTAL_IN_27M	84
	CLK_GPU_55S	CLK_GPU	GFX_XTAL_OUT_27M	84
SMB				
	SMB_PHY	SMB	GPU_SMB_CLK	85
	SMB_PHY	SMB	GPU_SMB_DAT	85
PCIe Compensation				
	PCIE_50S	COMP_PCIE	PCIE_CALR_RX	
	PCIE_50S	COMP_PCIE	PCIE_CALR_TX	
MISC				
	XDP_PHY	XDP	TEST_GFX_JTAG_TDO	
	XDP_PHY	XDP	TEST_GFX_JTAG_TDI	
	XDP_PHY	XDP	TEST_GFX_JTAG_TMS	
	XDP_PHY	XDP	TEST_GFX_JTAG_TRST_L	

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing		
Reset				
GDDR_AB_RESET	GDDR_50S	GDDR_CTRL	FB_AB_RST_RR	77
GDDR_AB_RESET	GDDR_50S	GDDR_CTRL	FB_AB_RST_R	77
GDDR_AB_RESET	GDDR_50S	GDDR_CTRL	FB_AB_RESET_L	77 79 80
GDDR_CD_RESET	GDDR_50S	GDDR_CTRL	FB_CD_RST_RR	78
GDDR_CD_RESET	GDDR_50S	GDDR_CTRL	FB_CD_RST_R	78
GDDR_CD_RESET	GDDR_50S	GDDR_CTRL	FB_CD_RESET_L	78 81 82

SYNC_MASTER=J78_MLB SYNC_DATE=02/21/2014

PAGE TITLE: GDDR5/GPU Constraints

Apple Inc.

DRAWING NUMBER: 051-1635 SIZE: D

REVISION: 5.0.0

BRANCH: proto2

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GDDR5 FRAME BUFFER C

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1642 GDDR_C0_MA	GDDR_MA_PHY	GDDR_C_0_MA	FB_C0_A<8..0>	NO_TEST=TRUE	78 81
1643 GDDR_C1_MA	GDDR_MA_PHY	GDDR_C_1_MA	FB_C1_A<8..0>	NO_TEST=TRUE	78 81
Address Dynamic Bus Inv					
1644 GDDR_C0_ADBI	GDDR_ADBI_PHY	GDDR_C_0_ADBI	FB_C0_ABI_L	NO_TEST=TRUE	78 81
1645 GDDR_C1_ADBI	GDDR_ADBI_PHY	GDDR_C_1_ADBI	FB_C1_ABI_L	NO_TEST=TRUE	78 81
Control					
1647 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CKE_L	NO_TEST=TRUE	78 81
1648 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CS_L	NO_TEST=TRUE	78 81
1649 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_WE_L	NO_TEST=TRUE	78 81
1650 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CAS_L	NO_TEST=TRUE	78 81
1651 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_RAS_L	NO_TEST=TRUE	78 81
1652 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CKE_L	NO_TEST=TRUE	78 81
1653 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CS_L	NO_TEST=TRUE	78 81
1654 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_WE_L	NO_TEST=TRUE	78 81
1655 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CAS_L	NO_TEST=TRUE	78 81
1656 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_RAS_L	NO_TEST=TRUE	78 81
Clock					
1657 GDDR_C0_CLK	GDDR_CLK_PHY	GDDR_C_0_CLK	FB_C0_CLK_P	NO_TEST=TRUE	78 81
1658 GDDR_C0_CLK	GDDR_CLK_PHY	GDDR_C_0_CLK	FB_C0_CLK_N	NO_TEST=TRUE	78 81
1659 GDDR_C1_CLK	GDDR_CLK_PHY	GDDR_C_1_CLK	FB_C1_CLK_P	NO_TEST=TRUE	78 81
1660 GDDR_C1_CLK	GDDR_CLK_PHY	GDDR_C_1_CLK	FB_C1_CLK_N	NO_TEST=TRUE	78 81
Data					
1661 GDDR_C0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<7..0>	NO_TEST=TRUE	78 81
1662 GDDR_C0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<15..8>	NO_TEST=TRUE	78 81
1663 GDDR_C0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<23..16>	NO_TEST=TRUE	78 81
1664 GDDR_C0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<31..24>	NO_TEST=TRUE	78 81
1665 GDDR_C1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<7..0>	NO_TEST=TRUE	78 81
1666 GDDR_C1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<15..8>	NO_TEST=TRUE	78 81
1667 GDDR_C1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<23..16>	NO_TEST=TRUE	78 81
1668 GDDR_C1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<31..24>	NO_TEST=TRUE	78 81
Error Detection					
1674 GDDR_C0_EDC0	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<0>	NO_TEST=TRUE	78 81
1675 GDDR_C0_EDC1	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<1>	NO_TEST=TRUE	78 81
1676 GDDR_C0_EDC2	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<2>	NO_TEST=TRUE	78 81
1677 GDDR_C0_EDC3	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<3>	NO_TEST=TRUE	78 81
1670 GDDR_C1_EDC0	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<0>	NO_TEST=TRUE	78 81
1671 GDDR_C1_EDC1	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<1>	NO_TEST=TRUE	78 81
1672 GDDR_C1_EDC2	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<2>	NO_TEST=TRUE	78 81
1673 GDDR_C1_EDC3	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<3>	NO_TEST=TRUE	78 81
Data Dynamic Bus Inv					
1669 GDDR_C0_DBI0	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<0>	NO_TEST=TRUE	78 81
1678 GDDR_C0_DBI1	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<1>	NO_TEST=TRUE	78 81
1679 GDDR_C0_DBI2	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<2>	NO_TEST=TRUE	78 81
1680 GDDR_C0_DBI3	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<3>	NO_TEST=TRUE	78 81
1681 GDDR_C1_DBI0	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<0>	NO_TEST=TRUE	78 81
1682 GDDR_C1_DBI1	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<1>	NO_TEST=TRUE	78 81
1683 GDDR_C1_DBI2	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<2>	NO_TEST=TRUE	78 81
1684 GDDR_C1_DBI3	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<3>	NO_TEST=TRUE	78 81
Forwarded Clock					
1685 GDDR_C0_WCK0	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_P<0>	NO_TEST=TRUE	78 81
1686 GDDR_C0_WCK0	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_N<0>	NO_TEST=TRUE	78 81
1687 GDDR_C0_WCK1	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_P<1>	NO_TEST=TRUE	78 81
1688 GDDR_C0_WCK1	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_N<1>	NO_TEST=TRUE	78 81
1689 GDDR_C1_WCK0	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_P<0>	NO_TEST=TRUE	78 81
1690 GDDR_C1_WCK0	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_N<0>	NO_TEST=TRUE	78 81
1691 GDDR_C1_WCK1	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_P<1>	NO_TEST=TRUE	78 81
1692 GDDR_C1_WCK1	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_N<1>	NO_TEST=TRUE	78 81

GDDR5 FRAME BUFFER D

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1693 GDDR_D0_MA	GDDR_MA_PHY	GDDR_D_0_MA	FB_D0_A<8..0>	NO_TEST=TRUE	78 82
1694 GDDR_D1_MA	GDDR_MA_PHY	GDDR_D_1_MA	FB_D1_A<8..0>	NO_TEST=TRUE	78 82
Address Dynamic Bus Inv					
1695 GDDR_D0_ADBI	GDDR_ADBI_PHY	GDDR_D_0_ADBI	FB_D0_ABI_L	NO_TEST=TRUE	78 82
1697 GDDR_D1_ADBI	GDDR_ADBI_PHY	GDDR_D_1_ADBI	FB_D1_ABI_L	NO_TEST=TRUE	78 82
Control					
1698 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CKE_L	NO_TEST=TRUE	78 82
1699 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CS_L	NO_TEST=TRUE	78 82
1700 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_WE_L	NO_TEST=TRUE	78 82
1702 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CAS_L	NO_TEST=TRUE	78 82
1703 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_RAS_L	NO_TEST=TRUE	78 82
1704 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CKE_L	NO_TEST=TRUE	78 82
1705 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CS_L	NO_TEST=TRUE	78 82
1706 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_WE_L	NO_TEST=TRUE	78 82
1707 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CAS_L	NO_TEST=TRUE	78 82
1708 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_RAS_L	NO_TEST=TRUE	78 82
Clock					
1709 GDDR_D0_CLK	GDDR_CLK_PHY	GDDR_D_0_CLK	FB_D0_CLK_P	NO_TEST=TRUE	78 82
1710 GDDR_D0_CLK	GDDR_CLK_PHY	GDDR_D_0_CLK	FB_D0_CLK_N	NO_TEST=TRUE	78 82
1712 GDDR_D1_CLK	GDDR_CLK_PHY	GDDR_D_1_CLK	FB_D1_CLK_P	NO_TEST=TRUE	78 82
1713 GDDR_D1_CLK	GDDR_CLK_PHY	GDDR_D_1_CLK	FB_D1_CLK_N	NO_TEST=TRUE	78 82
Data					
1714 GDDR_D0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<7..0>	NO_TEST=TRUE	78 82
1715 GDDR_D0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<15..8>	NO_TEST=TRUE	78 82
1716 GDDR_D0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<23..16>	NO_TEST=TRUE	78 82
1717 GDDR_D0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<31..24>	NO_TEST=TRUE	78 82
1718 GDDR_D1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<7..0>	NO_TEST=TRUE	78 82
1719 GDDR_D1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<15..8>	NO_TEST=TRUE	78 82
1720 GDDR_D1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<23..16>	NO_TEST=TRUE	78 82
1721 GDDR_D1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<31..24>	NO_TEST=TRUE	78 82
Error Detection					
1726 GDDR_D0_EDC0	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<0>	NO_TEST=TRUE	78 82
1727 GDDR_D0_EDC1	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<1>	NO_TEST=TRUE	78 82
1728 GDDR_D0_EDC2	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<2>	NO_TEST=TRUE	78 82
1729 GDDR_D0_EDC3	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<3>	NO_TEST=TRUE	78 82
1722 GDDR_D1_EDC0	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<0>	NO_TEST=TRUE	78 82
1723 GDDR_D1_EDC1	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<1>	NO_TEST=TRUE	78 82
1724 GDDR_D1_EDC2	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<2>	NO_TEST=TRUE	78 82
1725 GDDR_D1_EDC3	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<3>	NO_TEST=TRUE	78 82
Data Dynamic Bus Inv					
1730 GDDR_D0_DBI0	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<0>	NO_TEST=TRUE	78 82
1731 GDDR_D0_DBI1	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<1>	NO_TEST=TRUE	78 82
1732 GDDR_D0_DBI2	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<2>	NO_TEST=TRUE	78 82
1733 GDDR_D0_DBI3	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<3>	NO_TEST=TRUE	78 82
1734 GDDR_D1_DBI0	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<0>	NO_TEST=TRUE	78 82
1735 GDDR_D1_DBI1	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<1>	NO_TEST=TRUE	78 82
1736 GDDR_D1_DBI2	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<2>	NO_TEST=TRUE	78 82
1737 GDDR_D1_DBI3	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<3>	NO_TEST=TRUE	78 82
Forwarded Clock					
1738 GDDR_D0_WCK0	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_P<0>	NO_TEST=TRUE	78 82
1739 GDDR_D0_WCK0	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_N<0>	NO_TEST=TRUE	78 82
1740 GDDR_D0_WCK1	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_P<1>	NO_TEST=TRUE	78 82
1741 GDDR_D0_WCK1	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_N<1>	NO_TEST=TRUE	78 82
1742 GDDR_D1_WCK0	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_P<0>	NO_TEST=TRUE	78 82
1743 GDDR_D1_WCK0	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_N<0>	NO_TEST=TRUE	78 82
1744 GDDR_D1_WCK1	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_P<1>	NO_TEST=TRUE	78 82
1745 GDDR_D1_WCK1	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_N<1>	NO_TEST=TRUE	78 82

SYNC_MASTER=J78 MLB SYNC_DATE=02/21/2014

PAGE TITLE
GDDR5 FB C/D CONSTRAINTS

Apple Inc.

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
BLC_DIFFPAIR	*	Y	0.2 MM	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM
BLC_MISC_PHY	*	BLC_55S
BLC_SNS_DIFF	*	BLC_DIFFPAIR

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45 MM	2000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	3000
PHASE_SW2SW	*	=1:1_SPACING	1000
PHASE_SW2GND	*	=2:1_SPACING	1000

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel’oh or sel’oh? Neither! It’s SIT’arrr

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I680	POWER	POWER	12V			PP12V_BKLT_SNS	69
I745	POWER	POWER	12V			PP12V_BKLT_FUSED	69
I750	POWER	POWER	12V			PP12V_S0_BKLT_FILT	69
I777	POWER	POWER	12V			PP12V_S0_BKLT_PWR	69 70
I778	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R	69
I779	POWER	POWER	5V			PP5V_S0_BKLT_VDDA	69
I781	POWER	POWER	5V			PP5V_S0_BKLT_VDDD	69
I748	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO	69
Local Ground							
I824	GND	GND	0V			BKLT_GNDA	69
I825	GND	GND	0V			BKLT_GNDD	69
I830	GND	GND	0V			BKLT_GND_BST_GD	69
Backlight							
I752	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE	69
I753	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_SNUBBER	69
I780	POWER_BLC_RET	BLC_HV				LED_RETURN_1_FB	69 70
I788	POWER_BLC_RET	BLC_HV				LED_RETURN_2_FB	69 70
I750	POWER_BLC_RET	BLC_HV				LED_RETURN_3_FB	69 70
I797	POWER_BLC_RET	BLC_HV				LED_RETURN_4_FB	69 70
I792	POWER_BLC_RET	BLC_HV				LED_RETURN_5_FB	69 70
I793	POWER_BLC_RET	BLC_HV				LED_RETURN_6_FB	69 70
I816	POWER_BLC_RET	BLC_HV				LED_RETURN_7_FB	69 70
I811	POWER_BLC_RET	BLC_HV				LED_RETURN_8_FB	69 70
I812	POWER_BLC_RET	BLC_HV				LED_RETURN_9_FB	69 70
I785	POWER_BLC_RET	BLC_HV				LED_RETURN_1	70
I787	POWER_BLC_RET	BLC_HV				LED_RETURN_2	70
I795	POWER_BLC_RET	BLC_HV				LED_RETURN_3	70
I786	POWER_BLC_RET	BLC_HV				LED_RETURN_4	70
I796	POWER_BLC_RET	BLC_HV				LED_RETURN_5	70
I787	POWER_BLC_RET	BLC_HV				LED_RETURN_6	70
I800	POWER_BLC_RET	BLC_HV				LED_RETURN_7	70
I807	POWER_BLC_RET	BLC_HV				LED_RETURN_8	70
I808	POWER_BLC_RET	BLC_HV				LED_RETURN_9	70
Output Bus							
I770	POWER_BLC	BLC_HV	67V			BKLT_BOOST	69 70
I772	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1	70
I774	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2	70

Backlight Current Sense

Electrical Contraint Set	Physical	Spacing		
I837	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD1 69 70
I838	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN1_Q 69 70
I839	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD2 69 70
I840	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN2_Q 69 70
I841	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD3 69 70
I842	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN3_Q 69 70
I843	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD4 69 70
I837	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN4_Q 69 70
I837	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD5 69 70
I838	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN5_Q 69 70
I839	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD6 69 70
I840	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN6_Q 69 70
I841	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD7 69 70
I842	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN7_Q 69 70
I843	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD8 69 70
I844	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN8_Q 69 70
I844	BACKLIGHT_GD	BLC_SNS_DIFF	SENSE	BKLT_GD9 69 70
I845	BACKLIGHT_ISEN	BLC_SNS_DIFF	SENSE	BKLT_ISEN9_Q 69 70
I805		SNS_DIFF_PHY	SENSE	BKLT_SNSP 69
I849		SNS_DIFF_PHY	SENSE	BKLT_SNSN 69
I806		SNS_DIFF_PHY	SENSE	BKLT_SNSP_R 69
I805		SNS_DIFF_PHY	SENSE	BKLT_SNSN_R 69

Cello Miscellaneous

Electrical Contraint Set	Physical	Spacing		
SPI				
I664	SMB_PHY	SMB	BKLT_SCL	
I665	SMB_PHY	SMB	BKLT_SDA	
I834	SMB_PHY	SMB	I2C_DBG_BKLT_SDA_R	
I835	SMB_PHY	SMB	I2C_DBG_BKLT_SCL_R	
CONTROL				
I814	BLC_MISC_PHY	BLC_CTL	BLC_LSYNC	42 69
I819	BLC_MISC_PHY	BLC_CTL	BLC_LSYNC_R	69
I826	BLC_MISC_PHY	BLC_CTL	BLC_VSYNC	42 69
I828	BLC_MISC_PHY	BLC_CTL	BLC_VSYNC_R	69
I817	BLC_MISC_PHY	BLC_CTL	TCON_BLC_EN	42 69
I818	BLC_MISC_PHY	BLC_CTL	TCON_BLC_EN_R	
I827	BLC_MISC_PHY	BLC_CTL	TCON_BLC_EN_LED	3 42
I820	BLC_MISC_PHY	BLC_CTL	BLC_EN	42
I824	BLC_MISC_PHY	BLC_CTL	DP_INTPNL_ML_HPD	42 43 69
I829	BLC_MISC_PHY	BLC_CTL	DP_INTPNL_ML_HPD_R	69
I824	BLC_MISC_PHY	BLC_CTL	DP_INT_EG_SL_HPD	42 84
I825	BLC_MISC_PHY	BLC_CTL	DP_INT_EG_ML_HPD	43 84

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PAGE TITLE: BLC Constraints

Apple Inc.

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GPU CORE PHASES

	Electrical Contraint Set Input Bus	Physical	Spacing	Voltage	DIDT	NO_TEST	
H80		POWER	POWER	12V			PP12V_S0_GPUCORE_FLT 87 88 89
H77		POWER	POWER	5V			PP5V_S0_GPUCORE_VCC
	Local Ground						
H150		GND	GND	0V			AGND_GPU
H149		POWER	POWER	1V			PPGPUCORE_S0_SENSE_1
H148		POWER	POWER	1V			PPGPUCORE_S0_SENSE_2 88
H146		POWER	POWER	1V			PPGPUCORE_S0_SENSE_3 88
H145		POWER	POWER	1V			PPGPUCORE_S0_SENSE_4 88
H143		POWER	POWER	1V			PPGPUCORE_S0_SENSE_5 89
H142		POWER	POWER	1V			PPGPUCORE_S0_SENSE_6 89
H139		VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_1 87 88
H140		VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_2 87 88
H138		VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_3 87 88
H137		VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_4 87 89
H135		VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_5 87 89
H134		VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_6 87 89
H133		VR_CTL_PHY	VR_CTL				VCR_TD_1
H132		VR_CTL_PHY	VR_CTL				VCR_TD_2
H131		VR_CTL_PHY	VR_CTL				VCR_TD_3
H130		VR_CTL_PHY	VR_CTL				VCR_TD_4
H129		VR_CTL_PHY	VR_CTL				VCR_TD_5
H128		VR_CTL_PHY	VR_CTL				VCR_TD_6
H127		VR_CTL_PHY	VR_CTL				VR_GPU_PWM1_R
H126		VR_CTL_PHY	VR_CTL				VR_GPU_PWM2_R
H125		VR_CTL_PHY	VR_CTL				VR_GPU_PWM3_R
H124		VR_CTL_PHY	VR_CTL				VR_GPU_PWM4_R
H123		VR_CTL_PHY	VR_CTL				VR_GPU_PWM5_R
H122		VR_CTL_PHY	VR_CTL				VR_GPU_PWM6_R
H121		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_1 88
H120		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_2 88
H119		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_3 88
H118		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_4 89
H117		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_5 89
H116		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_6 89
H115		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1
H114		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2
H113		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_3
H112		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_4
H111		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_5
H110		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_6
H109		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1
H108		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC
H107		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2
H106		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC
H105		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3
H104		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3_RC
H103		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4
H102		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4_RC
H101		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_5
H100		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_5_RC
H99		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_6
H98		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_6_RC
H97		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_1
H96		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_2
H95		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_3
H94		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_4
H93		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_5
H92		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_6
H91		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1
H90		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2
H89		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_3
H88		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_4
H87		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_5
H86		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_6
H85		VR_CTL_PHY	VR_SWITCH	12V	TRUE		VR_PHASE_GPUCORE_1 88
H84		VR_CTL_PHY	VR_SWITCH	12V	TRUE		VR_PHASE_GPUCORE_2 88
H83		VR_CTL_PHY	VR_SWITCH	12V	TRUE		VR_PHASE_GPUCORE_3 88
H82		VR_CTL_PHY	VR_SWITCH	12V	TRUE		VR_PHASE_GPUCORE_4 89
H81		VR_CTL_PHY	VR_SWITCH	12V	TRUE		VR_PHASE_GPUCORE_5 89
H79		VR_CTL_PHY	VR_SWITCH	12V	TRUE		VR_PHASE_GPUCORE_6 89
H157	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_1_N 87 88
H156	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_1_P 87 88
H155	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_2_N 87 88
H154	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_2_P 87 88
H153	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_3_N 87 88
H152	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_3_P 87 88
H151	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_4_N 87 89
H150	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_4_P 87 89
H149	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_5_N 87 89
H148	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_5_P 87 89
H147	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_6_N 87 89
H146	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_6_P 87 89
H145	ISNS_GPU_CORE		SENSE				VR_GPU_ISNS1_RR_2
H144	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_N
H143	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_P
H142	ISNS_GPU_CORE		SENSE				VR_GPU_ISNS2_RR_2
H141	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_N
H140	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_P
H139	ISNS_GPU_CORE		SENSE				VR_GPU_ISNS3_RR_2
H138	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_N
H137	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_P
H136	ISNS_GPU_CORE		SENSE				VR_GPU_ISNS4_RR_2
H135	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_N
H134	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_P
H133	ISNS_GPU_CORE		SENSE				VR_GPU_ISNS5_RR_2
H132	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS5_R_N
H131	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS5_R_P
H130	ISNS_GPU_CORE		SENSE				VR_GPU_ISNS6_RR_2
H129	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS6_R_N
H128	ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS6_R_P

GPU CORE CONTROLLER

	Electrical Contraint Set IR3566BM	Physical	Spacing	Voltage	DIDT	NO_TEST	
H153		VR_CTL_PHY	VR_CTL				VRG_VDF_R1
H152		VR_CTL_PHY	VR_CTL				VRG_VDF_R2
H151		VR_CTL_PHY	VR_CTL				VR_GPU_COMP
H150		VR_CTL_PHY	VR_CTL				VR_GPU_COMP_R
H149		VR_CTL_PHY	VR_CTL				VR_GPU_COMP_RC
H148		VR_CTL_PHY	VR_CTL				VR_GPU_DAC
H147		VR_CTL_PHY	VR_CTL				VR_GPU_FAN
H146		VR_CTL_PHY	VR_CTL				VR_GPU_FB
H145		VR_CTL_PHY	VR_CTL				VR_GPU_FB_R
H144		VR_CTL_PHY	VR_CTL				VR_GPU_FS
H143		VR_CTL_PHY	VR_CTL				VR_GPU_IMON 50 51 87
H142		VR_CTL_PHY	VR_CTL				VR_GPU_IMON_R 87
H141		VR_CTL_PHY	VR_CTL				VR_GPU_IOUT_PD
H140		VR_CTL_PHY	VR_CTL				VR_GPU_OFS
H139		VR_CTL_PHY	VR_CTL				VR_GPU_APA
H138			VR_CTL				VR_GPU_EN_VTT
H137			VR_CTL				PM_EN_REG_GPUCORE_S0 72 87
H136			VR_CTL				PM_EN_REG_GPU_CORE_S0_R
H135		VR_CTL_PHY	VR_CTL				VR_GPU_VRDHOT
H134			VR_CTL				GPU_PSI_L
H133			VR_CTL				GPU_PSI_L_R
H132			VR_CTL				PM_PGOOD_REG_GPUCORE_S0 72 87
H131		VR_CTL_PHY	VR_CTL				VR_GPU_REF
H130		VR_CTL_PHY	VR_CTL				VR_GPU_SS
H129		VR_CTL_PHY	VR_CTL				VR_GPU_TCOMP
H128		VR_CTL_PHY	VR_CTL				VR_GPU_TM
H127		VR_CTL_PHY	VR_CTL				VR_GPU_VDIFF
H126	VR_GPU_VSEN	VR_GPU_VSEN	SENSE				VR_GPU_VSEN 87
H125	VR_GPU_RGND	VR_GPU_VSEN	SENSE				VR_GPU_RGND 87
H124	VR_GPU_RCSP	VR_SENSE	SENSE				VR_GPU_RCSP_R 87
H123	VR_GPU_RCSM	VR_SENSE	SENSE				VR_GPU_RCSM_R 87
H122		VR_SENSE	SENSE				VR_GPU_RCSP_RT
H121		VR_SENSE	SENSE				VR_GPU_RCSM_RT
H120		SMB_PHY	SMB				SMB_VR_GPU_SDA_R 87
H119		SMB_PHY	SMB				SMB_VR_GPU_SCL_R 87
	GPU SERIAL VID						
H118	VR_GPU_SVC	VR_SVID_PHY	VR_SVID				VR_GPU_SVC 84 87
H117	VR_GPU_SVD	VR_SVID_PHY					VR_GPU_SVD 84 87
H116	VR_GPU_SVT	VR_SVID_PHY					VR_GPU_SVT 84 87
H115		VR_SVID_PHY	VR_SVID				VR_GPU_SVC_R 87
H114		VR_SVID_PHY					VR_GPU_SVD_R 87
H113		VR_SVID_PHY					VR_GPU_SVT_R 87
	Output Bus						
H160		POWER	POWER	1V			PPGPUCORE_S0 94
H159	VSNS_GPU_VDDCI	VR_SENSE	SENSE				SNS_GPU_VDDCI_P 75 91
H158	VSNS_GPU_VDDCI	VR_SENSE	SENSE				SNS_GPU_VDDCI_N 75 91
H157	ISNS_GPU_VDDCI	VR_SENSE	SENSE				GPU_ISNS_VDDCI_P 51 91
H156	ISNS_GPU_VDDCI	VR_SENSE	SENSE				GPU_ISNS_VDDCI_N 51 91
H155	VSNS_GPU_VDDCI_XW	VR_SENSE	SENSE				SNS_GPU_VDDCI_XW_P 91
H154	VSNS_GPU_VDDCI_XW	VR_SENSE	SENSE				SNS_GPU_VDDCI_XW_N 91
H107	VSNS_P0V95S0_XW	VR_SENSE	SENSE				SNS_P0V95S0_XW_P 92
H107	VSNS_P0V95S0_XW	VR_SENSE	SENSE				SNS_P0V95S0_XW_N 92

GPU FBVDDQ

	Electrical Contraint Set Input Bus	Physical	Spacing	Voltage	DIDT	NO_TEST	
H161		POWER	POWER	5V			REG_VCC_UA450 90
H162		POWER	POWER	5V			REG_PVCC_UA450 90
	Local Ground						
H163		GND	GND	0V			AGND_FBVDDQ 90
	FBVDDQ						
H165		POWER	VR_SWITCH	12V	TRUE		REG_PHASE_FBVDDQ 90
H166		POWER	VR_SWITCH	12V	TRUE		VR_PHASE_FBVDDQ 90
H167		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_FBVDDQ 90
H168		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_FBVDDQ_RC 90
H169		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ 90
H170		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_FBVDDQ 90
H171		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_FBVDDQ 90
H157		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_SET0 90
H156		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_SET1 90
H155		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_SET1_R 90
H154		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_SREF 90
H153			VR_CTL				GPU_FBVDDQ_ALTV 84 90
H152			VR_CTL				FBVDDQ_ALTV0_R 90
H151			VR_CTL				FBVDDQ_ALTV1_R 90
H150			VR_CTL				PM_EN_REG_GPU_VDDQ_S0 72 90
H149			VR_CTL				PM_EN_REG_GPU_VDDQ_S0_R
H148			VR_CTL				PM_PGOOD_REG_GPU_VDDQ_S0 72 90
H147		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_OCSET 90
H146		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_VO 90
H145		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_FB 90
H144		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_RTN 90
H143		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_FB_R 90
H142		VR_CTL_PHY	VR_CTL				REG_FBVDDQ_RTN_R 90
	Output Bus						
H140		POWER	POWER	1.5V			PPFBVDDQ_S0_GPU 94
H139		POWER	POWER	1.5V			VRDDQ_R

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GPU VDDCI

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J140	POWER	POWER	5V			REG_VCC_UA550 91
J141	POWER	POWER	5V			REG_PVCC_UA550 91
Local Ground						
J142	GND	GND	0V			AGND_GPU_VDDCI 91
GPU VDDCI						
J143	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPU_VDDCI 91
J144	POWER	VR_SWITCH	12V	TRUE		VR_PHASE_GPU_VDDCI 91
J145	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPU_VDDCI 91
J146	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPU_VDDCI_RC 91
J147	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPU_VDDCI 91
J148	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPU_VDDCI 91
J149	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPU_VDDCI 91
J150	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_SET0 91
J151	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_SET1 91
J152	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_SET1_R 91
J153	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_SREF 91
J154	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_OCSET 91
J155	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_VO 91
J156	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_FB 91
J157	VR_CTL_PHY	VR_CTL				REG_GPU_VDDCI_RTN 91
J158		VR_CTL				PM_EN_GPU_VDDCI_S0 72 91
J159		VR_CTL				PM_EN_GPU_VDDCI_S0_R 91
J160		VR_CTL				PM_PGOOD_REG_GPU_VDDCI_S0 72 91
J161		VR_CTL				GPU_VDDCI_ALTV 84 91
J162		VR_CTL				GPU_VDDCI_ALTV0 91
J163		VR_CTL				GPU_VDDCI_ALTV1 91
J164	POWER	POWER	0.85V			VRVDDCI_R 91

GPU VDD (1.8V)

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
GPU VDD						
J153	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_PVDDR 93
J154	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_PVDDR 93
J155	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_PVDDR_R 93
J156	GND	GND	0V			AGND_PVDDR 93
J157	VR_CTL_PHY	VR_CTL				REG_VSNSR_PVDDR 93
J158	VR_CTL_PHY	VR_CTL				REG_VSNS_PVDDR 93
J159	VR_CTL_PHY	VR_CTL				REG_SSTR_PVDDR 93
J160	VR_CTL_PHY	VR_CTL				REG_COMP_PVDDR 93
J161		VR_CTL				PM_EN_REG_PVDDCT_S0 72 93
J162		VR_CTL				PM_EN_REG_PVDDCT_S0_R 93
J163		VR_CTL				PM_PGOOD_REG_PVDDCT_S0 72 93

GPU CORE (CONT.)

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
J165 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_1_XW_N
J166 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_1_XW_P
J167 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_2_XW_N
J168 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_2_XW_P
J169 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_3_XW_N
J170 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_3_XW_P
J171 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_4_XW_N
J172 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_4_XW_P
J173 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_5_XW_N
J174 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_5_XW_P
J175 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_6_XW_N
J176 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_GPUCORE_ISNS_6_XW_P

GPU VDDC (0.95V)

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J177	POWER	POWER	5V			REG_VCC_UA660 92
J178	POWER	POWER	5V			REG_PVCC_UA660 92
Local Ground						
J179	GND	GND	0V			AGND_P0V95S0 92
GPU VDDC						
J180	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_P0V95S0 92
J181	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P0V95S0 92
J182	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P0V95S0_RC 92
J183	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P0V95S0 92
J184	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P0V95S0 92
J185	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_P0V95S0 92
J186	VR_CTL_PHY	VR_CTL				REG_P0V95S0_OCSET 92
J187	VR_CTL_PHY	VR_CTL				REG_P0V95S0_VO 92
J188	VR_CTL_PHY	VR_CTL				REG_P0V95S0_FB 92
J189	VR_CTL_PHY	VR_CTL				REG_P0V95S0_RTN 92
J190	VR_CTL_PHY	VR_CTL				REG_P0V95S0_SREF 92
J191		VR_CTL				PM_EN_REG_P0V95_S0 72 92
J192		VR_CTL				PM_EN_REG_P0V95_S0_R 92
J193		VR_CTL				PM_PGOOD_REG_P0V95_S0 72 92

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4V5_*

	Physical	Spacing	Netname	
I2	POWER	POWER	4V5_REG_IN	54

ENET_*

	Physical	Spacing	Netname	
I103	XDP_PHY	XDP	ENET_LOW_PWR	20 37 39

GPU_*

	Physical	Spacing	Netname	
I105	SPI_50S	SPI	GPU_ROM_CS_L	84
I106	SPI_50S	SPI	GPU_ROM_CS_L_R	84 85
I107	SPI_50S	SPI	GPU_ROM_SI	84
I108	SPI_50S	SPI	GPU_ROM_SI_R	84 85
I109	SPI_50S	SPI	GPU_ROM_SO	84 85
I111	SPI_50S	SPI	GPU_ROM_SO_R	85
I110	SPI_50S	SPI	GPU_ROM_WP_L	85
I172	SPI_50S	SPI	GPU_ROM_SCLK	
I177	SPI_50S	SPI	GPU_ROM_SCLK_R	

JTAG_*

	Physical	Spacing	Netname	
I112	XDP_PHY	XDP	JTAG_TBT_TDI	20 28
I113	XDP_PHY	XDP	JTAG_TBT_TDO	20 28
I114	XDP_PHY	XDP	JTAG_TBT_TMS	20 28

ISNS_*

Physical	Spacing	Netname

SMC_*

	Physical	Spacing	Netname	
I134	CLK_XTAL	XTAL	SMC_XTAL_R	47

REG_*

Physical	Spacing	Netname

SMBUS_*

	Physical	Spacing	Netname	
I120	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL	46 47
I121	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA	46 47

SMC_*

	Physical	Spacing	Netname	
I130	SENSE	SENSE	SMC_OOB1_RX_CN	36
I131	SENSE	SENSE	SMC_OOB1_RX_FILT	36

TSNS_*

	Electrical	Physical	Spacing	Netname	
I137	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_N	52
I138	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_P	52
I139	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_N	52
I140	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_P	52
I141	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_N	52
I142	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_P	52
I143	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_N	52
I144	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_P	52
I145	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_N	52
I146	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_P	52
I147	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_N	52
I148	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_P	52
I149	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_N	52
I150	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_P	52
I151	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_N	52
I152	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_P	52
I153	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_N	52
I154	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_P	52
I155	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_N	52
I156	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_P	52

BLC_*

	Physical	Spacing	Voltage	Netname
I32	BLC_CTL_PHY	BLC_CTL	5V	BLC_MCU_AOUT_R
I33	SMB_PHY	SMB		BLC_MCU_B_SDA_CONN
I34	XDP_PHY	CLK_JTAG		BLC_MCU_RTCK
I35	XDP_PHY	XDP		BLC_MCU_TCK
I36	XDP_PHY	XDP		BLC_MCU_TDI
I37	XDP_PHY	XDP		BLC_MCU_TDO
I38	XDP_PHY	XDP		BLC_MCU_TMS
I39	XDP_PHY	XDP		BLC_MCU_TRST
I40	XDP_PHY	XDP		BLC_MCU_TXD0

TBT_*

	Physical	Spacing	Voltage	Netname	
I130	TBT_I2C_55S	TBT_I2C		TBT_A_CONFIG1_RC	31
I131	TBT_I2C_55S	TBT_I2C		TBT_B_CONFIG1_RC	32

AYNCHRONOUS

	Electrical	Physical	Spacing	Netname	
I160		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L	6 46 47 63
I161		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L	6
I162		CPU_ASYNC_PHY	CPU_ASYNC	SMC_PECI_L	46 47
I163		CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERR_L	6 47
I164		CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD	6 14 18
I165		CPU_ASYNC_PHY	CPU_ASYNC	PM_SYNC	6 12
I166		CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L	14 47
I167		CPU_ASYNC_PHY	CPU_ASYNC	CPU_RESET_L	6 14 18
I168		CPU_ASYNC_PHY	CPU_ASYNC	SMC_CPU_CATERR_L	46 47
I170		CPU_ASYNC_PHY	CPU_ASYNC	PCH_PROCPWRGD	14
I171		PCH_ASYNC_PHY	PCH_ASYNC	GPU_GOOD	3 14 18

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ASYNC_ISO	*	=3:1_SPACING	?
PCH_ASYNC_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ASYNC	*	*	CPU_ASYNC_ISO
PCH_ASYNC	*	*	PCH_ASYNC_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_ASYNC_PHY	*	CPU_50S
PCH_ASYNC_PHY	*	PCH_50S

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