Model Name: 8I915PL-G REV1.0

SHEET	TITLE
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D
08	VCORE POWER
09	GMCH-GRANTSDALE_HOST
10	GMCH-GARNTSDALE_DDR
11	GMCH-GRANTSDALE_PCI E, DMI
12	GMCH-GRANTSDALE_INT VGA
13	GMCH-GRANTSDALE_GND
14	GMCH-GRANTSDALE_PWR
15	DDR CHANNEL A
16	DDR CHANNEL B
17	DDR TERMINATION
18	PCI EXPRESS*16 SLOT
19	ICH6 PCI, USB, DMI, LAN
20	ICH6 IDE, GPIO, SATA, CTRL
21	ICH6 VCC, GND
22	CLK GEN

SHEET	TITLE
23	PCI SLOT
24	PCI EXPRESS*1 SLOT
25	ITE8712HX
26	HWMO/FAN/FWH BIOS
27	KB_MS/GAME
28	COM/LPT/FDD
29	(FRONT+REAR)USB/RING/IDE
30	AZALIA CODEC ALC880/CMI9880
31	AUDIO JACK
32	LAN BCM5705E/5751
33	LAN BCM5751
34	ATX POWER CONN.
35	ALL POWER
36	1394 TSB43AB23
37	FRONT PANEL/BZ
38	RAID VIA6410
39	RAID IDE CONNECTOR
40	GPIO TABLE
41	RESET TABLE

COMPONENT SIDE (1 oz. Copper)
SOLDER SIDE (1 oz. Copper)

GIGABYTE

Title	Cover Sheet		
Size: Custom	Document Number: 8I915PL-G		Rev: 1.0
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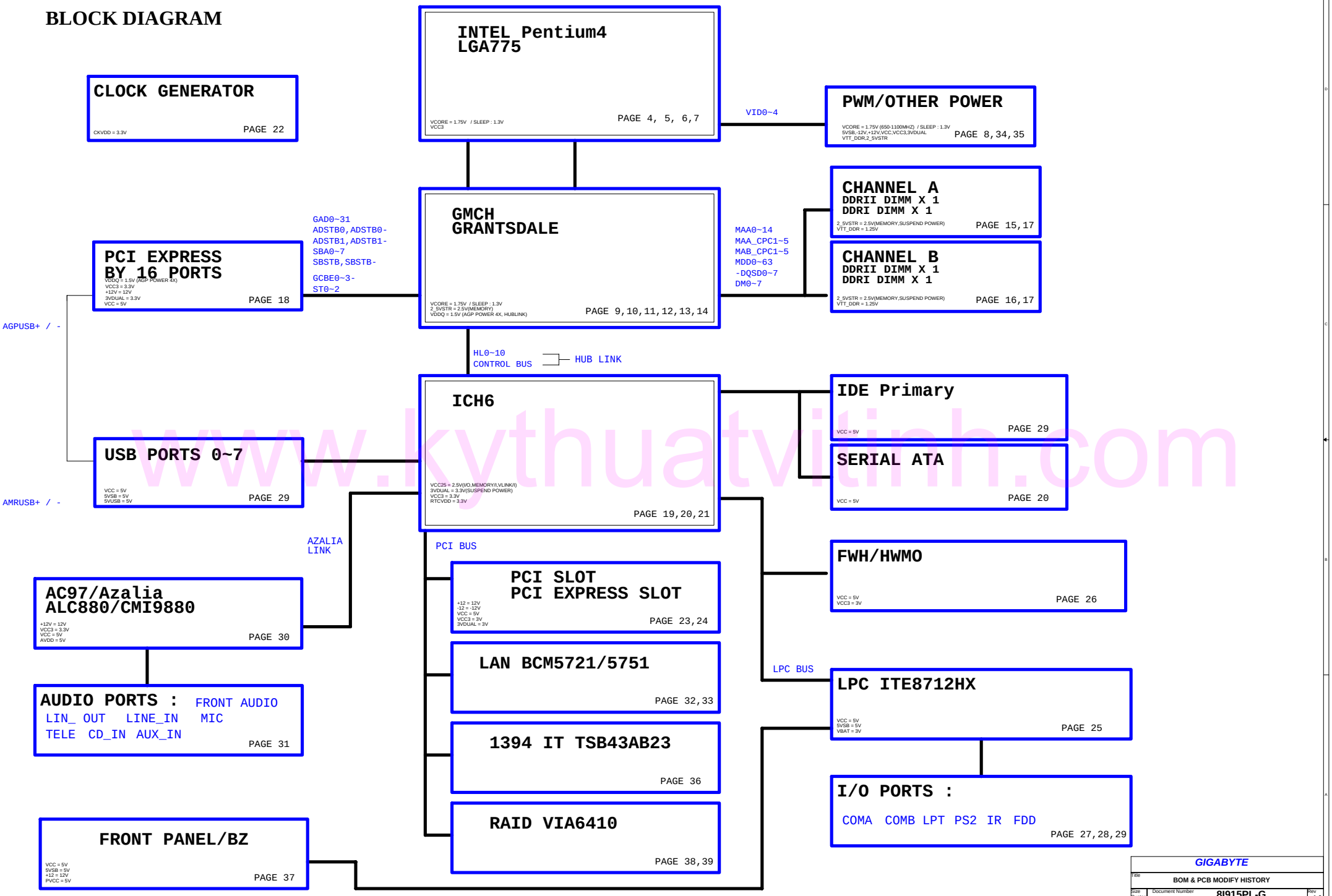
BLOCK DIAGRAM



GIGABYTE

Title	BOM & PCB MODIFY HISTORY	
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
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Model Name: 8I915PL-G
Version: 1.0

Component value change history

2004/11/22

Data	Change Item	Reason
915PL	PCB 8I915PC DUO Rev1.0 --> 8I915PL-G Rev1.0	
10A-0118	1. U19 ICH6 Rev.B1 --> C0	
	2. U9 915P Rev.B1 --> 915pl Rev.C2	
	3. DDRII1,DDRII2 REMOVE	
	4. Q259,Q260,Q274,Q275 2N7002 , R146=1K/6 , R1515=8.2K/6 REMOVE	

Circuit or PCB layout change for next version

PAGE	Change Item	Reason
0.1	EVT	
1.0	PCB 8I915PC DUO Rev0.1 --> 8I915PC DUO Rev1.0	
	ALL 0ohm resister remove , 注意鋪銅	
	CHOKE DL2,DL3,DL4 MODIFY FOOTPRINT=CHOKE06U-40A_1PDL	
	LU1 MARVELL8001 VDD15_L & AVDD25_L ADD 100U/DIP	
	ADD USB PROTECT DIODE	
	ITE8712 GPIO MODIFY FOR OVER VOLTAGE & TURBO PIN	
	LU1 MARVELL8001 PIN8,PIN9不要鋪銅,工廠ICT會SHORT	
	PROCHOT THERMAL RESISTOR REMOVE TO PWM MOSFET	
	背版(ICH6)ICT測試點,保持1.27mm以上	
	CPU PIN/H16 , PIN/U3 未LAUOUT TESTPOINT	
	注意VCC1_5切割 (干擾MCHCLK)	
	BAT SOCKET要改成CO-LAYOUT	
	AUDIO & LAN 之間的AGND,COMP-SOLDER SIDE切開,COMP增加CR32=2.2 ohm	
	PIN HEADER CHECK NEME RULE	

GIGABYTE

Title: BOM & PCB MODIFY HISTORY

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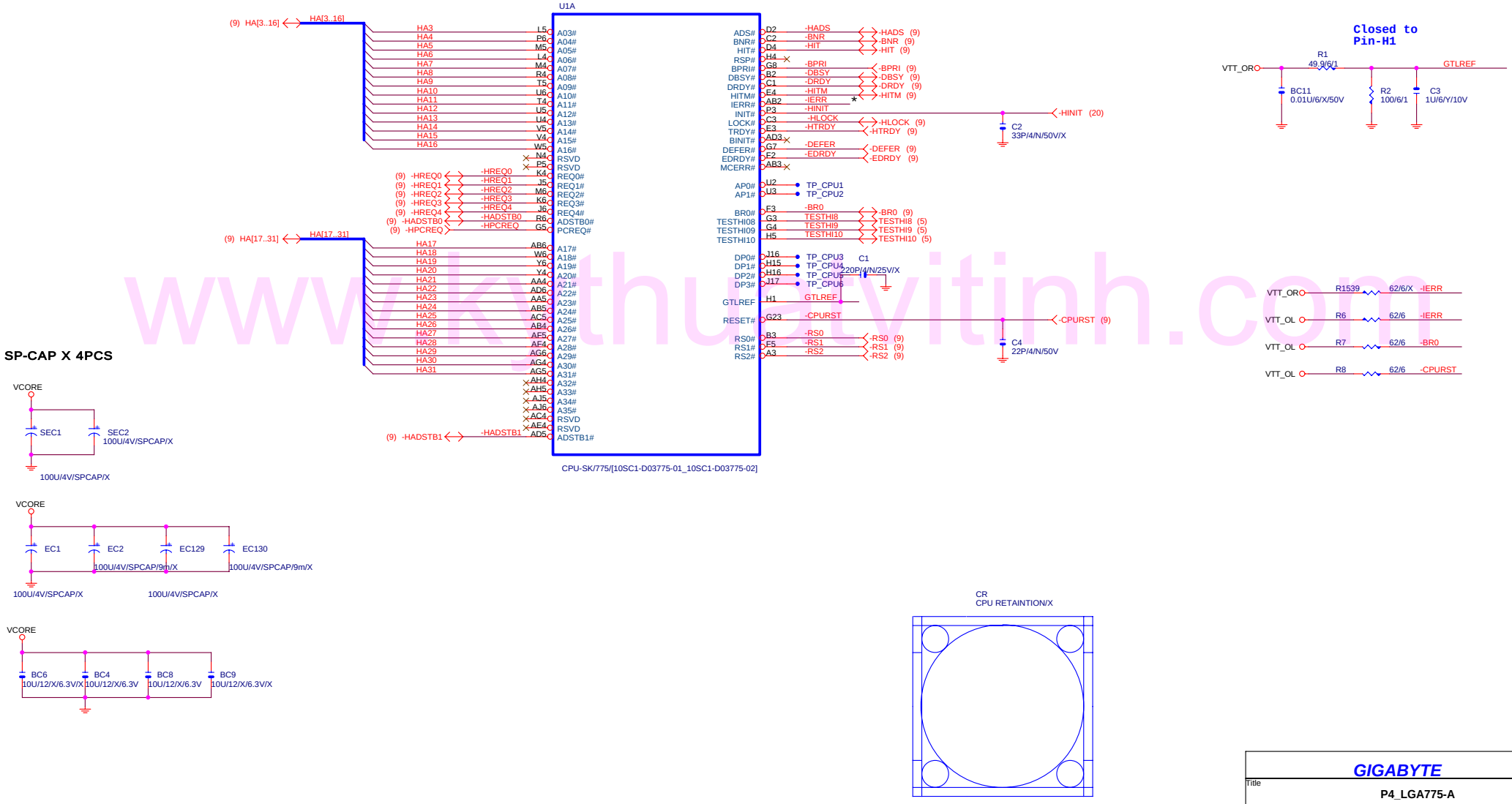

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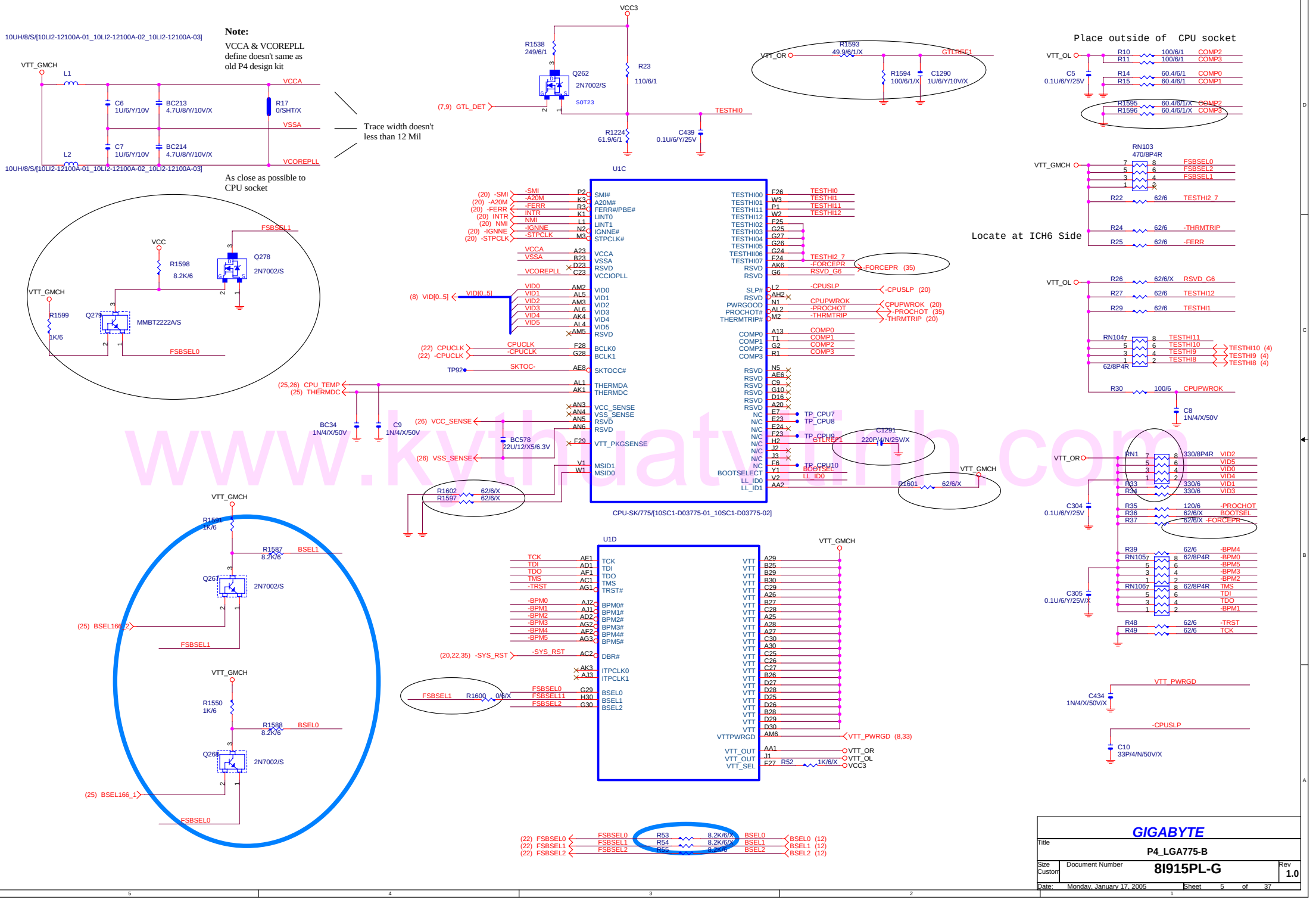
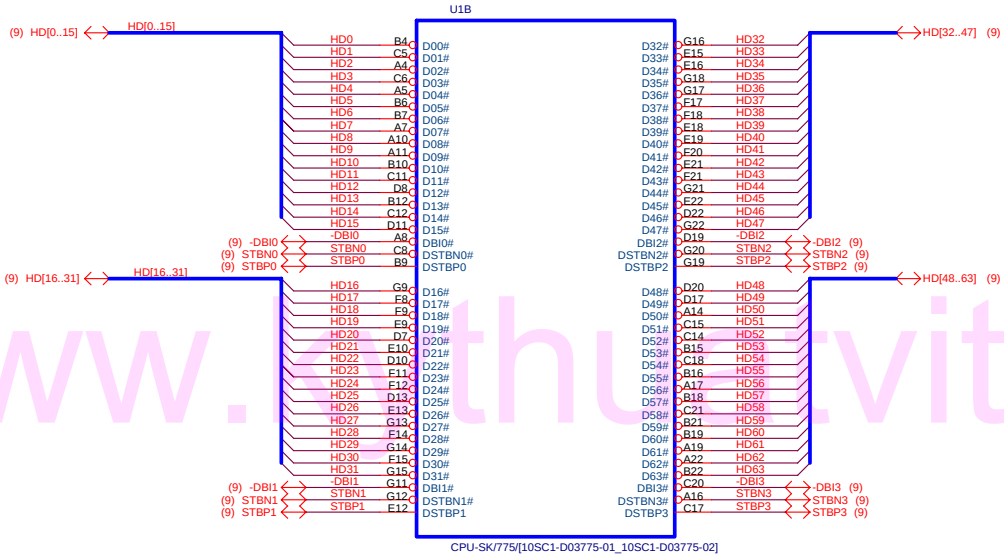
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 4 of 37	





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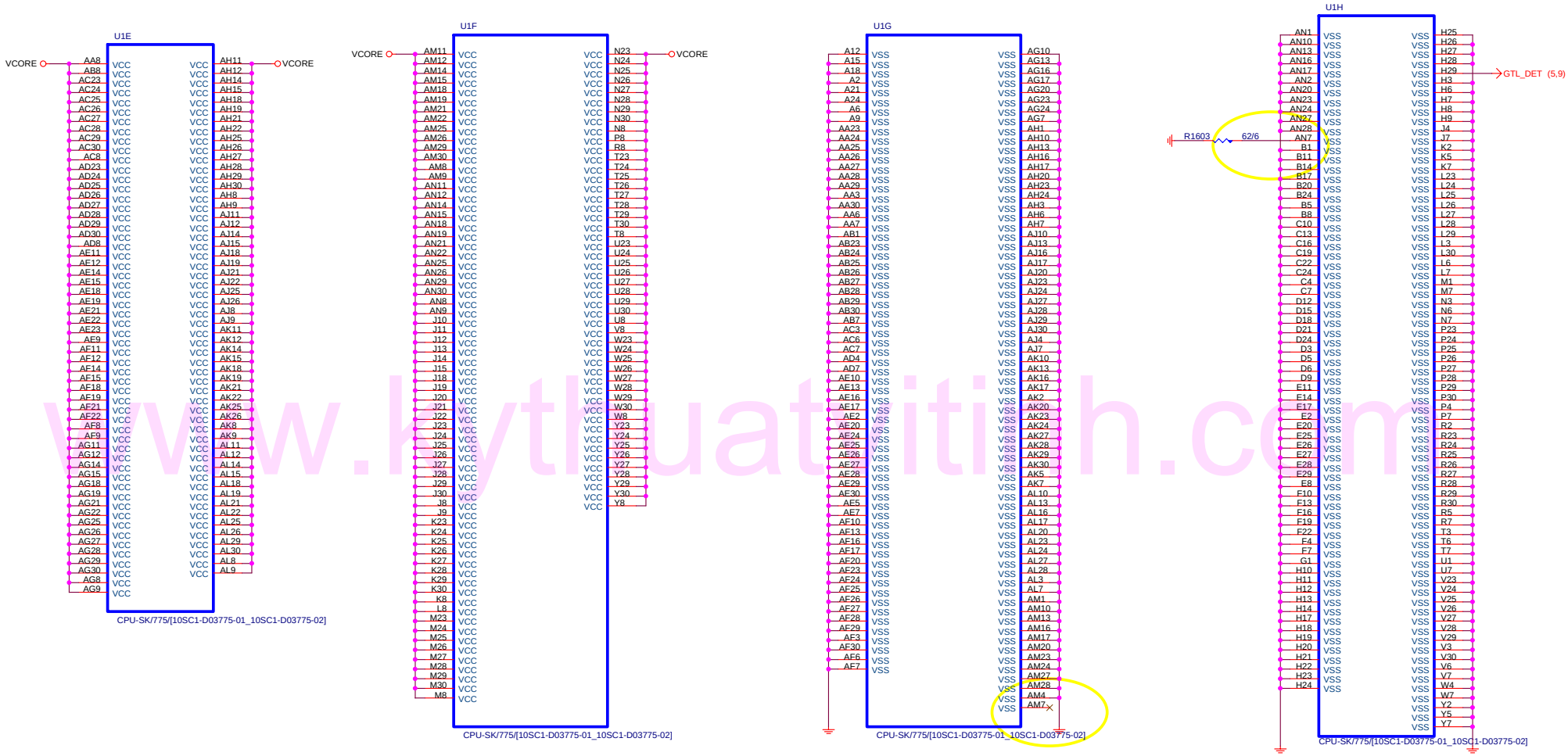
Title	P4_LGA775-C	
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 6 of 37	



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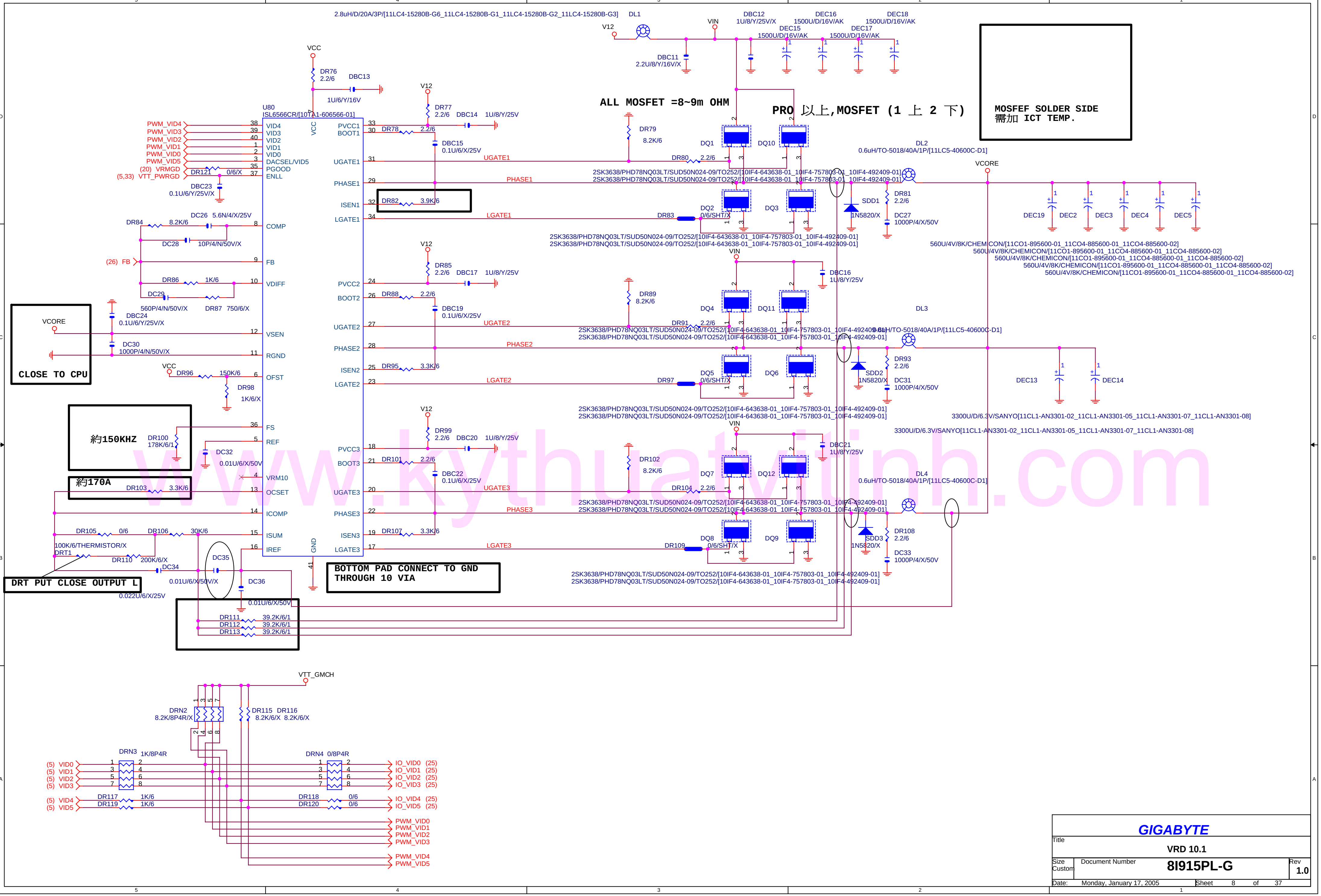
Size: Custom	Document Number: 8I915PL-G		Rev: 1.0
Date: Monday, January 17, 2005		Sheet 7 of 37	



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Title	VRD 10.1
Size: Custom; Document Number	8I915PL-G
Rev	1.0
Date:	Monday, January 17, 2005
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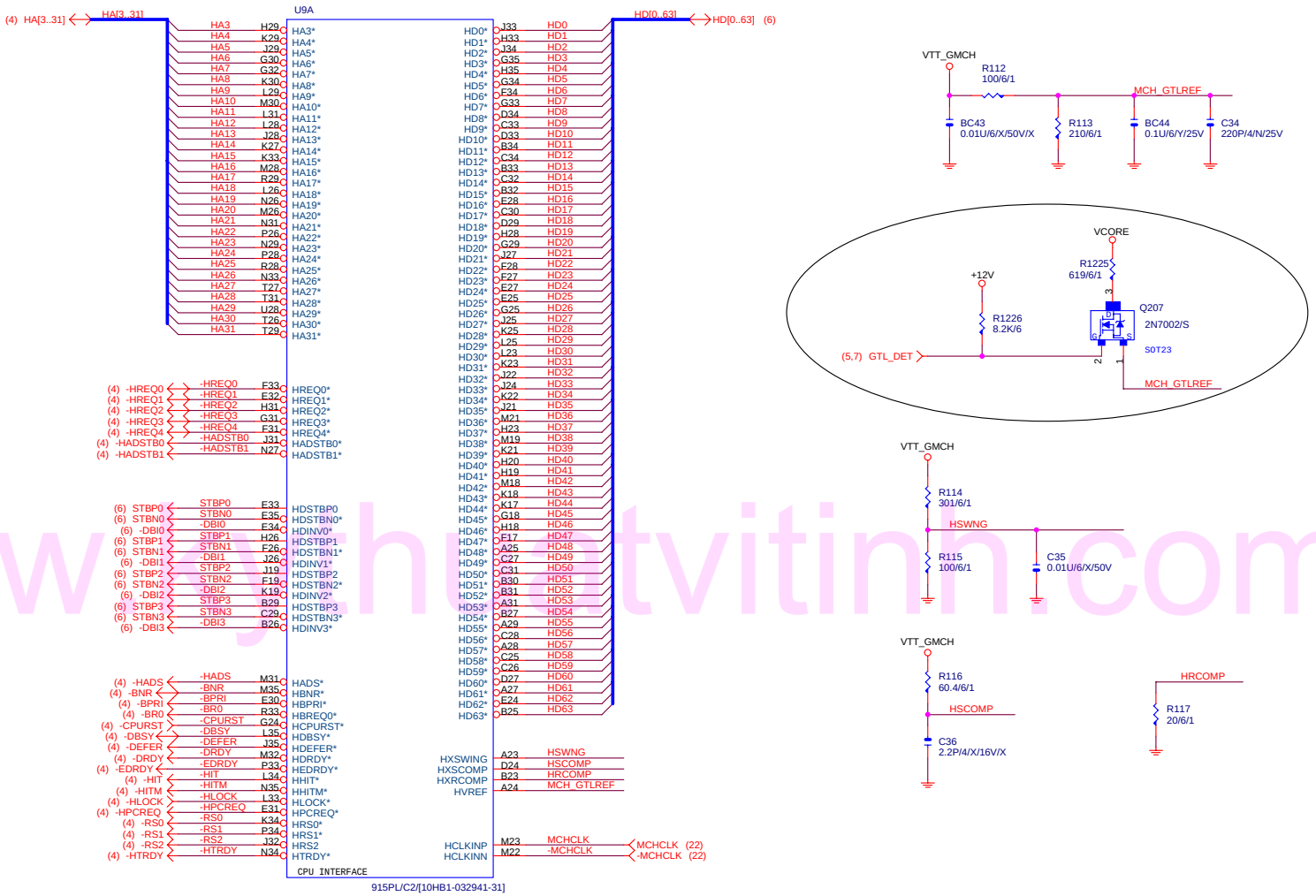

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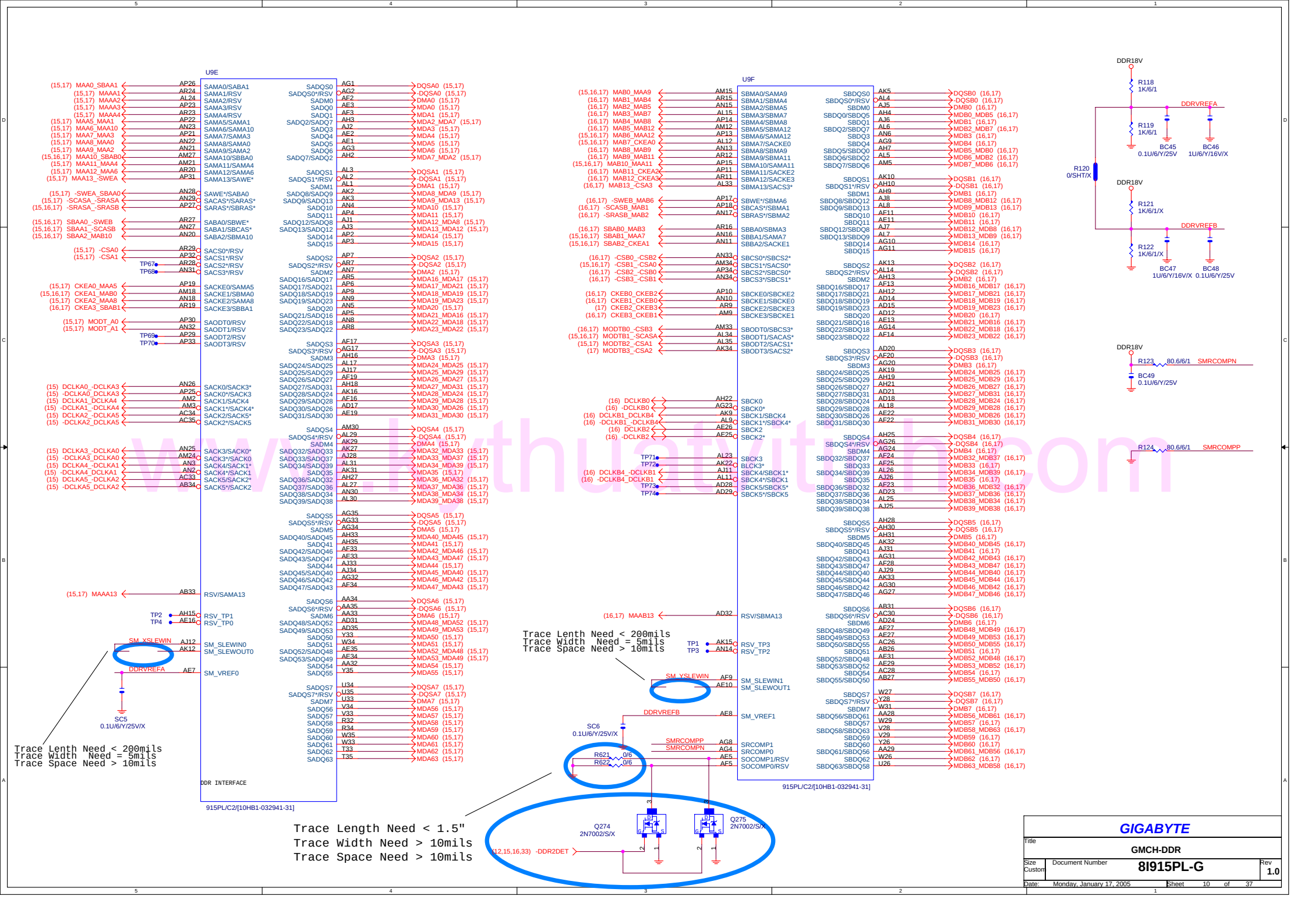
Title	GMCH-HOST		
Size: Custom	Document Number: 8I915PL-G		Rev: 1.0
Date: Monday, January 17, 2005	Sheet 9 of 37		



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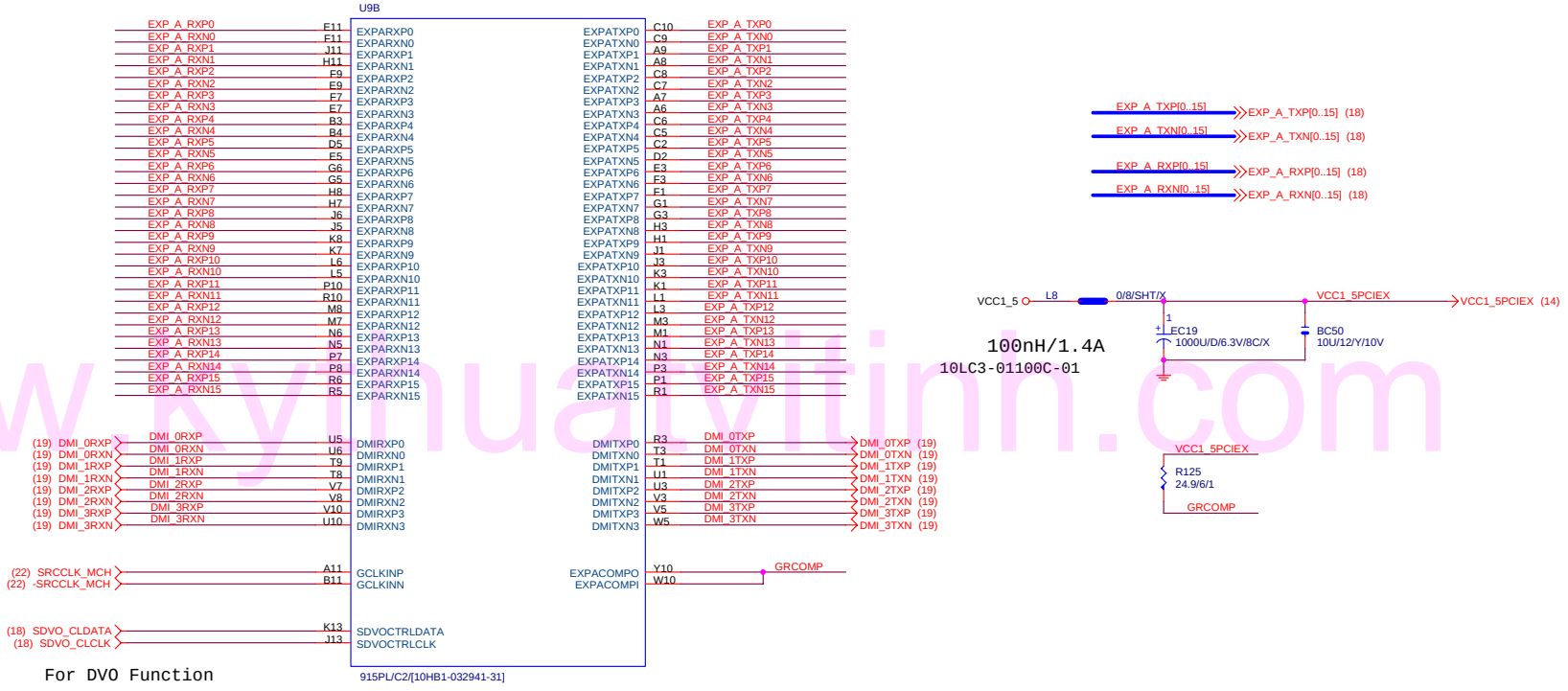
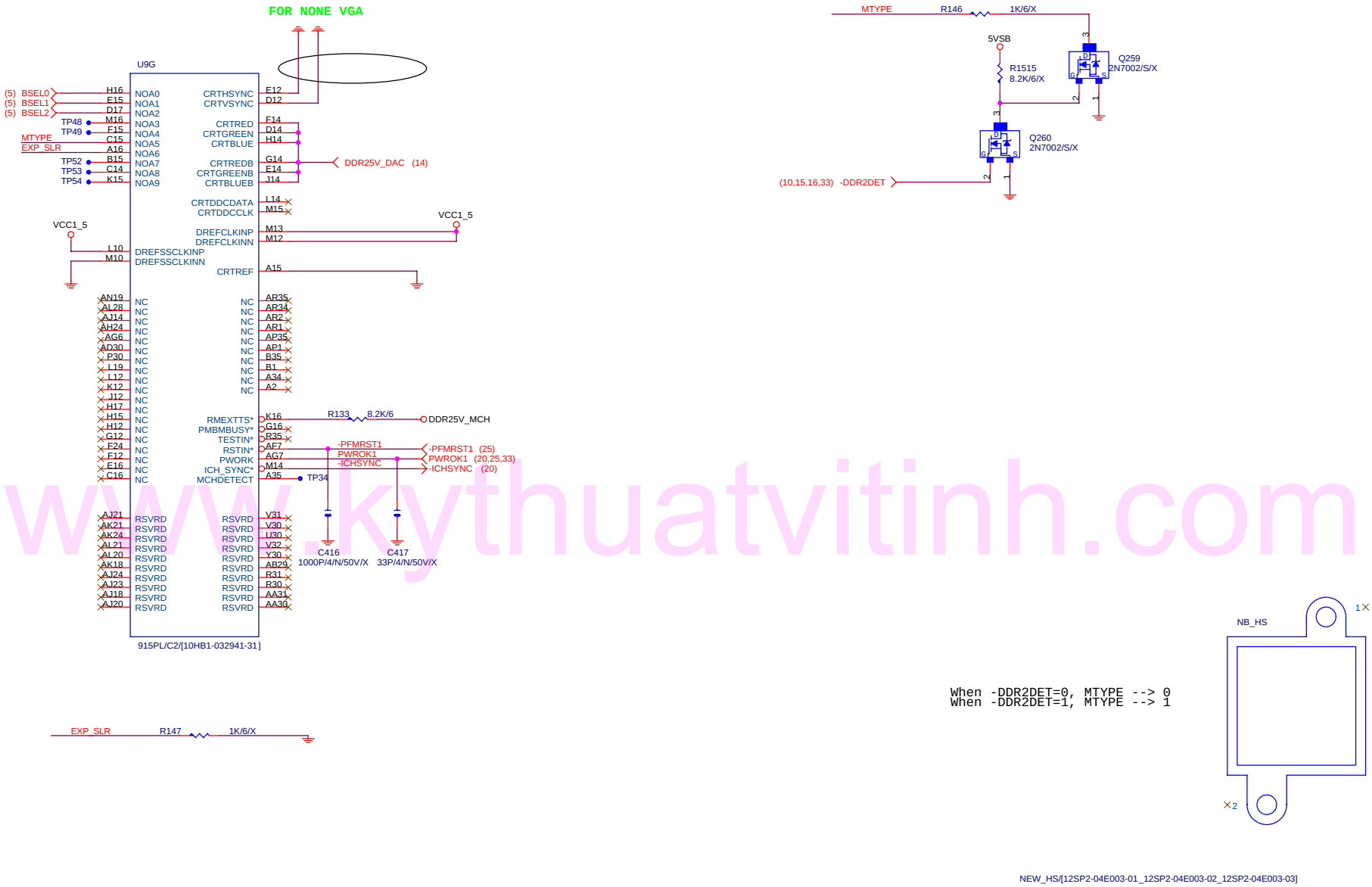
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 10 of 37	



GIGABYTE

Title	GMCH-PCI E & DMI	
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 11 of 37	



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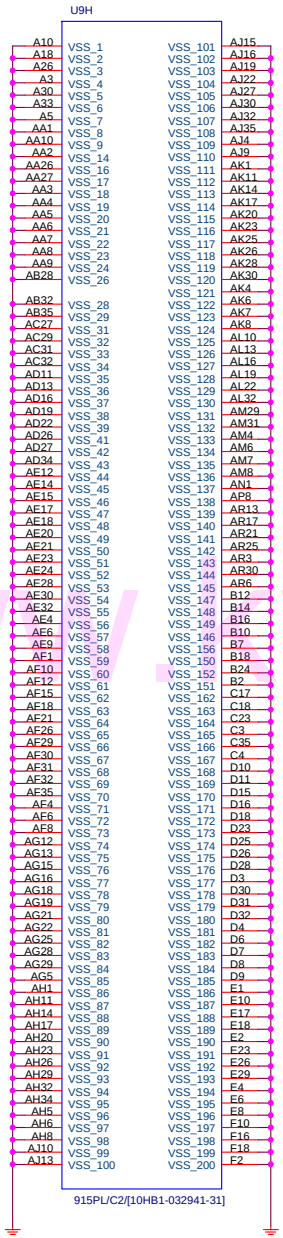
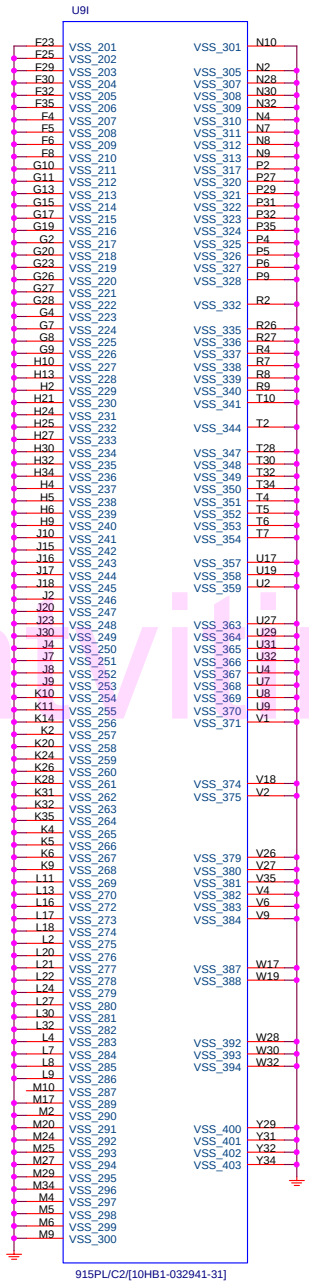
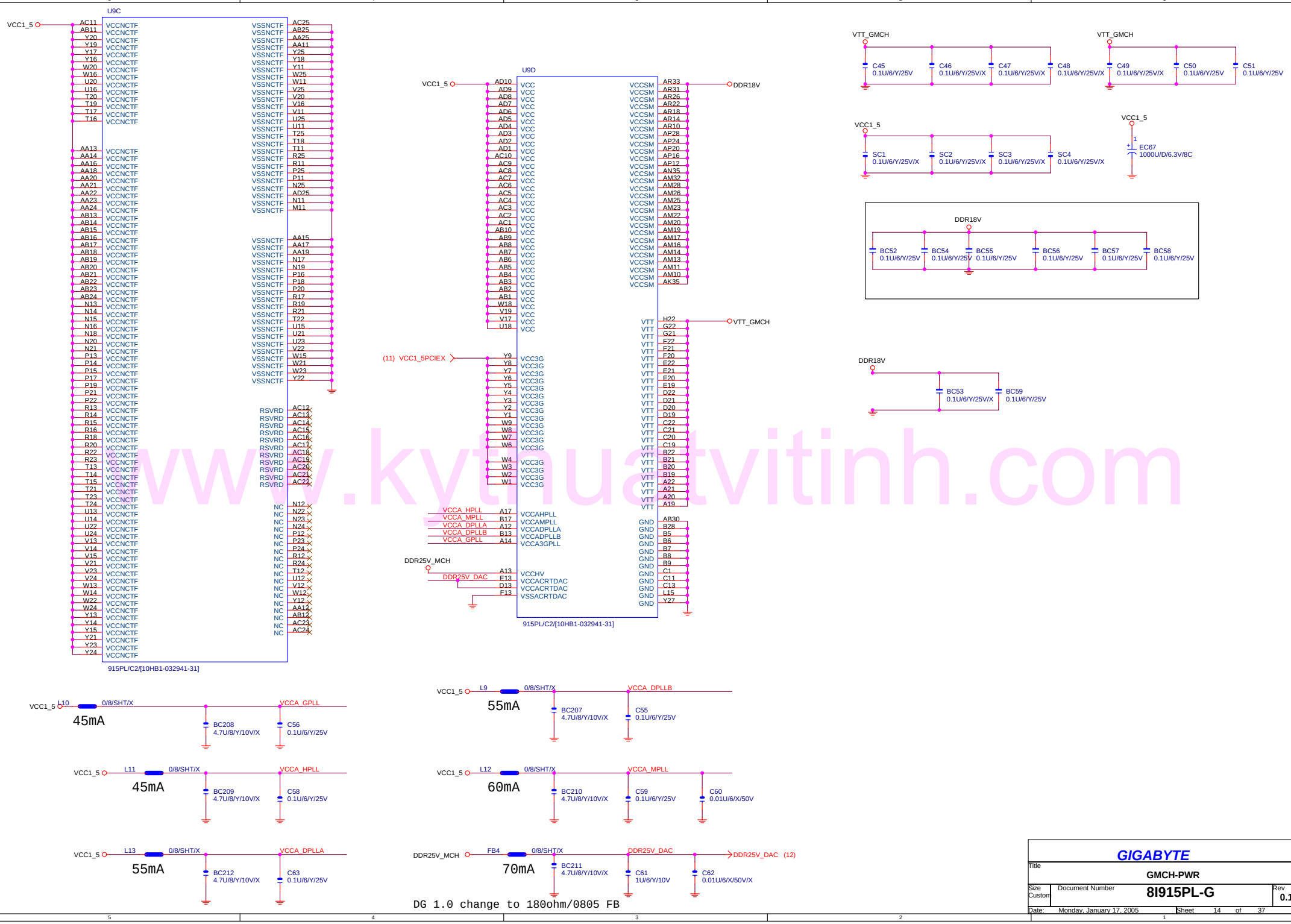
Title	GMCH-INTERNAL VGA	
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 12 of 37	

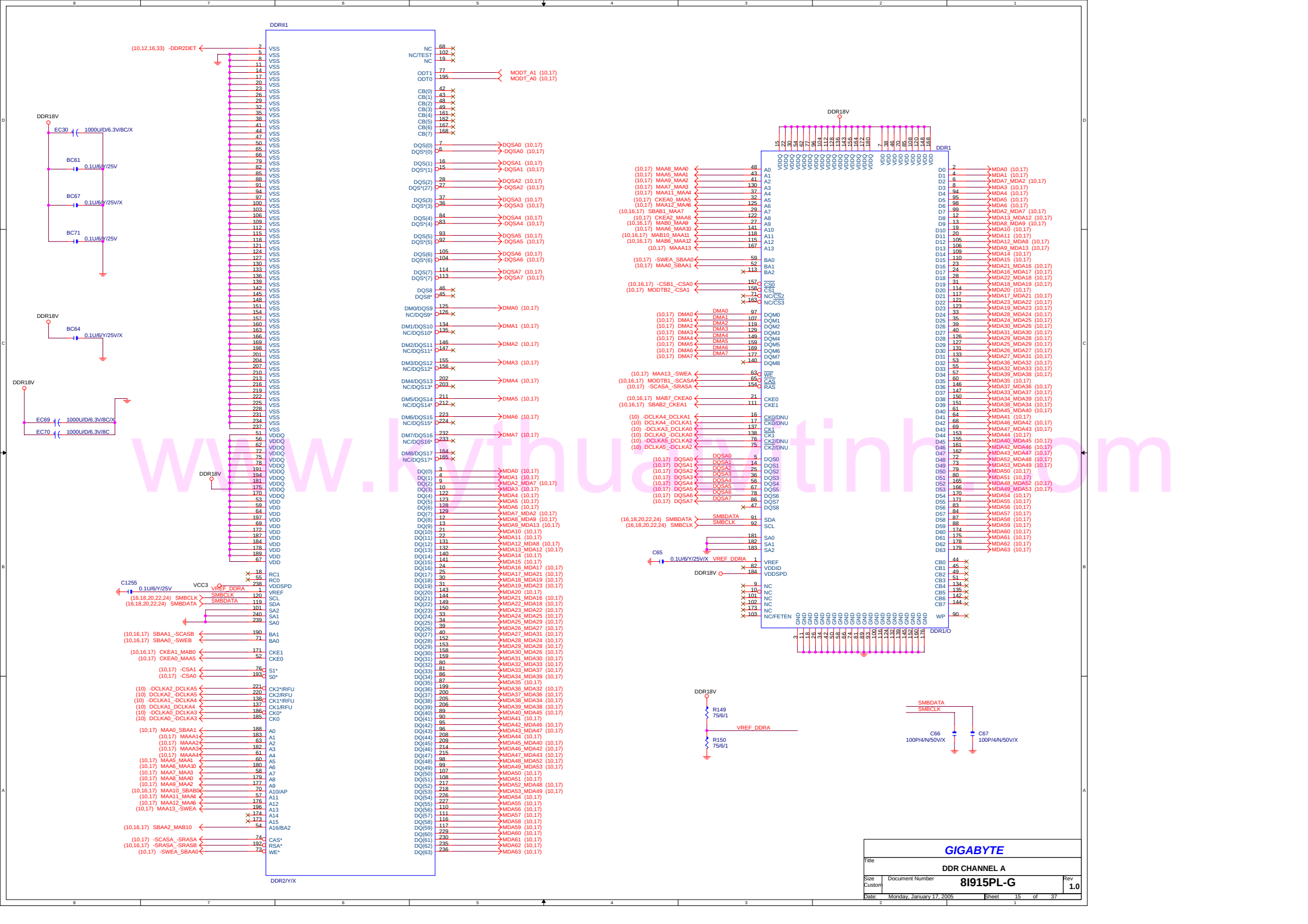


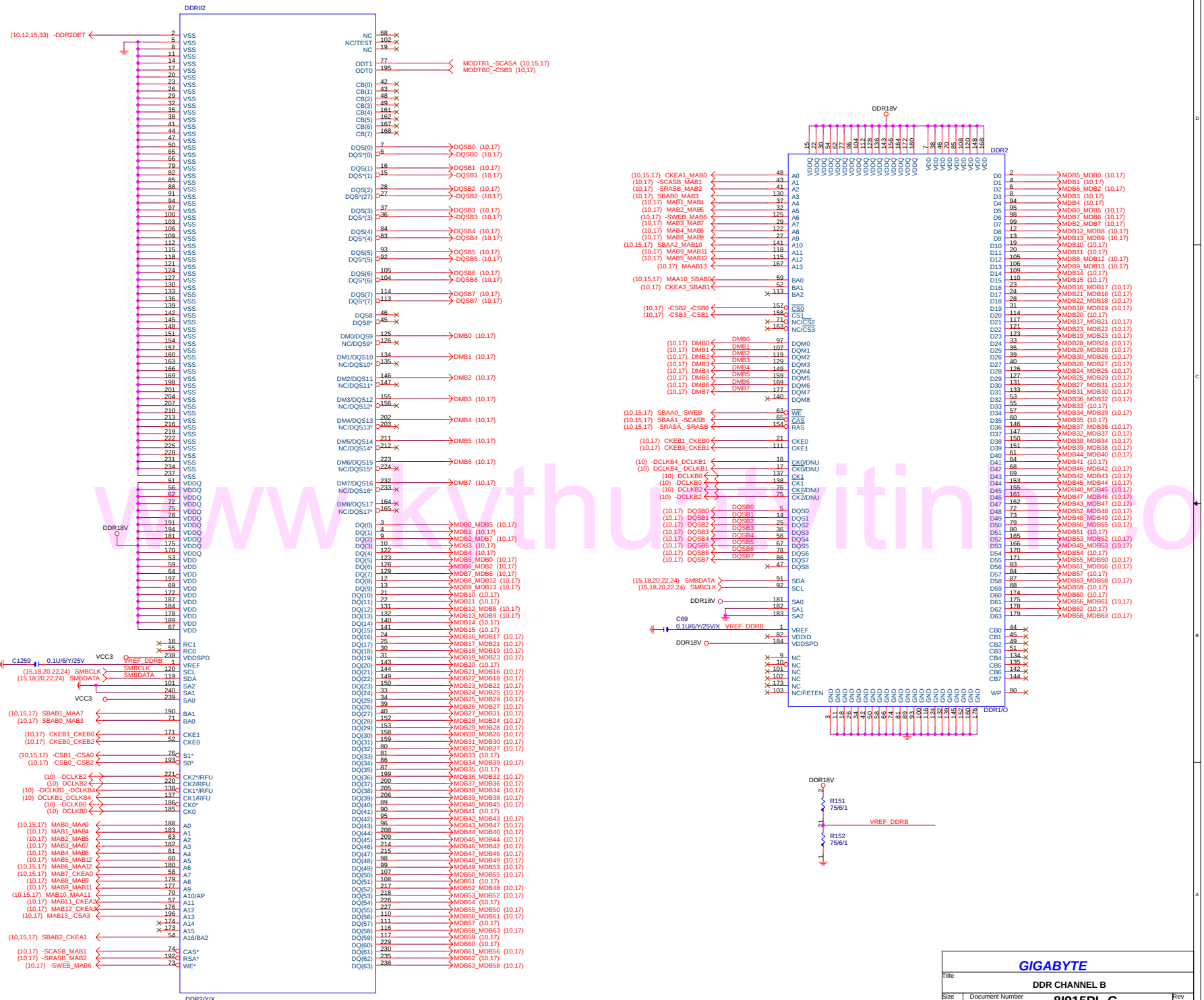


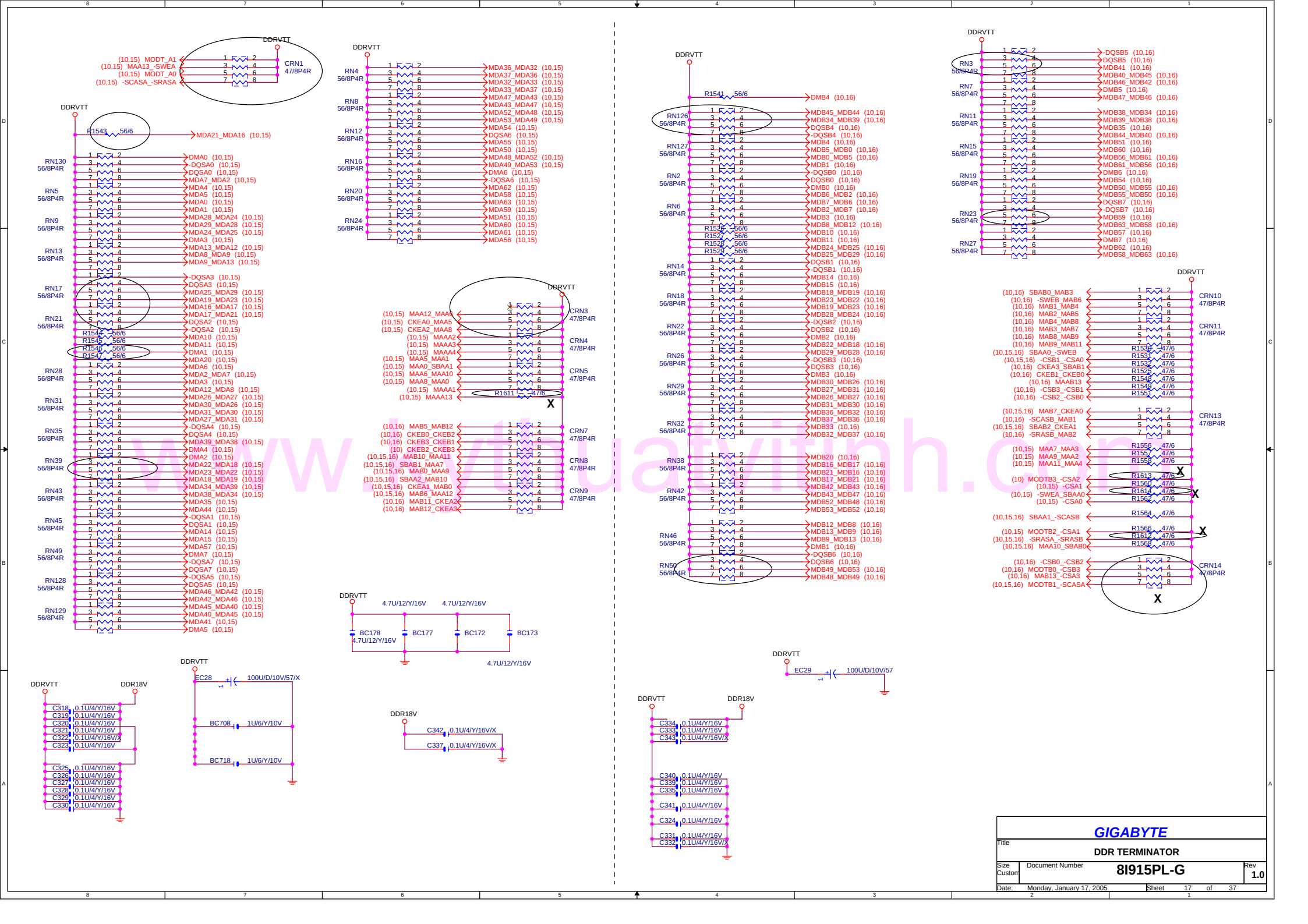
GIGABYTE

Title	GMCH-GND	
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 13 of 37	









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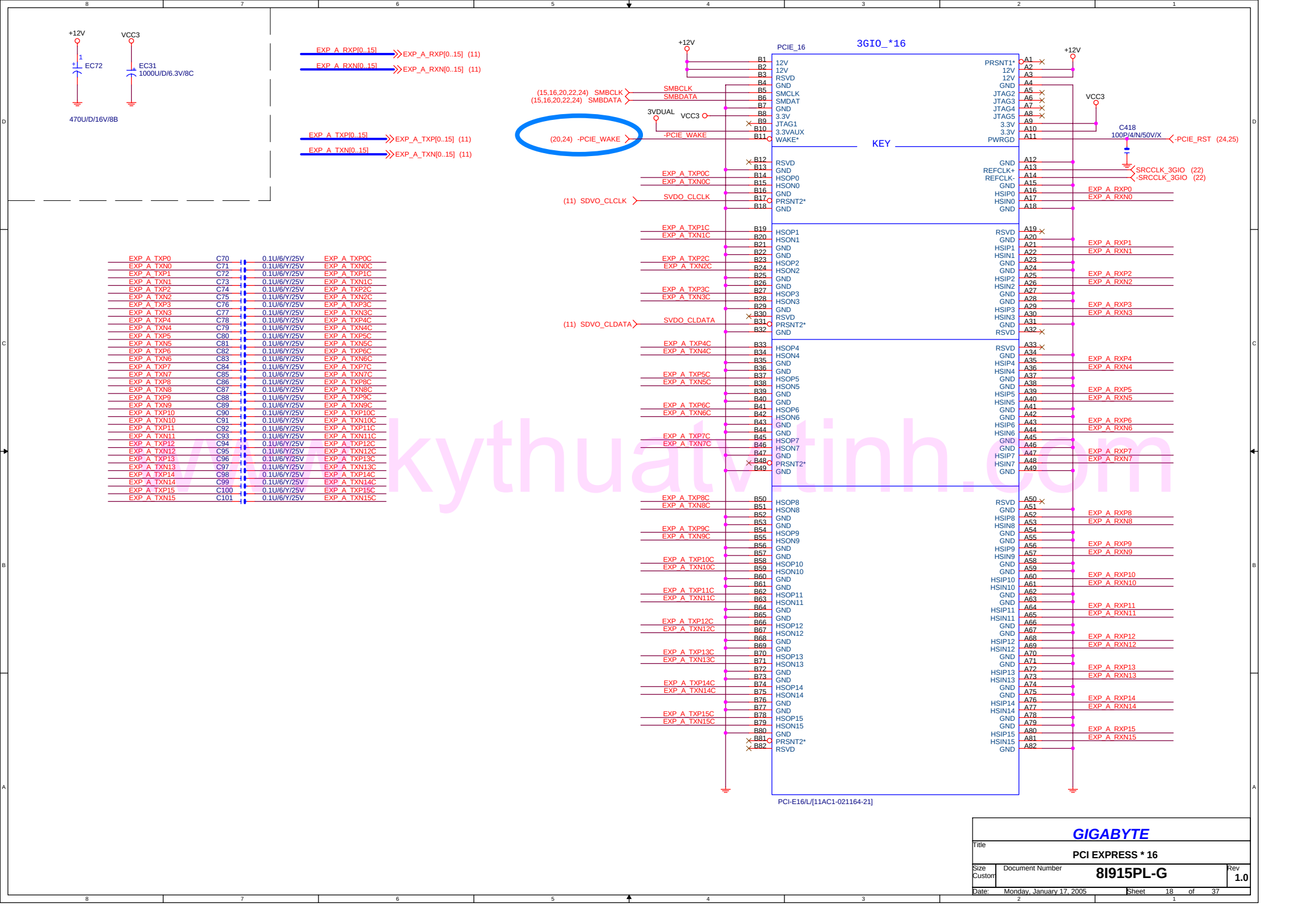
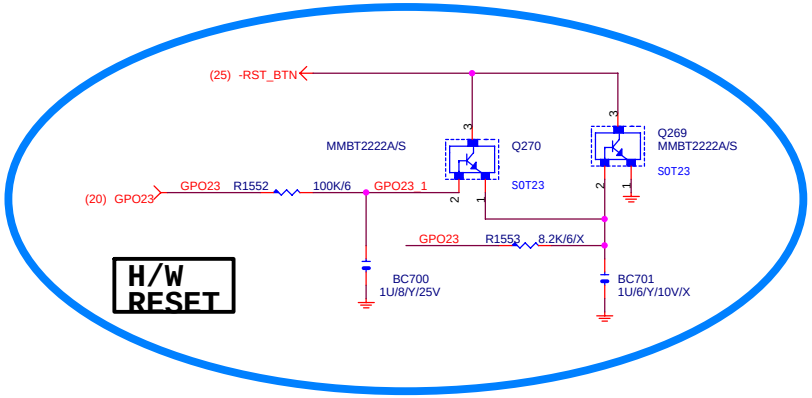
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 17 of 37	

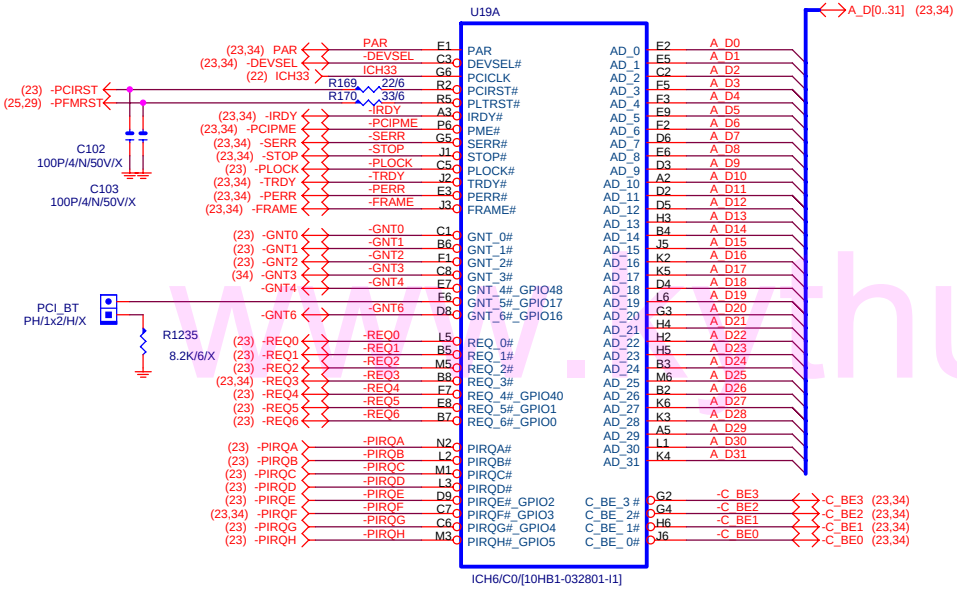


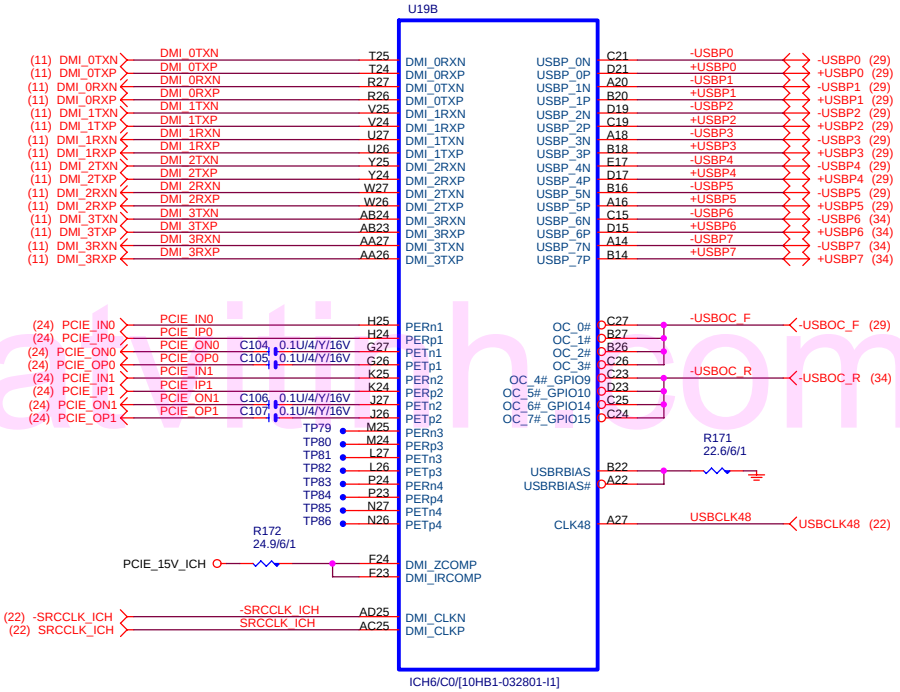
EXP_A_TXP0	C70	0.1U/6/Y/25V	EXP_A_TXP0C
EXP_A_TXN0	C71	0.1U/6/Y/25V	EXP_A_TXN0C
EXP_A_TXP1	C72	0.1U/6/Y/25V	EXP_A_TXP1C
EXP_A_TXN1	C73	0.1U/6/Y/25V	EXP_A_TXN1C
EXP_A_TXP2	C74	0.1U/6/Y/25V	EXP_A_TXP2C
EXP_A_TXN2	C75	0.1U/6/Y/25V	EXP_A_TXN2C
EXP_A_TXP3	C76	0.1U/6/Y/25V	EXP_A_TXP3C
EXP_A_TXN3	C77	0.1U/6/Y/25V	EXP_A_TXN3C
EXP_A_TXP4	C78	0.1U/6/Y/25V	EXP_A_TXP4C
EXP_A_TXN4	C79	0.1U/6/Y/25V	EXP_A_TXN4C
EXP_A_TXP5	C80	0.1U/6/Y/25V	EXP_A_TXP5C
EXP_A_TXN5	C81	0.1U/6/Y/25V	EXP_A_TXN5C
EXP_A_TXP6	C82	0.1U/6/Y/25V	EXP_A_TXP6C
EXP_A_TXN6	C83	0.1U/6/Y/25V	EXP_A_TXN6C
EXP_A_TXP7	C84	0.1U/6/Y/25V	EXP_A_TXP7C
EXP_A_TXN7	C85	0.1U/6/Y/25V	EXP_A_TXN7C
EXP_A_TXP8	C86	0.1U/6/Y/25V	EXP_A_TXP8C
EXP_A_TXN8	C87	0.1U/6/Y/25V	EXP_A_TXN8C
EXP_A_TXP9	C88	0.1U/6/Y/25V	EXP_A_TXP9C
EXP_A_TXN9	C89	0.1U/6/Y/25V	EXP_A_TXN9C
EXP_A_TXP10	C90	0.1U/6/Y/25V	EXP_A_TXP10C
EXP_A_TXN10	C91	0.1U/6/Y/25V	EXP_A_TXN10C
EXP_A_TXP11	C92	0.1U/6/Y/25V	EXP_A_TXP11C
EXP_A_TXN11	C93	0.1U/6/Y/25V	EXP_A_TXN11C
EXP_A_TXP12	C94	0.1U/6/Y/25V	EXP_A_TXP12C
EXP_A_TXN12	C95	0.1U/6/Y/25V	EXP_A_TXN12C
EXP_A_TXP13	C96	0.1U/6/Y/25V	EXP_A_TXP13C
EXP_A_TXN13	C97	0.1U/6/Y/25V	EXP_A_TXN13C
EXP_A_TXP14	C98	0.1U/6/Y/25V	EXP_A_TXP14C
EXP_A_TXN14	C99	0.1U/6/Y/25V	EXP_A_TXN14C
EXP_A_TXP15	C100	0.1U/6/Y/25V	EXP_A_TXP15C
EXP_A_TXN15	C101	0.1U/6/Y/25V	EXP_A_TXN15C

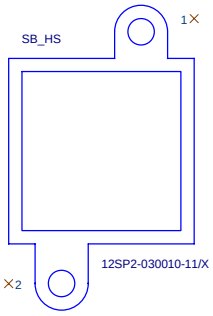
GIGABYTE			
Title: PCI EXPRESS * 16			
Size: Custom	Document Number: 8I915PL-G		Rev: 1.0
Date: Monday, January 17, 2005		Sheet 18 of 37	



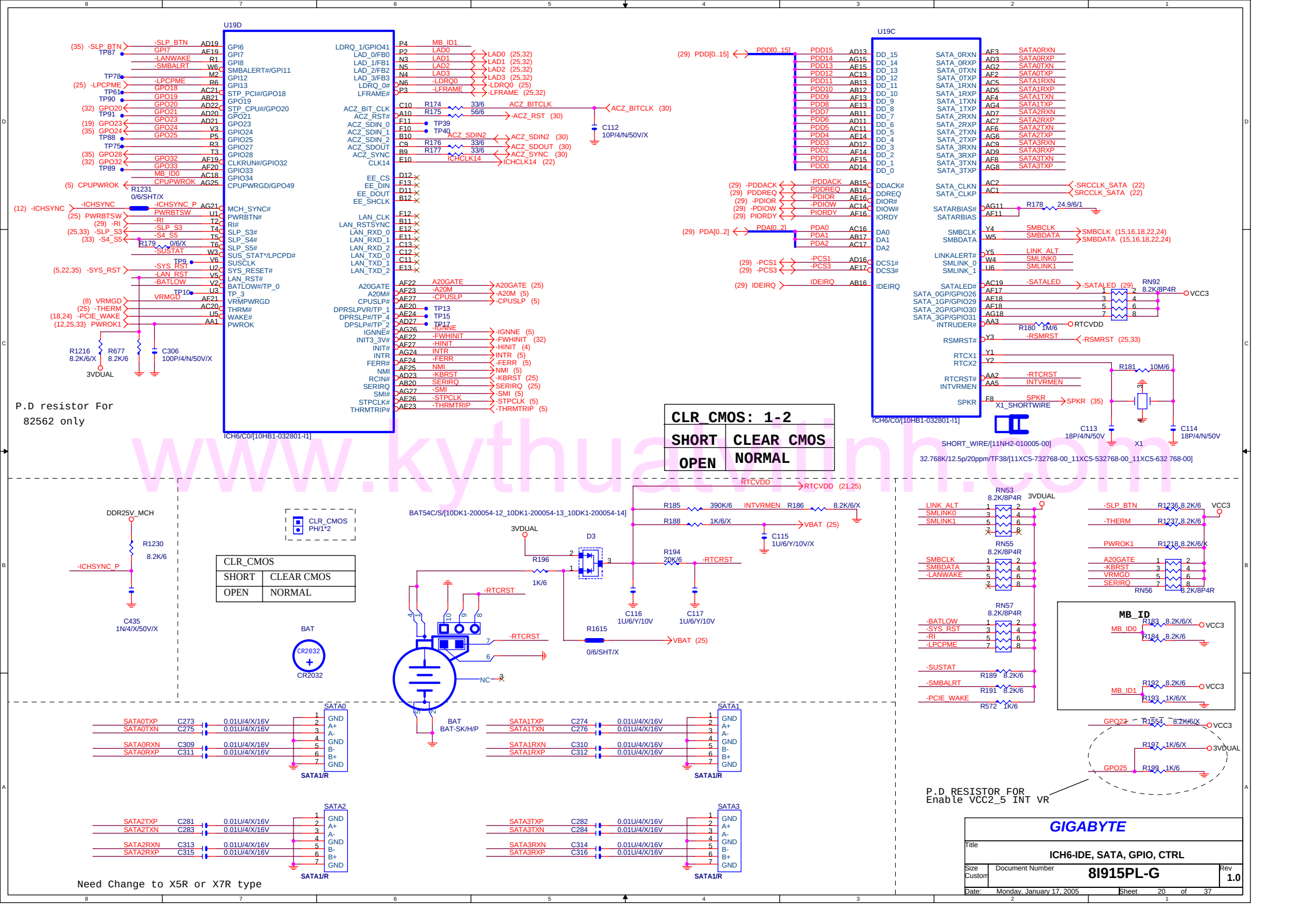
DMI Connection Note
GMCH TX Pin Need Connect to ICH6 RX Pin
ICH6 TX Pin Need Connect to GMCH RX Pin

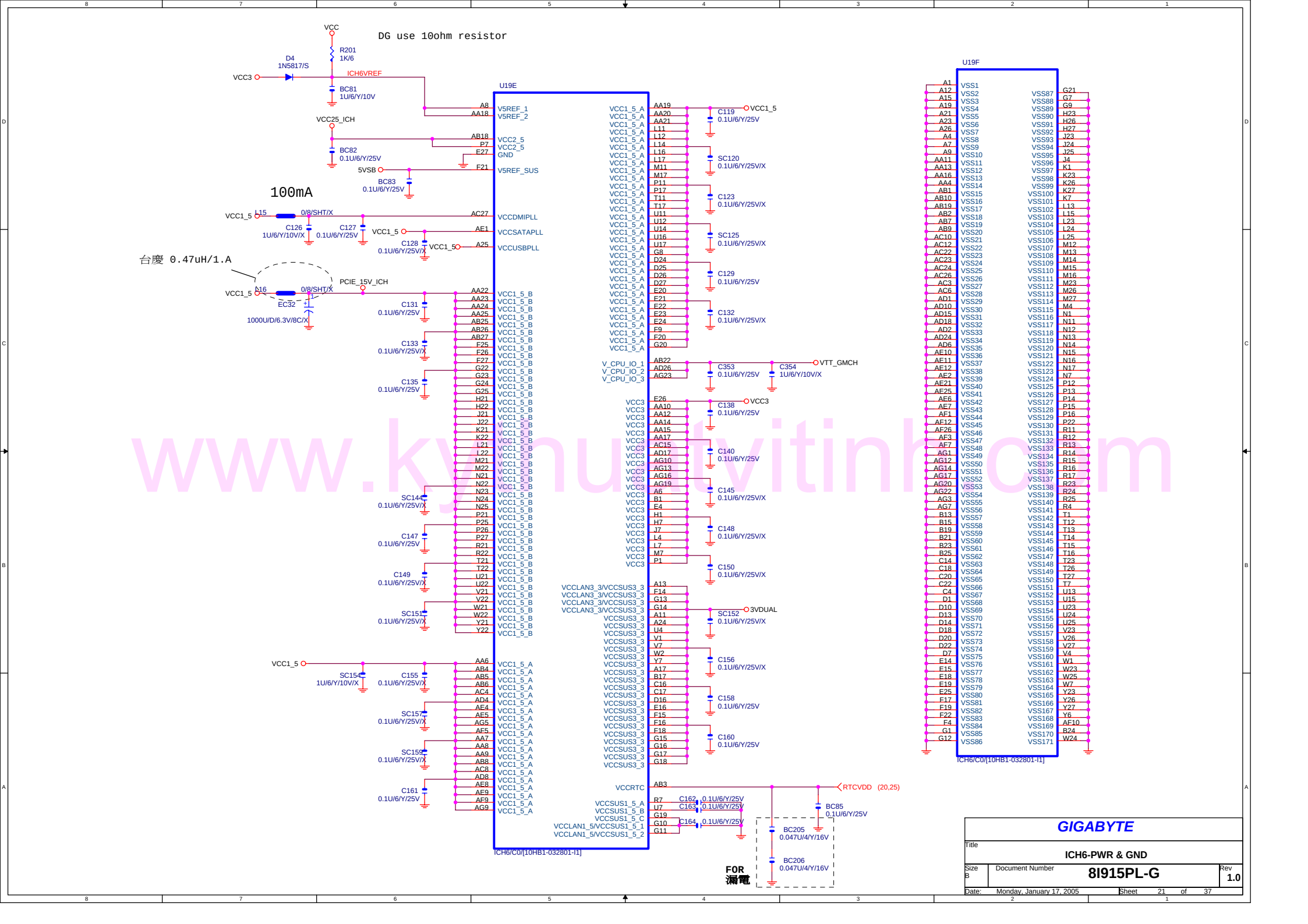


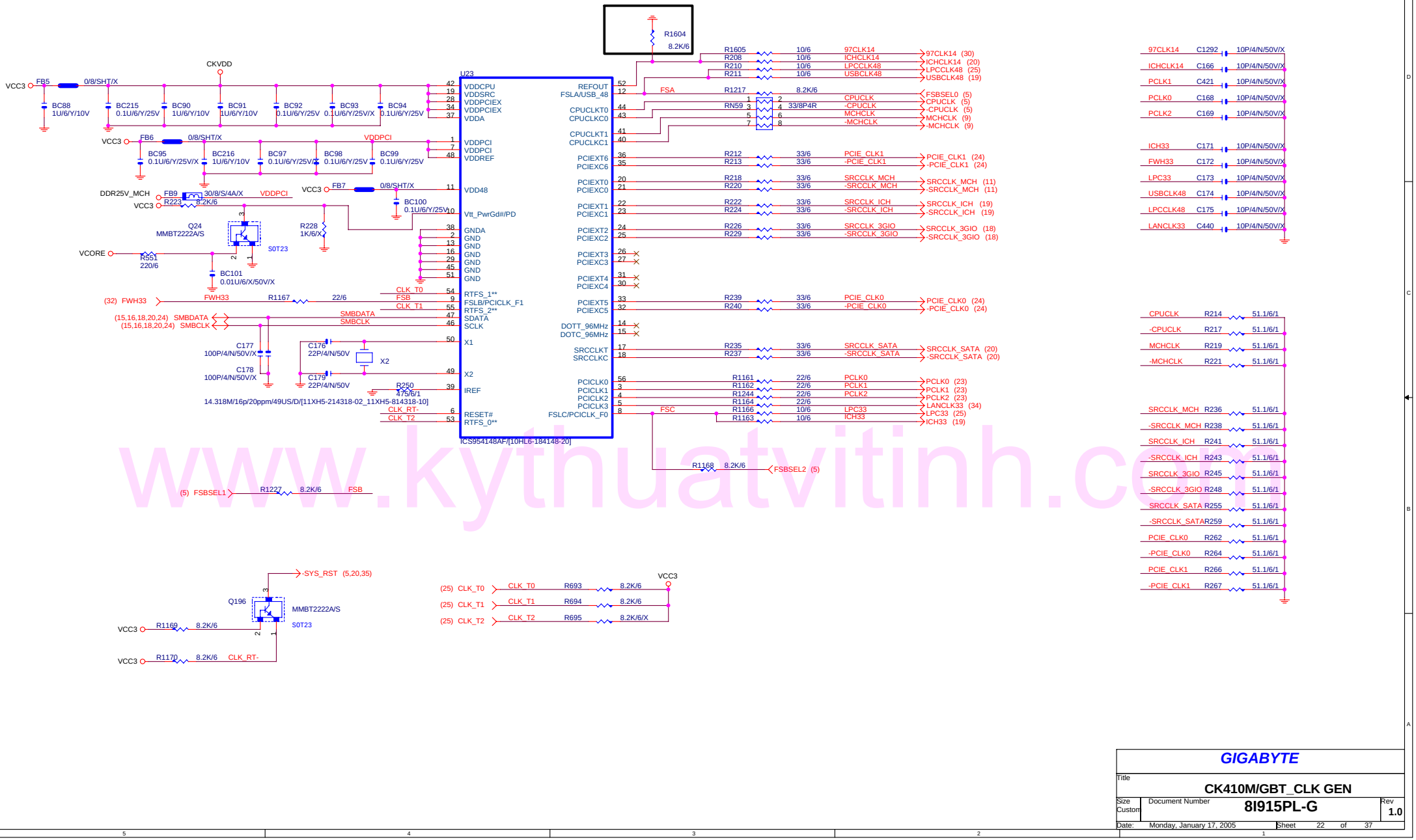




GIGABYTE		
Title: ICH6-PCI, DMI, LAN, USB		
Size: B	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 19 of 37	







GIGABYTE

Title	CK410M/GBT_CLK GEN
Size: Custom	Document Number: 8I915PL-G
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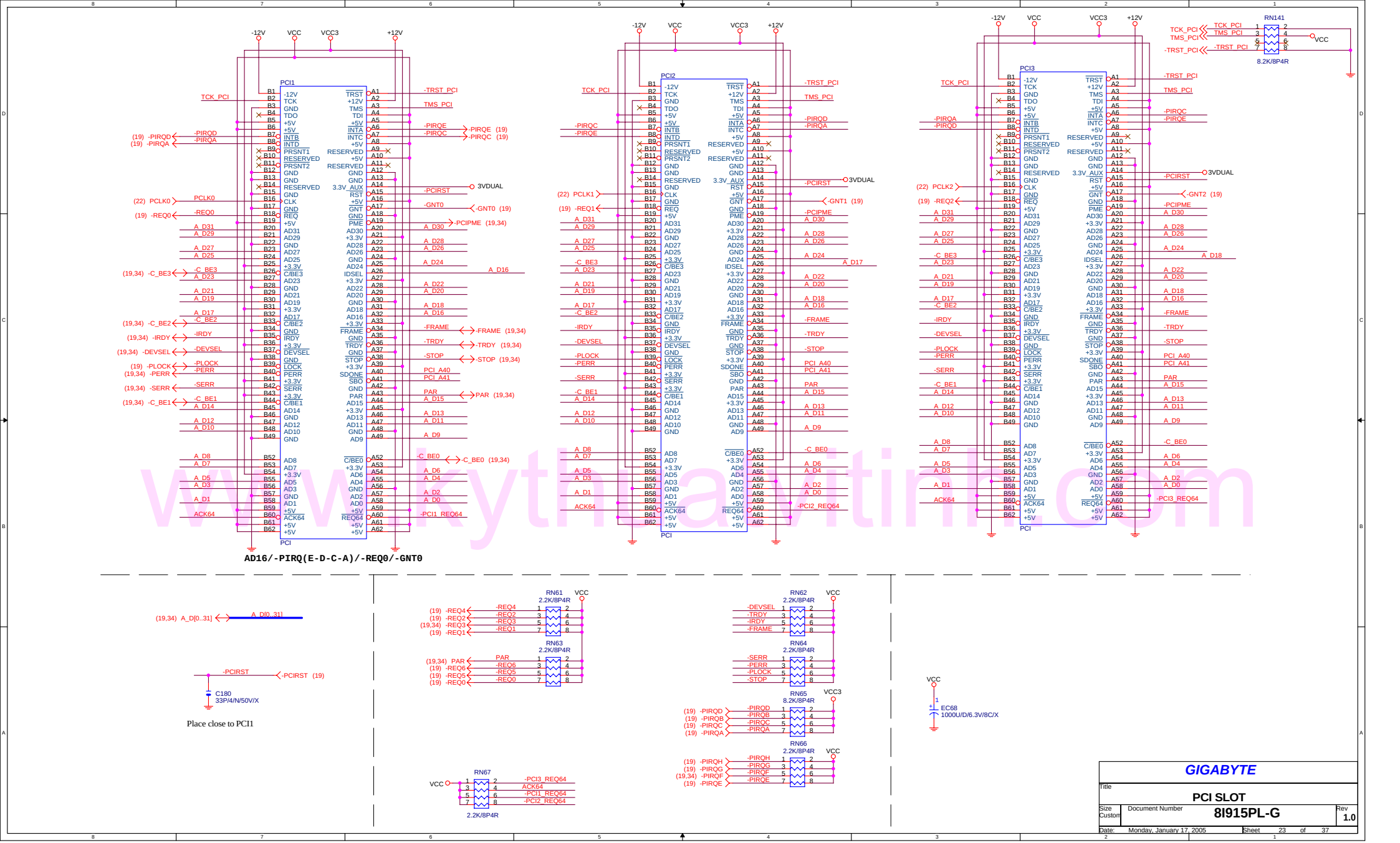
Date: Monday, January 17, 2005	Sheet 22 of 37



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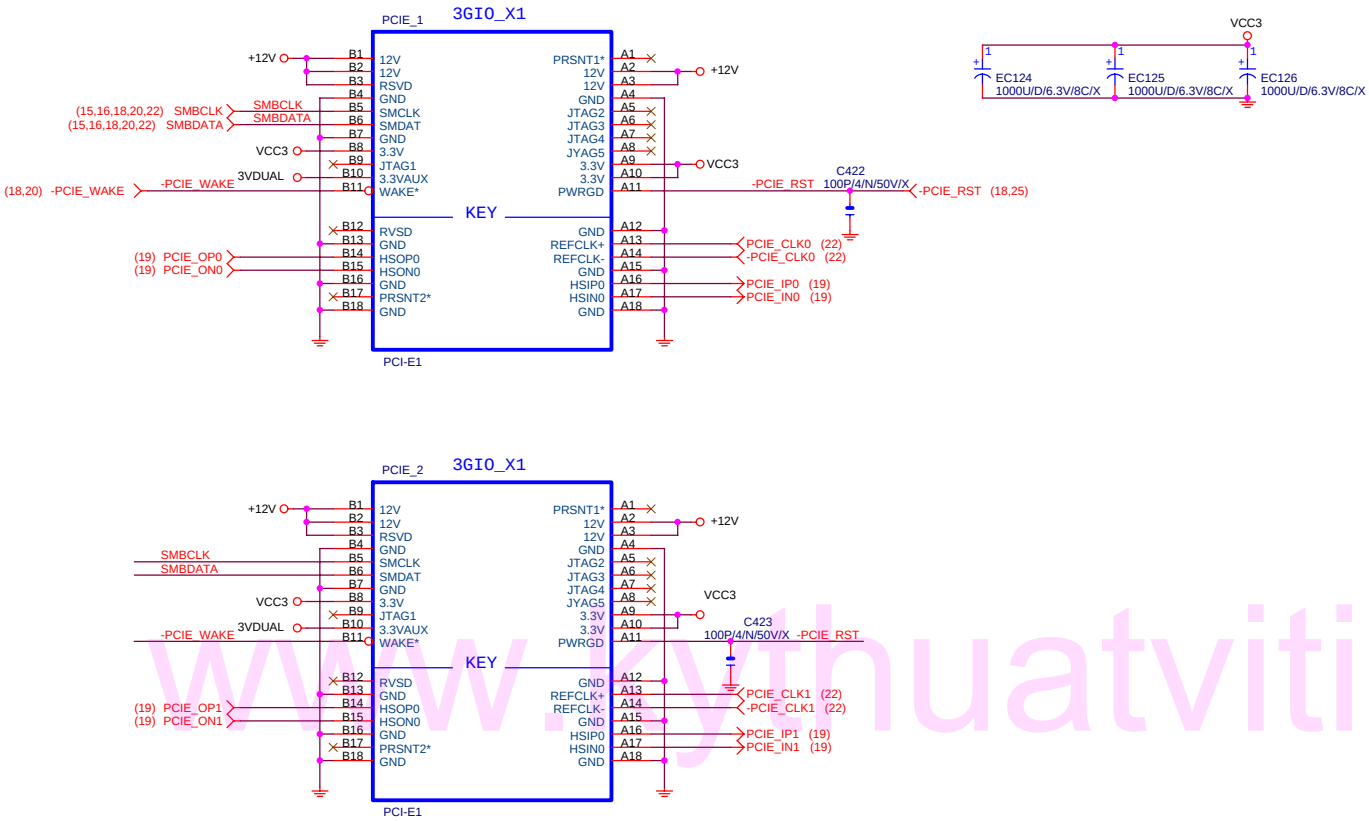
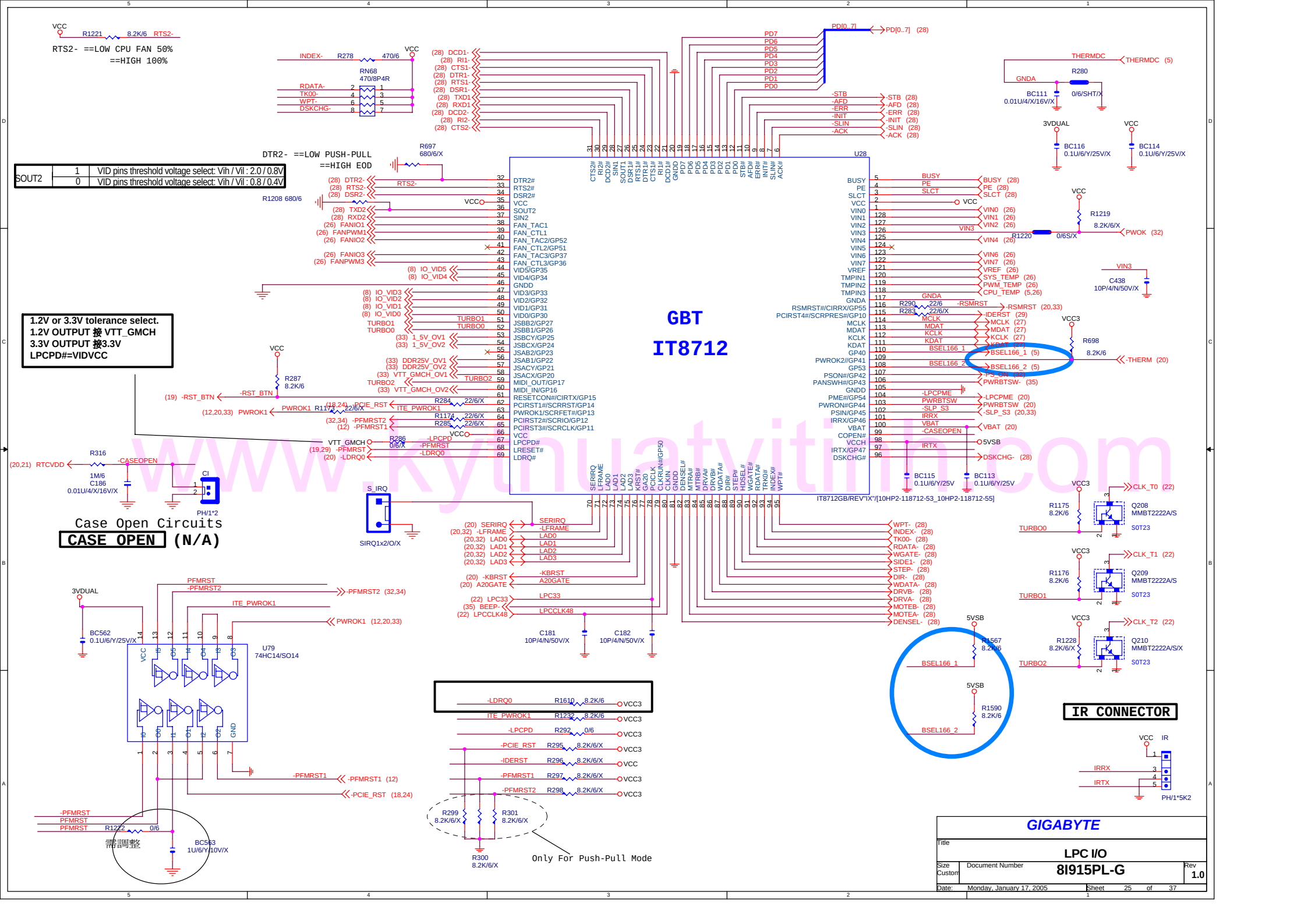
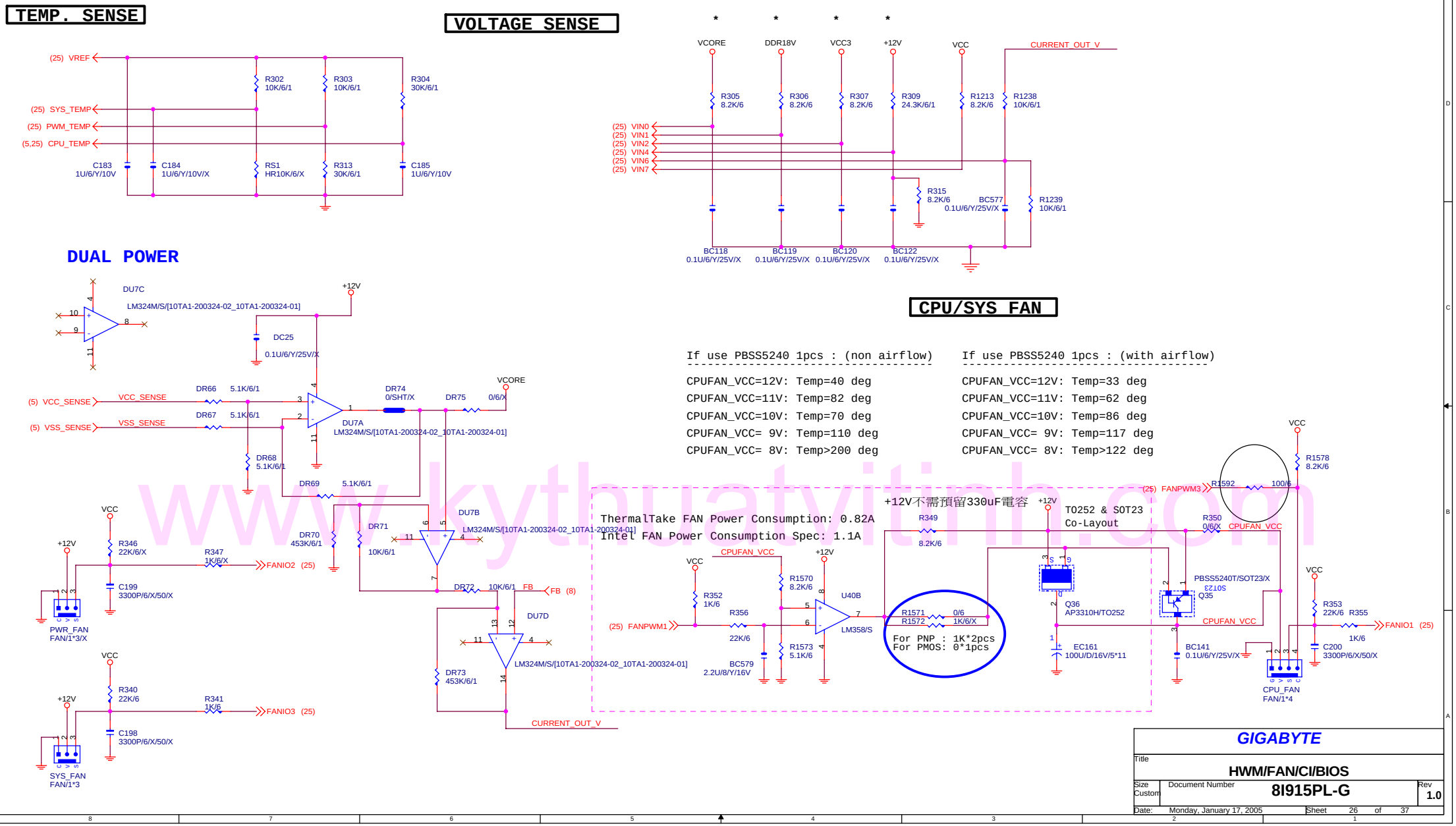
Size: Custom	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 23 of 37	

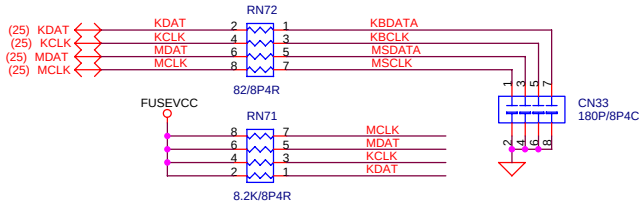


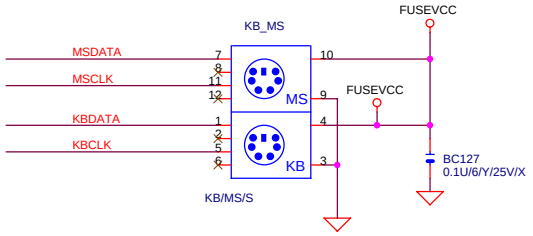
GIGABYTE		
Title: PCI E SLOT		
Size: B	Document Number: 8I915PL-G	Rev: 1.0
Date: Monday, January 17, 2005	Sheet 24 of 37	


RTS2- ==LOW CPU FAN 50%
==HIGH 100%
DTR2- ==LOW PUSH-PULL
==HIGH EOD
SOUT2
1 VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
0 VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V
1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接3.3V
LPCPD#=VIDVCC
GBT
IT8712
IT8712GB/REV"IX"/[10HP2-118712-53_10HP2-118712-55]
Case Open Circuits
CASE OPEN (N/A)
IR CONNECTOR
Only For Push-Pull Mode
需調整
GIGABYTE
LPC I/O
8I915PL-G
Monday, January 17, 2005

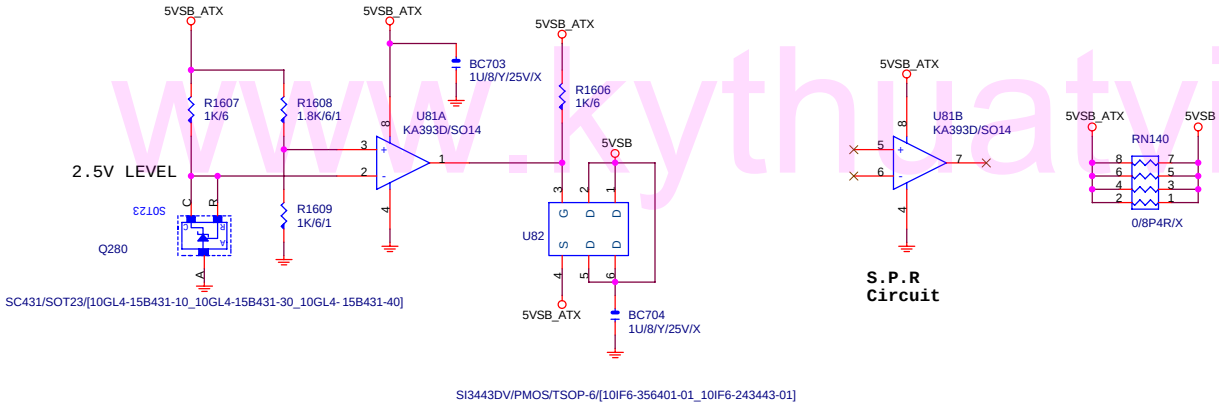


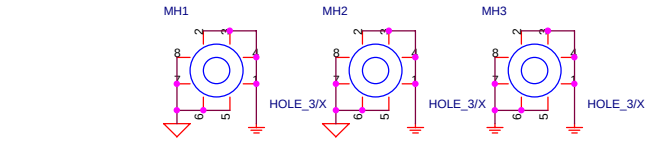
KB/MS

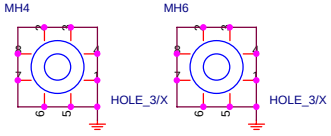


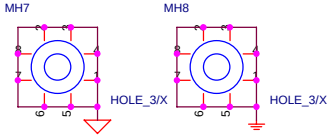


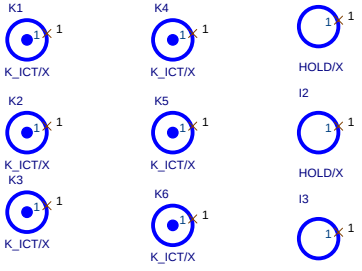
S.P.P.











GIGABYTE		
Title: PS/2 KB & MS		
Size: B	Document Number: 8I915PL-G	Rev: 1.0
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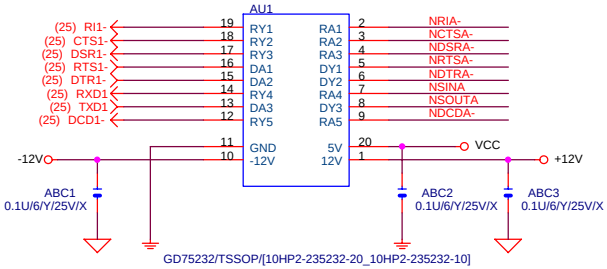
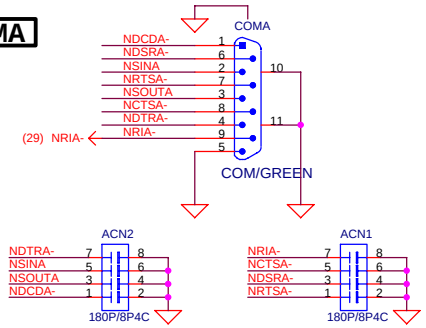
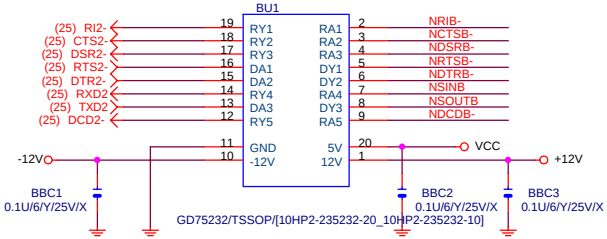
COMA/COMB

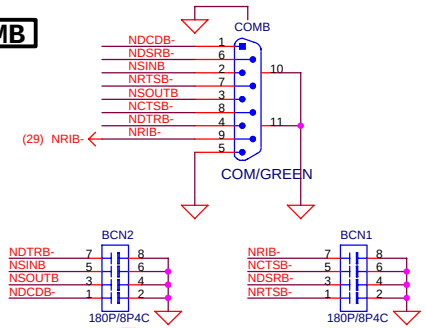


COMA

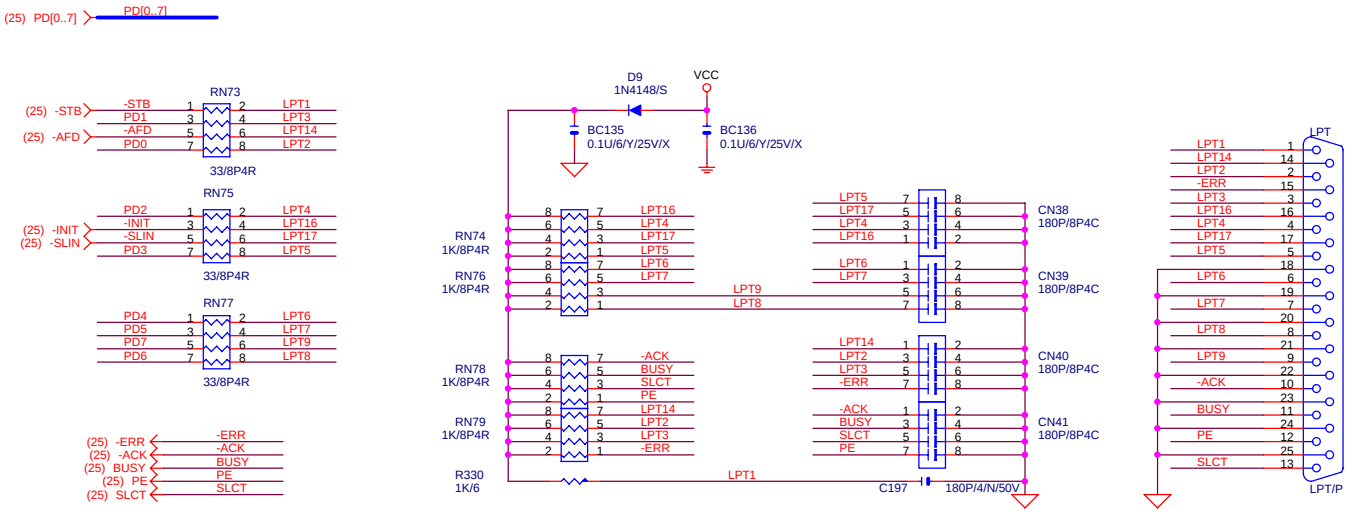


COMB

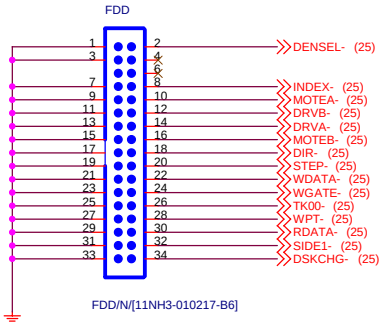




LPT



FLOPPY



GIGABYTE		
Title: COM, LPT, FDD		
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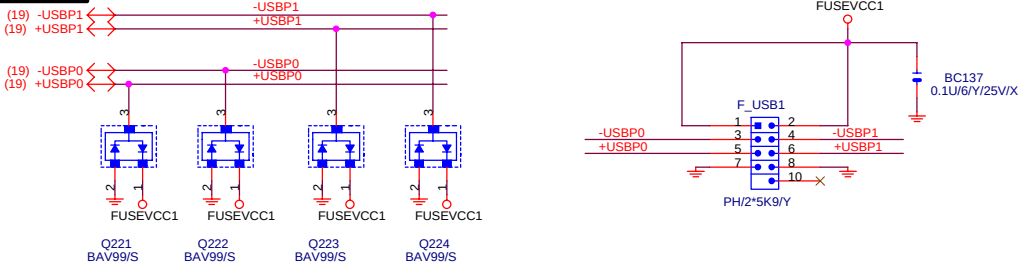
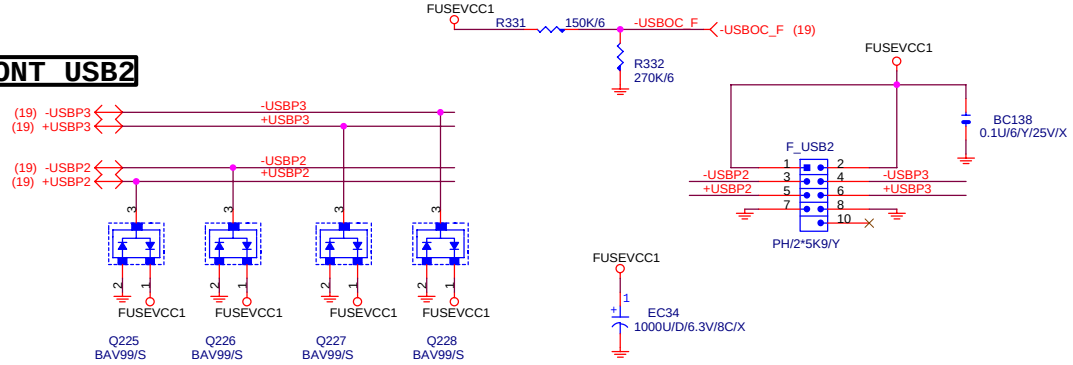
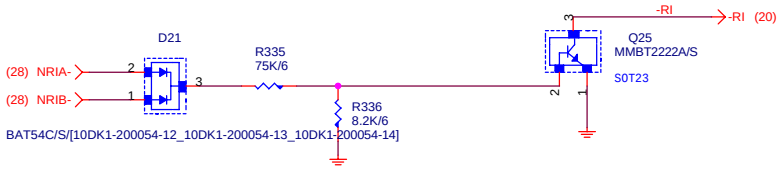
FRONT USB1



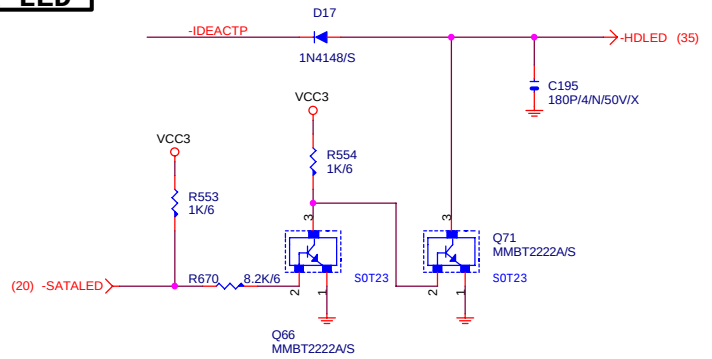
FRONT USB2



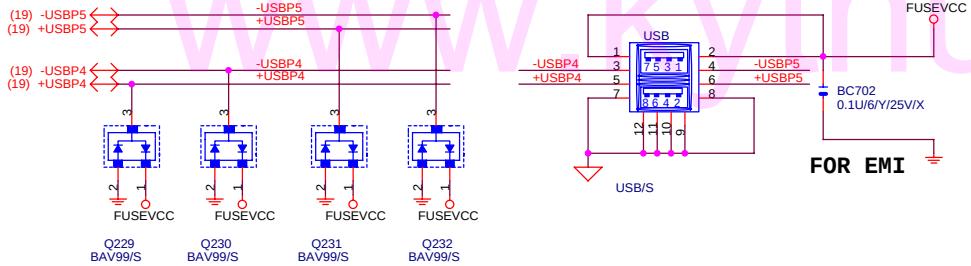
RING IN



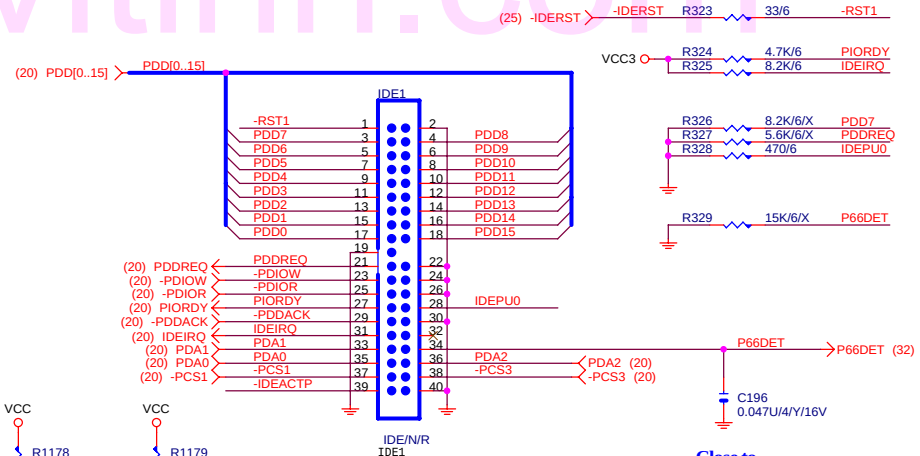
IDE/SATA LED



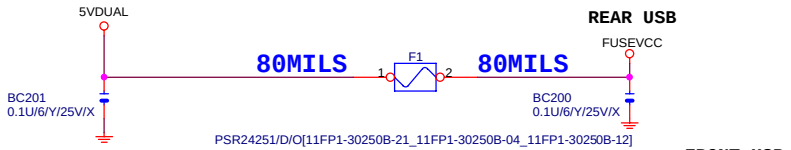
FUSEVCC,GAMEVCC



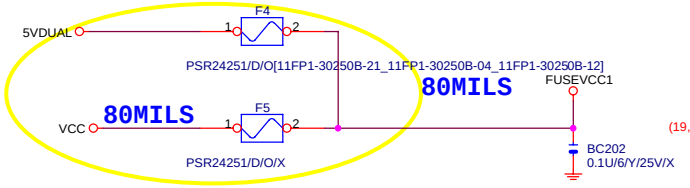
IDE



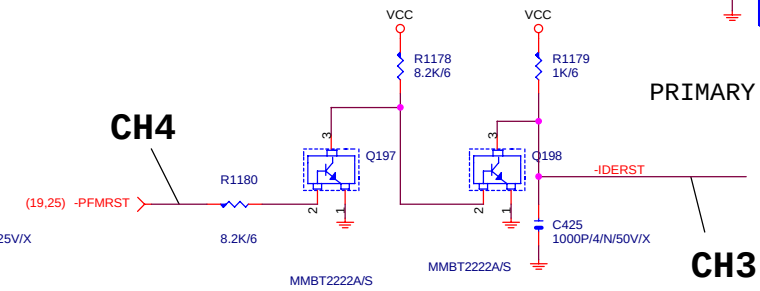
160MILS



FRONT USB



CH4



GIGABYTE		
Title: FRONT/REAR USB CONNECTOR/IDE		
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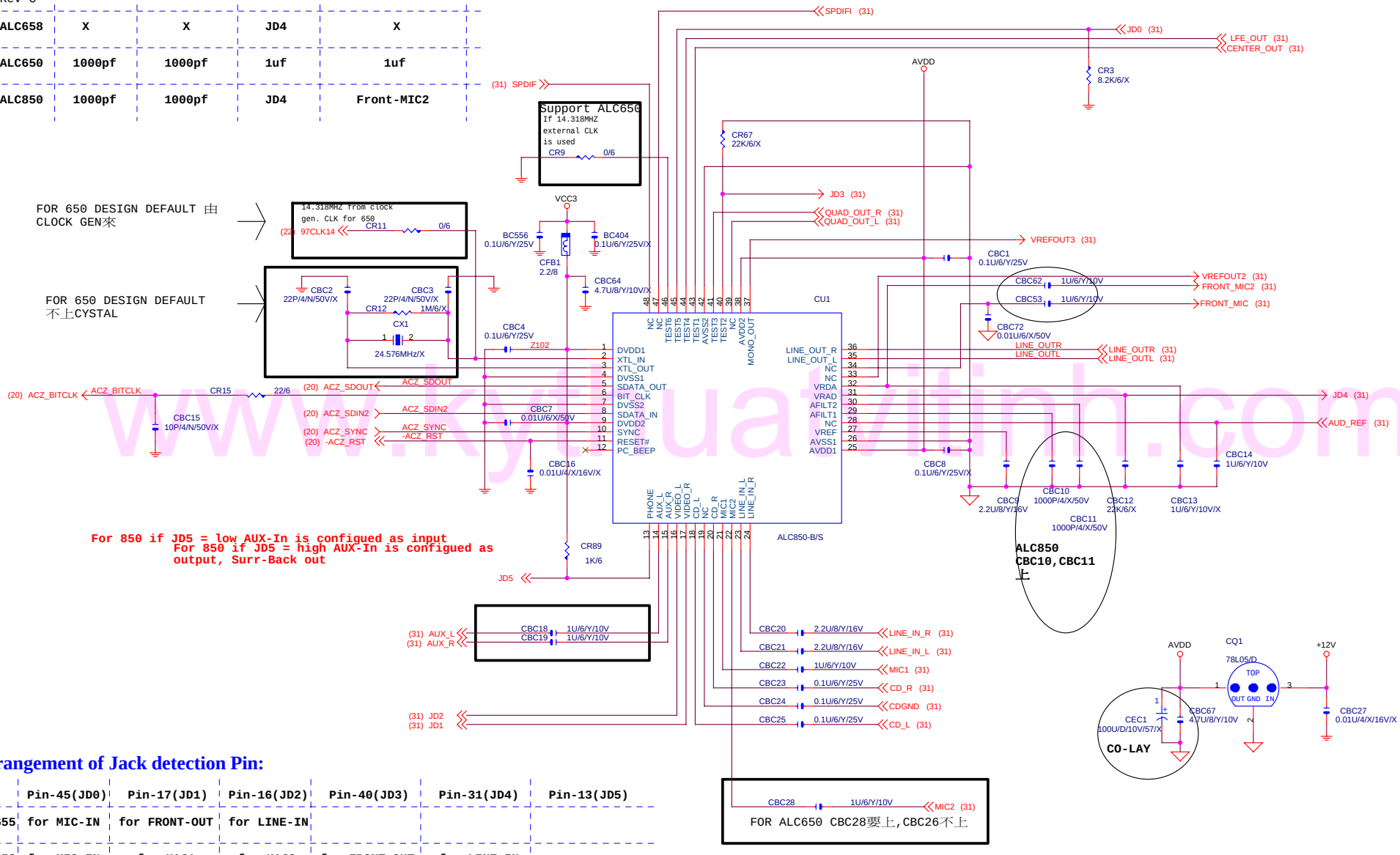
Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2

CR32 2.2/6

FOR EMI REQUEST

BETWEEN AUDIO1 & USB_LAN IN COMPONENT SIDE



For 850 if JD5 = low AUX-In is configued as input
For 850 if JD5 = high AUX-In is configued as output, Surr-Back out

Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT Exernal pull high is needed	for LINE-IN Exernal pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

For 850 if JD5 = low AUX-In is configued as input
For 850 if JD5 = high AUX-In is configued as output, Surr-Back out

GIGABYTE CORP.	
Title	ALC850
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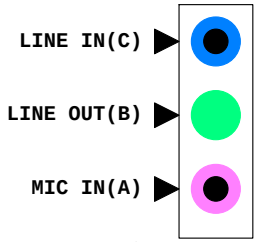
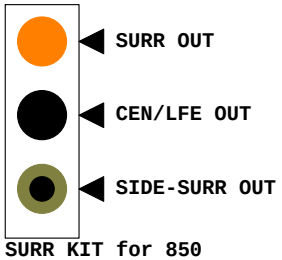
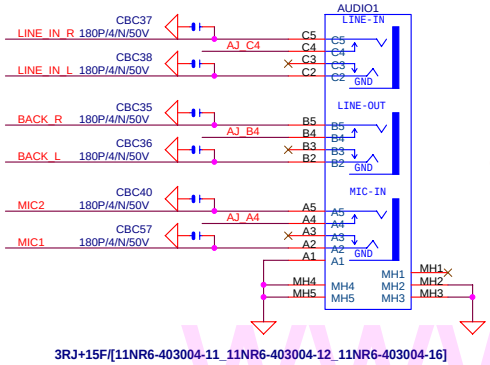


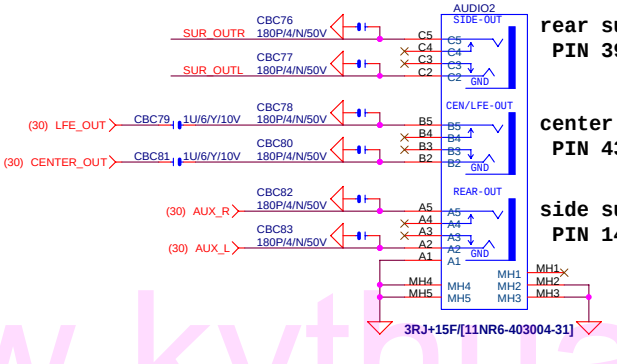
AUDIO PANEL
AUDIO1



SURR KIT for 850
AUDIO2



3RJ+15F/[11NR6-403004-11_11NR6-403004-12_11NR6-403004-16]

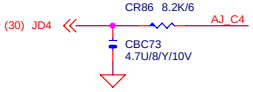


3RJ+15F/[11NR6-403004-31]

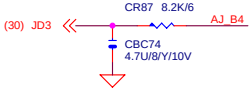
rear surround
PIN 39,41

center
PIN 43,44

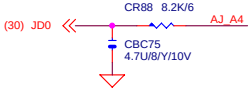
side surround
PIN 14,15



LINE-IN

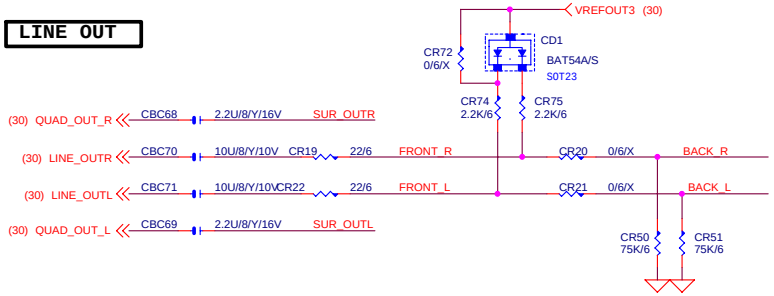


LINE-OUT

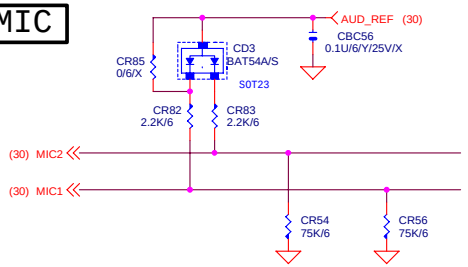


MIC-IN

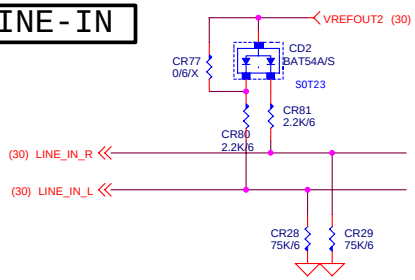
LINE OUT



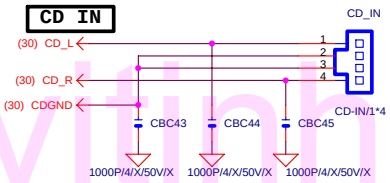
MIC



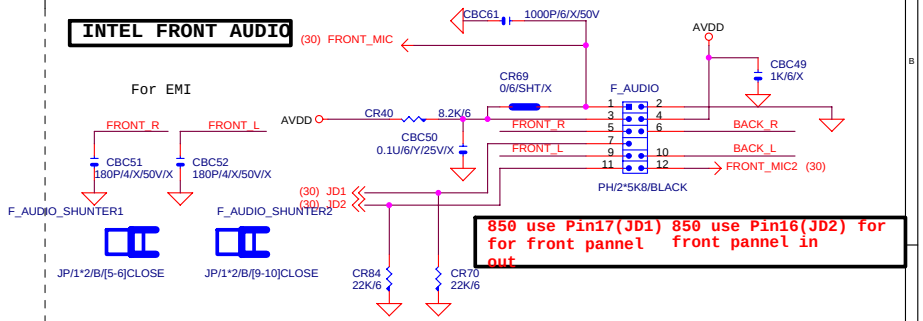
LINE-IN



CD IN

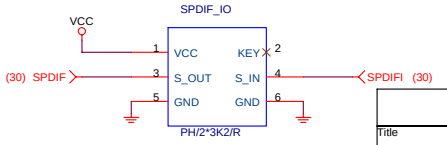


INTEL FRONT AUDIO



850 use Pin17(JD1) for front pannel
850 use Pin16(JD2) for front pannel in out

SPDIF_IO



GIGABYTE CORP.

Title: AUDIO OUTPUT,GAME PORT

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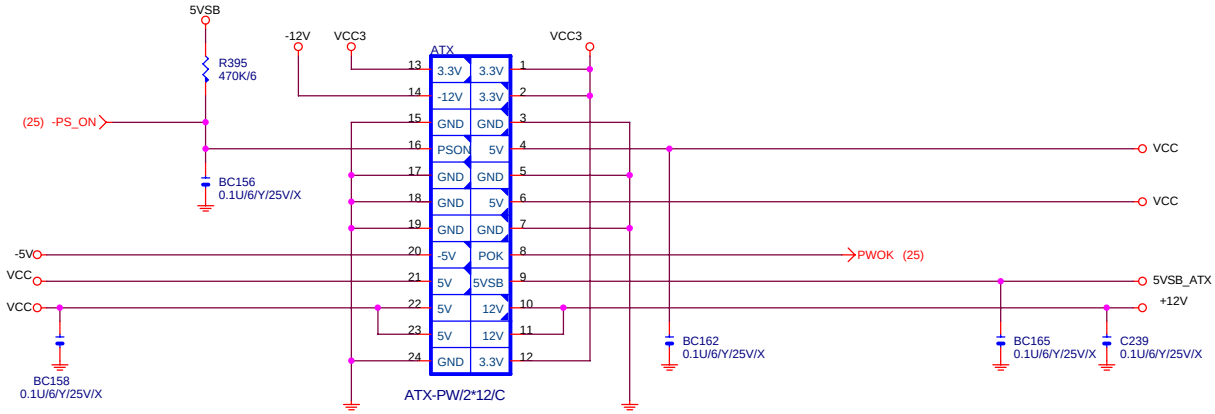
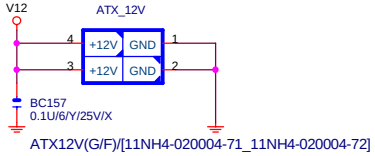
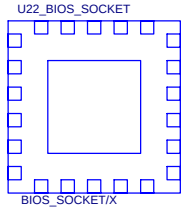
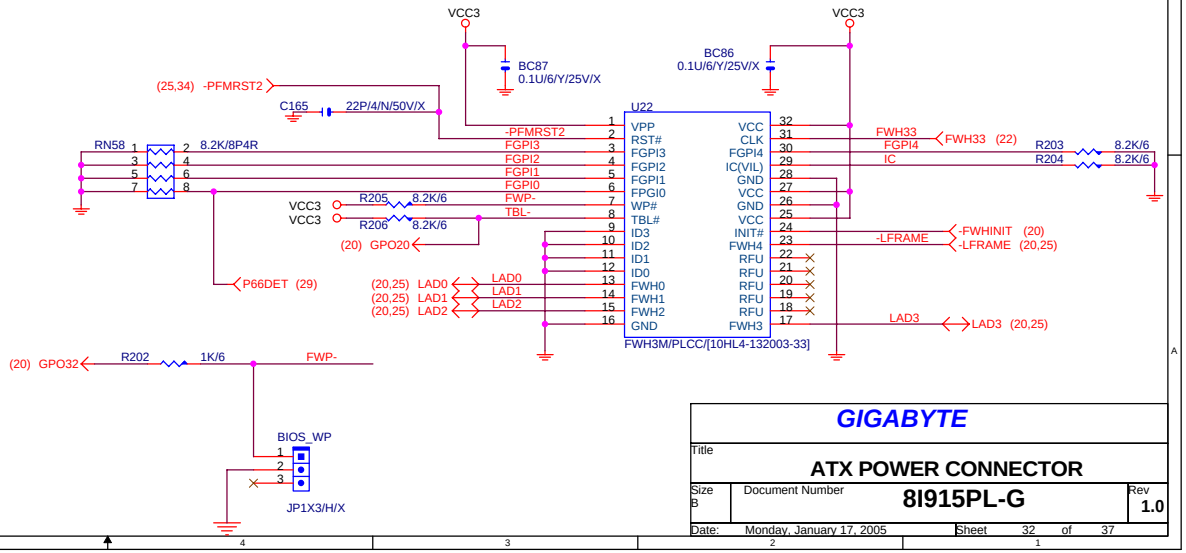
ATX POWER CONNECTOR







FWH BIOS



GIGABYTE		
Title	ATX POWER CONNECTOR	
Size B	Document Number 8I915PL-G	Rev 1.0
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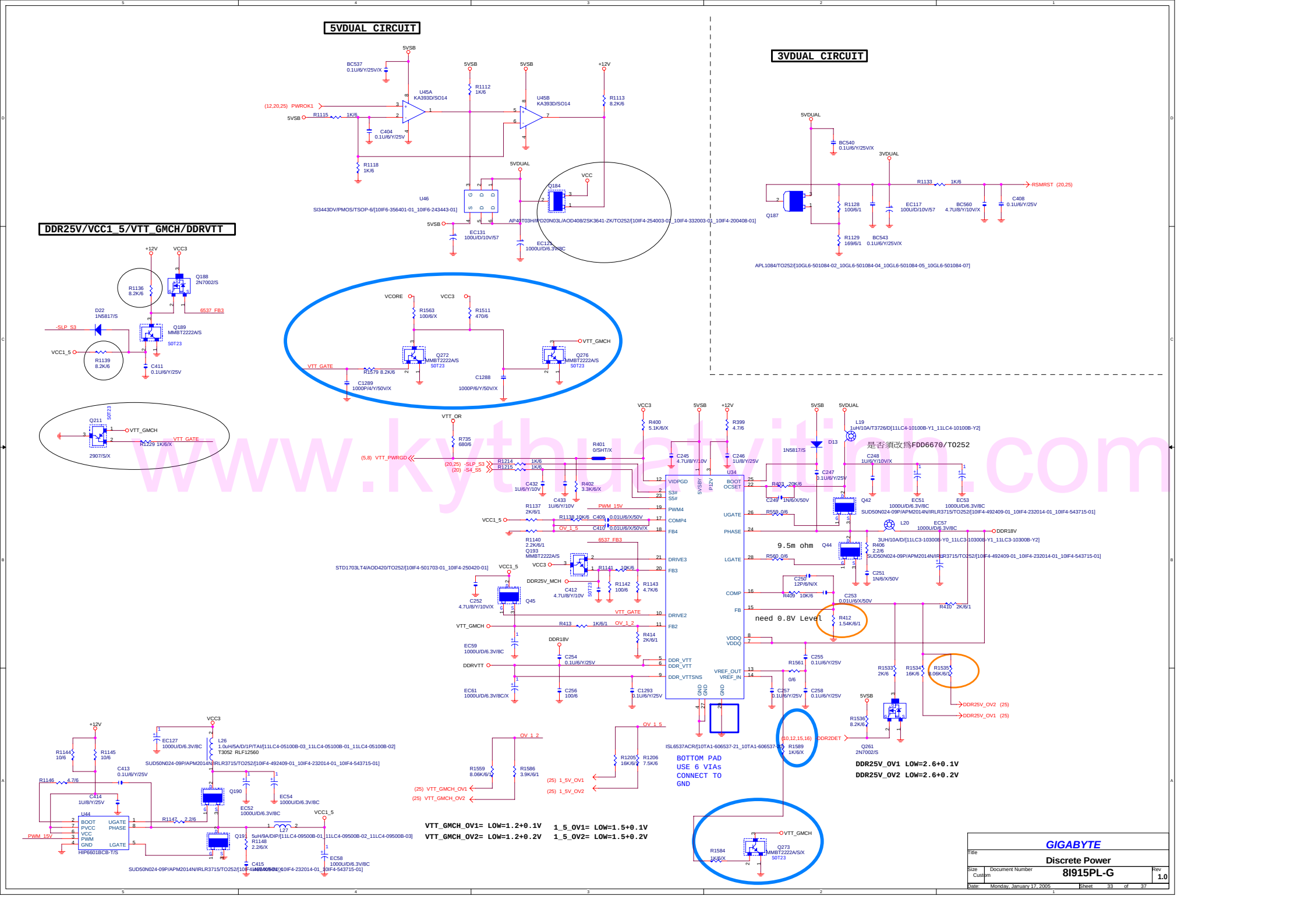

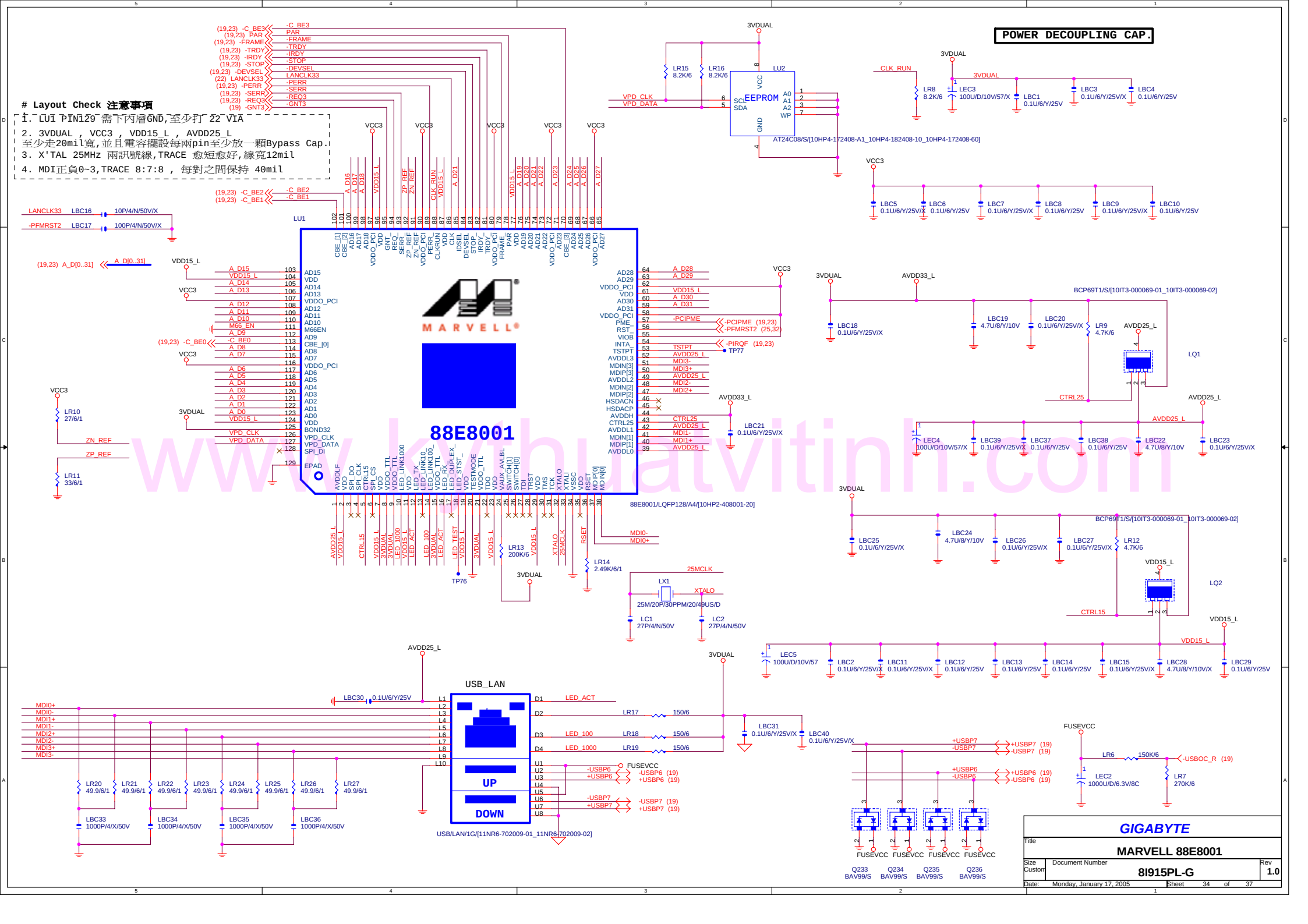
POWER DECOUPLING CAP.
Layout Check 注意事項
1. LU1 PIN129 需下內層GND,至少打 22 VIA
2. 3VDUAL , VCC3 , VDD15_L , AVDD25_L
至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8 , 每對之間保持 40mil
88E8001
88E8001/LQFP128/A4/[10HP2-408001-20]
AT24C08/S/[10HP4-172408-A1_10HP4-182408-10_10HP4-172408-60]
BCP69T1/S/[10IT3-000069-01_10IT3-000069-02]
USB_LAN
USB_LAN/1G/[11NR6-702009-01_11NR6-702009-02]
MARVELL
www.kythuatvitinh.com
GIGABYTE
MARVELL 88E8001
8I915PL-G
1.0
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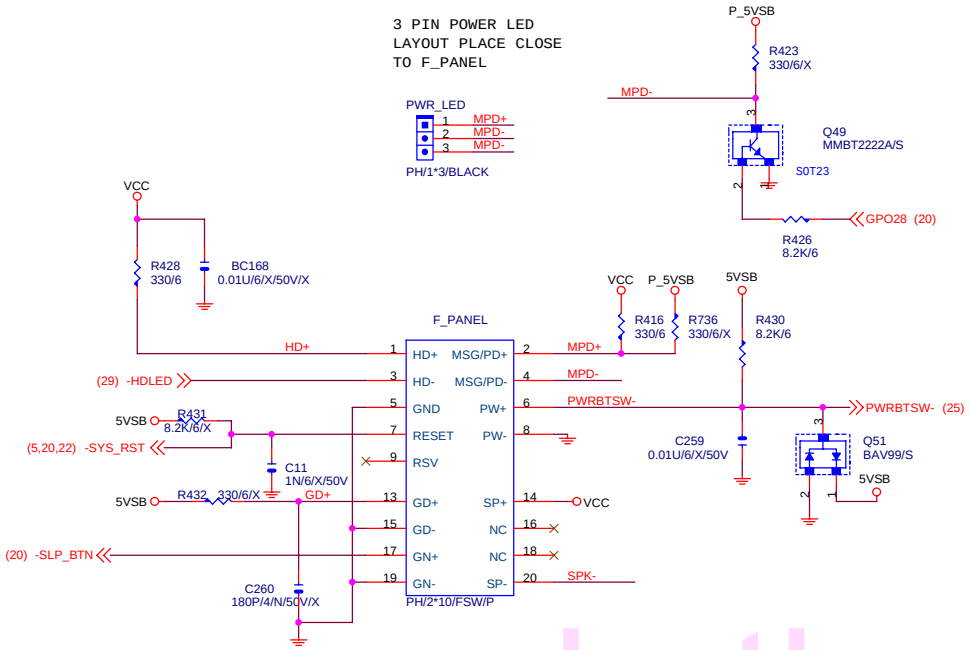
INTEL FRONT PANEL



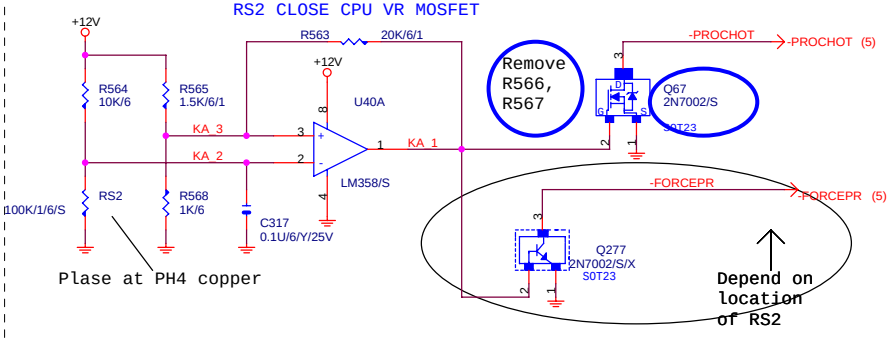
PROCESSOR HOT (N/A)

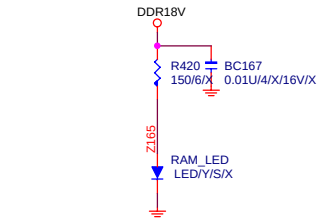
如果要用2N7002需注意OP output
Hi時的電壓是否遠大於2V。

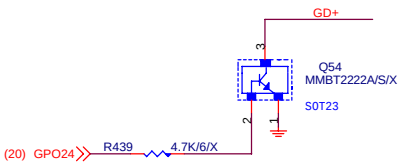
asserted at 130 degree (RS2=720 ohm)
deasserted at 115 degree (RS2=1270 ohm)

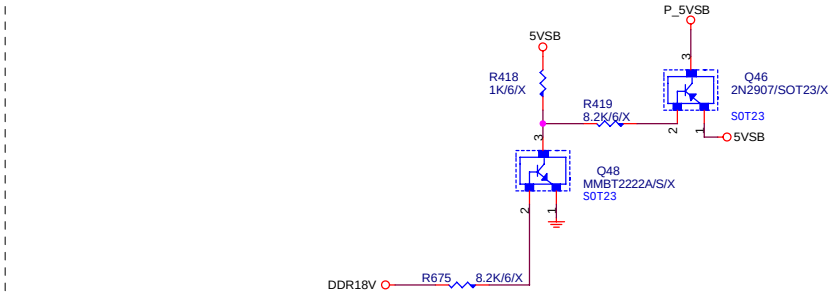
KA393改爲LM358，電源pin改接+12V，Prochot#溫度需重新調整之。

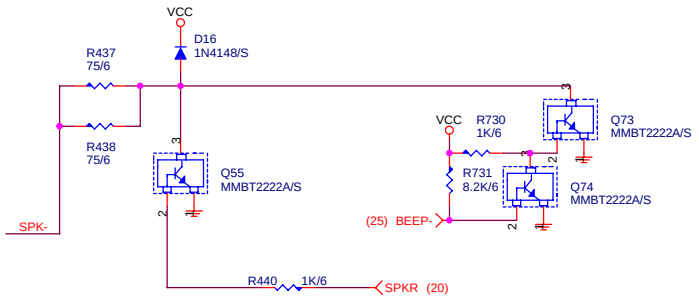
RS2 CLOSE CPU VR MOSFET











States for green LED NO1 GPO22 only S1 PROGRAMMING LOW

LED States	ACPI States	GPO28
ON	S1,S3	0
OFF	S0,S5	1

(GPO22 DEFAULT HIGH, main power)

States for a single-color power LED

LED States	ACPI States	GPO25	GPO27	GPO24
OFF	S1,S3,S5	1	1	NO1
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1

LED States	ACPI States	GPO25	GPO27	GPO22
OFF	S5	1	1	X
Steady Green	S0	1	1	1
Blinking Green	S0(message waiting)	1	B	1
Steady Yellow	S1,S3	1	0	NO1
Blinking Yellow	S1,S3(message waiting)	1	B	NO1

GIGABYTE

Title: FRONT PANEL

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INTEL ICH6 GPIO Implementation

紅字表示CPI/O 同PIN

GPI PIN

Pin Name	Pin Type	Power Well			GPIO Application
GPI[0]	Input	V5REF	-REQ[6]	(P.U VCC)	-REQ[6]
GPI[1]	Input	V5REF	-REQ[5]	(P.U VCC)	Reserved
GPI[5:2]	Input	V5REF	-PIRQ[H:E]	(P.U VCC)	PCI/LAN/NA/1394
GPI[6]	Input	VCC3	GPI[6]	(P.U VCC3)	-SLP_BTN
GPI[7]	Input	VCC3	GPI[7]	(NA)	DUALBIOS_INPUT
GPI[8]	Input	3VDUAL	GPI[8]	(P.U 3VDUAL)	-LANWAKE
GPI[10:9]	Input	3VDUAL	0C_4/5	(P.U 5VDUAL分壓)	-USBOC_R
GPI[11]	Input	3VDUAL	-SMBALERT	(P.U 3VDUAL)	-SMBALRT
GPI[12]	Input	VCC3	GPI[12]	(P.U VCC3)	ATX24_DET
GPI[13]	Input	3VDUAL	GPI[13]	(P.U 3VDUAL)	-LPCPME
GPI[15:14]	Input	3VDUAL	0C_6/7	(P.U 5VDUAL分壓)	-USBOC_R
GPO[16]	OUTPUT	VCC3	-GNT[6]	(integrated VCC3)	Reserved
GPO[17]	OUTPUT	VCC3	-GNT[5]	(integrated VCC3)	Reserved
GPO[18]	OUTPUT	VCC3	GPO[18]	(P.U VCC3)	LANRST-
GPO[19]	OUTPUT	VCC3	GPO[19]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[20]	OUTPUT	VCC3	GPO[20]	(P.U VCC3)	TBL-
GPO[21]	OUTPUT	VCC3	GPO[21]	(P.U VCC3)	DUAL_BIOS_OUTPUT
GPO[22]	Not Implemented		Not Implemented		Not Implemented
GPO[23]	OUTPUT	VCC3	GPO[23]	(P.U VCC3)	LANRST-
GPO[24]	IN/OUT	3VDUAL	GPO[24]	(NA)	GREEN_LED
GPO[25]	IN/OUT	3VDUAL	vcc_25vregulator	(NA)	Reserved
GPI[26]	Input	VCC3	SATA[0]GP	(P.U VCC3)	SATA[0]GP
GPIO[27]	IN/OUT	3VDUAL	GPIO[27]	(NA)	Reserved
GPIO[28]	IN/OUT	3VDUAL	GPO[28]	(NA)	PWD_LED
GPI[29]	Input	VCC3	SATA_1GP	(P.U VCC3)	SATA_1GP
GPI[30]	Input	VCC3	SATA_2GP	(P.U VCC3)	SATA_2GP
GPI[31]	Input	VCC3	SATA_3GP	(P.U VCC3)	SATA_3GP
GPIO[32]	IN/OUT	VCC3	GPO[32]	(NA)	FWP-
GPIO[33]	IN/OUT	VCC3	GPI[33]	(P.U VCC3)	-ACZ_DET
GPIO[34]	IN/OUT	VCC3	GPIO[34]	(P.U VCC3)	MB_ID0
GPI[40]	Input	V5REF	-REQ[4]	(P.U VCC)	-REQ[4]
GPI[41]	Input	VCC3	GPI[41]	(P.U VCC3)	MB_ID1
GPO[48]	OUTPUT	VCC3	-GNT[4]	(integrated VCC3)	Reserved
GPO[49]	OD O	V_CPU_IO	CPUPWROK	(P.U VTT_OR)	CPUPWROK
GP1O[35-39,42-47]	NOT IMPLEMENTED		NOT IMPLEMENTED		

GPO PIN

Pin Name	Pin Number	Power Well	Pin Type			GPIO Application

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ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GPO48	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GPO49	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP_BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX_DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GPO16	VCC3	CPU OV1 (-GNT6)			
GPO17	VCC3	-GNT5			
GPO18	VCC3	CPU OV2			
GPO19	VCC3	DUAL BIOS			
GPO20	VCC3	BIOS T-BLOCK			
GPO21	VCC3	DUAL BIOS			
GPO23	VCC3	DDR OV0			
GPIO24	3VDAUL	GREEN LED			
GPIO25	3VDAUL	DDR OV1			
GPI26	VCC3	SATA_GP0			
GPIO27	3VDAUL	+PWRLED			
GPIO28	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPIO32	VCC3	BIOS WP			
GPIO33	VCC3	AZALIA DET			
GPIO34	VCC3	M/B ID			
GPI40	V5REF	-REQ4			

PWROK/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-PFMRST_ -IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

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