Model Name: 8I915P-D PRO

Revision 2.0

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28	KB_PS2 & IR
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30	FAN CONTROL
31	COM_LPT
32	F_USB & R_USB CONNECTOR
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34	REAR AUDIO JACK
35	FRONT AUDIO JACK
36	Marvell 88E8001 1G LAN
37	TSB43AB23 1394A
38	VCORE POWER (VRD10.1 ISL6556)
39	DISCRETE POWER
40	ATX POWER CONN.

COMPONENT SIDE (1 oz. Copper)
VCC SIDE (1 oz. Copper)
GND SIDE (1 oz. Copper)
SOLDER SIDE (1 oz. Copper)

0.2 PCB Vendor: 育富，祥裕

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Title	Cover Sheet		
Size: Custom	Document Number: 8I915P-D PRO		Rev: 2.0
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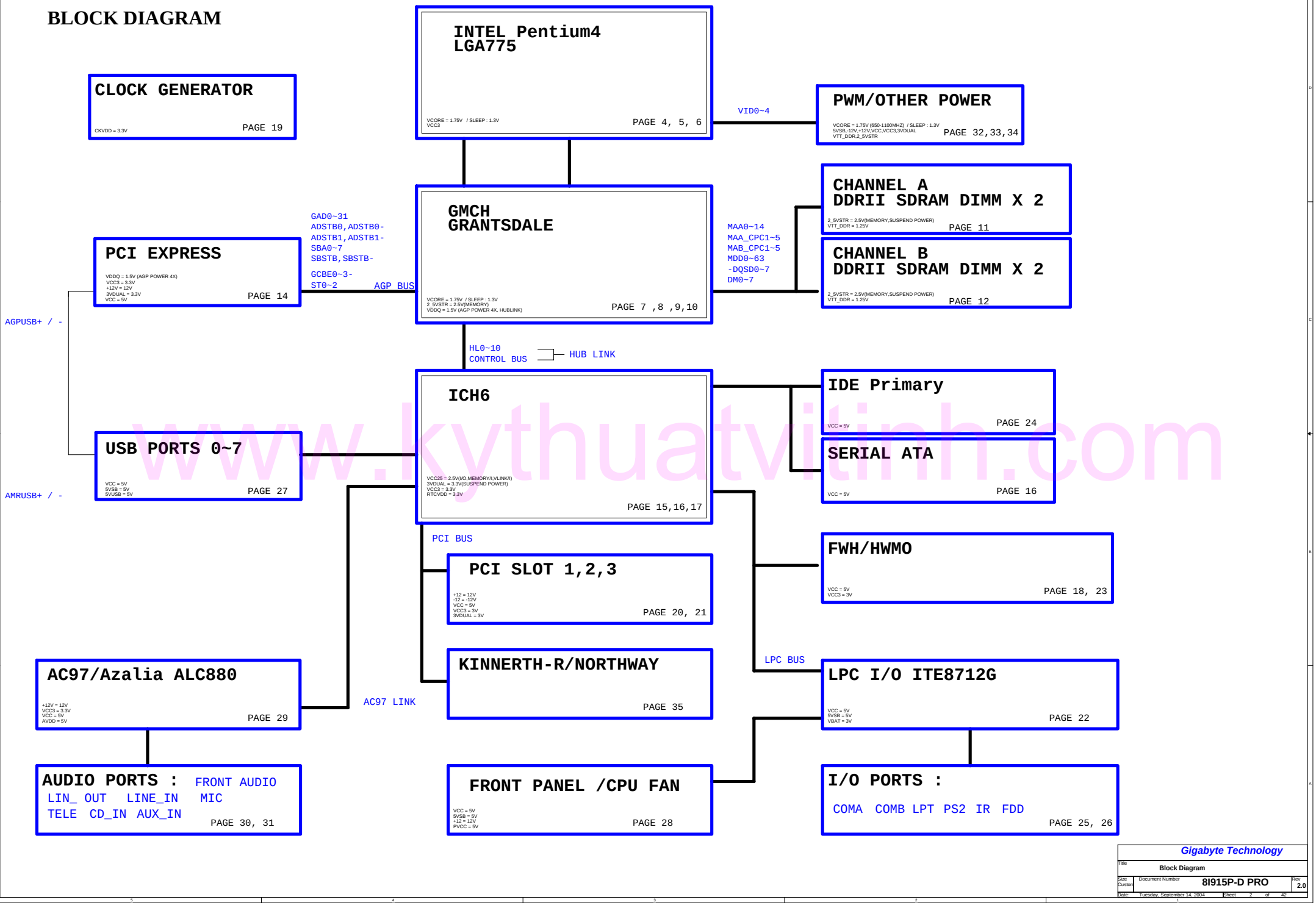
BLOCK DIAGRAM



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Title: Block Diagram

Size: Custom | Document Number: 8I915P-D PRO | Rev: 2.0

Date: Tuesday, September 14, 2004 | Sheet 2 of 42

Model Name: 8I915P-D PRO

Version: 2.0

Component value change history

Data	Change Item	Reason
93.05.10_1.0A	BOM Change from 8I915GDP_10A	
	U78: Phoenix Label, U77: Dual Bios Label	
	FDD6670(Q42,44,45)改9m ohm.	
	SPDIF_IN & OUT remove spring, AZALIA_FP change to Green Color	
	ALC880 Rev.E change to date code 0417 and after	Fix F_AUDIO noise
	Grantsdale-G change to Grantsdale-P	
	add 包材(Manual, Driver,...)	
	DR16 : 2.7K --> 2.2K	For Temperature balance
	NB_HEATSINK改12SP2-04F003-11/12/13	
	12LC2-03DUAL-00 --> 貼在PCI slot上	
93.05.18_1.0B	Remove C37,C38,C39	Remove 915P unused parts
	DDRVTT pull-down 100/6 for ISL6537 issue	For ISL6537 DDRVTT OVP issue.
	Remove R126, R127, R128	For 915P can not boot issue
	Line-out改串10U	For Frequency Response fail issue
	14.318 XTAL change to 22P	For RTC time is not correct issue.
93.05.28_1.0C	Q36加替料P06P03 (10IF4-450603-01)	for AP3310H single source issue.
	RS2改100K(10RH2-001003-21) for 功率問題。	For HR10K 功率不足issue.
	RS2:HR10K-->100K,R564: 1K/6/1-->10K/6/1, R565:1.69K/6/1-->2.32K/6/1	For RS2 功率不足issue
	680/6 from R1523 move to R1562	For CPU not mount Vcore output 7.8V issue.
	U28:IT8712(IX4主料, IX3 替料)	IT8712(IX4主料, IX3 替料)
	10U/12/X5R/16V實驗後改成Y5V	
93.06.01_10D	CPU pull-up from 51 ohm change to 62 ohm	減少零件種類
	R328 mount 470/6	For IDE cable select function
	MB_ID1(-REQ6) pull-up to VCC3	For PCI bandwidth is not enough issue.
	Remove RS1(HR10K)	don't need to detect system temp.
93.06.15_10D _ECN1	Add Color Box Feature & CPU Manual	包材修正

Circuit or PCB layout change for next version

PAGE	Change Item	Reason
93.02.18_0.2	-IO_PSON change to -PS_ON	
	R401與R400文字左右顛倒	
	SB HEATSINK改爲push-pin(RELAYOUT)	
	VTT_PWRGD改接VCC3分壓，不由ISL6537來	
	Remove SATACLK, SRCCLK_LAN trace & parts	
	Remove ACK64, PCI_A40,PCI_A41,GPO25,-LANWAKE ,-smbalrt,ATXGPO0,S66DET module port	
	invert DELAY1 and connect to DUAL_BIOS_DELAY	
	Add BAV70 for -NRIA & -NRIB enable -RI	
	Add 8.2K/6 between U24.12 and FSBSEL0	
	Rear FUSEVCC加寬, SB: VCC1_5銅箔修改	
	Vcore Power, Clock Gen, Reset circuit modify	
93.03.23_0.3	Vcore電感改DIP, MOS上1下2	
	VCC_SENSE與VSS_SENSE之間預留電容於CPU socket右邊	
	PCI test pin分別接GND與VCC	
	增加Turbo pin function (DU6), And Linear FAN control	
	U13: 74HCT32 change to IC14SOIC package	
	CPU socket內改成4個SP-CAP與10個1206電容共layout	
	Marvell LAN之電容位置修改, 5VDUAL整組移到ATX右方	
	北橋Grantsdale文字錯誤, PWROK1斷線修正	
	FB5~FB7 change to 0603	
	F2，EC35，IEC2, IEC3 卡到PCI2 長卡	
	CD_IN反轉180度，並略向下移	
	5VDUAL整組移到ATX右方	
1.0	Audio改後6，remove GAME, Add COMA(2x5)	
	VGA_COM改爲與COMA Co-Layout	
	F1向左上方移位以免折斷	
	加5VDUAL 1000U電容於L19左側	
	EC156 100U DIP/SMD共layout	
	4-wire FAN FANPWM3 add damping resistor 100 ohm.	For ITE chip burn-out issue.

Gigabyte Technology

Title: BOM & PCB MODIFY HISTORY

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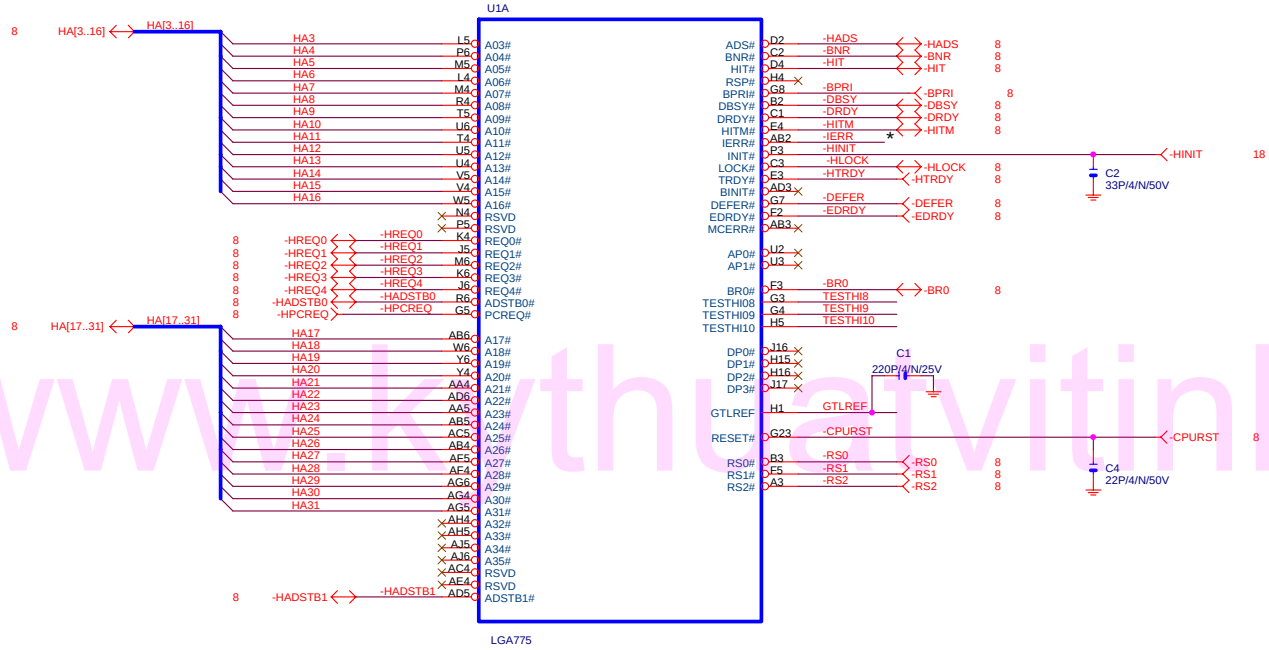
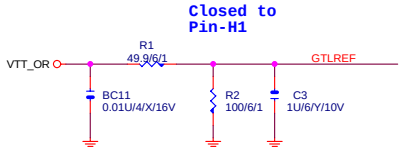
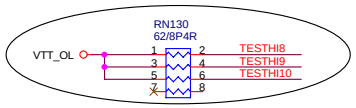
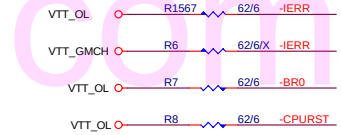
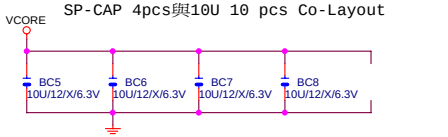
Date: Tuesday, September 14, 2004 | Sheet 3 of 42

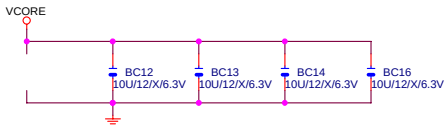


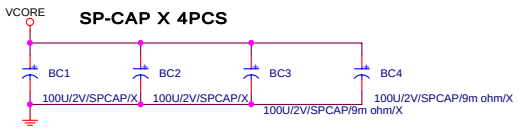


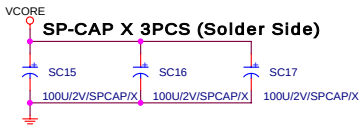


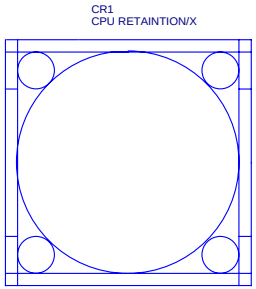












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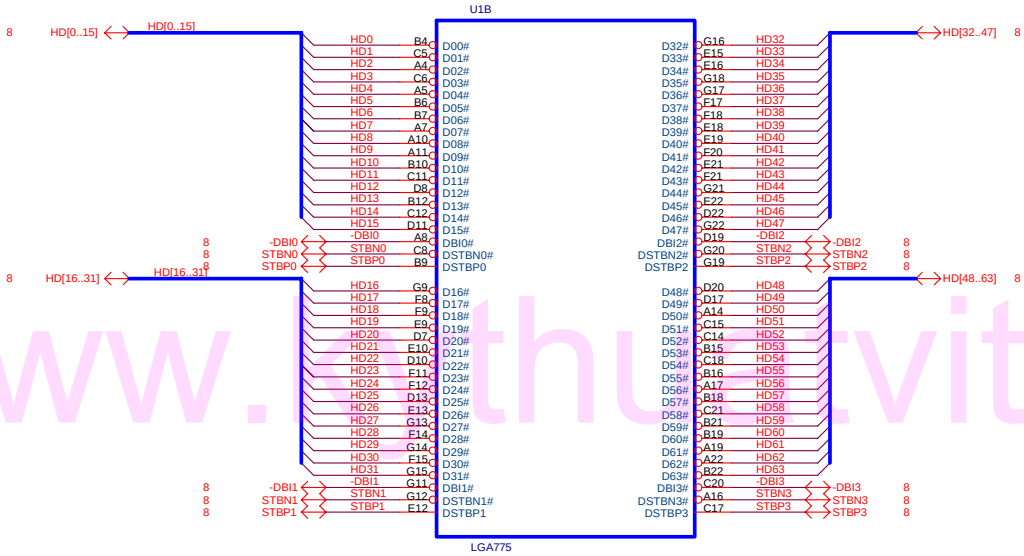

Gigabyte Technology			
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Size: Custom	Document Number: 8I915P-D PRO		Rev: 2.0
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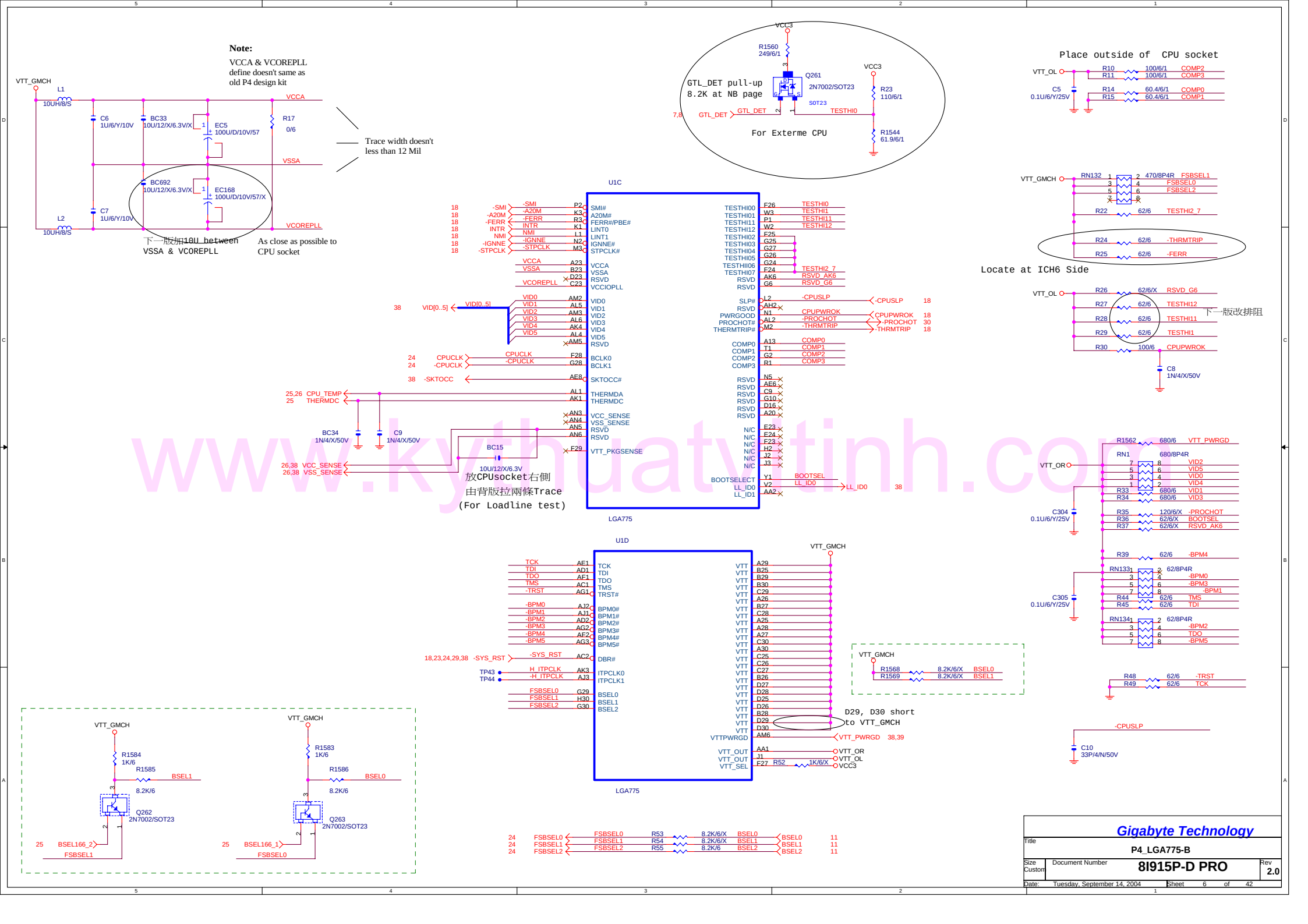

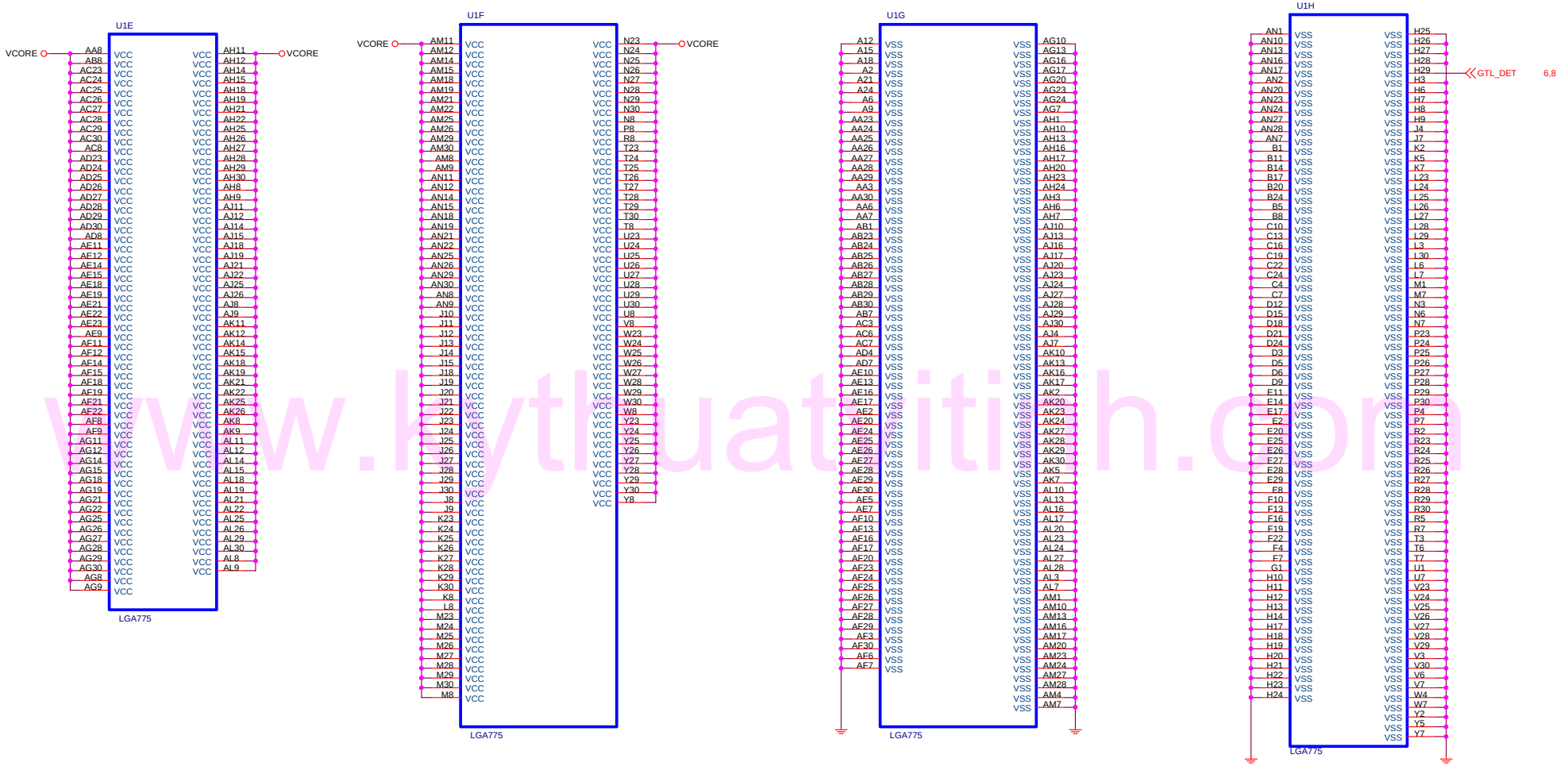

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Size: Custom	Document Number: 8I915P-D PRO		Rev: 2.0
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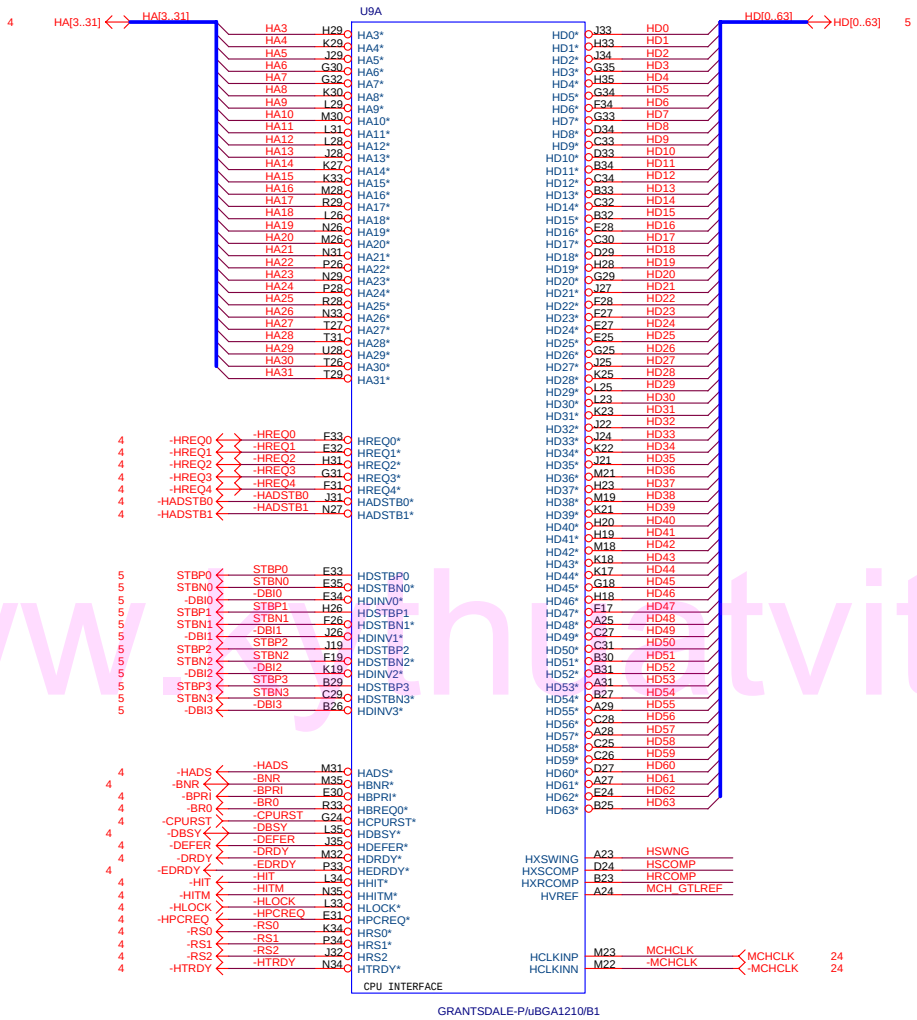

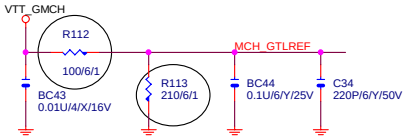

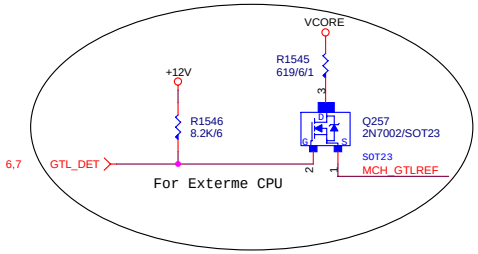

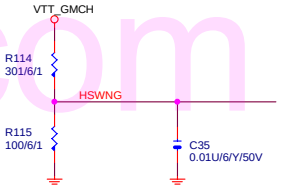

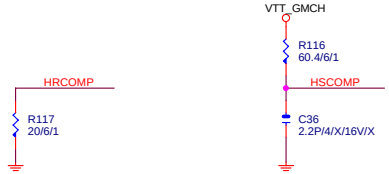

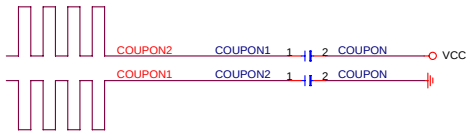

Title	GMCH-HOST
Size / Custom	Document Number: 8I915P-D PRO
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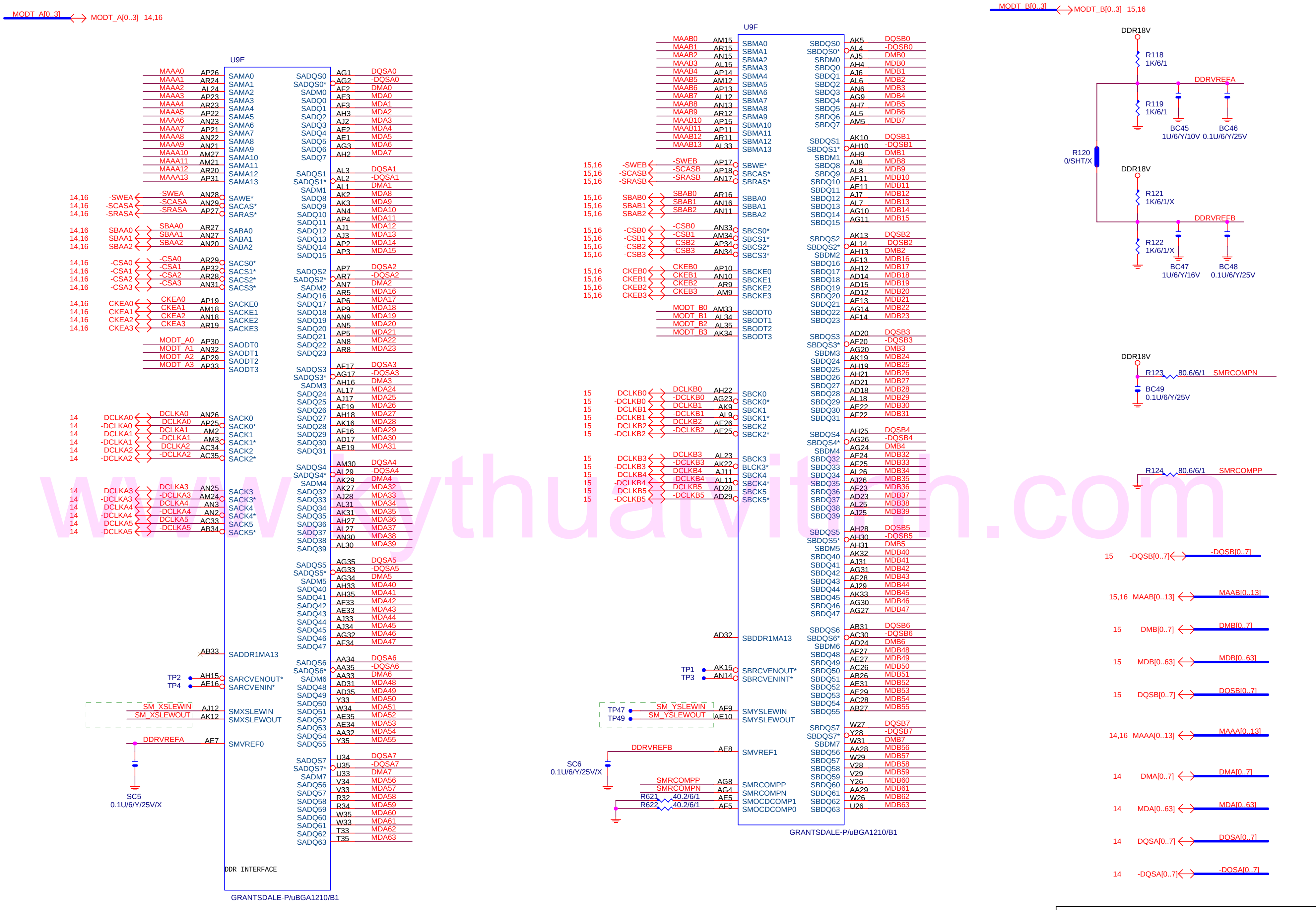
Gigabyte Technology



Gigabyte Technology

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Size	Document Number	Rev
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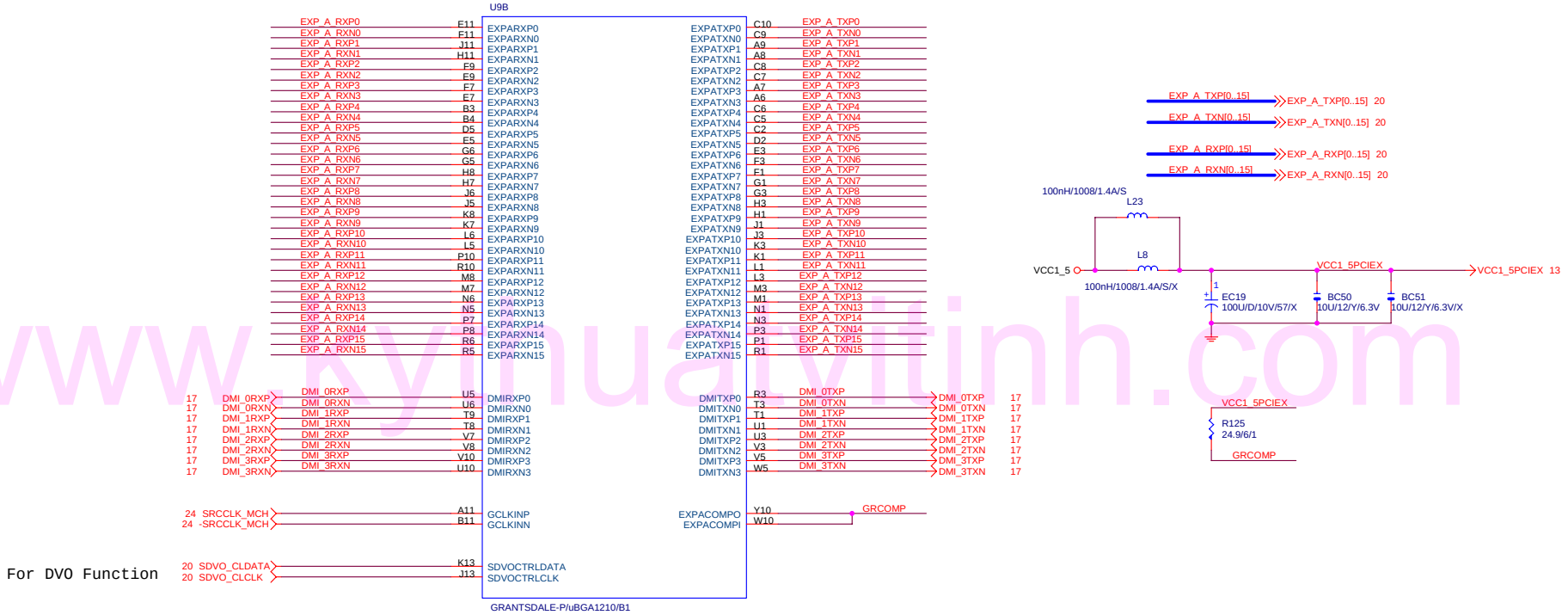

Gigabyte Technology		
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Size: Custom	Document Number: 8I915P-D PRO	Rev: 2.0
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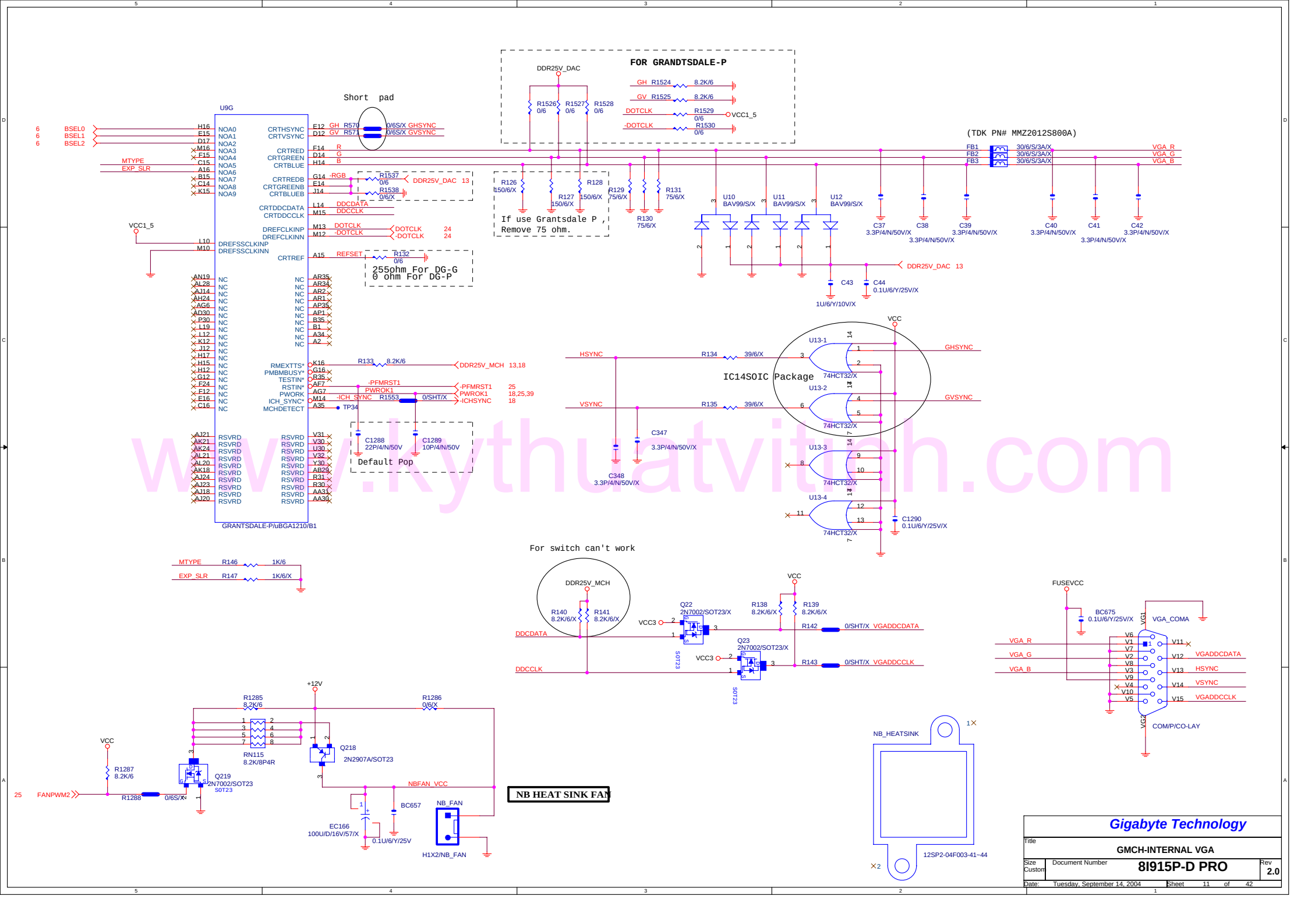

Gigabyte Technology	
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Size: Custom	Document Number: 8I915P-D PRO
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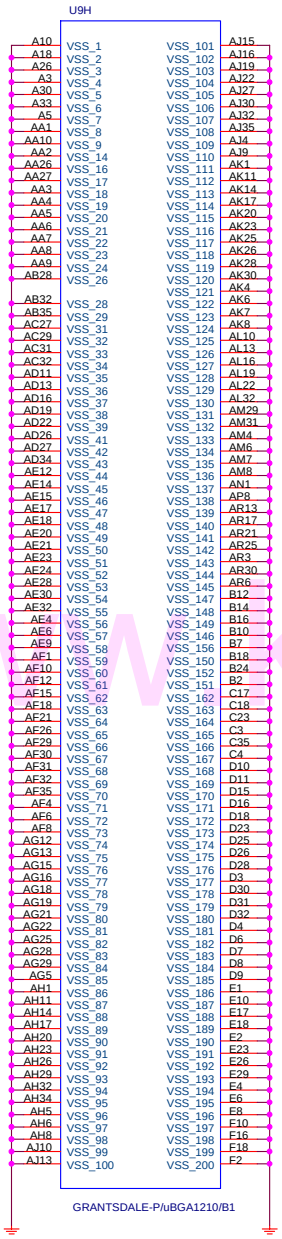

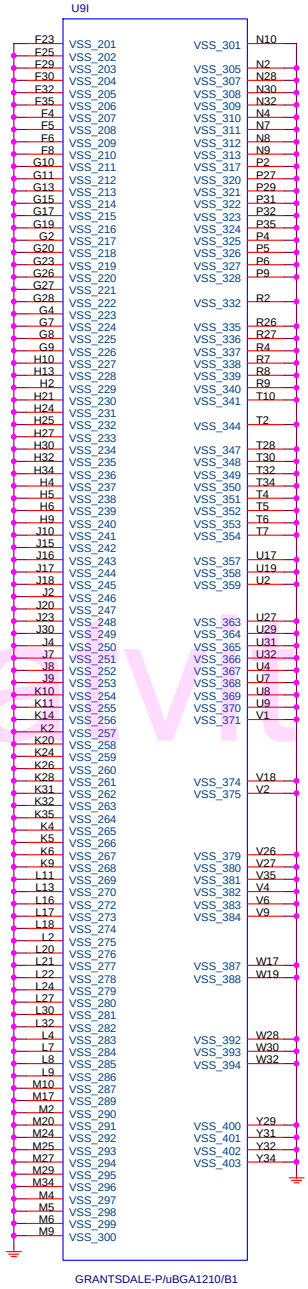

Gigabyte Technology

Title: GMCH-GND

Size: Custom | Document Number: 8I915P-D PRO | Rev: 2.0

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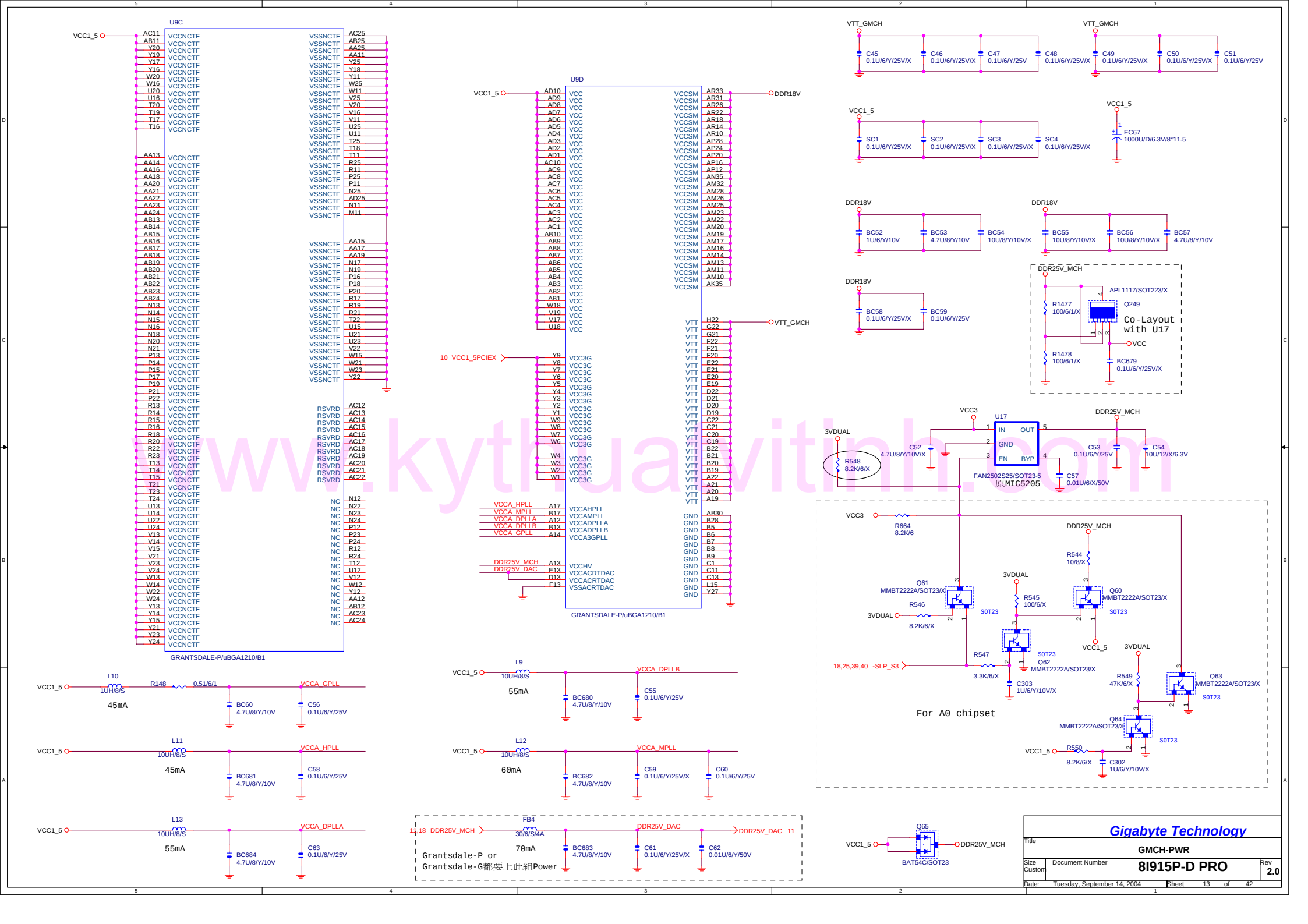

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Size: Custom	Document Number: 8I915P-D PRO	Rev: 2.0
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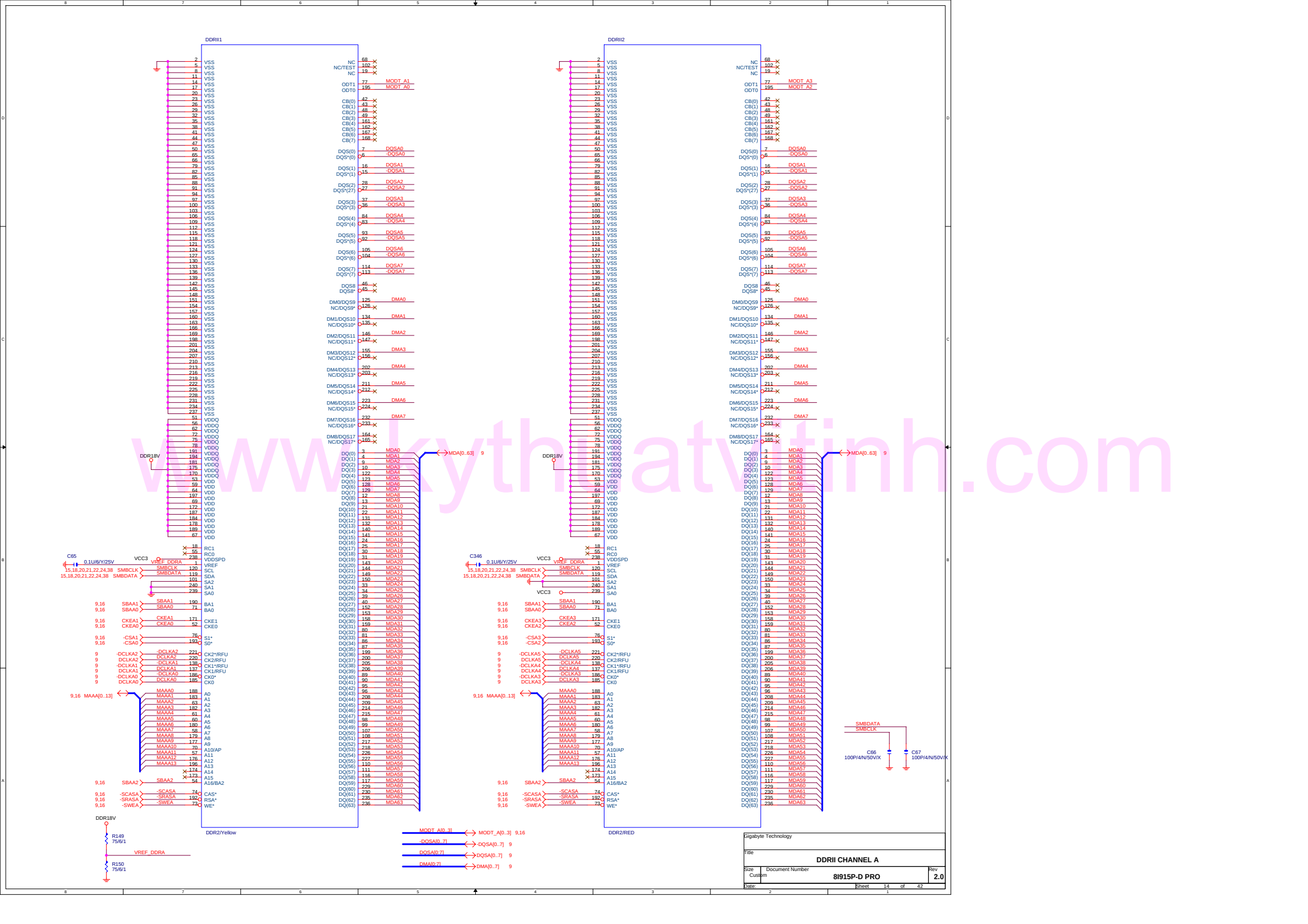
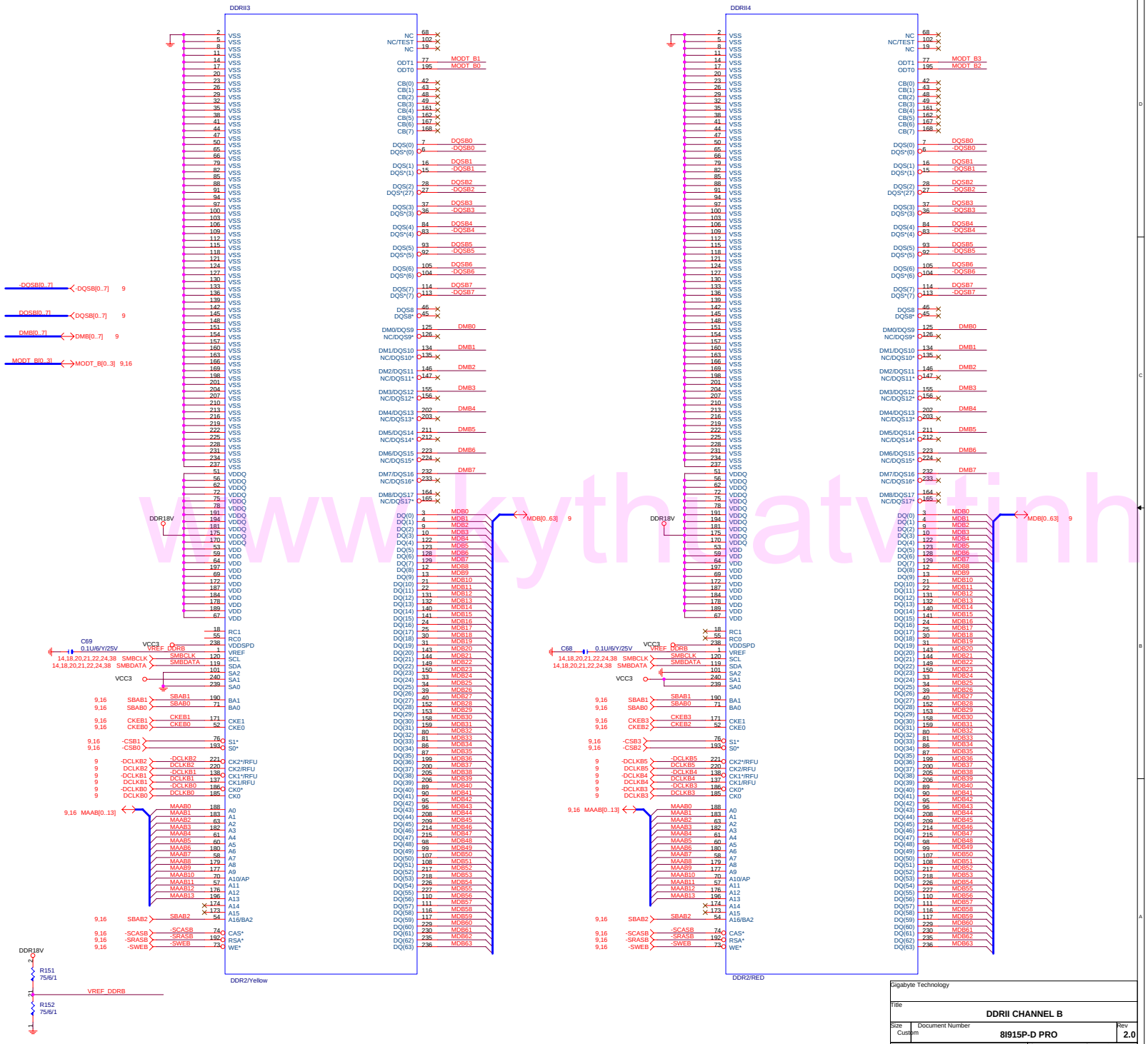


Gigabyte Technology

Title: **DDRII CHANNEL A**

Size: Custom | Document Number: **8I915P-D PRO** | Rev: **2.0**

Date: | Sheet 14 of 42



Gigabyte Technology		
Title	DDRII CHANNEL B	
Size: Custom	Document Number: 8I915P-D PRO	Rev: 2.0
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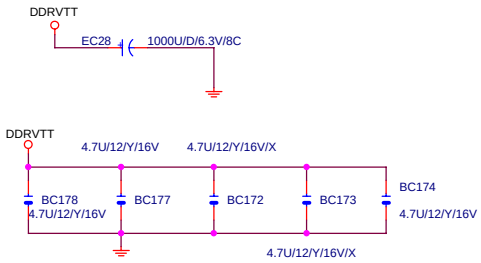
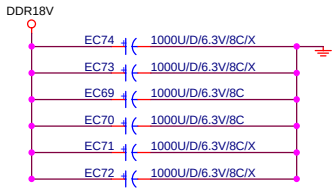
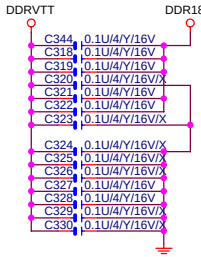
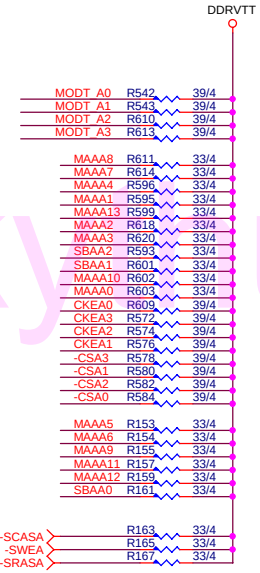
DDR TERMINATION CHANNEL A

DDRVTT Decouple

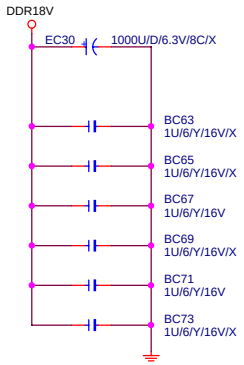


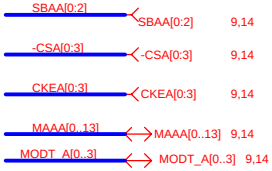






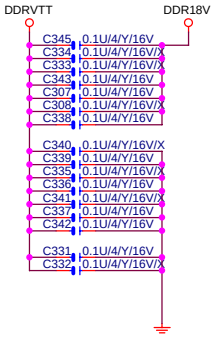
DDR18V Decouple

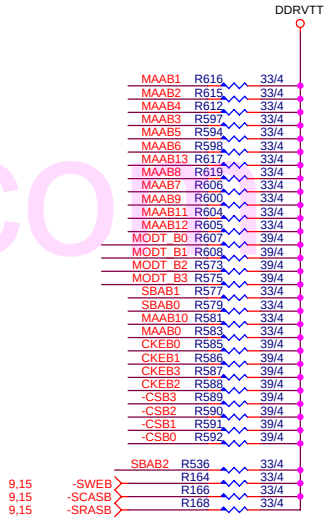




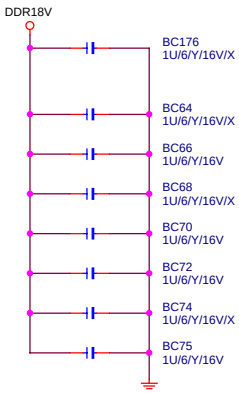
CHANNEL B

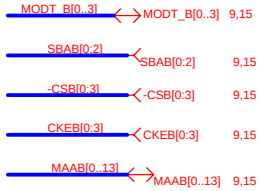
DDRVTT Decouple





DDR18V Decouple





Gigabyte Technology

Title: DDRII TERMINATOR

Size: B | Document Number: 8I915P-D PRO | Rev: 2.0

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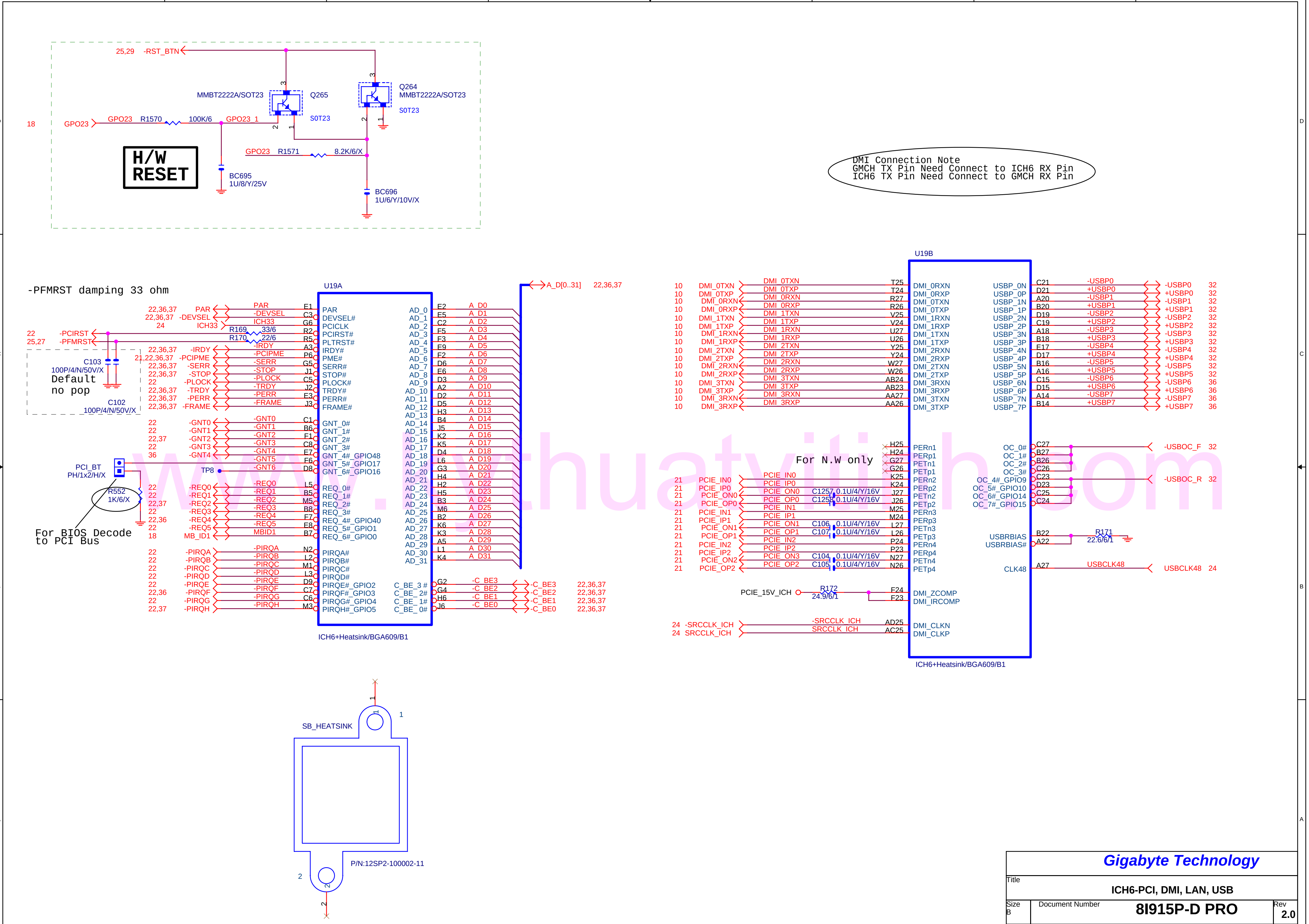

Gigabyte Technology

Title: ICH6-PCI, DMI, LAN, USB

Size	Document Number	Rev
B	8I915P-D PRO	2.0

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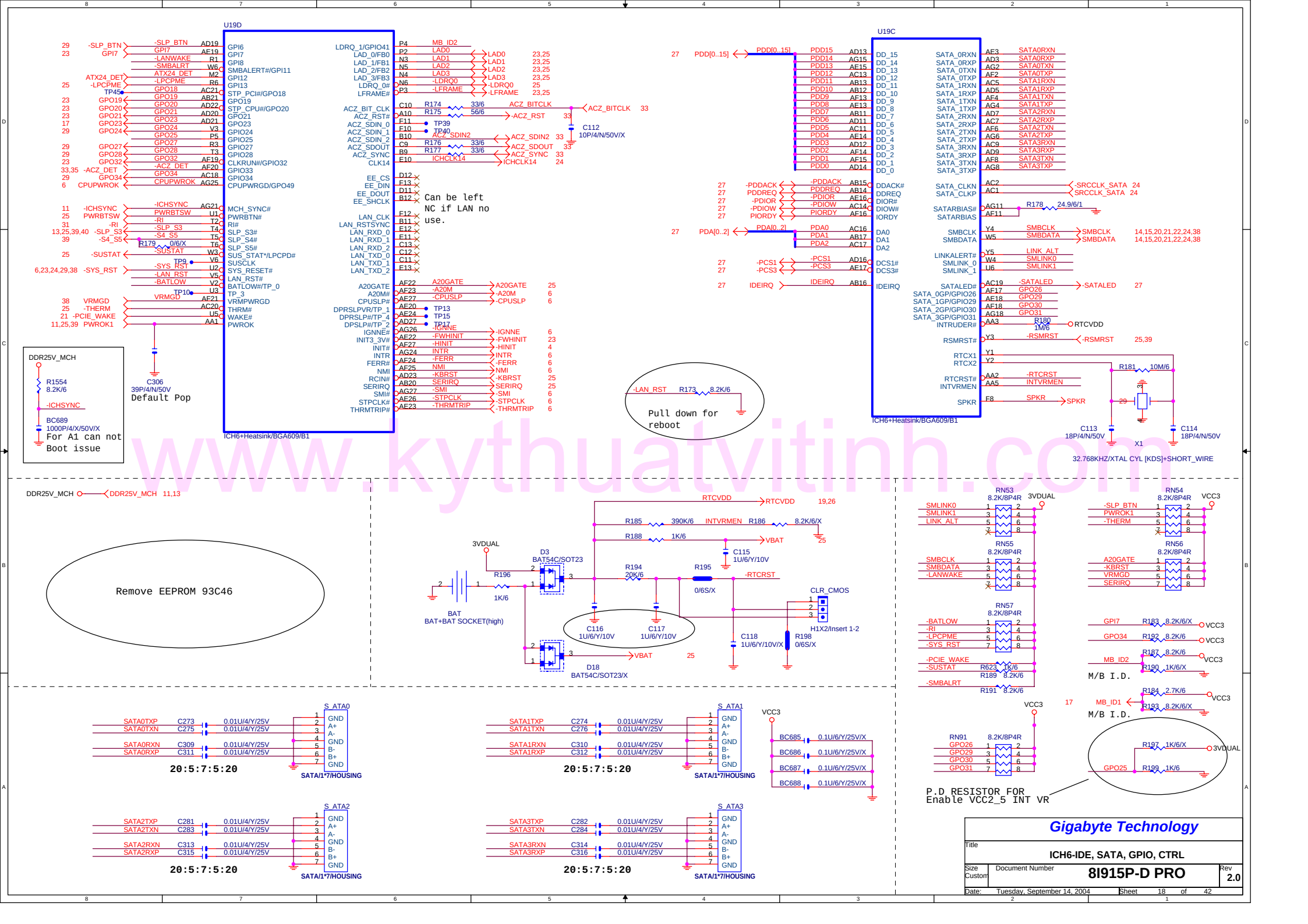

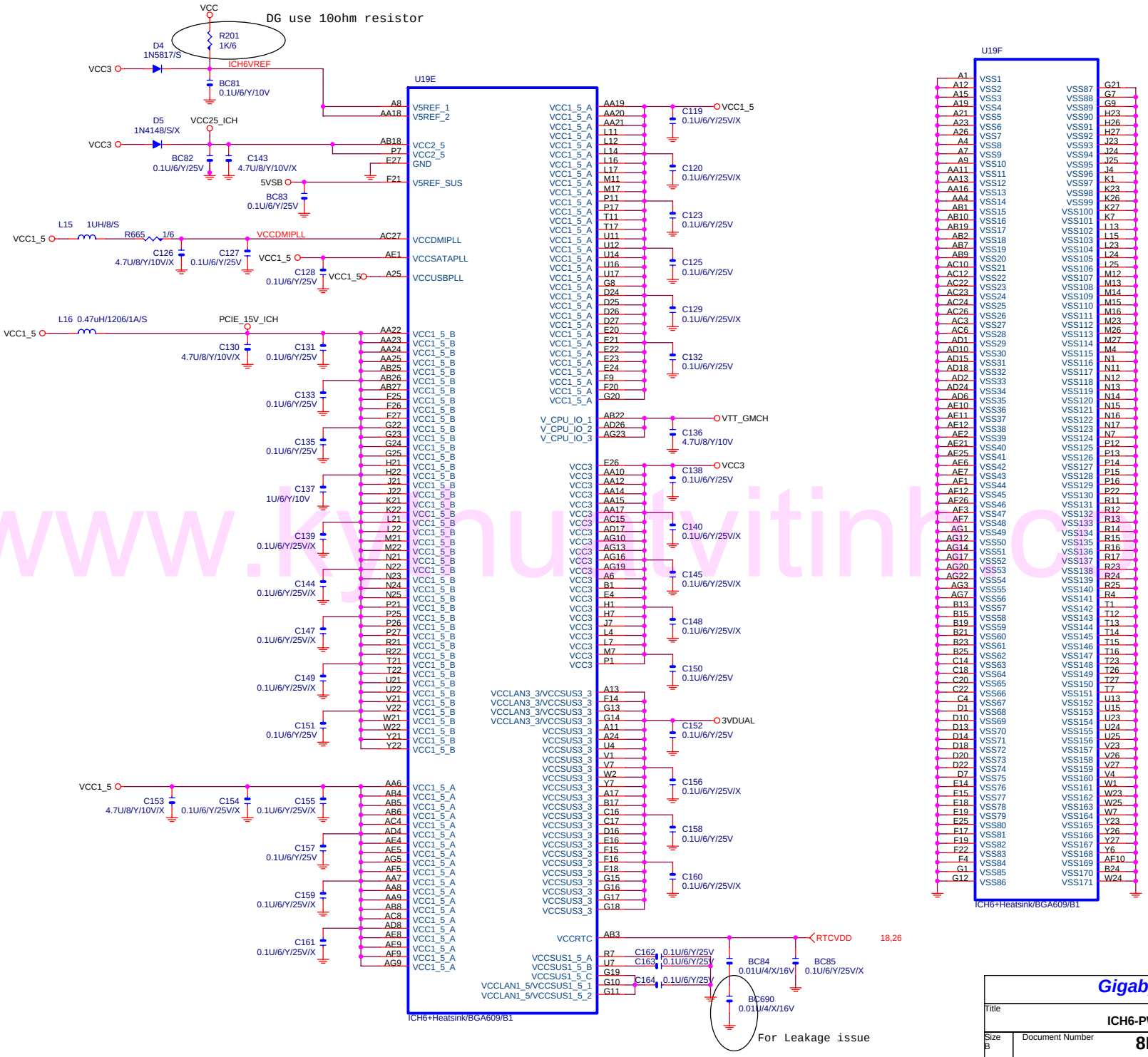

Gigabyte Technology			
Title: ICH6-PWR & GND			
Size: B	Document Number: 8I915P-D PRO		Rev: 2.0
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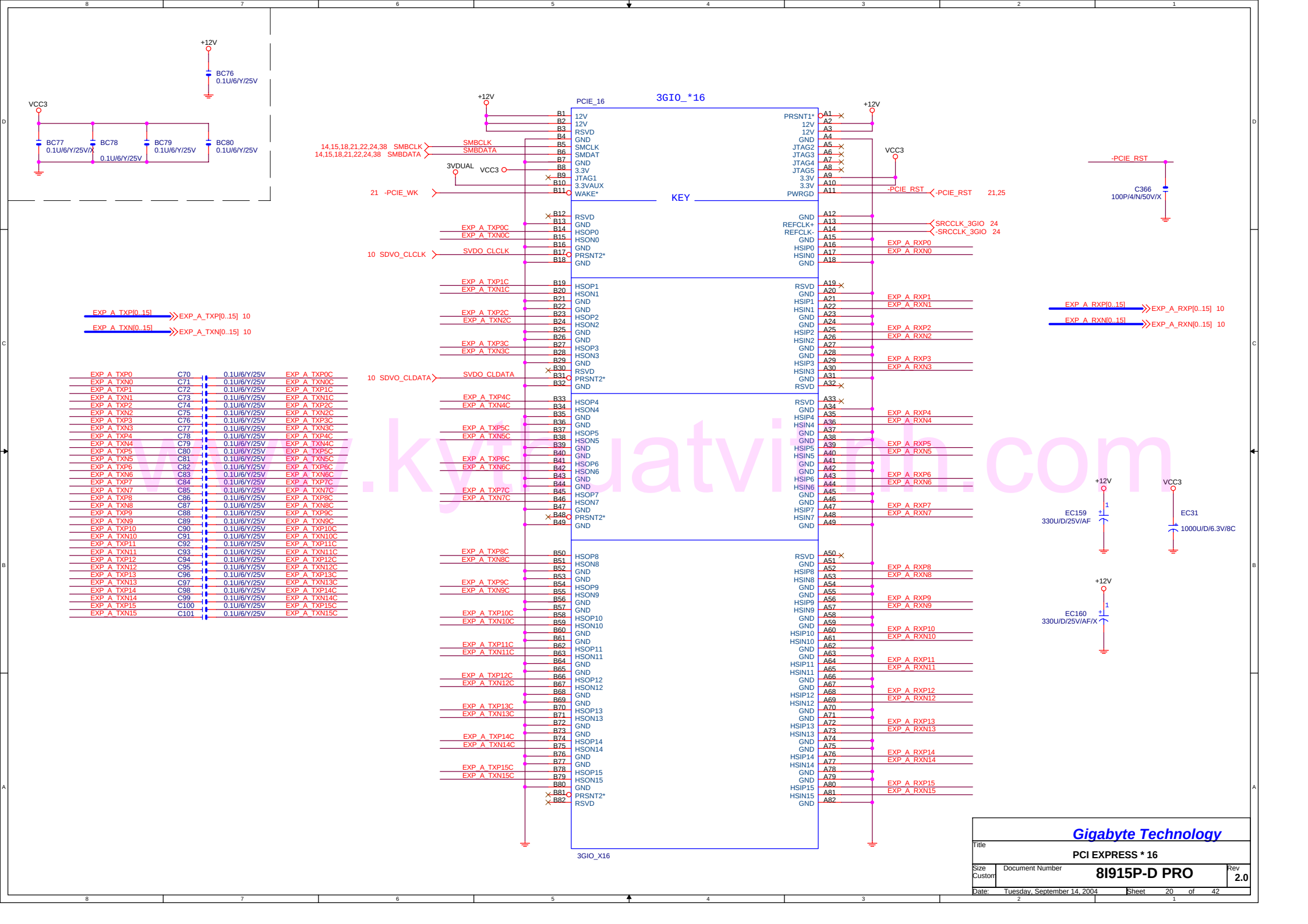
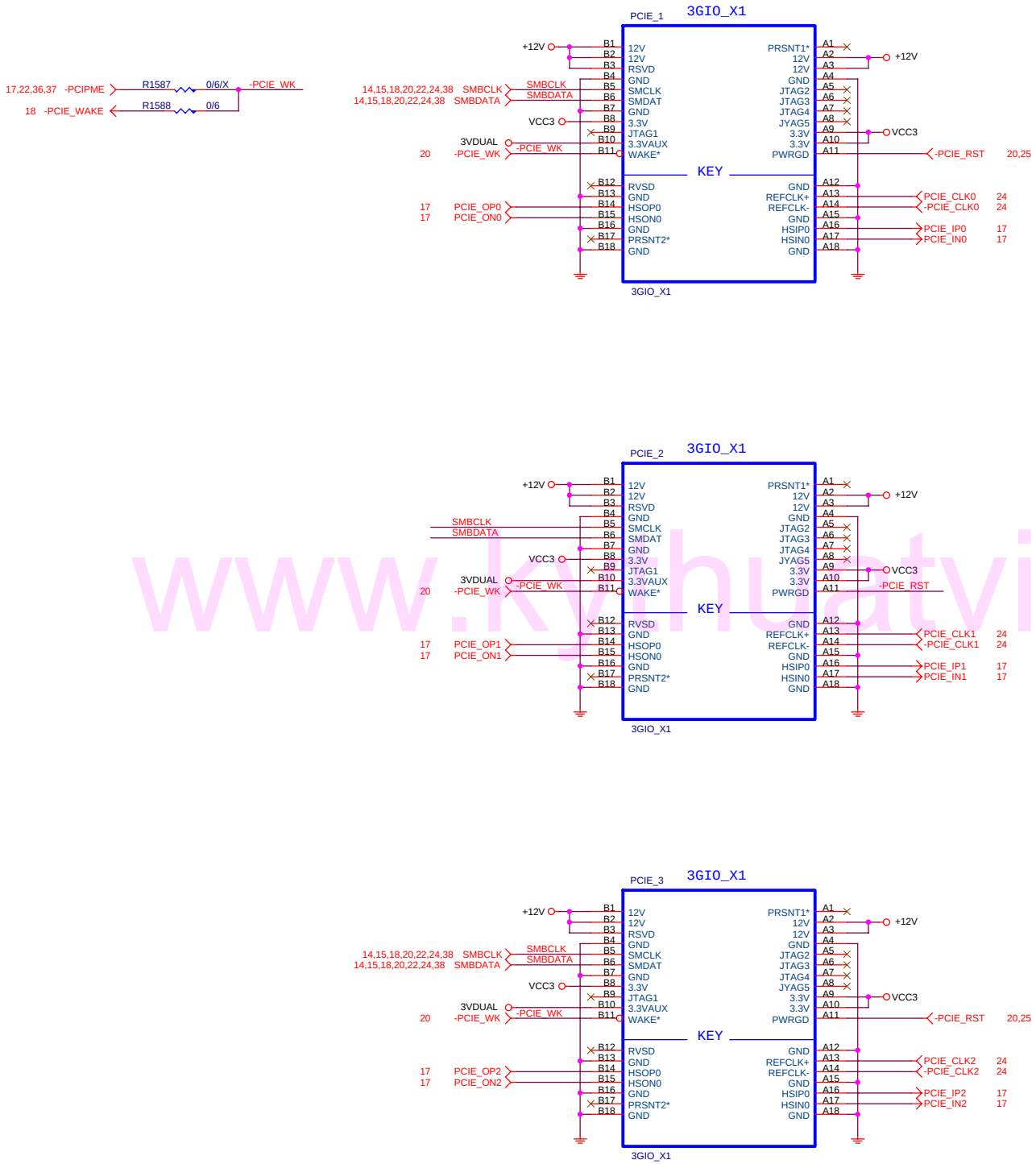


EXP_A_TXP0	C70	0.1U/6/Y/25V	EXP_A_TXP0C
EXP_A_TXN0	C71	0.1U/6/Y/25V	EXP_A_TXN0C
EXP_A_TXP1	C72	0.1U/6/Y/25V	EXP_A_TXP1C
EXP_A_TXN1	C73	0.1U/6/Y/25V	EXP_A_TXN1C
EXP_A_TXP2	C74	0.1U/6/Y/25V	EXP_A_TXP2C
EXP_A_TXN2	C75	0.1U/6/Y/25V	EXP_A_TXN2C
EXP_A_TXP3	C76	0.1U/6/Y/25V	EXP_A_TXP3C
EXP_A_TXN3	C77	0.1U/6/Y/25V	EXP_A_TXN3C
EXP_A_TXP4	C78	0.1U/6/Y/25V	EXP_A_TXP4C
EXP_A_TXN4	C79	0.1U/6/Y/25V	EXP_A_TXN4C
EXP_A_TXP5	C80	0.1U/6/Y/25V	EXP_A_TXP5C
EXP_A_TXN5	C81	0.1U/6/Y/25V	EXP_A_TXN5C
EXP_A_TXP6	C82	0.1U/6/Y/25V	EXP_A_TXP6C
EXP_A_TXN6	C83	0.1U/6/Y/25V	EXP_A_TXN6C
EXP_A_TXP7	C84	0.1U/6/Y/25V	EXP_A_TXP7C
EXP_A_TXN7	C85	0.1U/6/Y/25V	EXP_A_TXN7C
EXP_A_TXP8	C86	0.1U/6/Y/25V	EXP_A_TXP8C
EXP_A_TXN8	C87	0.1U/6/Y/25V	EXP_A_TXN8C
EXP_A_TXP9	C88	0.1U/6/Y/25V	EXP_A_TXP9C
EXP_A_TXN9	C89	0.1U/6/Y/25V	EXP_A_TXN9C
EXP_A_TXP10	C90	0.1U/6/Y/25V	EXP_A_TXP10C
EXP_A_TXN10	C91	0.1U/6/Y/25V	EXP_A_TXN10C
EXP_A_TXP11	C92	0.1U/6/Y/25V	EXP_A_TXP11C
EXP_A_TXN11	C93	0.1U/6/Y/25V	EXP_A_TXN11C
EXP_A_TXP12	C94	0.1U/6/Y/25V	EXP_A_TXP12C
EXP_A_TXN12	C95	0.1U/6/Y/25V	EXP_A_TXN12C
EXP_A_TXP13	C96	0.1U/6/Y/25V	EXP_A_TXP13C
EXP_A_TXN13	C97	0.1U/6/Y/25V	EXP_A_TXN13C
EXP_A_TXP14	C98	0.1U/6/Y/25V	EXP_A_TXP14C
EXP_A_TXN14	C99	0.1U/6/Y/25V	EXP_A_TXN14C
EXP_A_TXP15	C100	0.1U/6/Y/25V	EXP_A_TXP15C
EXP_A_TXN15	C101	0.1U/6/Y/25V	EXP_A_TXN15C

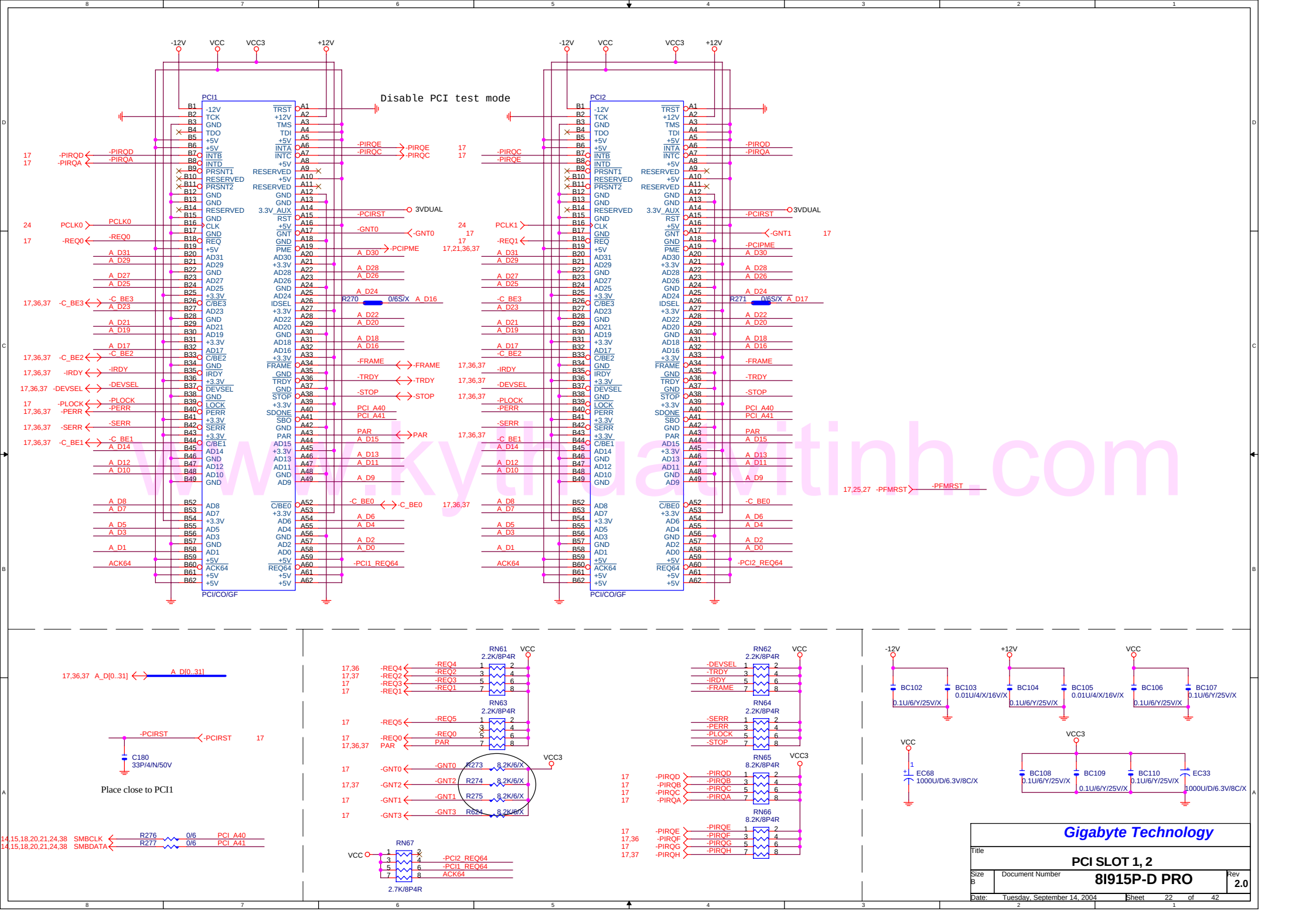
B1	12V		PRSNT1*	A1			
B2	12V		12V	A2			
B3	RSVD		12V	A3			
B4	GND		GND	A4			
B5	SMCLK	SMBCLK	JTAG2	A5			
B6	SMDAT	SMBDATA	JTAG3	A6			
B7	GND		JTAG4	A7			
B8	3.3V	VCC3	JTAG5	A8			
B9	JTAG1		3.3V	A9			
B10	3.3VAUX		3.3V	A10			
B11	WAKE*	-PCIE_WK	PWRGD	A11	-PCIE_RST	-PCIE_RST	21,25
B12	RSVD		GND	A12			
B13	GND		REFCLK+	A13	SRCCLK_3GIO		24
B14	HSOP0	EXP_A_TXP0C	REFCLK-	A14	-SRCCLK_3GIO		24
B15	HSON0	EXP_A_TXN0C	GND	A15			
B16	GND		HSIP0	A16	EXP_A_RXP0		
B17	PRSNT2*	SVDO_CLCLK	HSIN0	A17	EXP_A_RXN0		
B18	GND		GND	A18			
B19	HSOP1	EXP_A_TXP1C	RSVD	A19			
B20	HSON1	EXP_A_TXN1C	GND	A20			
B21	GND		HSIP1	A21	EXP_A_RXP1		
B22	GND		HSIN1	A22	EXP_A_RXN1		
B23	HSOP2	EXP_A_TXP2C	GND	A23			
B24	HSON2	EXP_A_TXN2C	GND	A24			
B25	GND		HSIP2	A25	EXP_A_RXP2		
B26	GND		HSIN2	A26	EXP_A_RXN2		
B27	HSOP3	EXP_A_TXP3C	GND	A27			
B28	HSON3	EXP_A_TXN3C	GND	A28			
B29	GND		HSIP3	A29	EXP_A_RXP3		
B30	RSVD		HSIN3	A30	EXP_A_RXN3		
B31	PRSNT2*	SVDO_CLDATA	GND	A31			
B32	GND		RSVD	A32			
B33	HSOP4	EXP_A_TXP4C	RSVD	A33			
B34	HSON4	EXP_A_TXN4C	GND	A34			
B35	GND		HSIP4	A35	EXP_A_RXP4		
B36	GND		HSIN4	A36	EXP_A_RXN4		
B37	HSOP5	EXP_A_TXP5C	GND	A37			
B38	HSON5	EXP_A_TXN5C	GND	A38			
B39	GND		HSIP5	A39	EXP_A_RXP5		
B40	GND		HSIN5	A40	EXP_A_RXN5		
B41	HSOP6	EXP_A_TXP6C	GND	A41			
B42	HSON6	EXP_A_TXN6C	GND	A42			
B43	GND		HSIP6	A43	EXP_A_RXP6		
B44	GND		HSIN6	A44	EXP_A_RXN6		
B45	HSOP7	EXP_A_TXP7C	GND	A45			
B46	HSON7	EXP_A_TXN7C	GND	A46			
B47	GND		HSIP7	A47	EXP_A_RXP7		
B48	PRSNT2*		HSIN7	A48	EXP_A_RXN7		
B49	GND		GND	A49			
B50	HSOP8	EXP_A_TXP8C	RSVD	A50			
B51	HSON8	EXP_A_TXN8C	GND	A51			
B52	GND		HSIP8	A52	EXP_A_RXP8		
B53	GND		HSIN8	A53	EXP_A_RXN8		
B54	HSOP9	EXP_A_TXP9C	GND	A54			
B55	HSON9	EXP_A_TXN9C	GND	A55			
B56	GND		HSIP9	A56	EXP_A_RXP9		
B57	GND		HSIN9	A57	EXP_A_RXN9		
B58	HSOP10	EXP_A_TXP10C	GND	A58			
B59	HSON10	EXP_A_TXN10C	GND	A59			
B60	GND		HSIP10	A60	EXP_A_RXP10		
B61	GND		HSIN10	A61	EXP_A_RXN10		
B62	HSOP11	EXP_A_TXP11C	GND	A62			
B63	HSON11	EXP_A_TXN11C	GND	A63			
B64	GND		HSIP11	A64	EXP_A_RXP11		
B65	GND		HSIN11	A65	EXP_A_RXN11		
B66	HSOP12	EXP_A_TXP12C	GND	A66			
B67	HSON12	EXP_A_TXN12C	GND	A67			
B68	GND		HSIP12	A68	EXP_A_RXP12		
B69	GND		HSIN12	A69	EXP_A_RXN12		
B70	HSOP13	EXP_A_TXP13C	GND	A70			
B71	HSON13	EXP_A_TXN13C	GND	A71			
B72	GND		HSIP13	A72	EXP_A_RXP13		
B73	GND		HSIN13	A73	EXP_A_RXN13		
B74	HSOP14	EXP_A_TXP14C	GND	A74			
B75	HSON14	EXP_A_TXN14C	GND	A75			
B76	GND		HSIP14	A76	EXP_A_RXP14		
B77	GND		HSIN14	A77	EXP_A_RXN14		
B78	HSOP15	EXP_A_TXP15C	GND	A78			
B79	HSON15	EXP_A_TXN15C	GND	A79			
B80	GND		HSIP15	A80	EXP_A_RXP15		
B81	PRSNT2*		HSIN15	A81	EXP_A_RXN15		
B82	RSVD		GND	A82			

Gigabyte Technology

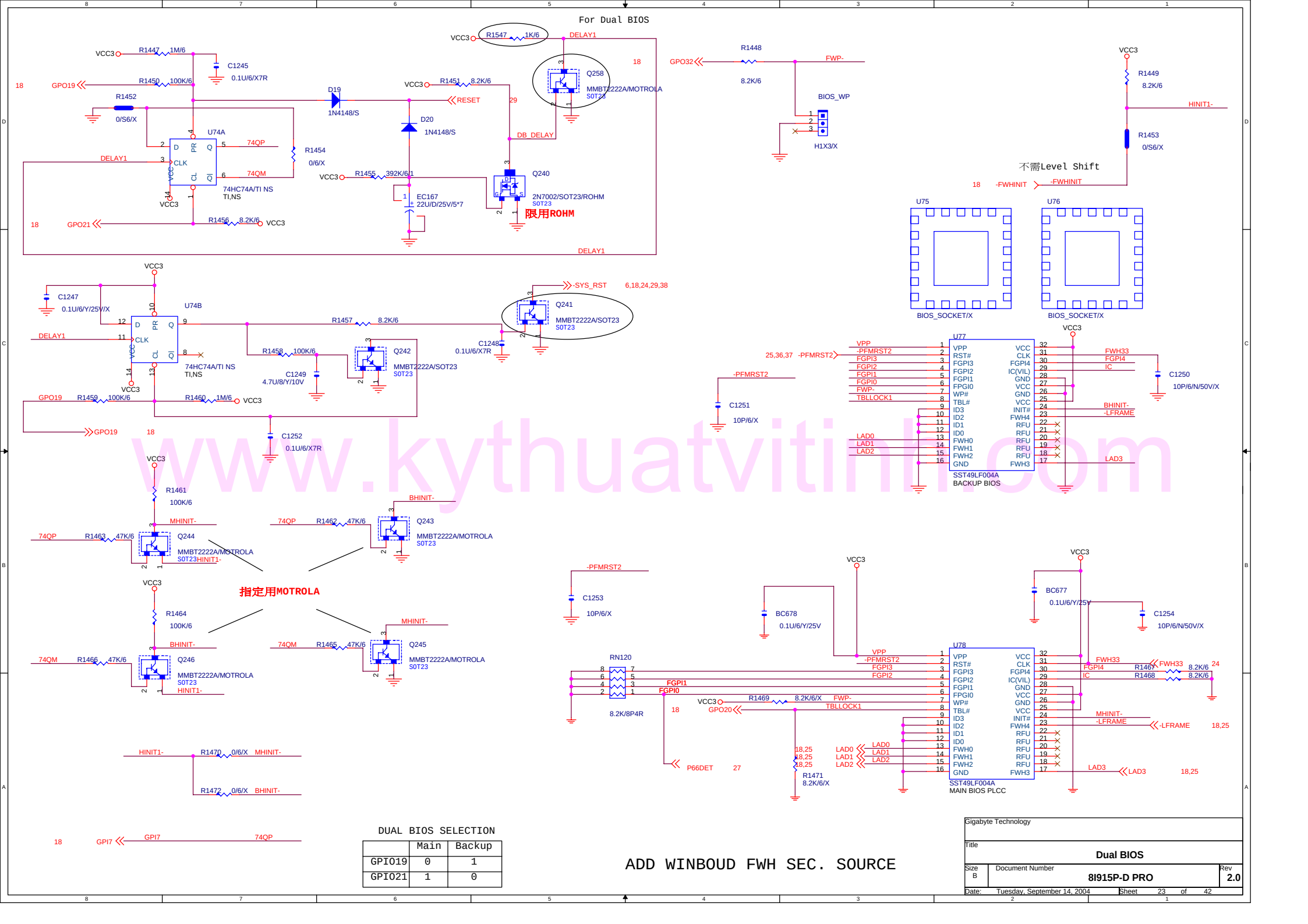
Title	PCI EXPRESS * 16		
Size: Custom	Document Number: 8I915P-D PRO		Rev: 2.0
Date: Tuesday, September 14, 2004	Sheet 20 of 42		



Gigabyte Technology		
Title: PCI E SLOT 1, 2, 3		
Size: B	Document Number: 8I915P-D PRO	Rev: 2.0
Date: Tuesday, September 14, 2004	Sheet 21 of 42	



Gigabyte Technology		
Title	PCI SLOT 1, 2	
Size B	Document Number 8I915P-D PRO	Rev 2.0
Date: Tuesday, September 14, 2004	Sheet 22 of 42	

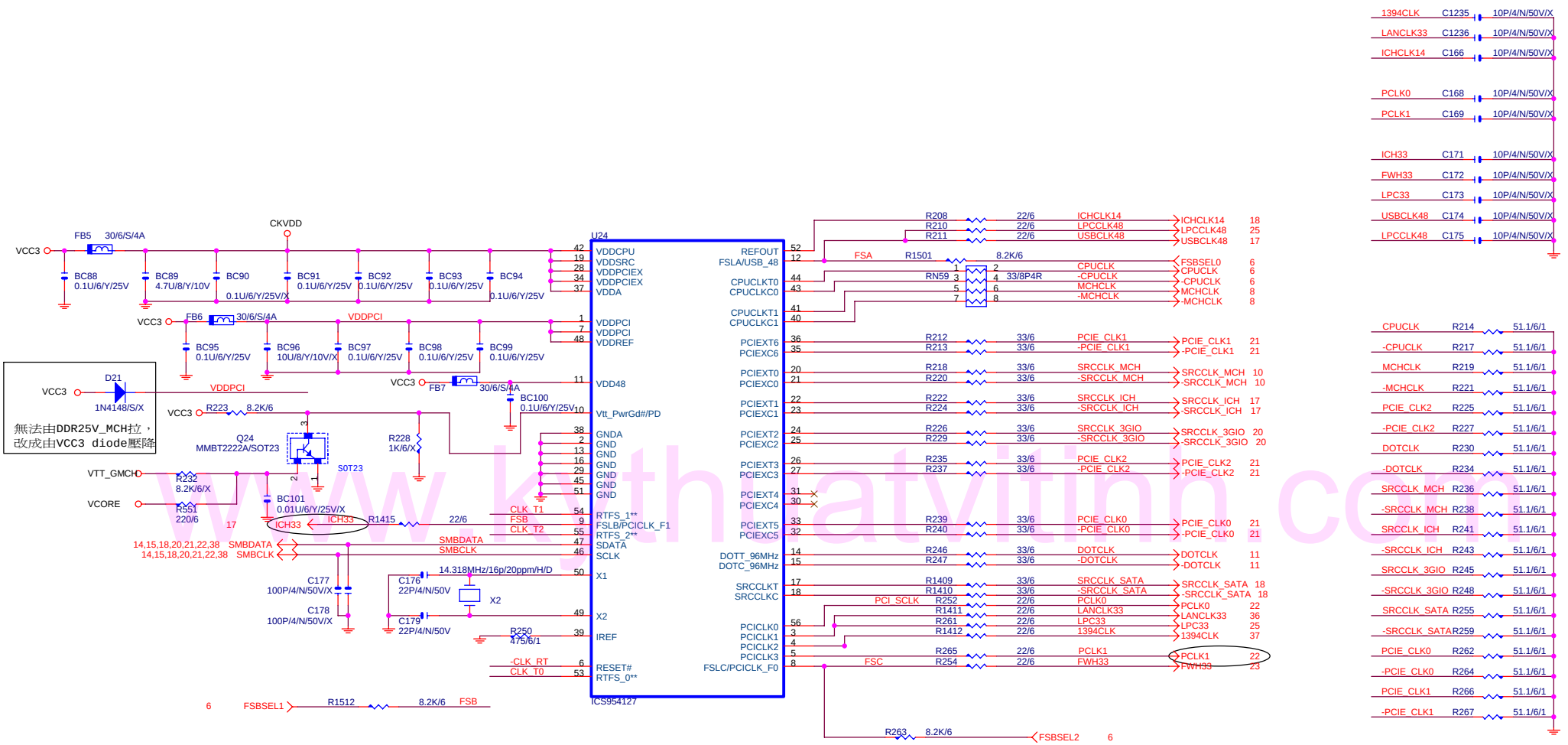


DUAL BIOS SELECTION

	Main	Backup
GPIO19	0	1
GPIO21	1	0

ADD WINBOUD FWH SEC. SOURCE

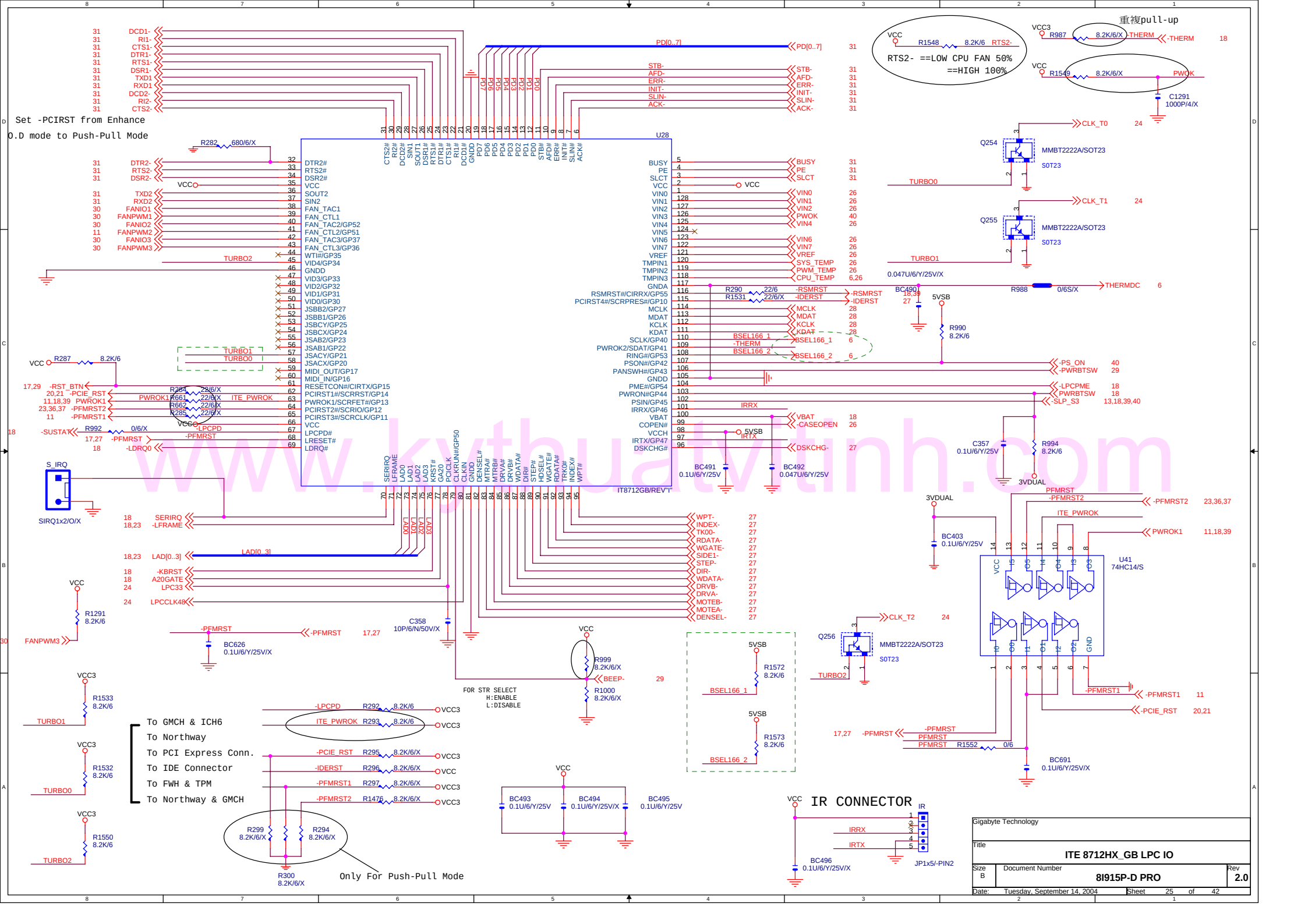
Gigabyte Technology			
Title: Dual BIOS			
Size: B	Document Number: 8I915P-D PRO		Rev: 2.0
Date: Tuesday, September 14, 2004	Sheet 23 of 42		

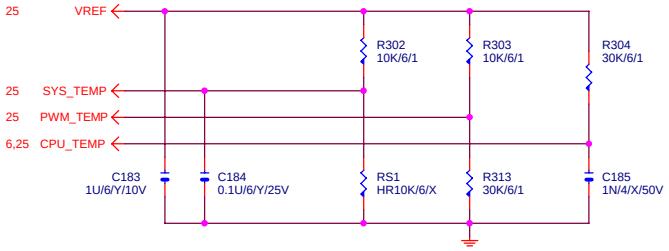


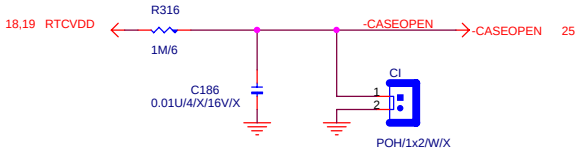
T2	T1	T0	FSB
0	0	0	200
0	0	1	202
0	1	0	206
0	1	1	210
1	0	0	214
1	0	1	218
1	1	0	220
1	1	1	222

Intel Confidential

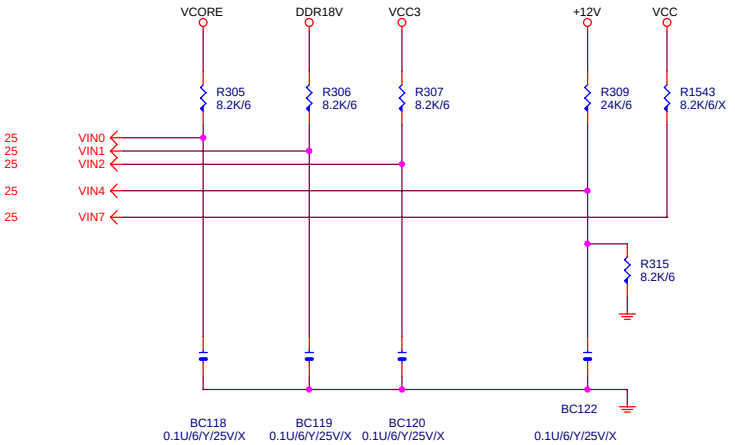
Title	CK410M/GBT_CLK GEN	
Size: Custom	Document Number: 8I915P-D PRO	Rev: 2.0
Date: Tuesday, September 14, 2004	Sheet 24 of 42	

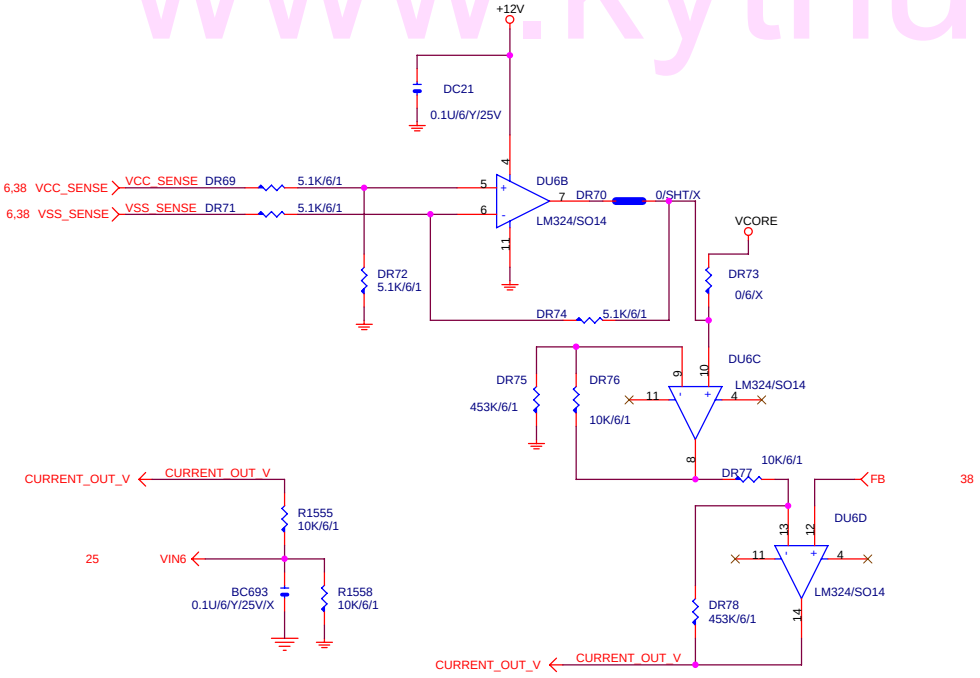

Set -PCIRST from Enhance
O.D mode to Push-Pull Mode
U28
IT8712GB/REV"I"
重複pull-up
RTS2- ==LOW CPU FAN 50%
==HIGH 100%
FOR STR SELECT
H:ENABLE
L:DISABLE
To GMCH & ICH6
To Northway
To PCI Express Conn.
To IDE Connector
To FWH & TPM
To Northway & GMCH
Only For Push-Pull Mode
IR CONNECTOR
Gigabyte Technology
Title
ITE 8712HX_GB LPC IO
Size B
Document Number
8I915P-D PRO
Rev 2.0
Date: Tuesday, September 14, 2004
Sheet 25 of 42

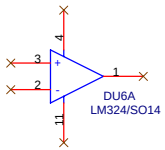




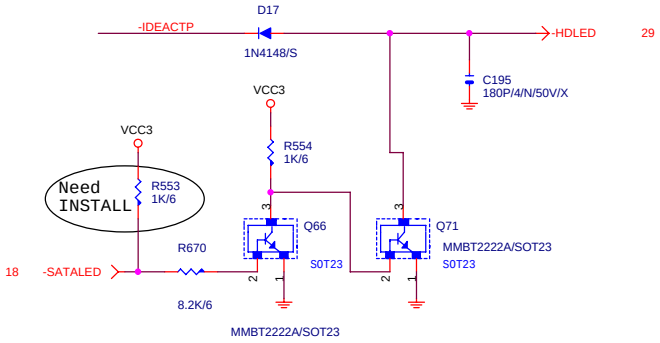
Case Open Circuits

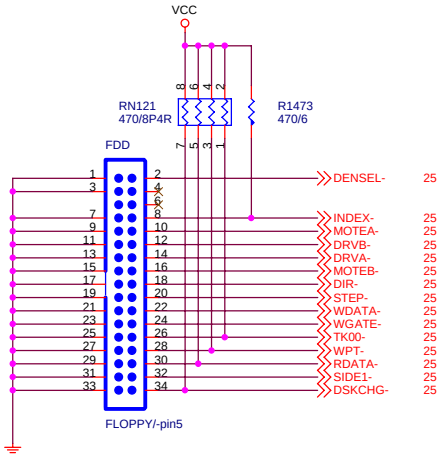


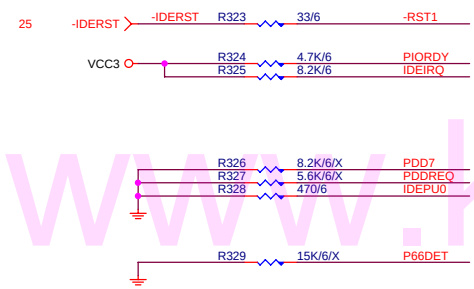


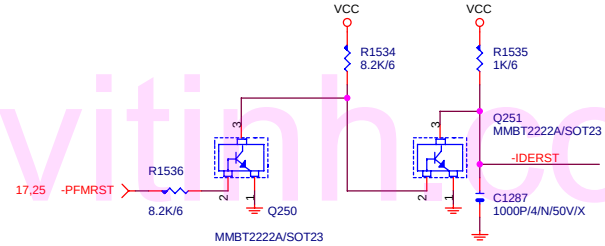


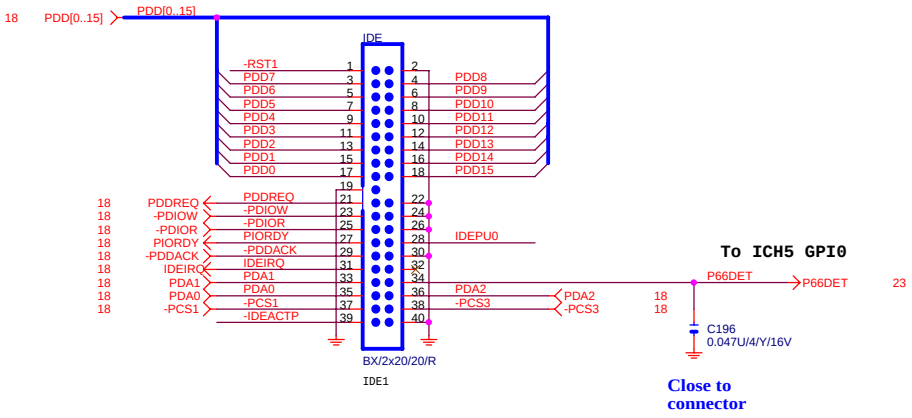
Gigabyte Technology		
Title: HARDWARE MONITOR		
Size: B	Document Number: 8I915P-D PRO	Rev: 2.0
Date: Tuesday, September 14, 2004	Sheet 26 of 42	











PRIMARY IDE CONNECTOR

Gigabyte Technology		
Title: IDE, FDD		
Size: B	Document Number: 8I915P-D PRO	Rev: 2.0
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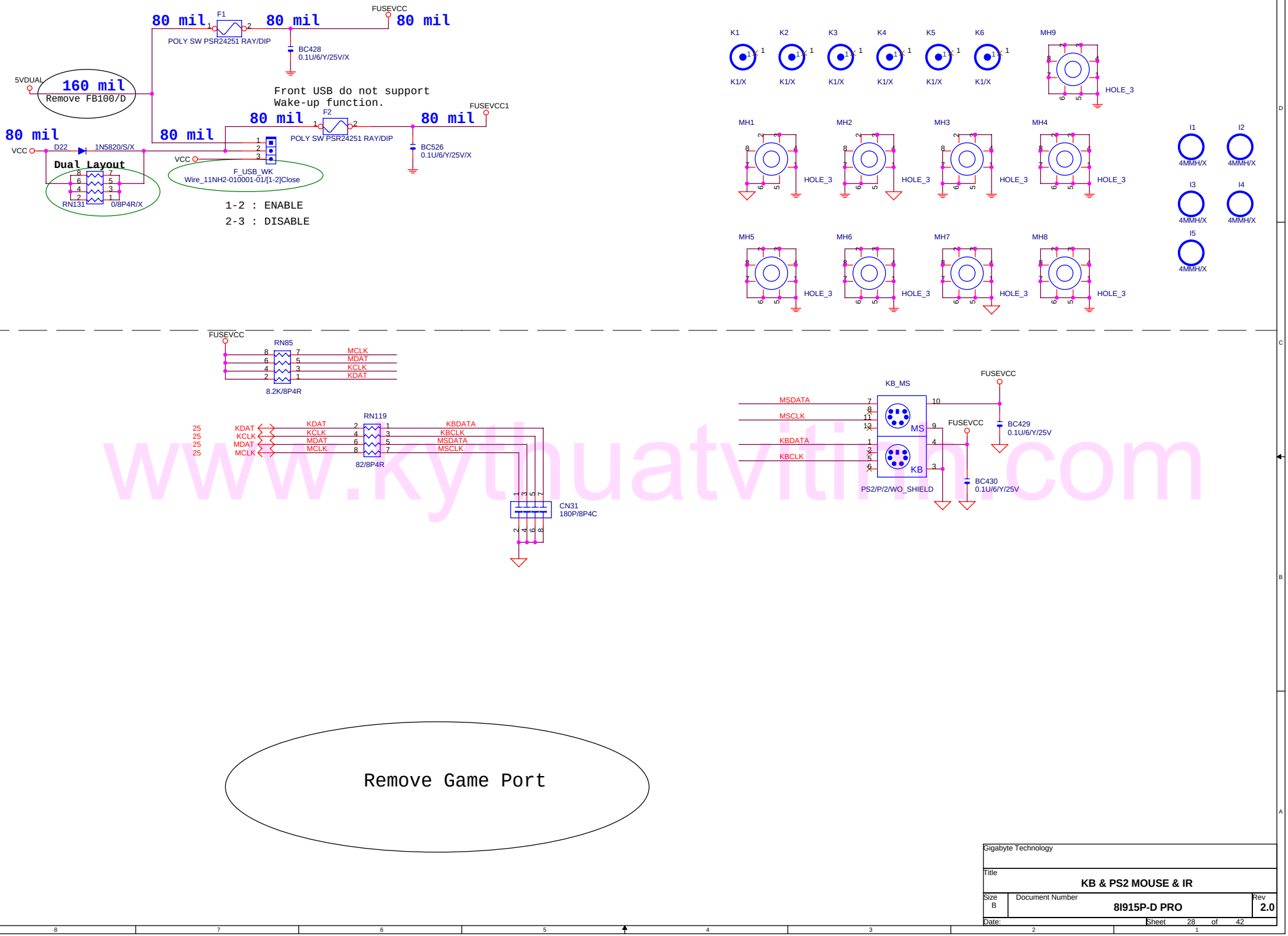
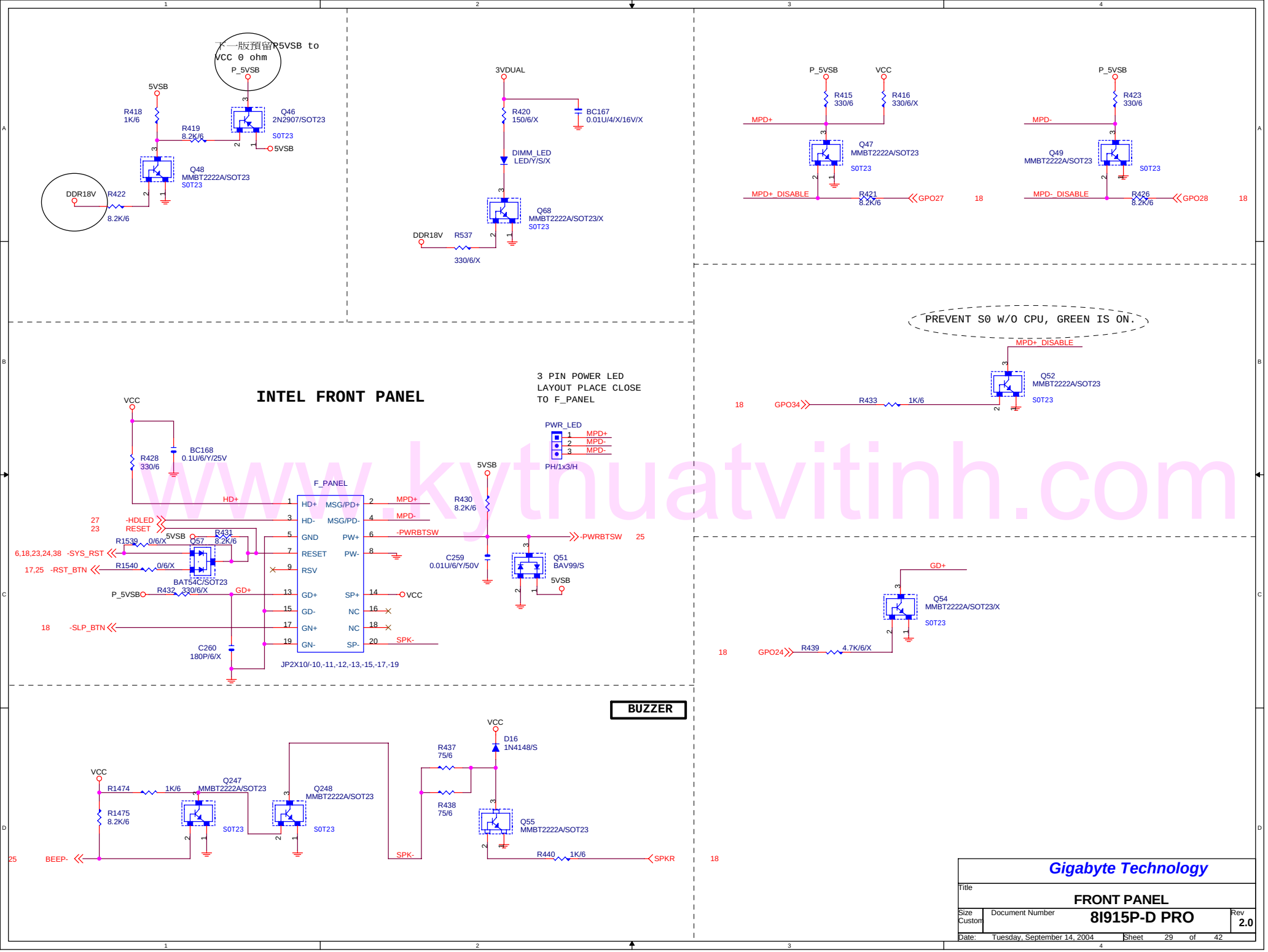


Gigabyte Technology			
Title	KB & PS2 MOUSE & IR		
Size B	Document Number 8I915P-D PRO		Rev 2.0
Date:	Sheet 28 of 42		



Gigabyte Technology	
Title	FRONT PANEL
Size: Custom	Document Number: 8I915P-D PRO
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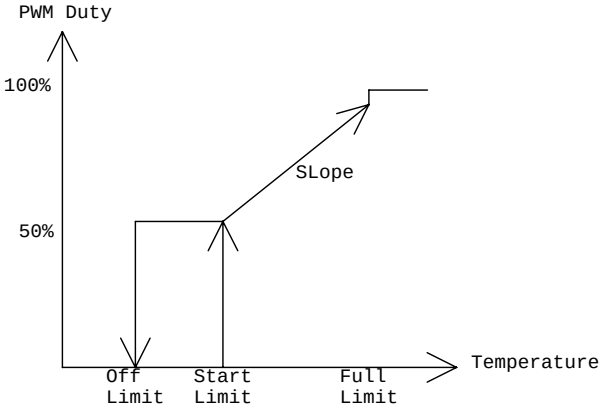
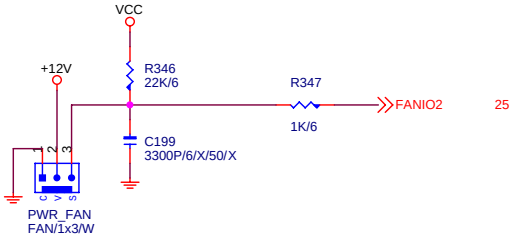
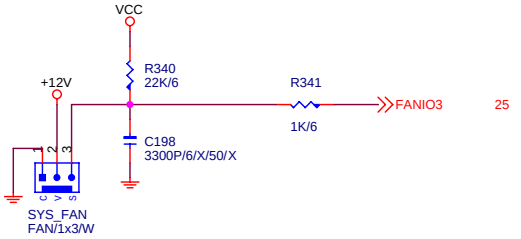


Table1:	3 pin FAN	
Off Limit	0 degree	0 PWM
Start Limit	40 degree	77 PWM
Full Limit	65 degree	127 PWM
Slope	2 PWM/degree	

Table2:	4 pin FAN	
Off Limit	0 degree	0 PWM
Start Limit	40 degree	0 PWM
Full Limit	65 degree	127 PWM
Slope	1 PWM/degree	

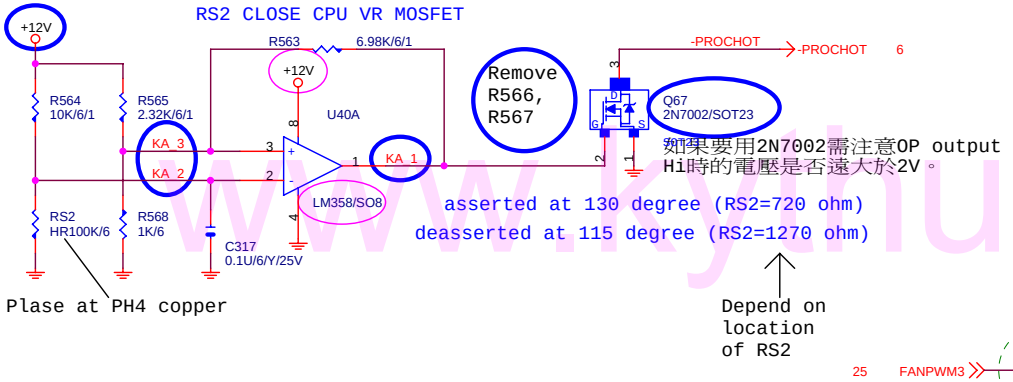




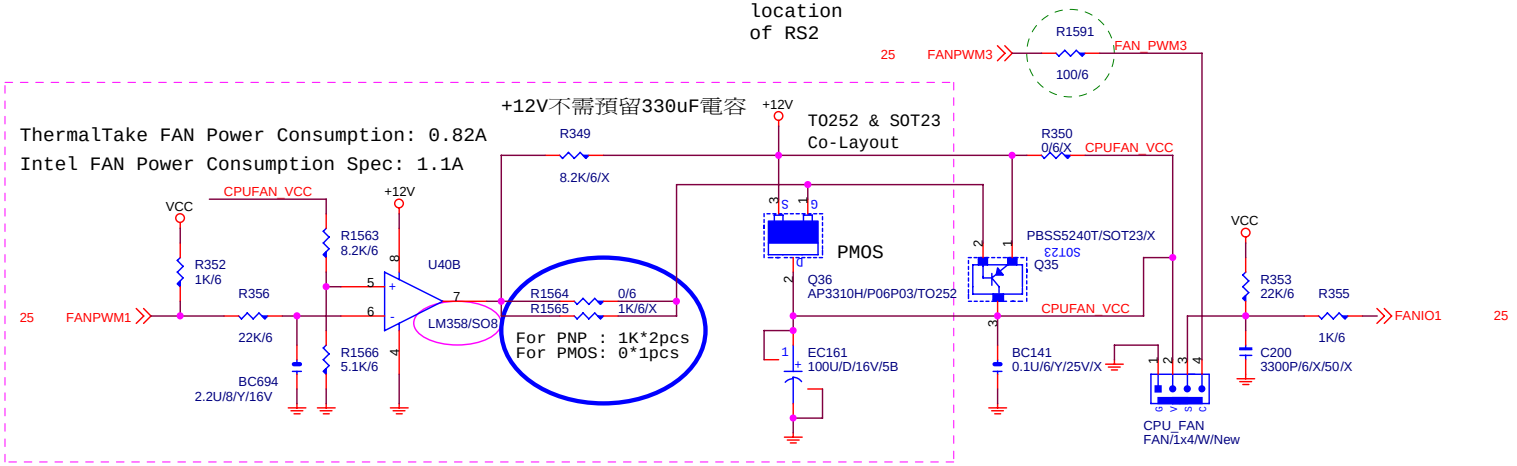
If +12V=12.15V, LM358 output Hi=10.93V

KA393改爲LM358，電源pin改接+12V，Prochot#溫度需重新調整之。

RS2 CLOSE CPU VR MOSFET



FAN_VCC	PWM_DUTY
11.5V	87 %
11.0V	84 %
10.5V	80 %
10.0V	76 %
9.50V	72 %
9.00V	69 %
8.80V	67 %~19%



If use PBSS5240 1pcs : (non airflow)

CPUFAN_VCC=12V: Temp=40 deg
CPUFAN_VCC=11V: Temp=82 deg
CPUFAN_VCC=10V: Temp=70 deg
CPUFAN_VCC= 9V: Temp=110 deg
CPUFAN_VCC= 8V: Temp>200 deg

If use PBSS5240 1pcs : (with airflow)

CPUFAN_VCC=12V: Temp=33 deg
CPUFAN_VCC=11V: Temp=62 deg
CPUFAN_VCC=10V: Temp=86 deg
CPUFAN_VCC= 9V: Temp=117 deg
CPUFAN_VCC= 8V: Temp>122 deg

Gigabyte Technology

Title: FAN CONTROL

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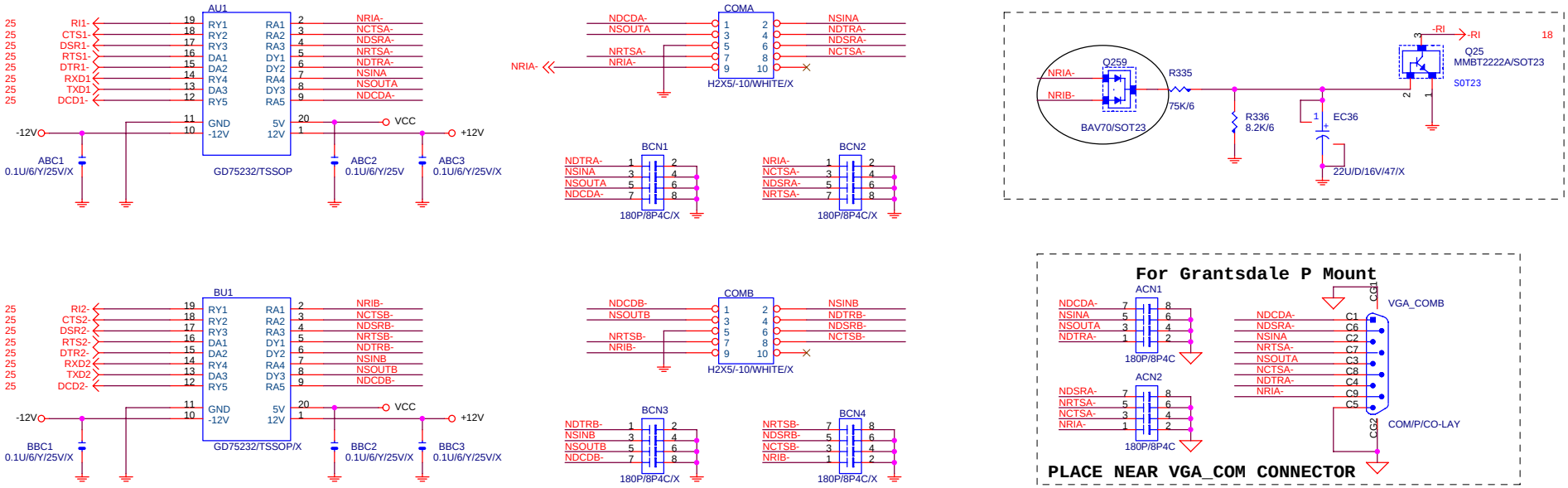

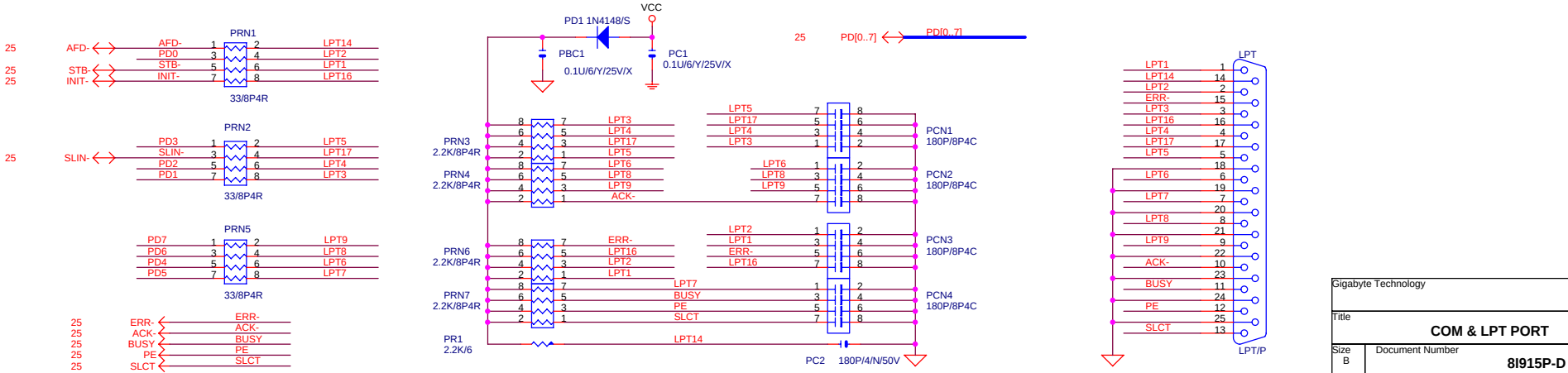

Gigabyte Technology		
Title: COM & LPT PORT		
Size: B	Document Number: 8I915P-D PRO	Rev: 2.0
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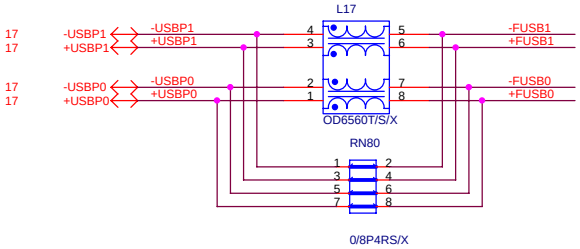
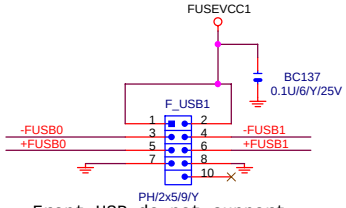
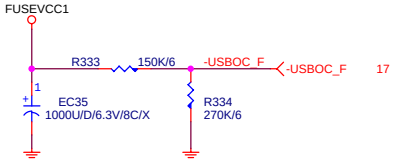
FRONT USB

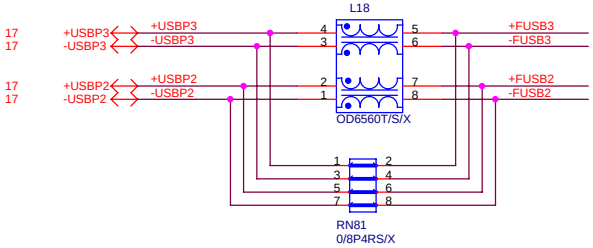
ICH6 USB2.0

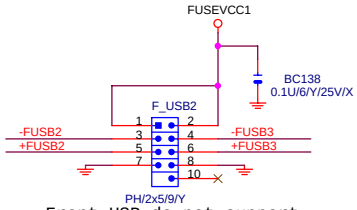




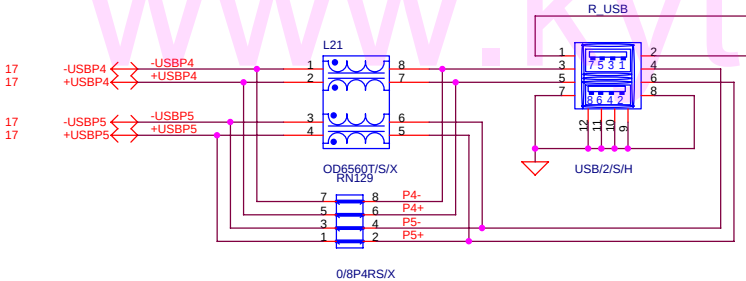
Front USB do not support Wake-up function.

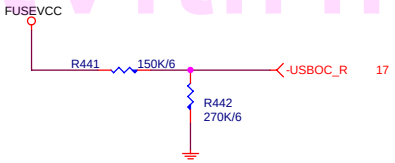






Front USB do not support Wake-up function.





Gigabyte Technology		
Title: F_USB & R_USB CONNECTOR		
Size: B	Document Number: 8I915P-D PRO	Rev: 2.0
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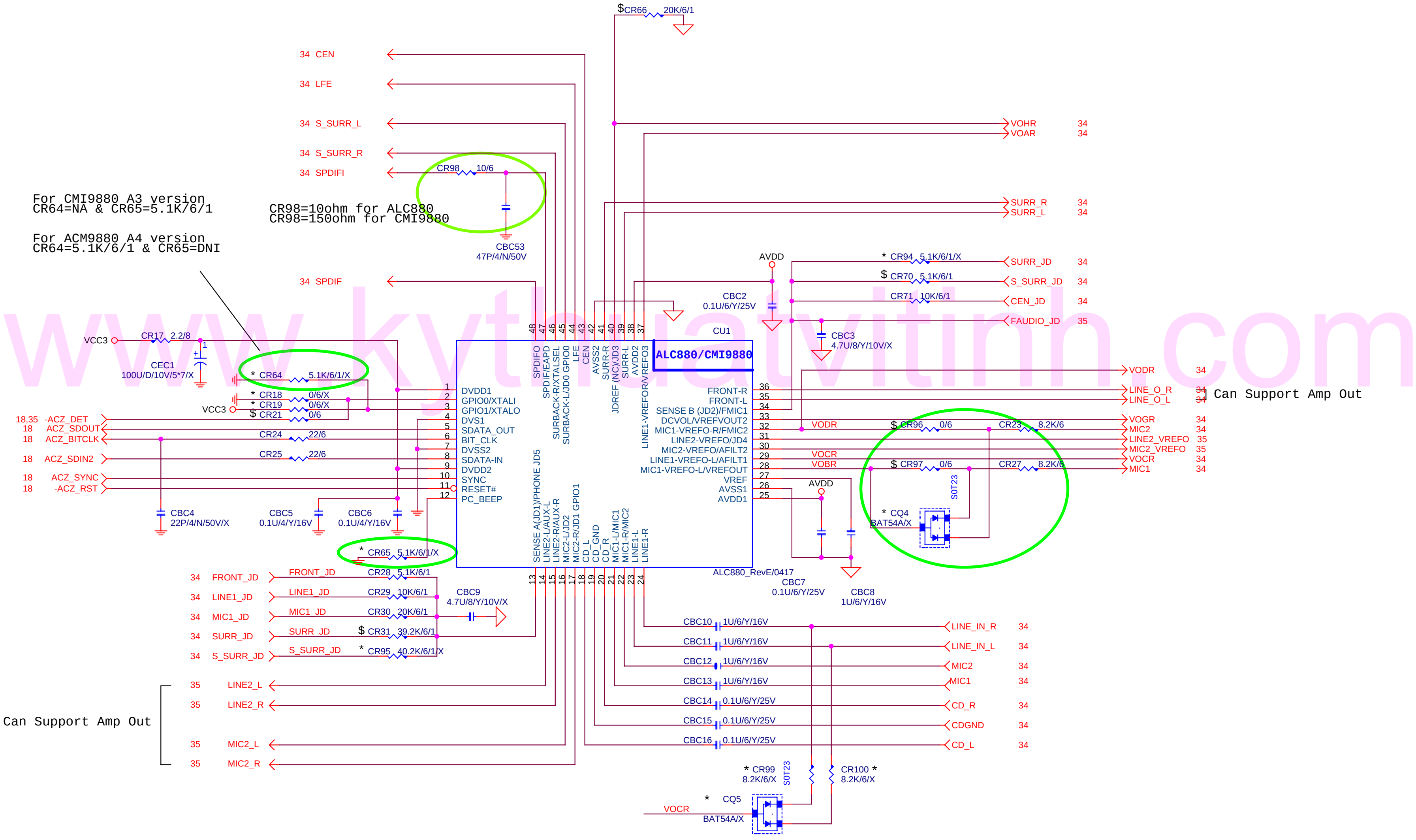
"$" means for ALC880 only

"*" means for CMI9880 only



Intel Confidential

Title	AZALIA: ALC880 / CMI9880	
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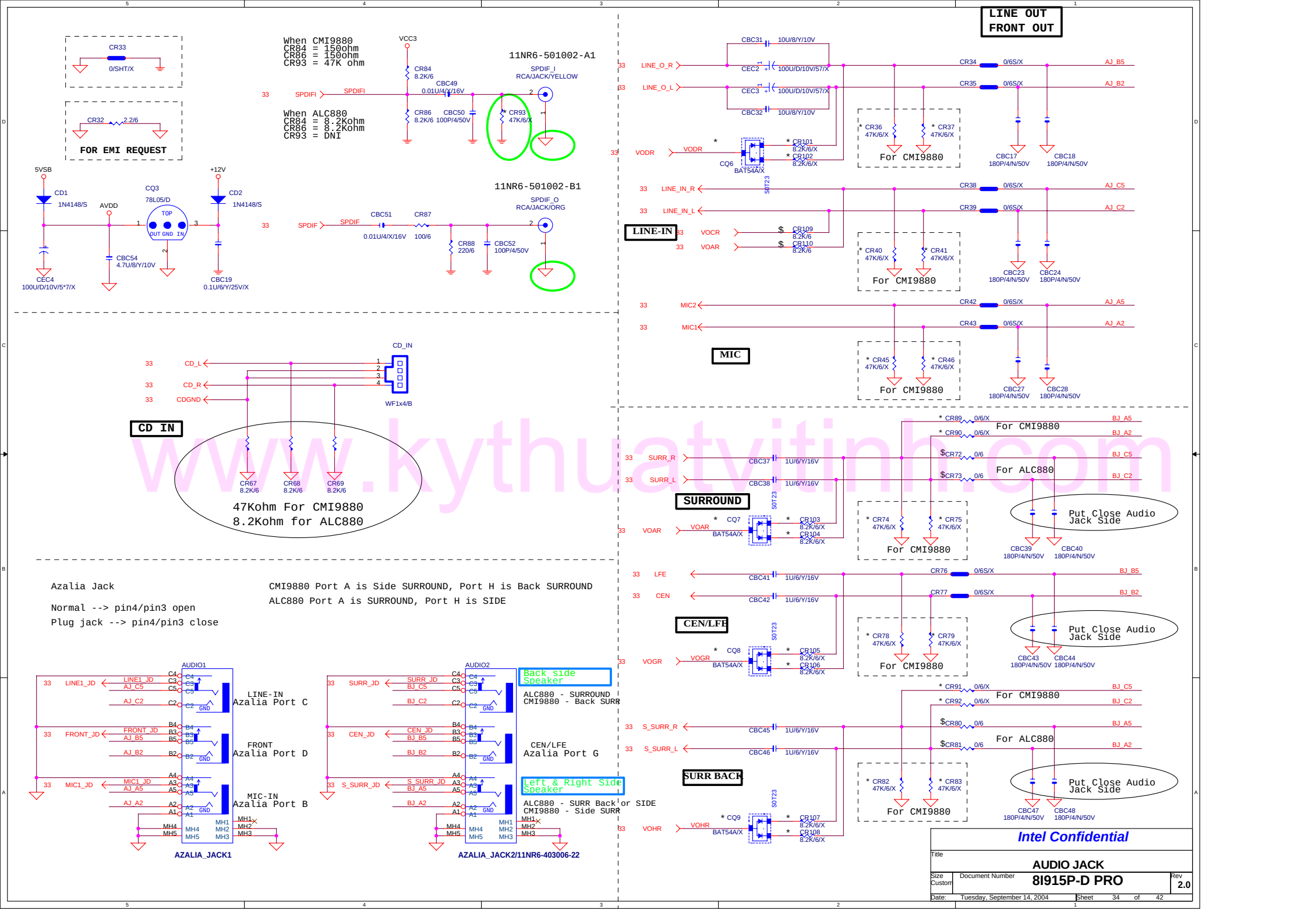

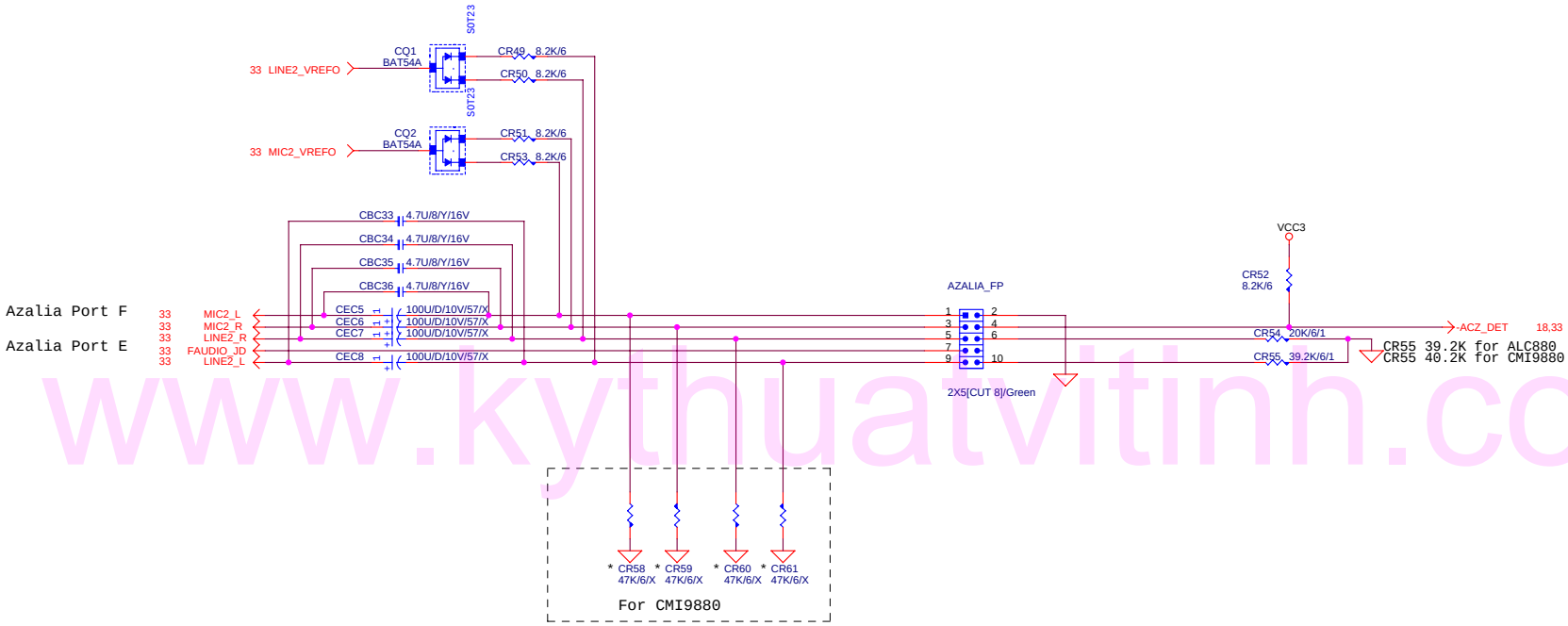

Intel Confidential			
Title: FRONT AUDIO CONNECTOR			
Size: Custom	Document Number: 8I915P-D PRO		Rev: 2.0
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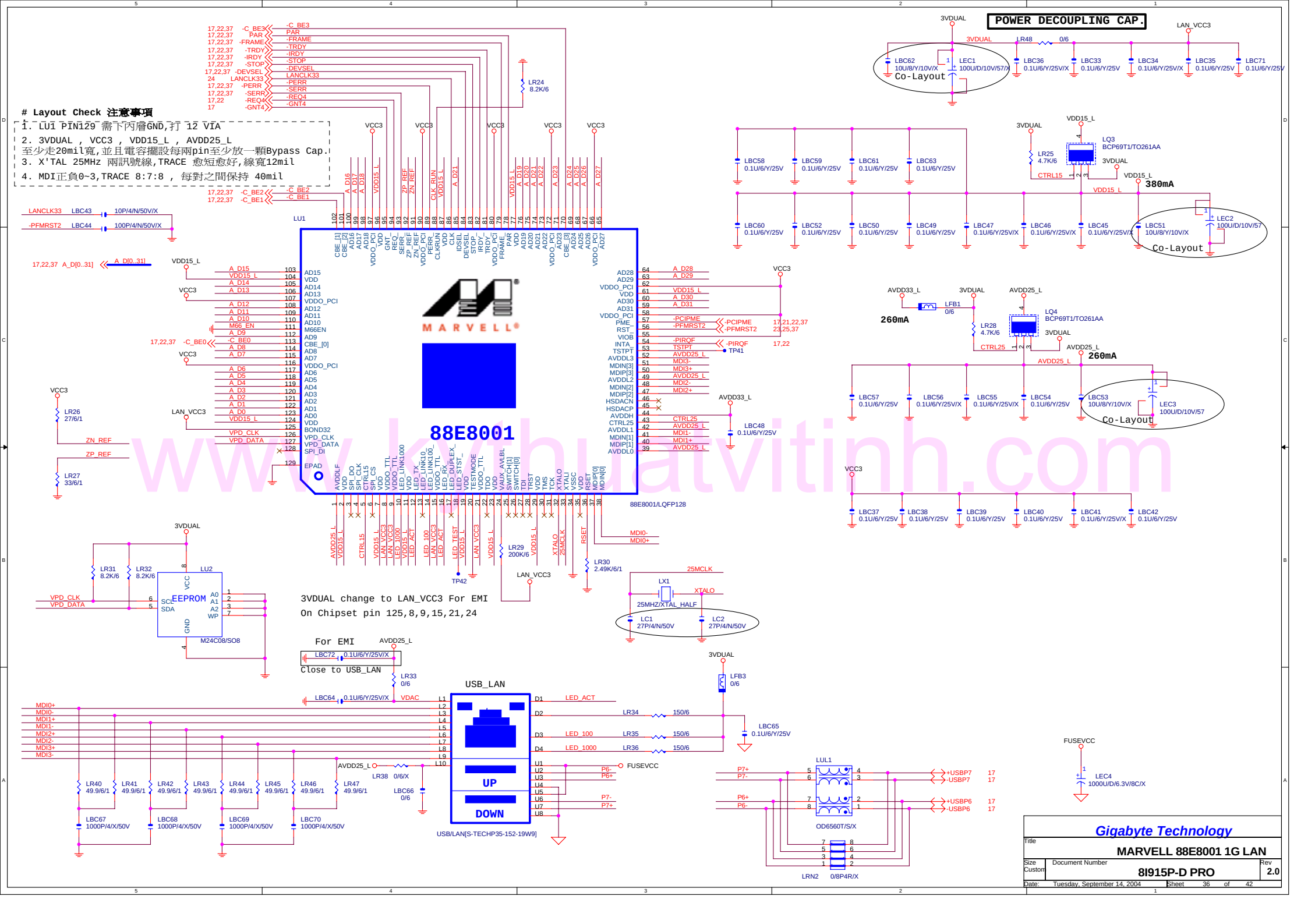
POWER DECOUPLING CAP.
Layout Check 注意事項
1. LU1 PIN129 需下丙層GND,打 12 VIA
2. 3VDUAL , VCC3 , VDD15_L , AVDD25_L
至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8 , 每對之間保持 40mil
88E8001
88E8001/LQFP128
MARVELL
3VDUAL change to LAN_VCC3 For EMI
On Chipset pin 125,8,9,15,21,24
For EMI
Close to USB_LAN
USB_LAN
USB/LAN[S-TECHP35-152-19W9]
EEPROM
M24C08/SO8
OD6560T/S/X
Co-Layout
260mA
380mA
Gigabyte Technology
MARVELL 88E8001 1G LAN
8I915P-D PRO
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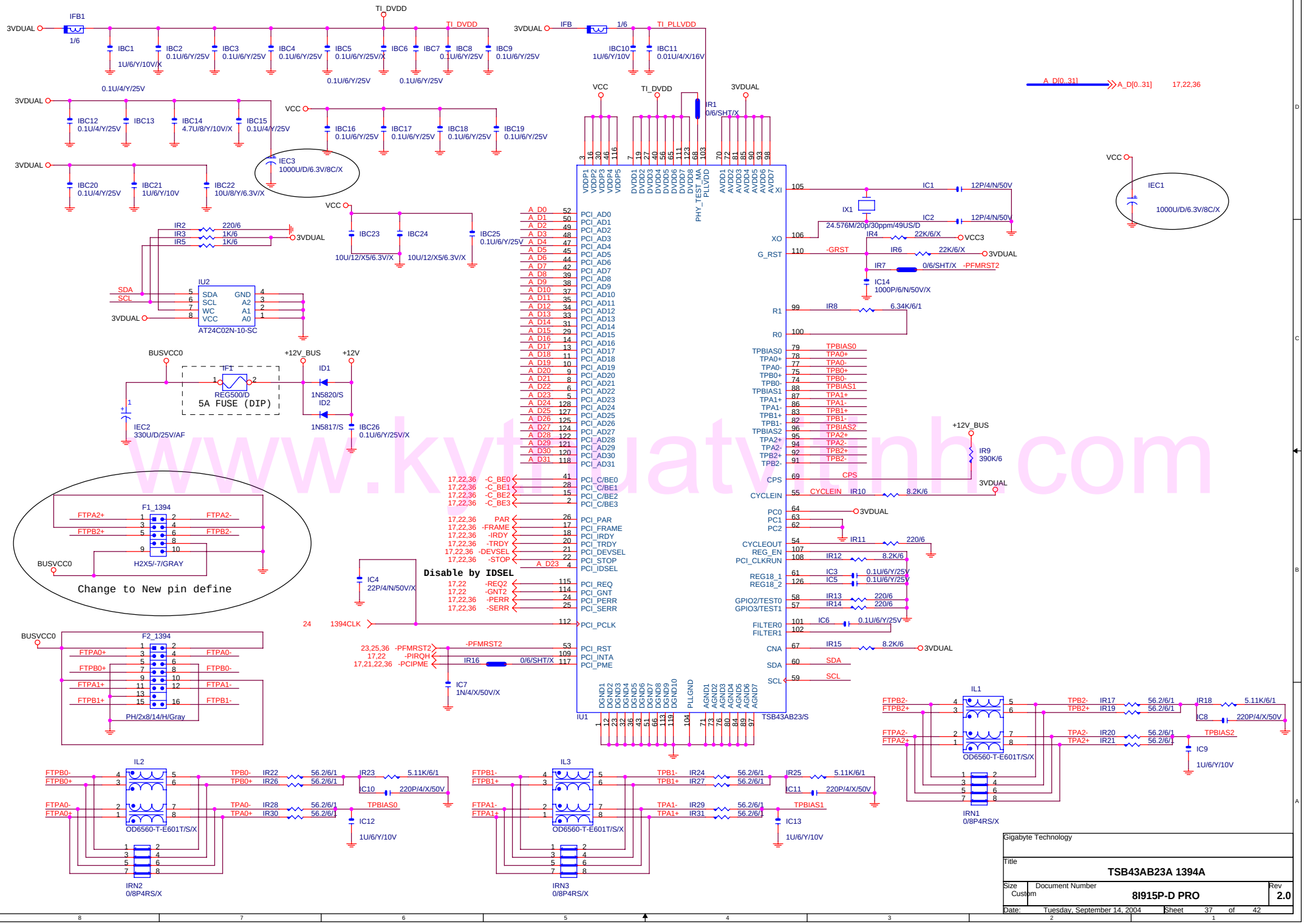

Gigabyte Technology		
Title	TSB43AB23A 1394A	
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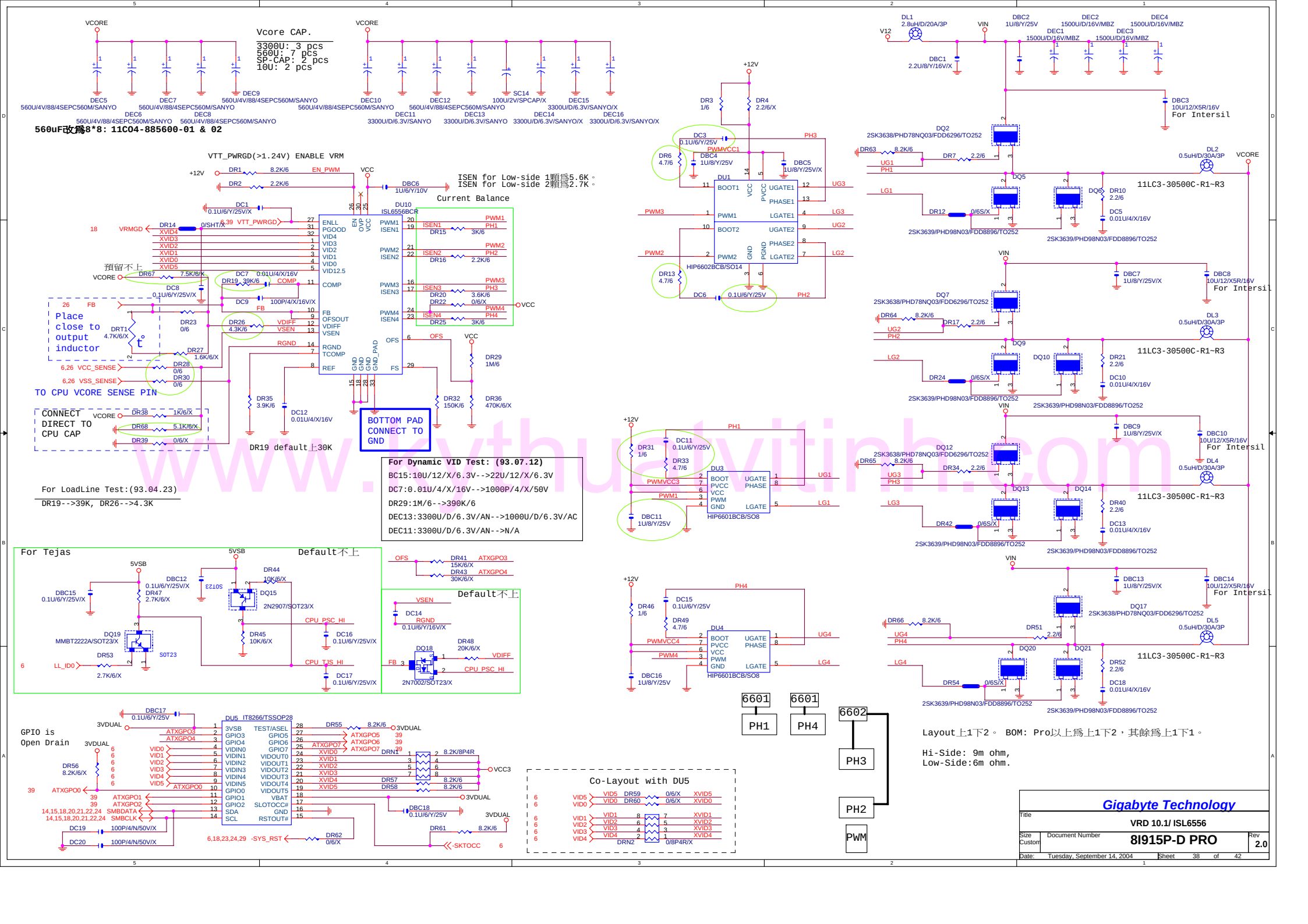
Vcore CAP.
3300U: 3 pcs
560U: 7 pcs
SP-CAP: 2 pcs
10U: 2 pcs
560uF改爲8*8: 11CO4-885600-01 & 02
VTT_PWRGD(>1.24V) ENABLE VRM
ISEN for Low-side 1顆爲5.6K。
ISEN for Low-side 2顆爲2.7K。
Current Balance
預留不上
Place close to output inductor
TO CPU VCORE SENSE PIN
CONNECT DIRECT TO CPU CAP
BOTTOM PAD CONNECT TO GND
DR19 default上30K
For LoadLine Test:(93.04.23)
DR19-->39K, DR26-->4.3K
For Dynamic VID Test: (93.07.12)
BC15:10U/12/X/6.3V-->22U/12/X/6.3V
DC7:0.01U/4/X/16V-->1000P/4/X/50V
DR29:1M/6-->390K/6
DEC13:3300U/D/6.3V/AN-->1000U/D/6.3V/AC
DEC11:3300U/D/6.3V/AN-->N/A
For Tejas
Default不上
Default不上
GPIO is Open Drain
Co-Layout with DU5
6601
PH1
6601
PH4
6602
PH3
PH2
PWM
Layout上1下2。 BOM: Pro以上爲上1下2，其餘爲上1下1。
Hi-Side: 9m ohm,
Low-Side:6m ohm.
Gigabyte Technology
VRD 10.1/ ISL6556
8I915P-D PRO
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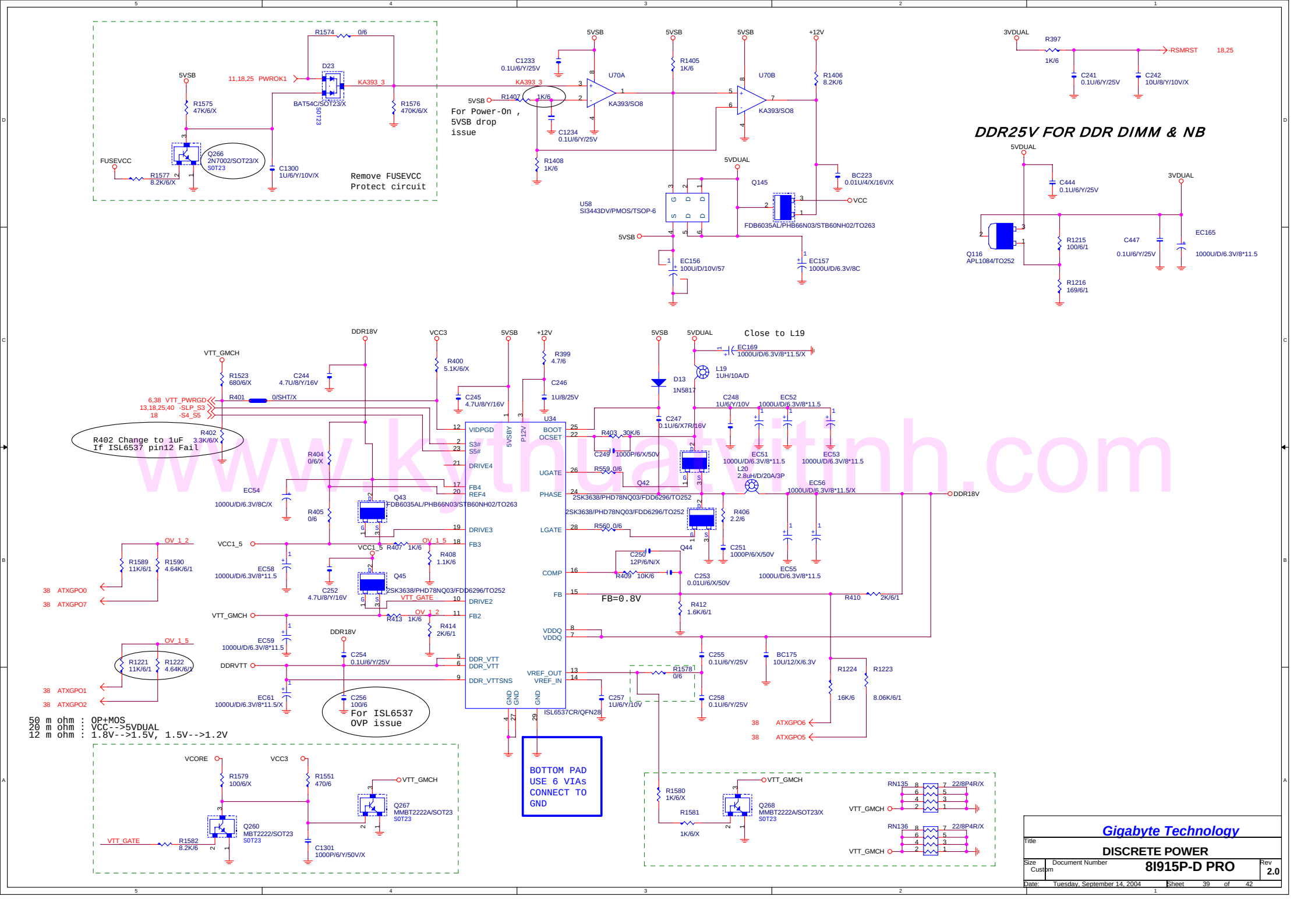

Gigabyte Technology			
Title: DISCRETE POWER			
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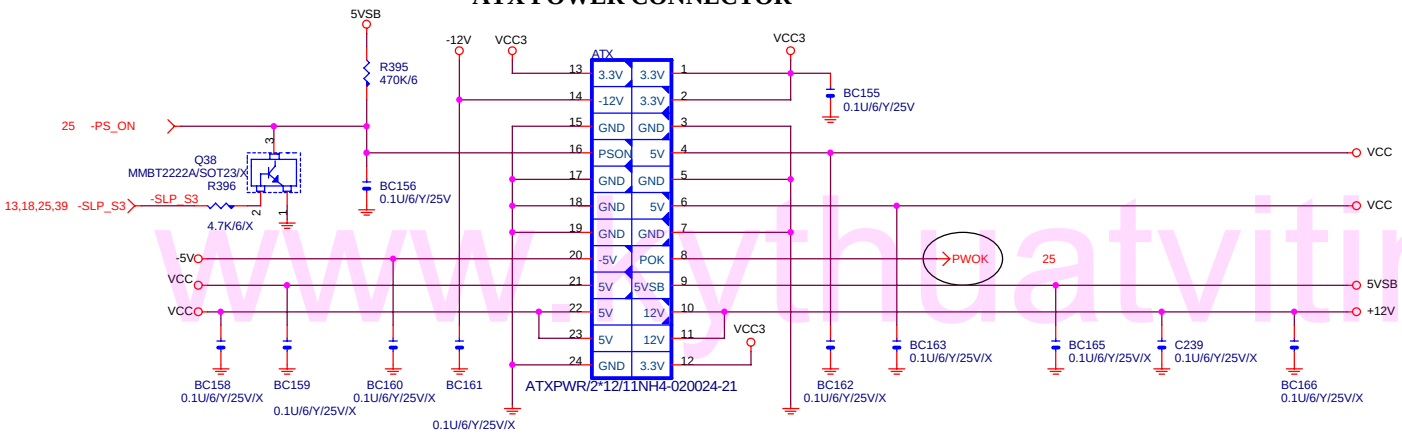
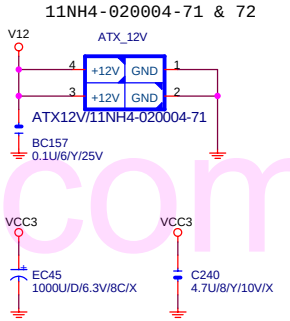
ATX POWER CONNECTOR



11NH4-020024-21 & 22

11NH4-020004-71 & 72



Gigabyte Technology		
Title: ATX POWER CONNECTOR		
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ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GPO48	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GPO49	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP_BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX_DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GPO16	VCC3	CPU OV1 (NC)			
GPO17	VCC3	-GNT5			
GPO18	VCC3	CPU OV2 (NC)			
GPO19	VCC3	DUAL BIOS			
GPO20	VCC3	BIOS T-BLOCK			
GPO21	VCC3	DUAL BIOS			
GPO23	VCC3	DDR OV0 (NC)			
GPIO24	3VDAUL	GREEN LED			
GPIO25	3VDAUL	DDR OV1 (NC)			
GPI26	VCC3	SATA_GP0			
GPIO27	3VDAUL	+PWRLED			
GPIO28	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPIO32	VCC3	BIOS WP			
GPIO33	VCC3	AZALIA DET			
GPIO34	VCC3	PWRLED			
GPI40	V5REF	-REQ4			

PWROK/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

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Title: GPIO/RESET TABLE

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Model Name: 8I915P-D PRO

Version:2.0

AUTOBOM
92/11/11

Component value change history

Date	Change Item	Reason
93.06.24_1.0E	PCI pull-up value change, VCC:2.2K, VCC3:8.2K	
	CKEA0 terminator R609改爲39 ohm.	
	VCC3 mount 2pcs 1000uF cap.(EC31)	For VCC3 -10% fail issue.
93.07.14_1.1A	Support DDRII 600	
	Add FUSEVCC short protect	
	Add VTT_GMCH OV circuit	
	FANPWM3 add damping resistor	
93.08.06_2.0A	-RTCRST change to 20K & 1uF	Follow Intel Recommend
	Add 24AS0-SATAAD-01 (SATA--> IDE)	
	Manual 1.0 change to 2.0	modify SATA1-4 to SATA0-3
93.08.16_2.0A_ECN1	ISL6537 add 10TA1-606537-11 second source	Add ISL6537 second source
93.08.19_2.0B	FUSEVCC改由5VDUAL來轉	Fix USB Device外接電源倒灌issue.
	FUSEVCC短路保護線路阻值修正	Fix some ATX Power can not boot issue.
93.09.14_2.0C	REmove FUSEVCC protect circuit	prevent some condition can not power on issue.

Circuit or PCB layout change for next version

Date	Change Item	Reason
	FB add ICT	
	DU5 add pn1 sign.	

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Title: BOM & PCB MODIFY HISTORY

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