RS880PM-AM VER:1.0.

SCHEMATICS TABLE:

AM3+ Stackup(1080 prepreg,4L)

	Layer Material	OZ	Hight(mm)	Hight(mil)	GECS	Intel-6
	Solder Mask		0.0254	1.00		
	Plating	1.0	0.0356	1.40	1.4~1.9	1.9
L1	Cu	0.5	0.0178	0.7		
	Dielectric(HRC)		0.0686	2.70		
L2	Cu	1.0/2.0	0.03555/0.0711	1.40/2.80		
	Dielectric		1.1379	44.8		
L3	Cu	1.0/2.0	0.03555/0.0711	1.40/2.80		
	Dielectric(HRC)		0.0686	2.70		
L4	Cu	0.5	0.0178	0.7		
	Plating	1.0	0.0356	1.40	1.4~1.9	1.9
	Solder Mask		0.0254	1.00		
		Total	1.5748			

Job	Signature	Date
Schematics Designer	Dennis/Scott	03/08/'11~ 01/08/'11
Layout		03/08/'11
Approval		

PCB STACK: L1:TOP L2:PWR L3:GND L4:BOTTOM

PCB Size : 244x244x1.6mm,4L(62mil=1.57mm),1080-prepreg

(1)47079_2_02 AMD Family 15h Processor Electrical Data Sheet (NDA)_2010-03-xx
(2)46103_rs880_dg_nda_1.06 RS880-Series IGP Motherboard Design Guide (NDA)_2010-09-07
(3)48702_sb9xx_dg_nda_1.00 SB9xx Motherboard Design Guide (NDA)_2010-08-20
(4)Ref.Dory_D(RS880P/SB950) Dory Schematic for AM3r2 (PDF)_2010-11-29

Elitegroup Computer Systems

Title: Cover Page

Size: Custom | Document Number: RS880PM-AM | Rev: 1.0

Date: Thursday, May 26, 2011 | Sheet 1 of 37

Consumer

Follow acer EE V5.21 D.G.

CPU PWM
Intersil 6328CRZ (QFN-48) 29
MP:Apr '11
TDP:95W (reserve 125W)

Int driver*2 → Ext driver*2 → Gate Driver Intersil (SOP-8) 6612ACBZS*2

CPU Vcore 4-phase (only power pack)
- i) H-side 2MOS ii) L-side 2MOS (with heat sink position for H-side) 29
- i) H-side 2MOS ii) L-side 2MOS (with heat sink position for H-side) 29
- 820uF*8

Int driver*1 → **VDDNB 1-phase** (only power pack)
- i) H-side 1MOS ii) L-side 2MOS 29
- 820uF*3

(1-1)AM3+/enable loadline, AM3/disable loadline
(1-2)Dual OCP(TDC/Spike)
(2)PSI_L
(3)APD(Automatic Phase Dropping)
(4)APA(Adaptive Phase Alignment)
(5)DCR current sensing

SVC/D:Serial VID Clock/Data

CPU	AM3(938,45nm)	AM3(938,45nm) AM3+(940,32nm)
Socket	AM3(941) Ivory	AM3b(942) Black

Power Pack	95W 3-Phase	125W 4-Phase
H-Side	1	2
L-Side	2	2
CPU-FAN	3-pin	4-pin

Zambezi AM3+ (做比西河)
Family 15h, 32nm
AMD AM3+ package & AM3b Socket(black,942)
SVI only
Side Band Temp. Sensor I/F only
MT C1E/PSI_L
VDD(Vcore) loadline
Up to 8 cores SCM
TDP:95W/(125W reserve)
Ini. Production:Aug '11 3,4,5,6

Channel A: DDR3 1066, 1333, 1600, 1866 → Blue Unbuffered DDR3 DIMM1 (DIMM4(A0)/DIMM1(A0)), Black Unbuffered DDR3 DIMM2 (DIMM2(A1)) — Layer-4
Channel B: DDR3 1066, 1333, 1600, 1866 (128bit) → Blue Unbuffered DDR3 DIMM3 (DIMM3(B0)), Black Unbuffered DDR3 DIMM4 (DIMM1(B1)/DIMM4(B1)) — Layer-1

ncHT3.0 5.2GT/s Link: OUT / IN 16x16

RS880P(AMD 880G)
HT LINK0 CPU I/F
DX10.1 IGP
TMDS/HDMI
Display Port X2
Side Port Memory
2 X8 PCIE I/F
1 X4 PCIE I/F WITH SB
6 X1 PCIE I/F (FCBGA,528)
TDP:18W PtoP RS780 9,,10,11,12,13
Production: Feb '11

- Rear IO HDMI CON. 19 ← TMDS
- Rear IO VGA CON. 19 ← VGA
- 5.0GT/s PCIE X16 GEN2 I/F → PCIE X 16 SLOT (Black) 20
- PCIE X1(2) GEN2 I/F → NB_GPP_0 / NB_GPP_1
  - PCIE X 1 Slot 1 (White) 20
  - PCIE X 1 Slot 2 (White) 20

(1)Hybrid Crossfire : support (onboard + PCIEx16)
(2)Surround view : support

A-Link GEN 2(4X PCIE)

SB950
4 X 1 PCIE GEN2 I/F
USB2.0 (14)+ 1.1(2)
SATA3.0 (6 PORTS)
INT CLK GEN
GBMAC
AZALIA HD AUDIO
LPC I/F(S5)
SPI I/F
ACPI 1.1
HW Monitor — Not PtoP SB700
PCI/PCI BDGE — TDP:6W
INT RTC (FCBGA,605)
EC 14,15,16,17,18
Production: Feb '11

- HD AUDIO I/F → HD AUDIO 26
  - Rear IO HD AUDIO 27
  - Header (H5x2,Purple) HD AUDIO 27
  - Header (H1x4,black) SPDIFO Near PCIEX16 (reserve) 27
- SATA3.0 (6Gb/s) I/F — RAID 0,1,5,10 eSATA*6 port
  - SATA#1 (All black) 16
  - SATA#2 16
  - SATA#3 16
  - SATA#6 (reserve) 16
  - SATA#5 16
  - SATA#4 16

PS:SATA2.0 and SATA3.0 has different footprint.

- SPI I/F → SPI ROM (32Mb) 16
- PCI → PCI Slot 1 (White) 22
- LPC I/F → Super IO Fintek F71869A EuP,G3 to S5(RI1#,VBAT) (LQFP128) 23
  - HW Monitor I/F ← HW Monitor: (1)Internal: 3.3V/5VSB/VBAT (2)External:CPU core/1.1V/5V/12V (3)CPU/SYS/Vcore MOS temperature detect. (4)CPU(AM3/AM3+) Temperature detect SB-TSI 23
  - PS/2 → KB&MS 24

- USB 2.0 → Rear IO (w/LAN) USB 0 / USB 1 21; Rear IO USB 5 / USB 4 / USB 3 / USB 2 21 — S4/S4 wo 5V_Dual
- USB 2.0 → Header 21: USB 6/7 (Black), USB 8/9 (H5x2,Yellow), USB 10/11 (Black), USB 12/13 (reserve) — For card reader. — S4/S4 wo 5V_Dual
- PCIE X1 GEN2 I/F → SB_GPP_0 → Giga LAN RTL8111E-VL (QFN48) 25 → Rear IO LAN CON. 25
- PCIE X1 GEN2 I/F → SB_GPP_1 → USB3.0 Host Etron EJ168 (TQFP100) 28 → Rear IO USB3.0 CON. (2 ports) 28 — USB 2.0(480Mb/s) USB 3.0(5Gb/s) — S4/S4 wo 5V_Dual

WOL:Enable LAN LED(Rear Side)

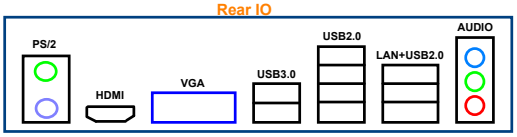
LAN	LED	S0/S1	S3	S4/S5
Rear Side	Active-LED (Single Color)	Access:Blink (WOL:Disable, S0=Blink, S1=OFF) Others:OFF	Access:Blink Others:OFF	Access:Blink Others:OFF
	Speed-LED (Dual Color)	Disconnected:OFF 1000 :ON with A color: Amber 100 :ON with A color: Green 10 :OFF	OFF	OFF

ErP lot 6.0 (2010, SYS<1W)	Sleep State	WOL	Commercial Project
Disable Enable(X)	S1/S3/S4/S5 S1/S3/S4	Support Support	"After G3" required

PS:2013(SYS<0.5W) is better.

	USB	PS/2
S0	VCC5	VCC5
S1	VCC5	VCC5
S3	5VSB	5VSB
S4/S5	0V	0V

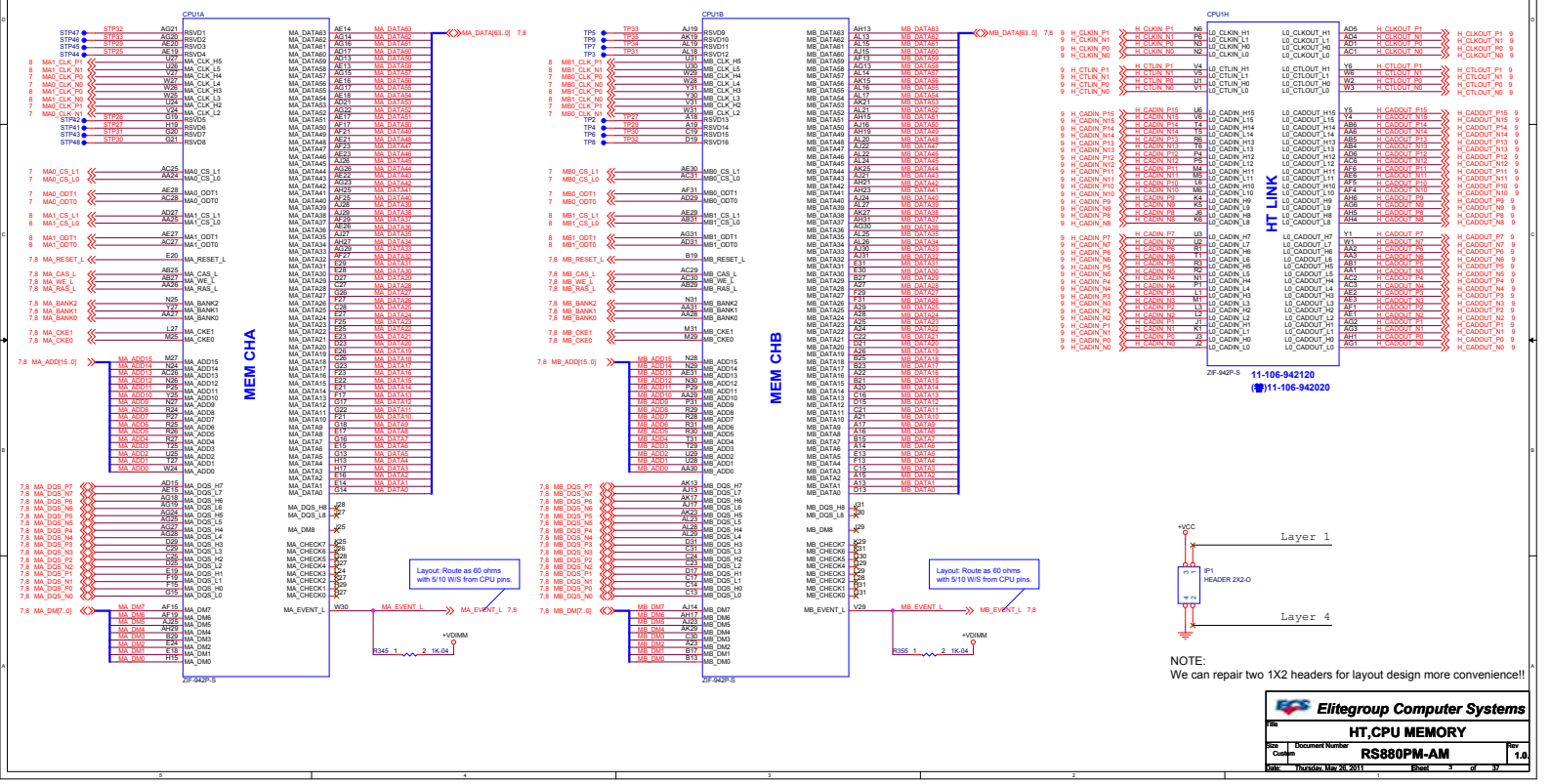
Rear IO



Elitegroup Computer Systems

Title: BLOCK DIAGRAM
Size: Custom | Document Number: RS880PM-AM | Rev: 1.0
Date: Thursday, May 26, 2011 | Sheet 2 of 37

CPU Memory



NOTE:
We can repair two 1X2 headers for layout design more convenience!!

Elitegroup Computer Systems			
Title: HT,CPU MEMORY			
Size: Custom	Document Number: RS880PM-AM		Rev: 1.0
Date: Thursday, May 26, 2011	Sheet 3 of 37		

CPU Control and Miscellaneous

CPU	AM3	AM3+
Core_Type (G5-pin)	GND	floating
Droop Control	Disable (100K)	Enable (0 ohm)
Offset Control	Disable	Enable (35 mV)

Note: Update with new clock termination scheme, if necessary.

SIC:Sideband Temperature Sensor I/F Clock

Place witin 500 mils of the CPU socket.

FDV301N-S 03-050-530106

74AUP1G07GW (02-197-007131) OD-BUFFER(NEED PULL HIGH)

Vgs(th)=1.2v

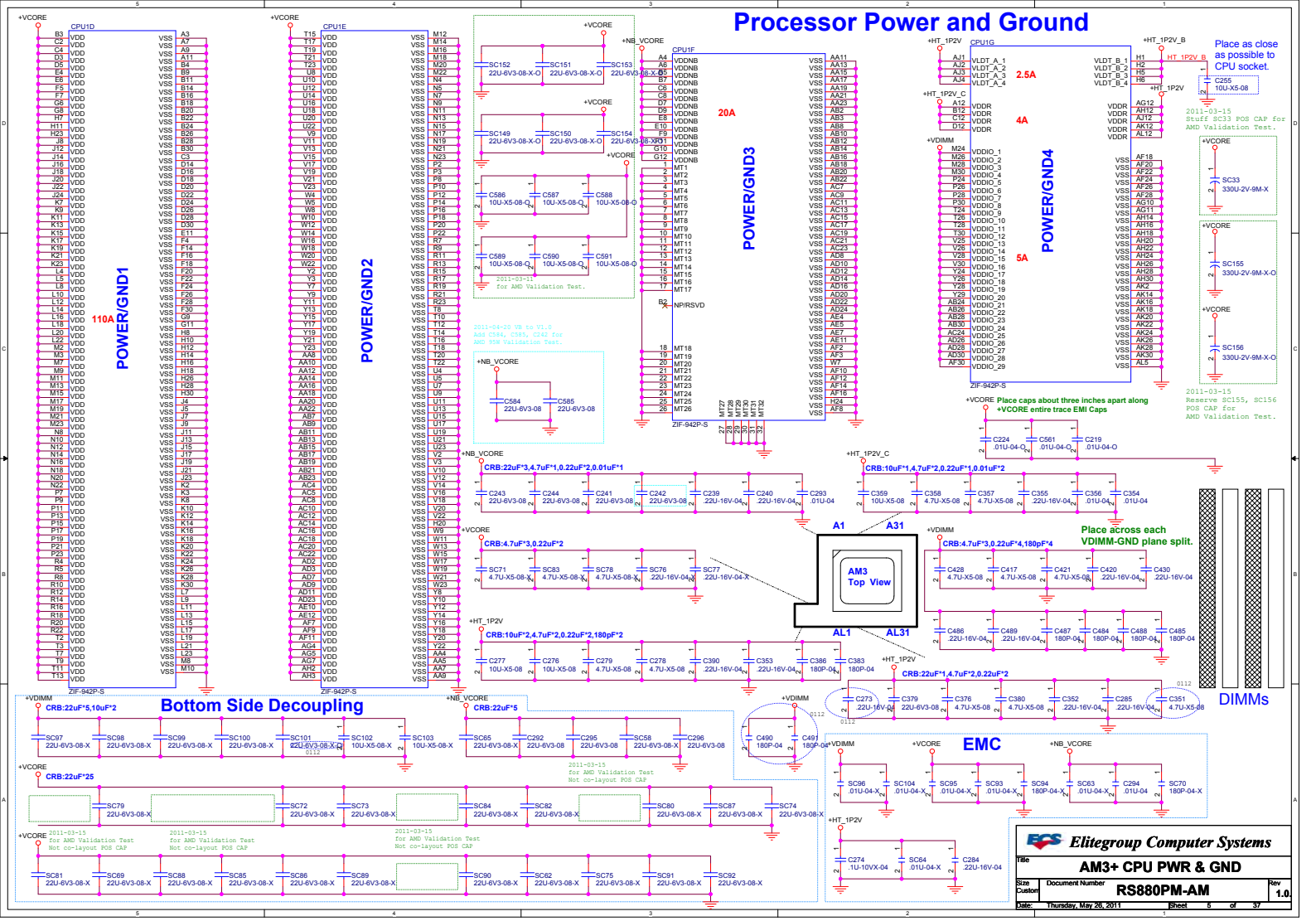
Elitegroup Computer Systems

Title: CPU CONTROL & MISC

Size: Custom | Document Number: RS880PM-AM | Rev: 1.0

Date: Thursday, May 26, 2011 | Sheet 4 of 37

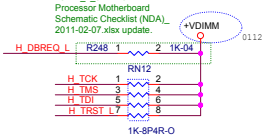
Processor Power and Ground



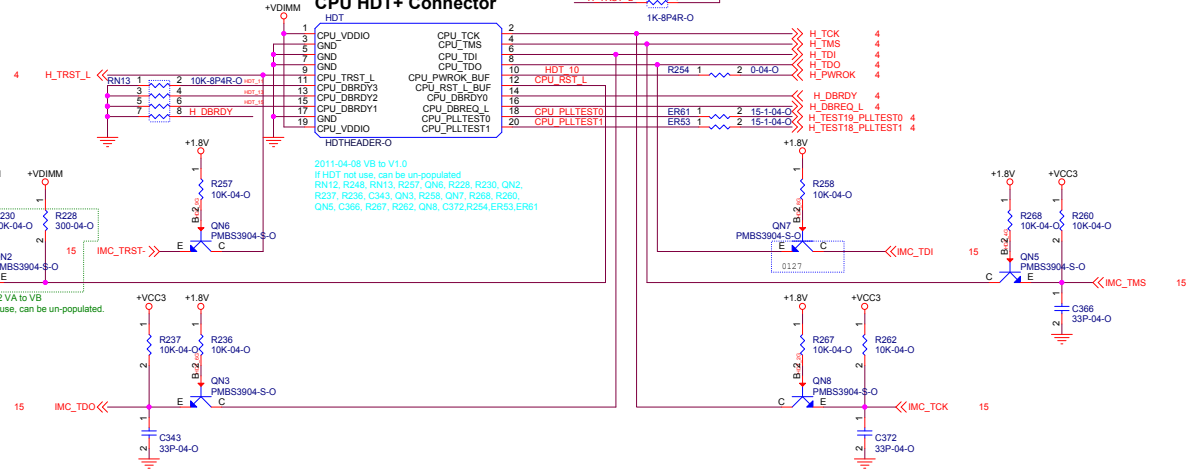
HDT:Hardware Debug Tool

11-106-942120
(替)11-106-942020

2011-03-08 VA to VB
48121_1_02 AM3r2
Processor Motherboard
Schematic Checklist (NDA)_
2011-02-07.xlsx update.



CPU HDT+ Connector



Elitegroup Computer Systems		
Title: HDT		
Size: Custom	Document Number: RS880PM-AM	Rev: 1.0
Date: Thursday, May 26, 2011	Sheet 6 of 37	

2011-05-13 V1.0 to V1.0(.)
DIMM1 rename to DIMM4 for meet Acer spec

silkscreen	Channel
DIMM1	CHA,MA0 SA1,0=0,0
DIMM2	CHA,MA1 SA1,0=1,0
DIMM3	CHB,MB0 SA1,0=0,1
DIMM4	CHB,MB1 SA1,0=1,1

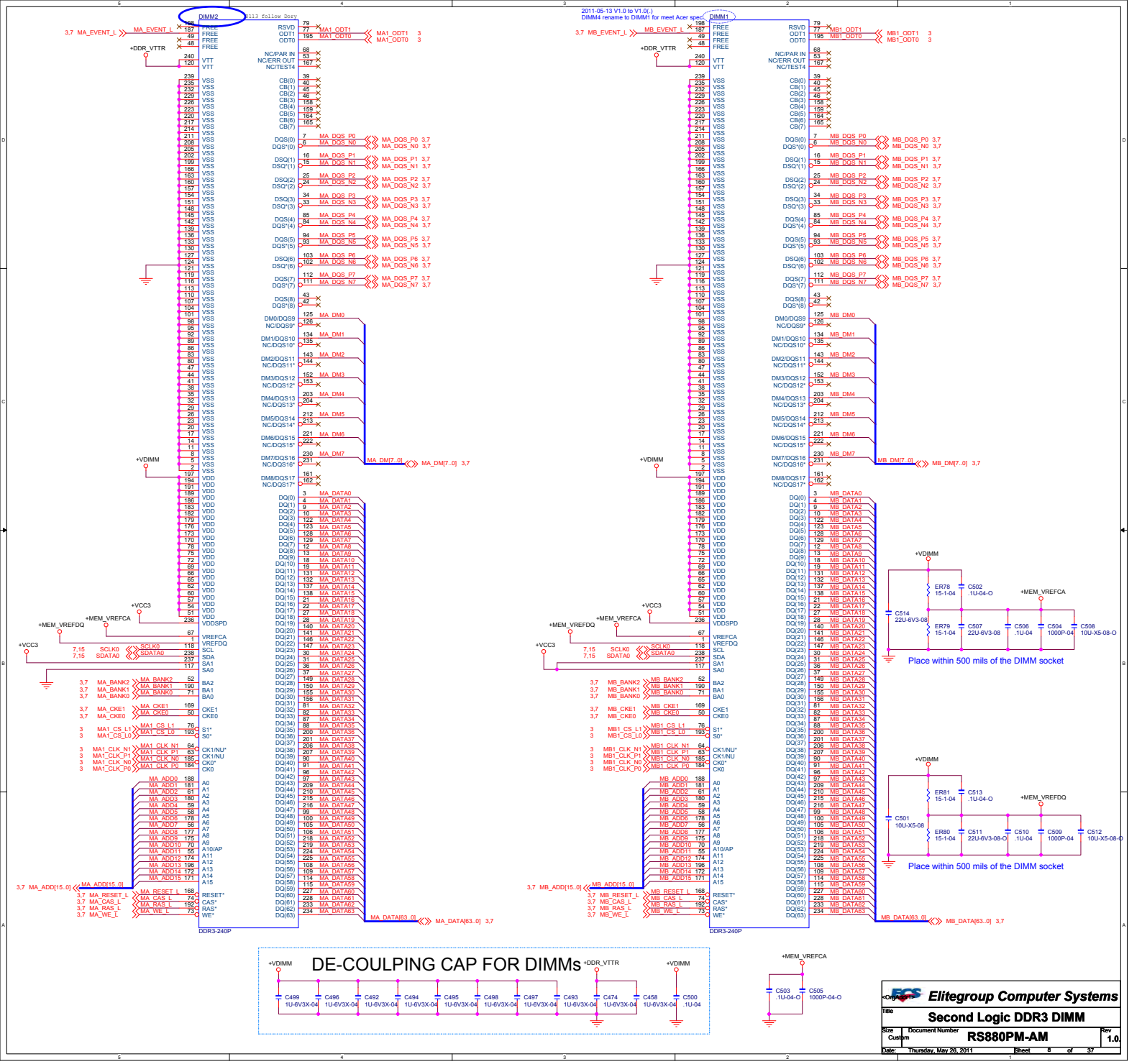
Dual Ch (A+B) same color.

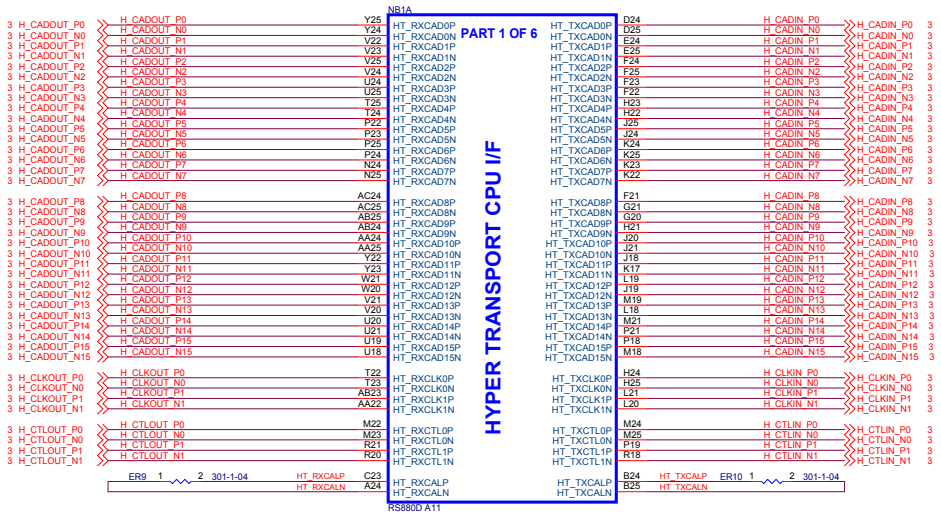
Elitegroup Computer Systems

Title: First Logic DDR3 DIMM

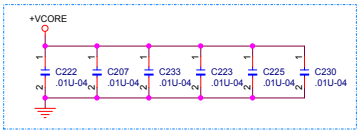
Size	Document Number	Rev
Custom	RS880PM-AM	1.0

Date: Thursday, May 26, 2011 Sheet 7 of 37

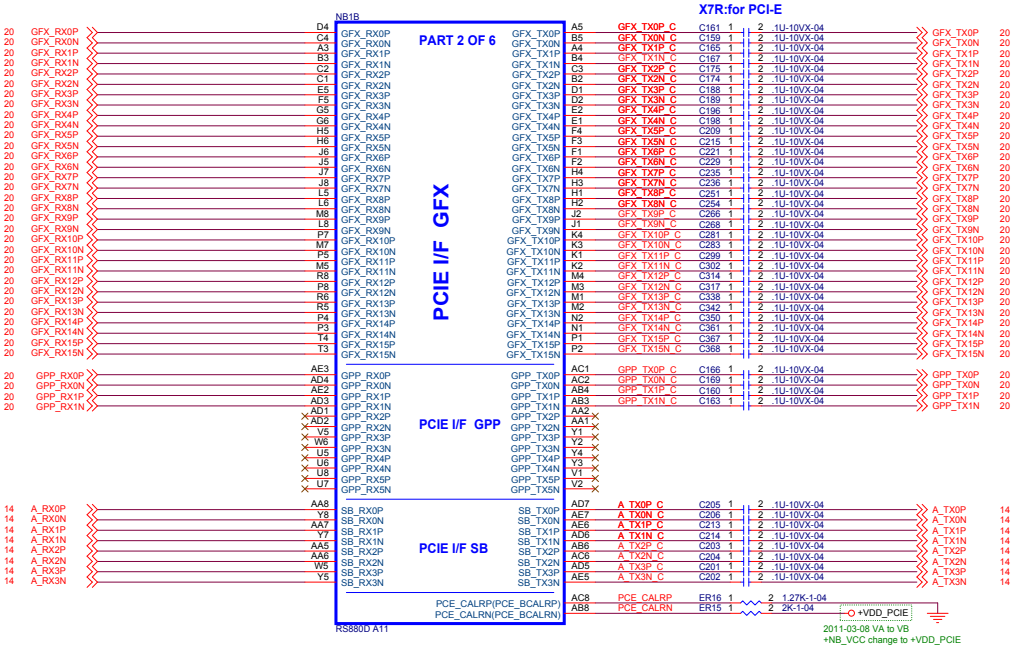

DIMM2
2013 follow Dory
DIMM1
2011-05-13 V1.0 to V1.0(.)
DIMM4 rename to DIMM1 for meet Acer spec.
DDR3-240P
DE-COULPING CAP FOR DIMMs
Place within 500 mils of the DIMM socket
Place within 500 mils of the DIMM socket



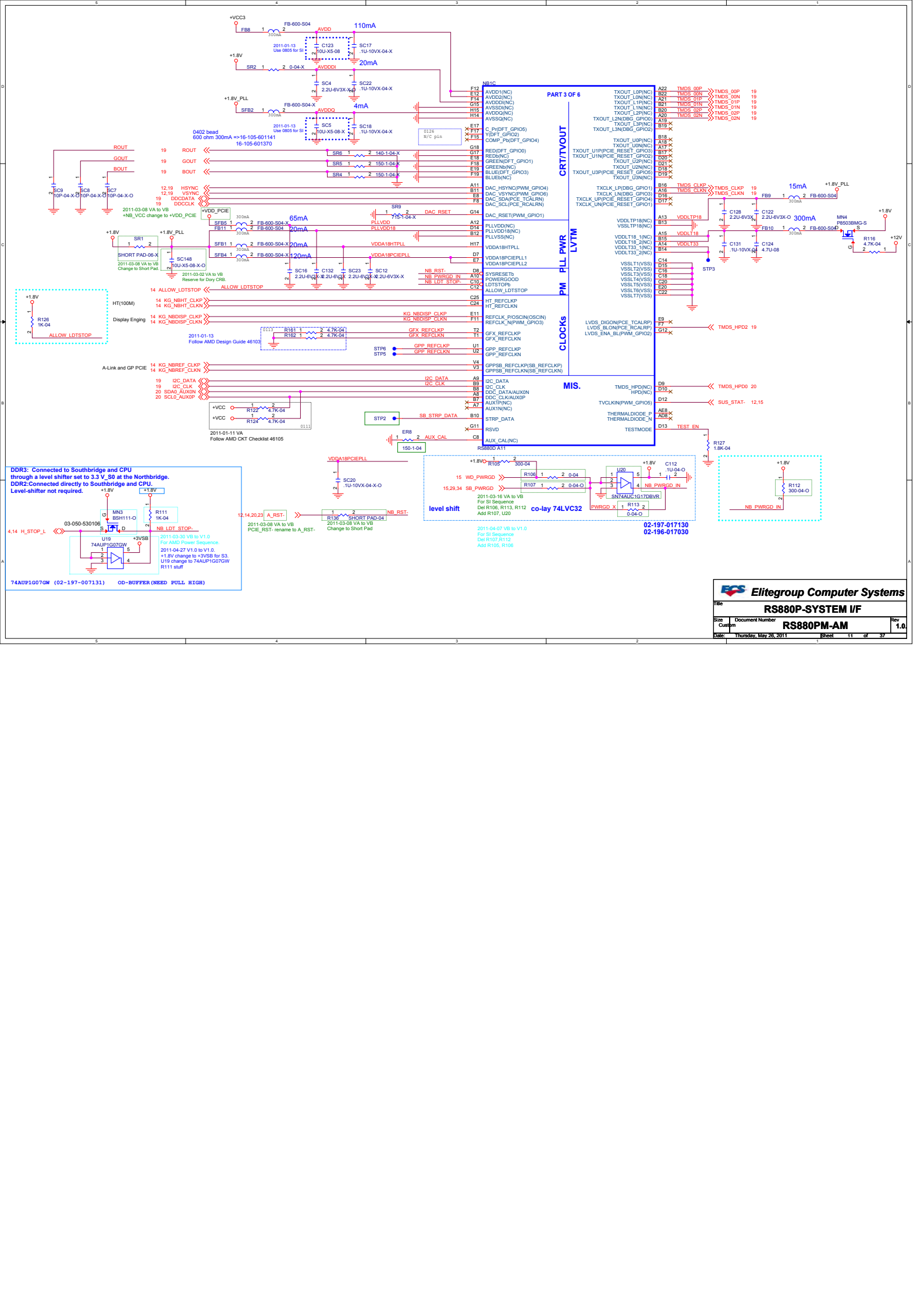
HT LINK STITCHING CAPS.



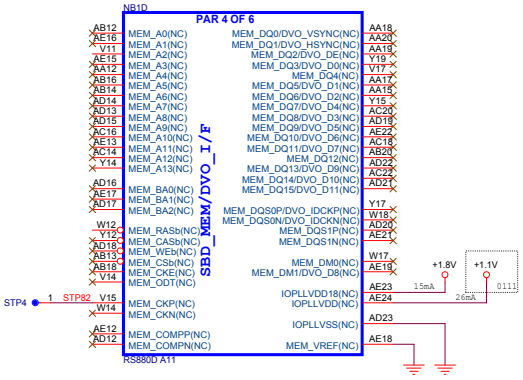
Elitegroup Computer Systems		
Title: RS880P-HT LINK I/F		
Size: Custom	Document Number: RS880PM-AM	Rev: 1.0
Date: Thursday, May 26, 2011	Sheet 9 of 37	

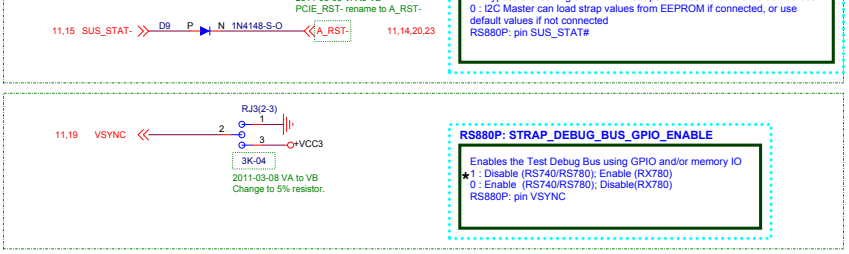


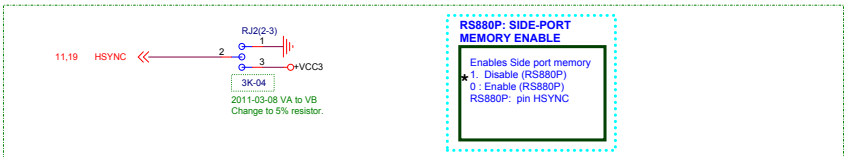
Elitegroup Computer Systems			
Title: RS880P-PCIE I/F			
Size: Custom	Document Number: RS880PM-AM		Rev: 1.0
Date: Thursday, May 26, 2011	Sheet 10 of 37		


NB1C
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.
RS880D A11
DDR3: Connected to Southbridge and CPU
through a level shifter set to 3.3 V_S0 at the Northbridge.
DDR2:Connected directly to Southbridge and CPU.
Level-shifter not required.
74AUP1G07GW (02-197-007131) OD-BUFFER(NEED PULL HIGH)
level shift
co-lay 74LVC32
02-197-017130
02-196-017030
Elitegroup Computer Systems
RS880P-SYSTEM I/F
RS880PM-AM
Thursday, May 26, 2011

RS880P STRAPS







Elitegroup Computer Systems

Title: RS880P-SPMEM/STRAPS

Size	Document Number	Rev
Custom	RS880PM-AM	1.0

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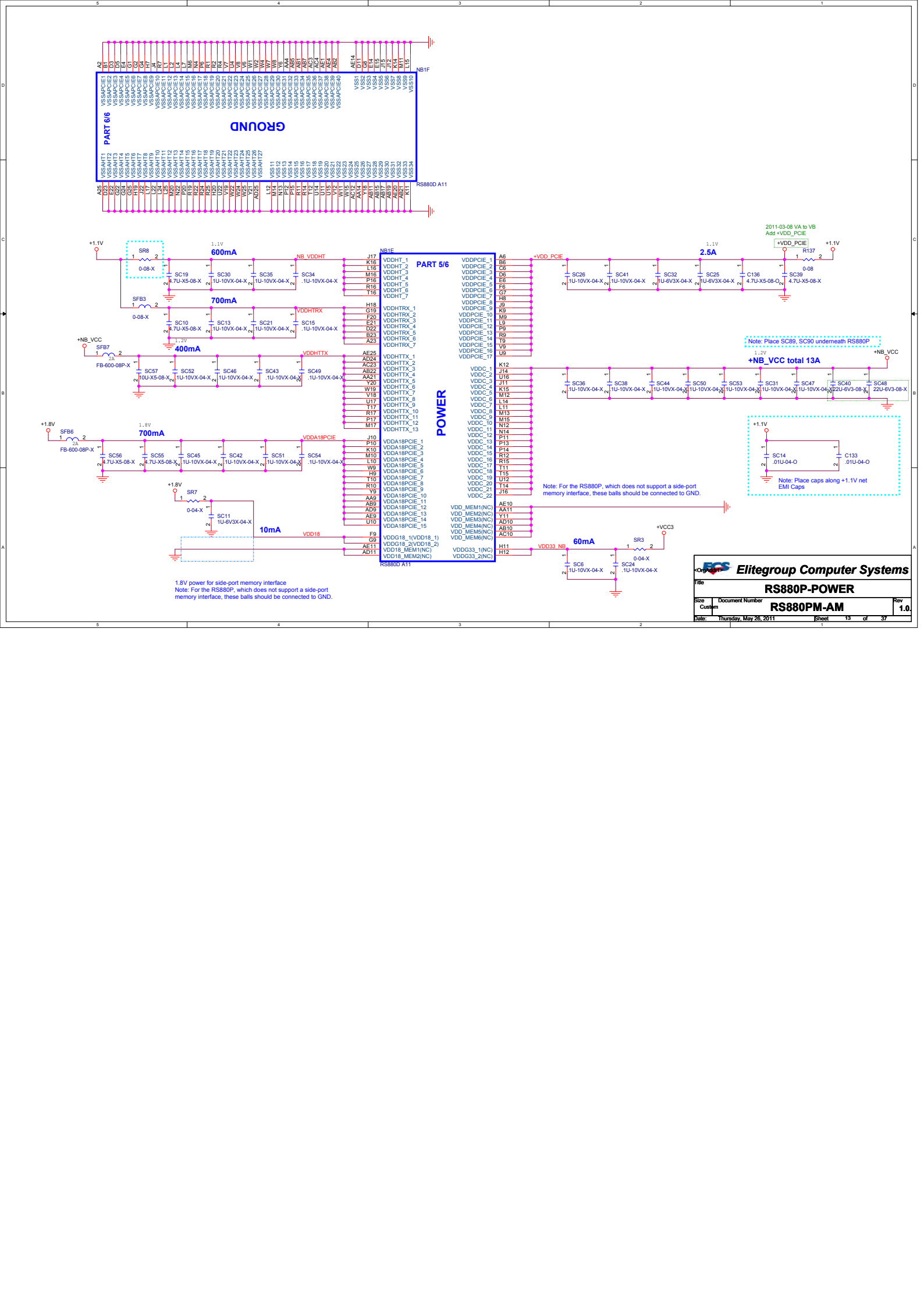
PART 6/6
GROUND
NB1F
RS880D A11
PART 5/6
POWER
NB1E
RS880D A11
2011-03-08 VA to VB
Add +VDD_PCIE
+1.1V
600mA
700mA
400mA
2.5A
+NB_VCC total 13A
+1.8V
700mA
10mA
60mA
+VCC3
+NB_VCC
+VDD_PCIE
NB_VDDHT
VDDHTRX
VDDHTTX
VDDA18PCIE
VDD18
VDD33_NB
Note: Place SC89, SC90 underneath RS880P
Note: Place caps along +1.1V net
EMI Caps
Note: For the RS880P, which does not support a side-port
memory interface, these balls should be connected to GND.
1.8V power for side-port memory interface
Note: For the RS880P, which does not support a side-port
memory interface, these balls should be connected to GND.
Elitegroup Computer Systems
RS880P-POWER
RS880PM-AM
Rev 1.0
Thursday, May 26, 2011
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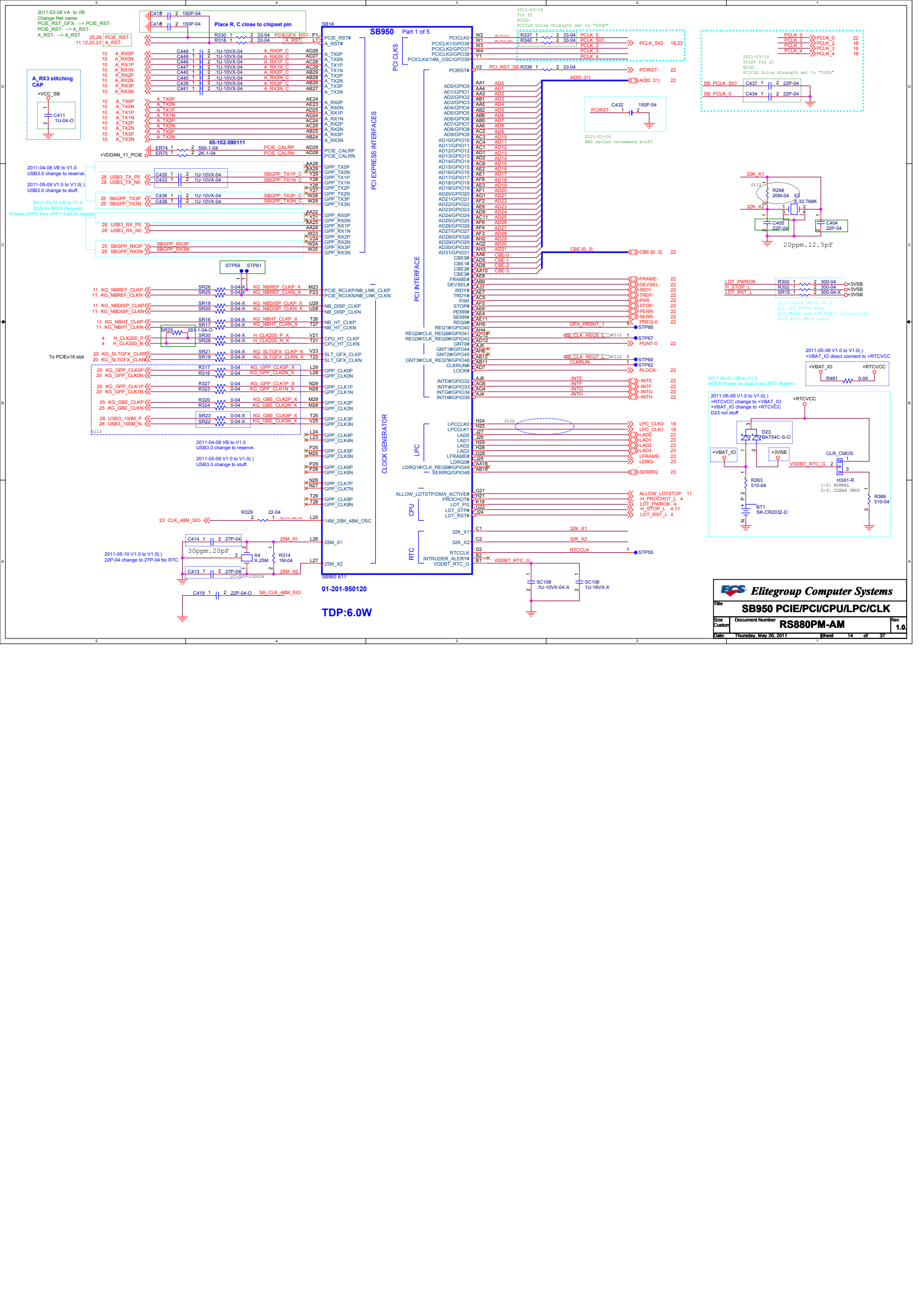
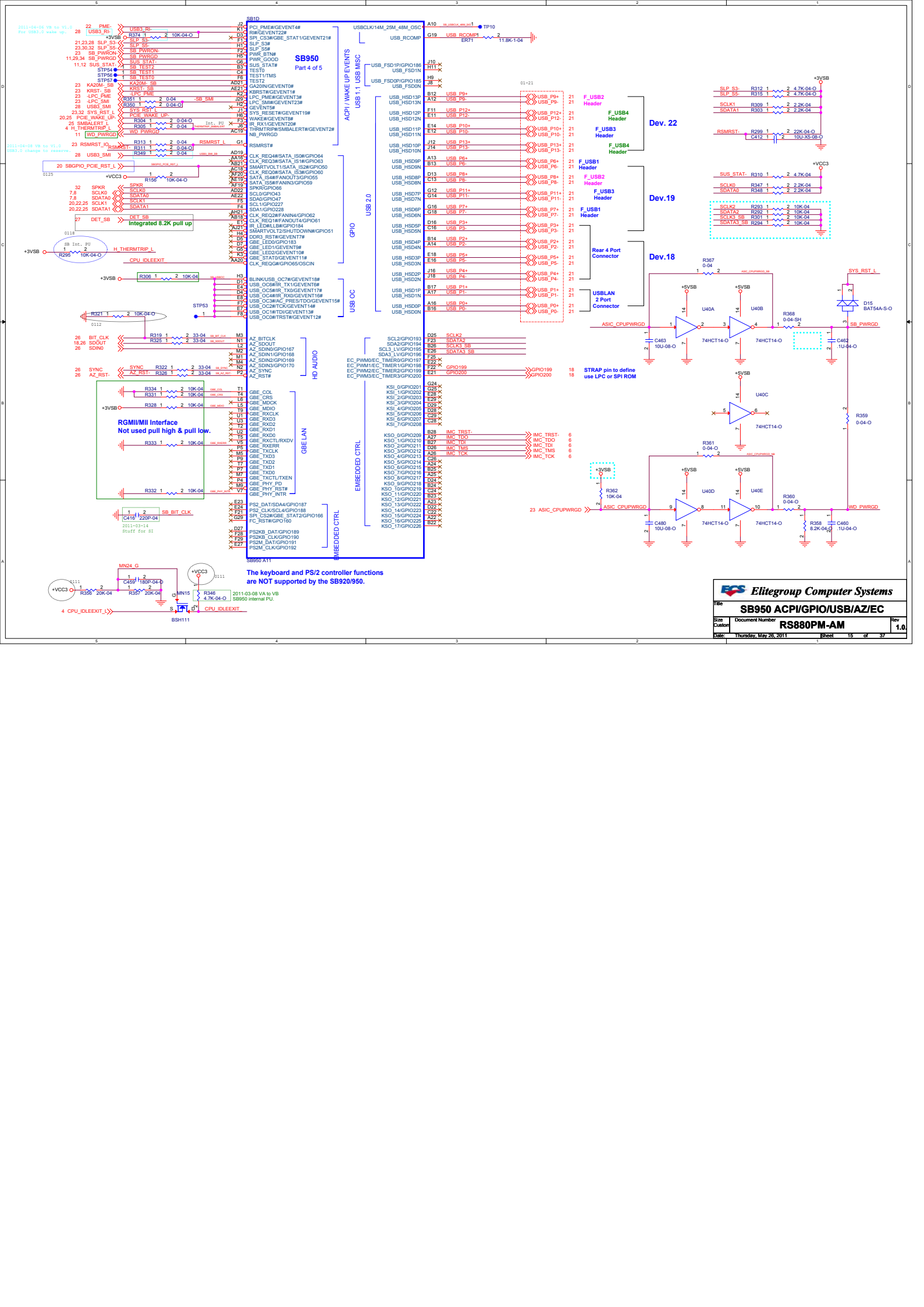
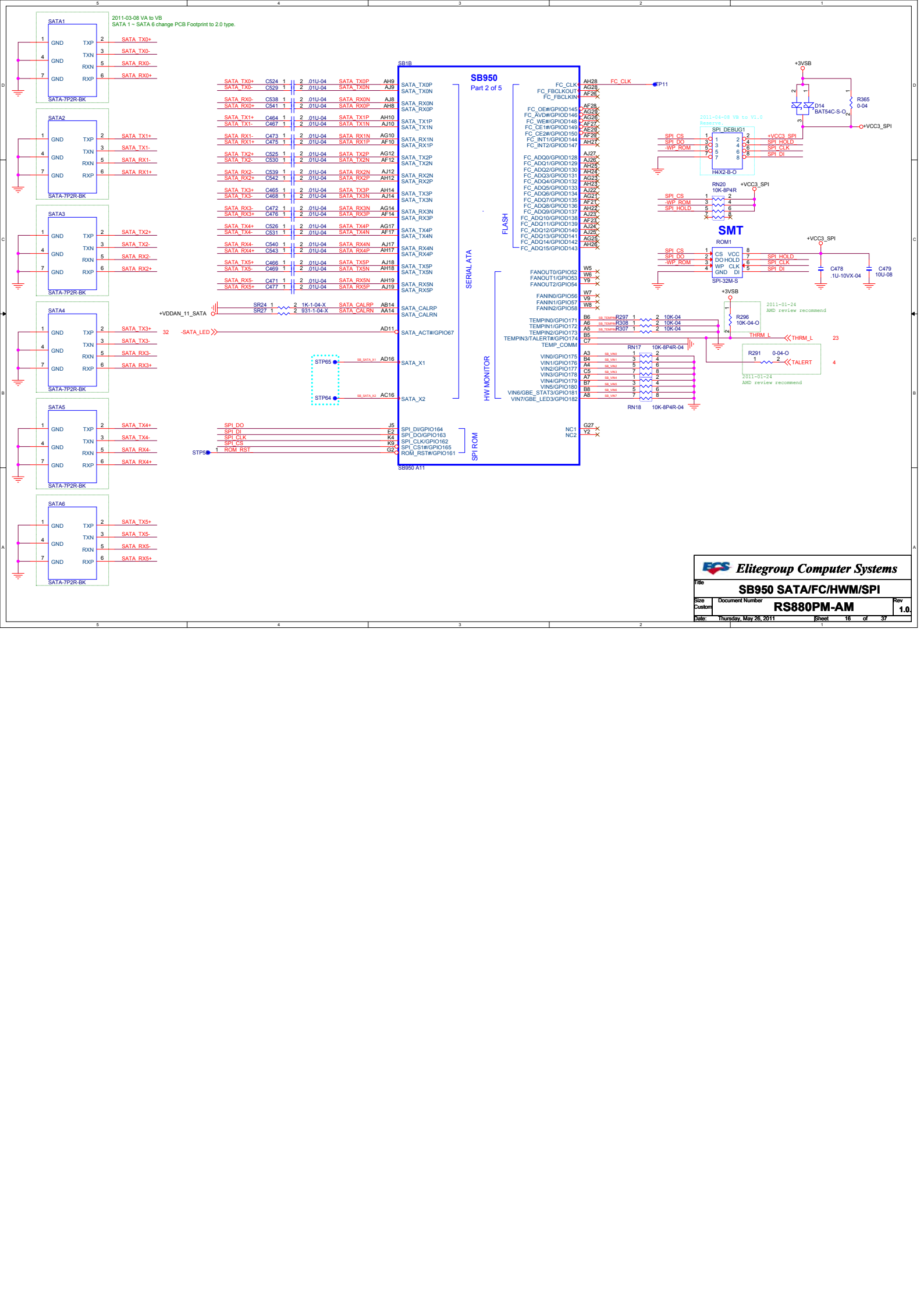
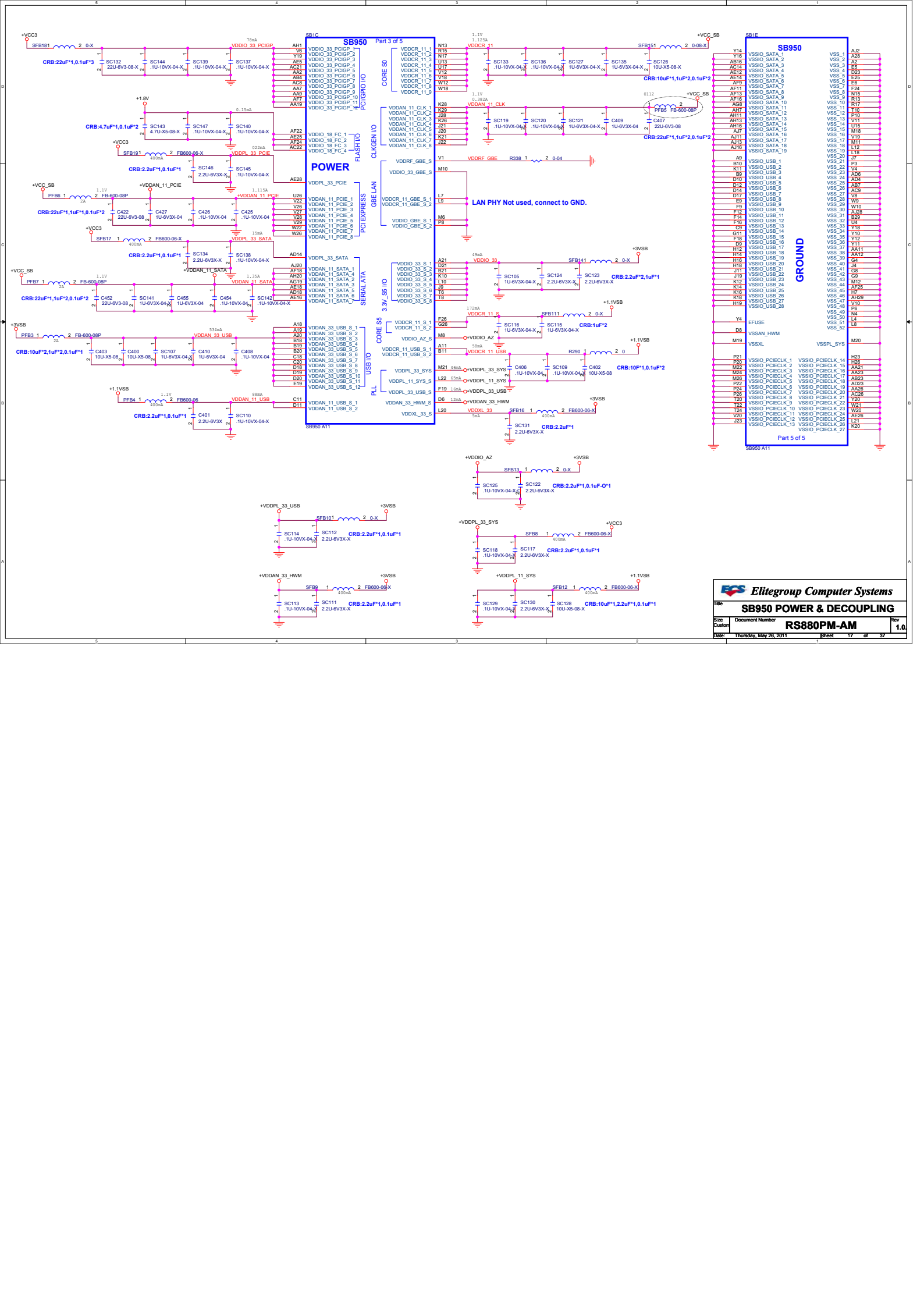

SB950
Part 1 of 5
SB950 A11
01-201-950120
TDP:6.0W
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
Elitegroup Computer Systems
SB950 PCIE/PCI/CPU/LPC/CLK
RS880PM-AM
Rev 1.0
Thursday, May 26, 2011


SB950
Part 4 of 5
SB1D
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
Integrated 8.2K pull up
RGMII/MII Interface
Not used pull high & pull low.
The keyboard and PS/2 controller functions
are NOT supported by the SB920/950.
SB950 A11
Dev. 22
Dev.19
Dev.18
F_USB2 Header
F_USB4 Header
F_USB3 Header
F_USB1 Header
Rear 4 Port Connector
USBLAN 2 Port Connector
STRAP pin to define use LPC or SPI ROM
Elitegroup Computer Systems
SB950 ACPI/GPIO/USB/AZ/EC
RS880PM-AM
Thursday, May 26, 2011


2011-03-08 VA to VB
SATA 1 ~ SATA 6 change PCB Footprint to 2.0 type.
SATA1
SATA2
SATA3
SATA4
SATA5
SATA6
SATA-7P2R-BK
SB1B
SB950
Part 2 of 5
SERIAL ATA
FLASH
HW MONITOR
SPI ROM
SB950 A11
SMT
ROM1
SPI-32M-S
SPI_DEBUG1
H4X2-B-O
Elitegroup Computer Systems
SB950 SATA/FC/HWM/SPI
RS880PM-AM
Thursday, May 26, 2011


SB950
Part 3 of 5
POWER
LAN PHY Not used, connect to GND.
SB950 A11
GROUND
Part 5 of 5
Elitegroup Computer Systems
SB950 POWER & DECOUPLING
RS880PM-AM
Rev 1.0
Thursday, May 26, 2011
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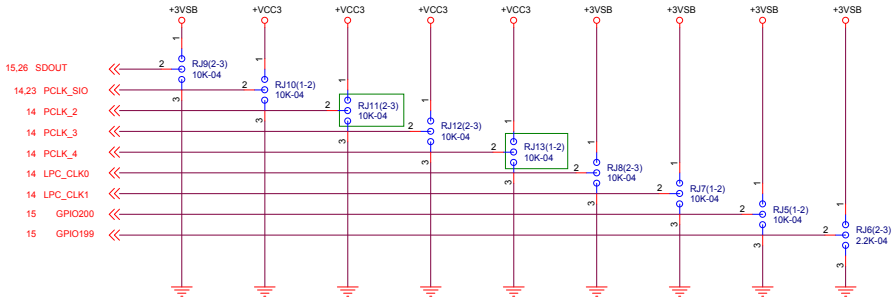

REQUIRED STRAPS

This strap is not used if the strap CLKGEN is configured for external clock generator mode.

	AZ_SDOUT	PCLK_SIO	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GP200 GP199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2 * DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	Required setting for integrated clock mode * DEFAULT	EC ENABLED	Internal CLOCK MODE * DEFAULT	ROM TYPE: H, H = Reserved H, L = SPI ROM * DEFAULT L, H = LPC ROM L, L = FWH ROM
PULL LOW	Performance Mode * DEFAULT	FORCE PCIE GEN1	Watchdog Timer Disabled * DEFAULT	IGNORE DEBUG STRAP * DEFAULT	Reserved	EC DISABLED * DEFAULT	External CLOCK MODE	

Elitegroup Computer Systems

Title: SB950 STRAPS

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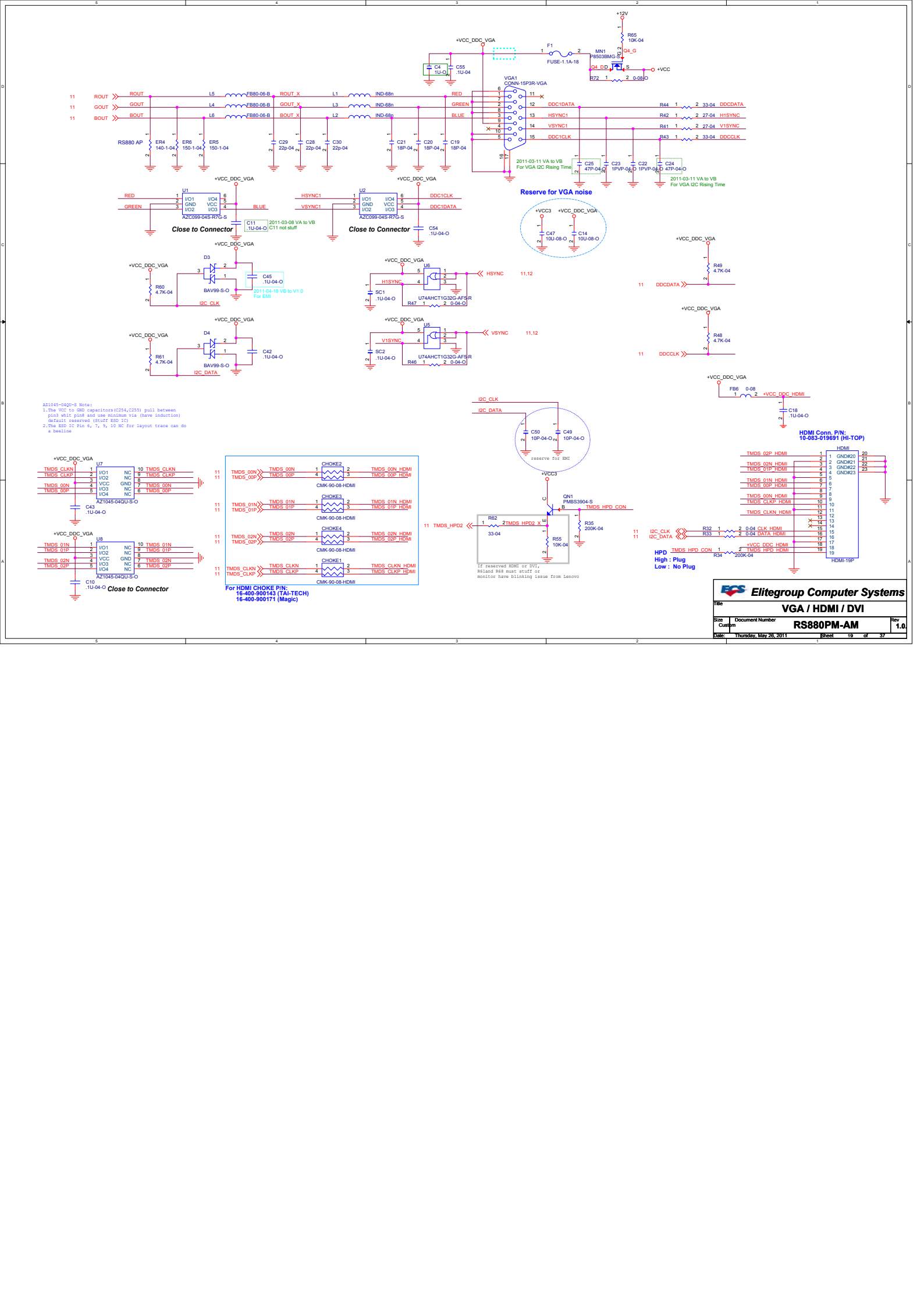
+12V
R65 10K-04
Q4_G
MN1 P8503BMG-S
Q4_DD
S
+VCC
R72 0-08
F1
FUSE-1.1A-18
+VCC_DDC_VGA
C4 1U-O
C55 .1U-04
VGA1 CONN-15P3R-VGA
ROUT
GOUT
BOUT
RS880 AP
ER4 140-1-04
ER6 150-1-04
ER5 150-1-04
L5 FB80-06-B
L4 FB80-06-B
L6 FB80-06-B
ROUT_X
GOUT_X
BOUT_X
L1 IND-68n
L3 IND-68n
L2 IND-68n
RED
GREEN
BLUE
C29 22p-04
C28 22p-04
C30 22p-04
C21 18P-04
C20 18P-04
C19 18P-04
DDC1DATA
HSYNC1
VSYNC1
DDC1CLK
R44 33-04 DDCDATA
R42 27-04 H1SYNC
R41 27-04 V1SYNC
R43 33-04 DDCCLK
2011-03-11 VA to VB
For VGA I2C Rising Time
C25 47P-04-O
C23 1PVP-04-O
C22 1PVP-04-O
C24 47P-04-O
U1
AZC099-04S-R7G-S
Close to Connector
C11 .1U-04-O
2011-03-08 VA to VB
C11 not stuff
U2
Close to Connector
C54 .1U-04-O
Reserve for VGA noise
+VCC3
C47 10U-08-O
C14 10U-08-O
D3
BAV99-S-O
R60 4.7K-04
I2C_CLK
C45 .1U-04-O
2011-04-18 VB to V1.0
For EMI
U6
HSYNC
H1SYNC
SC1 .1U-04-O
U74AHCT1G32G-AF5-R
R47 0-04-O
11,12
D4
R61 4.7K-04
I2C_DATA
C42 .1U-04-O
U5
V1SYNC
SC2 .1U-04-O
VSYNC
R46 0-04-O
R49 4.7K-04
DDCDATA
R48 4.7K-04
DDCCLK
FB6 0-08
+VCC_DDC_HDMI
C18 .1U-04-O
AZ1045-04QU-S Note:
1.The VCC to GND capacitors(C254,C255) pull between
pin3 whit pin8 and use minimum via (have induction)
default reserved (Stuff ESD IC)
2.The ESD IC Pin 6, 7, 9, 10 NC for layout trace can do
a beeline
I2C_CLK
I2C_DATA
C50 10P-04-O
C49 10P-04-O
reserve for EMI
HDMI Conn. P/N:
10-083-019691 (HI-TOP)
HDMI
HDMI-19P
U7
U8
AZ1045-04QU-S-O
C43 .1U-04-O
C10 .1U-04-O
Close to Connector
CHOKE2
CHOKE3
CHOKE4
CHOKE1
CMK-90-08-HDMI
For HDMI CHOKE P/N:
16-400-900143 (TAI-TECH)
16-400-900171 (Magic)
QN1 PMBS3904-S
TMDS_HPD_CON
TMDS_HPD2
R62 33-04
R35 200K-04
R55 10K-04
If reserved HDMI or DVI,
R5land R68 must stuff or
monitor have blinking issue from Lenovo
HPD
High : Plug
Low : No Plug
R34 200K-04
Elitegroup Computer Systems
VGA / HDMI / DVI
RS880PM-AM
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Date: Thursday, May 26, 2011
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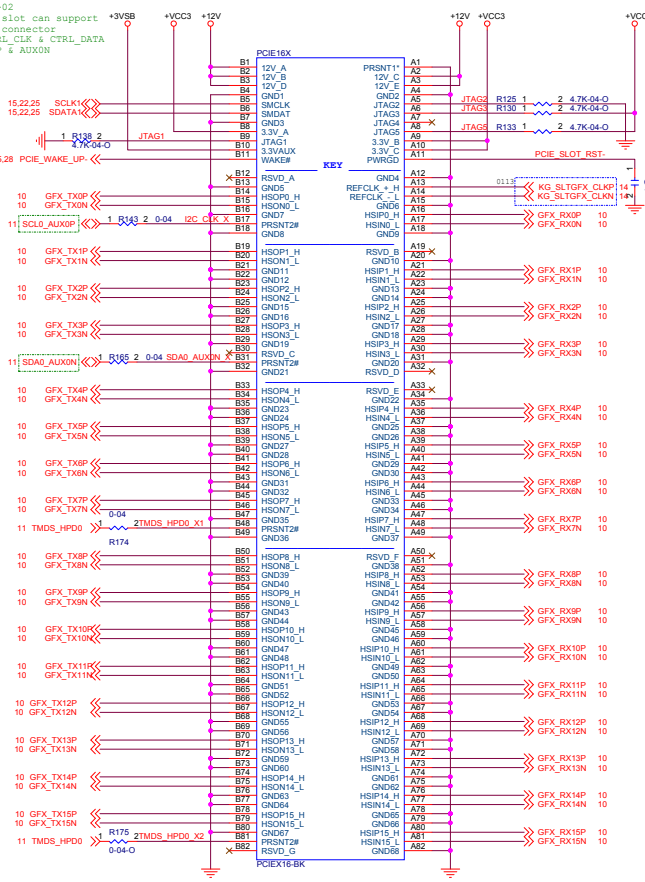
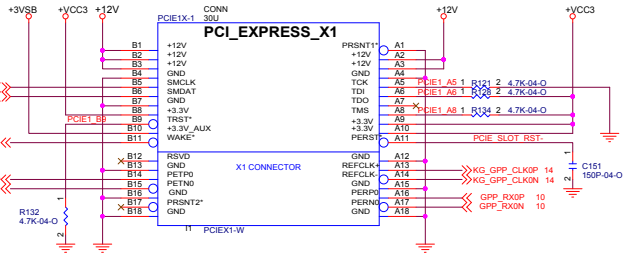
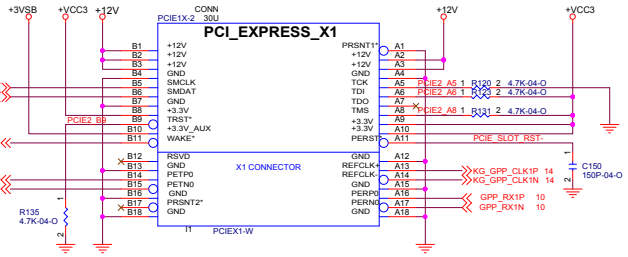
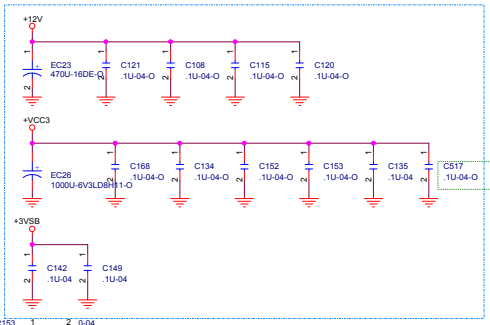
2011-03-02
PCIE16X slot can support HDMI&DP connector
HDMI:CTRL_CLK & CTRL_DATA
DP:AUX0P & AUX0N



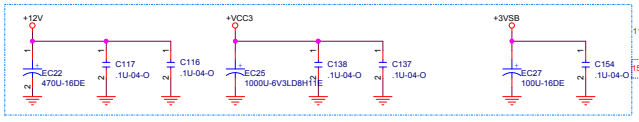


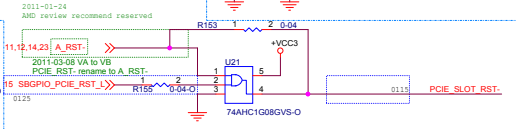


Please place the caps close to PCIE1,PCIE2 Slot.



Please place the caps close to PCIEX16 Slot.





Elitegroup Computer Systems		
Title: PCIE/16X/1X		
Size: Custom	Document Number: RS880PM-AM	Rev: 1.0
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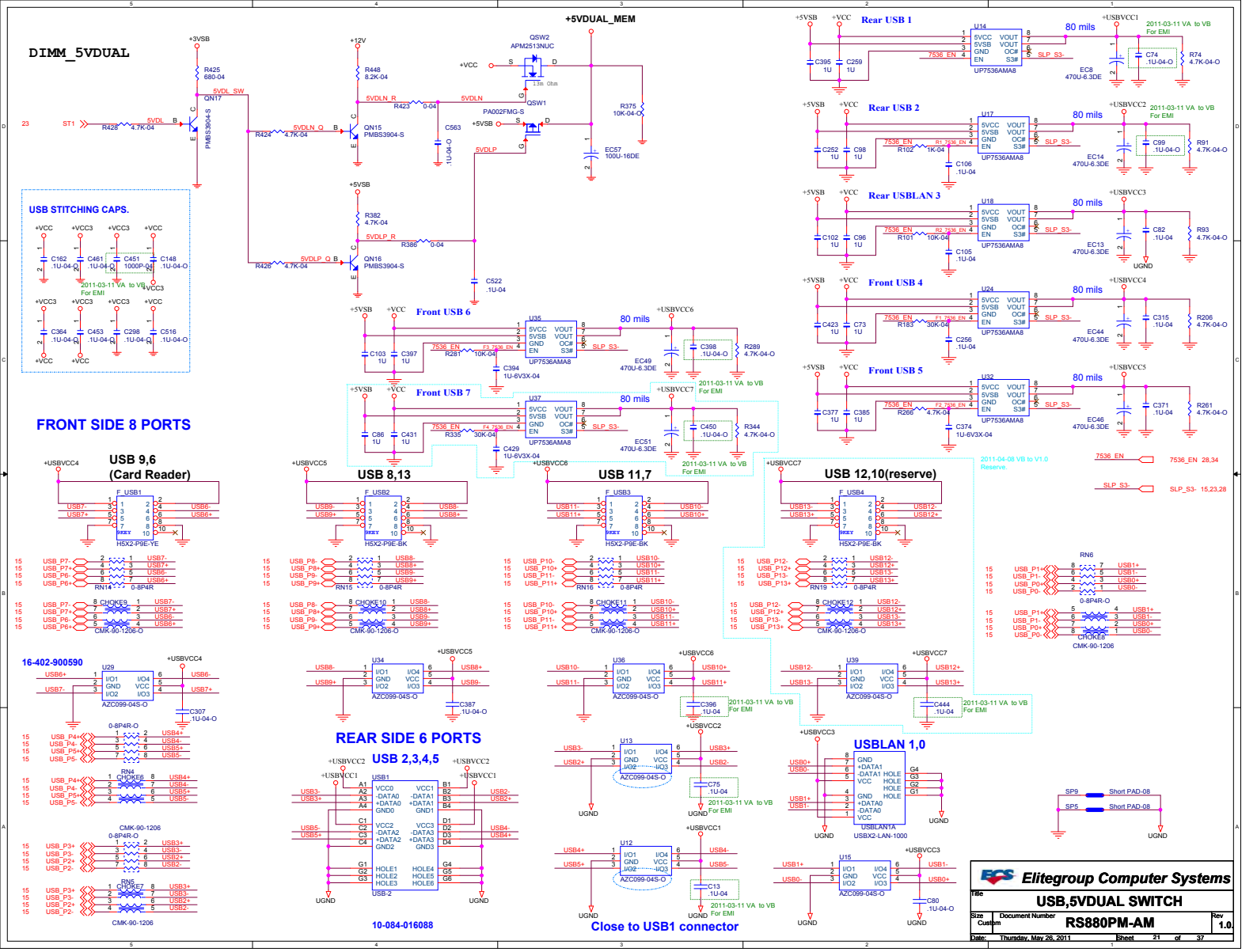
DIMM_5VDUAL
+5VDUAL_MEM
USB STITCHING CAPS.
FRONT SIDE 8 PORTS
USB 9,6
(Card Reader)
USB 8,13
USB 11,7
USB 12,10(reserve)
REAR SIDE 6 PORTS
USB 2,3,4,5
USBLAN 1,0
Close to USB1 connector
10-084-016088
16-402-900590
Rear USB 1
Rear USB 2
Rear USBLAN 3
Front USB 4
Front USB 5
Front USB 6
Front USB 7
80 mils
2011-03-11 VA to VB For EMI
2011-04-08 VB to V1.0 Reserve.
Elitegroup Computer Systems
USB,5VDUAL SWITCH
RS880PM-AM
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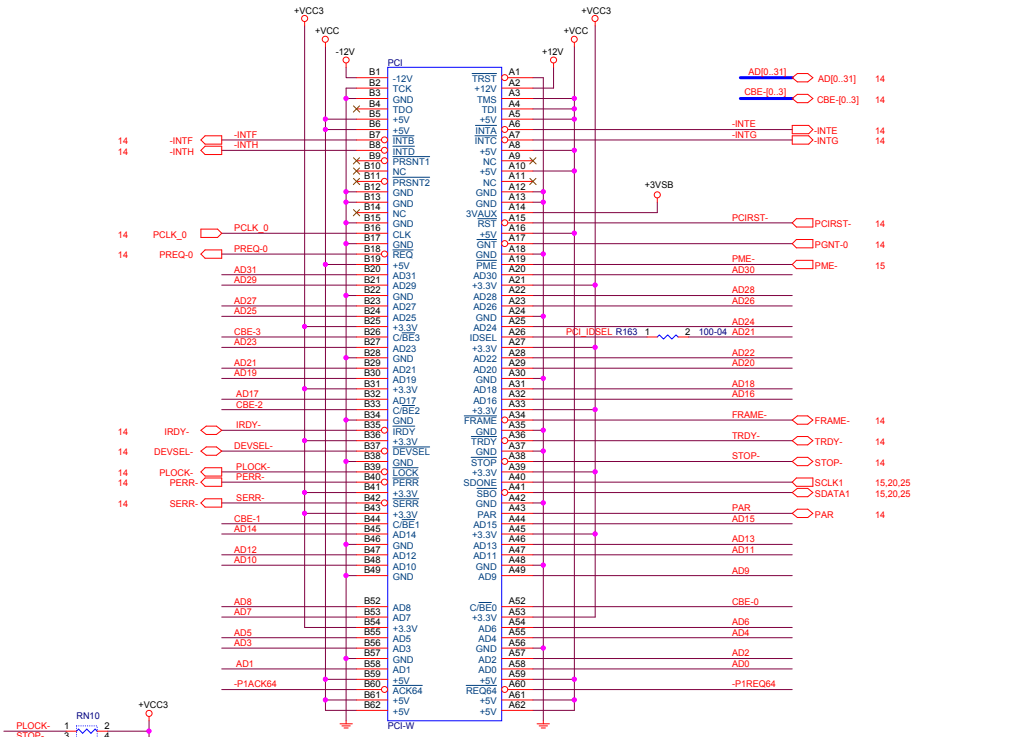
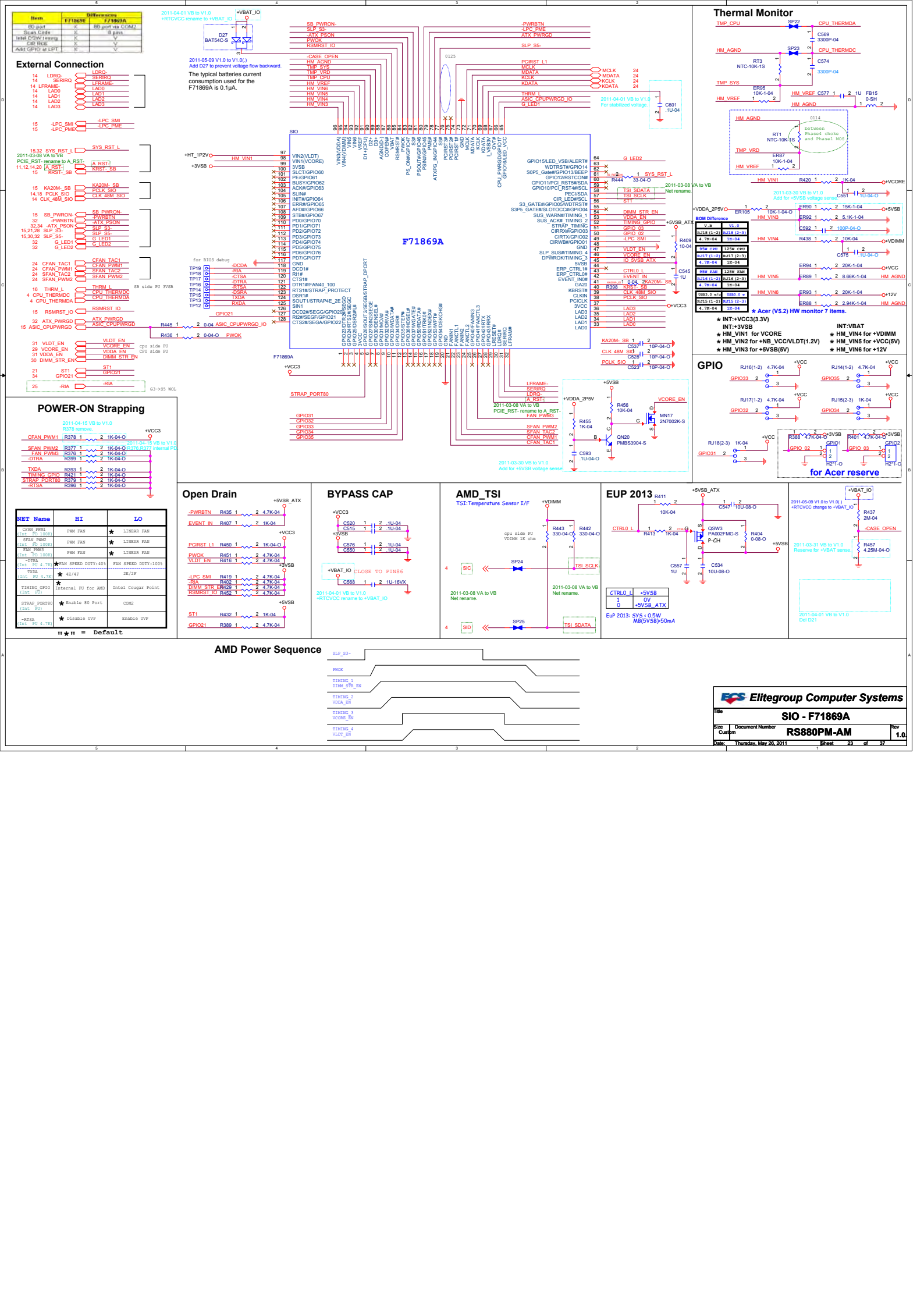


Elitegroup Computer Systems		
Title: PCI SLOT		
Size: Custom	Document Number: RS880PM-AM	Rev: 1.0
Date: Thursday, May 26, 2011	Sheet 22 of 37	


Item
Differences
F71869E
F71869A
80 port
X
80 port via COM2
Scan Code
X
6 pins
Intel DSW timing
X
V
CIR RCE
X
V
Add GPIO at LPT
X
V
External Connection
LDRQ-
SERIRQ
LFRAME-
LAD0
LAD1
LAD2
LAD3
-LPC_SMI
-LPC_PME
SYS_RST_L
A_RST#
KRST#_SB
KA20M#_SB
PCLK_SIO
CLK_48M_SIO
SB_PWRON-
-PWRBTN
-ATX_PSON
SLP_S3-
SLP_S5-
G_LED1
G_LED2
CFAN_TAC1
CFAN_PWM1
SFAN_TAC2
SFAN_PWM2
THRM_L
CPU_THERMDC
CPU_THERMDA
RSMRST_IO
ATX_PWRGD
ASIC_CPUPWRGD
VLDT_EN
VCORE_EN
VDDA_EN
DIMM_STR_EN
ST1
GPIO21
-RIA
SB side PU 3VSB
G3->S5 WOL
POWER-ON Strapping
2011-04-15 VB to V1.0
R378 remove.
+VCC3
CFAN_PWM1 R378 1 2 1K-04-O
SFAN_PWM2 R377 1 2 1K-04-O
FAN_PWM3 R376 1 2 1K-04-O
-DTRA R399 1 2 1K-04-O
TXDA R393 1 2 1K-04-O
TIMING_GPIO R421 1 2 1K-04-O
STRAP_PORT80 R379 1 2 1K-04-O
-RTSA R396 1 2 1K-04-O
2011-04-15 VB to V1.0
R376,R377 internal PD
NET Name
HI
LO
CFAN_PWM1 (Int. PD 100K)
PWM FAN
LINEAR FAN
SFAN_PWM2 (Int. PD 100K)
PWM FAN
LINEAR FAN
FAN_PWM3 (Incl. PD 100K)
PWM FAN
LINEAR FAN
-DTRA (Int. PU 4.7K)
FAN SPEED DUTY:40%
FAN SPEED DUTY:100%
TXDA (Int. PU 4.7K)
4E/4F
2E/2F
TIMING_GPIO (Int. PU)
Internal PU for AMD
Intel Cougar Point
STRAP_PORT80 (Int PU)
Enable 80 Port
COM2
-RTSA (Int. PU 4.7K)
Disable UVP
Enable UVP
"*" = Default
2011-04-01 VB to V1.0
+RTCVCC rename to +VBAT_IO
+VBAT_IO
D27
BAT54C-S
2011-05-09 V1.0 to V1.0(.)
Add D27 to prevent voltage flow backward.
The typical batteries current consumption used for the F71869A is 0.1μA.
SB_PWRON-
SLP_S3-
-ATX_PSON
PWOK
RSMRST_IO
-CASE_OPEN
HM_AGND
TMP_SYS
TMP_VRD
TMP_CPU
HM_VREF
HM_VIN6
HM_VIN5
HM_VIN4
HM_VIN3
SIO
F71869A
+HT_1P2V
+3VSB
HM_VIN1
for BIOS debug
-DCDA
-RIA
-CTSA
-DTRA
-RTSA
-DSRA
TXDA
RXDA
GPIO21
R445 1 2 0-04 ASIC_CPUPWRGD_IO
R436 1 2 0-04-O PWOK
cpu side PU
CPU side PU
+VCC3
STRAP_PORT80
GPIO31
GPIO32
GPIO33
GPIO34
GPIO35
-PWRBTN
-LPC_PME
ATX_PWRGD
SLP_S5-
PCIRST_L1
MCLK
MDATA
KCLK
KDATA
THRM_L
ASIC_CPUPWRGD_IO
G_LED1
MCLK 24
MDATA 24
KCLK 24
KDATA 24
C601 1U-04
2011-04-01 VB to V1.0
For stabilized voltage.
G_LED2
SYS_RST_L
R444 33-04-O
2011-03-08 VA to VB
Net rename.
TSI_SDATA
TSI_SCLK
ST1
DIMM_STR_EN
VDDA_EN
TIMING_GPIO
GPIO_03
GPIO_02
-LPC_SMI
VLDT_EN
VCORE_EN
IO_SVSB_ATX
+5VSB_ATX
R409 10-04
C545 1U
CTRL0_L
EVENT_IN
R398 0-04
KRST#_SB
CLK_48M_SIO
PCLK_SIO
GA20
KBRST#
CLKIN
PCICLK
3VCC
LAD3
LAD2
LAD1
LAD0
+VCC3
KA20M#_SB C537 10P-04-O
CLK_48M_SIO C528 10P-04-O
PCLK_SIO C523 10P-04-O
LFRAME-
SERIRQ
LDRQ-
(A_RST)
2011-03-08 VA to VB
PCIE_RST- rename to A_RST-
FAN_PWM3
SFAN_PWM2
SFAN_TAC2
CFAN_PWM1
CFAN_TAC1
+VDDA_2P5V
+5VSB
R455 1K-04
R456 10K-04
VCORE_EN
MN17 2N7002K-S
QN20 PMBS3904-S
C593 .1U-04-O
2011-03-30 VB to V1.0
Add for +5VSB voltage sense.
Thermal Monitor
TMP_CPU
SP22
CPU_THERMDA
C569 3300P-04
HM_AGND
SP23
CPU_THERMDC
C574 3300P-04
RT3 NTC-10K-1S
TMP_SYS
ER95 10K-1-04
HM_VREF
C577 1U
FB15 0-SH
HM_AGND
0114
between Phase4 choke and Phase1 MOS
RT1 NTC-10K-1S
TMP_VRD
ER87 10K-1-04
HM_VREF
HM_VIN1
R420 2K-04
+VCORE
C551 1U-04-O
2011-03-30 VB to V1.0
Add for +5VSB voltage sense.
+VDDA_2P5V
ER105 10K-1-04-O
+5VSB
HM_VIN3
ER90 15K-1-04
ER92 5.1K-1-04
C592 100P-04-O
HM_VIN4
R438 10K-04
+VDIMM
C575 1U-04-O
ER94 20K-1-04
+VCC
HM_VIN5
ER89 8.66K-1-04
HM_AGND
HM_VIN6
ER93 20K-1-04
+12V
ER88 2.94K-1-04
HM_AGND
BOM Difference
V_B
V1_0
4.7K-04
1K-04
95W CPU
125W CPU
RJ17 (1-2)
RJ17 (2-3)
95W FAN
125W FAN
RJ16 (1-2)
RJ16 (2-3)
DDR3.0 w/o
DDR3.0 w
RJ15 (1-2)
RJ15 (2-3)
★ Acer (V5.2) HW monitor 7 items.
★ INT:+VCC3(3.3V)
INT:+3VSB
INT:VBAT
★ HM_VIN1 for VCORE
★ HM_VIN2 for +NB_VCC/VLDT(1.2V)
★ HM_VIN3 for +5VSB(5V)
★ HM_VIN4 for +VDIMM
★ HM_VIN5 for +VCC(5V)
★ HM_VIN6 for +12V
GPIO
RJ16(1-2) 4.7K-04
RJ14(1-2) 4.7K-04
GPIO33
GPIO35
RJ17(1-2) 4.7K-04
RJ15(2-3) 1K-04
GPIO32
GPIO34
RJ18(2-3) 1K-04
GPIO31
R388 4.7K-04-O
R401 4.7K-04-O
GPIO1
GPIO2
GPIO_02
GPIO_03
H21-O
for Acer reserve
Open Drain
-PWRBTN R435 1 2 4.7K-04
EVENT_IN R407 1 2 1K-04
PCIRST_L1 R450 1 2 1K-04-O
PWOK R451 1 2 4.7K-04
VLDT_EN R416 1 2 4.7K-04
-LPC_SMI R419 1 2 4.7K-04
-RIA R402 1 2 4.7K-04
DIMM_STR_EN R429 1 2 4.7K-04
RSMRST_IO R452 1 2 4.7K-04
ST1 R432 1 2 1K-04
GPIO21 R389 1 2 4.7K-04
BYPASS CAP
C520 1 2 .1U-04
C515 1 2 .1U-04
C576 1 2 .1U-04
C550 1 2 .1U-04
CLOSE TO PIN86
C568 1 2 1U-16VX
2011-04-01 VB to V1.0
+RTCVCC rename to +VBAT_IO
AMD_TSI
TSI:Temperature Sensor I/F
+VDIMM
cpu side PU
VDIMM 1K ohm
R443 330-04-O
R442 330-04-O
SP24
SIC
TSI_SCLK
2011-03-08 VA to VB
Net rename.
SP25
SID
TSI_SDATA
EUP 2013
+5VSB_ATX
R411 10-04K
C547 10U-08-O
CTRL0_L
R413 1K-04
QSW3 PA002FMG-S P-CH
R404 0-08-O
+5VSB
C557 1U
C534 10U-08-O
CTRL0_L +5VSB
1 0V
0 +5VSB_ATX
EuP 2013: SYS < 0.5W
MB(5VSB)<50mA
+VBAT_IO
2011-05-09 V1.0 to V1.0(.)
+RTCVCC change to +VBAT_IO
R437 2M-04
-CASE_OPEN
2011-03-31 VB to V1.0
Reserve for +VBAT sense.
R457 4.25M-04-O
2011-04-01 VB to V1.0
Del D21
AMD Power Sequence
SLP_S3-
PWOK
TIMING_1
DIMM_STR_EN
TIMING_2
VDDA_EN
TIMING_3
VCORE_EN
TIMING_4
VLDT_EN
Elitegroup Computer Systems
Title
SIO - F71869A
Size
Custom
Document Number
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1.0
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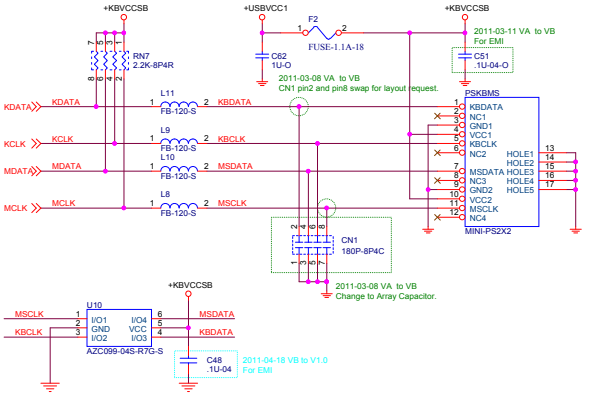
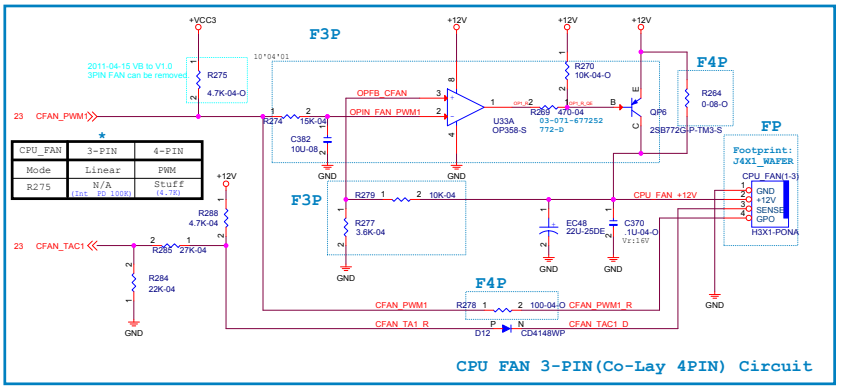
PS2



Close to PSKBMS connector

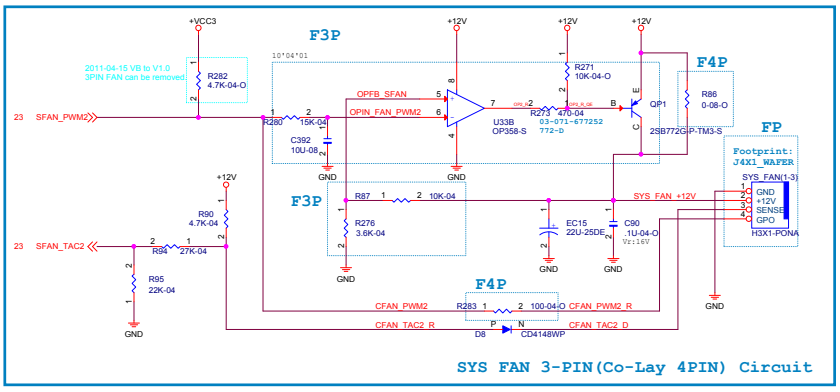


CPU_FAN	3-PIN	4-PIN
Mode	Linear	PWM
R275	N/A (Int PD 100K)	Stuff (4.7K)

CPU FAN 3-PIN(Co-Lay 4PIN) Circuit

CPU FAN:3PIN(95W),4PIN(125W)

	MODE	F3P	F4P	FP Value	R275
*	3PIN	V	X	H3X1-PONA	X
	4PIN	X	V	H4X1-PONA	V



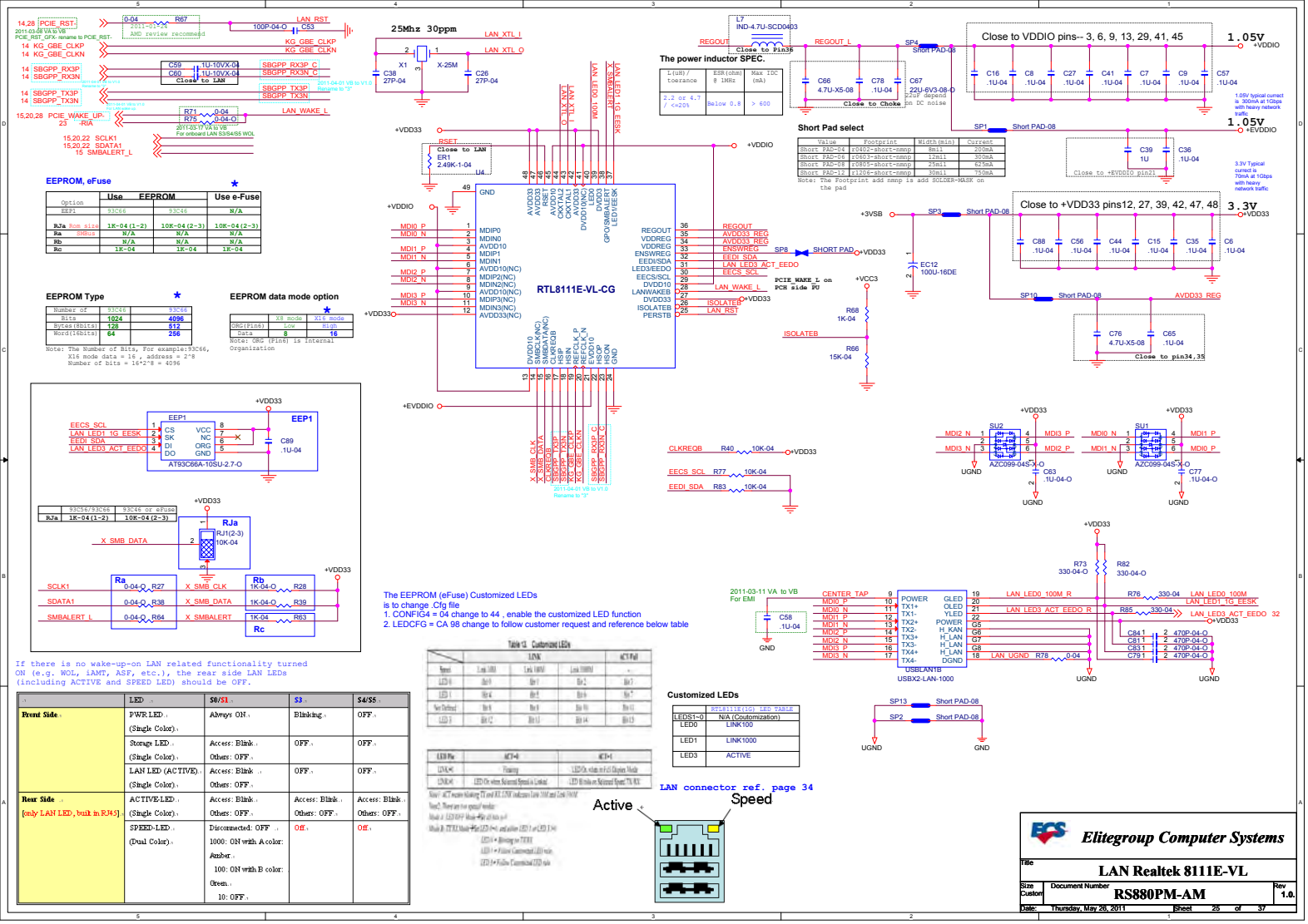
SYS FAN 3-PIN(Co-Lay 4PIN) Circuit

SYS FAN

	MODE	F3P	F4P	FP Value	R282
*	3PIN	V	X	H3X1-PONA	X
	4PIN	X	V	H4X1-PONA	V

Elitegroup Computer Systems

Title	FAN,PS2,FAN	
Size: Custom	Document Number: RS880PM-AM	Rev: 1.0
Date: Thursday, May 26, 2011	Sheet 24 of 37	



Option	Use EEPROM		Use e-Fuse
EEP1	93C66	93C46	N/A
RJa Rom size	1K-04(1-2)	10K-04(2-3)	10K-04(2-3)
Ra SMBus	N/A	N/A	N/A
Rb	N/A	N/A	N/A
Rc	1K-04	1K-04	1K-04

Number of Bits	93C46	93C66
	1024	4096
Bytes(8bits)	128	512
Word(16bits)	64	256

Note: The Number of Bits, For example:93C66,
X16 mode data = 16 , address = 2^8
Number of bits = 16*2^8 = 4096

	X8 mode	X16 mode
ORG(Pin6)	Low	High
Data	8	16

Note: ORG (Pin6) is Internal Organization

	93C56/93C66	93C46 or eFuse
RJa	1K-04(1-2)	10K-04(2-3)

L(uH) / tolerance	ESR(ohm) @ 1MHz	Max IDC (mA)
2.2 or 4.7 / <=20%	Below 0.8	> 600

Value	Footprint	Width(min)	Current
Short PAD-04	r0402-short-nmmp	8mil	200mA
Short PAD-06	r0603-short-nmmp	12mil	300mA
Short PAD-08	r0805-short-nmmp	25mil	625mA
Short PAD-12	r1206-short-nmmp	30mil	750mA

Note: The Footprint add nmmp is add SOLDER-MASK on the pad

LED1~0	RTL8111E(1G) LED TABLE
LED0	LINK100
LED1	LINK1000
LED3	ACTIVE

	LED	S0/S1	S3	S4/S5
Front Side	PWR LED (Single Color)	Always ON	Blinking	OFF
	Storage LED (Single Color)	Access: Blink Others: OFF	OFF	OFF
	LAN LED (ACTIVE) (Single Color)	Access: Blink Others: OFF	OFF	OFF
Rear Side [only LAN LED, built in RJ45]	ACTIVE LED (Single Color)	Access: Blink Others: OFF	Access: Blink Others: OFF	Access: Blink Others: OFF
	SPEED LED (Dual Color)	Disconnected: OFF 1000: ON with A color: Amber 100: ON with B color: Green 10: OFF	Off	Off

Title	LAN Realtek 8111E-VL
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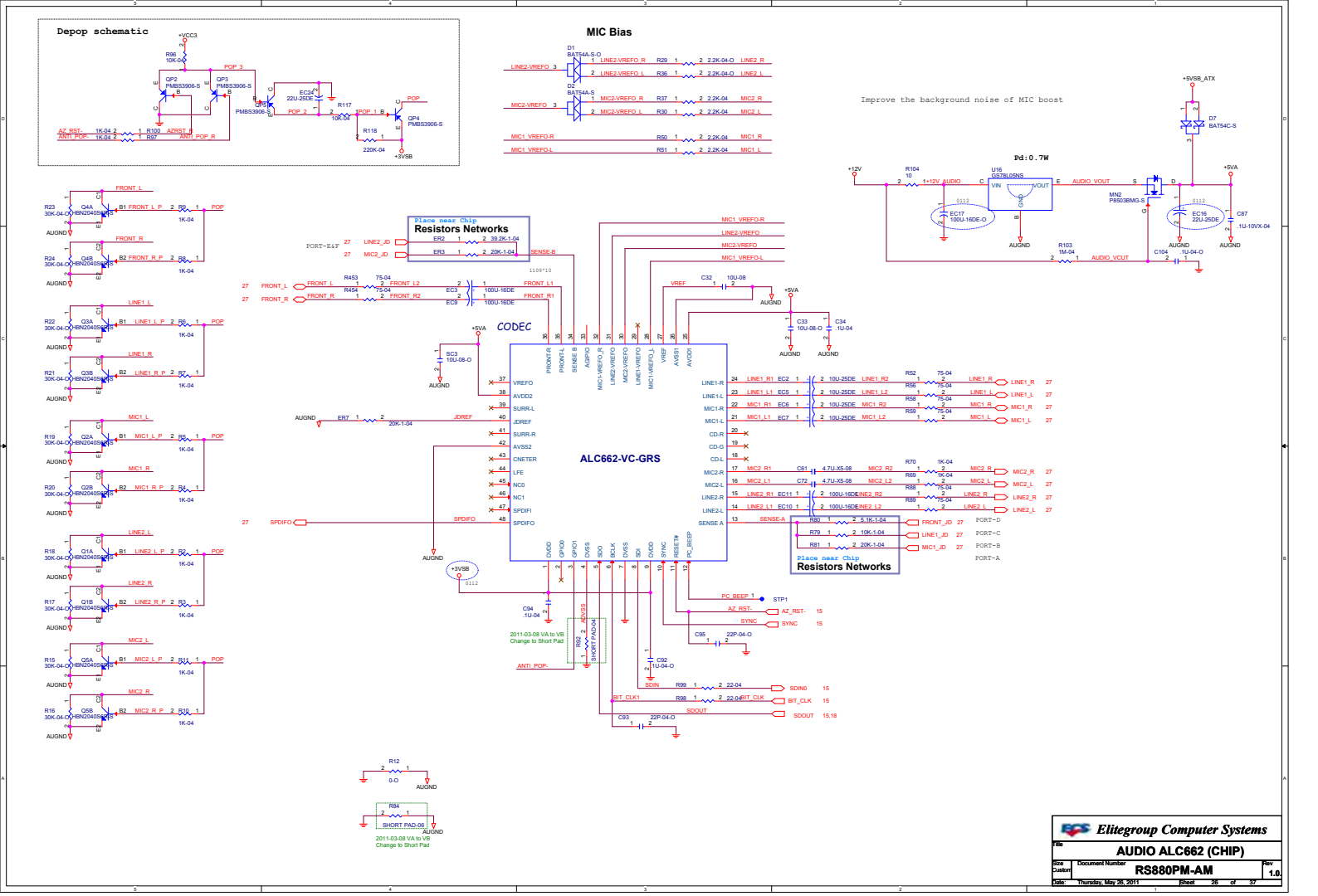
Depop schematic
MIC Bias
Improve the background noise of MIC boost
Pd:0.7W
Place near Chip
Resistors Networks
CODEC
ALC662-VC-GRS
2011-03-08 VA to VB
Change to Short Pad
Elitegroup Computer Systems
AUDIO ALC662 (CHIP)
RS880PM-AM
1.0
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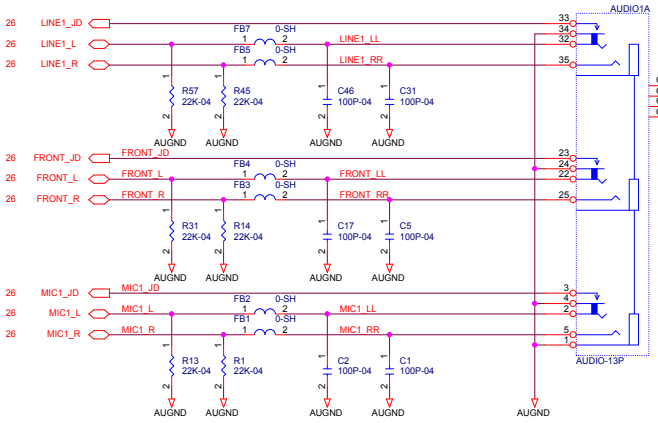
REAR-AUDIO

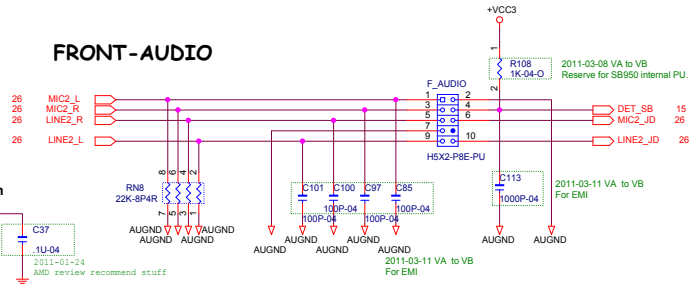


Line in

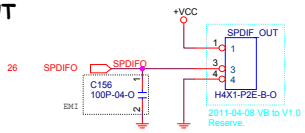
Front out

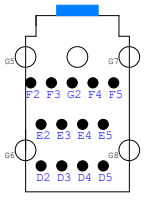
Mic in

FRONT-AUDIO

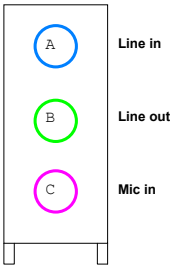


SPDIF-OUT





TOP VIEW



Line in

Line out

Mic in

FRONT VIEW

Elitegroup Computer Systems		
Title: AUDIO ALC662 (PANEL)		
Size: B	Document Number: RS880PM-AM	Rev: 1.0
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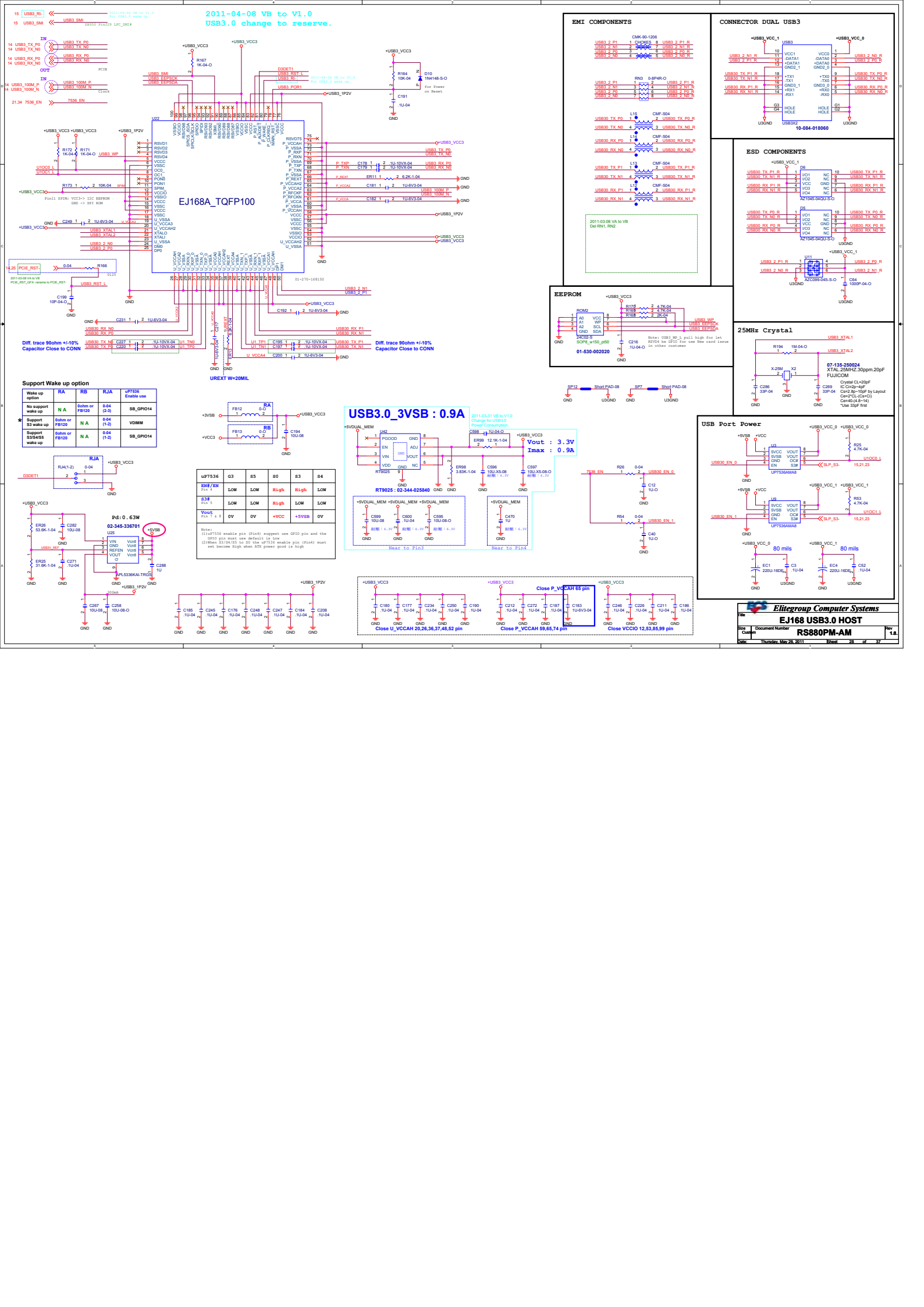
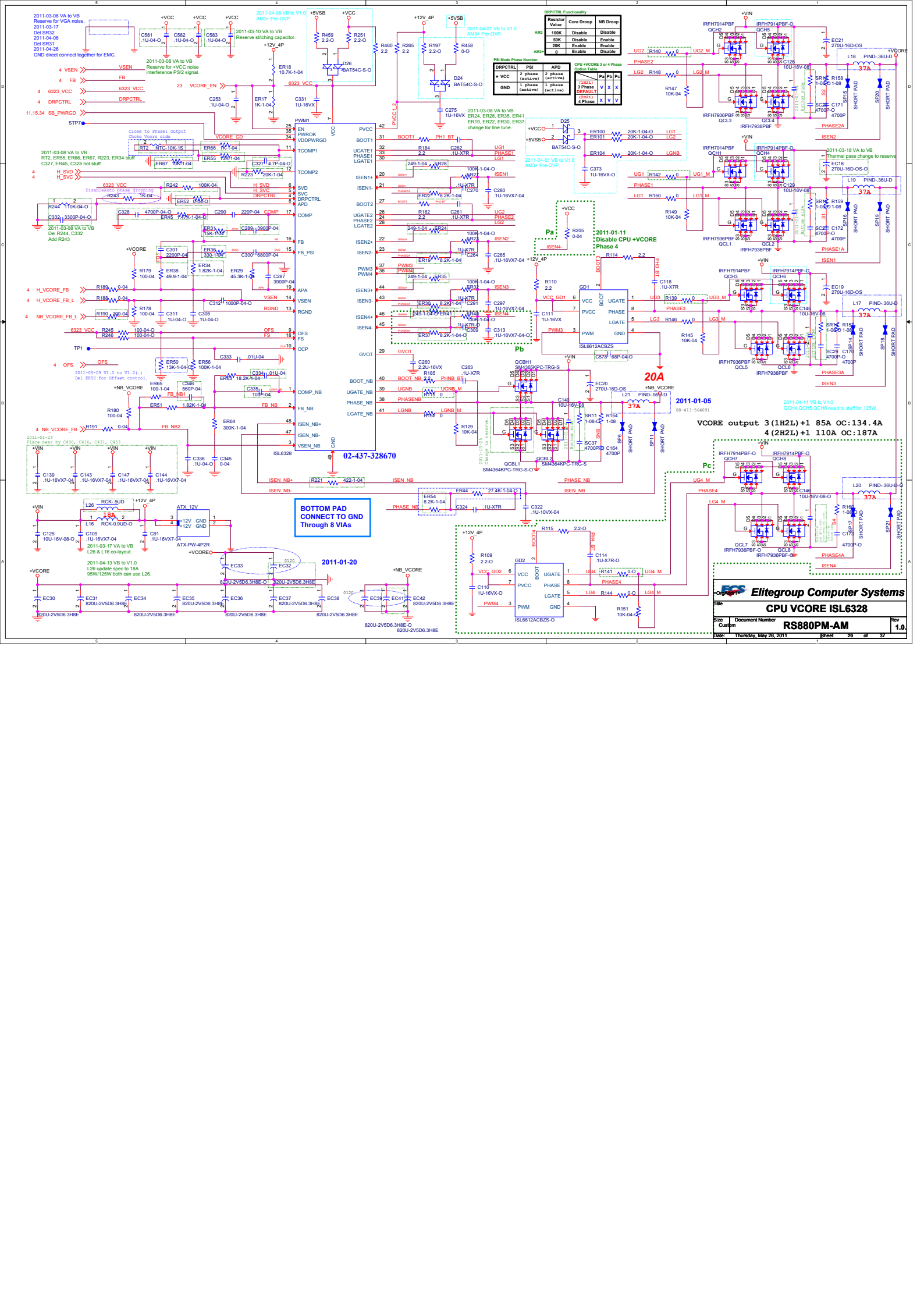

2011-04-08 VB to V1.0
USB3.0 change to reserve.
EJ168A_TQFP100
EMI COMPONENTS
CONNECTOR DUAL USB3
ESD COMPONENTS
EEPROM
25MHz Crystal
USB Port Power
USB3.0_3VSB : 0.9A
Vout : 3.3V
Imax : 0.9A
Support Wake up option
Diff. trace 90ohm +/-10%
Capacitor Close to CONN
UREXT W=20MIL
Close U_VCCAH 20,26,36,37,48,52 pin
Close P_VCCAH 59,65,74 pin
Close VCCIO 12,53,85,99 pin
Elitegroup Computer Systems
EJ168 USB3.0 HOST
RS880PM-AM


2011-03-08 VA to VB
Reserve for VGA noise.
2011-03-17
Del SR32
2011-04-06
Del SR31
2011-04-26
GND direct connect together for EMC.
2011-03-08 VA to VB
Reserve for +VCC noise interference PS/2 signal.
2011-03-10 VA to VB
Reserve stitching capacitor.
2011-04-06 VB to V1.0
AM3+ Pre-OVP.
2011-04-01 VB to V1.0
AM3+ Pre-OVP.
2011-03-08 VA to VB
ER24, ER28, ER35, ER41
ER19, ER22, ER30, ER37
change for fine tune.
2011-04-01 VB to V1.0
AM3+ Pre-OVP.
2011-03-08 VA to VB
RT2, ER55, ER66, ER67, R223, ER34 stuff
C327, ER45, C328 not stuff
2011-03-08 VA to VB
Del R244, C332
Add R243
2011-01-11
Disable CPU +VCORE
Phase 4
2011-01-05
20A
VCORE output 3(1H2L)+1 85A OC:134.4A
4(2H2L)+1 110A OC:187A
2011-01-20
2011-04-11 VB to V1.0
QCH4,QCH5,QCH6 need to stuff for 125W
2011-04-13 VB to V1.0
L26 update spec to 18A
95W/125W both can use L26.
2011-03-18 VA to VB
Thermal pass change to reserve
2011-05-09 V1.0 to V1.0(.)
Del ER50 for Offset control.
2011-01-24
Place near by C406, C416, C431, C453
Close to Phasel Output Choke Vcore side
Disable auto phase dropping
Change to reserve.
02-437-328670
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs
PWM1
ISL6328
ISL6612ACBZS
SM4364KPC-TRG-S
SM4364KPC-TRG-S-O
BAT54C-S-O
IRFH7914PBF
IRFH7914PBF-O
IRFH7936PBF
IRFH7936PBF-O
DRPCTRL Functionality
PSI Mode Phase Number
CPU +VCORE 3 or 4 Phase Option Table
Elitegroup Computer Systems
CPU VCORE ISL6328
RS880PM-AM
Size: Custom
Rev: 1.0
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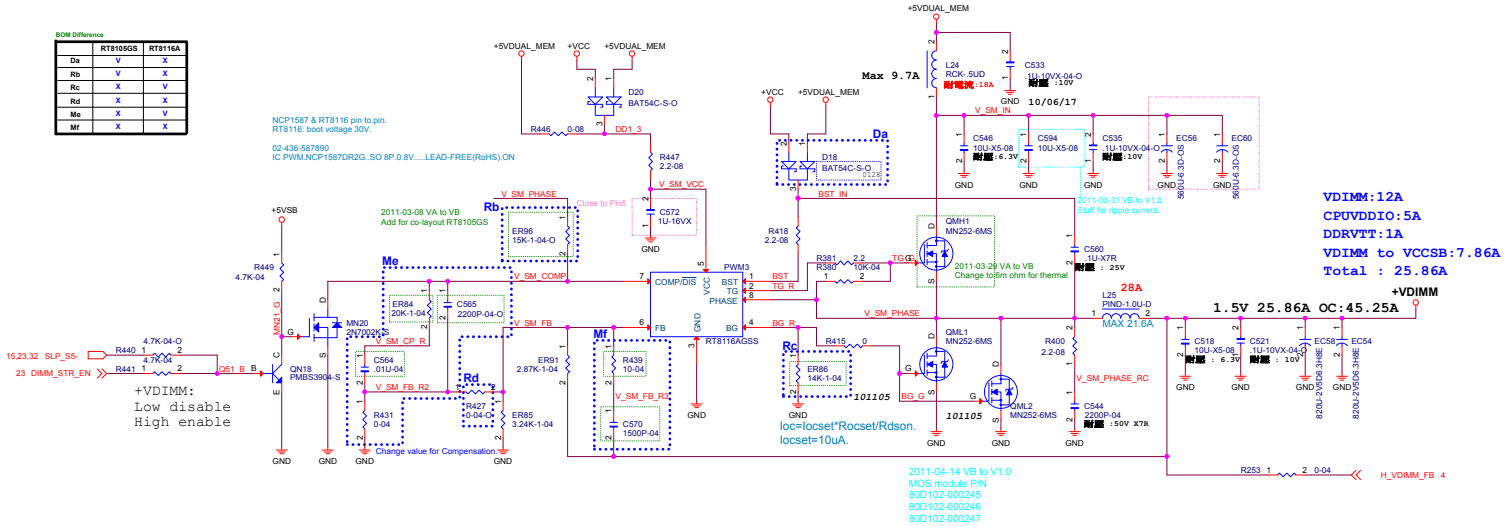
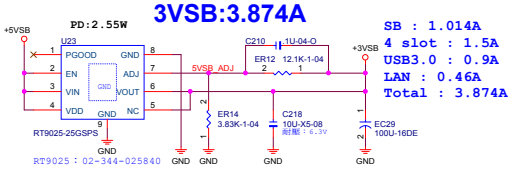
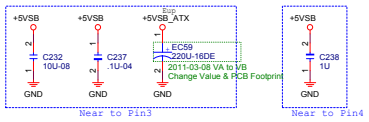
DDRIII Voltage

BOM Difference	RT8105GS	RT8116A
Da	V	X
Rb	V	X
Rc	X	V
Rd	X	X
Me	X	V
Mf	X	X

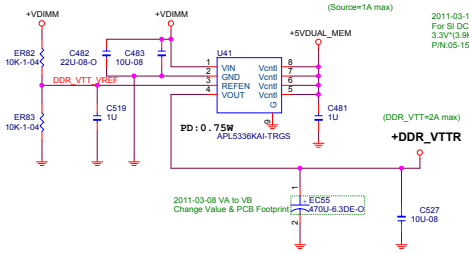


3VSB:3.874A

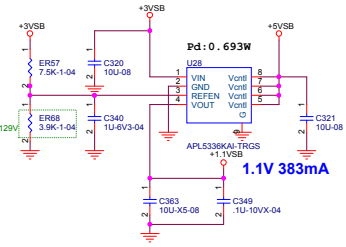




DDR_VTTR (0.75V,1A)



SB 1.1VSB



Elitegroup Computer Systems			
Title: DC POWER, DDRIII POWER			
Size: Custom	Document Number: RS880PM-AM		Rev: 1.0
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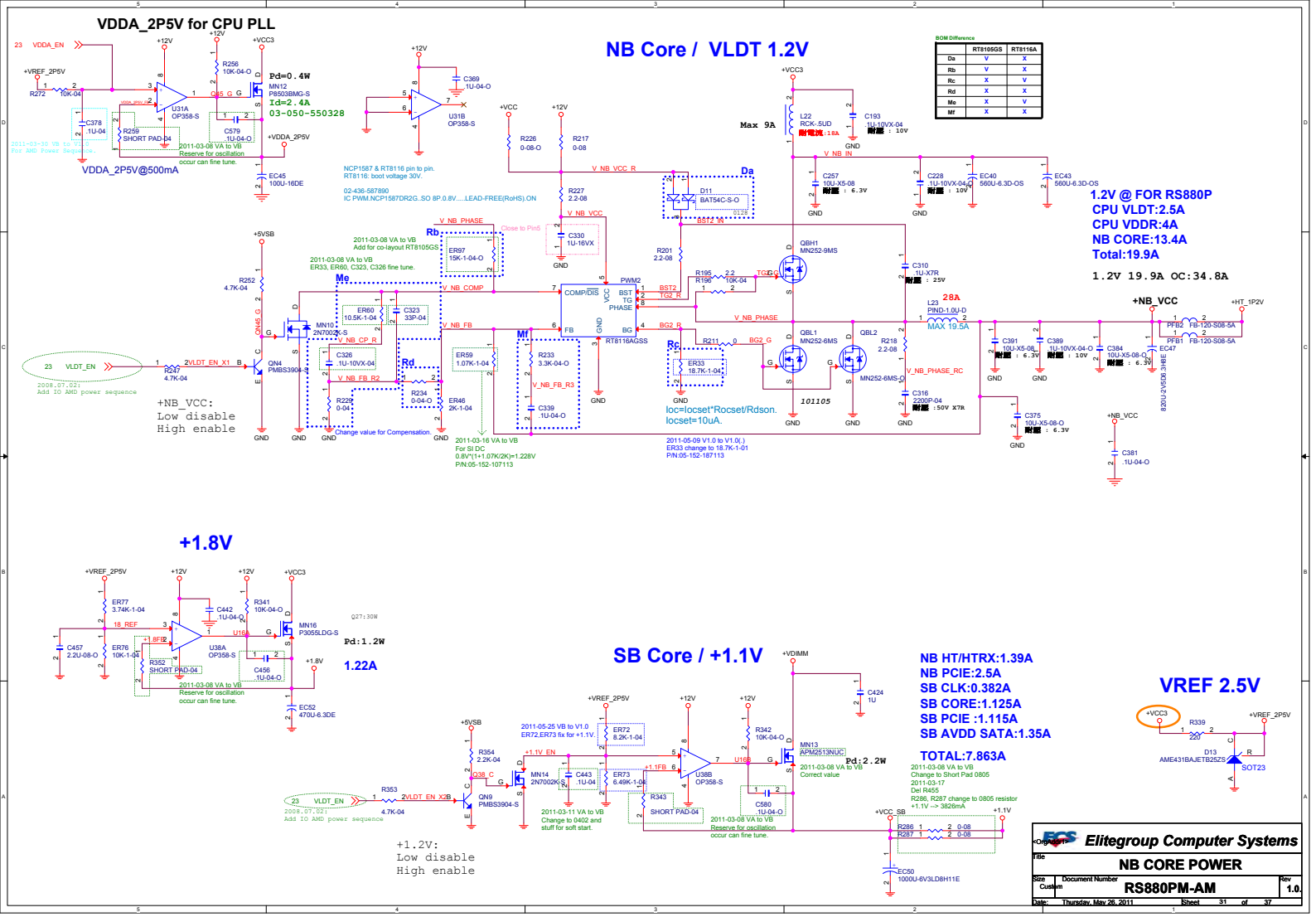

	RT8105GS	RT8116A
Da	V	X
Rb	V	X
Rc	X	V
Rd	X	X
Me	X	V
Mf	X	X

Elitegroup Computer Systems

Title: NB CORE POWER

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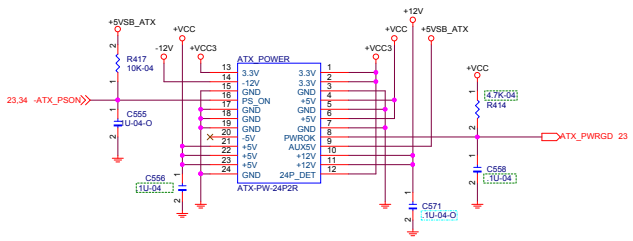
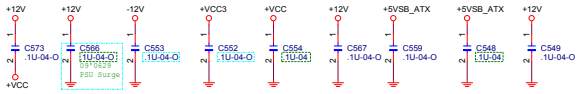
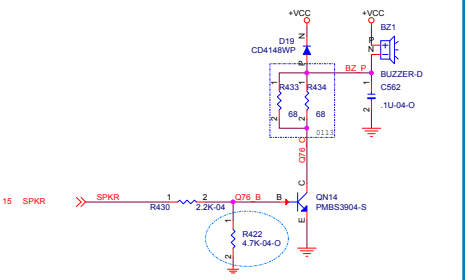
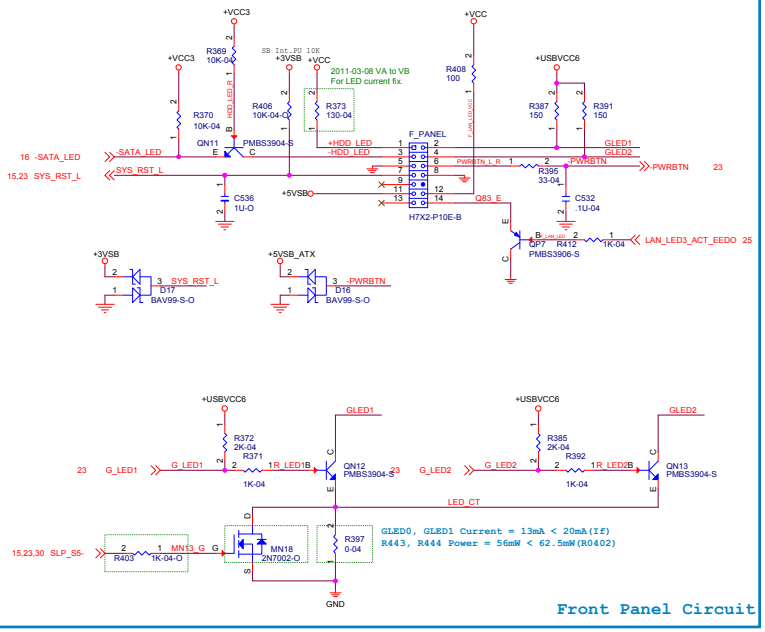


For EMI.



Buzzer Circuit





Front Panel Circuit

<Org Name>	Elitegroup Computer Systems		
Title	PANEL,ATX24P		
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SB950

Name	Type	Voltage	Functional Description	Net
GPIO61	I/O	VCC3	F_AUDIO detect	DET_SB
IDLEEXIT	I	VCC3	indicates processor is ready to enter or exit C1E	CPU_IDLEEXIT_
GPIO199	I/O	3VSB	SPI ROM strape	GPIO199
GPIO200	I/O	3VSB	SPI ROM strape	GPIO200

F71869A

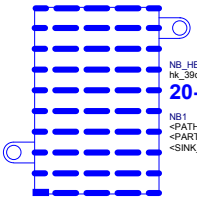
Name	Type	Voltage	Functional Description	Net
RI1#	I	3VSB	WOL	-RIA
GPIO31	I/O	VCC3	reserve	GPIO31
GPIO32	I/O	VCC3	reserve	GPIO32
GPIO33	I/O	VCC3	reserve	GPIO33
GPIO34	I/O	VCC3	reserve	GPIO34
GPIO35	I/O	VCC3	reserve	GPIO35
GPIO02	I/O	3VSB	for Acer reserve	GPIO_02
GPIO03	I/O	3VSB	for Acer reserve	GPIO_03
GPIO15/LEDVSB	I/O	3VSB	LED2	G_LED2
GPIO16/LEDVCC	I/O	3VSB	LED1	G_LED1
OVT#	O	3VSB	to SB TALERT#	THRM_L
GPIO21	I/O	3VSB(5V)	reserve for UP7536 control	GPIO21
CTRL0#	OD	3VSB(5V)	for Eup control	CTRL0_L
S3_GATE1	OD	3VSB(5V)	for S3 VDIMM DUAL power control	ST1

For 103 (wire)

For 104

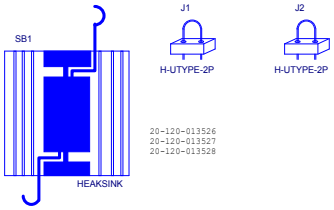
CR2032

For 104



For 104

For 104



<Org Name>	Elitegroup Computer Systems		
Title	Attention		
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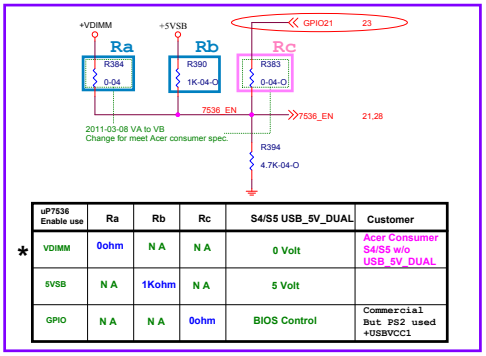
2011-03-14 VA to VB
Not reserved.

NB_PWRGOOD Sequence

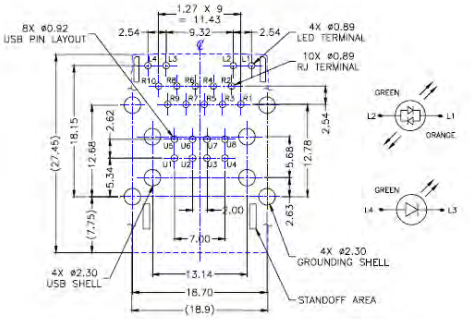
PS/2 Keyboard		Consumer	
BIOS Option	System State	Eup Lot "Disabled"	Eup Lot "Enabled"
		WakeUp	WakeUp
Disable	S1/S3	N	N
	S4/S5	N/A	N/A
	After G3	N/A	N/A
Enable	S1/S3	Y	Y
	S4/S5	N/A	N/A
	After G3	N/A	N/A
S1/S3 Wakeup	S1/S3	N/A	N/A
(If support)	S4/S5	N/A	N/A
	After G3	N/A	N/A
S4/S5 Wakeup	S1/S3	N/A	N/A
(If support)	S4/S5	N/A	N/A
	After G3	N/A	N/A

USB Keyboard & Mouse		Consumer	
BIOS Option	System State	Eup Lot "Disabled"	Eup Lot "Enabled"
		WakeUp	WakeUp
Disable	S1/S3	N	N
	S4/S5	N/A	N/A
	After G3	N/A	N/A
Enable	S1/S3	Y	Y
	S4/S5	N/A	N/A
	After G3	N/A	N/A
S1/S3 Wakeup	S1/S3	N/A	N/A
(If support)	S4/S5	N/A	N/A
	After G3	N/A	N/A
S4/S5 Wakeup	S1/S3	N/A	N/A
(If support)	S4/S5	N/A	N/A
	After G3	N/A	N/A

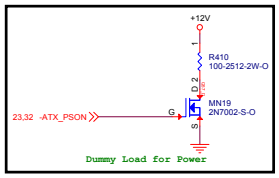


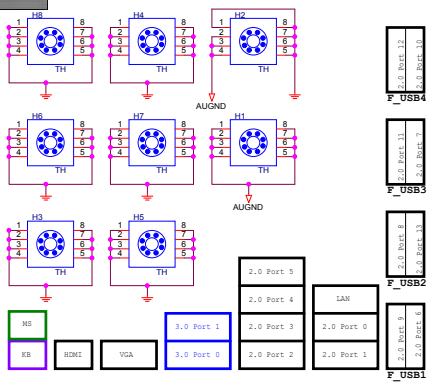
uP7536 Enable use	Ra	Rb	Rc	S4/S5 USB_5V_DUAL	Customer
* VDIMM	0ohm	N A	N A	0 Volt	Acer Consumer S4/S5 w/o USB_5V_DUAL
5VSB	N A	1Kohm	N A	5 Volt	
GPIO	N A	N A	0ohm	BIOS Control	Commercial But PS2 used +USBVCC1

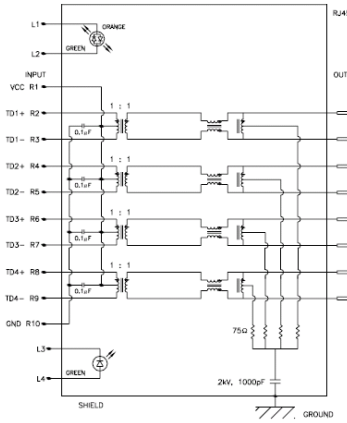
PCB Layout



Schematic







2011-03-15 VA to VB
Reserve for reset issue.

POWER GOOD & ENABLES

Elitegroup Computer Systems

Title: Power Sequence

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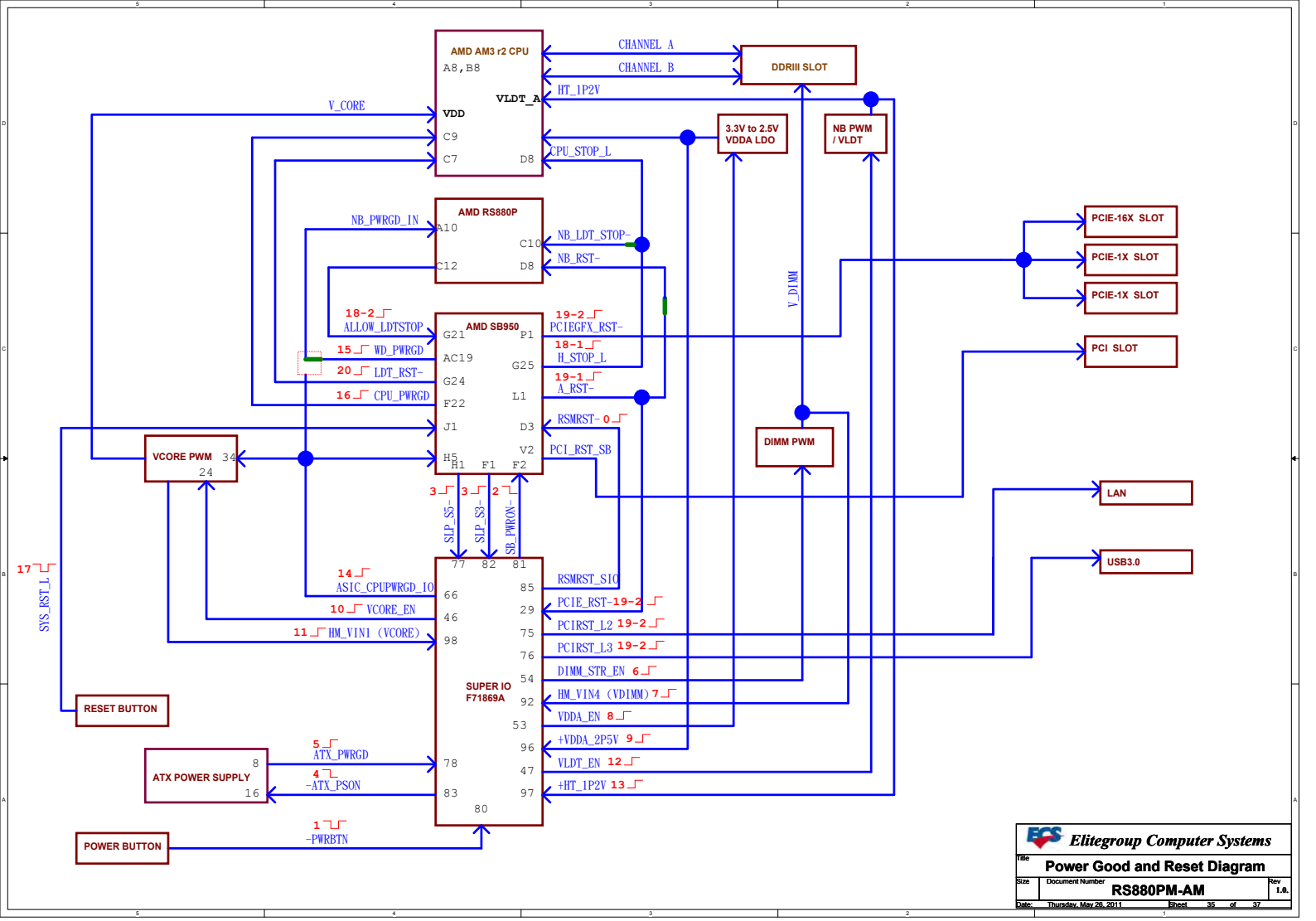
AMD AM3 r2 CPU
A8,B8
VLDT_A
VDD
C9
C7
D8
CHANNEL A
CHANNEL B
HT_1P2V
V_CORE
CPU_STOP_L
DDRIII SLOT
3.3V to 2.5V VDDA LDO
NB PWM / VLDT
AMD RS880P
A10
C10
C12
D8
NB_PWRGD_IN
NB_LDT_STOP-
NB_RST-
V_DIMM
PCIE-16X SLOT
PCIE-1X SLOT
PCIE-1X SLOT
PCI SLOT
AMD SB950
G21
P1
AC19
G25
G24
L1
F22
J1
D3
H5
V2
H1
F1
F2
18-2 ALLOW_LDTSTOP
15 WD_PWRGD
20 LDT_RST-
16 CPU_PWRGD
19-2 PCIEGFX_RST-
18-1 H_STOP_L
19-1 A_RST-
RSMRST- 0
PCI_RST_SB
VCORE PWM
34
24
DIMM PWM
LAN
USB3.0
3
3
2
SLP_S5-
SLP_S3-
SB_PWRON-
77
82
81
17
SYS_RST_L
14 ASIC_CPUPWRGD_IO
10 VCORE_EN
11 HM_VIN1 (VCORE)
66
46
98
85
29
75
76
54
92
53
96
47
97
RSMRST_S1O
PCIE_RST-19-2
PCIRST_L2 19-2
PCIRST_L3 19-2
DIMM_STR_EN 6
HM_VIN4 (VDIMM) 7
VDDA_EN 8
+VDDA_2P5V 9
VLDT_EN 12
+HT_1P2V 13
SUPER IO F71869A
RESET BUTTON
5 ATX_PWRGD
4 -ATX_PSON
8
ATX POWER SUPPLY
16
78
83
80
1 -PWRBTN
POWER BUTTON
Elitegroup Computer Systems
Title
Power Good and Reset Diagram
Size
Document Number
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1.0
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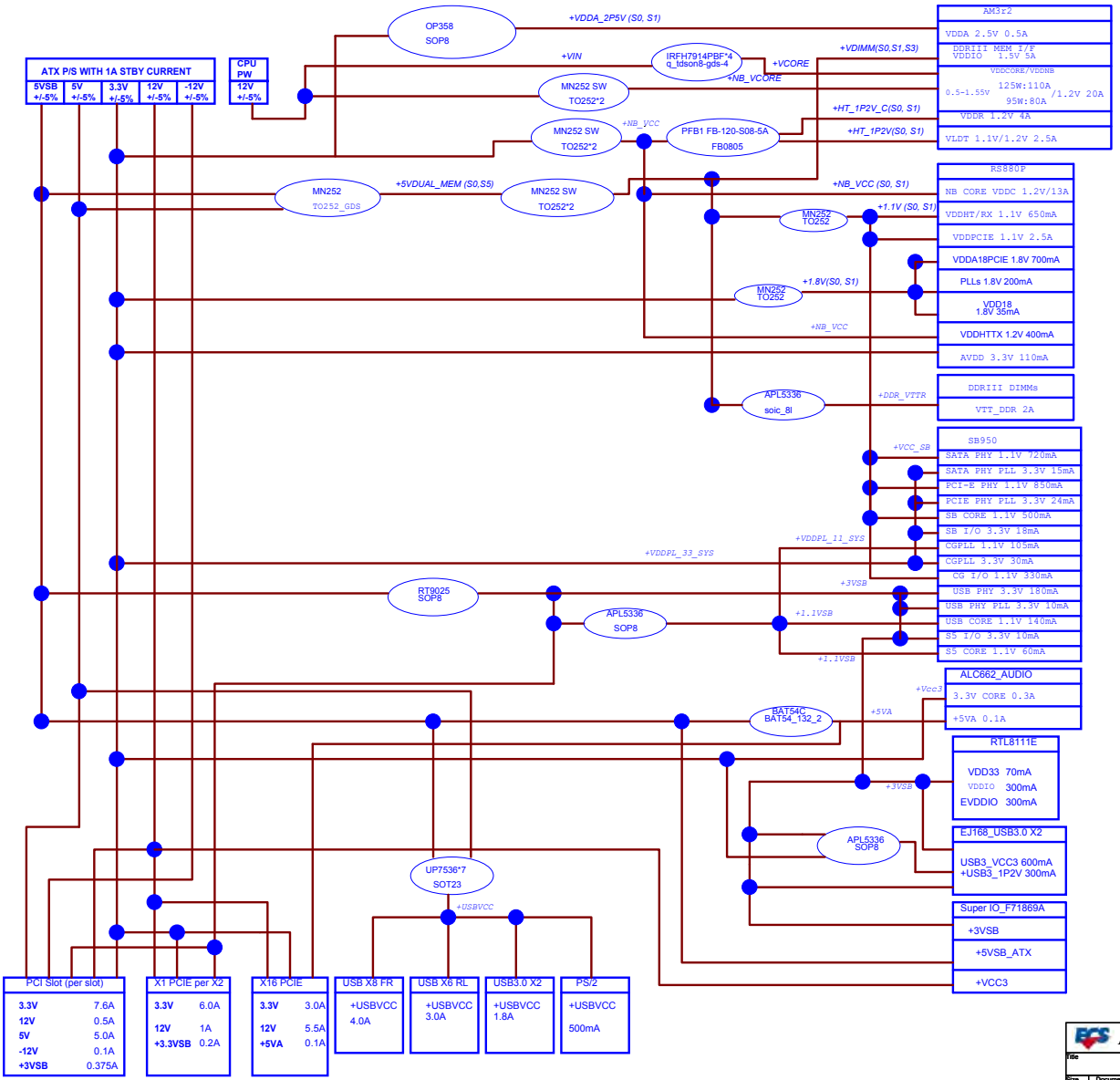

Elitegroup Computer Systems

Title: Power Distribution

Size | Document Number: RS880PM-AM | Rev: 1.0

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REVISION HISTORY:

Rev	Date	Notes
A	2011-01	
B	2011-03-08	Page 04 Net name SCLK3, SDATA3 change to SIC, SID. R202, R208, R212 change to Short Pad. R186 stuff for AM3 compatible. Add DRPCTRL circuit. Page 05 For AMD Validation fine tune. Del SC59,SC60,SC61,SC66,SC67,SC68 Add C584~C591, SC149~SC154 SC33,SC155,SC156 (POS CAP 330uF) Page 06 R248 change to 1K-04 for AM3r2 Schematic Checklist update. R228 R230 QN2 can be un-populated. Page 10 +NB_VCC change to +VDD_PCIE Page 11 R136, SR1 change to Short Pad. Reserve SC148 for meet Dory CRB. PCIE_RST- rename to A_RST- +NB_VCC change to +VDD_PCIE Del R106,R113 Add R107,U20 for Sequence. Page 12 PCIE_RST- rename to A_RST- RJ2,RJ3 change to 5% resistor. Page 13 Add +VDD_PCIE Page 14 PCIE_RST_GFX- rename to PCIE_RST- PCIE_RST- rename to A_RST- A_RST- rename to A_RST R337,R340 change to 22-04 C434,C437 stuff for SI Page 15 R346 not stuff because SB950 have internal PU. Stuff C416 for SI. Page 16 SATA1~SATA6 change PCB footprint to 2.0 type. Page 19 C11 not stuff. C45 stuff for EMI C24,C25 change to 47pF for I2C rising time Page 20 PCIE_RST- rename to A_RST- C13,C74,C75,C99,C396,C398,C444,C450,C451 for EMI Page 21 C13,C74,C75,C99,C396,C398,C444,C450,C451 for EMI Page 22 C393,C399 for EMI Page 23 PCIE_RST- rename to A_RST- Net name SCLK3, SDATA3 change to SIC, SID. Net name TSI_CLK, TSI_SDA change to TSI_SCLK, TSI_SDATA. Page 24 C68, C69, C70, C71 change to CN1. CN1 Pin2 and Pin8 swap for layout modify. C51 for EMI Page 25 PCIE_RST_GFX- rename to PCIE_RST- R71 for onboard LAN S3/S4/S5 WOL C58 for EMI Page 26 R84, R92 change to Short Pad. Page 27 Reserve R108 for SB950 internal PU. C85,C97,C100,C101,C113 for EMI Page 28 PCIE_RST_GFX- rename to PCIE_RST- Del RN1, RN2 Page 29 SR31 reserve for VGA noise. C581,C582 reserve for +VCC noise interference PS/2 signal. C583 reserve stitching capacitor. L26 co-layout L16 for 95W solution. Design change for AMD Validation Test, please refer to p.29 . Page 30 Design change for Validation Test, please refer to p.30. EC55,EC59 change value and footprint. ER68 change to 3.9K for DC. Page 31 Reserve R259,R343,R352,C456,C579,C580 for oscillationoccur can fine tune. ER9 change to 1.07K for DC. C443 stuff for soft start. Page 32 R373 chane to 130-04 for LED current fix. Page 33 NB Heat Sink chane Height to 25mm P/N:20-120-011492 Page 34 Del R383, add R384 for meet Acer consumer spec. Reserve D22 for reset issue.
1.0	2011-04-21	Page 04 Del MN6,MN8,MN9, add U26,U27,U30 for PWROK, LDT_RST#, LDT_STOP# Rising Time. Page 05 Add C242(4.7uF change to 22uF),C584,C585 for AMD validation test. Page 06 Del HDT connector miscellaneous components. Page 11 Del MN3,R111, add U19 for AMD Power Sequence. Del R107,R112, add R105,R106 for SI Sequence. Page 14 GPP_TX0P/N, GPP_RX0P/N shift to GPP_TX3P/N, GPP_RX3P/N for LAN PME. Del C433,C435,SR22,SR23 (USB3.0 change to reserve) Add R300,R302,SR15 for PWROK,LDT_RST#,LDT_STOP# Rising Time. Add Acer Power on w/o battery circuit. Page 15 Add Net USB3_RI- for USB3.0 wake up. Del R349 (USB3.0 change to reserve) Page 16 Del SPI_DEBUG1 for A5 stage. Page 19 Del C45 for EMI. Page 23 +RTCVCC rename to +VBAT_IO. Del R376,R377,R378 for internal PD. Add C601 for stabilized voltage.
1.0(.)	2011-05-12	Page 04 Change U26,U27,U30 to 74AUP1G07GW for PWROK, LDT_RST#, LDT_STOP# Rising Time. Add MN21,MN22,R461,ER102 for PWM Offset control. Page 11 Change U19 to 74AUP1G07GW and add R111 for AMD Power Sequence. Page 14 Add C433,C435,SR22,SR23 (USB3.0 change to stuff). C413,C414 change to 27P-04 for dynamic RTC. Del D23 and add R461 for follow AMD DG. Page 23 Add D27 to prevent voltage flow backward. Page 28 USB3.0 change to stuff. Page 29 Del ER50 for Offset control. Page 31 ER33 change to 18.7K-1-04 for OCP. ER72 change to 8.2K-1-04 ER73 change to 6.49K-1-04 for +1.1V.

Elitegroup Computer Systems

Title: History

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