RS780Q-LM3 VER:1.01

2009 / 11 / 9

SCHEMATICS TABLE:

PCB Size: 244mm*224mm

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTOM
2116, 5mils, 60 ohm

GPIO Pin

SB710

Name	Pin	Voltage	Function	Note
IMC_GPIO8	A18	3.3V_S5	F_USB1 detect	
IMC_GPIO9	B18	3.3V_S5	F_USB2 detect	
IMC_GPIO10	F21	3.3V_S5	F_USB3 detect	
IMC_GPIO11	D21	3.3V_S5	LC CLR_CMOS	
GPIO5	Y19	3.3V	F_AUDIO detect	
GPIO14	J1	3.3V_S5	Use to control USB dual power	default=Low

ITE8720

Name	Pin	Voltage	Function	Note
GP14	31	5V	COM1 detect	
GP22	25	5V_S5	Power LED0	
GP23	24	5V_S5	Power LED1	
GP30	19	5V	BEEP	
GP31	18	5V	BIOS reserve	
GP34	14	5V	BIOS reserve	
GP35	13	5V	BIOS reserve	
GP40	79	5V_S5	VDIMM Dual switch	
GP33	16	5V	Sensor header ID1	
GP47	66	5V	Sensor header ID2	
GP50	48	5V	BIOS reserve	

Elitegroup Computer Systems

Title: Cover Page

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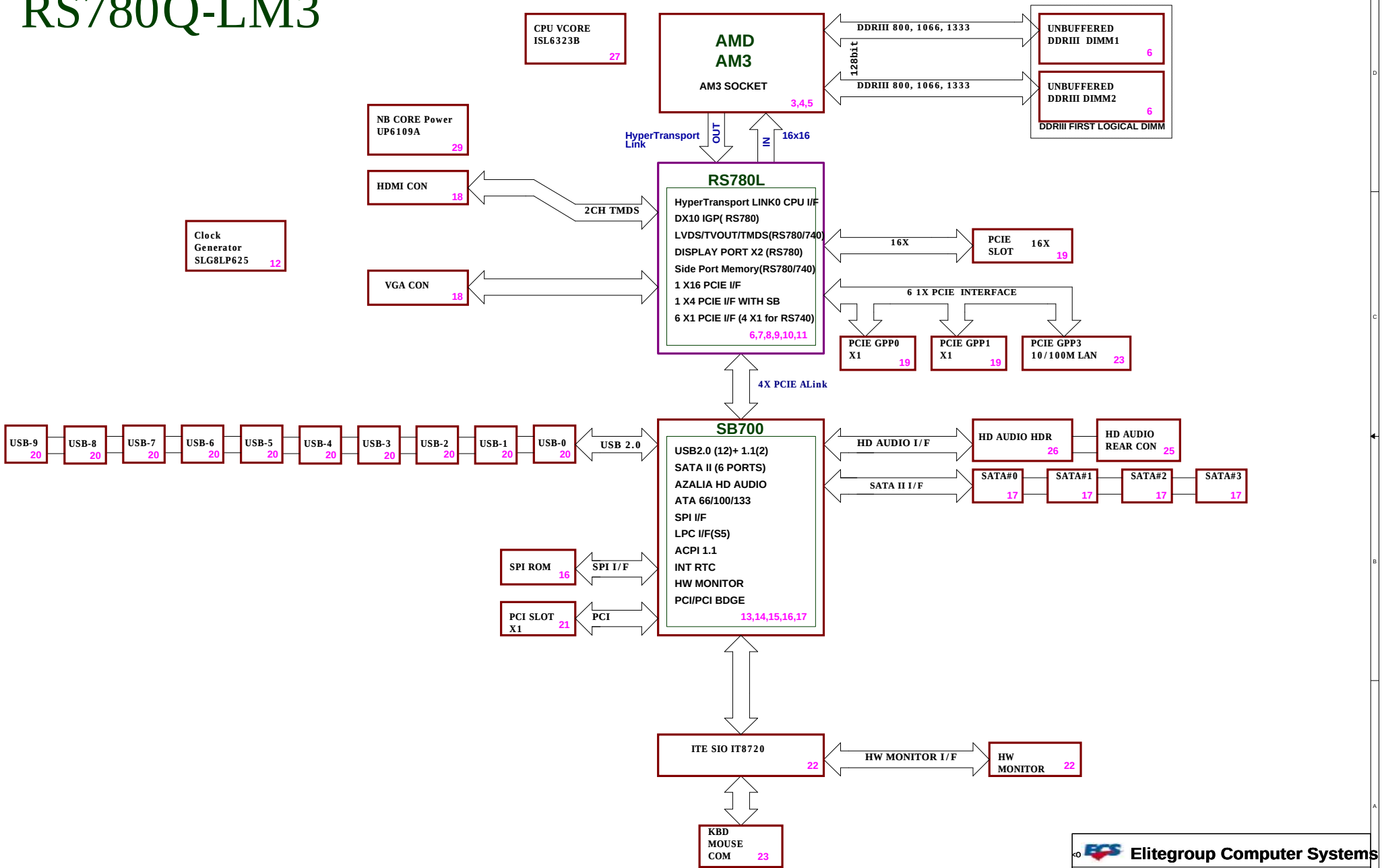
RS780Q-LM3



Elitegroup Computer Systems

Title	BLOCK DIAGRAM	
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
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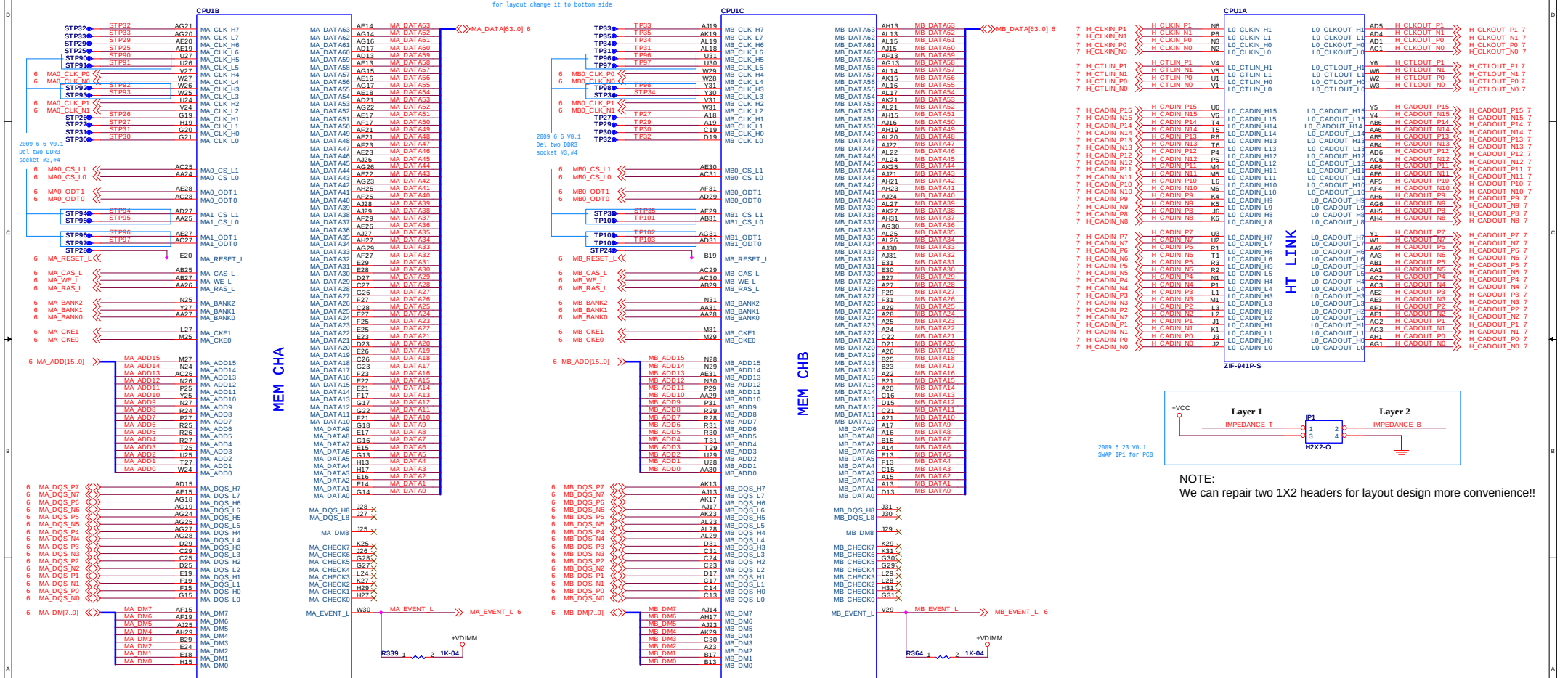
CPU Memory

DDR3 Memory Interface A

DDR3 Memory Interface B

HT LINK



NOTE:
We can repair two 1X2 headers for layout design more convenience!!

Elitegroup Computer Systems			
Title: HT,CPU MEMORY			
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CPU Control and Miscellaneous

VDDA_2P5V for CPU PLL

VDDA_2P5V@250mA

Note: Update with new clock termination scheme, if necessary.

2009 6 24 V0.1 Add FB17 stuff 0 ohm for SI

2009 11 9 V1.0 to V1.01 Change EC43 from 100uF to 470uF for VDDA_1_2 overshoot

2009 6 6 V0.1 The Side Band Interface bus is not used and del ohm for cost down Del R269,R251,R248

2009 6 6 V0.1 Del level shift for cost down

2009 6 6 V0.1 The Side Band Interface bus is not used and del ohm for cost down

FDV301N-S 03-050-530106

2009 6 6 V0.1 The Side Band Interface bus is not used for cost down

2009 6 6 V0.1 RN8 reserved for cost down

2009 6 29 V0.1 Add R240 reserved for PSI_L function

2009 6 6 V0.1 Del R282,R292 for cost down

2009 9 17 V0.2 to V1.0 Stuff R252 300-04 for DBREQ_L should not be lower than VIH min during normal processor operation from AMD Family 10h PEDS.

2009 7 29 V0.1 to V0.2 C65 stuff 10u-08 for SI

2009 6 6 V0.1 C65 reserved for cost down

2009 7 31 V0.1 to V0.2 Add reserved C299,C300 for SI

Place witin 500 mils of the CPU socket.

Use buffered reset

HDT Header

AM3 Top View

Title	CPU CONTROL & MISC
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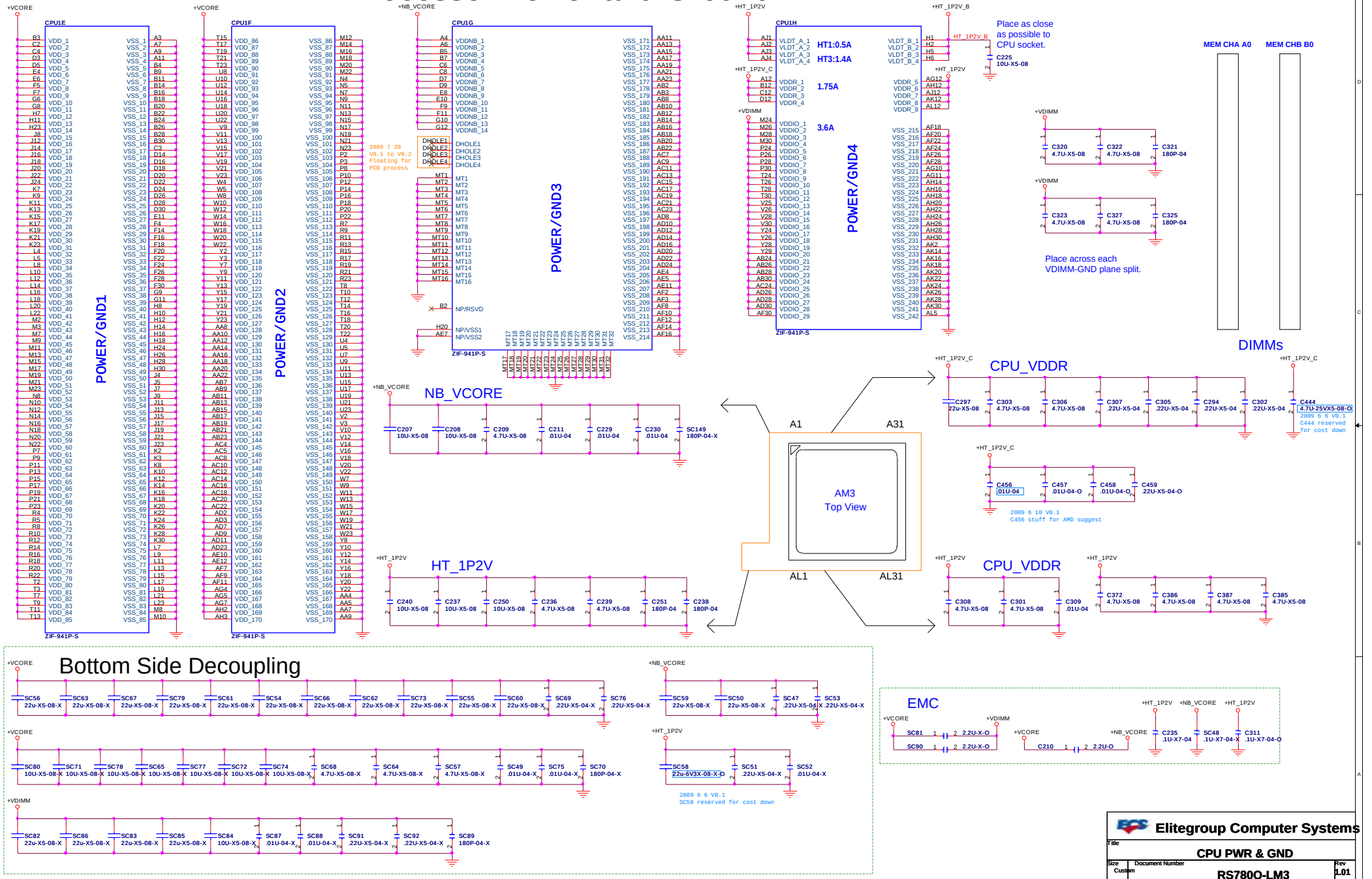
Elitegroup Computer Systems

Processor Power and Ground



Bottom Side Decoupling

EMC

Elitegroup Computer Systems		
Title: CPU PWR & GND		
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
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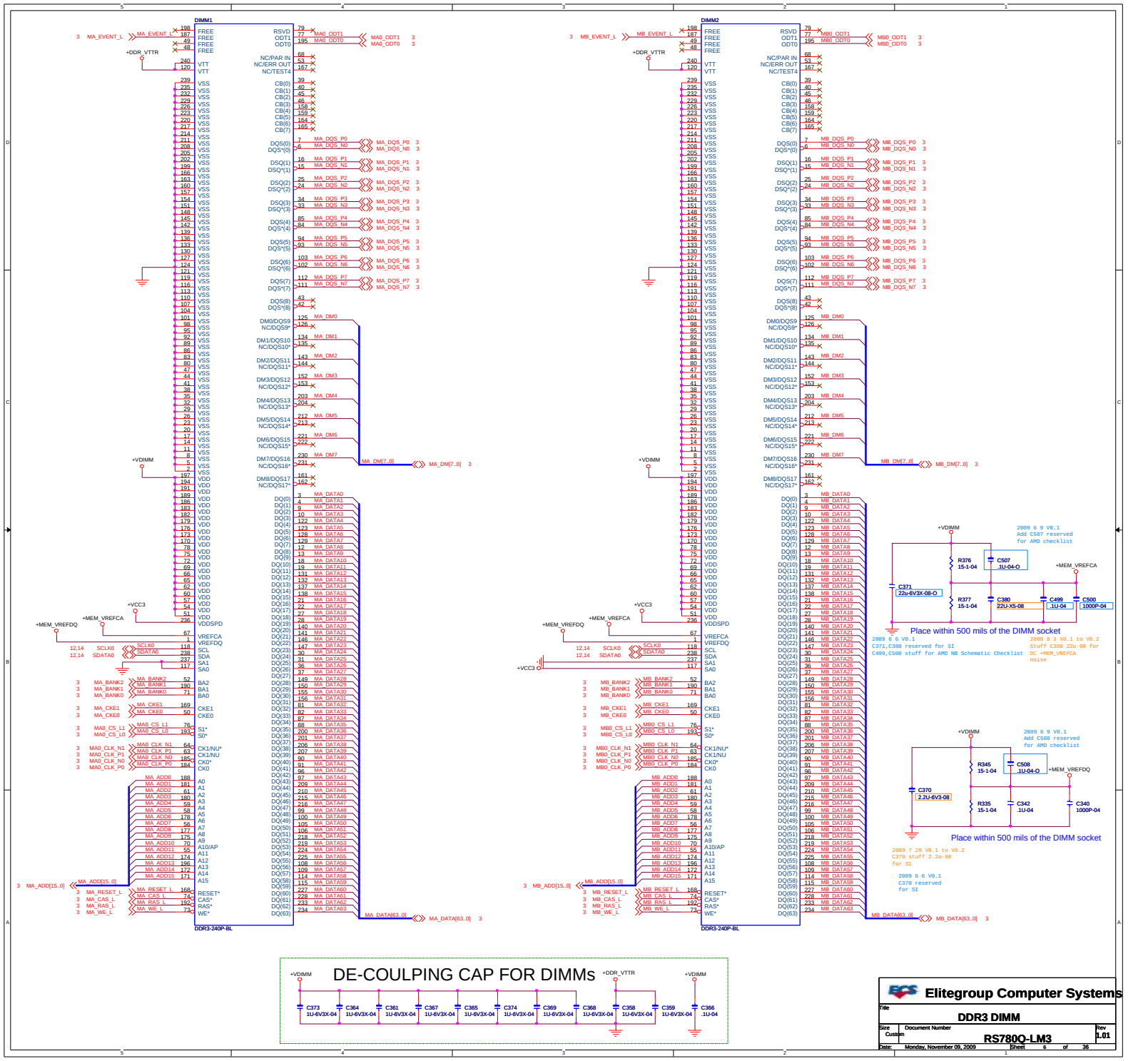
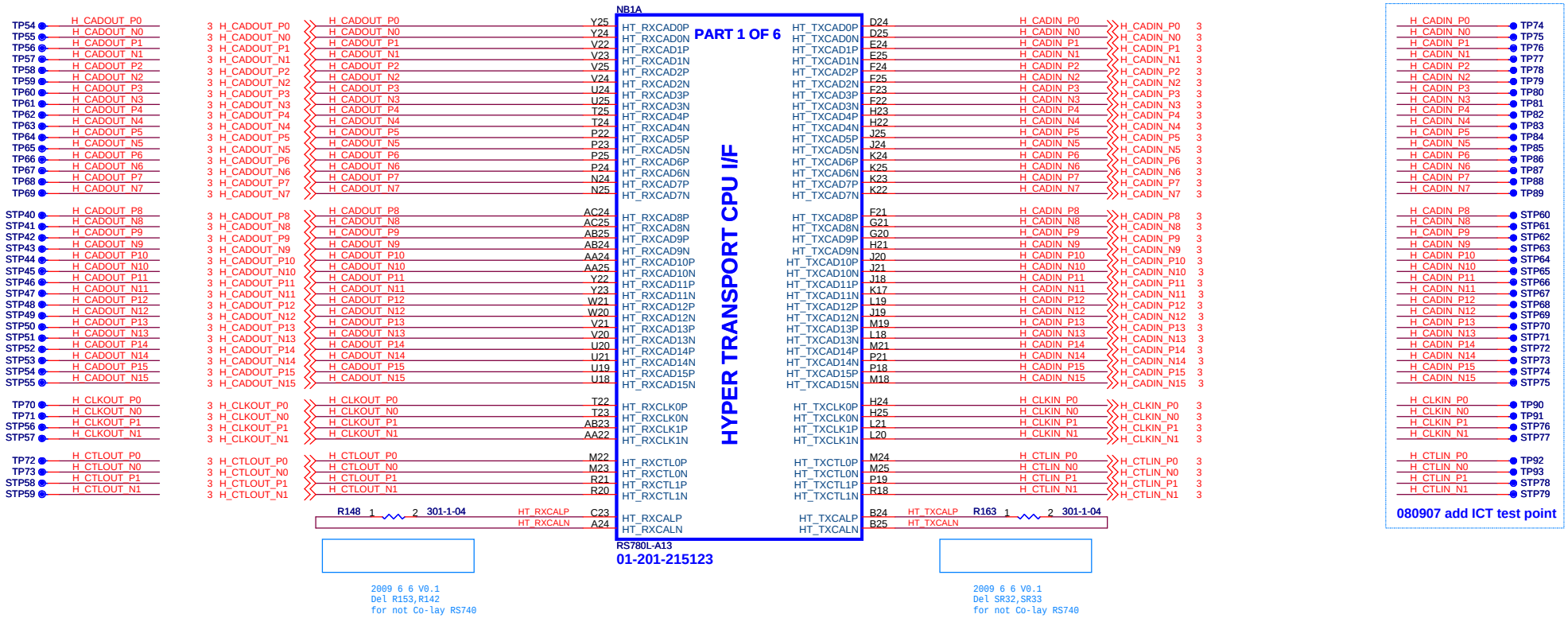
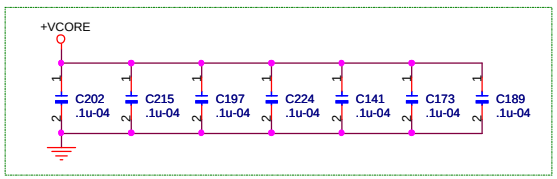

DIMM1
DIMM2
DDR3-240P-BL
DDR3-240P-BL
MA_EVENT_L
MB_EVENT_L
+DDR_VTTR
+VDIMM
+VCC3
+MEM_VREFCA
+MEM_VREFDQ
MA_DM[7..0]
MB_DM[7..0]
MA_DATA[63..0]
MB_DATA[63..0]
MA_ADD[15..0]
MB_ADD[15..0]
MA_RESET_L
MB_RESET_L
MA_CAS_L
MB_CAS_L
MA_RAS_L
MB_RAS_L
MA_WE_L
MB_WE_L
MA0_ODT1
MA0_ODT0
MB0_ODT1
MB0_ODT0
MA_DQS_P0
MA_DQS_N0
MB_DQS_P0
MB_DQS_N0
SCLK0
SDATA0
MA_BANK2
MA_BANK1
MA_BANK0
MB_BANK2
MB_BANK1
MB_BANK0
MA_CKE1
MA_CKE0
MB_CKE1
MB_CKE0
MA0_CS_L1
MA0_CS_L0
MB0_CS_L1
MB0_CS_L0
MA0_CLK_N1
MA0_CLK_P1
MA0_CLK_N0
MA0_CLK_P0
MB0_CLK_N1
MB0_CLK_P1
MB0_CLK_N0
MB0_CLK_P0
Place within 500 mils of the DIMM socket
Place within 500 mils of the DIMM socket
DE-COULPING CAP FOR DIMMs
C373 1U-6V3X-04
C364 1U-6V3X-04
C361 1U-6V3X-04
C367 1U-6V3X-04
C365 1U-6V3X-04
C374 1U-6V3X-04
C369 1U-6V3X-04
C368 1U-6V3X-04
C358 1U-6V3X-04
C359 1U-6V3X-04
C366 .1U-04
Elitegroup Computer Systems
DDR3 DIMM
RS780Q-LM3
Monday, November 09, 2009



HT LINK STITCHING CAPS.



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Title	RS780-HT LINK I/F	
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
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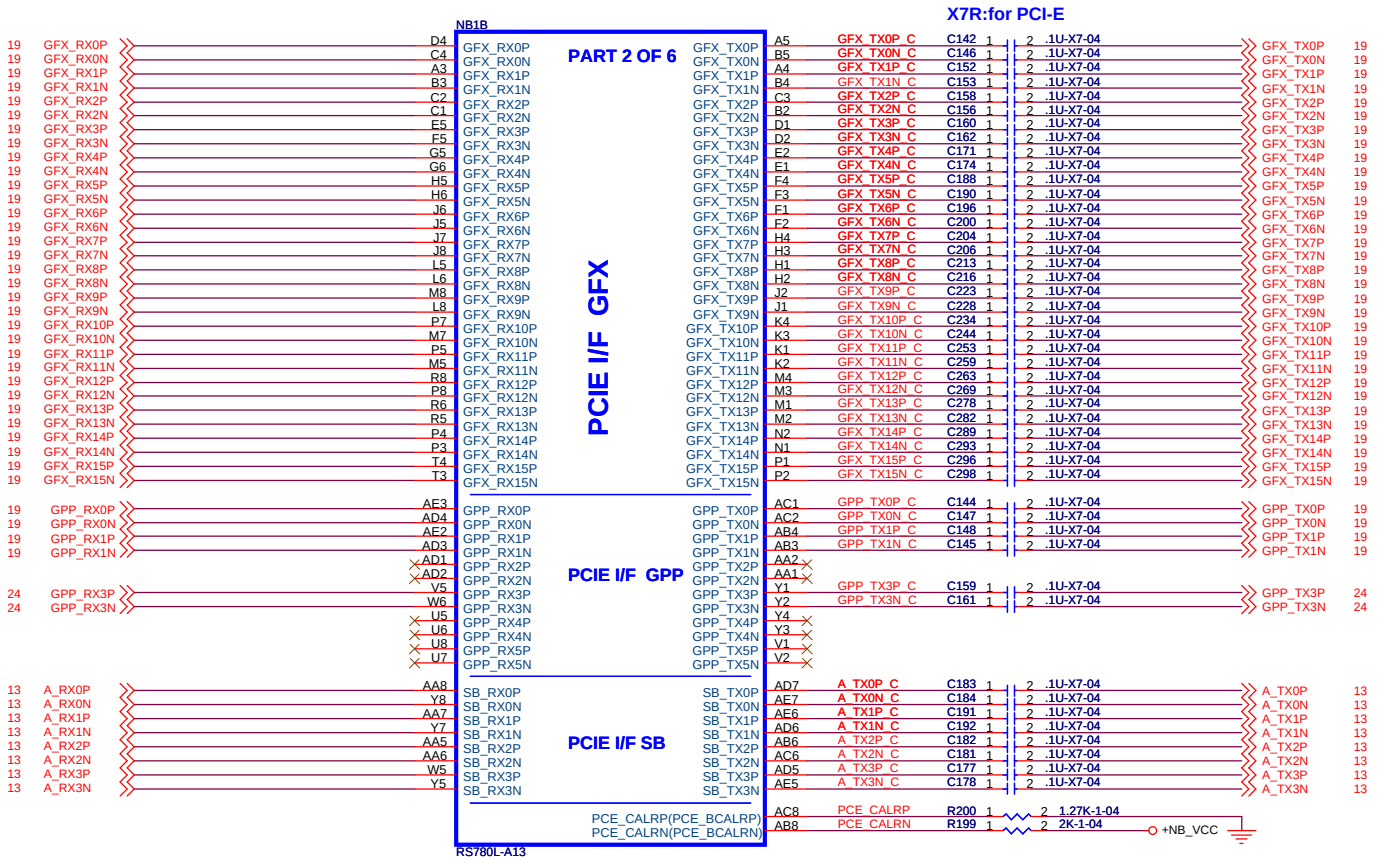
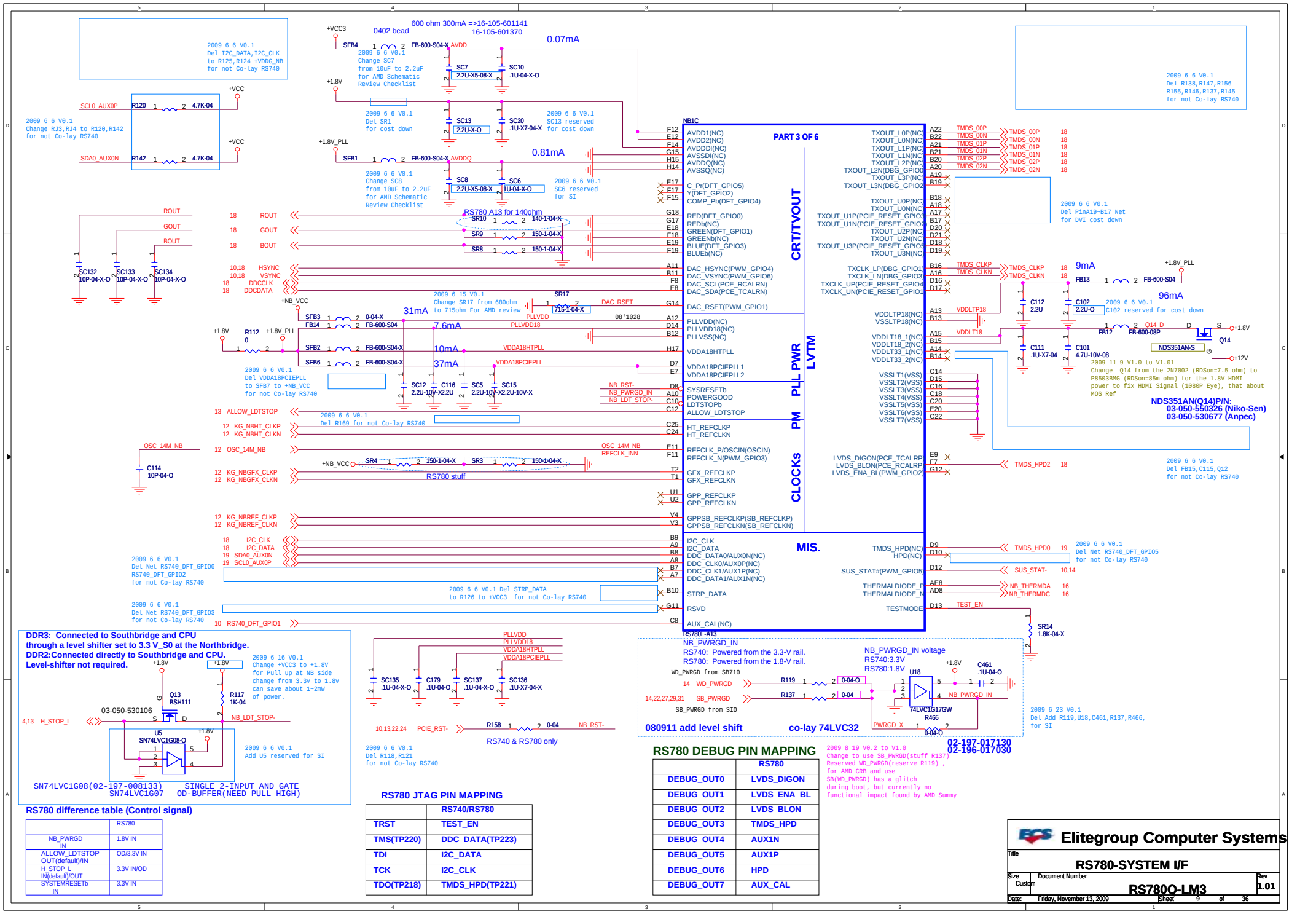


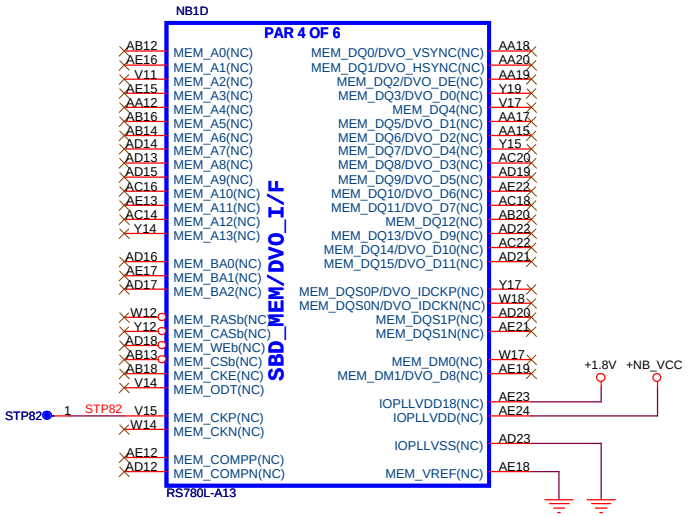
Elitegroup Computer Systems		
Title: RS780-PCIE I/F		
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
Date: Monday, November 09, 2009	Sheet 8 of 36	



	RS780
NB_PWRGD IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OD/3.3V IN
H_STOP_L IN(default)/OUT	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN

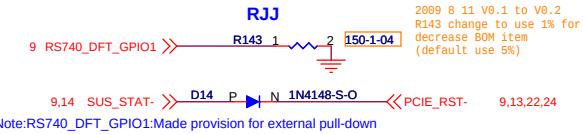
	RS740/RS780
TRST	TEST_EN
TMS(TP220)	DDC_DATA(TP223)
TDI	I2C_DATA
TCK	I2C_CLK
TDO(TP218)	TMDS_HPD(TP221)

	RS780
DEBUG_OUT0	LVDS_DIGON
DEBUG_OUT1	LVDS_ENA_BL
DEBUG_OUT2	LVDS_BLON
DEBUG_OUT3	TMDS_HPD
DEBUG_OUT4	AUX1N
DEBUG_OUT5	AUX1P
DEBUG_OUT6	HPD
DEBUG_OUT7	AUX_CAL



RS740/RS780 STRAPS

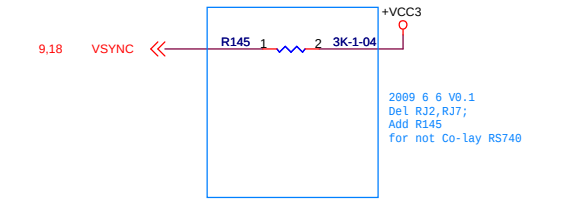
Note: for RS780, change RJJ to 150R as AUX_CAL,place close to pin C8



Note:RS740_DFT_GPIO1:Made provision for external pull-down which is not installed by default. Northbridge has an internal pull-up for bypassing EEPROM strapping and using default values for RS740

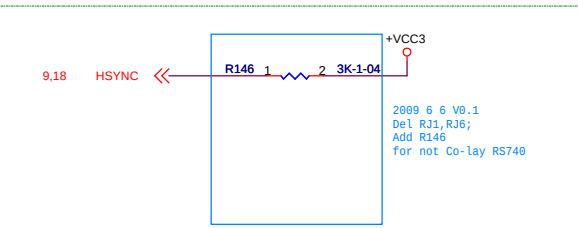
RS740/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740: pin DFT_GPIO1
RS780: pin SUS_STAT#



RS740/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RS780: pin VSYNC



RS740/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC

RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus using PCIE bus
1. Disable (can be enabled thru nbcfg register)
0 : Enable
RS780: configurable thru register setting only
RS740: Not supported

Elitegroup Computer Systems		
Title: RS780-SPMEM/STRAPS		
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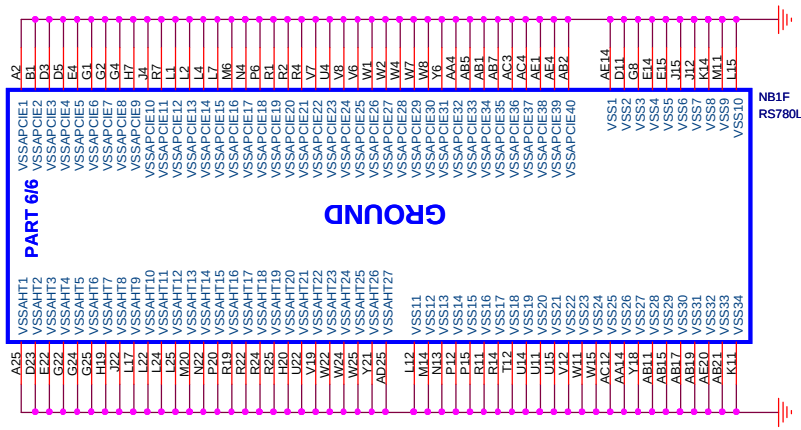
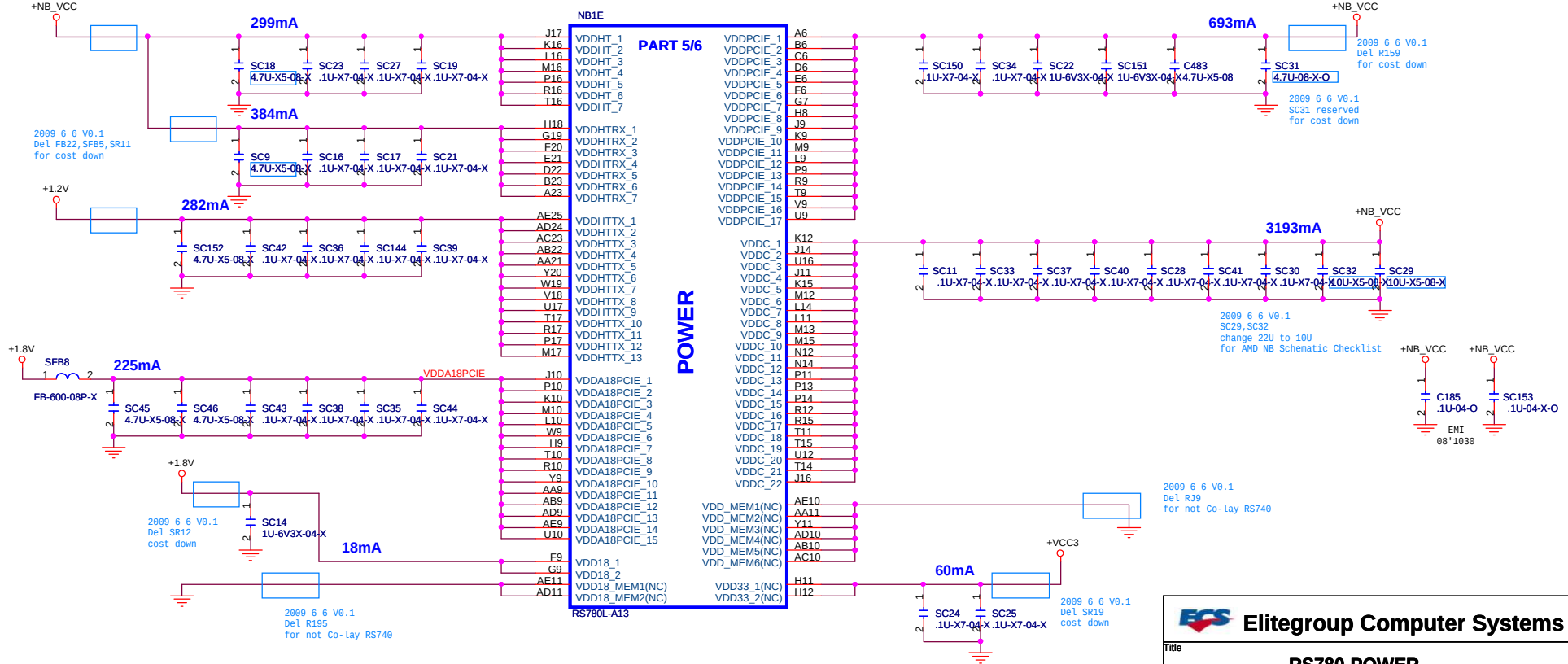
RS740/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RS780	PIN NAME	RS740	RS780
VDDHT	NC	+1.1V	IOPLLVDD	+1.2V	+1.1V
VDDHTRX	NC	+1.1V	AVDD	+3.3V	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	+1.8V	+1.8V
VDDA18PCIE	NC	+1.8V	AVDDQ	+1.8V	+1.8V
VDD18	+1.8V	+1.8V	PLLVDD	+1.2V	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	+1.8V	+1.8V
VDDPCIE	+1.2V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V
VDDC	+1.2V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	+1.8V	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	+1.8V
VDD33	+3.3V	+3.3V	VDDLT18	+1.8V	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	+3.3V	NC



2009 6 10 V0.1
change SC18~ SC9 from 22U to 4.7U
for AMD Schematic Checklist



Elitegroup Computer Systems		
Title: RS780-POWER		
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
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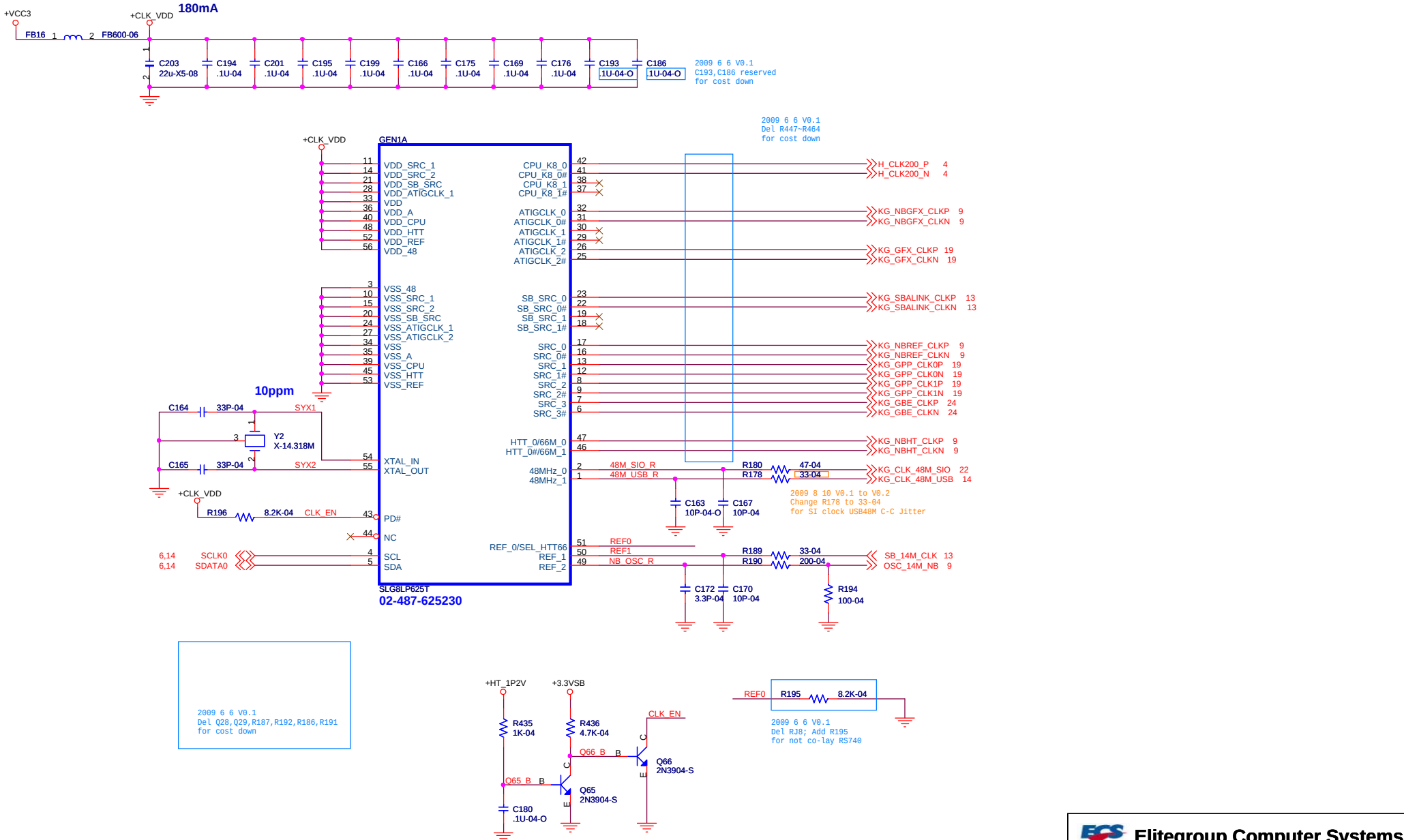

Elitegroup Computer Systems

Title: CLOCK GENERATOR SLG8LP625

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2009 8 4 V0.1 to V0.2
R359 change to 22-04
for SI PCIE reset ring down

SB1A

SB700
Part 1 of 5

PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC

SB700 A12 / SB750 A12: Not connected.
SB700 A13 / SB750 A13 / SB710:
Crystal Oscillator Used: Connected to the 14.318180-MHz XTAL (± 20 PPM) with a 22-pF (preliminary value) cap to GND and a 10-M? 5% resistor to 25M_X2.
OR
Crystal Oscillator Not Used: Connected to a 14-MHz clock from the external clock generator and terminated per the external CLKGEN requirements. Used 110-? 1% series termination resistor and 75-? 1% resistor to GND to limit signal swing to 1.2 V.

2009 6 6 V0.1
Del R424
for cost down

2009 7 29 V0.1 to V0.2
Change crystal X1 library for
Lenovo request change holder

2009 7 29 V0.1 to V0.2
Add test point STP1,
STP2 for ICT test

2009 7 29 V0.1 to V0.2
Change crystal holder for
Lenovo request

2009 6 16 V0.1
Add test point TP104,TP105
for AMD review

2009 6 6 V0.1
Del R485,R506,507,R508,R437,R509 for cost down

2009 6 6 V0.1
Del R443 for cost down

2009 6 6 V0.1
Del Net INTRUDER_L
for del case open function

2009 8 11 V0.1 to V0.2
R313 change to use 5% for
follow CRB and decrease BOM item

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

INTRUDER_ALERT# if no use, it have internal pull high 500K to VBAT

SB710
01-201-700122

for SI reserve
0.1A to 1.0

Elitegroup Computer Systems

Title: SB710-PCIE/PCI/CPU/LPC/CLK

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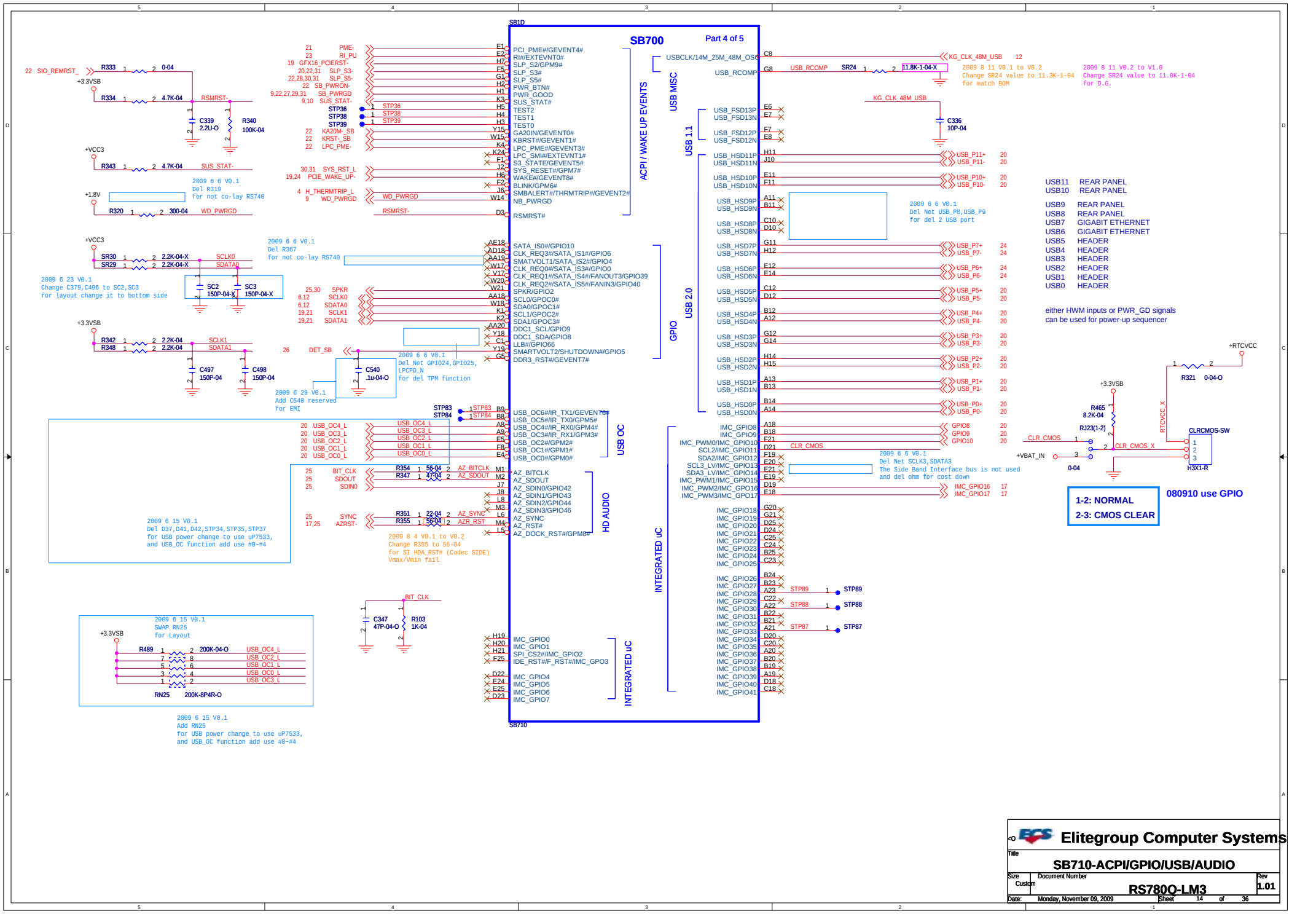
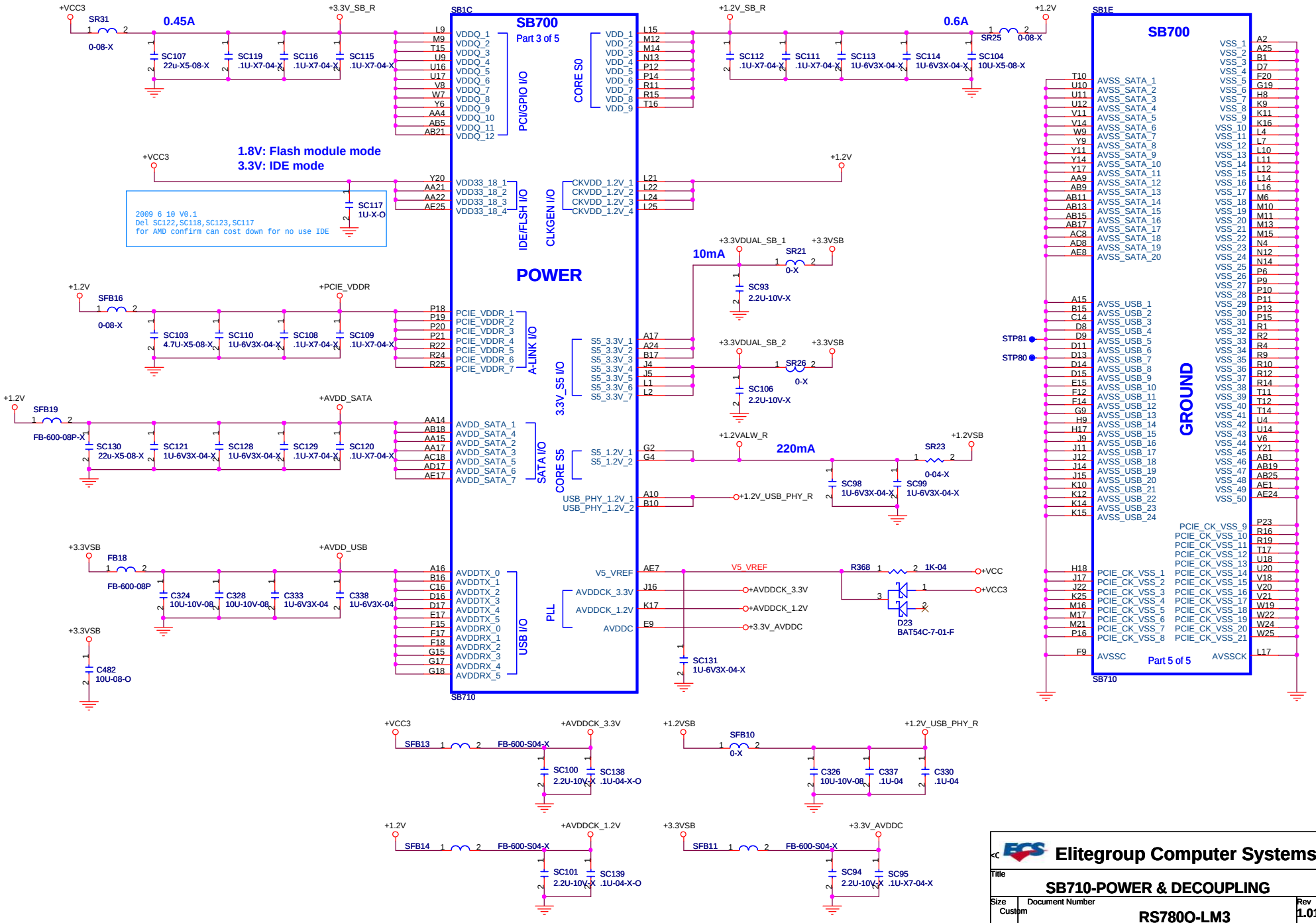
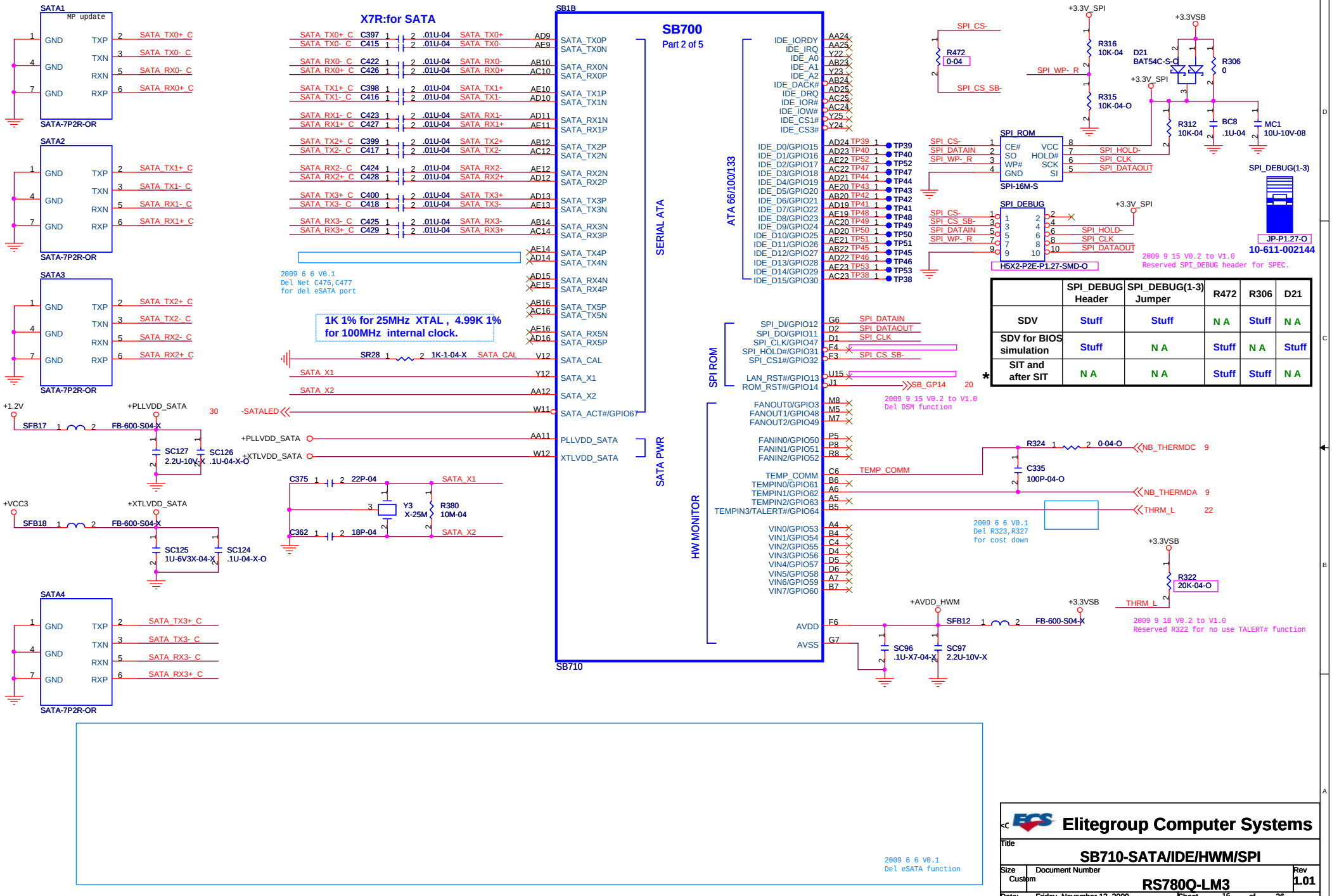

SB1D
SB700
Part 4 of 5
PCI_PME#/GEVENT4#
RI##/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB MISC
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB 1.1
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMATVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
GPIO
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
HD AUDIO
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
INTEGRATED uC
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
INTEGRATED uC
SB710
KG_CLK_48M_USB
USB_RCOMP
SR24
11.8K-1-04-X
2009 8 11 V0.1 to V0.2
Change SR24 value to 11.3K-1-04
for match BOM
2009 8 11 V0.2 to V1.0
Change SR24 value to 11.8K-1-04
for D.G.
C336
10P-04
USB_P11+
USB_P11-
USB_P10+
USB_P10-
USB_P7+
USB_P7-
USB_P6+
USB_P6-
USB_P5+
USB_P5-
USB_P4+
USB_P4-
USB_P3+
USB_P3-
USB_P2+
USB_P2-
USB_P1+
USB_P1-
USB_P0+
USB_P0-
2009 6 6 V0.1
Del Net USB_P8,USB_P9
for del 2 USB port
USB11 REAR PANEL
USB10 REAR PANEL
USB9 REAR PANEL
USB8 REAR PANEL
USB7 GIGABIT ETHERNET
USB6 GIGABIT ETHERNET
USB5 HEADER
USB4 HEADER
USB3 HEADER
USB2 HEADER
USB1 HEADER
USB0 HEADER
either HWM inputs or PWR_GD signals
can be used for power-up sequencer
+RTCVCC
R321 0-04-O
+3.3VSB
R465 8.2K-04
RJ23(1-2)
RTCVCC_X
CLRCMOS-SW
H3X1-R
CLR_CMOS
CLR_CMOS_X
+VBAT_IN
0-04
1-2: NORMAL
2-3: CMOS CLEAR
080910 use GPIO
22 SIO_REMRST_
R333 0-04
+3.3VSB
R334 4.7K-04
RSMRST-
C339 2.2U-O
R340 100K-04
+VCC3
R343 4.7K-04
SUS_STAT-
2009 6 6 V0.1
Del R319
for not co-lay RS740
+1.8V
R320 300-04
WD_PWRGD
21 PME-
23 RI_PU
19 GFX16_PCIERST-
20,22,31 SLP_S3-
22,28,30,31 SLP_S5-
22 SB_PWRON-
9,22,27,29,31 SB_PWRGD
9,10 SUS_STAT-
STP36
STP38
STP39
22 KA20M-_SB
22 KRST-_SB
22 LPC_PME-
30,31 SYS_RST_L
19,24 PCIE_WAKE_UP-
4 H_THERMTRIP_L
9 WD_PWRGD
RSMRST-
+VCC3
SR30 2.2K-04-X
SR29 2.2K-04-X
SCLK0
SDATA0
2009 6 23 V0.1
Change C379,C496 to SC2,SC3
for layout change it to bottom side
SC2 150P-04-X
SC3 150P-04-X
2009 6 6 V0.1
Del R367
for not co-lay RS740
25,30 SPKR
6,12 SCLK0
6,12 SDATA0
19,21 SCLK1
19,21 SDATA1
+3.3VSB
R342 2.2K-04
R348 2.2K-04
SCLK1
SDATA1
C497 150P-04
C498 150P-04
26 DET_SB
C540 .1u-04-O
2009 6 6 V0.1
Del Net GPIO24,GPIO25,
LPCPD_N
for del TPM function
2009 6 29 V0.1
Add C540 reserved
for EMI
STP83
STP84
20 USB_OC4_L
20 USB_OC3_L
20 USB_OC2_L
20 USB_OC1_L
20 USB_OC0_L
25 BIT_CLK
25 SDOUT
25 SDIN0
R354 56-04
R347 47-04
AZ_BITCLK
AZ_SDOUT
25 SYNC
17,25 AZRST-
R351 22-04
R355 56-04
AZ_SYNC
AZR_RST
2009 6 15 V0.1
Del D37,D41,D42,STP34,STP35,STP37
for USB power change to use uP7533,
and USB_OC function add use #0~#4
2009 8 4 V0.1 to V0.2
Change R355 to 56-04
for SI HDA_RST# (Codec SIDE)
Vmax/Vmin fail
BIT_CLK
C347 47P-04-O
R103 1K-04
2009 6 15 V0.1
SWAP RN25
for Layout
+3.3VSB
R489 200K-04-O
USB_OC4_L
USB_OC2_L
USB_OC1_L
USB_OC0_L
USB_OC3_L
RN25 200K-8P4R-O
2009 6 15 V0.1
Add RN25
for USB power change to use uP7533,
and USB_OC function add use #0~#4
IMC_GPIO16 17
IMC_GPIO17 17
STP89
STP88
STP87
2009 6 6 V0.1
Del Net SCLK3,SDATA3
The Side Band Interface bus is not used
and del ohm for cost down
Elitegroup Computer Systems
Title
SB710-ACPI/GPIO/USB/AUDIO
Size Custom
Document Number
RS780Q-LM3
Rev 1.01
Date: Monday, November 09, 2009
Sheet 14 of 36

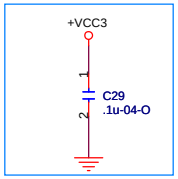

SB1C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
CORE S5
SATA I/O
USB I/O
PLL
SB710
SB1E
SB700
GROUND
Part 5 of 5
SB710
0.45A
0.6A
10mA
220mA
1.8V: Flash module mode
3.3V: IDE mode
2009 6 10 V0.1
Del SC122,SC118,SC123,SC117
for AMD confirm can cost down for no use IDE
+VCC3
+3.3V_SB_R
+1.2V_SB_R
+1.2V
+3.3VDUAL_SB_1
+3.3VDUAL_SB_2
+3.3VSB
+1.2VALW_R
+1.2VSB
+PCIE_VDDR
+AVDD_SATA
+AVDD_USB
+1.2V_USB_PHY_R
V5_VREF
+AVDDCK_3.3V
+AVDDCK_1.2V
+3.3V_AVDDC
+VCC
+VCC3
STP81
STP80
SR31 0-08-X
SR25 0-08-X
SR21 0-X
SR26 0-X
SR23 0-04-X
SFB16 0-08-X
SFB19 FB-600-08P-X
FB18 FB-600-08P
SFB13 FB-600-S04-X
SFB10 0-X
SFB14 FB-600-S04-X
SFB11 FB-600-S04-X
R368 1K-04
D23 BAT54C-7-01-F
SC107 22u-X5-08-X
SC119 .1U-X7-04-X
SC116 .1U-X7-04-X
SC115 .1U-X7-04-X
SC112 .1U-X7-04-X
SC111 .1U-X7-04-X
SC113 1U-6V3X-04-X
SC114 1U-6V3X-04-X
SC104 10U-X5-08-X
SC117 1U-X-O
SC93 2.2U-10V-X
SC106 2.2U-10V-X
SC103 4.7U-X5-08-X
SC110 1U-6V3X-04-X
SC108 .1U-X7-04-X
SC109 .1U-X7-04-X
SC130 22u-X5-08-X
SC121 1U-6V3X-04-X
SC128 1U-6V3X-04-X
SC129 .1U-X7-04-X
SC120 .1U-X7-04-X
SC98 1U-6V3X-04-X
SC99 1U-6V3X-04-X
SC131 1U-6V3X-04-X
C324 10U-10V-08
C328 10U-10V-08
C333 1U-6V3X-04
C338 1U-6V3X-04
C482 10U-08-O
SC100 2.2U-10V-X
SC138 .1U-04-X-O
SC101 2.2U-10V-X
SC139 .1U-04-X-O
C326 10U-10V-08
C337 .1U-04
C330 .1U-04
SC94 2.2U-10V-X
SC95 .1U-X7-04-X
Elitegroup Computer Systems
SB710-POWER & DECOUPLING
RS780Q-LM3
Size Custom
Document Number
Rev 1.01
Date: Friday, November 13, 2009
Sheet 15 of 36



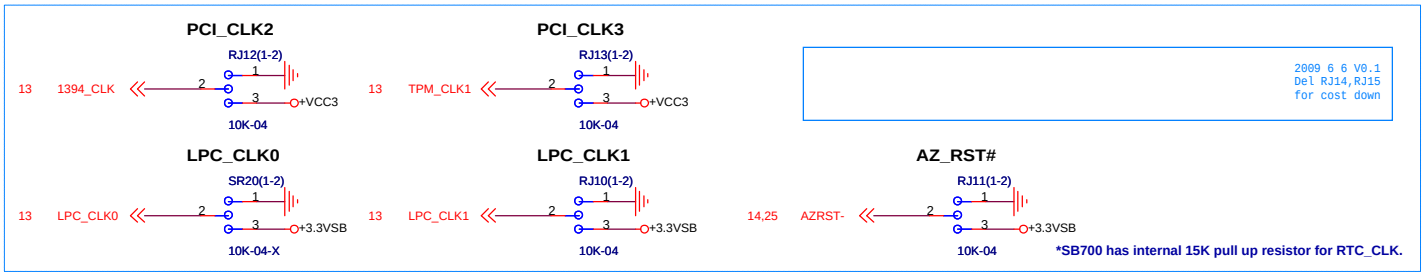
	SPI_DEBUG Header	SPI_DEBUG(1-3) Jumper	R472	R306	D21
SDV	Stuff	Stuff	N A	Stuff	N A
SDV for BIOS simulation	Stuff	N A	Stuff	N A	Stuff
SIT and after SIT	N A	N A	Stuff	Stuff	N A

Title	SB710-SATA/IDE/HWM/SPI
Size	Custom
Document Number	RS780Q-LM3
Rev	1.01
Date:	Friday, November 13, 2009
Sheet	16 of 36

Elitegroup Computer Systems



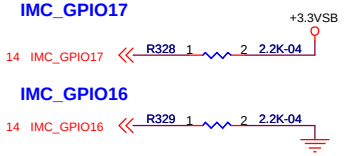
2009 6 29 V0.1
Add C29 reserved
for EMI



2009 6 6 V0.1
Del RJ14,RJ15
for cost down

*SB700 has internal 15K pull up resistor for RTC_CLK.

STRAP of ROM select---Default is SPI ROM



IMC_GPIO17	IMC_GPIO16
ROM TYPE:	
H, H = Reserved	
H, L = SPI ROM DEFAULT	
L, H = LPC ROM	
L, L = FWH ROM	

REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3			LPC_CLK0	LPC_CLK1	AZ_RST#
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS			ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT

Elitegroup Computer Systems

Title: SB710-STRAPS

Size: Custom | Document Number: RS780Q-LM3 | Rev: 1.01

Date: Thursday, November 12, 2009 | Sheet 17 of 36

RS780 A13 *:
- GREEN/BLUE: Connected to GND through two separate 150-? 1% resistors.
- RED: Connected to GND through two separate 140-? 1% resistors.

2009 7 30 V0.1 to V0.2
Add reserved +VCC_VGA source
for HDMI

2009 6 30 V0.1
Change Location to VGA
for Lenovo request

2009 7 28 V0.1 to V0.2
Add reserved C5,C6,C7 for VGA noise

Close to Connector

2009 7 28 V0.1 to V0.2
Power name Change +VCC_DDC_VGA
for DVI change to HDMI

RS780:5V,4.7K

2009 8 4 V0.1 to V0.2
Net I2C_DATA,I2C_CLK
add reserved D37,D34,C343,C344
for ESD

2009 6 6 V0.1
Del level shift
for not co-lay RS740

2009 7 30 V0.1 to V0.2
Add reserved +VCC_VGA source
for HDMI

2009 7 28 V0.1 to V0.2
Change DVI to HDMI
for Lenovo SPEC. change

HDMI Conn. P/N:
10-083-019691 (HI-TOP)

AZ1045-04QU-S Note:
1.The VCC to GND capacitors(C254,C255) pull between
pin3 whit pin8 and use minimum via (have induction)
default reserved (Stuff ESD IC)
2.The ESD IC Pin 6, 7, 9, 10 NC for layout trace can do
a beeline

2009 8 4 V0.1 to V0.2
U8 pin1,2;9,10 and 4,5;7,6
swap for HDMI Layout

2009 7 31 V0.1 to V0.2
SC142,SC143 change to top side,
rename to C254,C255

2009 6 6 V0.1
Del for NB use RS760,
for DVI Single-Link (RS760 only support Single-Link)

2009 6 19 V0.1
SWAP CHOKE19~CHOKE22
for Layout

2009 8 4 V0.1 to V0.2
CHOKE21,CHOKE22
swap for HDMI Layout

For HDMI CHOKE P/N:
16-400-900143 (TAI-TECH)
16-400-900171 (Magic)

2009 11 9 V1.0 to V1.01
CHOKE19,CHOKE20,CHOKE21,CHOKE22
change use to HDMI CHOKE for SI(1080P Eye)

If reserved HDMI or DVI,
R61and R68 must stuff or
monitor have blinking issue from Lenovo

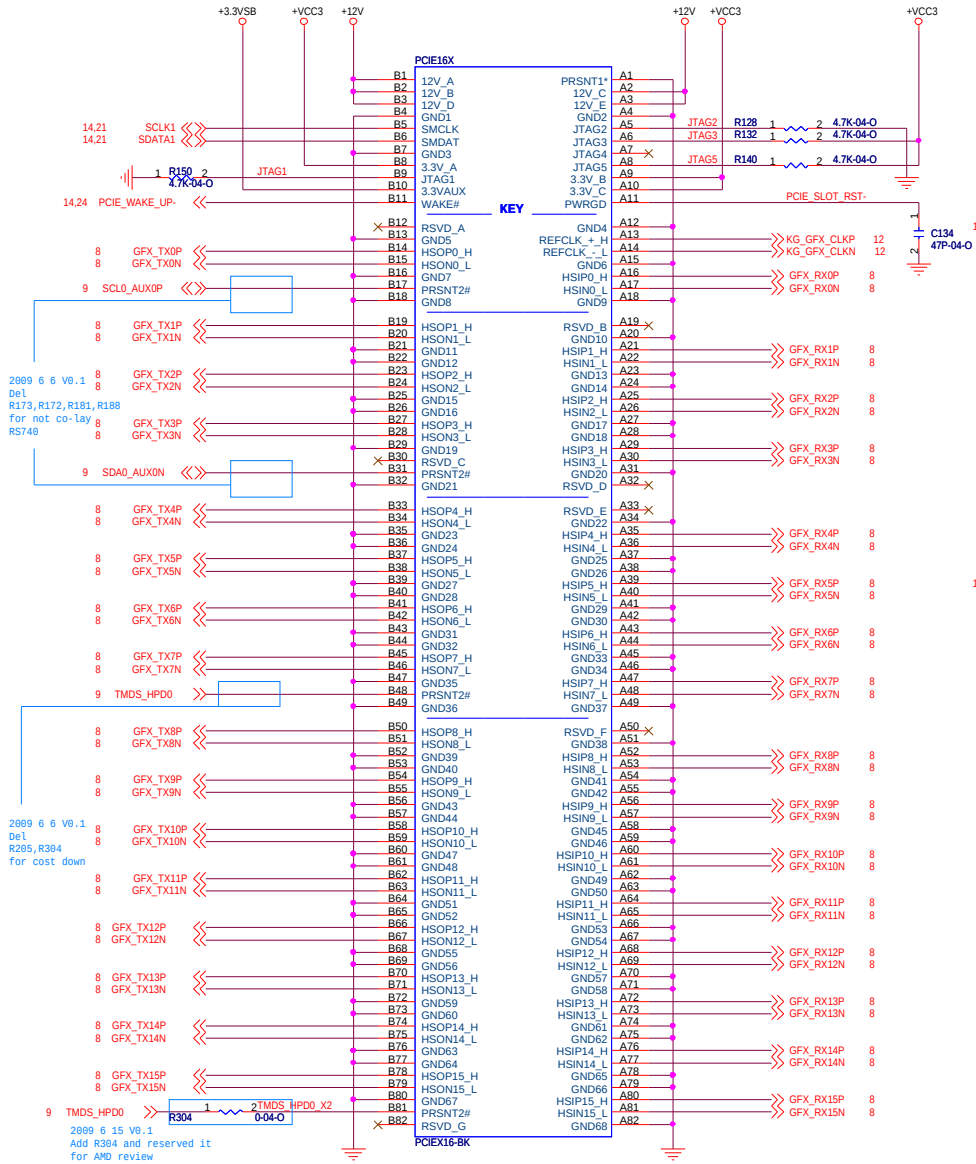
2009 11 9 V1.0 to V1.01
1.Change HDMI conn. use
have screw hole for EMI

Elitegroup Computer Systems

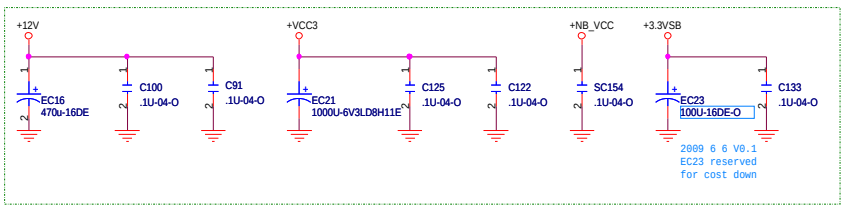
Title: VGA / HDMI

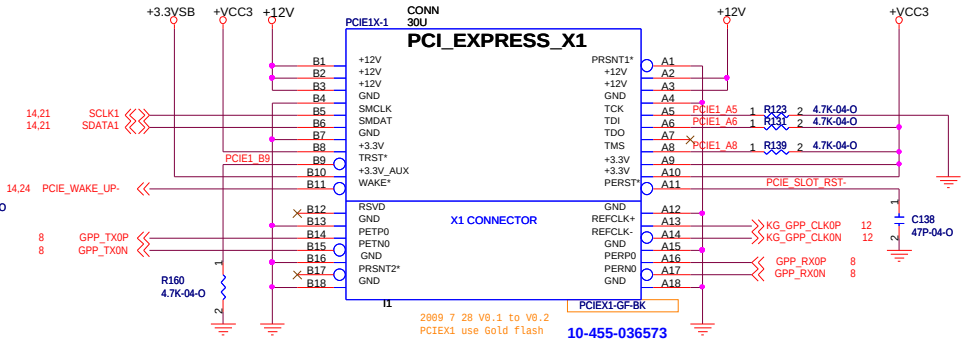
Size: Custom | Document Number: RS780Q-LM3 | Rev: 1.01

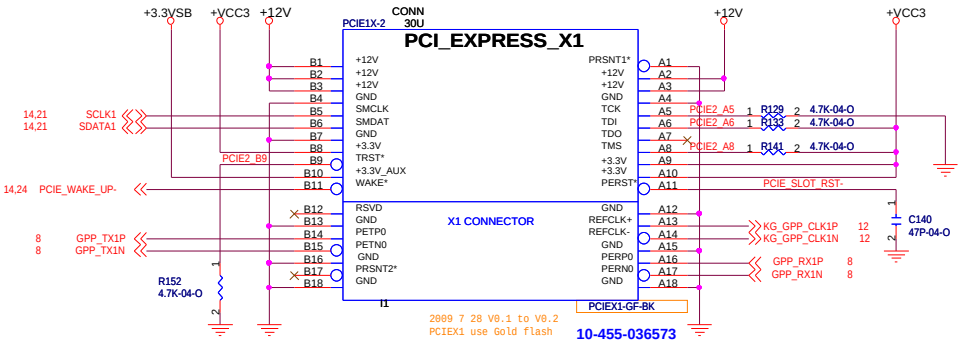
Date: Friday, November 13, 2009 | Sheet 18 of 36



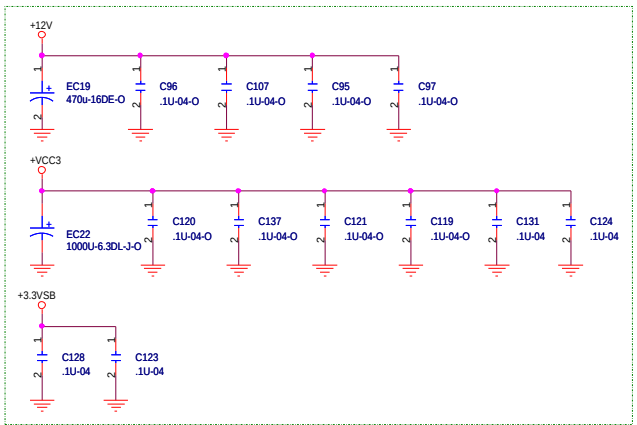
Please place the caps close to PCIEX16 Slot.

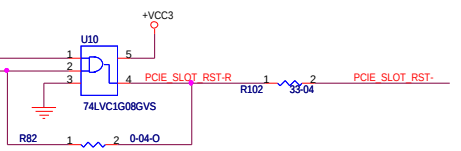






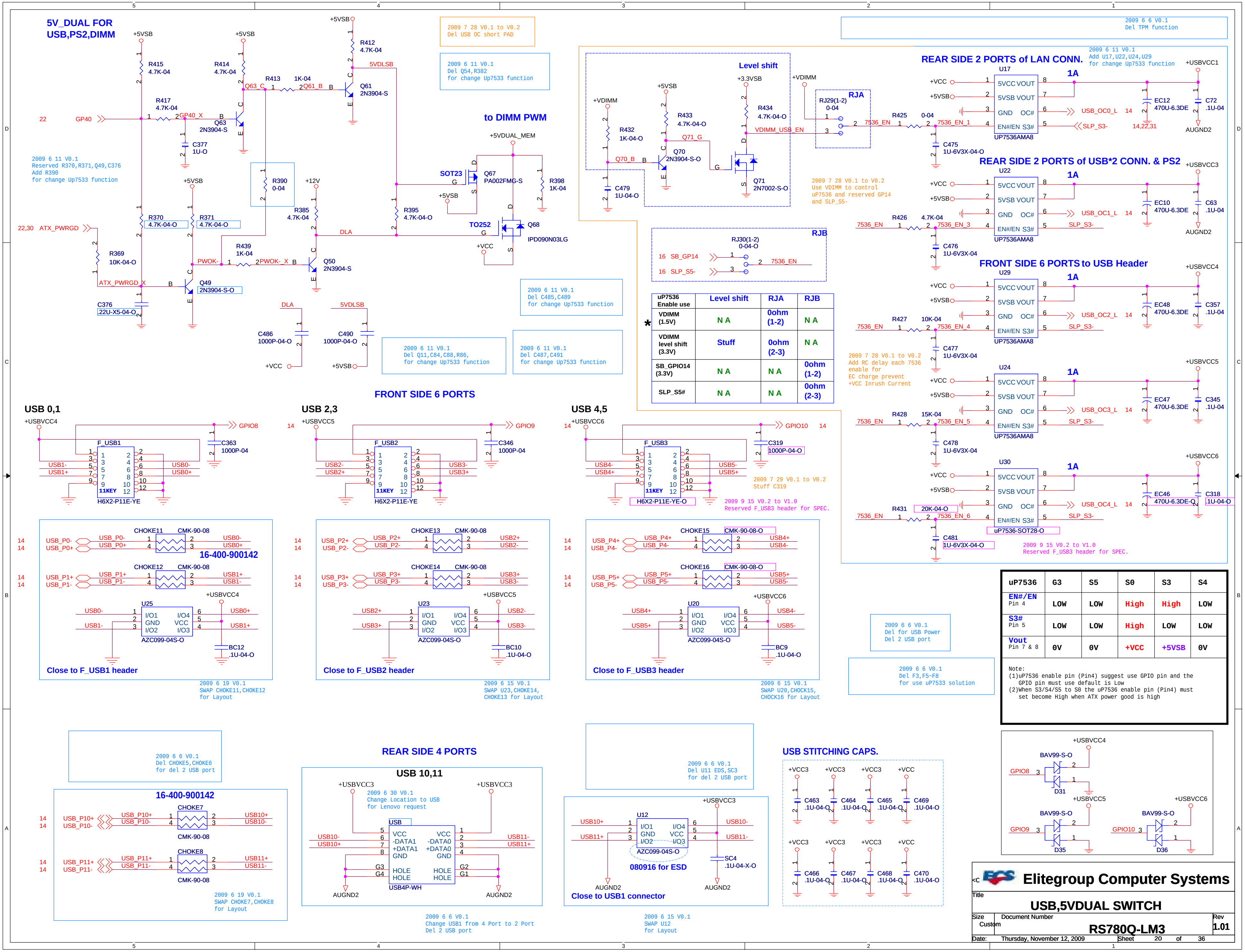
Please place the caps close to PCIE1,PCIE2 Slot.





Elitegroup Computer Systems

Title	PCIE/16X/1X	
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
Date: Friday, November 13, 2009	Sheet 19 of 36	



uP7536 Enable use	Level shift	RJA	RJB
VDIMM (1.5V)	N A	0ohm (1-2)	N A
VDIMM level shift (3.3V)	Stuff	0ohm (2-3)	N A
SB_GPIO14 (3.3V)	N A	N A	0ohm (1-2)
SLP_S5#	N A	N A	0ohm (2-3)

uP7536	G3	S5	S0	S3	S4
EN#/EN Pin 4	LOW	LOW	High	High	LOW
S3# Pin 5	LOW	LOW	High	LOW	LOW
Vout Pin 7 & 8	0V	0V	+VCC	+5VSB	0V

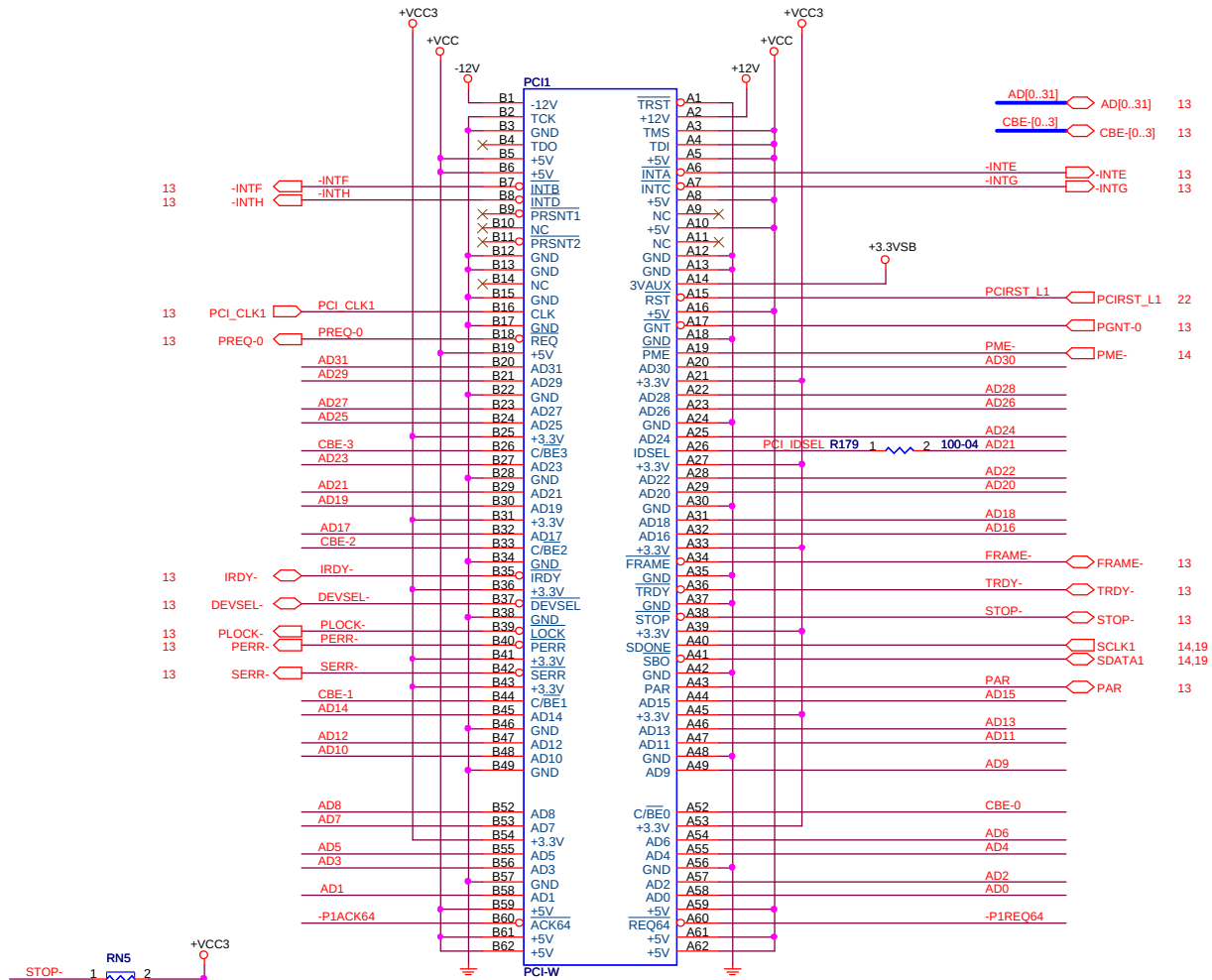
Note:
(1)uP7536 enable pin (Pin4) suggest use GPIO pin and the GPIO pin must use default is Low
(2)When S3/S4/S5 to S0 the uP7536 enable pin (Pin4) must set become High when ATX power good is high

Elitegroup Computer Systems

Title: USB,5VDUAL SWITCH

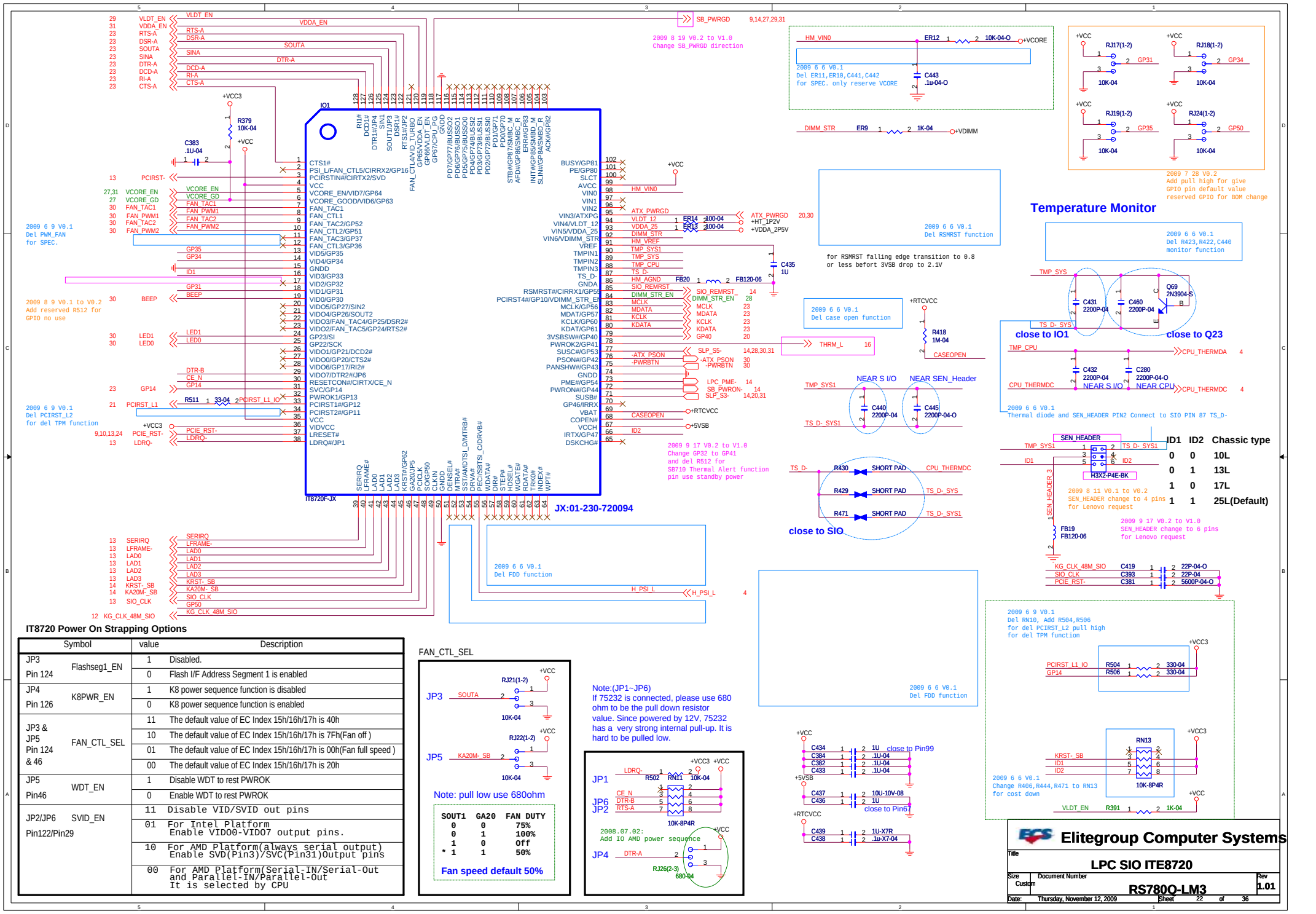
Size	Document Number	Rev
Custom	RS780Q-LM3	1.01

Date: Thursday, November 12, 2009 Sheet 20 of 36



Elitegroup Computer Systems

Title	PCI SLOT	
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
Date: Thursday, November 12, 2009	Sheet 21 of 36	

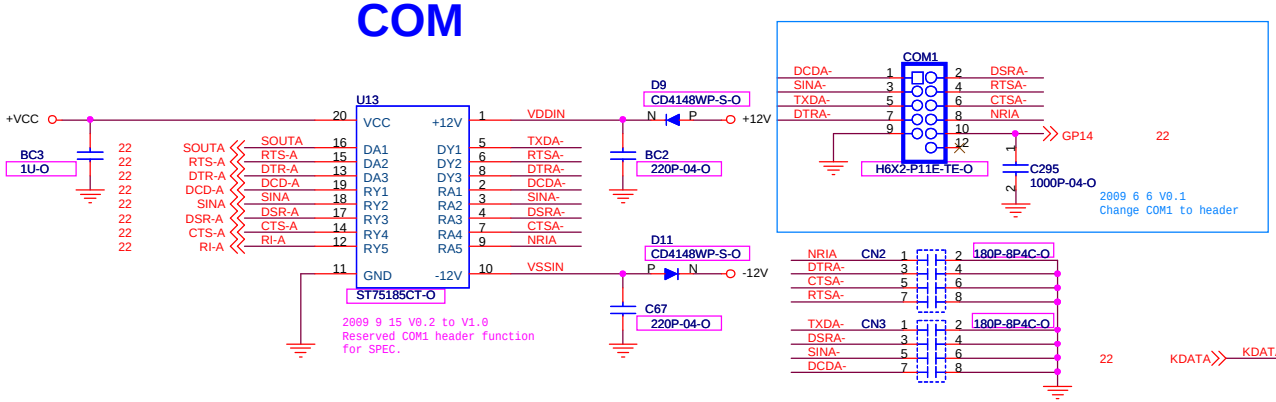


IT8720 Power On Strapping Options

Symbol		value	Description
JP3 Pin 124	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 40h
		10	The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 20h
JP5 Pin46	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP2/JP6 Pin122/Pin29	SVID_EN	11	Disable VID/SVID out pins
		01	For Intel Platform Enable VID00-VID07 output pins.
		10	For AMD Platform(always serial output) Enable SVD(Pin3)/SVC(Pin31)Output pins
		00	For AMD Platform(Serial-IN/Serial-Out and Parallel-IN/Parallel-Out It is selected by CPU

FAN_CTL_SEL

COM



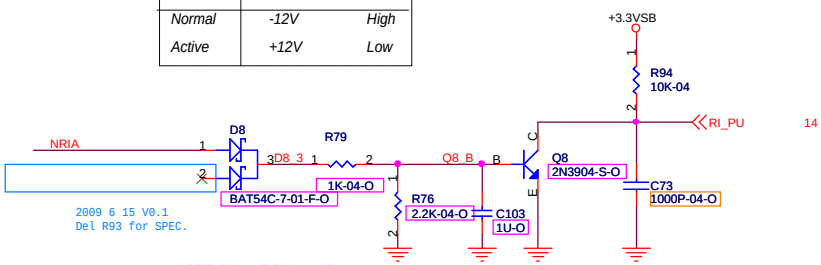
2009 9 15 V0.2 to V1.0
Reserved COM1 header function
for SPEC.

2009 6 6 V0.1
Change COM1 to header

2009 6 15 V0.1
Del U18,C300,C299,BC5,COM2 for SPEC.

2009 6 15 V0.1
Del CN4,CN5 for SPEC.

	NRIA	RI#
Normal	-12V	High
Active	+12V	Low



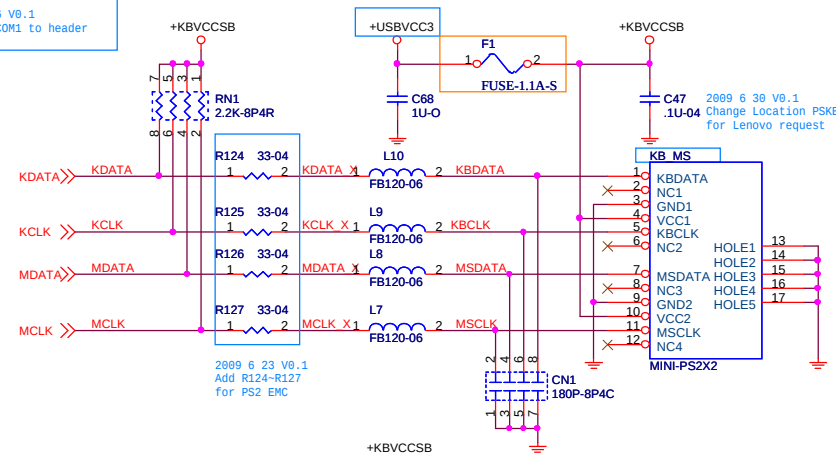
2009 6 15 V0.1
Del R93 for SPEC.

2009 9 15 V0.2 to V1.0
Reserved COM1 header function
for SPEC.

2009 7 28 V0.1 to V0.2
C73 reserved and use C103
for S5 auto wake up

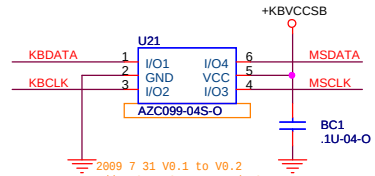
PS2

2009 6 6 V0.1
Change KBVCCSB source to +USBVCC3
for 5VDUAL change to use uP7533



2009 6 30 V0.1
Change Location PSKBM1 to KB_MS
for Lenovo request

2009 6 23 V0.1
Add R124~R127
for PS2 EMC



2009 7 31 V0.1 to V0.2
Add R124~R127 reserved U21
for PS2 EMC

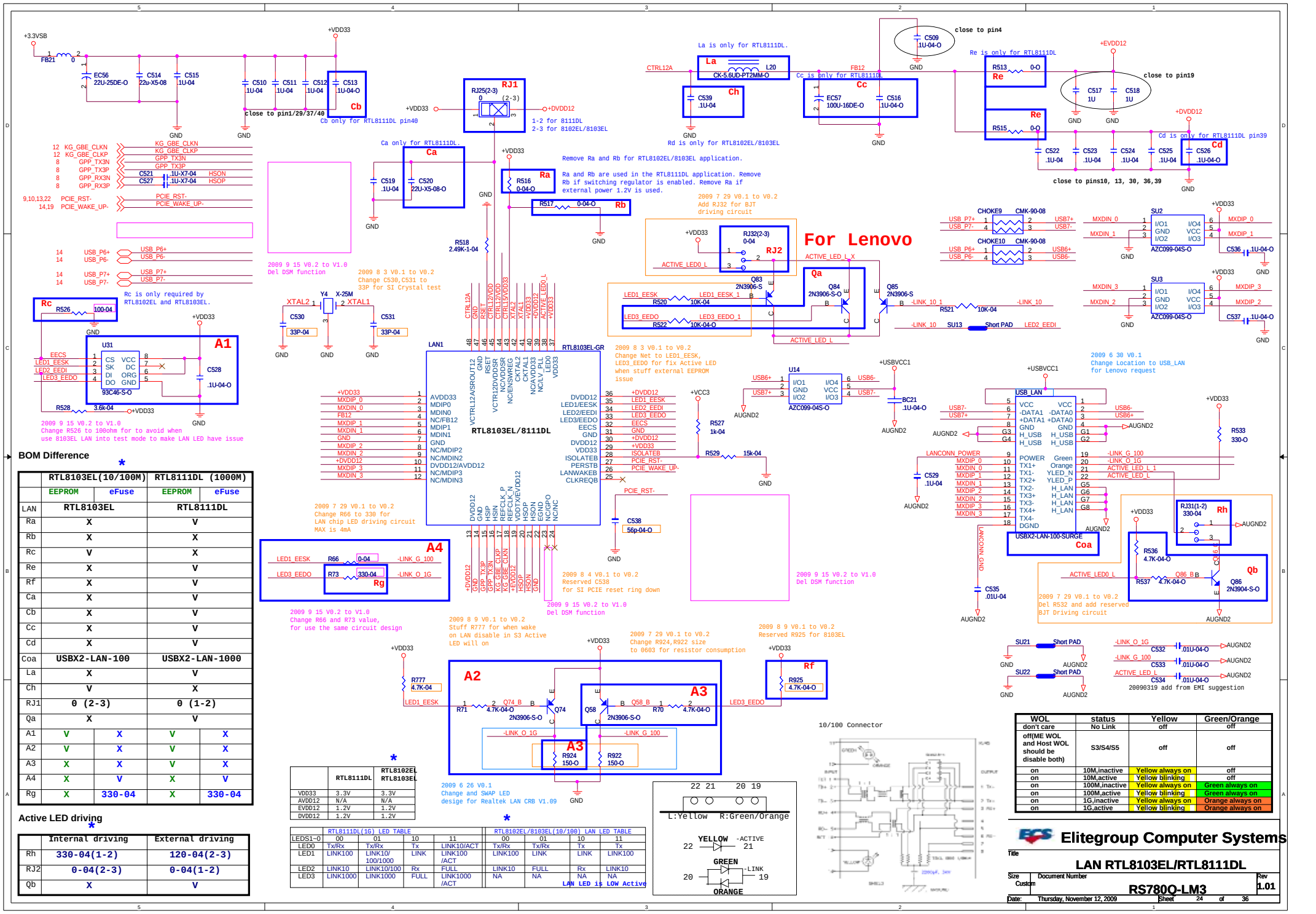
Close to PSKBM1 connector

Elitegroup Computer Systems

Title: PS2 / COM PORT

Size: Custom | Document Number: RS780Q-LM3 | Rev: 1.01

Date: Thursday, November 12, 2009 | Sheet 23 of 36



BOM Difference

*

	RTL8103EL(10/100M)		RTL8111DL (1000M)	
	EEPROM	eFuse	EEPROM	eFuse
LAN	RTL8103EL		RTL8111DL	
Ra	X		V	
Rb	X		X	
Rc	V		X	
Re	X		V	
Rf	X		V	
Ca	X		V	
Cb	X		V	
Cc	X		V	
Cd	X		V	
Coa	USBX2-LAN-100		USBX2-LAN-1000	
La	X		V	
Ch	V		X	
RJ1	0 (2-3)		0 (1-2)	
Qa	X		V	
A1	V	X	V	X
A2	V	X	V	X
A3	X	X	V	X
A4	X	V	X	V
Rg	X	330-04	X	330-04

Active LED driving

*

	Internal driving	External driving
Rh	330-04(1-2)	120-04(2-3)
RJ2	0-04(2-3)	0-04(1-2)
Qb	X	V

*

	RTL8111DL	RTL8102EL RTL8103EL
VDD33	3.3V	3.3V
AVDD12	N/A	N/A
EVDD12	1.2V	1.2V
DVDD12	1.2V	1.2V

*

RTL8111DL(1G) LED TABLE					RTL8102EL/8103EL(10/100) LAN LED TABLE			
LEDS1~0	00	01	10	11	00	01	10	11
LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ACT	Tx/Rx	Tx/Rx	Tx	Tx
LED1	LINK100	LINK10/ 100/1000	LINK	LINK100 /ACT	LINK100	LINK	LINK	LINK100
LED2	LINK10	LINK10/100	Rx	FULL	LINK10	FULL	Rx	LINK10
LED3	LINK1000	LINK1000	FULL	LINK1000 /ACT	NA	NA	NA	NA

LAN LED is LOW Active

WOL	status	Yellow	Green/Orange
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive	Yellow always on	off
on	10M,active	Yellow blinking	off
on	100M,inactive	Yellow always on	Green always on
on	100M,active	Yellow blinking	Green always on
on	1G,inactive	Yellow always on	Orange always on
on	1G,active	Yellow blinking	Orange always on

Elitegroup Computer Systems

Title: LAN RTL8103EL/RTL8111DL

Size: Custom | Document Number: RS780Q-LM3 | Rev: 1.01

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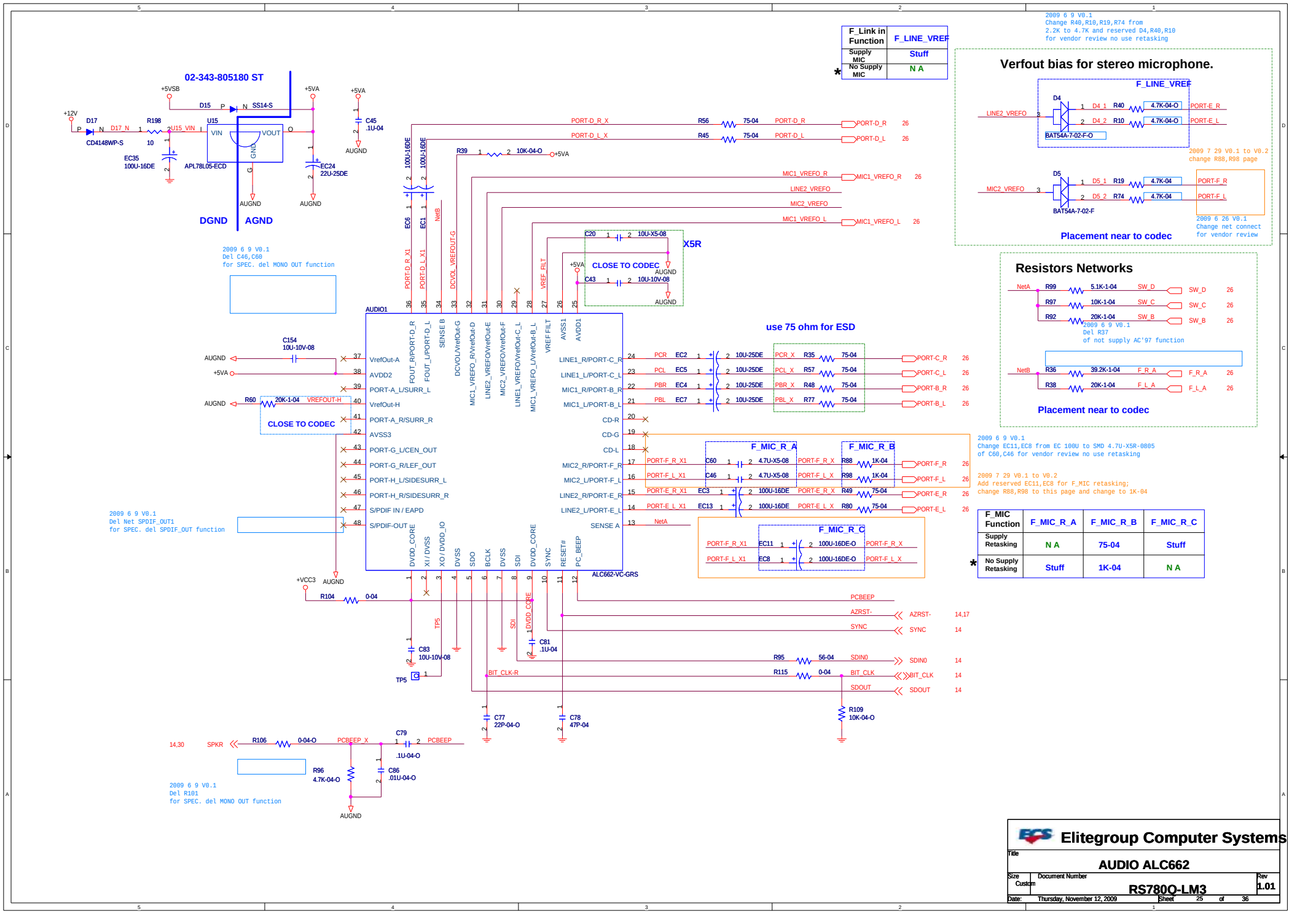
02-343-805180 ST
DGND
AGND
AUDIO1
ALC662-VC-GRS
F_Link in Function
F_LINE_VREF
Supply MIC
Stuff
No Supply MIC
N A
Verfout bias for stereo microphone.
F_LINE_VREF
Placement near to codec
Resistors Networks
Placement near to codec
use 75 ohm for ESD
CLOSE TO CODEC
X5R
F_MIC_R_A
F_MIC_R_B
F_MIC_R_C
F_MIC Function
F_MIC_R_A
F_MIC_R_B
F_MIC_R_C
Supply Retasking
No Supply Retasking
N A
75-04
Stuff
1K-04
Elitegroup Computer Systems
AUDIO ALC662
RS780Q-LM3
1.01
Thursday, November 12, 2009
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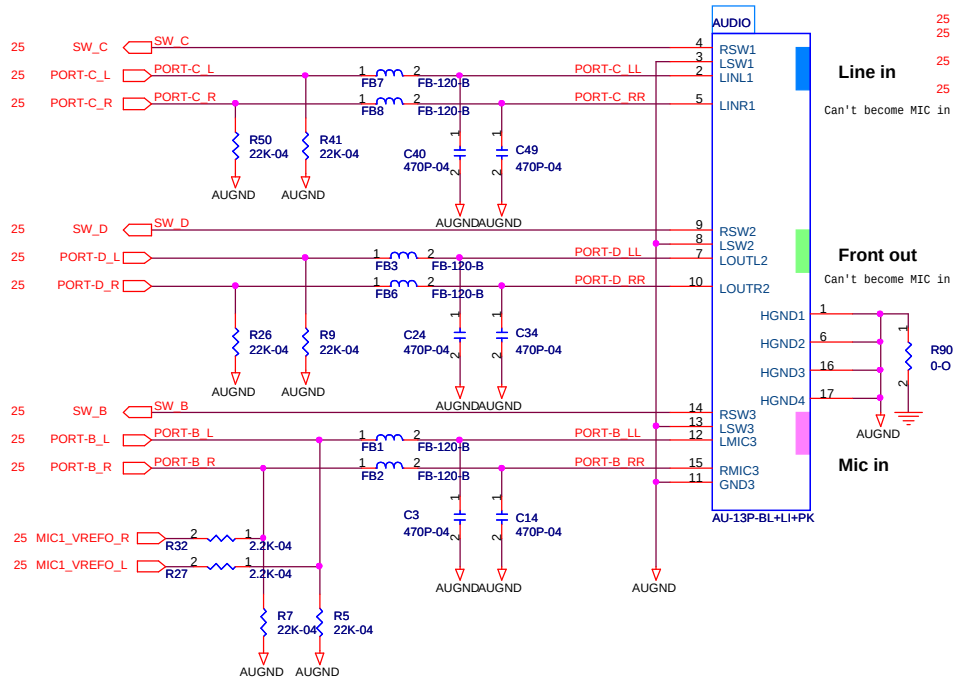
2009 6 30 V0.1
Change Location to AUDIO
for Lenovo request

2009 6 26 V0.1
Change net connect
for vendor review

2009 7 29 V0.1 to V0.2
Del net and change R88,R98
to previous page

about BAT54A concern



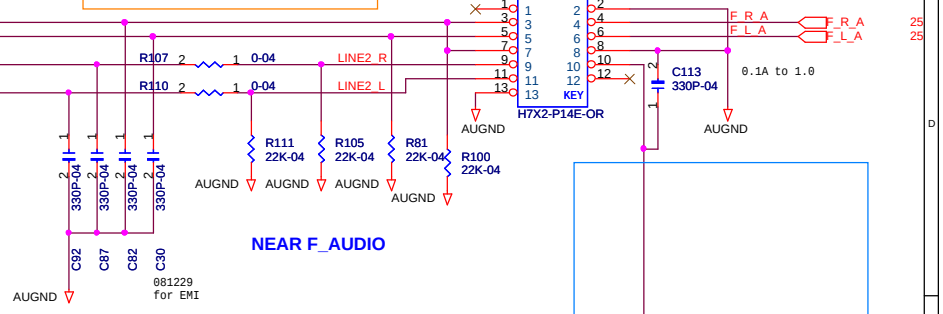
Line in

Can't become MIC in

Front out

Can't become MIC in

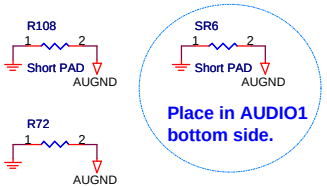
Mic in



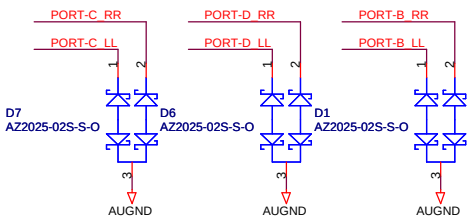
NEAR F_AUDIO

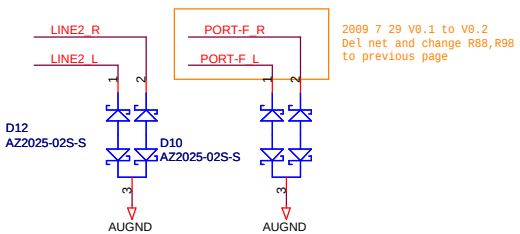
2009 6 9 V0.1
Del Q1,R114,C104,R113
of not supply AC'97 function

080911 Realtek recommend



08'1229
change footprint for CODEC





2009 7 29 V0.1 to V0.2
Del net and change R88,R98
to previous page

2009 6 9 V0.1
Del R3,R2,C2,C1,R1,R6,C19,U1,
R4,D3,MONO_OUT,D2,C22
for SPEC. del MONO OUT function

Elitegroup Computer Systems

Title	AUDIO ALC662	
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
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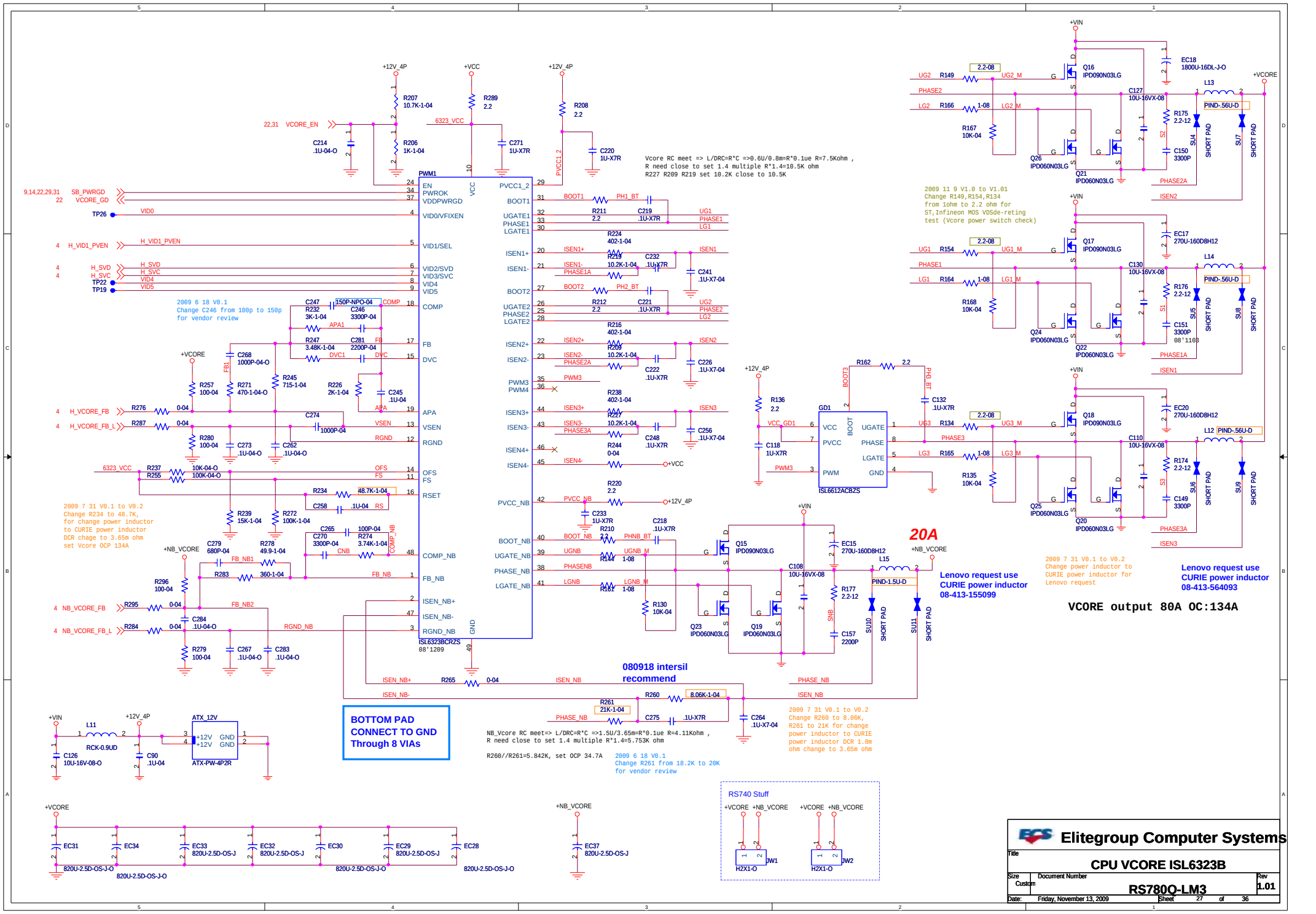
PWM1
ISL6323BCRZS
08'1209
ISL6612ACBZS
GD1
Q15 IPD090N03LG
Q19 IPD060N03LG
Q23 IPD060N03LG
Q16 IPD090N03LG
Q26 IPD060N03LG
Q21 IPD060N03LG
Q17 IPD090N03LG
Q24 IPD060N03LG
Q22 IPD060N03LG
Q18 IPD090N03LG
Q25 IPD060N03LG
Q20 IPD060N03LG
20A
Lenovo request use CURIE power inductor 08-413-155099
Lenovo request use CURIE power inductor 08-413-564093
VCORE output 80A OC:134A
080918 intersil recommend
BOTTOM PAD CONNECT TO GND Through 8 VIAs
RS740 Stuff
2009 6 18 V0.1 Change C246 from 100p to 150p for vendor review
2009 7 31 V0.1 to V0.2 Change R234 to 48.7K, for change power inductor to CURIE power inductor DCR chage to 3.65m ohm set Vcore OCP 134A
2009 11 9 V1.0 to V1.01 Change R149,R154,R134 from 1ohm to 2.2 ohm for ST,Infineon MOS VDSde-reting test (Vcore power switch check)
2009 7 31 V0.1 to V0.2 Change power inductor to CURIE power inductor for Lenovo request
2009 7 31 V0.1 to V0.2 Change R260 to 8.06K, R261 to 21K for change power inductor to CURIE power inductor DCR 1.8m ohm change to 3.65m ohm
2009 6 18 V0.1 Change R261 from 18.2K to 20K for vendor review
Vcore RC meet => L/DRC=R*C =>0.6U/0.8m=R*0.1ue R=7.5Kohm , R need close to set 1.4 multiple R*1.4=10.5K ohm R227 R209 R219 set 10.2K close to 10.5K
NB_Vcore RC meet=> L/DRC=R*C =>1.5U/3.65m=R*0.1ue R=4.11Kohm , R need close to set 1.4 multiple R*1.4=5.753K ohm
R260//R261=5.842K, set OCP 34.7A
Elitegroup Computer Systems
CPU VCORE ISL6323B
RS780Q-LM3
1.01
Friday, November 13, 2009
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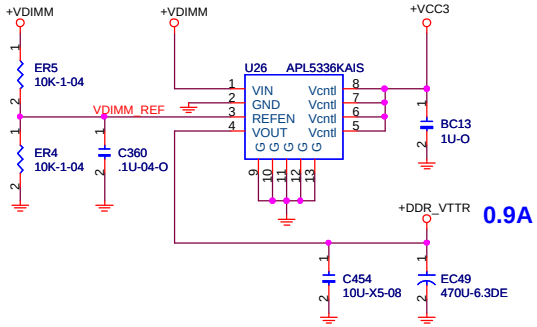
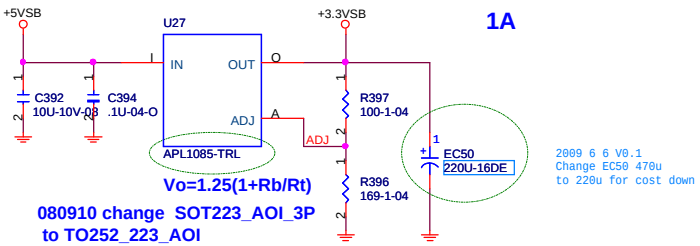
DDR_VTTR

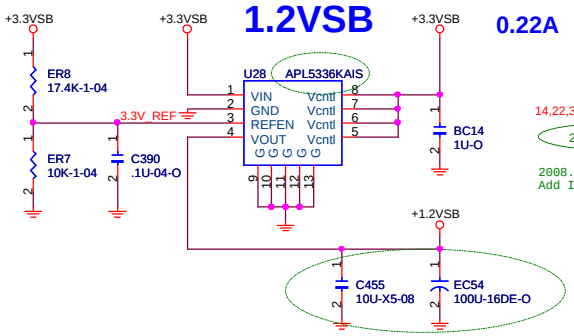


080828 UPI recommend.

3VSB

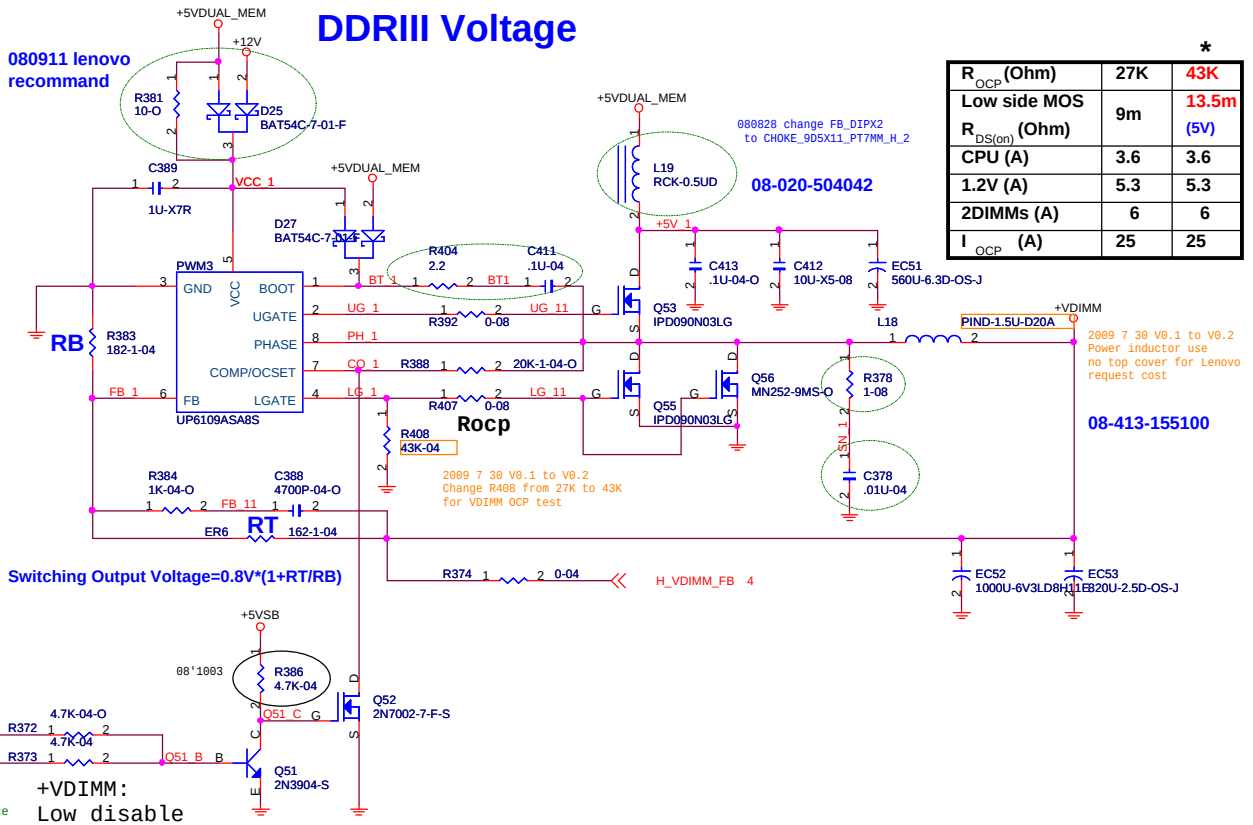


1.2VSB



080828 UPI recommend.

DDRIII Voltage



*		
R_{OCP} (Ohm)	27K	43K
Low side MOS $R_{DS(on)}$ (Ohm)	9m	13.5m (5V)
CPU (A)	3.6	3.6
1.2V (A)	5.3	5.3
2DIMMs (A)	6	6
I_{OCP} (A)	25	25

Elitegroup Computer Systems

Title: DC POWER, DDRIII POWER

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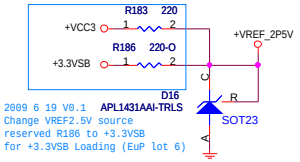
VREF 2.5V



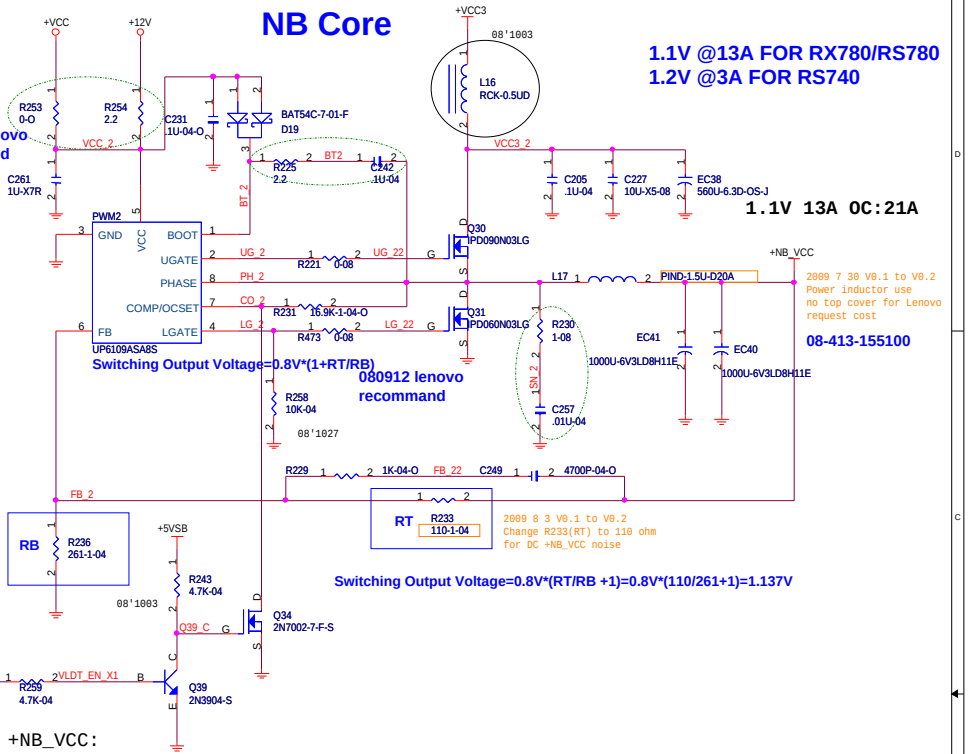
2009 6 19 V0.1
Change VREF2.5V source
reserved R186 to +3.3VSB
for +3.3VSB Loading (EuP lot 6)

NB Core

1.1V @13A FOR RX780/RS780
1.2V @3A FOR RS740

1.1V 13A OC:21A

080909 lenovo recommand



Switching Output Voltage=0.8V*(1+RT/RB)

080912 lenovo recommand

2009 7 30 V0.1 to V0.2
Power inductor use
no top cover for Lenovo
request cost

08-413-155100

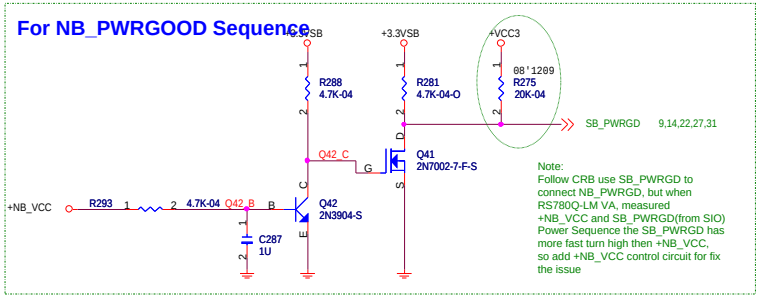
2009 8 3 V0.1 to V0.2
Change R233(RT) to 110 ohm
for DC +NB_VCC noise

Switching Output Voltage=0.8V*(RT/RB +1)=0.8V*(110/261+1)=1.137V

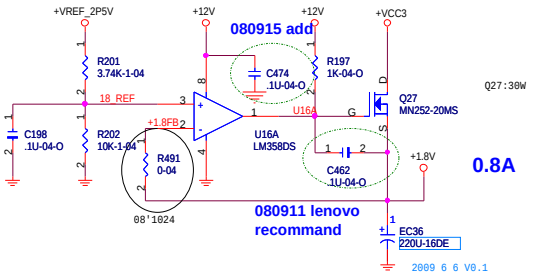
2008.07.02:
Add IO AMD power sequence

+NB_VCC:
Low disable
High enable

For NB_PWRGOOD Sequence



Note:
Follow CRB use SB_PWRGD to connect NB_PWRGD, but when RS780Q-LM VA, measured +NB_VCC and SB_PWRGD(from SIO) Power Sequence the SB_PWRGD has more fast turn high then +NB_VCC, so add +NB_VCC control circuit for fix the issue

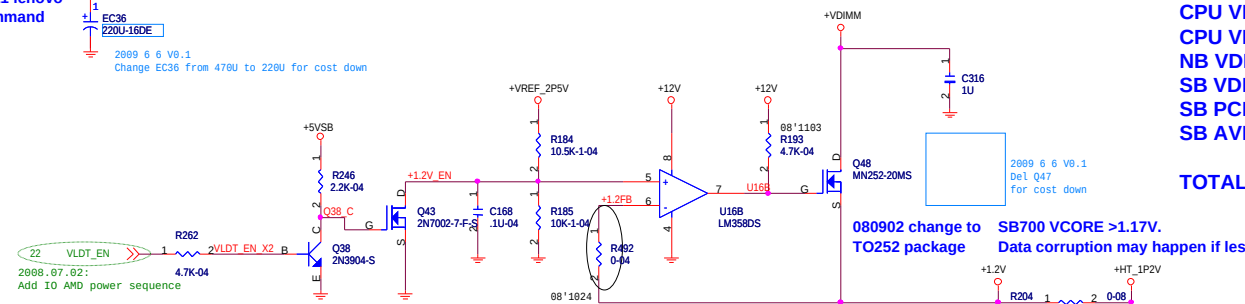


2009 6 6 V0.1
Change EC36 from 470U to 220U for cost down

RS780 USE

CPU VLDT:1.4A
CPU VDDR:1.75A
NB VDDHTTX:0.25A
SB VDD:0.6A
SB PCIE VDDR:0.8A
SB AVDD SATA:0.5A

TOTAL:5.3A Q47,Q48:30W



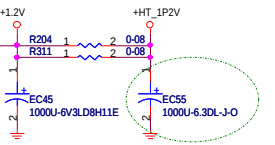
2009 6 6 V0.1
Del Q47
for cost down

080902 change to TO252 package

SB700 VCORE >1.17V.
Data corruption may happen if less than 1.17V

+1.2V:
Low disable
High enable

2009 6 6 V0.1
Del RN4,R203
for not Co-lay RS740



080909 add

Elitegroup Computer Systems

Title	NB CORE POWER	
Size: Custom	Document Number: RS780Q-LM3	Rev: 1.01
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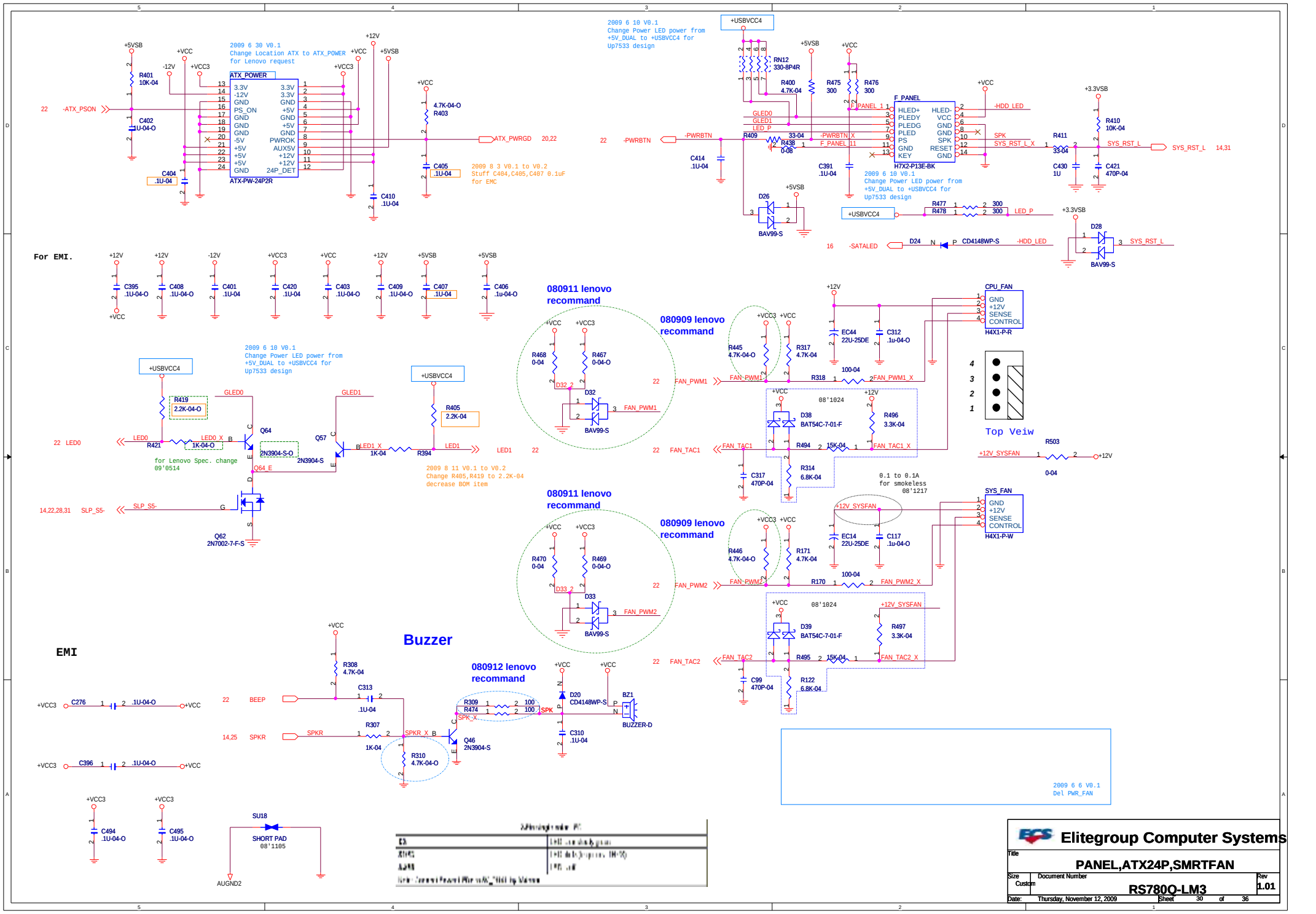

Elitegroup Computer Systems

Title: **PANEL,ATX24P,SMRTFAN**

Size	Document Number	Rev
Custom	RS780Q-LM3	1.01

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POWER GOOD & ENABLES

ATHLON64 POWER GOOD & ENABLES CIRCUIT

2009 6 6 V0.1
Del reserved
AMD Power sequence
function

2009 6 6 V0.1
Move DIMM_STR_EN Pull high +5VSB R393 to Page 28
for Del reserved
AMD Power sequence
function

2009 7 29 V0.1 to V0.2
D29,D30 stuff for reset issue

14,30 SYS_RST_L — D29 BAT54C-7-01-F

SS0520 >>>> 03-021-252040

14,20,22 SLP_S3- — D30 BAT54C-7-01-F

080909 lenovo recommand

2009 6 6 V0.1
D30,D31 reserved for
AMD Power sequence
function(Use SIO8720 sequence)

2009 8 19 V0.2 to V1.0
Change SB_PWRGD direction

SB_PWRGD 9,14,22,27,29

POWER GOOD CIRCUIT

+VCC3 — R420 10K-04-O

2008.07.02:
Add IO AMD power sequence

VCORE_EN 22,27

+VCC — R483 4.7K-04
+5VSB — R482 4.7K-04
VDDA_EN_H 4
Q73_G — Q73 2N7002-7-F-S
22 VDDA_EN — R484 1K-04 — Q72_B — Q72 2N3904-S
C187 .1U-04-O

Lenovo request
0.1A to 1.0

2009 6 6 V0.1
Del H7,H8 for PCB SIZE change to 244*224mm

H1 H2 H3 H4 H5 H6 TH

AUGND AUGND

+USBVCC5 — RN23 330-8P4R — Q79_C — Q79 PMBT2222A-S — R406 1K-04 — Q79_B — R375 1K-04 — Q76_B — Q76 PMBT2222A-S — RN20 330-8P4R — +USBVCC1

+USBVCC6 — RN24 330-8P4R — Q80_C — Q80 PMBT2222A-S — R416 1K-04 — Q80_B — R389 1K-04 — Q77_B — Q77 PMBT2222A-S — RN21 330-8P4R — +USBVCC3

2009 6 6 V0.1
Add RN22~RN24,Q78~80,R375,R389,R482,R406,
R416 for USB drain circuit

+5VSB — R490 1K-04 — Q75_C — R402 1K-04 — Q78_B — Q78 PMBT2222A-S — RN22 330-8P4R — +USBVCC4

08'1023

14,22,28,30 SLP_S5- — R499 15K-04 — SLP_S5-_X — Q75 PMBT2222A-S — C492 .1u-04-O

+5VSB — R501 1K — C493 .1u-04-O 08'1105

2009 6 6 V0.1
Del minimum load function

Elitegroup Computer Systems

Title: POWER ENABLE

Size	Document Number	Rev
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SB710

Name	Type	Voltage	Default	Functional Description	Function
GPIO4	I/O	3.3V	Input	Smartvolt Select 1/Serial ATA Interlock 2/GPIO 4	H_PRESENT_L
IMC_GPIO8	I/O	3.3V_S5	Input	IMC_GPIO8	F_USB1 detect
IMC_GPIO9	I/O	3.3V_S5	Input	IMC_GPIO9	F_USB2 detect
IMC_GPIO10	I/O	3.3V_S5	Input	IMC_GPIO10	F_USB3 detect
IMC_GPIO11	I/O	3.3V_S5	Input	IMC_GPIO11	LC CLR_CMOS
IMC_GPIO13	I/O	3.3V_S5	Input	Low Voltage SMBus Clock 3/IMC_GPIO13	SMCLK3
IMC_GPIO14	I/O	3.3V_S5	Input	Low Voltage SMBus Data 3/IMC_GPIO14	SMDATA3
GPIO5	I/O	3.3V	Input	SMARTVOLT2/SHUTDOWN#/GPIO5	F_AUDIO detect
GPIO9	I/O	3.3V	Input	DDC1_SCL/GPIO9	N/A
GPIO8	I/O	3.3V	Input	DDC1_SDA/GPIO8	N/A
GPIO66	I/O	3.3V_S5	Input	Low-Low Battery/GPIO 66	LPCPD_N
GPIO14	I/O	3.3V_S5	Output	Use to control USB dual power	GPO14

ITE8720

Name	Type	Voltage	Functional Description	Function
GP14	I/O	5V	Serial VID clock/PECI request/GPIO14	COM1 detect
GP22	I/O	5V_S5	Serial flash clock/GPIO22	Power LED
GP23	I/O	5V_S5	Serial flash in data/GPIO23	SUS LED
GP30	I/O	5V	Voltage ID0/GPIO30	BEEP
GP31	I/O	5V	Voltage ID1/GPIO31	BIOS reserve
GP34	I/O	5V	Voltage ID4/GPIO34	BIOS reserve
GP35	I/O	5V	Voltage ID5/GPIO35	BIOS reserve
GP40	I/O	5V_S5	3VSBSW/GP40	Dual switch
GP33	I/O	5V	VID3/GP33	Sensor header ID1
GP47	I/O	5V	IR output/GP47	Sensor header ID2
GP50	I/O	5V	Serial flash data output/GPIO50	BIOS reserve

For 104

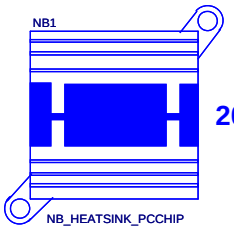
BT1

CR2032

CLRCMOS-SW(1-2)

JP-R

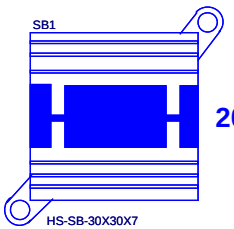
NB1



20-120-014500

NB_HEATSINK_PCCHIP

SB1



20-120-010773

HS-SB-30X30X7

Elitegroup Computer Systems

Title: Attention

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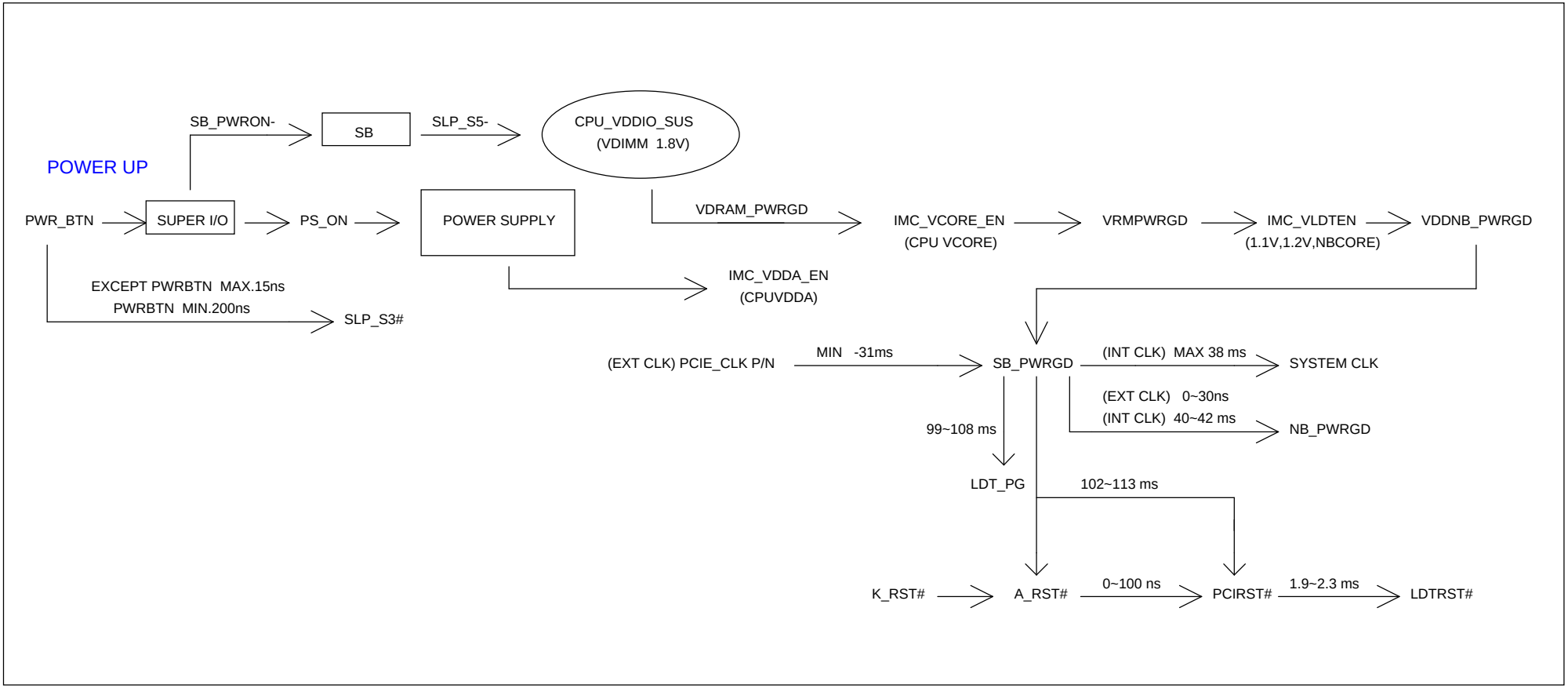

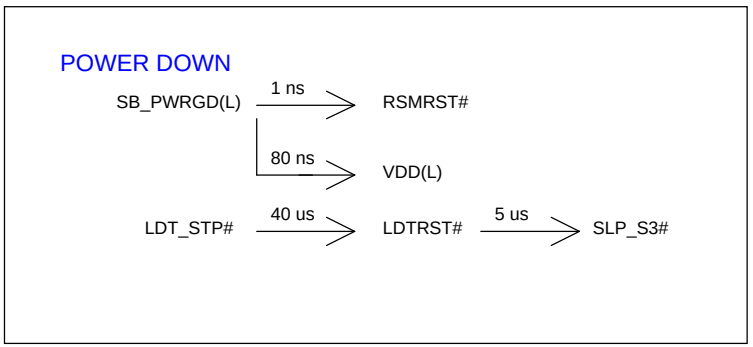

Elitegroup Computer Systems

Title: Power Sequence

Size: Custom | Document Number: RS780Q-LM3 | Rev: 1.01

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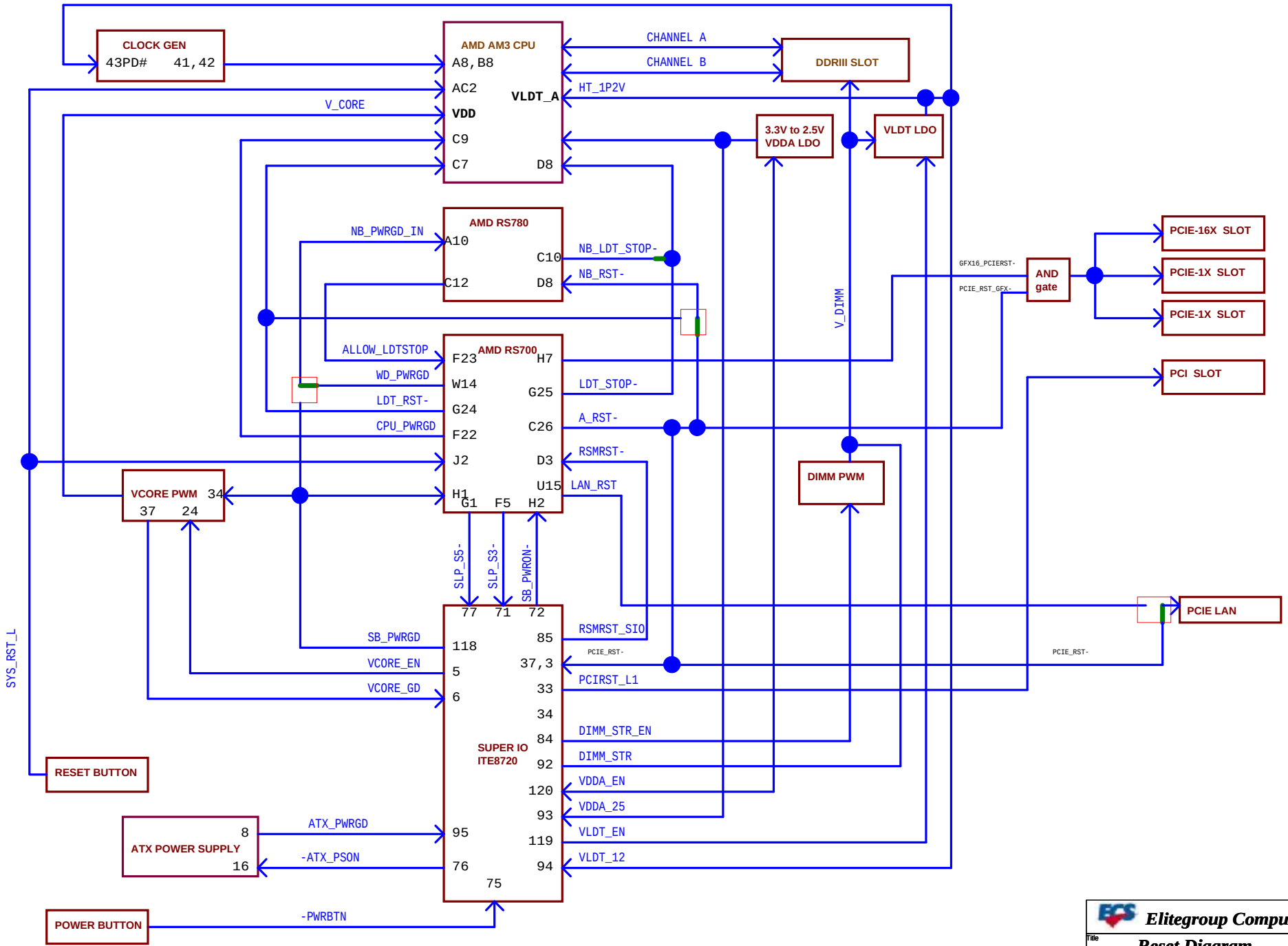
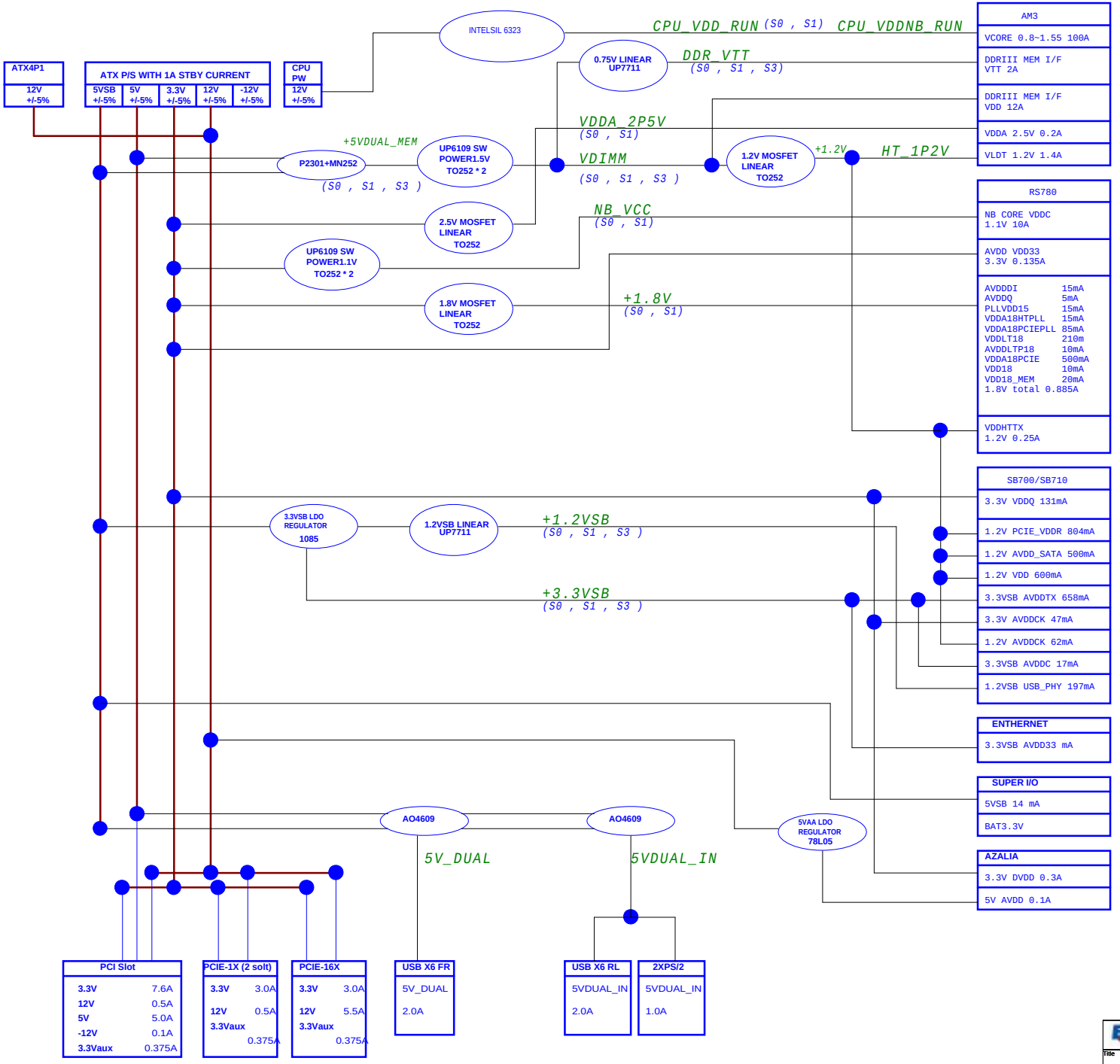


Elitegroup Computer Systems

Title: Reset Diagram

Size | Document Number: RS780Q-LM3 | Rev: 1.01

Date: Thursday, November 12, 2009 | Sheet 34 of 36



Elitegroup Computer Systems

Title: Power Distribution

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REVISION HISTORY:

Rev	Date	Notes
0.1	09'0606	**Change from RS780Q-LM2 V1.0 modify reserve function to meet RS780Q-LM3 V0.1 Spec.**
		Page 3 1.Change DIMMA1,B1 net to test port for SPEC. change
		Page 4 1.Del FB17,R282,R248,R292 for cost down 2.Del Q36,R263,R240,R269,R251,R248 for The Side Band Interface bus is not used 3.Change R264 from 300 to 1K for The Side Band Interface bus is not used 4.Del Q35,R26,R286,Q37,R266,C252,R250,R249,C260,Q33,R223,C255,R222,Q32,C254 reserved level shift function 5.C65,RN8 reserced for cost down
		Page 5 1.C444,SC58 reserced for cost down 2.Add C507,C508 and reserved for AMD checklist 3.C456 stuff for AMD suggest
		Page 6 1.C370,C371,C380 reserved for SI 2.C499,C500 stuff for AMD NB Schematic Checklist
		Page 7 1.Del 2 DIMM slot for SPEC. and shift page 2.Del R153,R142,SR32,SR33 for not Co-lay RS740
		Page 9 1.Del FB15,C115,Q12,R138,R147,R156,R155,R146,R137,R145,R169,R126,R125,R124,SFB7,R121 R118 ; Change RJ3,RJ4 to R120,R142 for not Co-lay RS740 2.Del SR1; Reserve R127,U17,SC13,SC6; Stuff R119,R466 for cost down 3.Change SC7,SC8 from 10uF to 2.2uF for AMD Schematic Review Checklist 4.Del R119,U17,C461,R127,R466,for AMD confirm NB_PWRGD_IN can cost down 5.Del PinA19~B17 Net for DVI Single-Link (RS760 only support Single-Link)
		Page 10 1.Del RJ2,RJ7,RJ1,RJ6,SR2,SR5,R143; Add R145,R146 for not Co-lay RS740
		Page 11 1.Del R195,RJ9 for not Co-lay RS740 2.Del SR12,FB22,SFB5,SR11,R159,SR19; Reserve SC31for cost down 3.Change SC29,SC32 from 22u to 10u for AMD NB Schematic Checklist
		Page 12 1.Del RJ8; Add R195 for not co-lay RS740 2.Del Q28,Q29,R187,R192,,R186,R191,R447~R464; Reserve C193,C186 for cost down
		Page 13 1.Del R424,R443,R485,R506,R50,R508,R437,R509 for cost down 2.Del Net INTRUDER_L for del case open function
		Page 14 1.Del Net SCLK3,SDATA3 The Side Band Interface bus is not used and del ohm for cost down 2.Del Net USB_P8,USB_P9,5VDUAL_IN_OC2 for del 2 USB port 3.Del Net GPIO24,GPIO25, LPCPD_N for del TPM function 4.Del R367,R319 for not co-lay RS740
		Page 15 1.Del SC122,SC118,SC123,SC117 for AMD confirm can cost down for no use IDE
		Page 16 1.Del eSATA function 2.Del Net C476,C477 for del eSATA port 3.Del R323,R327 for cost down
		Page 17 1.Del RJ14,RJ15 for cost down
		Page 18 1.Del Q7,R71,Q6,R70 for not co-lay RS740 2.Del CHOCKE17,CHOCKE18,CHOCKE23,U5,SC140,SC141,U9 for DVI Single-Link (RS760 only support Single-Link) 3.Del Q2,R46,R55,Q3,R59,R47 for not co-lay RS740
		Page 19 1.Del R173,R172,R181,R188 for not co-lay RS740 2.Del R205,R304; reserved EC23 for cost down
		Page 20 1.Del F4,SU14,EC9,C75,CHOCKE5,CHOCKE6,U11,SC3; Change USB1 from 4 Port to 2 Port 2.Del U24,R336,R338,R344,R346,R350,R353,R357,R341,R487,R486,R337,R349,R352,R325,R358, BC11,EEP3,R332,C334,C329,C341,C344,C343,C348 for SPEC. del TPM function
		Page 21 1.Change EC25 from 1000U to 220U Change EC42 from 1000U to 22U for cost down
		Page 22 1.Del FDD for SPEC. del FDD function 2.Del R479,R510,C488,R480,Q71,Q70,R481 for del RSMRST function 3.Change R406,R444,R471 to RN13 for cost down 4.Del R423,R422,C440 monitor function 5.Del CAS-OPEN for SPE. del case open function 6.Thermal diode and SEN_HEADER PIN2 Connect to SIO PIN 87 TS_D- 7.Del ER11,ER10,C441,C442 for SPEC. only reserve VCORE
		Page 23 1.COM1 Port change to header, COM2 Port change to connector and reserved
		Page 24 1.Del R54(Rf),R66(Rb),R78(Rd),R87,Q10,C70,C62,C74,C80(Mb),EEP1,C7,C4(Eb) for not co-layout 88E8070 2.Del R28 for vendor confirm can cost down 3.Change C71 from 4.7u to 10u for vendor review suggest
		Page 25 1.Change EC11,EC8 from EC100U to SMD4.7U-08 of C44,C46; Change R40,R10,R19,R74 from 2.2K to 4.7K and reserved D4,R40,R10 for vendor review no use retasking 2.Del R37of not supply AC'97 function 3.Del Net SPDIF_OUT1 for SPEC. del SPDIF_OUT function 4.Del C46,C60,R101 for SPEC. del MONO_OUT function
		Page 26 1.Del R3,R2,C2,C1,R1,R6,C19,U1,R4,D3,MONO_OUT,D2,C22 for SPEC. del MONO OUT function 2.Del Q1,R114,C104,R113 of not supply AC'97 function 3.Del R13,C105,C89,R151,SPDIF_HEADER for SPEC. del SPDIF_OUT function
		Page 28 1.Change EC50 470u to 220u for cost down
		Page 29 1.Del RN4,R203 for not Co-lay RS740 2.Del Q47;hange EC36 from 470U to 220U for cost down 3.Change VREF2.5V source from +3.3VSB to +VCC3 for +3.3VSB Loading
		Page 30 1.Del PWR_FAN,R498,C217,EC39,R493,D40,R228,R243 for SPEC. del PWR_FAN function
		Page 31 1.D29,D30 reserved for AMD Power sequence function(Use SIO8720 sequence) 2.Del R500,Q78 for del reserved minimum load function 3.Add R375, R389 for USB drain circuit 4.Del H7,H8 for PCB SIZE change to 244*224mm
0.2	09'0730	**RS780Q-LM3 V0.2 SPEC. change, DVI change HDMI**
		Page 4 1.C65 stuff 10u-08 for VDIMM(close CPU) noise 2.Add reserved C299,C300 for SI (for CPU Reset,CPU Power good)
		Page 5 1.Floating CPU DHOLE1~DHOLE4 for PCB process 2.C370 stuff 2.2u-08 for VDIMM(close CPU) noise
		Page 6 1.Stuff C380 22u-08 for DC +MEM_VREFCA noise
0.2	09'0730	**RS780Q-LM3 V0.2 SPEC. change, DVI change HDMI**
		Page 10 1.R143 change to use 1% for decrease BOM item (default use 5%)
		Page 12 1.Change R178 to 33-04 for SI clock USB48M C-C Jitter
		Page 13 1.Change crystal holder for Lenovo request 2.Add test point STP1,STP2 for ICT test 3.R359 change to 22-04 for SI PCIE reset ring down 4.Change crystal X1 library for Lenovo request change holder 5.R313 change to use 5% for follow CRB and decrease BOM item
		Page 14 1.Change R355 to 56-04 for SI HDA_RST# (Codec SIDE) Vmax/Vmin fail
		Page 18 1.Change DVI to HDMI for Lenovo SPEC. change add reserved +VCC_VGA source for HDMI(reference CRB) 2.Add reserved C5,C6,C7 for VGA noise 3.SC142,SC143 change to top side,rename to C254,C255 4.U8 pin1,2;9,10 and 4,5;7,6 swap for HDMI Layout 5.CHOKE21,CHOKE22 swap for HDMI Layout 6.Net I2C_DATA,I2C_CLK add reserved D37,D34,C343,C344 for ESD
		Page 19 1.PCIEX1 use Gold flash for Lenovo SPEC.
		Page 20 1.Del USB OC short PAD 2.Use VDIMM to control uP7536 and reserved GP14 and SLP_S5- 3.Add RC delay each 7536 enable for EC charge prevent +VCC Inrush Current 4.Stuff C319 1000P for USB GPIO
		Page 21 1.Stuff C304 0.1uF for EMC
		Page 22 1.Add pull high for give GPIO pin default value reserved GPIO for BOM change 2.Add reserved R512 for GPIO no use 3.SEN_HEADER change to 4 pins for Lenovo request
		Page 23 1.C73 reserved and use C103 for S5 auto wake up 2.Add R124~R127 reserved U21 for PS2 EMC
		Page 24 1.Del R532 and add reserved BJT Driving circuit 2.Add RJ32 for BJT driving circuit 3.Change R924,R922 size to 0603 for resistor consumption 4.Change R66 to 330 for LAN chip LED driving circuit MAX is 4mA 5.Change Net to LED1_EESK,LED3_EEDO for fix Active LEDwhen stuff external EEPROM issue 6.Change C530,C531 to 33P for SI Crystal test 7.C538 reserved for SI PCIE reset ring down 8.Stuff R777 for when wake on LAN disable in S3 Active LED will on, reserved R925 for 8103EL
		Page 25 1.Add reserved EC11,EC8 for F_MIC retasking; change R88,R98 to this page and change to 1K-04 2.change R88,R98 page
		Page 26 1.Del net and change R88,R98 to previous page
		Page 27 1.Change power inductor(L12,L13,L14,L15) to CURIE power inductor for Lenovo request 2.Change R260 to 8.06K, R261 to 21K, R234 to 48.7Kfor change power inductor to CURIE power inductor DCR 1.8m ohm change to 3.65m ohm
		Page 28 1.Change R408 from 27K to 43K for VDIMM OCP test 2.Power inductor L18 use no top cover for Lenovo request cost
		Page 29 1.Power inductor L17 use no top cover for Lenovo request cost 2.Change R233(RT) to 110 ohm for DC +NB_VCC noise
		Page 30 1.Stuff C404,C405,C407 0.1uF for EMC 2.Change R405,R419 to 2.2K-04 decrease BOM item
		Page 31 1.D29,D30 stuff for reset issue
1.0	09'0915	**Page 4** 1.Stuff R252 300-04 for DBREQ_L should not be lower than VIH min during normal processor operation from AMD Family 10h PEDS.
		Page 9 1.Change to use SB_PWRGD(stuff R137) Reserved WD_PWRGD(reserve R119) , for AMD CRB and use SB(WD_PWRGD) has a glitch during boot, but currently no functional impact found by AMD Summy
		Page 16 1.Reserved SPI_DEBUG header for SPEC. 2.Del DSM function del SB GP13 & GP31 for no use
		Page 20 1.Reserved F_USB3 header for SPEC.
		Page 22 1.Change SB_PWRGD direction 2.SEN_HEADER change to 6 pins for Lenovo request 3.Change GP32 to GP41 for SB710 Thermal Alert function pin use standby power
		Page 23 1.Reserved COM1 header function for SPEC.
		Page 24 1.Del DSM function for no use 2.Change R66 and R73 value, for use the same circuit design 3.Change R526 to 100ohm for to avoid when use 8103EL LAN into test mode to make LAN LED have issue
		Page 31 1.Change SB_PWRGD direction
1.01	09'1110	**Page 4** 1.Change EC43 from 100uF to 470uF for VDDA_1_2 overshoot
		Page 9 1.Change Q14 from the 2N7002 (RDSon=7.5 ohm) to P8503BMG (RDSon=85m ohm) for the 1.8V HDMI power to fix HDMI Signal (1080P Eye), that about MOS Ref
		Page 18 1.Change HDMI conn. use have screw hole for EMI 2.CHOKE19,CHOKE20,CHOKE21,CHOKE22 change use to HDMI CHOKE for SI(1080P Eye)
		Page 27 1.Change R149,R154,R134 from 1ohm to 2.2 ohm for ST,Infineon MOS VDS de-reting test (Vcore power switch check)
		Other 1.Layout move the MAC address on silkscreen top for it too close P/N Label, bar code had screen issue by Lenovo

Elitegroup Computer Systems

Title: History

Size: Custom | Document Number: RS780Q-LM3 | Rev: 1.01

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