RS780M-A2 V : 1.0

SCHEMATICS TABLE:

Page	Index	Page	Index
1	COVER PAGE	20	SB700 SATA/IDE/HWM/SPI
2	BLOCK DIADRAM	21	SB700 STRAPS
3	CPU M2-1 HyperTransport	22	PCI1&2
4	CPU M2-2 DDR2	23	USB/IDE
5	CPU M2-3 Miscellany	24	PCI-E x1(2 SLOTS) & PCI3
6	CPU M2-4 Power and Ground	25	PCIE LAN RTL8111C/8101E-1
7	First Logic DDR2 DIMM	26	Audio Codec ALC888S
8	Second Logic DDR2 DIMM	27	Audio Interface
9	DDR2 Termination	28	JMB361 ESATA+USB
10	CLOCK GEN ICS9LPRS471	29	IT8726
11	RS780 HT LINK I/F	30	FAN CTAL
12	RS780 PCIE I/F	31	FRONT PANEL
13	RS780 SYSTEM I/F	32	OVER CLOCK / PS2
14	RS780 POWER	33	CPU VCORE ISL6323
15	PCI-E X16 CONN&PCI-E X8CONN	34	NB POWER
16	VGA/HDMI	35	DC-DC
17	SB700 STRAP/PWR/DECOUPLING	36	POWER SEQUENCE
18	SB700 PCIE/PCI/CPU/LPC	37	CLOCK DISTRIBUTION
19	SB700 ACPI/GPIO//USB/AUDIO	38	POWER DELIVERY CHART
		39	Attention&104&IMPENDANCE

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

3) DESIGN NOTES in red are critical, and must be understood and followed.

REVISION HISTORY:

Rev	Date	Notes
VA	2008/08/12	
V1.0	2008/09/18	

Modify RS780D

DEL	ADD
1. SP	1. JMB361(ESATA)
2. PCIE SW	2. +1 PCI
3. -1 PCIE x16	3. POWER LED
4. -1 LAN 8112	
5. 1394	
6. 4PIN POWER	

PCB STACK:
L1:TOP
L2:PWR
L3:GND
L4:BOTTON

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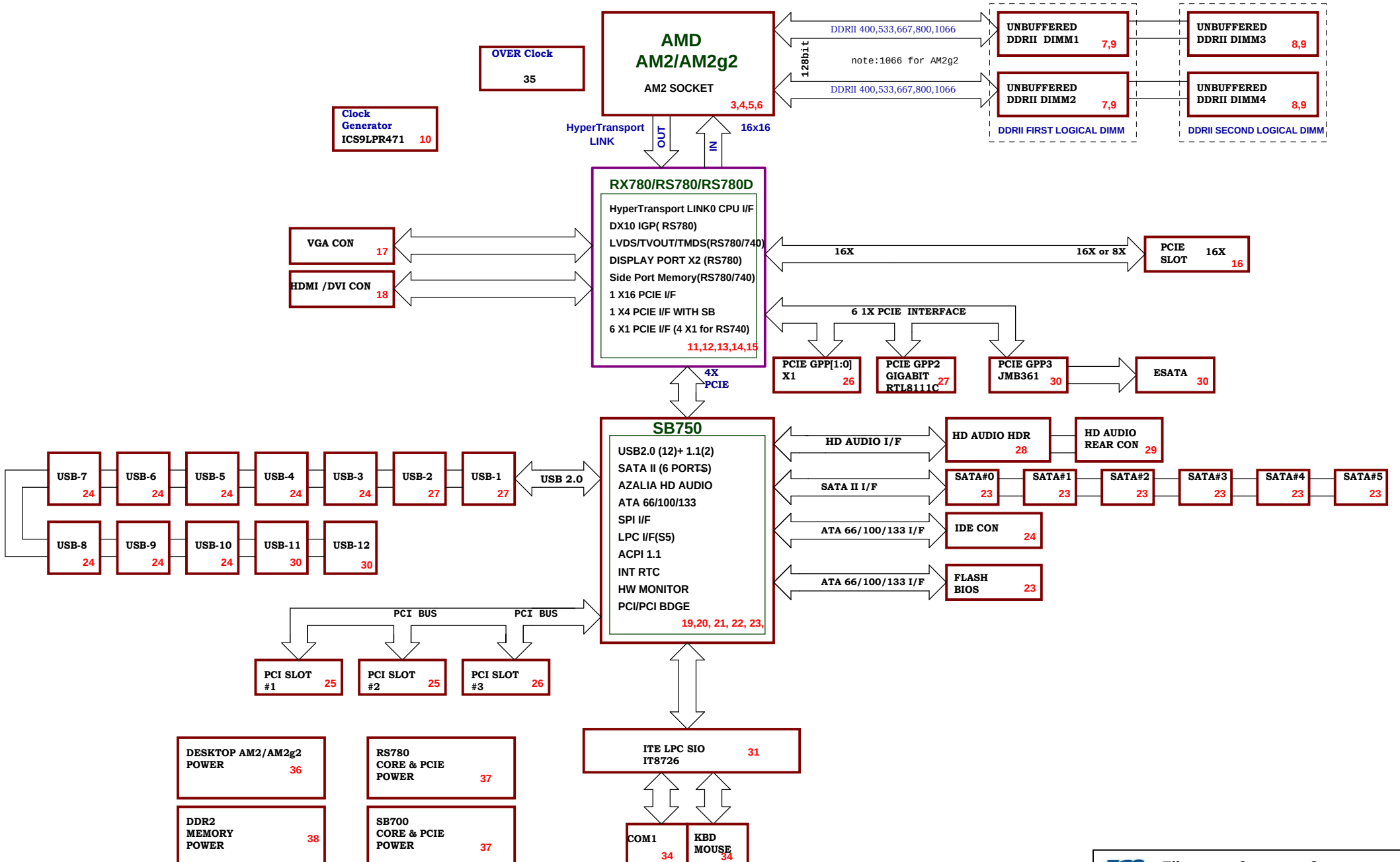
Title: Cover Page

Size: Custom | Document Number: RS780M-A2 | Rev: 1.0

Date: Tuesday, October 21, 2008 | Sheet 1 of 39

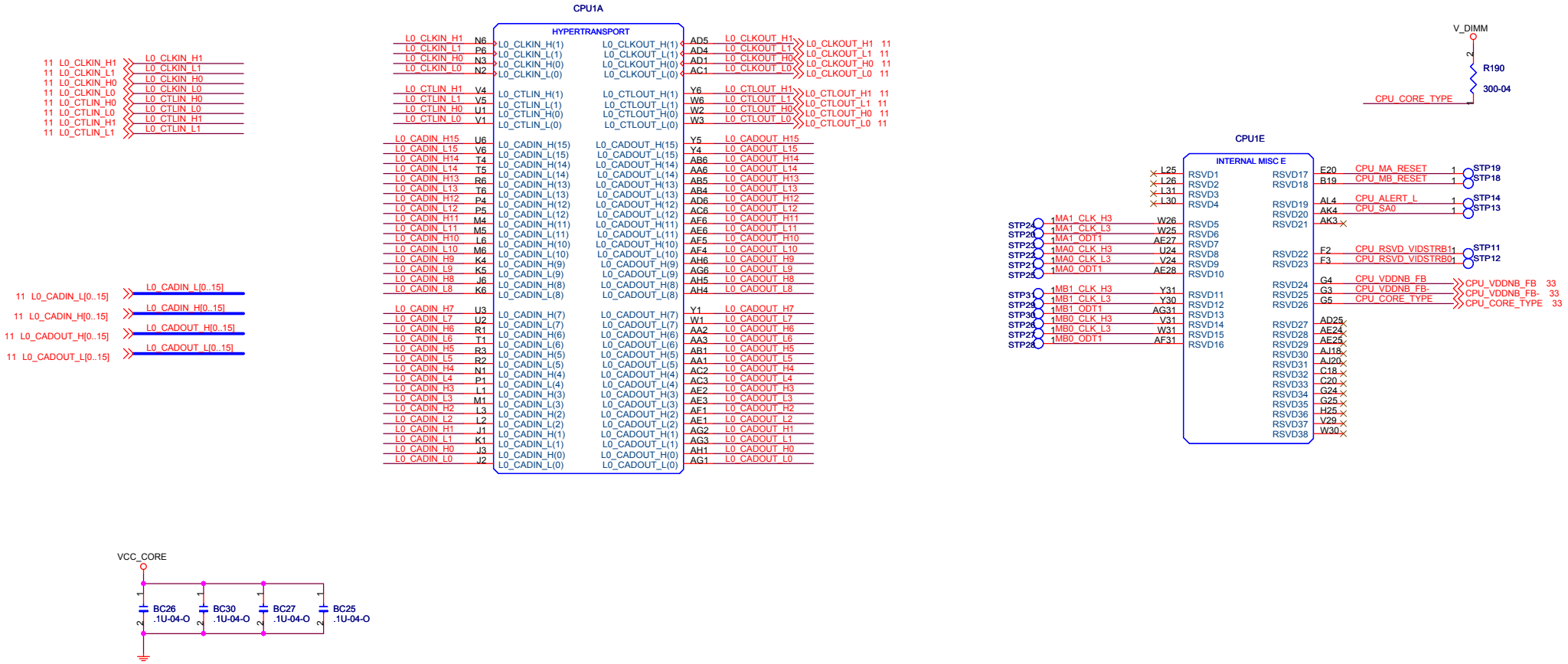


Elitegroup Computer Systems

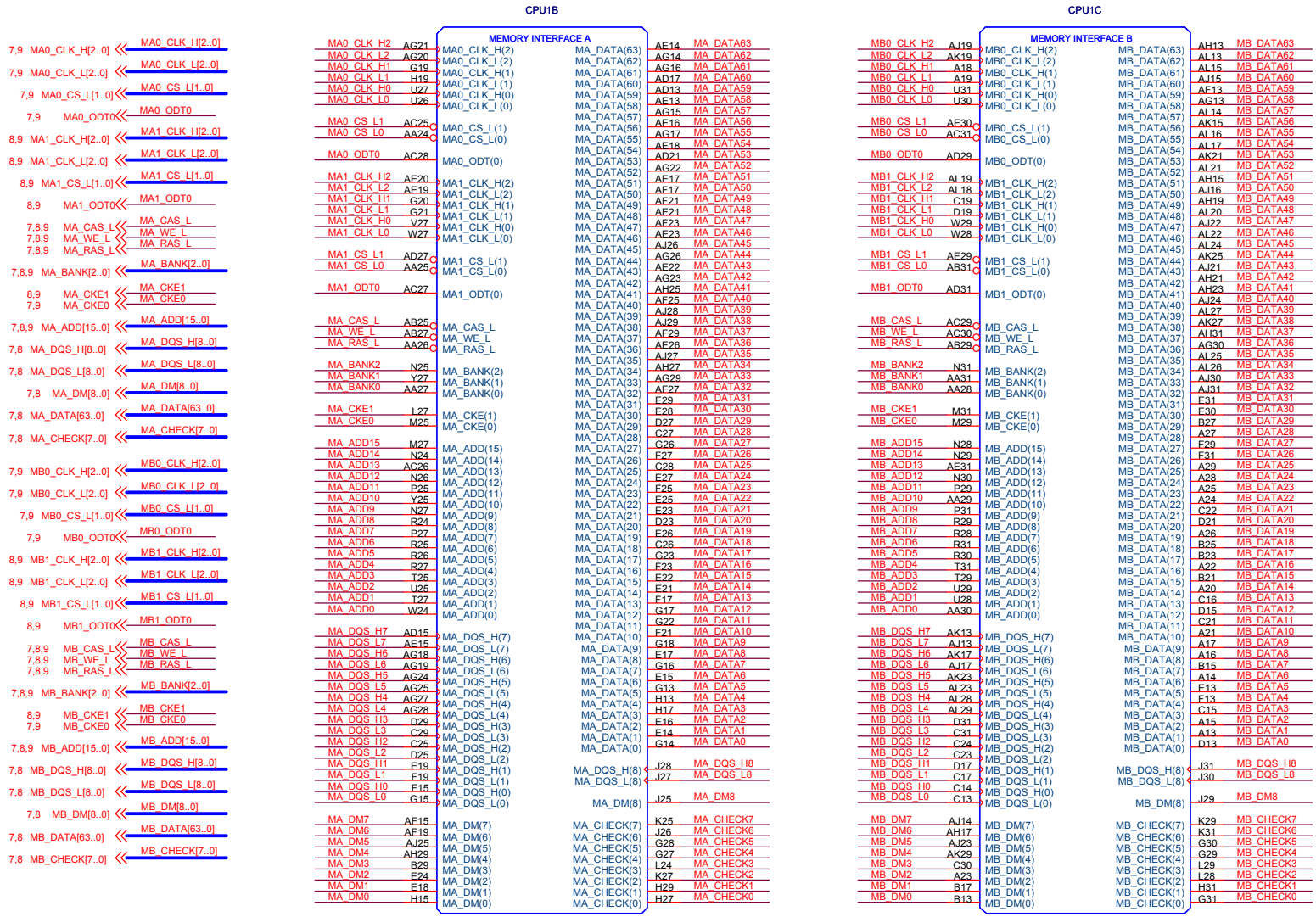
Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	RS780M-A2	1.0

Date: Tuesday, October 21, 2008 Sheet 2 of 39

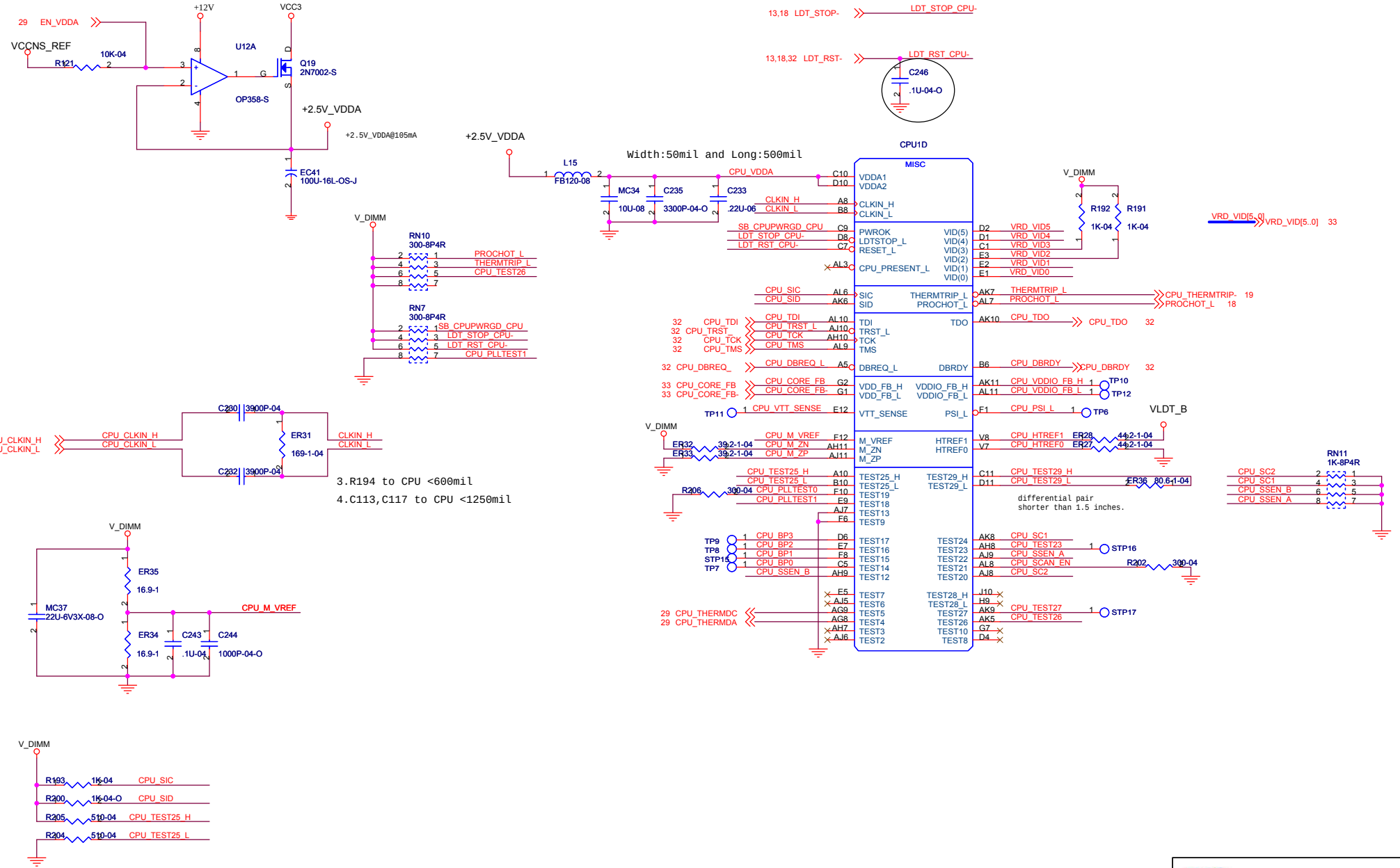


Elitegroup Computer Systems		
Title: CPU M2-1 HyperTransport		
Size: Custom	Document Number: RS780M-A2	Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 3 of 39	

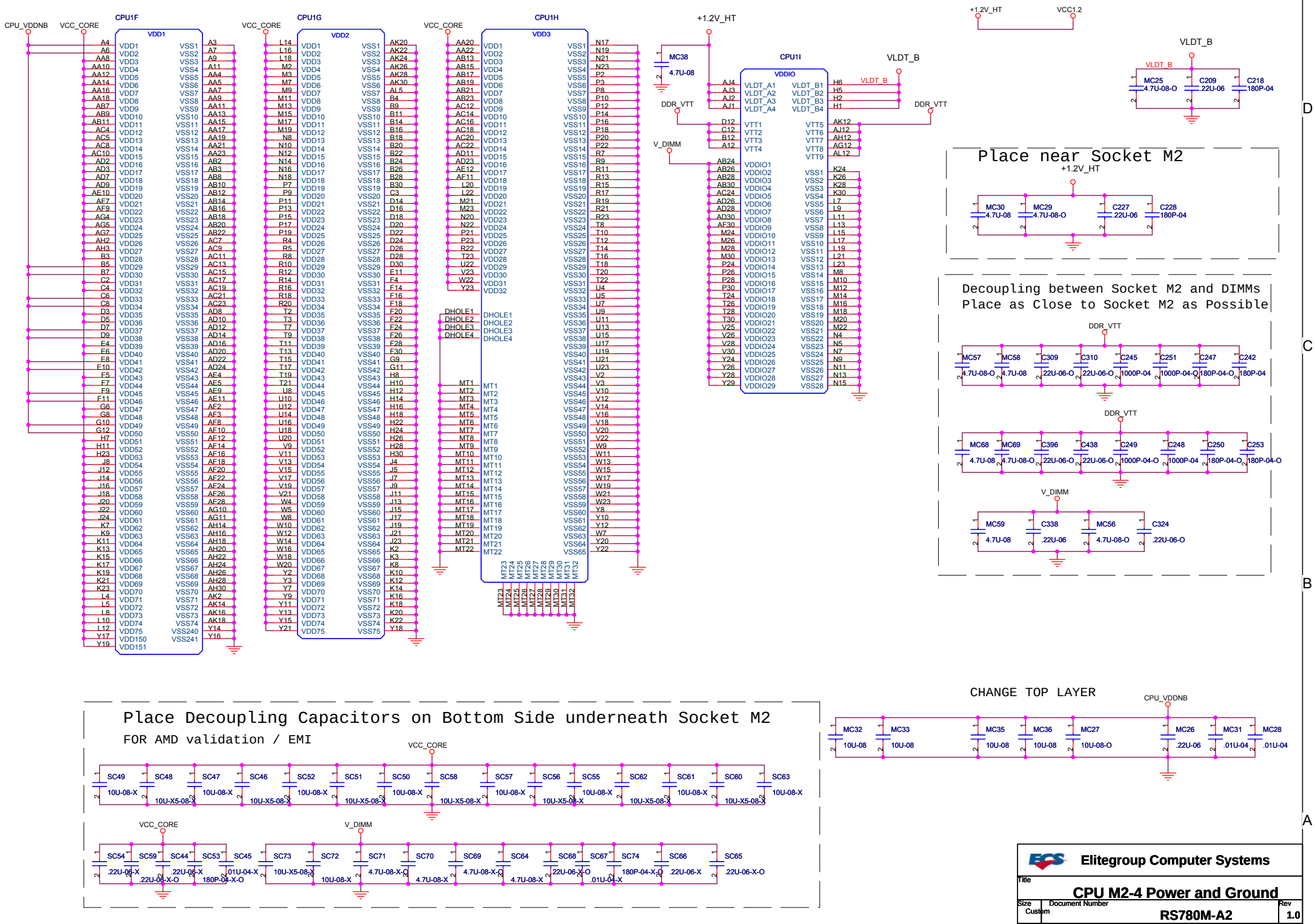


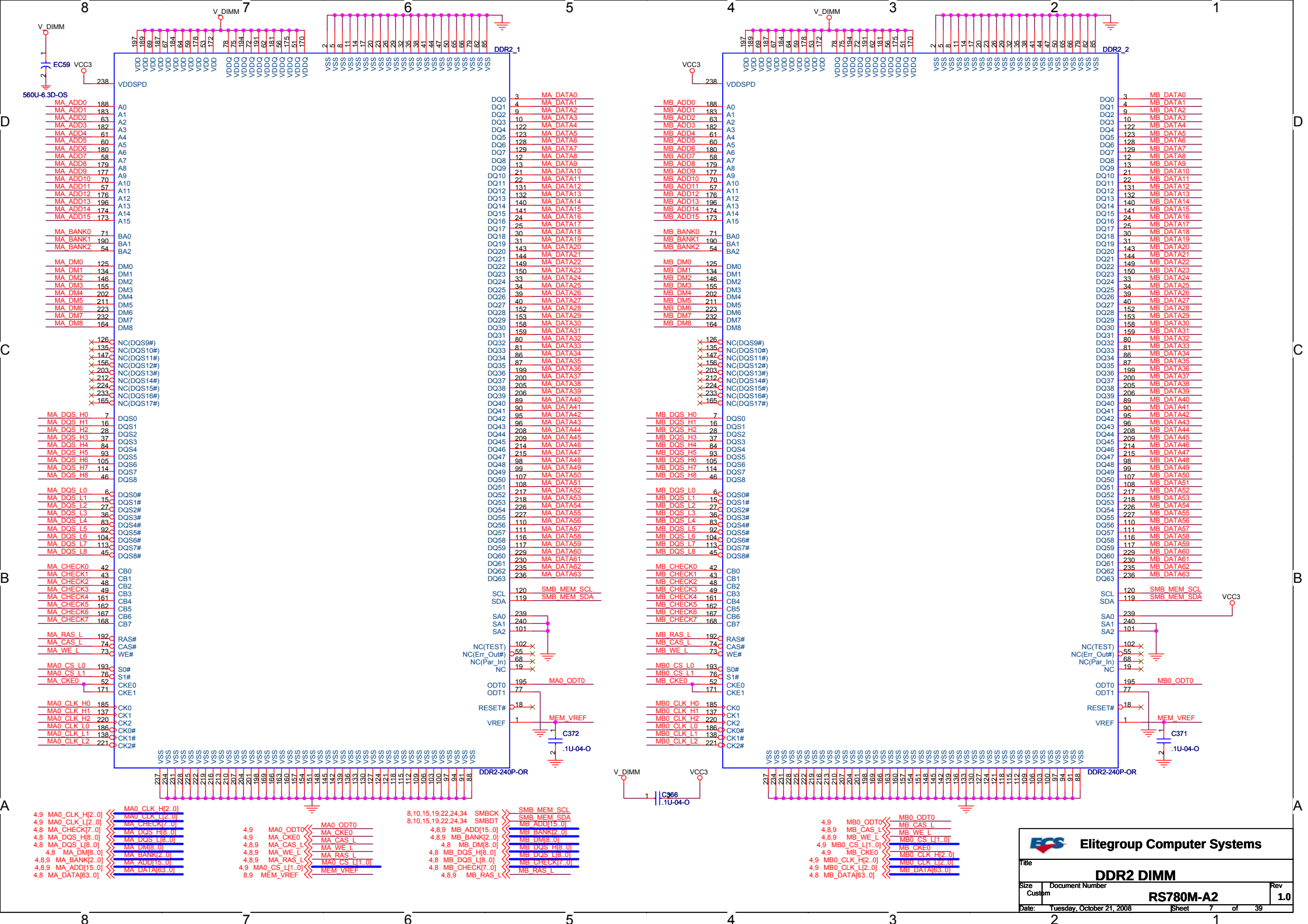
Elitegroup Computer Systems	
Title	CPU M2-2 DDR2
Size: Custom	Document Number: RS780M-A2
Rev	1.0
Date: Tuesday, October 21, 2008	Sheet 4 of 39

+2.5V_VDDA for CPU PLL



Elitegroup Computer Systems	
Title	CPU M2-3 Miscellany
Size: Custom	Document Number: RS780M-A2
Rev	1.0
Date: Tuesday, October 21, 2008	Sheet 5 of 39


CPU1F
CPU1G
CPU1H
CPU1I
VDD1
VDD2
VDD3
VDDIO
CPU_VDDNB
VCC_CORE
+1.2V_HT
VCC1.2
VLDT_B
DDR_VTT
V_DIMM
MC38
4.7U-08
Place near Socket M2
MC30
MC29
MC25
C227
C209
C218
C228
.22U-06
180P-04
Decoupling between Socket M2 and DIMMs
Place as Close to Socket M2 as Possible
MC57
MC58
C309
C310
C245
C251
C247
C242
MC68
MC69
C396
C438
C249
C248
C250
C253
MC59
C338
MC56
C324
Place Decoupling Capacitors on Bottom Side underneath Socket M2
FOR AMD validation / EMI
SC49
SC48
SC47
SC46
SC52
SC51
SC50
SC58
SC57
SC56
SC55
SC62
SC61
SC60
SC63
SC54
SC59
SC44
SC53
SC45
SC73
SC72
SC71
SC70
SC69
SC64
SC68
SC67
SC74
SC66
SC65
CHANGE TOP LAYER
MC32
MC33
MC35
MC36
MC27
MC26
MC31
MC28
Elitegroup Computer Systems
CPU M2-4 Power and Ground
RS780M-A2
Tuesday, October 21, 2008
Sheet 6 of 39



Title	DDR2 DIMM
Size	Custom
Document Number	RS780M-A2
Rev	1.0
Date:	Tuesday, October 21, 2008
Sheet	7 of 39

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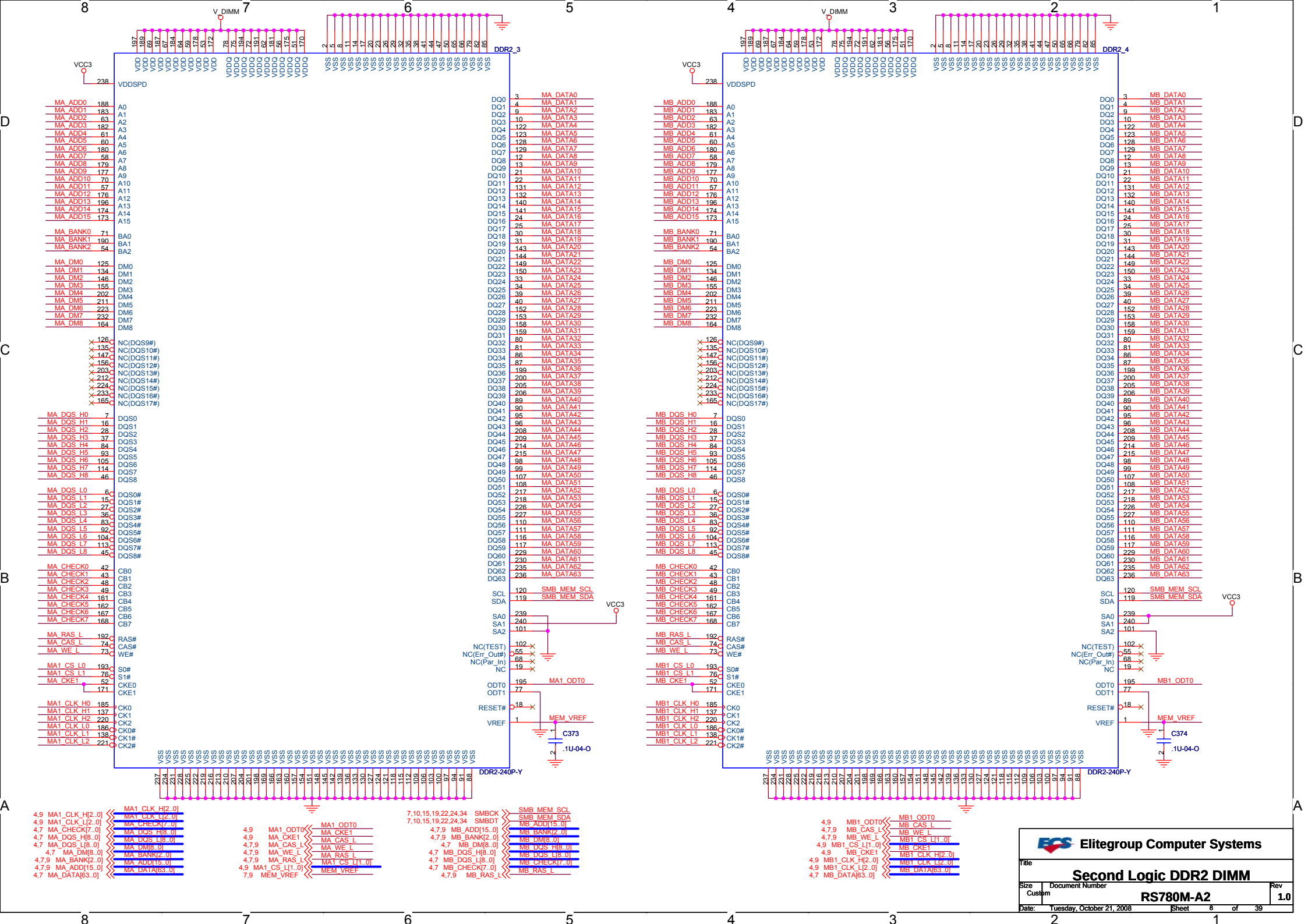
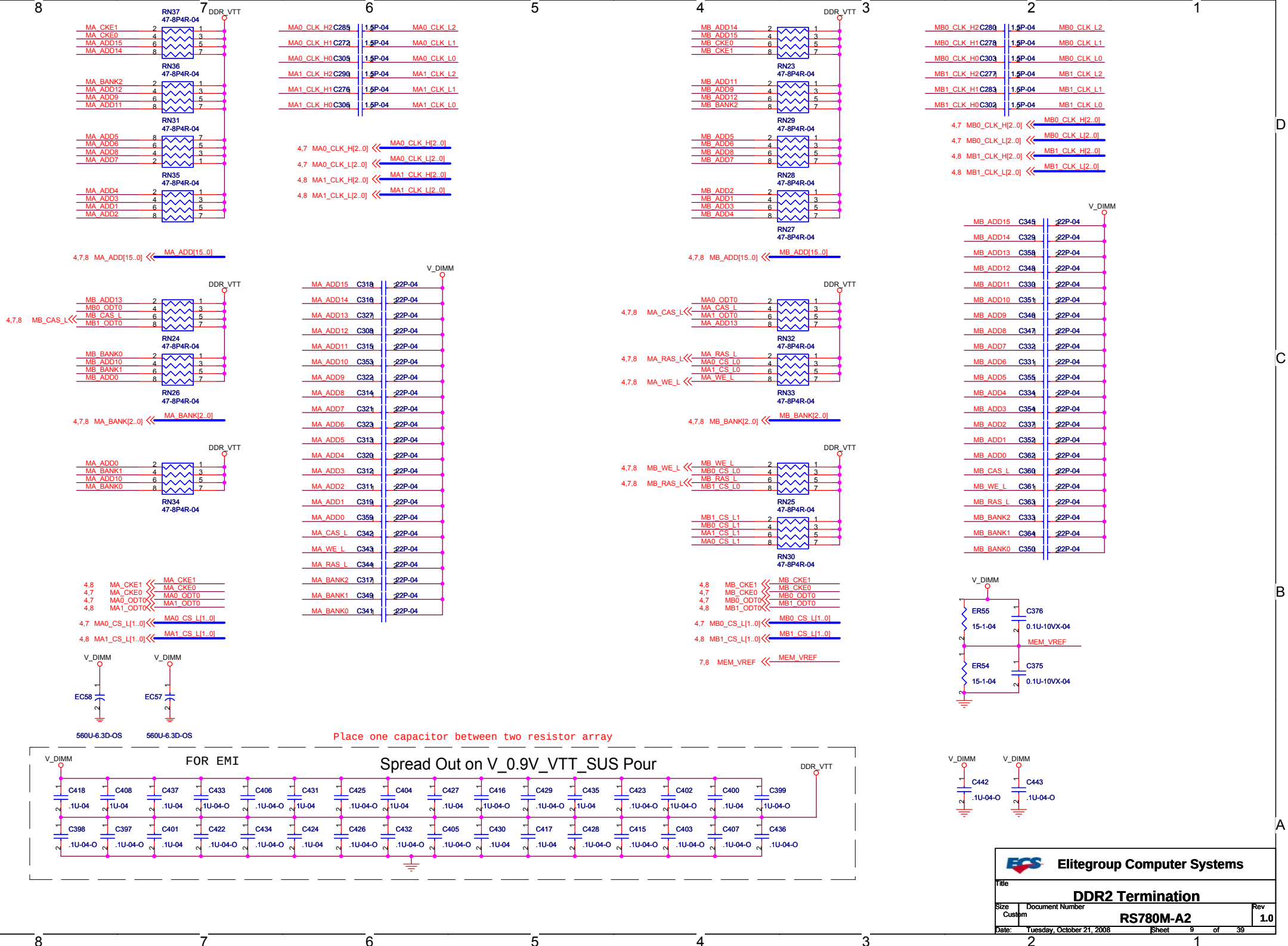
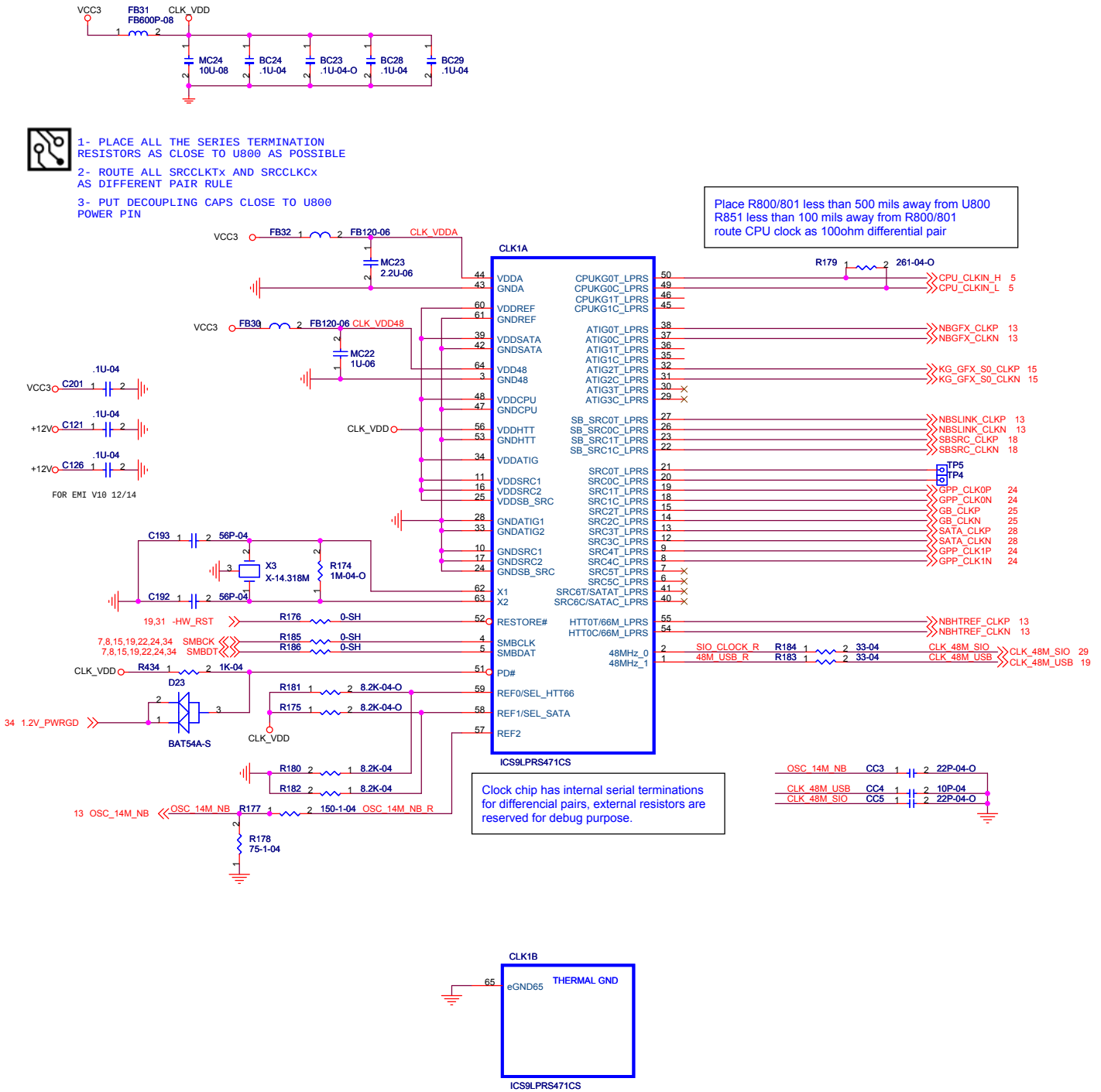

DDR2_3
DDR2_4
DDR2-240P-Y
V_DIMM
VCC3
VDDSPD
MA_ADD0
MA_ADD1
MA_ADD2
MA_ADD3
MA_ADD4
MA_ADD5
MA_ADD6
MA_ADD7
MA_ADD8
MA_ADD9
MA_ADD10
MA_ADD11
MA_ADD12
MA_ADD13
MA_ADD14
MA_ADD15
MA_BANK0
MA_BANK1
MA_BANK2
MA_DM0
MA_DM1
MA_DM2
MA_DM3
MA_DM4
MA_DM5
MA_DM6
MA_DM7
MA_DM8
MA_DQS_H0
MA_DQS_H1
MA_DQS_H2
MA_DQS_H3
MA_DQS_H4
MA_DQS_H5
MA_DQS_H6
MA_DQS_H7
MA_DQS_H8
MA_DQS_L0
MA_DQS_L1
MA_DQS_L2
MA_DQS_L3
MA_DQS_L4
MA_DQS_L5
MA_DQS_L6
MA_DQS_L7
MA_DQS_L8
MA_CHECK0
MA_CHECK1
MA_CHECK2
MA_CHECK3
MA_CHECK4
MA_CHECK5
MA_CHECK6
MA_CHECK7
MA_RAS_L
MA_CAS_L
MA_WE_L
MA1_CS_L0
MA1_CS_L1
MA_CKE1
MA1_CLK_H0
MA1_CLK_H1
MA1_CLK_H2
MA1_CLK_L0
MA1_CLK_L1
MA1_CLK_L2
MA_DATA0
MA_DATA1
MA_DATA2
MA_DATA3
MA_DATA4
MA_DATA5
MA_DATA6
MA_DATA7
MA_DATA8
MA_DATA9
MA_DATA10
MA_DATA11
MA_DATA12
MA_DATA13
MA_DATA14
MA_DATA15
MA_DATA16
MA_DATA17
MA_DATA18
MA_DATA19
MA_DATA20
MA_DATA21
MA_DATA22
MA_DATA23
MA_DATA24
MA_DATA25
MA_DATA26
MA_DATA27
MA_DATA28
MA_DATA29
MA_DATA30
MA_DATA31
MA_DATA32
MA_DATA33
MA_DATA34
MA_DATA35
MA_DATA36
MA_DATA37
MA_DATA38
MA_DATA39
MA_DATA40
MA_DATA41
MA_DATA42
MA_DATA43
MA_DATA44
MA_DATA45
MA_DATA46
MA_DATA47
MA_DATA48
MA_DATA49
MA_DATA50
MA_DATA51
MA_DATA52
MA_DATA53
MA_DATA54
MA_DATA55
MA_DATA56
MA_DATA57
MA_DATA58
MA_DATA59
MA_DATA60
MA_DATA61
MA_DATA62
MA_DATA63
SMB_MEM_SCL
SMB_MEM_SDA
MA1_ODT0
MEM_VREF
C373
C374
.1U-04-O
MB_ADD0
MB_ADD1
MB_ADD2
MB_ADD3
MB_ADD4
MB_ADD5
MB_ADD6
MB_ADD7
MB_ADD8
MB_ADD9
MB_ADD10
MB_ADD11
MB_ADD12
MB_ADD13
MB_ADD14
MB_ADD15
MB_BANK0
MB_BANK1
MB_BANK2
MB_DM0
MB_DM1
MB_DM2
MB_DM3
MB_DM4
MB_DM5
MB_DM6
MB_DM7
MB_DM8
MB_DQS_H0
MB_DQS_H1
MB_DQS_H2
MB_DQS_H3
MB_DQS_H4
MB_DQS_H5
MB_DQS_H6
MB_DQS_H7
MB_DQS_H8
MB_DQS_L0
MB_DQS_L1
MB_DQS_L2
MB_DQS_L3
MB_DQS_L4
MB_DQS_L5
MB_DQS_L6
MB_DQS_L7
MB_DQS_L8
MB_CHECK0
MB_CHECK1
MB_CHECK2
MB_CHECK3
MB_CHECK4
MB_CHECK5
MB_CHECK6
MB_CHECK7
MB_RAS_L
MB_CAS_L
MB_WE_L
MB1_CS_L0
MB1_CS_L1
MB_CKE1
MB1_CLK_H0
MB1_CLK_H1
MB1_CLK_H2
MB1_CLK_L0
MB1_CLK_L1
MB1_CLK_L2
MB_DATA0
MB_DATA1
MB_DATA2
MB_DATA3
MB_DATA4
MB_DATA5
MB_DATA6
MB_DATA7
MB_DATA8
MB_DATA9
MB_DATA10
MB_DATA11
MB_DATA12
MB_DATA13
MB_DATA14
MB_DATA15
MB_DATA16
MB_DATA17
MB_DATA18
MB_DATA19
MB_DATA20
MB_DATA21
MB_DATA22
MB_DATA23
MB_DATA24
MB_DATA25
MB_DATA26
MB_DATA27
MB_DATA28
MB_DATA29
MB_DATA30
MB_DATA31
MB_DATA32
MB_DATA33
MB_DATA34
MB_DATA35
MB_DATA36
MB_DATA37
MB_DATA38
MB_DATA39
MB_DATA40
MB_DATA41
MB_DATA42
MB_DATA43
MB_DATA44
MB_DATA45
MB_DATA46
MB_DATA47
MB_DATA48
MB_DATA49
MB_DATA50
MB_DATA51
MB_DATA52
MB_DATA53
MB_DATA54
MB_DATA55
MB_DATA56
MB_DATA57
MB_DATA58
MB_DATA59
MB_DATA60
MB_DATA61
MB_DATA62
MB_DATA63
MB1_ODT0
MB_CKE1
MB_CAS_L
MB_WE_L
MB1_CS_L1
MB_CKE1
MB1_CLK_H2
MB1_CLK_L2
MB_DATA63..0
MA1_CLK_H2..0
MA1_CLK_L2..0
MA_CHECK7..0
MA_DQS_H8..0
MA_DQS_L8..0
MA_DM8..0
MA_BANK2..0
MA_ADD15..0
MA_DATA63..0
MA_CKE1
MA_CAS_L
MA_WE_L
MA_RAS_L
MA1_CS_L1..0
MEM_VREF
SMBCK
SMBDT
SMB_MEM_SCL
SMB_MEM_SDA
MB_ADD15..0
MB_BANK2..0
MB_DM8..0
MB_DQS_H8..0
MB_DQS_L8..0
MB_CHECK7..0
MB_RAS_L
MB1_ODT0
MB_CAS_L
MB_WE_L
MB1_CS_L1..0
MB_CKE1
MB1_CLK_H2..0
MB1_CLK_L2..0
MB_DATA63..0
Elitegroup Computer Systems
Second Logic DDR2 DIMM
RS780M-A2
Custom
1.0
Tuesday, October 21, 2008
Sheet 8 of 39


RN37 47-8P4R-04
MA_CKE1
MA_CKE0
MA_ADD15
MA_ADD14
RN36 47-8P4R-04
MA_BANK2
MA_ADD12
MA_ADD9
MA_ADD11
RN31 47-8P4R-04
MA_ADD5
MA_ADD6
MA_ADD8
MA_ADD7
RN35 47-8P4R-04
MA_ADD4
MA_ADD3
MA_ADD1
MA_ADD2
DDR_VTT
4,7,8 MA_ADD[15..0]
MA_ADD[15..0]
MA0_CLK_H2 C285 1.5P-04 MA0_CLK_L2
MA0_CLK_H1 C272 1.5P-04 MA0_CLK_L1
MA0_CLK_H0 C305 1.5P-04 MA0_CLK_L0
MA1_CLK_H2 C290 1.5P-04 MA1_CLK_L2
MA1_CLK_H1 C276 1.5P-04 MA1_CLK_L1
MA1_CLK_H0 C306 1.5P-04 MA1_CLK_L0
4,7 MA0_CLK_H[2..0]
4,7 MA0_CLK_L[2..0]
4,8 MA1_CLK_H[2..0]
4,8 MA1_CLK_L[2..0]
MA0_CLK_H[2..0]
MA0_CLK_L[2..0]
MA1_CLK_H[2..0]
MA1_CLK_L[2..0]
RN24 47-8P4R-04
MB_ADD13
MB0_ODT0
MB_CAS_L
MB1_ODT0
4,7,8 MB_CAS_L
RN26 47-8P4R-04
MB_BANK0
MB_ADD10
MB_BANK1
MB_ADD0
4,7,8 MA_BANK[2..0]
MA_BANK[2..0]
RN34 47-8P4R-04
MA_ADD0
MA_BANK1
MA_ADD10
MA_BANK0
V_DIMM
MA_ADD15 C318 22P-04
MA_ADD14 C316 22P-04
MA_ADD13 C327 22P-04
MA_ADD12 C309 22P-04
MA_ADD11 C315 22P-04
MA_ADD10 C353 22P-04
MA_ADD9 C322 22P-04
MA_ADD8 C314 22P-04
MA_ADD7 C321 22P-04
MA_ADD6 C323 22P-04
MA_ADD5 C313 22P-04
MA_ADD4 C320 22P-04
MA_ADD3 C312 22P-04
MA_ADD2 C311 22P-04
MA_ADD1 C319 22P-04
MA_ADD0 C359 22P-04
MA_CAS_L C342 22P-04
MA_WE_L C343 22P-04
MA_RAS_L C344 22P-04
MA_BANK2 C317 22P-04
MA_BANK1 C349 22P-04
MA_BANK0 C341 22P-04
4,8 MA_CKE1
4,7 MA_CKE0
4,7 MA0_ODT0
4,8 MA1_ODT0
MA_CKE1
MA_CKE0
MA0_ODT0
MA1_ODT0
4,7 MA0_CS_L[1..0]
4,8 MA1_CS_L[1..0]
MA0_CS_L[1..0]
MA1_CS_L[1..0]
V_DIMM
EC58
EC57
560U-6.3D-OS
560U-6.3D-OS
RN23 47-8P4R-04
MB_ADD14
MB_ADD15
MB_CKE0
MB_CKE1
RN29 47-8P4R-04
MB_ADD11
MB_ADD9
MB_ADD12
MB_BANK2
RN28 47-8P4R-04
MB_ADD5
MB_ADD6
MB_ADD8
MB_ADD7
RN27 47-8P4R-04
MB_ADD2
MB_ADD1
MB_ADD3
MB_ADD4
DDR_VTT
4,7,8 MB_ADD[15..0]
MB_ADD[15..0]
MB0_CLK_H2 C280 1.5P-04 MB0_CLK_L2
MB0_CLK_H1 C278 1.5P-04 MB0_CLK_L1
MB0_CLK_H0 C303 1.5P-04 MB0_CLK_L0
MB1_CLK_H2 C277 1.5P-04 MB1_CLK_L2
MB1_CLK_H1 C283 1.5P-04 MB1_CLK_L1
MB1_CLK_H0 C302 1.5P-04 MB1_CLK_L0
4,7 MB0_CLK_H[2..0]
4,7 MB0_CLK_L[2..0]
4,8 MB1_CLK_H[2..0]
4,8 MB1_CLK_L[2..0]
MB0_CLK_H[2..0]
MB0_CLK_L[2..0]
MB1_CLK_H[2..0]
MB1_CLK_L[2..0]
RN32 47-8P4R-04
MA0_ODT0
MA_CAS_L
MA1_ODT0
MA_ADD13
4,7,8 MA_CAS_L
RN33 47-8P4R-04
MA_RAS_L
MA0_CS_L0
MA1_CS_L0
MA_WE_L
4,7,8 MA_RAS_L
4,7,8 MA_WE_L
4,7,8 MB_BANK[2..0]
MB_BANK[2..0]
RN25 47-8P4R-04
MB_WE_L
MB0_CS_L0
MB_RAS_L
MB1_CS_L0
4,7,8 MB_WE_L
4,7,8 MB_RAS_L
RN30 47-8P4R-04
MB1_CS_L1
MB0_CS_L1
MA1_CS_L1
MA0_CS_L1
V_DIMM
MB_ADD15 C345 22P-04
MB_ADD14 C329 22P-04
MB_ADD13 C358 22P-04
MB_ADD12 C348 22P-04
MB_ADD11 C330 22P-04
MB_ADD10 C351 22P-04
MB_ADD9 C346 22P-04
MB_ADD8 C347 22P-04
MB_ADD7 C332 22P-04
MB_ADD6 C331 22P-04
MB_ADD5 C355 22P-04
MB_ADD4 C334 22P-04
MB_ADD3 C354 22P-04
MB_ADD2 C337 22P-04
MB_ADD1 C352 22P-04
MB_ADD0 C362 22P-04
MB_CAS_L C360 22P-04
MB_WE_L C361 22P-04
MB_RAS_L C363 22P-04
MB_BANK2 C333 22P-04
MB_BANK1 C364 22P-04
MB_BANK0 C350 22P-04
4,8 MB_CKE1
4,7 MB_CKE0
4,7 MB0_ODT0
4,8 MB1_ODT0
MB_CKE1
MB_CKE0
MB0_ODT0
MB1_ODT0
4,7 MB0_CS_L[1..0]
4,8 MB1_CS_L[1..0]
MB0_CS_L[1..0]
MB1_CS_L[1..0]
7,8 MEM_VREF
MEM_VREF
V_DIMM
ER55 15-1-04
C376 0.1U-10VX-04
MEM_VREF
ER54 15-1-04
C375 0.1U-10VX-04
Place one capacitor between two resistor array
FOR EMI
Spread Out on V_0.9V_VTT_SUS Pour
V_DIMM
DDR_VTT
C418 .1U-04
C408 .1U-04
C437 .1U-04
C433 .1U-04-O
C406 .1U-04-O
C431 .1U-04
C425 .1U-04-O
C404 .1U-04
C427 .1U-04
C416 .1U-04-O
C429 .1U-04-O
C435 .1U-04
C423 .1U-04-O
C402 .1U-04-O
C400 .1U-04
C399 .1U-04-O
C398 .1U-04-O
C397 .1U-04-O
C401 .1U-04
C422 .1U-04-O
C434 .1U-04-O
C424 .1U-04
C426 .1U-04-O
C432 .1U-04-O
C405 .1U-04-O
C430 .1U-04
C417 .1U-04
C428 .1U-04-O
C415 .1U-04-O
C403 .1U-04-O
C407 .1U-04-O
C436 .1U-04-O
V_DIMM
V_DIMM
C442 .1U-04-O
C443 .1U-04-O
Elitegroup Computer Systems
Title
DDR2 Termination
Size Custom
Document Number RS780M-A2
Rev 1.0
Date: Tuesday, October 21, 2008
Sheet 9 of 39



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 75R/100R
RS780 (Single-ended)	1.1V 150R/75R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

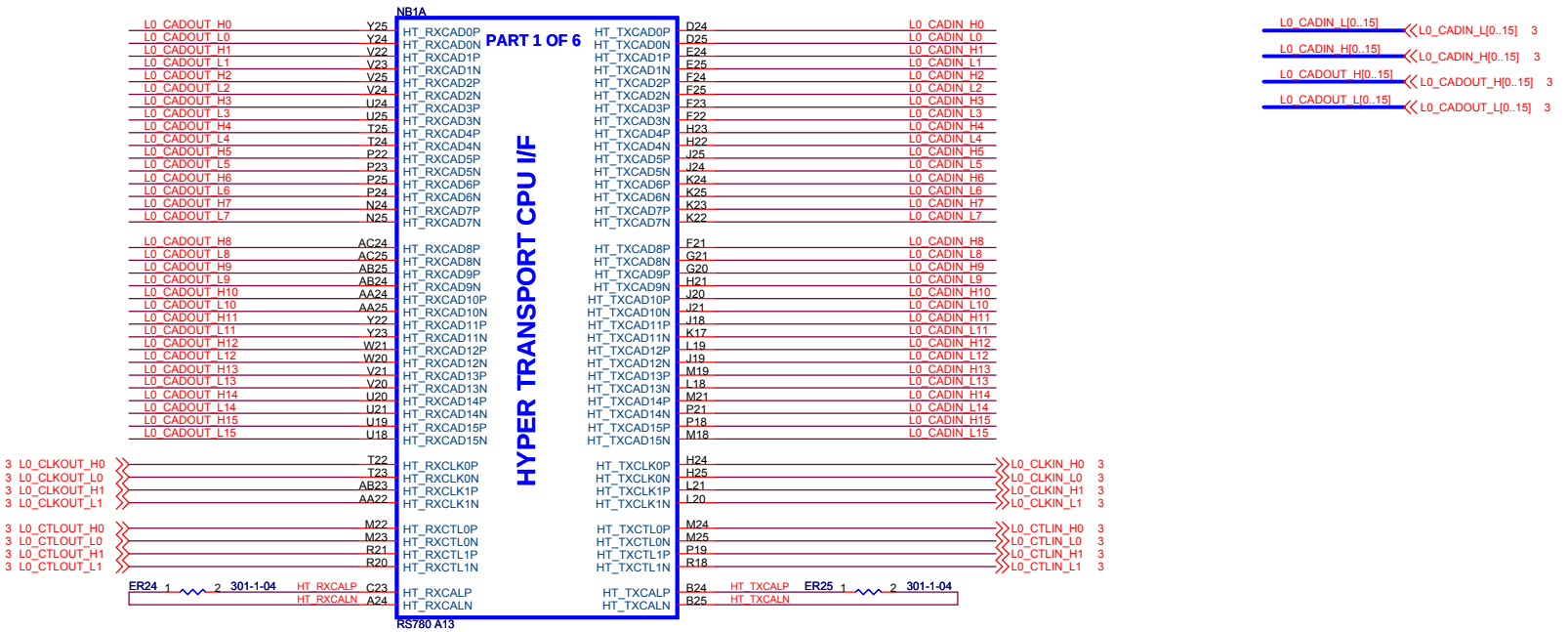
REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

Elitegroup Computer Systems

Title: CLOCK GEN ICS9LPRS472

Size | Document Number: RS780M-A2 | Rev: 1.0

Date: Tuesday, October 21, 2008 | Sheet 10 of 39



RX780/RS740/RS780 difference table (HT LINK)

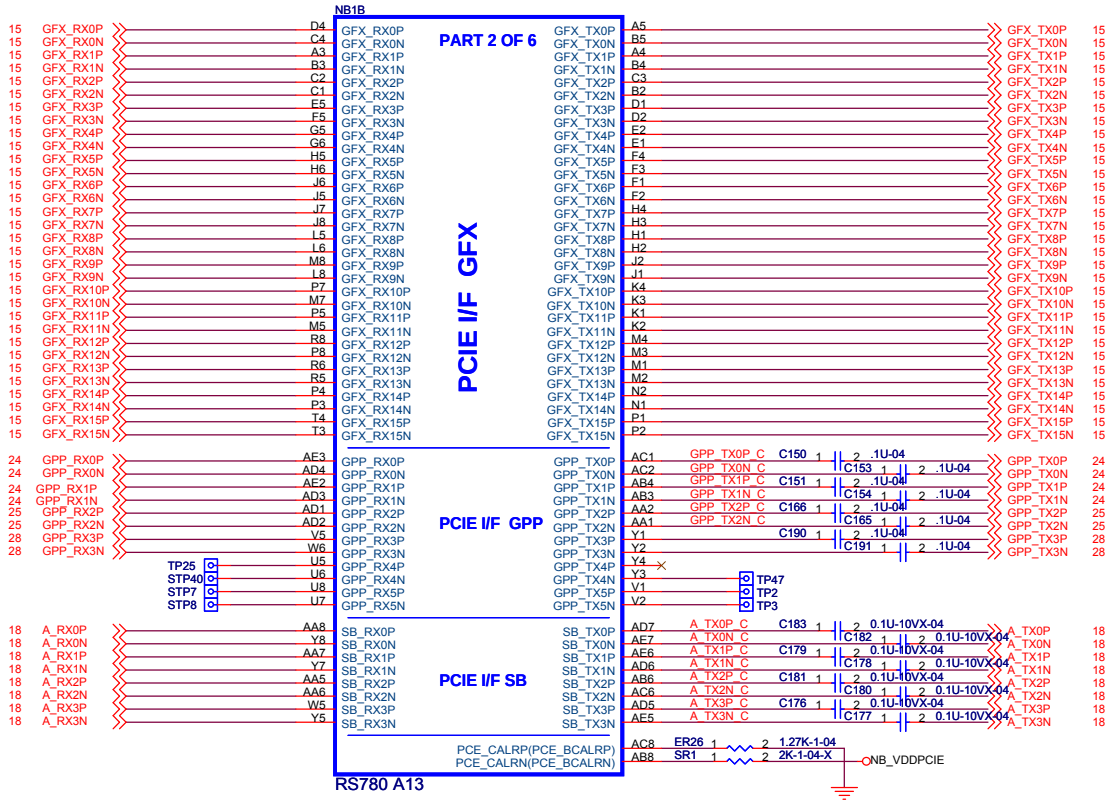
SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R *	1.21K	301R

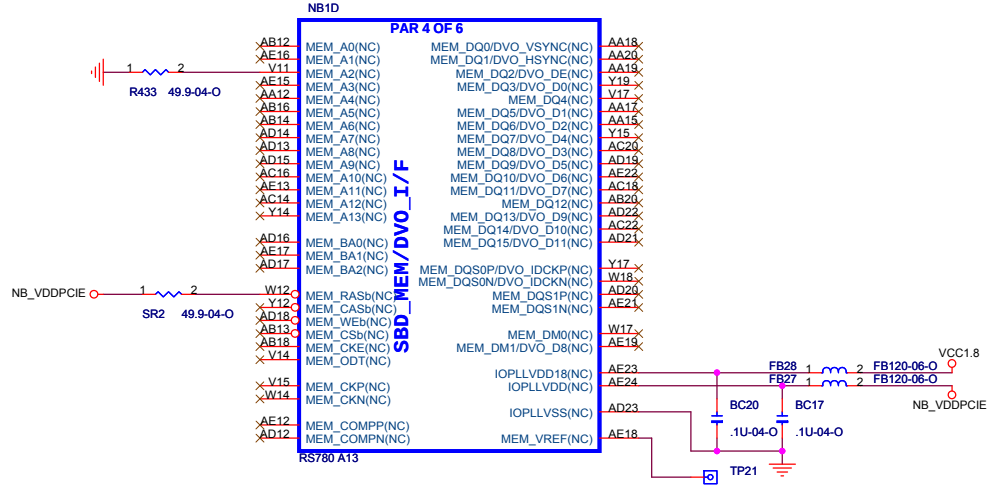
Elitegroup Computer Systems

Title: RS780 HT LINK I/F

Size | Document Number: RS780M-A2 | Rev: 1.0

Date: Tuesday, October 21, 2008 | Sheet 11 of 39





RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable
0 : Enable
RS780: pin VSYNC
```

RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1.  Disable
0 : Enable
RS780:  pin HSYNC
```

13,16 HSYNC — R437 3K-04 — VCC3

RS780 GFX Slot Routing table

GFX_MODE_SELECT	GFX SLOTS MODE
0	X16 LANES MODE (DEFAULT)
1	TWO X8 LANES MODE

RS780 GPP Routing table

	RS780
GPP X4 CONNECTOR	GPP[3:0]
GPP X1 CONNECTOR	GPP4
GIGABIT ETHERNET	GPP5

RS780 Display Port Support (muxed on GFX)

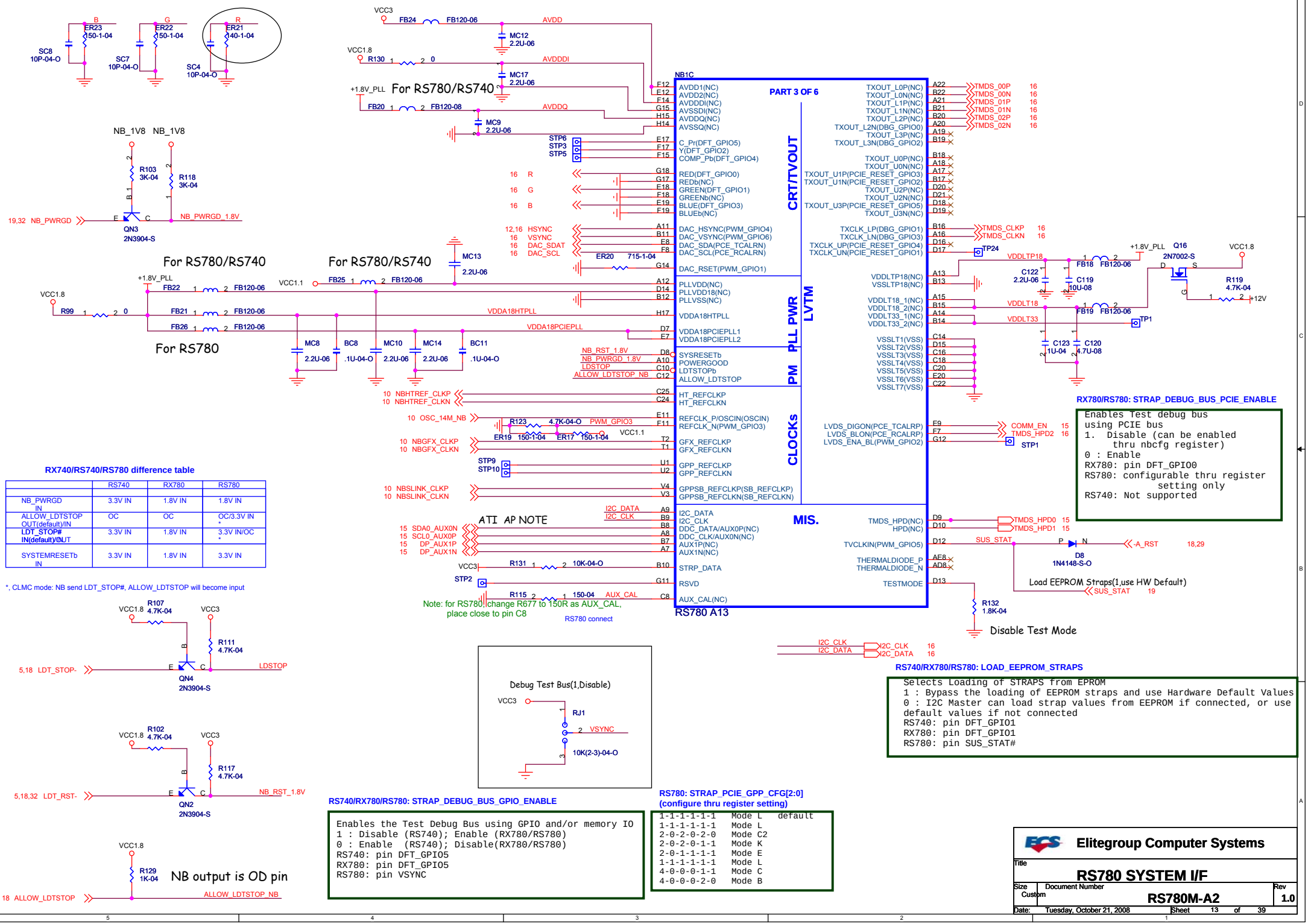
DP0	GFX_TX0,TX1,TX2 and TX3
	AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7
	AUX1 and HPD1

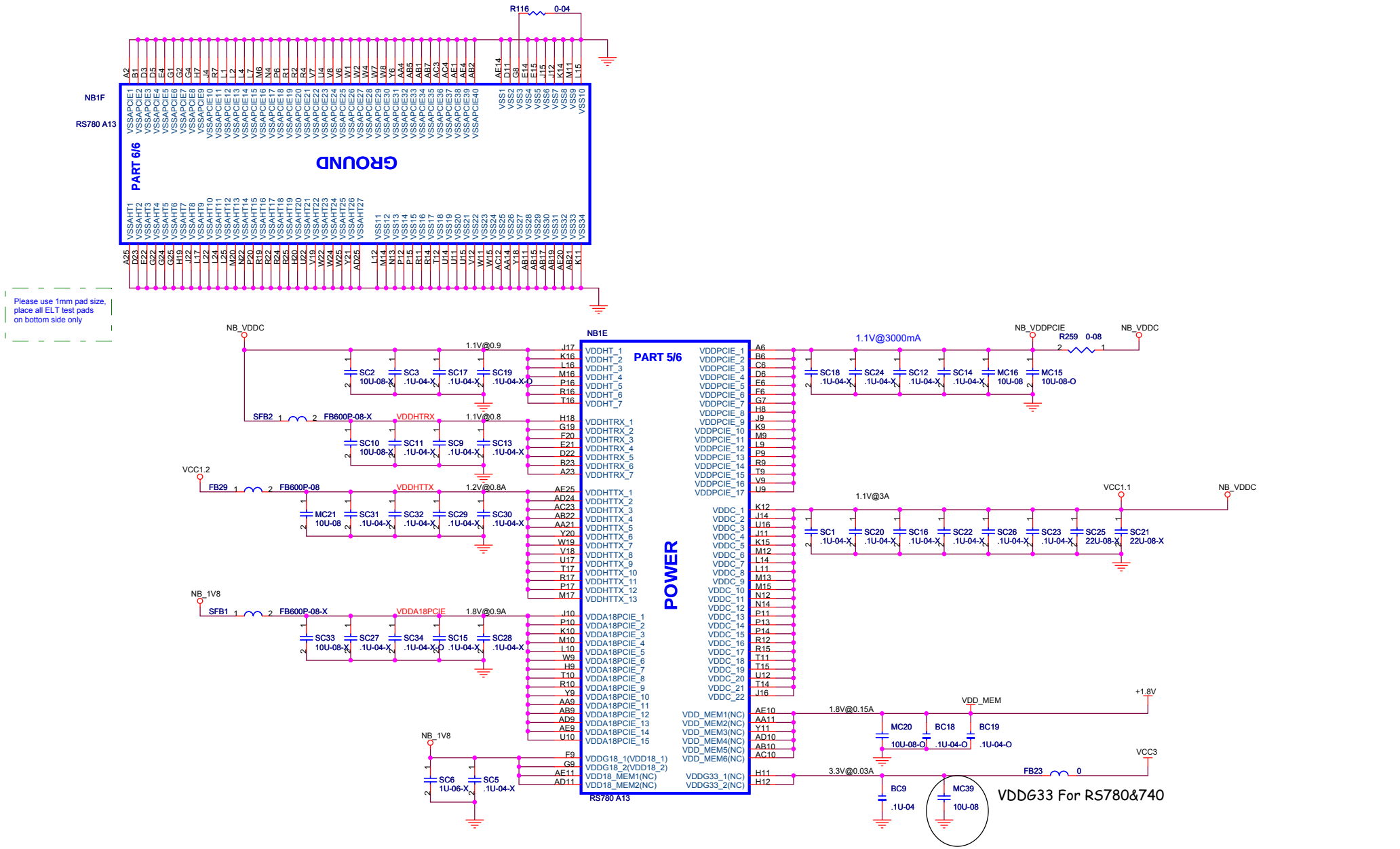
Elitegroup Computer Systems

Title: **RS780 PCIE I/F**

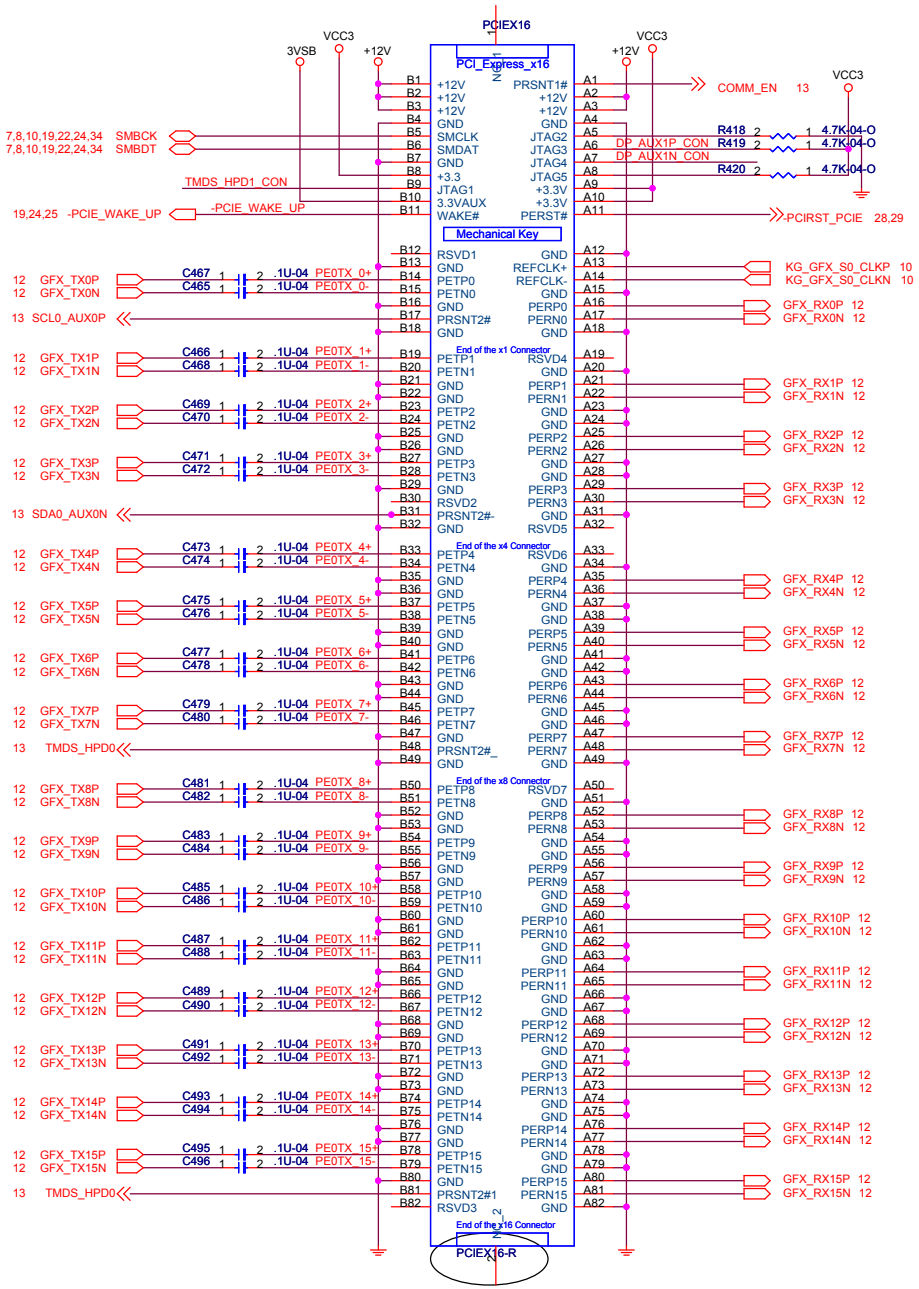
Size: Custom | Document Number: **RS780M-A2** | Rev: 1.0

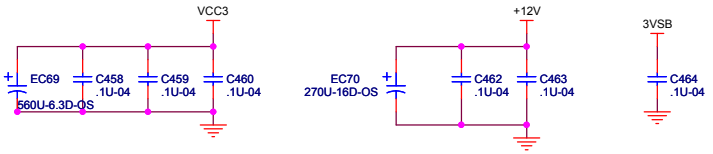
Date: Tuesday, October 21, 2008 | Sheet 12 of 39


SC8 10P-04-O
SC7 10P-04-O
SC4 10P-04-O
ER23 150-1-04
ER22 150-1-04
ER21 140-1-04
B
G
R
NB_1V8 NB_1V8
R103 3K-04
R118 3K-04
19,32 NB_PWRGD
NB_PWRGD_1.8V
QN3 2N3904-S
For RS780/RS740
For RS780/RS740
For RS780
VCC3
FB24 FB120-06
AVDD
MC12 2.2U-06
VCC1.8
R130 0
AVDDDI
MC17 2.2U-06
+1.8V_PLL
For RS780/RS740
FB20 FB120-08
AVDDQ
MC9 2.2U-06
MC13 2.2U-06
+1.8V_PLL
FB22 FB120-06
VCC1.1
FB25 FB120-06
VCC1.8
R99 0
FB21 FB120-06
FB26 FB120-06
VDDA18HTPLL
VDDA18PCIEPLL
MC8 2.2U-06
BC8 .1U-04-O
MC10 2.2U-06
MC14 2.2U-06
BC11 .1U-04-O
NB1C
PART 3 OF 6
AVDD1(NC)
AVDD2(NC)
AVDDDI(NC)
AVSSDI(NC)
AVDDQ(NC)
AVSSQ(NC)
C_Pr(DFT_GPIO5)
Y(DFT_GPIO2)
COMP_Pb(DFT_GPIO4)
RED(DFT_GPIO0)
REDb(NC)
GREEN(DFT_GPIO1)
GREENb(NC)
BLUE(DFT_GPIO3)
BLUEb(NC)
DAC_HSYNC(PWM_GPIO4)
DAC_VSYNC(PWM_GPIO6)
DAC_SDA(PCE_TCALRN)
DAC_SCL(PCE_RCALRN)
DAC_RSET(PWM_GPIO1)
CRT/TVOUT
PLLVDD(NC)
PLLVDD18(NC)
PLLVSS(NC)
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
PLL PWR
LVTM
SYSRESETb
POWERGOOD
LDTSTOPb
ALLOW_LDTSTOP
PM
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN(OSCIN)
REFCLK_N(PWM_GPIO3)
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP)
GPPSB_REFCLKN(SB_REFCLKN)
CLOCKs
I2C_DATA
I2C_CLK
DDC_DATA/AUX0P(NC)
DDC_CLK/AUX0N(NC)
AUX1P(NC)
AUX1N(NC)
STRP_DATA
RSVD
AUX_CAL(NC)
MIS.
TXOUT_L0P(NC)
TXOUT_L0N(NC)
TXOUT_L1P(NC)
TXOUT_L1N(NC)
TXOUT_L2P(NC)
TXOUT_L2N(DBG_GPIO0)
TXOUT_L3P(NC)
TXOUT_L3N(DBG_GPIO2)
TXOUT_U0P(NC)
TXOUT_U0N(NC)
TXOUT_U1P(PCIE_RESET_GPIO3)
TXOUT_U1N(PCIE_RESET_GPIO2)
TXOUT_U2P(NC)
TXOUT_U2N(NC)
TXOUT_U3P(PCIE_RESET_GPIO5)
TXOUT_U3N(NC)
TXCLK_LP(DBG_GPIO1)
TXCLK_LN(DBG_GPIO3)
TXCLK_UP(PCIE_RESET_GPIO4)
TXCLK_UN(PCIE_RESET_GPIO1)
VDDLTP18(NC)
VSSLTP18(NC)
VDDLT18_1(NC)
VDDLT18_2(NC)
VDDLT33_1(NC)
VDDLT33_2(NC)
VSSLT1(VSS)
VSSLT2(VSS)
VSSLT3(VSS)
VSSLT4(VSS)
VSSLT5(VSS)
VSSLT6(VSS)
VSSLT7(VSS)
LVDS_DIGON(PCE_TCALRP)
LVDS_BLON(PCE_RCALRP)
LVDS_ENA_BL(PWM_GPIO2)
TMDS_HPD(NC)
HPD(NC)
TVCLKIN(PWM_GPIO5)
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
RS780 A13
TMDS_00P 16
TMDS_00N 16
TMDS_01P 16
TMDS_01N 16
TMDS_02P 16
TMDS_02N 16
TMDS_CLKP 16
TMDS_CLKN 16
TP24
VDDLTP18
C122 2.2U-06
FB18 FB120-06
C119 10U-08
+1.8V_PLL
Q16 2N7002-S
VCC1.8
R119 4.7K-04
+12V
VDDLT18
FB19 FB120-06
VDDLT33
TP1
C123 1U-04
C120 4.7U-08
COMM_EN 15
TMDS_HPD2 16
STP1
TMDS_HPD0 15
TMDS_HPD1 15
SUS_STAT
D8 1N4148-S-O
-A_RST 18,29
Load EEPROM Straps(1,use HW Default)
SUS_STAT 19
R132 1.8K-04
Disable Test Mode
I2C_CLK 16
I2C_DATA 16
NB_RST_1.8V
NB_PWRGD_1.8V
LDSTOP
ALLOW_LDTSTOP_NB
10 NBHTREF_CLKP
10 NBHTREF_CLKN
10 OSC_14M_NB
R123 4.7K-04-O
PWM_GPIO3
ER19 150-1-04
ER17 150-1-04
VCC1.1
10 NBGFX_CLKP
10 NBGFX_CLKN
STP9
STP10
10 NBSLINK_CLKP
10 NBSLINK_CLKN
ATI AP NOTE
15 SDA0_AUX0N
15 SCL0_AUX0P
15 DP_AUX1P
15 DP_AUX1N
R131 10K-04-O
STP2
R115 150-04
AUX_CAL
Note: for RS780, change R677 to 150R as AUX_CAL, place close to pin C8
RS780 connect
16 R
16 G
16 B
12,16 HSYNC
16 VSYNC
16 DAC_SDAT
16 DAC_SCL
ER20 715-1-04
STP6
STP3
STP5
RX740/RS740/RS780 difference table
RS740
RX780
RS780
NB_PWRGD IN
3.3V IN
1.8V IN
1.8V IN
ALLOW_LDTSTOP OUT(default)/IN
OC
OC
OC/3.3V IN *
LDT_STOP# IN(default)/OUT
3.3V IN
1.8V IN
3.3V IN/OC *
SYSTEMRESETb IN
3.3V IN
1.8V IN
3.3V IN
*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input
R107 4.7K-04
R111 4.7K-04
5,18 LDT_STOP-
LDSTOP
QN4 2N3904-S
R102 4.7K-04
R117 4.7K-04
5,18,32 LDT_RST-
NB_RST_1.8V
QN2 2N3904-S
R129 1K-04
NB output is OD pin
18 ALLOW_LDTSTOP
ALLOW_LDTSTOP_NB
Debug Test Bus(1,Disable)
RJ1
VSYNC
10K(2-3)-04-O
RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE
Enables Test debug bus
using PCIE bus
1. Disable (can be enabled
thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
setting only
RS740: Not supported
RS740/RX780/RS780: LOAD_EEPROM_STRAPS
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
RS780: STRAP_PCIE_GPP_CFG[2:0]
(configure thru register setting)
1-1-1-1-1-1 Mode L default
1-1-1-1-1-1 Mode L
2-0-2-0-2-0 Mode C2
2-0-2-0-1-1 Mode K
2-0-1-1-1-1 Mode E
1-1-1-1-1-1 Mode L
4-0-0-0-1-1 Mode C
4-0-0-0-2-0 Mode B
Elitegroup Computer Systems
Title
RS780 SYSTEM I/F
Size Custom
Document Number
RS780M-A2
Rev 1.0
Date: Tuesday, October 21, 2008
Sheet 13 of 39

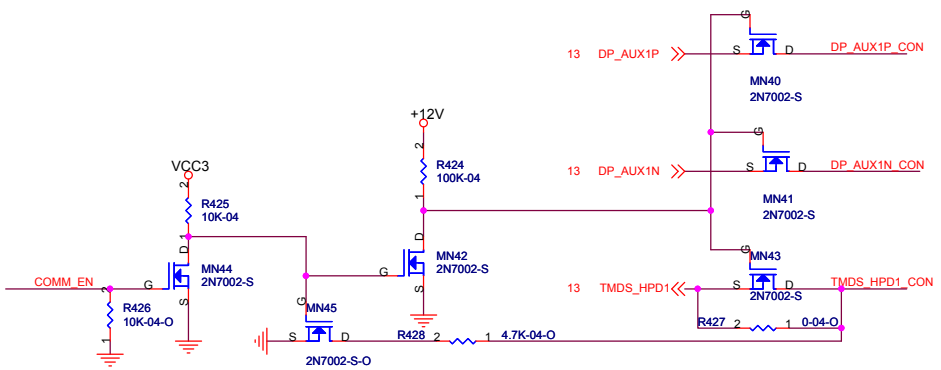


Elitegroup Computer Systems			
Title: RX780 POWER			
Size: Custom	Document Number: RS780M-A2		Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 14 of 39		





SWITCH CIRCUIT FOR SECONDARY DISPLAYPORT



Elitegroup Computer Systems		
Title: PCI-E X16 CONN&PCIE*8CONN		
Size: Custom	Document Number: RS780M-A2	Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 15 of 39	

External Connection

12,13 HSYNC
13 VSYNC
13 R
13 G
13 B
13 DAC_SDAT
13 DAC_SCL

HSYNC
VSYNC
R
G
B
DAC_SDAT
DAC_SCL

MGREEN
MBLUE
U4
AZC099-04S-O
VCC
MRED
C78 .1U-04

Close to Connector

HSYNC
R78 0-04-O
H_SYNC
U8
74LVC32-5-S
H_SYNC

VSYNC
R54 0-04-O
V_SYNC
U5
74LVC32-5-S
V_SYNC

R789
0-08-O
FOR EMI

VCC
BC110 .1U-04
BC105 .1U-04
BC106 .1U-04

VGA
MRED
MGREEN
MBLUE
CONN-15P3R-VGA

SDATV
H_SYNC R68 22-04
V_SYNC R55 22-04
SCLKV
VGA_HSYNC
VGA_VSYNC
C79 22P-VP-O
C96 22P-VP-O
C77 68P
C94 68P

ER13 140-1-04
ER14 150-1-04
ER15 150-1-04
EMI 6dB
0321 rev:1.0
R
G
B
L2 0
L4 0
L6 0
L3 FB30-06
L5 FB30-06
L7 FB30-06
MRED
MGREEN
MBLUE
C74 10P-04
C93 10P-04
C105 10P-04
C108 10P-04
C95 10P-04
C90 10P-04
C106 10P-04
C101 10P-04
C92 10P-04

13 DAC_SDAT
R56 6.8K-04
SDATV

13 DAC_SCL
R79 6.8K-04
SCLKV

VCC3
BC7 .1U-04-O
VCC5
BC6 4.7U-08

SDATV
VGA_VSYNC
U6
AZC099-04S-O
VGA_HSYNC
SCLKV
C102 .1U-04-O

Close to Connector

13 TMDS_02P
13 TMDS_02N
13 TMDS_01P
13 TMDS_01N
HDMI_TXD2P
HDMI_TXD2N
HDMI_TXD1P
HDMI_TXD1N
CMF6 0-8P4R
HDMI_TXD2P_HD
HDMI_TXD2N_HD
HDMI_TXD1P_HD
HDMI_TXD1N_HD

13 TMDS_00P
13 TMDS_00N
13 TMDS_CLKP
13 TMDS_CLKN
HDMI_TXD0P
HDMI_TXD0N
HDMI_TXC0P
HDMI_TXC0N
CMF7 0-8P4R
HDMI_TXD0P_HD
HDMI_TXD0N_HD
HDMI_TXC0P_HD
HDMI_TXC0N_HD

HDMI
HDMI_TXD2P_HD
HDMI_TXD2N_HD
HDMI_TXD1P_HD
HDMI_TXD1N_HD
HDMI_TXD0P_HD
HDMI_TXD0N_HD
HDMI_TXC0P_HD
HDMI_TXC0N_HD
CLK_HDMI
DATA_HDMI
VCC_HDMI
HPLG_HDMI
GND#20
GND#21
GND#22
GND#23
HDMI-19SMD

USBVCC_5
USB
USBP8-
USBP8+
USBP9-
USBP9+
VCC1
-DATA0
+DATA0
GND1
HOLE2
HOLE3
VCC
-DATA1
+DATA1
GND
HOLE
HOLE1
G1
G2
G3
G4
USBX2
AUGND2
AUGND2

VCC
BC107 .1U-04-O
BC108 .1U-04-O
VCC3
VCC3
EMI

Schematic just only for reference!
Please see its reference design guide.

VCC_DDC
VCC
F11
FUSE-1.1A-18
FB46
FB600P-08
VCC_HDMI
C103 .1U-04
FOR EMI

VCC_DDC
R457 2.2K-04
R458 2.2K-04
13 I2C_CLK
13 I2C_DATA
FB47
FB48
FB120-06-B
FB120-06-B
CLK_HDMI
DATA_HDMI

19 USB_P8+
19 USB_P8-
19 USB_P9+
19 USB_P9-
RN43 0-8P4R
USBP8+
USBP8-
USBP9+
USBP9-
U35
AZC099-04S-O
AUGND2

Hot Plug Detect 3

VCC3
2N3904-S
QN24
R712 10K-04
HPLG_HDMI
13 TMDS_HPD2
R713 10K-04

R717
0-08-O
R718
0-08-O
FOR HDMI EMI

Elitegroup Computer Systems

Title: **VGA/HDMI**

Size: Custom
Document Number: **RS780M-A2**
Rev: **1.0**
Date: Tuesday, October 21, 2008
Sheet 16 of 39

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

Follow ATI A.P Note

SB700A11

SB700A12

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

SB1C SB700 Part 3 of 5

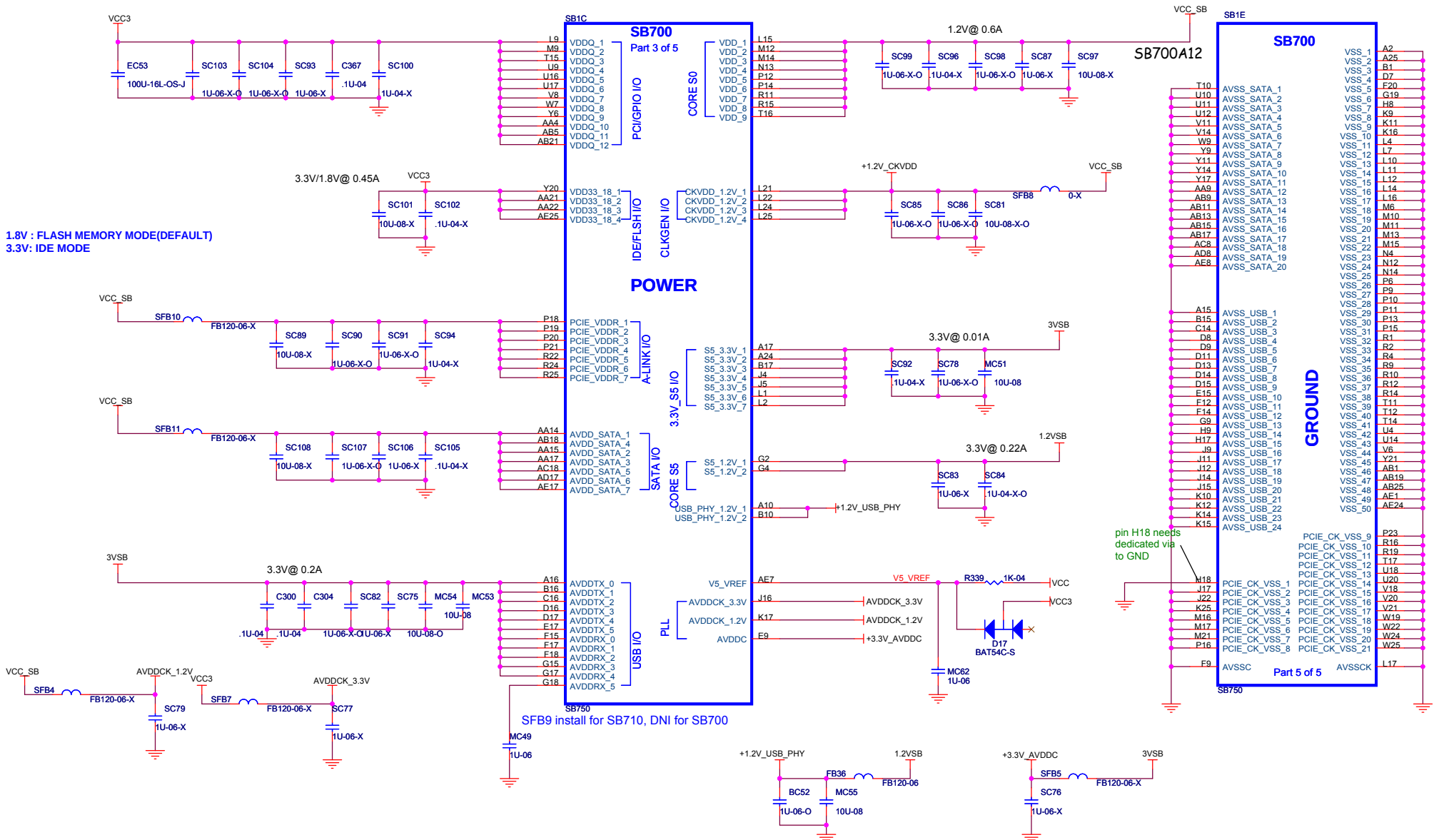
SB1E SB700 Part 5 of 5

POWER

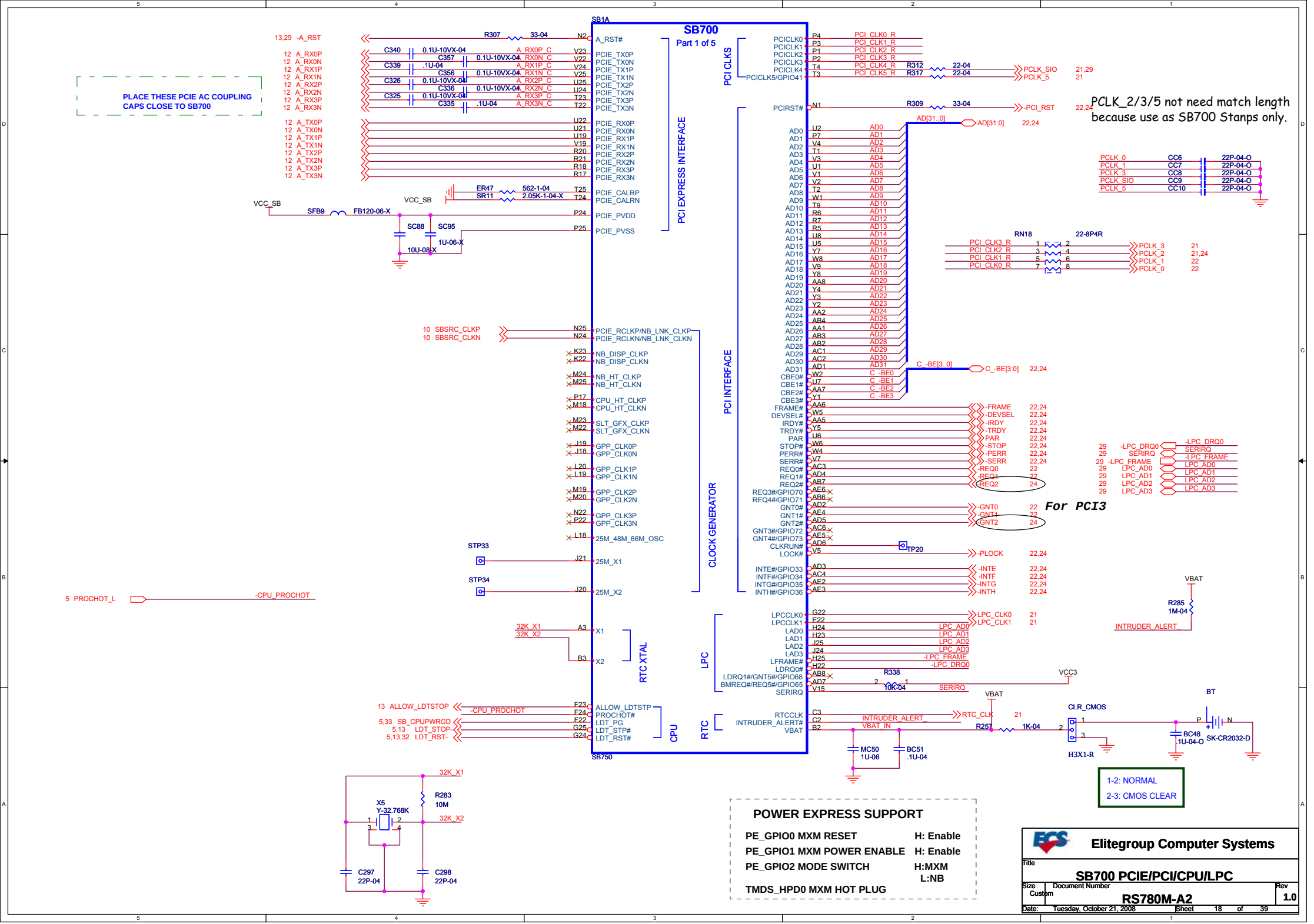
GROUND

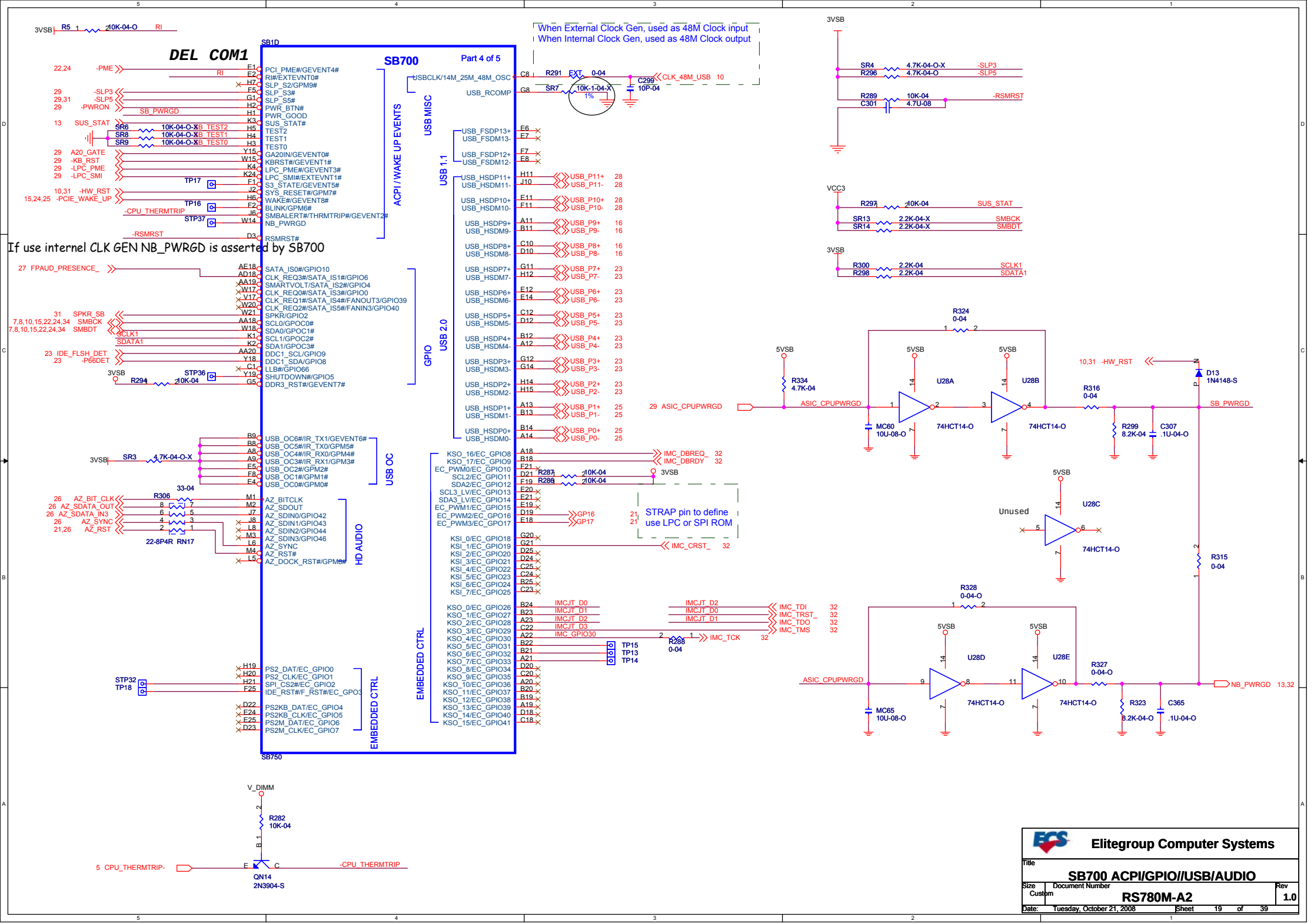
SFB9 install for SB710, DNI for SB700

pin H18 needs dedicated via to GND



Elitegroup Computer Systems			
Title: SB700 PWR/DECOUPLING			
Size: Custom	Document Number: RS780M-A2		Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 17 of 39		


SB1A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB750
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB700
PCLK_2/3/5 not need match length because use as SB700 Stanps only.
For PCI3
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH H:MXM L:NB
TMDS_HPD0 MXM HOT PLUG
1-2: NORMAL
2-3: CMOS CLEAR
Elitegroup Computer Systems
SB700 PCIE/PCI/CPU/LPC
RS780M-A2
Tuesday, October 21, 2008


DEL COM1
SB1D
SB700
Part 4 of 5
When External Clock Gen, used as 48M Clock input
When Internal Clock Gen, used as 48M Clock output
If use internel CLK GEN NB_PWRGD is asserted by SB700
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
EMBEDDED CTRL
STRAP pin to define use LPC or SPI ROM
Unused
SB750
Elitegroup Computer Systems
SB700 ACPI/GPIO//USB/AUDIO
RS780M-A2
Tuesday, October 21, 2008

Note: Do we still keep mobile SATA connector?
Is there any side affect to test RAID mode?

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
SR2 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

SB1B

SB700
Part 2 of 5

SB750

SERIAL ATA

SATA_TX0+ AD9
SATA_TX0- AE9
SATA_RX0- AB10
SATA_RX0+ AC10
SATA_TX1+ AE10
SATA_TX1- AD10
SATA_RX1- AD11
SATA_RX1+ AE11
SATA_TX2+ AB12
SATA_TX2- AC12
SATA_RX2- AE12
SATA_RX2+ AD12
SATA_TX3+ AD13
SATA_TX3- AE13
SATA_RX3- AB14
SATA_RX3+ AC14
SATA_TX4+ AE14
SATA_TX4- AD14
SATA_RX4- AD15
SATA_RX4+ AE15
SATA_TX5+ AB16
SATA_TX5- AC16
SATA_RX5- AE16
SATA_RX5+ AD16

SR12 1K-1-04-X SATA_CAL V12
SATA_CAL
SATA_X1 Y12
SATA_X1
SATA_X2 AA12
SATA_X2
23 -SATA_LED W11
SATA_ACT#/GPIO67

SATA PWR

PLLVDD_ATA AA11
PLLVDD_SATA_1
XTLVDD_ATA W12
XTLVDD_SATA

ATA 66/100/133

IDE_IORDY AA24 PIDE_RDY 23
IDE_IRQ AA25 PIDE_IRQ 23
IDE_A0 Y22 PIDE_A0 23
IDE_A1 AB23 PIDE_A1 23
IDE_A2 Y23 PIDE_A2 23
IDE_DACK# AB24 -PIDE_DAK 23
IDE_DRQ AD25 PIDE_DRQ 23
IDE_IOR# AC25 -PIDE_IOR 23
IDE_IOW# AC24 -PIDE_IOW 23
IDE_CS1# Y25 -PIDE_CS1 23
IDE_CS3# Y24 -PIDE_CS3 23

IDE_D0/GPIO15 AD24 IDE_D0
IDE_D1/GPIO16 AD23 IDE_D1
IDE_D2/GPIO17 AE22 IDE_D2
IDE_D3/GPIO18 AC22 IDE_D3
IDE_D4/GPIO19 AD21 IDE_D4
IDE_D5/GPIO20 AE20 IDE_D5
IDE_D6/GPIO21 AB20 IDE_D6
IDE_D7/GPIO22 AD19 IDE_D7
IDE_D8/GPIO23 AE19 IDE_D8
IDE_D9/GPIO24 AC20 IDE_D9
IDE_D10/GPIO25 AD20 IDE_D10
IDE_D11/GPIO26 AE21 IDE_D11
IDE_D12/GPIO27 AB22 IDE_D12
IDE_D13/GPIO28 AD22 IDE_D13
IDE_D14/GPIO29 AE23 IDE_D14
IDE_D15/GPIO30 AC23 IDE_D15
IDE_D[15..0] PIDE_D[15..0] 23

SPI ROM

SPI_DI/GPIO12 G6 SPI_DO
SPI_DO/GPIO11 D2 SPI_DI
SPI_CLK/GPIO47 D1 SPI_CLK
SPI_HOLD#/GPIO31 F4 SPI_HOLD
SPI_CS#/GPIO32 F3 SPI_CS

LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1
STP35
TP19

HW MONITOR

FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7
FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8
TEMP_COMM C6
TEMPIN0/GPIO61 B6
TEMPIN1/GPIO62 A6
TEMPIN2/GPIO63 A5
TEMPIN3/TALERT#/GPIO64 B5
VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7

VCC3
R290
10K-04
-THRM 29

HWM_AGND TRACE AT LEAST 10MIL WIDE

AVDD_HWM
3VSB
AVDD F6
SFB6 0-X
AVSS G7
SC80 1U-06-X-O

10P-04 C368 SATA_X1
X6
X-25M
R337 10M-04
10P-04 C369 SATA_X2

VCC_SB PLLVDD_ATA
FB38 FB120-06
MC63 1U-06
MC64 1U-06-O
CAP CLOSE TO THE BALL OF U600

VCC3 XTLVDD_ATA
FB37 FB120-06
MC61 1U-06
CAP CLOSE TO THE BALL OF U600

SATA1 SATA_TX0+ SATA_TX0- SATA_RX0- SATA_RX0+ SATA-7P2R-OR
SATA2 SATA_TX1+ SATA_TX1- SATA_RX1- SATA_RX1+ SATA-7P2R-OR
SATA3 SATA_TX2+ SATA_TX2- SATA_RX2- SATA_RX2+ SATA-7P2R-OR
SATA4 SATA_TX3+ SATA_TX3- SATA_RX3- SATA_RX3+ SATA-7P2R-OR
SATA5 SATA_TX4+ SATA_TX4- SATA_RX4- SATA_RX4+ SATA-7P2R-OR
SATA6 SATA_TX5+ SATA_TX5- SATA_RX5- SATA_RX5+ SATA-7P2R-OR

SO8 MN and MW co-layout layout draw

150 mil

208 mil 3VSB
D16 BAT54C-S-O
R329 0-04

SPI_DEBUG
SPI_CS SPI_DO -WP_ROM
29 -WP_ROM
VCC3_DUAL_SPI SPI_HOLD SPI_CLK SPI_DI
H4X2-B

VCC3 VCC3
R401 4.7K-04-O
R402 4.7K-04
-WP_ROM1 -WP_ROM -WP_ROM 29
BIOS_WP H3X1-R-O

BIOSWP	BIOS PROTECT
1-2	DISABLE
2-3	ENABLE

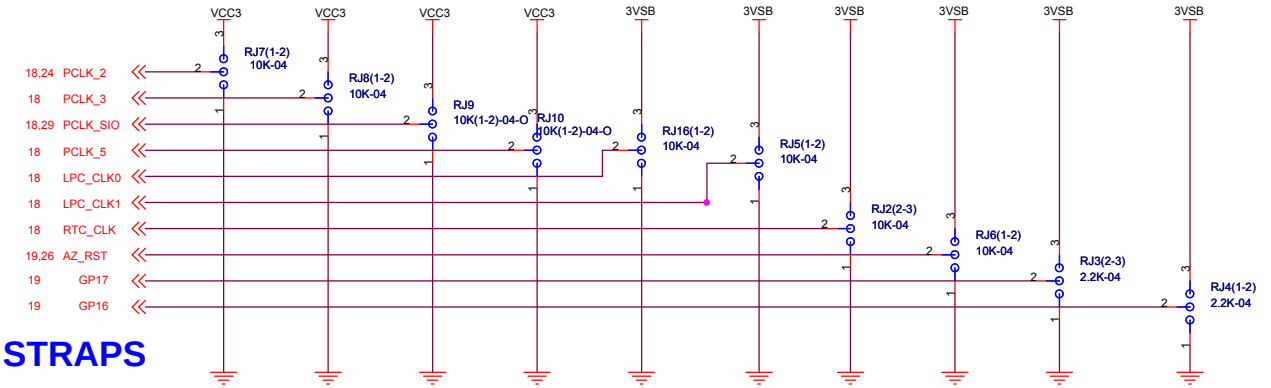
VCC3_DUAL_SPI
R331 1K-04-O
ROM2 **SMT**
SPI_CS SPI_DO -WP_ROM
CE# SO WP# GND VCC HOLD# SCK SI
SPI_HOLD SPI_CLK SPI_DI
R332 10K-04
R333 0-04-O SPI_HOLD
SPI-ROM-D-4M-O
01-530-004110

Co-lay
for SPI ROM

208mil width
ROM1 **DIP**
SPI_CS SPI_DO -WP_ROM
CE# SO WP# GND VCC HOLD# SCK SI
SPI_HOLD SPI_CLK SPI_DI
VCC3_DUAL_SPI
BC61 .1U-04
SPI-8D

Elitegroup Computer Systems	
Title	SB700 SATA/IDE/HWM/SPI
Size: Custom	Document Number: RS780M-A2
Rev	1.0
Date: Tuesday, October 21, 2008	Sheet 20 of 39

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT L, H = LPC ROM L, L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

Del PCIE Debug EEPROM Strap

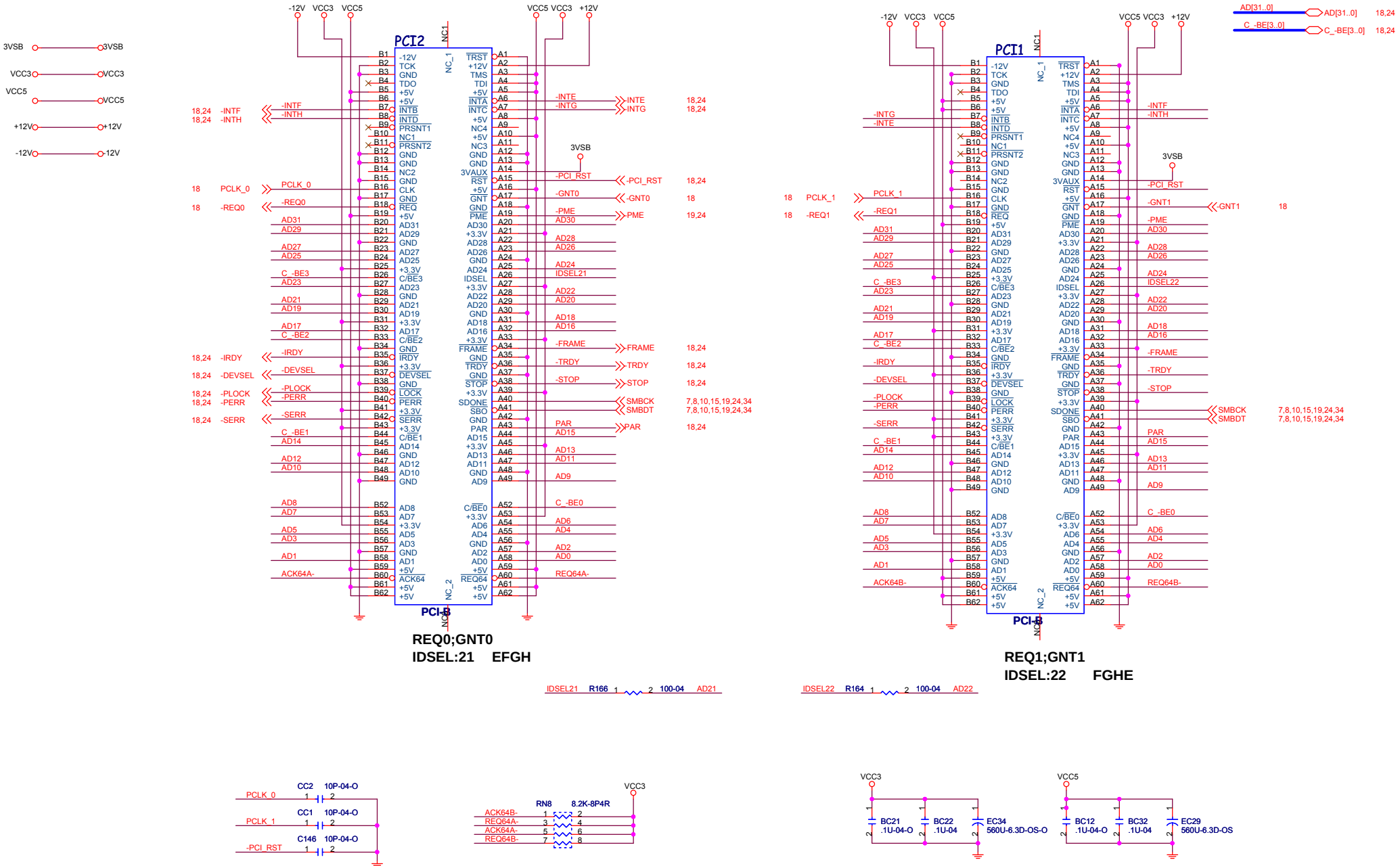
Del Debug straps 070423

Elitegroup Computer Systems

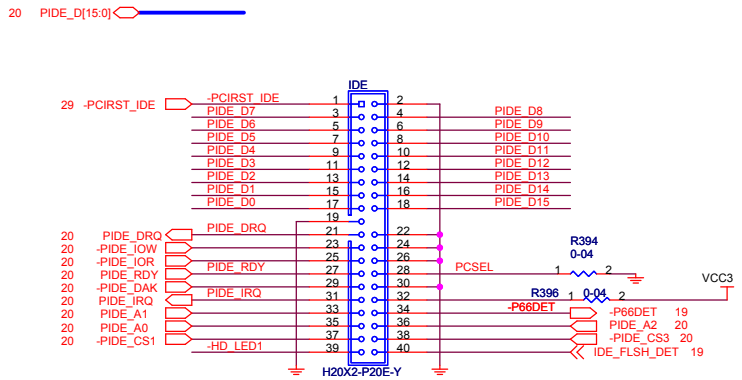
Title: SB700 Straps

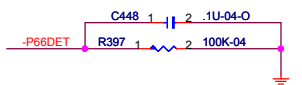
Size: Custom | Document Number: RS780M-A2 | Rev: 1.0

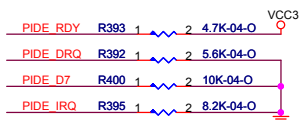
Date: Tuesday, October 21, 2008 | Sheet 21 of 39

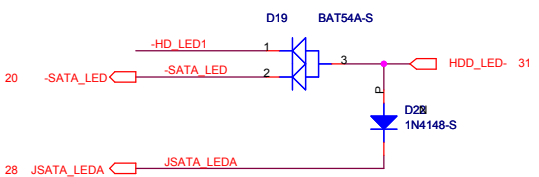


Elitegroup Computer Systems		
Title	PCI1&2	
Size: Custom	Document Number: RS780M-A2	Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 22 of 39	

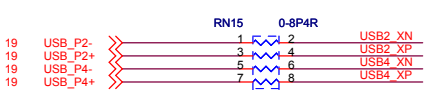


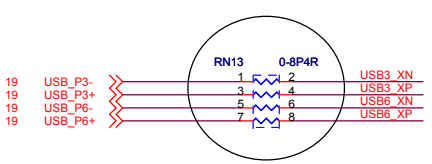


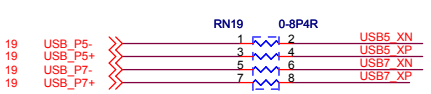


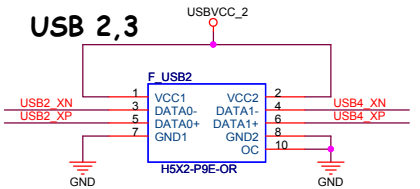


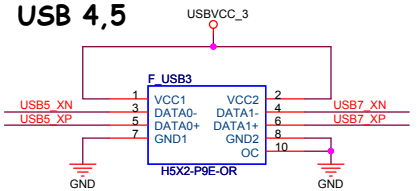
change to bat54a for space 6/8

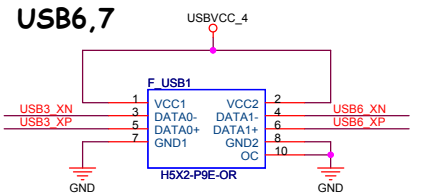


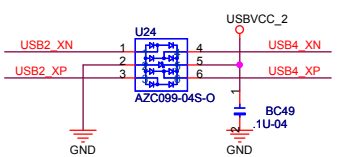


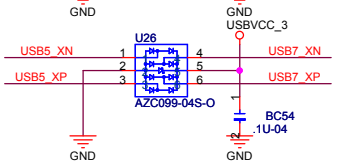


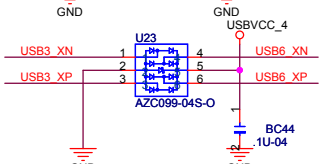


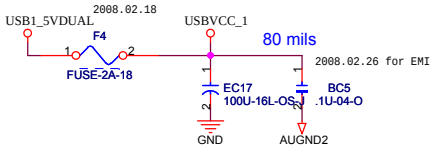


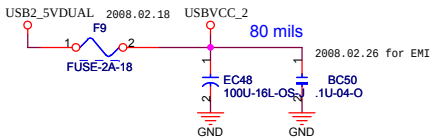


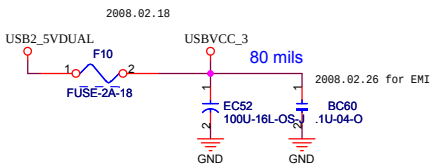


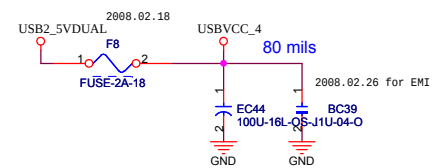


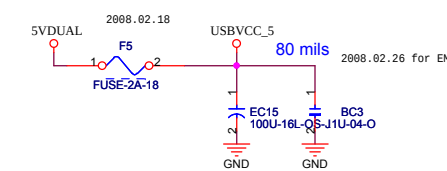


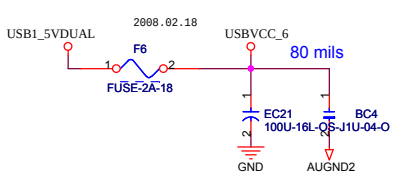








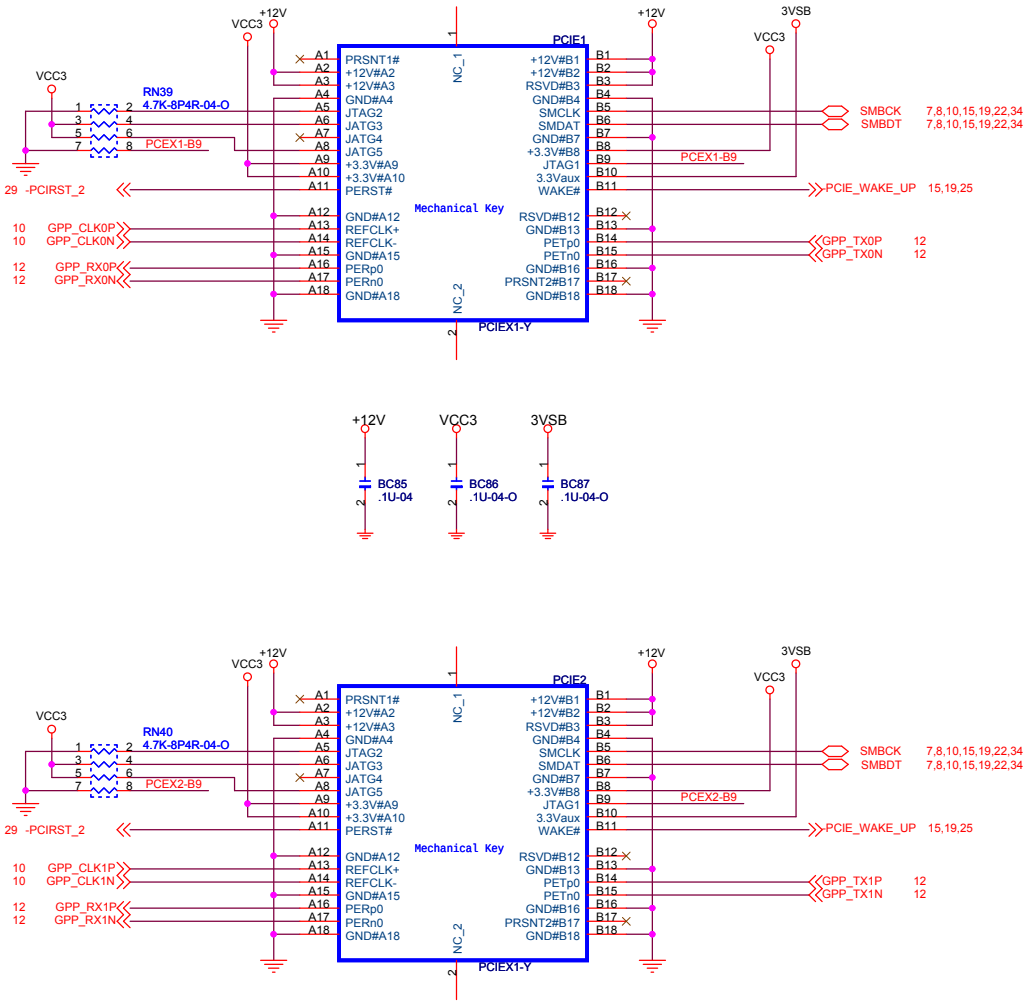




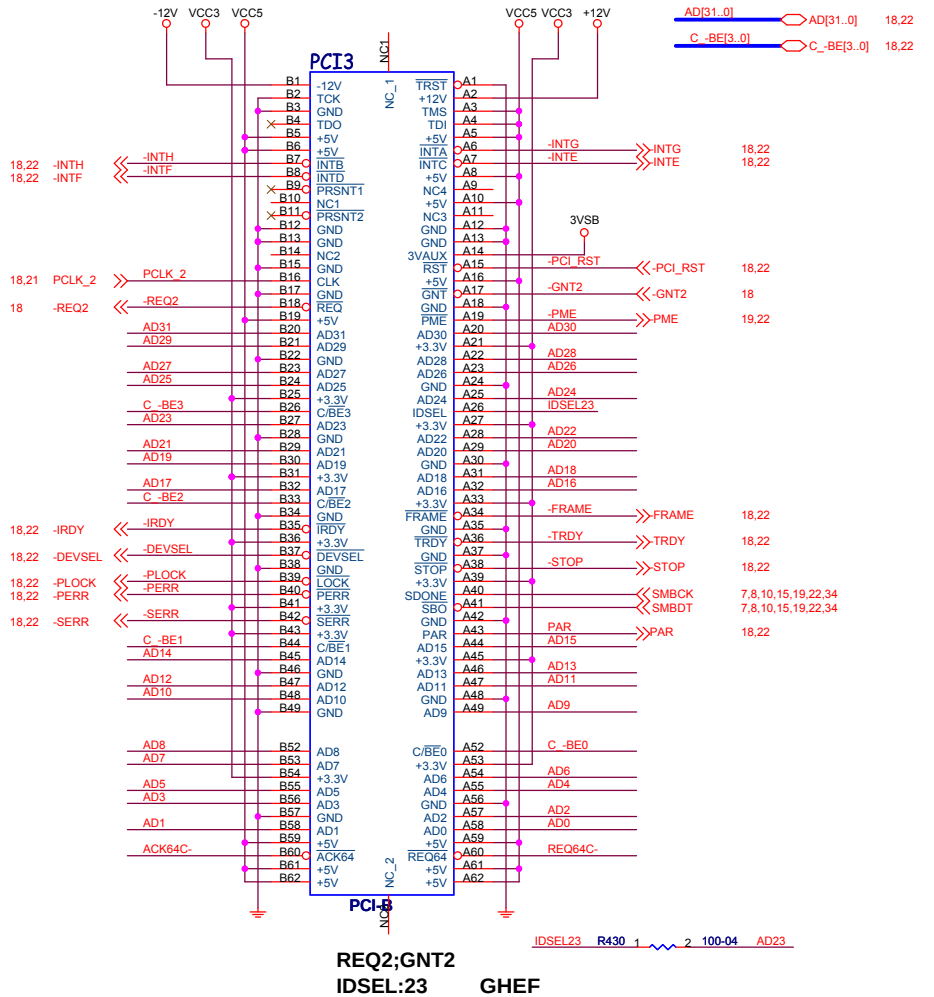
Elitegroup Computer Systems

Title	USB&IDE	
Size: Custom	Document Number: RS780M-A2	Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 23 of 39	

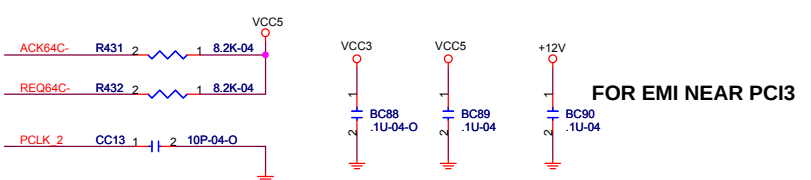
PCI-E x1 SLOT



PCI SLOT



REQ2;GNT2
IDSEL:23 GHEF

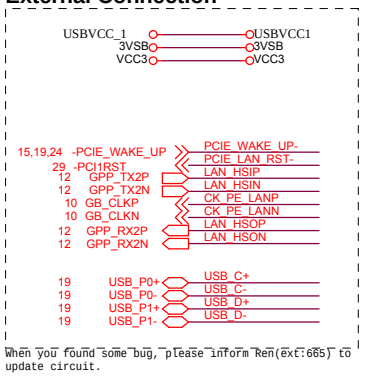


FOR EMI NEAR PCI3

Elitegroup Computer Systems

Title	PCI-E x1(2 SLOTS)	
Size: Custom	Document Number: RS780M-A2	Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 24 of 39	

External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.

新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端

LAN_HSIP/N請接到SB的PCIE TX端

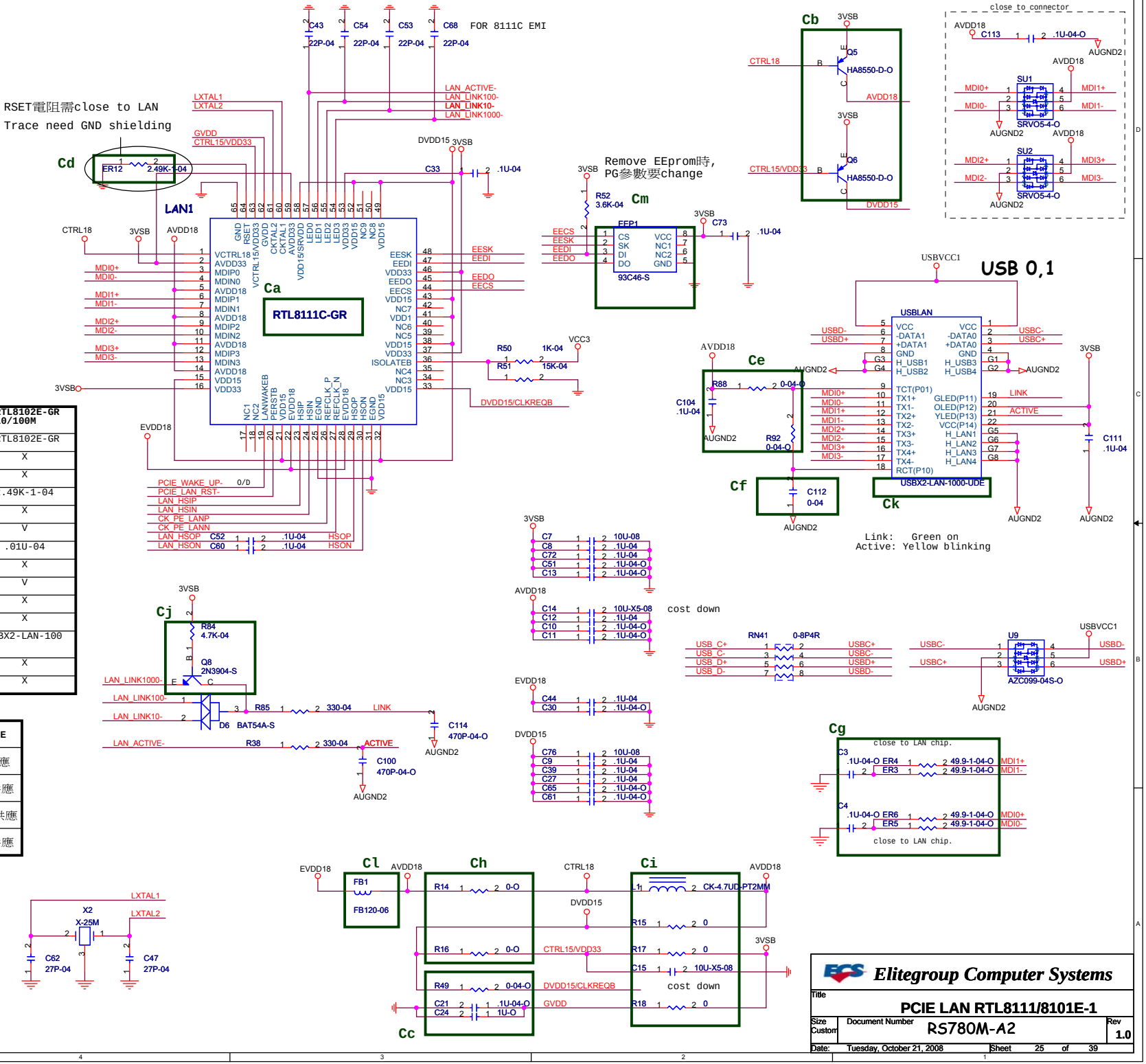
LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

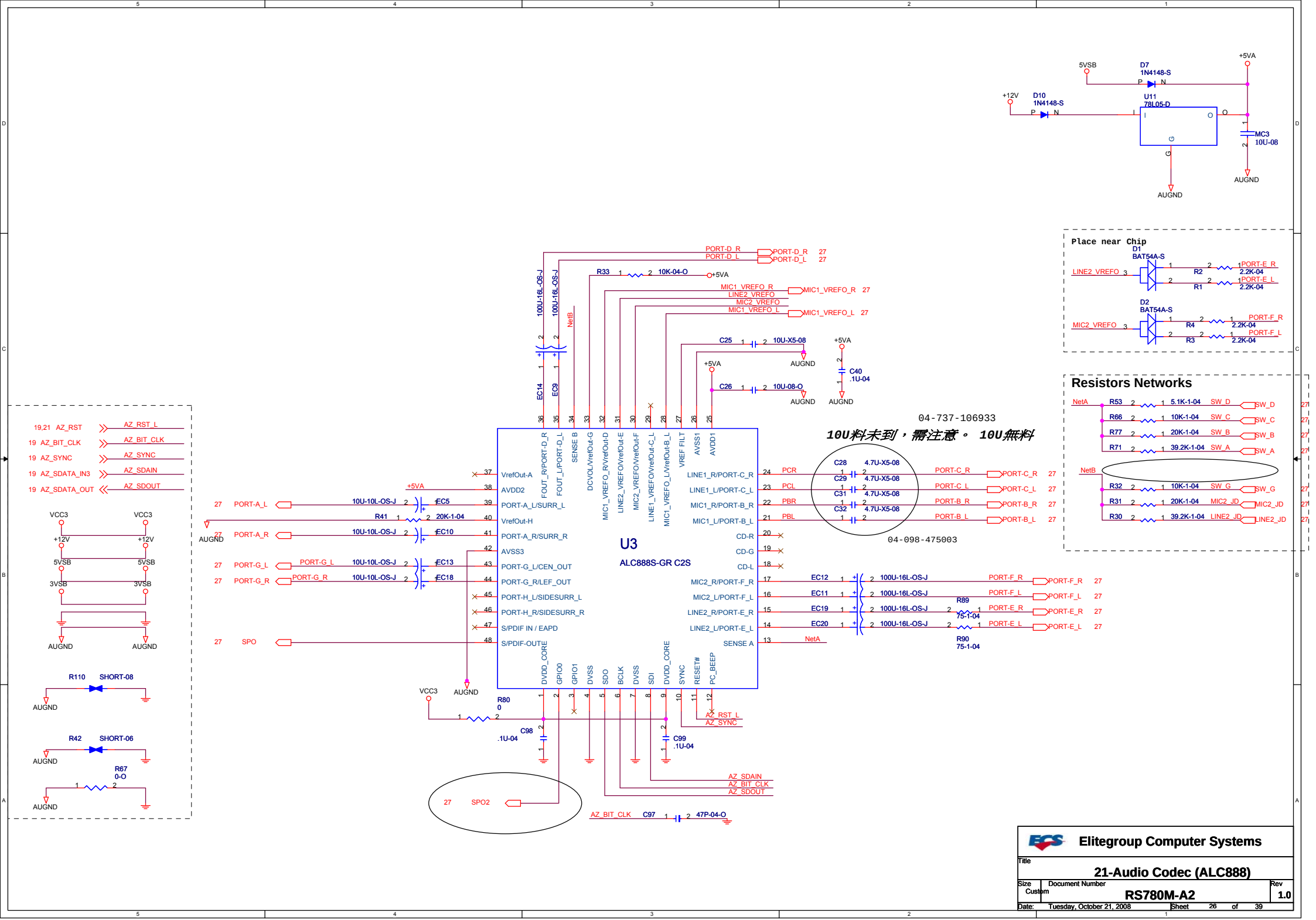
BOM Difference

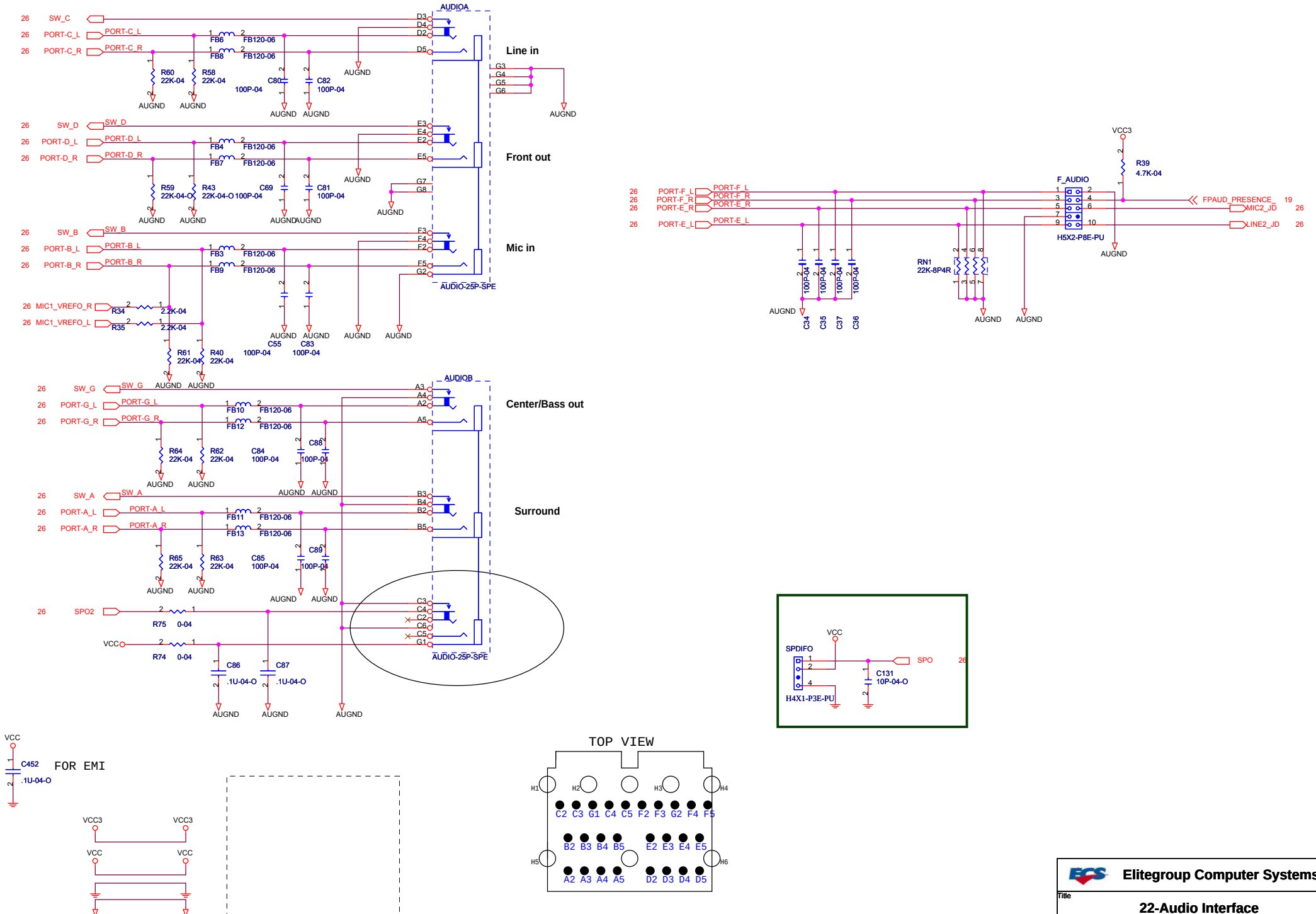
	RTL8101E-GR 10/100M	RTL8111B-GR 1000M	RTL8111C-GR 1000M	RTL8111D-GR 1000M	RTL8102E-GR 10/100M
Ca	RTL8101E-GR	RTL8111B-GR	RTL8111C-GR	RTL8111D-GR	RTL8102E-GR
Cb	X	V	X	X	X
Cc	V	V	X	X	X
Cd	2K-1-04	2.49K-1-04	2.49K-1-04	2.49K-1-04	2.49K-1-04
Ce1	V	X	X	X	X
Ce2	V	X	X	X	V
Cf	.01U-04	0-04	0-04	0-04	.01U-04
Cg	V	X	X	X	X
Ch	V	X	X	X	V
Ci	X	X	V	V	X
Cj	X	V	V	V	X
Ck	USBX2-LAN-100 symmetric	USBX2-LAN-1000			USBX2-LAN-100
Cl	0	0	0	0	X
Cm	V	V	V	X	X

Power Difference

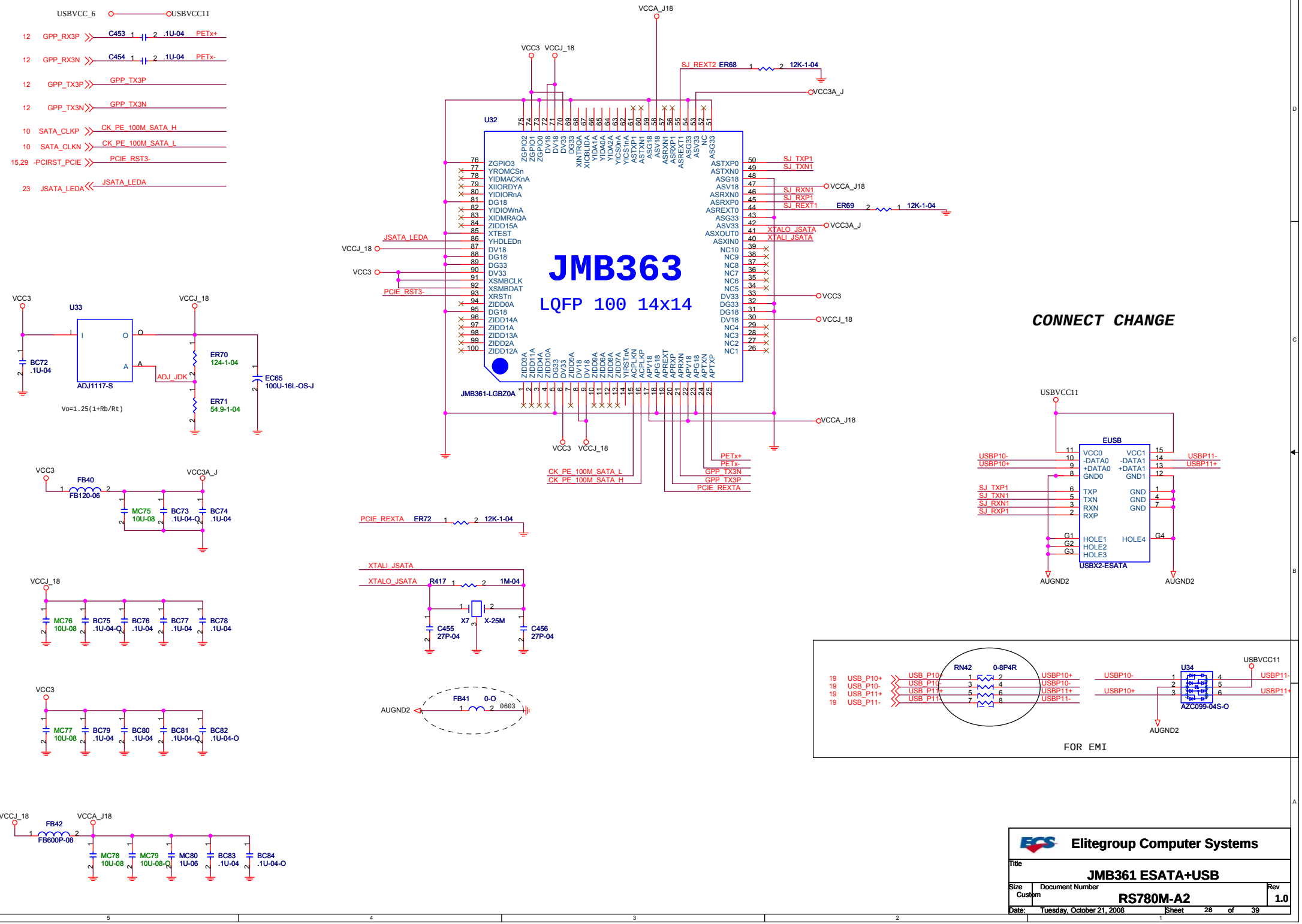
	RTL8101E	RTL8111B	RTL8111C/D	RTL8102E
AVDD33	3.3V 3VSB供應	3.3V 3VSB供應	3.3V 3VSB供應	3.3V 3VSB供應
AVDD18	1.8V CTRL18供應	1.8V 3VSB轉BJT供應	1.2V CTRL18供應	1.2V CTRL18供應
EVDD18	1.8V CTRL18供應	1.8V 3VSB轉BJT供應	1.2V CTRL18供應	1.2V pinself 供應
DVDD15	1.5V CTRL15供應	1.5V 3VSB轉BJT供應	1.2V CTRL18供應	1.2V CTRL15供應




U3
ALC888S-GR C2S
04-737-106933
10U料未到，需注意。 10U無料
04-098-475003
Place near Chip
Resistors Networks
Elitegroup Computer Systems
21-Audio Codec (ALC888)
RS780M-A2
Tuesday, October 21, 2008



Elitegroup Computer Systems			
Title: 22-Audio Interface			
Size: Custom	Document Number: RS780M-A2		Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 27 of 39		



Elitegroup Computer Systems			
Title: JMB361 ESATA+USB			
Size: Custom	Document Number: RS780M-A2		Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 28 of 39		

del 5VSB and NBPWM control GPIO 6/8

External Connection

change from pin85 to here
for non standby GPIO 5/15

change to reset
chip:gigalan/1394 5/8

ADD NBFAN

If you found anything wrong with this circuit,please contact with Jack Hu (Ext:622)

9/12

Wired with pin91

IT8726F-S/FX

For COM2 co-lay

HW STRAPPING

pin121	JP1	Flashseg1_EN	0:Enable
pin122	JP2	SerFlh_SO_SEL	0:FLH_SO1
pin124	JP3	CHIP_SEL	CHIP_SEL
pin1	JP4	BUF_SEL	1:PCIRST# O.D.
p2/46	JP5/7	FAN_CTL_SEL	
pin5	JP6	VID_ISEL	
pin46	JP7	WDT_EN	
pin38	JP8	VIDO_EN	

RS75232 internal pull high.

chang jp1 pull high 8/3

A20_GATE : Pull low for PWM
Value=25% just after power-on

FDD

FDD signals : RDATA#, INDEX#, TRAK0#, DSKCHG#, WP# is input pin.

Key pin (No through hole)

H17X2-P5E-B

Thermal Monitor

add for K8 sequence 6/8

* HM_VIN0 for VCORE
* HM_VIN1 for VCC
* HM_VIN6 for V_DIMM

HM_VIN3 for ATX PWRGD
HM_VIN2 for VCC3
HM_VIN4 for VLDT 1.2V I/P
HM_VIN5 for -12V

BIOS SELECTION

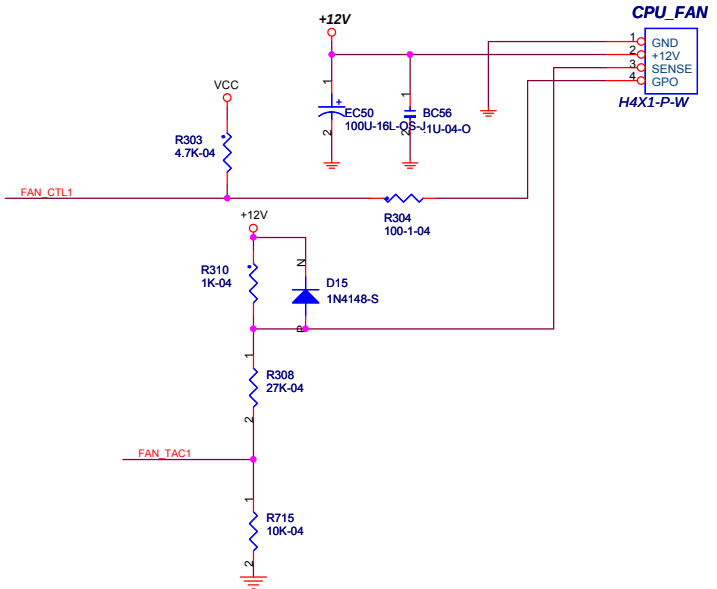
BYPASS CAP

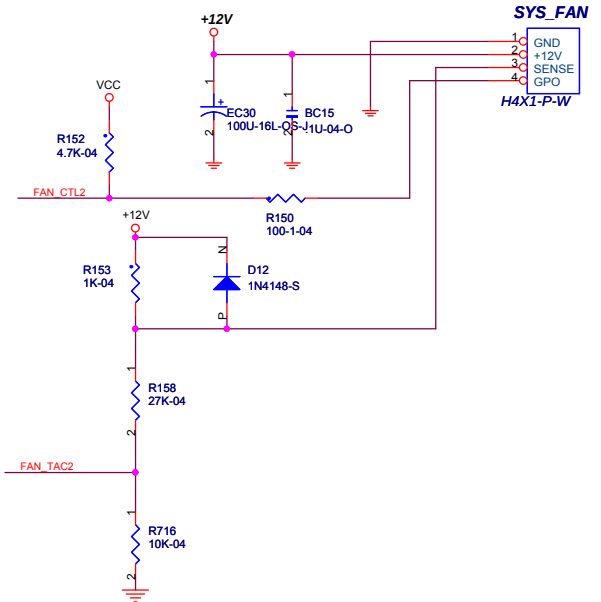
CLOSE TO PIN67

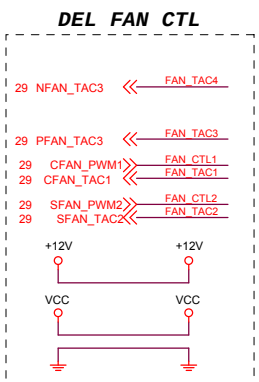
CLOSE TO PIN69

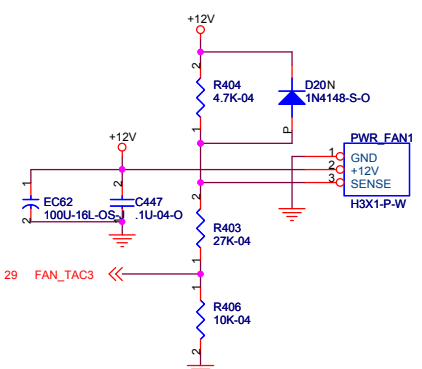
Elitegroup Computer Systems

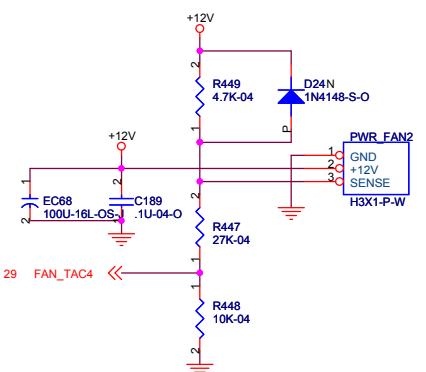
Title	IT8726	
Size: Custom	Document Number: RS780M-A2	Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 29 of 39	









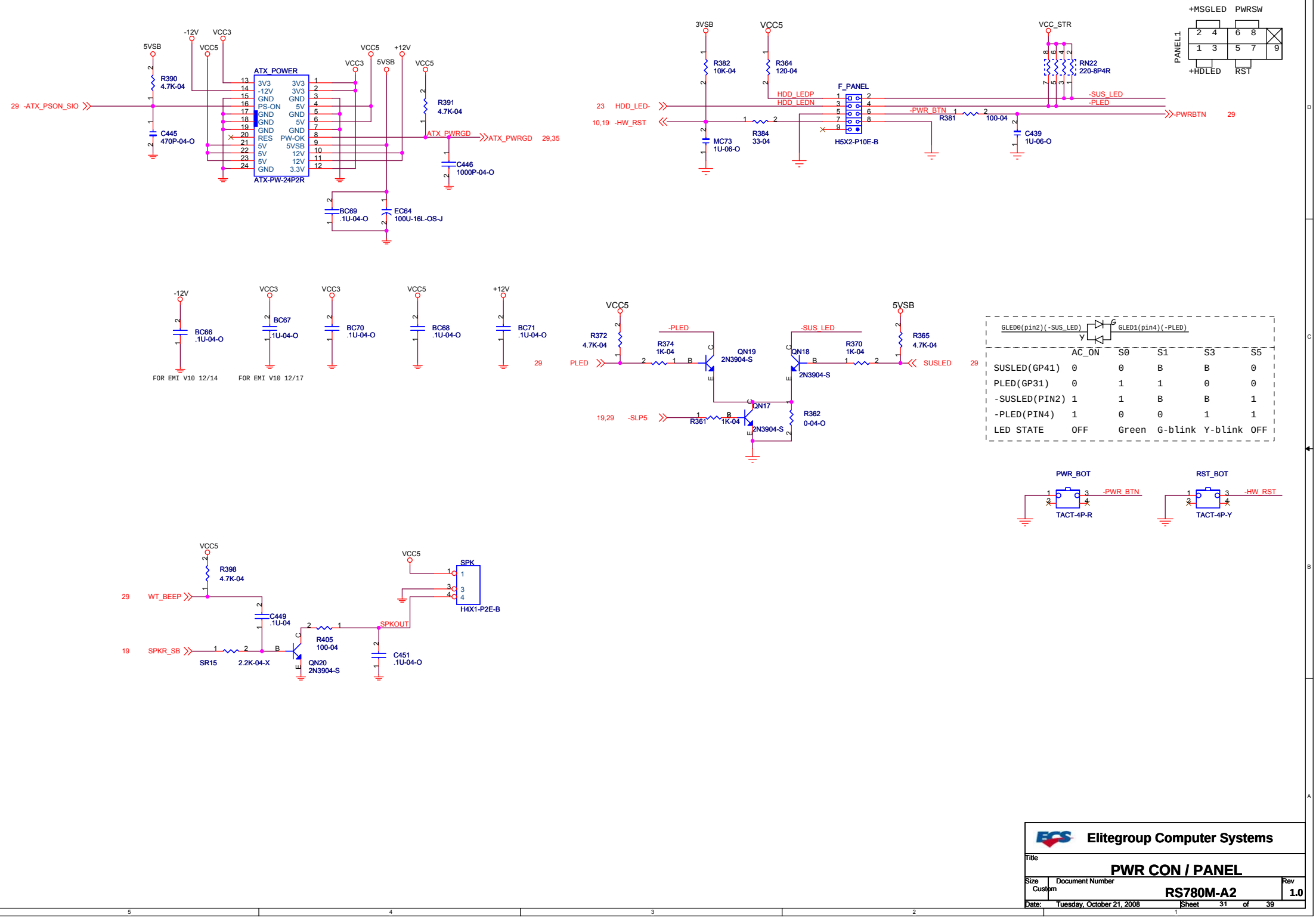


Elitegroup Computer Systems

Title: H/W MONITOR

Size	Document Number	Rev
Custom	RS780M-A2	1.0

Date: Tuesday, October 21, 2008 Sheet 30 of 39

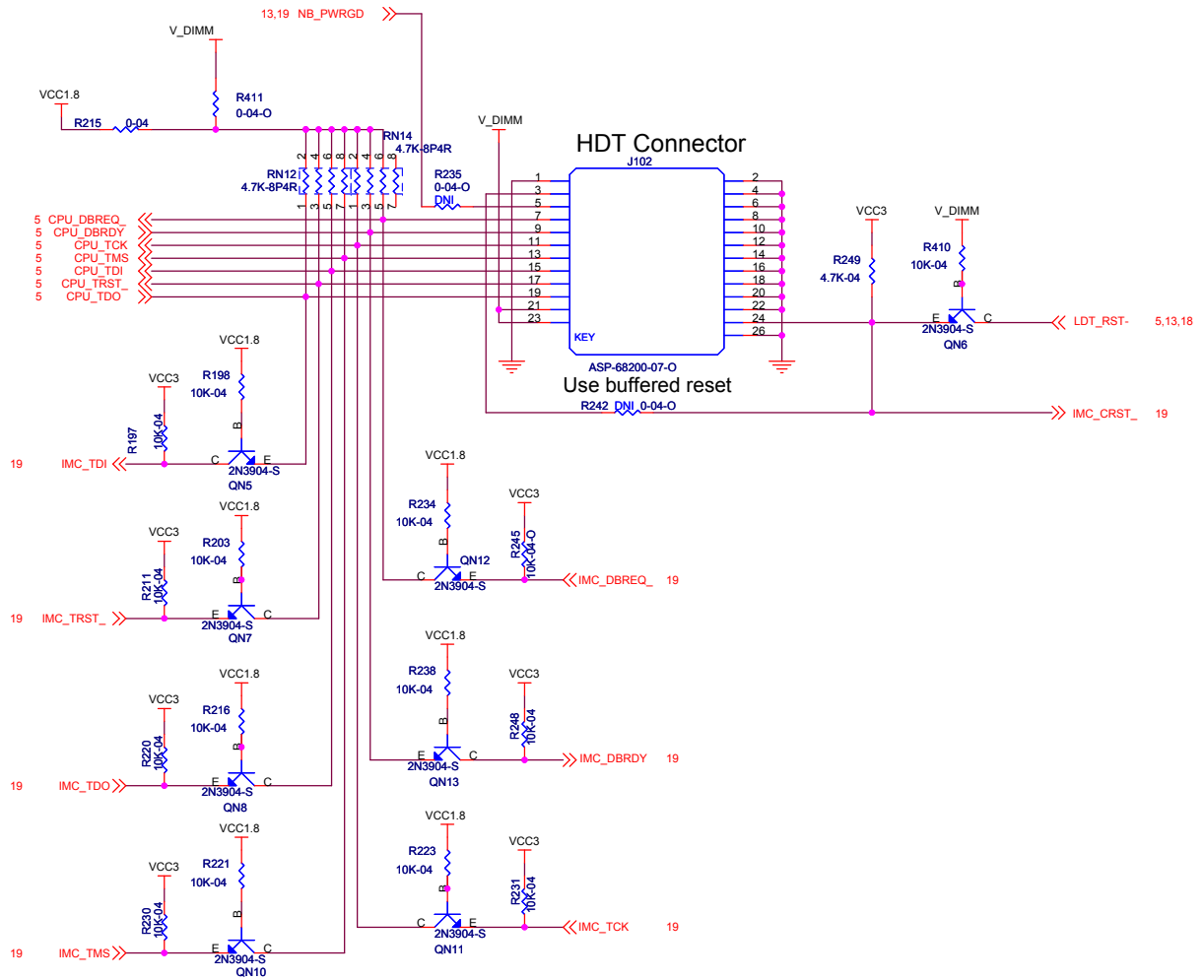


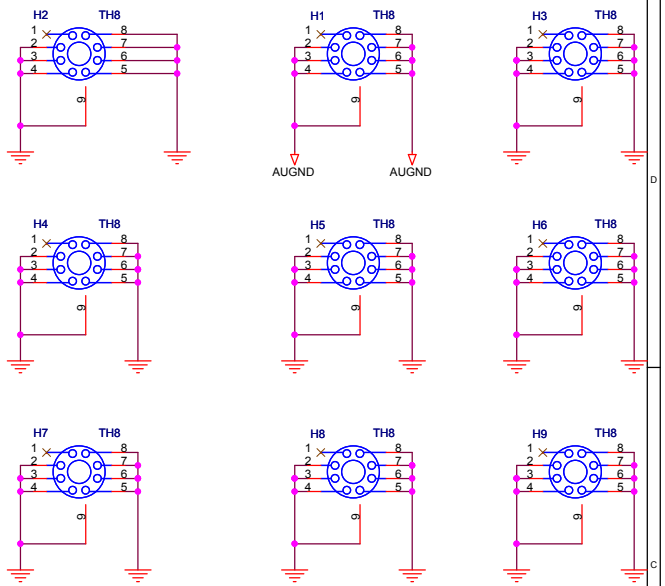
Elitegroup Computer Systems

Title: PWR CON / PANEL

Size: Custom | Document Number: RS780M-A2 | Rev: 1.0

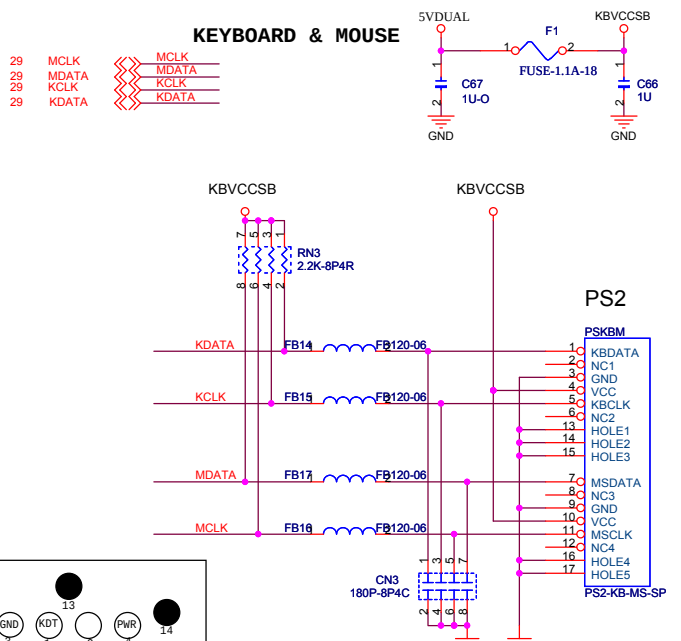
Date: Tuesday, October 21, 2008 | Sheet 31 of 39

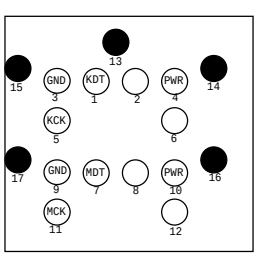




IR

KEYBOARD & MOUSE





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Title: OVER CLOCK/PS2

Size: Custom | Document Number: RS780M-A2 | Rev: 1.0

Date: Tuesday, October 21, 2008 | Sheet 32 of 39

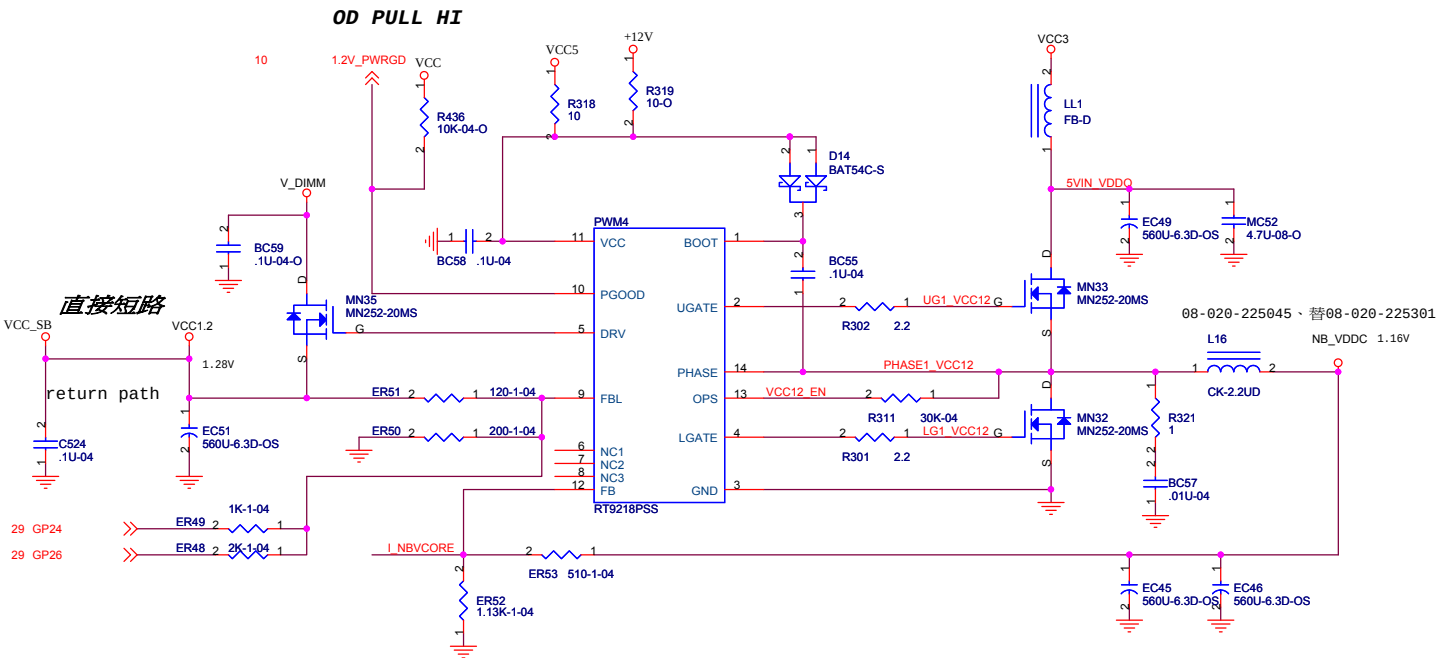
C138,C133,C146,C152 use 0.1uF/X7R
C123,C122,C130,C61 use 0.1uF/X7R
MC2,MC1,MC3,MC11 install

BOTTOM PAD
CONNECT TO GND
Through 8 VIAs

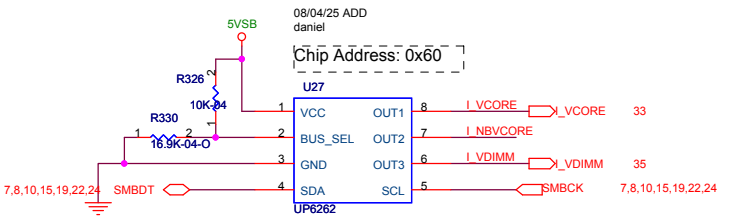
FOR Return path

Title	CPU VCORE ISL6323
Size	Document Number: RS780M-A2
Rev	1.0
Date:	Tuesday, October 21, 2008
Sheet	33 of 39

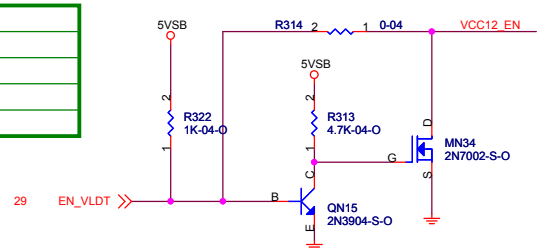
Elitegroup Computer Systems

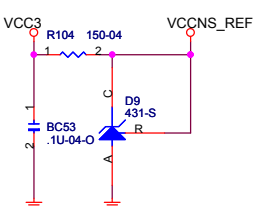


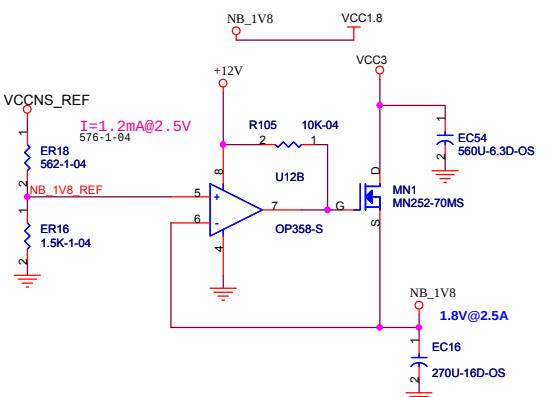
uP6262的電流輸出與ΔVout的關系如下:
選取從uP6262輸出的方向爲正, 則VCORE,CPUVTT及V_DIMM的ΔVout爲:
ΔVout = -Ic * RFB;
RFB爲:
1. For VCORE, RFB= ER43 = 2K OHM;
2. For CPUVTT, RFB = ER52 = 931 OHM;
3. For V_DIMM, RFB = ER56 = 887 OHM.



	GP24	GP26
1.35V	0	0
1.3V	0	1
1.25V	1	0
1.2V	1	1







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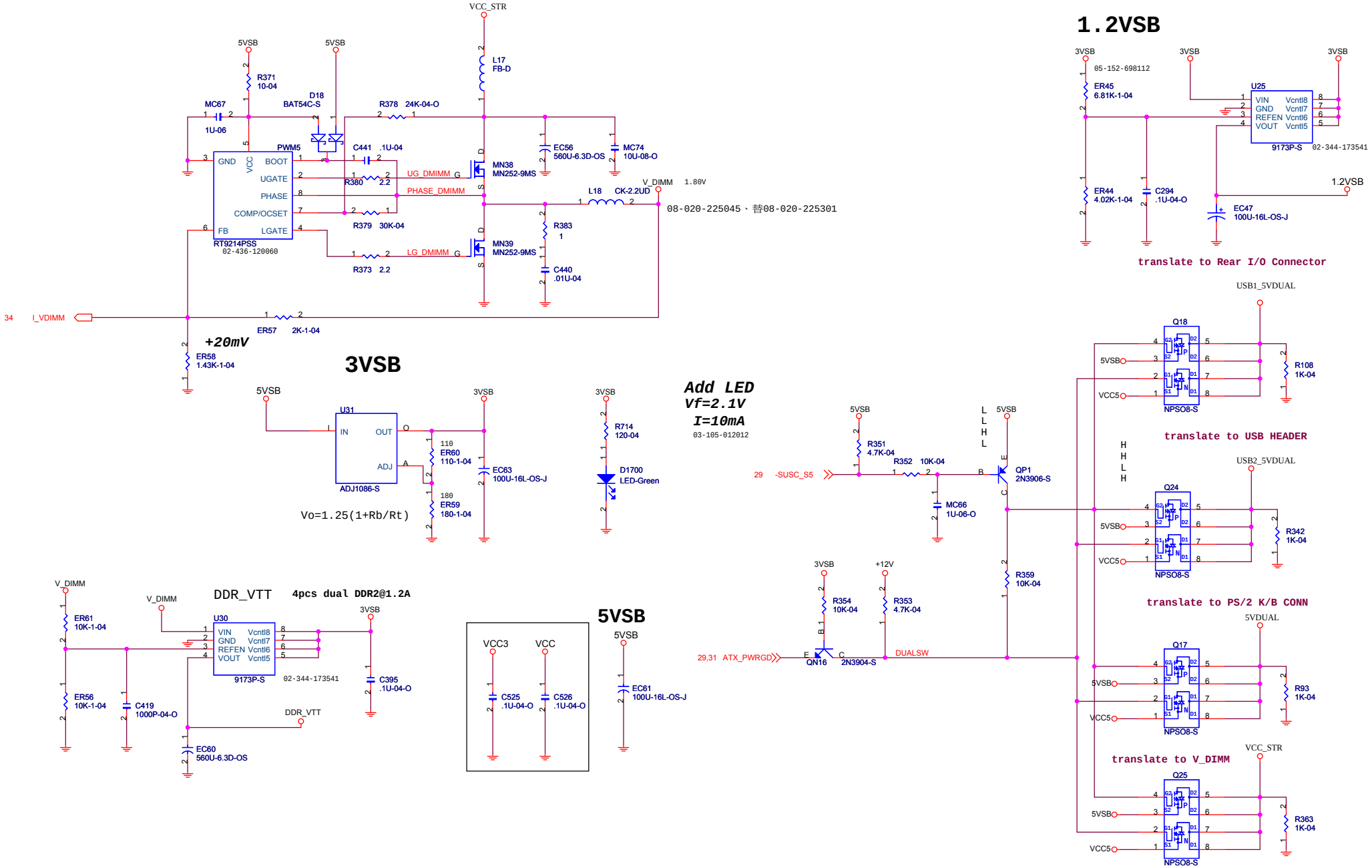
Title	NB POWER	
Size: Custom	Document Number: RS780M-A2	Rev: 1.0
Date: Tuesday, October 21, 2008	Sheet 34 of 39	



	S5	enter S0	S0	enter S3	exit S3	enter S5	S5
-SUSC_S5	0	0	1	1	1	0	0
ATX_PWRGD	0	1	1	0	1	1	0
QP1 pinC	5VSB	5VSB	12V	0	12V	5VSB	5VSB
DUALSW	0	12V	12V	0	12V	12V	0
VCCSTR	X	VCC5	VCC5	5VSB	VCC5	VCC	0
VDIMM	X	V	V	V	V	V	X

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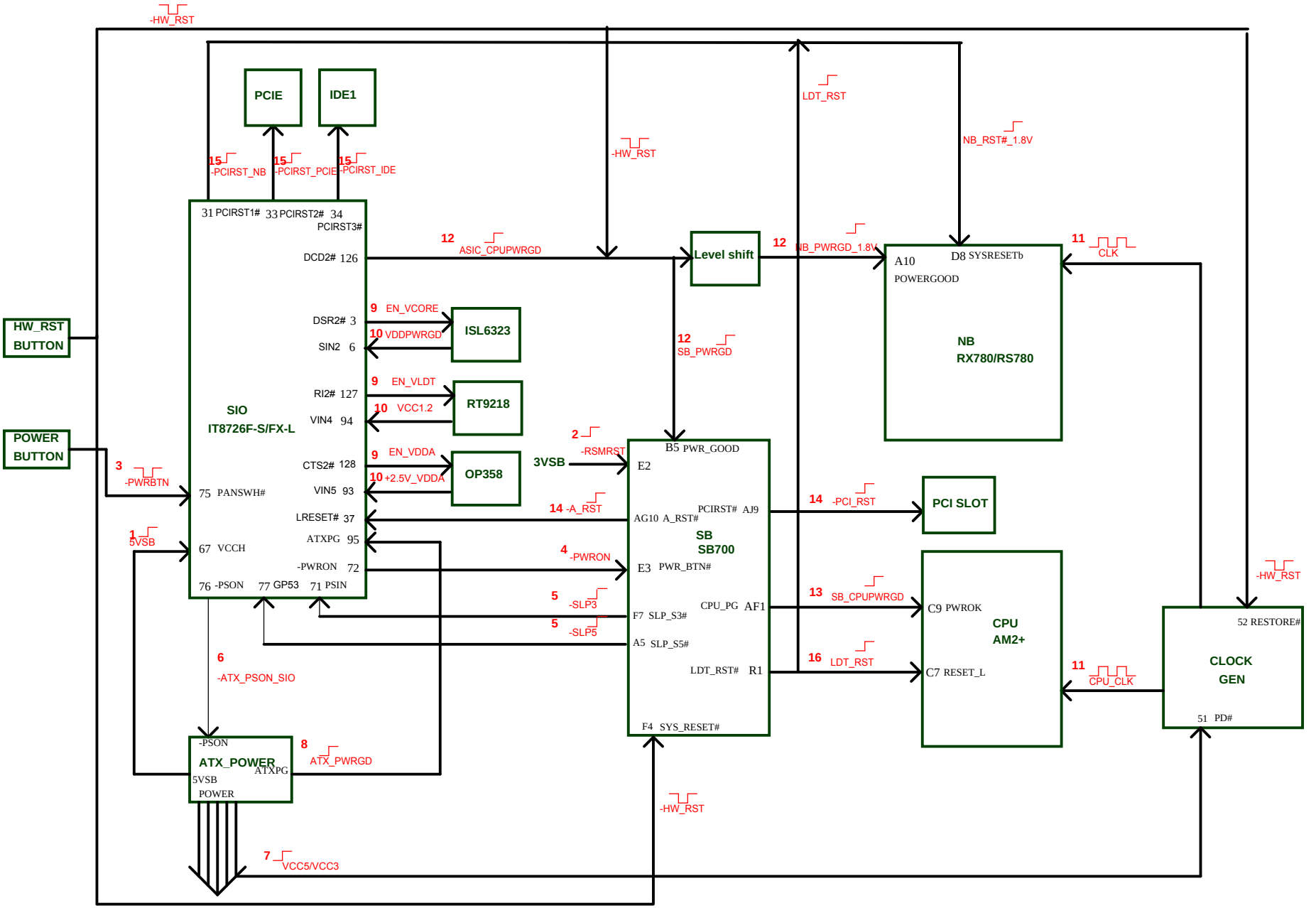
Title: DC-DC

Size: Custom | Document Number: RS780M-A2 | Rev: 1.0

Date: Tuesday, October 21, 2008 | Sheet 35 of 39



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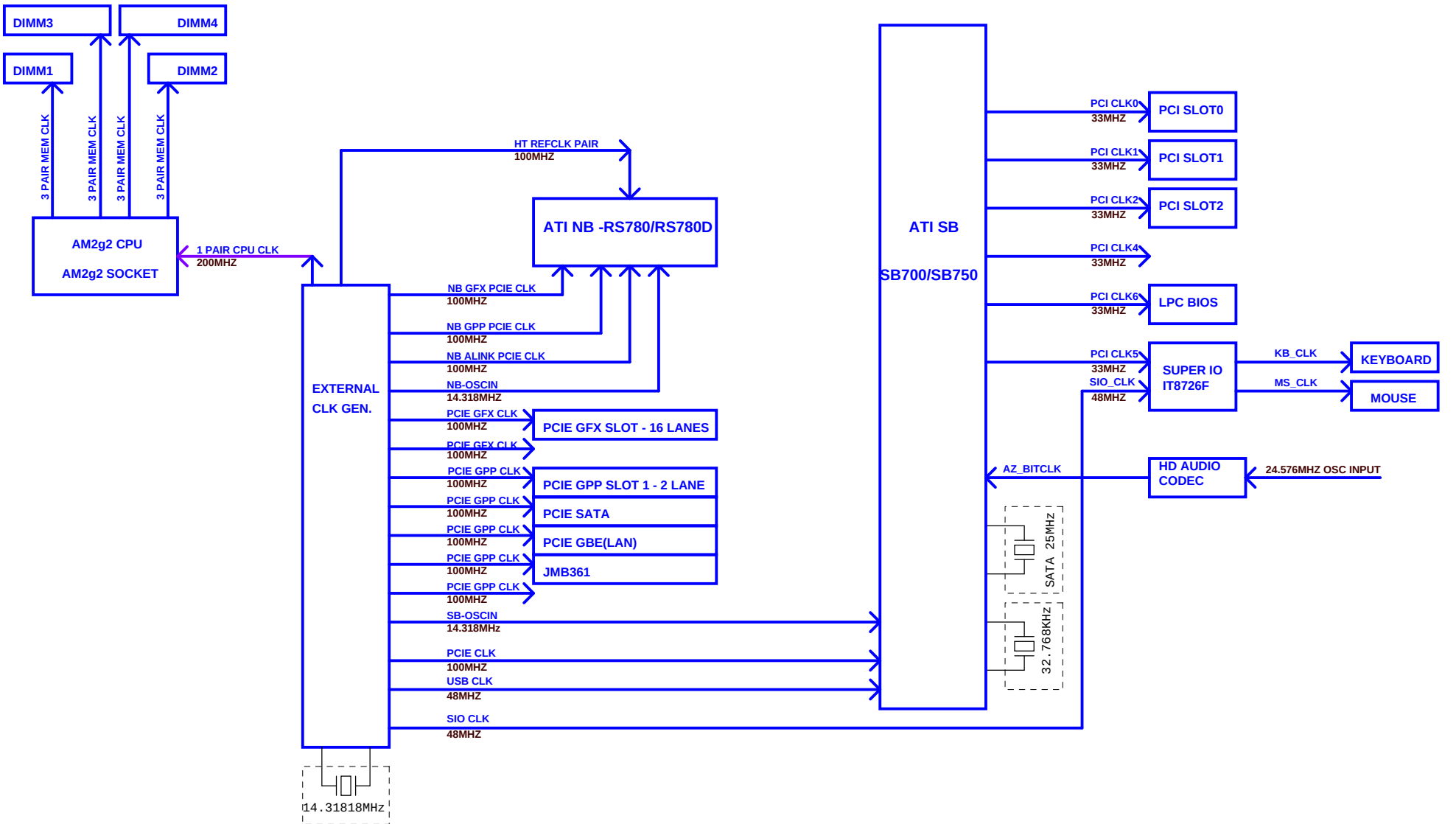
Title: POWER SEQUENCE

Size	Document Number	Rev
Custom	RS780M-A2	1.0

Date: Tuesday, October 21, 2008 Sheet 36 of 39



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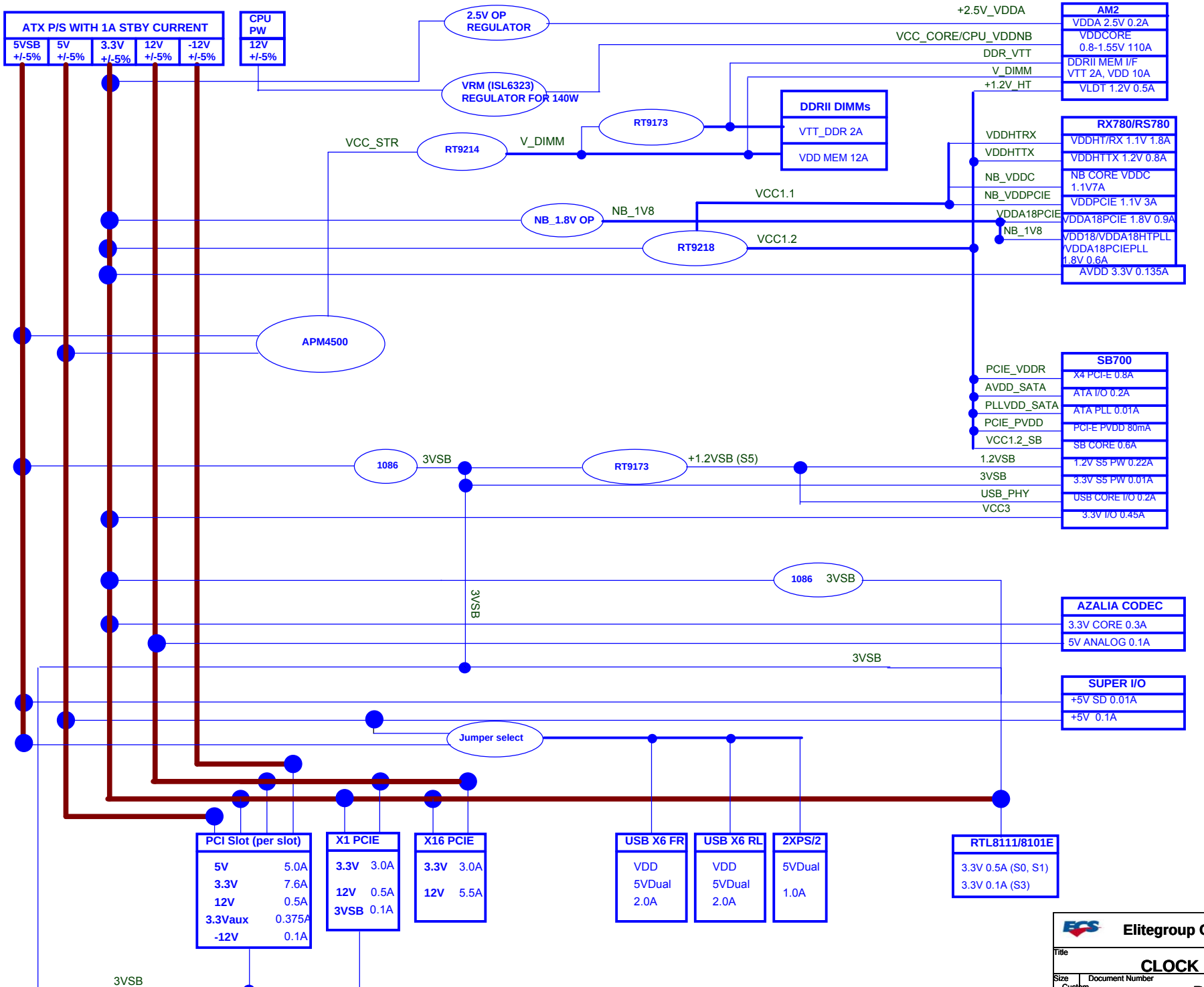
Title: CLOCK DISTRIBUTION

Size	Document Number	Rev
Custom	RS780M-A2	1.0

Date: Tuesday, October 21, 2008 Sheet 37 of 39


ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
CPU PW
12V +/-5%
2.5V OP REGULATOR
VRM (ISL6323) REGULATOR FOR 140W
+2.5V_VDDA
VCC_CORE/CPU_VDDNB
DDR_VTT
V_DIMM
+1.2V_HT
AM2
VDDA 2.5V 0.2A
VDDCORE 0.8-1.55V 110A
DDRII MEM I/F VTT 2A, VDD 10A
VLDT 1.2V 0.5A
DDRII DIMMs
VTT_DDR 2A
VDD MEM 12A
RT9173
RT9214
VCC_STR
V_DIMM
RX780/RS780
VDDHTRX
VDDHTTX
NB_VDDC
NB_VDDPCIE
VDDA18PCIE
NB_1V8
VDDHT/RX 1.1V 1.8A
VDDHTTX 1.2V 0.8A
NB CORE VDDC 1.1V7A
VDDPCIE 1.1V 3A
VDDA18PCIE 1.8V 0.9A
VDD18/VDDA18HTPLL /VDDA18PCIEPLL 1.8V 0.6A
AVDD 3.3V 0.135A
NB_1.8V OP
NB_1V8
VCC1.1
RT9218
VCC1.2
APM4500
SB700
PCIE_VDDR
AVDD_SATA
PLLVDD_SATA
PCIE_PVDD
VCC1.2_SB
X4 PCI-E 0.8A
ATA I/O 0.2A
ATA PLL 0.01A
PCI-E PVDD 80mA
SB CORE 0.6A
1086
3VSB
RT9173
+1.2VSB (S5)
1.2VSB
3VSB
USB_PHY
VCC3
1.2V S5 PW 0.22A
3.3V S5 PW 0.01A
USB CORE I/O 0.2A
3.3V I/O 0.45A
1086
3VSB
3VSB
AZALIA CODEC
3.3V CORE 0.3A
5V ANALOG 0.1A
3VSB
SUPER I/O
+5V SD 0.01A
+5V 0.1A
Jumper select
PCI Slot (per slot)
5V 5.0A
3.3V 7.6A
12V 0.5A
3.3Vaux 0.375A
-12V 0.1A
X1 PCIE
3.3V 3.0A
12V 0.5A
3VSB 0.1A
X16 PCIE
3.3V 3.0A
12V 5.5A
USB X6 FR
VDD
5VDual
2.0A
USB X6 RL
VDD
5VDual
2.0A
2XPS/2
5VDual
1.0A
RTL8111/8101E
3.3V 0.5A (S0, S1)
3.3V 0.1A (S3)
3VSB
Elitegroup Computer Systems
Title
CLOCK DISTRIBUTION
Size Custom
Document Number
RS780M-A2
Rev 1.0
Date: Tuesday, October 21, 2008
Sheet 38 of 39

SB600 PinD23 GPIO5:audio PANEL_DETECT(1:no,0:yes)
SB600 PinC26 GPIO8:PCEI_GFX1_PRSNT-
SB600 PinD26 GPIO9:-P66DET

8726 GPIO使用:
Pin14-GPIO34用作WT_BEEP
Pin13-GPIO35 用作NB_PWM_enable控制
Pin18-GPIO31 PLED
Pin78-GP41 SUSLED
Pin28-GP17 -WP_ROM
Pin79-GPIO40: SIO_VDUAL control 5vdual
Pin28-GP22-THRM
Pin27-GP20:-LPC_SMI
Pin70-GP46:Control v_dimm

For 103

X5(WIRE)

XTAL-JW

PCI SLOT1:REQ0;GNT0 IDSEL:21 INT:EFGH
PCI SLOT2:REQ1;GNT1 IDSEL:22 INT:FGHE
PCI SLOT3:REQ2;GNT2 IDSEL:23 INT:GHEF

NB_PWM1: Regulate VCC_CORE

NB_PWM2: Regulate V_DIMM

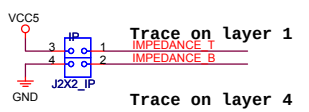
GPP:0-->PCIEx1
GPP:1-->PCIEx1
GPP:2-->GIGA LAN

PCB Impedance control

Impedance (ohm)	Trace Width (mil) (S/W/S)	Trace Length (inch)	Pre-preg	
60	5 (20/5/20)	6	2116	V
50	4 (50/4/50)	6	1080	
42	6 (50/6/50)	6	1080	

1)Circuit type 1

Layer 1:TOP
Layer 2:GND
Layer 3:LNNER
Layer 4:PWR
Layer 5:GND
Layer 6:BOTTOM



Trace on layer 1

Trace on layer 4

For 104

NB1(104)

NB_HEATSINK

ROM1(104)

SPI-ROM-D-8M

BT(104)

KTS
LITHIUM BATTERY
CD2032

BATTERY

CLR_CMOS(1-2)

JP-R

SB1(104)

SB_HEATSINK

Notes:
1). "PWR" net means inner power plane under impedance trace.
2). "GND" net means inner ground plane under impedance trace.
3). IP1 footprint is J2X2_IP
4). After nelist running, please specially take care the single net name: "IMPEDANCE_T" and "IMPEDANCE_B".

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Title: 104&IMPENDANCE

Size: Custom | Document Number: RS780M-A2 | Rev: 1.0

Date: Tuesday, October 21, 2008 | Sheet 39 of 39