Q67H2-AD/ Q65H2-AD/ H67H2-AD

Rev : 1.0

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NOTE:

REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/22	Initial version
V.B	2010/08/24	
V.C	2010/09/10	
V.1.0	2010/09/16	

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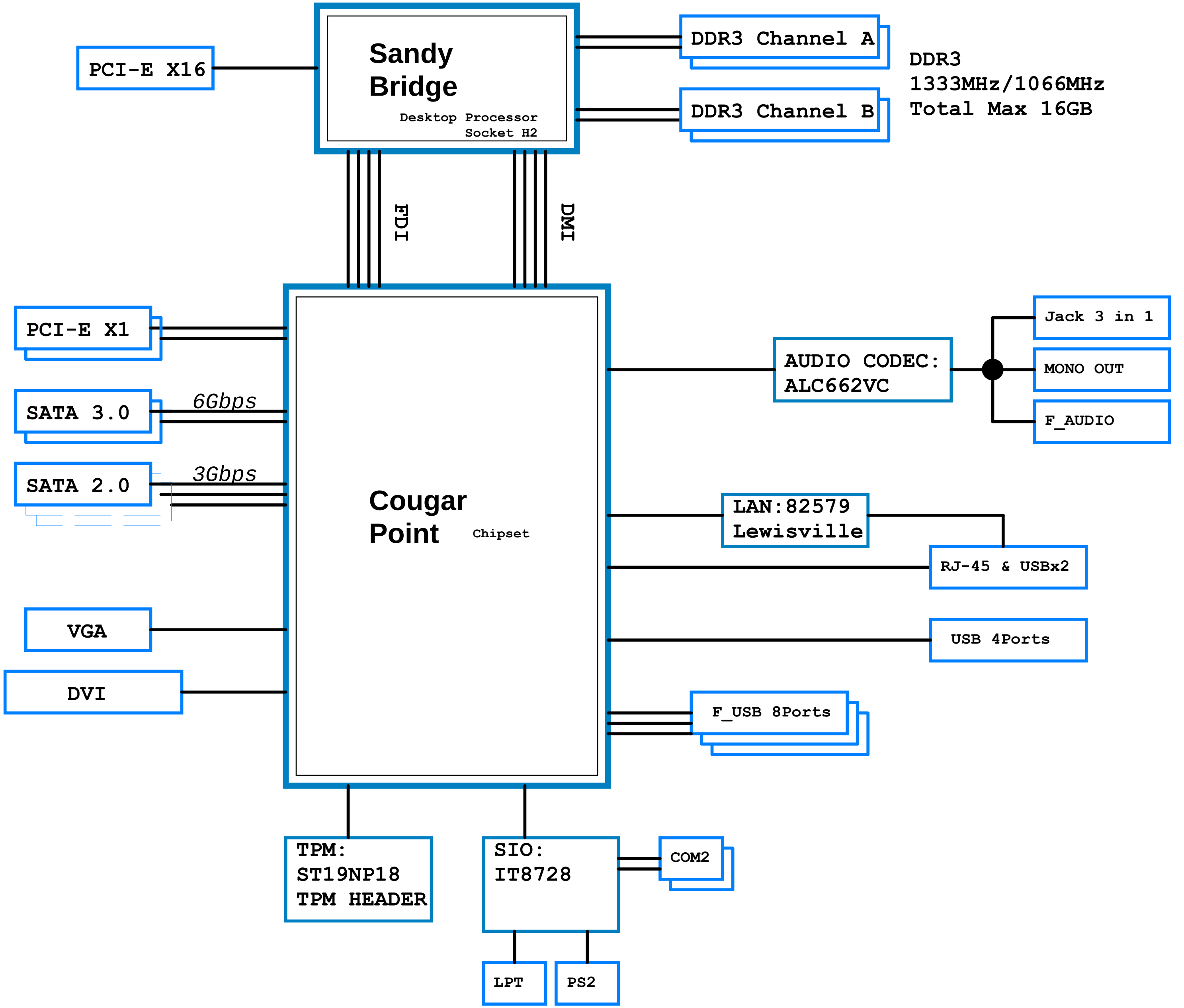

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Title	Block Diagram	
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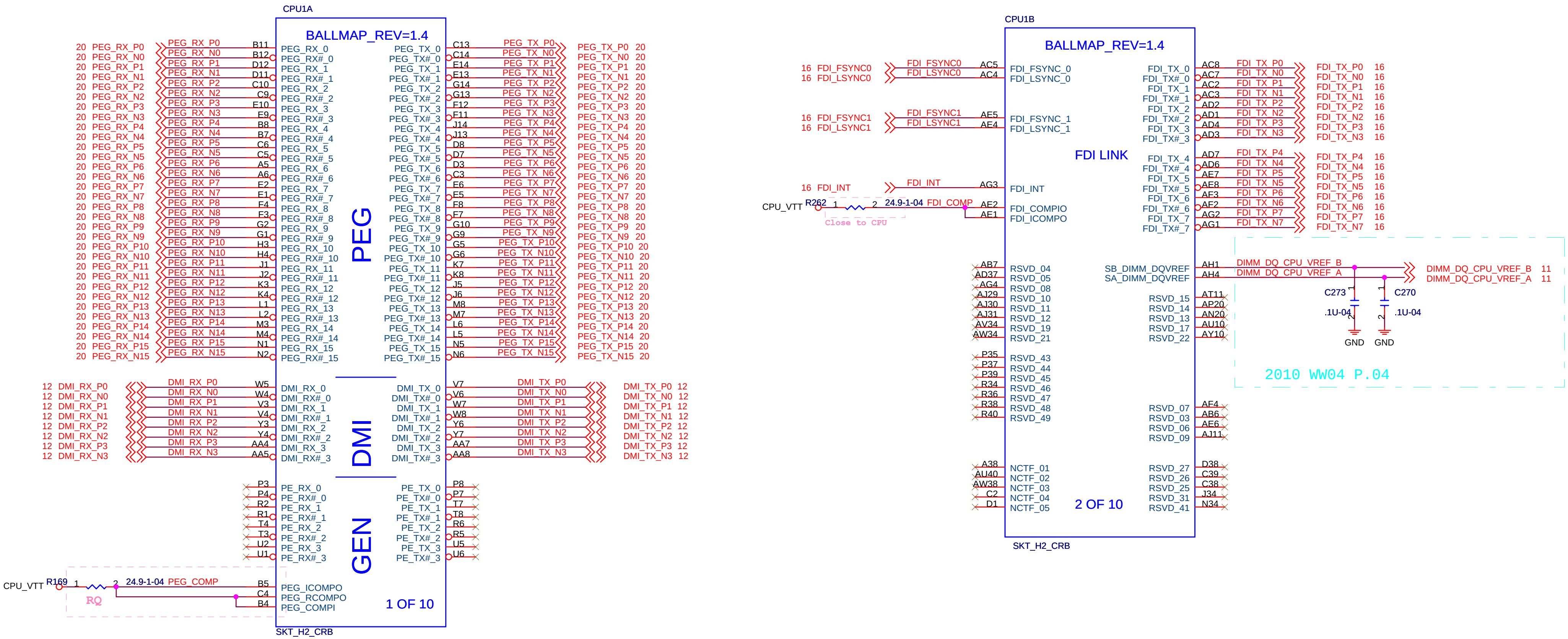
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	LPT Detect	GPI
GPIO22	VCC3	CLR_CMOS	GPI
GPIO38	VCC3	KM Detect	GPI
GPIO39	VCC3	SENSE_Header	GPI
GPIO48	VCC3	SENSE_Header	GPI
GPIO21	VCC3	COM2 Detect	GPI
GPIO36	VCC3	TCM,TPM Detect	GPI
GPIO37	VCC3	TCM,TPM Detect	GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

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Title	CPU - DMI/FDI/PEG
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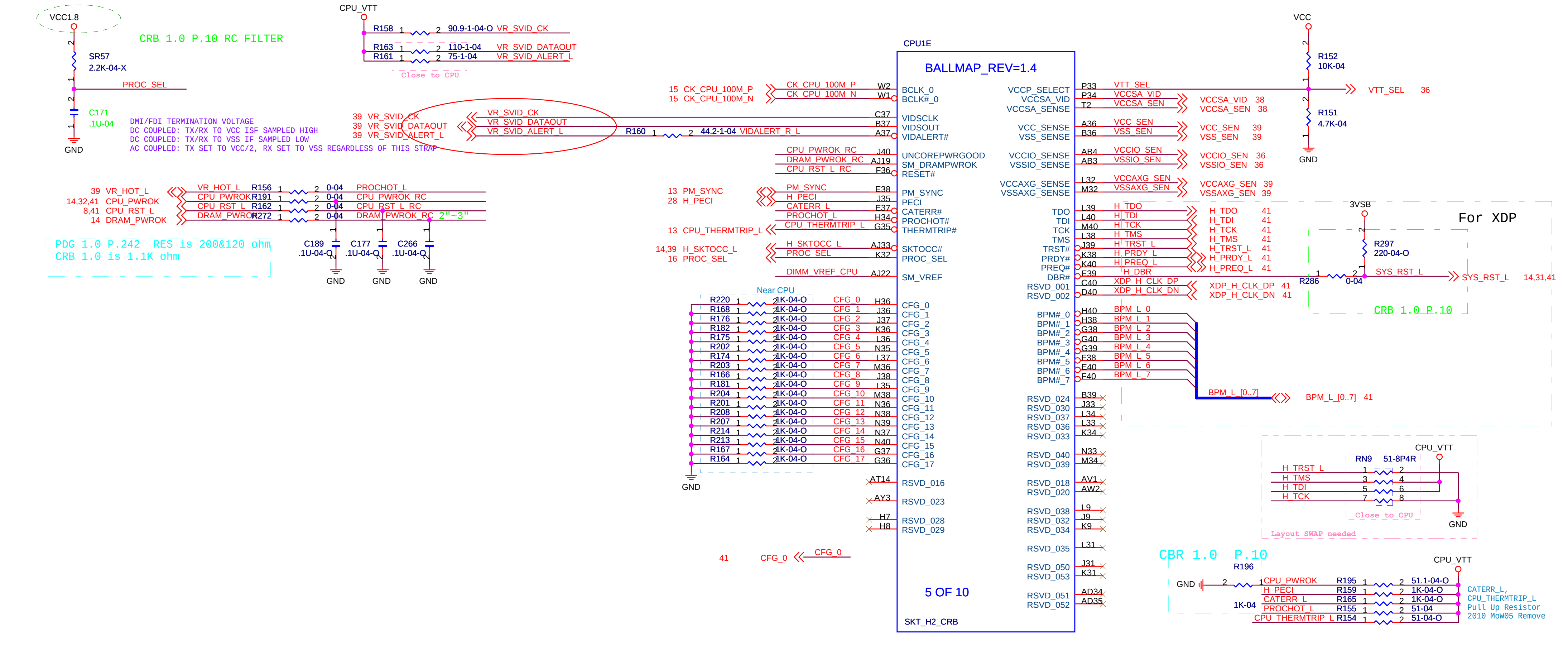
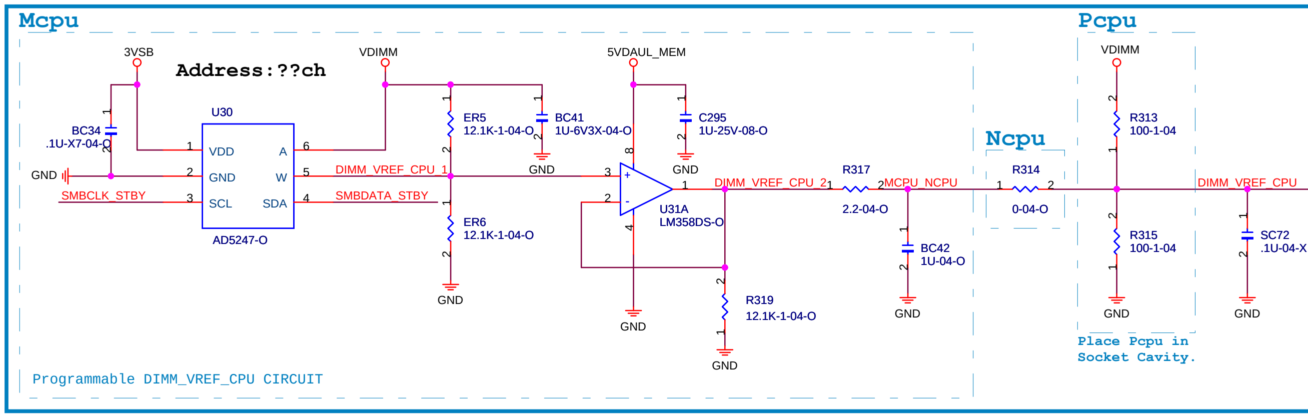


CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

	PCIE CONFIG	SEL0	SEL1
*	1 X 16	1	1
	2 X 8	0	1

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4



Layout Note:
All Parts Close yo CPU

10 mils

DIMM_VREF_CPU Control Mode:

Control Mode / Part	Divider	PCH + Controller
Mcpu	X	V
Ncpu	X	V
Pcpu	V	X

Default

DIMM_VREF_CPU Control Circuit

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Title	CPU - MISC
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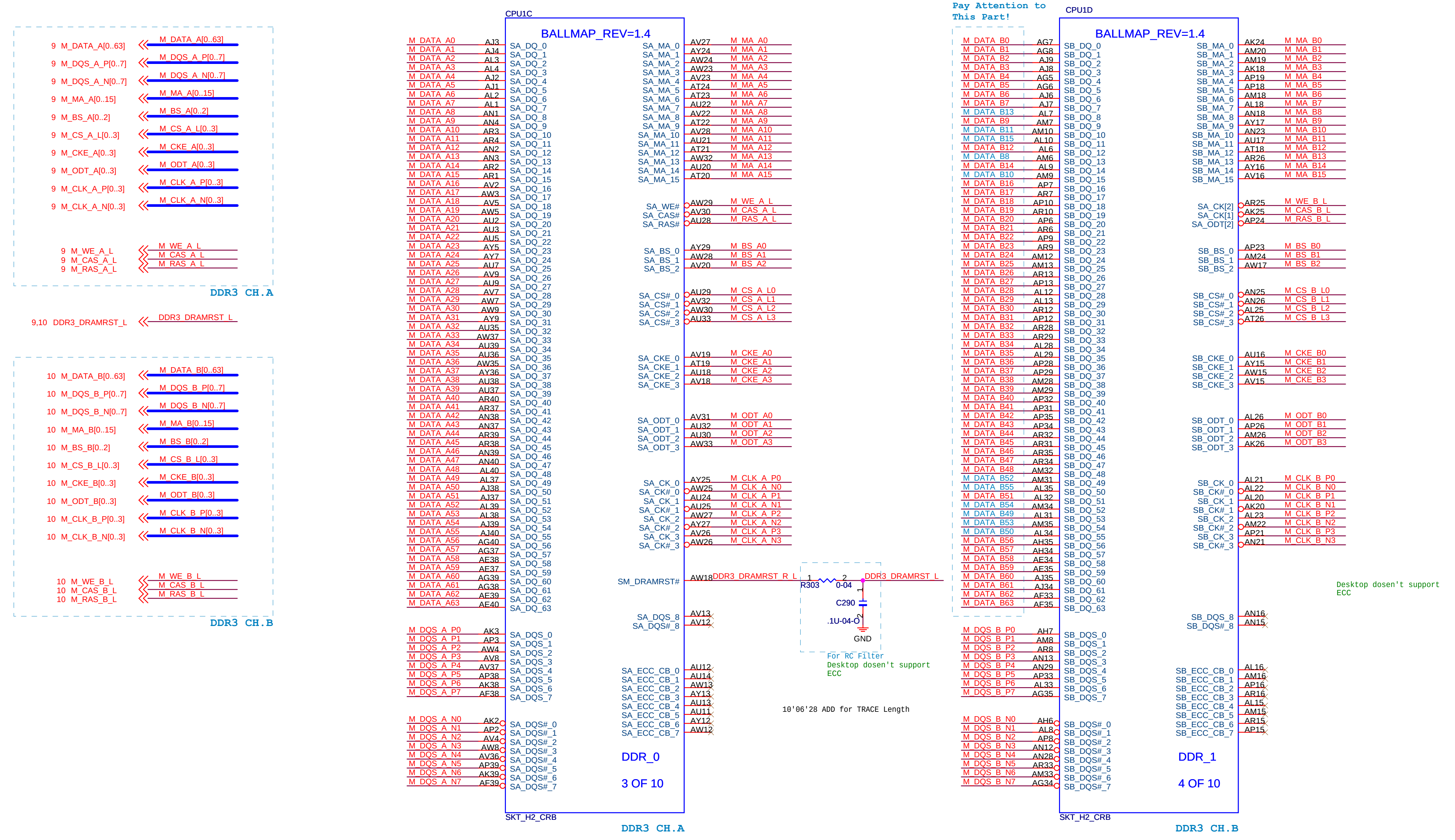

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Title: CPU - DDR3

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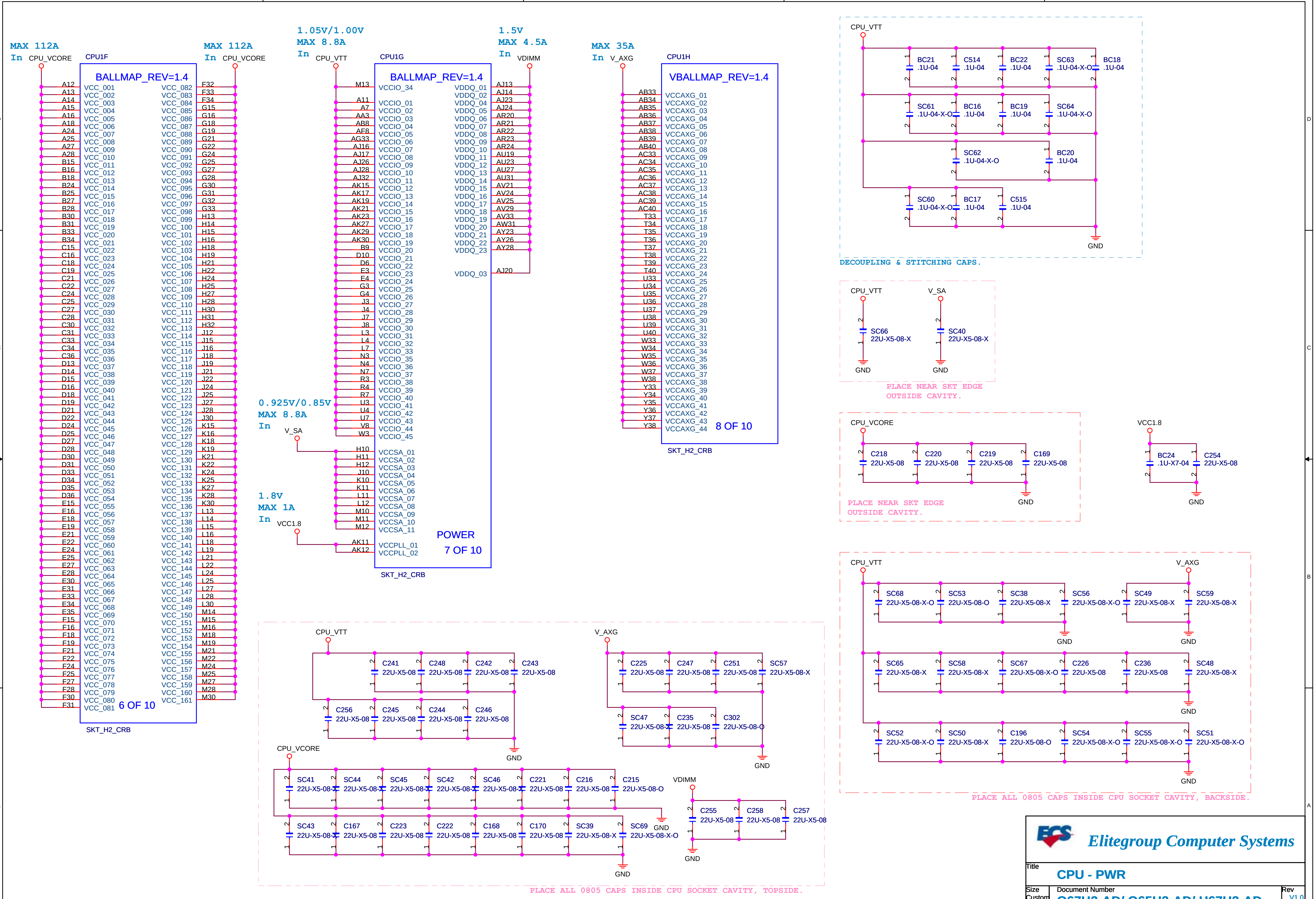

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Title	CPU - PWR
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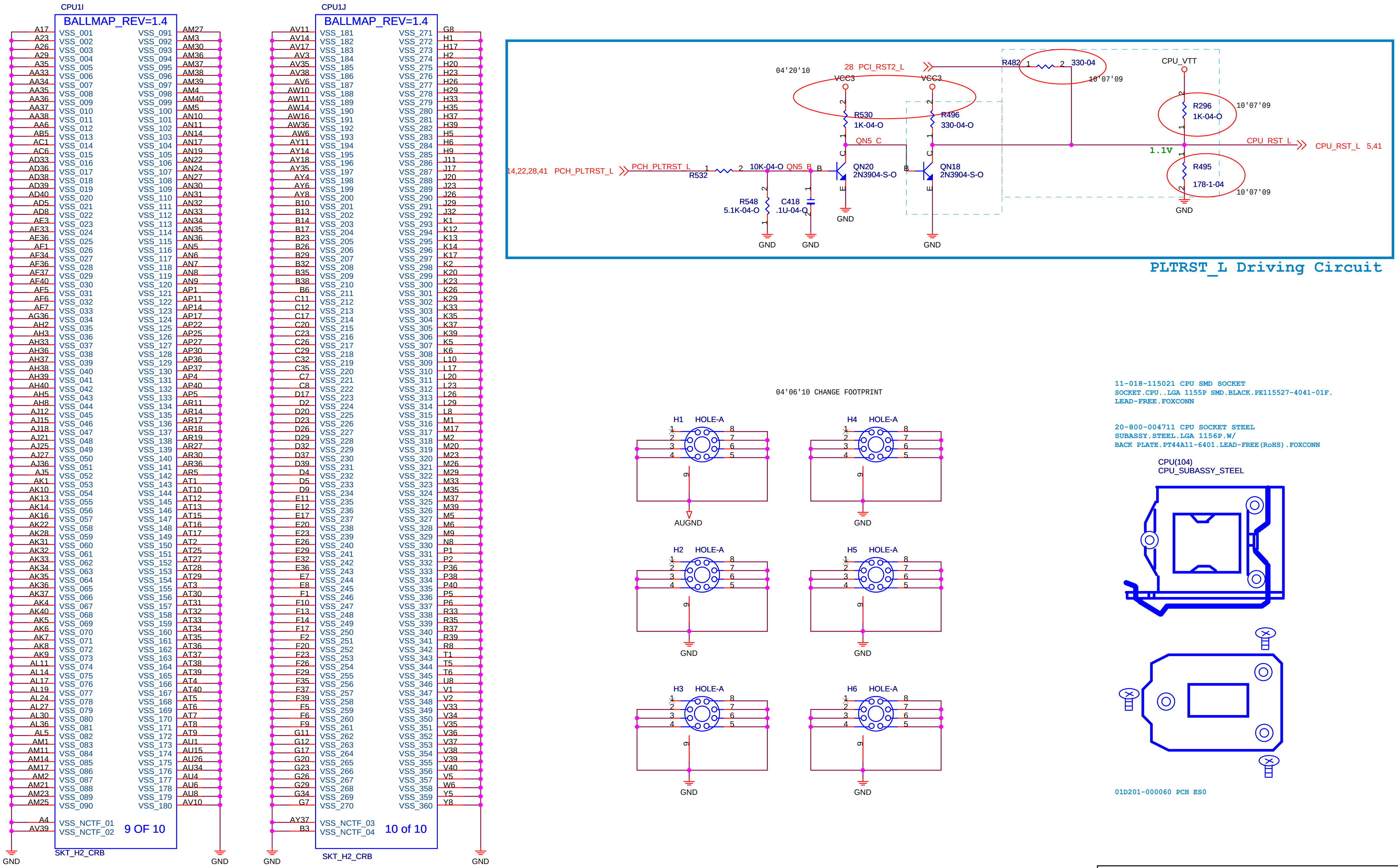

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Title	CPU - GND, CPU_RST_L
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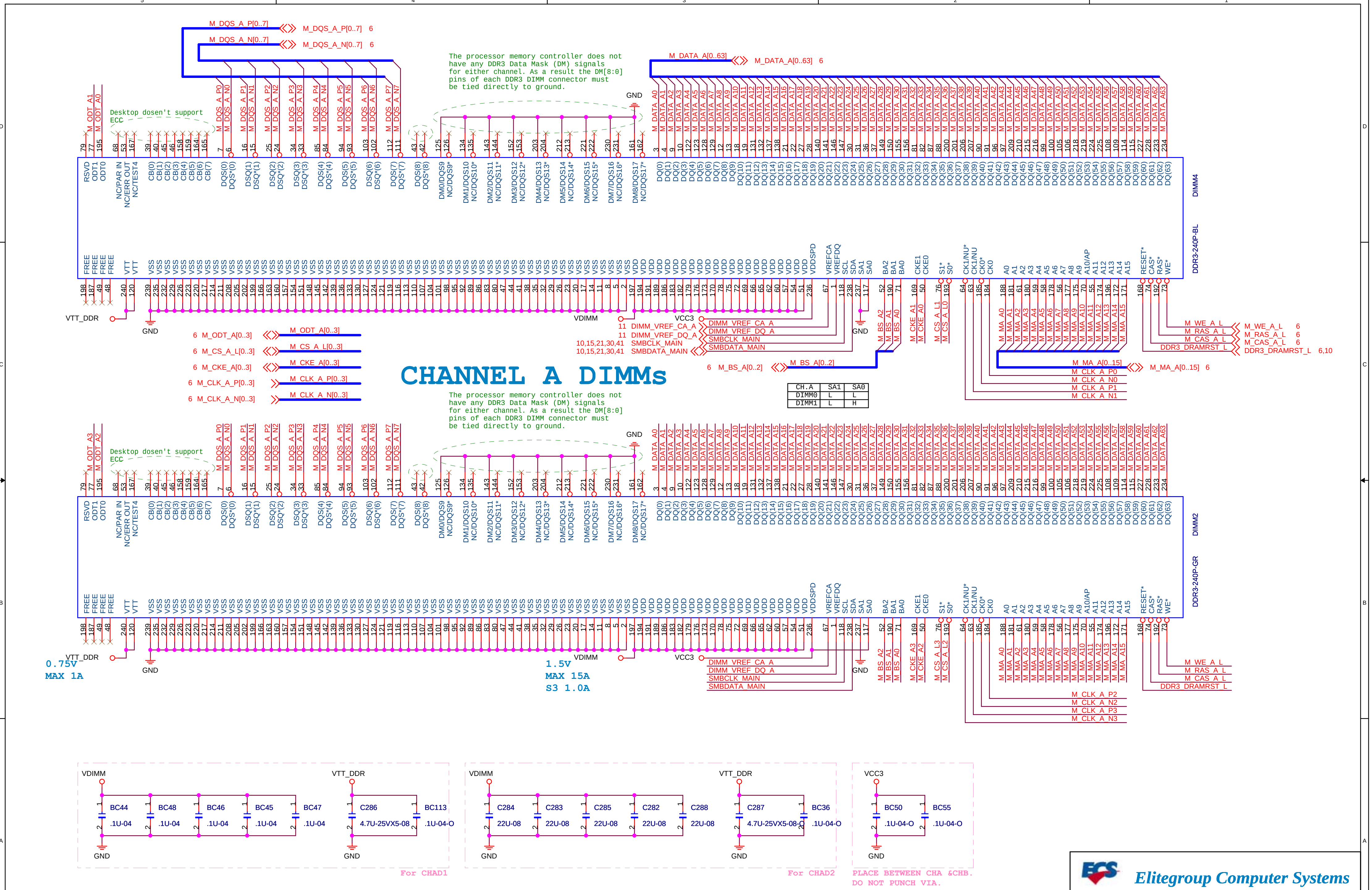

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Title	DDR3 - CHA DIMM0/1
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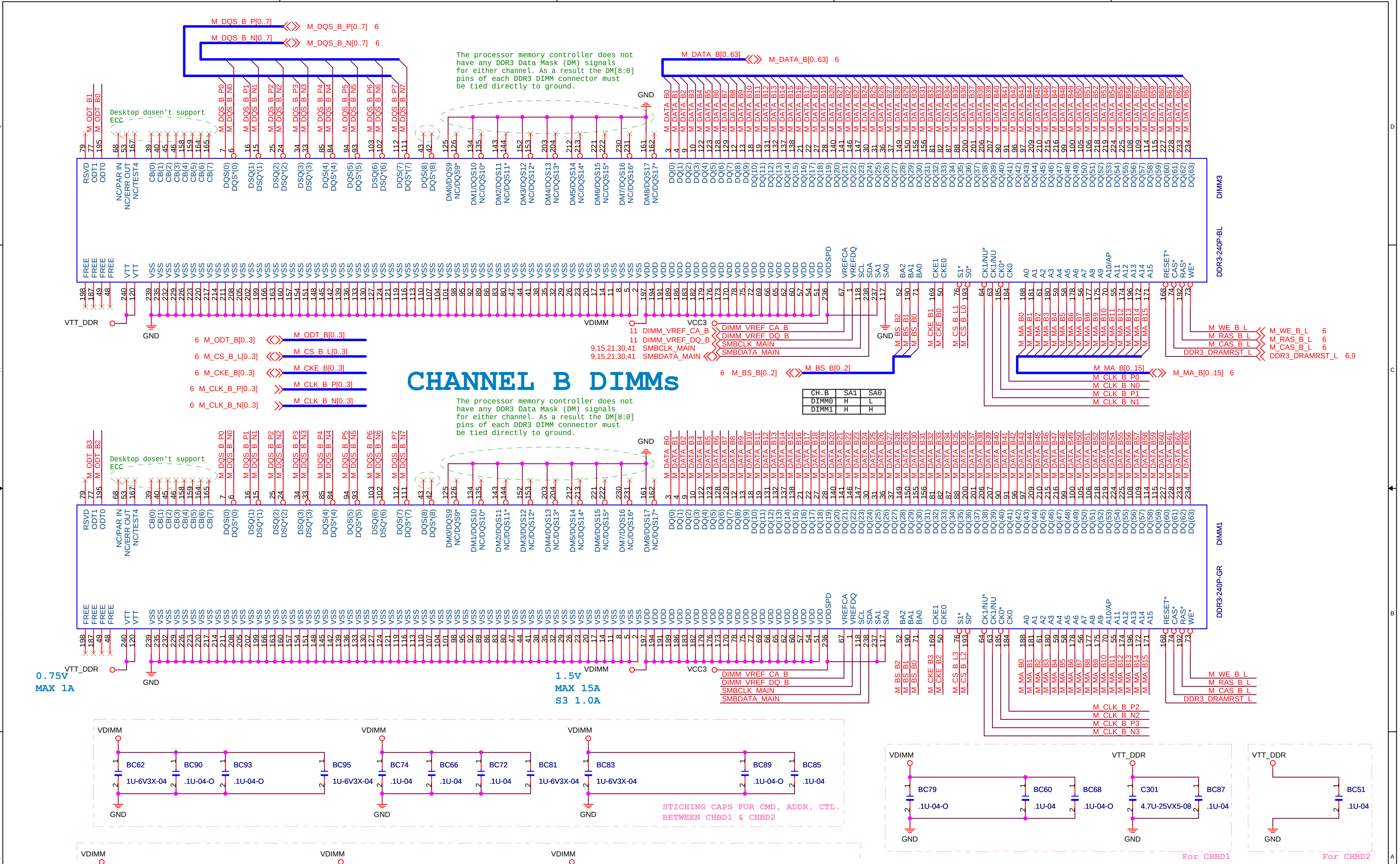

CH.B	SA1	SA0
DIMM0	H	L
DIMM1	H	H

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Title	DDR3 - CHB DIMM0/1
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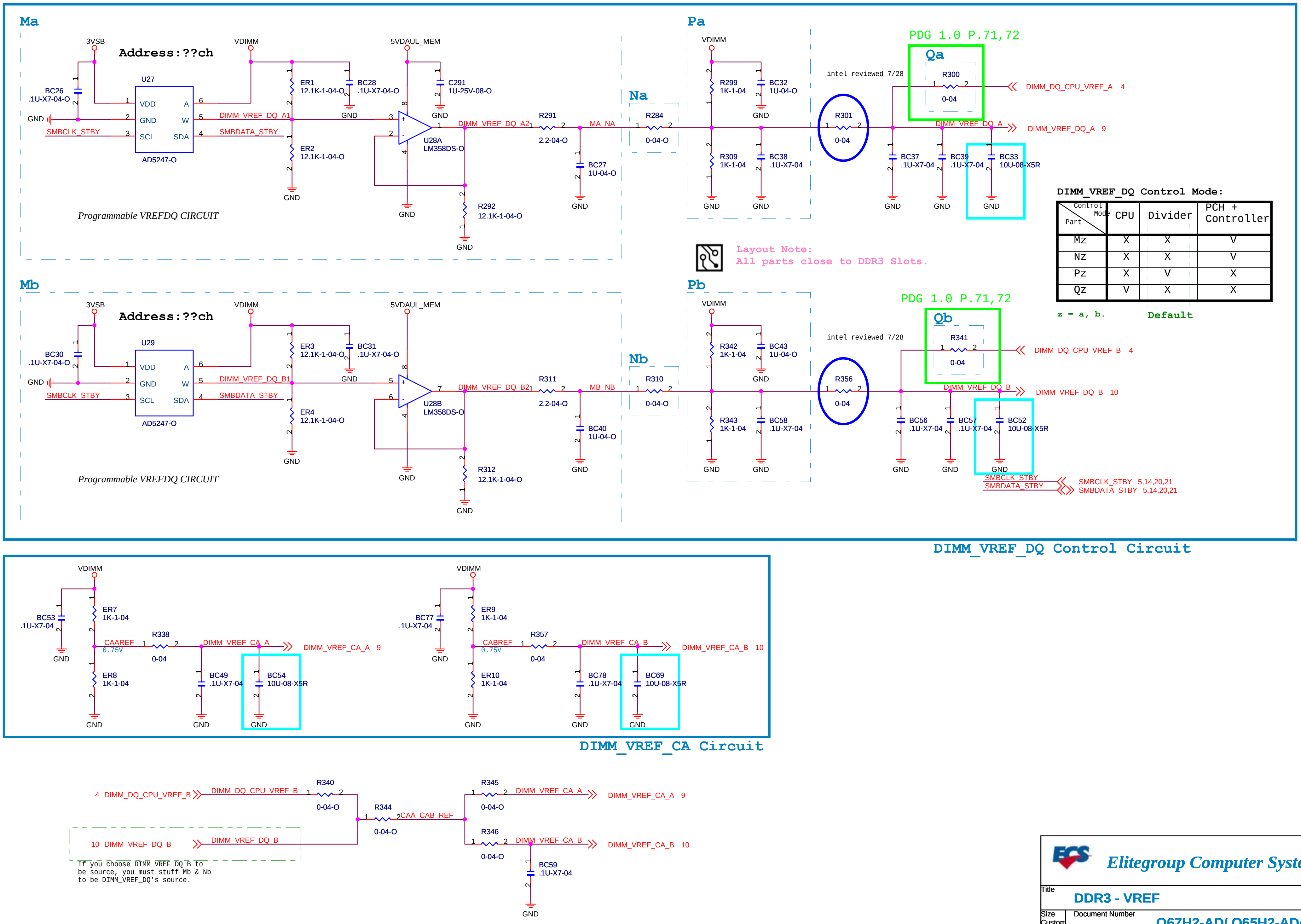

DIMM_VREF_DQ Control Mode:

Control Mode / Part	CPU	Divider	PCH + Controller
Mz	X	X	V
Nz	X	X	V
Pz	X	V	X
Qz	V	X	X

z = a, b. Default

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Title: DDR3 - VREF

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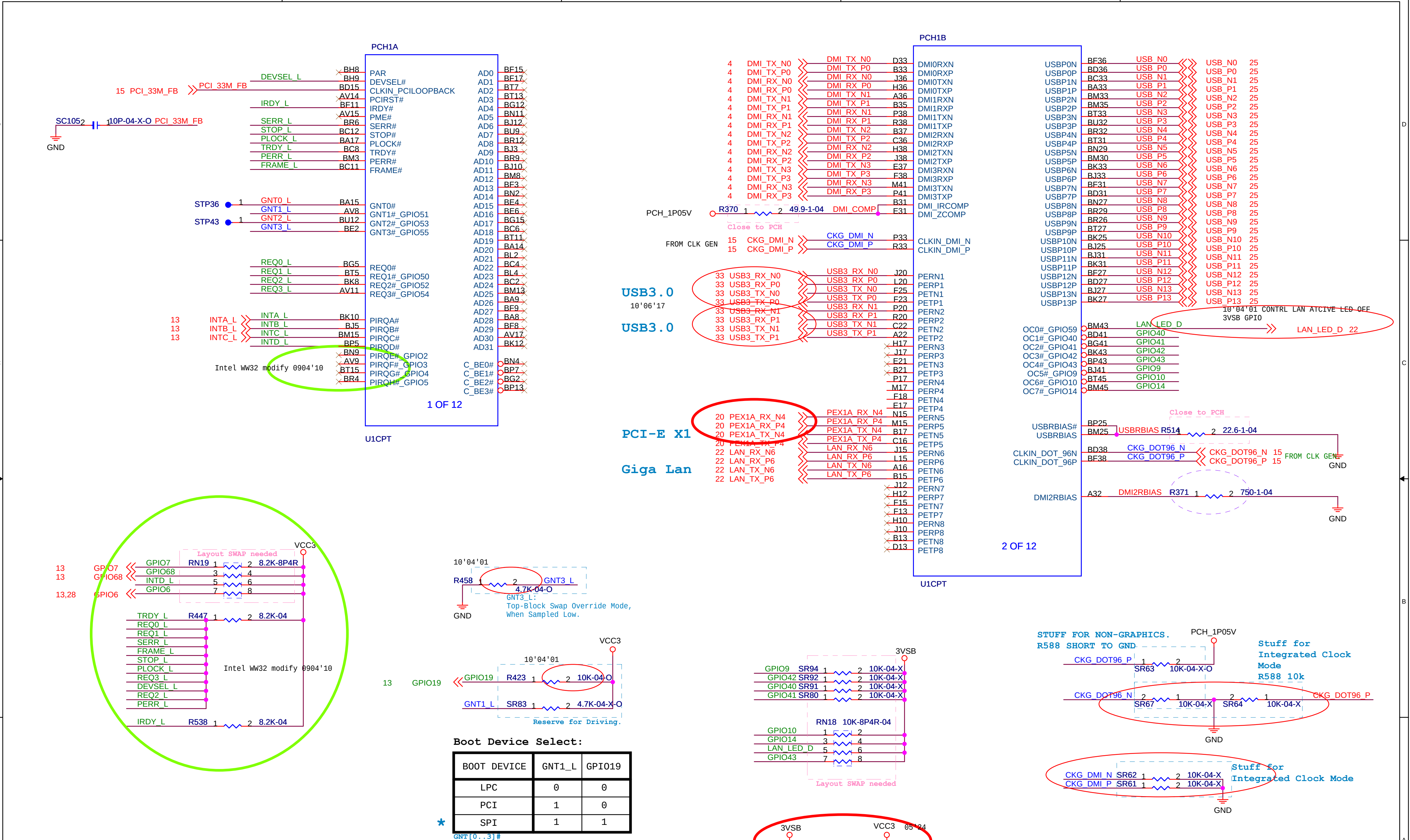

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
* SPI	1	1

GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

GNT1#, GPIO19 Follow CPT EDS V0.7,
CRB V0.7, PDG V0.8

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Title: PCH - DMI/PCI/PE/USB

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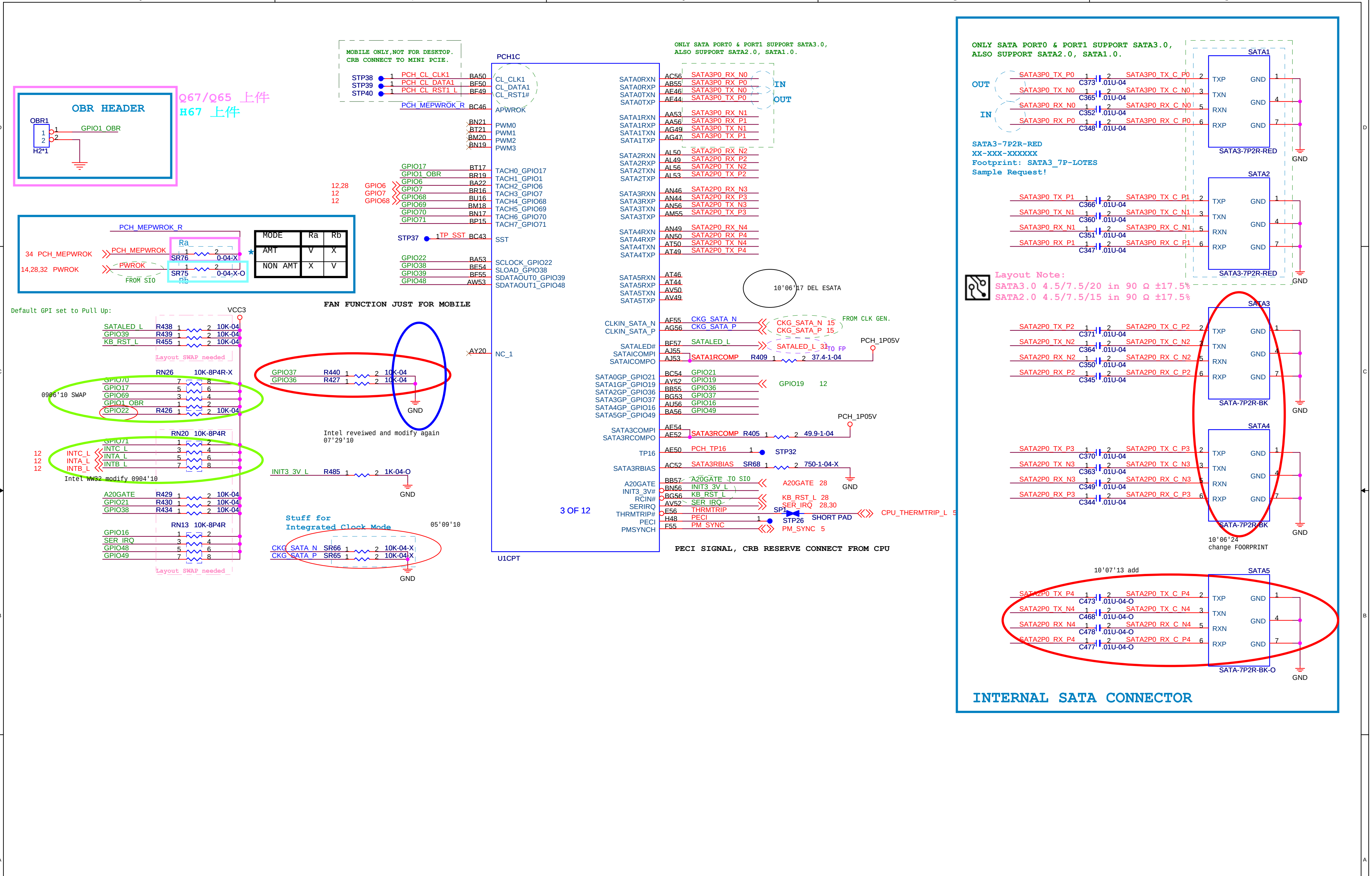

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Title: PCH - SATA, SATA CONN

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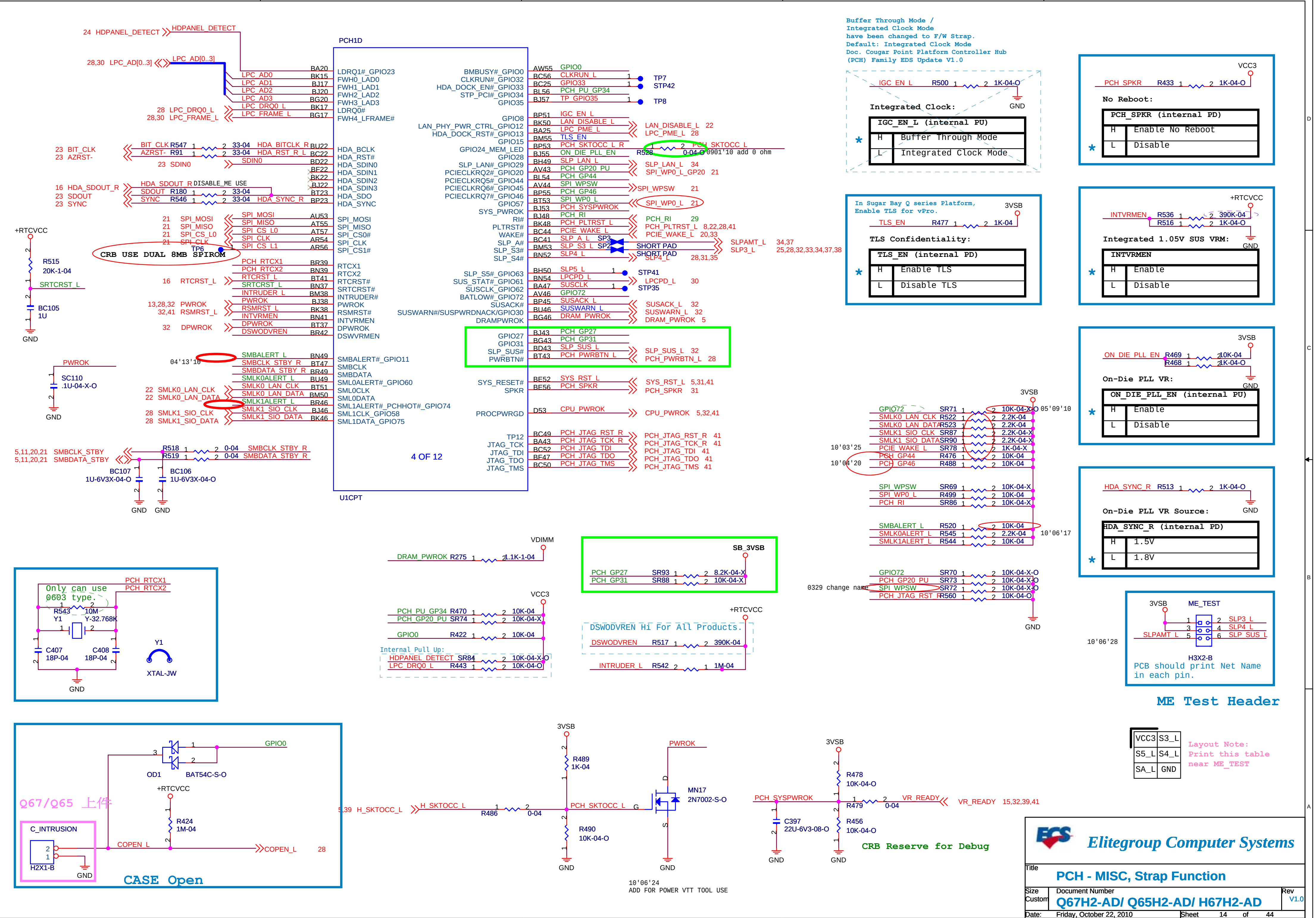

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Title: PCH - MISC, Strap Function

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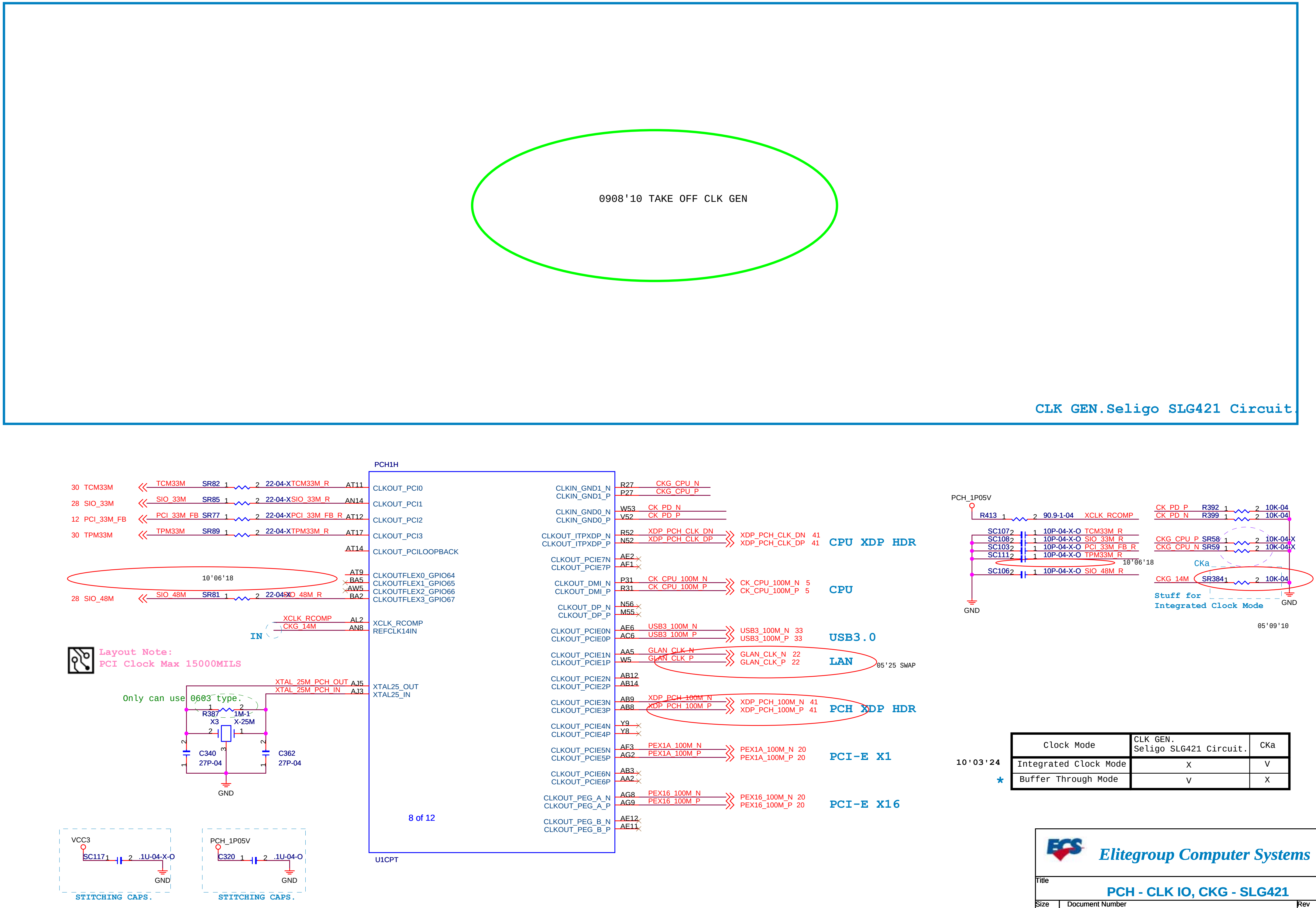

Clock Mode	CLK GEN. Seligo SLG421 Circuit.	CKa
Integrated Clock Mode	X	V
★ Buffer Through Mode	V	X

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Title: **PCH - CLK IO, CKG - SLG421**

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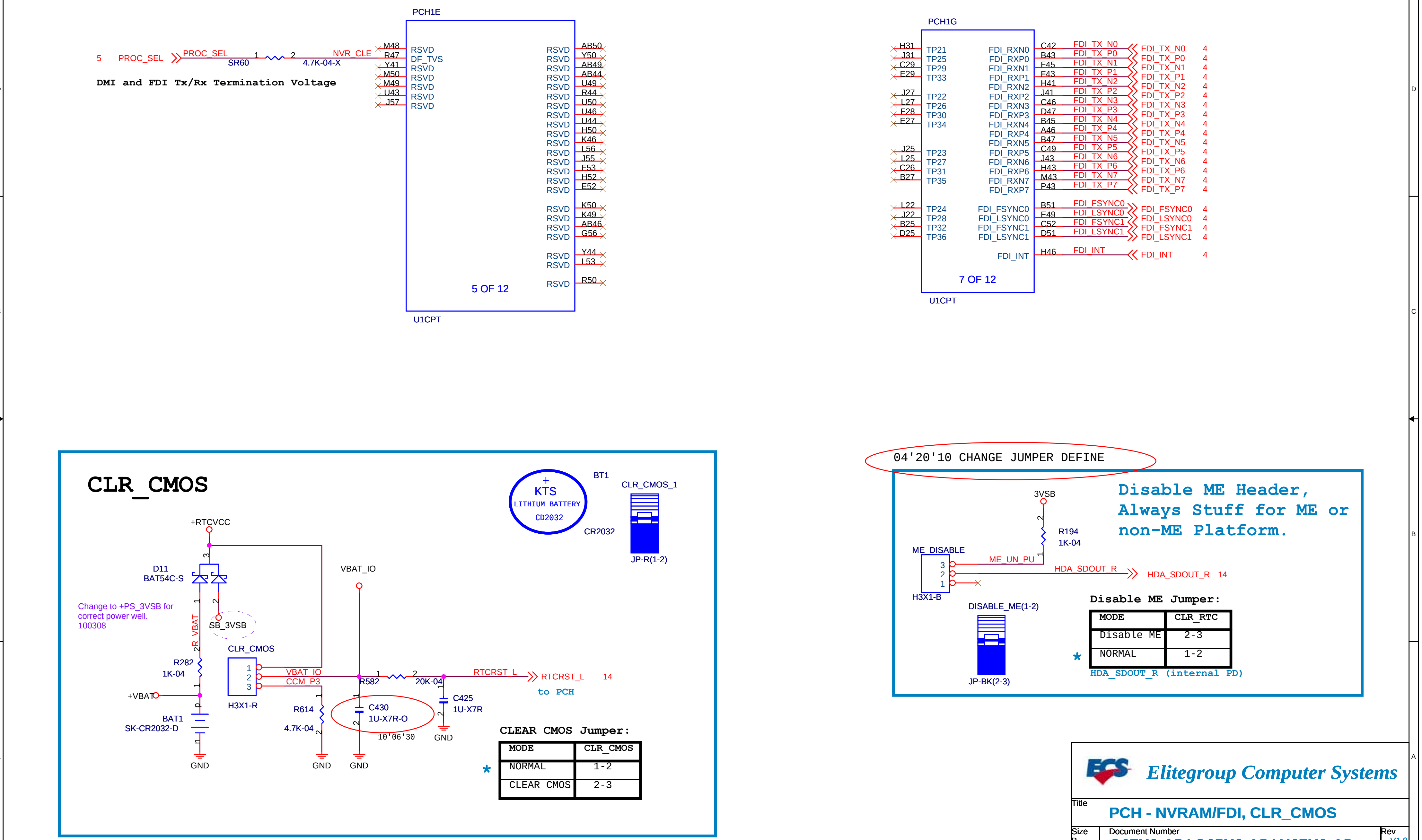

CLEAR CMOS Jumper:

MODE	CLR_CMOS
* NORMAL	1-2
CLEAR CMOS	2-3

Disable ME Jumper:

MODE	CLR_RTC
Disable ME	2-3
* NORMAL	1-2

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Title: PCH - NVRAM/FDI, CLR_CMOS

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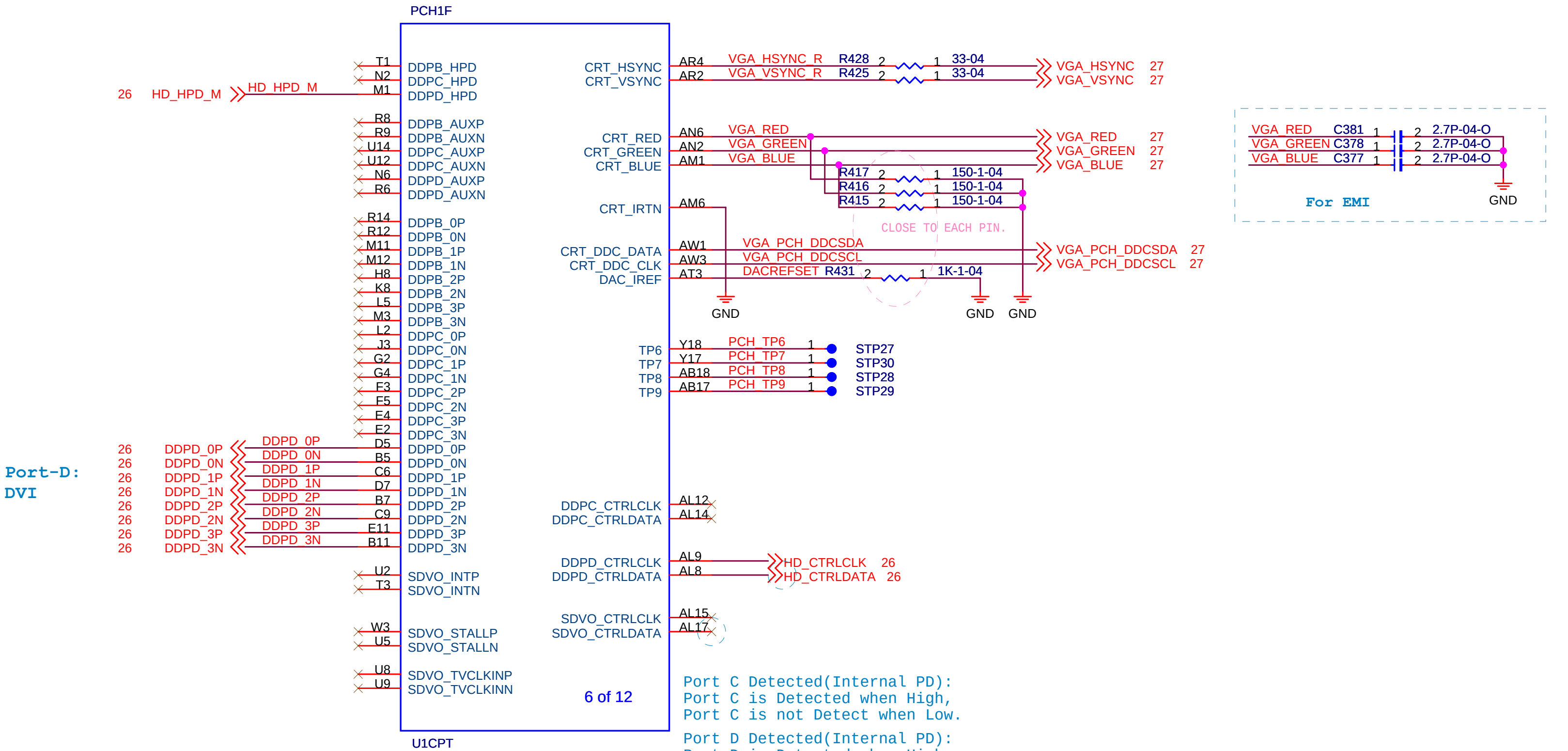

Port C Detected(Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.

Port D Detected(Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.

Port B Detected(Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.

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Title	PCH - DP/VGA	
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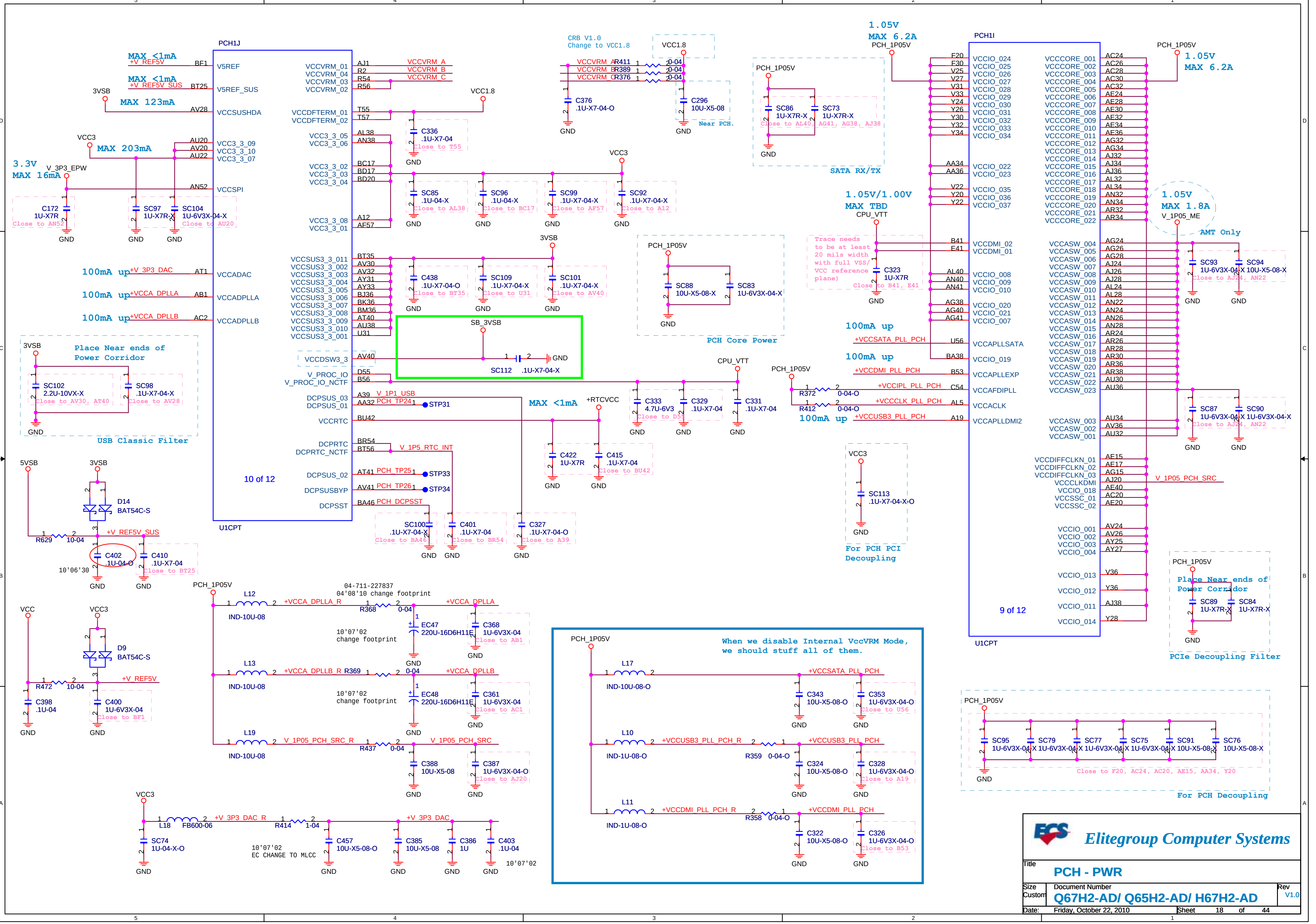

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Title: PCH - PWR

Size: Custom

Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD

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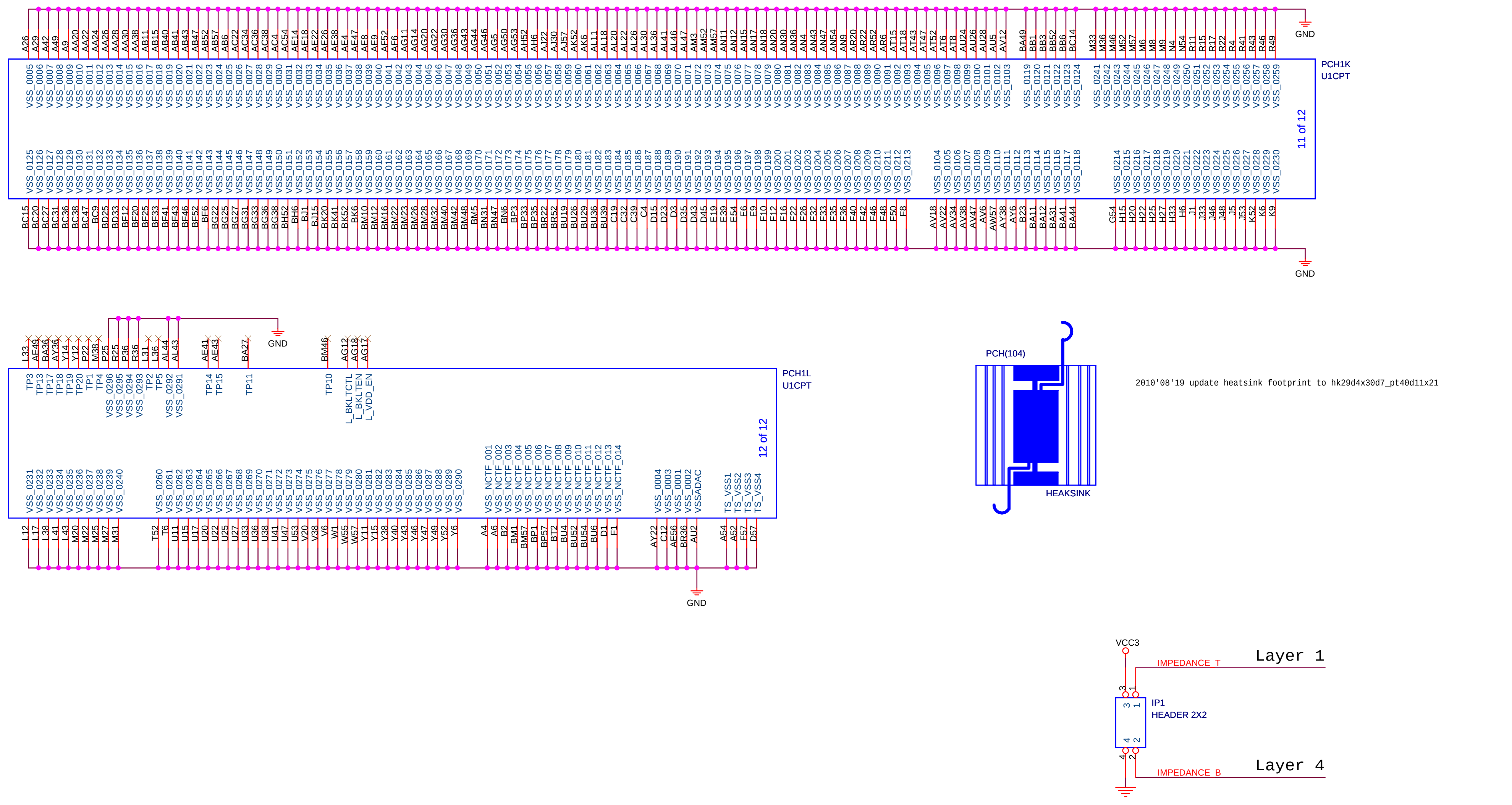

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Title	PCH - GND	
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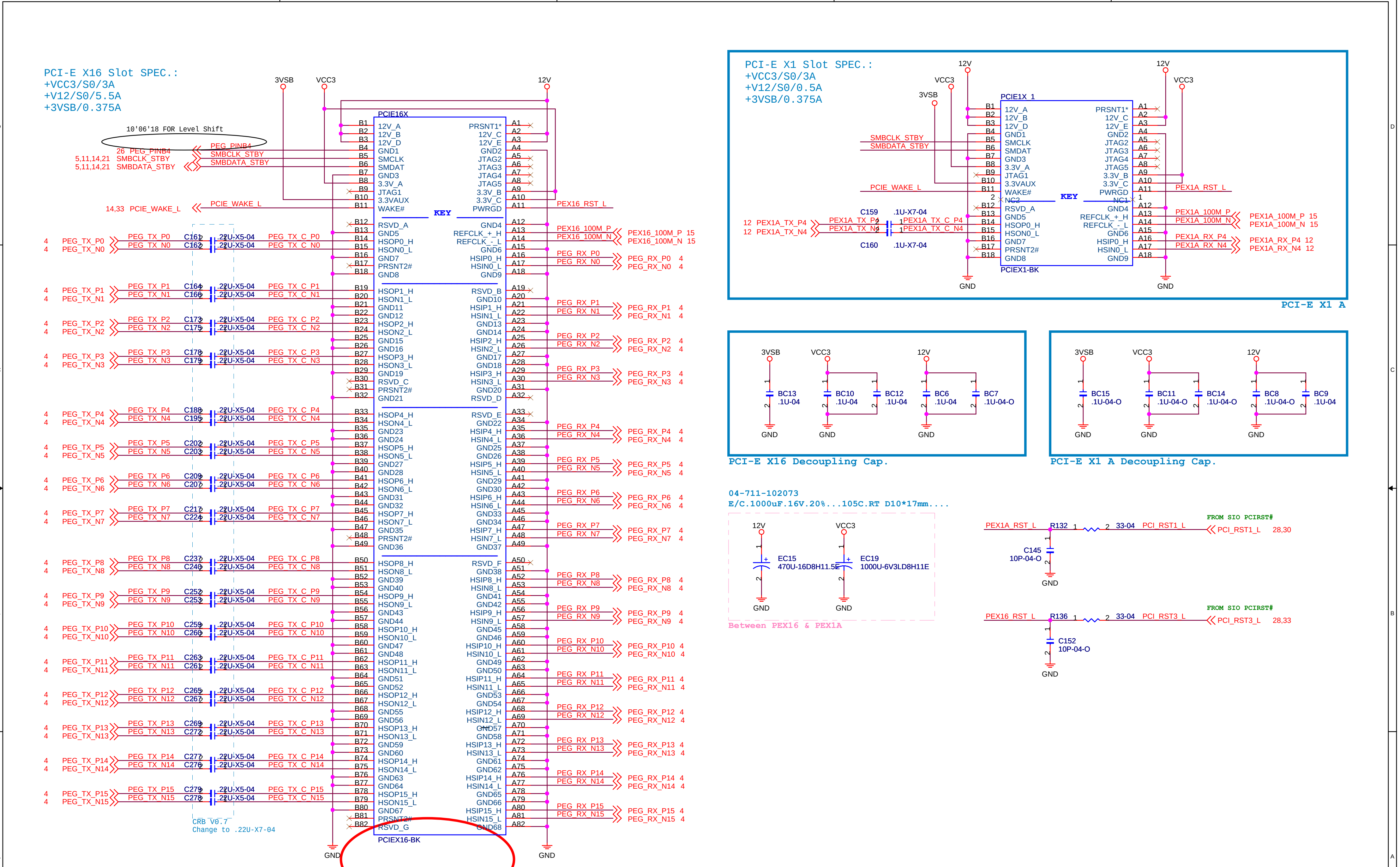

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Title: Slot - PCI-EX16/PCI-EX1

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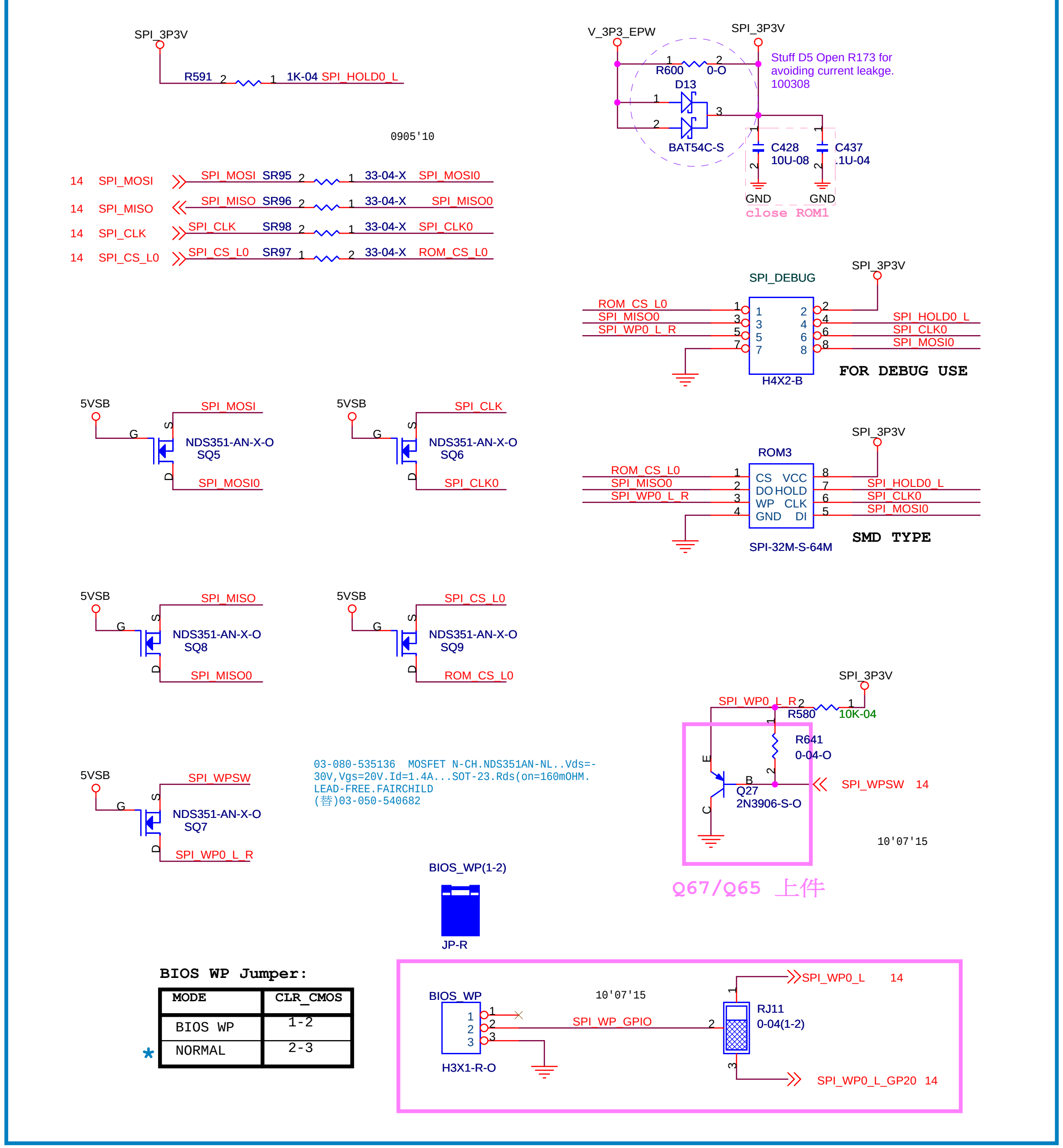
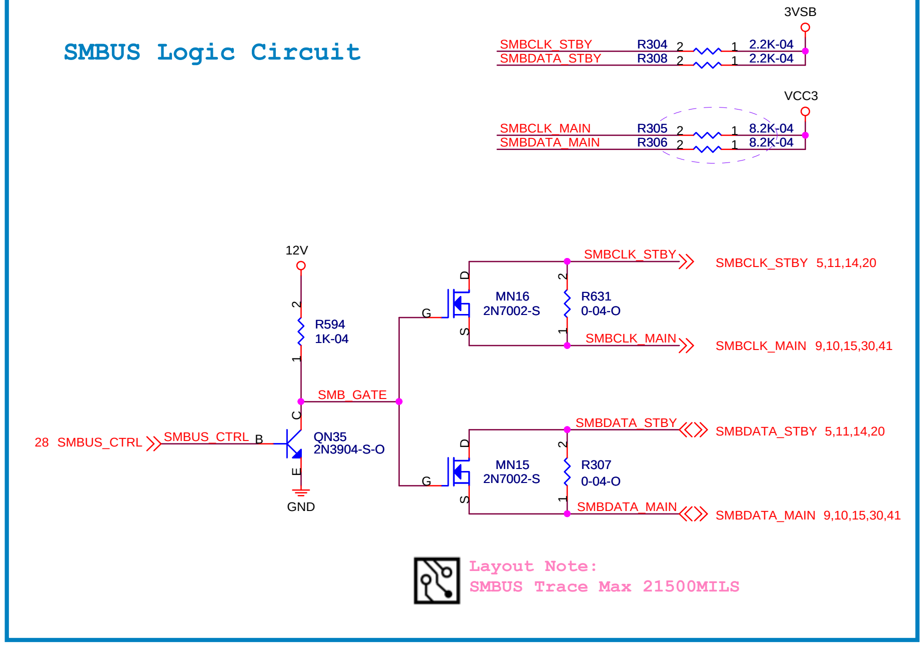
SPI ROM Circuit



BIOS WP Jumper:

MODE	CLR_CMOS
BIOS WP	1-2
* NORMAL	2-3

SMBUS Logic Circuit



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Title	SPI ROM, SMBUS	
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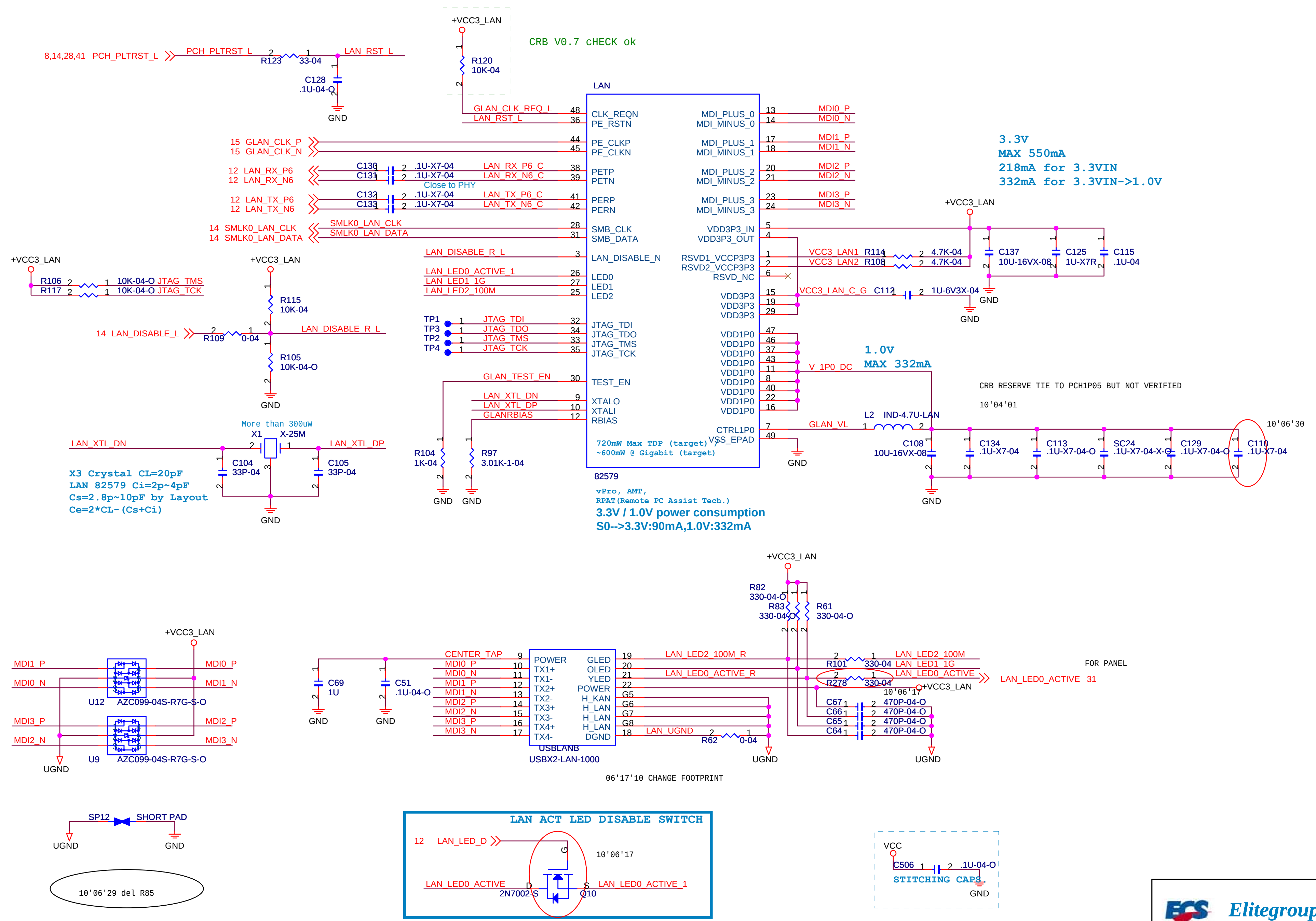

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Title: LAN PHY - 82579, USBLAN

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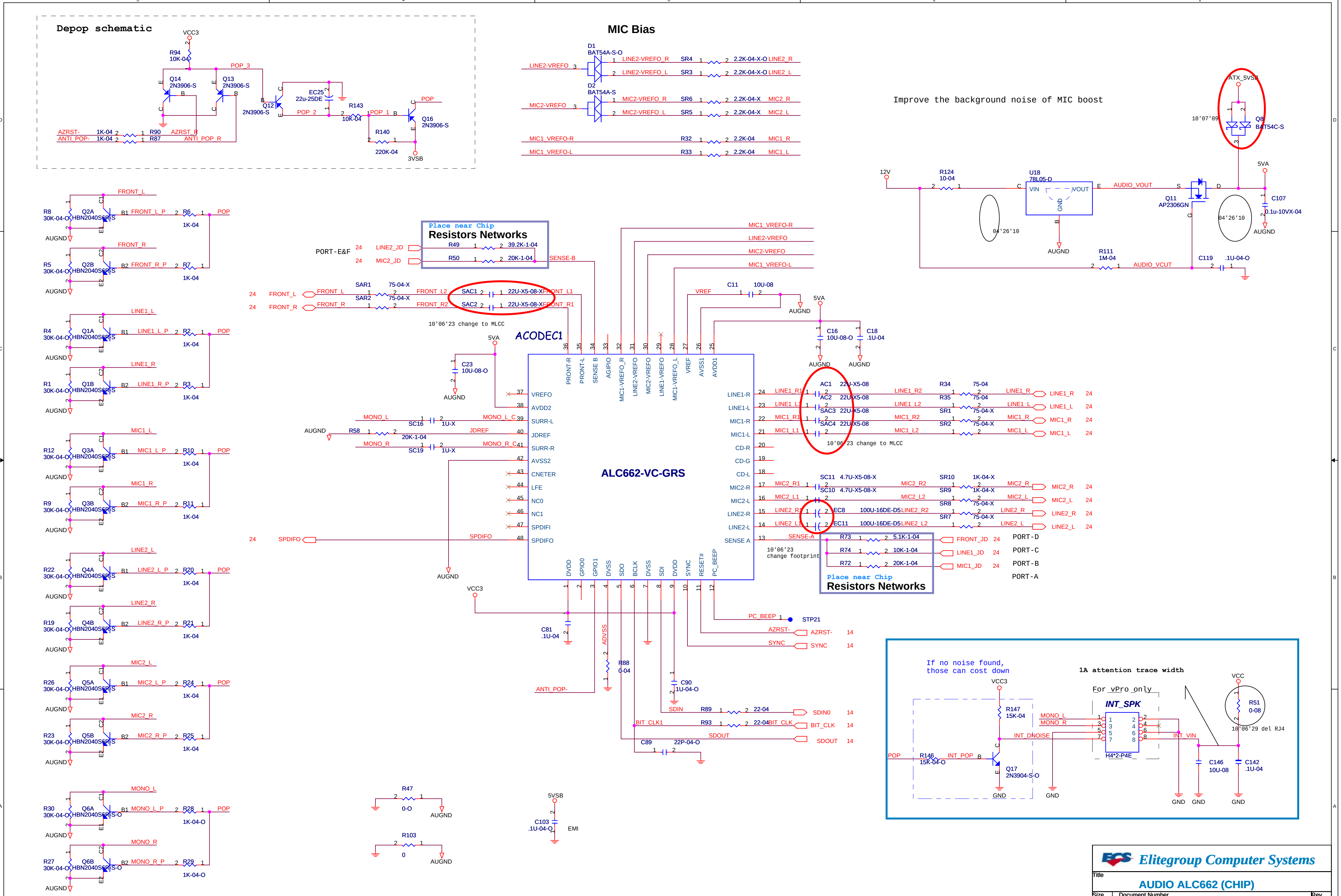

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Title: AUDIO ALC662 (CHIP)

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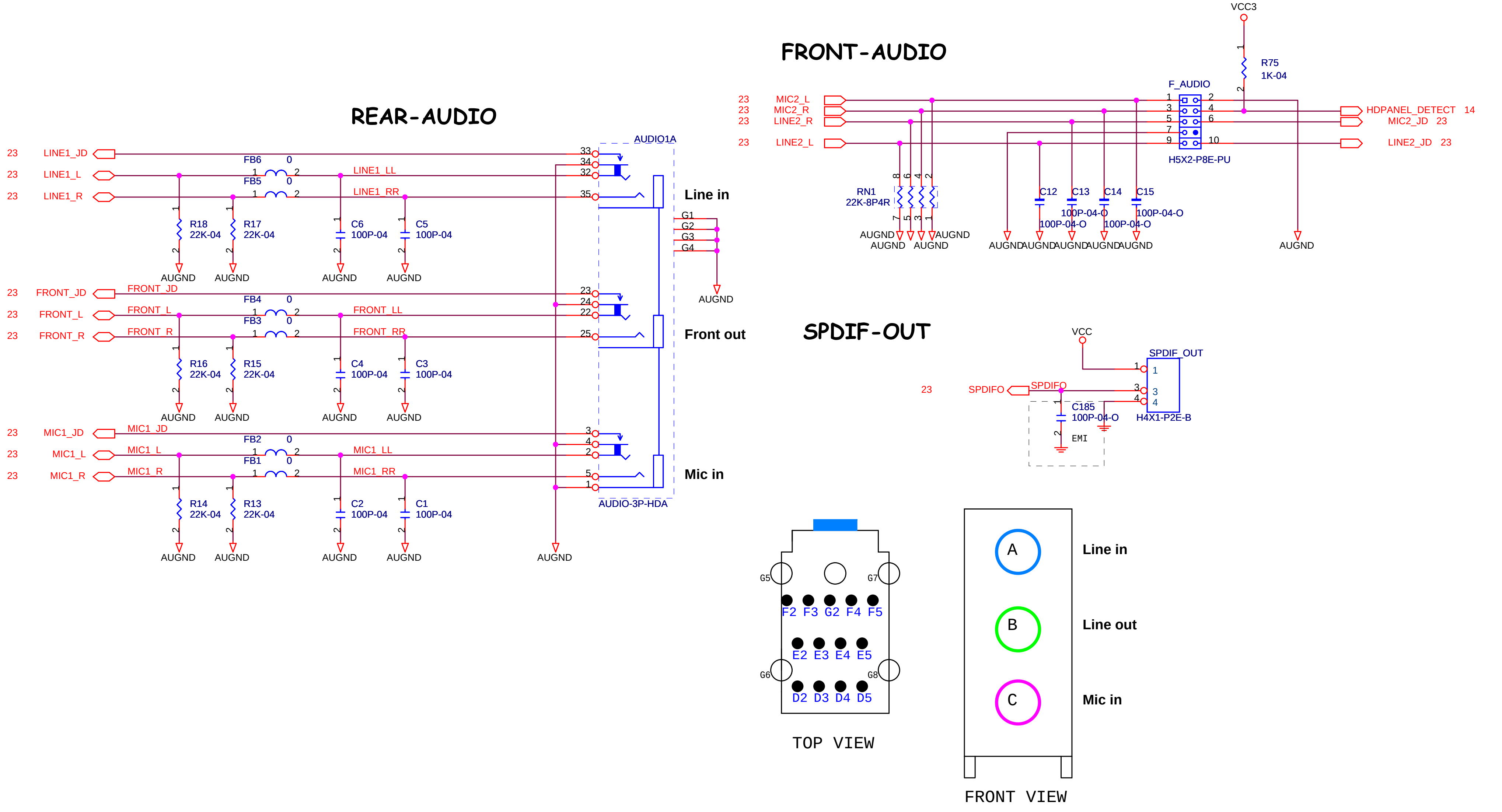

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Title
AUDIO ALC662 (PANEL)

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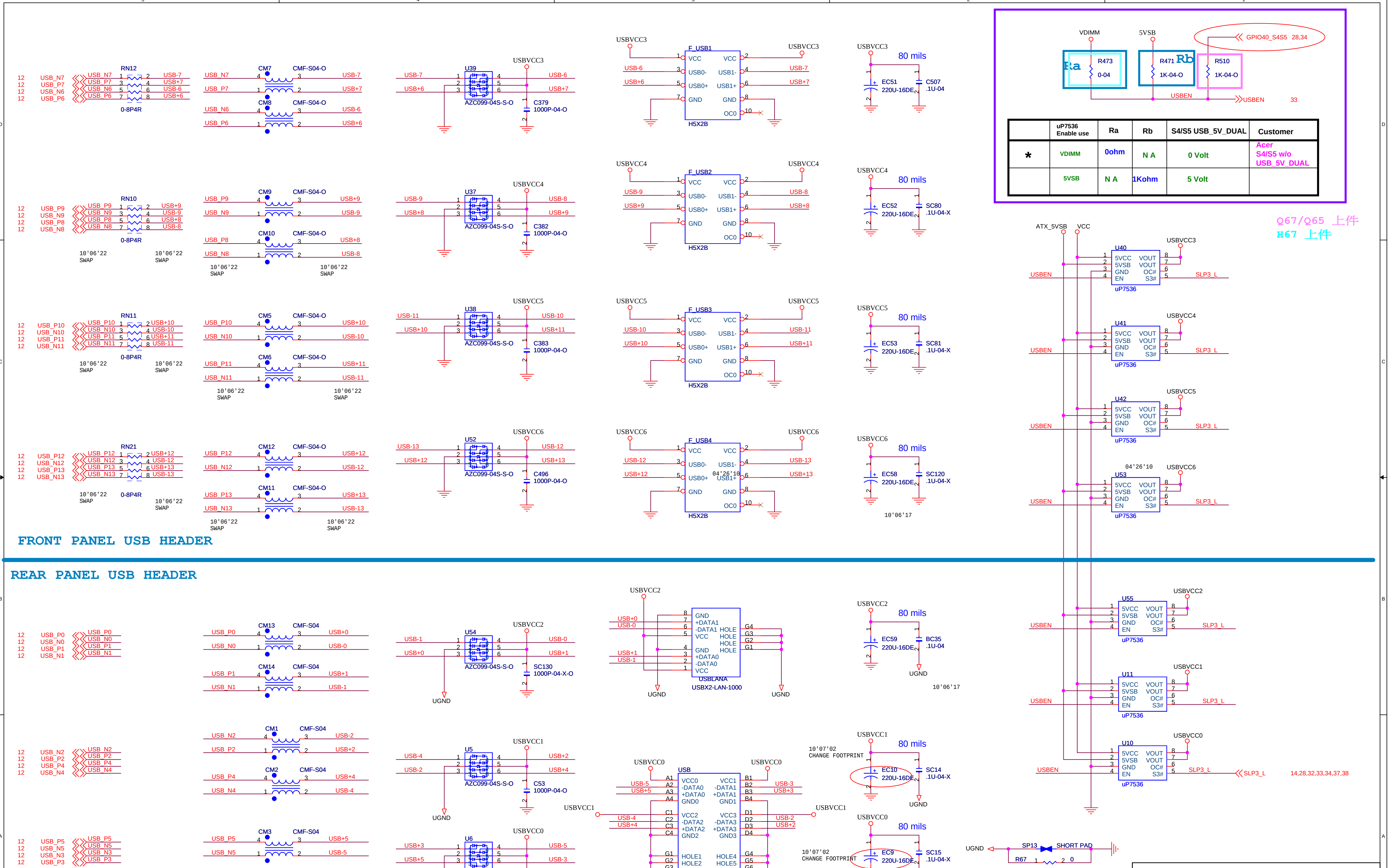

	uP7536 Enable use	Ra	Rb	S4/S5 USB_5V_DUAL	Customer
*	VDIMM	0ohm	N A	0 Volt	Acer S4/S5 w/o USB_5V_DUAL
	5VSB	N A	1Kohm	5 Volt	

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Title: USB - PWR/CONN/HDR

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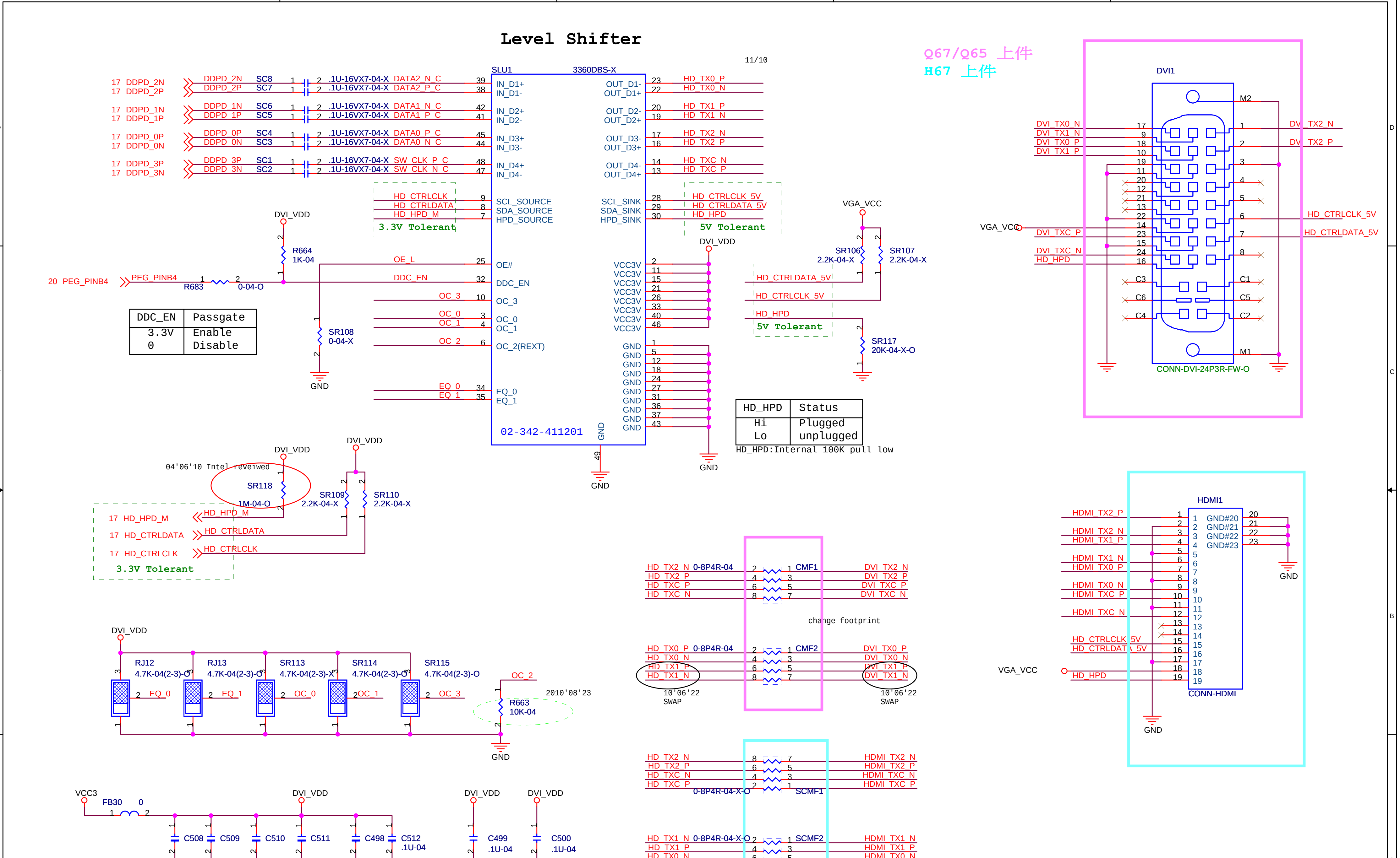
Level Shifter



DDC_EN	Passgate
3.3V	Enable
0	Disable

HD_HPD	Status
Hi	Plugged
Lo	unplugged

HD_HPD:Internal 100K pull low

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Title
DVI HDMI(either one)

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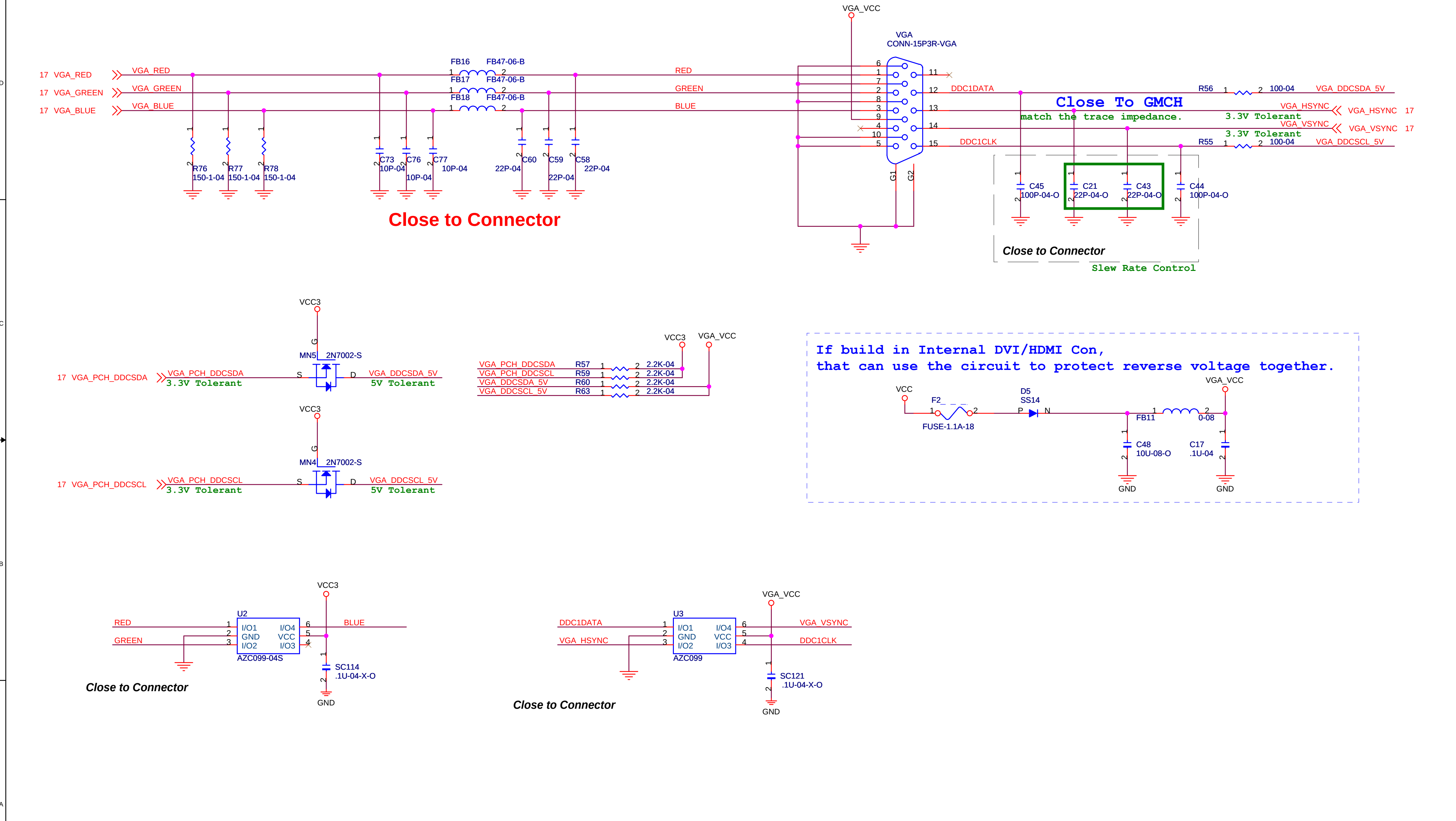

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Title	VGA CONNECTOR
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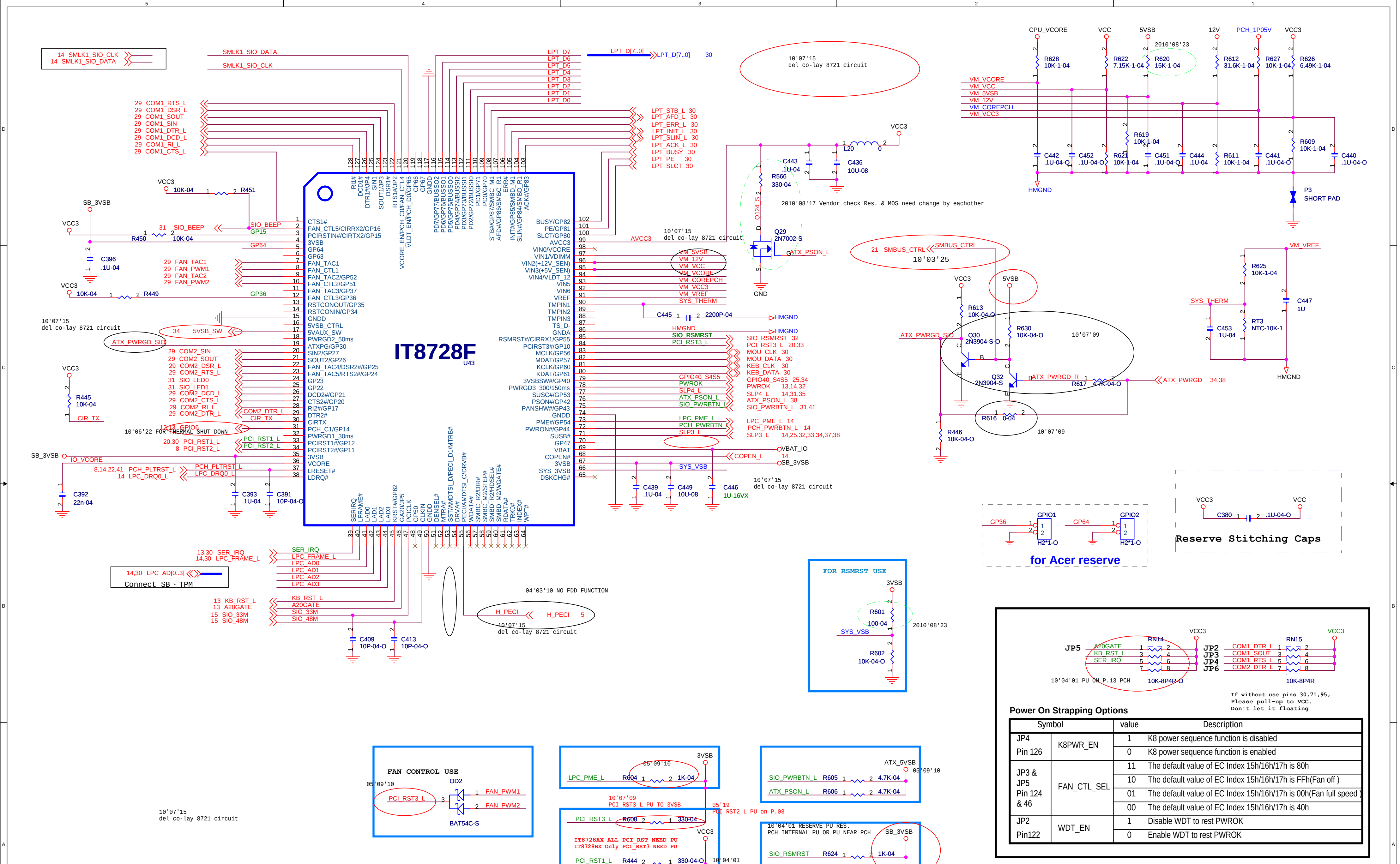

Power On Strapping Options

Symbol		value	Description
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is disabled
		0	K8 power sequence function is enabled
JP3 & JP5 Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 80h
		10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
		01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00	The default value of EC Index 15h/16h/17h is 40h
JP2 Pin122	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK

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Title: SIO IT8720F

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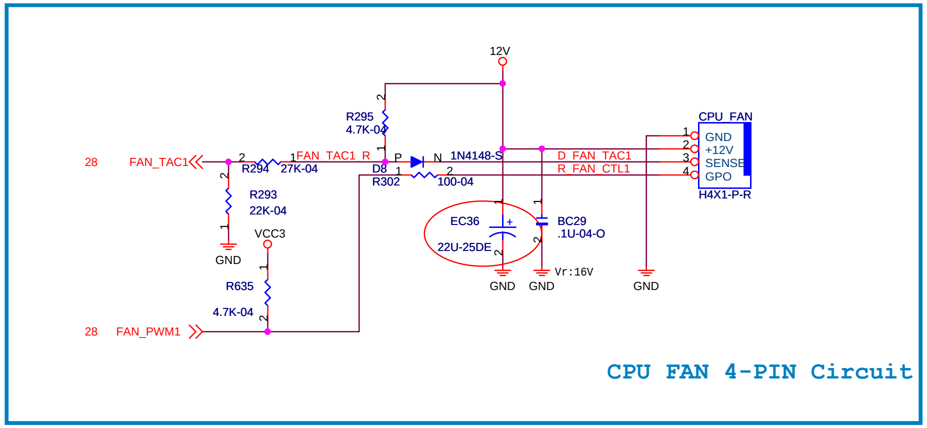

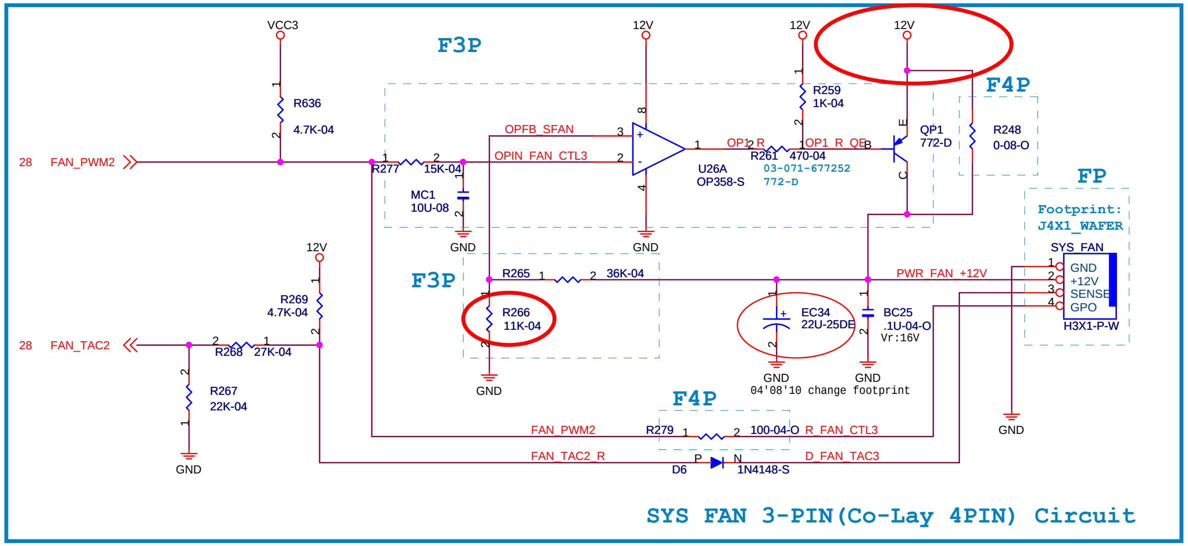

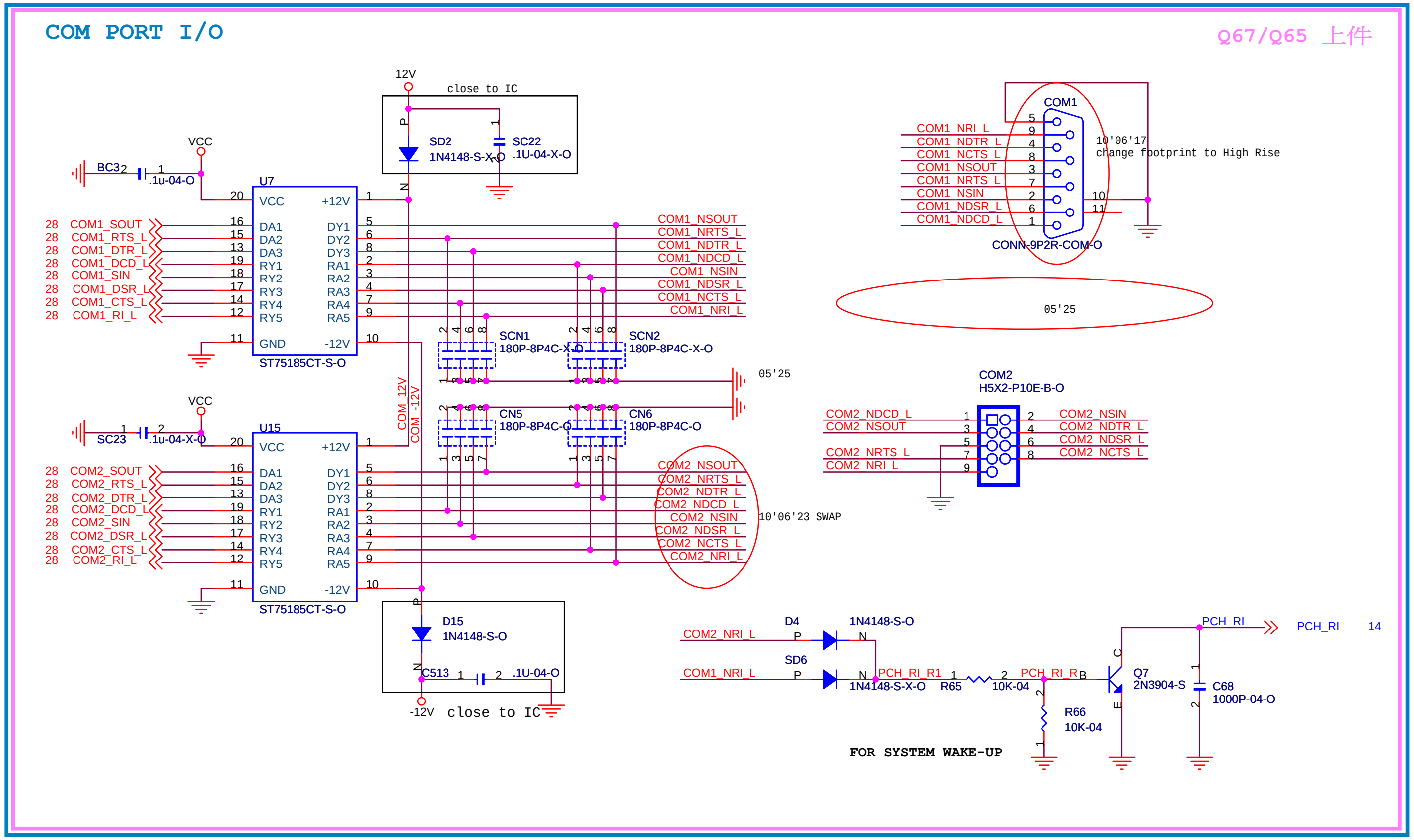

PWR FAN:

MODE	F3P	F4P	FP Value
* 3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

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Title: FAN, COM

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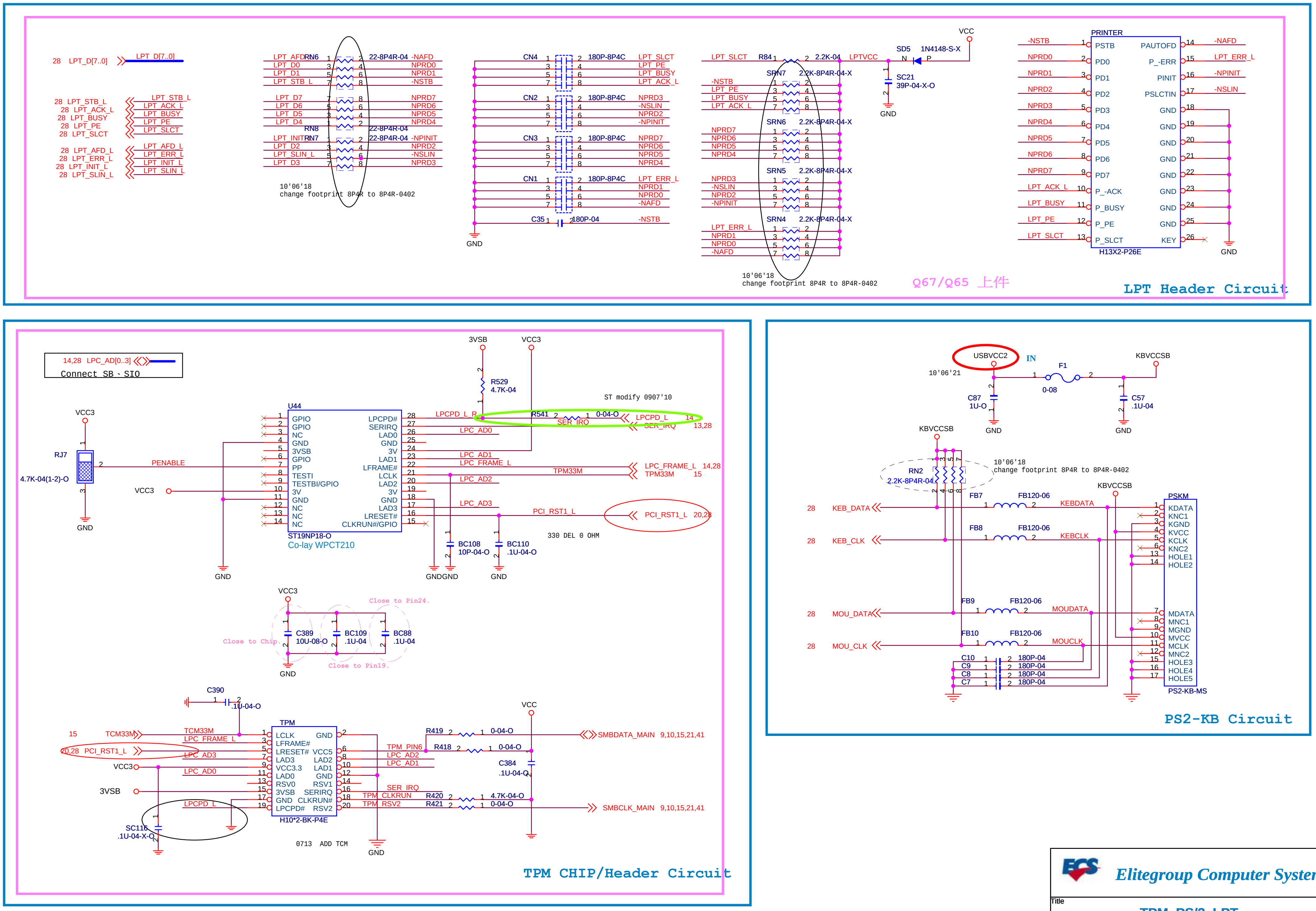

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Title: TPM, PS/2, LPT

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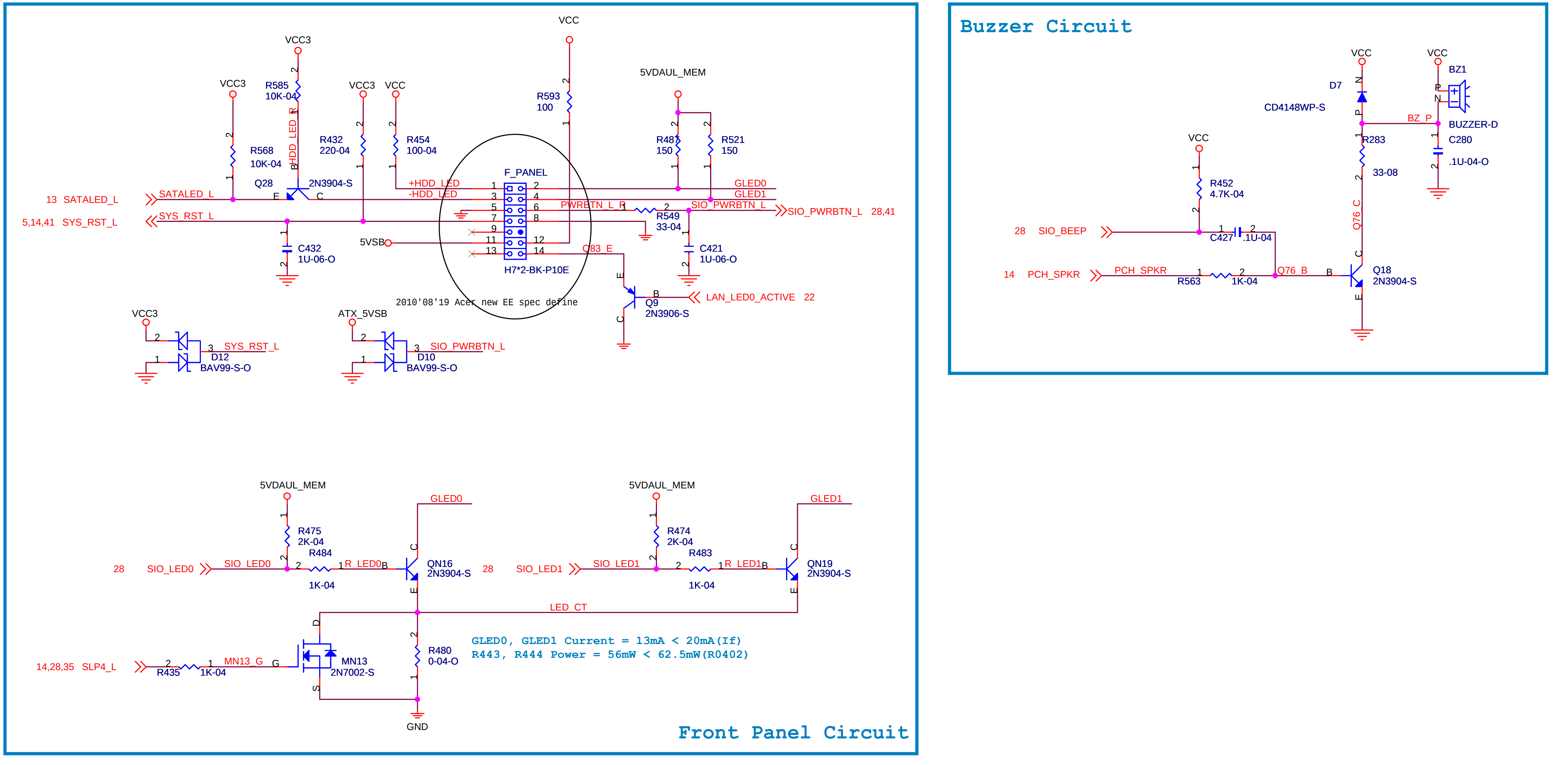

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Title	F_PANEL, BUZ	
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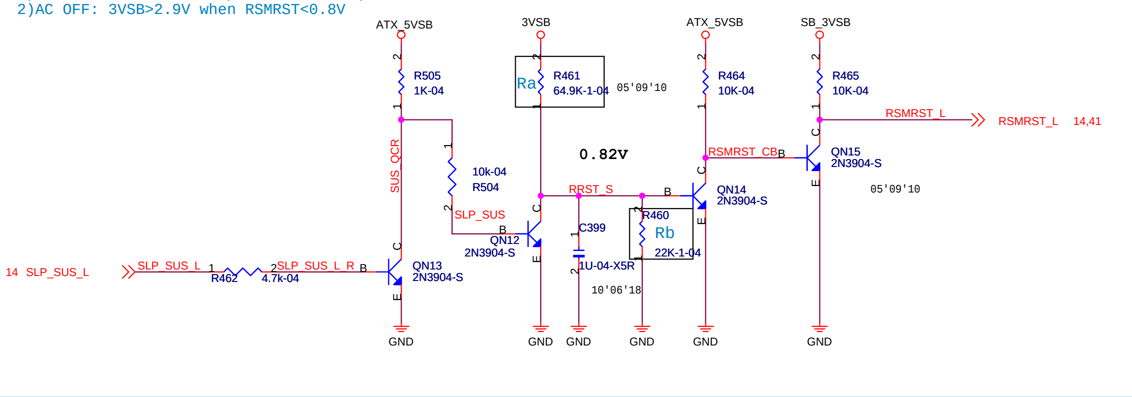
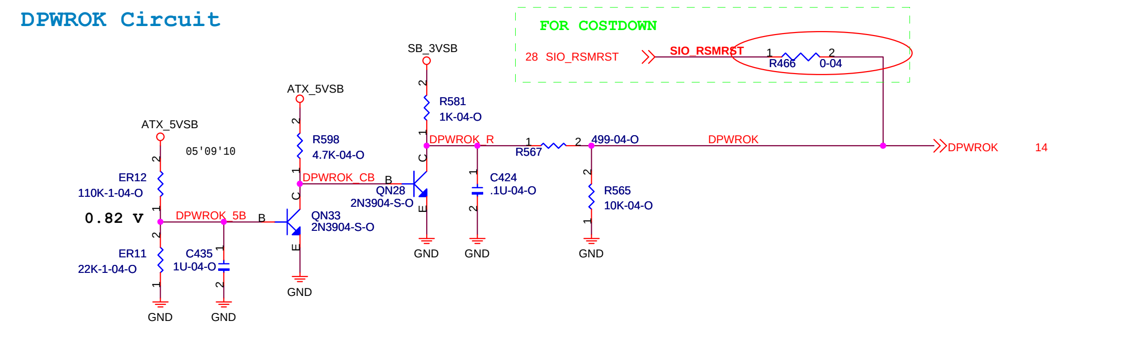
RSMRST Circuit

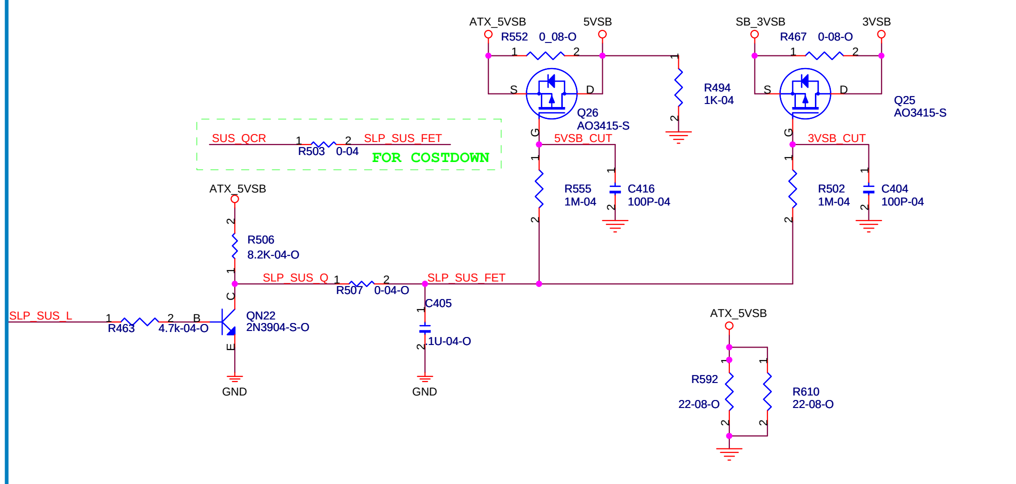
MODIFY Ra/Rb VALUE FOR FOLLOWING RULES
1)AC ON: 3VSB vs RSMRST(t204: min 10ms)
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V

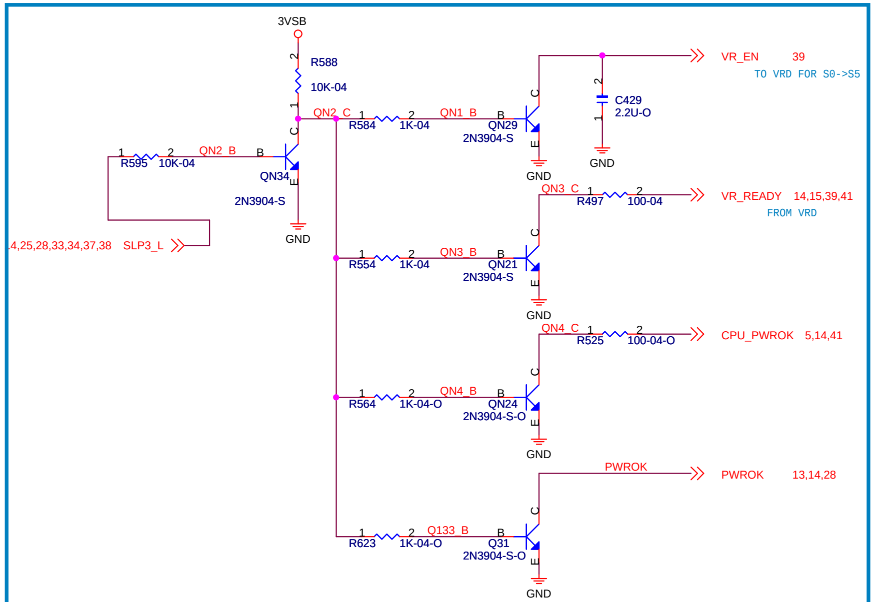


DPWROK Circuit

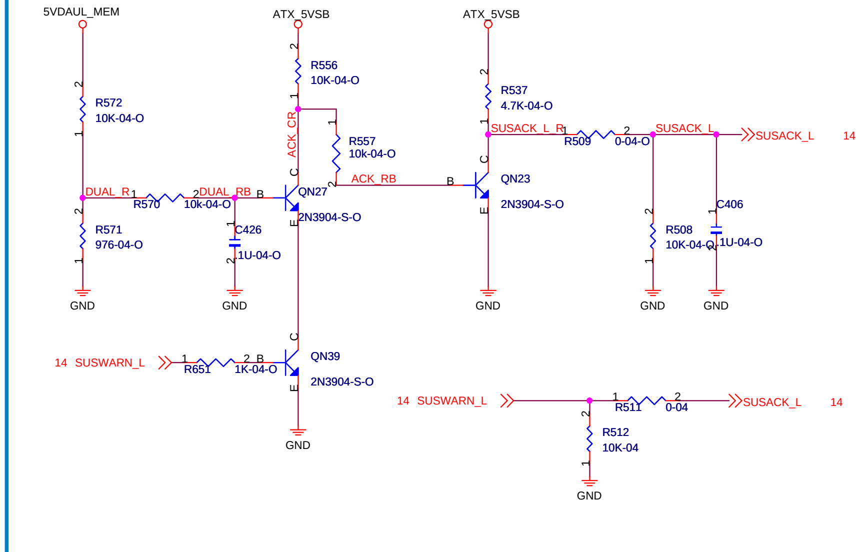


SUS_3/5VSB SWITCH





Power Down Sequencing Circuit



SUSACK_L CTRL CIRCUIT

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Title
SEQUENCE/ DSW CKT

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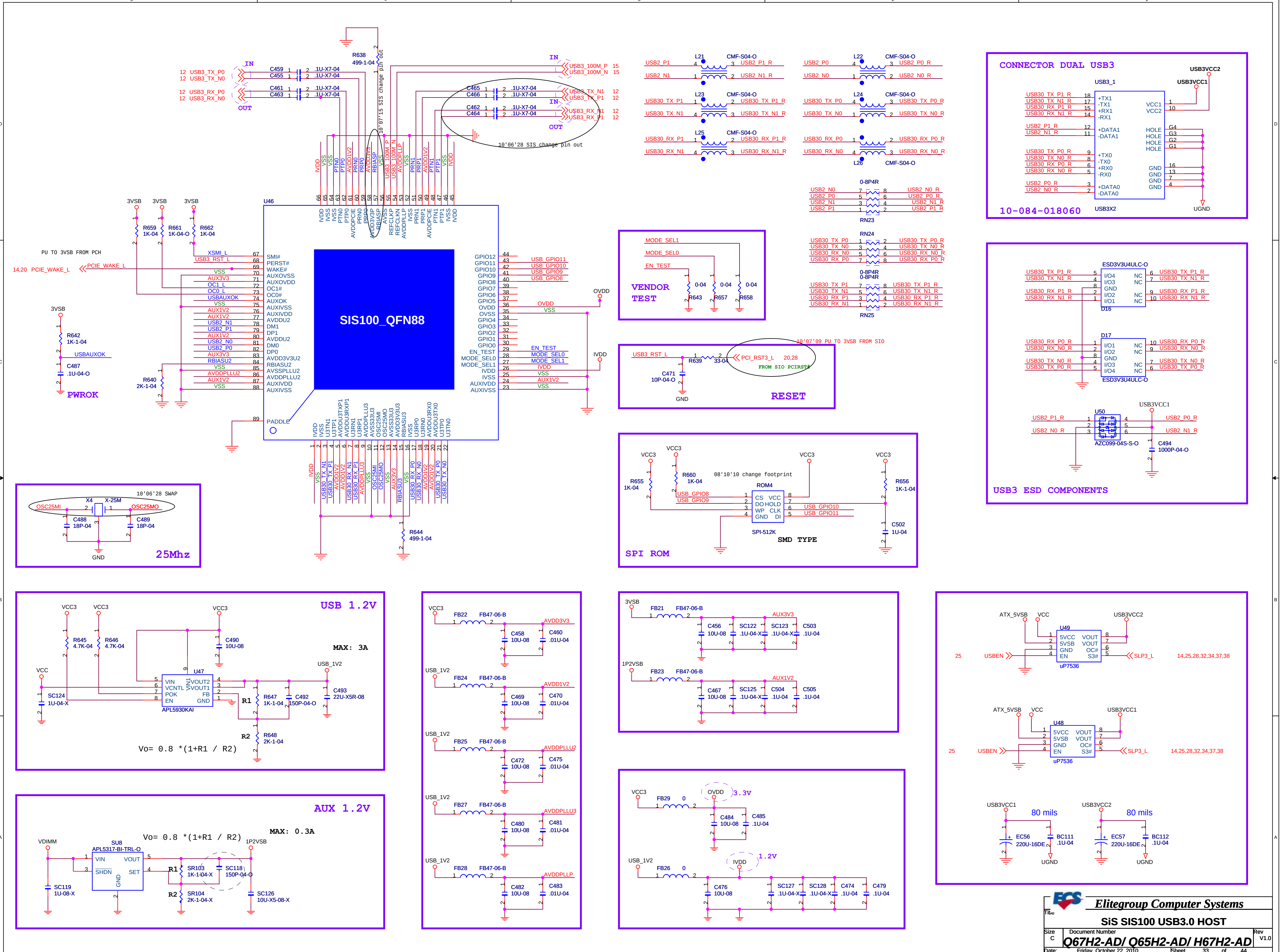

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Title: SiS SIS100 USB3.0 HOST

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C	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0

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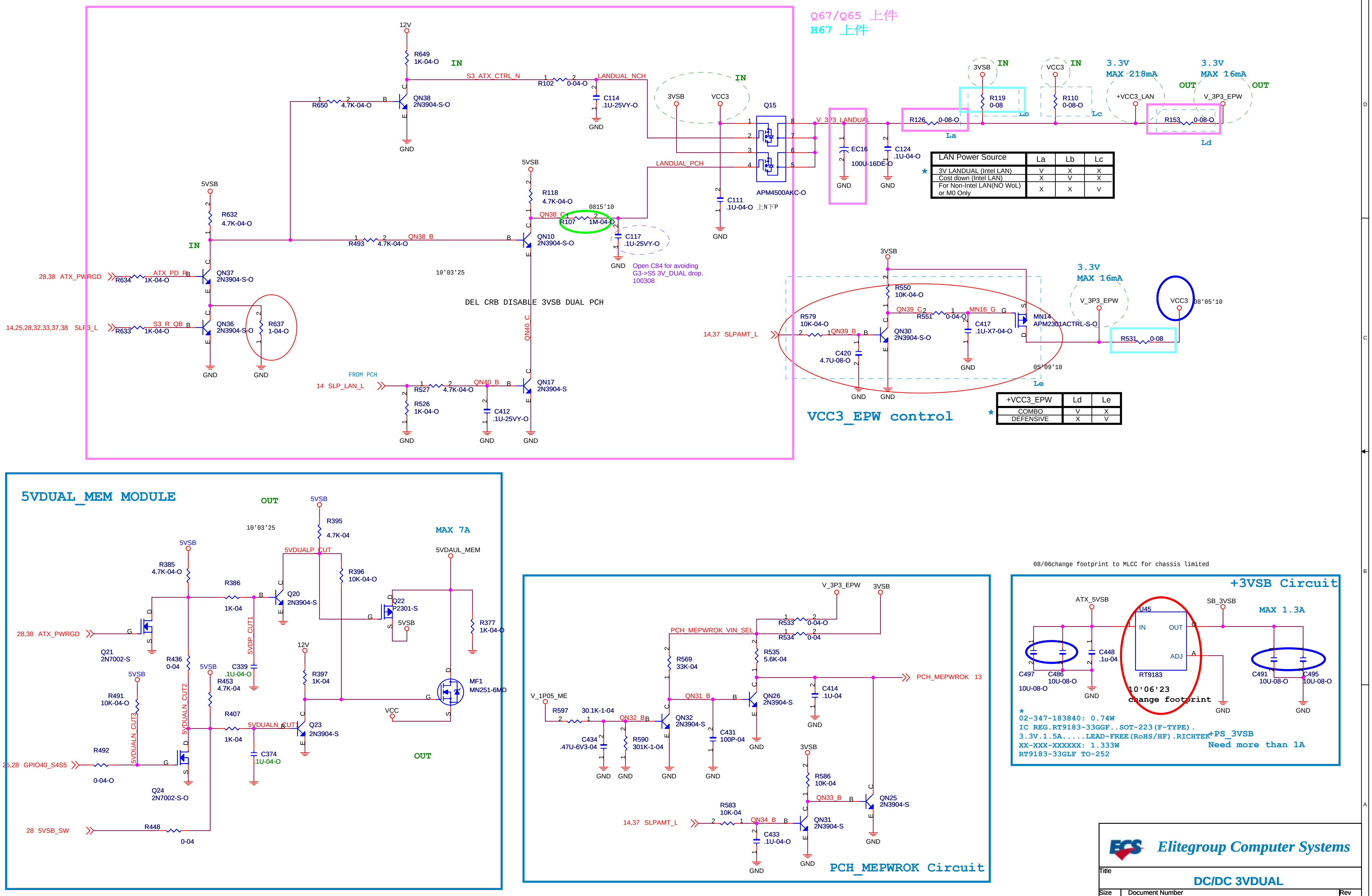

LAN Power Source	La	Lb	Lc
3V LANDUAL (Intel LAN)	V	X	X
Cost down (Intel LAN)	X	V	X
For Non-Intel LAN(NO WoL) or M0 Only	X	X	V

+VCC3_EPW	Ld	Le
COMBO	V	X
DEFENSIVE	X	V

08/06change footprint to MLCC for chassis limited

*
02-347-183840: 0.74W
IC REG.RT9183-33GGF..SOT-223(F-TYPE).
3.3V.1.5A.....LEAD-FREE(RoHS/HF).RICHTEK
XX-XXX-XXXXXX: 1.333W
RT9183-33GLF TO-252

Elitegroup Computer Systems

Title: DC/DC 3VDUAL

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

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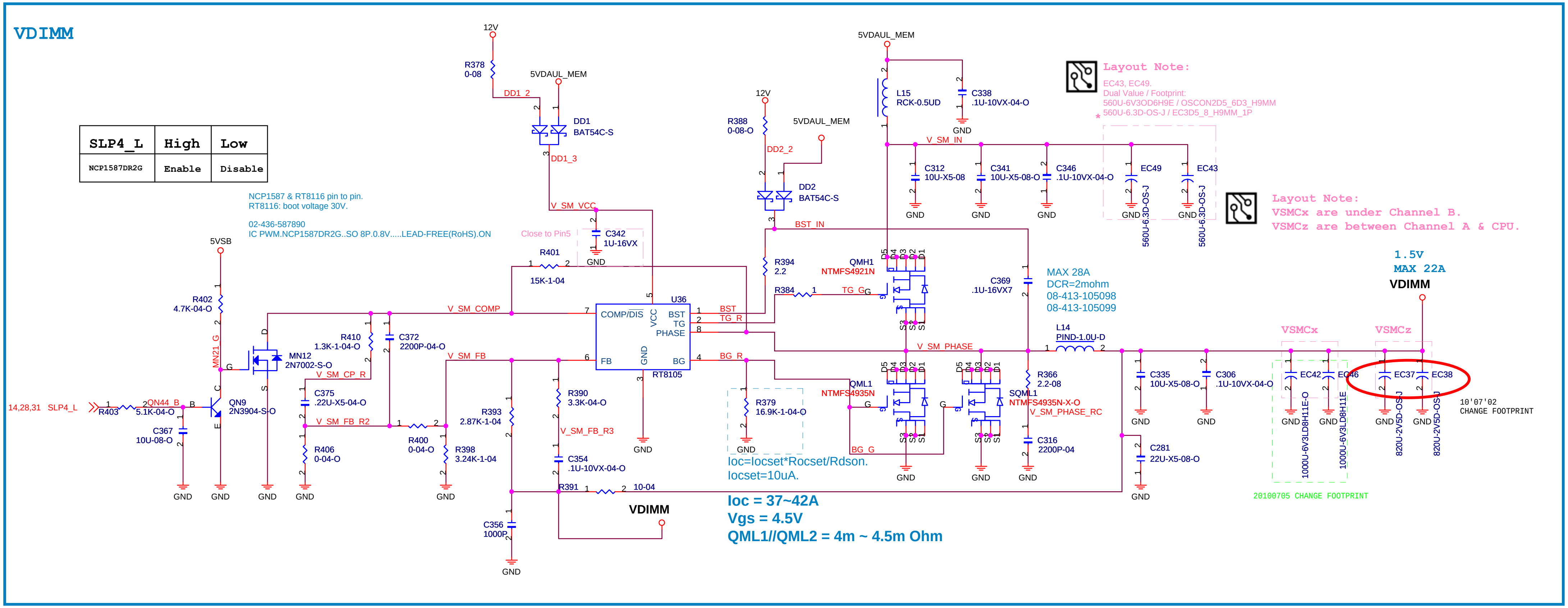

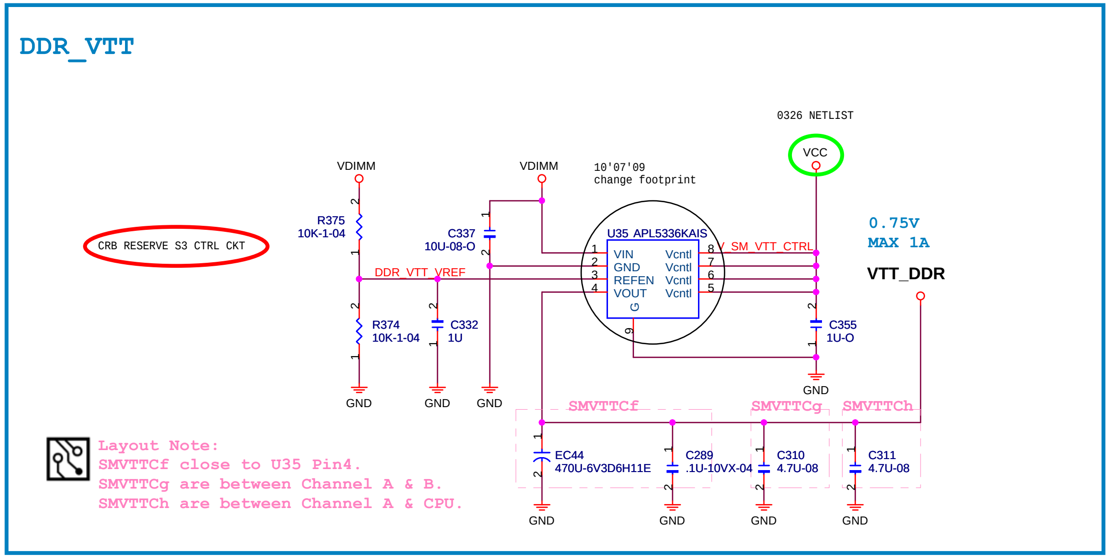

Elitegroup Computer Systems

Title	DC/DC VDIMM/DDR_VTT/5VDUAL
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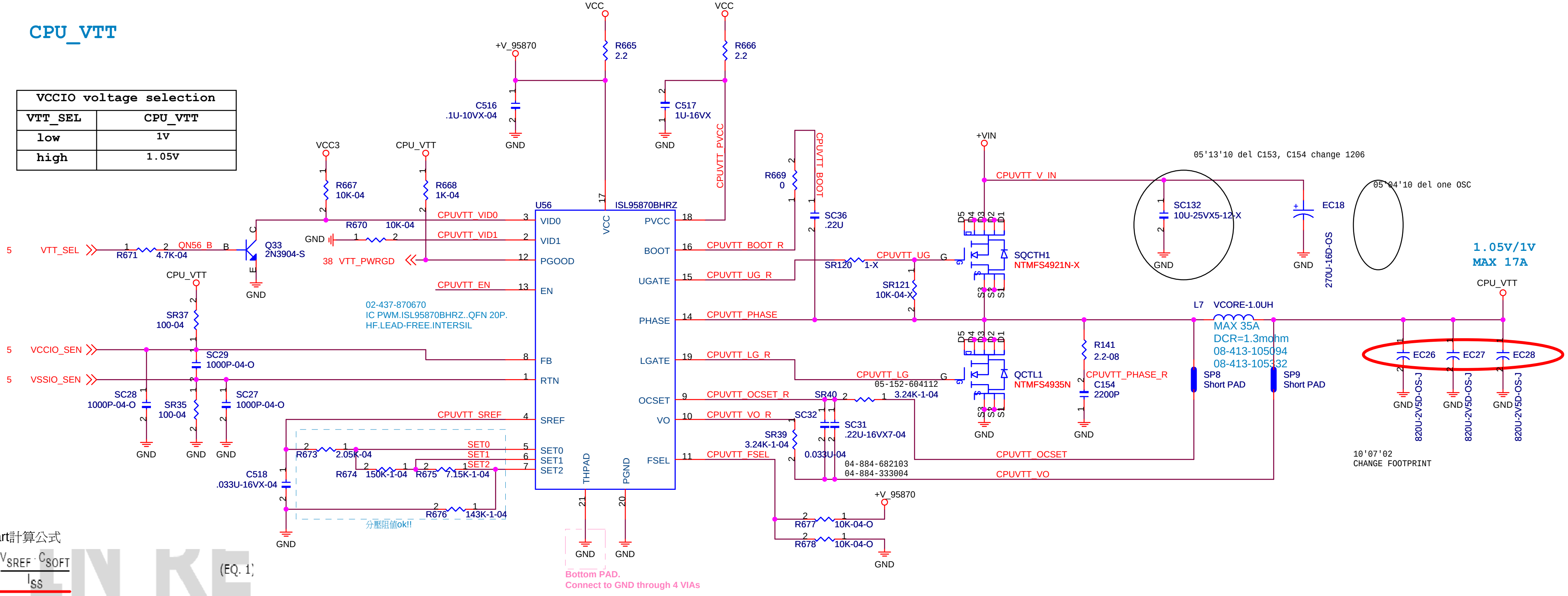
CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad \text{(EQ. 1)}$$

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

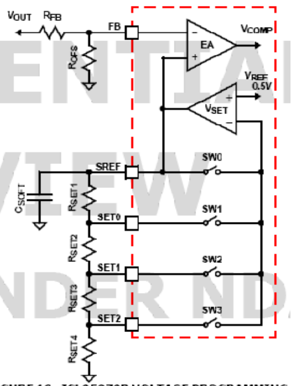
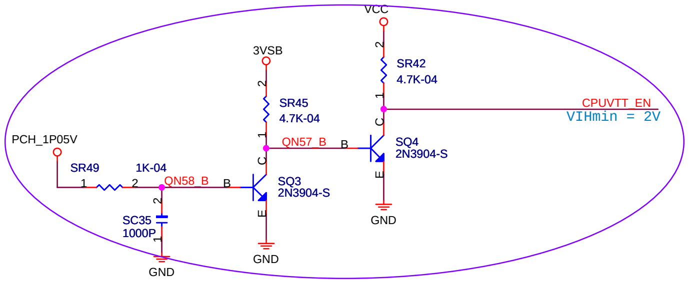


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT



Elitegroup Computer Systems

Title	DC/DC V_CPUVTT		
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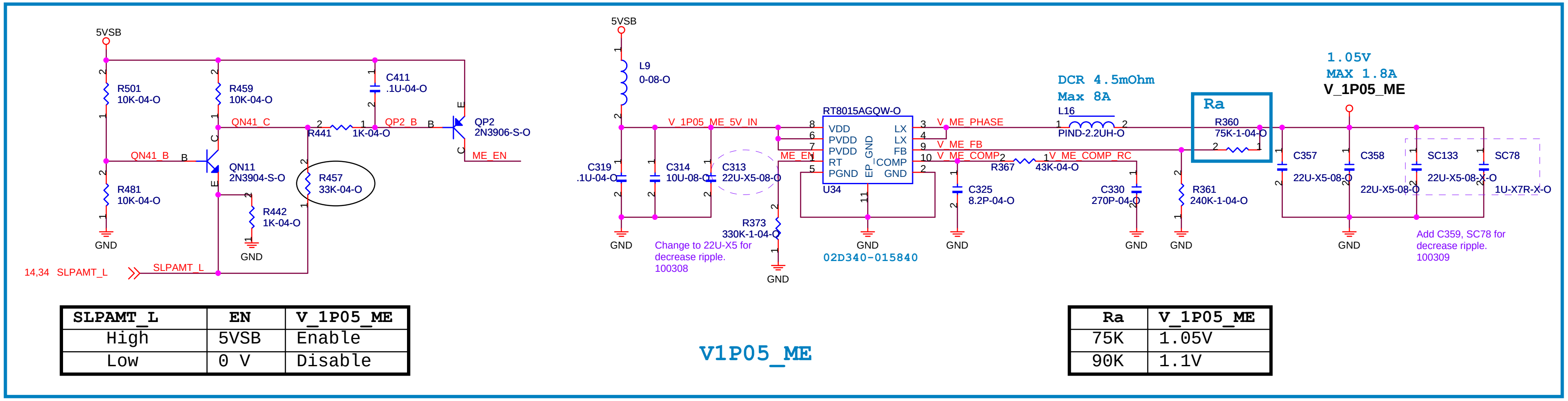
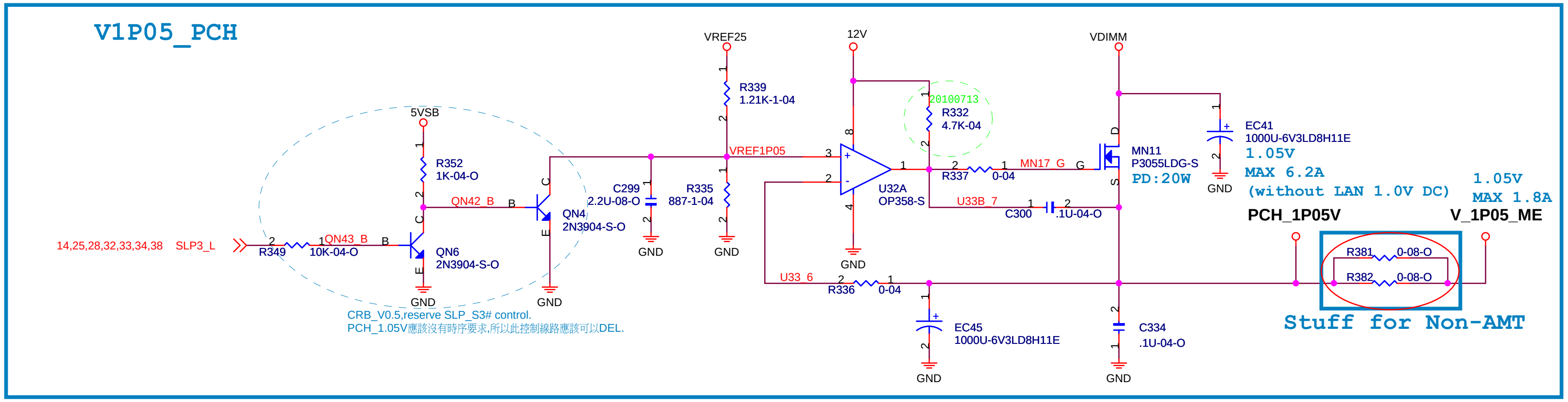


SLPAMT_L	EN	V_1P05_ME
High	5VSB	Enable
Low	0 V	Disable

Ra	V_1P05_ME
75K	1.05V
90K	1.1V



BOM Note:

02-340-015840....dfn10_rt8106a
IC REG.RT8015AGQW.WDFN 10P.3A.LEAD-FREE(RoHS/HF).
RICHTEK

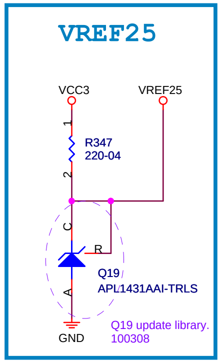
08-413-225094....choke_2r2m_pt4d9x4d6mm
POWER IND.2.2uH.20%.8A.4.5m OHM.DIP 2P.8.2*8.2*7.5*6.7
mm.AKL0806MN-2R2M-L3.2....LEAD-FREE(RoHS).MAGIC

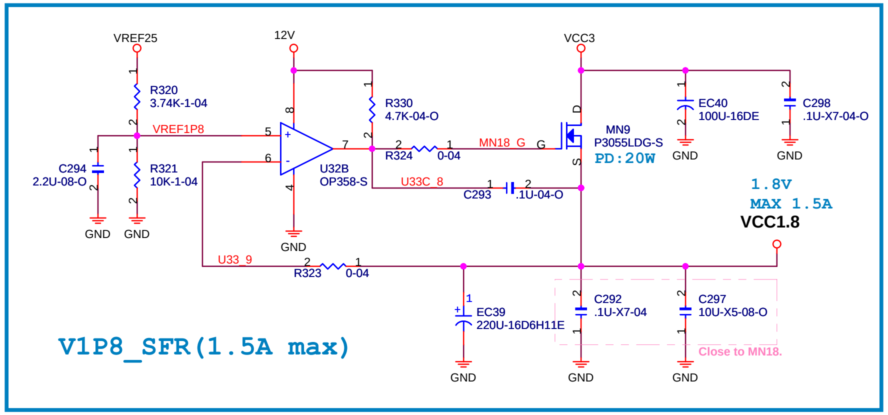
05-152-750113
RES.75K.1/16W.1%..SMD 0402......LEAD-FREE(RoHS/HF).

05-152-430103
RES.43K.1/16W.5%..SMD 0402......LEAD-FREE(RoHS/HF).

05-152-240114
RES.240K.1/16W.1%..SMD 0402......LEAD-FREE(RoHS/HF).

04-880-828100
C/C.8.2pF.50V.0.25pf..NPO...SMD 0402....LEAD-FREE(RoHS/HF).





Elitegroup Computer Systems

Title	DC/DC V1P05_PCH,ME/V1P8_SFR	
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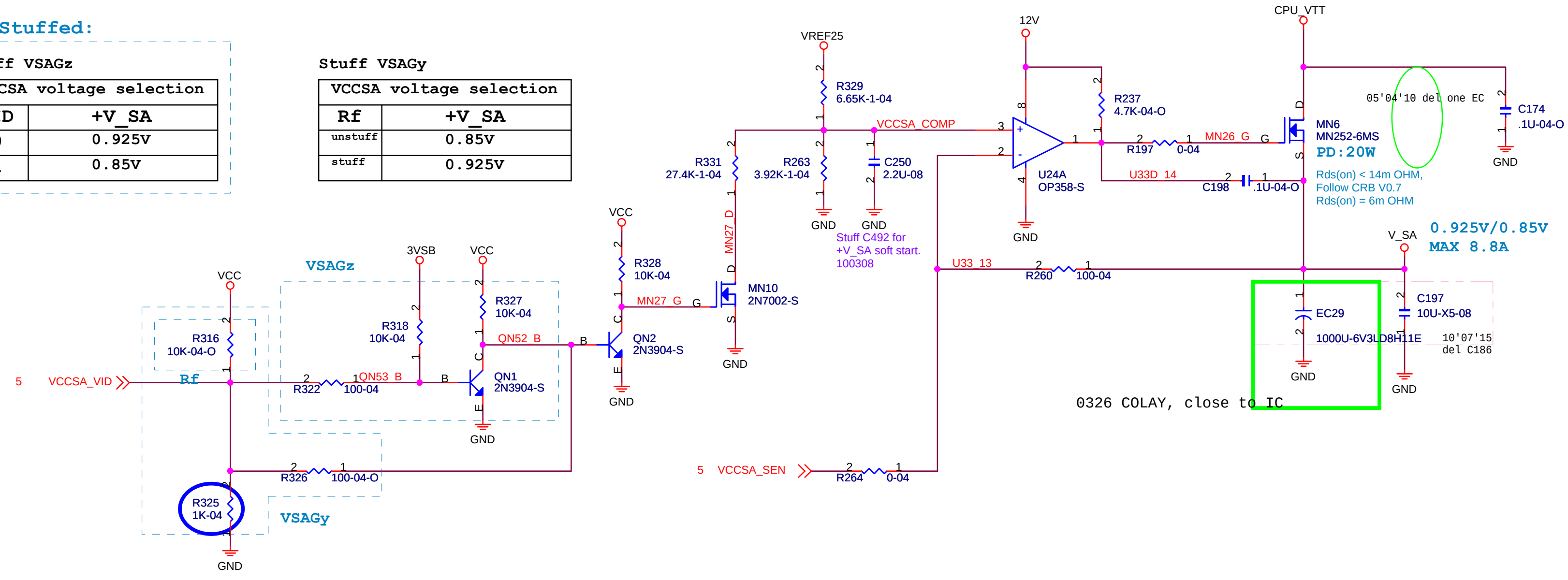
Default Stuffed:

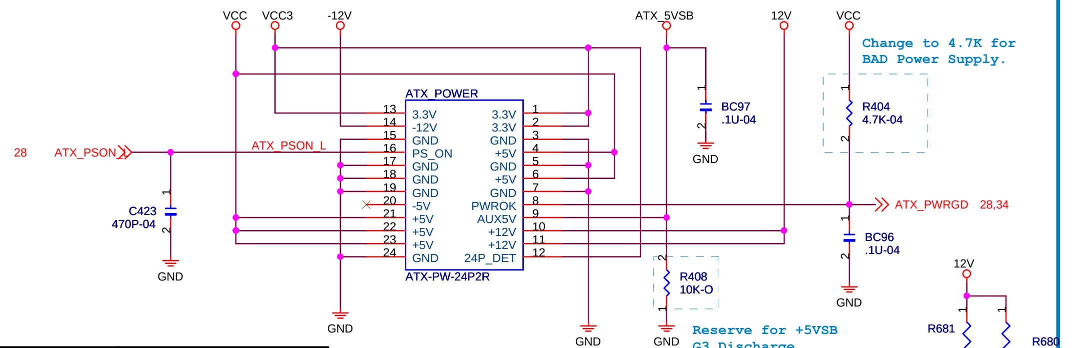
Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
* 1	0.85V

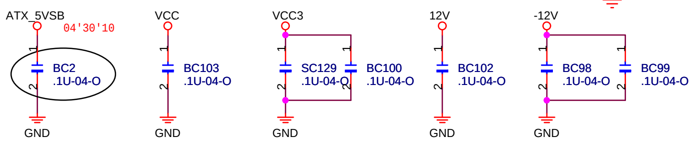
Stuff VSAGy

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V



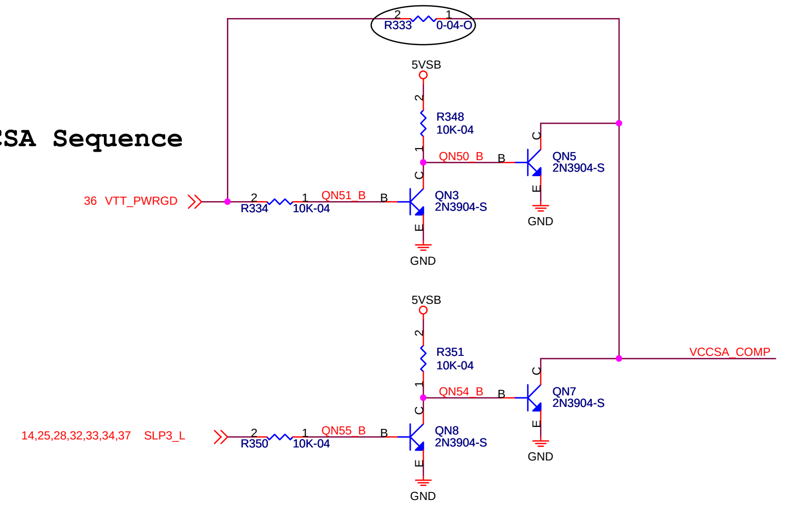


OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0



ATX Power 24PIN

VCCSA Sequence



Elitegroup Computer Systems

Title: DC/DC VCCSA, ATXPWR

Size	Document Number	Rev
Custom	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0

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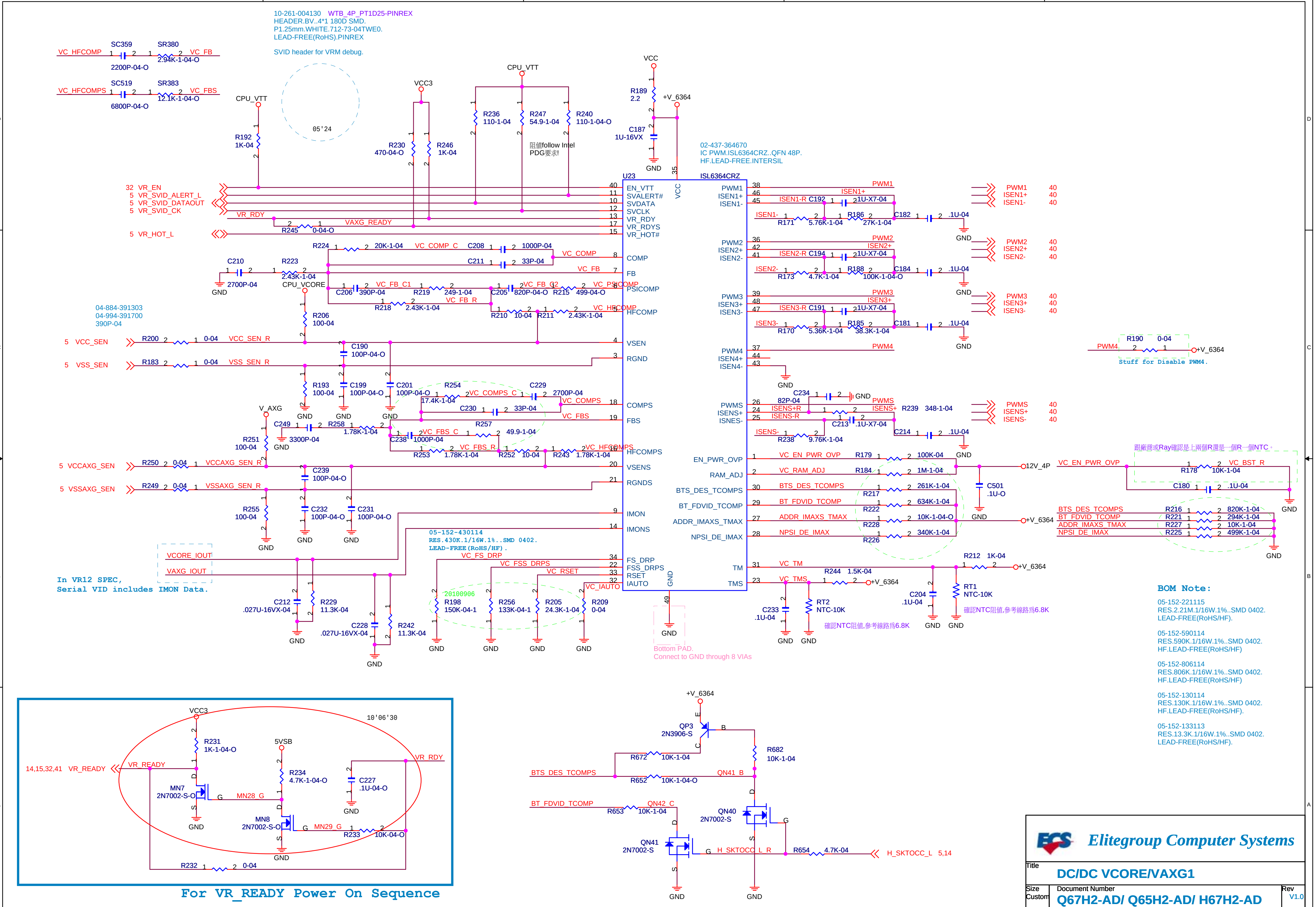

BOM Note:

05-152-221115
RES.2.21M.1/16W.1%..SMD 0402.
LEAD-FREE(RoHS/HF).

05-152-590114
RES.590K.1/16W.1%..SMD 0402.
HF.LEAD-FREE(RoHS/HF)

05-152-806114
RES.806K.1/16W.1%..SMD 0402.
HF.LEAD-FREE(RoHS/HF)

05-152-130114
RES.130K.1/16W.1%..SMD 0402.
HF.LEAD-FREE(RoHS/HF).

05-152-133113
RES.13.3K.1/16W.1%..SMD 0402.
LEAD-FREE(RoHS/HF).

Elitegroup Computer Systems

Title	DC/DC VCORE/VAXG1	
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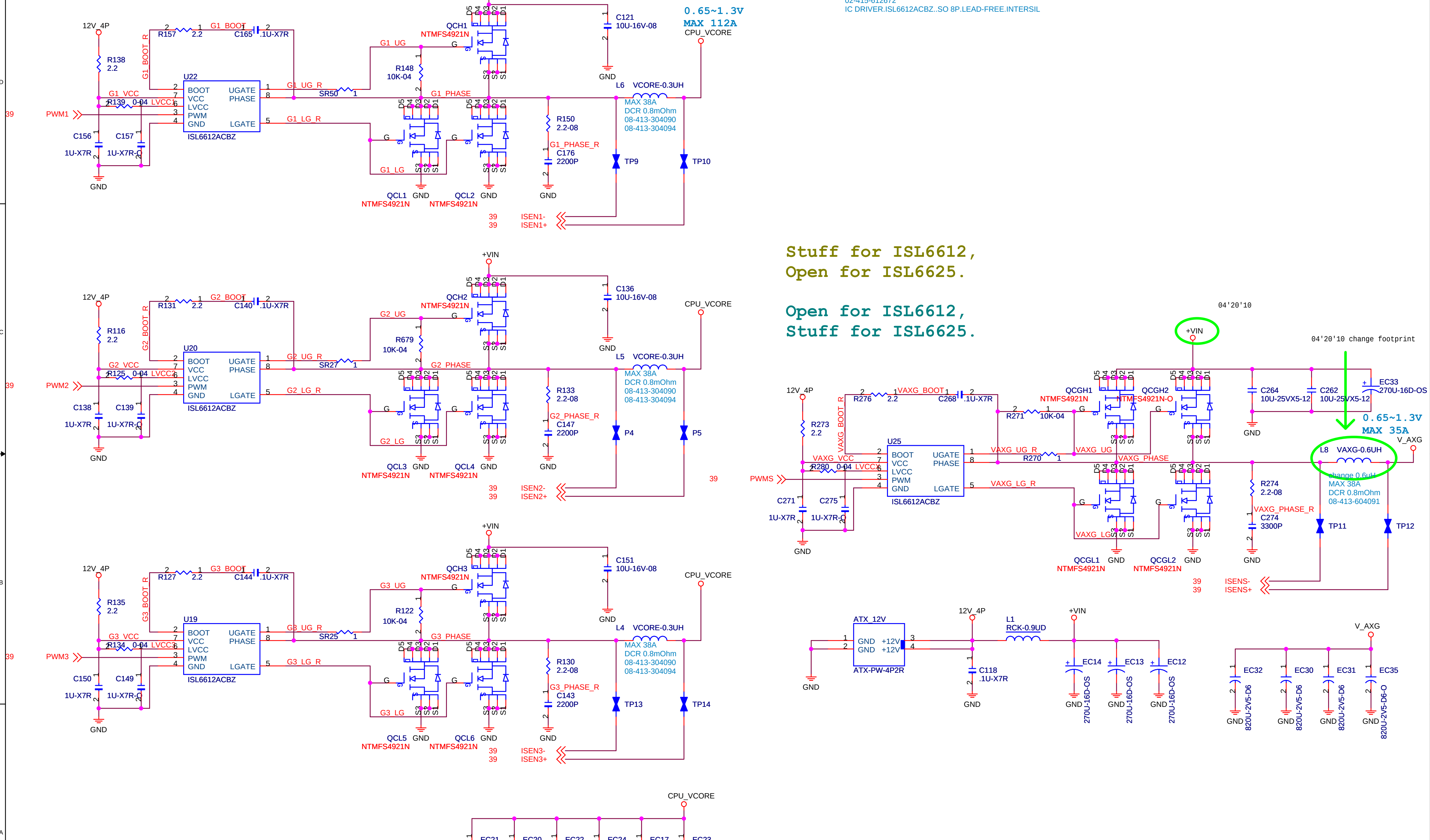
**Vcore先4 phases上1下2,placement放不下再改3相上2下2.
**ISL6625明天Q1底才有sample,先用ISL6612CB.



Elitegroup Computer Systems

Title: DC/DC VCORE/VAXG2

Size	Document Number	Rev
Custom	Q67H2-AD/ Q65H2-AD/ H67H2-AD	V1.0

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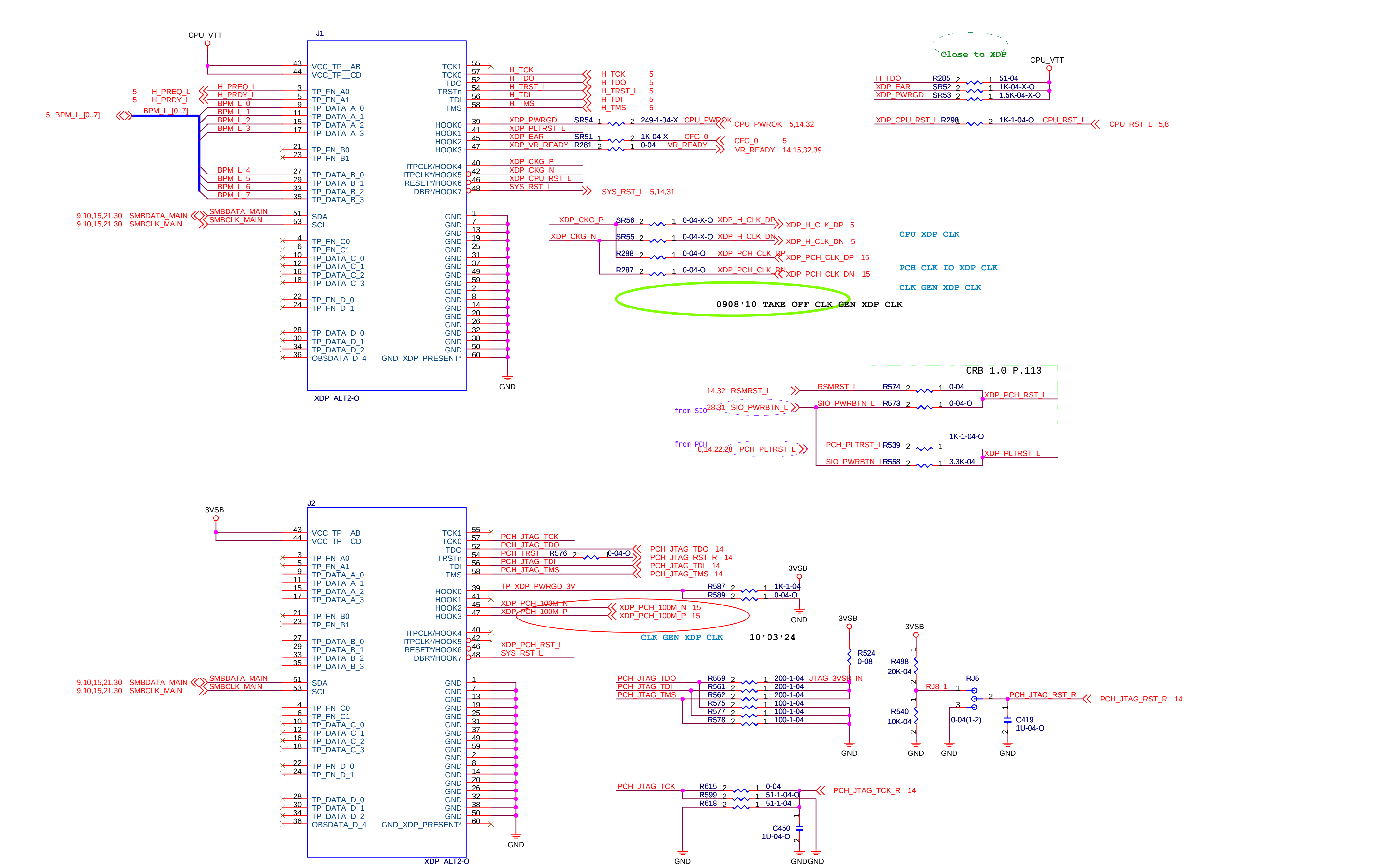

DESIGN NOTE:
PCH JTAG

DESIGN NOTE:
DEFENSIVE DESIGN

Elitegroup Computer Systems

Title: XDP

Size: Custom | Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD | Rev: V1.0

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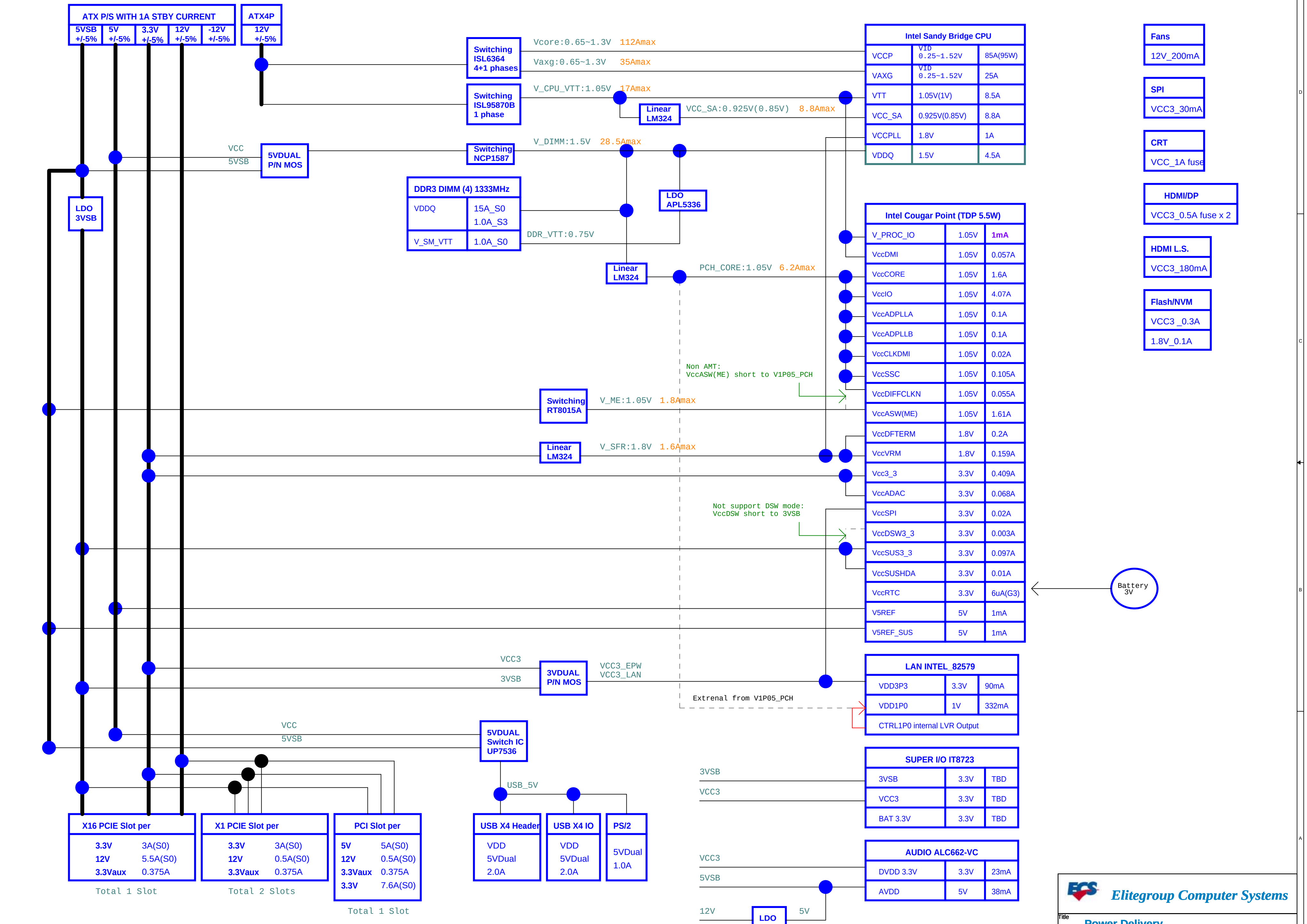

Elitegroup Computer Systems

Title	Power Delivery
Size	C
Document Number	Q67H2-AD/ Q65H2-AD/ H67H2-AD
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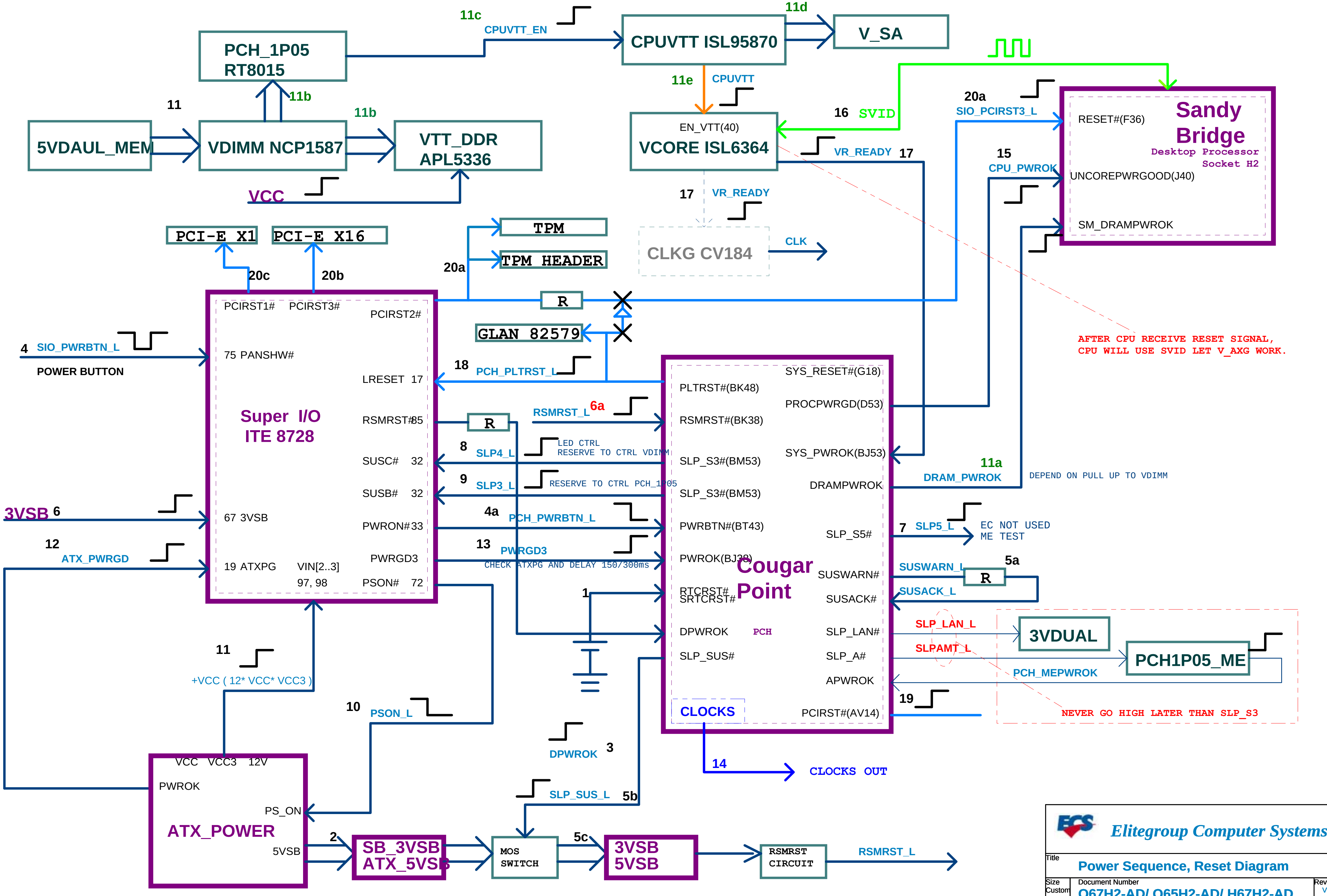

Elitegroup Computer Systems

Title	Power Sequence, Reset Diagram	
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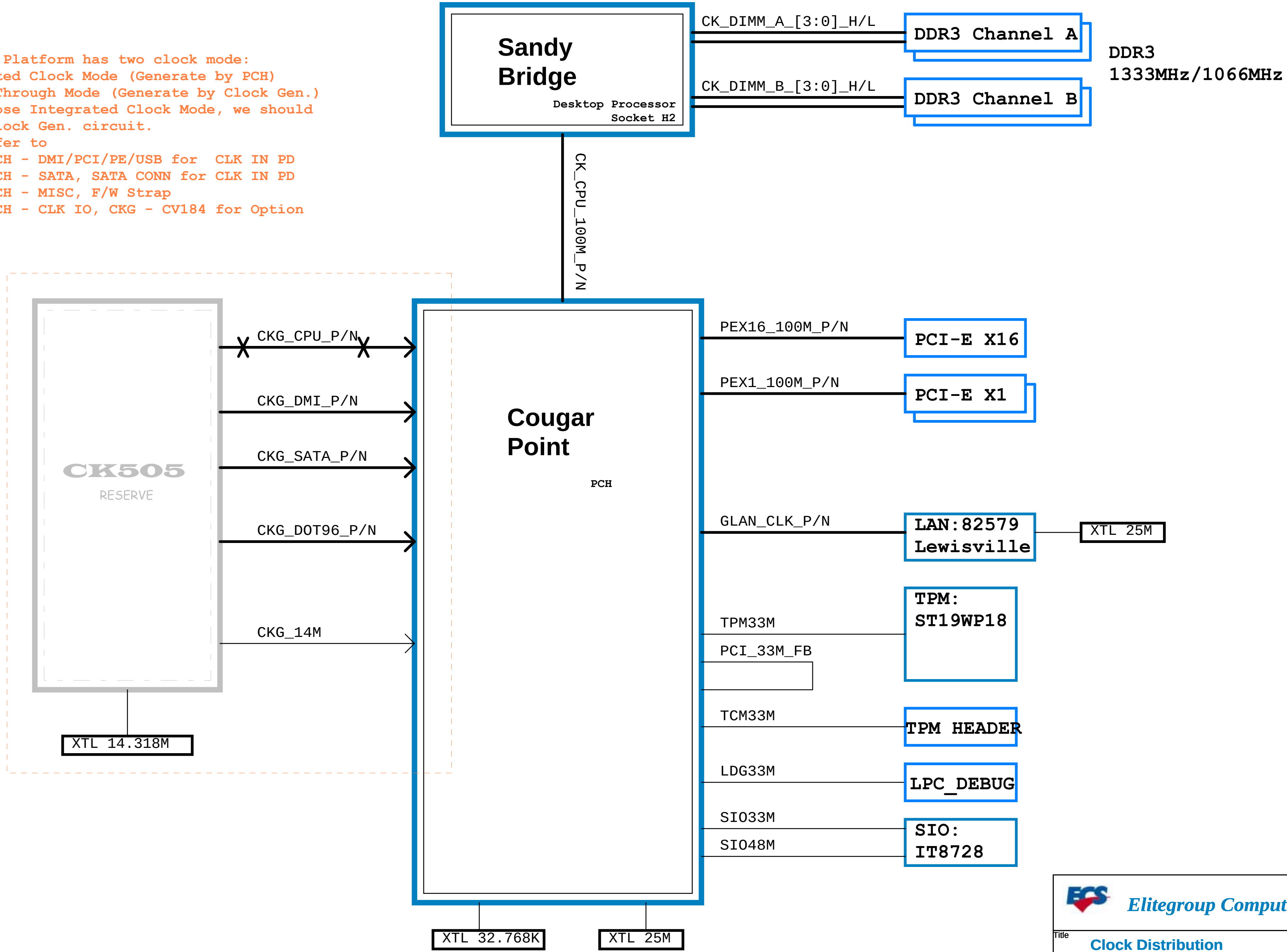
NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option



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Title	Clock Distribution	
Size: Custom	Document Number: Q67H2-AD/ Q65H2-AD/ H67H2-AD	Rev: V1.0
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