Olympus Block Diagram

Project code: 91.4Y601.001
PCB P/N : 48.4Y603.0SA
REVISION : 07258-3

CLK GEN.
ICS 9LPRS502
(RTM875T-605) 3
71.09502.00W

Mobile CPU
Penryn
4, 5

G7921
07

HOST BUS 667/800/1066MHz@1.05V

DDR2 socket 15
667/800MHz

DDR2 socket 16
667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
8,9,10,11,12,13,14

UMA

CRT 18
LCD 17
HDMI 25

PCIE*16
Extended VGA
ATI M82s
19,20,21,22,23,24

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 1.1
4 SATA
12 USB
High Definition Audio
LPC I/F
Serial Peripheral I/F
26,27,28,29,30

HP/SPDIF
INT.SPKR
MIC In
INT MIC ARRAY
Codec
ALC269
(include AMP) 34
Support Dolby HT
AZALIA

RJ11
MODEM
MDC Card 39

PCI BUS

Ricoh
R5C833
Cardreader
32,33

1394
CONN 33

MS/MS Pro/xD/
MMC/SD
5 in 1 33

LAN
Boardcom
10 /100M
BCM5906 35

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PCIe x1

Mini Card *2
Kedron a/b/g/n 40

LPC BUS

New card 41
PCI Express

SATA

SATA

Power switch 29

SATA-HDD 31

SATA-CDROM 31

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MINI USB
BlueTooth 39

KBC
Winbond
WPC776 38

SPI I/F

BIOS
2M byte 51

LPC
DEBUG
CONN. 31

Touch
Pad 51

INT.
KB 51

CIR 39

22

USB
2 Port 42

CAMERA 17

PCB 8-LAYER STACKUP

TOP	
GND	
S	
S	
PWR	
S	
GND	
BOTTOM	

SYSTEM DC/DC ISL6236 38

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC TPS51124 40

INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D5V_S3(10A)

TPS51117 39

DCBATOUT	1D8V_S3 (2.5A)

TPS51100 39

1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5308 39

3D3V_S0	2D5V_S0 (300mA)

CHARGER BQ24750 42

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6266A 37

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

NB DC/DC ISL6263A 41

INPUTS	OUTPUTS
DCBATOUT	GFX_CORE

SC411 48

DCBATOUT	1D5V_S3

BOM1

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: LT32M | Rev: -3

Date: Monday, July 07, 2008 | Sheet 1 of 55

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

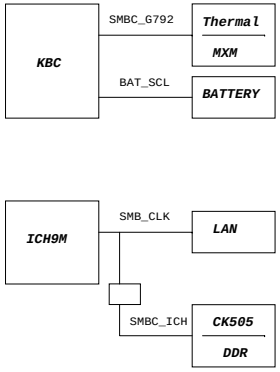
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=**The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

SMBus



PCI Routing

page 17

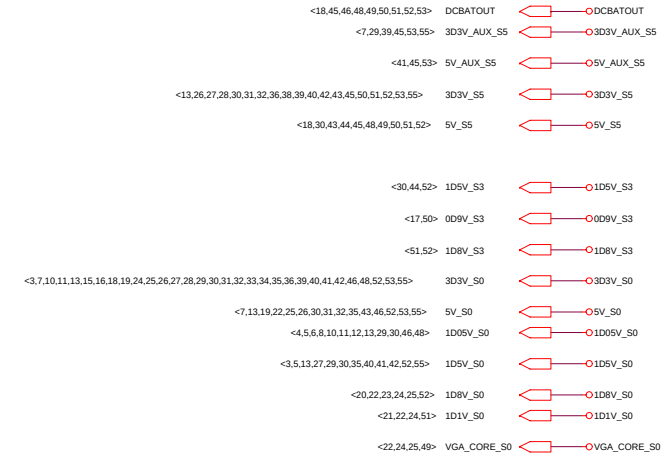
	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB Pair	USB Device
0	Combo(ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1



BOM1

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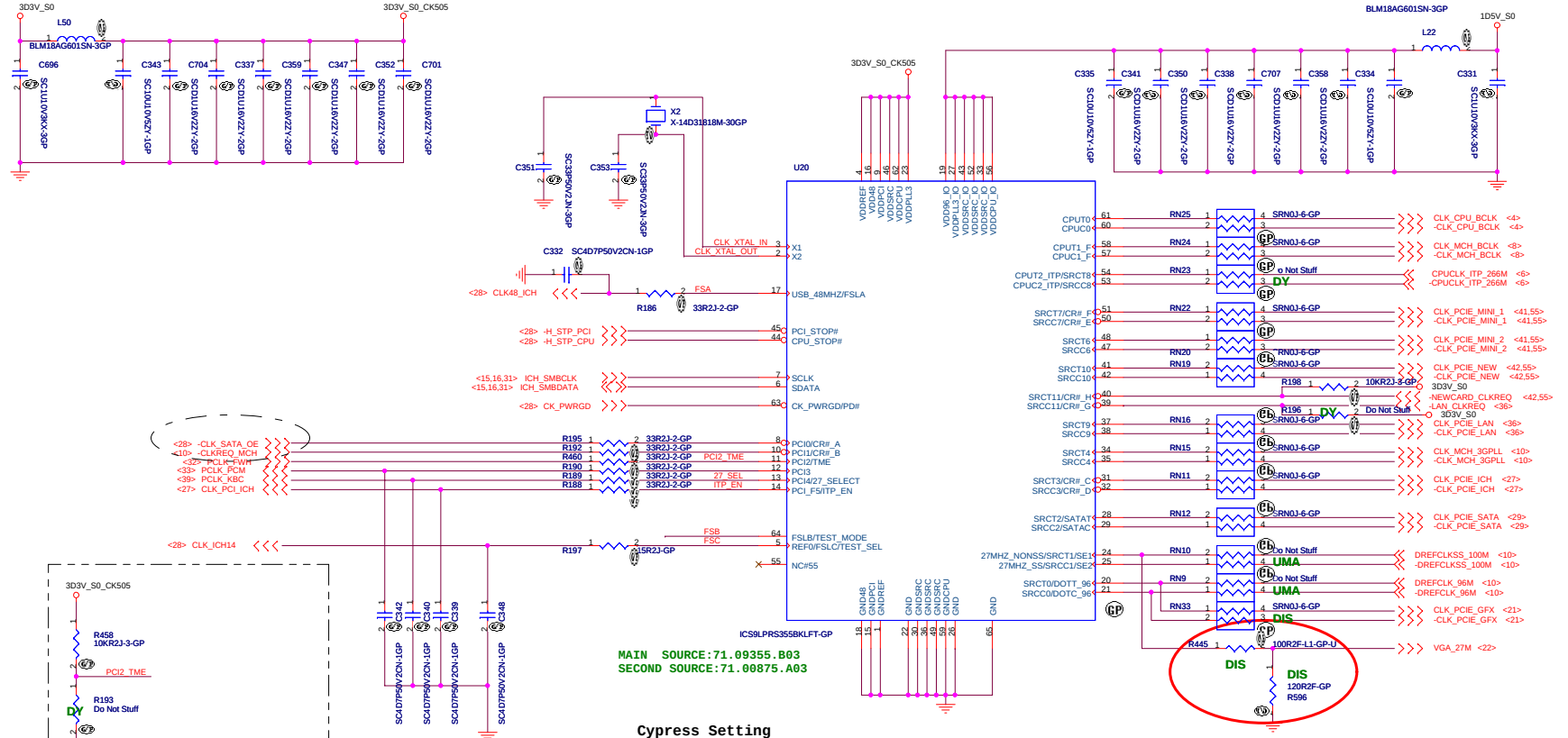
Title: Reference

Size: C | Document Number: LT32M | Rev: -3

Date: Monday, July 07, 2008 | Sheet 2 of 54



Design Note:

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

BOM1

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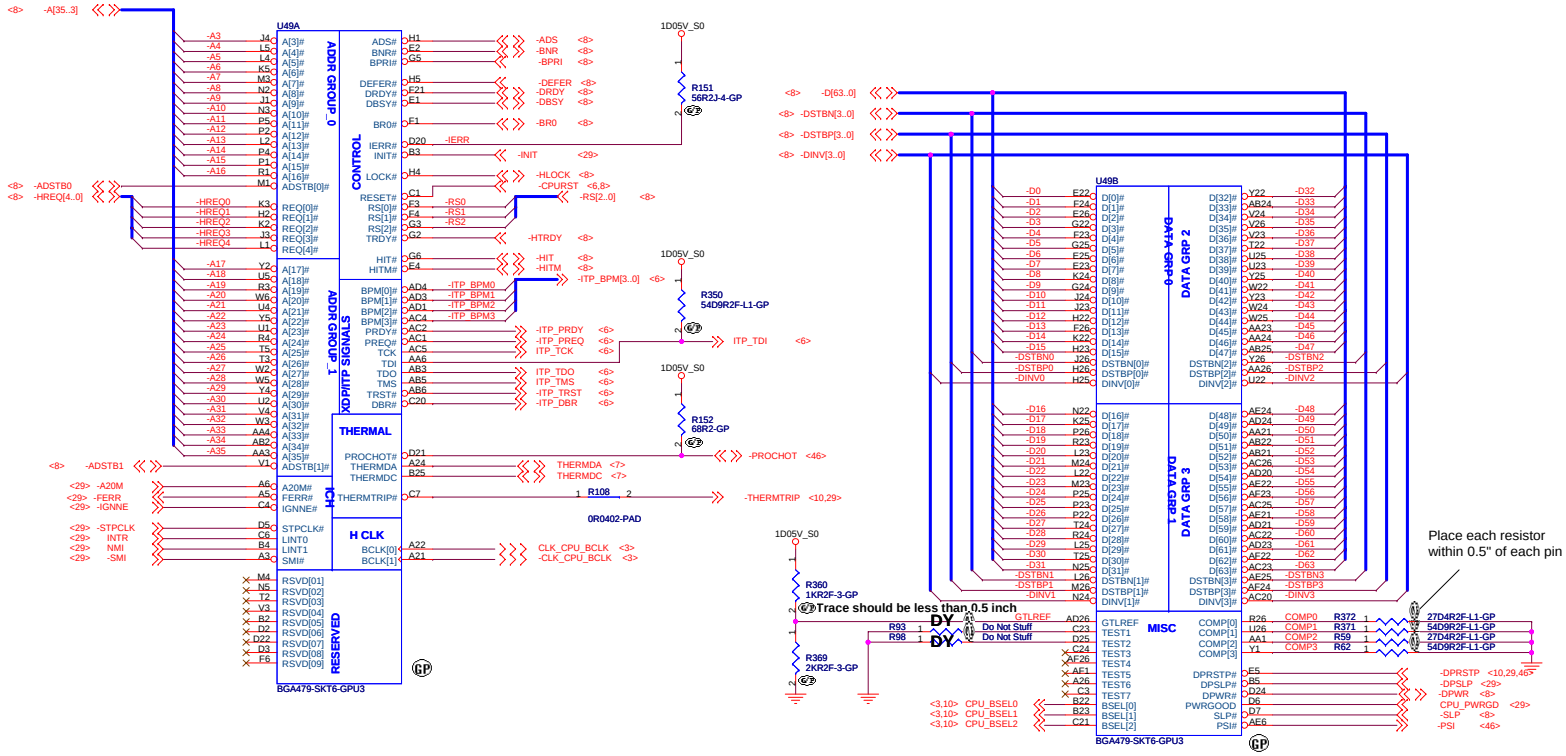
Title: Clock Generator

Size: Document Number: LT32M Rev: -3

Date: Monday, July 07, 2008 Sheet 3 of 54



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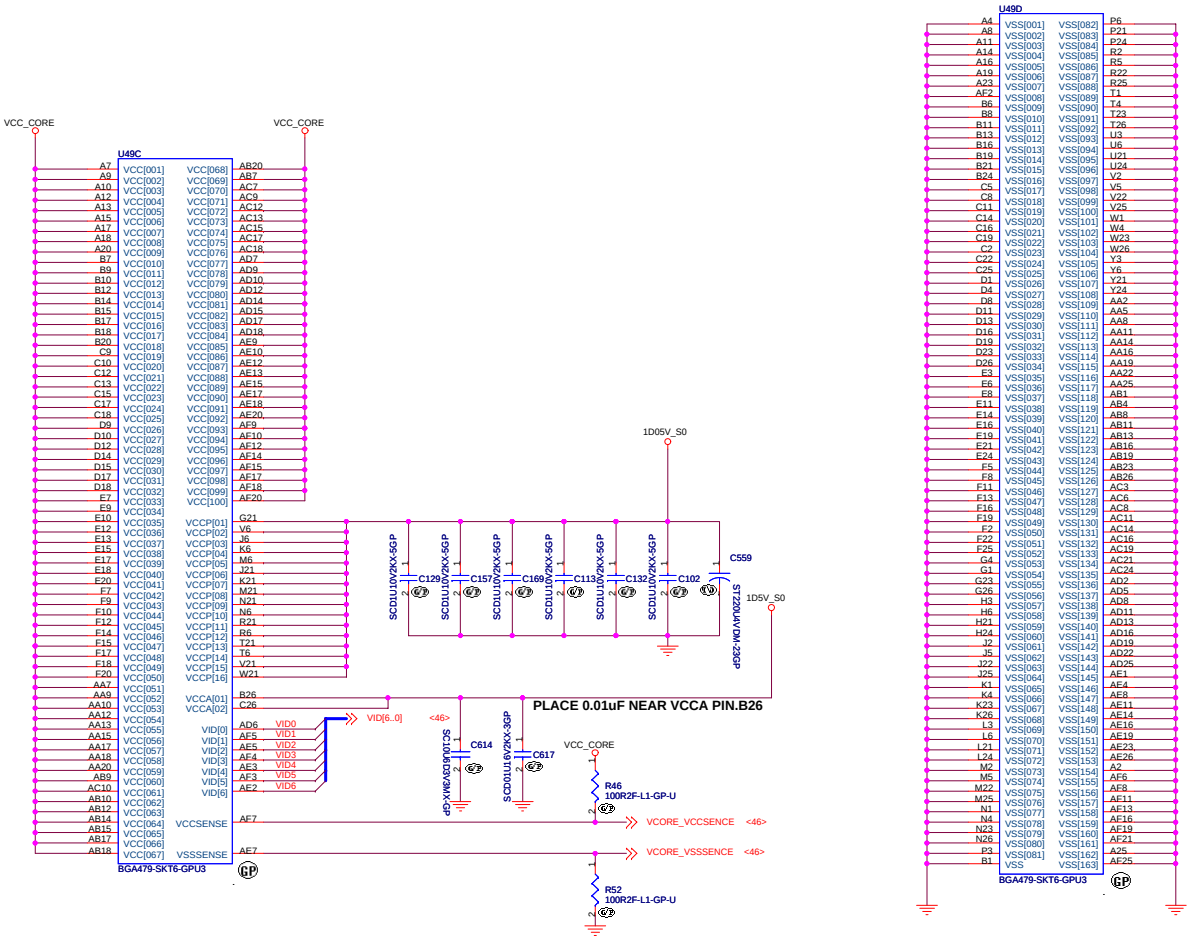
Title: **Penryn CPU(1/2)**

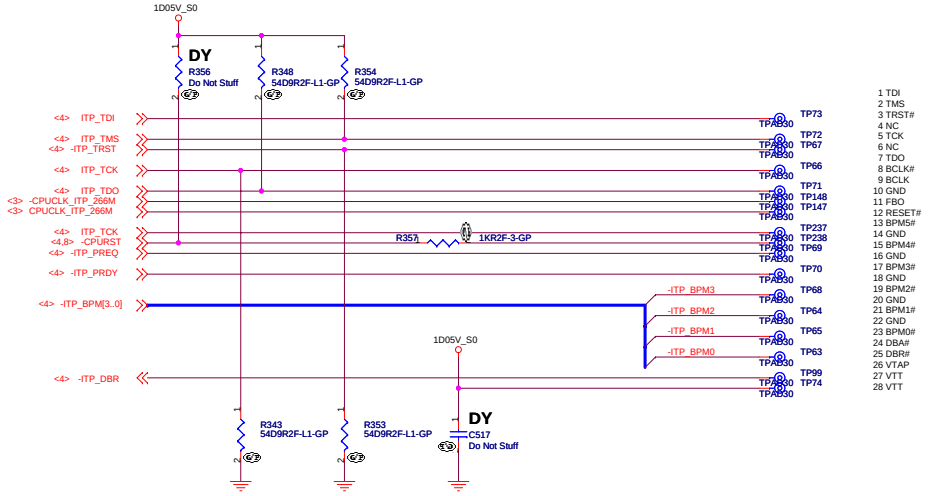
Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 4 of 54



BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Penryn CPU(2/2)***	
Size: C	Document Number: **LT32M**	Rev: -3
Date: Monday, July 07, 2008	Sheet 5 of 54	



(*1) TCK SIGNAL IS BRANCHED AT CPU's PIN

(*2) CPURST# SIGNAL IS BRANCHED AT GMCH's PIN

Ref Des	For ITP-XDP
J1	NO_ASM-->ASM
C157	NO_ASM-->ASM
R140	NO_ASM-->1K 5% ASM
R144	ASM (No Change)
R136	ASM-->NO_ASM
R145	ASM (No Change)
R141	ASM-->54.9 1% ASM
R143	ASM-->54.9 1% ASM

BOM1

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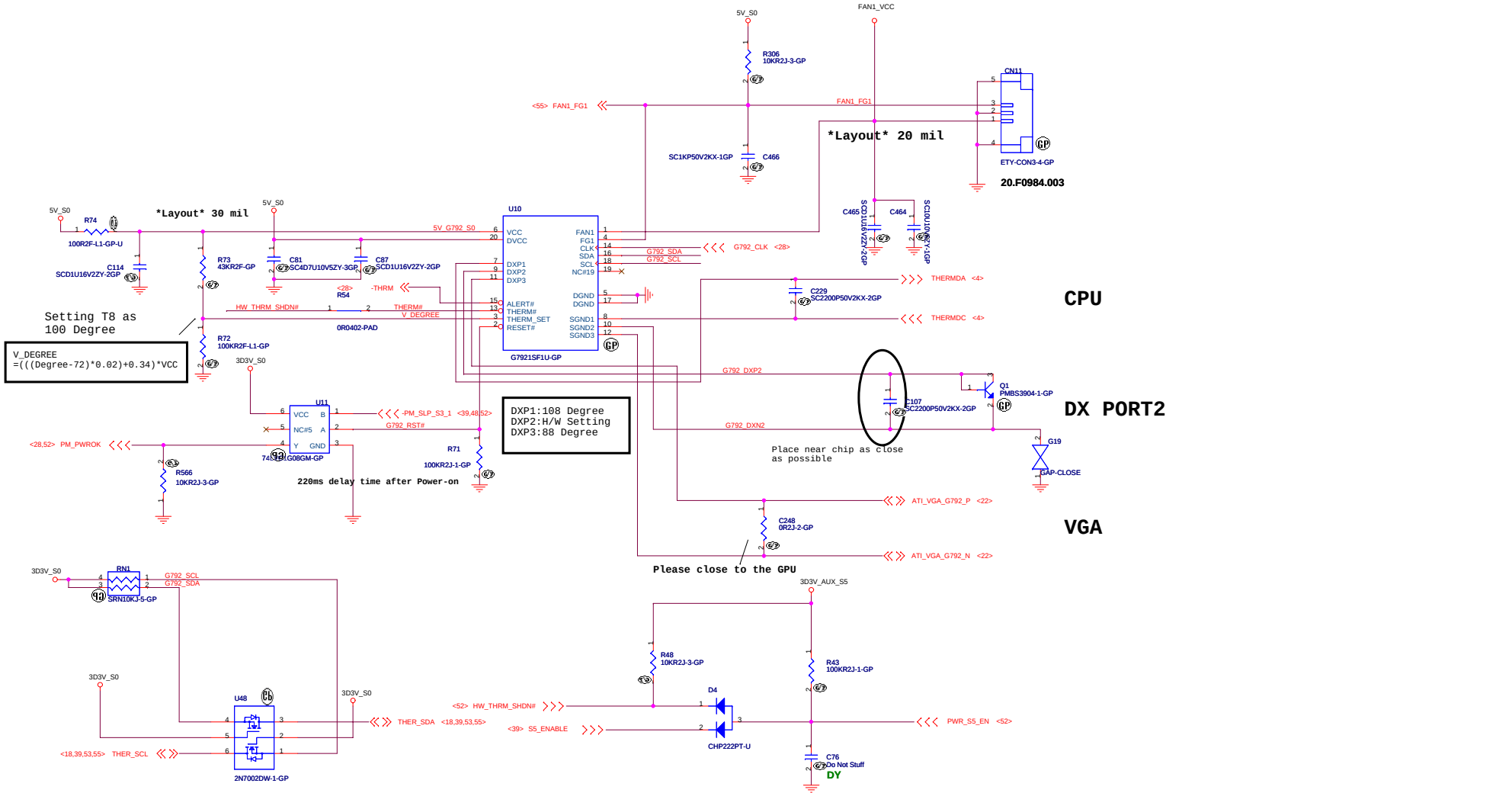
Title: ***ITP CONN***

Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 6 of 54



BOM1

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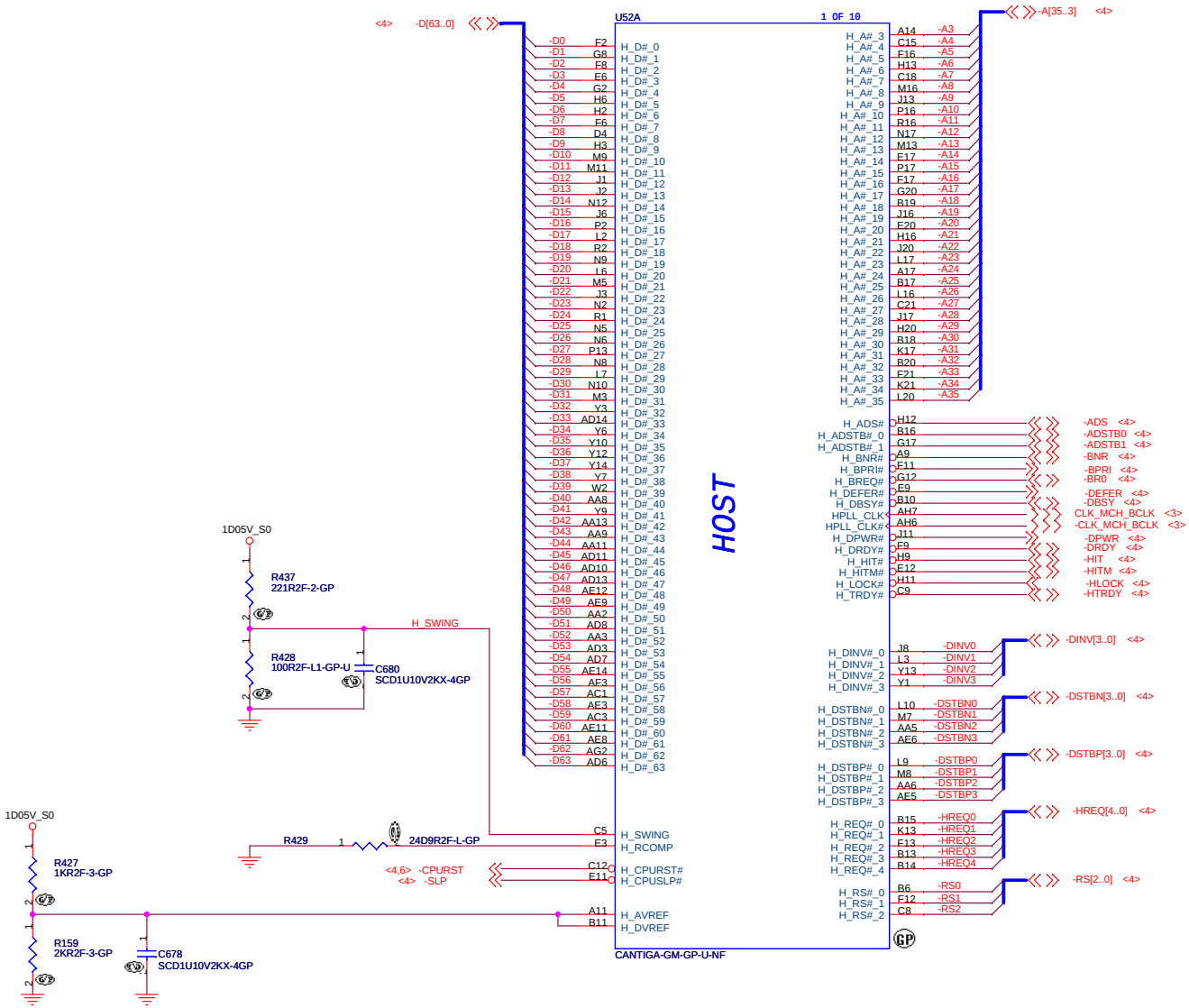
Title: ***Thermal/Fan Controllor G792***

Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 7 of 54



Route H_XSWING & H_YSWING
10 mil wide / 20 mil spacing

Route H_XRCOMP &
H_YRCOMP 10 mil wide /
20 mil spacing

BOM1

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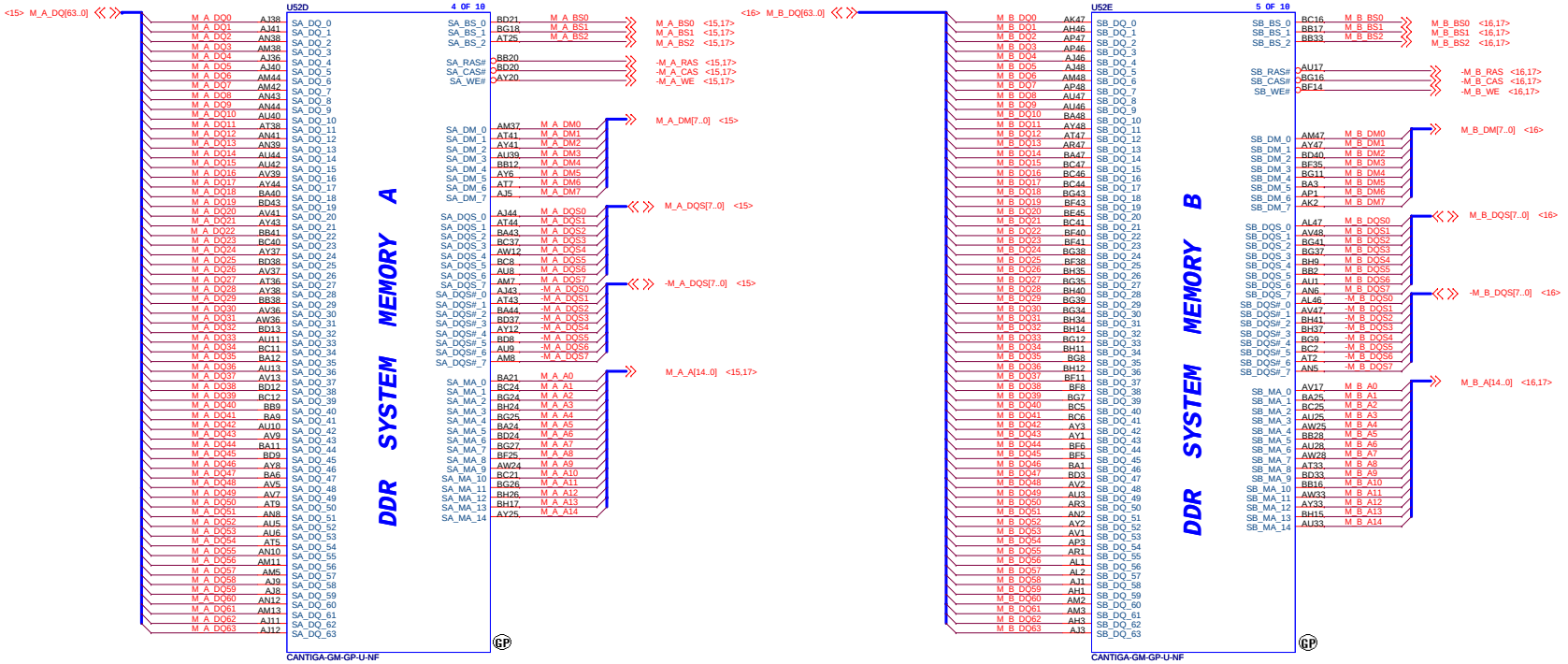
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cantiga(1/7):HOST I/F***

Size	Document Number	Rev
A3	LT32M	-3

Date: Monday, July 07, 2008 Sheet 8 of 54



BOM1

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Title: Cantiga(2/7):DDR3

Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 9 of 54

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
CFG6 : iTPM
CFG7 : ME Crypto
CFG9: PCIE STD& REV
CFG16 : FSB Dynamic ODT
CFG19 : DMI Lane reversal
CFG20 : DP concurrent
CFG[17:3]:internal pullup
CFG[20:18]:internal pulldown

FOR DDR2

FOR DDR2

FOR DDR2

FOR DDR2

0 DDR2

DIS

0201 SIZE

U52B — 2 OF 10 — CANTIGA-GM-GP-U-NF

RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA

BOM1

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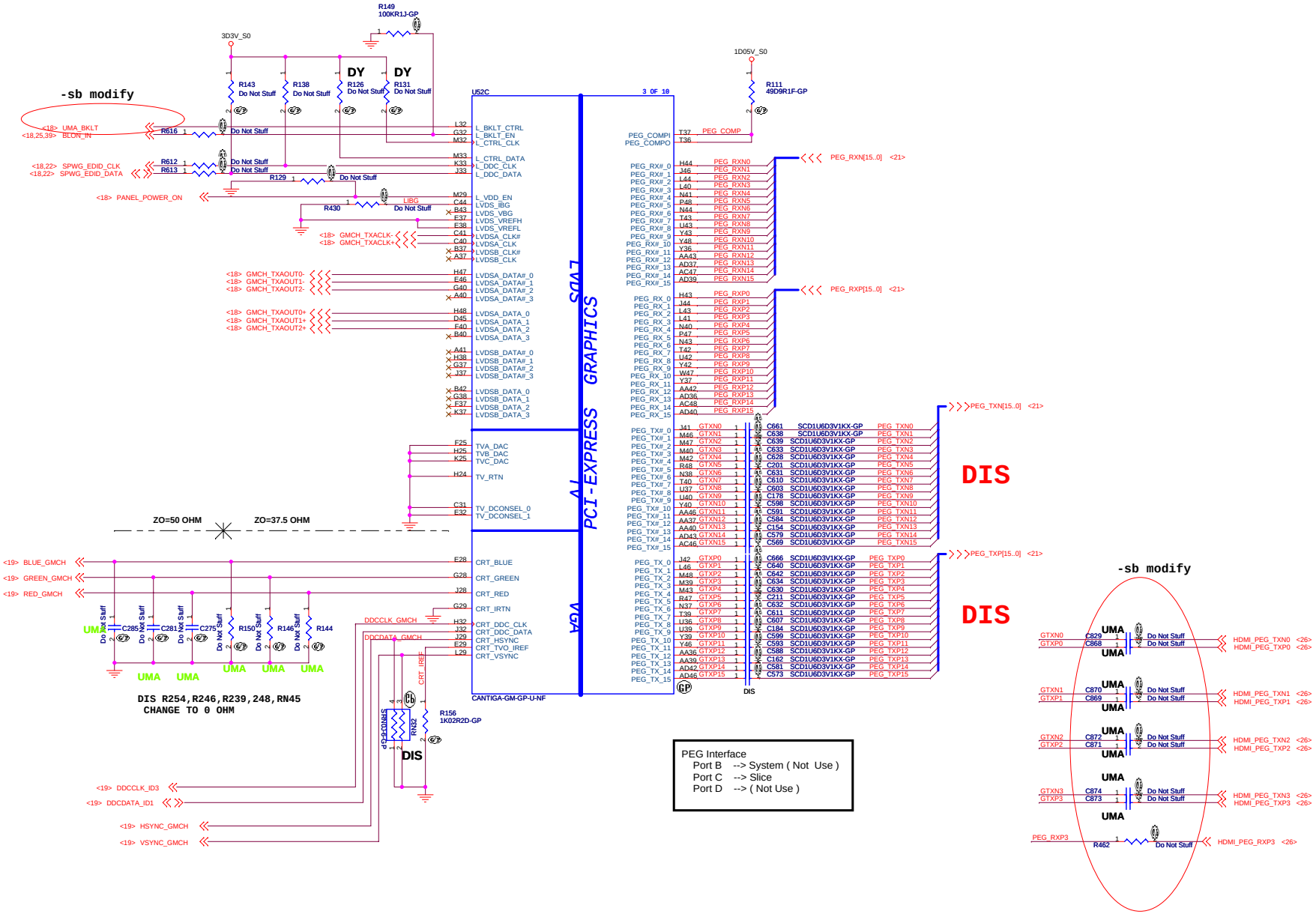
Title: Cantiga(3/7):DMI/PM/CFG/GF

Size: C | Document Number: LT32M | Rev: -3

Date: Monday, July 07, 2008 | Sheet 10 of 54



BOM1

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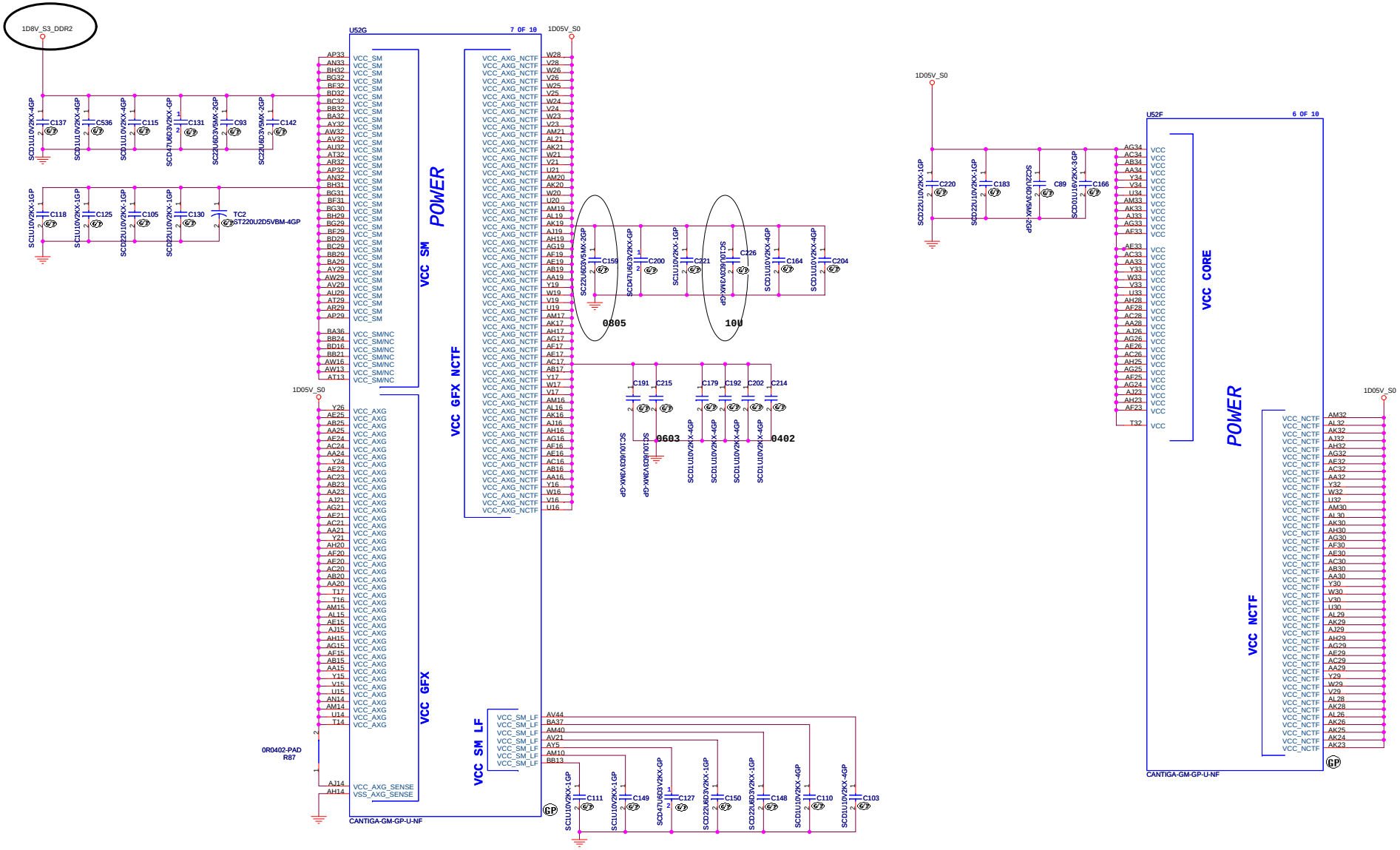
Title: CANTIGA(5/7)-VGA/LVDS		
Size: C	Document Number: LT32M	Rev: -3
Date: Monday, July 07, 2008	Sheet 11 of 54	

FOR DDR2



BOM1

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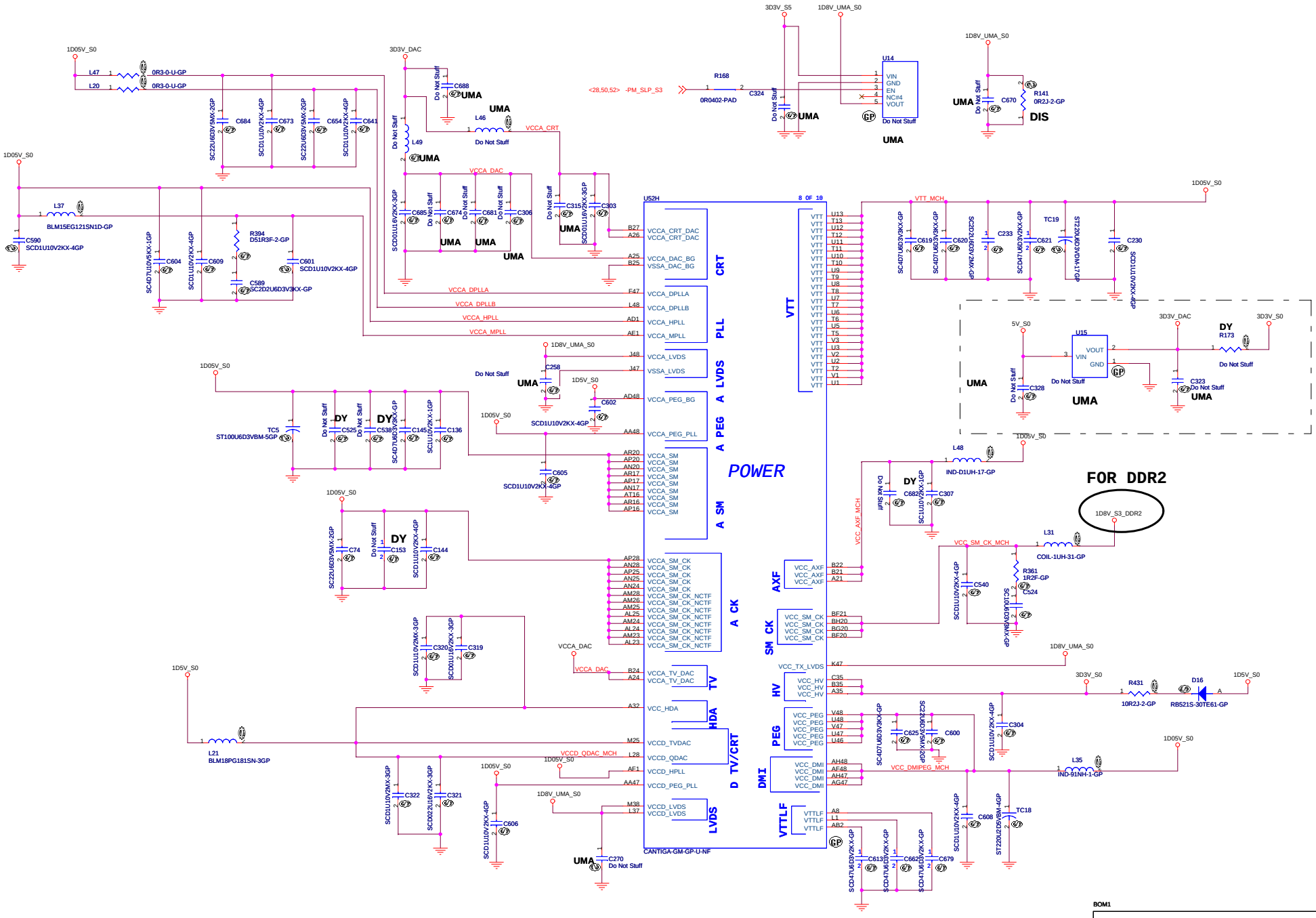
Title: Cantiga(5/7):VCC

Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 12 of 54


POWER
FOR DDR2
CANTIGA-GM-GP-U-NF
Wistron Corporation
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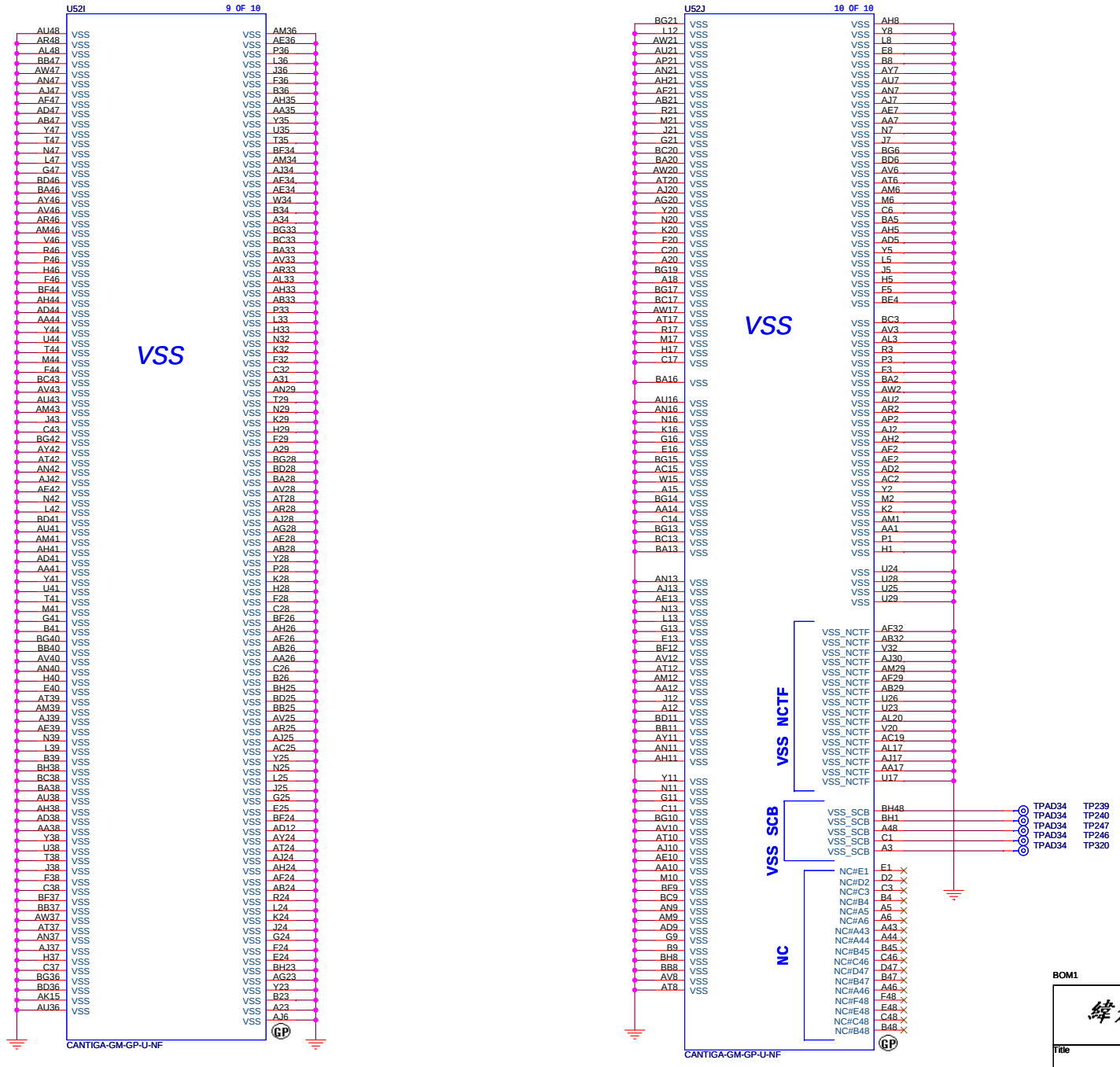
Taipei Hsien 221, Taiwan, R.O.C.
Cantiga(6/7):VCC
LT32M
Monday, July 07, 2008
Sheet 13 of 54



BOM1

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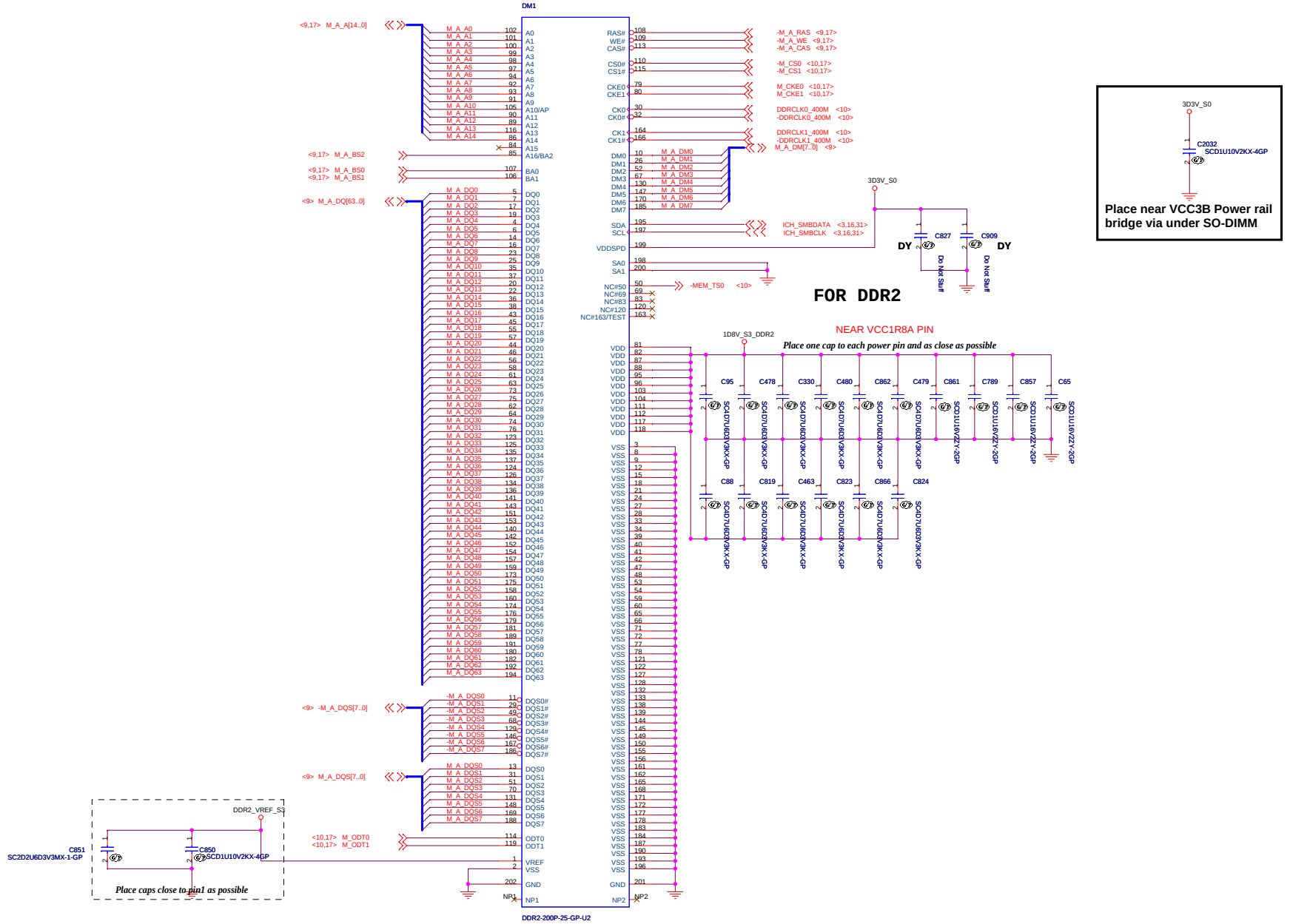
Title: **Cantiga(8/7):GND**

Size	Document Number	Rev
A3	LT32M	-3

Date: Monday, July 07, 2008 Sheet 14 of 54



BOM1

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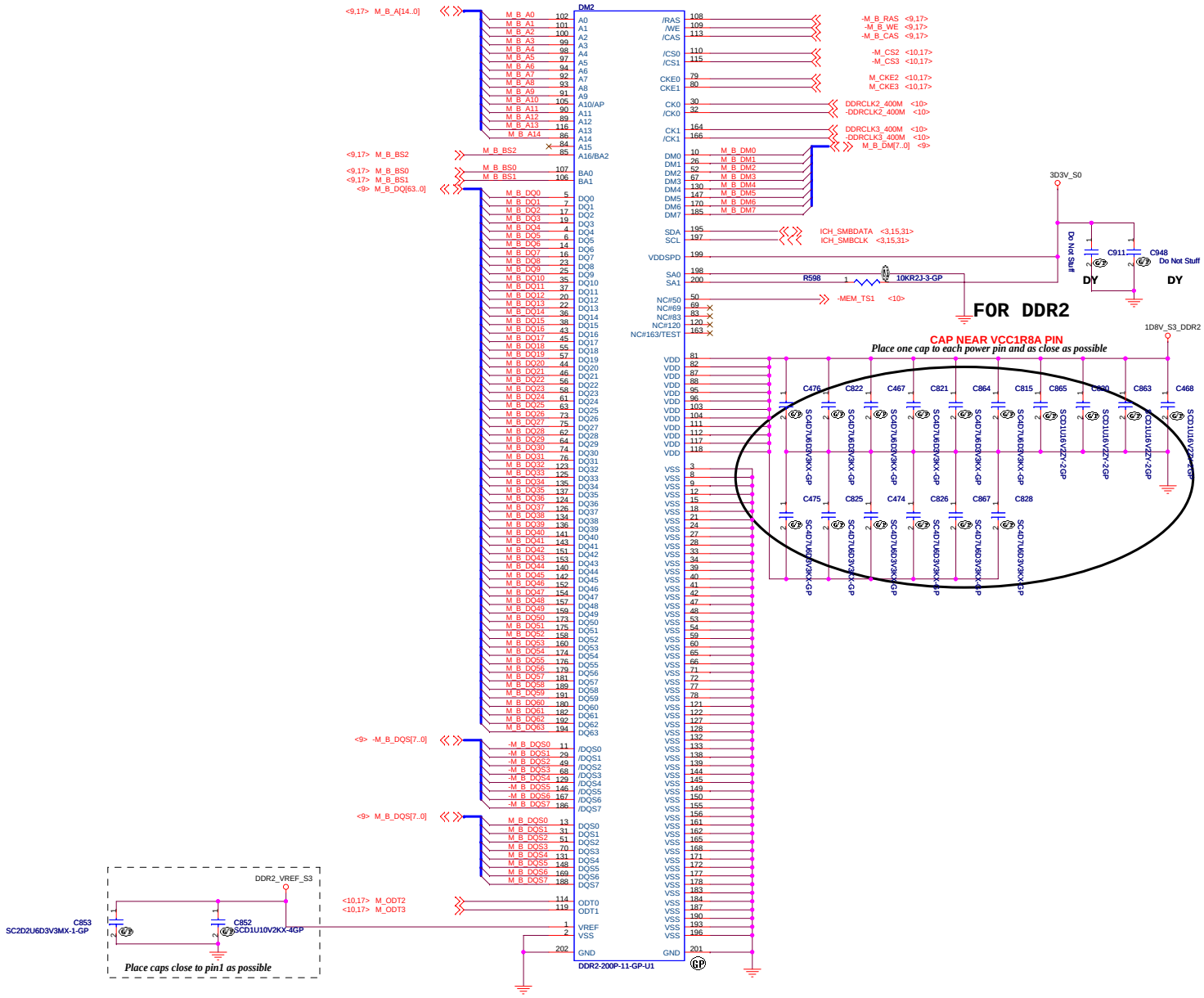
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2 SODIMM-A

Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 15 of 54



BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

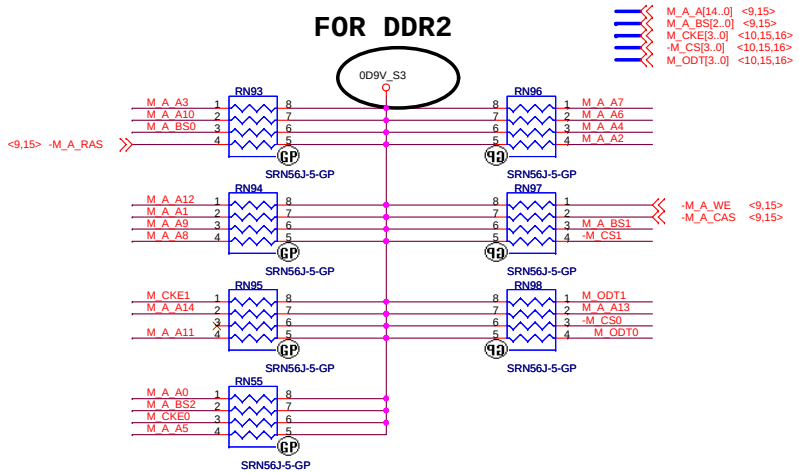
Title: DDR2 SODIMM-B

Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 16 of 54

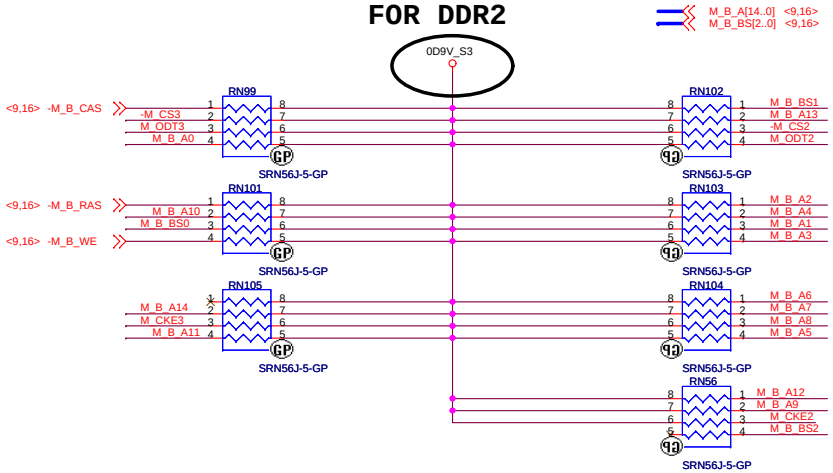
CHANNEL A PARALLEL TERMINATION

FOR DDR2

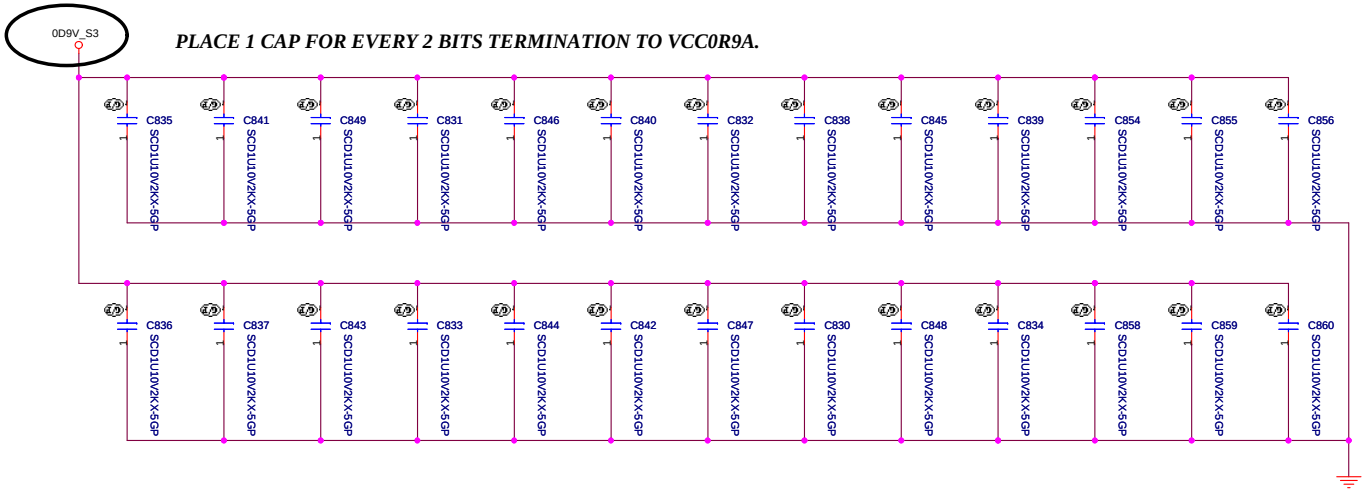


CHANNEL B PARALLEL TERMINATION

FOR DDR2



FOR DDR2



BOM1

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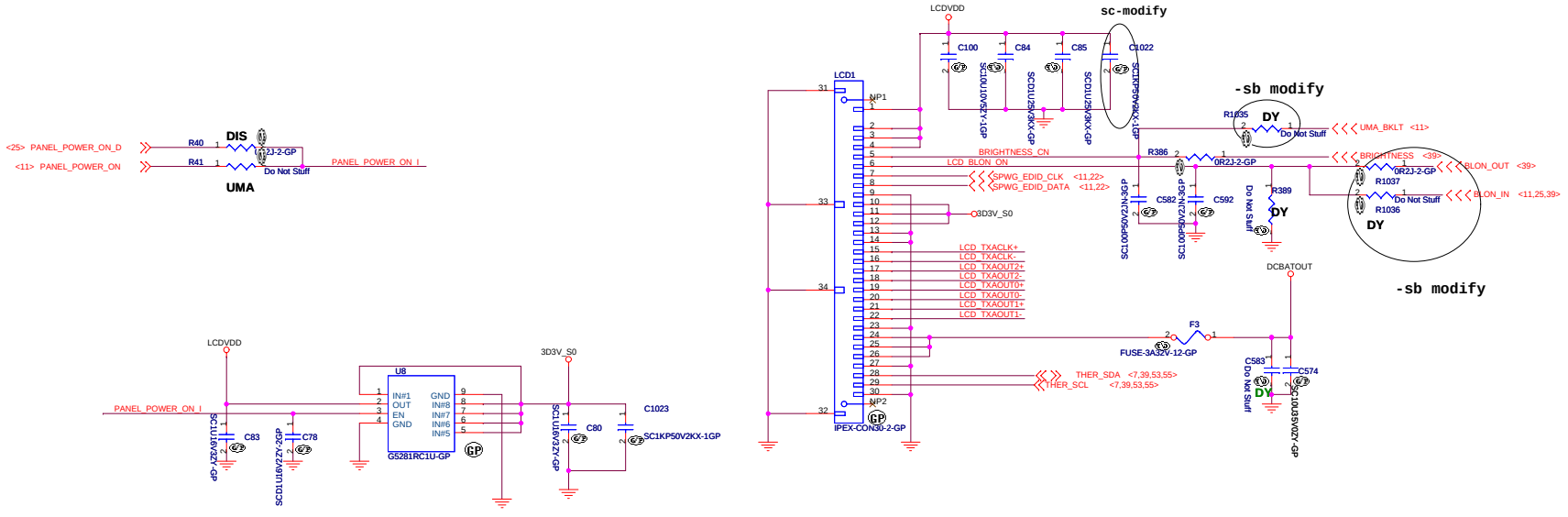
Taipei Hsien 221, Taiwan, R.O.C.

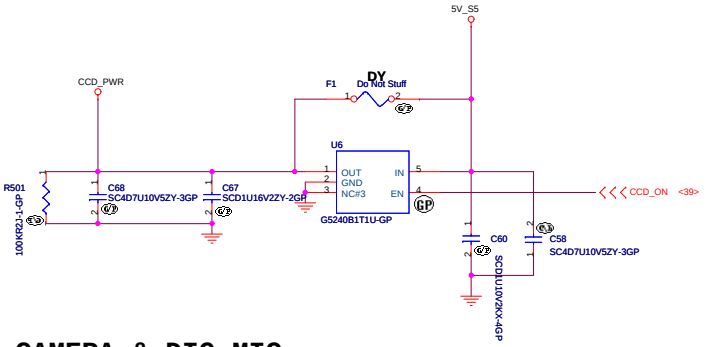
Title: **DDR-2 TERMINATION/DECOUPLING**

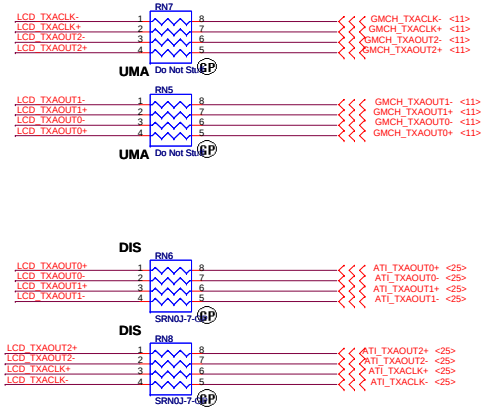
Size	Document Number	Rev
Custom	LT32M	-3

Date: Monday, July 07, 2008 Sheet 17 of 54

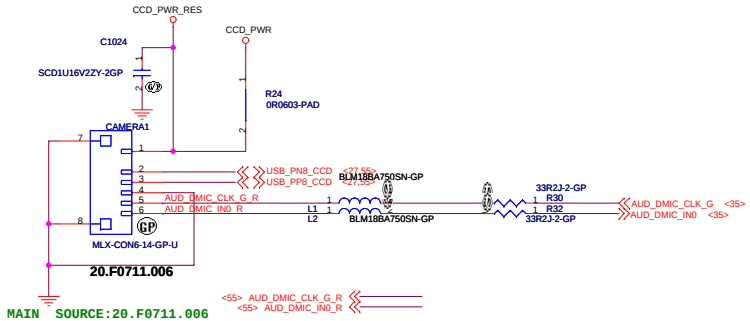
LCD/INVERTER CONN







CAMERA & DIG-MIC

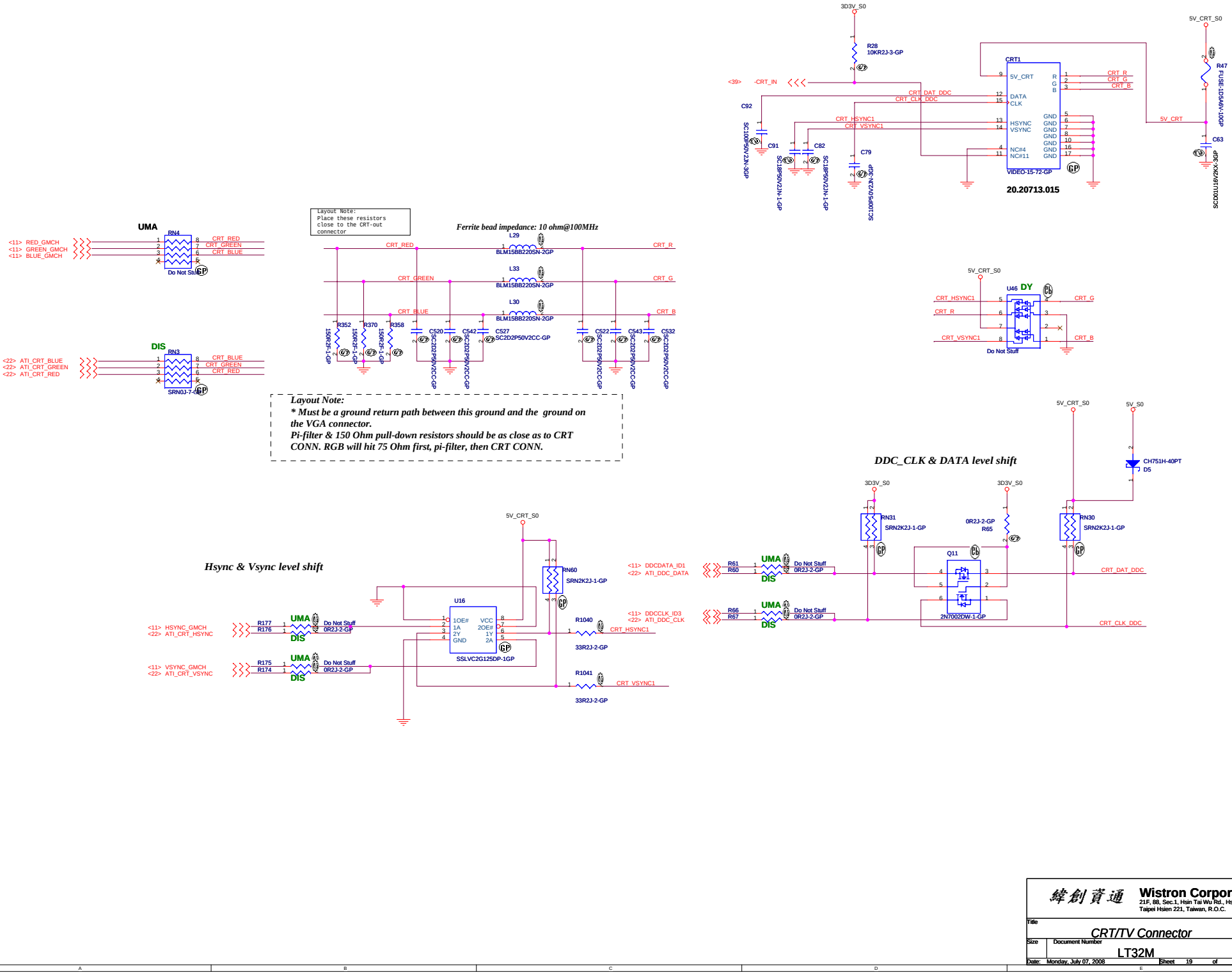


MAIN SOURCE:20.F0711.006
SECOND SOURCE:20.F0693.006

BOM1

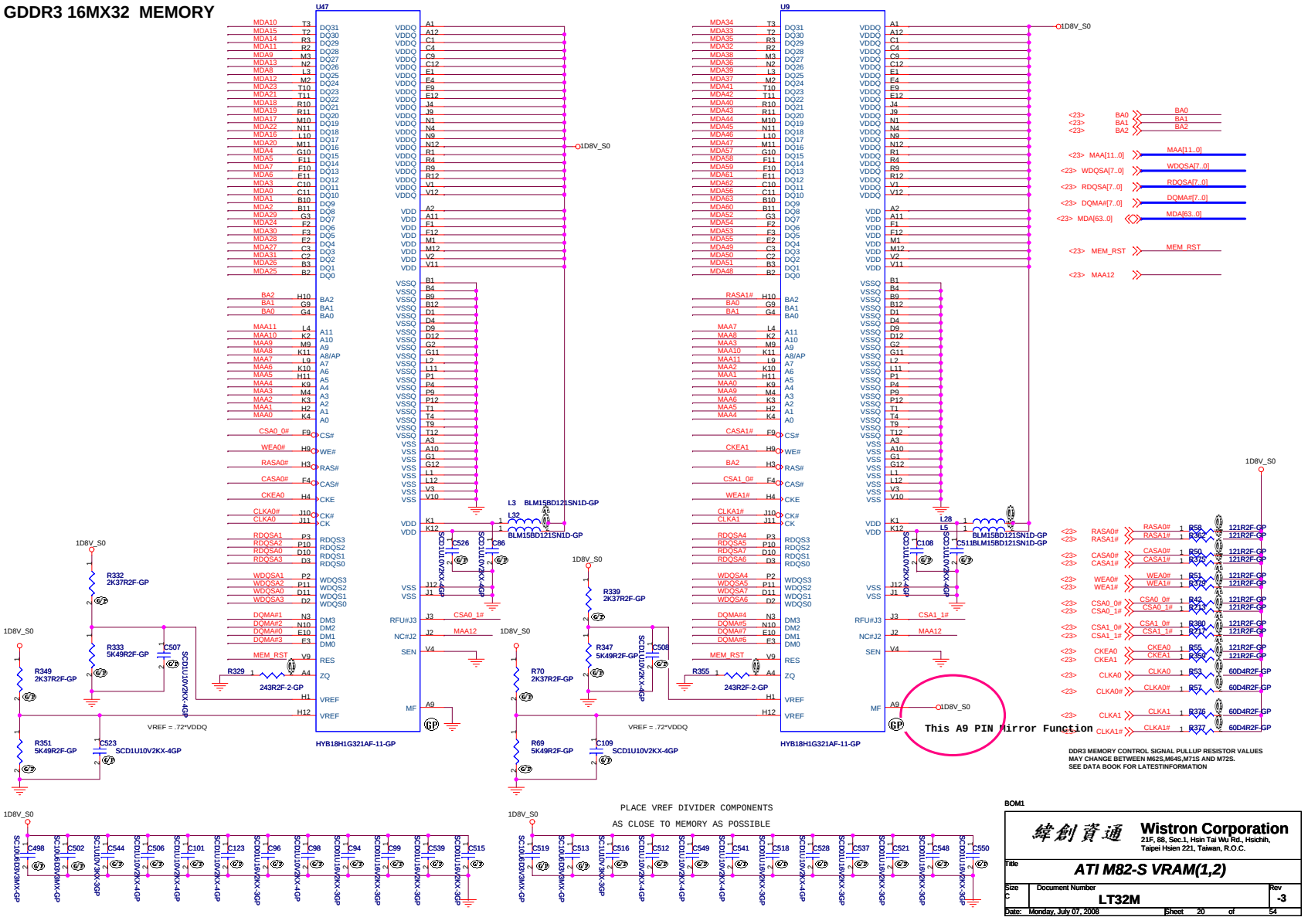
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LCD CONN & CAMERA & DIG-MIC		
Size	Document Number: LT32M	Rev: -3
Date: Monday, July 07, 2008	Sheet 18 of 54	

CRT I/F & CONNECTOR



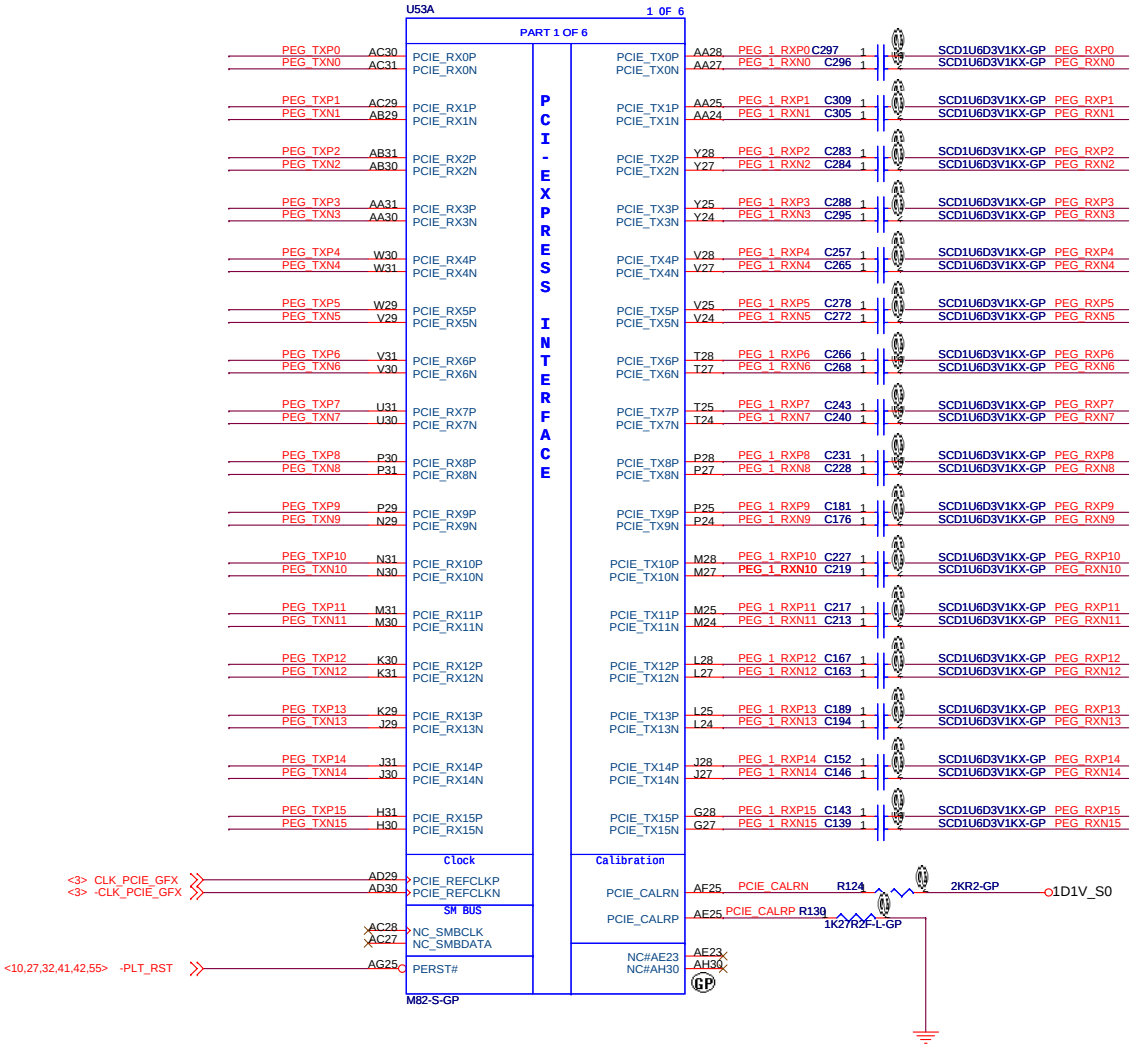
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT/TV Connector	
Size	Document Number: LT32M	Rev: -3
Date: Monday, July 07, 2008	Sheet 19 of 54	

GDDR3 16MX32 MEMORY



BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ATI M82-S VRAM(1,2)	
Size: C	Document Number: LT32M	Rev: -3
Date: Monday, July 07, 2008	Sheet 20 of 54	



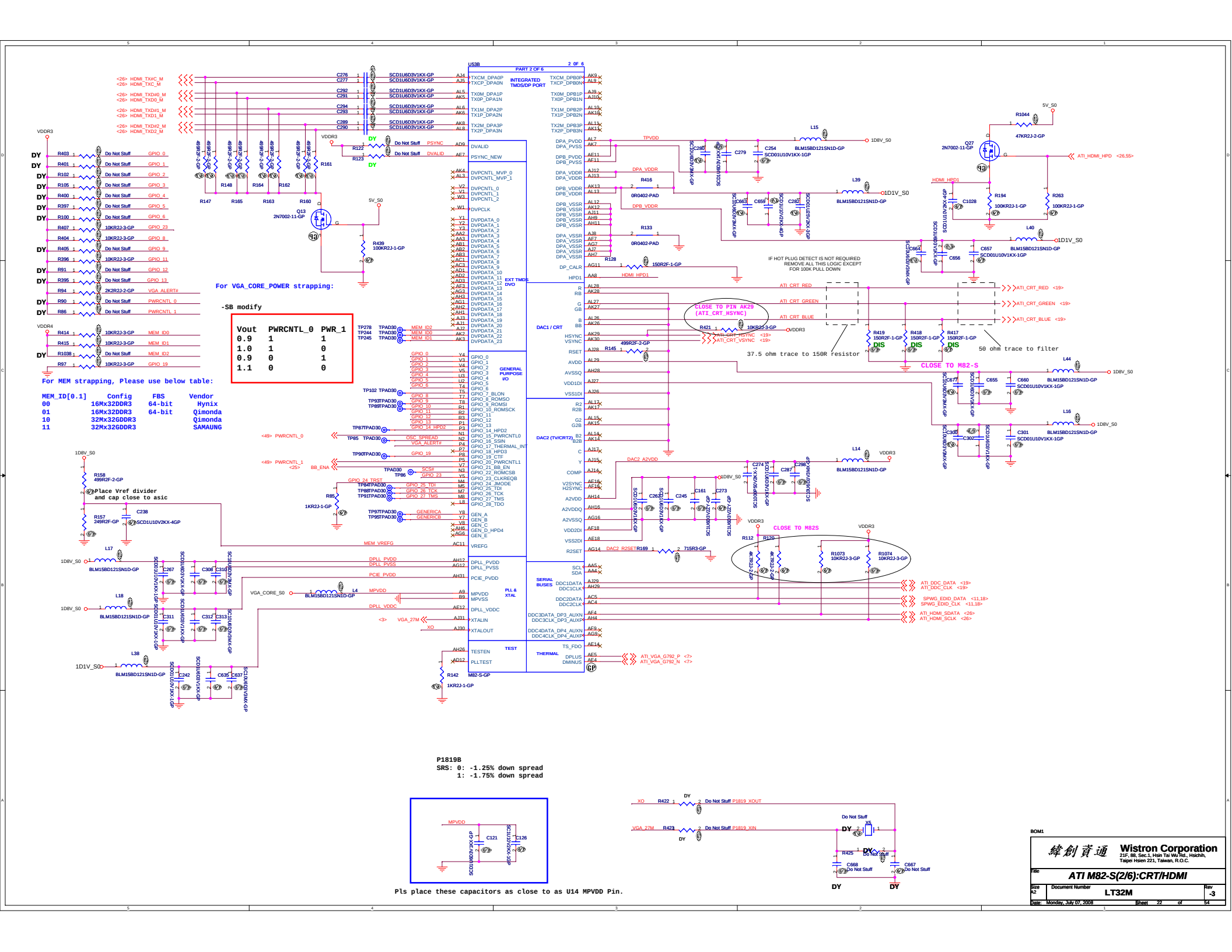
BOM1

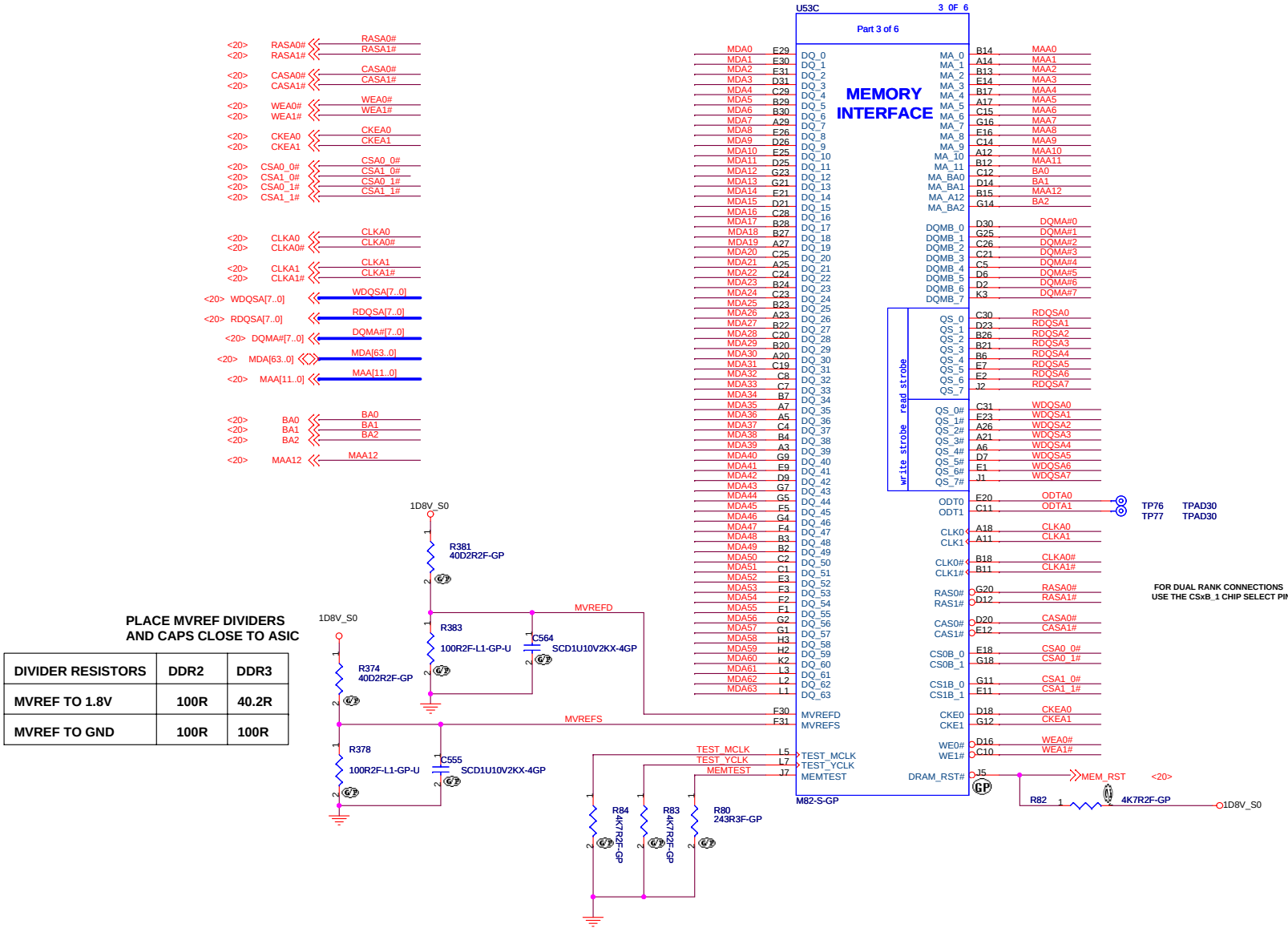
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M82-S(1/6):PCIE Interface**

Size	Document Number	Rev
A3	LT32M	-3

Date: Monday, July 07, 2008 Sheet 21 of 54


U53B
PART 2 OF 6
INTEGRATED TMDS/DP PORT
EXT TMDS DVO
GENERAL PURPOSE I/O
PLL & XTAL
TEST
SERIAL BUSES
THERMAL
DAC1 / CRT
DAC2 (TV/CRT2)
For VGA_CORE_POWER strapping:
-SB modify
Vout PWRCNTL_0 PWR_1
0.9 1 1
1.0 1 0
0.9 0 1
1.1 0 0
For MEM strapping, Please use below table:
MEM_ID[0.1] Config FBS Vendor
00 16Mx32DDR3 64-bit Hynix
01 16Mx32DDR3 64-bit Qimonda
10 32Mx32GDDR3 Qimonda
11 32Mx32GDDR3 SAMAUNG
Place Vref divider and cap close to asic
CLOSE TO PIN AK29 (ATI_CRT_HSYNC)
37.5 ohm trace to 150R resistor
50 ohm trace to filter
CLOSE TO M82-S
CLOSE TO M82S
IF HOT PLUG DETECT IS NOT REQUIRED REMOVE ALL THIS LOGIC EXCEPT FOR 100K PULL DOWN
P1819B
SRS: 0: -1.25% down spread
1: -1.75% down spread
Pls place these capacitors as close to as U14 MPVDD Pin.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI M82-S(2/6):CRT/HDMI
LT32M
Monday, July 07, 2008
Sheet 22 of 54



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

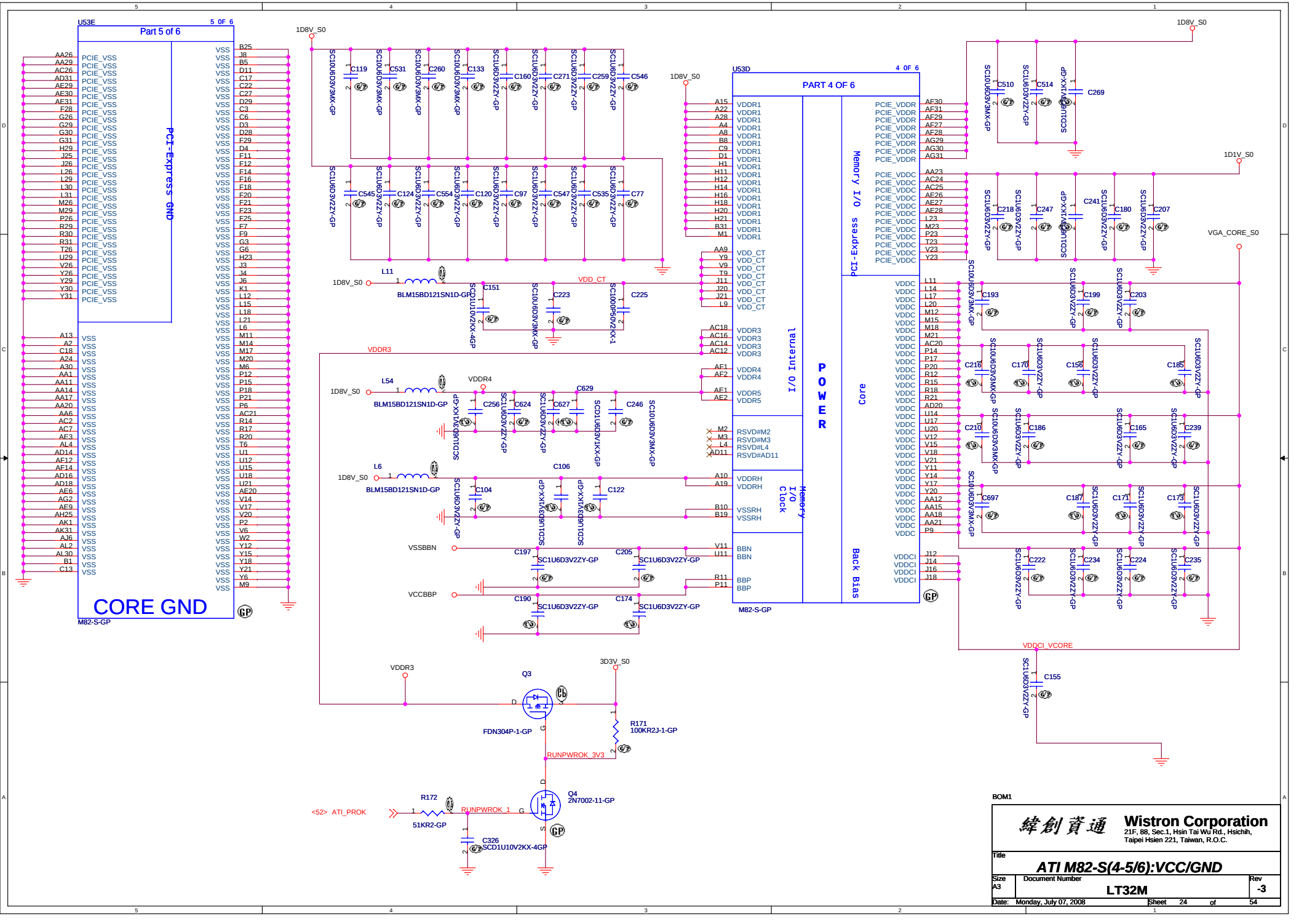
BOM1

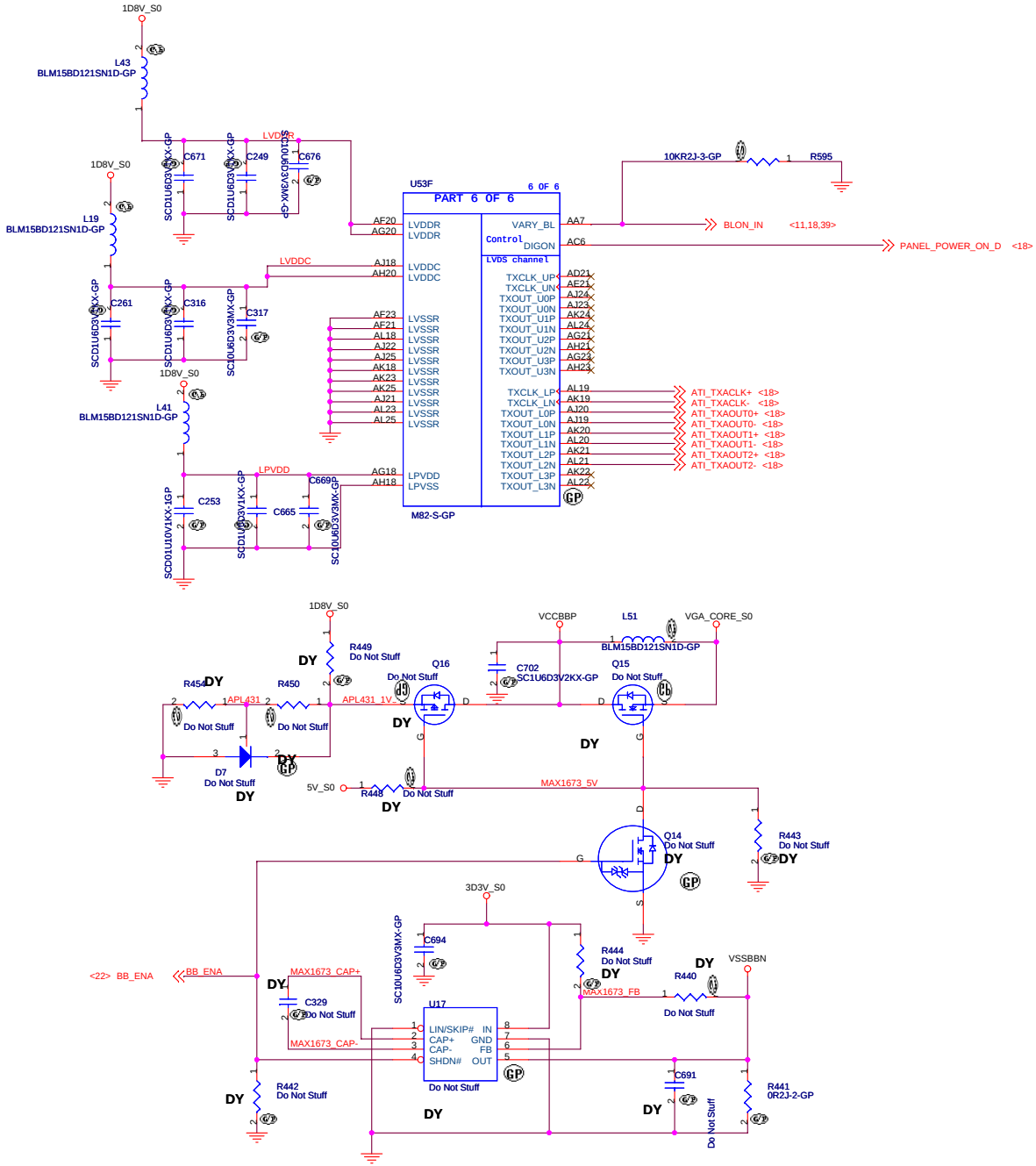
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M82-S(3/6):Memory Interface

Size	Document Number	Rev
A3	LT32M	-3

Date: Monday, July 07, 2008 Sheet 23 of 54


U53E
5 OF 6
Part 5 of 6
PCI-Express GND
CORE GND
M82-S-GP
U53D
4 OF 6
PART 4 OF 6
Memory I/O Express-ID
I/O Internal
POWER
Core
Back Bias
Memory I/O Clock
M82-S-GP
1D8V_S0
1D1V_S0
VGA_CORE_S0
VDDR3
VDDR4
VDD_CT
VDDCI_VCORE
3D3V_S0
VSSBBN
VCCBBP
RUNPWROK_3V3
RUNPWROK_1
Q3
FDN304P-1-GP
Q4
2N7002-11-GP
R171
100KR2J-1-GP
R172
51KR2-GP
L11
L54
L6
BLM15BD121SN1D-GP
C326
SCD1U10V2KX-4GP
<52> ATI_PROK
BOM1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M82-S(4-5/6):VCC/GND
Size
A3
Document Number
LT32M
Rev
-3
Date: Monday, July 07, 2008
Sheet 24 of 54



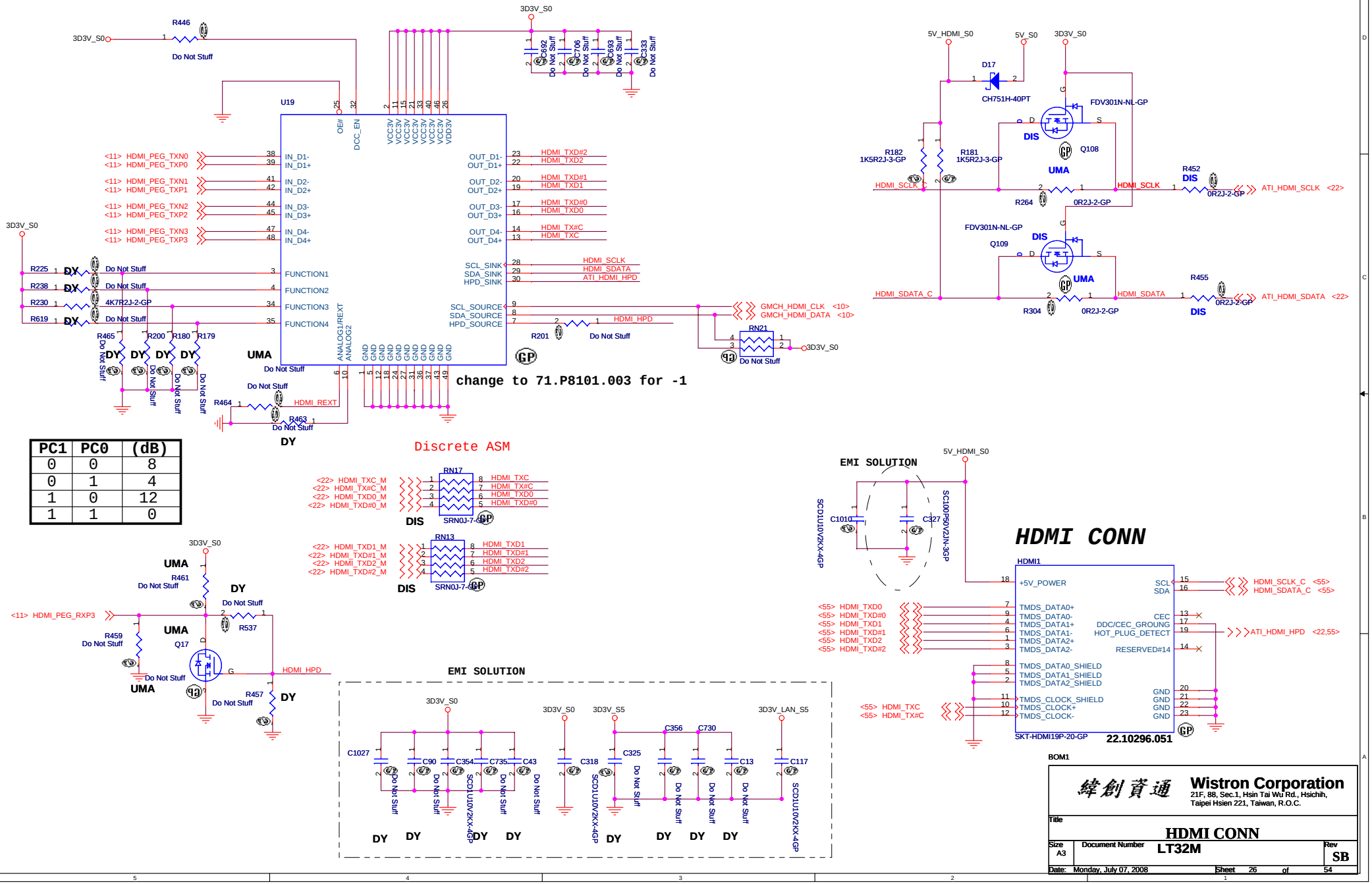
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

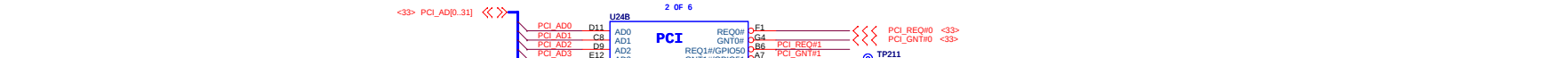
Title: ATI M82-S(6/6):LVDS

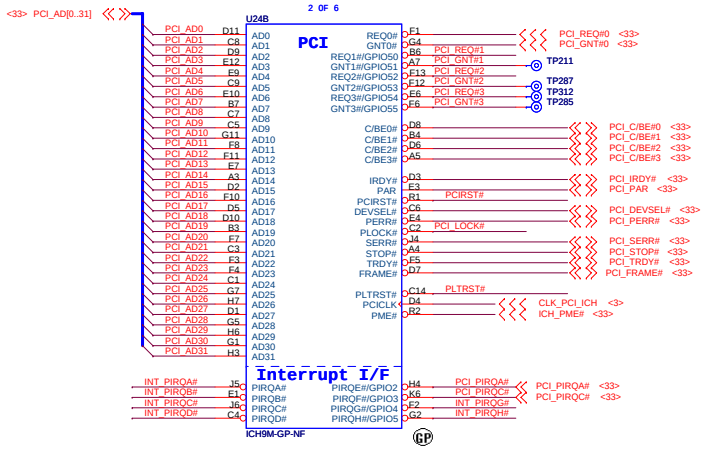
Size	Document Number	Rev
Custom	LT32M	-3

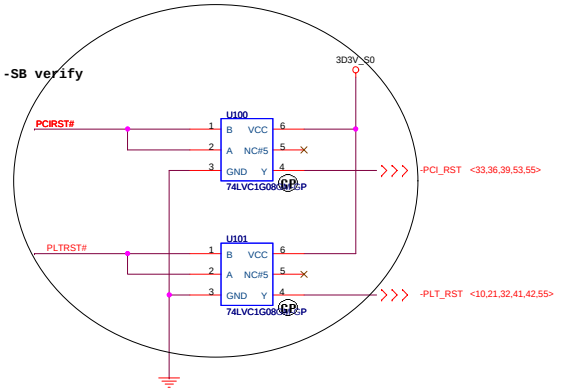
Date: Monday, July 07, 2008 Sheet 25 of 54

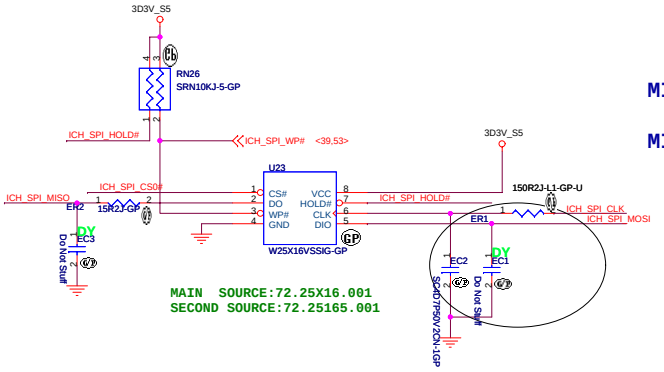


PC1	PC0	(dB)
0	0	8
0	1	4
1	0	12
1	1	0

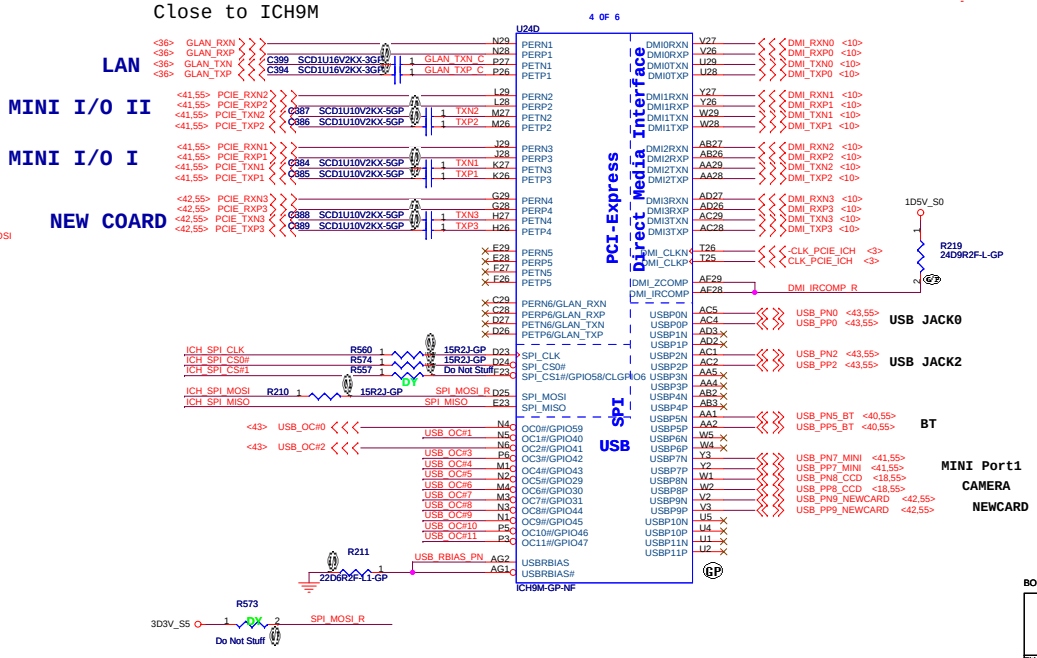


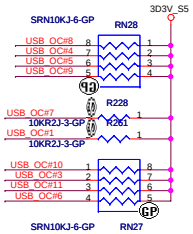




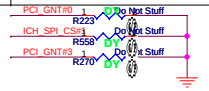


Close to ICH9M





BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	



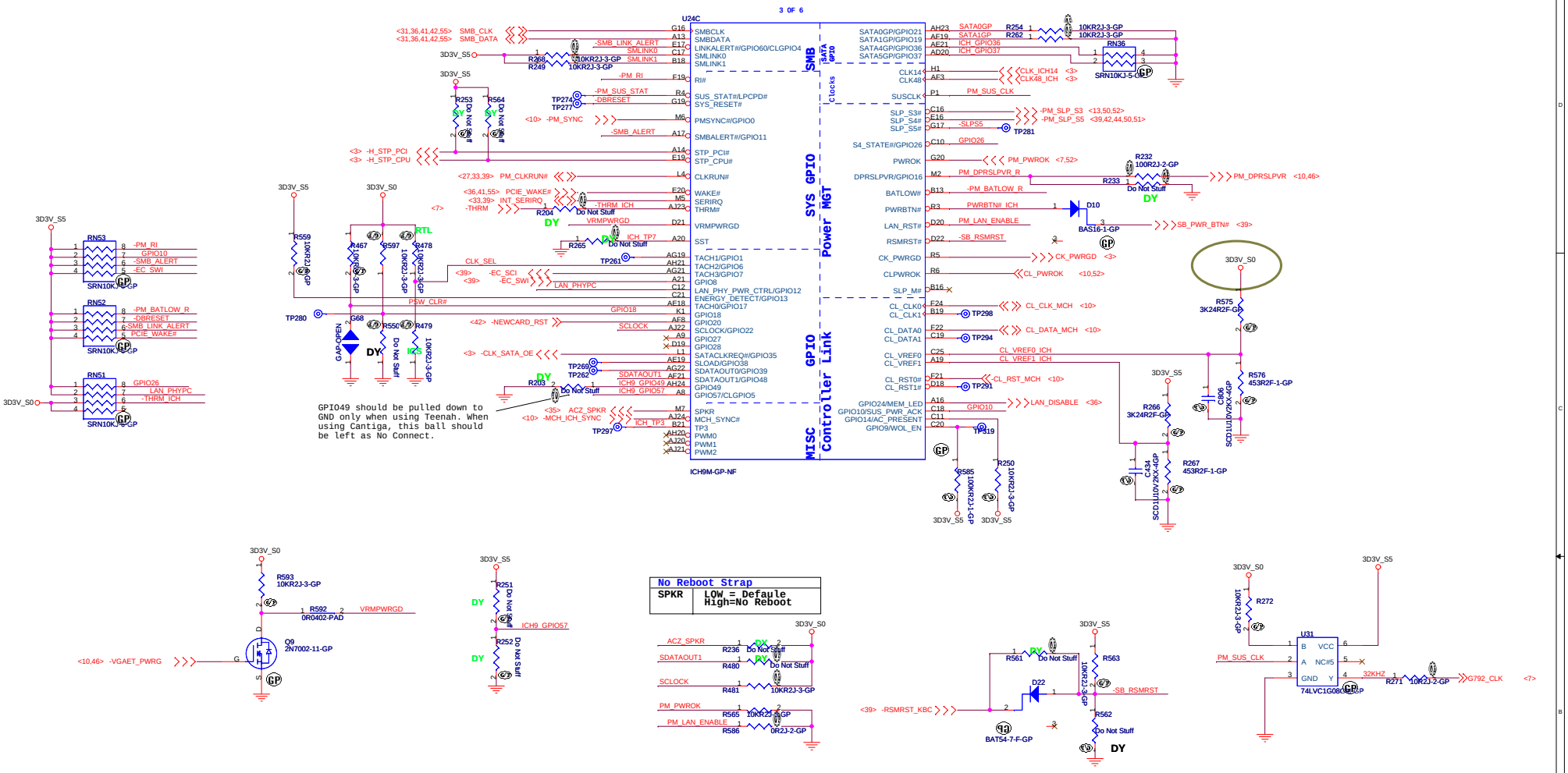
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 4)

Size	Document Number	Rev
	LT32M	-3

Date: Monday, July 07, 2008 Sheet 27 of 54


3 OF 6
U24C
ICH9M-GP-NF
SMB
GPIO
SYS_GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
LT32M
Rev
-3
Date: Monday, July 07, 2008
Sheet 28 of 54

MAIN SOURCE:20.F0411.003
SECOND SOURCE:20.D0246.103

20.F0714.003

KDS: RESO 32.768KHZ / 12P

GLAN_COMP place within 500 mil of ICH9M

U24A 1 OF 6

ICH9M-GP-NF

Place within 500 mils of ICH9 ball

Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

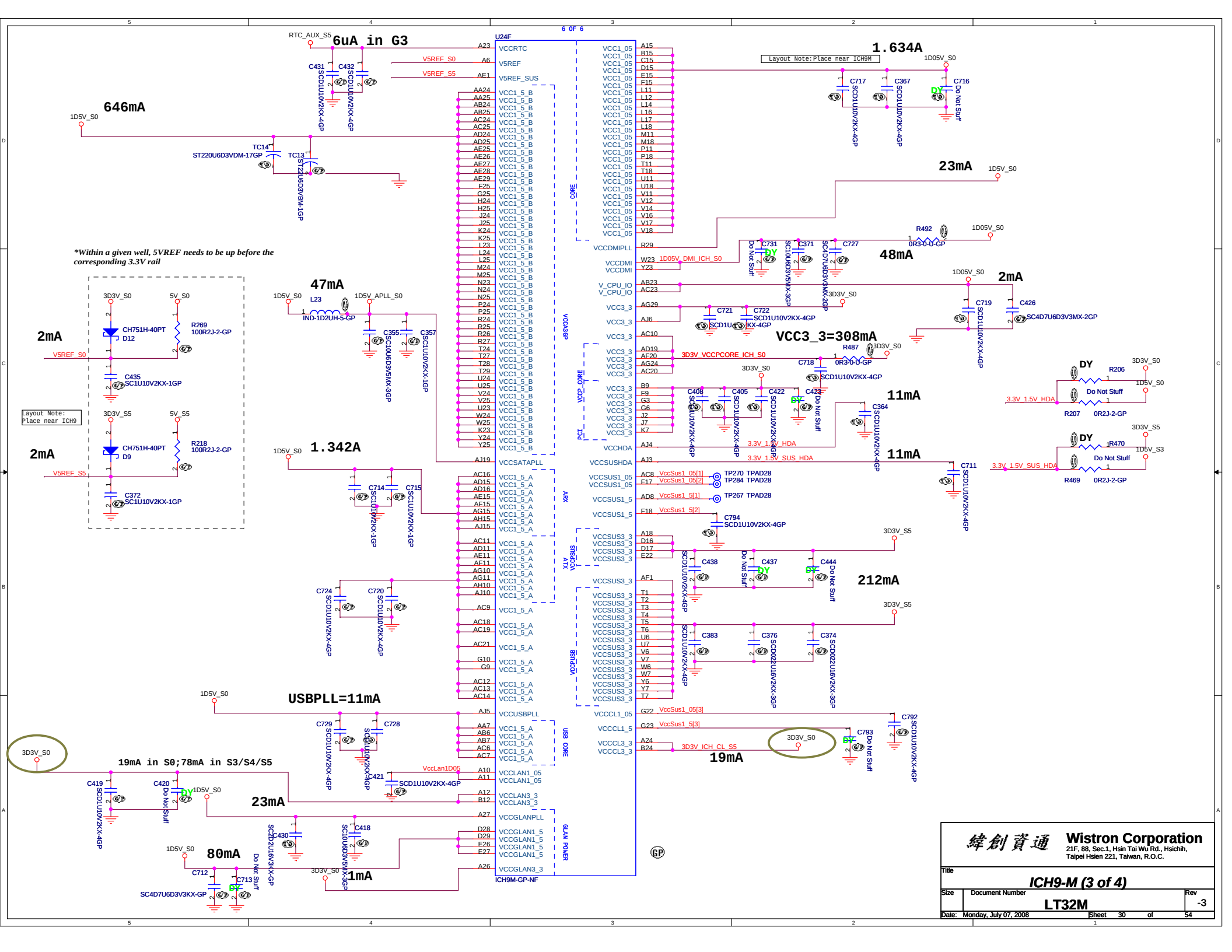
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH9-M (1 of 4)

Size: Document Number: LT32M Rev: -3

Date: Monday, July 07, 2008 Sheet 29 of 54


6uA in G3
646mA
1.634A
23mA
48mA
2mA
47mA
1.342A
VCC3_3=308mA
11mA
11mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
U24F
6 OF 6
ICH9M-GP-NF
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
LT32M
Monday, July 07, 2008
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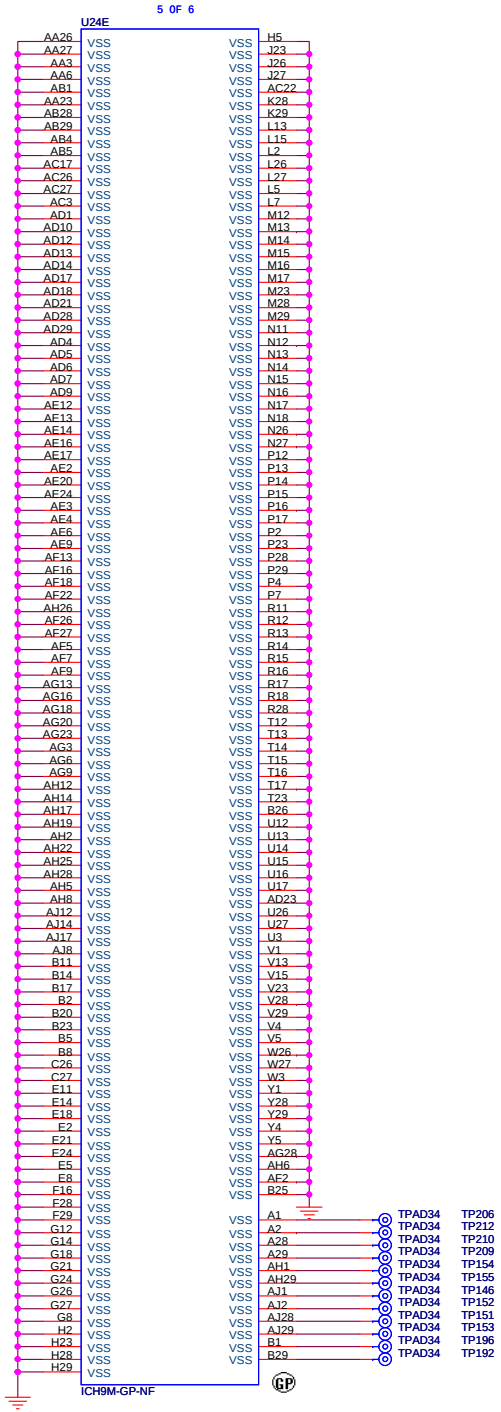
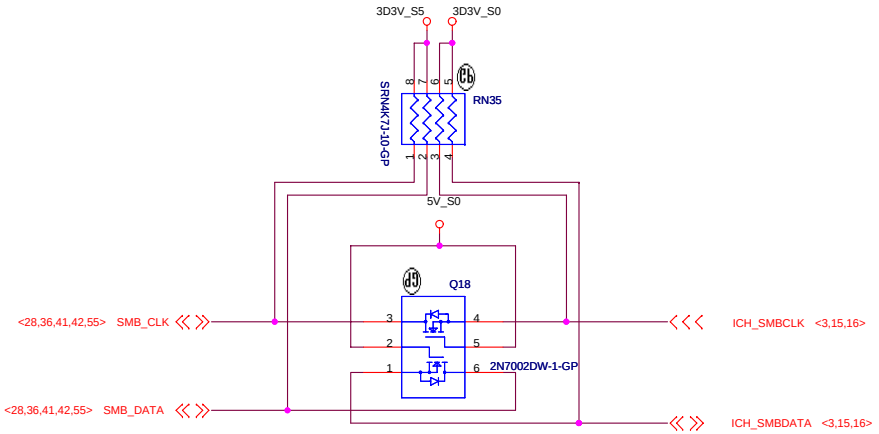
54
-3





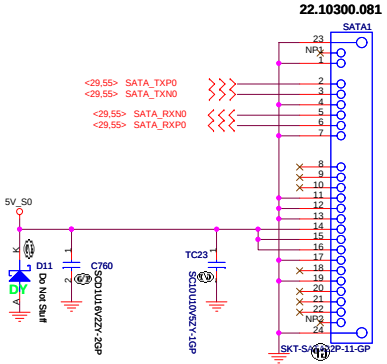
Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

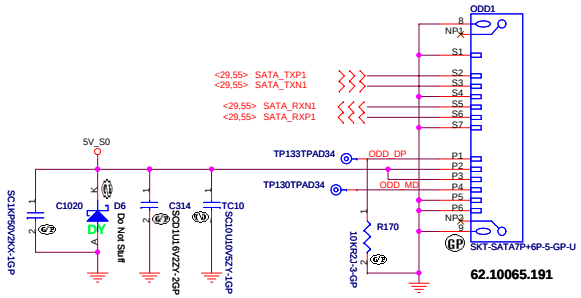
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH9-M (4 of 4)	
Size	Document Number: LT32M	Rev: -3
Date: Monday, July 07, 2008	Sheet 31 of 54	

SATA HD Connector



ODD Connector



Olympus LED's Location and Sequence

Left side				Right side
TouchPad-MUTE	POWER	Battery	WLAN	
LED1	LED3 LED8	LED4 LED5	LED6 LED7	

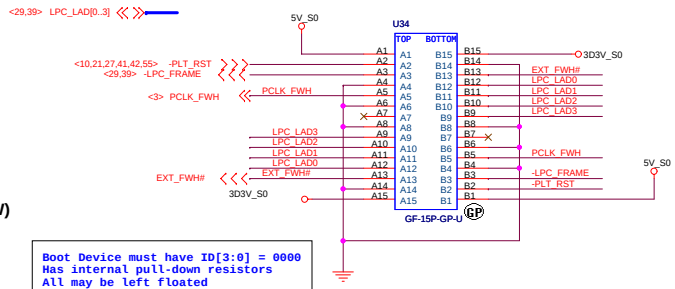
MAIN SOURCE:22.10300.081
SECOND SOURCE:20.80919.022

TOP VIEW

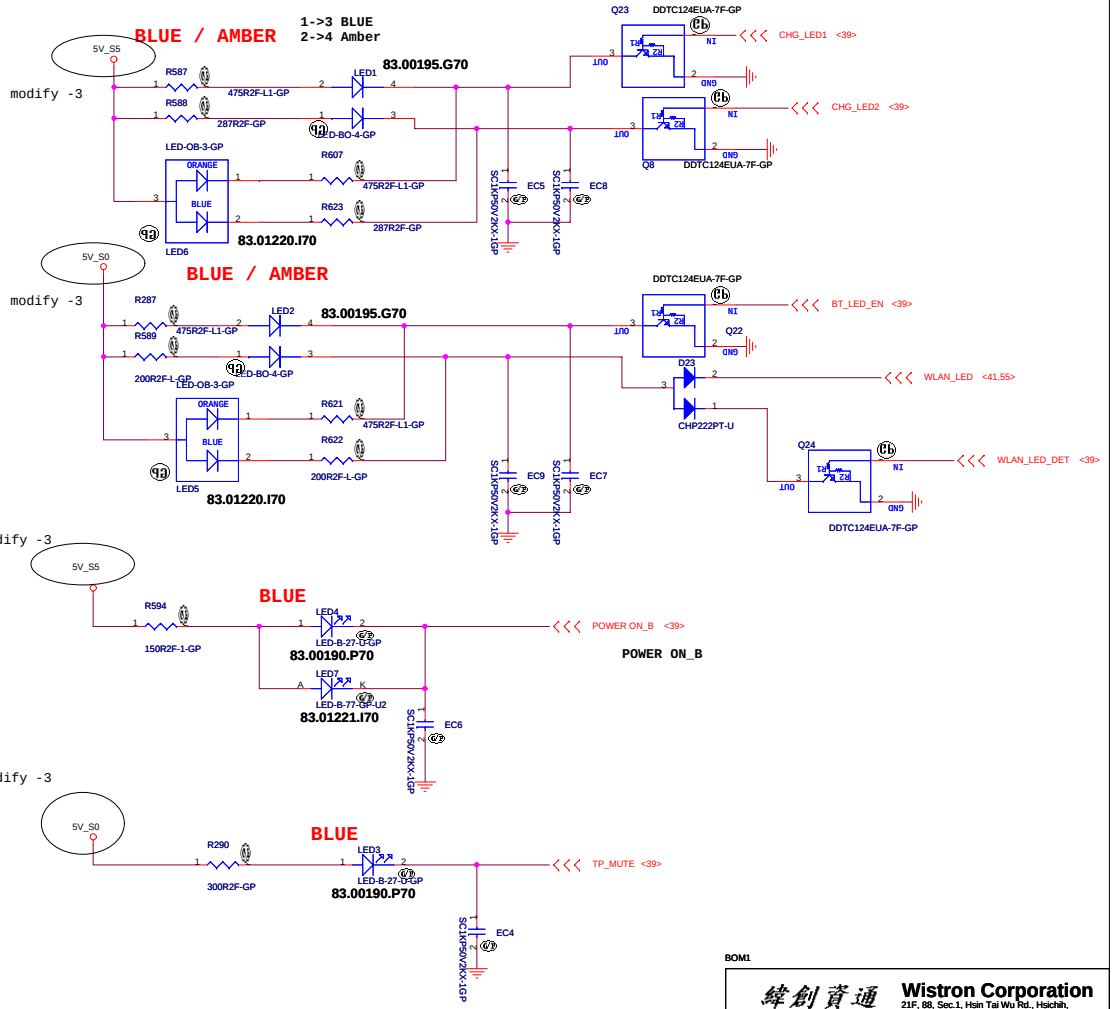
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



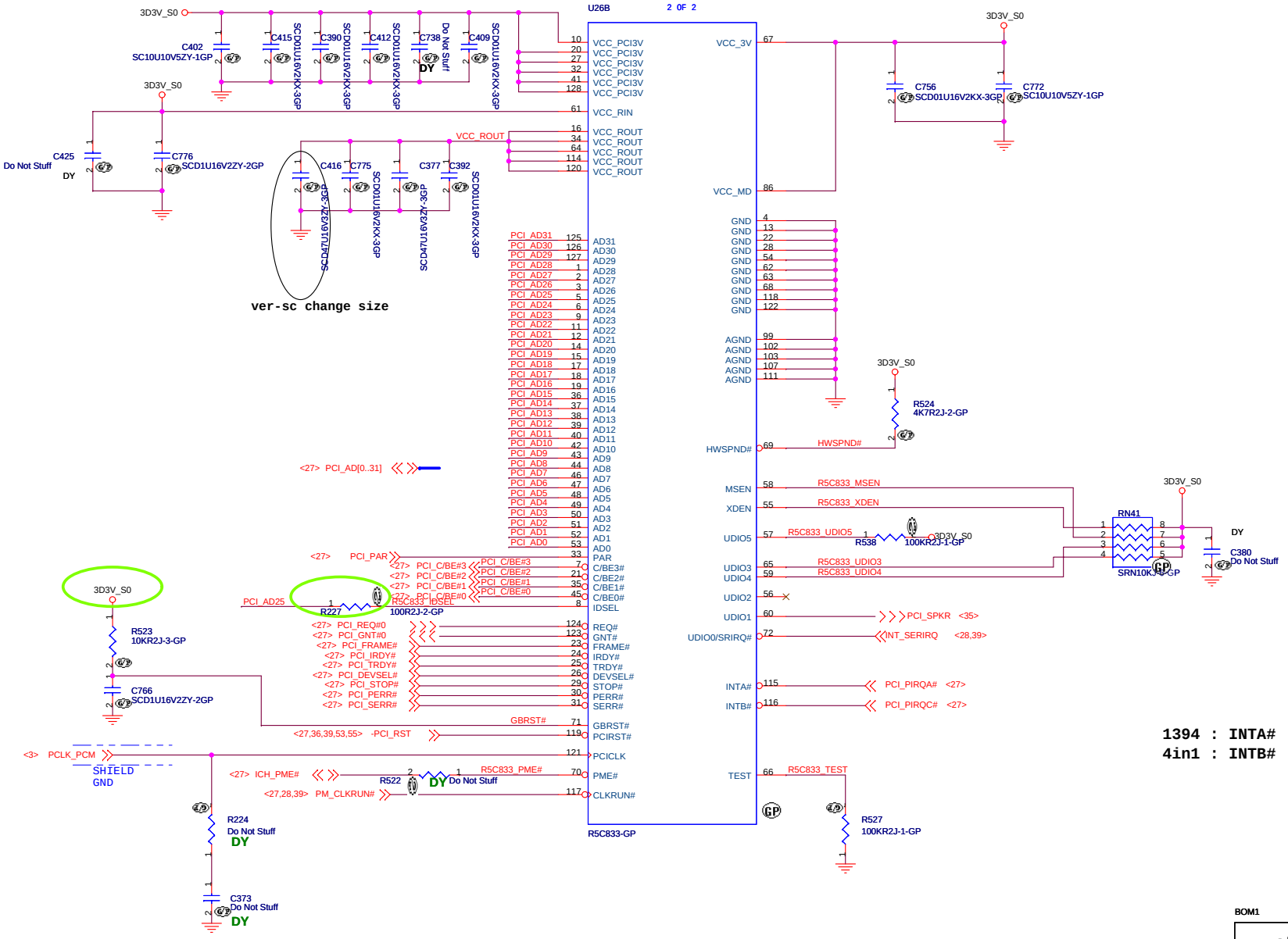
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/CDROM/DEBUG / LEDS

Size | Document Number: LT32M | Rev: -3

Date: Monday, July 07, 2008 | Sheet 32 of 54



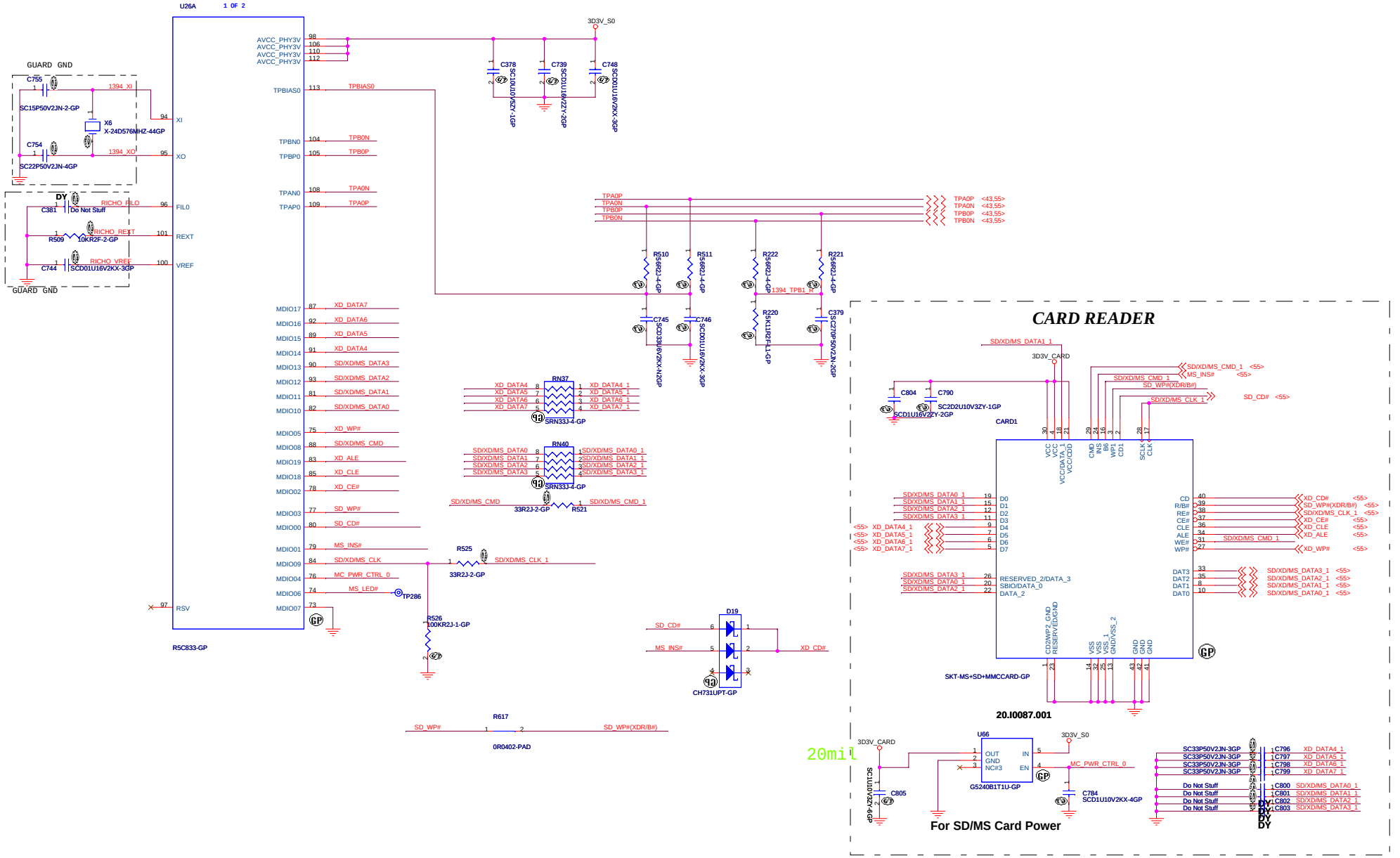
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/PCI

Size	Document Number	Rev
A3	LT32M	-3

Date: Monday, July 07, 2008 Sheet 33 of 54



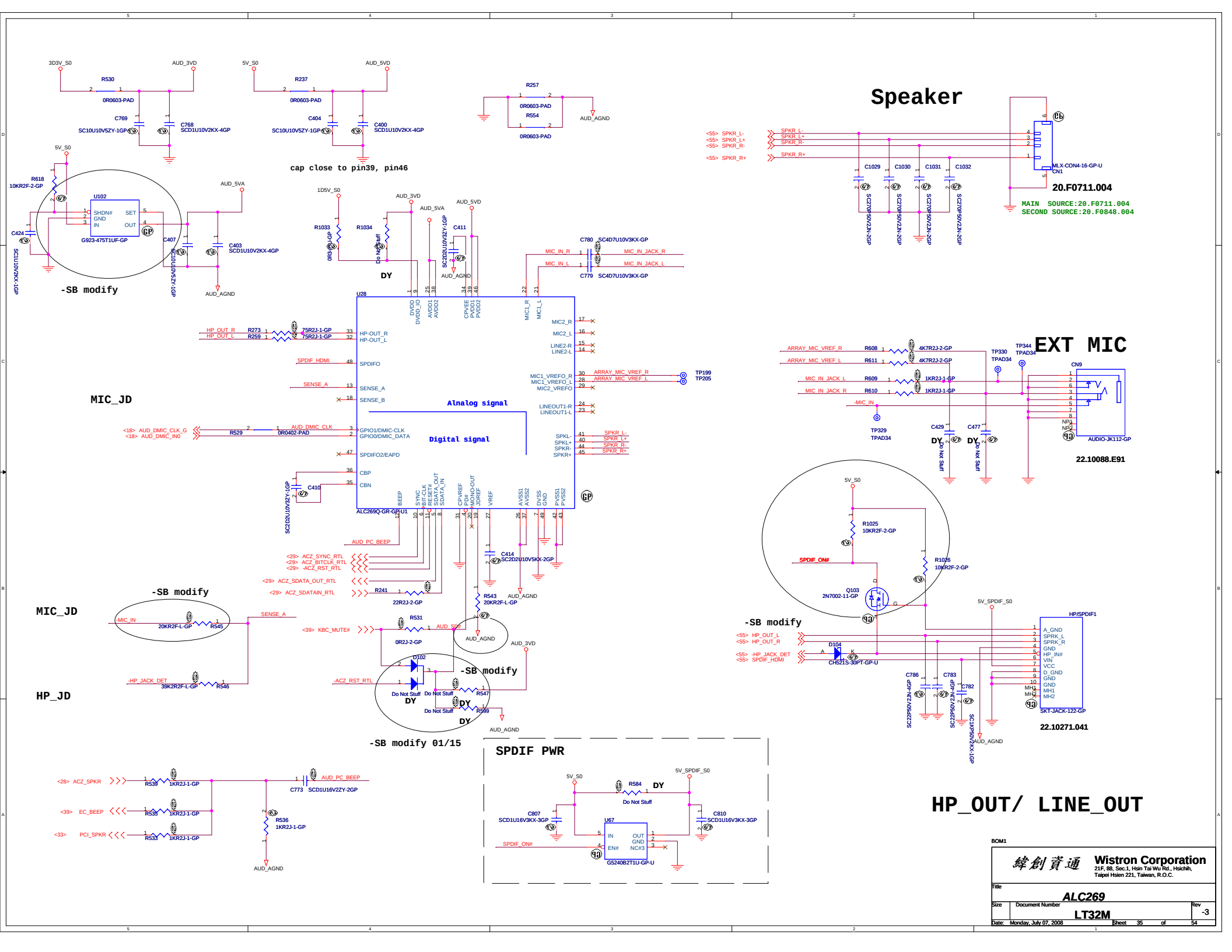
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C832/IEEE1394/SD/BT

Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 34 of 54


Speaker
20.F0711.004
MAIN SOURCE:20.F0711.004
SECOND SOURCE:20.F0848.004
EXT MIC
22.10088.E91
MIC_JD
HP_JD
-SB modify
-SB modify 01/15
Alnalog signal
Digital signal
cap close to pin39, pin46
SPDIF PWR
22.10271.041
HP_OUT/ LINE_OUT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ALC269
LT32M
-3
Monday, July 07, 2008
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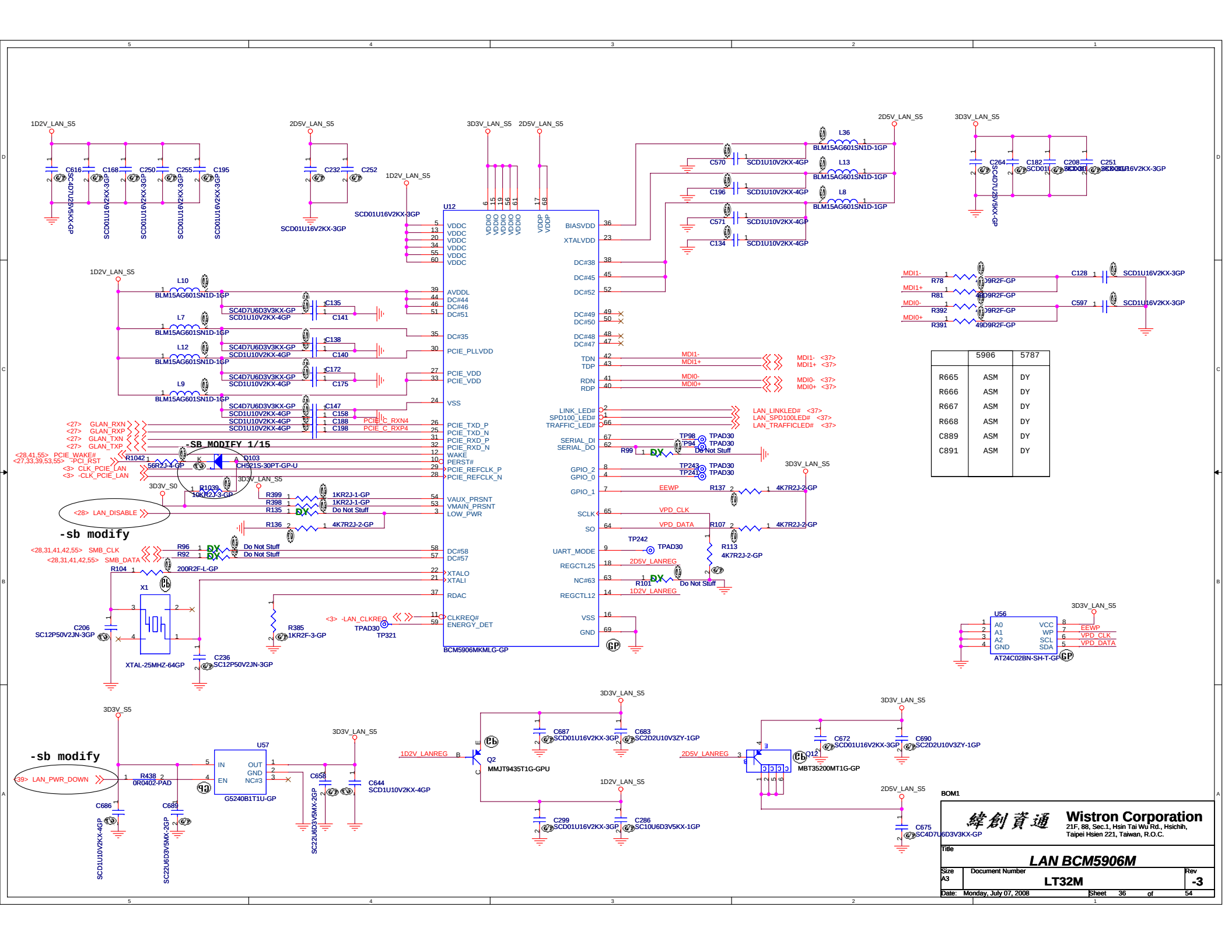
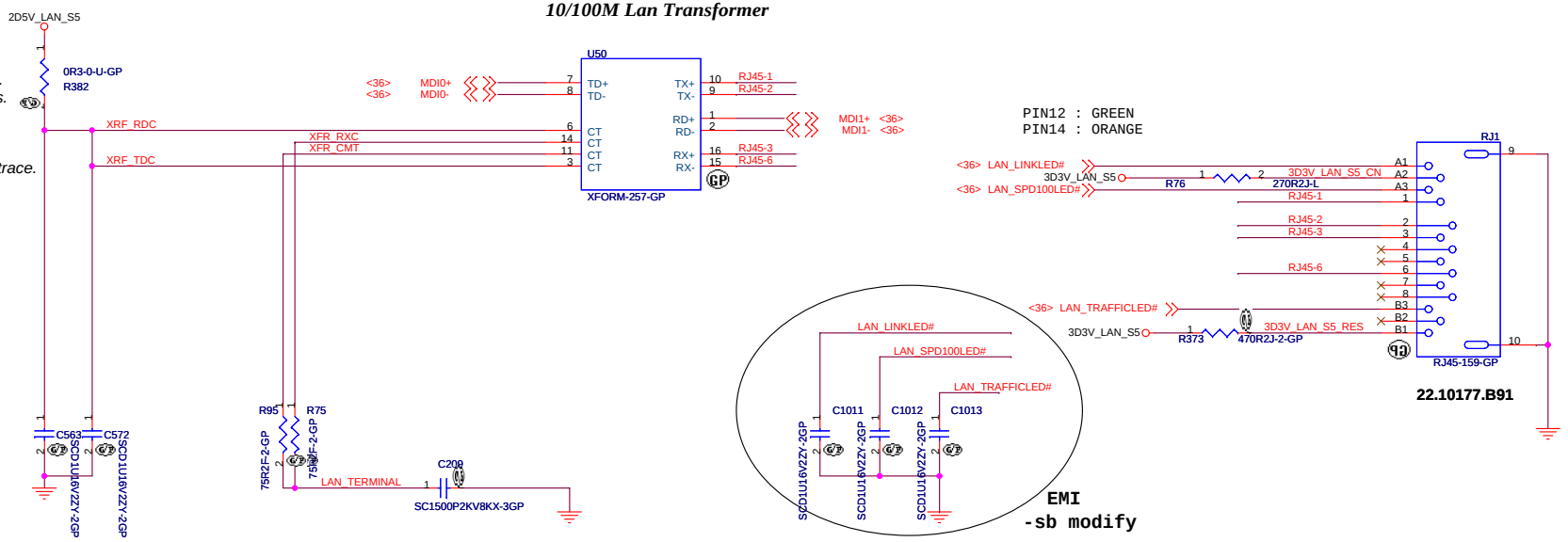
54



	5906	5787
R665	ASM	DY
R666	ASM	DY
R667	ASM	DY
R668	ASM	DY
C889	ASM	DY
C891	ASM	DY

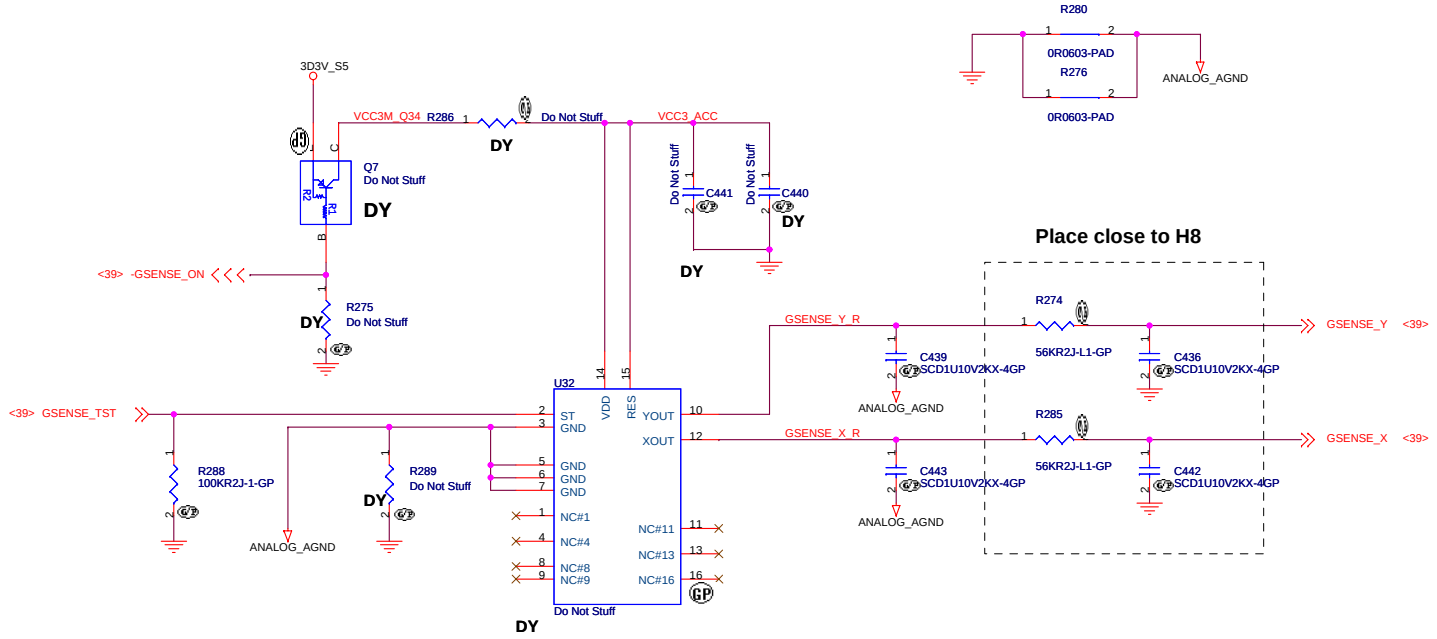
10/100M Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***LAN connector/NEW CARD/SIM***		
Size: A3	Document Number: **LT32M**	Rev: **-3**
Date: Monday, July 07, 2008	Sheet 37 of 54	



Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil for three Output traces

	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C439, C443, Q7, R286, R275, C441, C440, R288, R289 close to U32.

(2) Avoid routing under DCDC switching area.

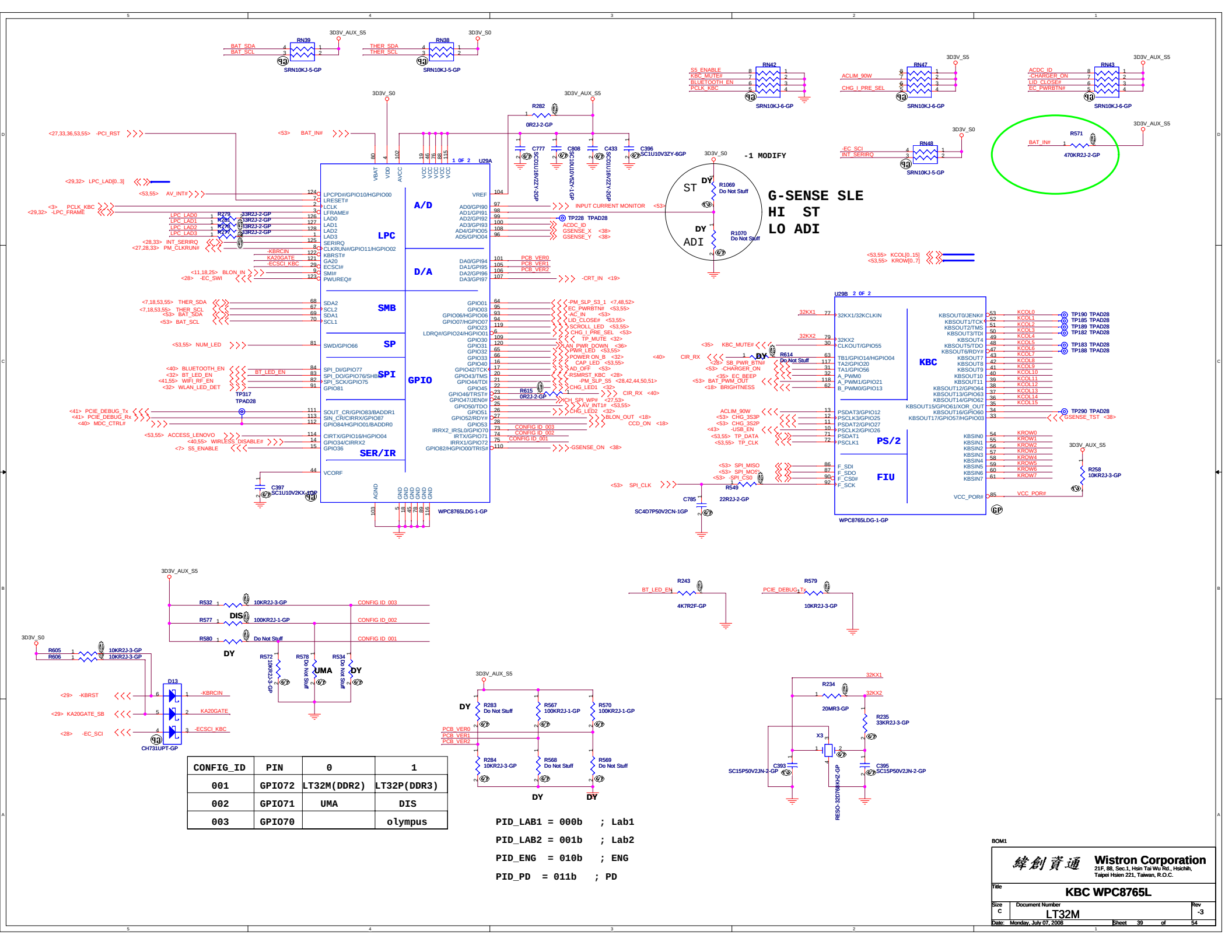
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***G-SENSOR***

Size	Document Number	Rev
A3	LT32M	-3

Date: Monday, July 07, 2008 Sheet 38 of 54



CONFIG_ID	PIN	0	1
001	GPIO72	LT32M(DDR2)	LT32P(DDR3)
002	GPIO71	UMA	DIS
003	GPIO70		olympus

```
PID_LAB1 = 000b   ; Lab1
PID_LAB2 = 001b   ; Lab2
PID_ENG  = 010b   ; ENG
PID_PD   = 011b   ; PD
```

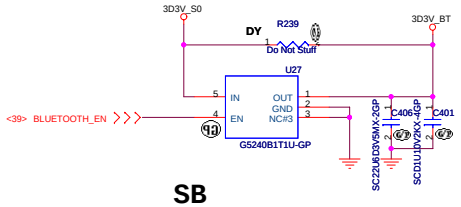
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KBC WPC8765L**

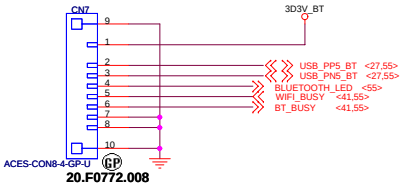
Size	Document Number	Rev
C	LT32M	-3

Date: Monday, July 07, 2008 Sheet 39 of 54



SB

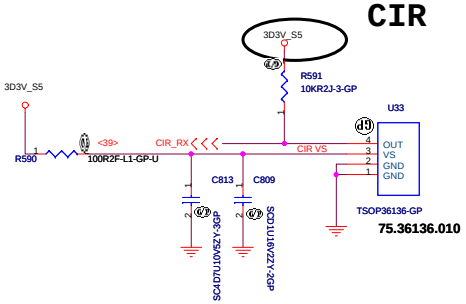
BT CONNECTOR



20.F0772.008

MAIN SOURCE:20.F0772.008
SECOND SOURCE:20.F0983.008

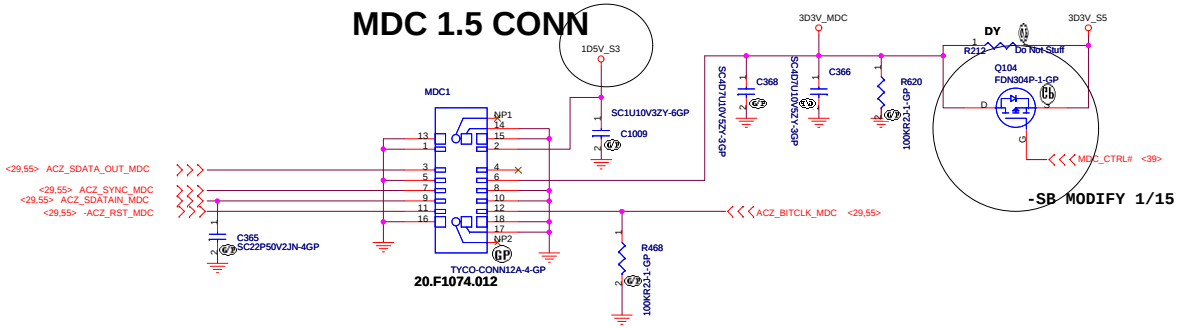
CIR



75.36136.010

-2 MODIFY 1/15

MDC 1.5 CONN

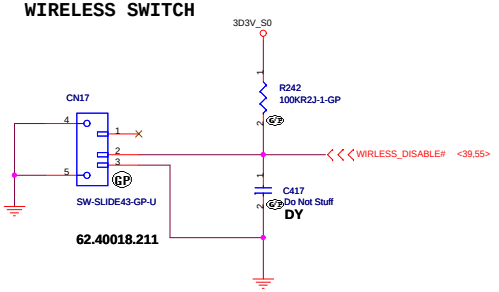


20.F1074.012

-SB MODIFY 1/15

MAIN SOURCE:20.F1074.012
SECOND SOURCE:20.F0676.012

WIRELESS SWITCH



62.40018.211

BOM1

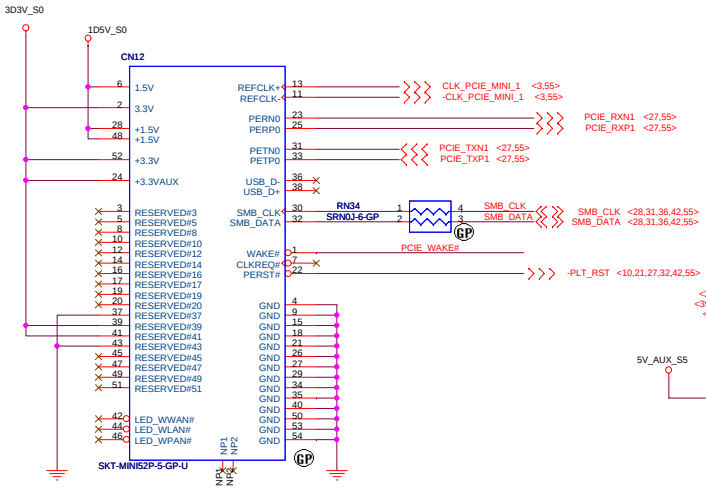
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Module_Blue Tooth/Modem/CIR	
Size	Document Number: LT32M	Rev: -3
Date: Monday, July 07, 2008	Sheet 40 of 54	

Mini PCI-E Connector

Only port-1 support USB

For Robson

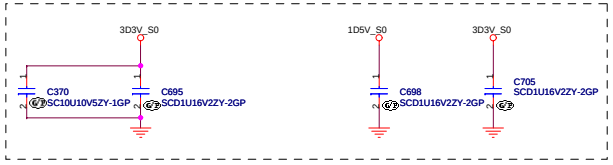
Port-1 High



20.F0832.052

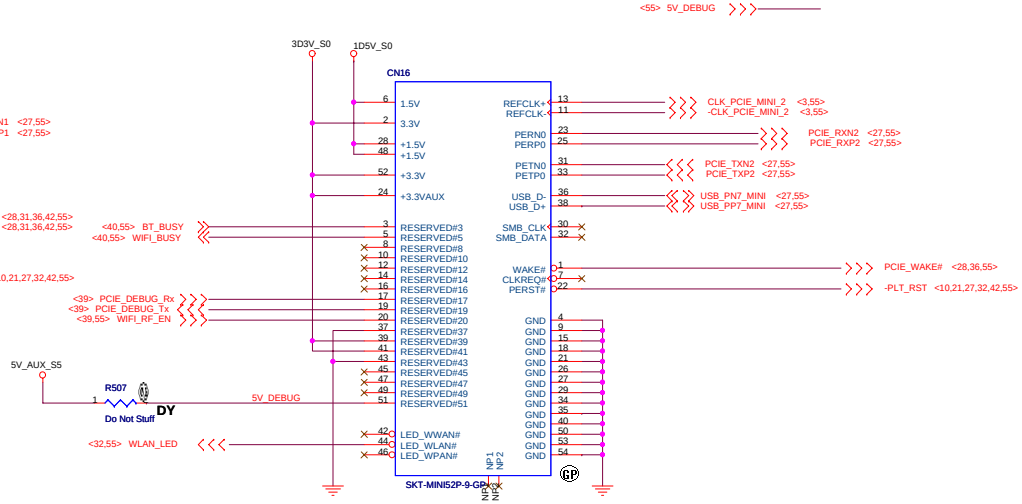
MAIN SOURCE:20.F0832.052

SECOND SOURCE:20.F1107.052



Mini PCI-E Connector

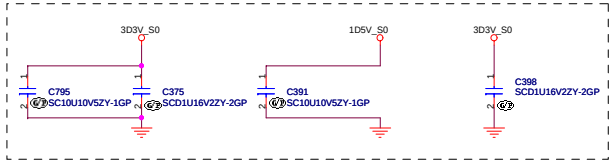
Port-2 low



62.10043.411

MAIN SOURCE:62.10043.411

SECOND SOURCE:20.F1084.052



BOM1

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD CONN .

Size: C | Document Number: LT32M | Rev: -3

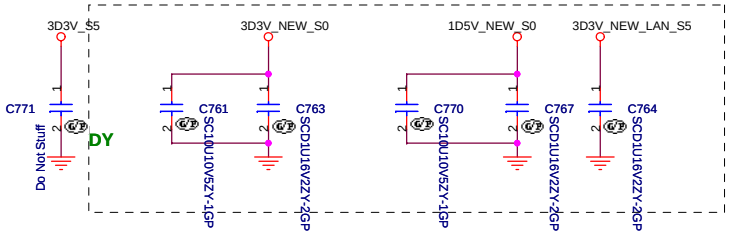
Date: Monday, July 07, 2008 | Sheet 41 of 54

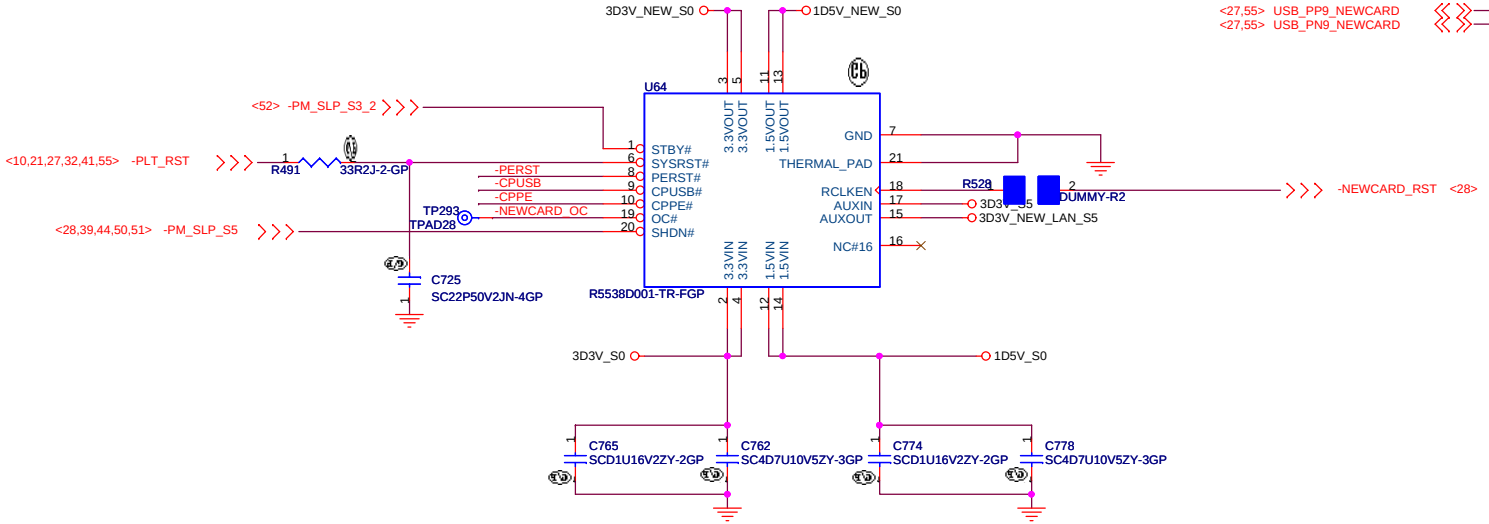
NEWCARD Connector

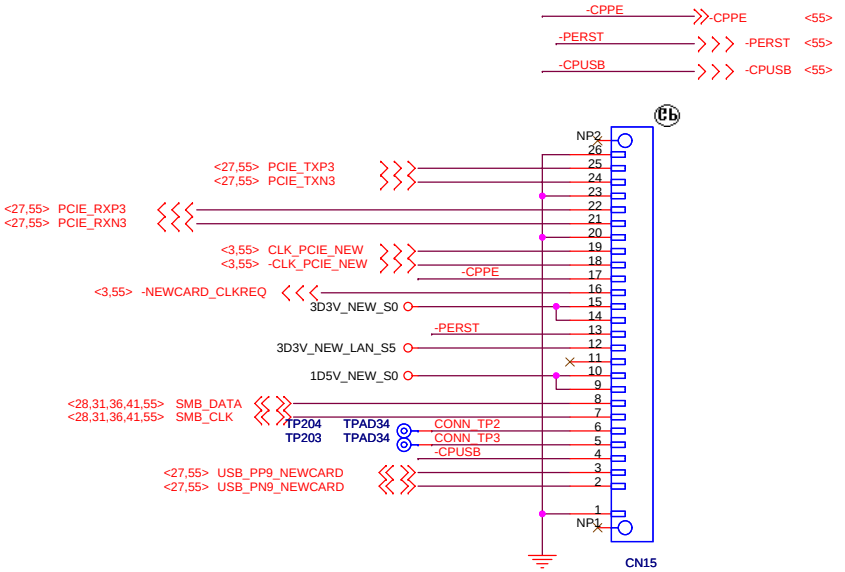
For Newcard socket

Place them Near to Chip

Place them Near to Connector







BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

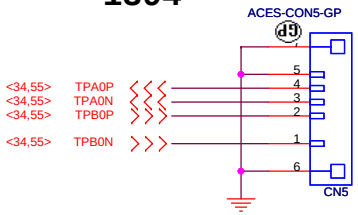
Title: Module_NewCard

Size	Document Number	Rev
	LT32M	-3

Date: Monday, July 07, 2008 Sheet 42 of 54

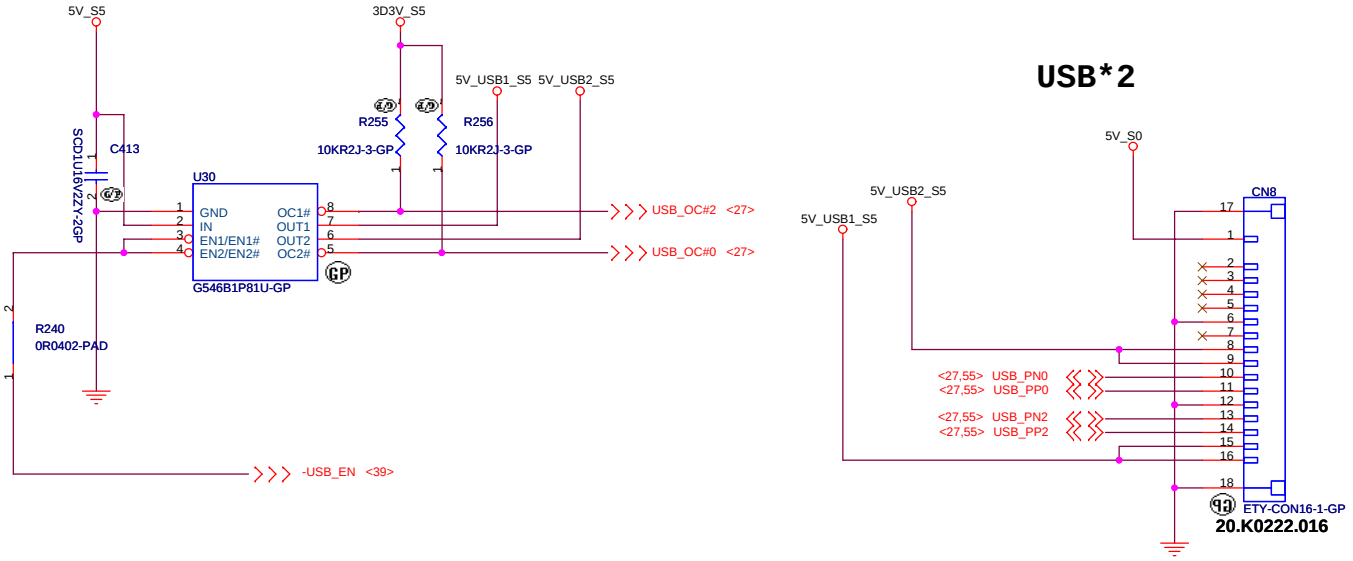
Low -End USB BOARD

1394



MAIN SOURCE:20.k0196.005
SECOND SOURCE:20.K0212.008

USB*2



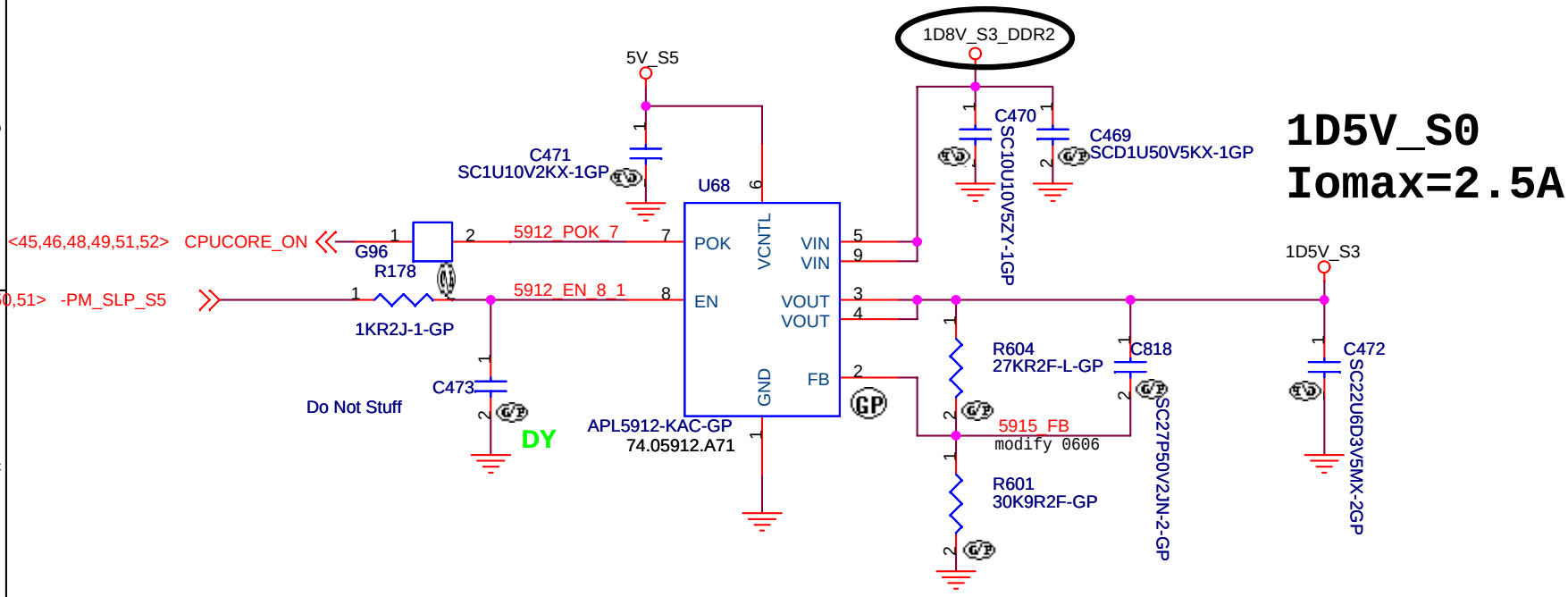
BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB I/O & 1394 CNN***

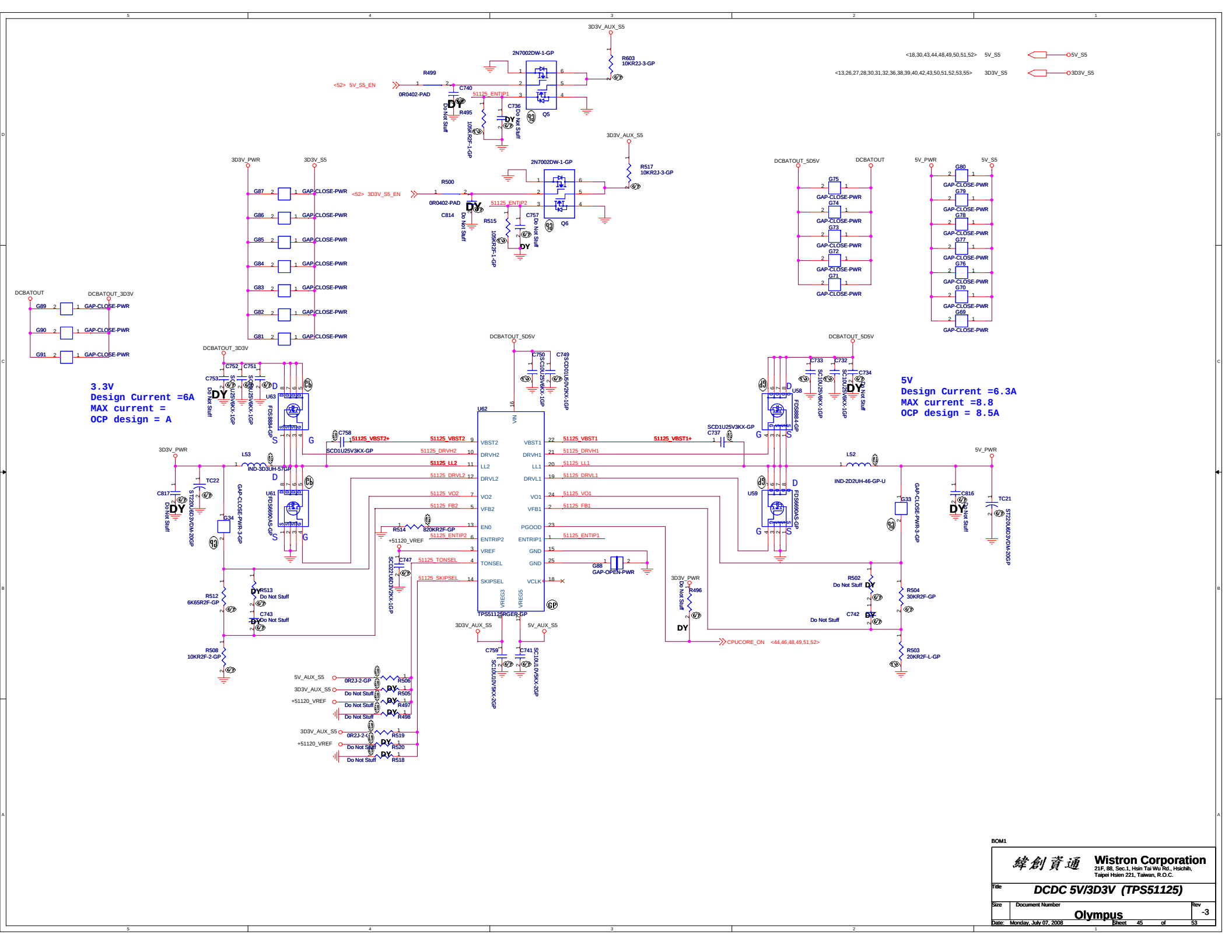
Size	Document Number	Rev
B	LT32M	-3

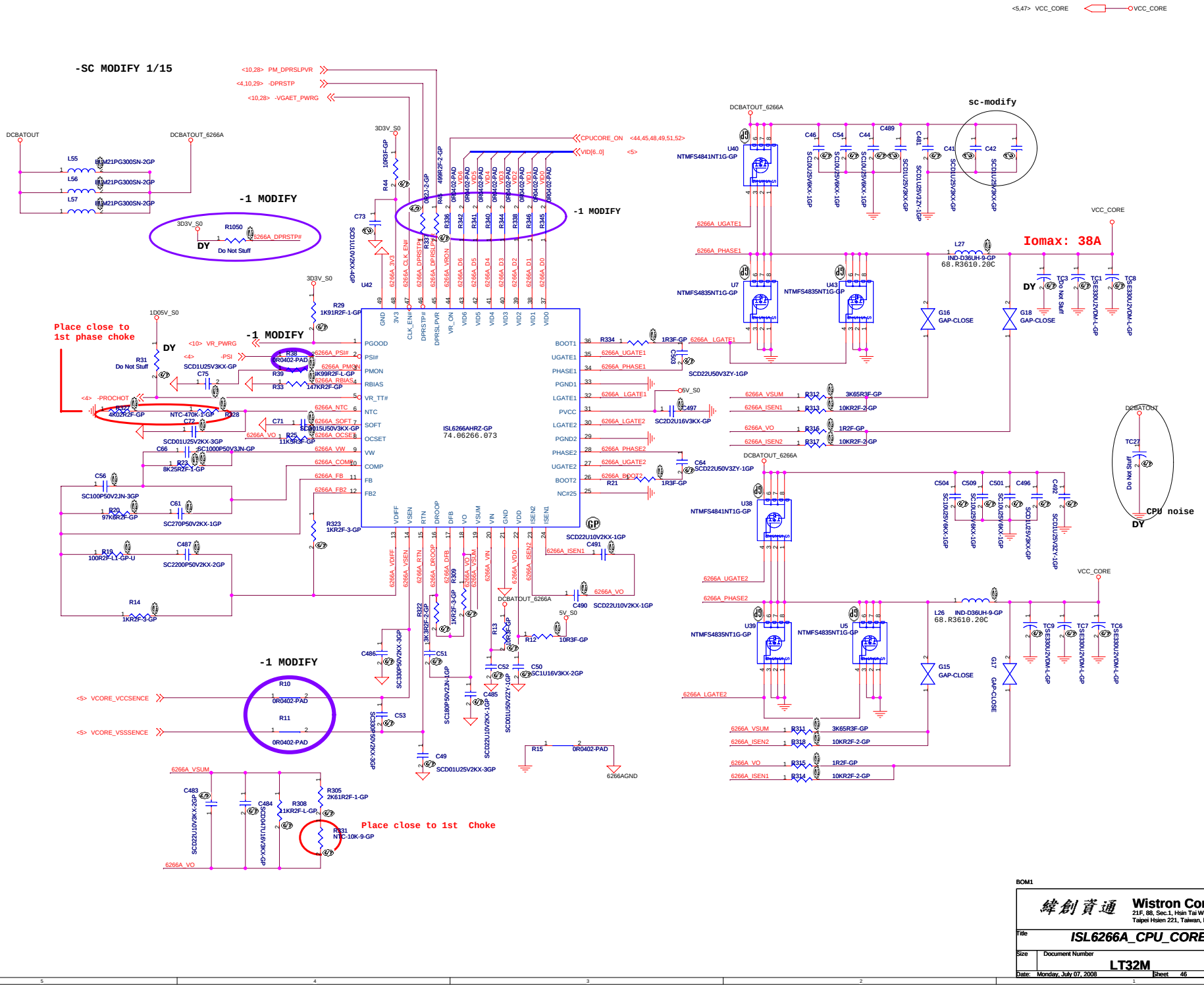
Date: Monday, July 07, 2008 Sheet 43 of 54



BOM1

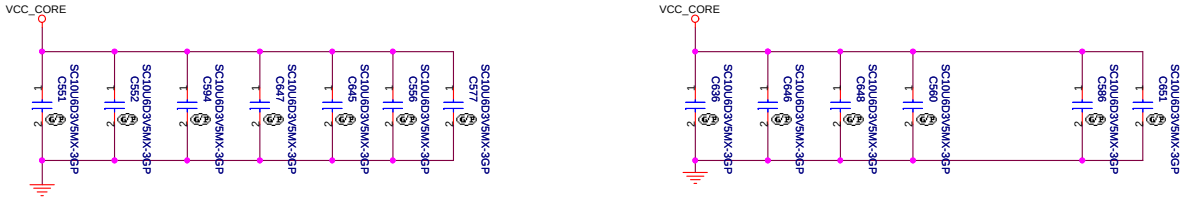
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***1D5V_S0***	
Size	Document Number **Olympus**	Rev -3
Date: Monday, July 07, 2008	Sheet 44 of 55	


3.3V
Design Current =6A
MAX current =
OCP design = A
5V
Design Current =6.3A
MAX current =8.8
OCP design = 8.5A
TPS51125RGER-GP
2N7002DW-1-GP
FDS8884-GP
FDS6690AS-GP
IND-3D3UH-57-GP
IND-2D2UH-46-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Olympus
Monday, July 07, 2008
Sheet 45 of 53
-3

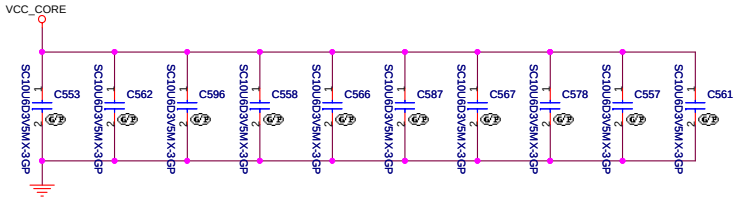


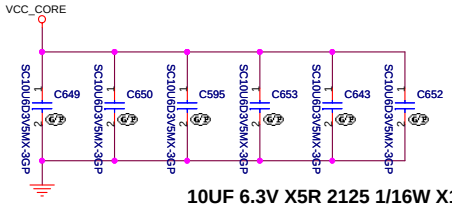
BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL6266A_CPU_CORE	
Size	Document Number	Rev
	LT32M	-3
Date: Monday, July 07, 2008	Sheet 46 of 55	



10UF 6.3V X5R 2125 1/16W X16 PCS





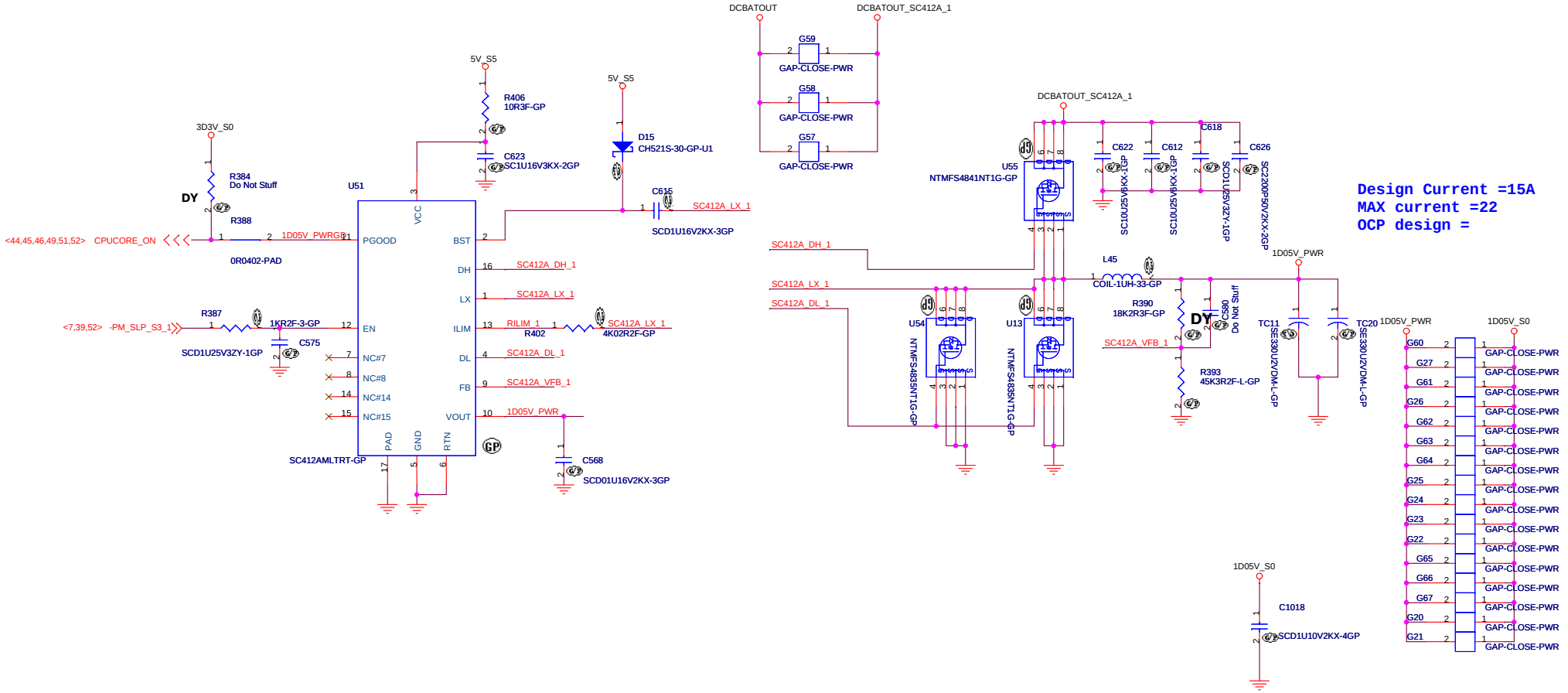
10UF 6.3V X5R 2125 1/16W X16 PCS

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VCCCPUCORE DECOUPLING***

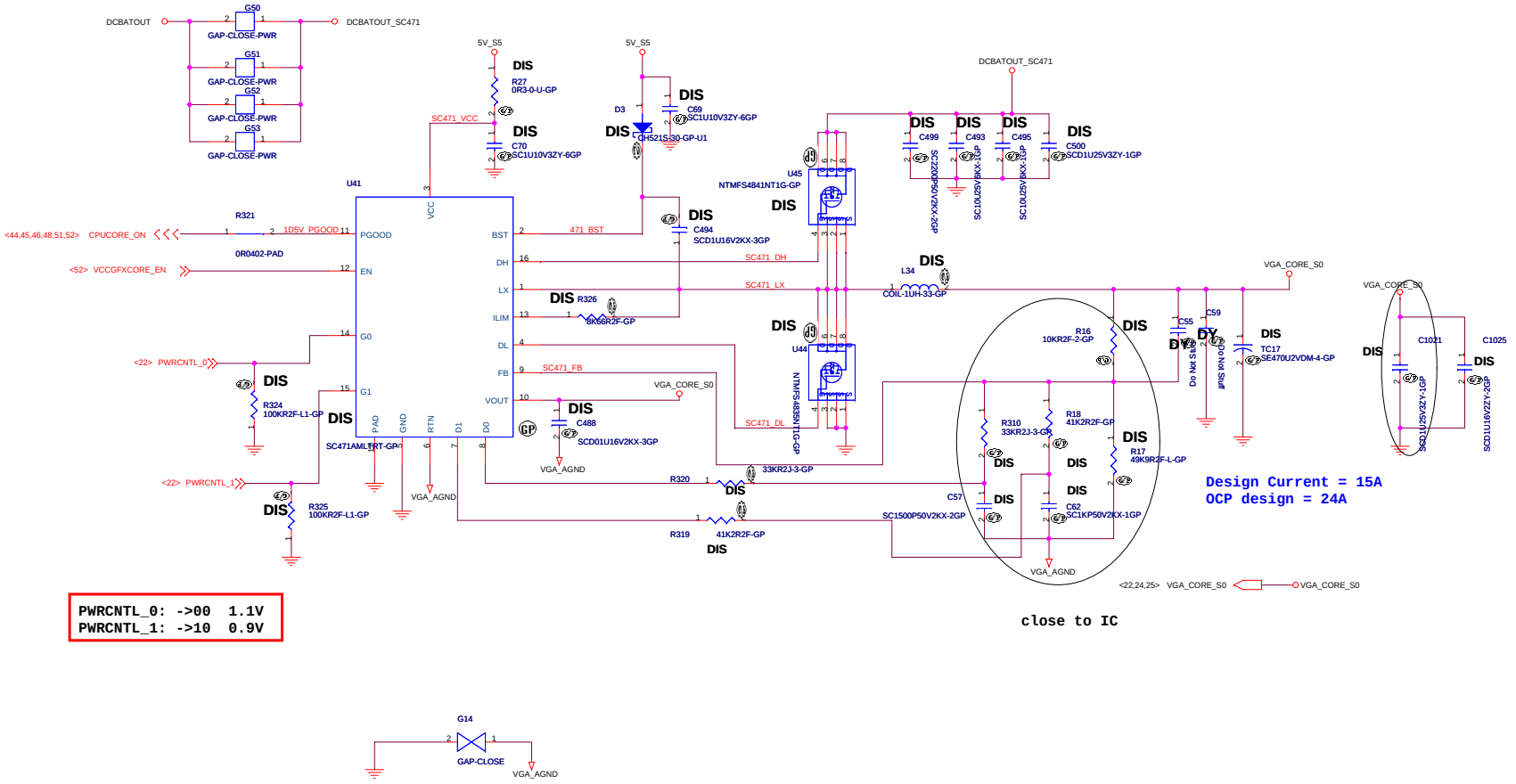
Size	Document Number	Rev
Custom	LT32M	-3
Date: Monday, July 07, 2008	Sheet 47 of 55	



BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***SC412A +1.05VM***	
Size A3	Document Number **LT32M**	Rev **-3**
Date: Monday, July 07, 2008	Sheet 48 of 55	



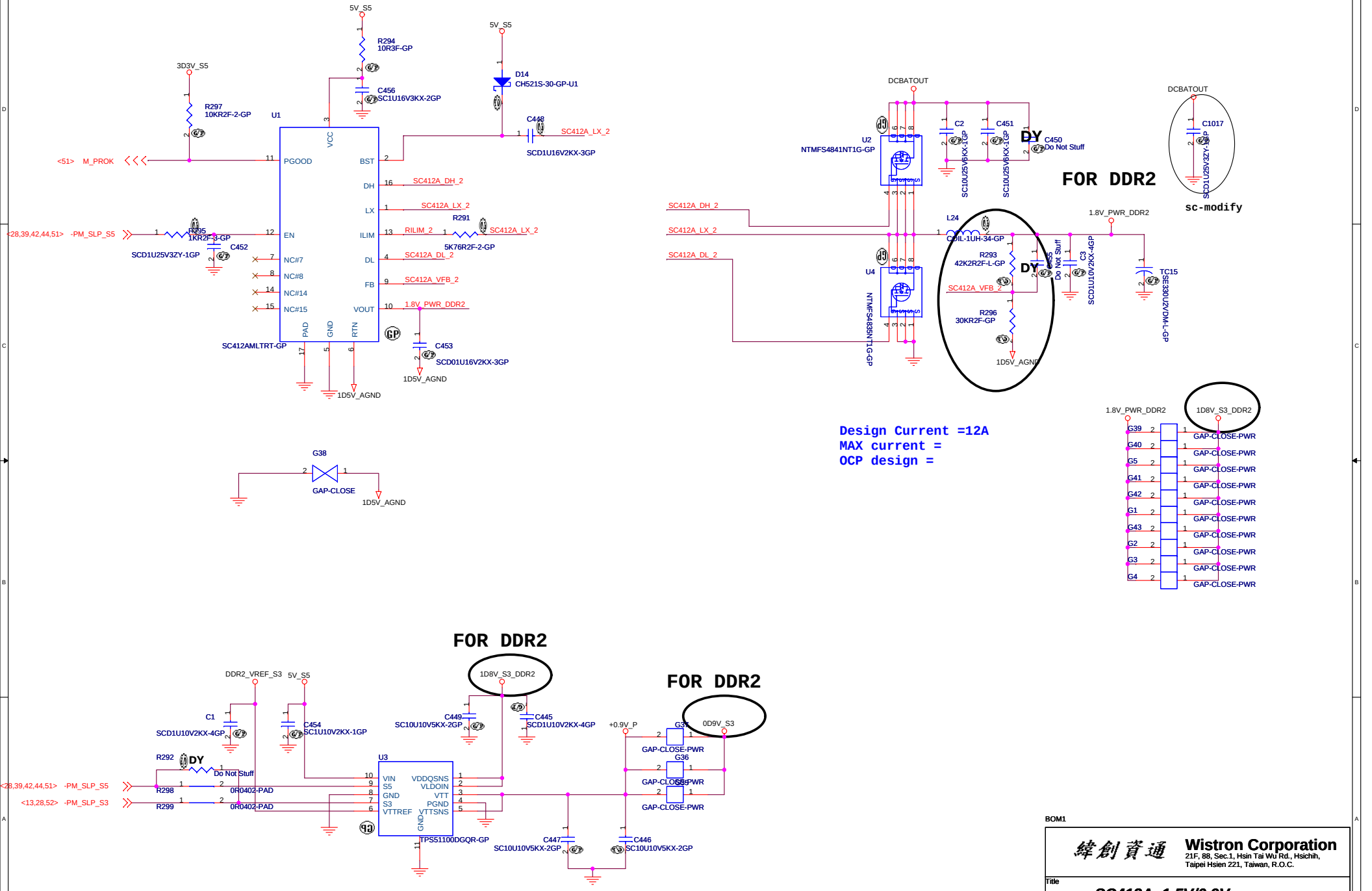
BOM1

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC471A VGA CORE

Size	Document Number	Rev
C	LT32M	-3

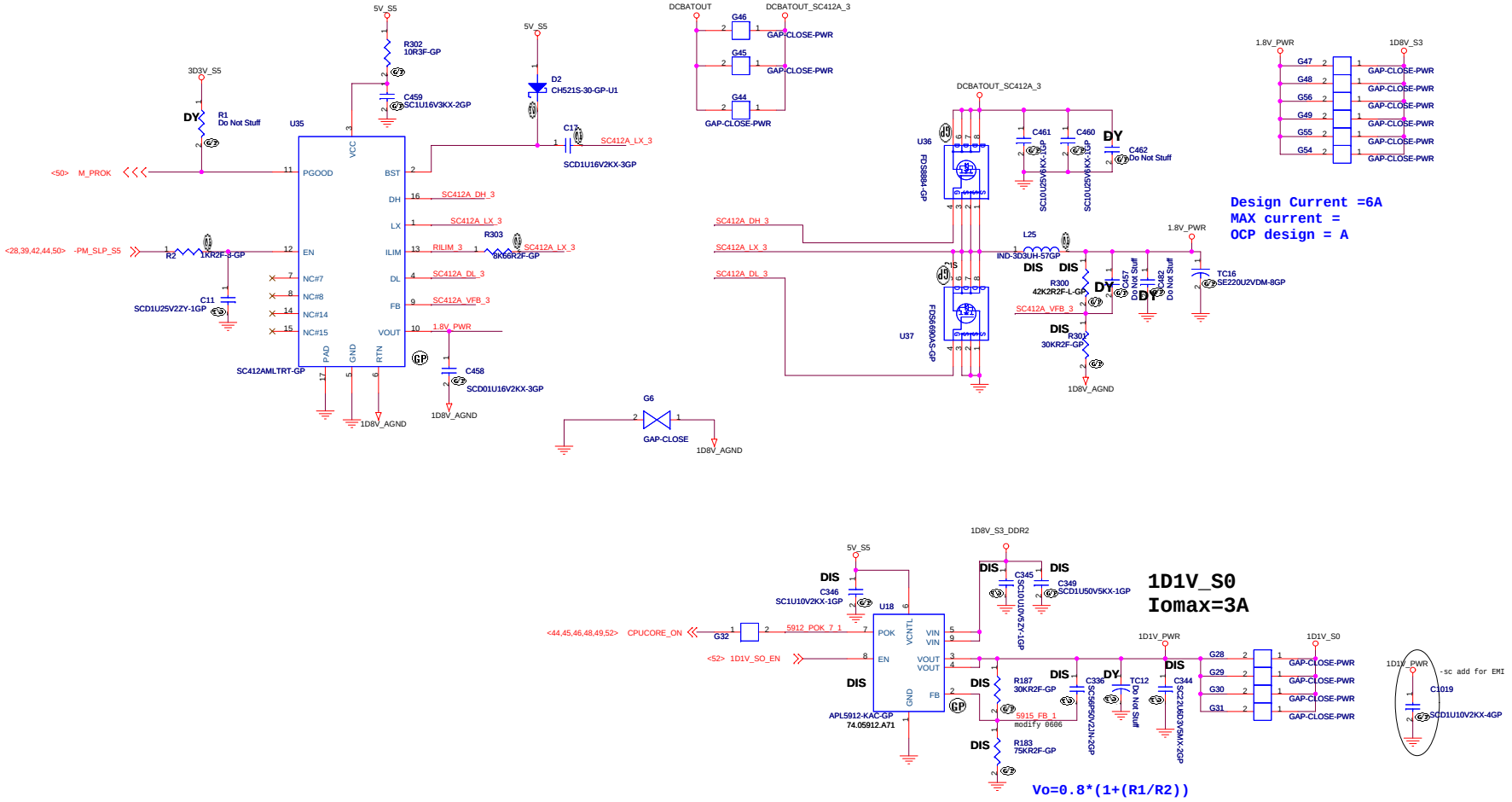
Date: Monday, July 14, 2008 Sheet 49 of 55



BOM1

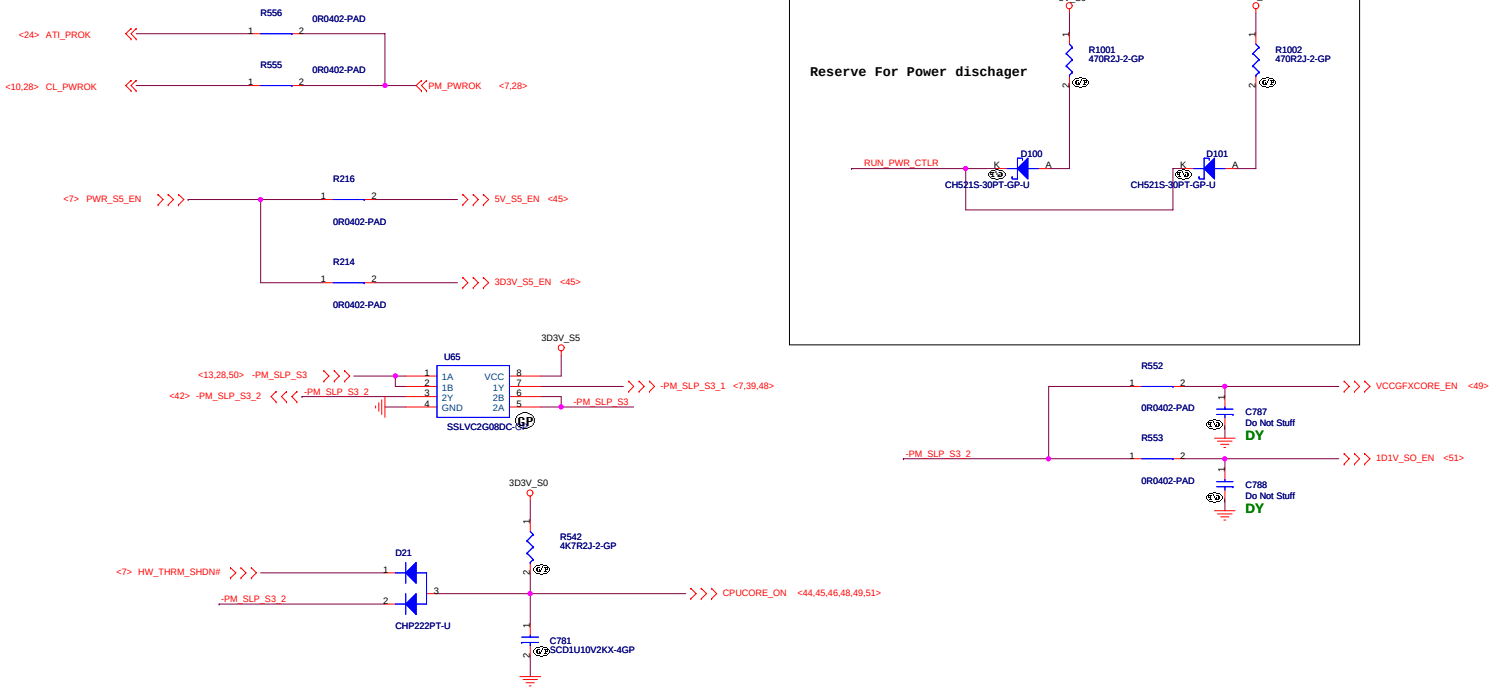
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
SC412A_1.5V/0.9V		
Size	Document Number	Rev
	LT32M	-3
Date: Monday, July 07, 2008	Sheet 50 of 55	

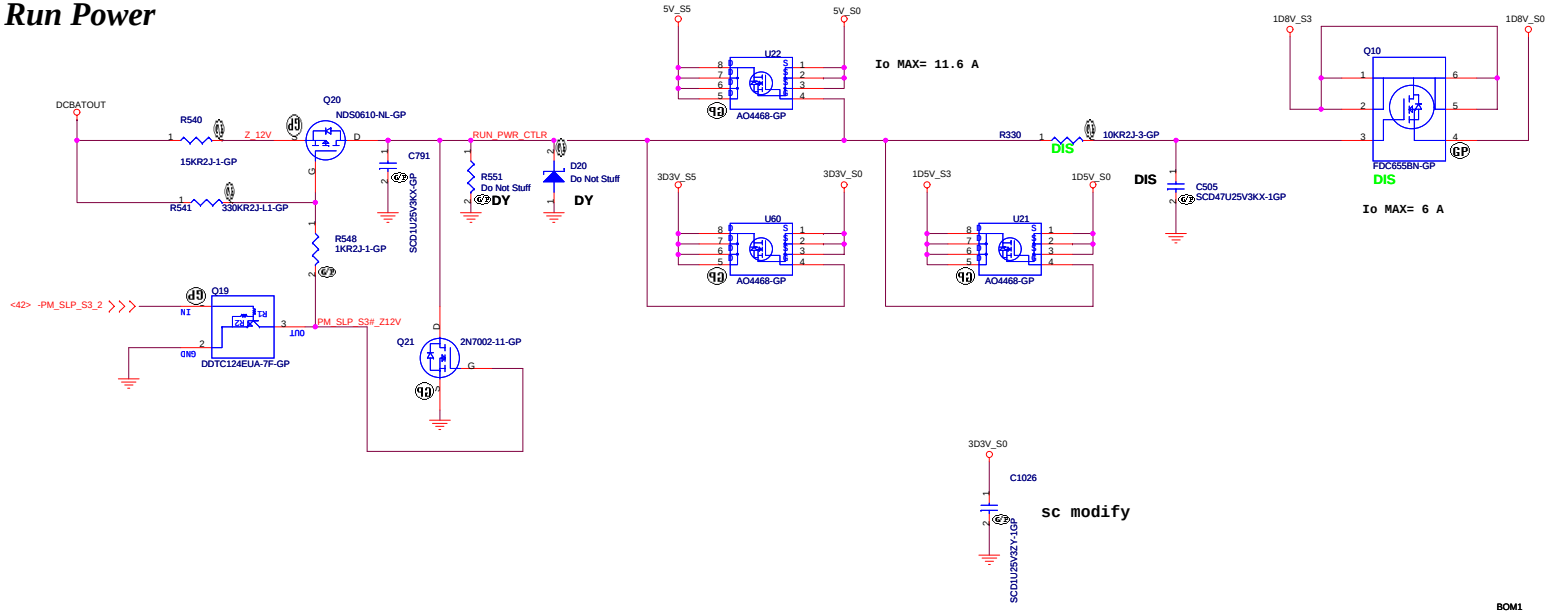


BOM1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SC412A_1.8V/1.1V***	
Size	Document Number **LT32M**	Rev -3
Date: Monday, July 07, 2008	Sheet 51 of 55	

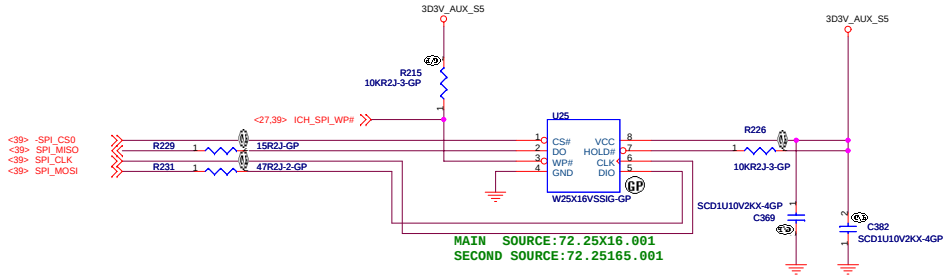


Run Power

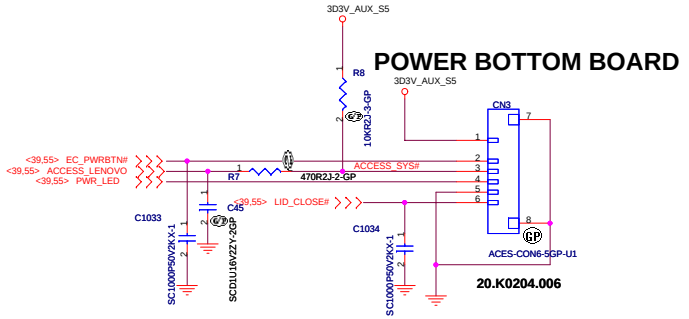


BOM1

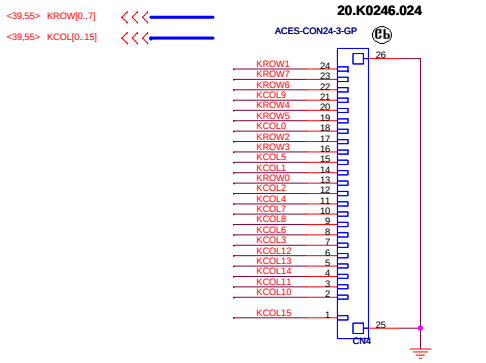
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWRPLANE&RESET LOGIC***	
Size	Document Number **LT32M**	Rev -3
Date: Monday, July 07, 2008	Sheet 52 of 55	



SPI FLASH

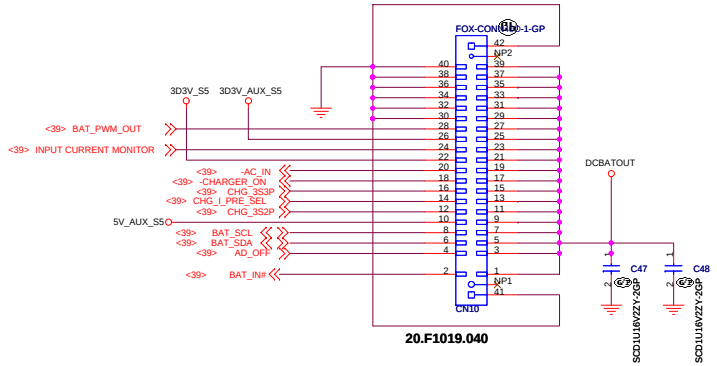


POWER BOTTOM BOARD



MAIN SOURCE:20.K0246.024

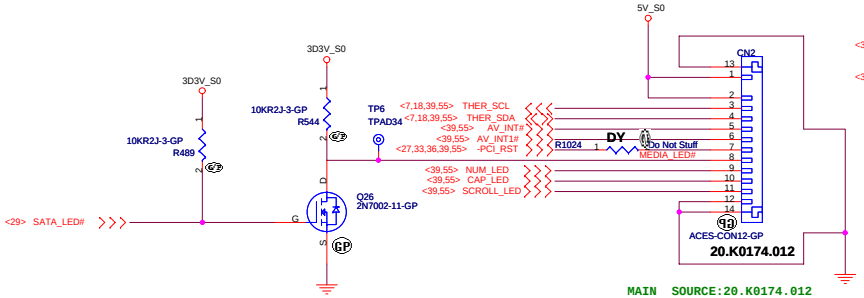
KEYBORD CONNECTOR



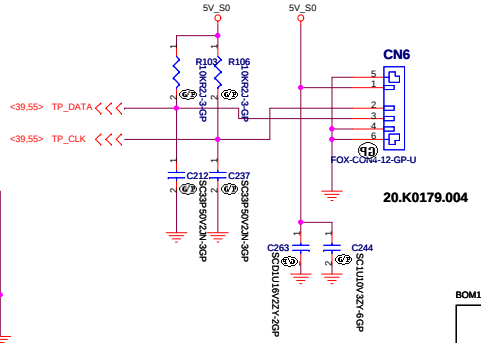
CHARGER CONNECTOR

AV Panel

TouchPad Connector

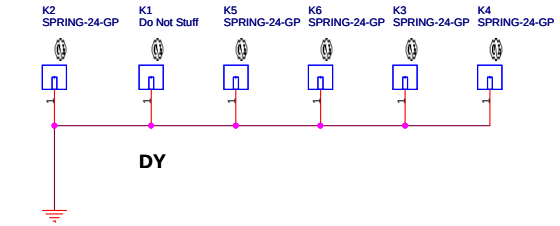


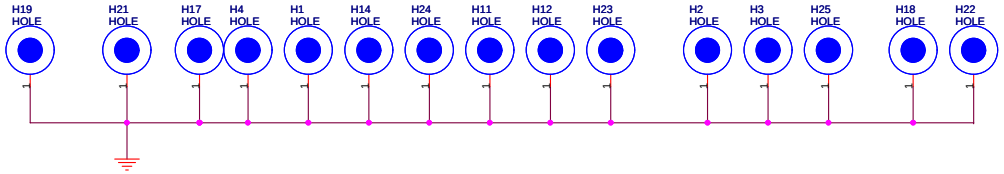
MAIN SOURCE:20.K0174.012
SECOND SOURCE:20.K0210.012

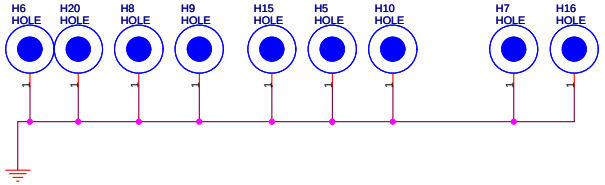


BOM1

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	KB/TP/SPI/AV/Charger	
Size	Document Number	Rev
	LT32M	-3
Date: Monday, July 07, 2008	Sheet 53 of 55	







BOM1

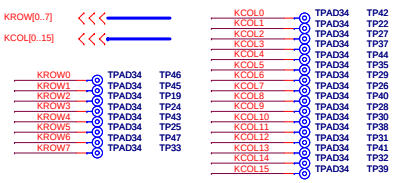
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PTH FOR SCREW HOLES***

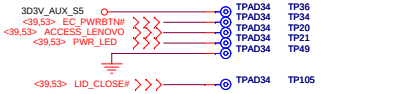
Size	Document Number	Rev
Custom	LT32M	-3

Date: Monday, July 07, 2008 Sheet 54 of 55

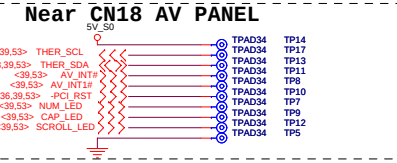
Near CN13 KB



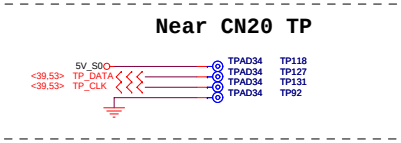
Near CN3 POWER BOOTOM BOARD



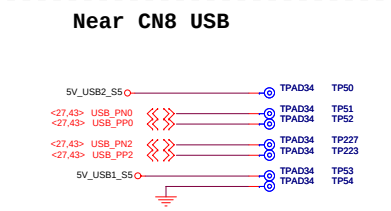
Near CN18 AV PANEL



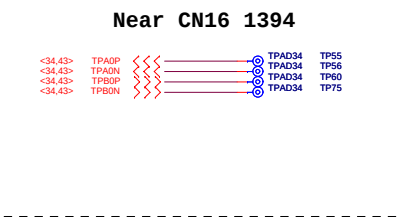
Near CN20 TP



Near CN8 USB



Near CN16 1394



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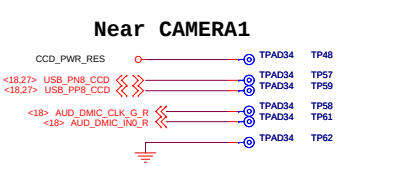

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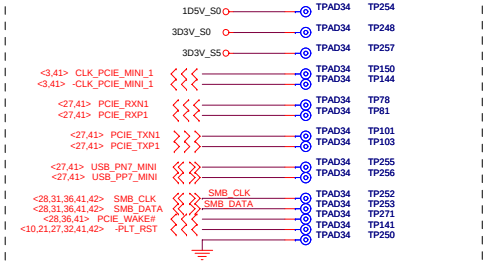

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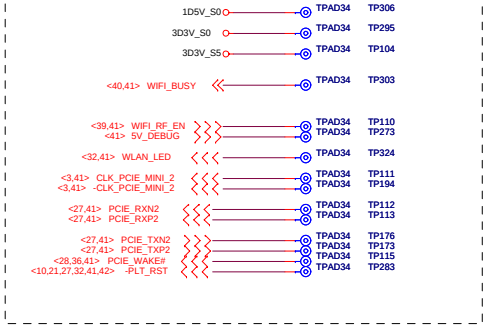

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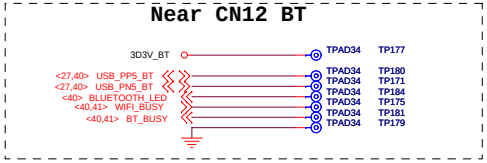

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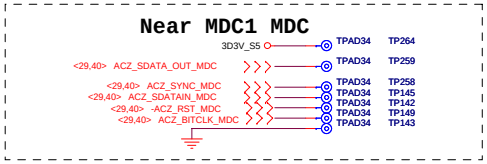

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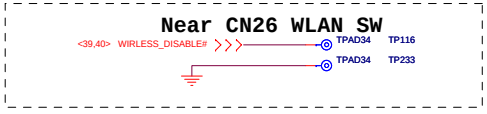

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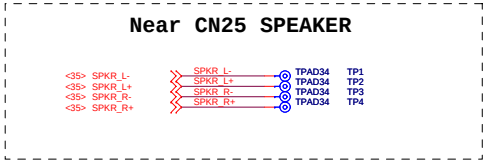

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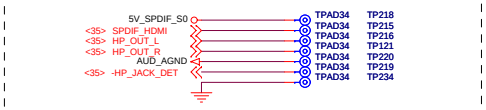

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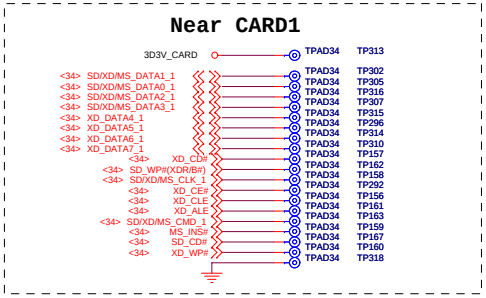

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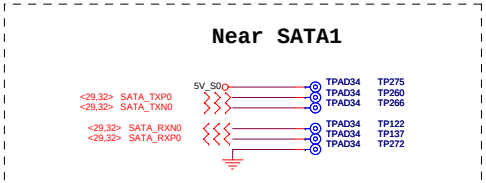

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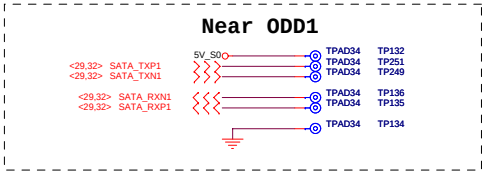

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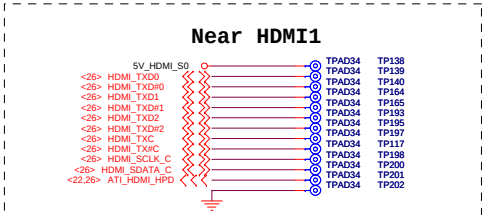

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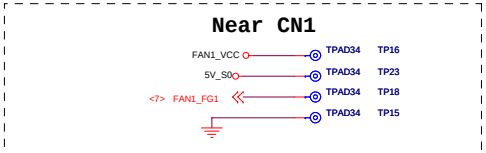

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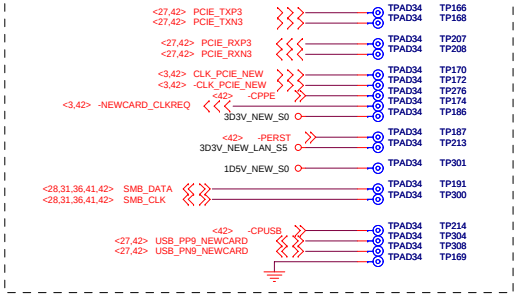

BOM1

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