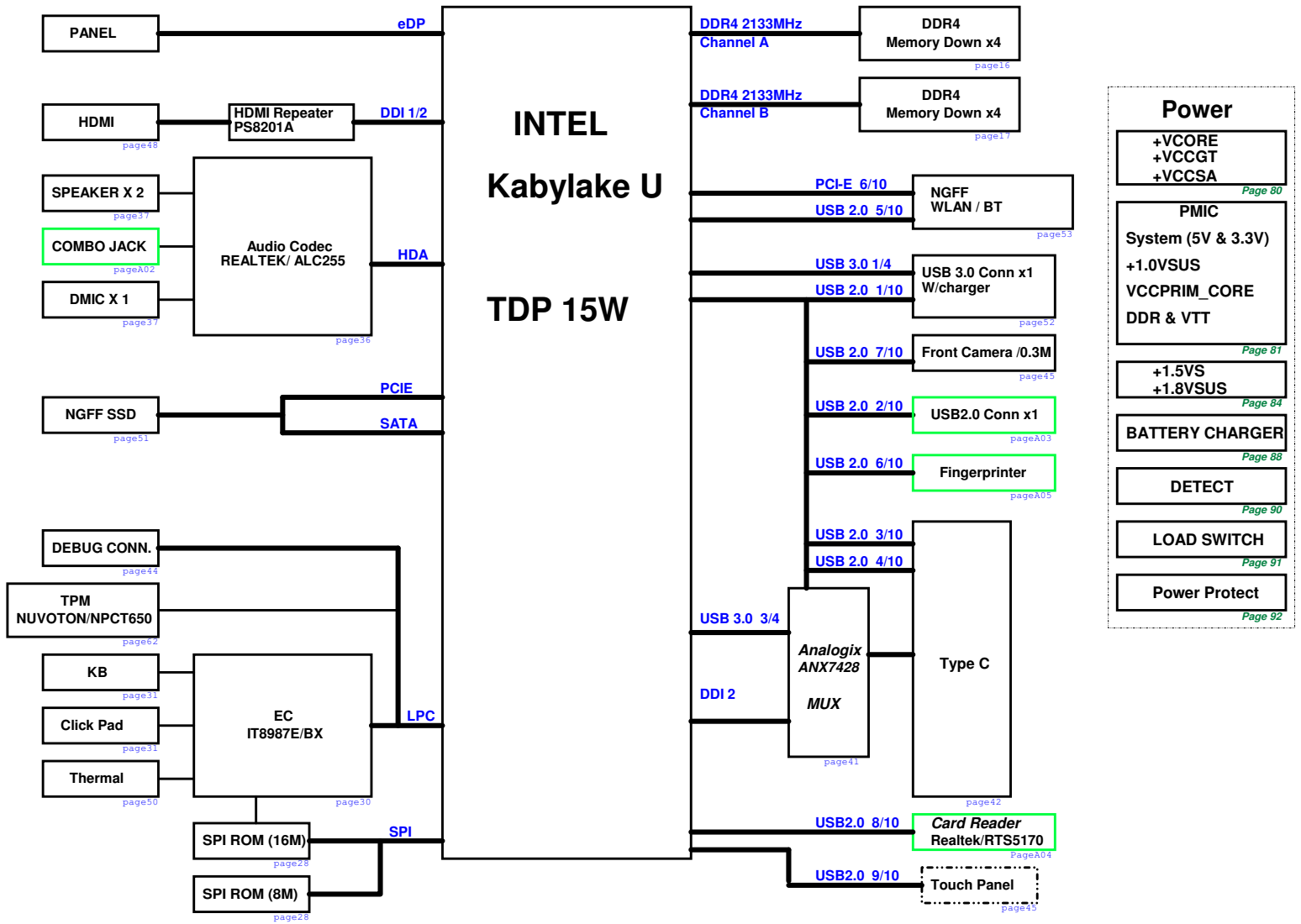
SYSTEM PAGE REF.

14" CARDB(X3) & M3RDA(M3) for Kabylake U Platform Block Diagram



Discharge Circuit — Page 57

DC & BATT. Conn. — Page 60

Reset Circuit — Page 32

Skew Holes — Page 65

<Variant Name>

PEGATRON Title : Block Diagram

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Friday, October 21, 2016 Sheet 1 of 97

EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name

PEGATRON Title : GPIO Setting

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
C	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 2 of 97

+VCCIO — +VCCIO 7,9,57,91
+VCCST_CPU — +VCCST_CPU 5,7,9,25,32
+VCCSTG — +VCCSTG 5,7
+3VS — +3VS 4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92

SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

U0301A

DDI Port 1: HDMI
47 DDI1_TXN2 — E55 DDI1_TXN[0]
47 DDI1_TXP2 — F55 DDI1_TXP[0]
47 DDI1_TXN1 — E58 DDI1_TXN[1]
47 DDI1_TXP1 — F58 DDI1_TXP[1]
47 DDI1_TXN0 — G53 DDI1_TXN[2]
47 DDI1_TXP0 — F56 DDI1_TXP[2]
47 DDI1_CLKN — G56 DDI1_TXN[3]
47 DDI1_CLKP — DDI1_TXP[3]

DDI Port 2: TYPE-C DP
41 DDI2_TXN0 — C50 DDI2_TXN[0]
41 DDI2_TXP0 — D50 DDI2_TXP[0]
41 DDI2_TXN1 — C52 DDI2_TXN[1]
41 DDI2_TXP1 — D52 DDI2_TXP[1]
41 DDI2_TXN2 — A50 DDI2_TXN[2]
41 DDI2_TXP2 — B50 DDI2_TXP[2]
41 DDI2_TXN3 — D51 DDI2_TXN[3]
41 DDI2_TXP3 — C51 DDI2_TXP[3]

DDI — DISPLAY SIDEBANDS — EDP

47 DDPB_CTRLCLK — L13 GPP_E18/DDPB_CTRLCLK
47 DDPB_CTRLDATA — L12 GPP_E19/DDPB_CTRLDATA
DDPC_CTRLCLK — N7 GPP_E20/DDPC_CTRLCLK
DDPC_CTRLDATA — N8 GPP_E21/DDPC_CTRLDATA
N11 GPP_E22
N12 GPP_E23

+VCCIO — R0301 2 1% 1 24.9Ohm DP_COMP — E52 eDP_RCOMP

940432
01V010000015

EDP_TXN[0] C47 — EDP_TXN0 45
EDP_TXP[0] C46 — EDP_TXP0 45
EDP_TXN[1] D46 — EDP_TXN1 45
EDP_TXP[1] C45 — EDP_TXP1 45
EDP_TXN[2] A45 — EDP_TXN2 45
EDP_TXP[2] B45 — EDP_TXP2 45
EDP_TXN[3] A47 — EDP_TXN3 45
EDP_TXP[3] B47 — EDP_TXP3 45

eDP x 4
-- WQHD 4 Lane
-- FHD 2 Lane

E45 EDP_AUXN — EDP_AUXN 45
F45 EDP_AUXP — EDP_AUXP 45

B52 EDP_DISP_UTIL

G50 DDI1_AUXN
F50 DDI1_AUXP
E48 DDI2_AUXN — DDI2_AUXN 41
F48 DDI2_AUXP — DDI2_AUXP 41
G46 RSVD_1
F46 RSVD_2

L9 GPP_E13/DDPB_HPD0 — DDI1_HPD 47
L7 GPP_E14/DDPC_HPD1 — DDI2_HPD 41
L6 EXT_SMI# R R0302 1 — 2 0Ohm EXT_SMI# — EXT_SMI# 30,44
N9 EXT_SCI# R R0303 1 — 2 0Ohm EXT_SCI# — EXT_SCI# 30
L10 eDP_HPD — eDP_HPD 45

Pull down at connector side

R12 eDP_BKLTEN — LCD_BKLTEN_PCH 21,45
R11 eDP_BKLTCTL — LCD_BL_PWM_PCH 45
U13 eDP_VDDEN — EDP_VDD_EN 45

DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
1 : port is detected

+3VS
DDPB_CTRLDATA R0304 1 — 2 2.2KOhm
DDPB_CTRLCLK R0338 1 — 2 2.2KOhm

+3VS
EXT_SCI# R0307 1 — 2 10KOhm
EXT_SMI# R0308 1 — 2 10KOhm

DDPC_HPD
DP: 100Kohm pull down on PCH Side
HDMI: 20Kohm pull down
DDI2_HPD R0337 1 — 2 100KOhm

+3VS
DDPC_CTRLDATA R0342 1 — 2 2.2KOhm
DDPC_CTRLCLK R0343 1 — 2 2.2KOhm

R1.0_10L ---Enable DP port

+VCCST_CPU — R0311 1KOhm
+VCCSTG — R0312 1KOhm 5%
141024 follow PDG V1.0 Table 10-4
Rpu = 1K ohm 5%
Rs = 500 ohm 5%
Closeer EC
+VCCST_CPU — R0313 49.9Ohm 1% @

U0301D

32 H_THRMTRIP# — H_PROCHOT# — R0314 1 30 2 499Ohm — H_PECI_EC
R0315 1 5% 2 43Ohm — H_PECI
SP0301 1 2 — PROCHOT#_R
T0306 1 — H_THRMTRIP#_R
SKTOCC# — TP_CATERR#_R

D63 CATERR#
A54 PECI
C65 PROCHOT#
C63 THERMTRIP#
A65 SKTOCC#

CPU MISC
C55 BPM#[0]
D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

A6 GPP_E3/CPU_GP0
A7 GPP_E7/CPU_GP1
BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3

R0316 1 1% 2 49.9Ohm — CPU_POPIRCOMP — AT16 PROC_POPIRCOMP
R0317 1 1% 2 49.9Ohm — PCH_POPIRCOMP — AU16 PCH_OPIRCOMP
R0318 1 1% 2 49.9Ohm — EDRAM_OPIO_RCOMP — H66 OPCE_RCOMP
R0319 1 1% 2 49.9Ohm — EOPIO_RCOMP — H65 OPC_RCOMP

940432
01V010000015

JTAG
PROC_TCK — B61 XDP_TCLK
PROC_TDI — D60 XDP_TDI_CPU
PROC_TDO — A61 XDP_TDO_CPU
PROC_TMS — C60 XDP_TMS_CPU
PROC_TRST# — B59 XDP_TRST_CPU_N

PCH_JTAG_TCK — B56 PCH_JTAG_TCLK — 1 T0315
PCH_JTAG_TDI — D59 PCH_JTAG_TDI
PCH_JTAG_TDO — A56 PCH_JTAG_TDO
PCH_JTAG_TMS — C59 PCH_JTAG_TMS
PCH_TRST# — C61 PCH_TRST_CPU_N
JTAGX — A59 XDP_TCLK_JTAGX

+VCCSTG
PCH_JTAG_TDO — XDP_TDO_CPU — R0323 2 1 51Ohm
PCH_JTAG_TMS — XDP_TMS_CPU — T0316
PCH_TRST_CPU_N — XDP_TRST_CPU_N — T0317
PCH_JTAG_TDI — XDP_TDI_CPU — T0318
XDP_TCLK_JTAGX — XDP_TCLK — R0324 2 1 51Ohm

Modify to XDP less

30 THRO_CPU — Q0301 2N7002 — R0341 0Ohm — H_PROCHOT#

R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result), 預留0ohm是調整空間

88 PROCHOT# — SP0325 0Ohm
80 VR_HOT# — R0320 0Ohm

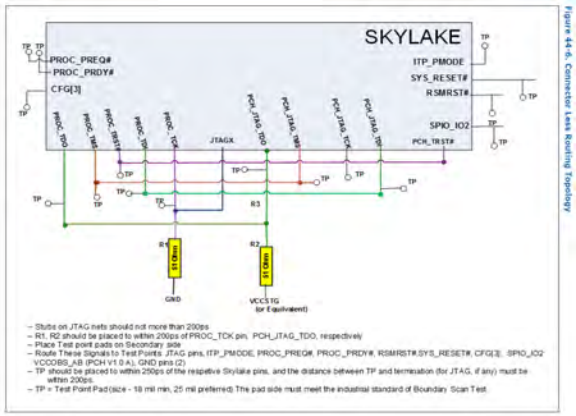


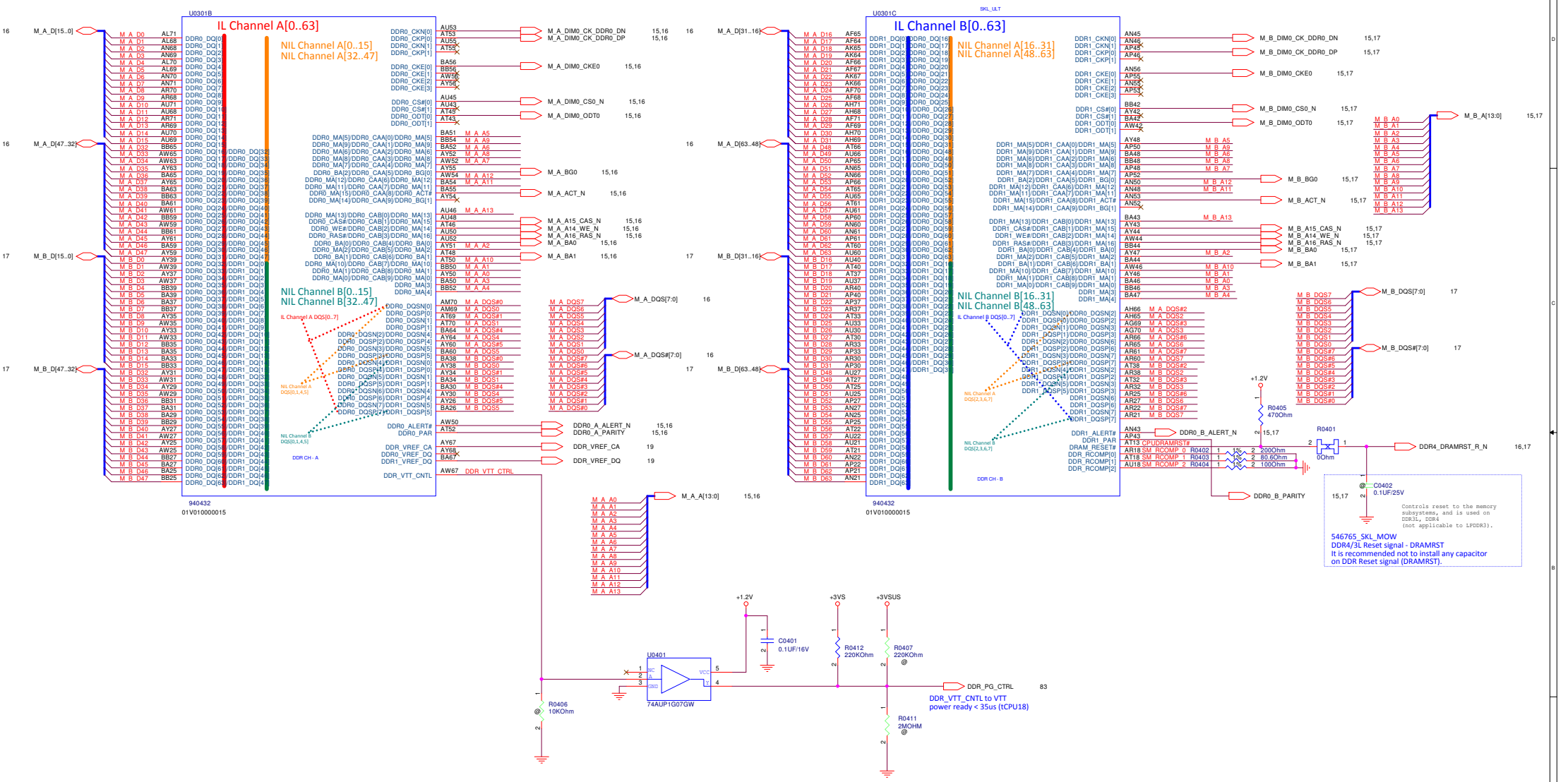
Figure 44-6. Connector Less Routing Topology

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CPU(1)_DDI/eDP
Engineer: Andy Kao
BG1/HW3

Size	Project Name	Rev
C	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 3 of 97



Symbol U0301 B

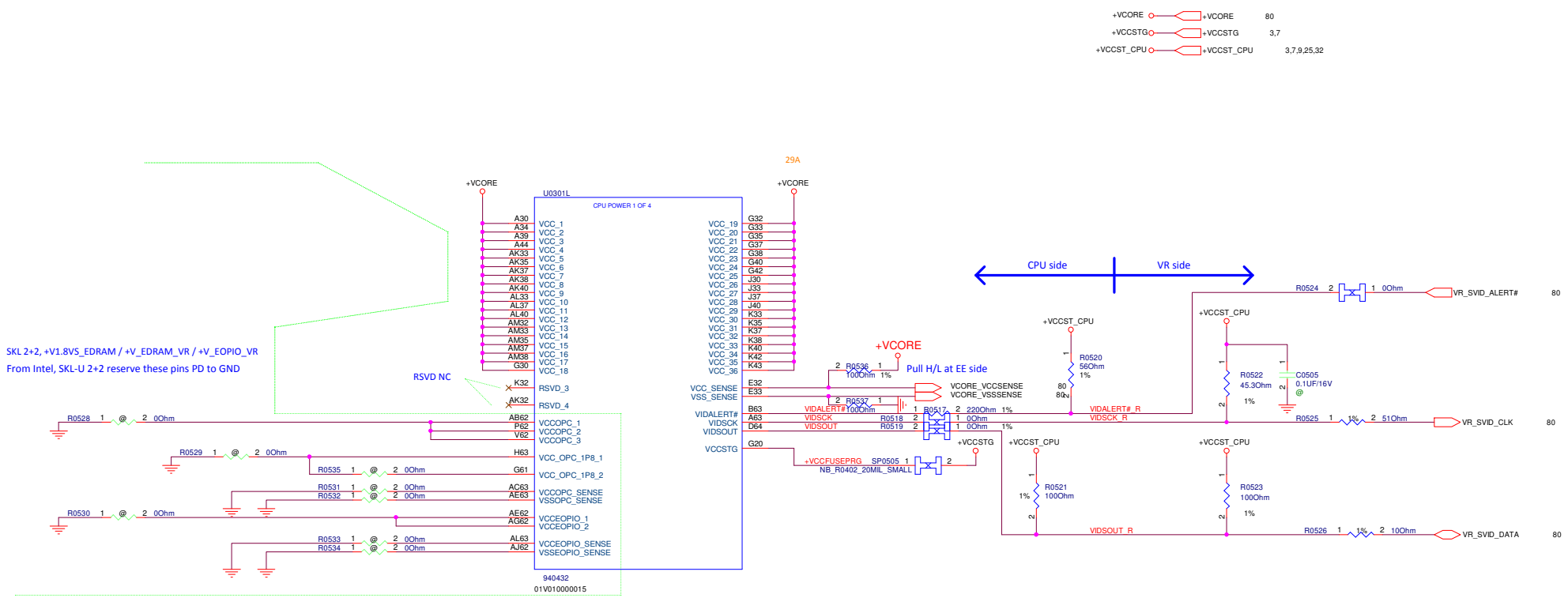
	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1		ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 2		ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 3		ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 4		
BYTE 5		
BYTE 6		
BYTE 7		

Symbol U0301 C

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 2		ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 3		ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 4		
BYTE 5		
BYTE 6		
BYTE 7		

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CPU(2)_DDR4
BG1/HW3
Engineer: Andy Kao
Size: Custom | Project Name: X3 | Rev: 1.0
Date: Wednesday, August 31, 2016 | Sheet 4 of 97



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

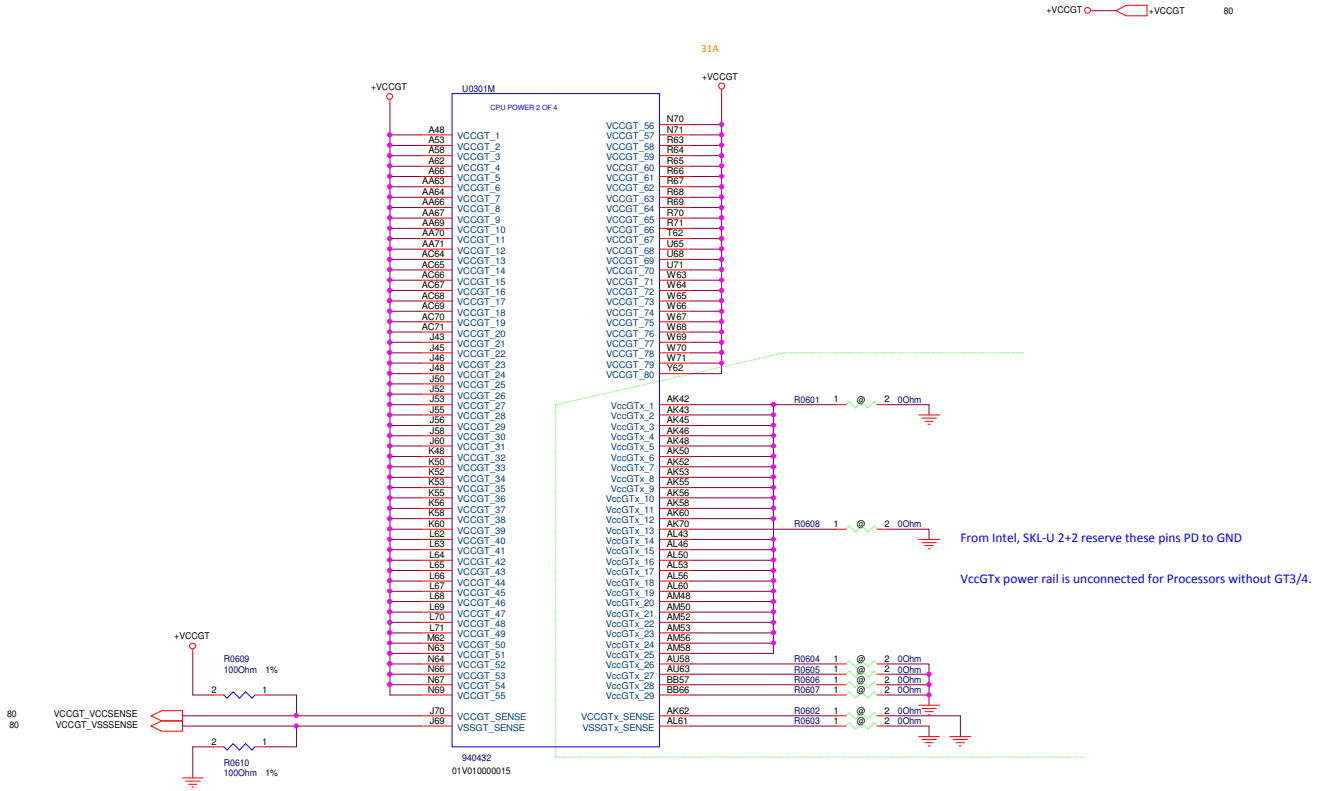
Title :CPU(3)_+VCCCORE

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 5 of 97



PEGATRON	Title : CPU(4)_+VCCGT		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3	Engineer: Andy Kao		
Size: C	Project Name: X3		Rev: 1.0
Date: Wednesday, August 31, 2016	Sheet 6 of 97		

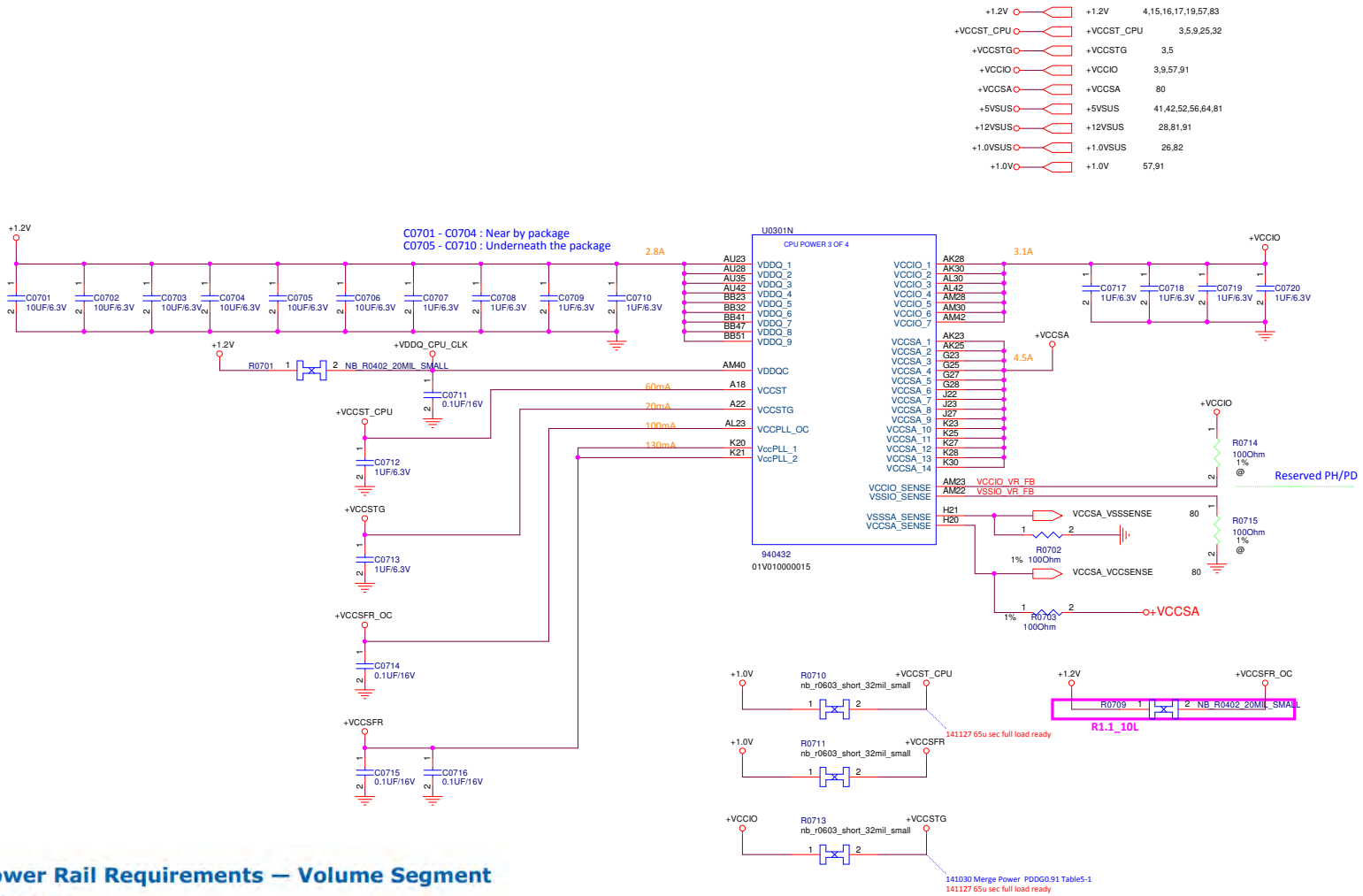


Table 5-1. Power Rail Requirements — Volume Segment — U-Line

Load switch (LS)	LS ENABLE	Load/Rail name	Imax (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc_{ST}	0.04
		Vcc_{PLL}(Vcc_{SFR})	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VccIO	3.0
		Vcc_{STG}	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu_04

PEGATRON
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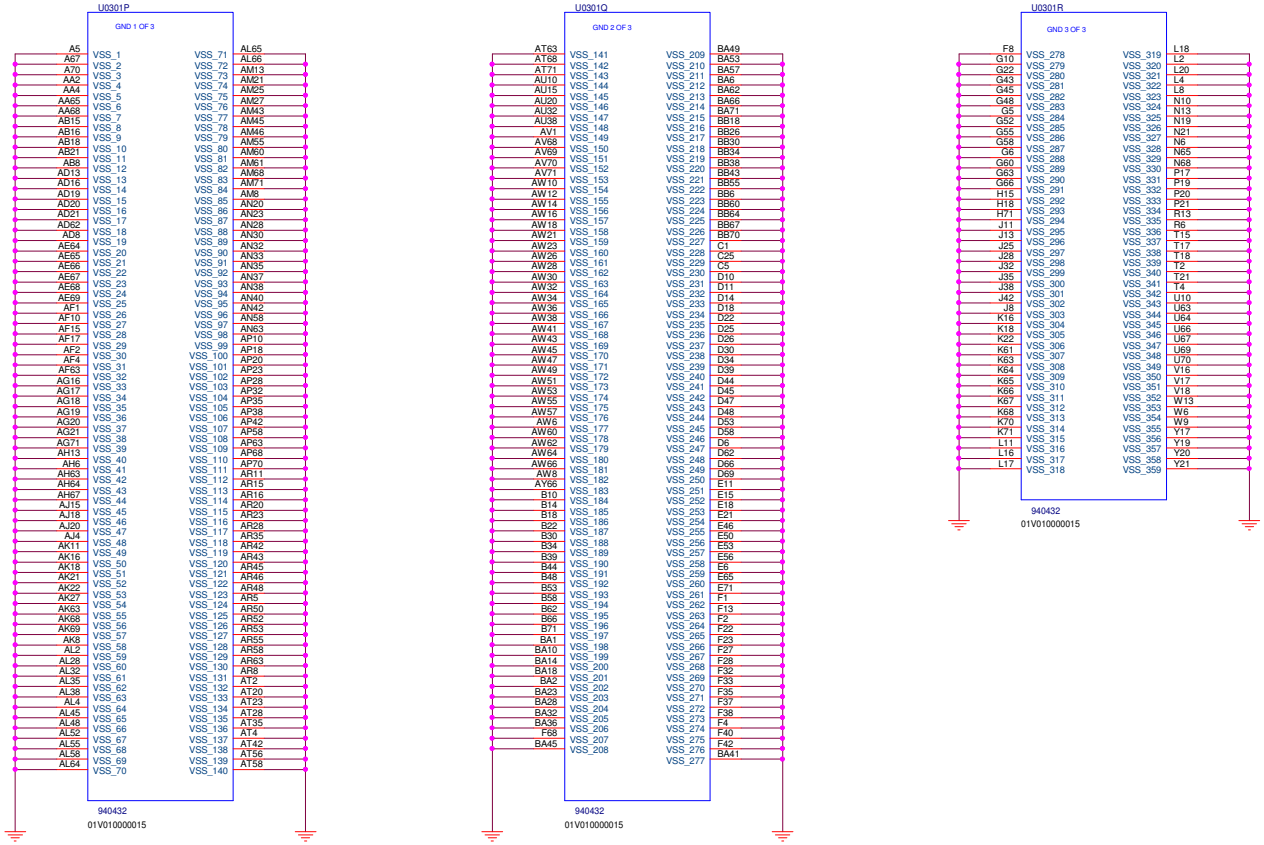
Title: CPU(5)_+VDDQ/IO/SA
BG1/HW3
Engineer: Andy Kao
Size: Custom | Project Name: X3 | Rev: 1.0
Date: Wednesday, August 31, 2016 | Sheet 7 of 97



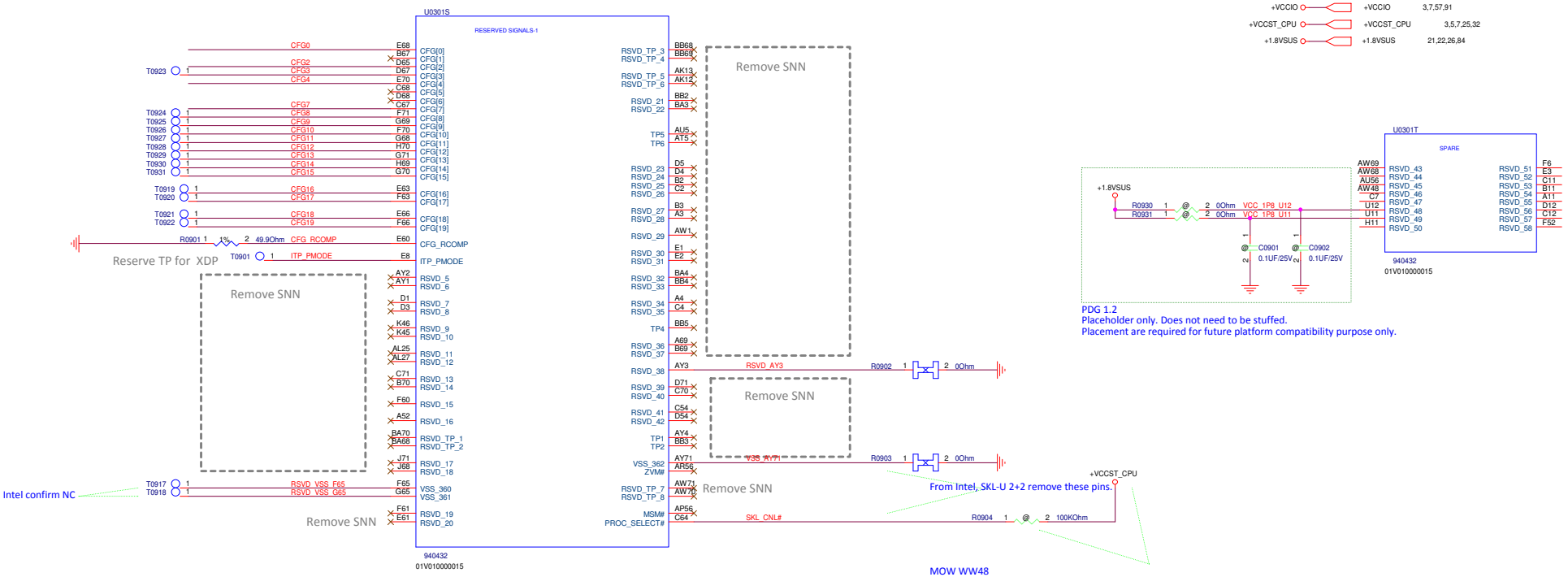
PEGATRON Title : CPU(6)_CPU GND

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

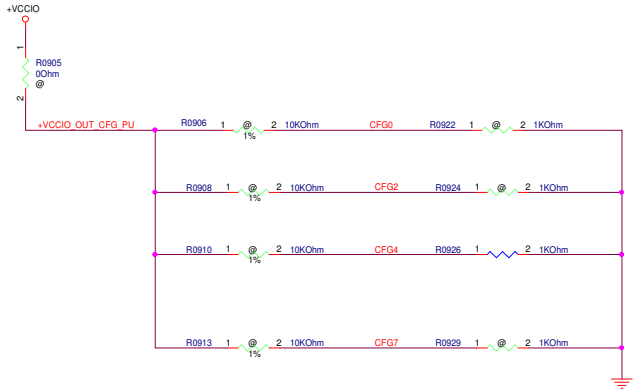
Size	Project Name	Rev
C	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 8 of 97



PDG 1.2
Placeholder only. Does not need to be stuffed.
Placement are required for future platform compatibility purpose only.

MOW WW48
1. Ball C64 which is PROC_SELECT# needs to be pulled to VCCST for Cannonlake support via 100K ohm resistor and with no resistor populated (floating pin) for Skylake.



6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :CPU(7)_CFG/RSVD
Engineer: Andy Kao
BG1/HW3
Size C | Project Name X3 | Rev 1.0
Date: Wednesday, August 31, 2016 | Sheet 9 of 97

PEGATRON

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Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 10 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 11 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 12 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 13 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

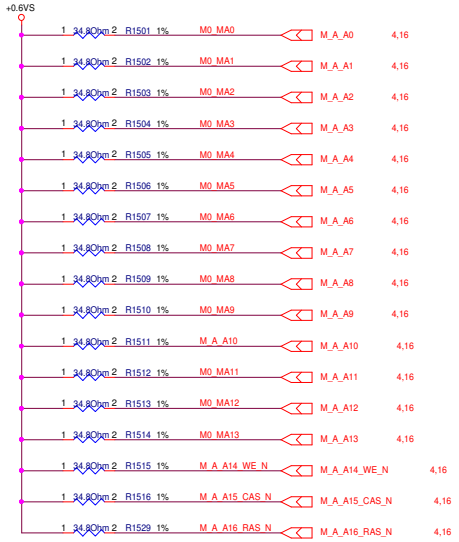
Size	Project Name	Rev
A	X3	1.0

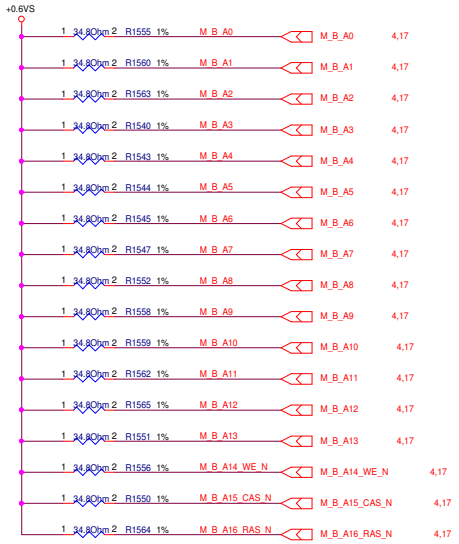
Date: Wednesday, August 31, 2016 Sheet 14 of 97

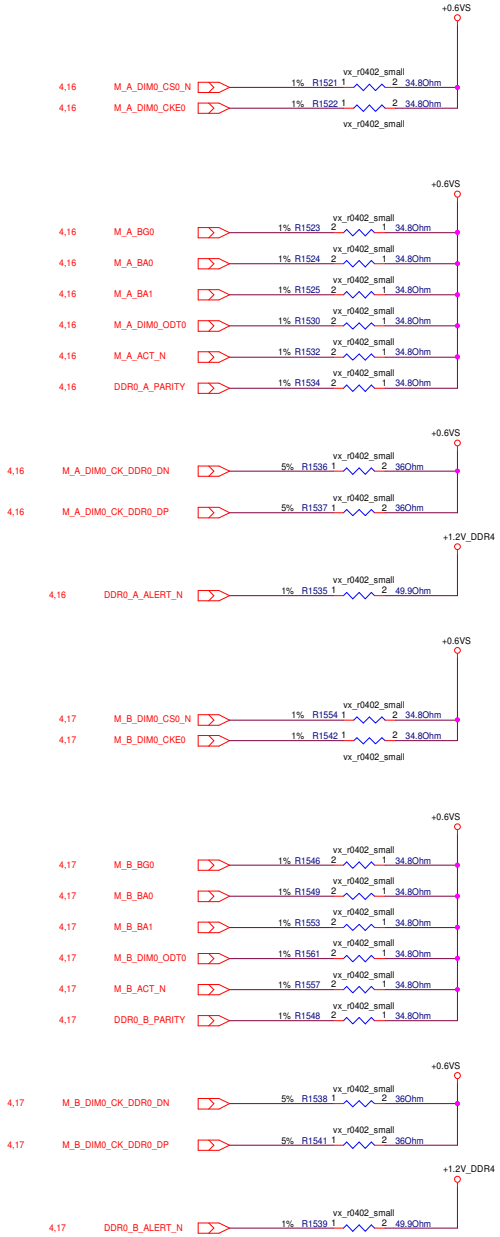
DDR4(0)_Termination

+0.6VS → +0.6VS 57,83

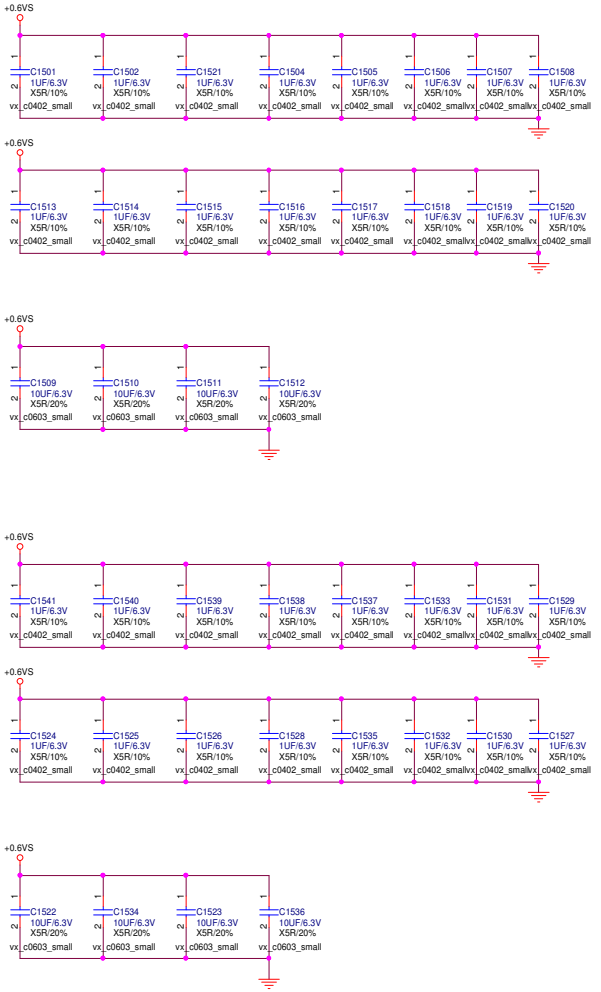
+1.2V_DDR4 → +1.2V_DDR4 4,7,16,17,19,57,83







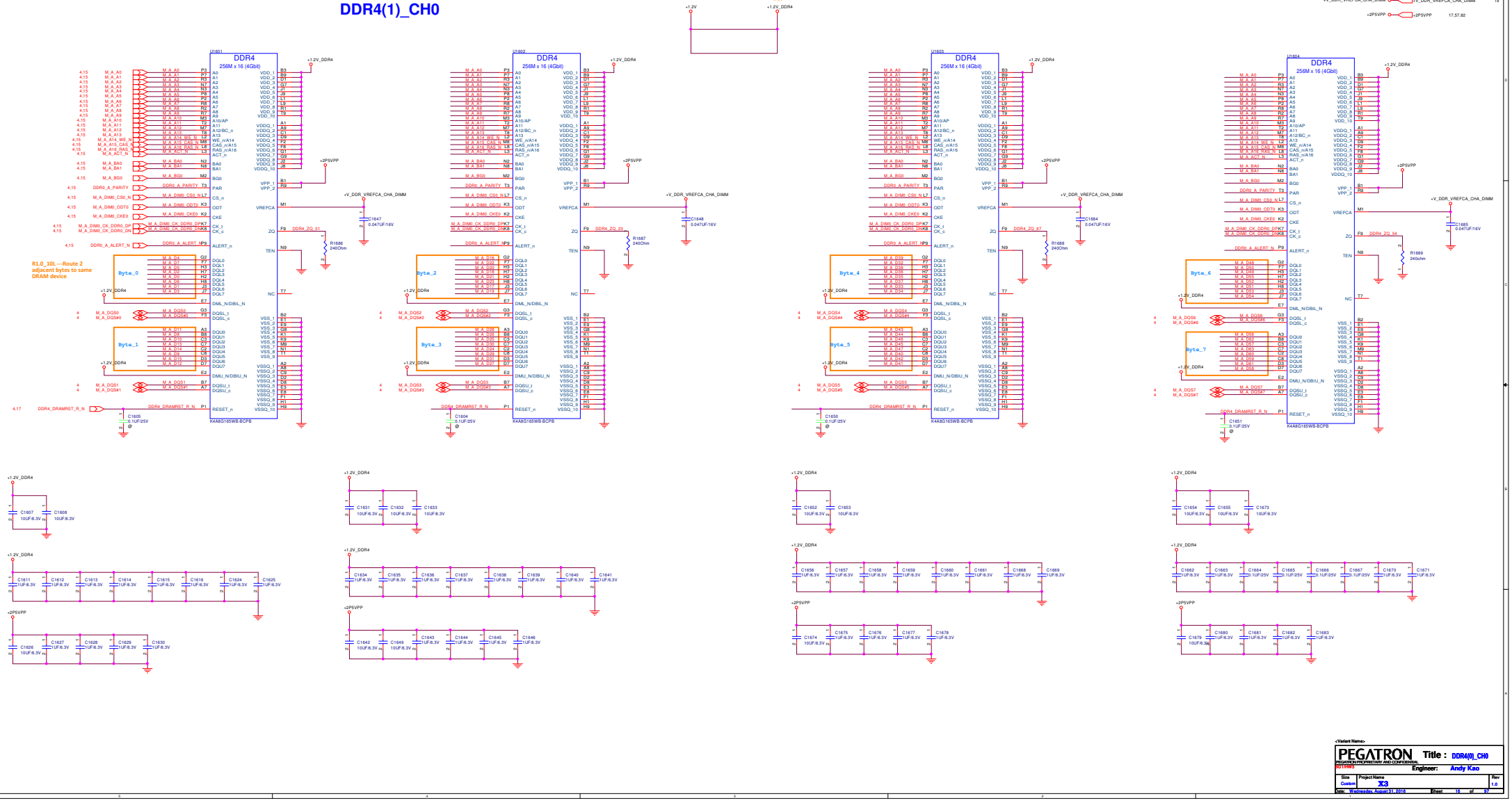
Average placed close to +VDDQ_VTT power plane



PEGATRON Title : DDR4(0)_Termination
PEGATRON PROPRIETARY AND CONFIDENTIAL
3G1/HW3 Engineer: Andy Kao
Size C | Project Name X3 | Rev 1.0
Date: Wednesday, August 31, 2016 Sheet 15 of 97

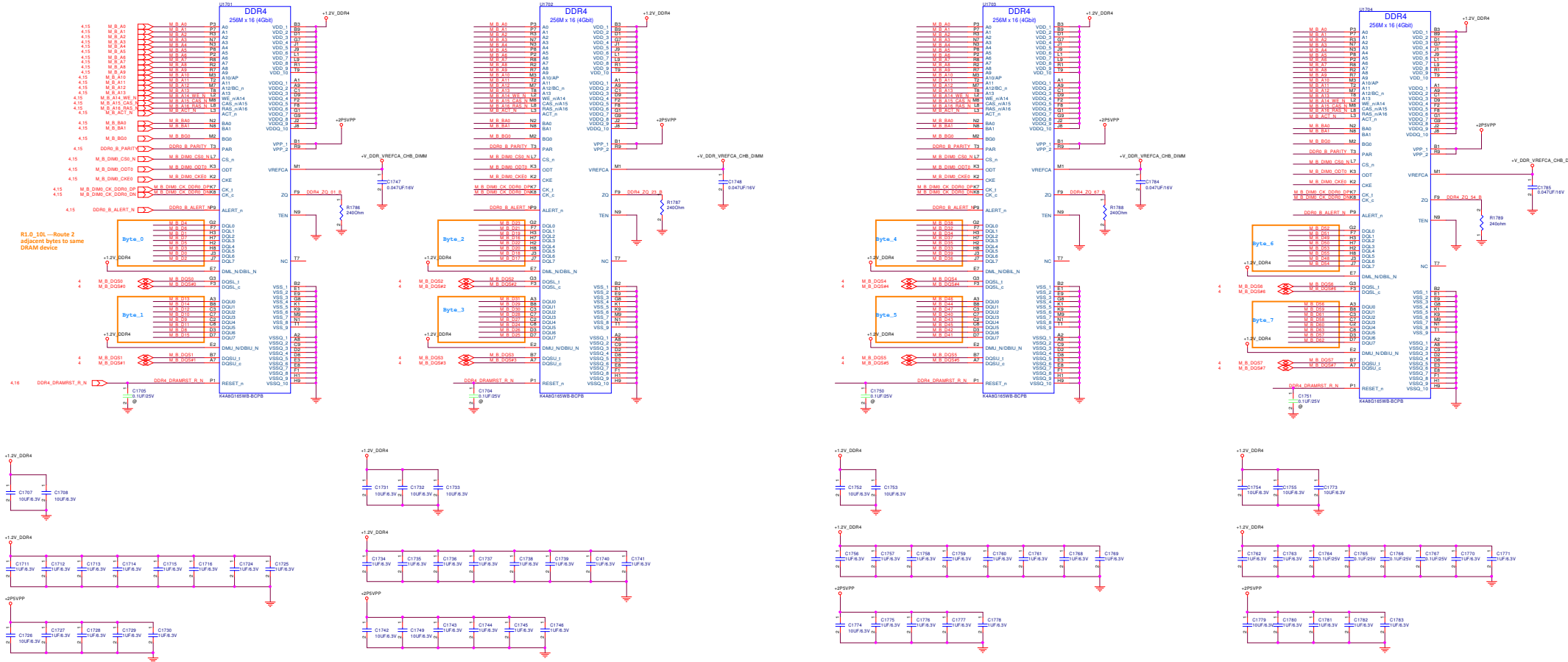
16

DDR4(1)_CH0



<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(0)_CH0
Engineer: Andy Kao
Size: Custom
Project Name: X3
Rev: 1.0
Date: Wednesday, August 31, 2016
Sheet 16 of 97

DDR4(2)_CH1



<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title :DDR4(2)_CH1
Engineer: Andy Kao
Size: Custom | Project Name: X3 | Rev: 1.0
Date: Wednesday, August 31, 2016 | Sheet 17 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

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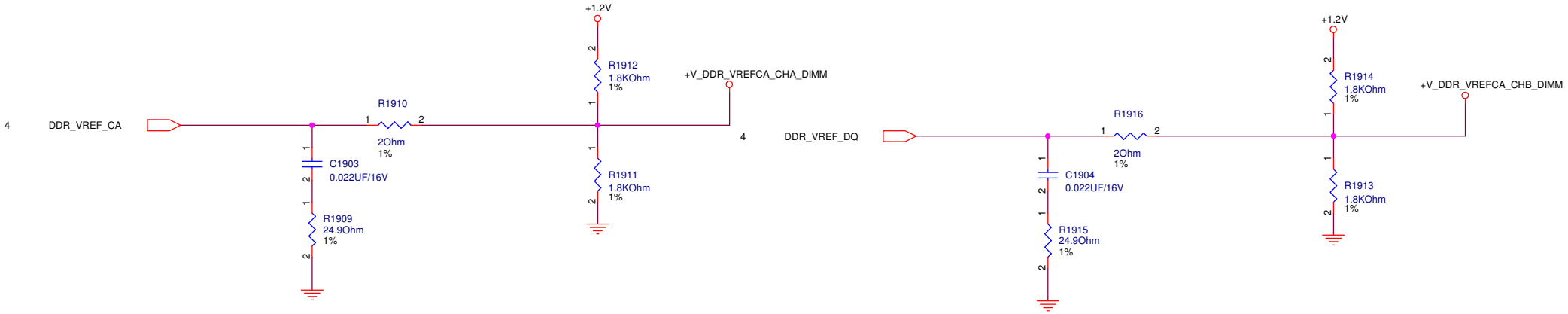
19

DDR4(3)_CA/DQ Voltage

+1.2V — +1.2V — 4,7,15,16,17,57,83
+V_DDR_VREFCA_CHB_DIMM — +V_DDR_VREFCA_CHB_DIMM — 17
+V_DDR_VREFCA_CHA_DIMM — +V_DDR_VREFCA_CHA_DIMM — 16

DDR4 Vref (Intel Schematic Review)



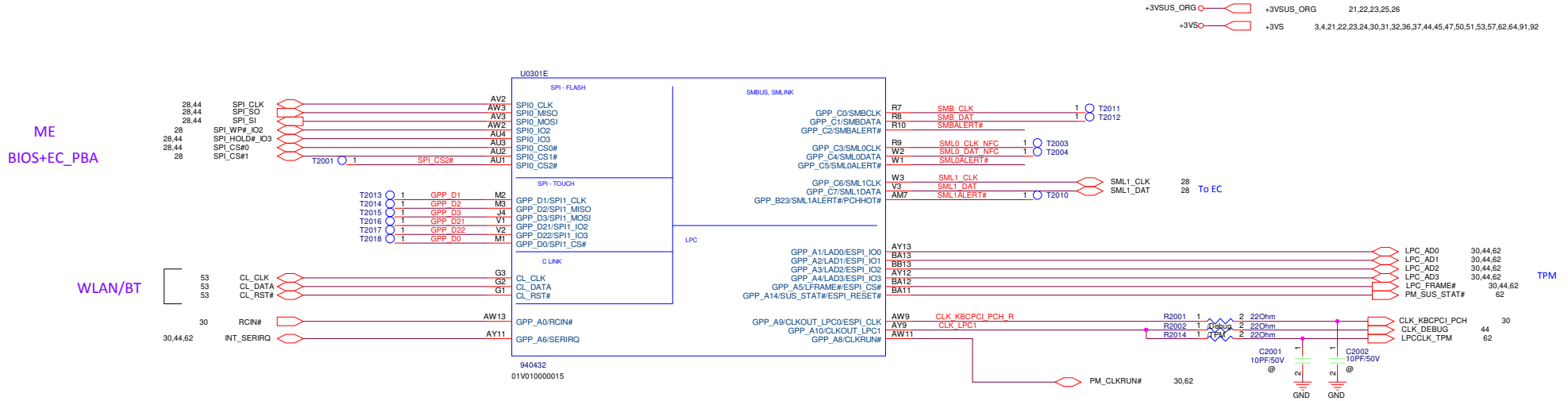
<Variant Name>

PEGATRON Title : DDR3(3)_CA/DQ Voltage

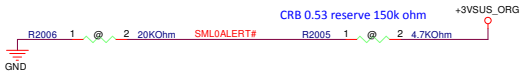
BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

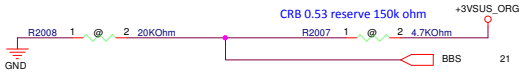
Date: Wednesday, August 31, 2016 Sheet 19 of 97



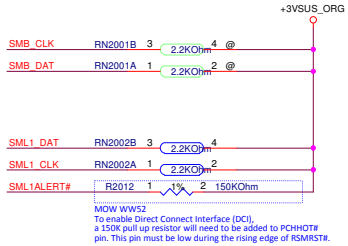
SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable



SML0ALERT# - Internal weak pull down 20 kohm
0 : LPC EC (default)
1 : eSPI EC



BBS - Internal weak pull down 20k ohm
Boot BIOS Strap
0 : SPI destination (default)
1 : LPC destination



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(1)_SPI/LPC

BG1/HW3

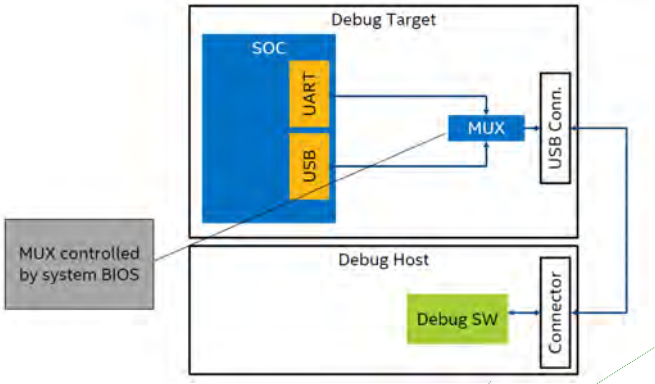
Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

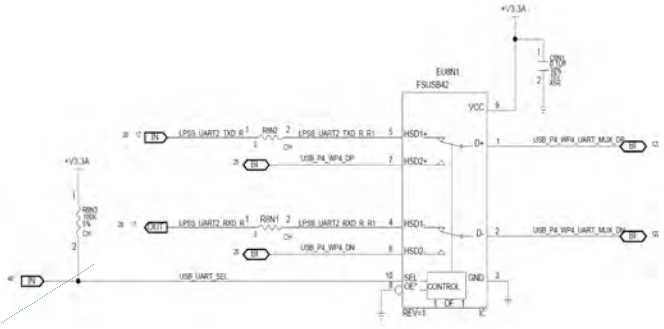
Date: Wednesday, August 31, 2016 Sheet 20 of 97

Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

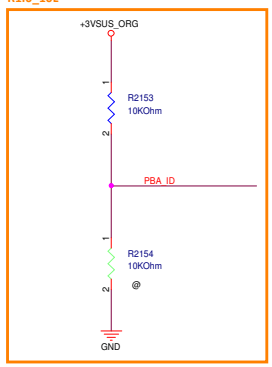
With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required



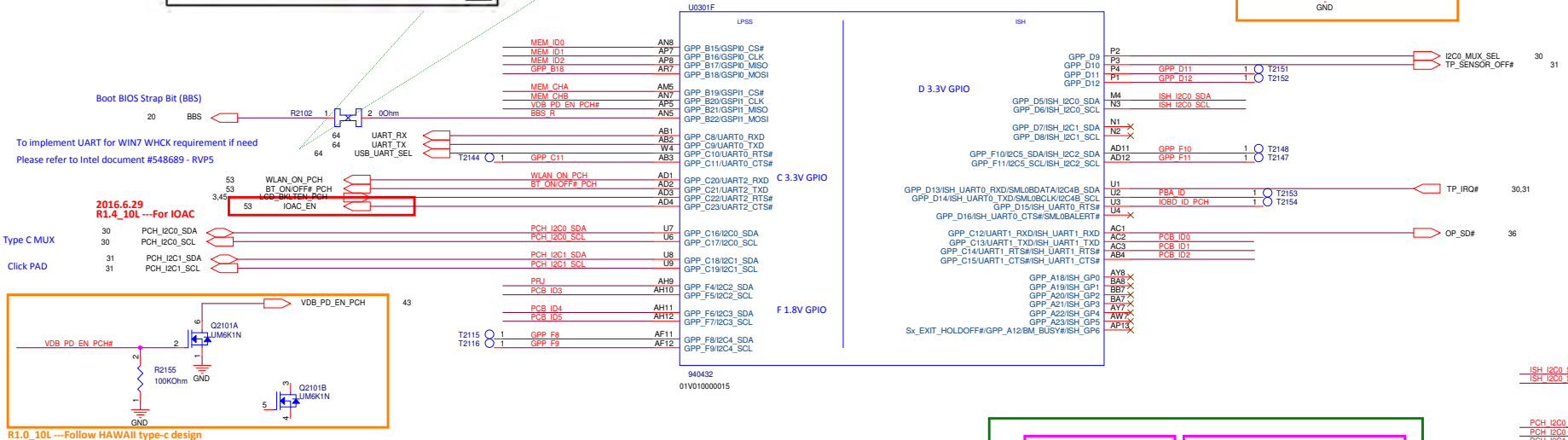
+3VS +3VS 3,4,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92



R1.0_10L



GPP_D14	1	0
PBA_ID	Enable	Disable



Boot BIOS Strap Bit (BBS)

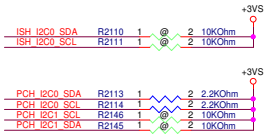
To implement UART for WIN7 WHCK requirement if need
Please refer to Intel document #548689 - RVP5

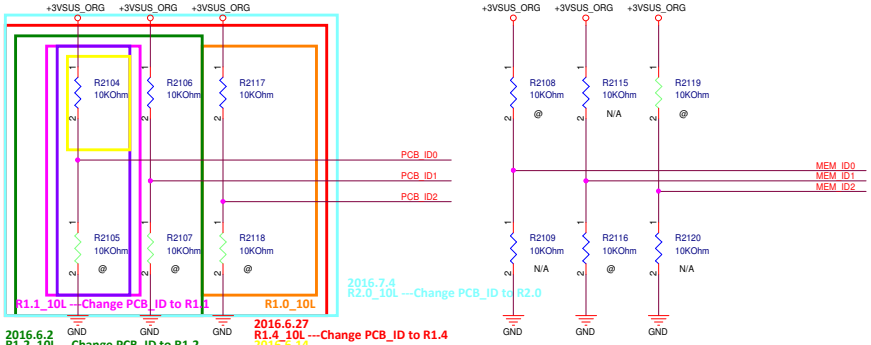
2016.6.29
R1.4_10L ---For IOAC

Type C MUX

Click PAD

R1.0_10L ---Follow HAWAII type-c design

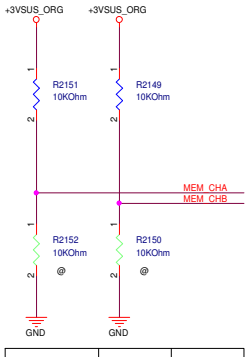


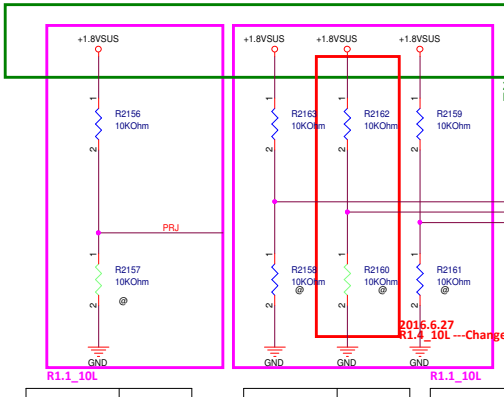


2016.6.2
R1.2_10L ---Change PCB_ID to R1.2
2016.6.14
R1.3_10L ---Change PCB_ID to R1.3

2016.6.27
R1.4_10L ---Change PCB_ID to R1.4
2016.6.14
R2.2_10L ---Change PCB_ID to R2.2

2016.7.4
R2.0_10L ---Change PCB_ID to R2.0





2016.6.2
R1.2_10L ---GPP_F is used by 1.8V

2016.6.27
R1.4_10L ---Change PCB_ID to R1.4

GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

Default is GPO, to reserve pull high to +3VSUS_ORG

	CHA	CHB
GPP_B19(0)	Disable	
GPP_B19(1)	Enable	
GPP_B20(0)		Disable
GPP_B20(1)		Enable

	PRJ
GPP_F4(0)	M3
GPP_F4(1)	X3

	PCB_ID3
GPP_F5(0)	SKL
GPP_F5(1)	KBL

	PCB_ID5
GPP_F7(0)	2133
GPP_F7(1)	2400

MB Version ID

	PCB_ID4 (GPP_F6)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R1.0	0	0	0
R1.1	0	0	1
R1.2	0	1	0
R1.3	0	1	1
R1.4	1	0	0
R2.0	1	0	1
R2.1	1	1	0
R2.2	1	1	1

	PCB_ID2 (GPP_C15)
8L	0
10L	1

Memory ID

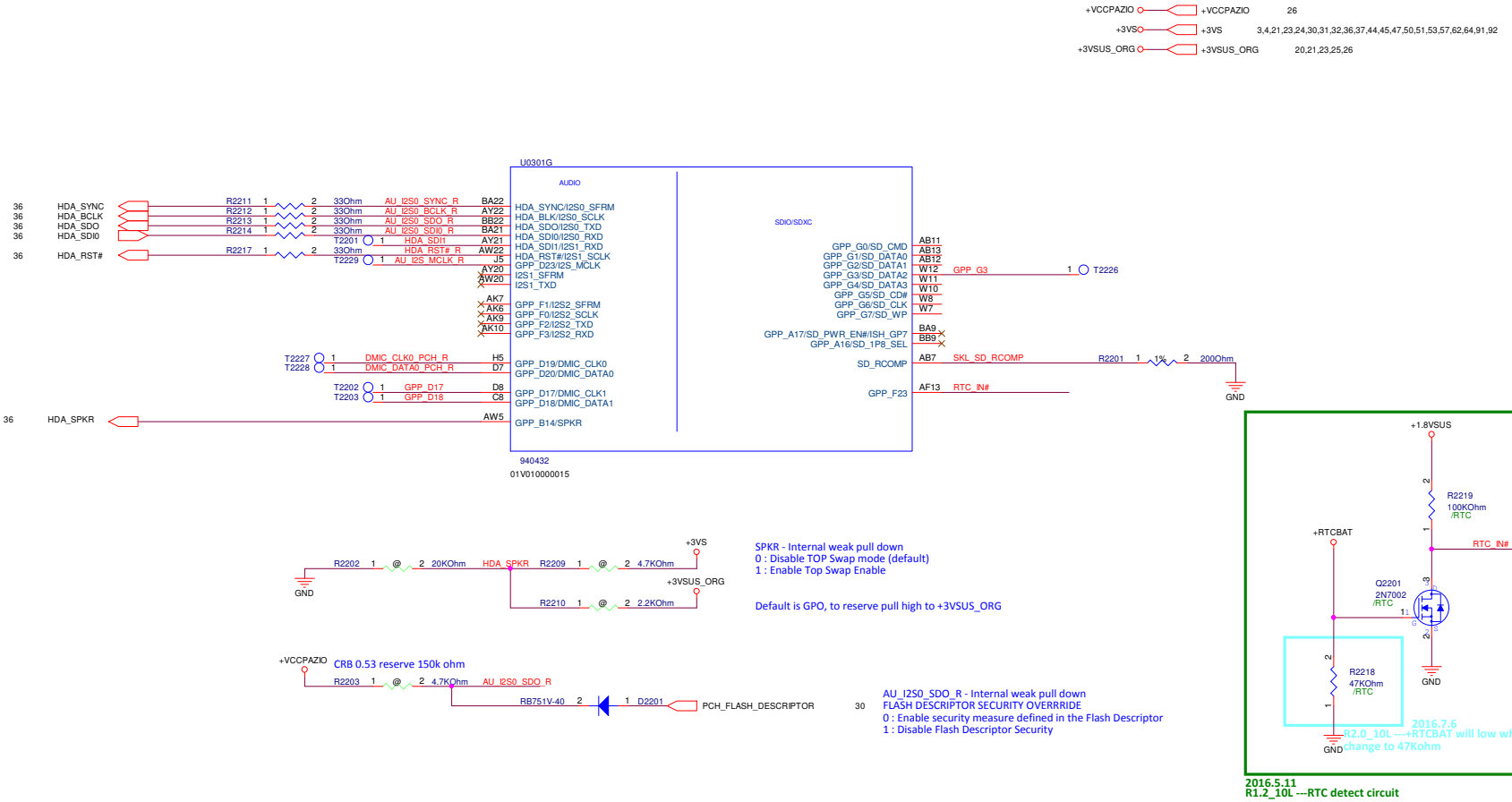
	MEM_ID1 (GPP_B16)
4Gb	0
8Gb	1

	MEM_ID2 (GPP_B17)	MEM_ID0 (GPP_B15)
SAMSUNG	0	0
HYNIX	0	1
MICRON	1	0
RSV	1	1

PEGATRON Title : PCH(2)_ISH
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Friday, September 02, 2016 Sheet 21 of 97



SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG

AU_I2S0_SDO_R - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRRIDE
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security

2016.5.11
R1.2_10L ---RTC detect circuit

<Variant Name>

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Title : PCH(3)_HDA/SDIO

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 22 of 97

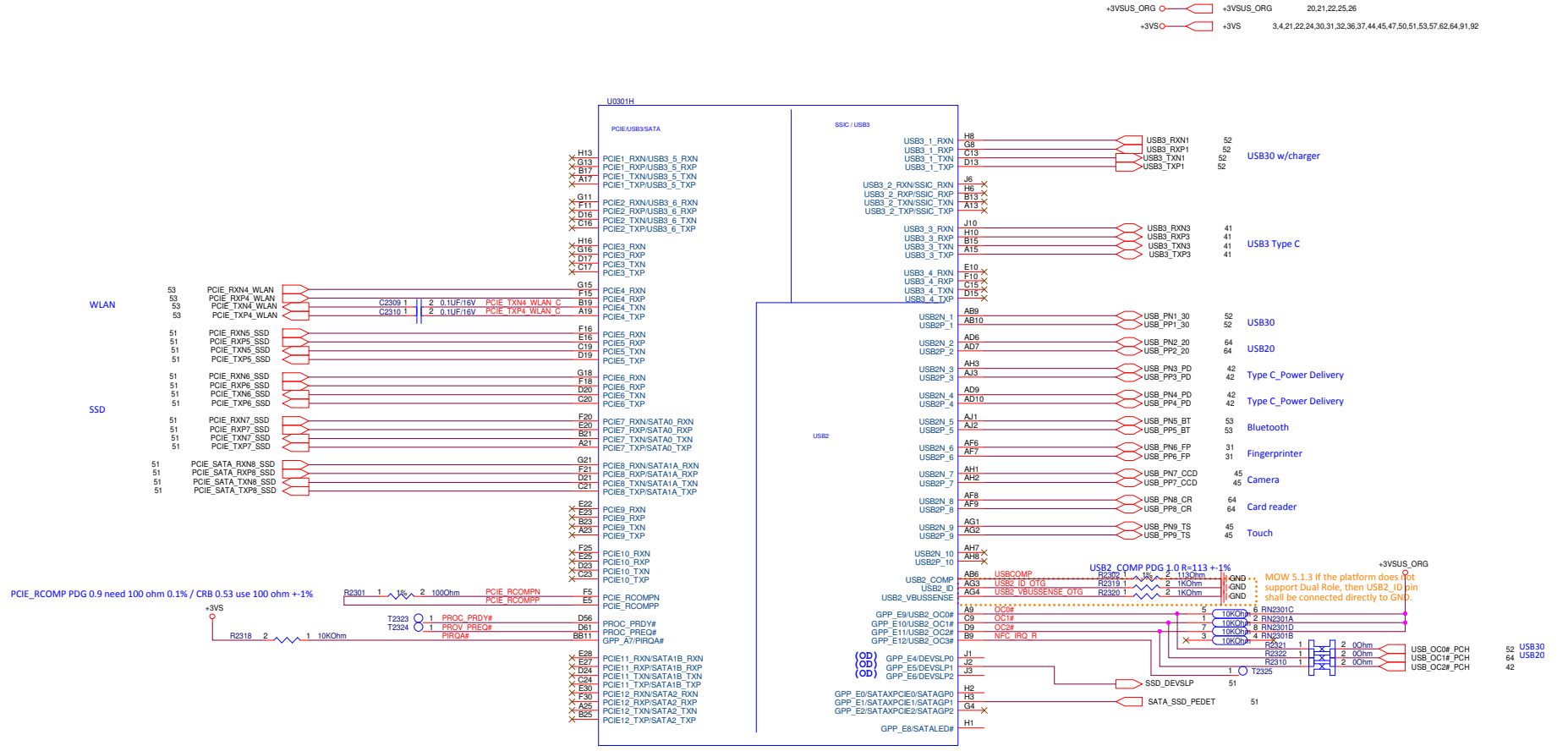


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1–8
2. USB 2.0 port numbers: 1–10
3. USB 2.0 port numbers: 1–6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U

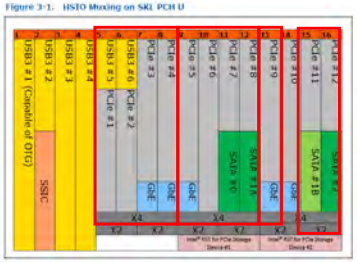
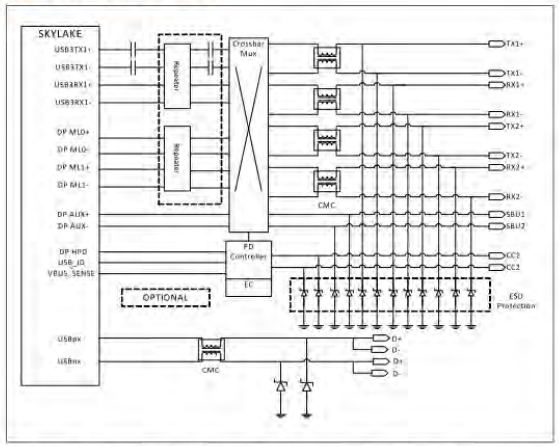


Figure 16-18.USB 3.0 Dual Role and DP x 2



Note: The figure above is a high level example implementation block; actual implementation on schematic may vary.

<Variant Name>

PEGATRON
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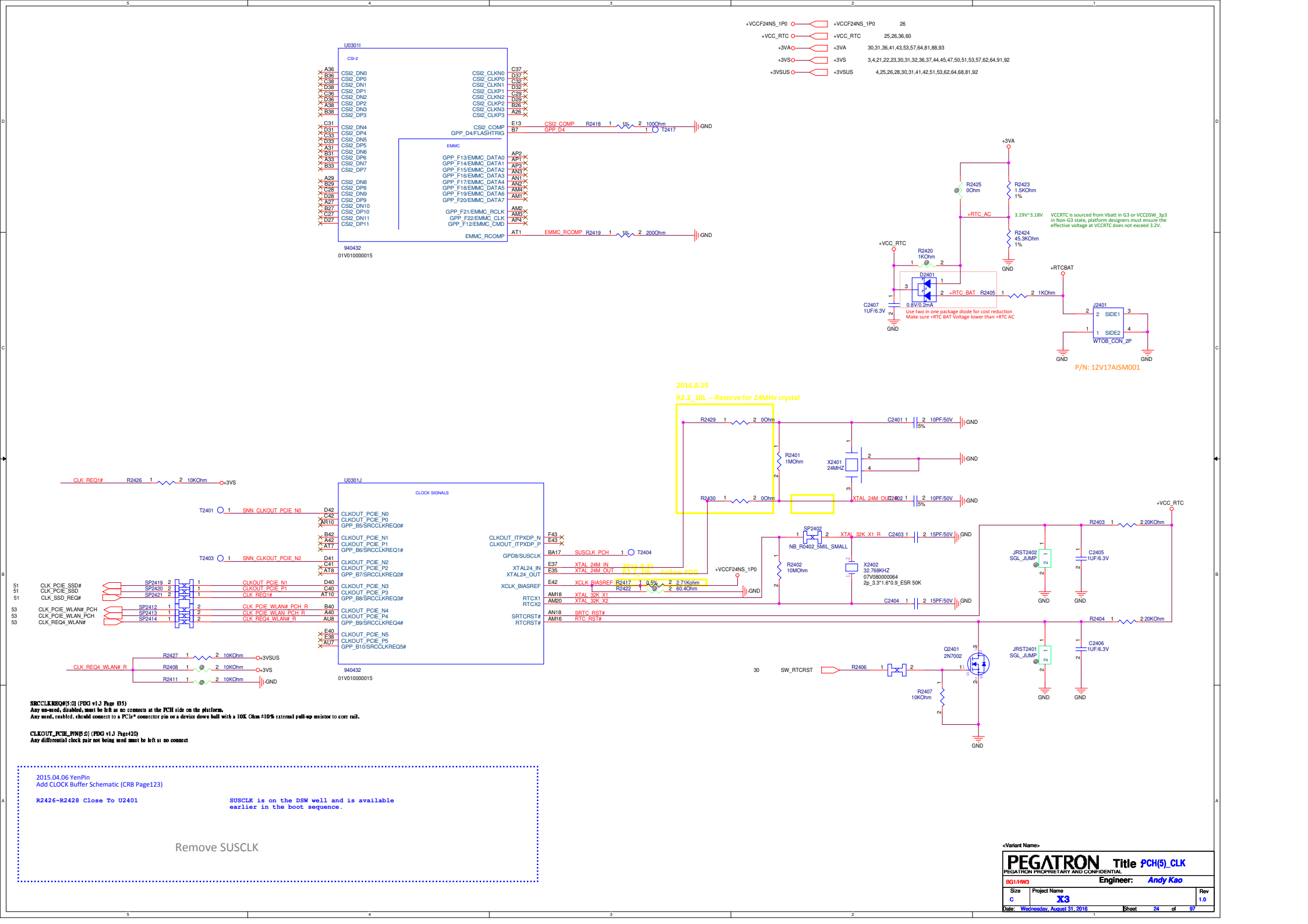
BG1/HW3

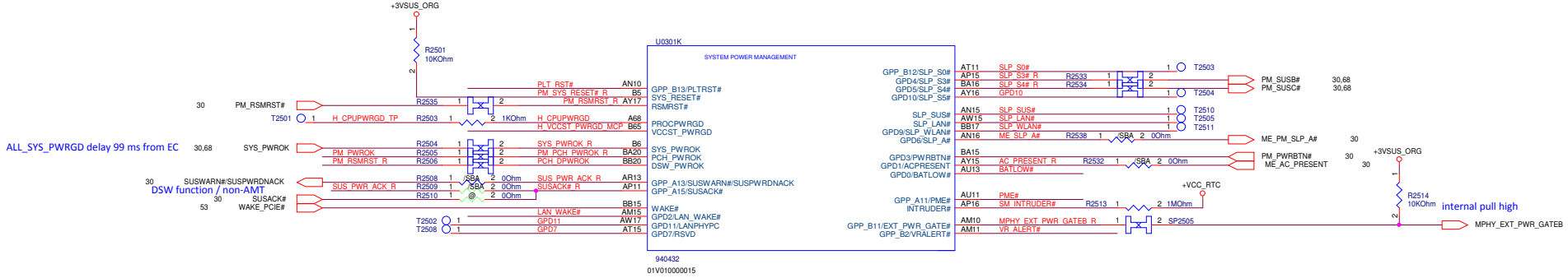
Title: PCH(4)_USB/PCIE/SATA
Engineer: Andy Kao

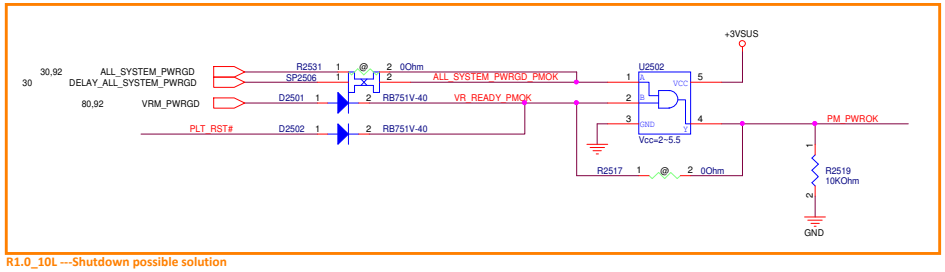
Size	Project Name	Rev
C	X3	1.0

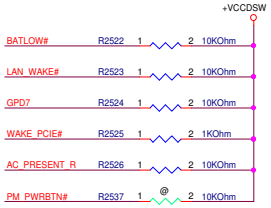
Date: Wednesday, August 31, 2016 Sheet 23 of 97

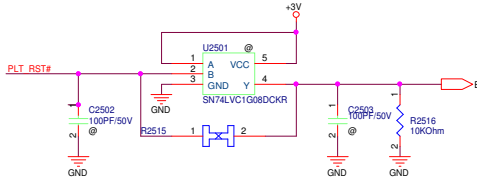

+VCCF24NS_1P0 +VCCF24NS_1P0 26
+VCC_RTC +VCC_RTC 25,26,36,60
+3VA +3VA 30,31,36,41,43,53,57,64,81,88,93
+3VS +3VS 3,4,21,22,23,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+3VSUS +3VSUS 4,25,26,28,30,31,41,42,51,53,62,64,68,81,92
U0301I
CSI-2
EMMC
940432
01V010000015
R2418 100Ohm
R2419 200Ohm
T2417
+3VA
R2425 0Ohm
R2423 1.5KOhm 1%
R2424 45.3KOhm 1%
+RTC_AC
3.19V~3.18V
VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V.
+VCC_RTC
R2420 1KOhm
D2401
0.8V/0.2mA
Use two in one package diode for cost reduction
Make sure +RTC BAT Voltage lower than +RTC AC
C2407 1UF/6.3V
+RTC_BAT
R2405 1KOhm
+RTCBAT
J2401
WTOB_CON_2P
P/N: 12V17AISM001
2016.8.29
R2.2_10L ---Reserve for 24MHz crystal
R2429 0Ohm
R2430 0Ohm
R2401 1MOhm
X2401 24MHZ
C2401 10PF/50V
XTAL_24M_OUT
C2402 10PF/50V
2016.8.31
R2.2_10L ---Follow PDG
SP2402
NB_R0402_5MIL_SMALL
XTAL_32K_X1_R
C2403 15PF/50V
R2402 10MOhm
X2402
32.768KHZ
07V080000064
2p_3.3*1.6*0.9_ESR 50K
C2404 15PF/50V
R2403 220KOhm
R2404 220KOhm
C2405 1UF/6.3V
C2406 1UF/6.3V
JRST2402
JRST2401
SGL_JUMP
Q2401
2N7002
R2407 10KOhm
R2406
SW_RTCRST
CLK_REQ1#
R2426 10KOhm
+3VS
U0301J
CLOCK SIGNALS
T2401 SNN_CLKOUT_PCIE_N0
T2403 SNN_CLKOUT_PCIE_N2
CLK_PCIE_SSD#
CLK_PCIE_SSD
CLK_SSD_REQ#
CLK_PCIE_WLAN#_PCH
CLK_PCIE_WLAN_PCH
CLK_REQ4_WLAN#
SP2419
SP2420
SP2421
SP2412
SP2413
SP2414
CLK_REQ4_WLAN#_R
R2427 10KOhm
R2408 10KOhm
R2411 10KOhm
+3VSUS
SUSCLK_PCH
T2404
+VCCF24NS_1P0
R2417 2.71Kohm
R2422 60.4Ohm
XTAL_24M_IN
XTAL_24M_OUT
XCLK_BIASREF
XTAL_32K_X1
XTAL_32K_X2
SRTC_RST#
RTC_RST#
SRCCLKREQ#[5:0] (PDG v1.3 Page 135)
Any un-used, disabled, must be left as no connects at the PCH side on the platform.
Any used, enabled, should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail.
CLKOUT_PCIE_P/N[5:0] (PDG v1.3 Page420)
Any differential clock pair not being used must be left as no connect
2015.04.06 YenPin
Add CLOCK Buffer Schematic (CRB Page123)
R2426~R2428 Close To U2401
SUSCLK is on the DSW well and is available earlier in the boot sequence.
Remove SUSCLK
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title PCH(5)_CLK
BG1/HW3
Engineer: Andy Kao
Size C
Project Name X3
Rev 1.0
Date: Wednesday, August 31, 2016
Sheet 24 of 97

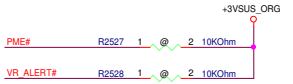
+3VSUS_ORG — +3VSUS_ORG 20,21,22,23,26
+VCC_RTC — +VCC_RTC 24,26,36,60
+VCCDSW — +VCCDSW 26,30
+VCCST_CPU — +VCCST_CPU 3,5,7,9,32
+3V — +3V 31,57,82,91
+3VSUS — +3VSUS 4,24,26,28,30,31,41,42,51,53,62,64,68,81,92

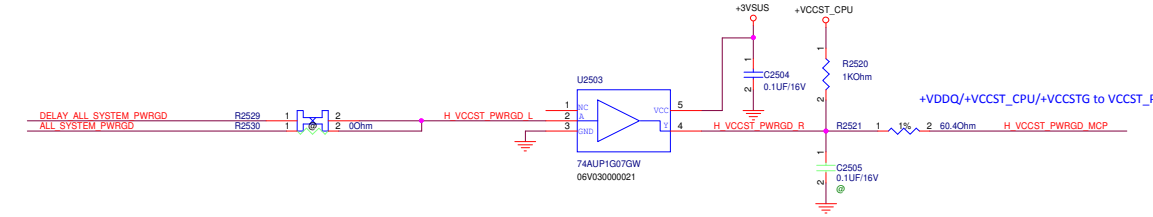




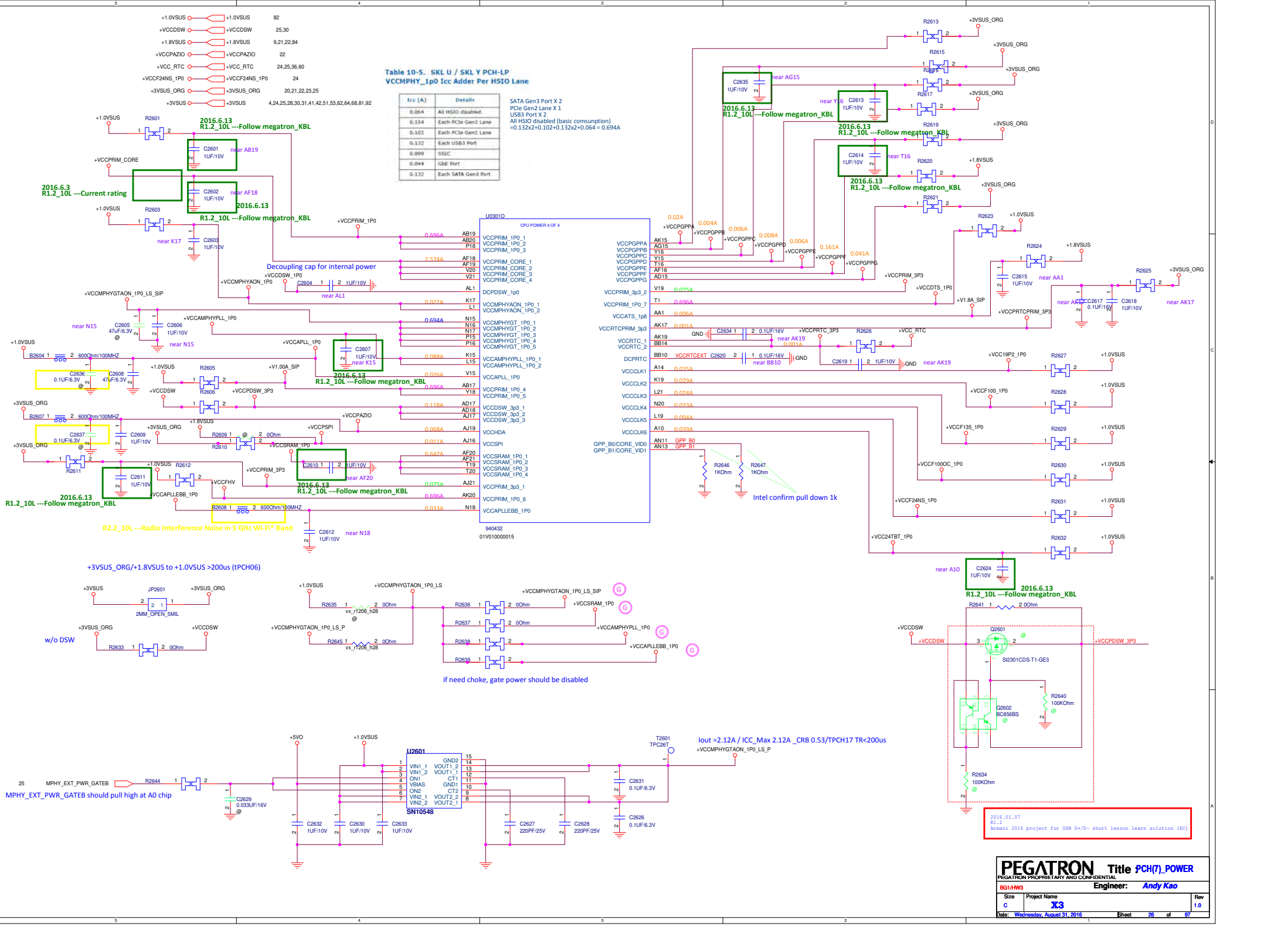








PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: SCH(6)_POWER MANAGE
BG1/HW3
Engineer: Andy Kao
Size: C | Project Name: X3 | Rev: 1.0
Date: Wednesday, August 31, 2016 | Sheet 25 of 97


+1.0VSUS +1.0VSUS 82
+VCCDSW +VCCDSW 25,30
+1.8VSUS +1.8VSUS 9,21,22,84
+VCCPAZIO +VCCPAZIO 22
+VCC_RTC +VCC_RTC 24,25,36,60
+VCCF24NS_1P0 +VCCF24NS_1P0 24
+3VSUS_ORG +3VSUS_ORG 20,21,22,23,25
+3VSUS +3VSUS 4,24,25,28,30,31,41,42,51,53,62,64,68,81,92
Table 10-5. SKL U / SKL Y PCH-LP
VCCMPHY_1p0 Icc Adder Per HSIO Lane
Icc (A) Details
0.064 All HSIO disabled.
0.154 Each PCIe Gen3 Lane
0.102 Each PCIe Gen2 Lane
0.132 Each USB3 Port
0.099 SSIC
0.044 GbE Port
0.132 Each SATA Gen3 Port
SATA Gen3 Port X 2
PCIe Gen2 Lane X 1
USB3 Port X 2
All HSIO disabled (basic comsunption)
=0.132x2+0.102+0.132x2+0.064 = 0.694A
2016.6.13
R1.2_10L ---Follow megatron_KBL
2016.6.3
R1.2_10L ---Current rating
Decoupling cap for internal power
U0301O
CPU POWER 4 OF 4
940432
01V010000015
R2.2_10L ---Radio Interference Noise in 5 GHz Wi-Fi* Band
Intel confirm pull down 1k
+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)
w/o DSW
if need choke, gate power should be disabled
MPHY_EXT_PWR_GATEB should pull high at A0 chip
U2601
SN10548
Iout =2.12A / ICC_Max 2.12A _CRB 0.53/TPCH17 TR<200us
2016.01.07
R1.2
Armani 2016 project for USB D+/D- short lesson learn solution (EC)
PEGATRON
Title PCH(7)_POWER
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3
Engineer: Andy Kao
Size C
Project Name X3
Rev 1.0
Date: Wednesday, August 31, 2016
Sheet 26 of 97

PEGATRON

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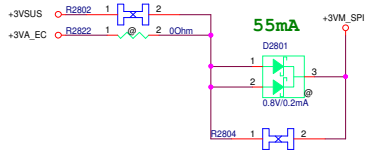
Title : <Title>

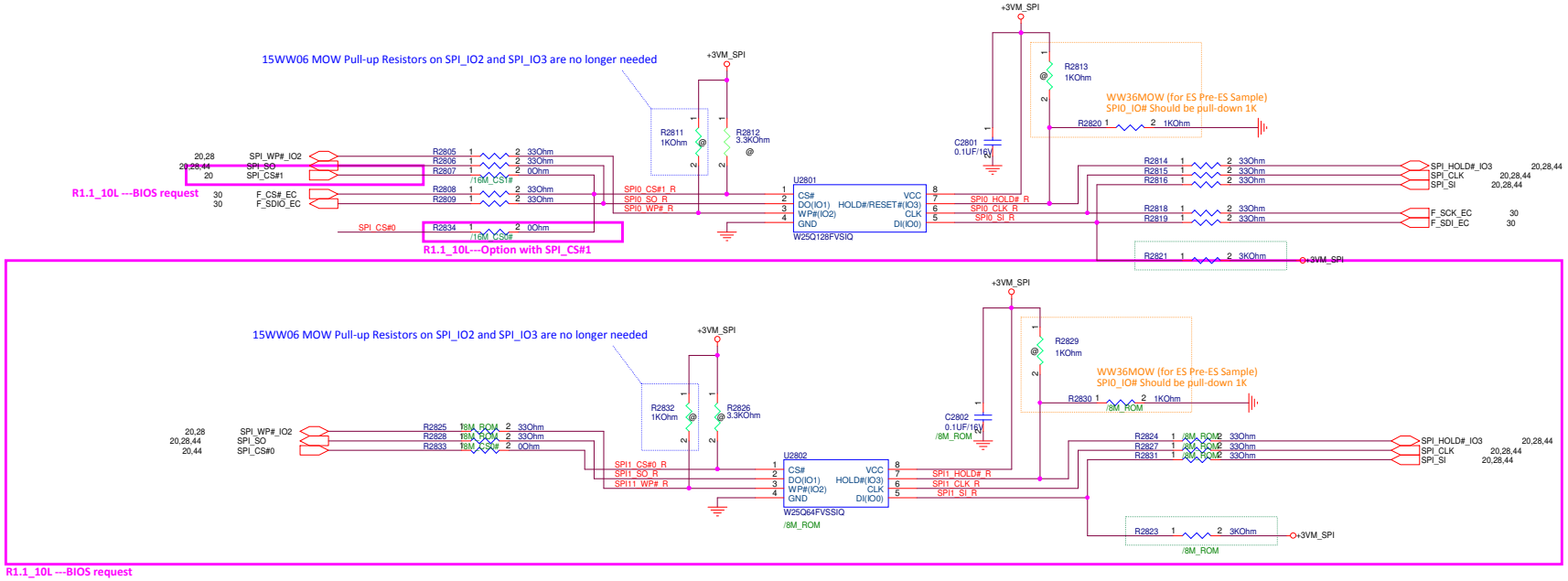
BG1/HW3

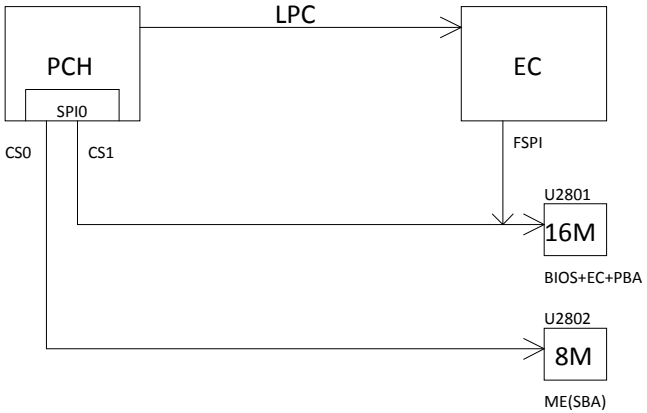
Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

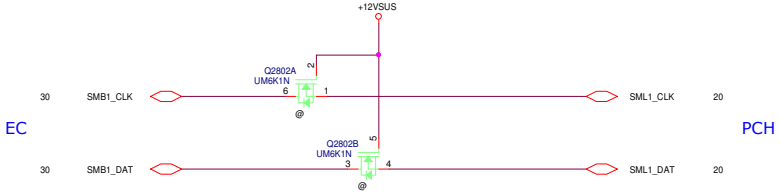
Date: Wednesday, August 31, 2016 Sheet 27 of 97







PCH SMBus



<Variant Name>

PEGATRON Title : PCH(9)_SPI,SMB

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
C	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 28 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

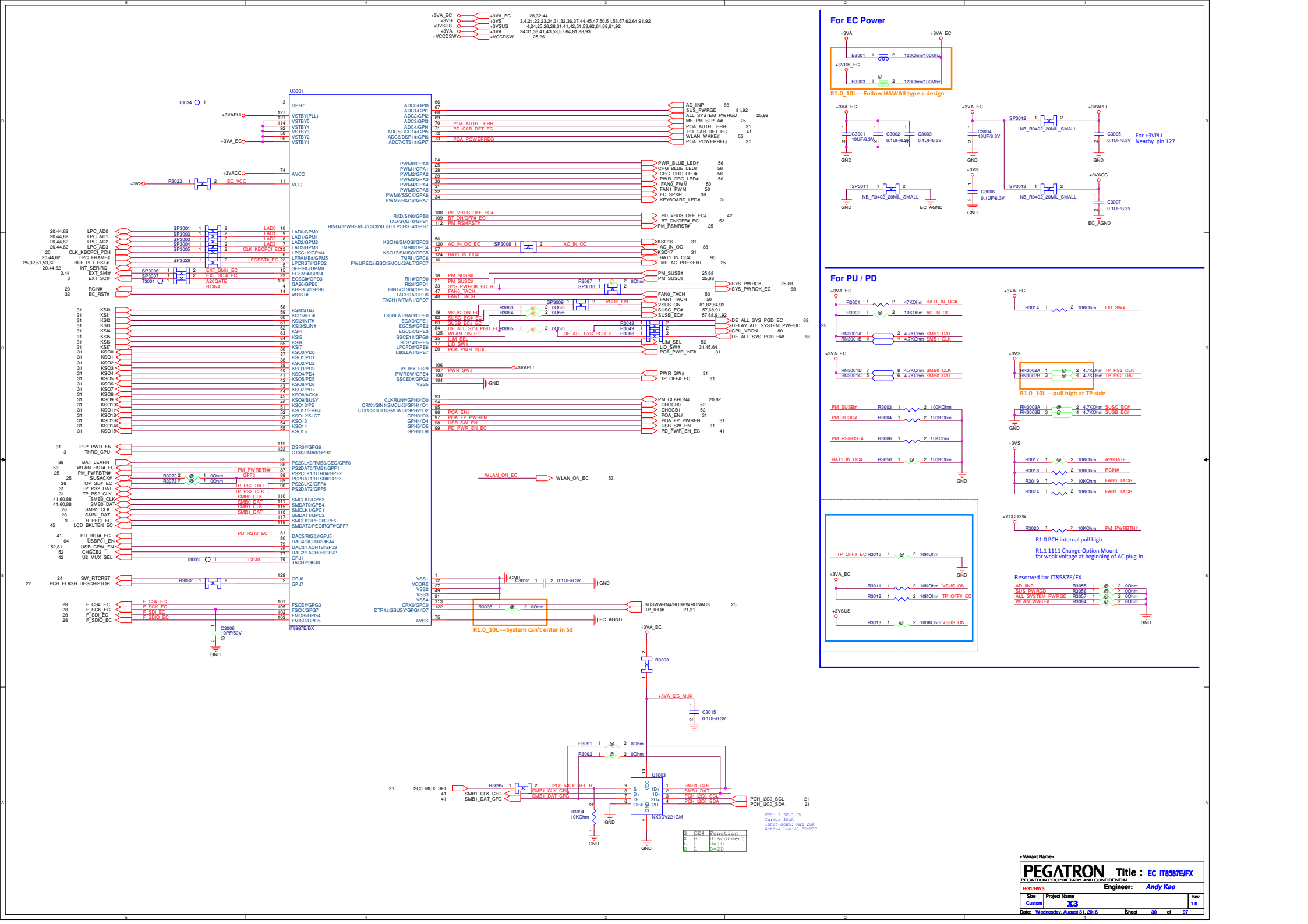
Title : <Title>

BG1/HW3

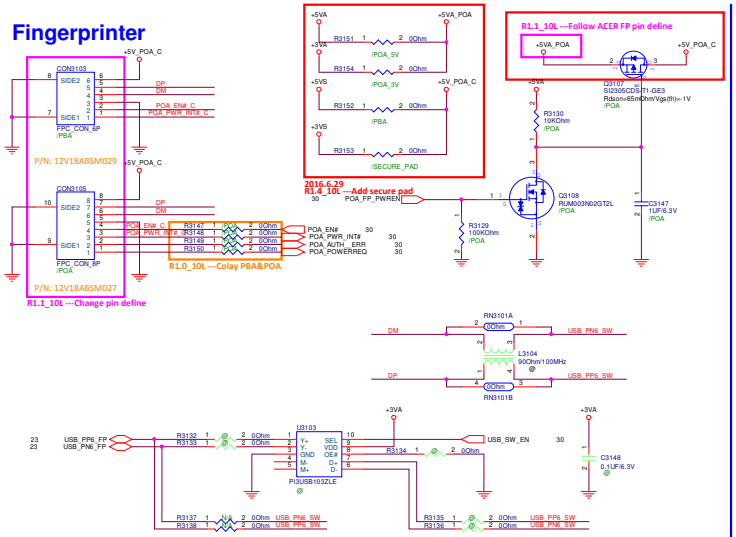
Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

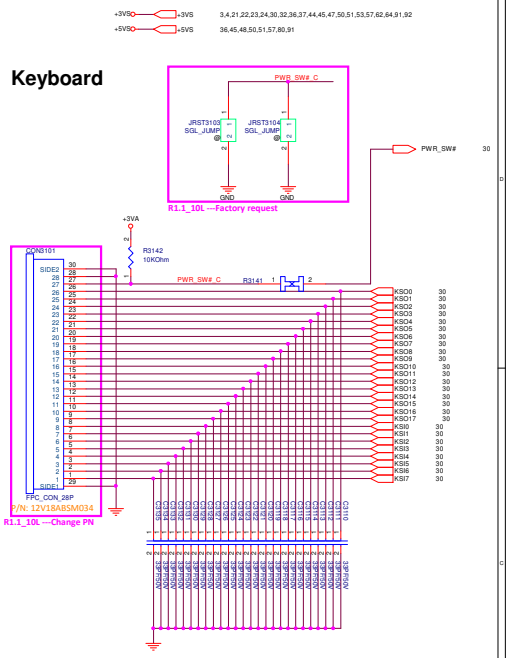
Date: Wednesday, August 31, 2016 Sheet 29 of 97


For EC Power
R1.0_10L ---Follow HAWAII type-c design
For +3VPLL
Nearby pin 127
For PU / PD
R1.0_10L ---pull high at TP side
R1.0 PCH internal pull high
R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in
Reserved for IT8587E/FX
R1.0_10L ---System can't enter in S3
U3001
IT8987E/BX
U3003
NX3DV221GM
VCC: 2.3V~3.6V
Iq:Max 30uA
Ishut-down: Max 2uA
Active Low:<0.25*VCC
<Variant Name>
PEGATRON
Title : EC_IT8587E/FX
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Andy Kao
BG1HW3
Size Custom
Project Name X3
Rev 1.0
Date: Wednesday, August 31, 2016
Sheet 30 of 97

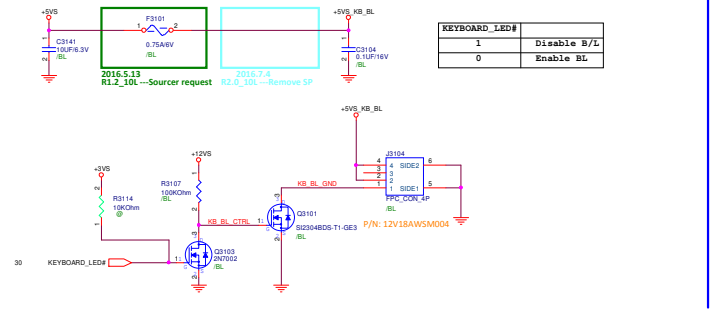
Fingerprinter



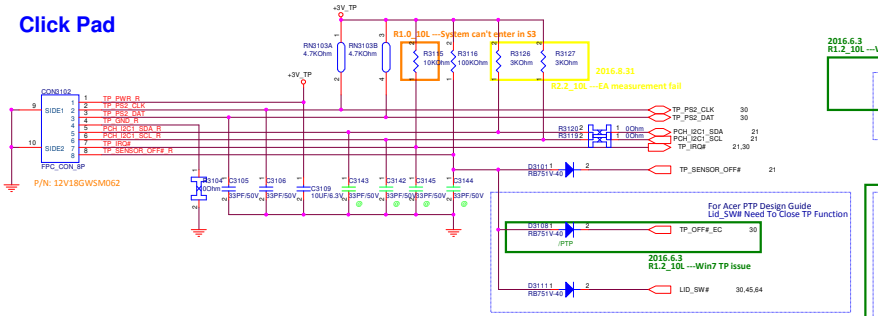
Keyboard

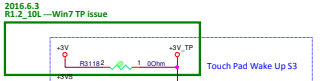


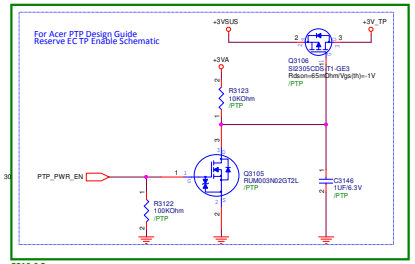
Keyboard LED



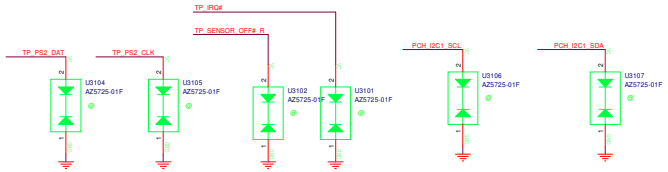
Click Pad







Reserve for EMI



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : EC_KB, TP

BG1/HW3

Engineer: Andy Kao

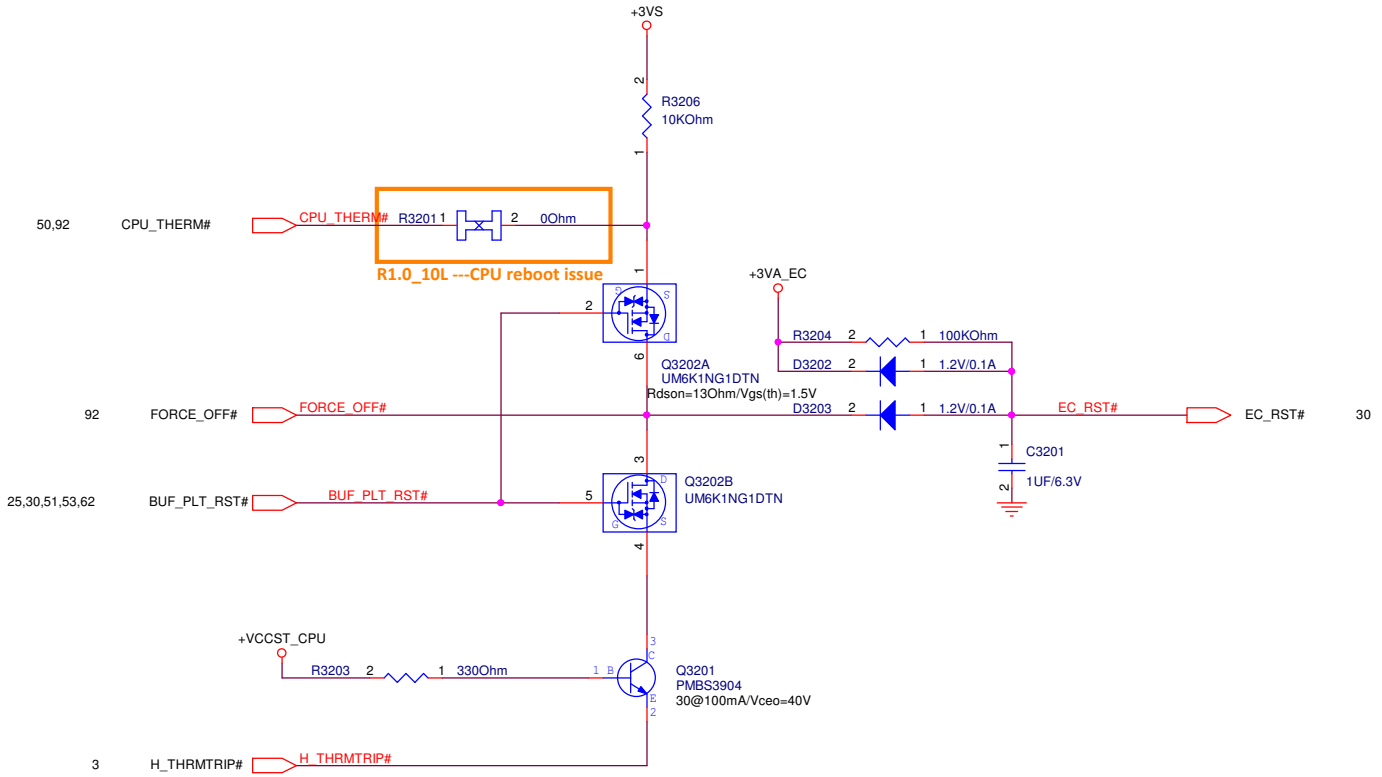
Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 31 of 97

+VCCST_CPU — +VCCST_CPU 3,5,7,9,25

+3VA_EC — +3VA_EC 28,30,44

+3VS — +3VS 3,4,21,22,23,24,30,31,36,37,44,45,47,50,51,53,57,62,64,91,92



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 32 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 33 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 34 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 35 of 97

AUD_ALC255

+1.5VS → +1.5VS 47,57,85
+3VS → +3VS 3,4,21,22,23,24,30,31,32,37,44,45,47,50,51,53,57,62,64,91,92
+5VS → +5VS 31,45,48,50,51,57,80,91

Analog
Digital

+1.5VS
L3601 1 2 120Ohm/100Mhz
C3612 10UF/6.3V
+5VS_PVDD_AVD
C3611 10UF/6.3V

AC_HP_R
AC_HP_L
LINE1_VREFO_L
LINE1_VREFO_R
MIC2_VREFO

+3VS_AUDIO
C3638 10UF/6.3V
C3617 1UF/6.3V
C3616 1UF/6.3V
C3615 2.2UF/6.3V
C3609 10UF/6.3V
R3635 100KOhm

+5VS_AUDIO
C3604 0.1UF/16V
C3637 10UF/6.3V
Place close to Pin 26

U3601A
CPVDD CBN CBP CPVEE HP-OUT-R/PORT-I-R HPOUT-L(PORT-I-L) LINE1-VREFO-L LINE1-VREFO-R MIC2-VREFO VREF LDO1-CAP AVDD AVSS1

CBP
AVSS2
LDO2-CAP
AVDD2
PVDD1
SPK-OUT-L+
SPK-OUT-L-
SPK-OUT-R-
SPK-OUT-R+
PVDD2
PDB
SPDIF-OUT/GPIO2
GND

H_SPKL+ H_SPKL- H_SPKR- H_SPKR+
PDB

LINE2-L(PORT-E-L)
LINE2-R(PORT-E-R)
LINE1-L(PORT-C-L)
LINE1-R(PORT-C-R)
VD33_STB
MIC_CAP
MIC2-R(PORT-F-R)/SLEEVE
MIC2-L(PORT-F-L)/RING
MONO-OUT
SPDIFO/FRONT_JD(JD3)/GPIO3
MIC2/LINE2_JD(JD2)
HP/LINE1_JD(JD1)

LINE1_L
LINE1_R
C3614 10UF/6.3V
SLEEVE
RING2
R3604 100KOhm
R3603 200KOhm
HP_JD#

+3VA
R3637 0Ohm
Digital
Analog
PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

Place close audio codec

DVDD GPIO/DMIC-DATA GPIO1/DMIC-CLK DC_DET SDATA-OUT BCLK LDO-CAP SDATA-IN DVDD-IO SYNC RESETB PCBEEP
ALC255-CGT

Analog
Digital

+3VS_AUDIO
C3605 10UF/6.3V
C3606 0.1UF/16V
Place close to pin 1

PC_BEEP
HDA_RST# 22
HDA_SYNC 22
HDA_SDI0 22
HDA_BCLK 22
HDA_SDO 22

+3VS_AUDIO
C3618 0.1UF/16V
C3625 10UF/6.3V

R3621 22Ohm
R3620 22Ohm
C3613 22PF/50V
MLCC 22PF/50V (0402) NPO 5%

DMIC_DAT
DMIC_CLK
R3614 0Ohm
R3615 22Ohm
C3629 33PF/50V
C3624 33PF/50V

2016.02.04
R1.2
EMC/Ricky changes 10 pF to 33 pF

2016.02.02
R1.2
Change 22 pF from 0201 to 0402

PC_BEEP C3602 0.1UF/16V PCBEEP
R3605 22KOhm
C3626 100PF/50V
R3618 4.7KOhm

R3638 0Ohm
R3639 0Ohm
D3603 1V/0.2A
HDA_SPKR 22
EC_SPKR 30

U3601B
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9
ALC255-CGT

R1.0_10L ---Support UAJ

LINE1_L	C3642	1 2	4.7UF/6.3V	AC_HP_L
LINE1_R	C3641	1 2	4.7UF/6.3V	AC_HP_R
LINE1_VREFO_L	R3707	1 2	4.7KOhm	AC_HP_L
LINE1_VREFO_R	R3708	1 2	4.7KOhm	AC_HP_R

+3VS_AUDIO
R3650 0Ohm
D3601 1V/0.1A
R3652 1KOhm
R3651 10KOhm
C3639 1UF/6.3V
PDB
21 OP_SD#
HDA_RST#
30 OP_SD#_EC
D3604 RB751V-40

In order to prevent the built-in LDO damaged from over-voltage on +5VSYS or Standby power line, we suggested using this Voltage suppressing device.

Add this Filter to avoid other components/chips be influenced

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

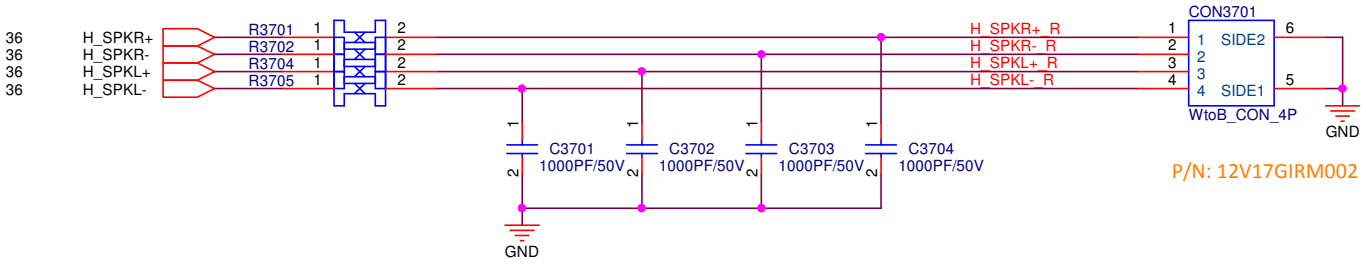
Grounding circuit for combo jack SLEEVE pin

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

2015.09.10 Edison
EMI 建議Audio moat 預留TVS

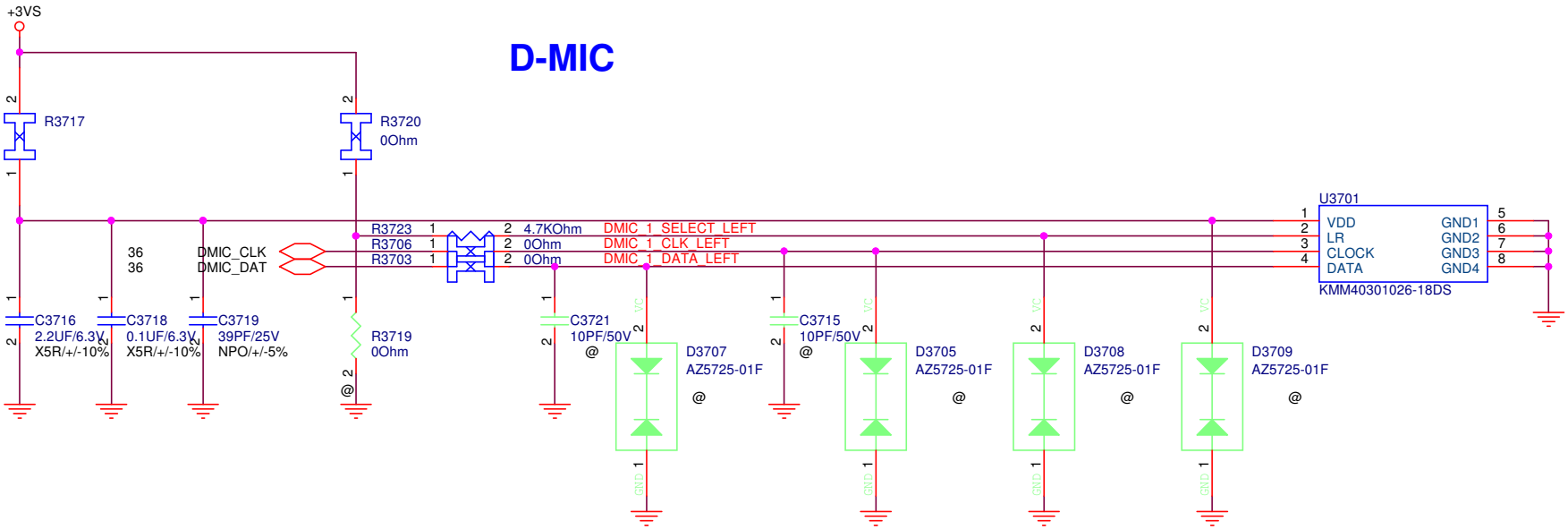
PEGATRON Title : AUD_ALC255
BG1/HW3 Engineer: Andy Kao
Size C | Project Name X3 | Rev 1.0
Date: Wednesday, August 31, 2016 | Sheet 36 of 97

Speaker



P/N: 12V17GIRM002

D-MIC



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Speaker

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 37 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 38 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 39 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 40 of 97

ANX7428

2016.7.6
R2.0_10L ---Keep original design

+3VDB_PD — R4134 0Ohm vx_r0402_0ohm_small — +3VA_PD
+3VSUS — R4130 0Ohm vx_r0402_0ohm_small @
+3VA — R4126 0Ohm vx_r0402_0ohm_small @
+5VSUS — R4129 — V5_VCONN

VBUS_USB_TYPE_C	VBUS_USB_TYPE_C	42,43
+3VA	+3VA	24,30,31,36,43,53,57,64,81,88,93
+3VA_PD	+3VA_PD	42
+3VSUS	+3VSUS	4,24,25,26,28,30,31,42,51,53,62,64,68,81,92
+3VDB_PD	+3VDB_PD	43

V5_VCONN — C4118 10UF/6.3V @

TBD
+3VA_PD — R4123 100KOHM vx_r0402_small — DDI2_AUXN_C
DDI2_AUXP_C — R4124 100KOHM vx_r0402_small

The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.

+3VA_PD — C4101 1UF/16V vx_c0402_small; C4102 0.1UF/6.3V; C4100 1000PF/50V vx_c0402_small
+3VA_PD — C4104 1UF/16V vx_c0402_small; C4105 0.1UF/6.3V; C4103 1000PF/50V vx_c0402_small

U4100A

Connect to DP Source	DDI2_TXP0	3	DP_LN_0P	1
	DDI2_TXN0	3	DP_LN_0N	2
	DDI2_TXP1	3	DP_LN_1P	7
	DDI2_TXN1	3	DP_LN_1N	8
	DDI2_TXP2	3	DP_LN_2P	9
	DDI2_TXN2	3	DP_LN_2N	10
	DDI2_TXP3	3	DP_LN_3P	3
	DDI2_TXN3	3	DP_LN_3N	4
	DDI2_AUXP	3	AUXP	16
	DDI2_AUXN	3	AUXN	17
	DDI2_HPD	3	HPD	37
Connect to USB3.0 signals	USB3_TXN3	23	SSTX_N	11
	USB3_TXP3	23	SSTX_P	5
	USB3_RXN3	23	SSRX_N	12
	USB3_RXP3	23	SSRX_P	6
	PD_RST#_EC	30	RESET_N	33
			NC	23
	SMB1_DAT_CFG	30	CFG_SDA	38
	SMB1_CLK_CFG	30	CFG_SCL	39
	SMB0_DAT	30,60,88	M_SCL/GPIO_4	43
	SMB0_CLK	30,60,88	M_SDA/GPIO_5	42
			TEST_EN	34
			DRP_EN	28
			I2C_ADR_1/GPIO_3	47
			I2C_ADR_0/INTP_IN/GPIO_2	48
			AVSS	49
			DVSS	46
			AVDD33_1	13
			AVDD33_2	24
			DVDD_IO	40
			SSTXP1	25
			SSTXN1	26
			SSRXN2	35
			SSRXP2	36
			SSTXP2	30
			SSTXN2	29
			SSRXN1	32
			SSRXP1	31
			SBU1	19
			SBU2	18
			CC1	21
			VCONN1_EN/GPIO_0	45
			CC_CAP	22
			CC2	20
			VCONN2_EN/GPIO_1	44
			VBUS_DIV6	15
			INTP_OUT	41
			CABLE_DET	14
			PWR_EN	27

Connect to USB Type-C connector

SSTXP1	UTC_A2_SSTXp1	42
SSTXN1	UTC_A3_SSTXn1	42
SSRXN2	UTC_A10_SSRXn2	42
SSRXP2	UTC_A11_SSRXp2	42
SSTXP2	UTC_B2_SSTXp2	42
SSTXN2	UTC_B3_SSTXn2	42
SSRXN1	UTC_B10_SSRXn1	42
SSRXP1	UTC_B11_SSRXp1	42
SBU1	UTC_A8_SBU1_AUX	42
SBU2	UTC_B8_SBU2_AUX	42

V5_VCONN is the power source for VCONN(UTC_B5_CC2 or UTC_A5_CC1).
Please make sure:
1) VCONN Voltage range [4.75V, 5.5V]
2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.

Reverse voltage protection is required.
It might be necessary to add a diode to protect the power supply.

Requirement of Q3:
1) Id >= 500mA (Vgs = - 4.5V).
2) Ron < 120 mOhm (Vgs = - 4.5V).
3) Max Vds >= -10V

CHIP_CC1 — R4102 — UTC_A5_CC1 42
CHIP_CC2 — R4105 — UTC_B5_CC2 42
C4106 1000PF/16V vx_c0201

V5_VCONN — R4103 100KOHM vx_r0402_small — U4101 TPS2041BDBVR (IN, OUT, GND, OC#, EN#)
V5_VCONN — R4121 100KOHM vx_r0402_small — U4102 TPS2041BDBVR (IN, OUT, GND, OC#, EN#)

0629-007K000
VIN: 2.7V~5.5V
Iq:Max 190uA
Ishut-down: Max 1uA
Active Low:<0.6V
ILMIT:0.6A~0.8A~1.0A

VBUS_USB_TYPE_C — R4107 750KOhm — R4110 150KOhm vx_r0402_small 1%

+3VA_PD — R4135 1.8KOHM — R4136 1.8KOHM — CFG_SDA / CFG_SCL
PD_VBUS_CTRL — R4120 4.7KOhm vx_r0402_small @ — +3VA_PD
R4125 2 1 100KOhm — PD_RST#_EC (From EC:)
R4133 — CFG_SDA; R4132 — CFG_SCL
R4127 vx_r0402_0ohm_small @ SMB_DAT_PD; R4128 @ SMB_CLK_PD 0Ohm vx_r0402_0ohm_small

M_SDA/GPIO_5 pin:
Connect to AP/CPU/Charge IC as a charge mode indicator.

Logic 0: Fast Charger Mode, charge voltage > 5V or charge current >= 1.5A.

Logic 1: Normal Charger Mode, charge voltage = 5V and charge current <1.5A.

+3VA_PD — R4109 4.7KOhm vx_r0402_small — DRP_EN
DRP_EN pin:
Logic 1: DRP Mode.
Logic 0: DFP Mode.
DRP_EN — R4112 4.7KOhm vx_r0402_small @

I2C_ADR_0 — R4118 — VBUS_DISCHARGE_CTRL 42

Change to 0650-0084000

I2C_ADR_1/GPIO_3 pin: Connected to AP or CPU as UART TXD
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used as software UART output after OCM boot.

I2C_ADR_0/INTP_IN/GPIO_2:
Connect to AP or CPU to control the discharge of VBUS.
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used for VBUS discharge control after OCM boot.

CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.

Note:
1. Set R21 = 100K, C15 = 22nF to filter the short high toggle pulse in DRP mode when cable is unplugged in ES chip.
2. Set R21 to 0R, C15 to DNP when this is fixed in CS chip.

PD_PWR_EN_EC 30 — R4122 100KOhm
PWR_EN pin:
Controlled by AP or CPU
Logic 1: to power up the chip.
Logic 0: to power down the chip.

INTP_OUT — (Default: O.D) — PD_INT# — T4101

INTP_OUT pin: interrupt output.
Connect to AP or CPU.

If AP or GPU's interrupt is low level triggered, set R16 = 4.7K, leave R22 not installed;
else if is high level triggered, set R22 =4.7K, leave R16 not installed.

CABLE_DET — R4113 — PD_CAB_DET_EC 30

U4100B
AVSS_1 50, AVSS_2 51, AVSS_3 52, AVSS_4 53, AVSS_5 54, AVSS_6 55, AVSS_7 56, AVSS_8 57
ANX7428QN-AB-R

I2C Address Selection:

I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

I2C_ADR_1 and I2C_ADR_0 pin:
1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

<Variant Name>

PEGATRON Title : POWER_FLOWCHART
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Andy Kao

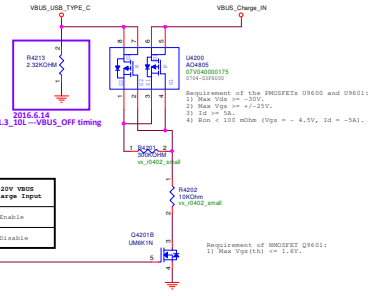
Size	Project Name	Rev
C	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 41 of 97

VBUS Control

Optional:
If PMIC can detect VBUS presence and disable/enable VBUS, the VBUS control circuit can be removed.

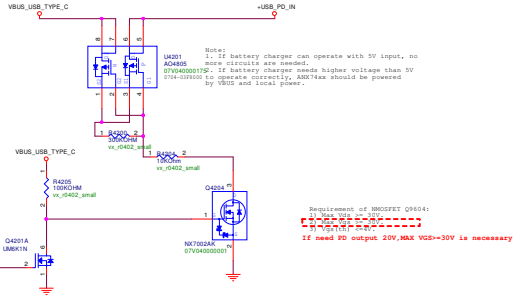
5V VBUS Output Control



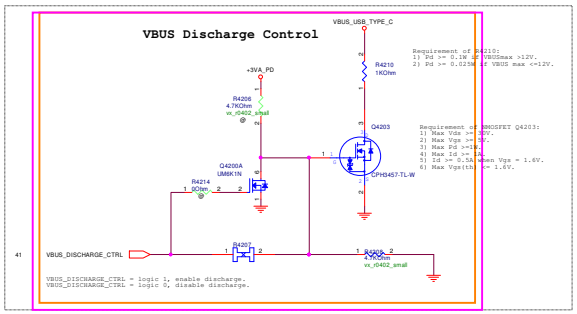
VBUS_CTRL Function:

VBUS_CTRL	5V VBUS Output	5~20V VBUS Charge Input
Logic 0	Disable	Enable
Logic 1	Enable	Disable

5~20V VBUS Charge Input Control

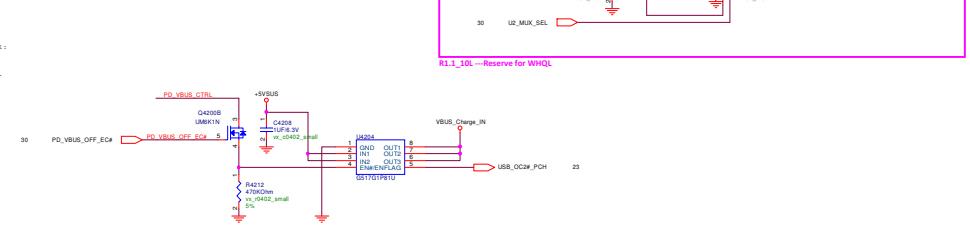


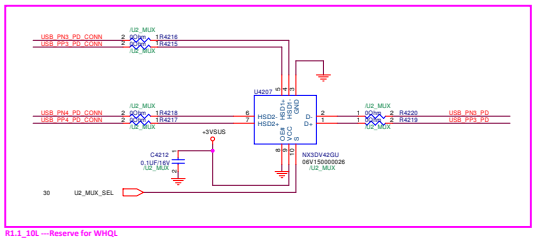
VBUS Discharge Control



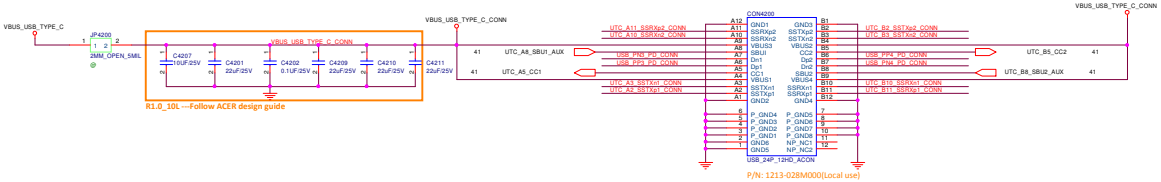
R1.0_10L ---Unmount discharge circuit

R1.1_10L ---PD test fail



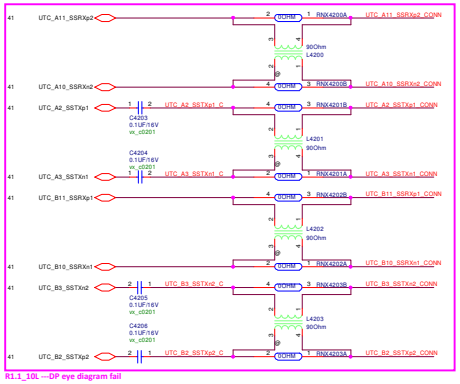


R1.1_10L ---Reserve for WHQL

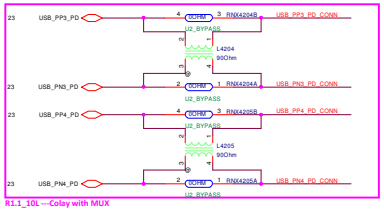


R1.1_10L ---Follow ACER design guide

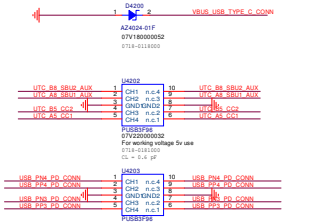
ESD



R1.1_10L ---DP eye diagram fail

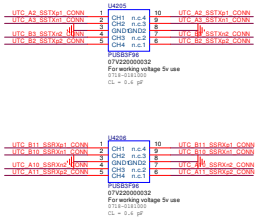


R1.1_10L ---Colay with MUX



USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1



<variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER_FLOWCHART

Engineer: Andy Kao

Size	Project Name	Rev
D	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 42 of 97

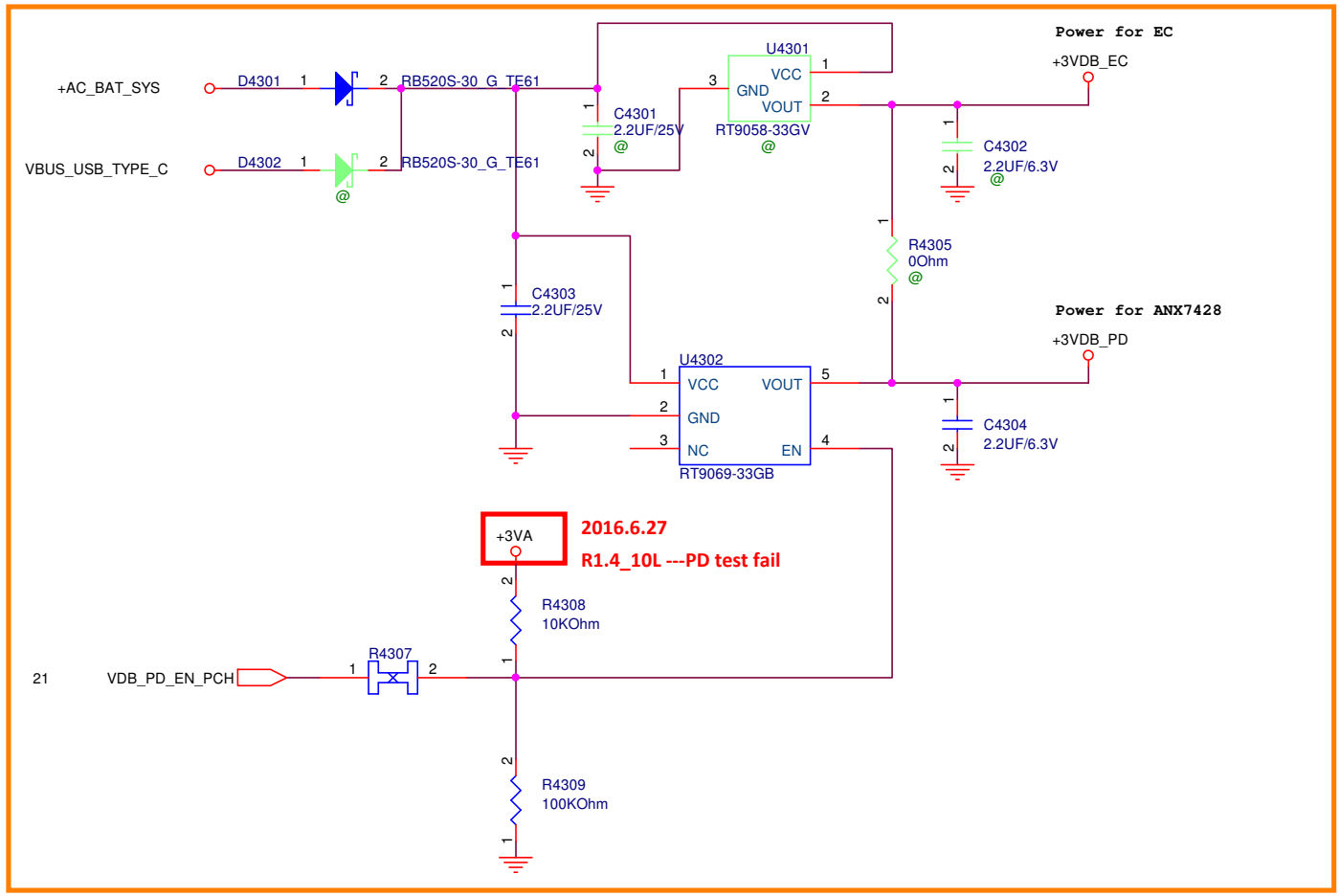
Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C	VBUS_USB_TYPE_C	41,42	
+AC_BAT_SYS	+AC_BAT_SYS	45,80,81,82,83,88	
+3VDB_EC	+3VDB_EC	30	
+3VDB_PD	+3VDB_PD	41	

Requirement of U1:
1) Vin range: 4V-30V.
2) Vout: EC's operating voltage + Vf of D1
3) Output current >= EC's operating current.

R1.0_10L ---Follow HAWAII type-c design



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

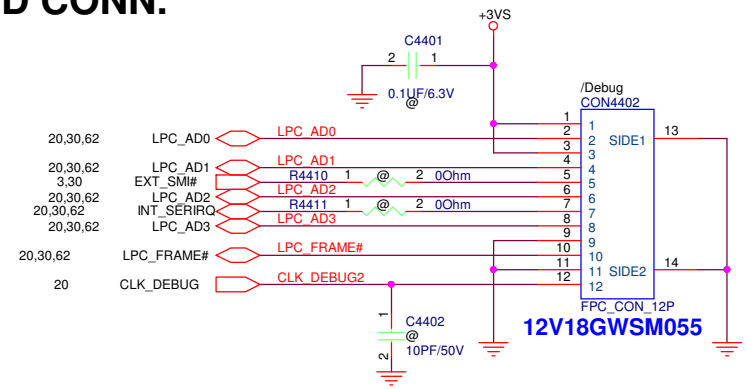
Title : Dead Battery

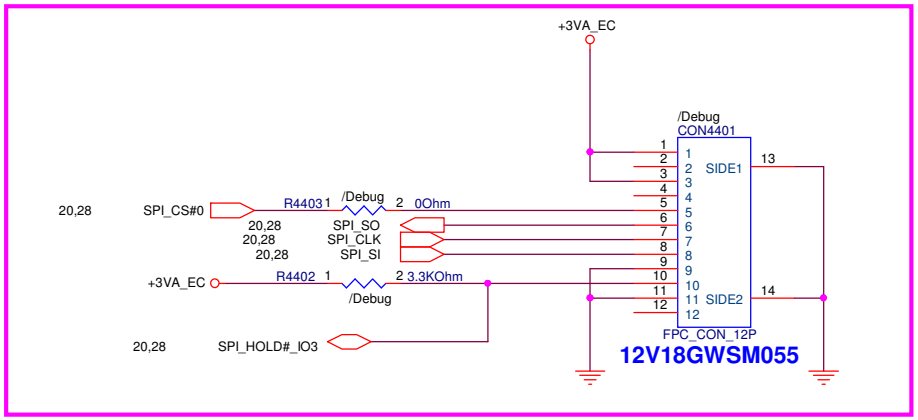
Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 43 of 97

DEBUG CARD CONN.





R1.1_10L ---BIOS request

<Variant Name>

PEGATRON Title : DEBUG CONN.

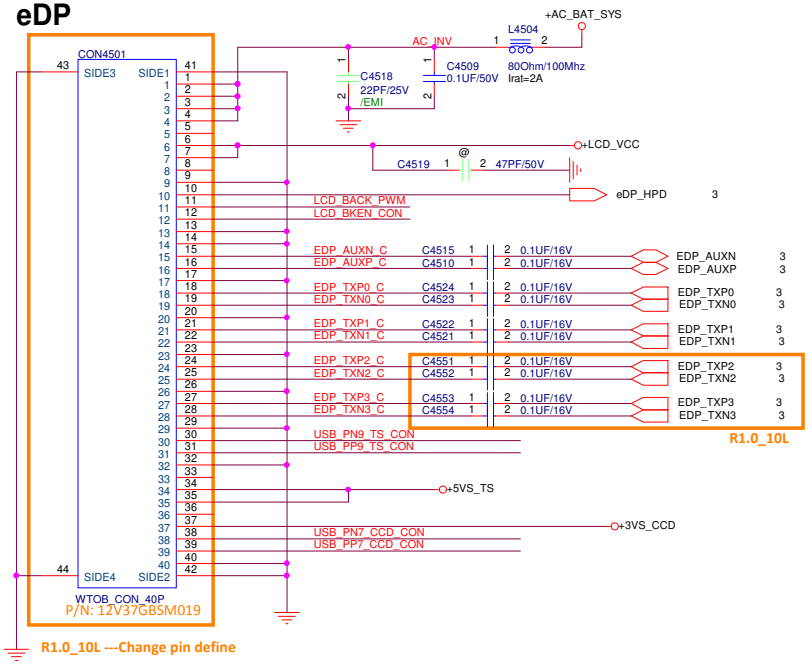
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

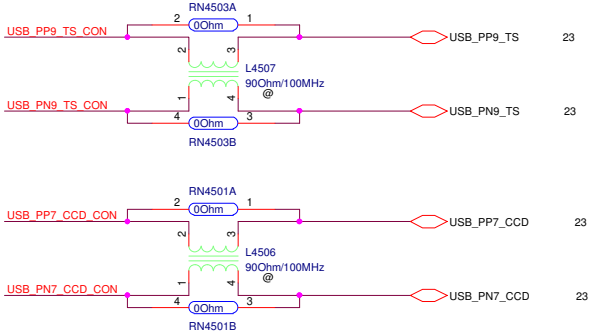
Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 44 of 97

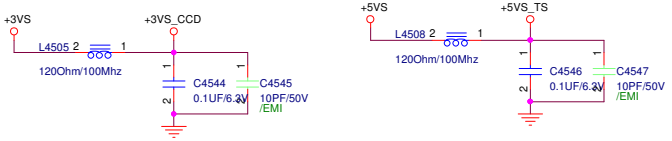
eDP

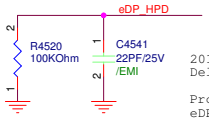


R1.0_10L ---Change pin define



Camera

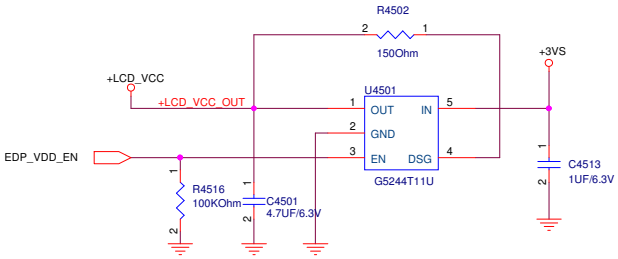


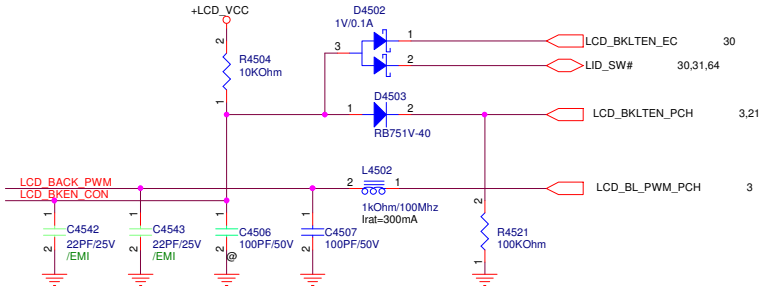


2015.04.14 YenPin
Delete eDP_HPD Pull High Path

Processor DisplayPort* Disabling and Termination Guidelines Checklist
eDP_HPD pull down to ground via 100K ohm resistor

LCD VDDEN / +LED_VCC





<variant_name>

PEGATRON Title : eDP CONN

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 45 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 46 of 97

T4702 1 PRE

Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

T4701 1 EQ

Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

T4703 1 ISET

TMDS output swing adjustment; Internal pull down at ~150k, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%

+3VS_PS — Vendor — R4725 4.7KOhm @ — PRE — R4726 4.7KOhm @ — GND

+3VS_PS — Vendor — R4727 4.7KOhm @ — EQ — R4728 4.7KOhm @ — GND

+3VS_PS — Vendor — R4729 4.7KOhm @ — ISET — R4730 4.7KOhm @ — GND

+3VS — R4718 — +3VS_PS

+1.5VS — R4721 — +1P5VS_PS

R1.1_10L ---Follow megatron

+3VS_PS — R4710 4.7KOhm — DDCBUF — R4714 4.7KOhm @ — GND

Enable active DDC buffer; Internal pull down at ~150KΩ, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor

SCL_SRC
SDA_SRC

3 DDPB_CTRLCLK — HDMI_SCL_PCH — R4733 — SCL_SRC
3 DDPB_CTRLDATA — HDMI_SDA_PCH — R4732 — SDA_SRC

1 T4704

IO_HDMI_SCL 48
IO_HDMI_SDA 48

+3VS_PS
+1P5VS_PS

C4704 0.1UF/6.3V
C4705 0.01UF/16V
C4701 0.01UF/16V

U4701A — PS8201ATQFN40GTR2-A0

3	DDI1_TXP2	C4729	HDMI_TXP2_PS	IN_D2p	OUT_D2p → HDMI_TXP2 48
3	DDI1_TXN2	C4730	HDMI_TXN2_PS	IN_D2n	OUT_D2n → HDMI_TXN2 48
			HPD_SRC	HPD_SRC	HPD_SNK → DP1_HPD_CON 48
3	DDI1_TXP1	C4731	HDMI_TXP1_PS	IN_D1p	OUT_D1p → HDMI_TXP1 48
3	DDI1_TXN1	C4732	HDMI_TXN1_PS	IN_D1n	OUT_D1n → HDMI_TXN1 48
3	DDI1_TXP0	C4733	HDMI_TXP0_PS	IN_D0p	OUT_D0p → HDMI_TXP0 48
3	DDI1_TXN0	C4734	HDMI_TXN0_PS	IN_D0n	OUT_D0n → HDMI_TXN0 48
				I2C_CTL_EN	CFG → R4715 2 @ 1 4.7KOhm → +3VS_PS
3	DDI1_CLKP	C4727	HDMI_CLKP_PS	IN_CKp	OUT_CKp → HDMI_CLKP 48
3	DDI1_CLKN	C4728	HDMI_CLKN_PS	IN_CKn	OUT_CKn → HDMI_CLKN 48

Configuration pin, 3.3V IO, internal pull down at ~150k. 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable

(Typ:1.5V ; Max:1.53V ; Min:1.47V)

3 DDI1_HPD — DDI1_HPD — R4731 — HPD_SRC

+3VS_PS — +1P5VS_PS — R4717 4.7KOhm @ — C4709 0.1UF/6.3V — C4710 0.01UF/16V — GND

R4701 4.99KOhm

C4706 0.1UF/6.3V
C4707 0.1UF/6.3V
C4708 0.1UF/6.3V

DC cou;ing enable; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

U4701B — PS8201ATQFN40GTR2-A0

42	EPAD1	EPAD8	49
43	EPAD2	EPAD7	48
44	EPAD3	EPAD6	47
45	EPAD4	EPAD5	46

R1.1_10L ---Sourcer request

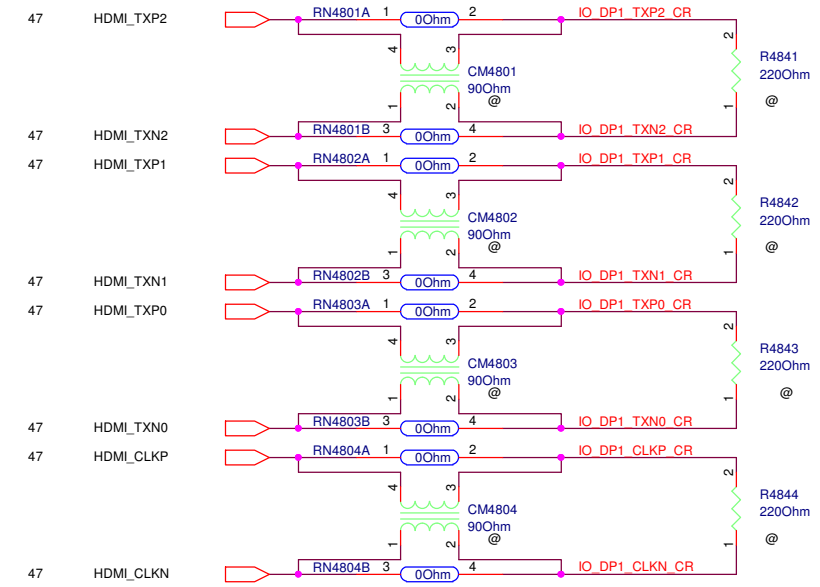
PEGATRON Title : HDMI-4K2K
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Andy Kao
BG1/HW3
Size C | Project Name X3 | Rev 1.0
Date: Wednesday, August 31, 2016 | Sheet 47 of 97

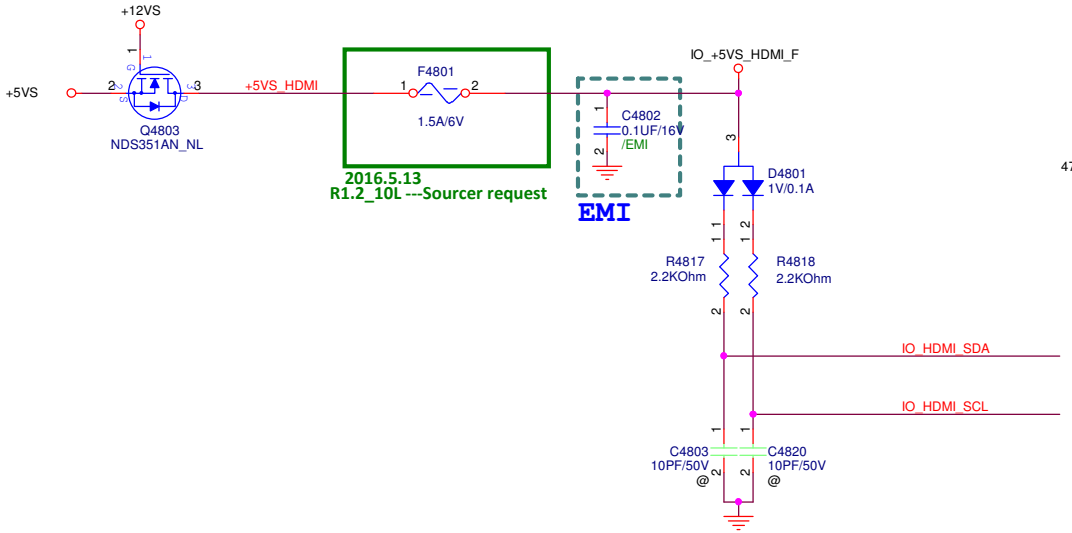
HDMI

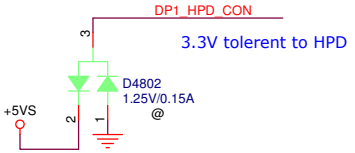
+3VS → +3VS 3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92

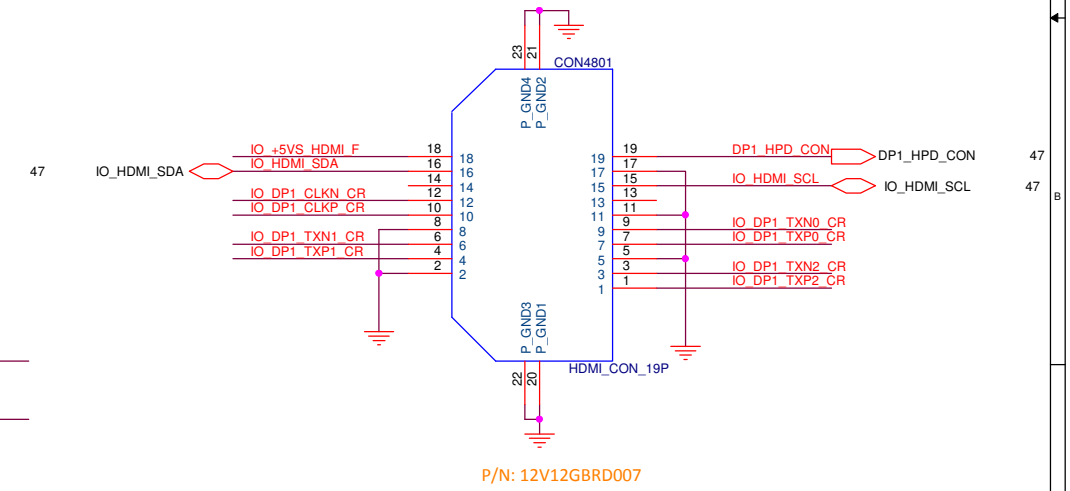
+5VS → +5VS 31,36,45,50,51,57,80,91

+12VS → +12VS 31,57,91









P/N: 12V12GBRD007

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : HDMI-4K2K

Engineer: Andy Kao

BG1/HW3

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 48 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

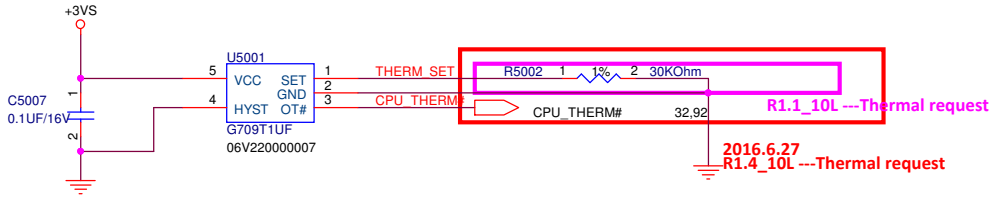
Size	Project Name	Rev
A	X3	1.0

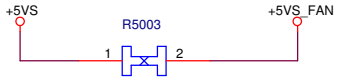
Date: Wednesday, August 31, 2016 Sheet 49 of 97

Thermal Sensor

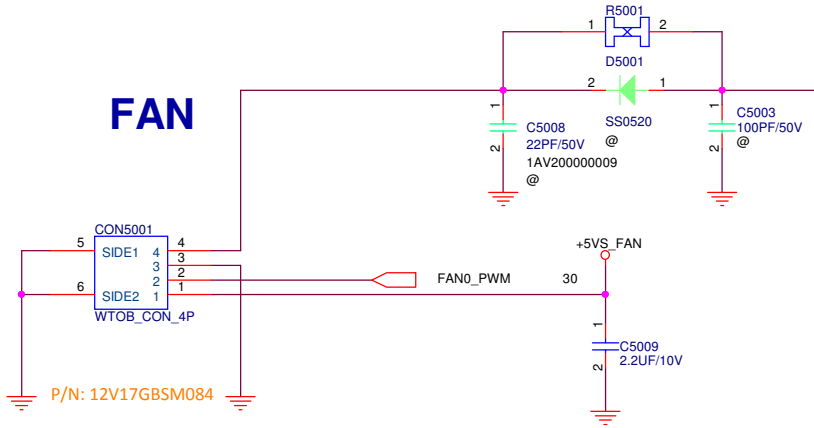
temp setting : 80 degree

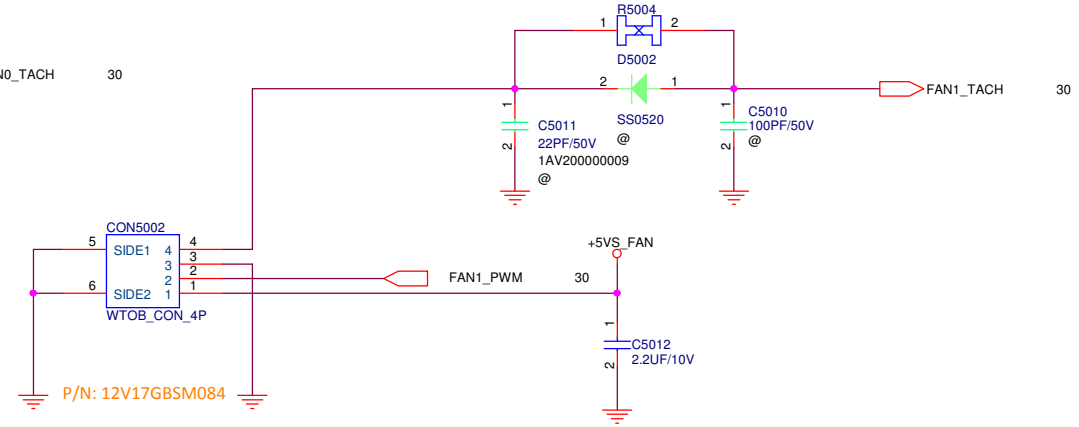
RSET(kΩ)= 0.0012T*T - 0.9308T + 96.147





FAN





<Variant Name>

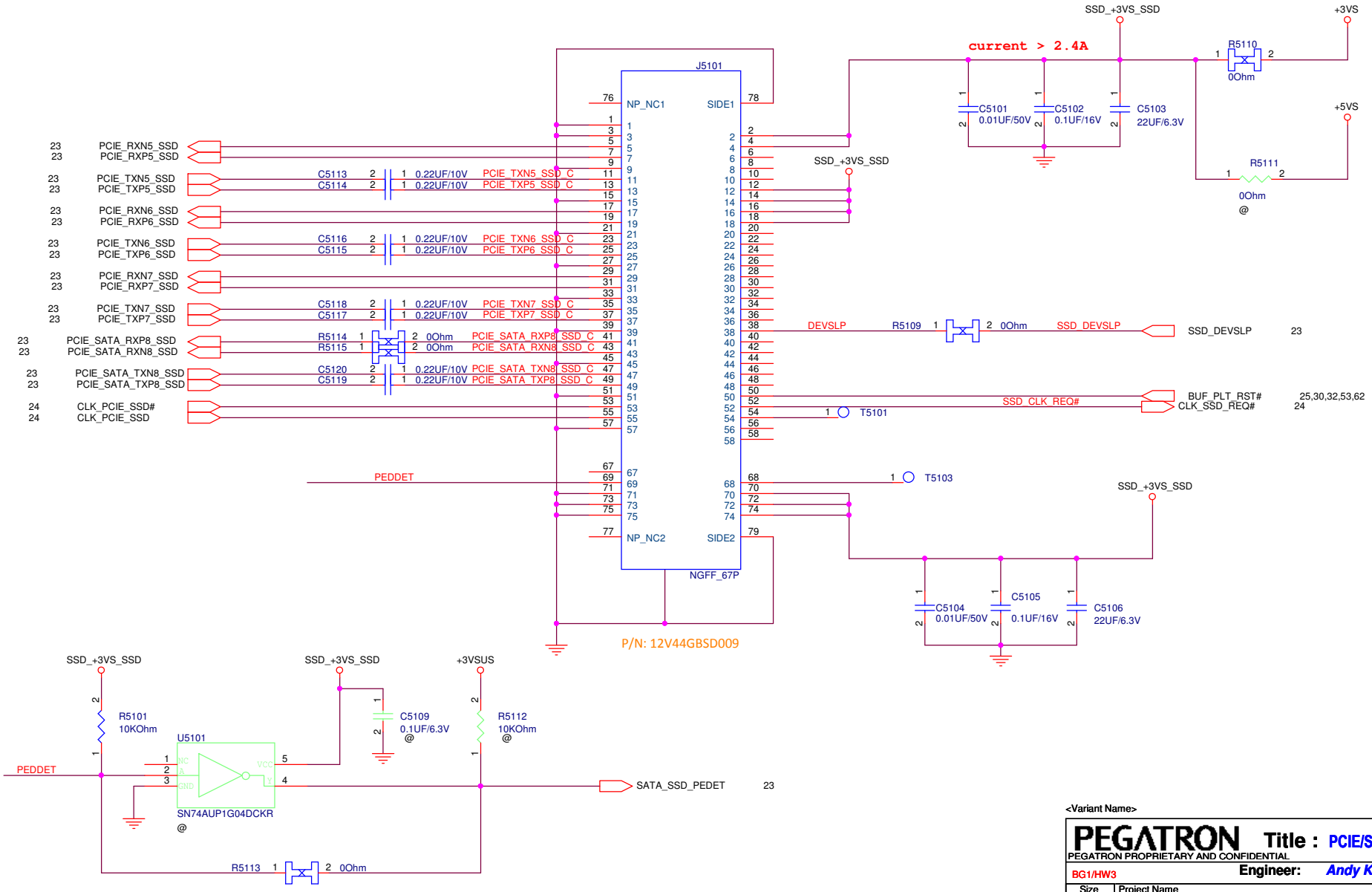
PEGATRON Title : Thermal/Fan

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 50 of 97

SSD(SATA/PCIE x4) NGFF socket (M-key)



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCIE/SATA SSD

BG1/HW3

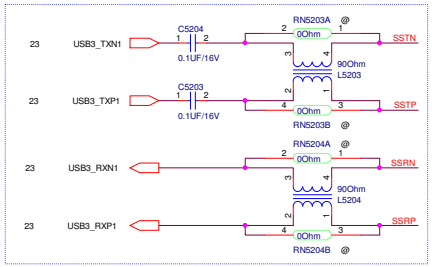
Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

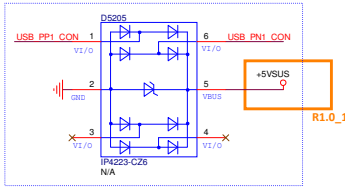
Date: Wednesday, August 31, 2016 Sheet 51 of 97

USB 3.0

USB3.0 Choke

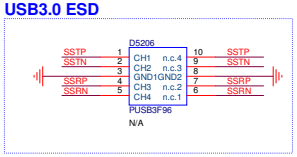


USB2.0 ESD

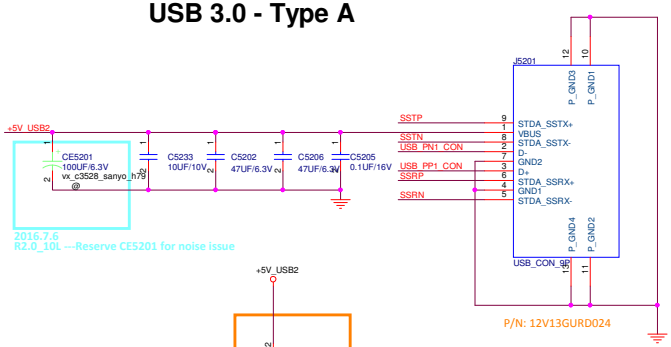


R1.0_10L ---Iphone charge issue

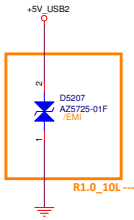
USB3.0 ESD



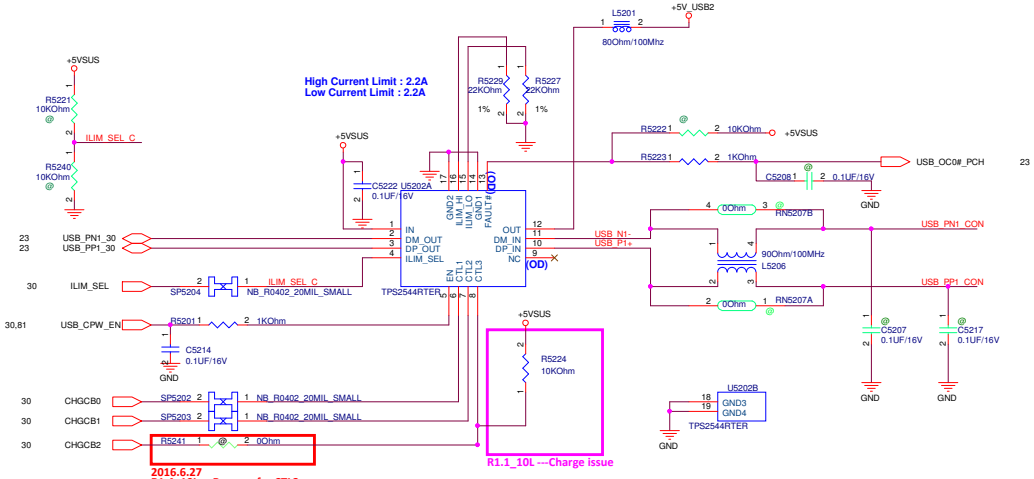
USB 3.0 - Type A



P/N: 12V13GURD024

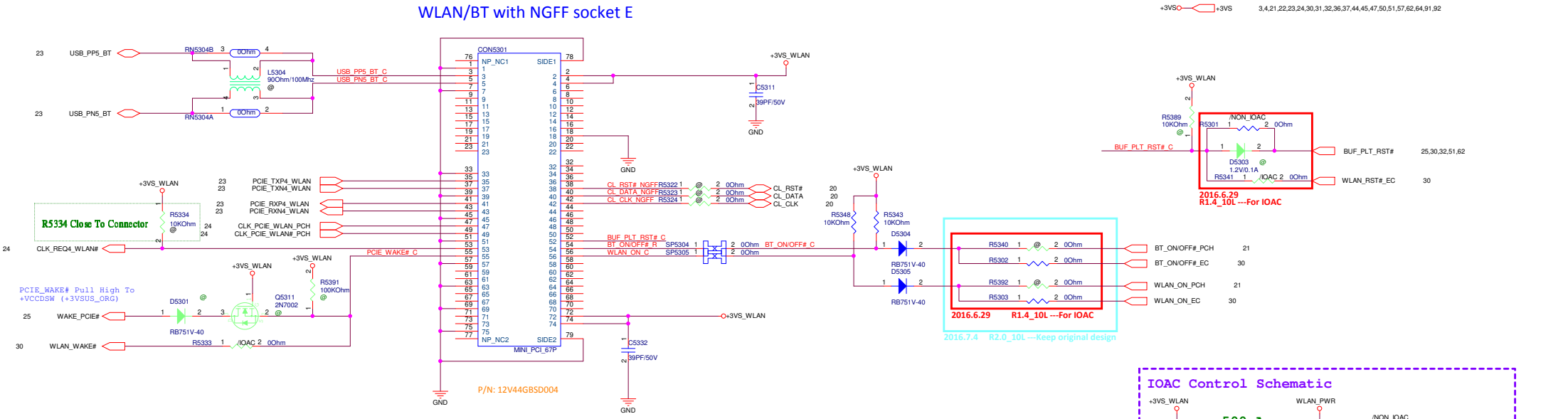


R1.0_10L ---For EMI



PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : USB JACK
	Engineer: Andy Kao
BG1/HW3	
Size: Custom	Project Name: X3
Rev: 1.0	
Date: Wednesday, August 31, 2016	Sheet 52 of 97

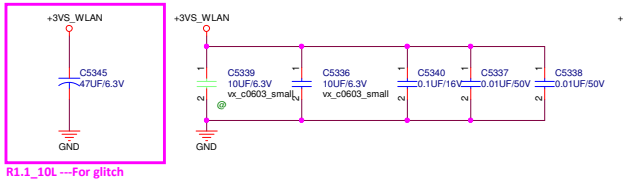
WLAN/BT with NGFF socket E



+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

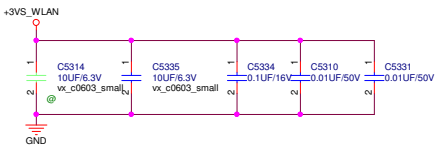
Place 10UF near +3V_WLAN_WP1 source side.



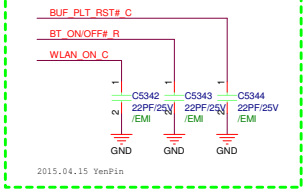
+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 72,74.

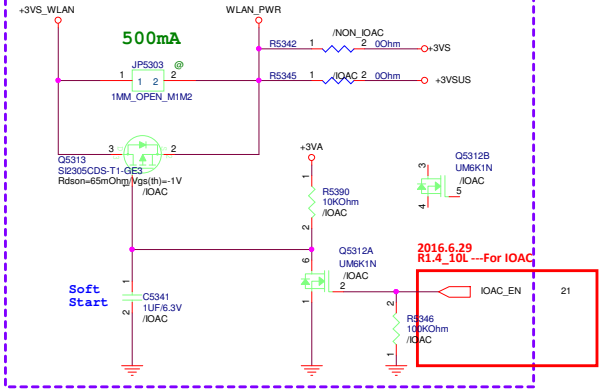
Place 10UF near +3V_WLAN_WP1 source side.



EMI Solution



IOAC Control Schematic



PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : WLAN		
BG1/HW3	Engineer: Andy Kao		
Size: Custom	Project Name: X3		Rev: 1.0
Date: Wednesday, August 31, 2016	Sheet 53 of 97		

PEGATRON

Title : USB HUB

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 54 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

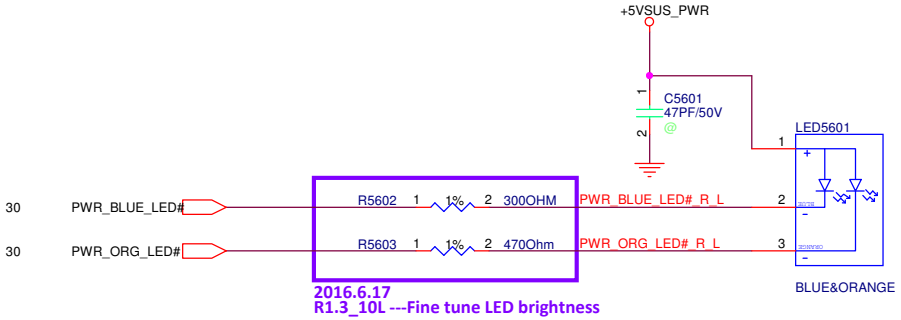
BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

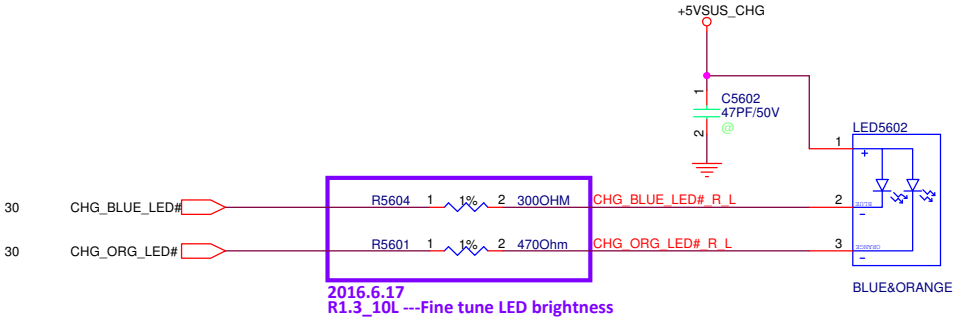
Date: Wednesday, August 31, 2016 Sheet 55 of 97

POWER LED

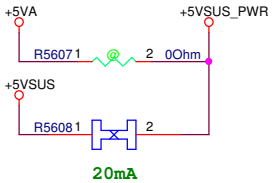


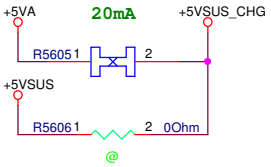
2016.6.17
R1.3_10L ---Fine tune LED brightness

Charger LED



2016.6.17
R1.3_10L ---Fine tune LED brightness





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LED_Indicator

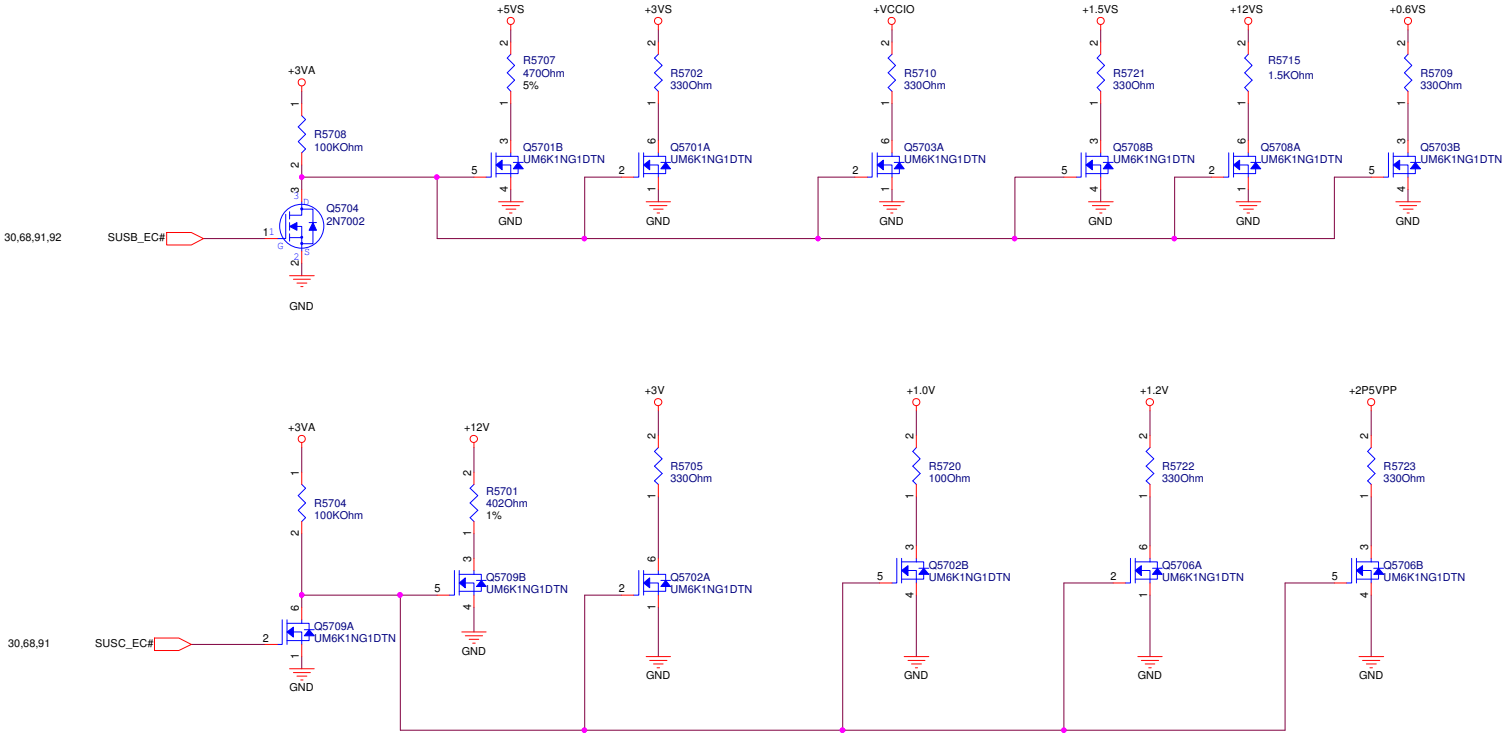
BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 56 of 97

Discharge Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DISCHARGE CKT

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 57 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 58 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

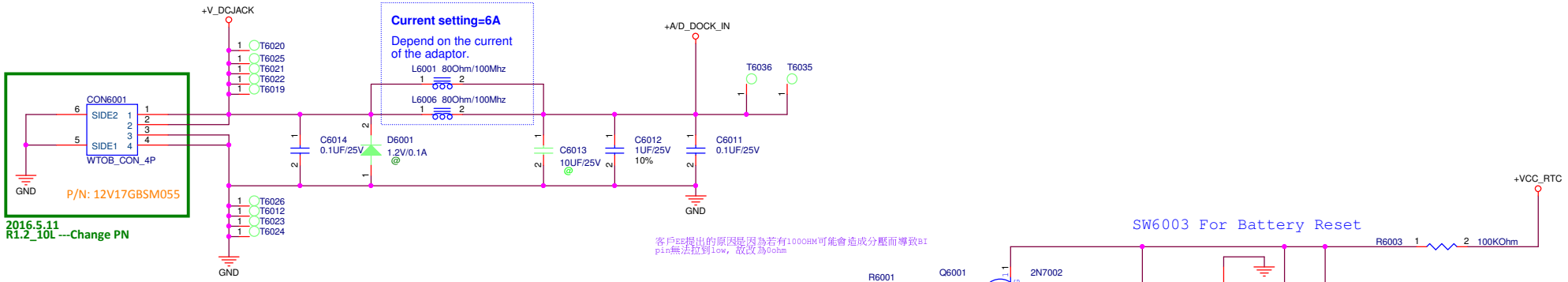
BG1/HW3

Engineer: Andy Kao

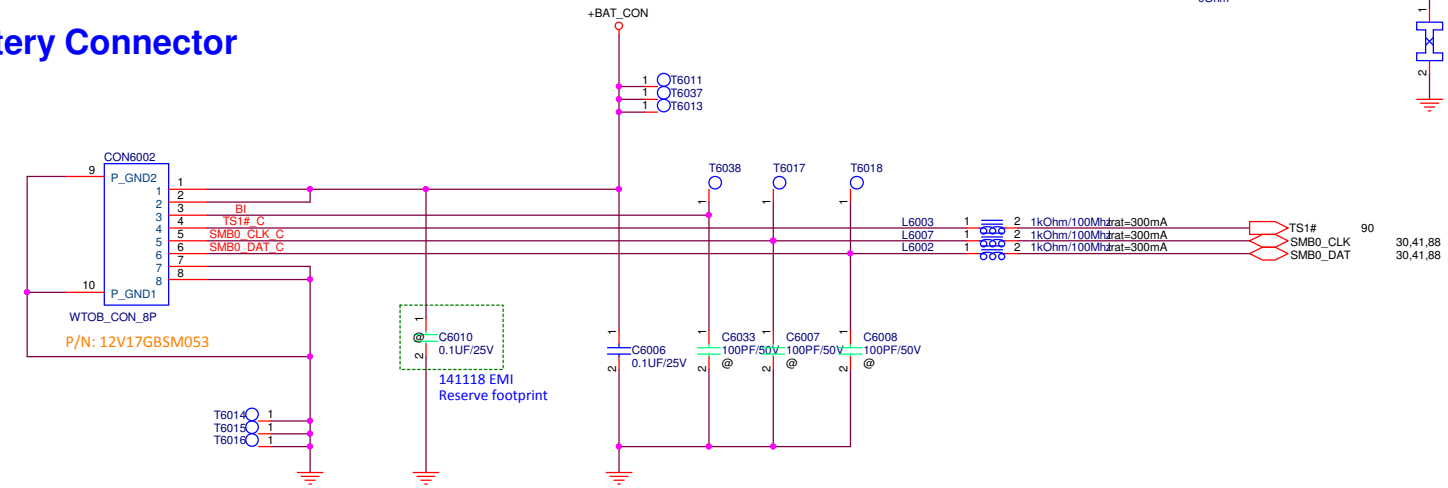
Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 59 of 97

DC Jack WtoB CONN



Battery Connector



PEGATRON	Title : DC_IN/BAT CONN	
BG1/HW3	Engineer: Andy Kao	
Size: Custom	Project Name: X3	Rev: 1.0
Date: Wednesday, August 31, 2016	Sheet 60 of 97	

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

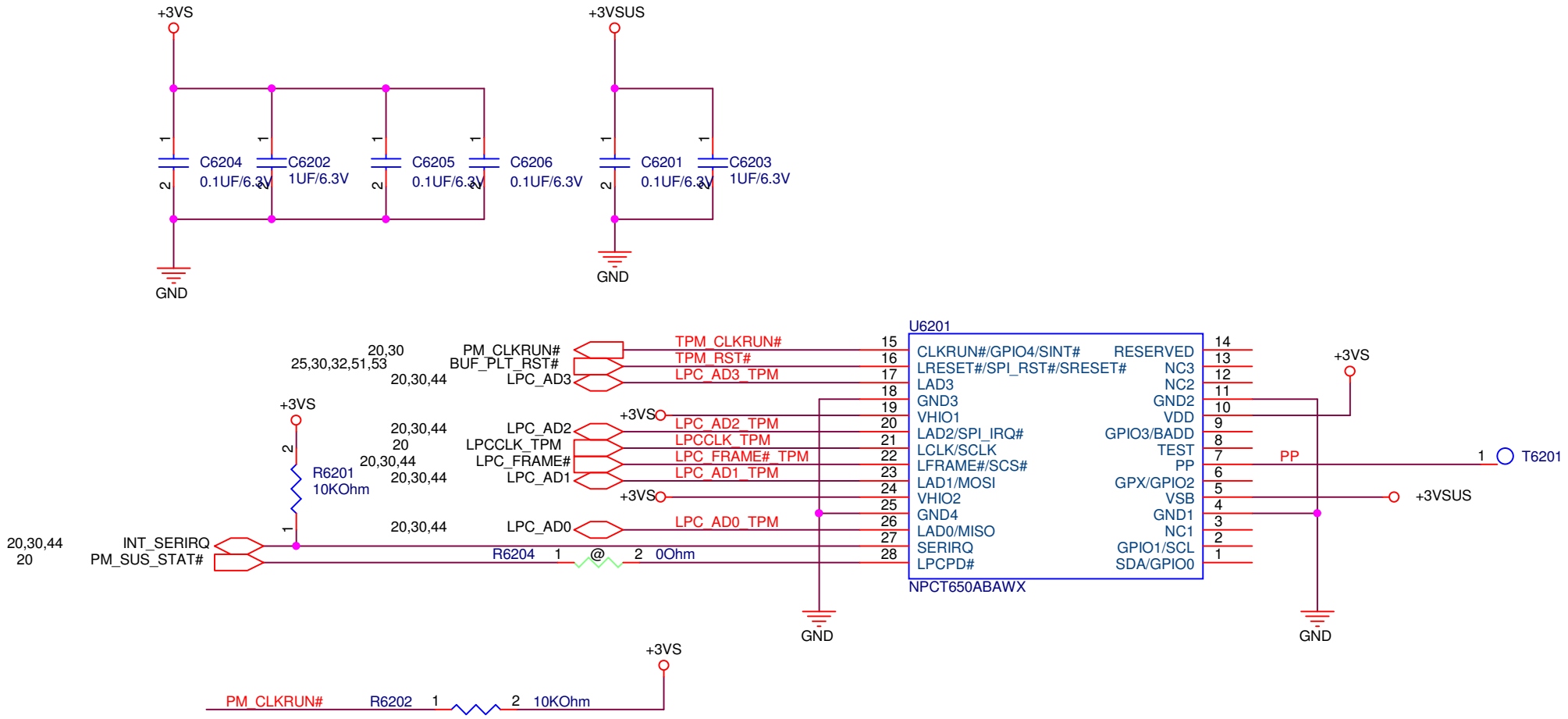
Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 61 of 97



Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

PEGATRON Title : TPM CONN

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 62 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

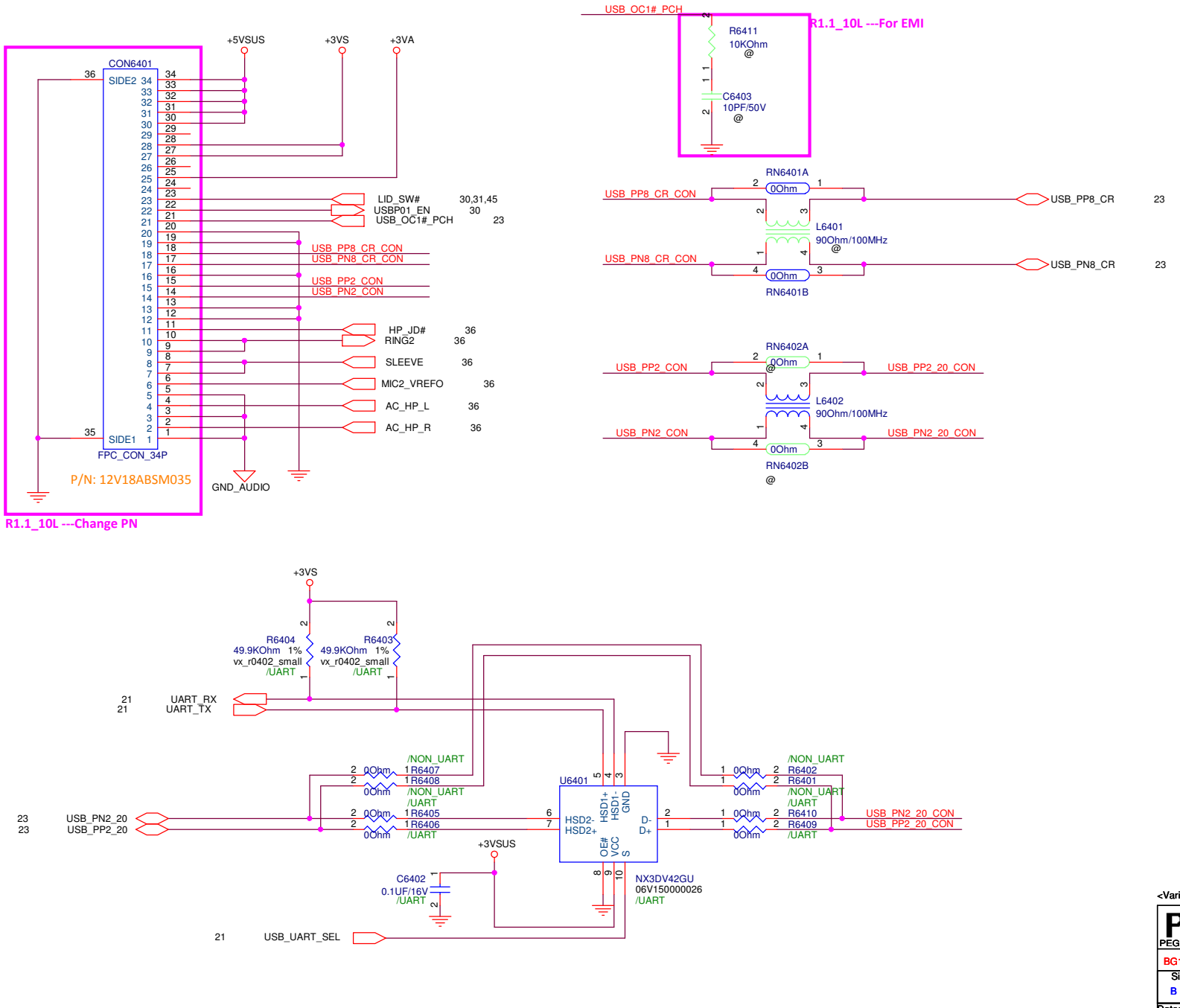
Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 63 of 97



<Variant Name>

PEGATRON Title : IO CON.

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 64 of 97

CPU NUT

H6501 CT264B176D146 GND
H6502 CT264B176D146 GND
H6503 CT264B176D146 GND
H6504 CT264B176D146 GND

6*2.5mm*1

H6545 C43D43N

H6535 C236D98 GND

6*3.1mm*1

H6543 CT236DO63x75 GND

2016.6.6 R1.2_10L ---For ME

CLIP

H6507 H6508 H6509 H6510 H6511
H6512 H6513 H6514 H6515 H6516 H6517 H6518
H6519 H6520 H6522 H6523 H6524 H6525
H6526 H6528 H6529 H6530 H6531 H6532
H6533 H6534

SUL-12A1M GND

2016.5.30
R1.2_10L ---For ME

Thermal screw*2

H6540 SP276D98

1	P_GND		
2	NP_NC1	NP_NC27	28
3	NP_NC2	NP_NC28	29
4	NP_NC3	NP_NC29	30
5	NP_NC4	NP_NC30	31
6	NP_NC5	NP_NC31	32
7	NP_NC6	NP_NC32	33
8	NP_NC7	NP_NC33	34
9	NP_NC8	NP_NC34	35
10	NP_NC9	NP_NC35	36
11	NP_NC10	NP_NC36	37
12	NP_NC11	NP_NC37	38
13	NP_NC12	NP_NC38	39
14	NP_NC13	NP_NC39	40
15	NP_NC14	NP_NC40	41
16	NP_NC15	NP_NC41	42
17	NP_NC16	NP_NC42	43
18	NP_NC17	NP_NC43	44
19	NP_NC18	NP_NC44	45
20	NP_NC19	NP_NC45	46
21	NP_NC20	NP_NC46	47
22	NP_NC21	NP_NC47	48
23	NP_NC22	NP_NC48	49
24	NP_NC23	NP_NC49	50
25	NP_NC24	NP_NC50	51
26	NP_NC25	NP_NC51	52
27	NP_NC26	NP_NC52	53

H6541 SP276D98

1	P_GND		
2	NP_NC1	NP_NC27	28
3	NP_NC2	NP_NC28	29
4	NP_NC3	NP_NC29	30
5	NP_NC4	NP_NC30	31
6	NP_NC5	NP_NC31	32
7	NP_NC6	NP_NC32	33
8	NP_NC7	NP_NC33	34
9	NP_NC8	NP_NC34	35
10	NP_NC9	NP_NC35	36
11	NP_NC10	NP_NC36	37
12	NP_NC11	NP_NC37	38
13	NP_NC12	NP_NC38	39
14	NP_NC13	NP_NC39	40
15	NP_NC14	NP_NC40	41
16	NP_NC15	NP_NC41	42
17	NP_NC16	NP_NC42	43
18	NP_NC17	NP_NC43	44
19	NP_NC18	NP_NC44	45
20	NP_NC19	NP_NC45	46
21	NP_NC20	NP_NC46	47
22	NP_NC21	NP_NC47	48
23	NP_NC22	NP_NC48	49
24	NP_NC23	NP_NC49	50
25	NP_NC24	NP_NC50	51
26	NP_NC25	NP_NC51	52
27	NP_NC26	NP_NC52	53

14*8mm*1

H6544 GND NP_NC D98_DO75X63N GND

2016.6.6 R1.2_10L ---For ME

13.5*8mm*1

H6542 GND NP_NC RT531X315BD98_D63N GND

2016.6.6 R1.2_10L ---For ME

Shielding PAD

H6536 C315D98 GND
H6537 C315D98 GND
H6538 C315D98 GND

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : NUT,Screw Hole

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 65 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 66 of 97

PEGATRON

Title : <Title>

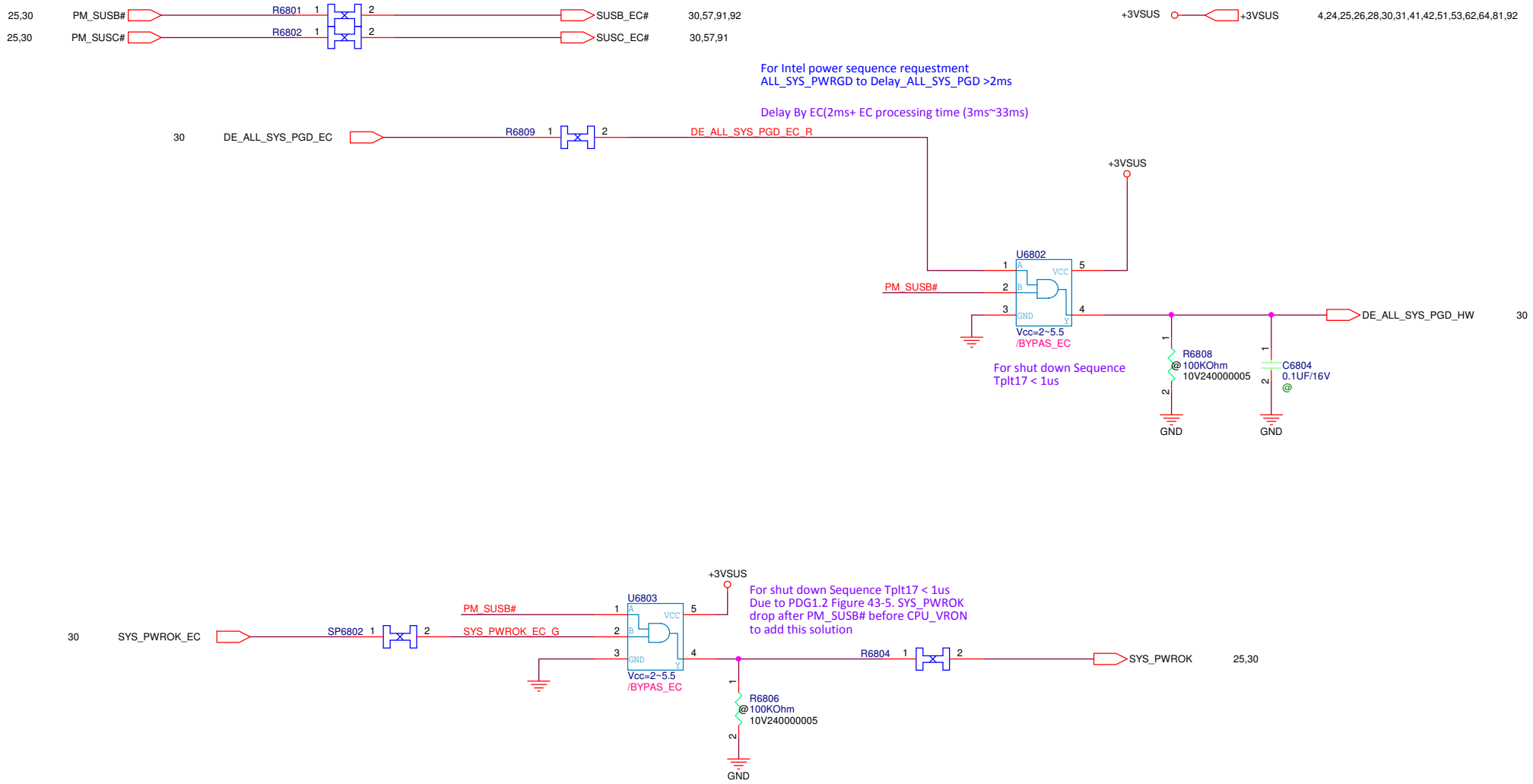
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 67 of 97



PEGATRON Title : POWER Sequence

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 68 of 97

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Power SW Board

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 69 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 70 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 71 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 72 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 73 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 74 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 75 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 76 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 77 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 78 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

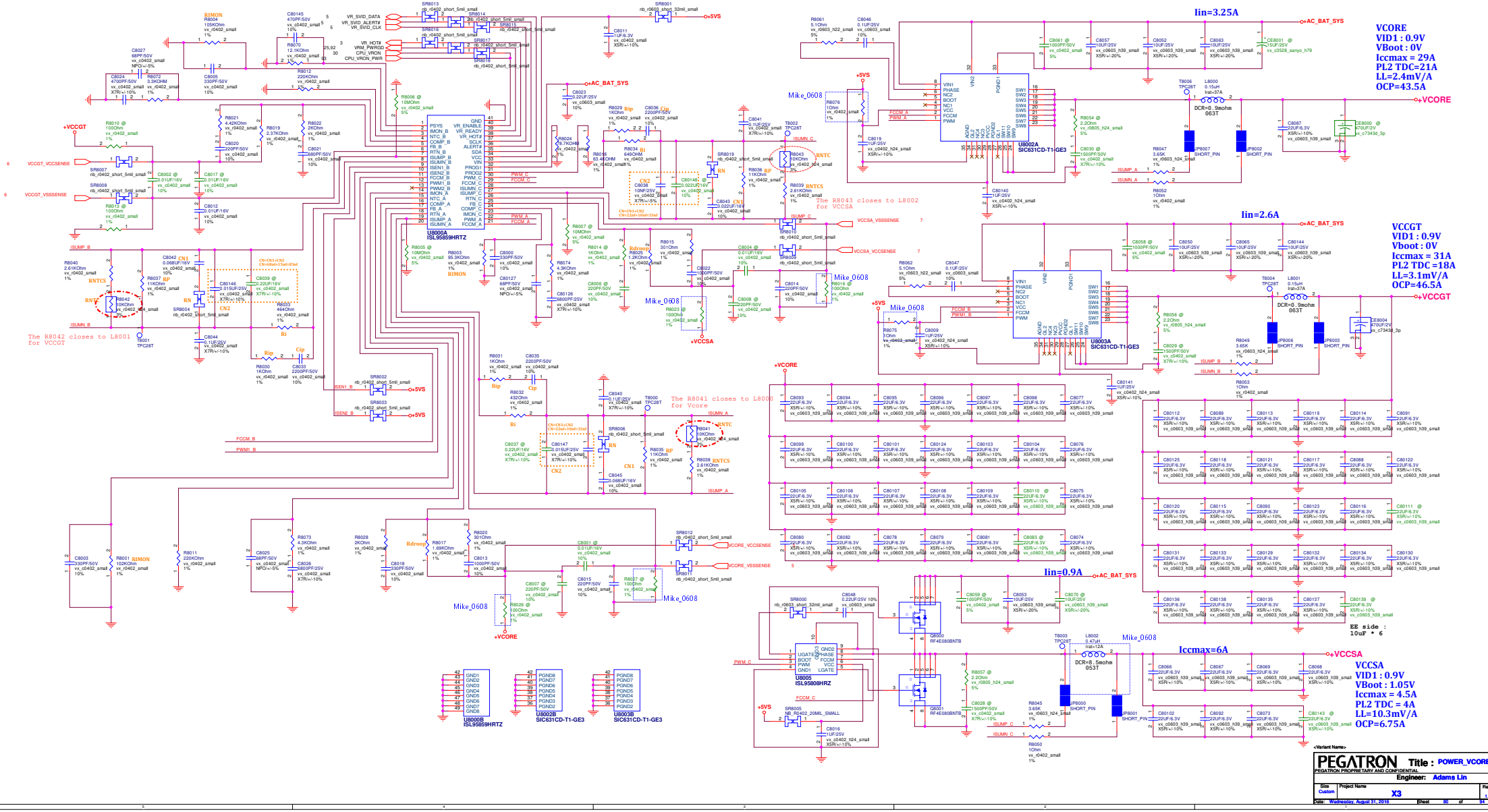
BG1/HW3

Engineer: Andy Kao

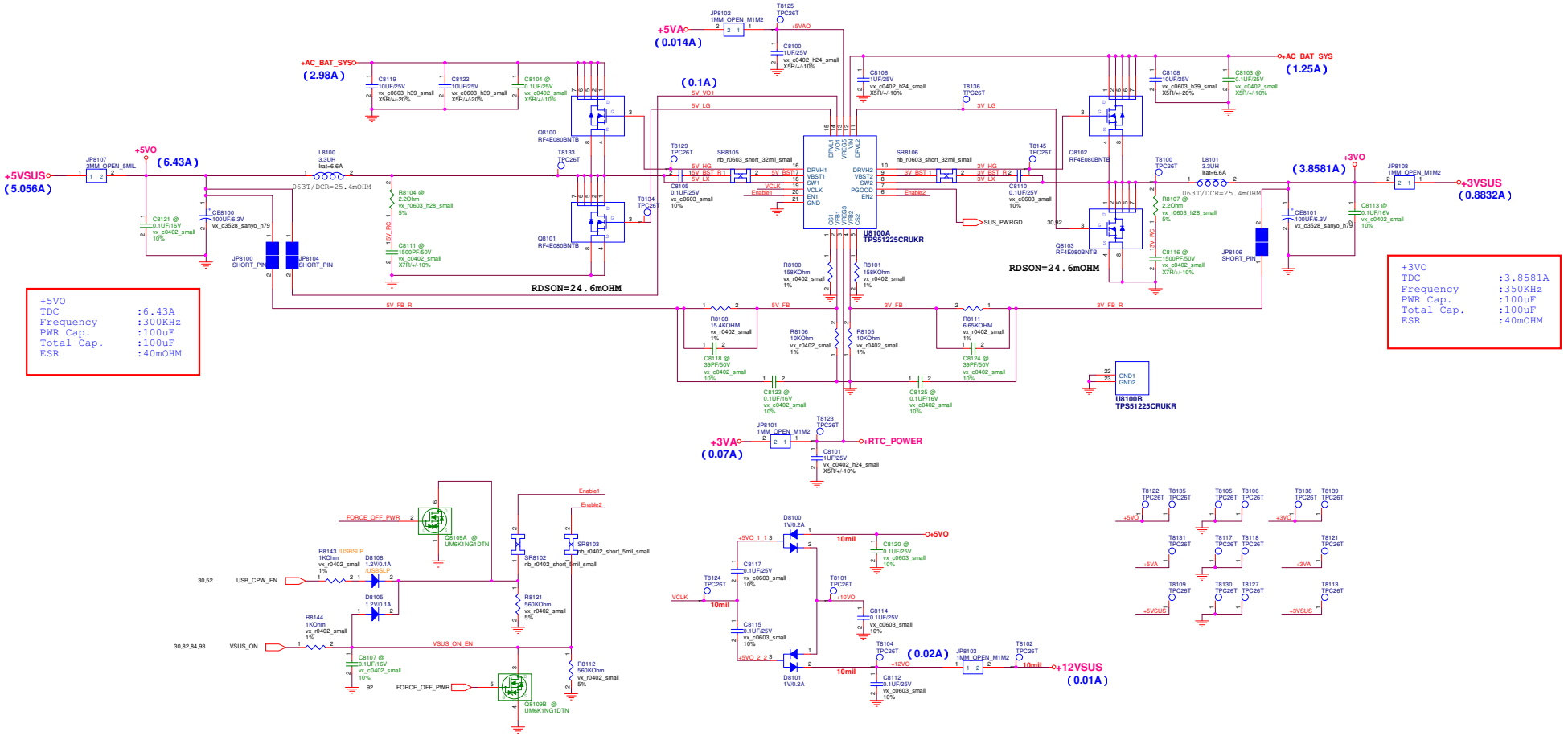
Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 79 of 97

VCORE & VCCGT & VCCSA POWER SUPPLY

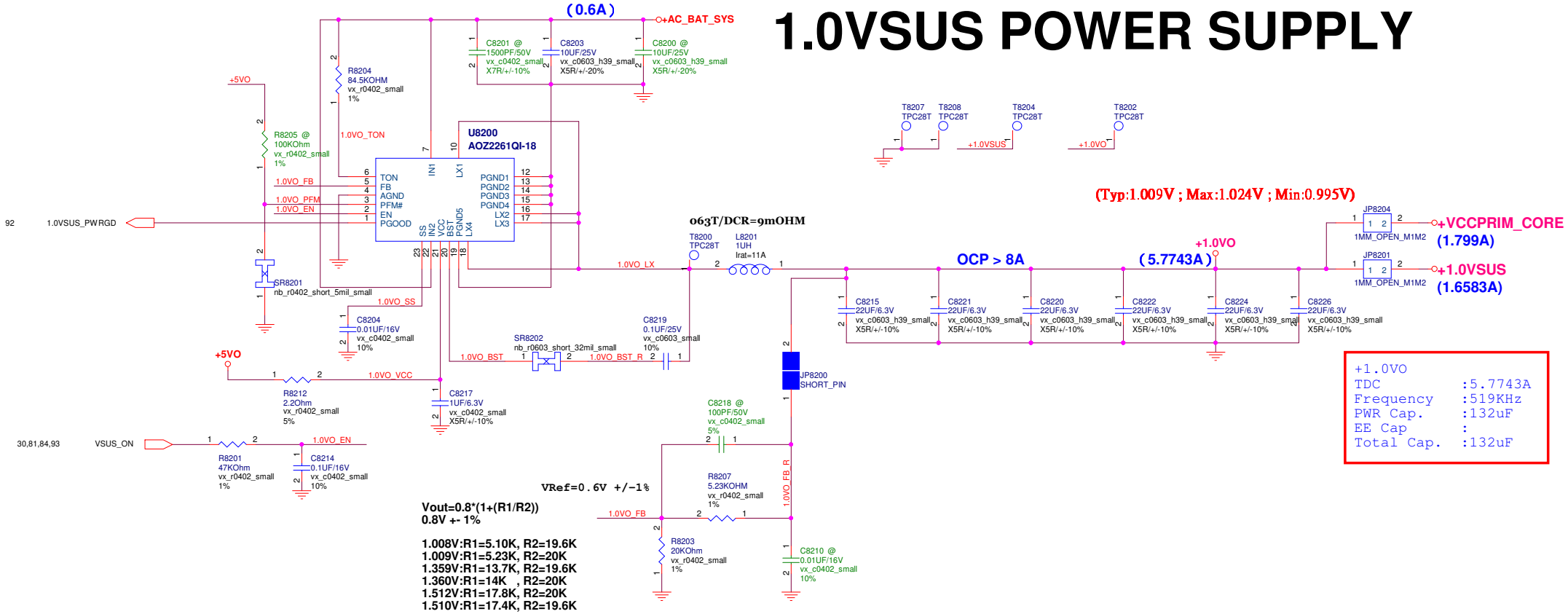


5VO & 3VO POWER SUPPLY



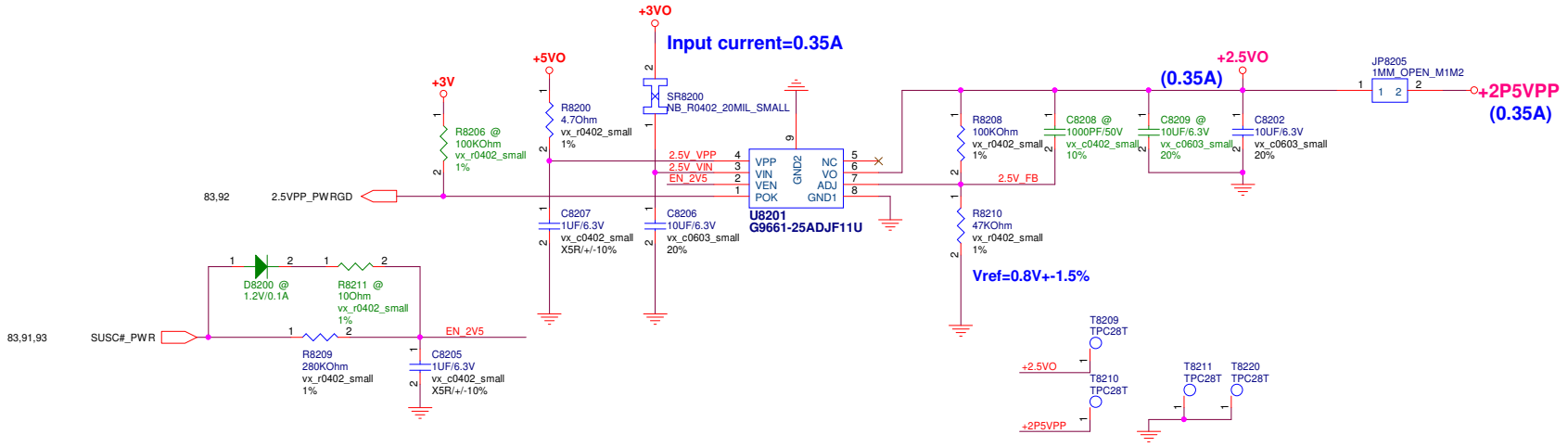
PEGATRON	Title : POWER_SYSTEM
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Adams Lin
BG1-POWER	
Size: Custom	Project Name: X3
Rev: 1.1	
Date: Wednesday, August 31, 2016	Sheet 81 of 94

1.0VSUS POWER SUPPLY



+1.0VO
TDC :5.7743A
Frequency :519KHz
PWR Cap. :132uF
EE Cap :
Total Cap. :132uF

2.5V POWER SUPPLY



+2.5VO
TDC :0.35A
OCP :3A
PWR Cap. :20uF
EE Cap. :10uF
Total Cap. :30uF

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

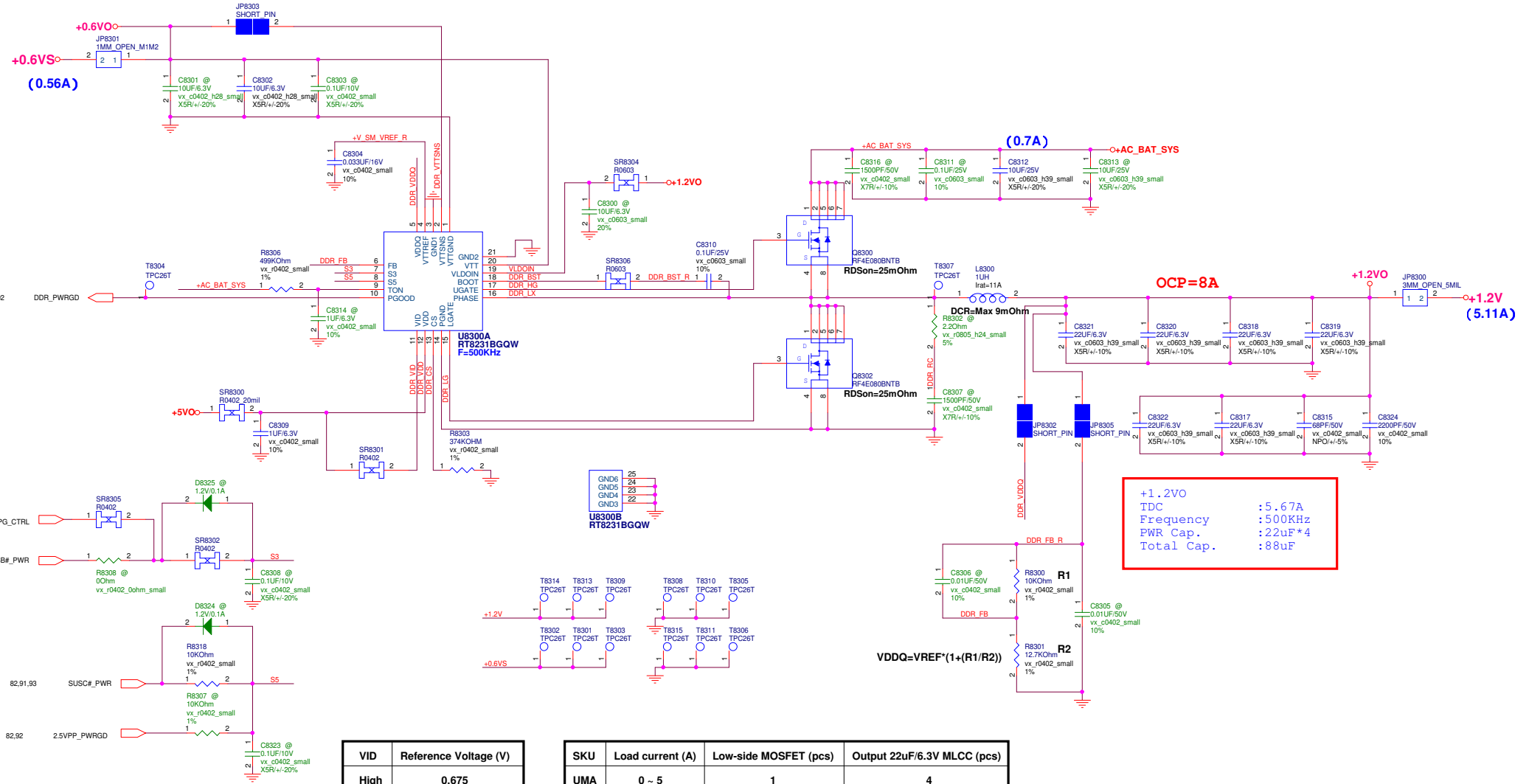
Title : P82_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Wednesday, August 31, 2016 Sheet 82 of 94

DDR & VTT POWER SUPPLY



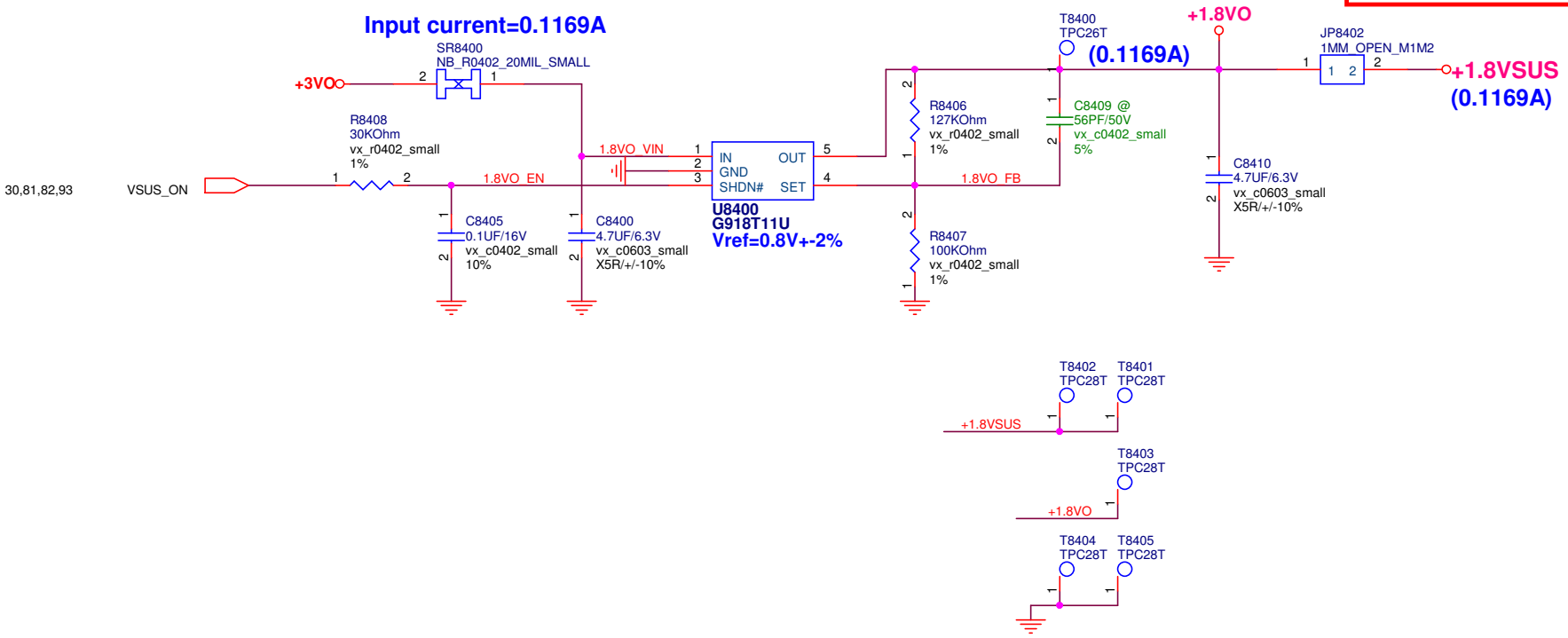
VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_DDR & VTT
Engineer: Adams Lin
BG1-POWER
Size: Custom | Project Name: X3 | Rev: 1.1
Date: Wednesday, August 31, 2016 | Sheet 83 of 94

1.8VSUS POWER SUPPLY

+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

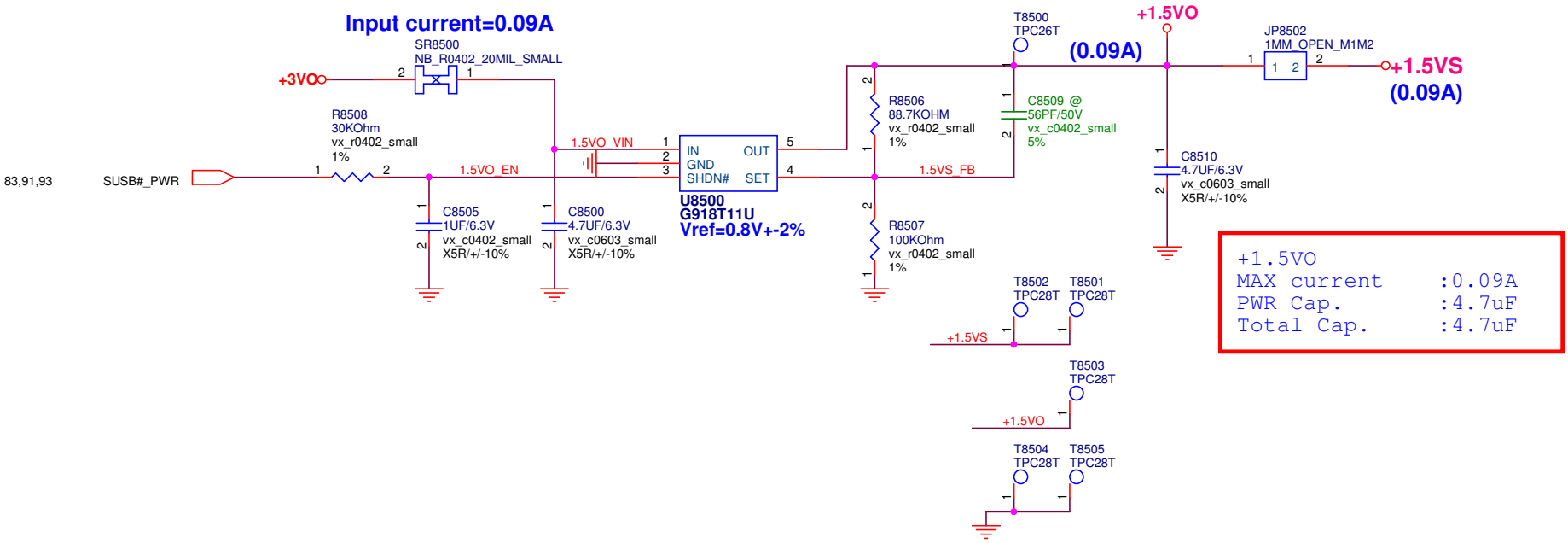
Title : POWER_+1.8VSUS

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Wednesday, August 31, 2016 Sheet 84 of 94

1.5VS POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

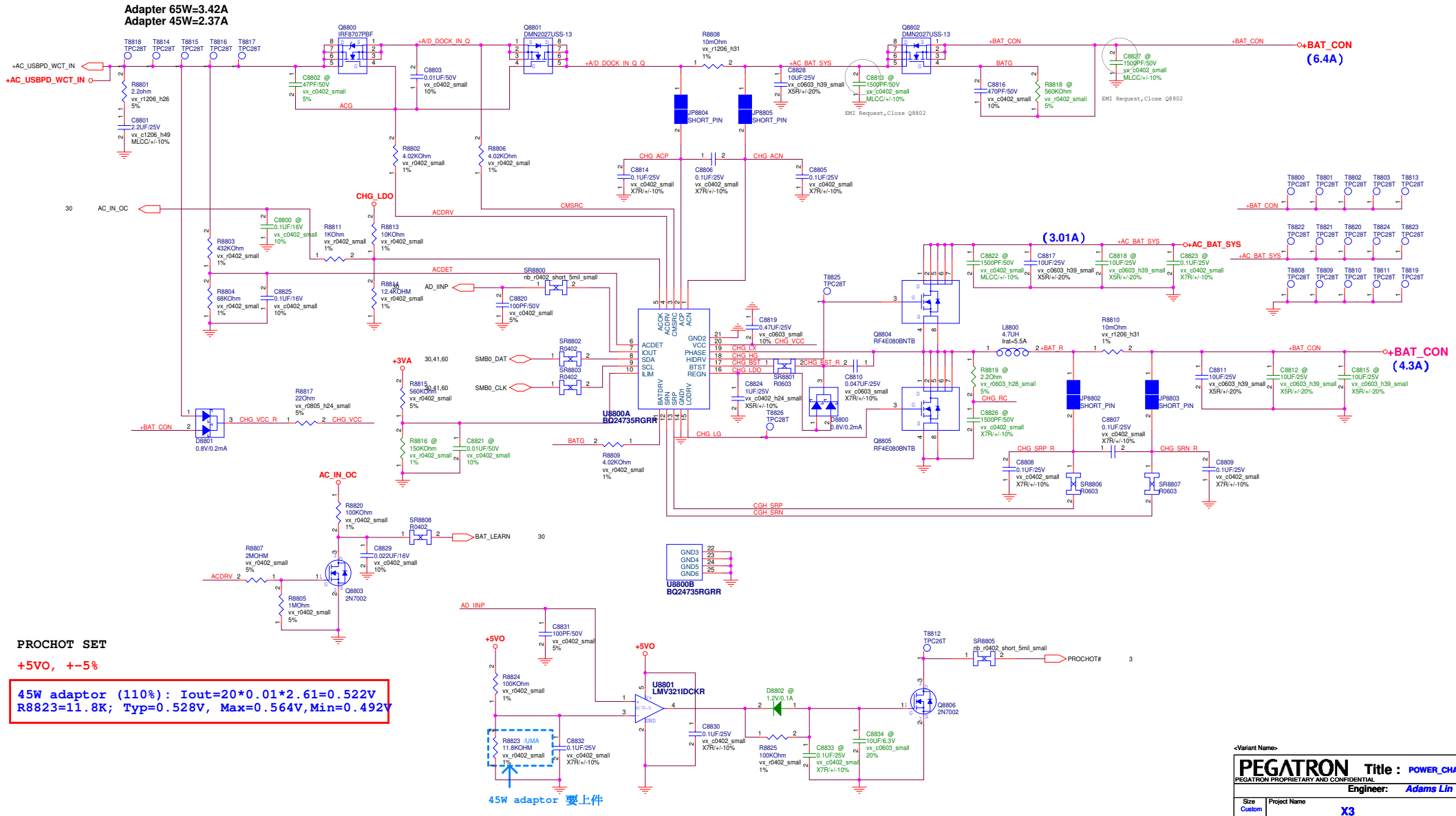
Title : POWER_+1.5VS

Engineer: Adams Lin

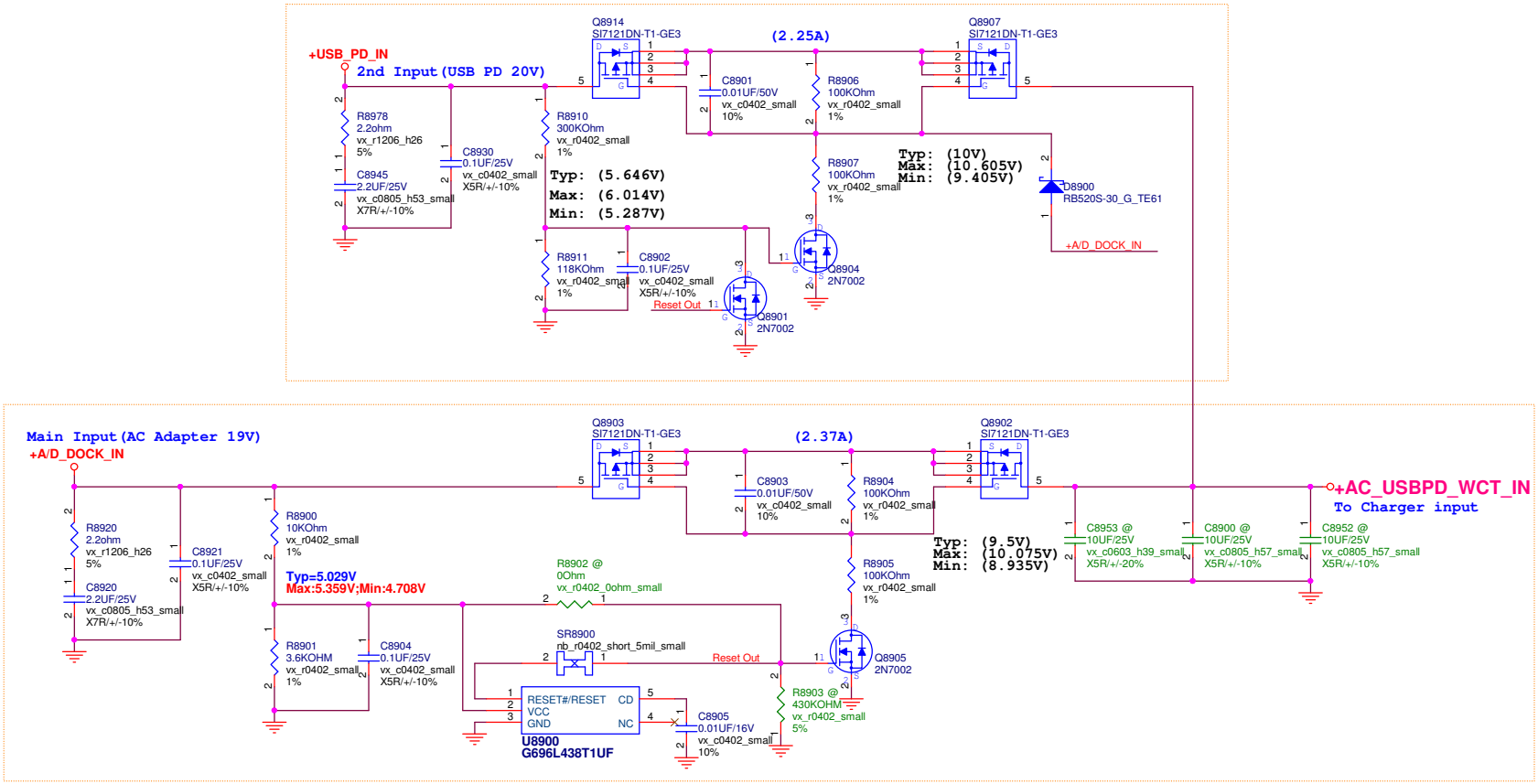
Size	Project Name	Rev
Custom	X3	1.1

Date: Wednesday, August 31, 2016 Sheet 85 of 94

BATTERY CHARGER



2 Input switch Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : AC&PD S.W.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

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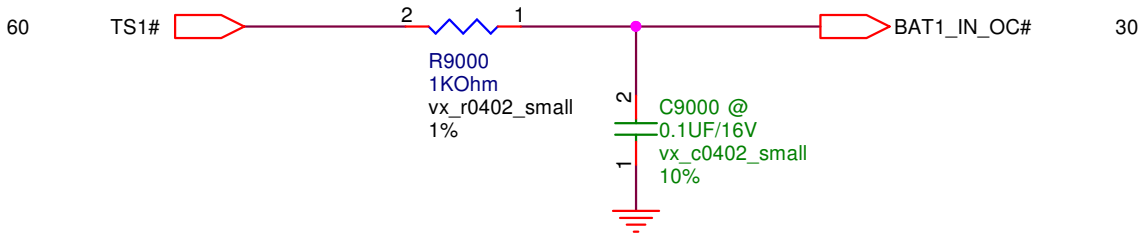
BATTERY IN DETECT



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

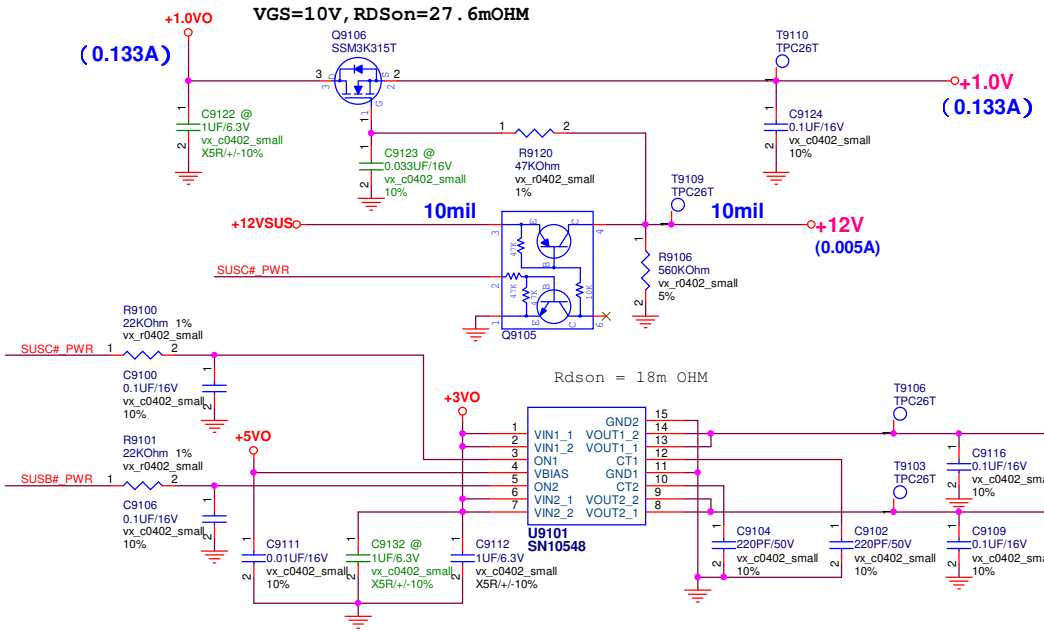
Title : POWER_DETECT

Engineer: Adams Lin

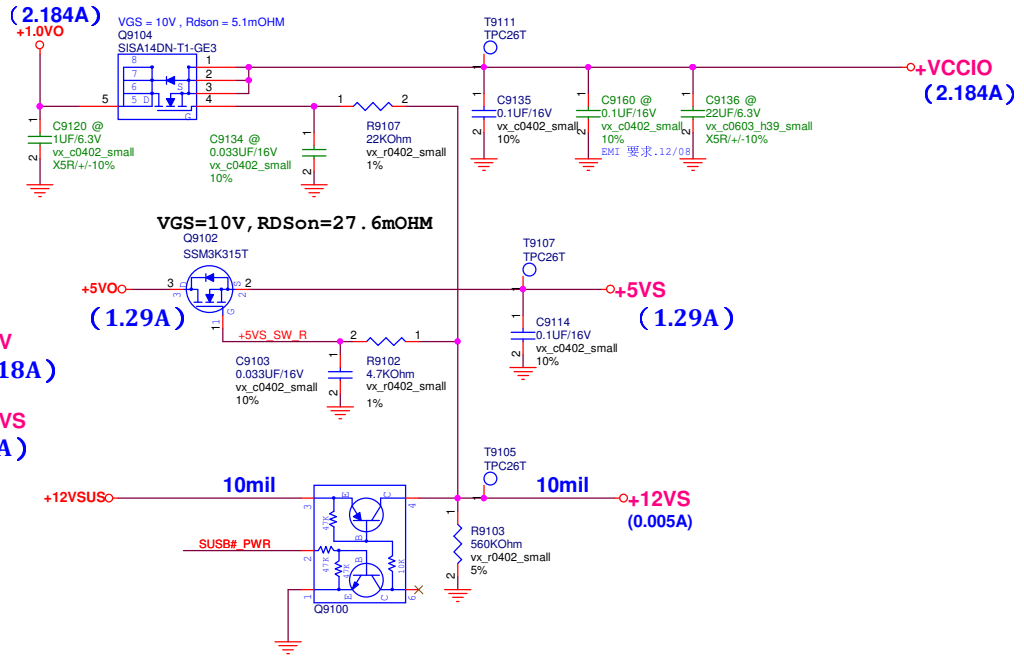
Size	Project Name	Rev
Custom	X3	1.1

Date: Wednesday, August 31, 2016 Sheet 90 of 94

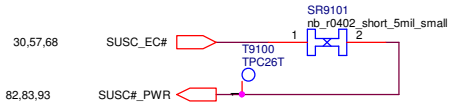
SUSC#_PWR POWER



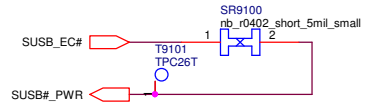
SUSB#_PWR POWER



SUSC#_PWR POWER Control



SUSB#_PWR POWER Control



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

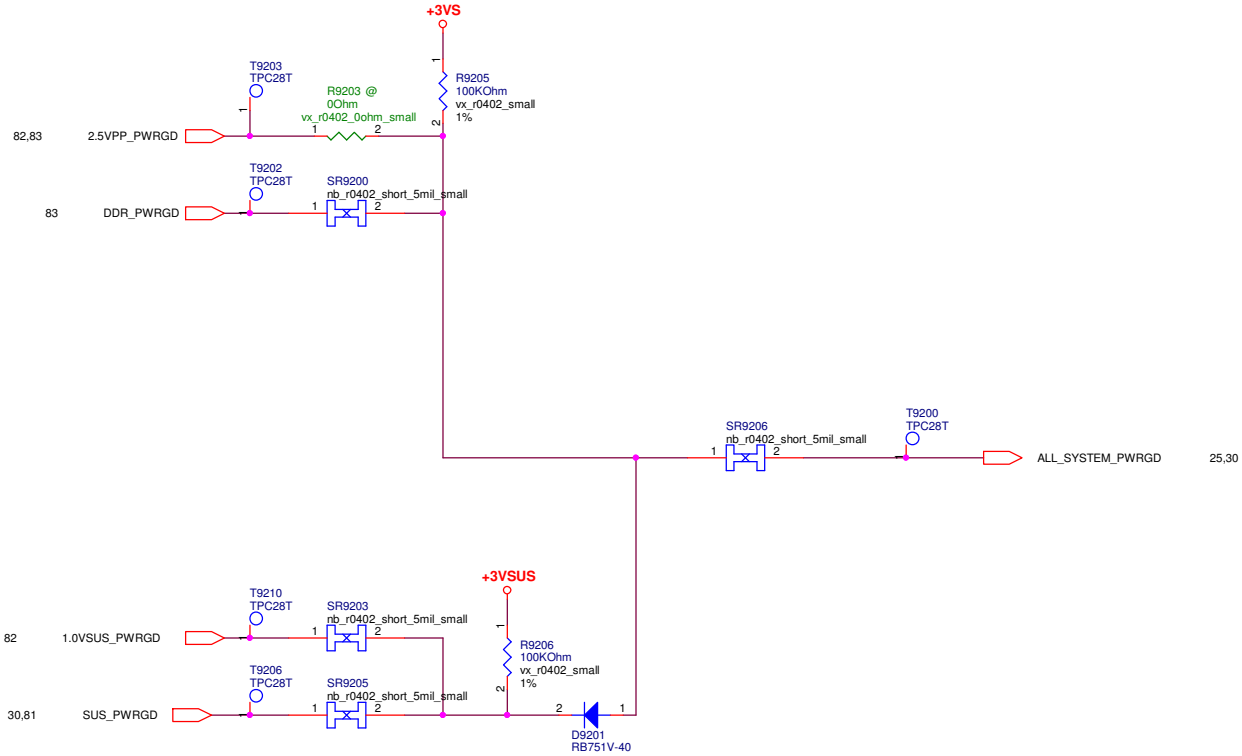
Title : POWER_LOAD SWITCH

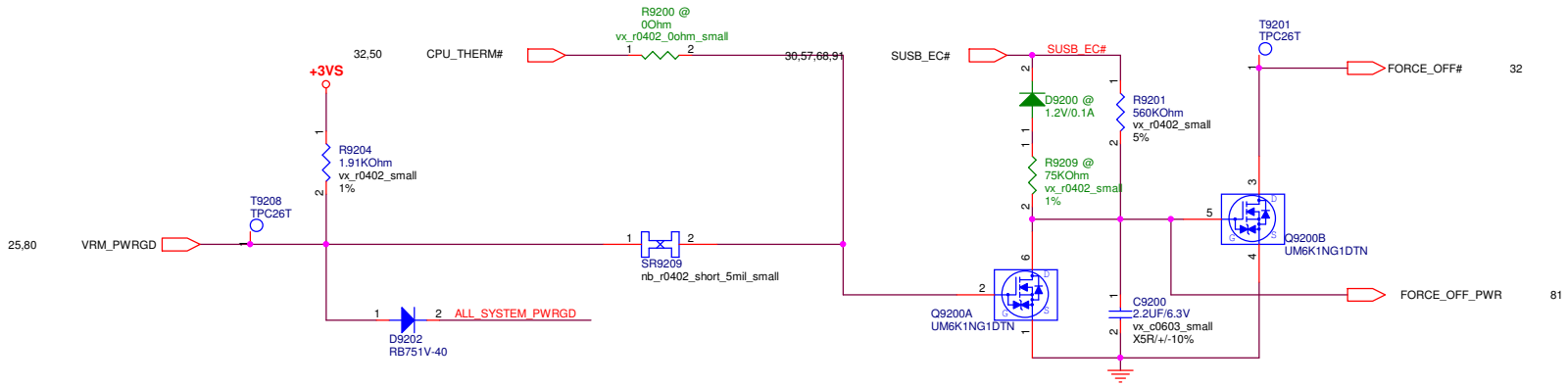
Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Wednesday, August 31, 2016 Sheet 91 of 94

POWER GOOD DETECTER





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

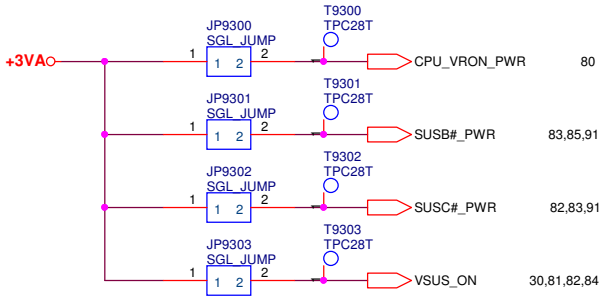
Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Wednesday, August 31, 2016 Sheet 92 of 94

+USB_PD_IN	+USB_PD_IN	42,89
+A/D_DOCK_IN	+A/D_DOCK_IN	60,89
+AC_USBPD_WCT_IN	+AC_USBPD_WCT_IN	88,89
+AC_BAT_SYS	+AC_BAT_SYS	43,45,80,81,82,83,88
+BAT_CON	+BAT_CON	60,88
+RTC_POWER	+RTC_POWER	81
+5VA	+5VA	31,56,81
+3VA	+3VA	24,30,31,36,41,43,53,57,64,81,88
+5VO	+5VO	26,81,82,83,88,91
+3VO	+3VO	81,82,84,85,91
+2.5VO	+2.5VO	82
+1.8VO	+1.8VO	84
+1.2VO	+1.2VO	83
+1.0VO	+1.0VO	82,91
+0.6VO	+0.6VO	83
+12VSUS	+12VSUS	28,81,91
+5VSUS	+5VSUS	41,42,52,56,64,81
+3VSUS	+3VSUS	4,24,25,26,28,30,31,41,42,51,53,62,64,68,81,92
+1.8VSUS	+1.8VSUS	9,21,22,26,84
+1.0VSUS	+1.0VSUS	26,82
+12V	+12V	57,91
+2P5VPP	+2P5VPP	16,17,57,82
+1.2V	+1.2V	4,7,15,16,17,19,57,83
+1.0V	+1.0V	7,57,91
+12VS	+12VS	31,48,57,91
+5VS	+5VS	31,36,45,48,50,51,57,80,91
+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+0.6VS	+0.6VS	15,57,83
+VCORE	+VCORE	5,80
+VCCGT	+VCCGT	6,80
+VCCSA	+VCCSA	7,80
+VCCIO	+VCCIO	3,7,9,57,91
+VCCPRIM_CORE	+VCCPRIM_CORE	26,82

FOR POWER TEST



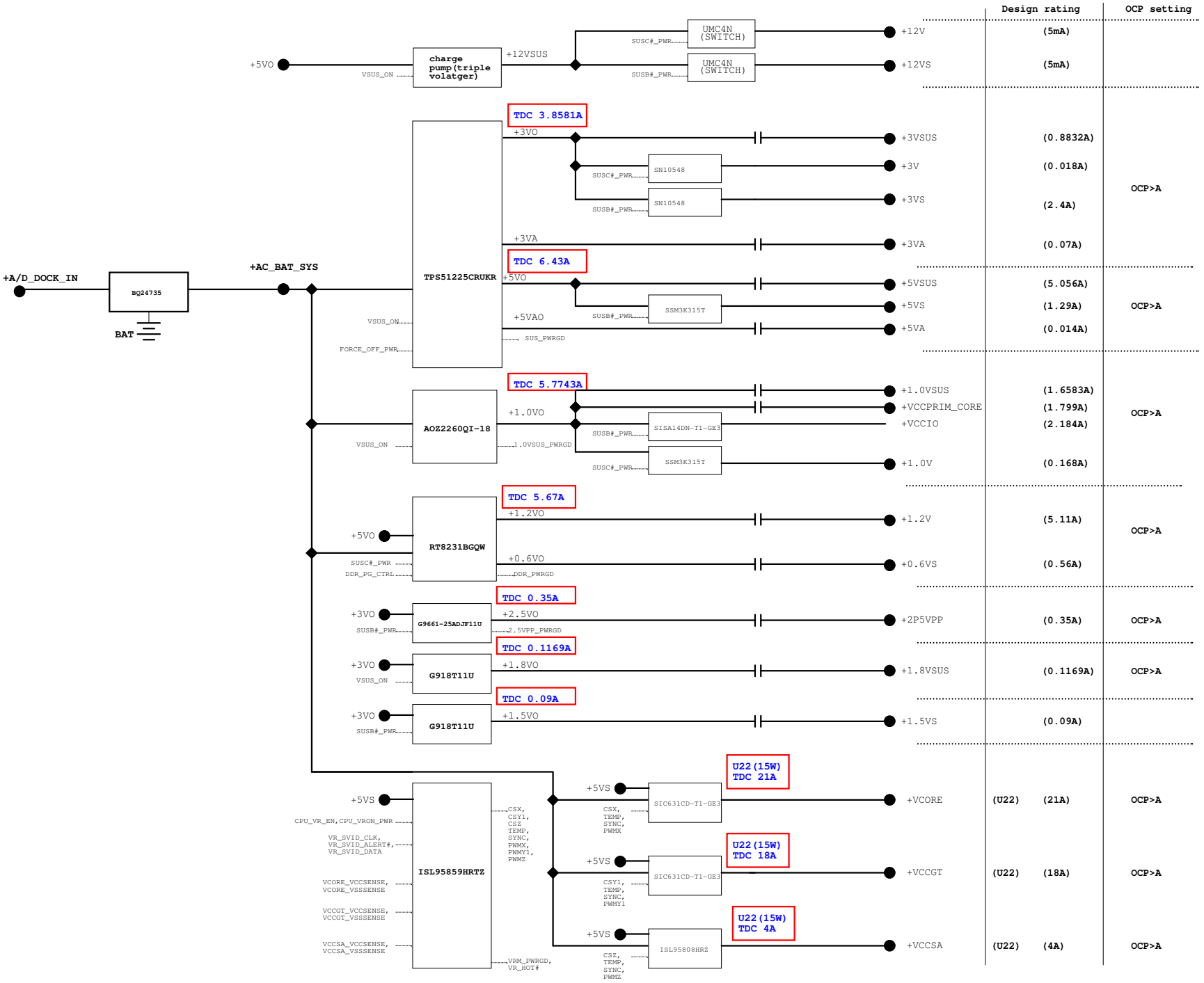
PEGATRON Title : POWER_SIGNAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-POWER Engineer: Adams Lin

Size	Project Name	Rev
B	X3	1.1

Date: Wednesday, August 31, 2016 Sheet 93 of 94



<Variant Name>

PEGATRON Title : POWER_FLOWCHART

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

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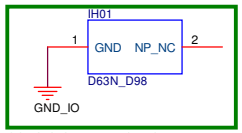
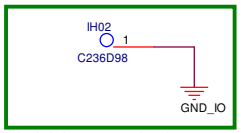


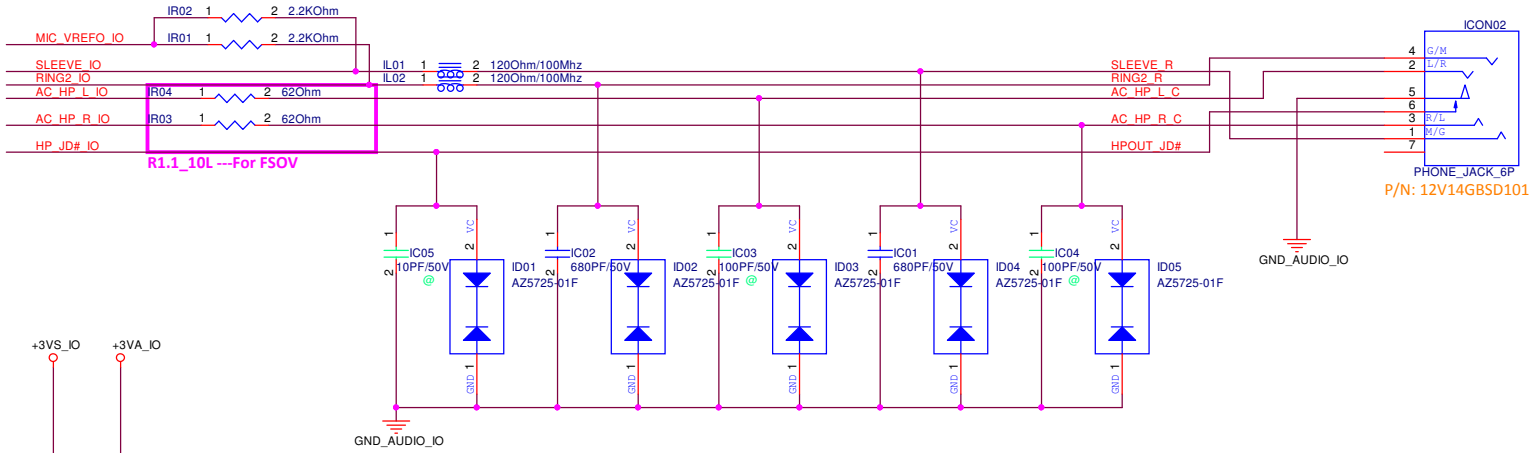
2016.6.6 R1.2_10L ---For ME

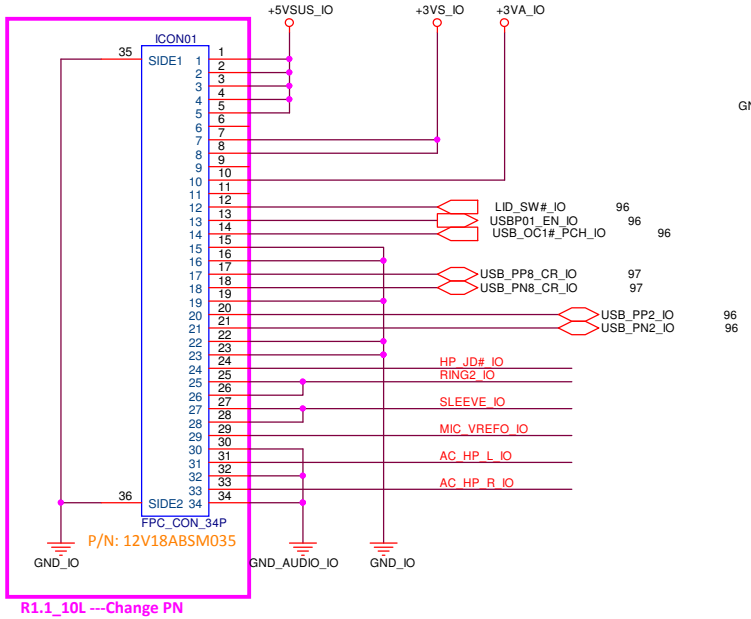


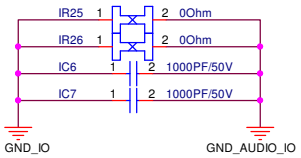
2016.6.6 R1.2_10L ---For ME

2016.7.14 R1.2_10L ---For ME

AUDIO JACK







PEGATRON Title : AUD(2)_SPK/JACK/DMIC

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
A3	X3	1.0

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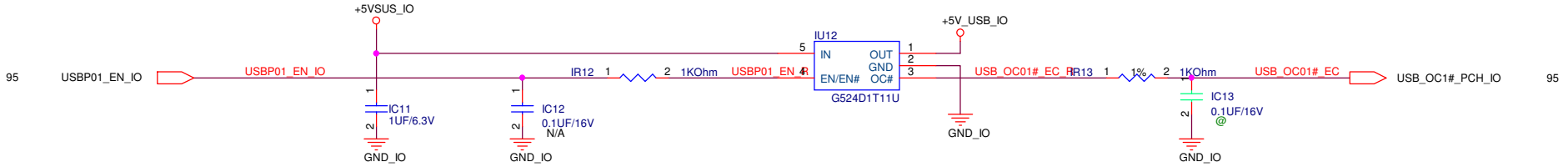
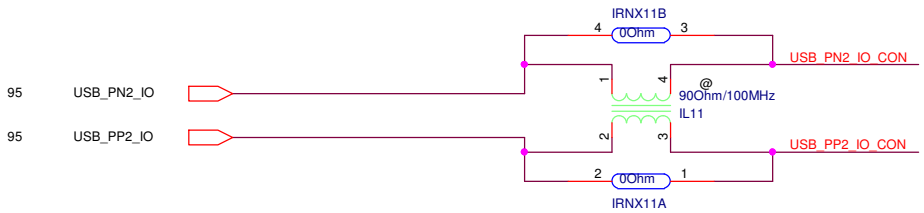
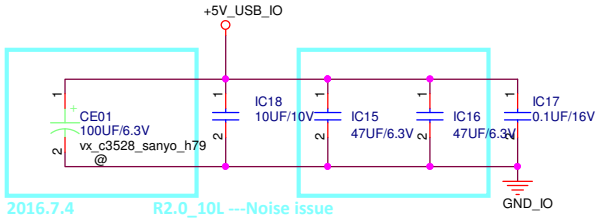
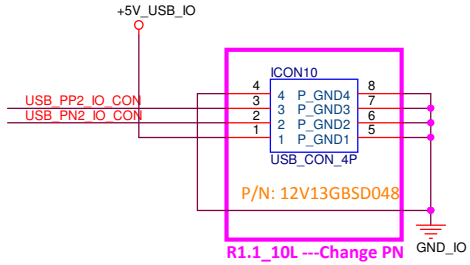
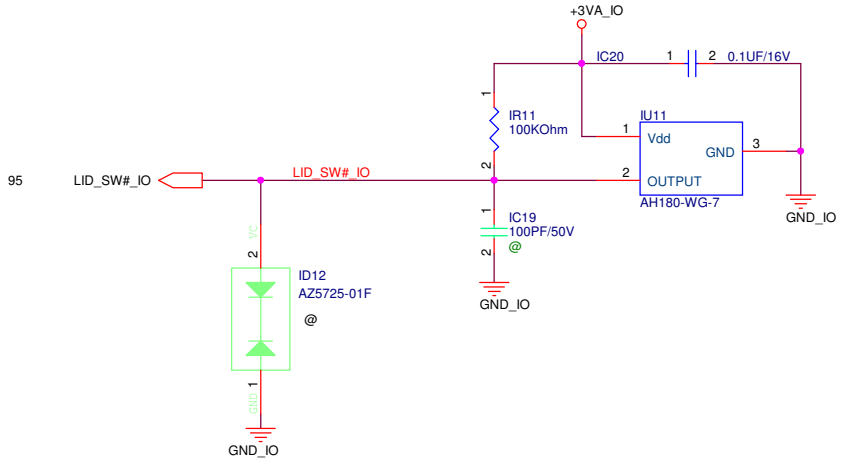


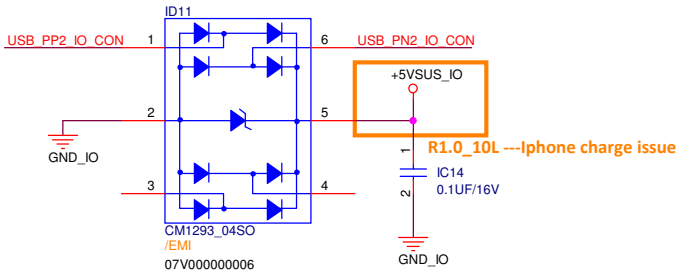


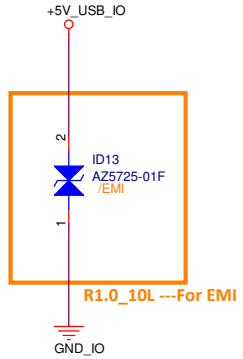






PLACE ESD Diodes near USB Connector





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB30_IO_CONN

Engineer: *Andy Kao*

BG1/HW3

Size	Project Name	Rev
B	X3	1.0

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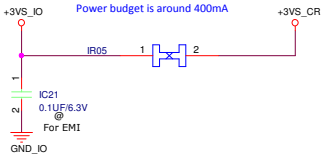
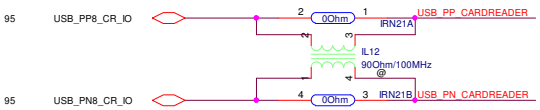
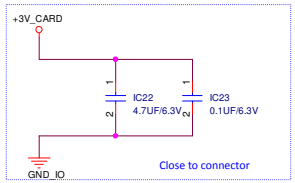
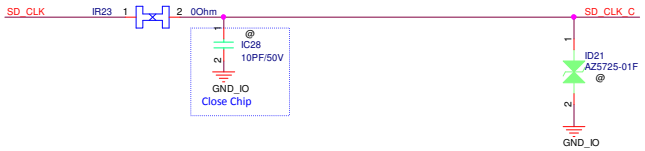
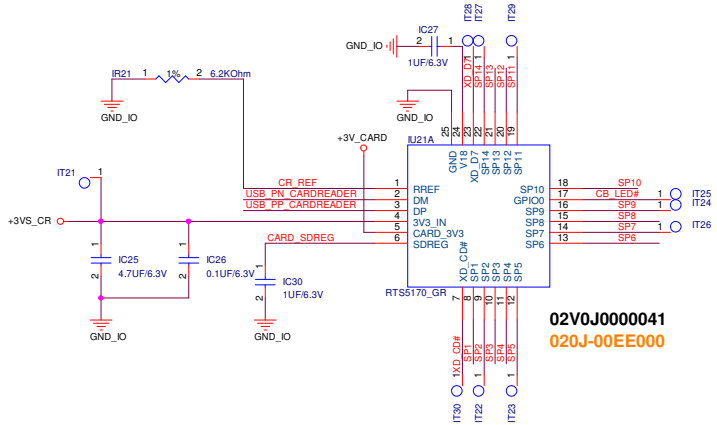
Cardreader

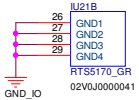


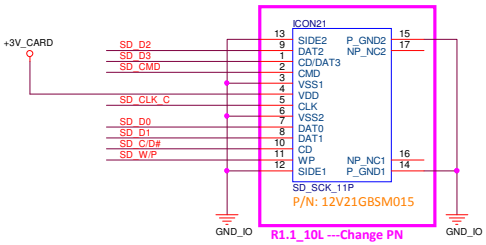












RTS5170-GR Share Pin Assignment

SP1	SD_W/P
SP3	SD_D1
SP4	SD_D0
SP6	SD_C/D#
SP8	SD_CLK
SP10	SD_CMD
SP12	SD_D3
SP13	SD_D2

<Variant Name>

PEGATRON Title : RTS5138-GR

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

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