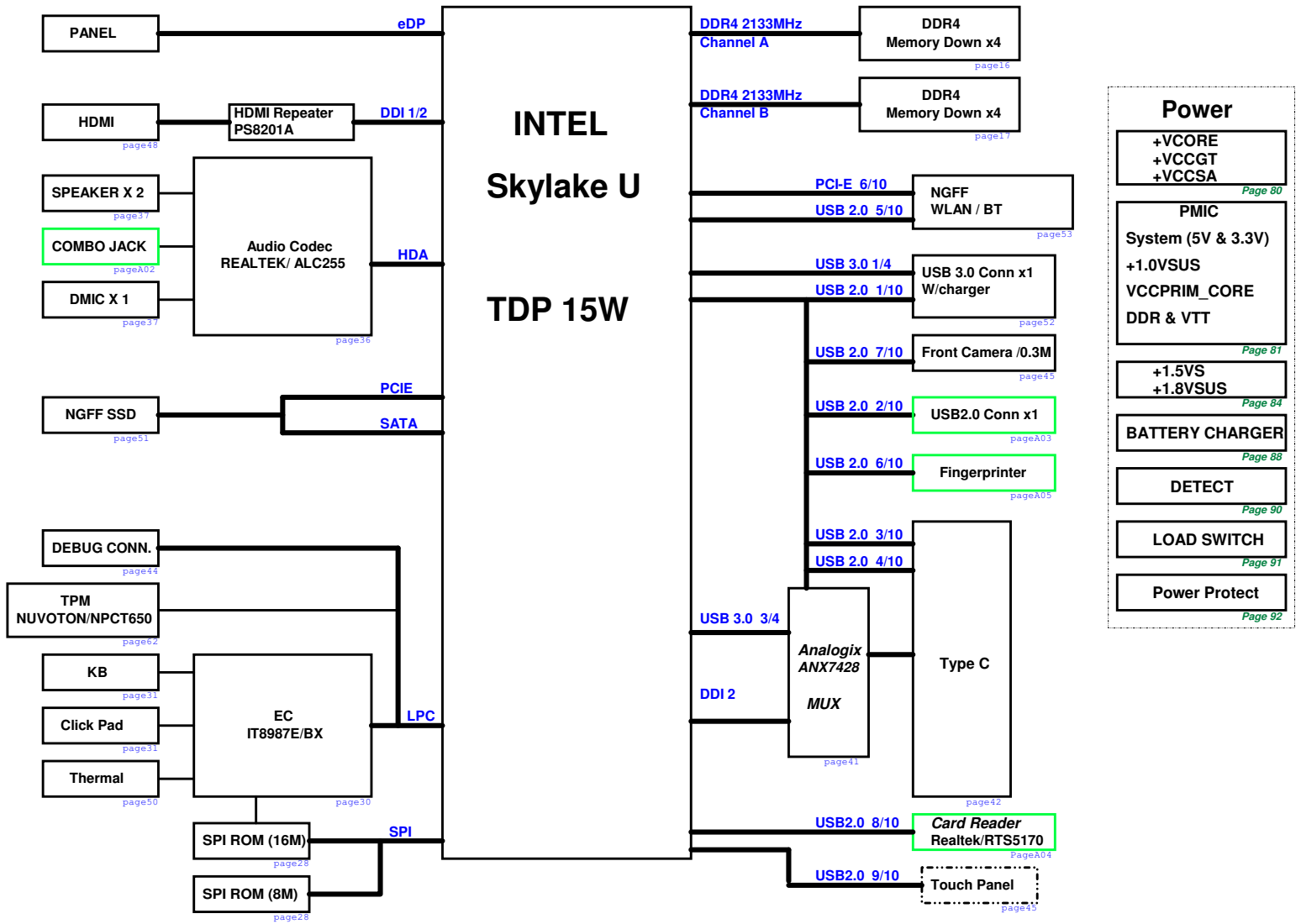
SYSTEM PAGE REF.

14" Cassiopeia (X3) for Skylake U Platform Block Diagram



Discharge Circuit — Page 57

DC & BATT. Conn. — Page 60

Reset Circuit — Page 32

Skew Holes — Page 65

<Variant Name>

PEGATRON Title : Block Diagram

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 1 of 97

EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name

EC GPIO	Use As	Signal Name

EC GPIO	Use As	Signal Name

PEGATRON Title : GPIO Setting

BG1/HW3 Engineer: *Andy Kao*

Size	Project Name	Rev
C	X3	1.0

Date: Monday, July 11, 2016 Sheet 2 of 97

+VCCIO — +VCCIO 7,9,57,91
+VCCST_CPU — +VCCST_CPU 5,7,9,25,32
+VCCSTG — +VCCSTG 5,7
+3VS — +3VS 4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92

SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

U0301A

DDI Port 1: HDMI
47 DDI1_TXN2 — E55 DDI1_TXN[0]
47 DDI1_TXP2 — F55 DDI1_TXP[0]
47 DDI1_TXN1 — E58 DDI1_TXN[1]
47 DDI1_TXP1 — F58 DDI1_TXP[1]
47 DDI1_TXN0 — G53 DDI1_TXN[2]
47 DDI1_TXP0 — F56 DDI1_TXP[2]
47 DDI1_CLKN — G56 DDI1_TXN[3]
47 DDI1_CLKP — DDI1_TXP[3]

DDI Port 2: TYPE-C DP
41 DDI2_TXN0 — C50 DDI2_TXN[0]
41 DDI2_TXP0 — D50 DDI2_TXP[0]
41 DDI2_TXN1 — C52 DDI2_TXN[1]
41 DDI2_TXP1 — D52 DDI2_TXP[1]
41 DDI2_TXN2 — A50 DDI2_TXN[2]
41 DDI2_TXP2 — B50 DDI2_TXP[2]
41 DDI2_TXN3 — D51 DDI2_TXN[3]
41 DDI2_TXP3 — C51 DDI2_TXP[3]

DDI — DISPLAY SIDEBANDS

47 DDPB_CTRLCLK — L13 GPP_E18/DDPB_CTRLCLK
47 DDPB_CTRLDATA — L12 GPP_E19/DDPB_CTRLDATA
DDPC_CTRLCLK — N7 GPP_E20/DDPC_CTRLCLK
DDPC_CTRLDATA — N8 GPP_E21/DDPC_CTRLDATA
N11 GPP_E22
N12 GPP_E23
+VCCIO — R0301 2 1% 1 24.9Ohm DP_COMP — E52 eDP_RCOMP

940432
01V010000015

EDP
EDP_TXN[0] — C47 — EDP_TXN0 45
EDP_TXP[0] — C46 — EDP_TXP0 45
EDP_TXN[1] — D46 — EDP_TXN1 45
EDP_TXP[1] — C45 — EDP_TXP1 45
EDP_TXN[2] — A45 — EDP_TXN2 45
EDP_TXP[2] — B45 — EDP_TXP2 45
EDP_TXN[3] — A47 — EDP_TXN3 45
EDP_TXP[3] — B47 — EDP_TXP3 45
EDP_AUXN — E45 — EDP_AUXN 45
EDP_AUXP — F45 — EDP_AUXP 45
EDP_DISP_UTIL — B52

eDP x 4
-- WQHD 4 Lane
-- FHD 2 Lane

DDI1_AUXN — G50
DDI1_AUXP — F50
DDI2_AUXN — E48 — DDI2_AUXN 41
DDI2_AUXP — F48 — DDI2_AUXP 41
RSVD_1 — G46
RSVD_2 — F46

GPP_E13/DDPB_HPD0 — L9 — DDI1_HPD 47
GPP_E14/DDPC_HPD1 — L7 — DDI2_HPD 41
GPP_E15/DDPD_HPD2 — L6 EXT_SMI# R R0302 1 — 2 0Ohm EXT_SMI# — EXT_SMI# 30,44
GPP_E16/DDPE_HPD3 — N9 EXT_SCI# R R0303 1 — 2 0Ohm EXT_SCI# — EXT_SCI# 30
GPP_E17/EDP_HPD — L10 eDP_HPD — eDP_HPD 45

Pull down at connector side

eDP_BKLTEN — R12 — LCD_BKLTEN_PCH 21,45
eDP_BKLTCTL — R11 — LCD_BL_PWM_PCH 45
eDP_VDDEN — U13 — EDP_VDD_EN 45

DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
1 : port is detected

+3VS
DDPB_CTRLDATA R0304 1 @ 2 2.2KOhm
DDPB_CTRLCLK R0338 1 @ 2 2.2KOhm

+3VS
EXT_SCI# R0307 1 2 10KOhm
EXT_SMI# R0308 1 2 10KOhm

DDPC_HPD
DP: 100Kohm pull down on PCH Side
HDMI: 20Kohm pull down
DDI2_HPD R0337 1 2 100KOhm

+3VS
DDPC_CTRLDATA R0342 1 2 2.2KOhm
DDPC_CTRLCLK R0343 1 2 2.2KOhm

R1.0_10L ---Enable DP port

+VCCST_CPU — R0311 1KOhm
+VCCSTG — R0312 1KOhm 5%
141024 follow PDG V1.0 Table 10-4
Rpu = 1K ohm 5%
Rs = 500 ohm 5%
Closer EC
+VCCST_CPU — R0313 49.9Ohm 1% @

32 H_THRMTRIP# — H_PROCHOT# — R0314 1 30 2 499Ohm — H_PECI_EC
R0315 1 5% 2 43Ohm — TP_CATERR# R — H_PECI
PROCHOT# R
SP0301 1 2 — H_THRMTRIP# R
T0306 1 — SKTOCC#

U0301D

CATERR# — D63 — TP_CATERR# R
PECI — A54 — H_PECI
PROCHOT# — C65 — PROCHOT# R
THERMTRIP# — C63 — H_THRMTRIP# R
SKTOCC# — A65 — SKTOCC#

CPU MISC
BPM#[0] — C55
BPM#[1] — D55
BPM#[2] — B54
BPM#[3] — C56

GPP_E3/CPU_GP0 — A6
GPP_E7/CPU_GP1 — A7
GPP_B3/CPU_GP2 — BA5
GPP_B4/CPU_GP3 — AY5

R0316 1 1% 2 49.9Ohm — CPU_POPIRCOMP — PROC_POPIRCOMP — AT16
R0317 1 1% 2 49.9Ohm — PCH_POPIRCOMP — PCH_OPIRCOMP — AU16
R0318 1 1% 2 49.9Ohm — EDRAM_OPIO_RCOMP — OPCE_RCOMP — H66
R0319 1 1% 2 49.9Ohm — EOPIO_RCOMP — OPC_RCOMP — H65

JTAG
PROC_TCK — B61 — XDP_TCLK
PROC_TDI — D60 — XDP_TDI_CPU
PROC_TDO — A61 — XDP_TDO_CPU
PROC_TMS — C60 — XDP_TMS_CPU
PROC_TRST# — B59 — XDP_TRST_CPU_N
PCH_JTAG_TCK — B56 — PCH_JTAG_TCLK — 1 T0315
PCH_JTAG_TDI — D59 — PCH_JTAG_TDI
PCH_JTAG_TDO — A56 — PCH_JTAG_TDO
PCH_JTAG_TMS — C59 — PCH_JTAG_TMS
PCH_TRST# — C61 — PCH_TRST_CPU_N
JTAGX — A59 — XDP_TCLK_JTAGX

+VCCSTG
PCH_JTAG_TDO — XDP_TDO_CPU — R0323 2 1 51Ohm
PCH_JTAG_TMS — XDP_TMS_CPU — 1 T0316
PCH_TRST_CPU_N — XDP_TRST_CPU_N — 1 T0317
PCH_JTAG_TDI — XDP_TDI_CPU — 1 T0318
XDP_TCLK_JTAGX — XDP_TCLK — R0324 2 1 51Ohm

940432
01V010000015

Modify to XDP less

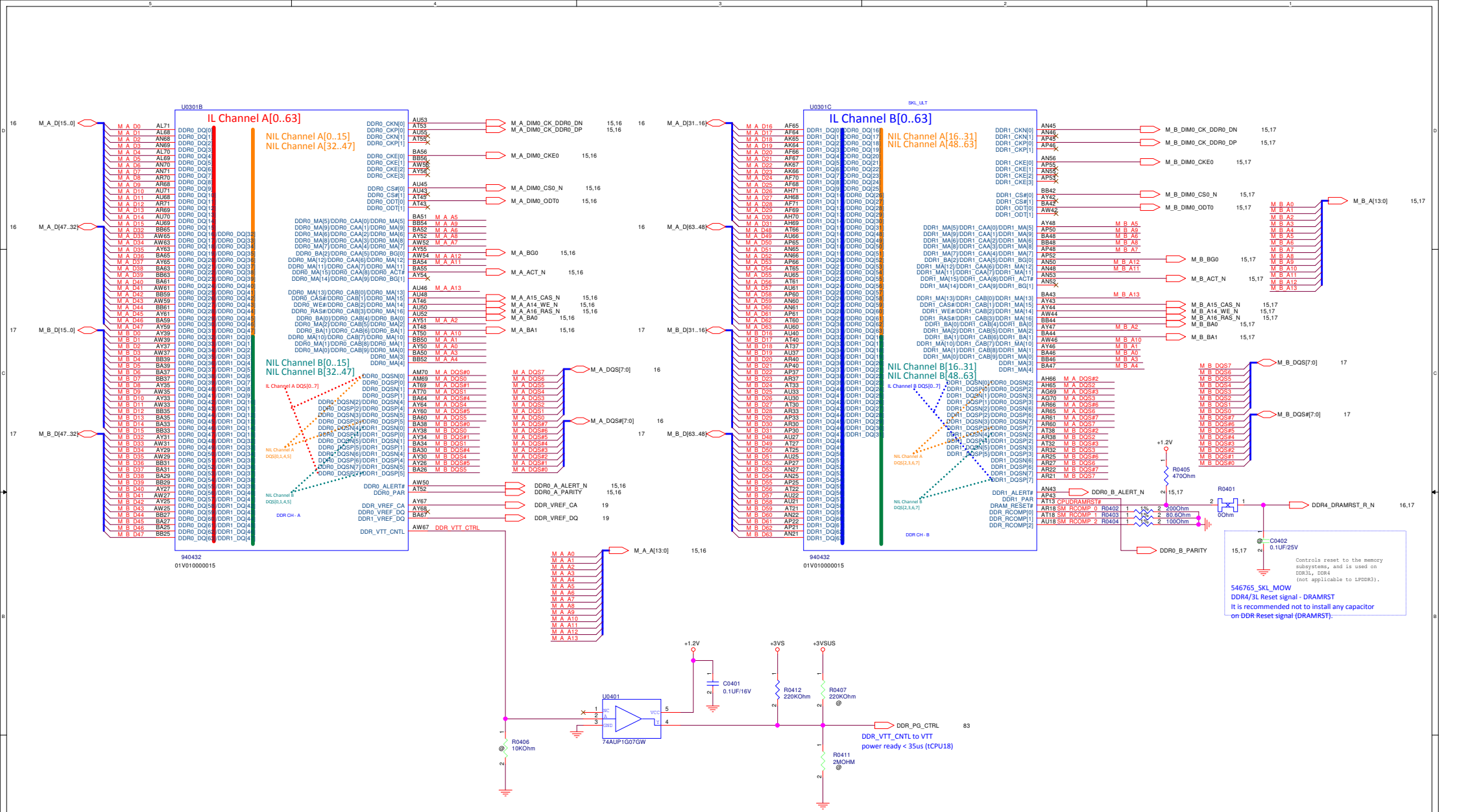
30 THRO_CPU
R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result),預留0ohm是調整空間
Q0301 2N7002
R0341 2 1 0Ohm — H_PROCHOT#
88 PROCHOT# — SP0325 2 1 0Ohm
80 VR_HOT# — R0320 2 @ 1 0Ohm

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CPU(1)_DDI/eDP
BG1/HW3
Engineer: Andy Kao

Size	Project Name	Rev
C	X3	1.0

Date: Monday, July 11, 2016 Sheet 3 of 97



Symbol U0301 B

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1		
BYTE 2		ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 3		
BYTE 4		ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 5		
BYTE 6		ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 7		

Symbol U0301 C

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		
BYTE 2		ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 3		
BYTE 4		ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 5		
BYTE 6		ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 7		

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

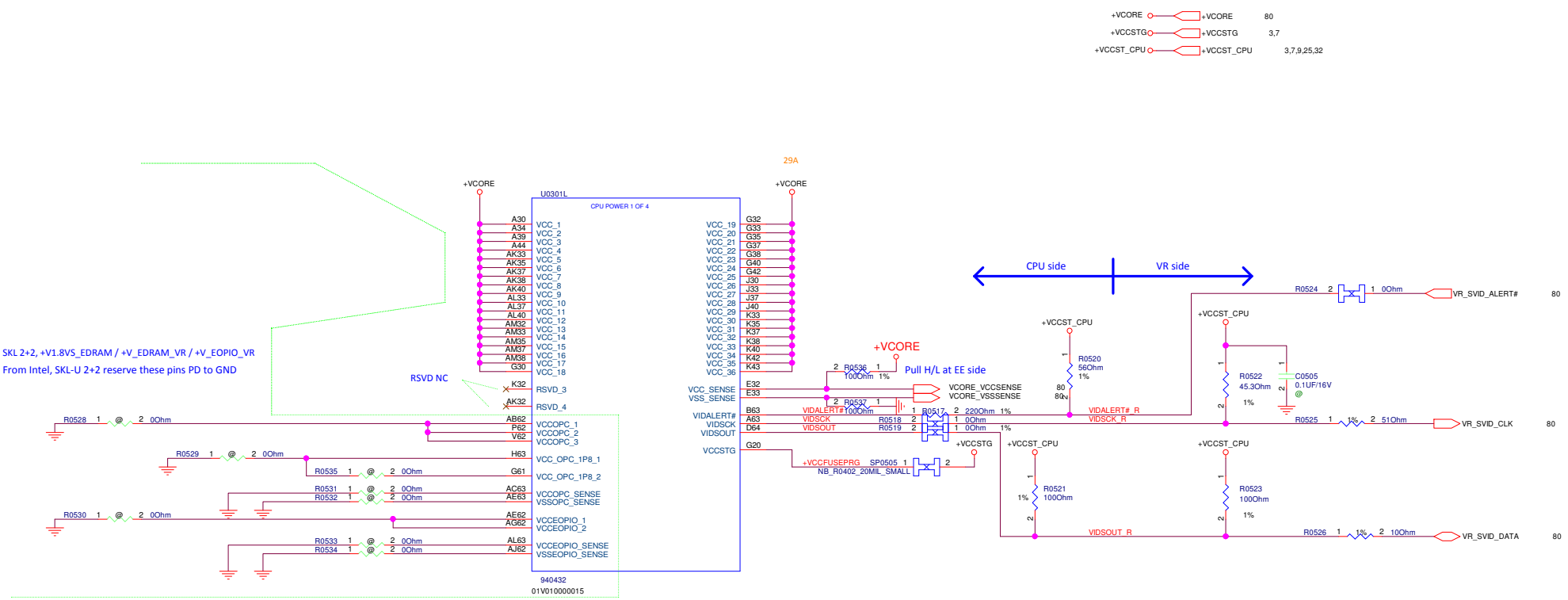
Title : CPU(2)_DDR4

Engineer: Andy Kao

BG1/HW3

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 4 of 97



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

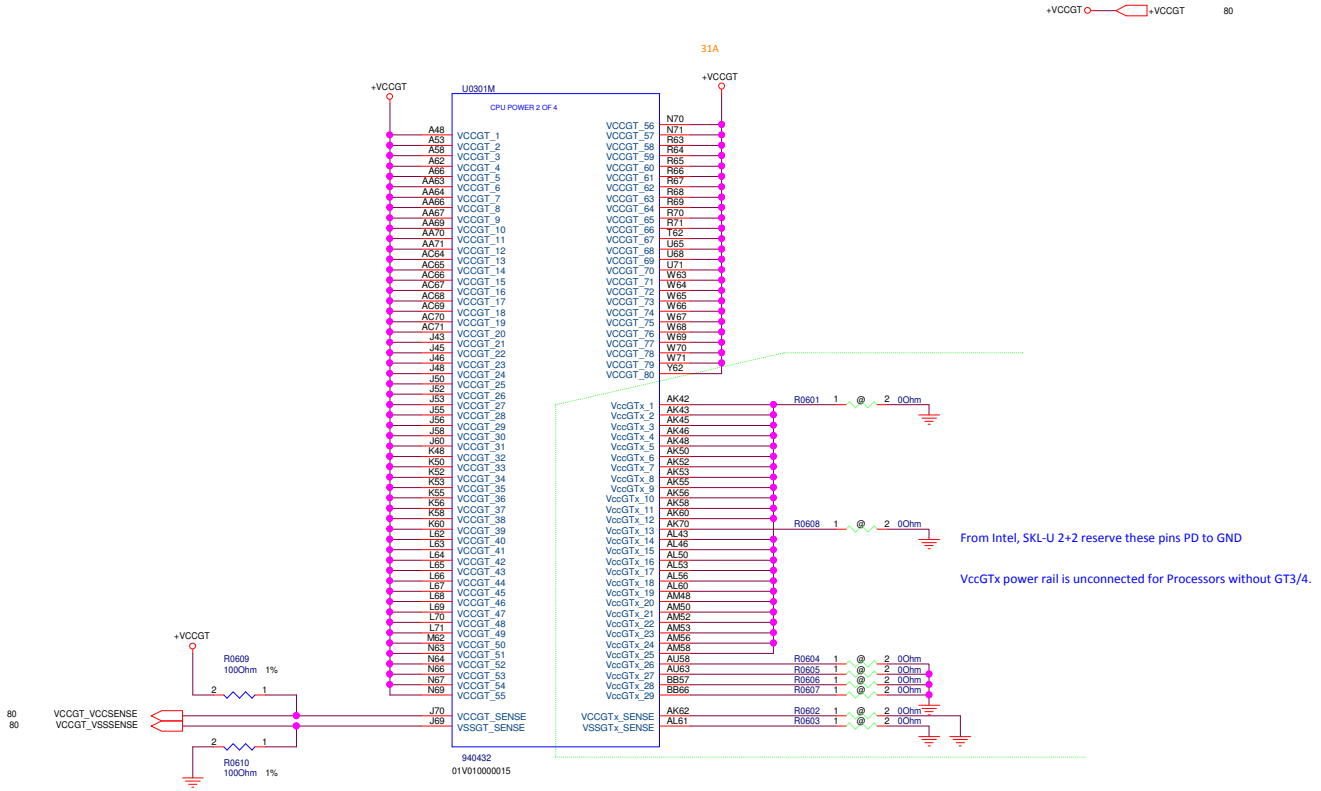
Title :CPU(3)_+VCCCORE

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 5 of 97



PEGATRON	Title : CPU(4)_+VCCGT	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3	Engineer: Andy Kao	
Size: C	Project Name: X3	Rev: 1.0
Date: Monday, July 11, 2016	Sheet 6 of 97	

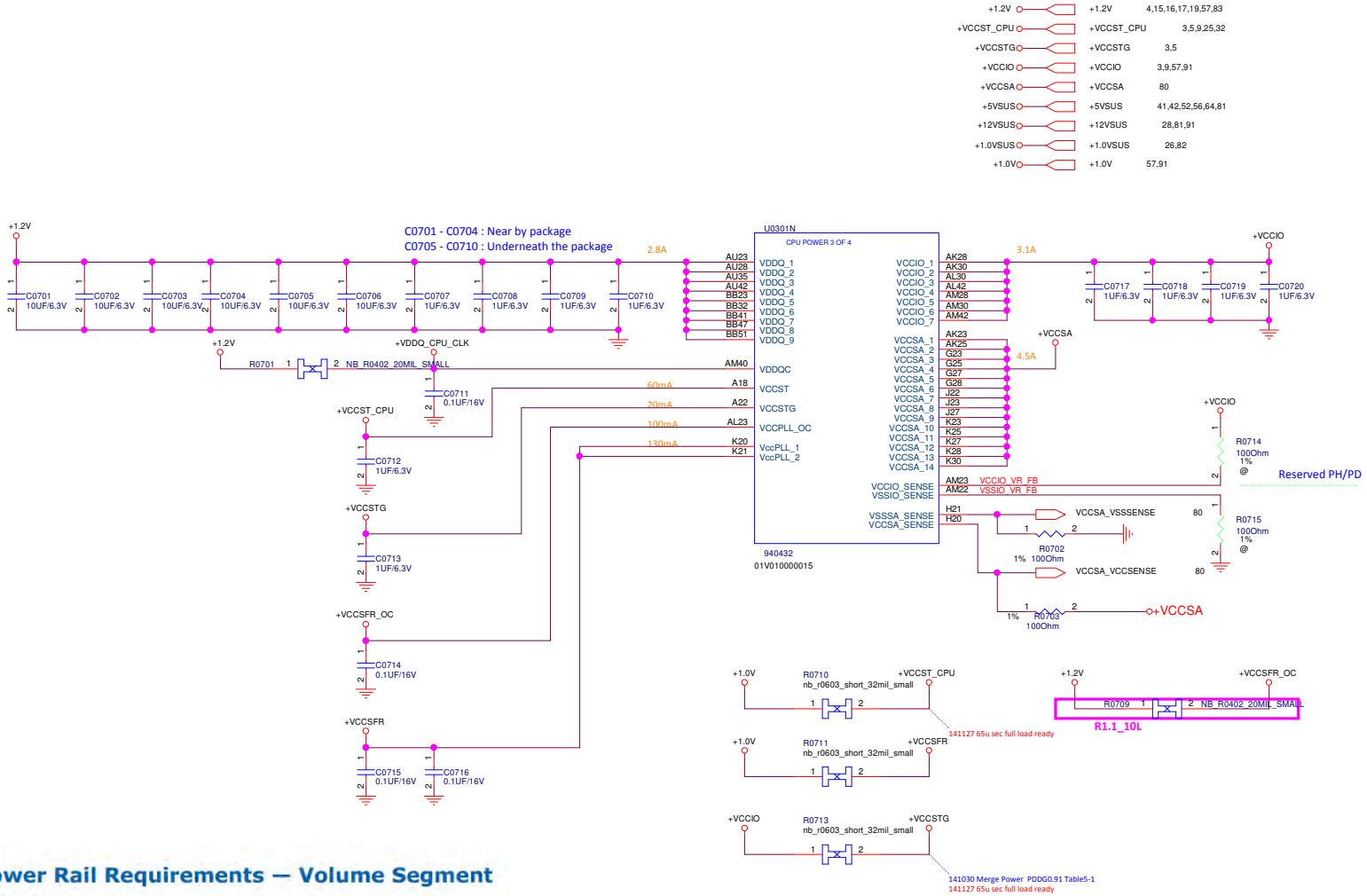
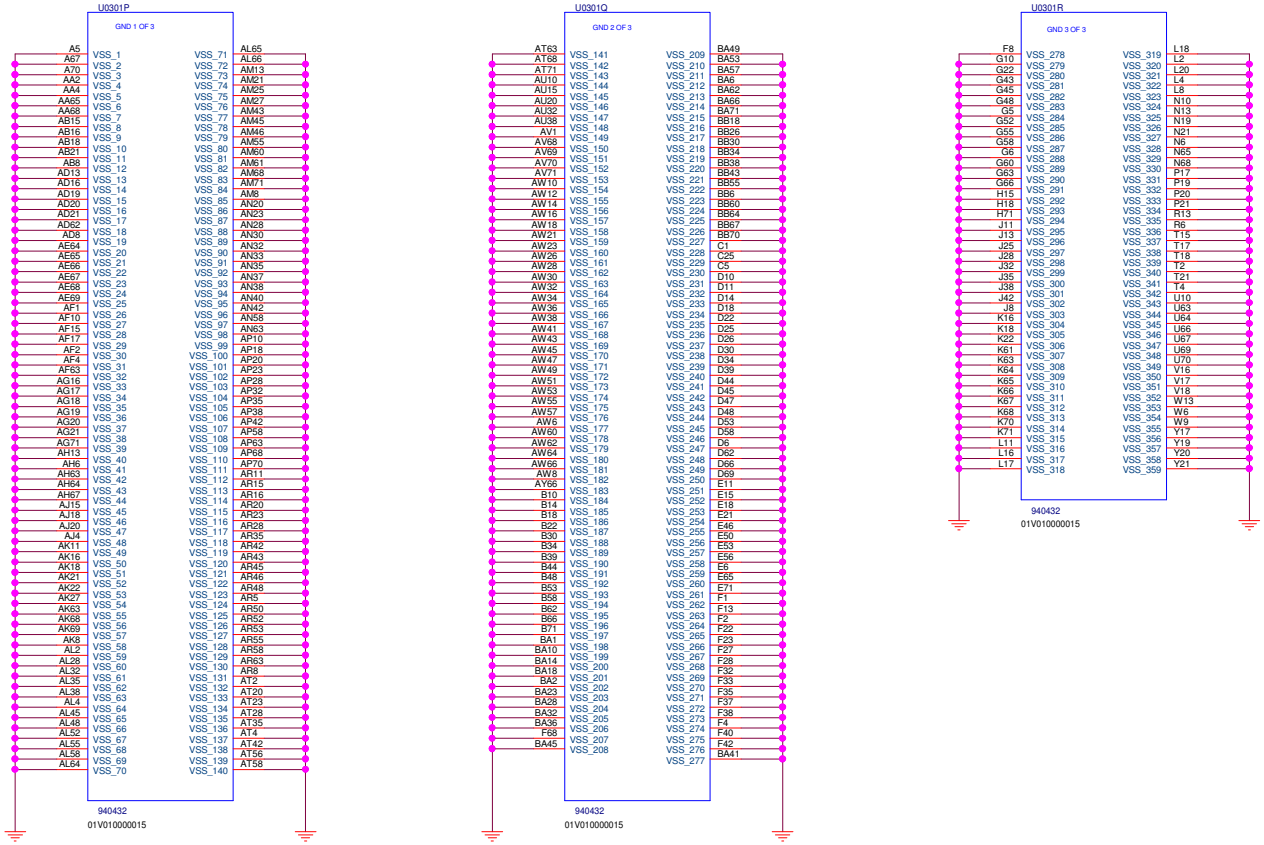


Table 5-1. Power Rail Requirements — Volume Segment — U-Line

Load switch (LS)	LS ENABLE	Load/Rail name	Imax (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc_{ST}	0.04
		Vcc_{PLL}(Vcc_{SFR})	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VccIO	3.0
		Vcc_{STG}	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu_04

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: CPU(5)_+VDDQ/IO/SA
BG1/HW3
Engineer: Andy Kao
Size: Custom | Project Name: X3 | Rev: 1.0
Date: Monday, July 11, 2016 | Sheet 7 of 97



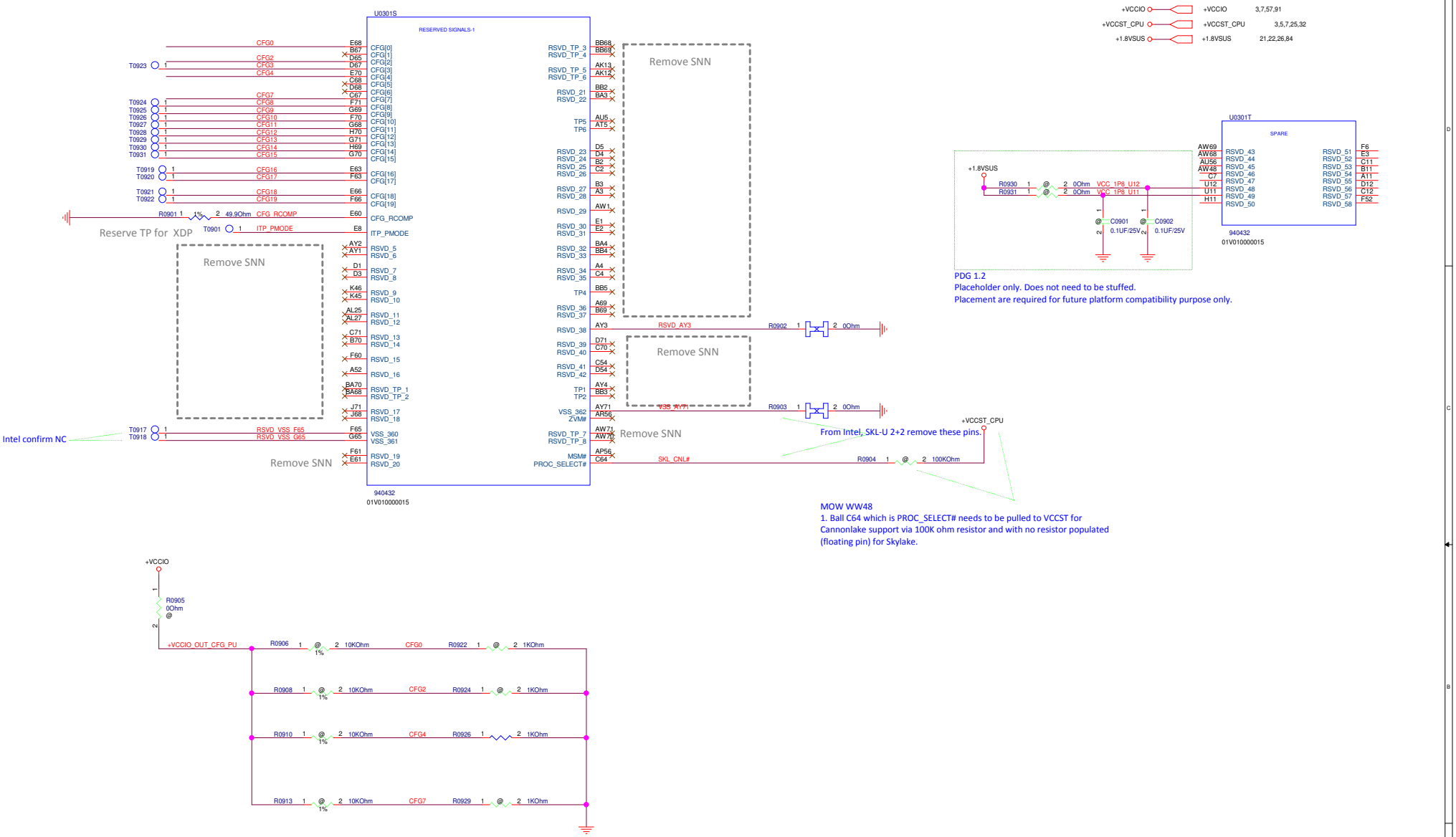
PEGATRON Title : CPU(6)_CPU GND

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
C	X3	1.0

Date: Monday, July 11, 2016 Sheet 8 of 97



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: CPU(7)_CFG/RSVD

Engineer: Andy Kao

BG1/HW3		
Size: C	Project Name: X3	Rev: 1.0
Date: Monday, July 11, 2016	Sheet 9 of 97	

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 10 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 11 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 12 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 13 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

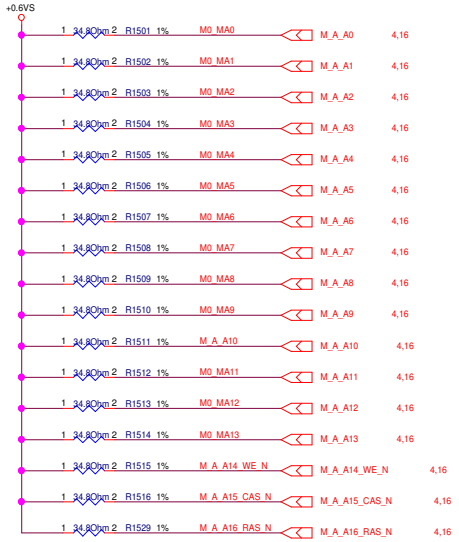
Date: Monday, July 11, 2016 Sheet 14 of 97

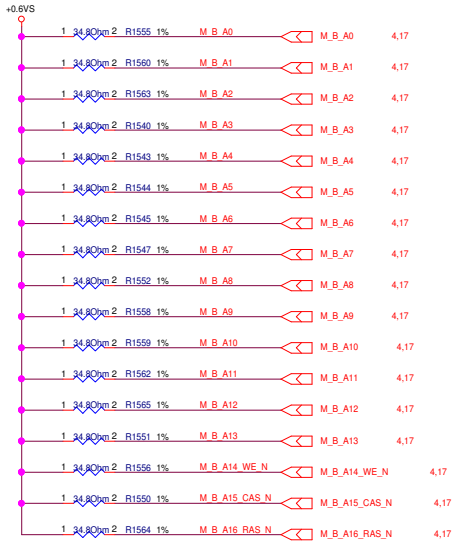
15

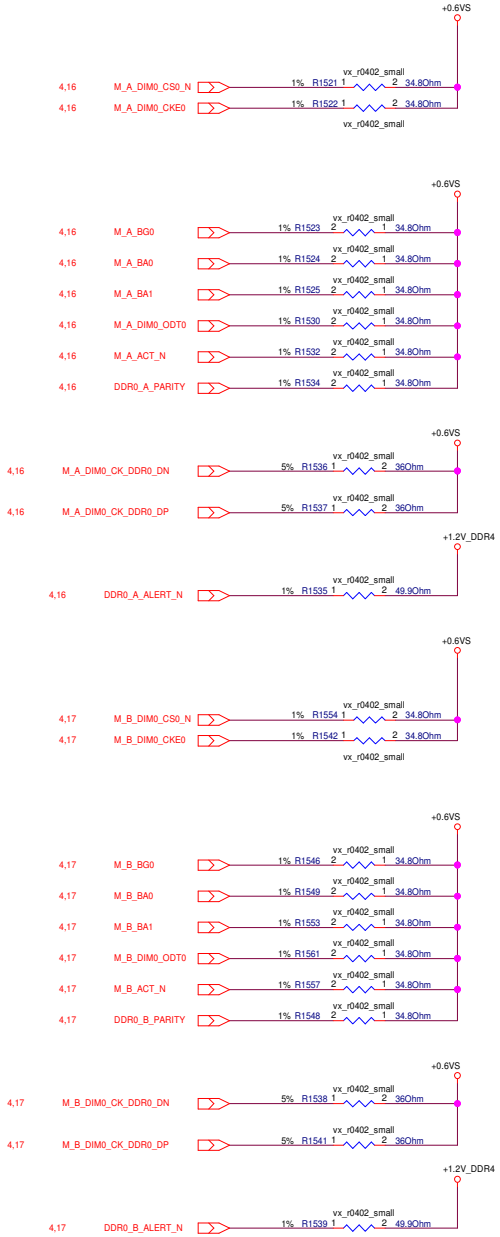
DDR4(0)_Termination

+0.6VS — +0.6VS — 57,83

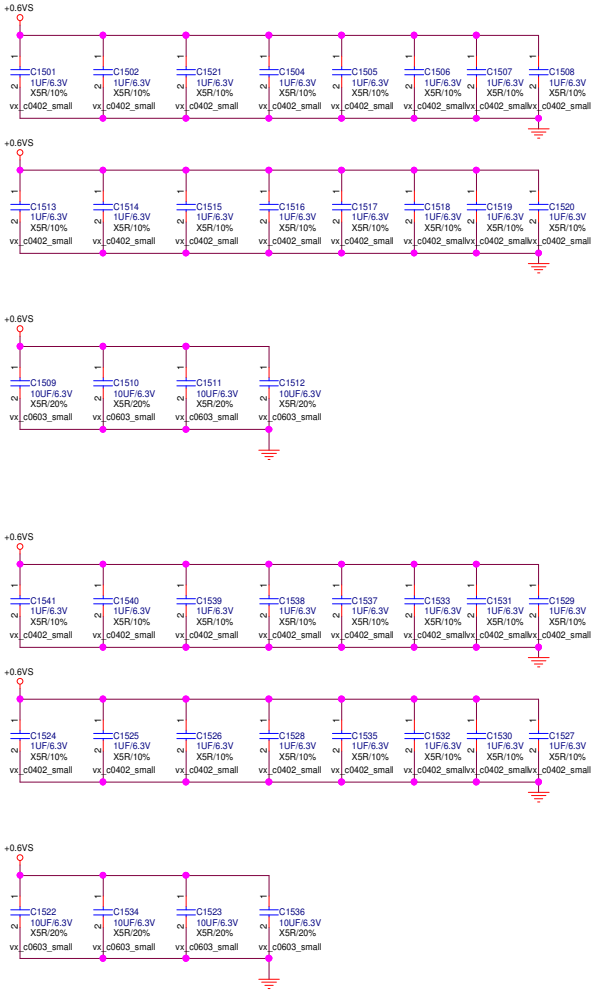
+1.2V_DDR4 — +1.2V_DDR4 — 4,7,16,17,19,57,83





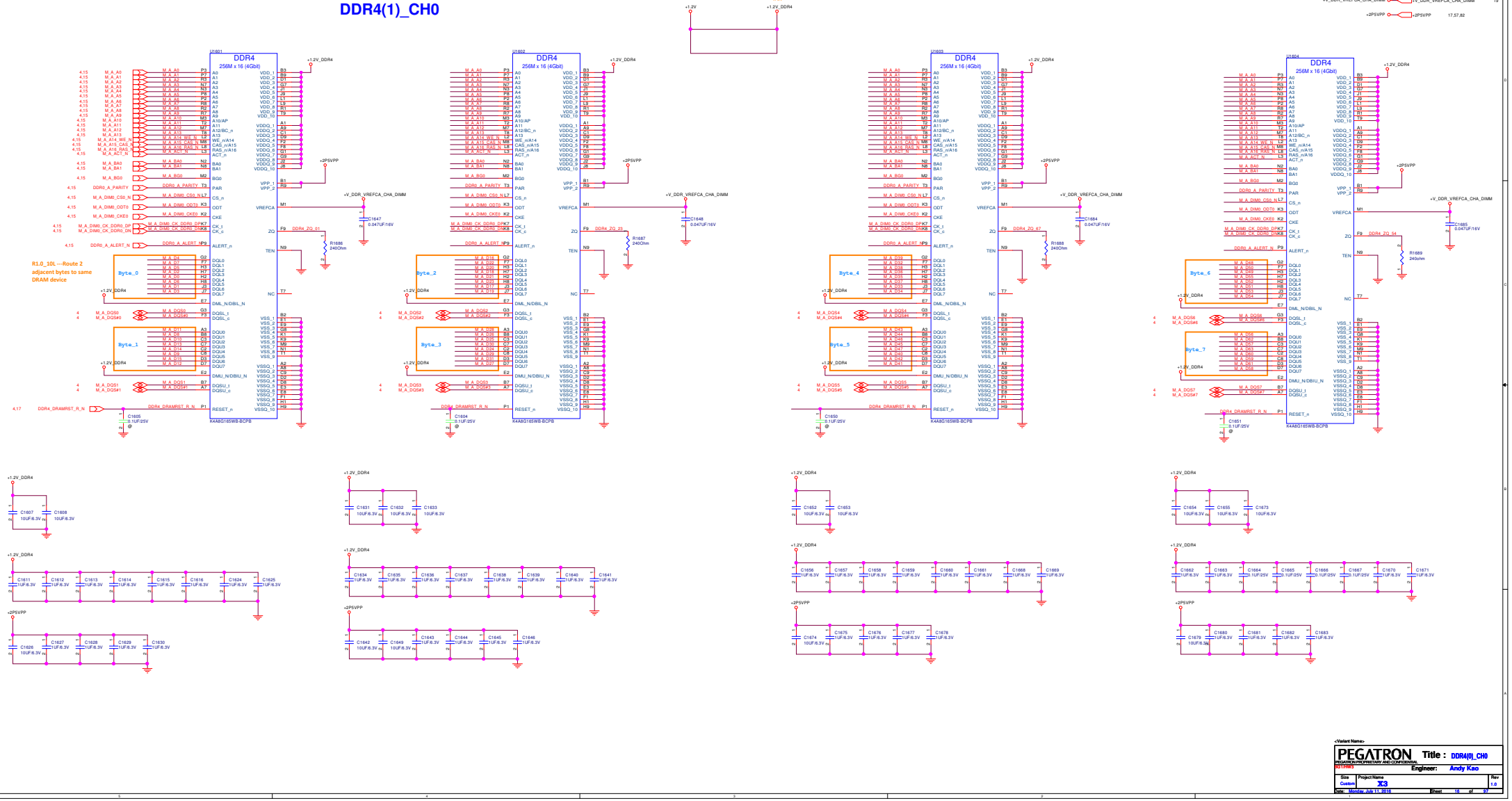


Average placed close to +VDDQ_VTT power plane

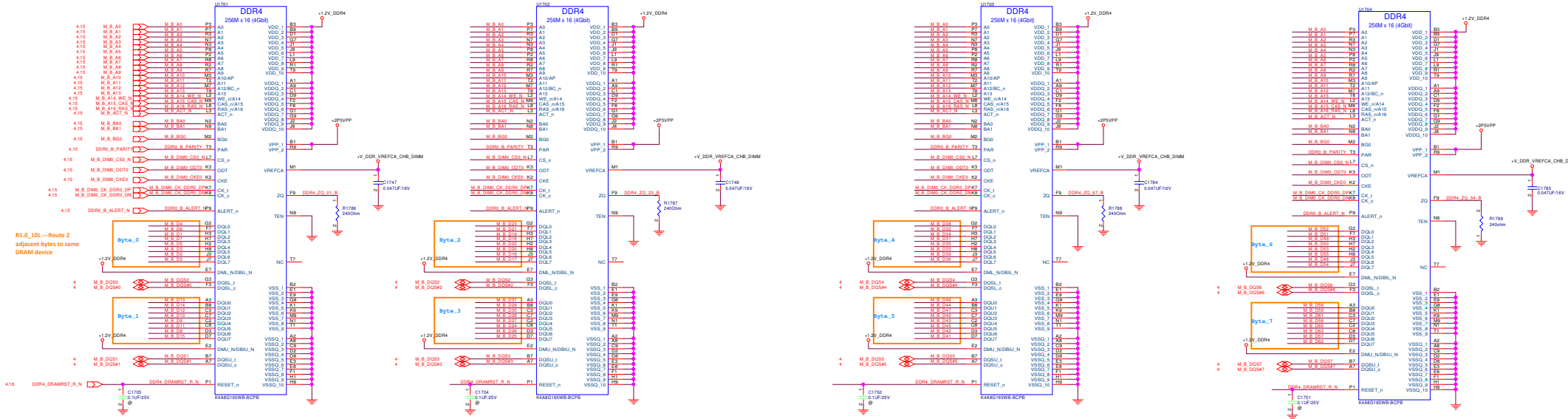


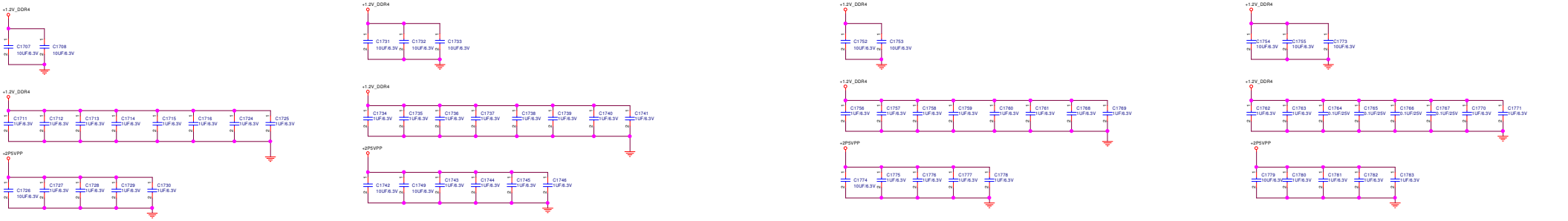
PEGATRON	Title : DDR4(0)_Termination		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
3G1/HW3	Engineer: Andy Kao		
Size: C	Project Name: X3		Rev: 1.0
Date: Monday, July 11, 2016	Sheet 15 of 97		

DDR4(1)_CH0


DDR4
256M x 16 (4Gbit)
K4A8G165WB-BCPB
Byte_0
Byte_1
Byte_2
Byte_3
Byte_4
Byte_5
Byte_6
Byte_7
+1.2V_DDR4
+2P5VPP
+V_DDR_VREFCA_CHA_DIMM
R1.0_10L---Route 2 adjacent bytes to same DRAM device

DDR4(2)_CH1


DDR4
256M x 16 (4Gbit)
K4A8G165WB-BCPB
Byte_0
Byte_1
Byte_2
Byte_3
Byte_4
Byte_5
Byte_6
Byte_7
+1.2V_DDR4
+2P5VPP
+V_DDR_VREFCA_CHB_DIMM
R1.0_10L---Route 2 adjacent bytes to same DRAM device


+1.2V_DDR4
+2P5VPP

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

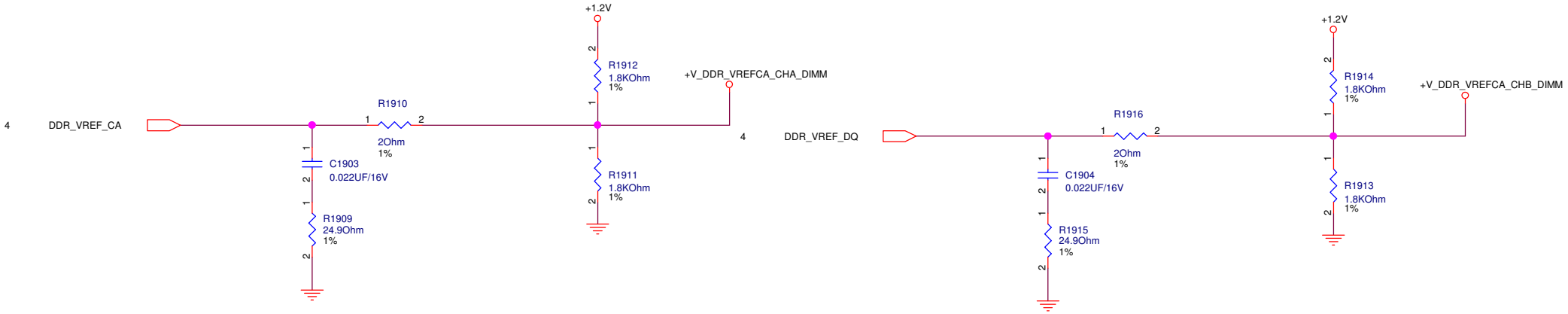
Date: Monday, July 11, 2016 Sheet 18 of 97

19

DDR4(3)_CA/DQ Voltage

+1.2V — +1.2V — 4,7,15,16,17,57,83
+V_DDR_VREFCA_CHB_DIMM — +V_DDR_VREFCA_CHB_DIMM — 17
+V_DDR_VREFCA_CHA_DIMM — +V_DDR_VREFCA_CHA_DIMM — 16

DDR4 Vref (Intel Schematic Review)



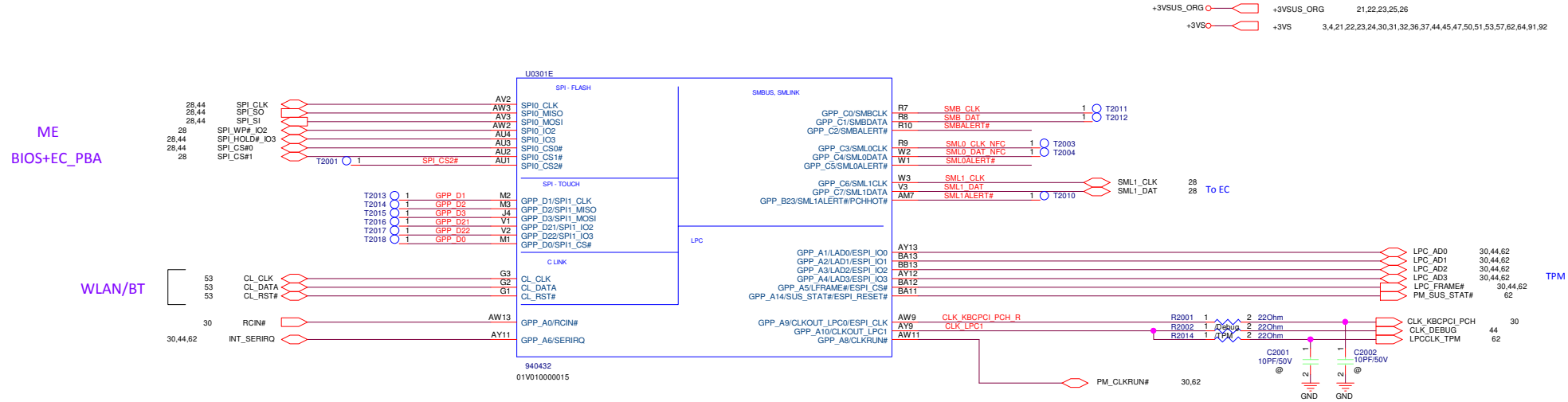
<Variant Name>

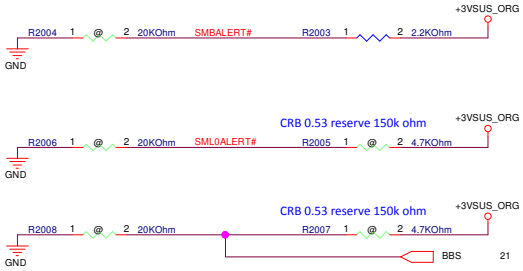
PEGATRON Title : DDR3(3)_CA/DQ Voltage

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 19 of 97

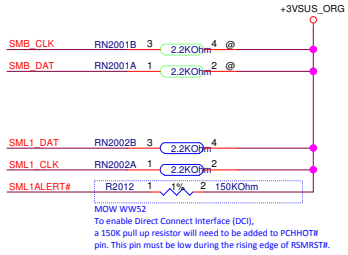




SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable

SML0ALERT# - Internal weak pull down 20 kohm
0 : LPC EC (default)
1 : eSPI EC

BBS - Internal weak pull down 20k ohm
Boot BIOS Strap
0 : SPI destination (default)
1 : LPC destination



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(1)_SPI/LPC

BG1/HW3

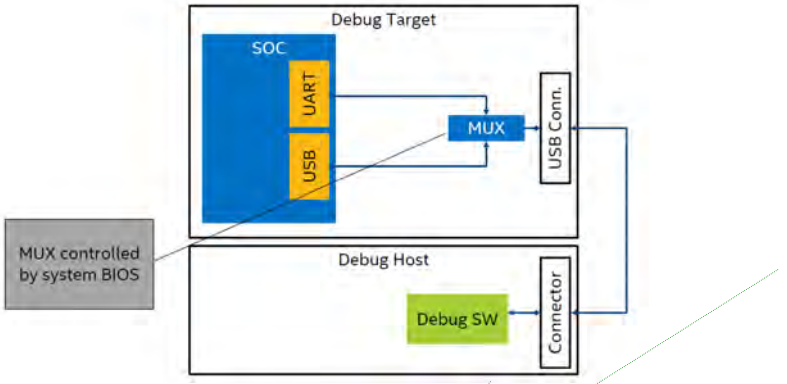
Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 20 of 97

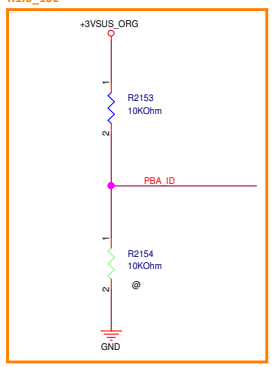
Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required



+3VS — +3VS 3,4,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92

R1.0_10L



GPP_D14	1	0
PBA_ID	Enable	Disable

Boot BIOS Strap Bit (BBS)

20 BBS — R2102 1 2 0Ohm — BBS_R

To implement UART for WIN7 WHCK requirement if need

Please refer to Intel document #548689 - RVP5

64 UART_RX — GPP_C8/UART0_RXD

64 UART_TX — GPP_C9/UART0_TXD

64 USB_UART_SEL — GPP_C10/UART0_RTS#

T2144 1 GPP_C11 — GPP_C11/UART0_CTS#

53 WLAN_ON_PCH — WLAN_ON_PCH — GPP_C20/UART2_RXD

53 BT_ON/OFF#_PCH — BT_ON/OFF#_PCH — GPP_C21/UART2_TXD

3,45 LCD_BKLTEN_PCH — GPP_C22/UART2_RTS#

53 IOAC_EN — GPP_C23/UART2_CTS#

2016.6.29
R1.4_10L ---For IOAC

Type C MUX

30 PCH_I2C0_SDA — PCH_I2C0_SDA — U7 — GPP_C16/I2C0_SDA

30 PCH_I2C0_SCL — PCH_I2C0_SCL — U6 — GPP_C17/I2C0_SCL

Click PAD

31 PCH_I2C1_SDA — PCH_I2C1_SDA — U8 — GPP_C18/I2C1_SDA

31 PCH_I2C1_SCL — PCH_I2C1_SCL — U9 — GPP_C19/I2C1_SCL

PRJ — AH9 — GPP_F4/I2C2_SDA

PCB_ID3 — AH10 — GPP_F5/I2C2_SCL

PCB_ID4 — AH11 — GPP_F6/I2C3_SDA

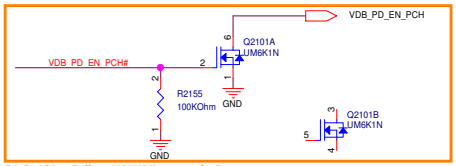
PCB_ID5 — AH12 — GPP_F7/I2C3_SCL

T2115 1 GPP_F8 — AF11 — GPP_F8/I2C4_SDA

T2116 1 GPP_F9 — AF12 — GPP_F9/I2C4_SCL

C 3.3V GPIO

F 1.8V GPIO



R1.0_10L ---Follow HAWAII type-c design

U0301F

LPSS

MEM_ID0 — AN8 — GPP_B15/GSPI0_CS#

MEM_ID1 — AP7 — GPP_B16/GSPI0_CLK

MEM_ID2 — AP8 — GPP_B17/GSPI0_MISO

GPP_B18 — AR7 — GPP_B18/GSPI0_MOSI

MEM_CHA — AM5 — GPP_B19/GSPI1_CS#

MEM_CHB — AN7 — GPP_B20/GSPI1_CLK

VDB_PD_EN_PCH# — AP5 — GPP_B21/GSPI1_MISO

BBS_R — AN5 — GPP_B22/GSPI1_MOSI

ISH

GPP_D9 — P2

GPP_D10 — P3

GPP_D11 — P4 — GPP_D11 1 T2151

GPP_D12 — P1 — GPP_D12 1 T2152

I2C0_MUX_SEL 30

TP_SENSOR_OFF# 31

GPP_D5/ISH_I2C0_SDA — M4 — ISH_I2C0_SDA

GPP_D6/ISH_I2C0_SCL — N3 — ISH_I2C0_SCL

GPP_D7/ISH_I2C1_SDA — N1

GPP_D8/ISH_I2C1_SCL — N2

GPP_F10/I2C5_SDA/ISH_I2C2_SDA — AD11 — GPP_F10 1 T2148

GPP_F11/I2C5_SCL/ISH_I2C2_SCL — AD12 — GPP_F11 1 T2147

GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA — U1

GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL — U2 — PBA_ID 1 T2153

GPP_D15/ISH_UART0_RTS# — U3 — IOBD_ID_PCH 1 T2154

GPP_D16/ISH_UART0_CTS#/SML0BALERT# — U4

TP_IRQ# 30,31

GPP_C12/UART1_RXD/ISH_UART1_RXD — AC1

GPP_C13/UART1_TXD/ISH_UART1_TXD — AC2 — PCB_ID0

GPP_C14/UART1_RTS#/ISH_UART1_RTS# — AC3 — PCB_ID1

GPP_C15/UART1_CTS#/ISH_UART1_CTS# — AB4 — PCB_ID2

OP_SD# 36

GPP_A18/ISH_GP0 — AY8

GPP_A19/ISH_GP1 — BA8

GPP_A20/ISH_GP2 — BB7

GPP_A21/ISH_GP3 — BA7

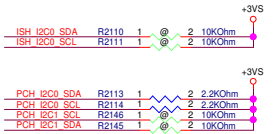
GPP_A22/ISH_GP4 — AY7

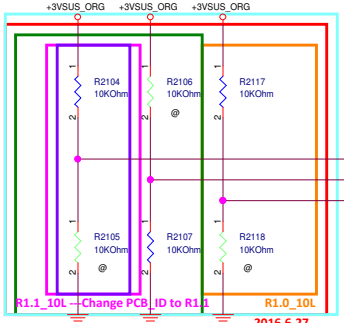
GPP_A23/ISH_GP5 — AW7

Sx_EXIT_HOLDOFF#/GPP_A12/BM_BUSY#/ISH_GP6 — AP13

940432

01V010000015



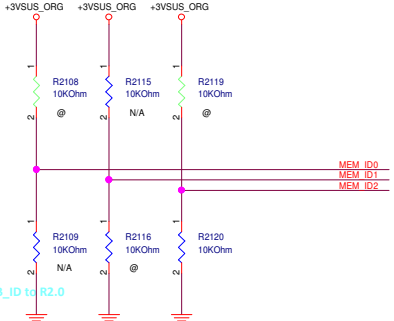


R1.1_10L ---Change PCB_ID to R1.1

R1.0_10L

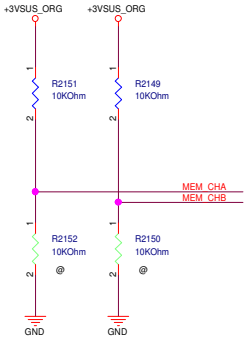
2016.6.2
R1.2_10L ---Change PCB_ID to R1.2

2016.6.14
R1.3_10L ---Change PCB_ID to R1.3

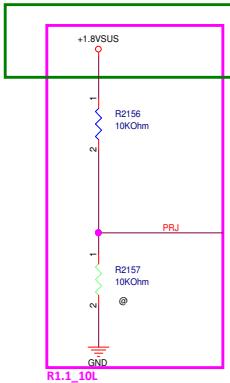


2016.6.7.4
R2.0_10L ---Change PCB_ID to R2.0

2016.6.27
R1.4_10L ---Change PCB_ID to R1.4



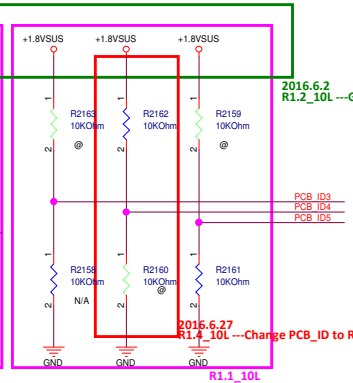
	CHA	CHB
GPP_B19(0)	Disable	
GPP_B19(1)	Enable	
GPP_B20(0)		Disable
GPP_B20(1)		Enable



R1.1_10L

	PRJ
GPP_F4(0)	M3
GPP_F4(1)	X3

2016.6.2
R1.2_10L ---GPP_F is used by 1.8V



R1.1_10L

	PCB_ID3
GPP_F5(0)	SKL
GPP_F5(1)	KBL

	PCB_ID5
GPP_F7(0)	2133
GPP_F7(1)	2400

GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

Default is GPO, to reserve pull high to +3VSUS_ORG

MB Version ID

	PCB_ID4 (GPP_F6)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R1.0	0	0	0
R1.1	0	0	1
R1.2	0	1	0
R1.3	0	1	1
R1.4	1	0	0
R2.0	1	0	1

	PCB_ID2 (GPP_C15)
8L	0
10L	1

	MEM_ID1 (GPP_B16)
4Gb	0
8Gb	1

Memory ID

	MEM_ID2 (GPP_B17)	MEM_ID0 (GPP_B15)
SAMSUNG	0	0
HYNIX	0	1
MICRON	1	0
RSV	1	1

PEGATRON Title : PCH(2)_ISH

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

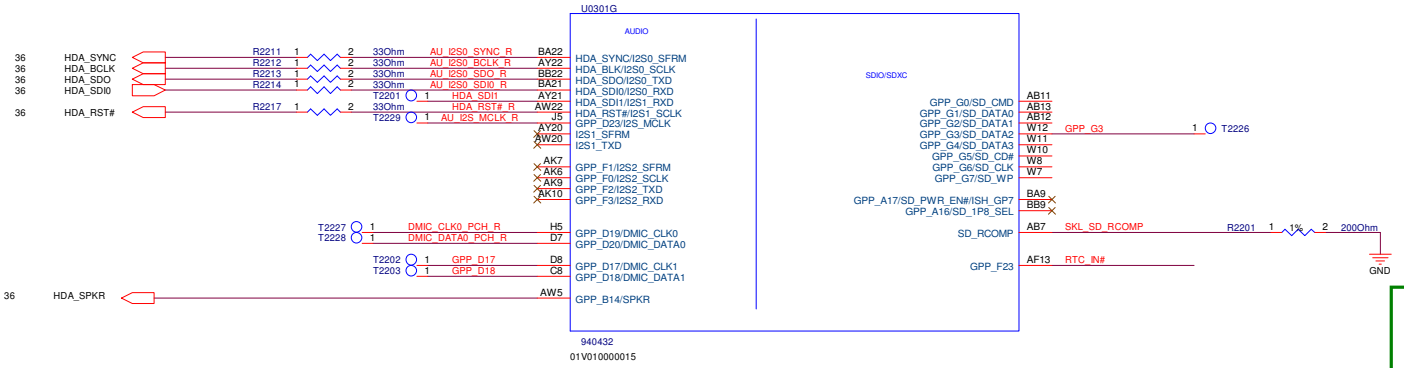
Size	Project Name	Rev
Custom	X3	1.0

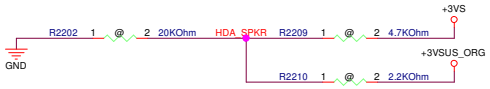
Date: Monday, July 11, 2016 Sheet 21 of 97

+VCCPAZIO +VCCPAZIO 26

+3VS +3VS 3,4,21,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92

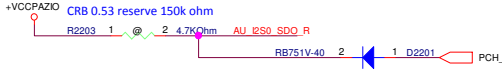
+3VSUS_ORG +3VSUS_ORG 20,21,23,25,26



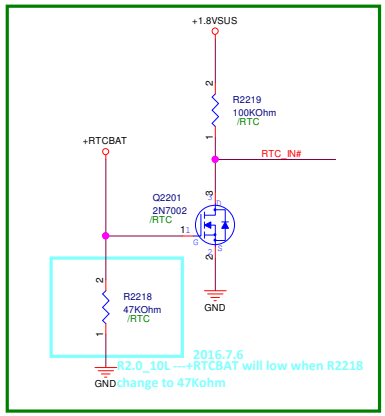


SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG



AU_I2S0_SDO_R - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRRIDE
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security



2016.5.11
R1.2_10L ---RTC detect circuit

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(3)_HDA/SDIO

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 22 of 97

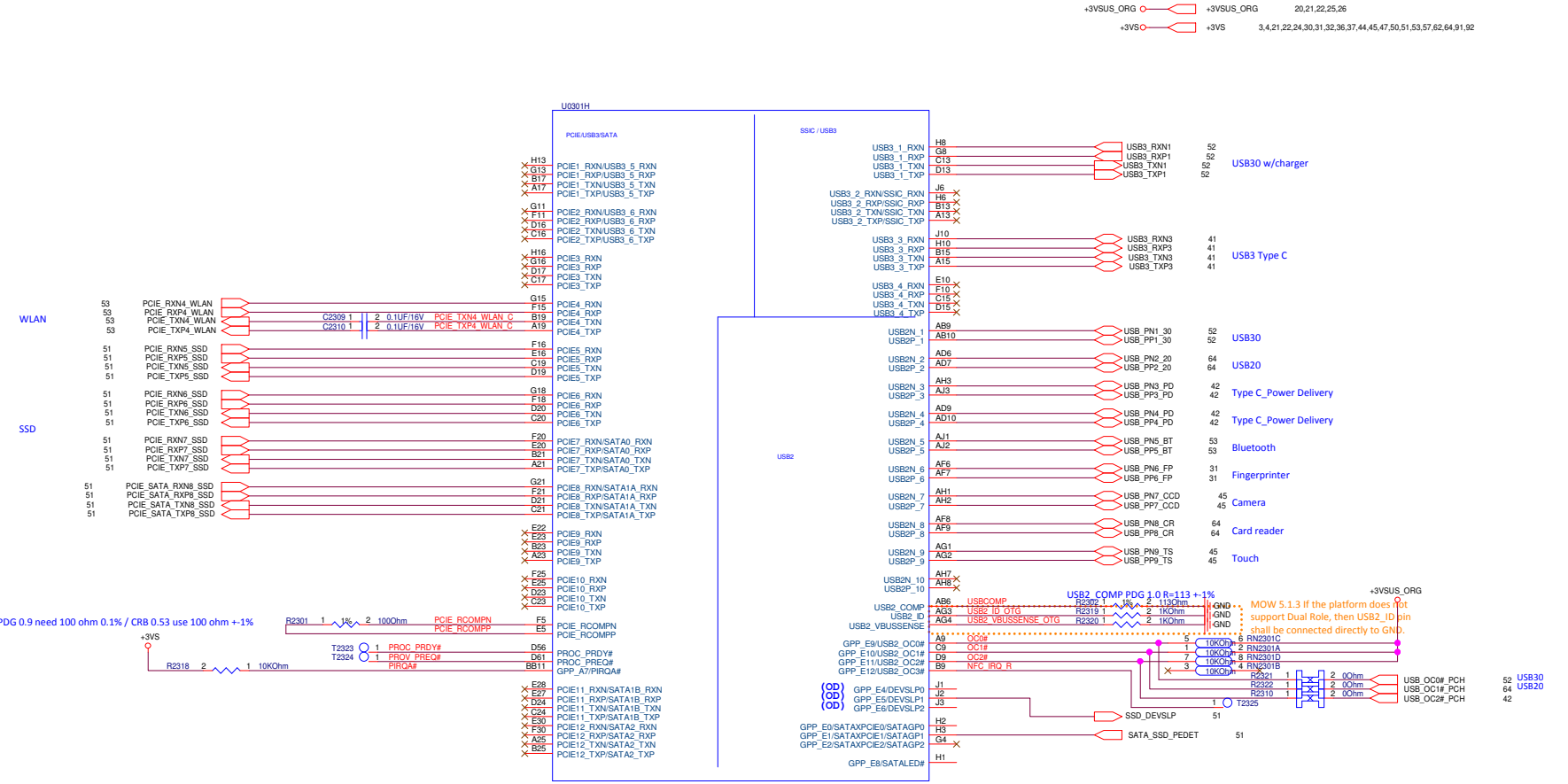


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1–8
2. USB 2.0 port numbers: 1–10
3. USB 2.0 port numbers: 1–6
4. SATA Express Capable Ports (x2)

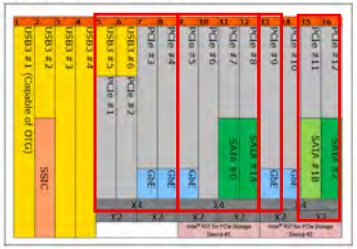
Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

3.4.1 SKL PCH U Flexible I/O

Figure 3-1. HSIO Muxing on SKL PCH U



<Variant Name>

PEGATRON
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Title: PCH(4)_USB/PCIE/SATA

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
C	X3	1.0

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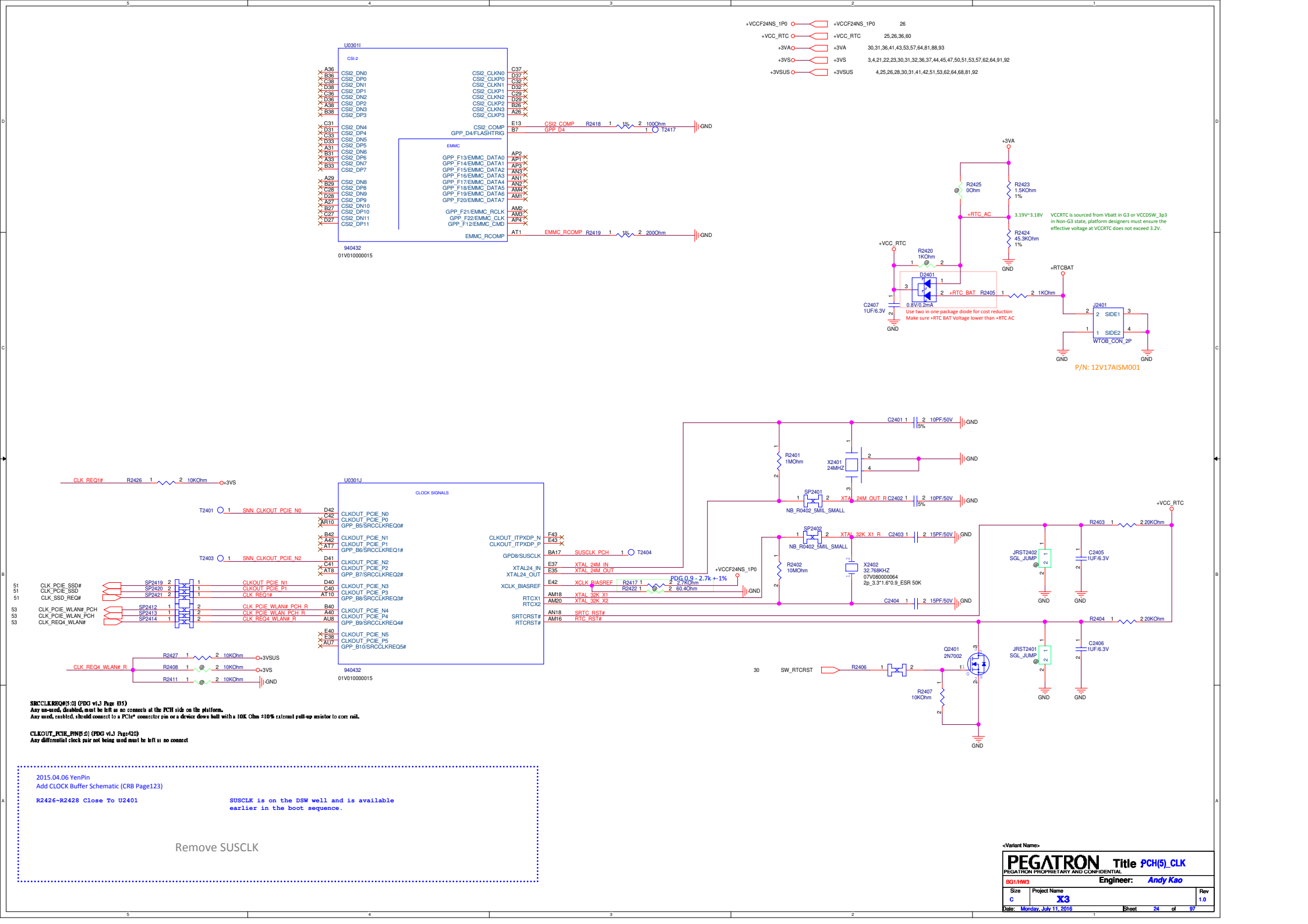
+VCCF24NS_1P0 +VCCF24NS_1P0 26
+VCC_RTC +VCC_RTC 25,26,36,60
+3VA +3VA 30,31,36,41,43,53,57,64,81,88,93
+3VS +3VS 3,4,21,22,23,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+3VSUS +3VSUS 4,25,26,28,30,31,41,42,51,53,62,64,68,81,92
U0301I
CSI-2
CSI2_DN0 CSI2_DP0 CSI2_DN1 CSI2_DP1 CSI2_DN2 CSI2_DP2 CSI2_DN3 CSI2_DP3
CSI2_DN4 CSI2_DP4 CSI2_DN5 CSI2_DP5 CSI2_DN6 CSI2_DP6 CSI2_DN7 CSI2_DP7
CSI2_DN8 CSI2_DP8 CSI2_DN9 CSI2_DP9 CSI2_DN10 CSI2_DP10 CSI2_DN11 CSI2_DP11
CSI2_CLKN0 CSI2_CLKP0 CSI2_CLKN1 CSI2_CLKP1 CSI2_CLKN2 CSI2_CLKP2 CSI2_CLKN3 CSI2_CLKP3
CSI2_COMP
GPP_D4/FLASHTRIG
EMMC
GPP_F13/EMMC_DATA0 GPP_F14/EMMC_DATA1 GPP_F15/EMMC_DATA2 GPP_F16/EMMC_DATA3 GPP_F17/EMMC_DATA4 GPP_F18/EMMC_DATA5 GPP_F19/EMMC_DATA6 GPP_F20/EMMC_DATA7
GPP_F21/EMMC_RCLK GPP_F22/EMMC_CLK GPP_F12/EMMC_CMD
EMMC_RCOMP
CSI2_COMP R2418 1 49.9 2 100Ohm 1 T2417 GND
EMMC_RCOMP R2419 1 49.9 2 200Ohm GND
940432
01V010000015
+3VA
R2425 0Ohm
R2423 1.5KOhm 1%
+RTC_AC
3.19V~3.18V
R2424 45.3KOhm 1%
GND
VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V.
+VCC_RTC
R2420 1KOhm
D2401
+RTC_BAT R2405 1 2 1KOhm
+RTCBAT
C2407 1UF/6.3V
0.8V/0.2mA
Use two in one package diode for cost reduction
Make sure +RTC BAT Voltage lower than +RTC AC
J2401
SIDE1 SIDE2
WTOB_CON_2P
P/N: 12V17AISM001
CLK_REQ1# R2426 1 2 10KOhm +3VS
U0301J
CLOCK SIGNALS
T2401 SNN_CLKOUT_PCIE_N0
T2403 SNN_CLKOUT_PCIE_N2
CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#
CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#
CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#
CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#
CLKOUT_ITPXDP_N CLKOUT_ITPXDP_P
GPD8/SUSCLK
XTAL24_IN XTAL24_OUT
XCLK_BIASREF
RTCX1 RTCX2
SRTCRST# RTCRST#
SUSCLK_PCH T2404
XTAL_24M_IN XTAL_24M_OUT
XCLK_BIASREF R2417 1 2 2.7KOhm PDG 0.9 ~ 2.7k +-1%
R2422 1 @ 2 60.4Ohm GND
XTAL_32K_X1 XTAL_32K_X2
SRTC_RST# RTC_RST#
940432
01V010000015
CLK_PCIE_SSD# SP2419 CLKOUT_PCIE_N1
CLK_PCIE_SSD SP2420 CLKOUT_PCIE_P1
CLK_SSD_REQ# SP2421 CLK_REQ1#
CLK_PCIE_WLAN#_PCH SP2412 CLK_PCIE_WLAN#_PCH_R
CLK_PCIE_WLAN_PCH SP2413 CLK_PCIE_WLAN_PCH_R
CLK_REQ4_WLAN# SP2414 CLK_REQ4_WLAN#_R
R2427 1 2 10KOhm +3VSUS
CLK_REQ4_WLAN#_R R2408 1 @ 2 10KOhm +3VS
R2411 1 @ 2 10KOhm GND
C2401 1 2 10PF/50V 5% GND
R2401 1MOhm
X2401 24MHZ
SP2401 XTAL_24M_OUT_R C2402 1 2 10PF/50V 5% GND
NB_R0402_5MIL_SMALL
SP2402 XTAL_32K_X1_R C2403 1 2 15PF/50V GND
NB_R0402_5MIL_SMALL
R2402 10MOhm
X2402 32.768KHZ 07V080000064 2p_3.3*1.6*0.9_ESR 50K
C2404 1 2 15PF/50V GND
+VCC_RTC
R2403 1 2 20KOhm
JRST2402 SGL_JUMP
C2405 1UF/6.3V
R2404 1 2 20KOhm
JRST2401 SGL_JUMP
C2406 1UF/6.3V
Q2401 2N7002
30 SW_RTCRST R2406 1 2
R2407 10KOhm
GND
SRCCLKREQ#[5:0] (PDG v1.3 Page 135)
Any un-used, disabled, must be left as no connects at the PCH side on the platform.
Any used, enabled, should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail.
CLKOUT_PCIE_P/N[5:0] (PDG v1.3 Page420)
Any differential clock pair not being used must be left as no connect
2015.04.06 YenPin
Add CLOCK Buffer Schematic (CRB Page123)
R2426~R2428 Close To U2401
SUSCLK is on the DSW well and is available earlier in the boot sequence.
Remove SUSCLK
<Variant Name>
PEGATRON
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Title PCH(5)_CLK
BG1/HW3
Engineer: Andy Kao
Size C
Project Name X3
Rev 1.0
Date: Monday, July 11, 2016
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+3VSUS_ORG — +3VSUS_ORG 20,21,22,23,26
+VCC_RTC — +VCC_RTC 24,26,36,60
+VCCDSW — +VCCDSW 26,30
+VCCST_CPU — +VCCST_CPU 3,5,7,9,32
+3V — +3V 31,57,82,91
+3VSUS — +3VSUS 4,24,26,28,30,31,41,42,51,53,62,64,68,81,92

+3VSUS_ORG
R2501 10KOhm
U0301K
SYSTEM POWER MANAGEMENT
940432
01V010000015

30 PM_RSMRST# — R2535 — PLT_RST# — PM_SYS_RESET# R — PM_RSMRST# R
T2501 — H_CPUPWRGD_TP — R2503 1KOhm — H_CPUPWRGD — H_VCCST_PWRGD_MCP
ALL_SYS_PWRGD delay 99 ms from EC
30,68 SYS_PWROK — R2504 R2505 R2506 — PM_PWROK PM_RSMRST_R — SYS_PWROK_R PM_PCH_PWROK_R PCH_DPWROK
30 SUSWARN#/SUSPWRDNACK — R2508 SBA 0Ohm — SUS_PWR_ACK_R — SUS_PWR_ACK_R
DSW function / non-AMT
30 SUSACK# — R2509 SBA 0Ohm — SUSACK# R
53 WAKE_PCIE# — R2510 @ 0Ohm — LAN_WAKE#
T2502 GPD11 — T2508 GPD7

GPP_B13/PLTRST# SYS_RESET# RSMRST# — PROCPWRGD VCCST_PWRGD — SYS_PWROK PCH_PWROK DSW_PWROK — GPP_A13/SUSWARN#/SUSPWRDNACK GPP_A15/SUSACK# — WAKE# GPD2/LAN_WAKE# GPD11/LANPHYPC GPD7/RSVD

GPP_B12/SLP_S0# GPD4/SLP_S3# GPD5/SLP_S4# GPD10/SLP_S5# — SLP_SUS# SLP_LAN# GPD9/SLP_WLAN# GPD6/SLP_A# — GPD3/PWRBTN# GPD1/ACPRESENT GPD0/BATLOW# — GPP_A11/PME# INTRUDER# — GPP_B11/EXT_PWR_GATE# GPP_B2/VRALERT#

AT11 SLP_S0# — T2503
AP15 SLP_S3# R — R2533 — PM_SUSB# 30,68
BA16 SLP_S4# R — R2534 — PM_SUSC# 30,68
AY16 GPD10 — T2504
AN15 SLP_SUS# — T2510
AW15 SLP_LAN# — T2505
BB17 SLP_WLAN# — T2511
AN16 ME_SLP_A# — R2538 SBA 0Ohm — ME_PM_SLP_A# 30
BA15
AY15 AC_PRESENT_R — R2532 SBA 0Ohm — PM_PWRBTN# 30 / ME_AC_PRESENT 30
AU13 BATLOW#
+VCC_RTC
AU11 PME#
AP16 SM_INTRUDER# — R2513 1 2 1MOhm
AM10 MPHY_EXT_PWR_GATEB_R — SP2505 — MPHY_EXT_PWR_GATEB
AM11 VR_ALERT#
+3VSUS_ORG — R2514 10KOhm — internal pull high

30,92 ALL_SYSTEM_PWRGD
30 DELAY_ALL_SYSTEM_PWRGD — R2531 @ 0Ohm — SP2506 — ALL_SYSTEM_PWRGD_PMOK
D2501 — RB751V-40 — VR_READY_PMOK
80,92 VRM_PWRGD
PLT_RST# — D2502 — RB751V-40
+3VSUS
U2502 Vcc=2~5.5
R2517 @ 0Ohm
PM_PWROK — R2519 10KOhm — GND
R1.0_10L ---Shutdown possible solution

+VCCDSW
BATLOW# R2522 10KOhm
LAN_WAKE# R2523 10KOhm
GPD7 R2524 10KOhm
WAKE_PCIE# R2525 1KOhm
AC_PRESENT_R R2526 10KOhm
PM_PWRBTN# R2537 @ 10KOhm

+3V
U2501 SN74LVC1G08DCKR
PLT_RST# — C2502 100PF/50V @ — R2515 — C2503 100PF/50V @ — R2516 10KOhm — BUF_PLT_RST# 30,32,51,53,62
GND

+3VSUS_ORG
internal pull high
PME# R2527 @ 10KOhm
Set to GPI
VR_ALERT# R2528 @ 10KOhm

EC delay ALL_SYSTEM_PWRGD 2ms
DELAY_ALL_SYSTEM_PWRGD — R2529 @ 0Ohm
ALL_SYSTEM_PWRGD — R2530 0Ohm
H_VCCST_PWRGD_L
U2503 74AUP1G07GW 06V030000021
+3VSUS — C2504 0.1UF/16V
+VCCST_CPU — R2520 1KOhm
H_VCCST_PWRGD_R — R2521 1% 60.4Ohm — H_VCCST_PWRGD_MCP
C2505 0.1UF/16V @
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms

PEGATRON
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Title: PCH(6)_POWER MANAGE
BG1/HW3
Engineer: Andy Kao
Size C | Project Name X3 | Rev 1.0
Date: Monday, July 11, 2016 | Sheet 25 of 97

+1.0VSUS	+1.0VSUS	82
+VCCDSW	+VCCDSW	25,30
+1.8VSUS	+1.8VSUS	9,21,22,84
+VCCPAZIO	+VCCPAZIO	22
+VCC_RTC	+VCC_RTC	24,25,36,60
+VCCF24NS_1P0	+VCCF24NS_1P0	24
+3VSUS_ORG	+3VSUS_ORG	20,21,22,23,25
+3VSUS	+3VSUS	4,24,25,28,30,31,41,42,51,53,62,64,68,81,92

Table 10-5. SKL U / SKL Y PCH-LP VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

SATA Gen3 Port X 2
PCIe Gen2 Lane X 1
USB3 Port X 2
All HSIO disabled (basic comsunption)
=0.132x2+0.102+0.132x2+0.064 = 0.694A

2016.6.3
R1.2_10L ---Current rating

2016.6.13
R1.2_10L ---Follow megatron_KBL

Decoupling cap for internal power

U0301O
CPU POWER 4 OF 4
940432
01V010000015

Intel confirm pull down 1k

+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)

w/o DSW

if need choke, gate power should be disabled

MPHY_EXT_PWR_GATEB should pull high at A0 chip

U2601
SN10548

Iout =2.12A / ICC_Max 2.12A _CRB 0.53/TPCH17 TR<200us

2016.01.07
R1.2
Armani 2016 project for USB D+/D- short lesson learn solution (EC)

PEGATRON Title PCH(7)_POWER
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW3
Engineer: Andy Kao
Size C | Project Name X3 | Rev 1.0
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PEGATRON

Title : <Title>

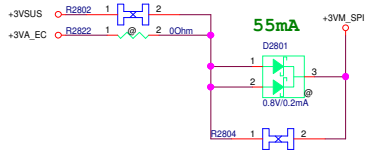
PEGATRON PROPRIETARY AND CONFIDENTIAL

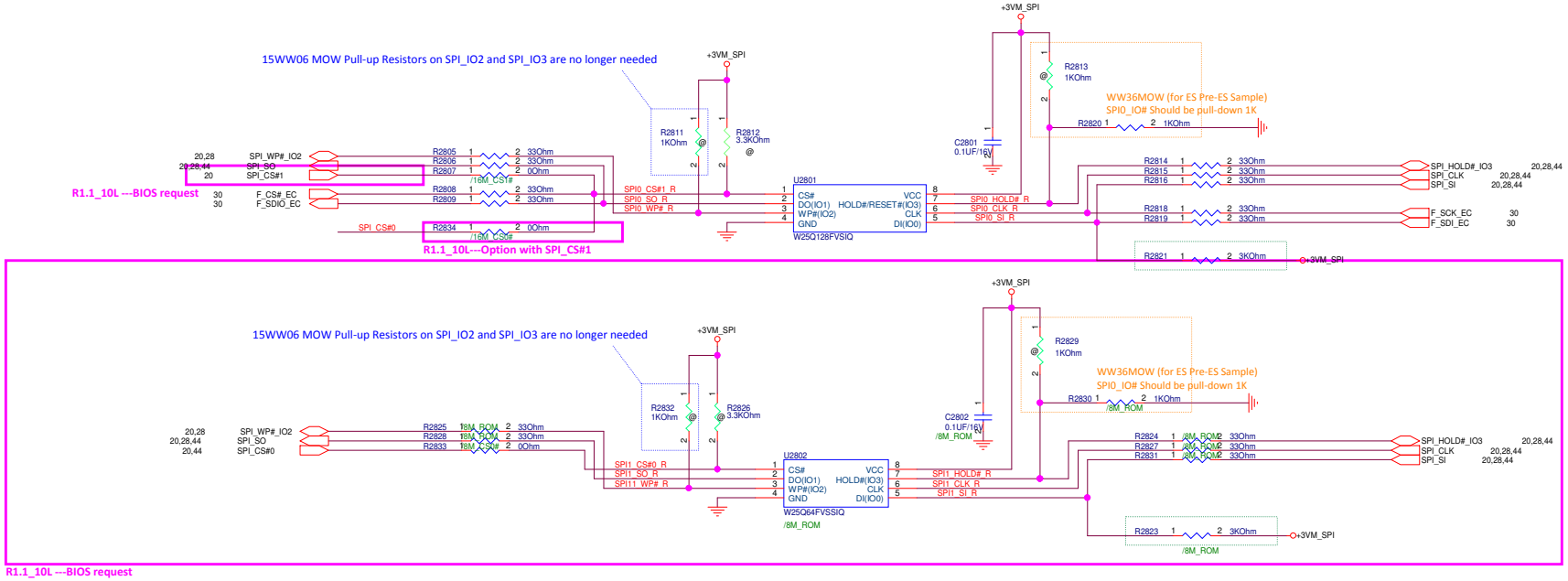
BG1/HW3

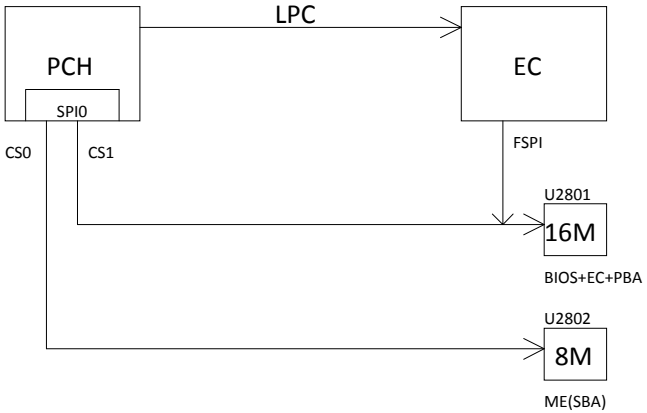
Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

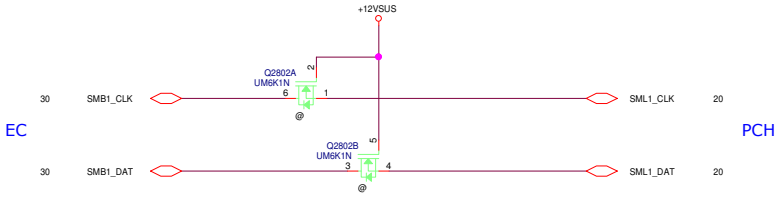
Date: Monday, July 11, 2016 Sheet 27 of 97







PCH SMBus



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCH(9)_SPI,SMB

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
C	X3	1.0

Date: Monday, July 11, 2016 Sheet 28 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

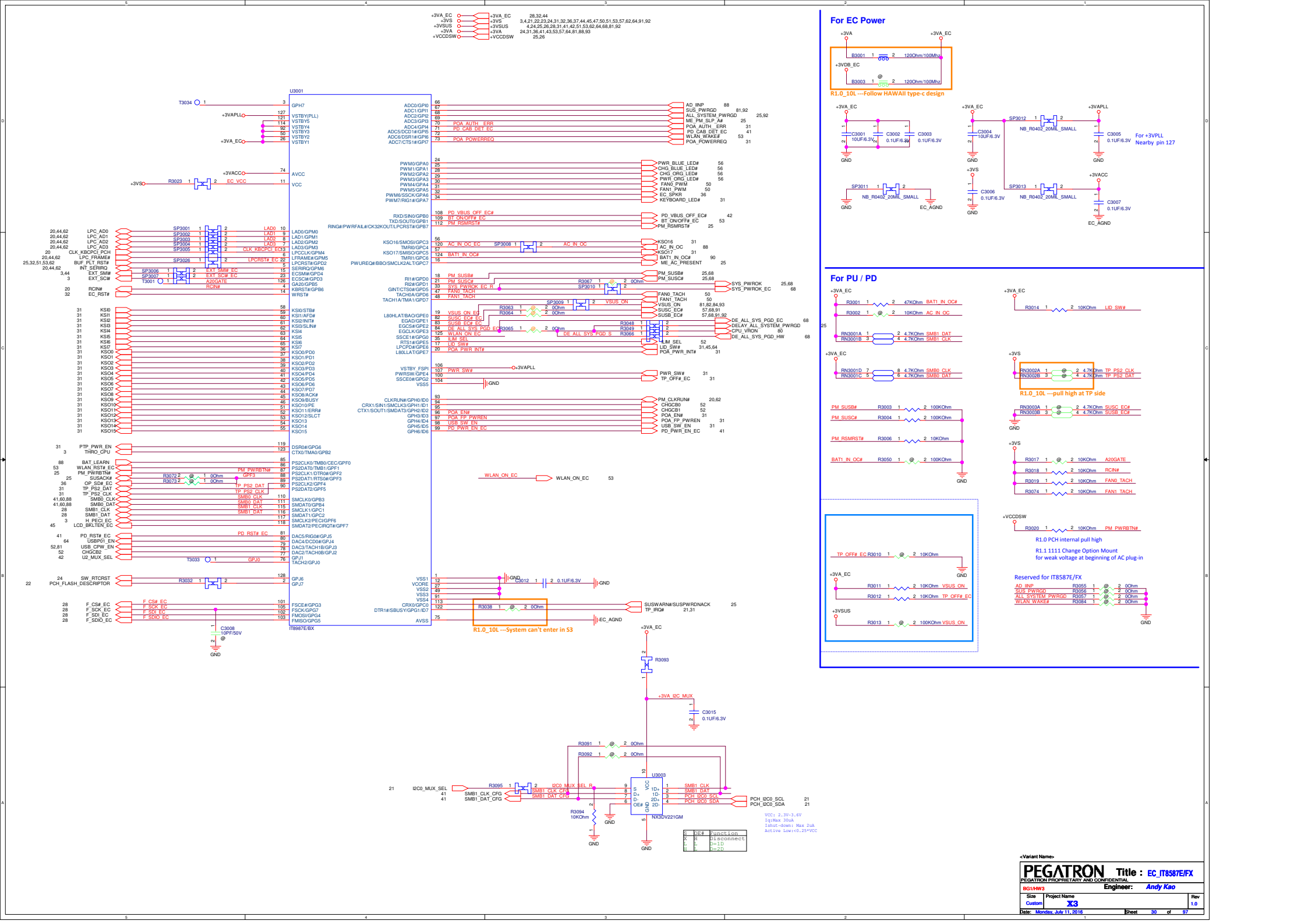
Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 29 of 97


For EC Power
R1.0_10L ---Follow HAWAII type-c design
For +3VPLL
Nearby pin 127
For PU / PD
R1.0_10L ---pull high at TP side
R1.0 PCH internal pull high
R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in
Reserved for IT8587E/FX
R1.0_10L ---System can't enter in S3
U3001
IT8987E/BX
U3003
NX3DV221GM
<Variant Name>
PEGATRON
Title : EC_IT8587E/FX
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Andy Kao
BG1HW3
Size: Custom
Project Name: X3
Rev: 1.0
Date: Monday, July 11, 2016
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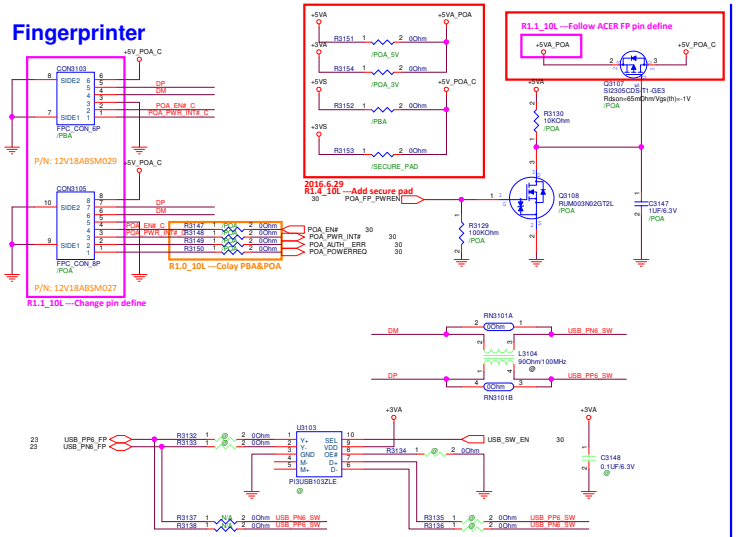
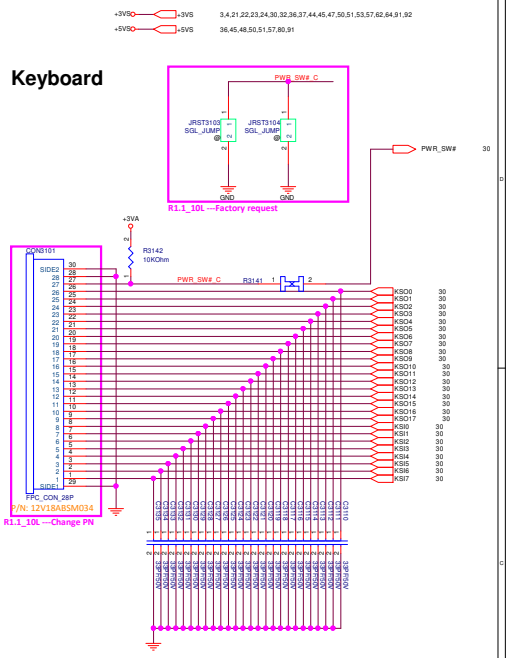
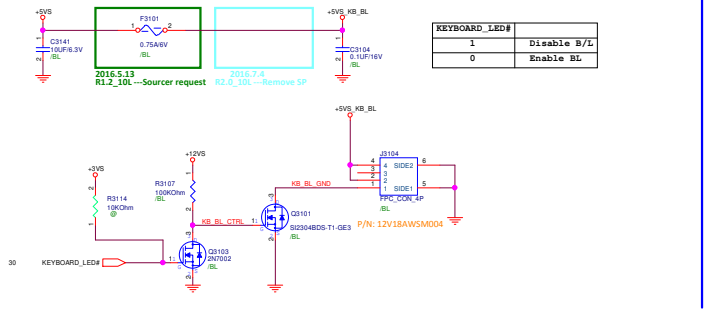
Fingerprinter



Keyboard

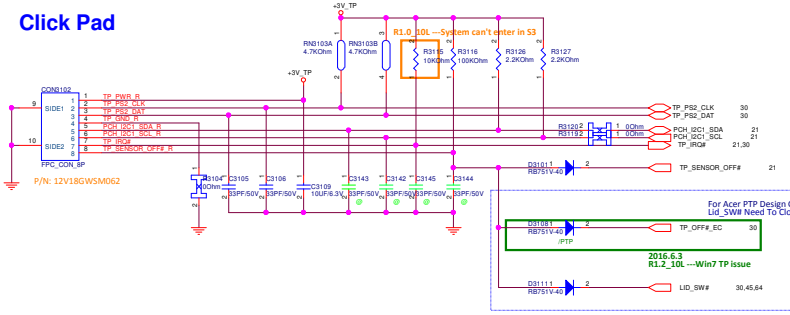


Keyboard LED

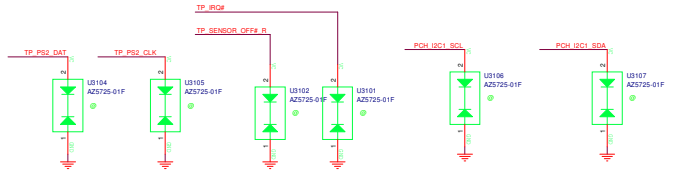


KEYBOARD_LED#	
1	Disable B/L
0	Enable BL

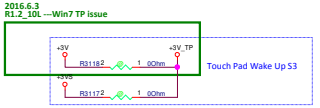
Click Pad

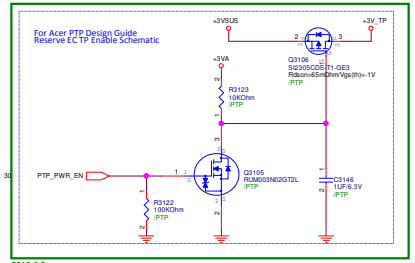


Reserve for EMI



2016.6.3
R1.2_10L ---Win7 TP issue





2016.6.3
R1.2_10L ---Win7 TP issue

PEGATRON	Title : EC_KB, TP	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3	Engineer: Andy Kao	
Size: Custom	Project Name: X3	Rev: 1.0
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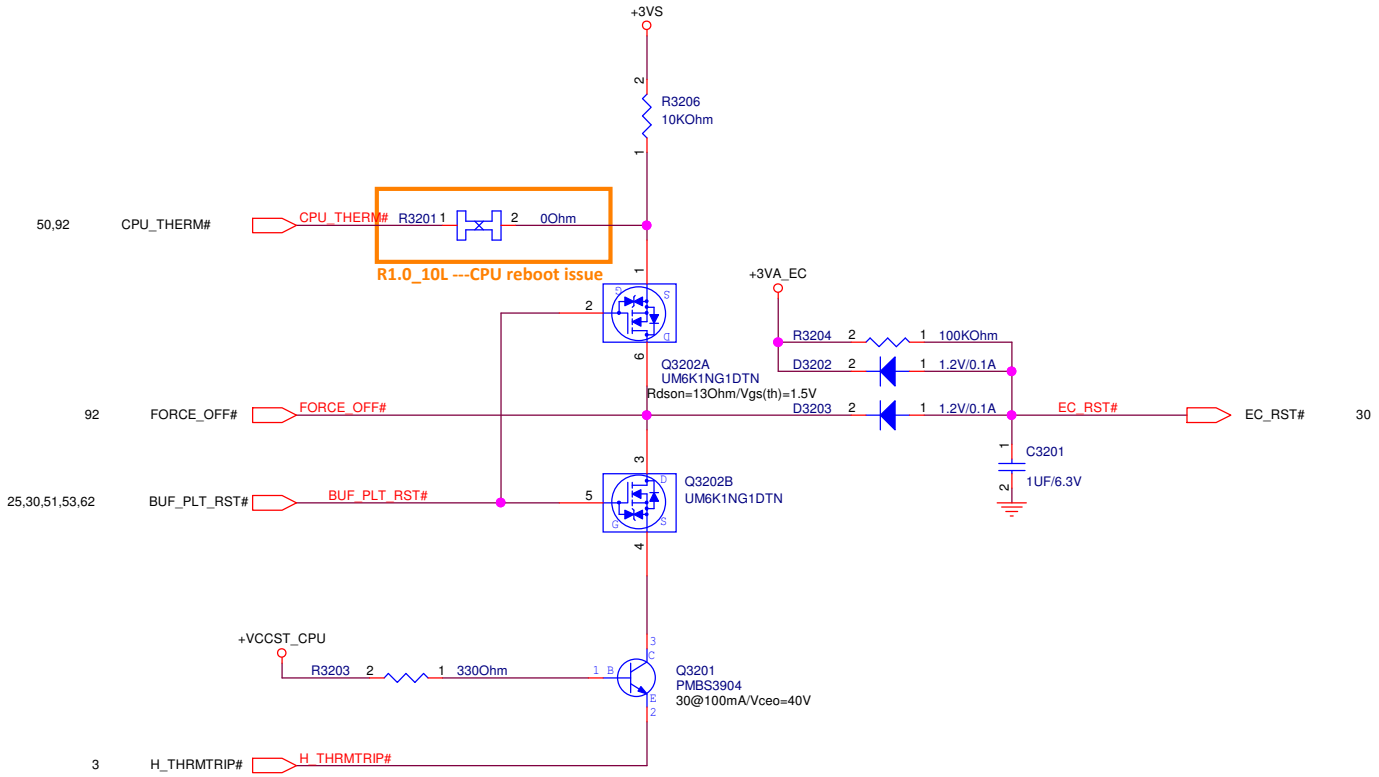
+VCCST_CPU — +VCCST_CPU 3,5,7,9,25

+3VA_EC — +3VA_EC 28,30,44

+3VS — +3VS 3,4,21,22,23,24,30,31,36,37,44,45,47,50,51,53,57,62,64,91,92



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 32 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

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PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

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PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

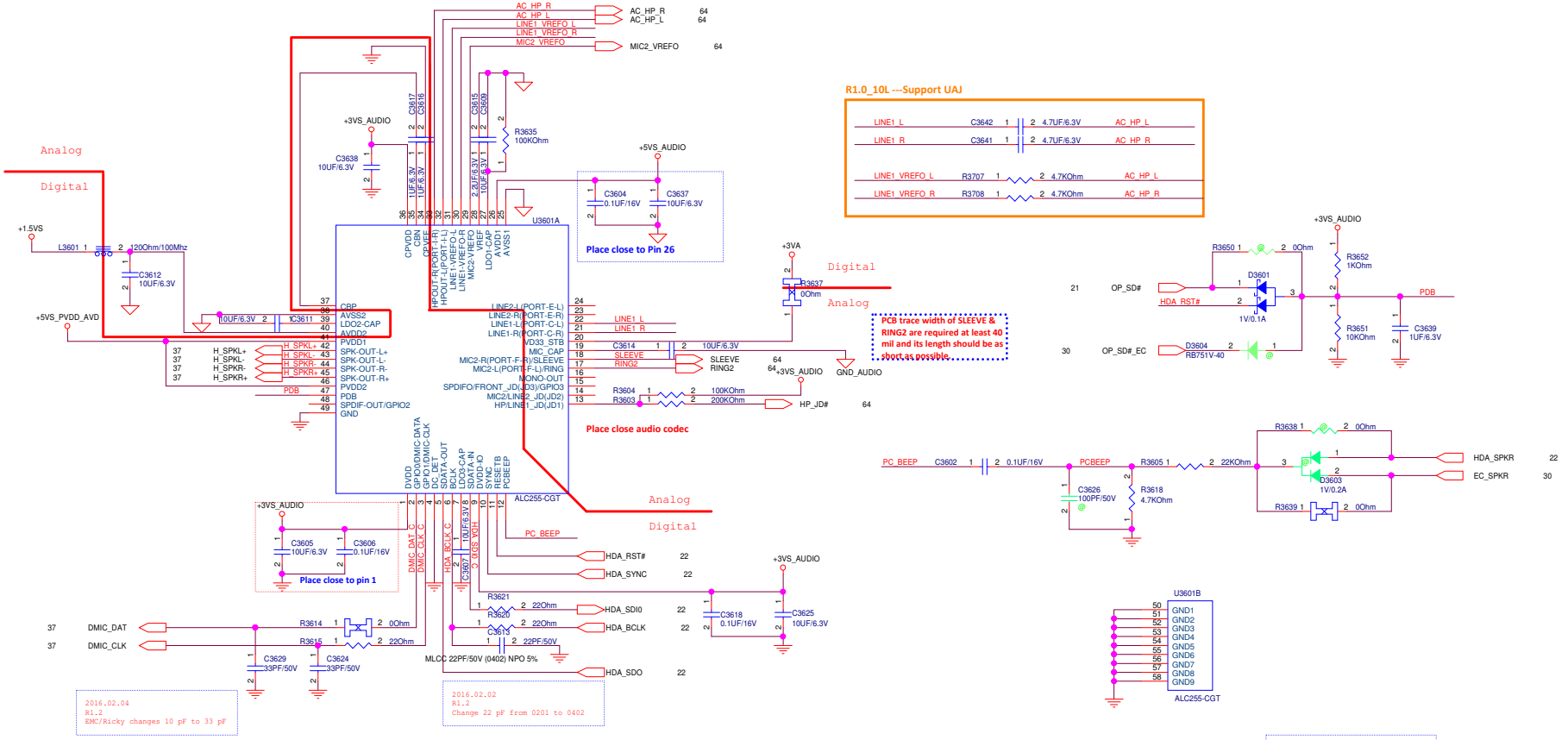
Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

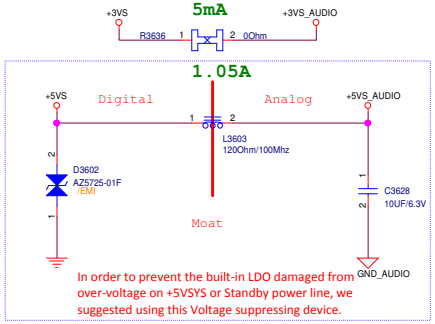
Date: Monday, July 11, 2016 Sheet 35 of 97

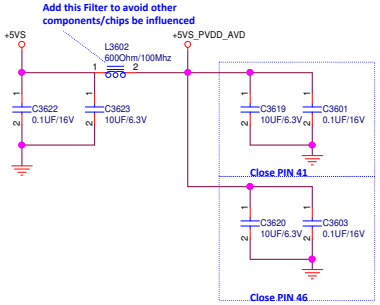
AUD_ALC255

+1.5VS → +1.5VS 47,57,85
+3VS → +3VS 3,4,21,22,23,24,30,31,32,37,44,45,47,50,51,53,57,62,64,91,92
+5VS → +5VS 31,45,48,50,51,57,80,91



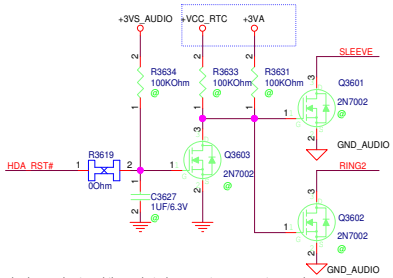
R1.0_10L ---Support UAJ



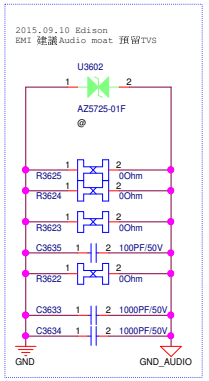


<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

Grounding circuit for combo jack SLEEVE pin

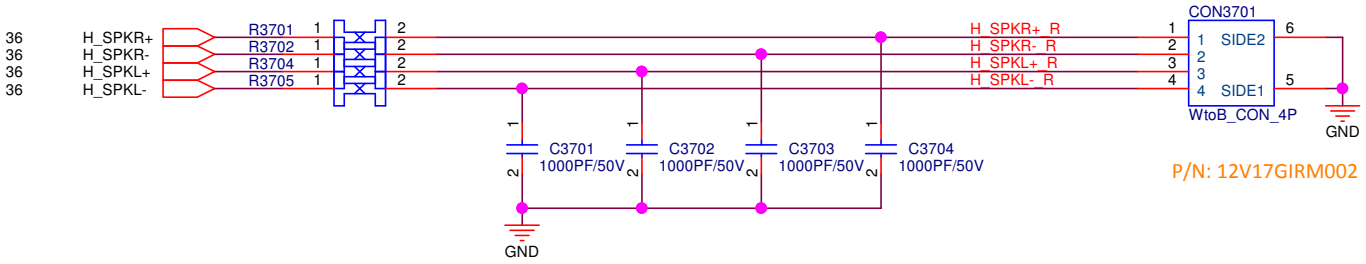


To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.



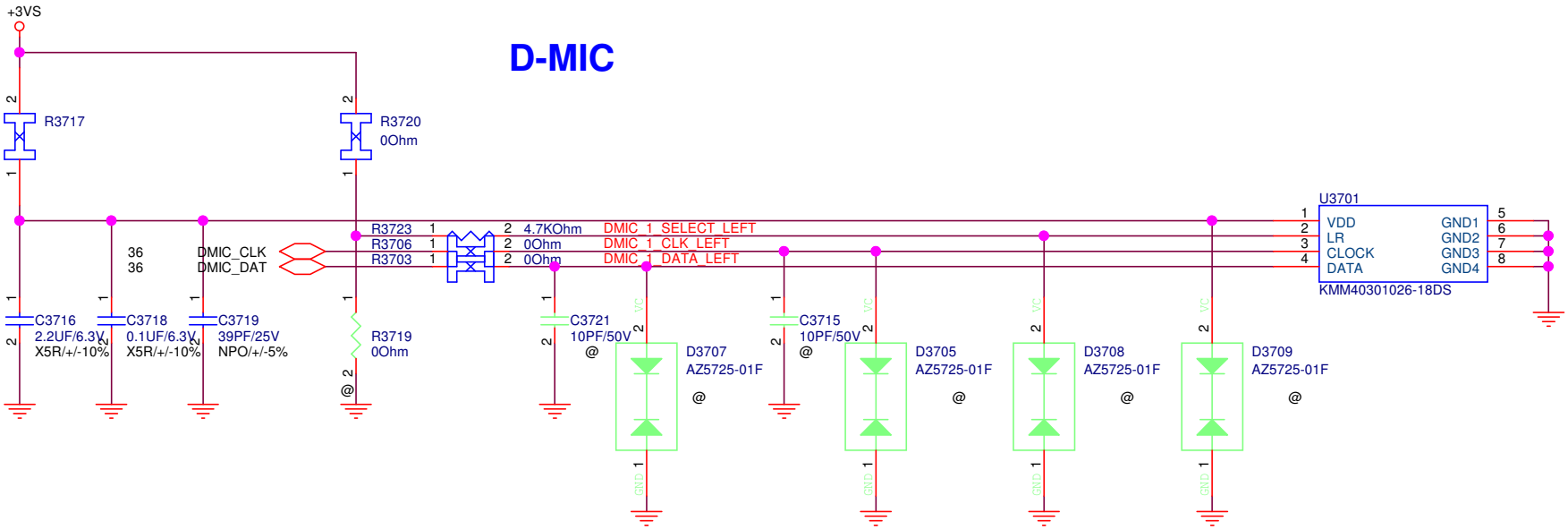
PEGATRON	Title : AUD_ALC255	
BG1/HW3	Engineer: Andy Kao	
Size: C	Project Name: X3	Rev: 1.0
Date: Monday, July 11, 2016	Sheet 36 of 97	

Speaker



P/N: 12V17GIRM002

D-MIC



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Speaker

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

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PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 38 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 39 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 40 of 97

ANX7428

2016.7.6
R2.0_10L ---Keep original design

+3VDB_PD — R4134 0Ohm vx_r0402_0ohm_small — +3VA_PD
+3VSUS — R4130 0Ohm vx_r0402_0ohm_small @
+3VA — R4126 0Ohm vx_r0402_0ohm_small @
+5VSUS — R4129 — V5_VCONN

VBUS_USB_TYPE_C	VBUS_USB_TYPE_C	42,43
+3VA	+3VA	24,30,31,36,43,53,57,64,81,88,93
+3VA_PD	+3VA_PD	42
+3VSUS	+3VSUS	4,24,25,26,28,30,31,42,51,53,62,64,68,81,92
+3VDB_PD	+3VDB_PD	43

V5_VCONN — C4118 10UF/6.3V @

TBD
+3VA_PD — R4123 100KOHM vx_r0402_small — DDI2_AUXN_C
DDI2_AUXP_C — R4124 100KOHM vx_r0402_small

C4101 1UF/16V vx_c0402_small — C4102 0.1UF/6.3V — C4100 1000PF/50V vx_c0402_small — +3VA_PD
+3VA_PD — C4104 1UF/16V vx_c0402_small — C4105 0.1UF/6.3V — C4103 1000PF/50V vx_c0402_small

The DVDD_IO can be power supplied by 1.8V ~ 3.3V:
If AP's IO type is 1.8V, select 1.8V power for DVDD_IO;
If AP's IO type is 3.3V, select 3.3V power for DVDD_IO.

V5_VCONN is the power source for VCONN(UTC_B5_CC2 or UTC_A5_CC1).
Please make sure:
1) VCONN Voltage range [4.75V, 5.5V]
2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.

Reverse voltage protection is required.
It might be necessary to add a diode to protect the power supply.

Requirement of Q3:
1) Id >= 500mA (Vgs = - 4.5V).
2) Ron < 120 mOhm (Vgs = - 4.5V).
3) Max Vds >= -10V

Connect to DP Source

3	DDI2_TXP0	1	DP_LN_0P
3	DDI2_TXN0	2	DP_LN_0N
3	DDI2_TXP1	7	DP_LN_1P
3	DDI2_TXN1	8	DP_LN_1N
3	DDI2_TXP2	9	DP_LN_2P
3	DDI2_TXN2	10	DP_LN_2N
3	DDI2_TXP3	3	DP_LN_3P
3	DDI2_TXN3	4	DP_LN_3N
3	DDI2_AUXP	16	AUXP
3	DDI2_AUXN	17	AUXN
3	DDI2_HPD	37	HPD

C4116 0.1UF/16V vx_c0402_small DDI2_AUXP_C
C4117 0.1UF/16V vx_c0402_small DDI2_AUXN_C
PD_HPD (P.P)

Connect to USB3.0 signals

23	USB3_TXN3	11	SSTX_N
23	USB3_TXP3	12	SSTX_P
23	USB3_RXN3	5	SSRX_N
23	USB3_RXP3	6	SSRX_P

30 PD_RST#_EC (From EC:) — R4125 2 1 100KOhm — 33 RESET_N
23 NC

+3VA_PD — R4135 1.8KOHM — R4136 1.8KOHM — CFG_SDA — CFG_SCL
42 PD_VBUS_CTRL — R4120 4.7KOhm vx_r0402_small @ — +3VA_PD
30,60,88 SMB0_DAT
30,60,88 SMB0_CLK
R4127 0Ohm vx_r0402_0ohm_small @ SMB_DAT_PD
R4128 0Ohm vx_r0402_0ohm_small @ SMB_CLK_PD
38 CFG_SDA
39 CFG_SCL
43 M_SCL/GPIO_4
42 M_SDA/GPIO_5

30 SMB1_DAT_CFG
30 SMB1_CLK_CFG
R4133 — R4132 — CFG_SDA — CFG_SCL

M_SDA/GPIO_5 pin:
Connect to AP/CPU/Charge IC as a charge mode indicator.

Logic 0: Fast Charger Mode, charge voltage > 5V or charge current >= 1.5A.

Logic 1: Normal Charger Mode, charge voltage = 5V and charge current <1.5A.

+3VA_PD — R4109 4.7KOhm vx_r0402_small — DRP_EN — R4112 4.7KOhm vx_r0402_small @
DRP_EN pin:
Logic 1: DRP Mode.
Logic 0: DFP Mode.
34 TEST_EN
28 DRP_EN

I2C_ADR_0 — R4118 — VBUS_DISCHARGE_CTRL 42
Int. PD 47 I2C_ADR_1/GPIO_3
Int. PD 48 I2C_ADR_0/INTP_IN/GPIO_2
ANX7428QN-AB-R

Change to 0650-0084000

I2C_ADR_1/GPIO_3 pin: Connected to AP or CPU as UART TXD
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used as software UART output after OCM boot.

I2C_ADR_0/INTP_IN/GPIO_2:
Connect to AP or CPU to control the discharge of VBUS.
1. Don*t care before reset released.
2. Used to config the I2C address right after reset released.
3. Used for VBUS discharge control after OCM boot.

U4100B
50 AVSS_1
51 AVSS_2
52 AVSS_3
53 AVSS_4
54 AVSS_5
55 AVSS_6
56 AVSS_7
57 AVSS_8
ANX7428QN-AB-R

I2C Address Selection:

I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

I2C_ADR_1 and I2C_ADR_0 pin:
1. The I2C address is determined approximately 500ns after RESET_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C_ADR_0 and I2C_ADR_1 pins.
3. If external pull-up resistor is not populated, the I2C_ADR_0 or I2C_ADR_1 is logic 0.
4. If external pull-up is populated, the I2C_ADR_0 or I2C_ADR_1 is logic 1.

U4100A

25	SSTXP1		
26	SSTXN1		
35	SSRXN2		
36	SSRXP2		
30	SSTXP2		
29	SSTXN2		
32	SSRXN1		
31	SSRXP1		
19	SBU1		
18	SBU2		
21	CC1		CHIP_CC1
45	VCONN1_EN/GPIO_0		VCONN1_EN
22	CC_CAP		CC_CAP
20	CC2		CHIP_CC2
44	VCONN2_EN/GPIO_1		VCONN2_EN
15	VBUS_DIV6		VBUS_DIV6
41	INTP_OUT		(Default: O.D)
14	CABLE_DET		
27	PWR_EN		

SSTXP1	UTC_A2_SSTXp1	42
SSTXN1	UTC_A3_SSTXn1	42
SSRXN2	UTC_A10_SSRXn2	42
SSRXP2	UTC_A11_SSRXp2	42
SSTXP2	UTC_B2_SSTXp2	42
SSTXN2	UTC_B3_SSTXn2	42
SSRXN1	UTC_B10_SSRXn1	42
SSRXP1	UTC_B11_SSRXp1	42
SBU1	UTC_A8_SBU1_AUX	42
SBU2	UTC_B8_SBU2_AUX	42

Connect to USB Type-C connector

CHIP_CC1 — R4102 — UTC_A5_CC1 42
VCONN1_EN
CC_CAP — C4106 1000PF/16V @ vx_c0201
CHIP_CC2 — R4105 — UTC_B5_CC2 42
VCONN2_EN
VBUS_USB_TYPE_C — R4107 750KOhm — VBUS_DIV6 — R4110 150KOhm 1% vx_r0402_small
INTP_OUT — PD_INT# — T4101
CABLE_DET — R4113 — PD_CAB_DET_EC 30
PWR_EN — PD_PWR_EN_EC 30 — R4122 100KOhm

V5_VCONN — R4103 100KOHM vx_r0402_small — U4101 TPS2041BDBVR (IN, OUT, GND, EN#, OC#)
V5_VCONN — R4121 100KOHM vx_r0402_small — U4102 TPS2041BDBVR (IN, OUT, GND, EN#, OC#)

0629-007K000
VIN: 2.7V-5.5V
Iq:Max 190uA
Ishut-down: Max 1uA
Active Low:<0.6V
ILMIT:0.6A-0.8A-1.0A

INTP_OUT pin: interrupt output.
Connect to AP or CPU.

If AP or GPU's interrupt is low level triggered, set R16 = 4.7K, leave R22 not installed;
else if is high level triggered, set R22 =4.7K, leave R16 not installed.

CABLE_DET pin: Connect to AP or CPU.
Logic 1: USB Type-C cable plug detected.
Logic 0: USB Type-C cable unplug detected.

Note:
1. Set R21 = 100K, C15 = 22nF to filter the short high toggle pulse in DRP mode when cable is unplugged in ES chip.
2. Set R21 to 0R, C15 to DNP when this is fixed in CS chip.

PWR_EN pin:
Controlled by AP or CPU
Logic 1: to power up the chip.
Logic 0: to power down the chip.

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_FLOWCHART
Engineer: Andy Kao

Size	Project Name	Rev
C	X3	1.0

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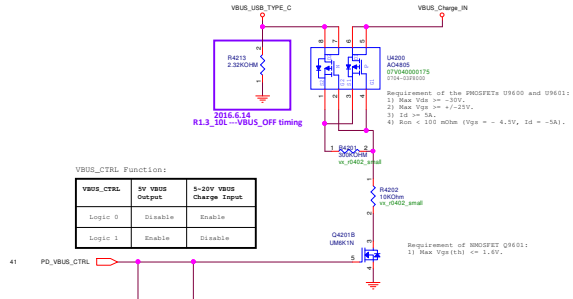
VBUS Control

Optional:
If PMIC can detect VBUS presence and disable/enable VBUS, the VBUS control circuit can be removed.

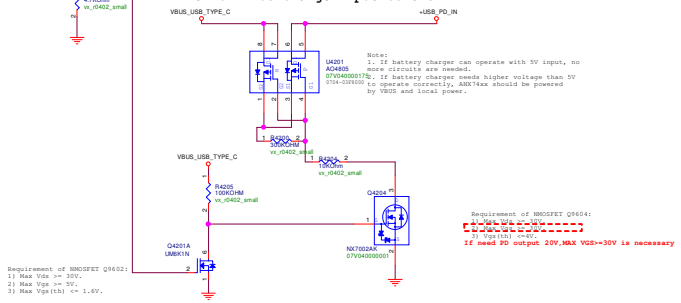
5V VBUS Output Control



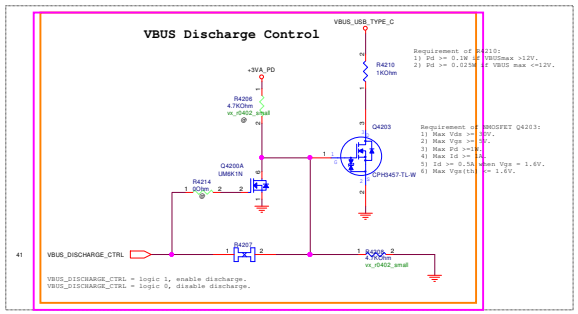
VBUS_CTRL Function:

VBUS_CTRL	5V VBUS Output	5~20V VBUS Charge Input
Logic 0	Disable	Enable
Logic 1	Enable	Disable

5~20V VBUS Charge Input Control

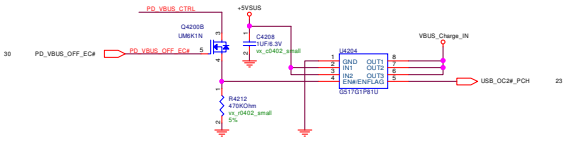


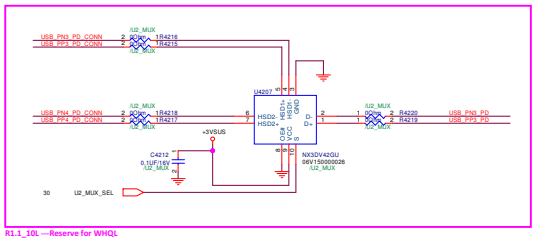
VBUS Discharge Control



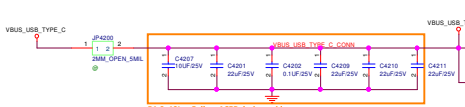
R1.0_10L ---Unmount discharge circuit

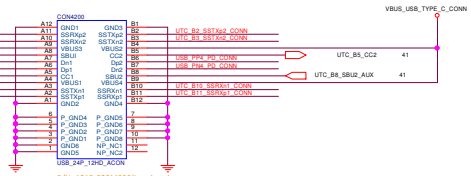
R1.1_10L ---PD test fail



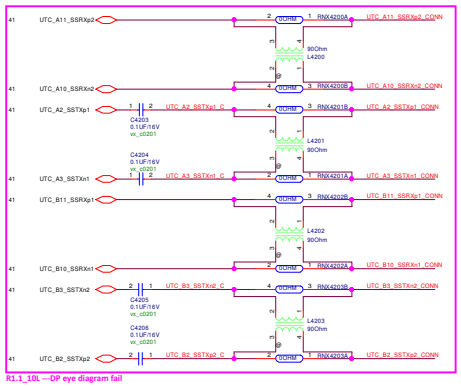


R1.1_10L ---Reserve for WHQL

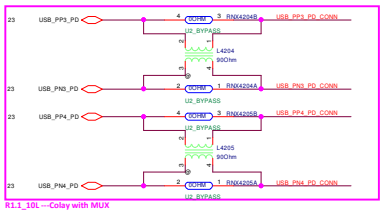




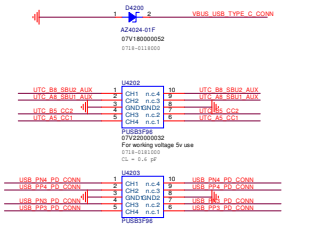
ESD



R1.1_10L ---DP eye diagram fail

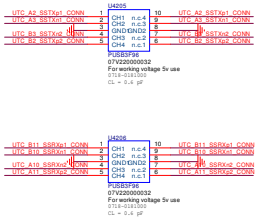


R1.1_10L ---Colay with MUX



USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1



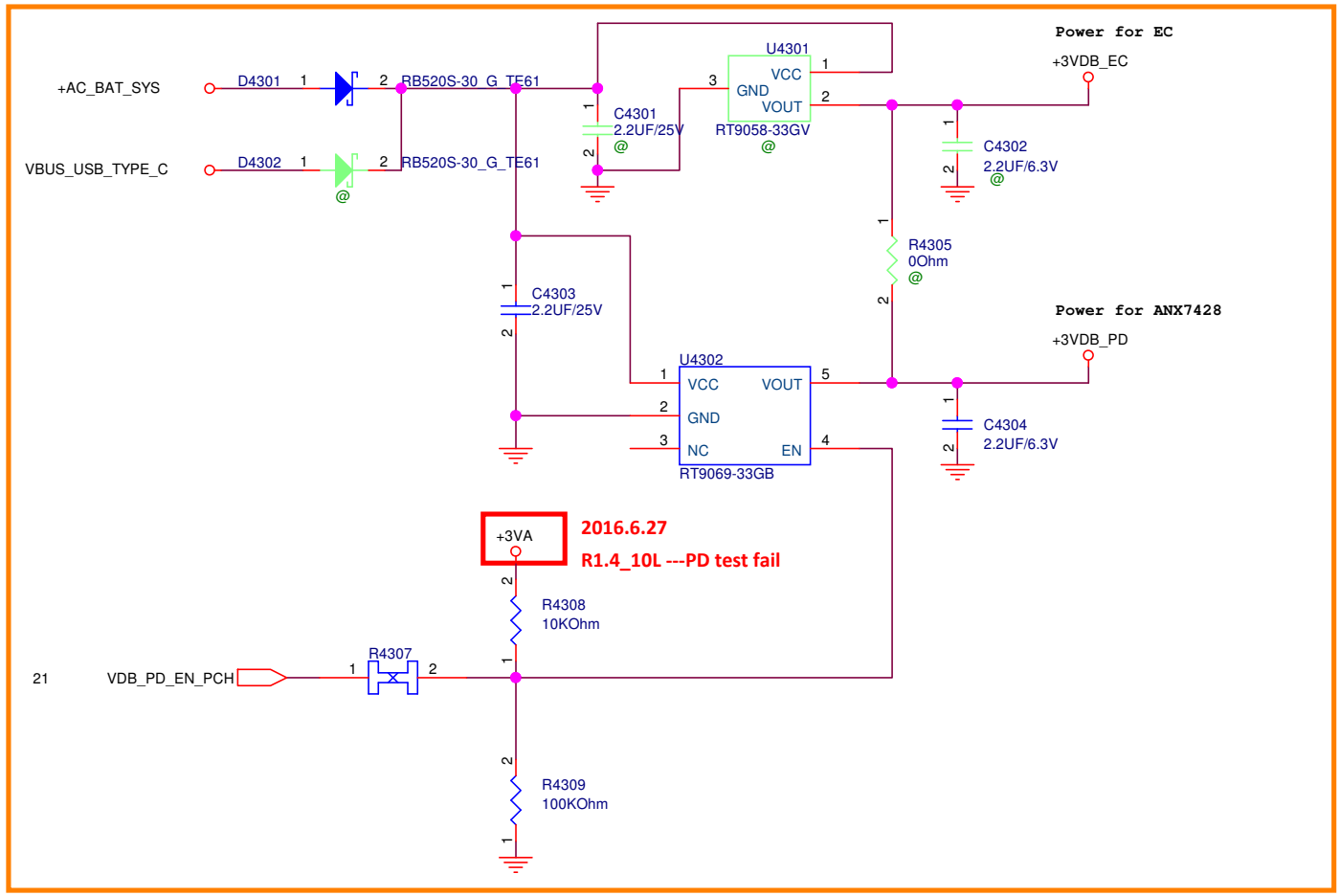
Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C	VBUS_USB_TYPE_C	41,42	
+AC_BAT_SYS	+AC_BAT_SYS	45,80,81,82,83,88	
+3VDB_EC	+3VDB_EC	30	
+3VDB_PD	+3VDB_PD	41	

Requirement of U1:
1) Vin range: 4V-30V.
2) Vout: EC's operating voltage + Vf of D1
3) Output current >= EC's operating current.

R1.0_10L ---Follow HAWAII type-c design



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

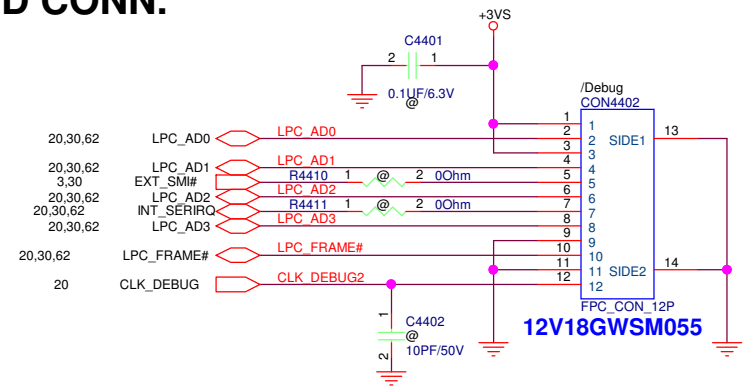
Title : Dead Battery

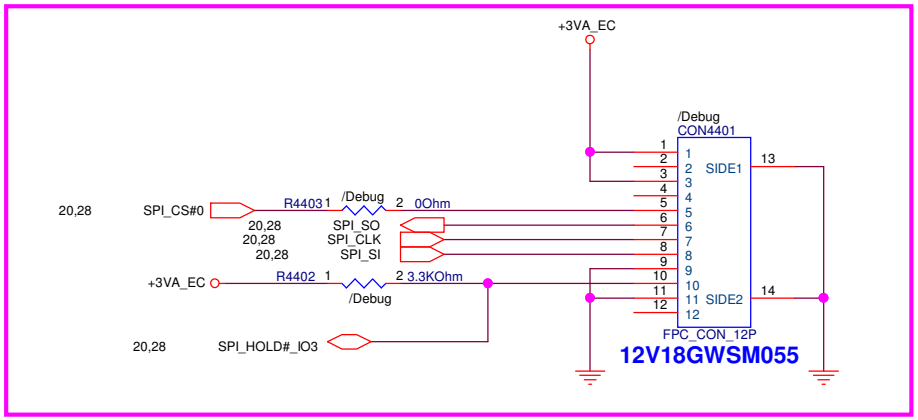
Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 43 of 97

DEBUG CARD CONN.





R1.1_10L ---BIOS request

<Variant Name>

PEGATRON Title : DEBUG CONN.

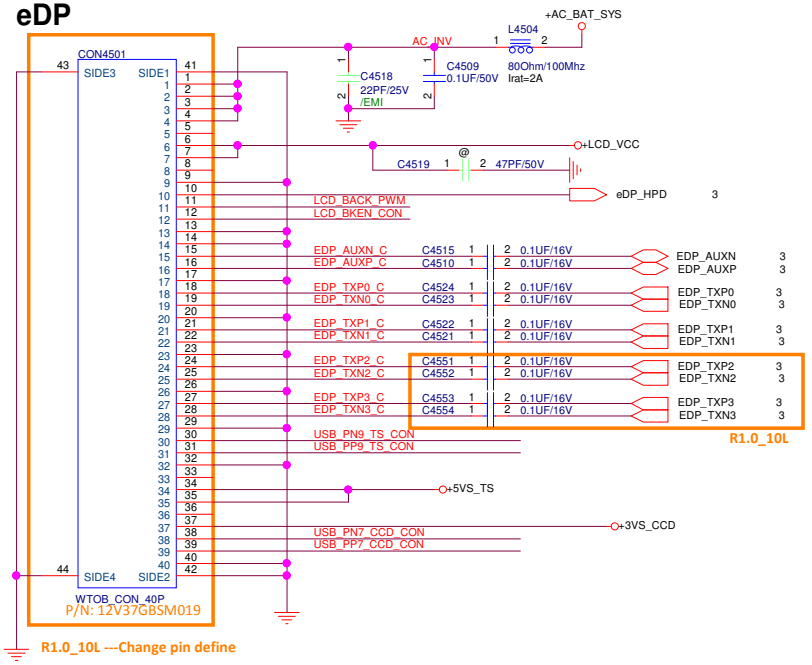
PEGATRON PROPRIETARY AND CONFIDENTIAL

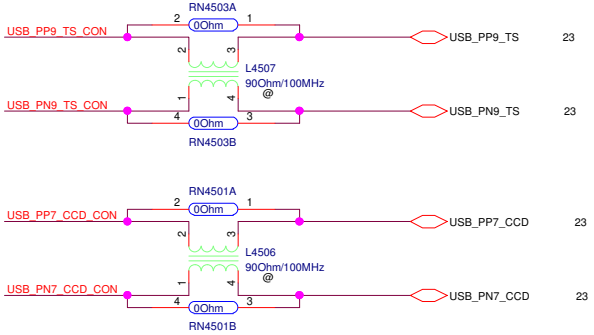
BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

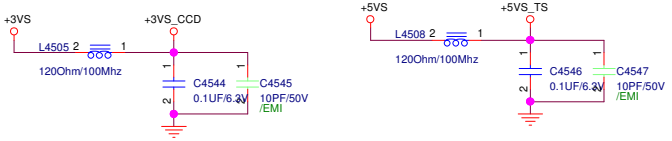
Date: Monday, July 11, 2016 Sheet 44 of 97

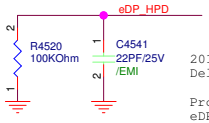
eDP





Camera

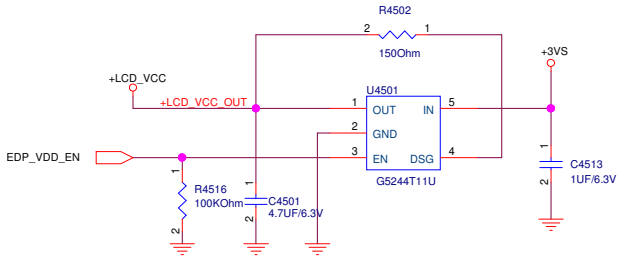


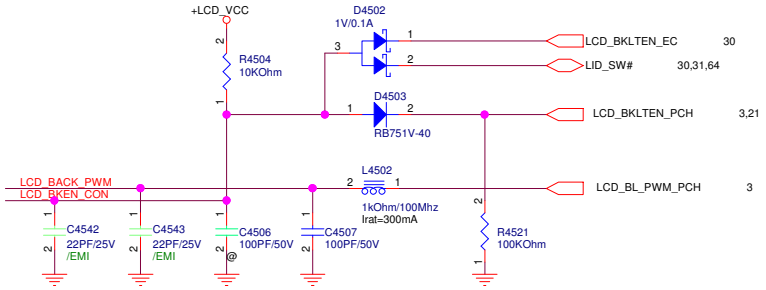


2015.04.14 YenPin
Delete eDP_HPD Pull High Path

Processor DisplayPort* Disabling and Termination Guidelines Checklist
eDP_HPD pull down to ground via 100K ohm resistor

LCD VDDEN / +LED_VCC





<Variant Name>

PEGATRON Title : eDP CONN

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 45 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 46 of 97

T4702 1 PRE

Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

T4701 1 EQ

Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

T4703 1 ISET

TMDS output swing adjustment; Internal pull down at ~150k, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%

+3VS_PS — R4725 4.7KOhm @ — PRE — R4726 4.7KOhm @ — GND (Vendor)
+3VS_PS — R4727 4.7KOhm @ — EQ — R4728 4.7KOhm @ — GND (Vendor)
+3VS_PS — R4729 4.7KOhm @ — ISET — R4730 4.7KOhm @ — GND (Vendor)

+3VS — R4718 — +3VS_PS

+1.5VS — R4721 — +1P5VS_PS

R1.1_10L ---Follow megatron

+3VS_PS — R4710 4.7KOhm — DDCBUF — R4714 4.7KOhm @ — GND

Enable active DDC buffer; Internal pull down at ~150KΩ, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor

SCL_SRC
SDA_SRC

3 DDPB_CTRLCLK — HDMI_SCL_PCH — R4733 — SCL_SRC
3 DDPB_CTRLDATA — HDMI_SDA_PCH — R4732 — SDA_SRC

1 T4704

U4701A — PS8201ATQFN40GTR2-A0

3 DDI1_TXP2	C4729 0.1UF/16V	HDMI_TXP2_PS	IN_D2p
3 DDI1_TXN2	C4730 0.1UF/16V	HDMI_TXN2_PS	IN_D2n
		HPD_SRC	HPD_SRC
3 DDI1_TXP1	C4731 0.1UF/16V	HDMI_TXP1_PS	IN_D1p
3 DDI1_TXN1	C4732 0.1UF/16V	HDMI_TXN1_PS	IN_D1n
3 DDI1_TXP0	C4733 0.1UF/16V	HDMI_TXP0_PS	IN_D0p
3 DDI1_TXN0	C4734 0.1UF/16V	HDMI_TXN0_PS	IN_D0n
			I2C_CTL_EN
3 DDI1_CLKP	C4727 0.1UF/16V	HDMI_CLKP_PS	IN_CKp
3 DDI1_CLKN	C4728 0.1UF/16V	HDMI_CLKN_PS	IN_CKn

OUT_D2p	30	HDMI_TXP2 48
OUT_D2n	29	HDMI_TXN2 48
HPD_SNK	28	DP1_HPD_CON 48
OUT_D1p	27	HDMI_TXP1 48
OUT_D1n	26	HDMI_TXN1 48
OUT_D0p	25	HDMI_TXP0 48
OUT_D0n	24	HDMI_TXN0 48
CFG	23	CFG R4715 2 @ 1 4.7KOhm +3VS_PS
	22	
OUT_CKp	21	HDMI_CLKP 48
OUT_CKn		HDMI_CLKN 48

IO_HDMI_SCL 48
IO_HDMI_SDA 48

+1P5VS_PS — C4704 0.1UF/6.3V — GND
+3VS_PS — C4705 0.01UF/16V — GND
+1P5VS_PS — C4701 0.01UF/16V — GND

Configuration pin, 3.3V IO, internal pull down at ~150k. 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable

(Typ:1.5V ; Max:1.53V ; Min:1.47V)

3 DDI1_HPD — DDI1_HPD — R4731 — HPD_SRC

+3VS_PS — R4717 4.7KOhm @ — DCIN_EN
+1P5VS_PS — R4701 4.99KOhm — EQ
+1P5VS_PS — C4706 0.1UF/6.3V — GND
+1P5VS_PS — C4707 0.1UF/6.3V — GND
+1P5VS_PS — C4708 0.1UF/6.3V — GND
+3VS_PS — C4709 0.1UF/6.3V — GND
+1P5VS_PS — C4710 0.01UF/16V — GND

DC coupling enable; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

U4701B — PS8201ATQFN40GTR2-A0

42	EPAD1	EPAD8	49
43	EPAD2	EPAD7	48
44	EPAD3	EPAD6	47
45	EPAD4	EPAD5	46

GND GND

R1.1_10L ---Sourcer request

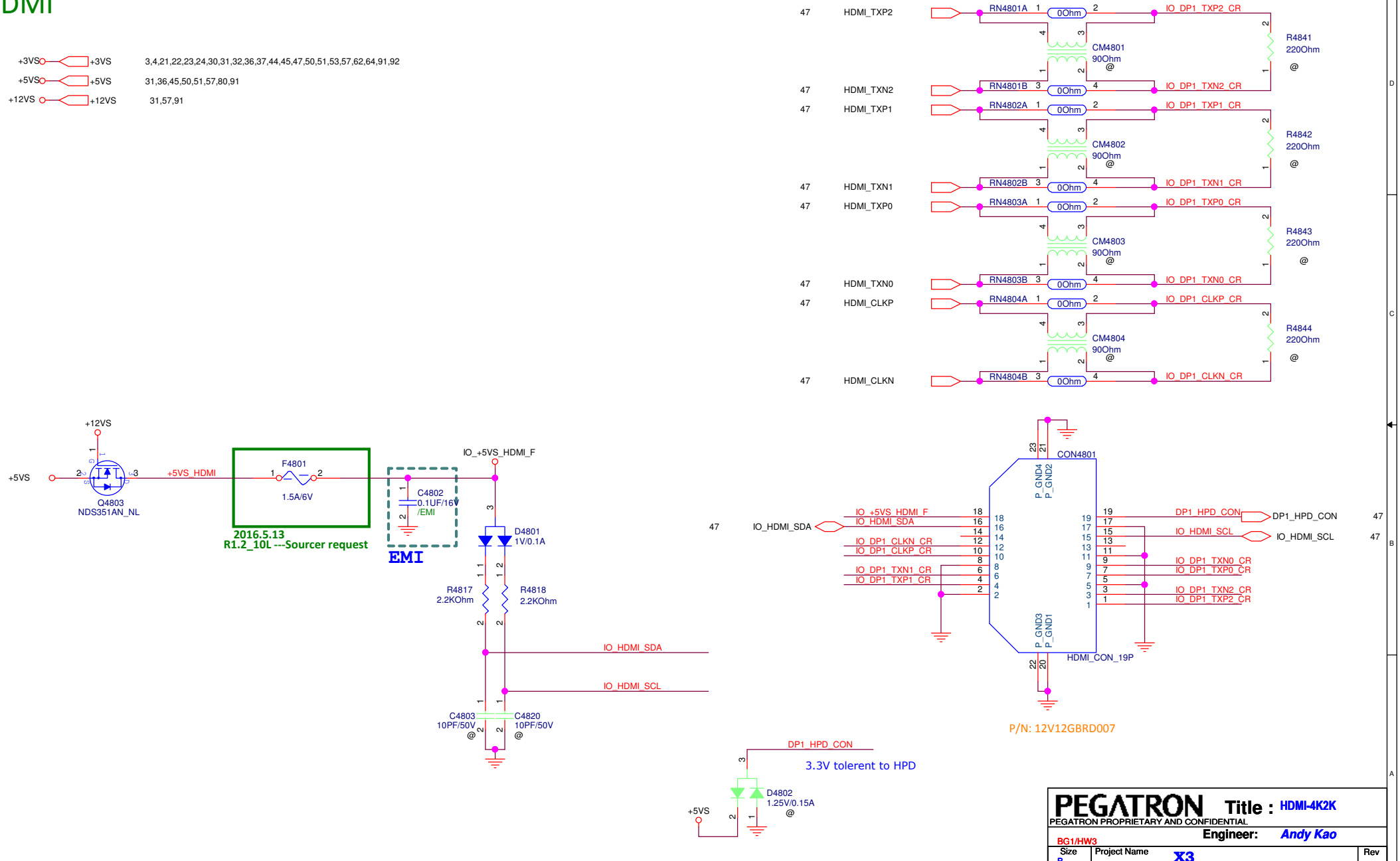
PEGATRON Title : HDMI-4K2K
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Andy Kao
BG1/HW3
Size C | Project Name X3 | Rev 1.0
Date: Monday, July 11, 2016 | Sheet 47 of 97

HDMI

+3VS → +3VS 3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92

+5VS → +5VS 31,36,45,50,51,57,80,91

+12VS → +12VS 31,57,91



PEGATRON Title : HDMI-4K2K

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Andy Kao

BG1/HW3

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 48 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

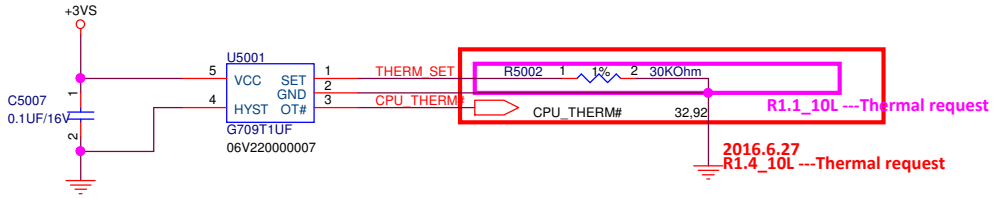
Size	Project Name	Rev
A	X3	1.0

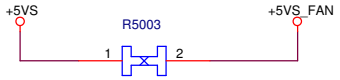
Date: Monday, July 11, 2016 Sheet 49 of 97

Thermal Sensor

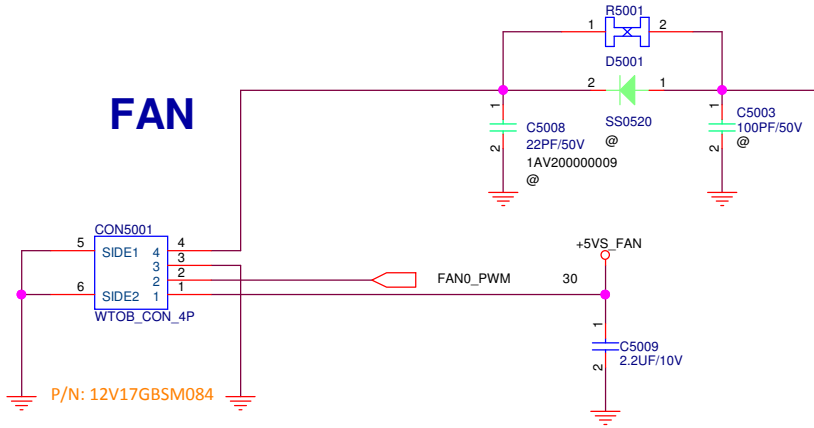
temp setting : 80 degree

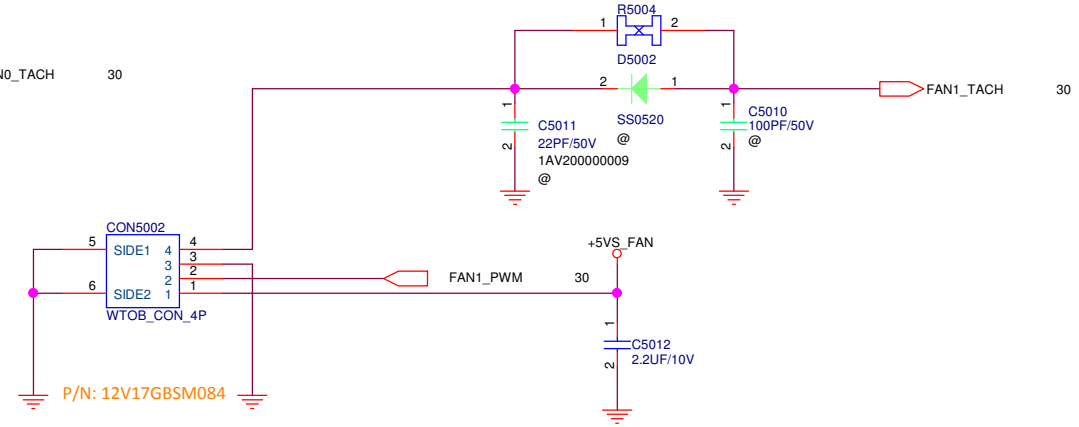
RSET(kΩ)= 0.0012T*T - 0.9308T + 96.147





FAN





<Variant Name>

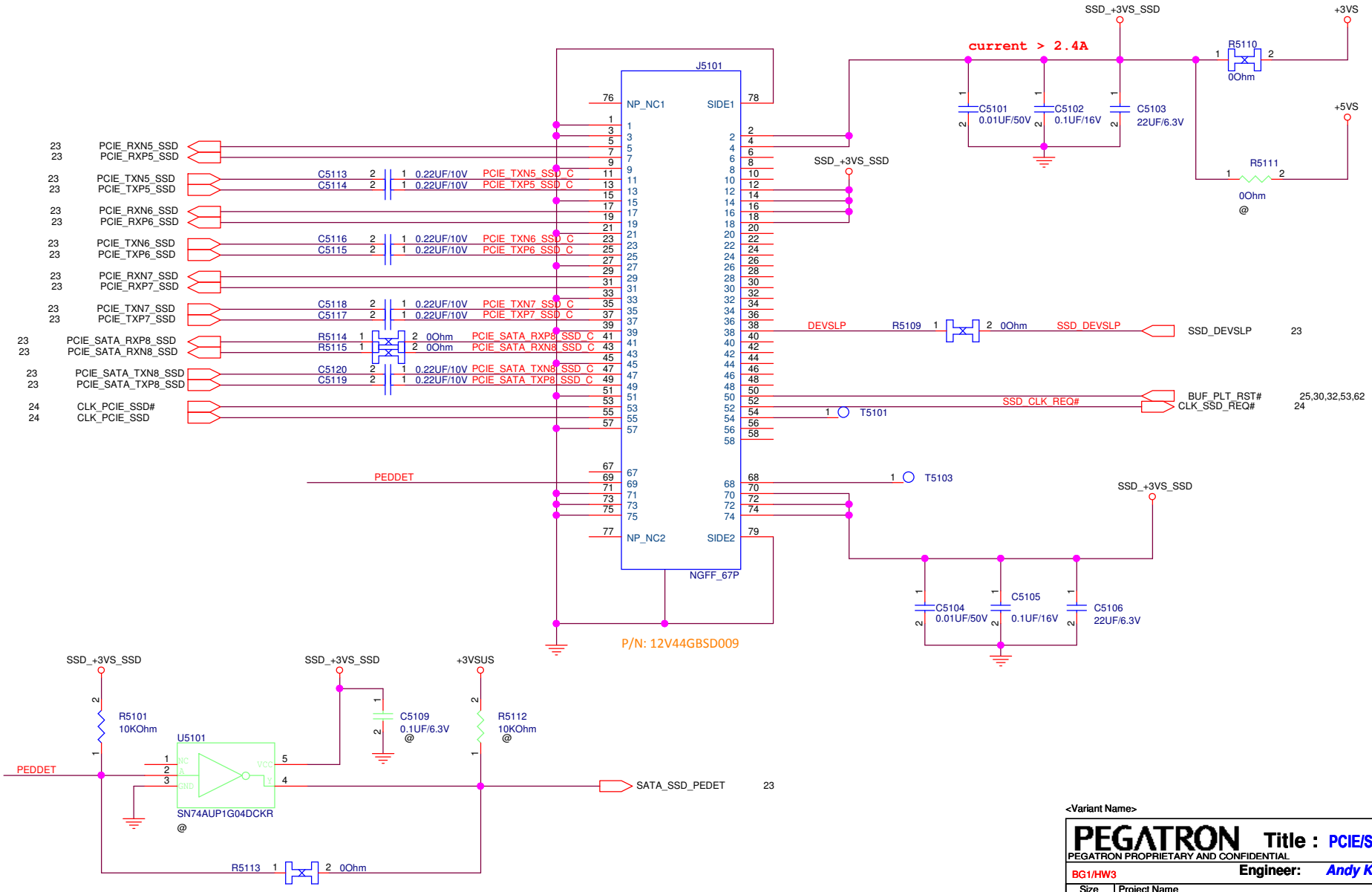
PEGATRON Title : Thermal/Fan

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 50 of 97

SSD(SATA/PCIE x4) NGFF socket (M-key)



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PCIE/SATA SSD

BG1/HW3

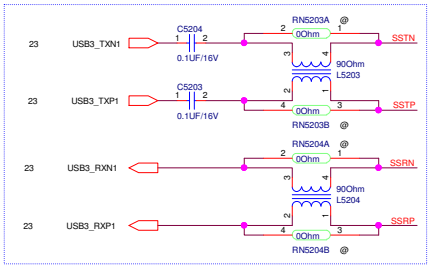
Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

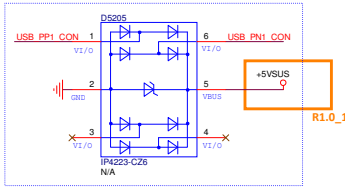
Date: Monday, July 11, 2016 Sheet 51 of 97

USB 3.0

USB3.0 Choke

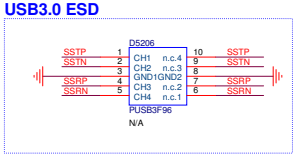


USB2.0 ESD

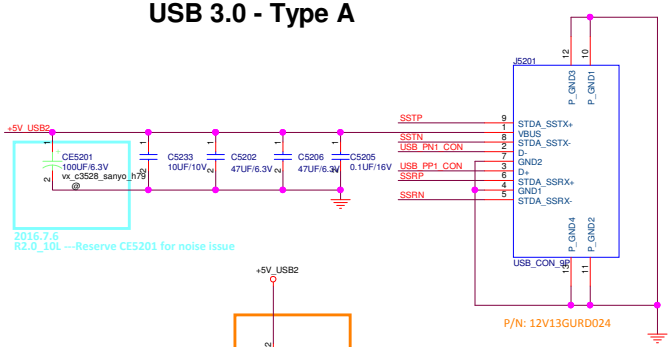


R1.0_10L ---Iphone charge issue

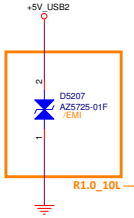
USB3.0 ESD



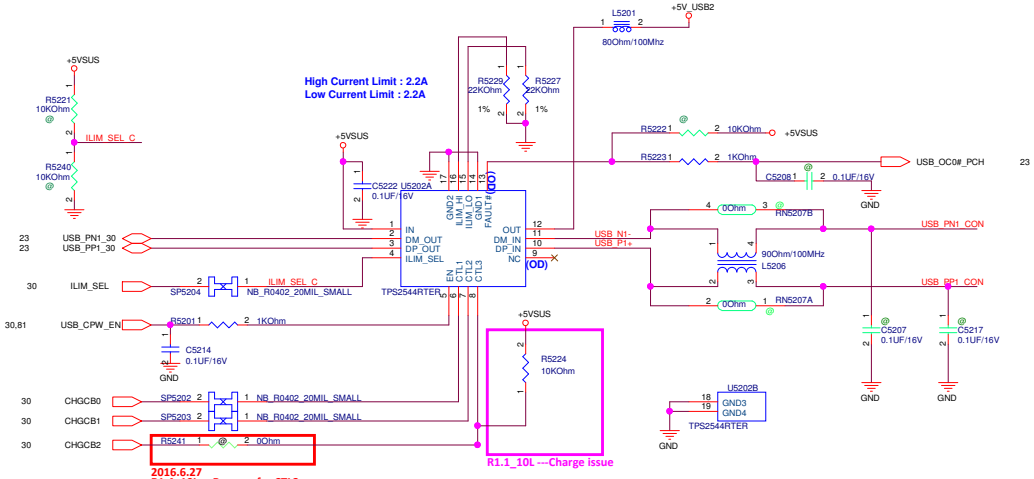
USB 3.0 - Type A



2016.7.6
R2.0_10L ---Reserve CE5201 for noise issue



R1.0_10L ---For EMI

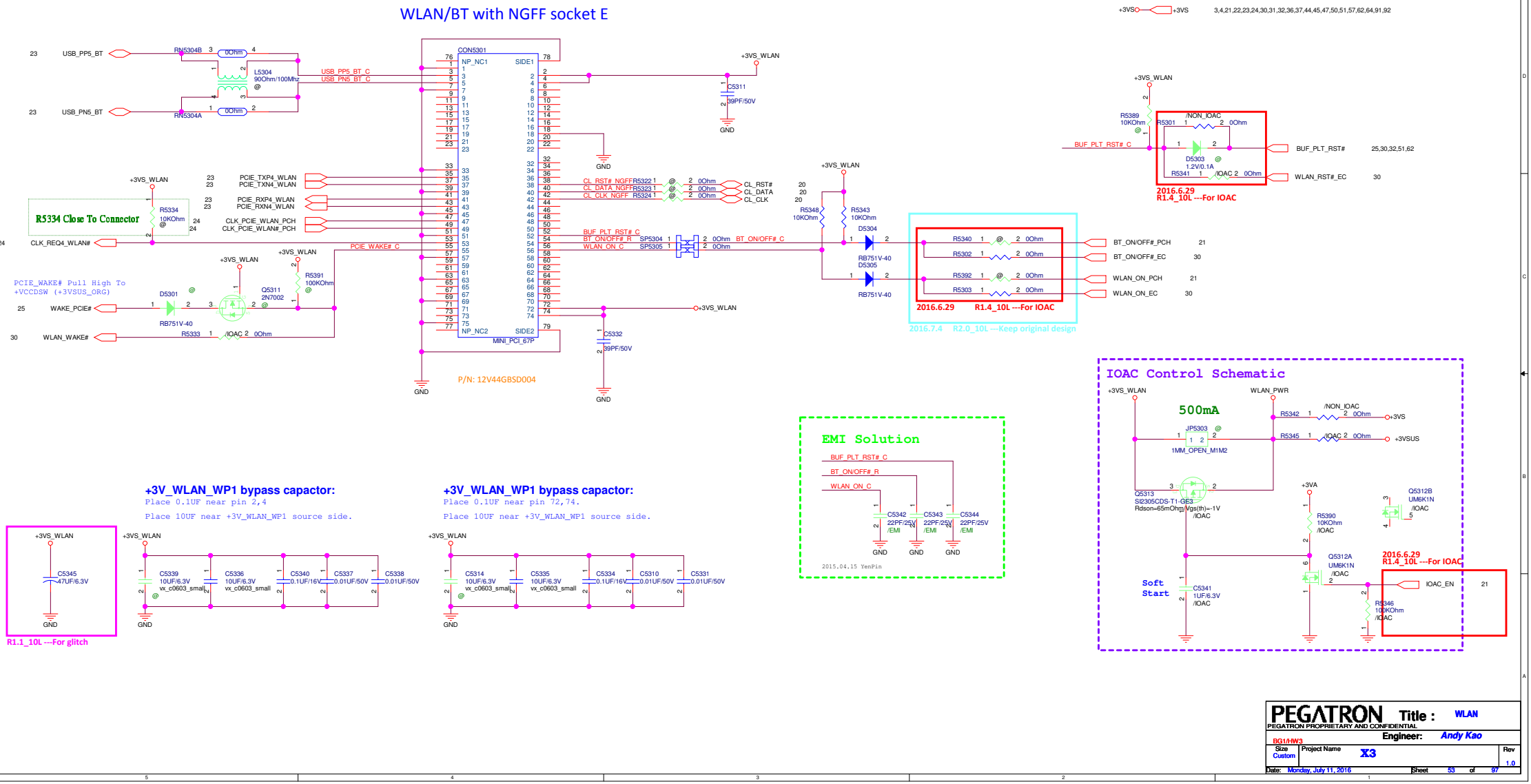


2016.6.27
R1.4_10L ---Reserve for CTL3

R1.1_10L ---Charge issue

PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : USB JACK
	Engineer: Andy Kao
BG1/HW3	
Size: Custom	Project Name: X3
Rev: 1.0	
Date: Monday, July 11, 2016	Sheet 52 of 97

WLAN/BT with NGFF socket E



+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

Place 10UF near +3V_WLAN_WP1 source side.

+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.

EMI Solution

IOAC Control Schematic

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : WLAN

Engineer: Andy Kao

BG1/HW3

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 53 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB HUB

<OrgName>

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 54 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

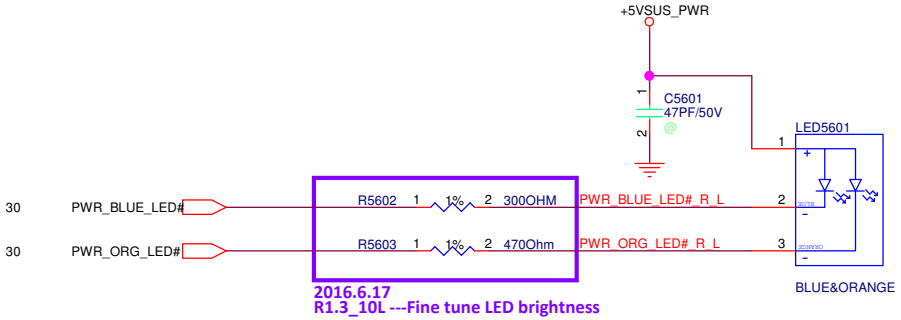
BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

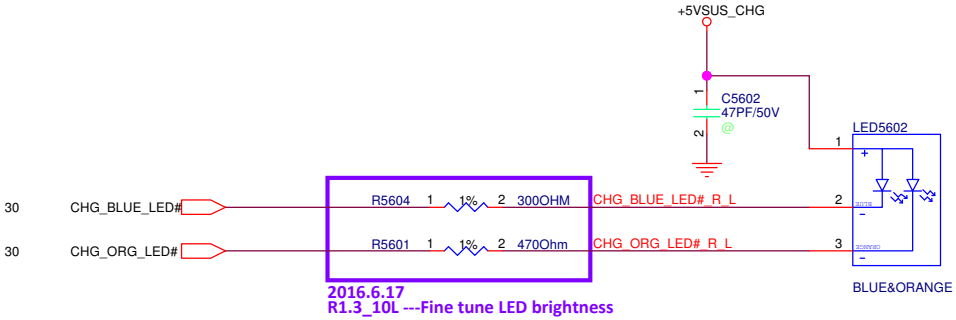
Date: Monday, July 11, 2016 Sheet 55 of 97

POWER LED

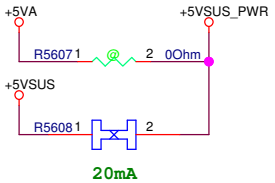


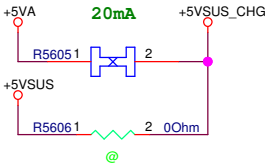
2016.6.17
R1.3_10L ---Fine tune LED brightness

Charger LED



2016.6.17
R1.3_10L ---Fine tune LED brightness





<Variant Name>

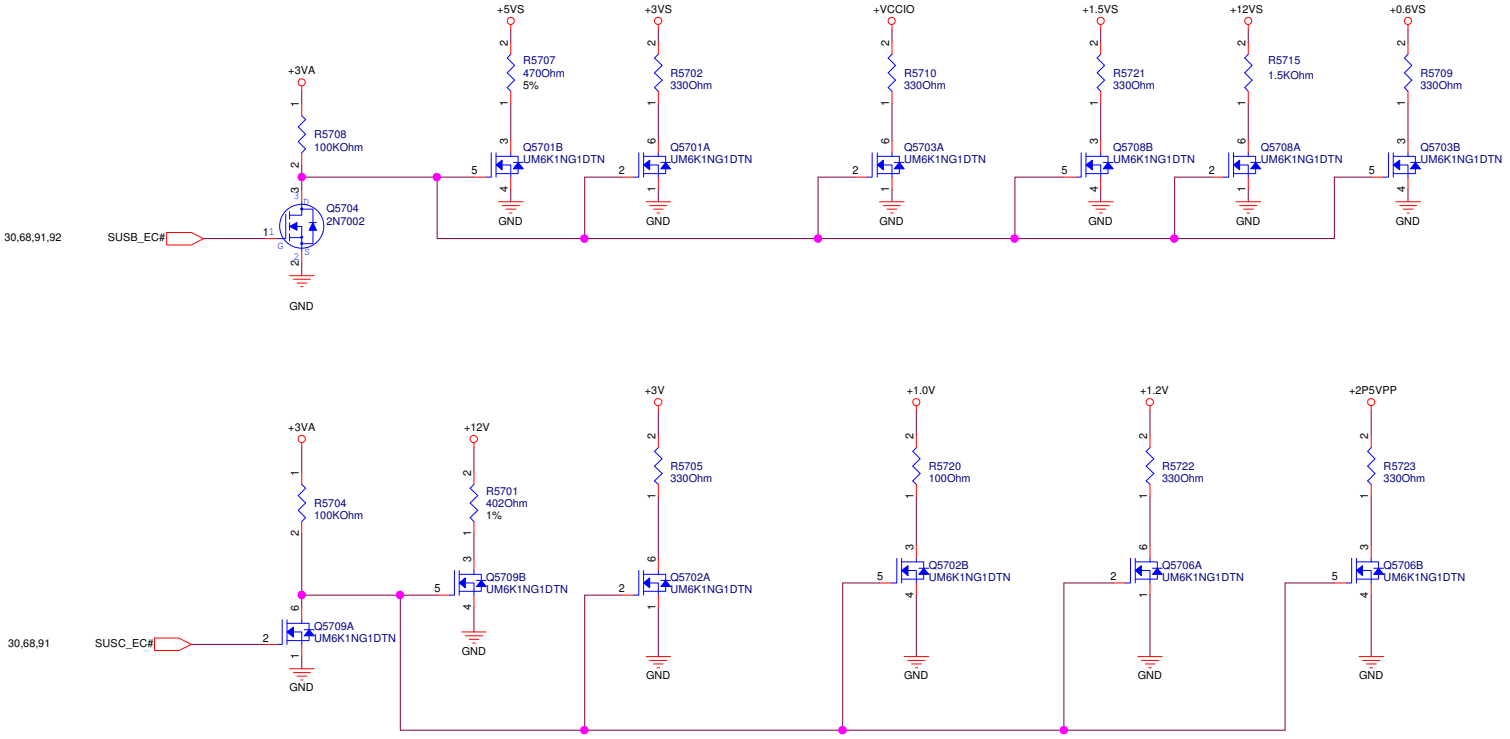
PEGATRON Title : LED_Indicator
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 56 of 97

Discharge Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DISCHARGE CKT

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 57 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 58 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

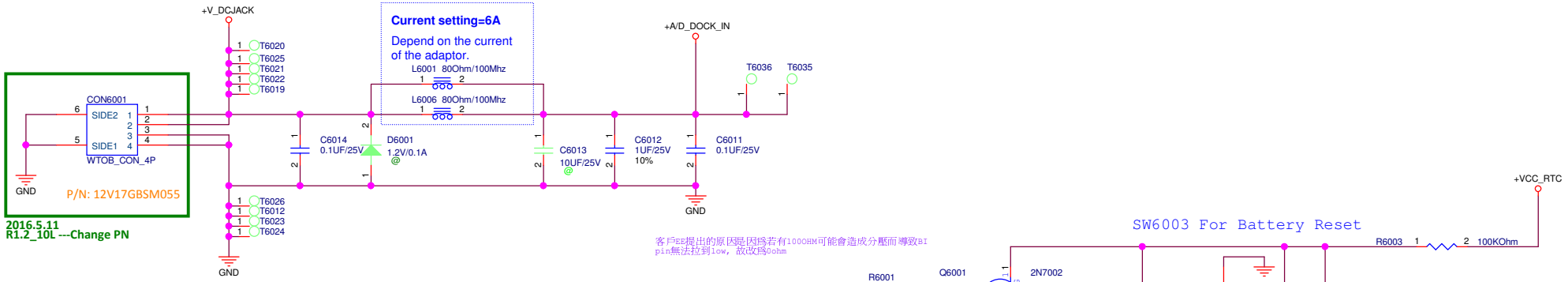
BG1/HW3

Engineer: *Andy Kao*

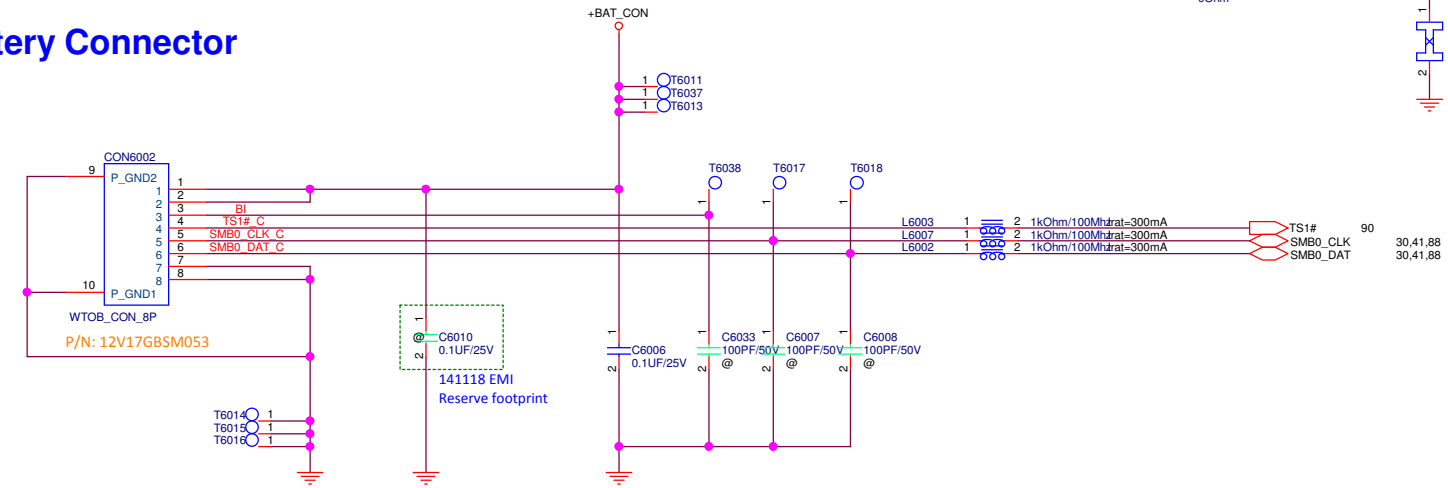
Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 59 of 97

DC Jack WtoB CONN



Battery Connector



PEGATRON	Title : DC_IN/BAT CONN	
BG1/HW3	Engineer: Andy Kao	
Size: Custom	Project Name: X3	Rev: 1.0
Date: Monday, July 11, 2016	Sheet 60 of 97	

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

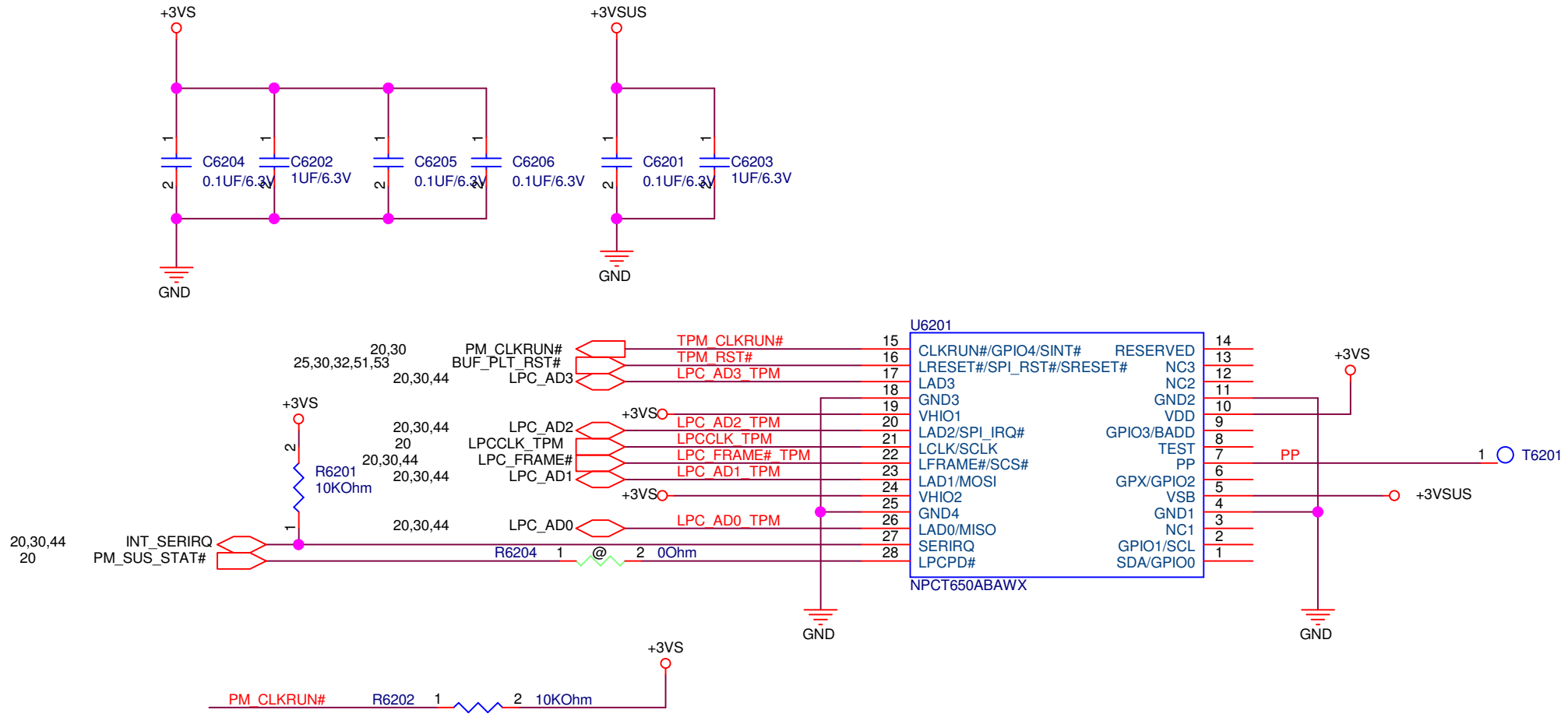
Title : <Title>

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 61 of 97



Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

PEGATRON

Title : TPM CONN

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

Date: Monday, July 11, 2016 Sheet 62 of 97

PEGATRON

Title : <Title>

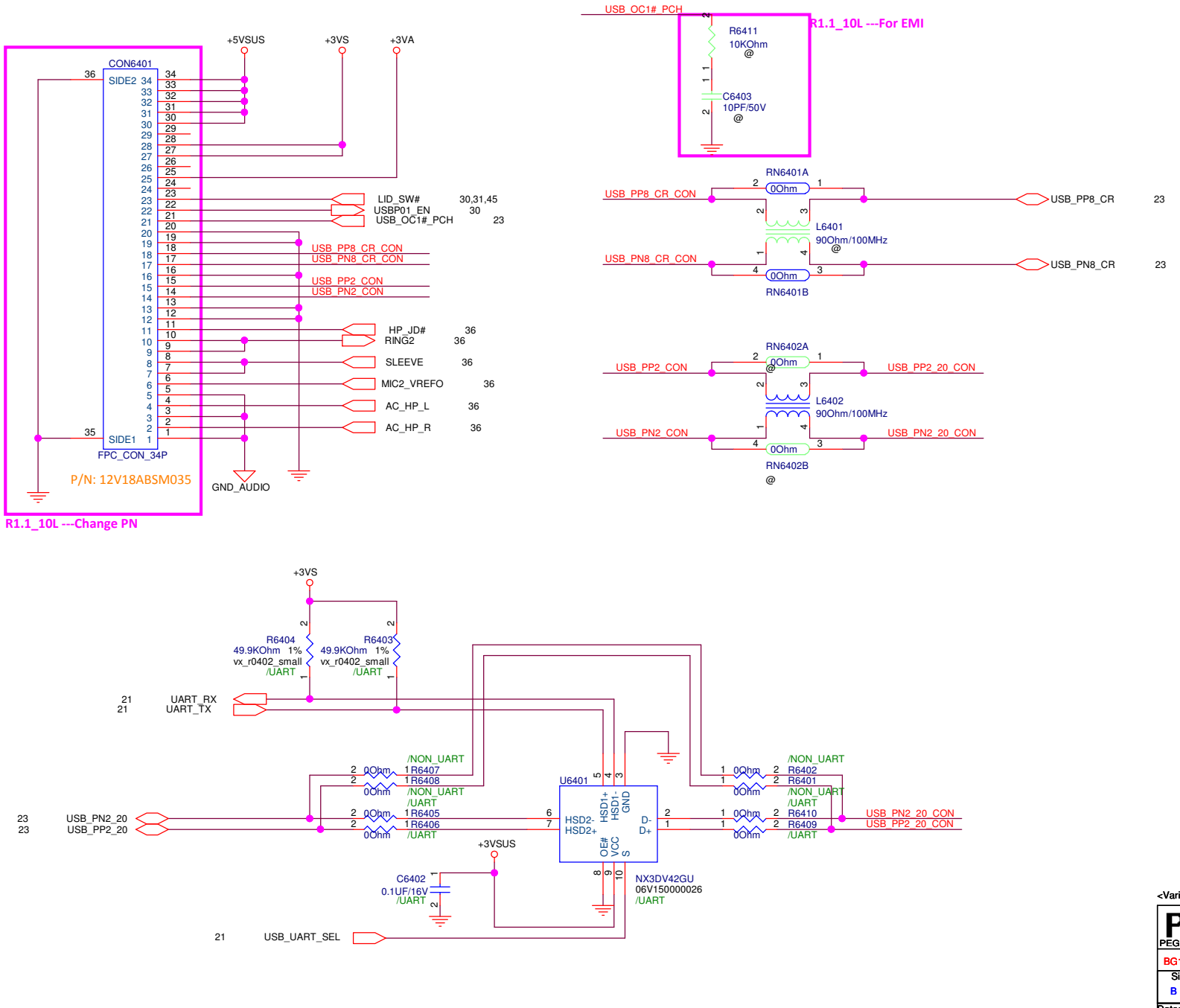
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 63 of 97



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : IO CON.

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 64 of 97

CPU NUT

H6501 CT264B176D146 GND
H6502 CT264B176D146 GND
H6503 CT264B176D146 GND
H6504 CT264B176D146 GND

6*2.5mm*1

H6545 C43D43N

H6535 C236D98 GND

6*3.1mm*1

H6543 CT236DO63x75 GND

2016.6.6 R1.2_10L ---For ME

CLIP

H6507 H6508 H6509 H6510 H6511
H6512 H6513 H6514 H6515 H6516 H6517 H6518
H6519 H6520 H6522 H6523 H6524 H6525
H6526 H6528 H6529 H6530 H6531 H6532
H6533 H6534

SUL-12A1M GND

2016.5.30
R1.2_10L ---For ME

Thermal screw*2

H6540 SP276D98

1	P_GND		
2	NP_NC1	NP_NC27	28
3	NP_NC2	NP_NC28	29
4	NP_NC3	NP_NC29	30
5	NP_NC4	NP_NC30	31
6	NP_NC5	NP_NC31	32
7	NP_NC6	NP_NC32	33
8	NP_NC7	NP_NC33	34
9	NP_NC8	NP_NC34	35
10	NP_NC9	NP_NC35	36
11	NP_NC10	NP_NC36	37
12	NP_NC11	NP_NC37	38
13	NP_NC12	NP_NC38	39
14	NP_NC13	NP_NC39	40
15	NP_NC14	NP_NC40	41
16	NP_NC15	NP_NC41	42
17	NP_NC16	NP_NC42	43
18	NP_NC17	NP_NC43	44
19	NP_NC18	NP_NC44	45
20	NP_NC19	NP_NC45	46
21	NP_NC20	NP_NC46	47
22	NP_NC21	NP_NC47	48
23	NP_NC22	NP_NC48	49
24	NP_NC23	NP_NC49	50
25	NP_NC24	NP_NC50	51
26	NP_NC25	NP_NC51	52
27	NP_NC26	NP_NC52	53

H6541 SP276D98

1	P_GND		
2	NP_NC1	NP_NC27	28
3	NP_NC2	NP_NC28	29
4	NP_NC3	NP_NC29	30
5	NP_NC4	NP_NC30	31
6	NP_NC5	NP_NC31	32
7	NP_NC6	NP_NC32	33
8	NP_NC7	NP_NC33	34
9	NP_NC8	NP_NC34	35
10	NP_NC9	NP_NC35	36
11	NP_NC10	NP_NC36	37
12	NP_NC11	NP_NC37	38
13	NP_NC12	NP_NC38	39
14	NP_NC13	NP_NC39	40
15	NP_NC14	NP_NC40	41
16	NP_NC15	NP_NC41	42
17	NP_NC16	NP_NC42	43
18	NP_NC17	NP_NC43	44
19	NP_NC18	NP_NC44	45
20	NP_NC19	NP_NC45	46
21	NP_NC20	NP_NC46	47
22	NP_NC21	NP_NC47	48
23	NP_NC22	NP_NC48	49
24	NP_NC23	NP_NC49	50
25	NP_NC24	NP_NC50	51
26	NP_NC25	NP_NC51	52
27	NP_NC26	NP_NC52	53

14*8mm*1

H6544 GND NP_NC D98_DO75X63N GND

2016.6.6 R1.2_10L ---For ME

13.5*8mm*1

H6542 GND NP_NC RT531X315BD98_D63N GND

2016.6.6 R1.2_10L ---For ME

Shielding PAD

H6536 C315D98 GND
H6537 C315D98 GND
H6538 C315D98 GND

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : NUT,Screw Hole

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 65 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 66 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 67 of 97

25,30 PM_SUSB# R6801 1 2 SUSB_EC# 30,57,91,92

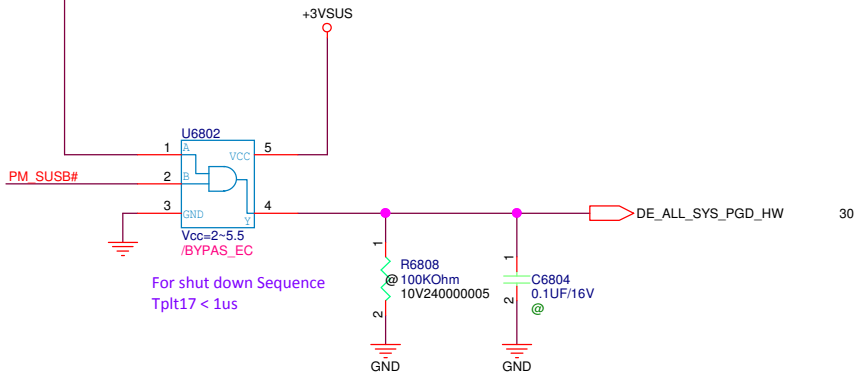
25,30 PM_SUSC# R6802 1 2 SUSC_EC# 30,57,91

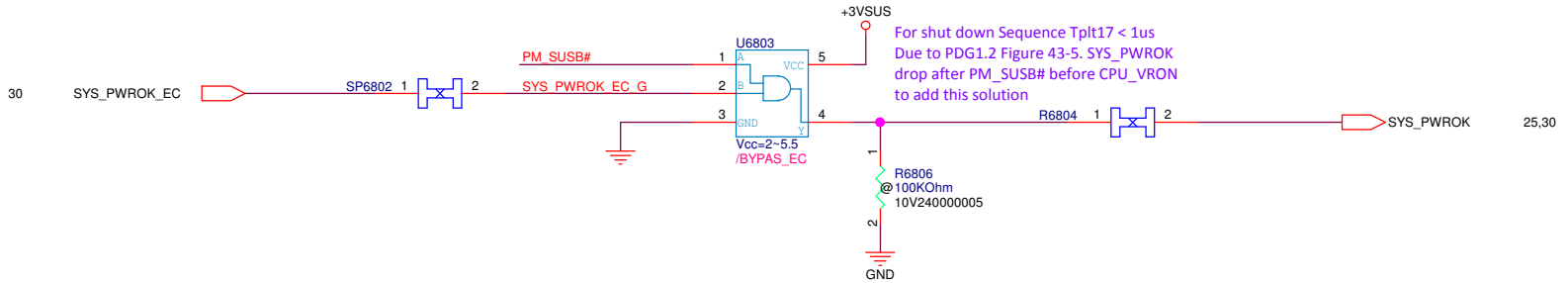
+3VSUS +3VSUS 4,24,25,26,28,30,31,41,42,51,53,62,64,81,92

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

Delay By EC(2ms+ EC processing time (3ms~33ms)

30 DE_ALL_SYS_PGD_EC R6809 1 2 DE_ALL_SYS_PGD_EC_R





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER Sequence

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 68 of 97

<Variant Name>

PEGATRON

Title : Power SW Board

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
B	X3	1.0

Date: Monday, July 11, 2016 Sheet 69 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 70 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 71 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 72 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 73 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 74 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 75 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 76 of 97

PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 77 of 97

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : <Title>

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 78 of 97

PEGATRON Title : <Title>

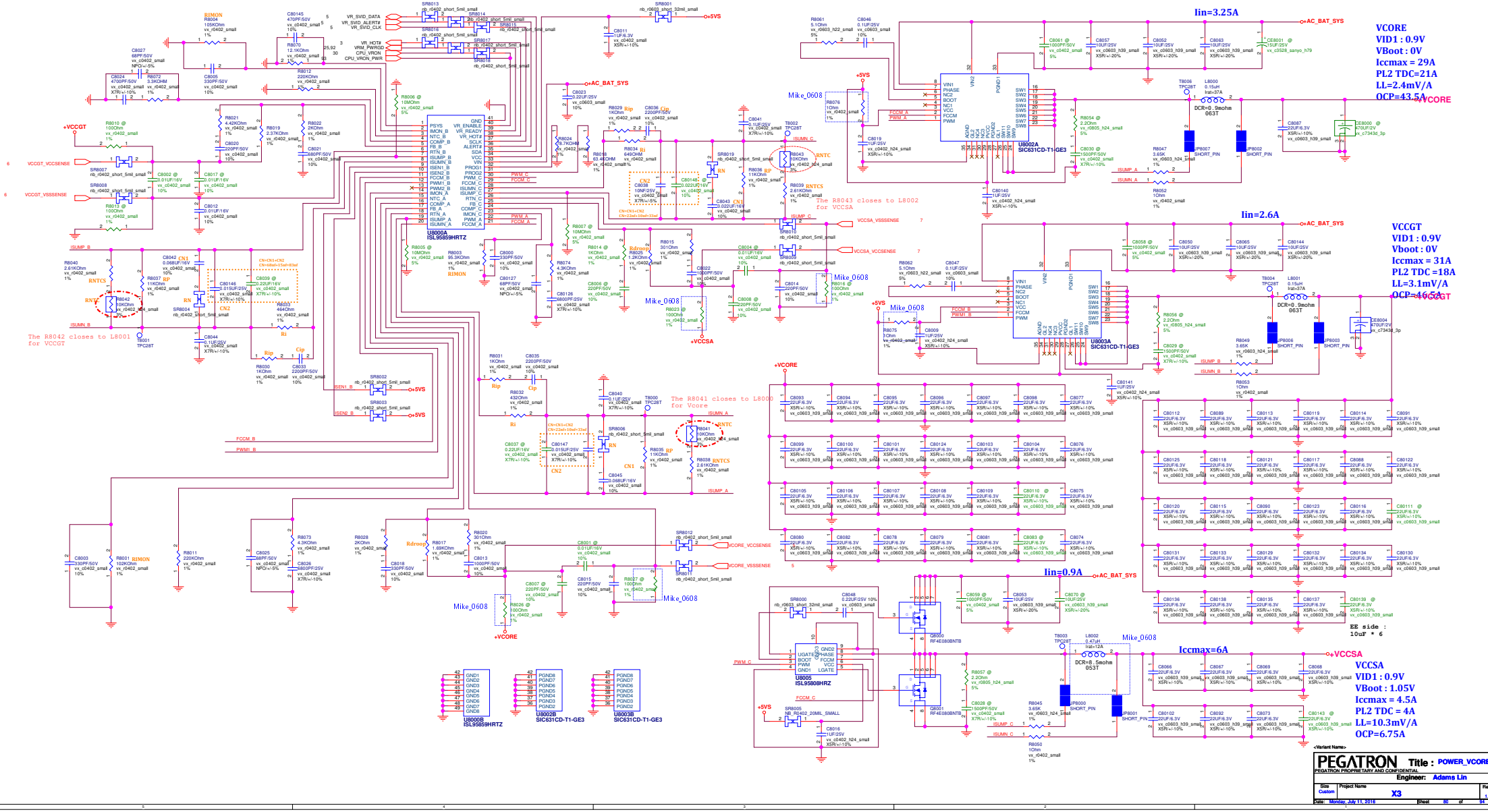
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: *Andy Kao*

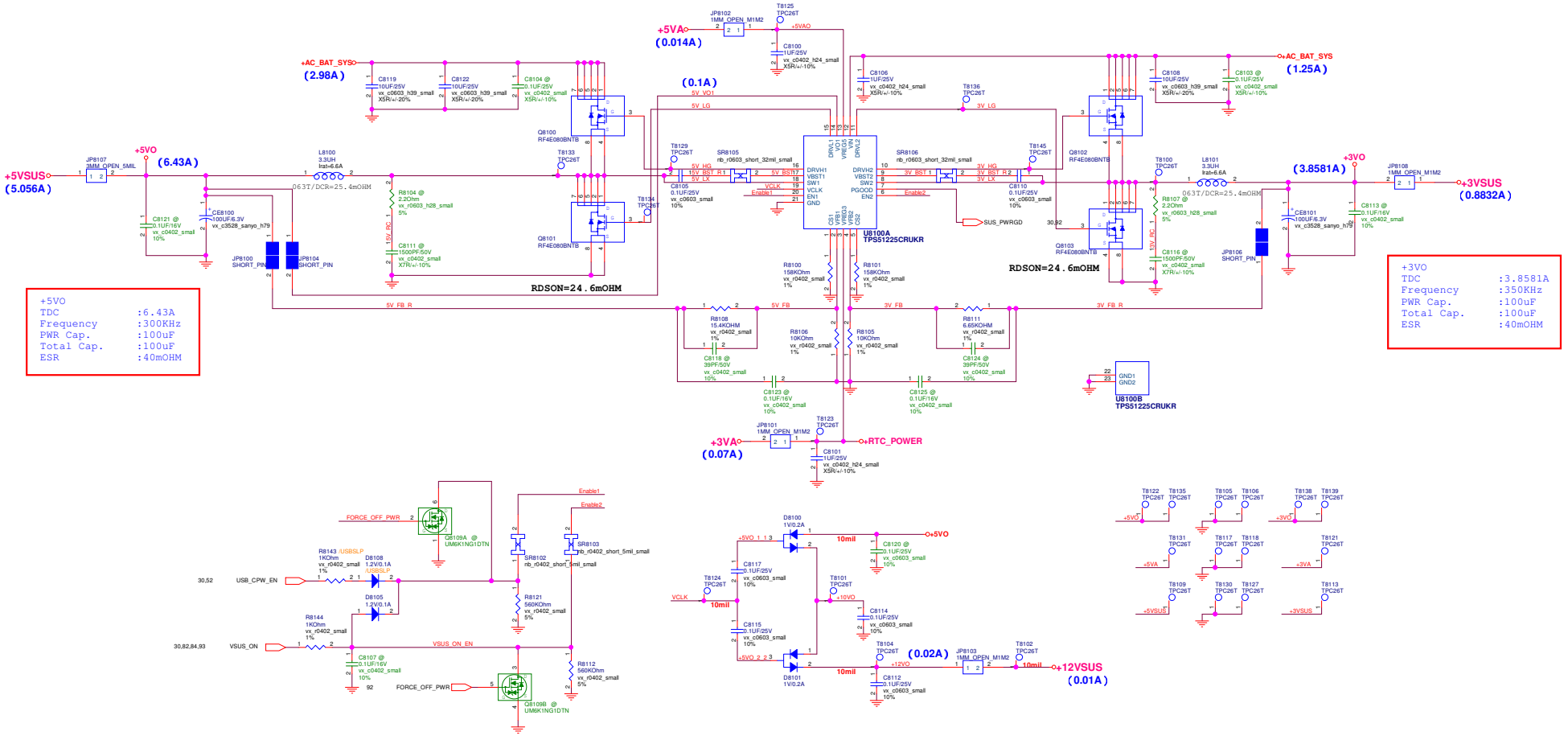
Size	Project Name	Rev
A	X3	1.0

Date: Monday, July 11, 2016 Sheet 79 of 97

VCORE & VCCGT & VCCSA POWER SUPPLY

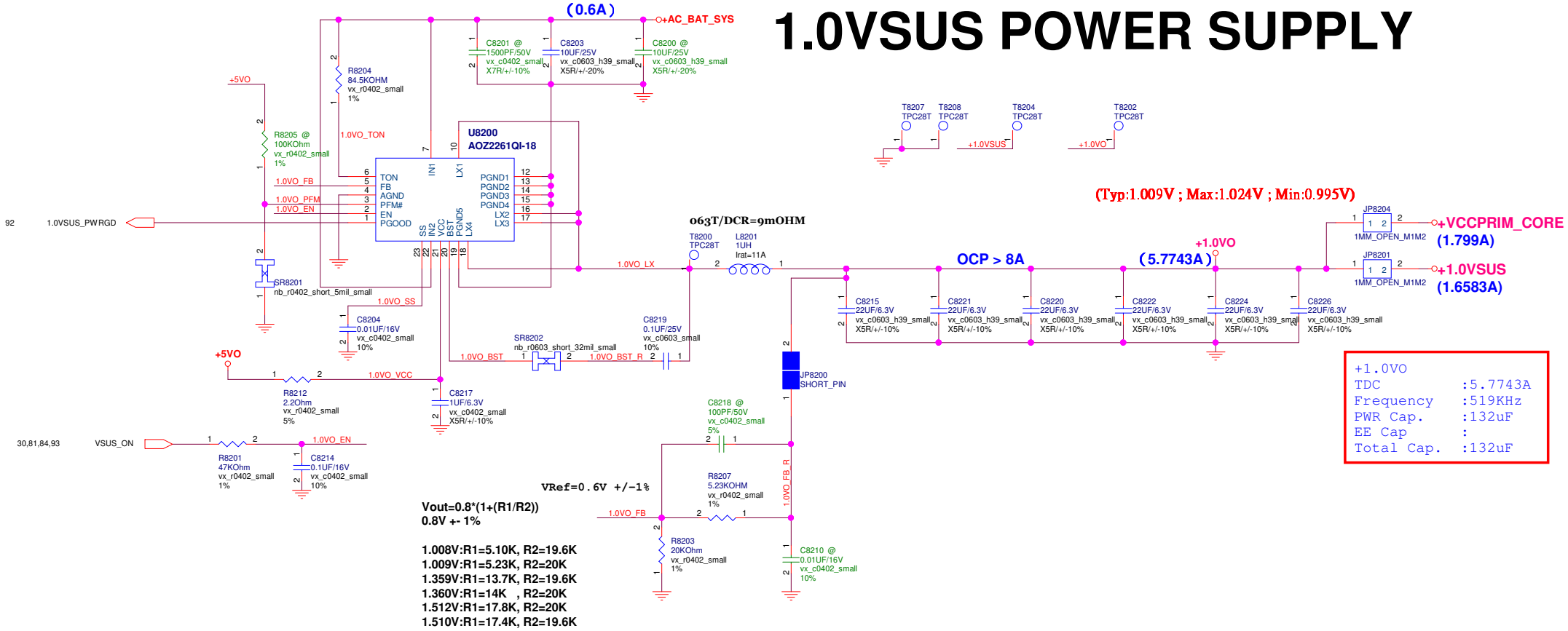


5VO & 3VO POWER SUPPLY

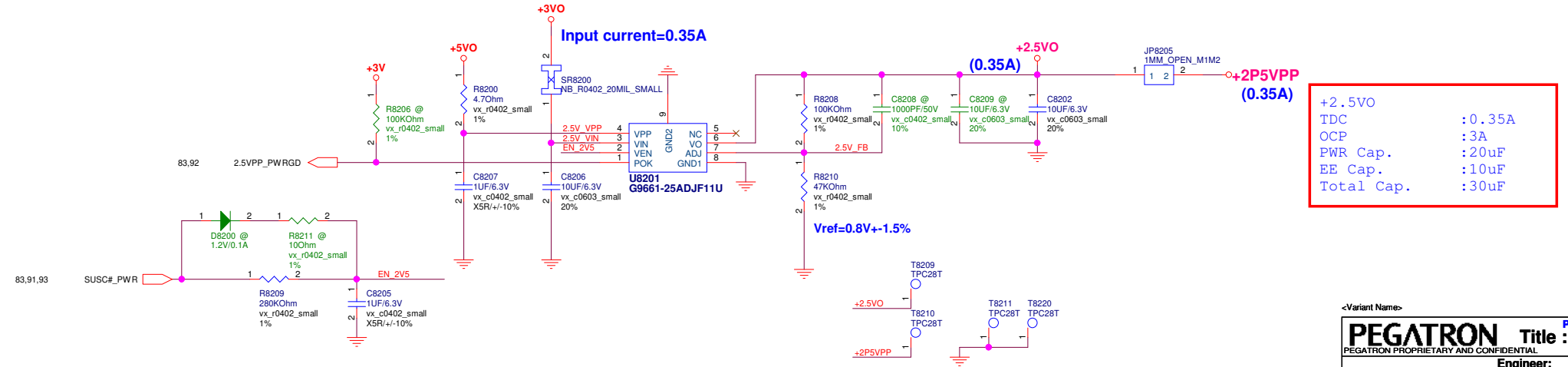


PEGATRON	Title : POWER_SYSTEM
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Adams Lin
R01-POWER	
Size: Custom	Project Name: X3
Rev: 1.1	
Date: Monday, July 11, 2016	Sheet 81 of 94

1.0VSUS POWER SUPPLY



2.5V POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

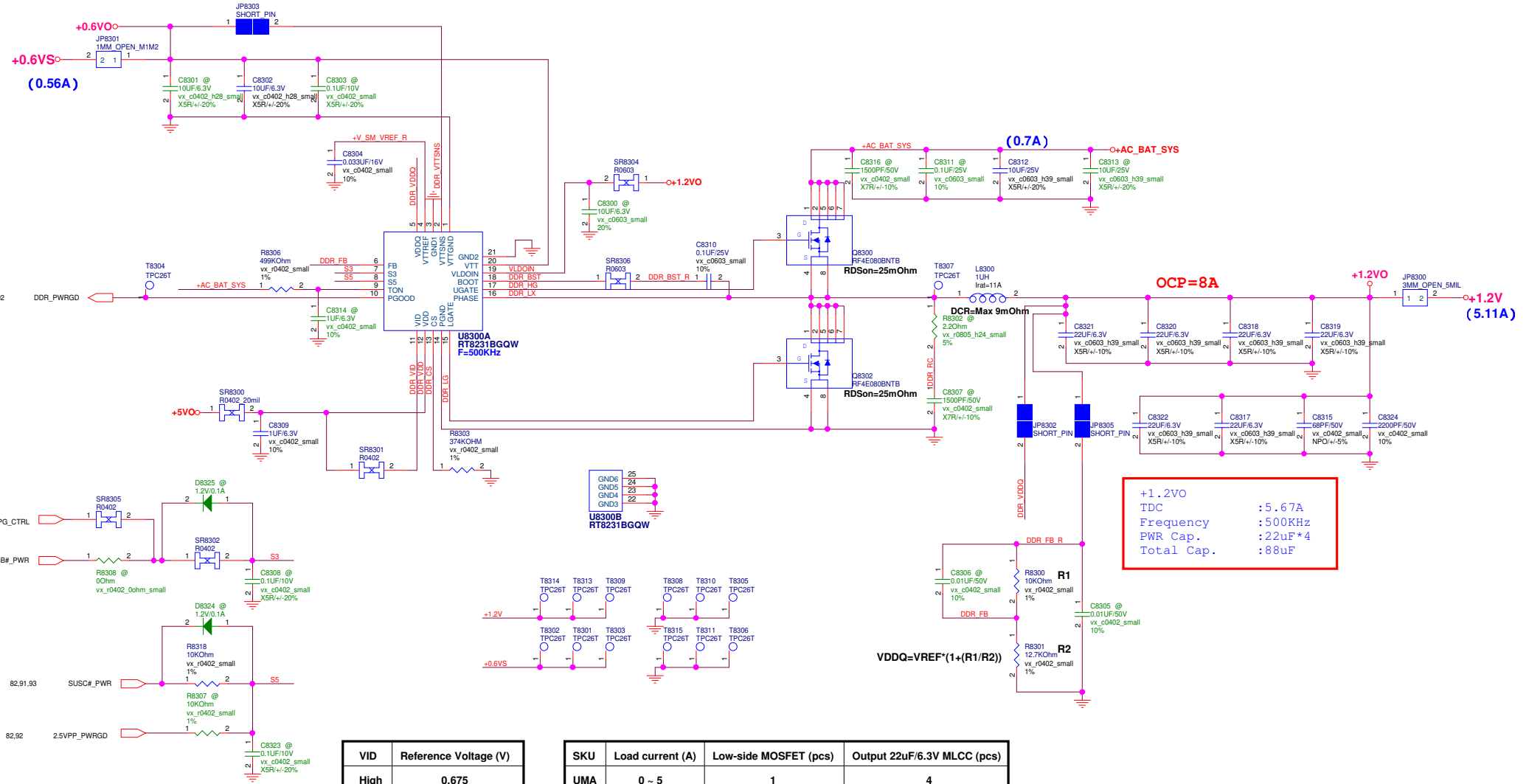
Title : P82_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Monday, July 11, 2016 Sheet 82 of 94

DDR & VTT POWER SUPPLY



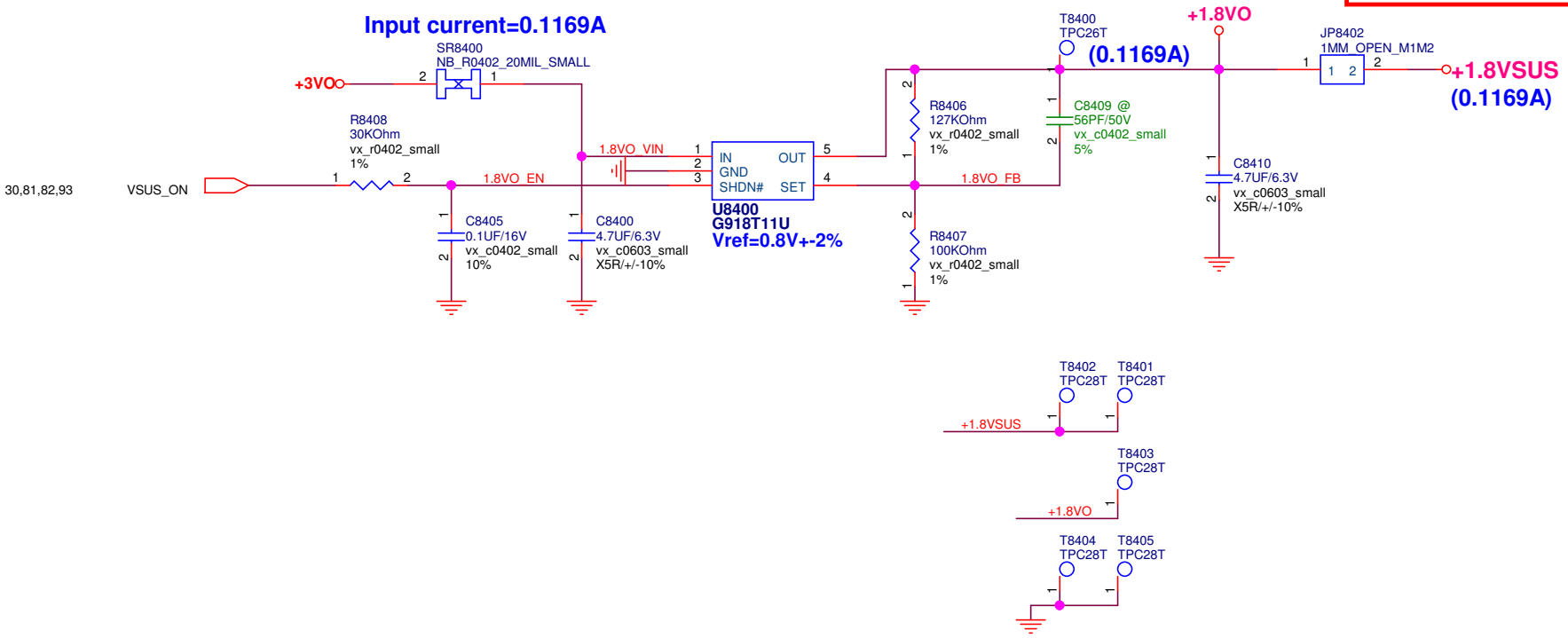
VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_DDR & VTT
BG1-POWER
Engineer: Adams Lin
Size: Custom
Project Name: X3
Rev: 1.1
Date: Monday, July 11, 2016
Sheet 83 of 94

1.8VSUS POWER SUPPLY

+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

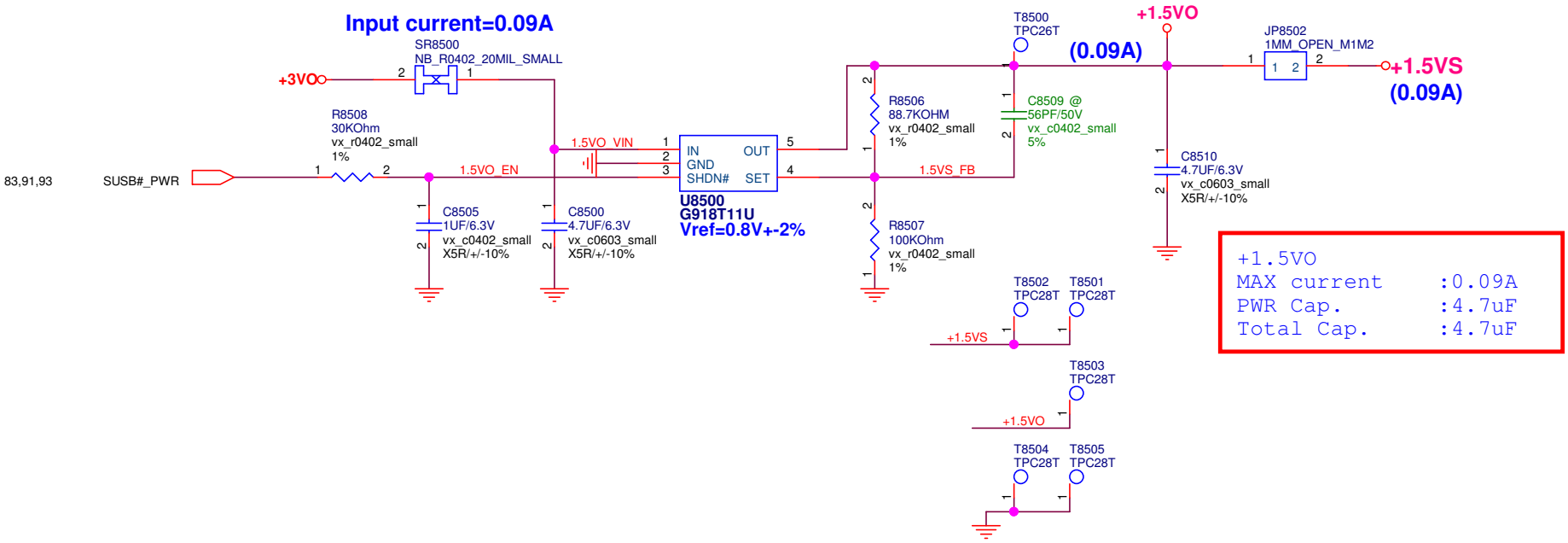
Title : POWER_+1.8VSUS

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Monday, July 11, 2016 Sheet 84 of 94

1.5VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+1.5VS

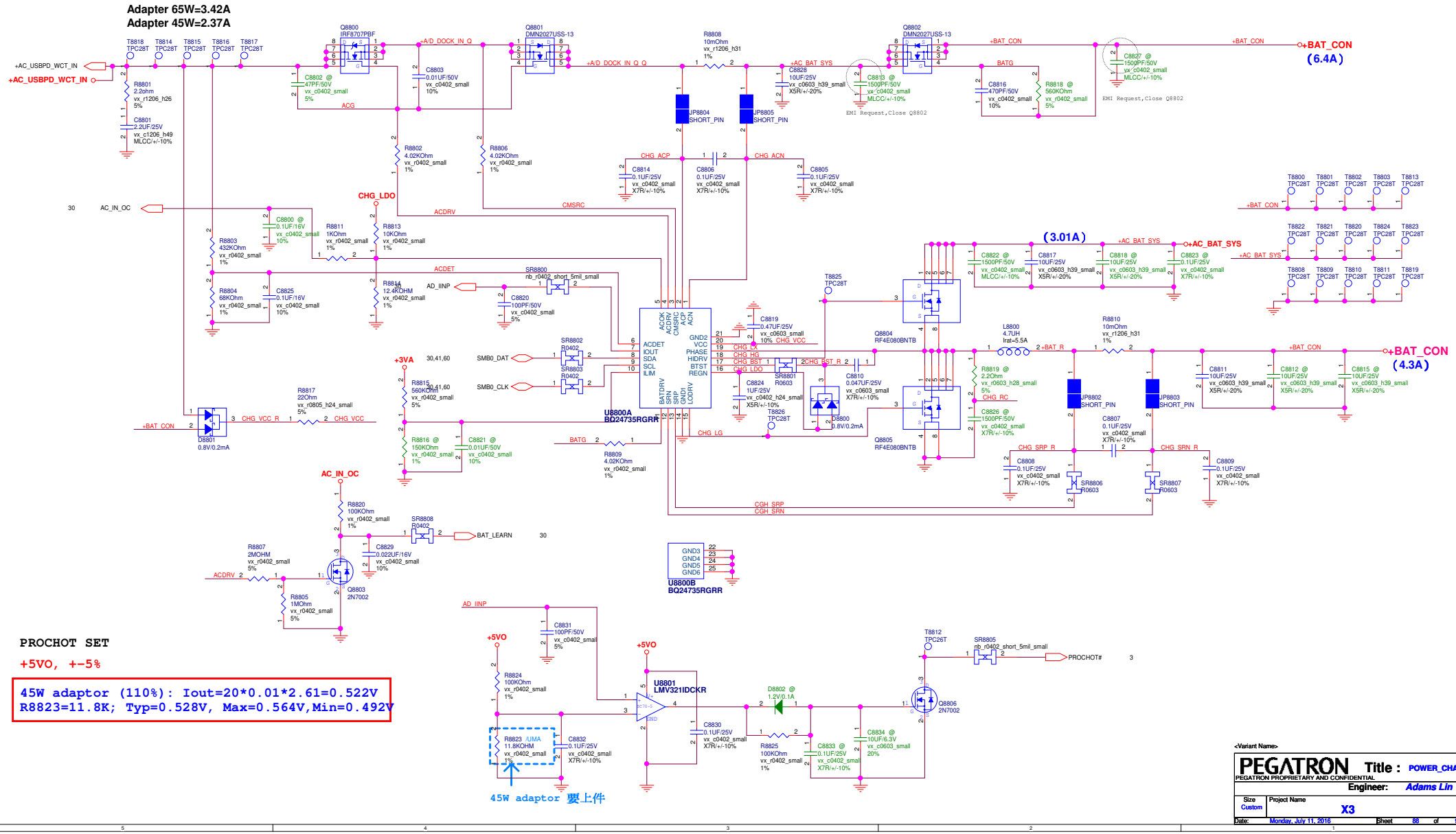
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Monday, July 11, 2016 Sheet 85 of 94

BATTERY CHARGER



PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_CHARGER
Engineer: Adams Lin
Size: Custom
Project Name: X3
Rev: 1.1
Date: Monday, July 11, 2016
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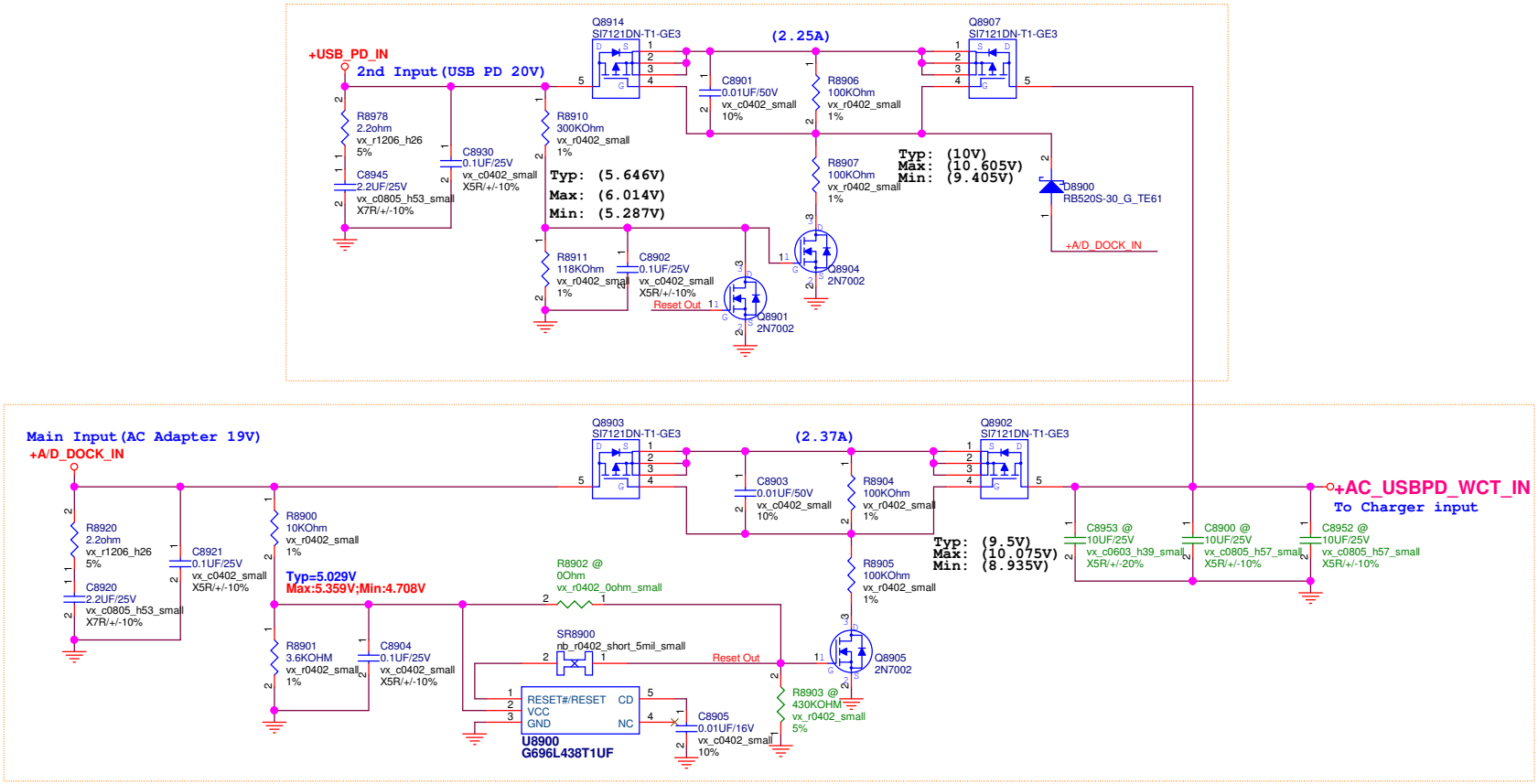
2 Input switch Circuit



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : AC&PD S.W.

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

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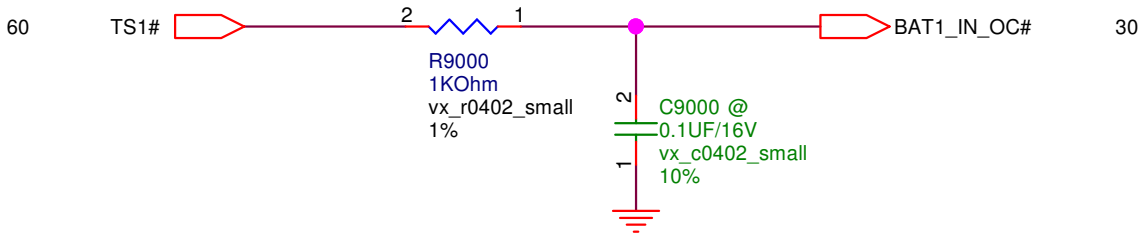
BATTERY IN DETECT



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

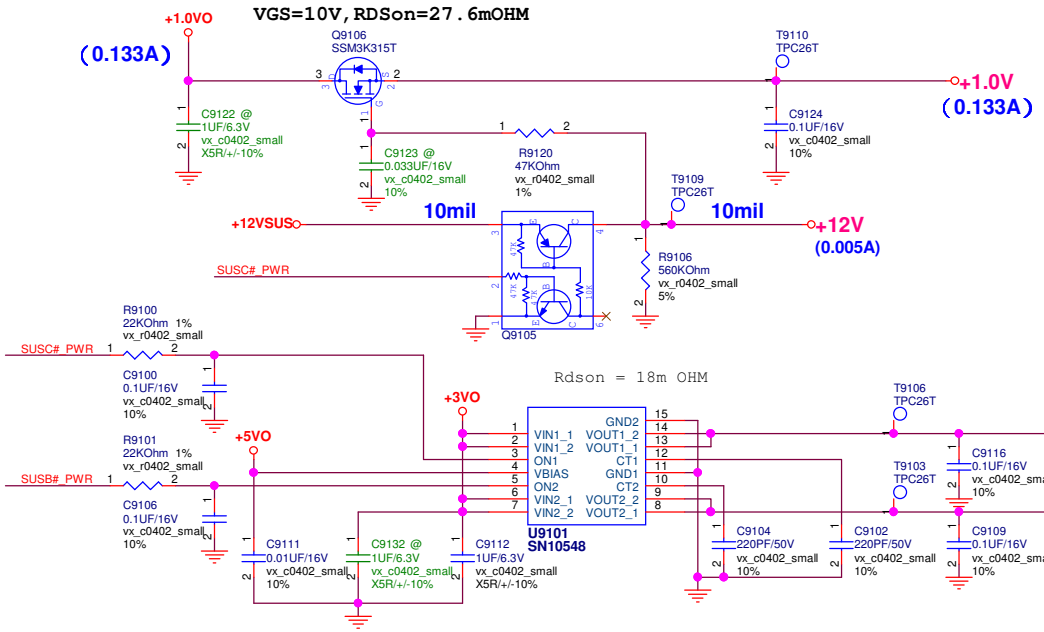
Title : POWER_DETECT

Engineer: Adams Lin

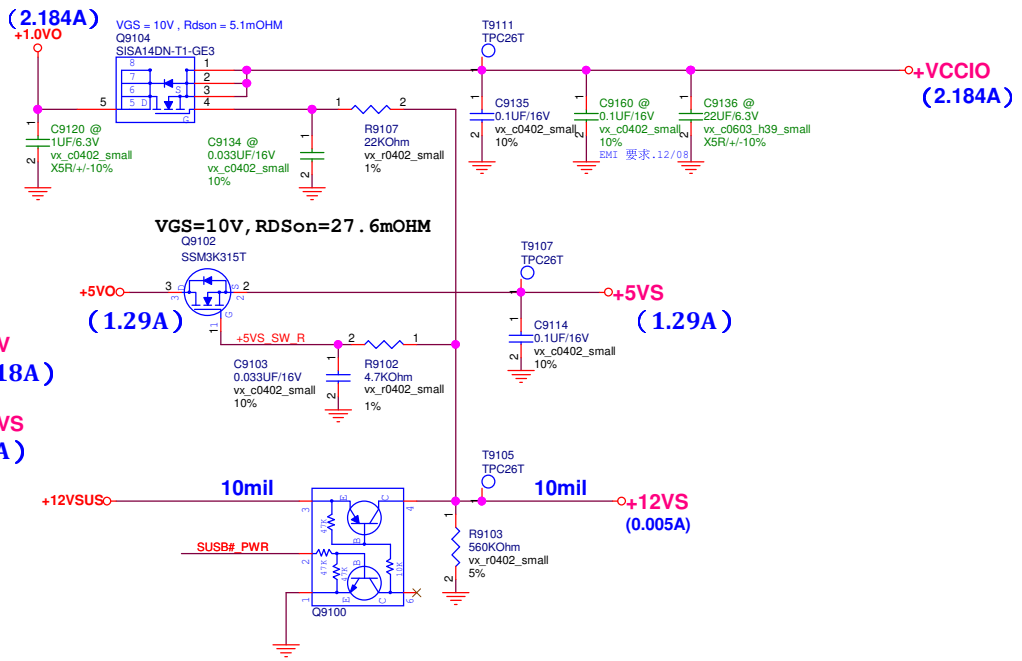
Size	Project Name	Rev
Custom	X3	1.1

Date: Monday, July 11, 2016 Sheet 90 of 94

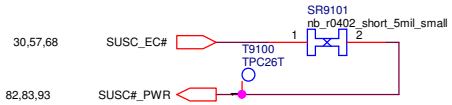
SUSC#_PWR POWER



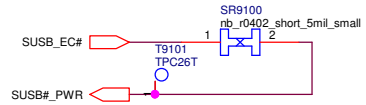
SUSB#_PWR POWER



SUSC#_PWR POWER Control



SUSB#_PWR POWER Control



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

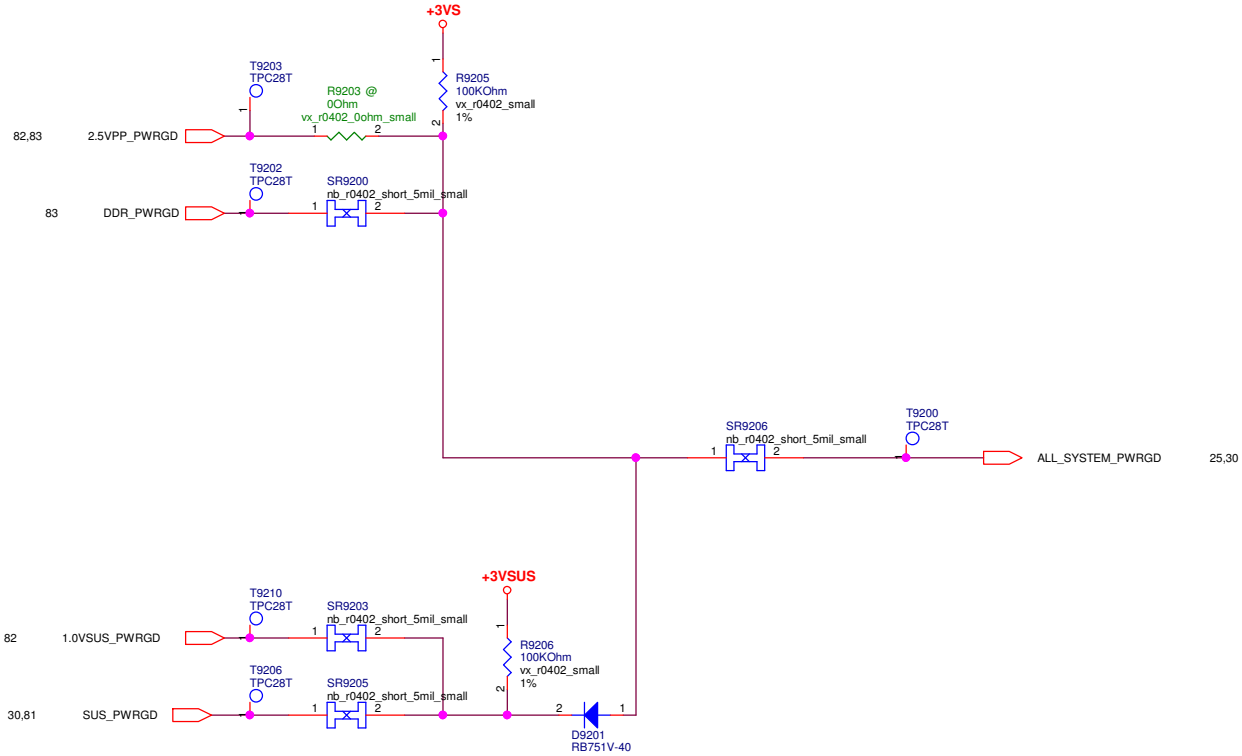
Title : POWER_LOAD SWITCH

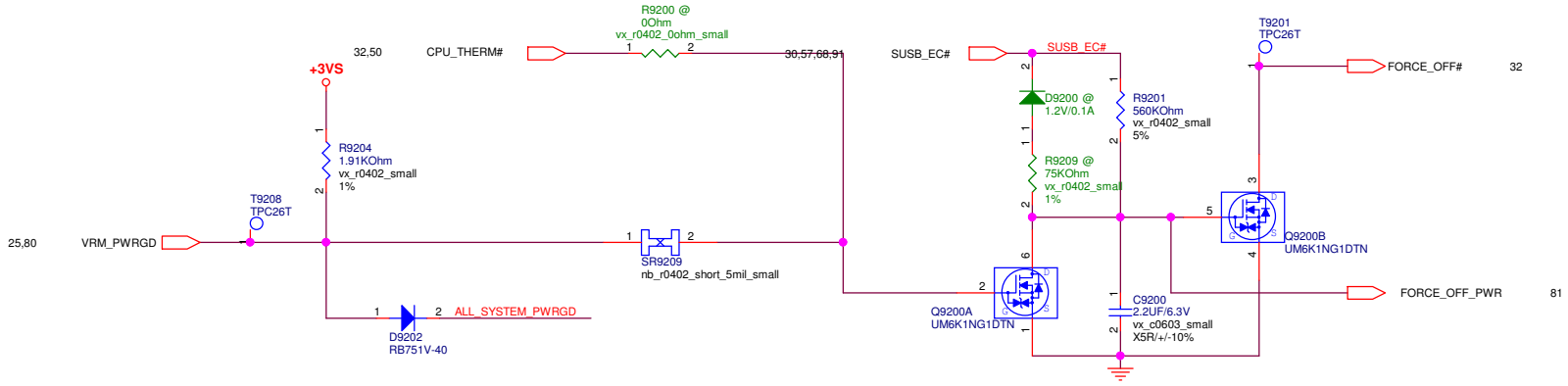
Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Monday, July 11, 2016 Sheet 91 of 94

POWER GOOD DETECTER





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

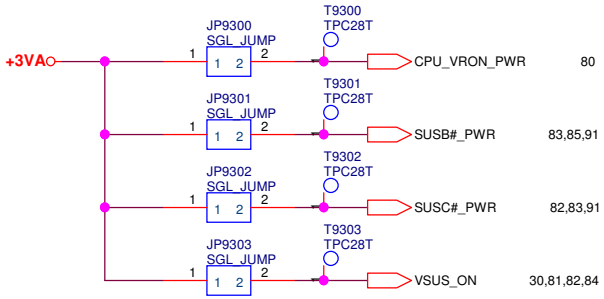
Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

Date: Monday, July 11, 2016 Sheet 92 of 94

+USB_PD_IN	+USB_PD_IN	42,89
+A/D_DOCK_IN	+A/D_DOCK_IN	60,89
+AC_USBPD_WCT_IN	+AC_USBPD_WCT_IN	88,89
+AC_BAT_SYS	+AC_BAT_SYS	43,45,80,81,82,83,88
+BAT_CON	+BAT_CON	60,88
+RTC_POWER	+RTC_POWER	81
+5VA	+5VA	31,56,81
+3VA	+3VA	24,30,31,36,41,43,53,57,64,81,88
+5VO	+5VO	26,81,82,83,88,91
+3VO	+3VO	81,82,84,85,91
+2.5VO	+2.5VO	82
+1.8VO	+1.8VO	84
+1.2VO	+1.2VO	83
+1.0VO	+1.0VO	82,91
+0.6VO	+0.6VO	83
+12VSUS	+12VSUS	28,81,91
+5VSUS	+5VSUS	41,42,52,56,64,81
+3VSUS	+3VSUS	4,24,25,26,28,30,31,41,42,51,53,62,64,68,81,92
+1.8VSUS	+1.8VSUS	9,21,22,26,84
+1.0VSUS	+1.0VSUS	26,82
+12V	+12V	57,91
+2P5VPP	+2P5VPP	16,17,57,82
+1.2V	+1.2V	4,7,15,16,17,19,57,83
+1.0V	+1.0V	7,57,91
+12VS	+12VS	31,48,57,91
+5VS	+5VS	31,36,45,48,50,51,57,80,91
+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+0.6VS	+0.6VS	15,57,83
+VCORE	+VCORE	5,80
+VCCGT	+VCCGT	6,80
+VCCSA	+VCCSA	7,80
+VCCIO	+VCCIO	3,7,9,57,91
+VCCPRIM_CORE	+VCCPRIM_CORE	26,82

FOR POWER TEST



PEGATRON Title : POWER_SIGNAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-POWER Engineer: Adams Lin

Size	Project Name	Rev
B	X3	1.1

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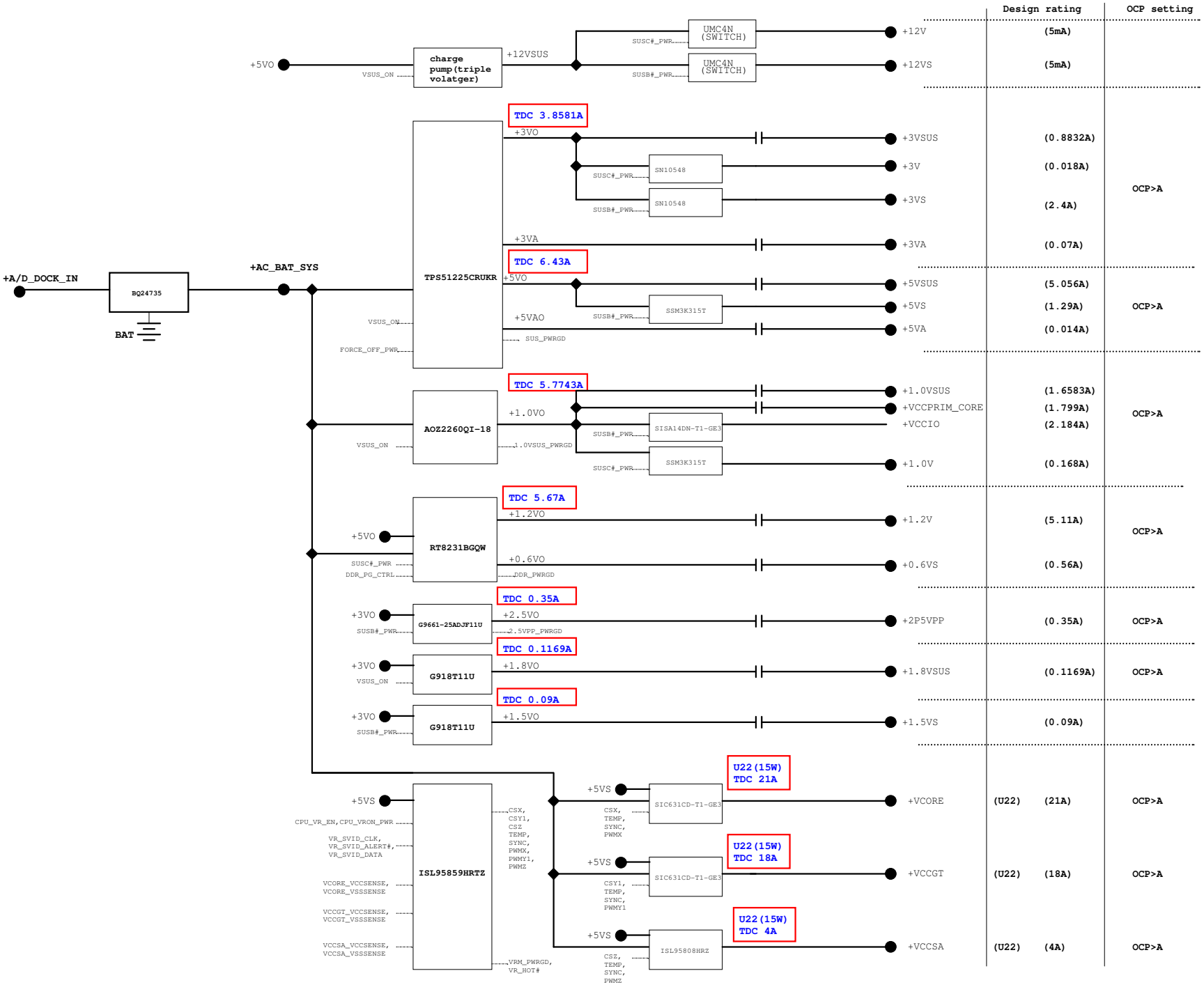

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER_FLOWCHART

Engineer: Adams Lin

Size	Project Name	Rev
Custom	X3	1.1

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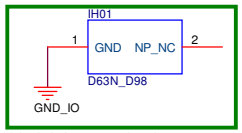
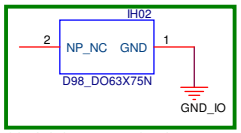
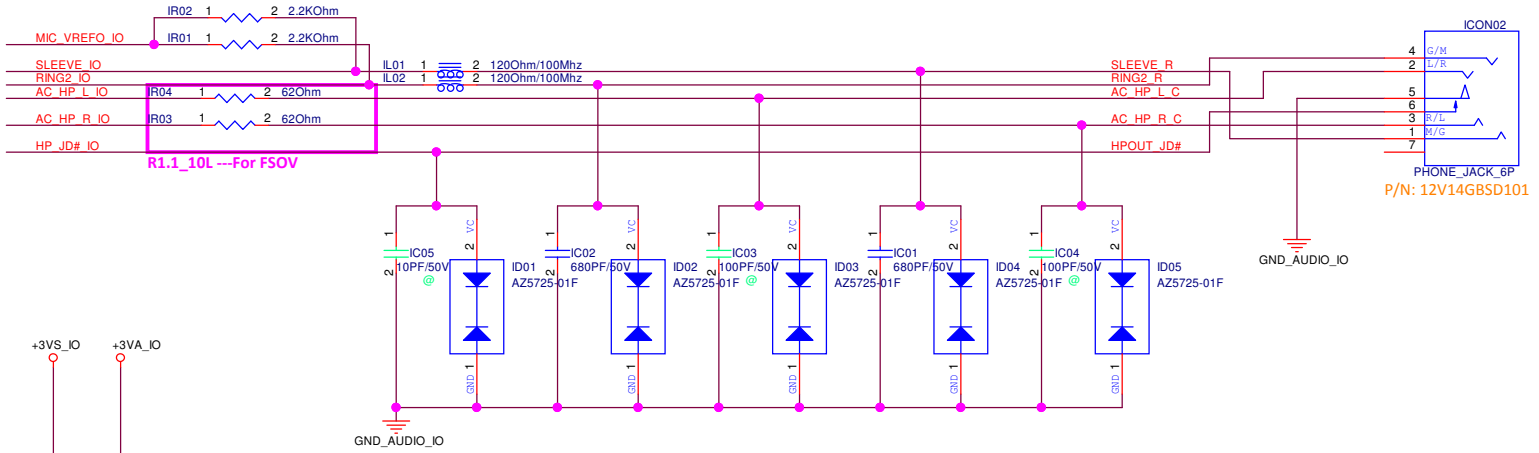


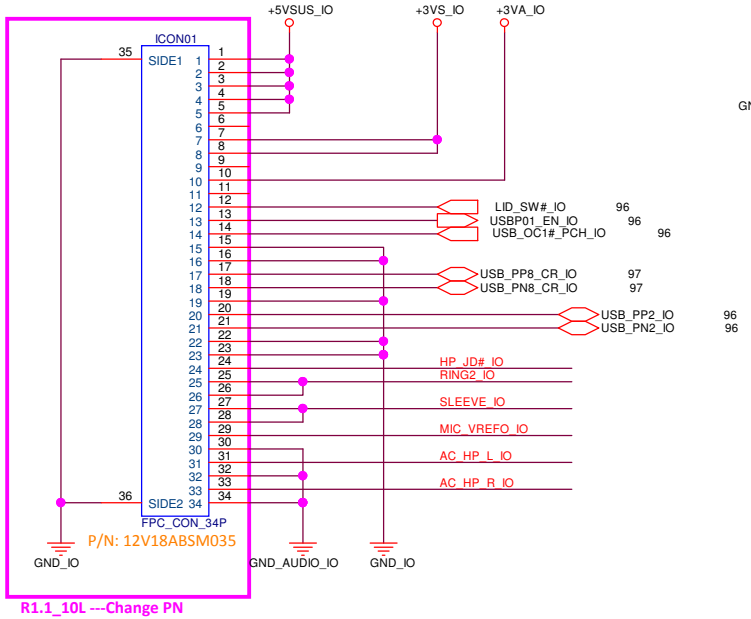
2016.6.6 R1.2_10L ---For ME

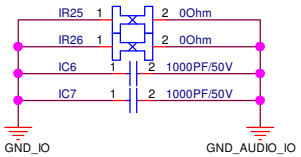


2016.6.6 R1.2_10L ---For ME

AUDIO JACK







PEGATRON Title : AUD(2)_SPK/JACK/DMIC

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
A3	X3	1.0

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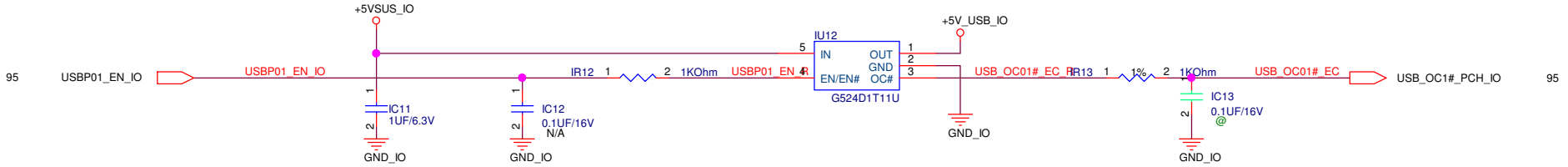
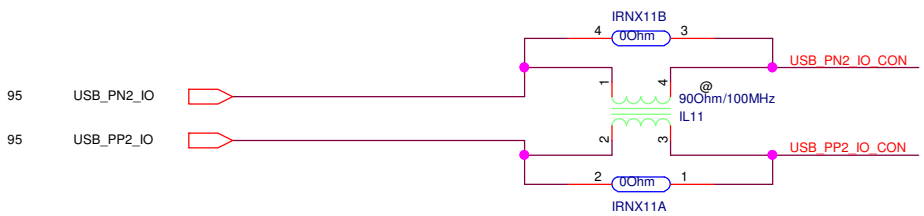
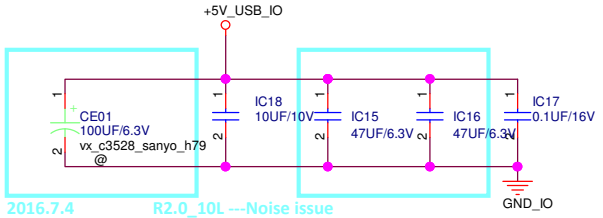
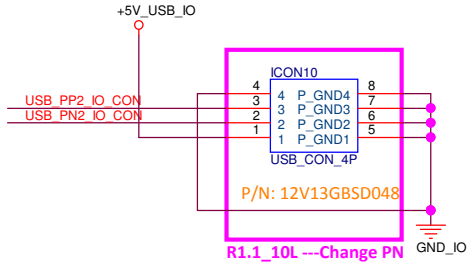
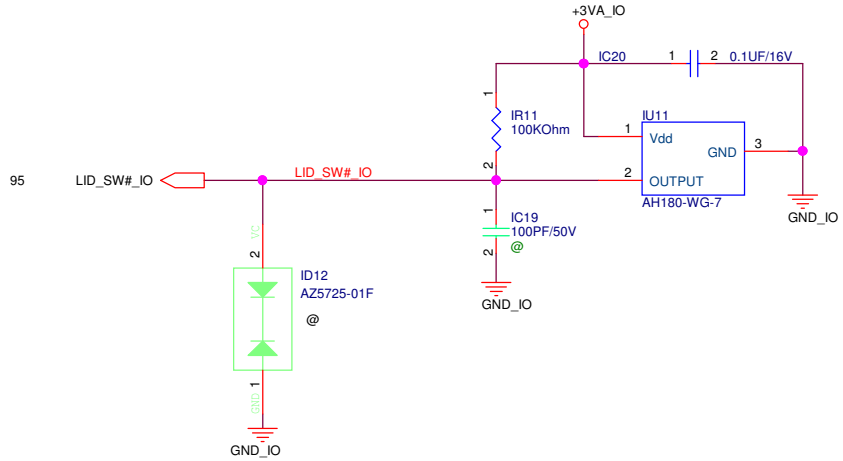


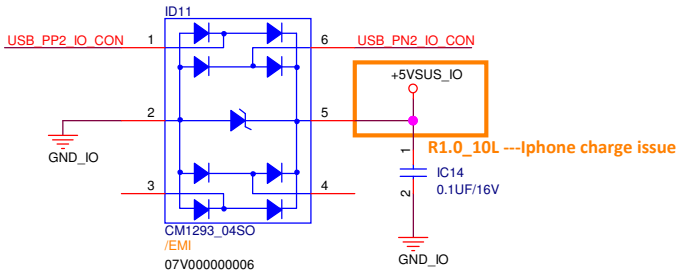


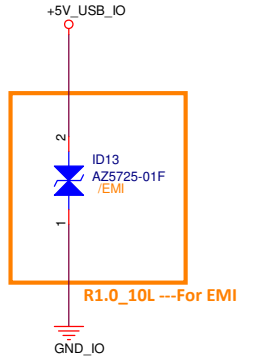






PLACE ESD Diodes near USB Connector





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB30_IO_CONN

Engineer: *Andy Kao*

BG1/HW3

Size	Project Name	Rev
B	X3	1.0

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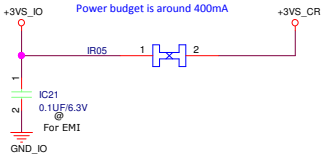
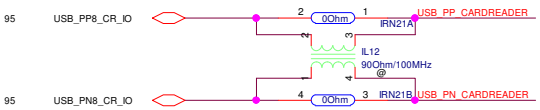
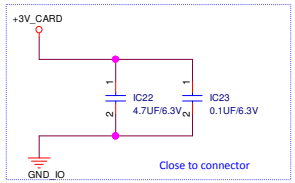
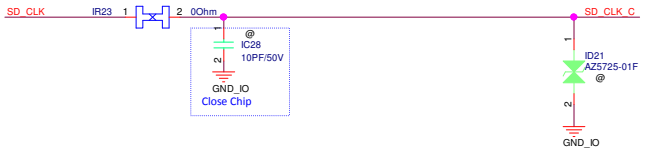
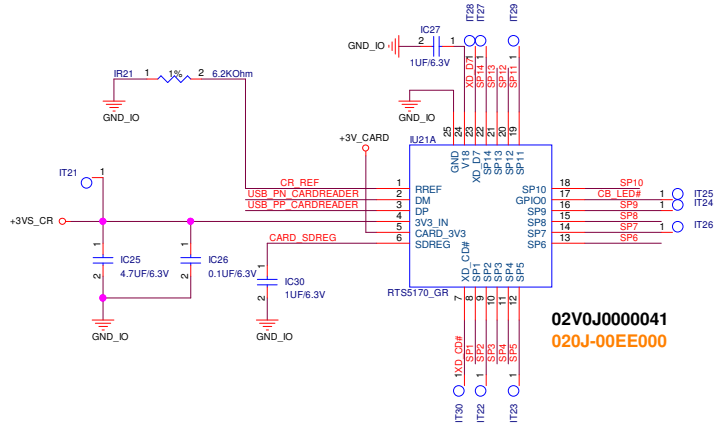
Cardreader











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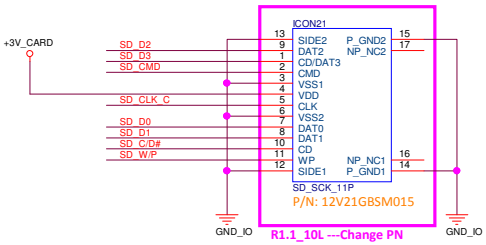

RTS5170-GR Share Pin Assignment

SP1	SD_W/P
SP3	SD_D1
SP4	SD_D0
SP6	SD_C/D#
SP8	SD_CLK
SP10	SD_CMD
SP12	SD_D3
SP13	SD_D2

<Variant Name>

PEGATRON Title : RTS5138-GR

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3 Engineer: Andy Kao

Size	Project Name	Rev
Custom	X3	1.0

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