17809 -1m Carlsberg_KL

Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

<Core Design>

緯創資通 Wistron Corporation
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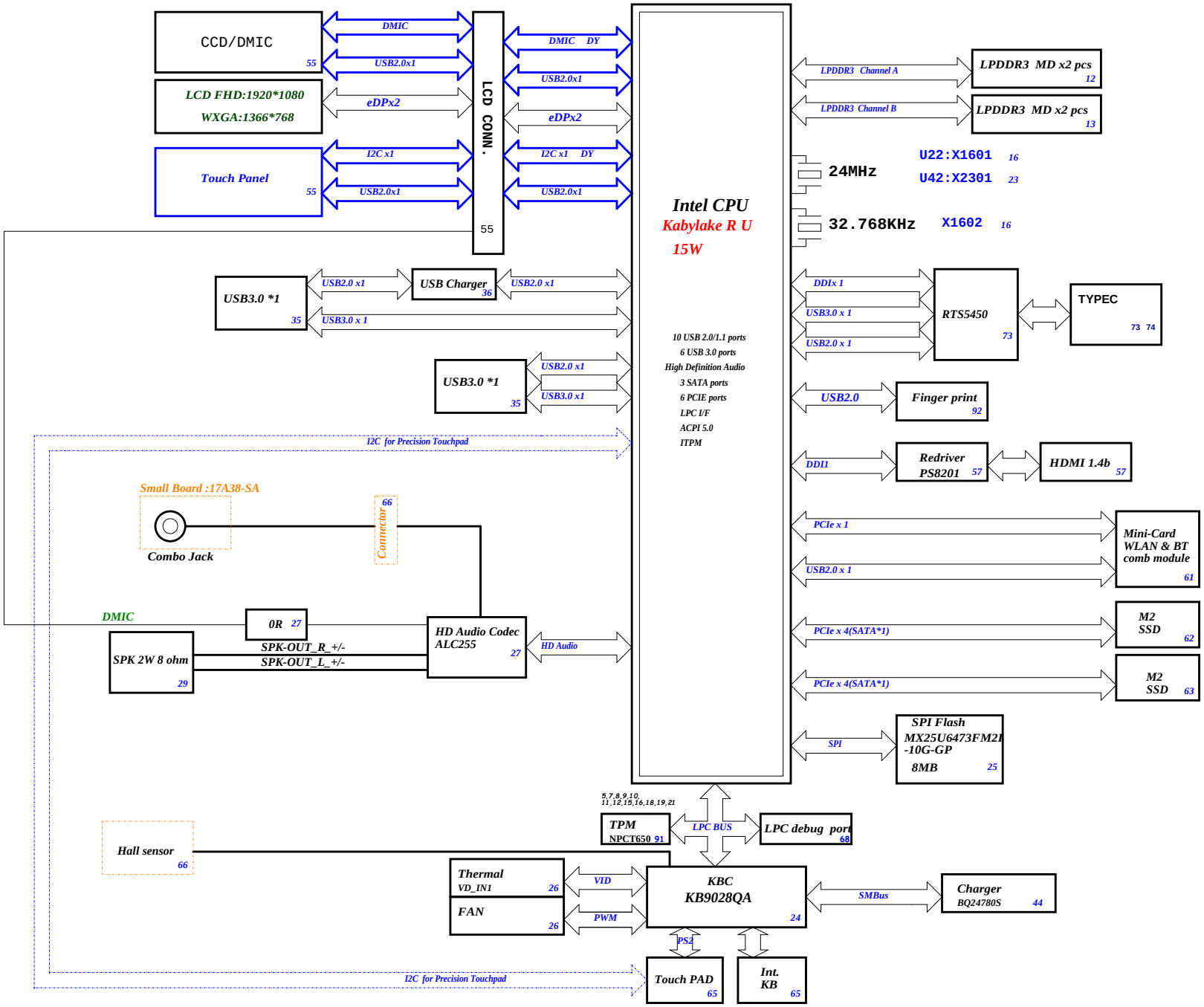
Title		
Cover Page		
Size: A3	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 1 of 106	

Project Code: 4PD0D7010001
PCB No : 17809
Revision : -1m



<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
Custom	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 2 of 106

Main Func = CPU

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1

55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

55 eDP_HPD_CPU
24 eDP_BLEN_CPU
55 eDP_BLCTRL_CPU
55 eDP_VDDEN_CPU

HDMI

57 HDMI_DATA_CPU_N2
57 HDMI_DATA_CPU_P2
57 HDMI_DATA_CPU_N1
57 HDMI_DATA_CPU_P1
57 HDMI_DATA_CPU_N0
57 HDMI_DATA_CPU_P0
57 HDMI_DATA_CPU_N3
57 HDMI_DATA_CPU_P3

14,57 HDMI_CLK_CPU
14,57 HDMI_DATA_CPU

57 HDMI_DET_CPU

TYPEC

73 DP_DDI_TX_N0
73 DP_DDI_TX_P0
73 DP_DDI_TX_N1
73 DP_DDI_TX_P1
73 DP_DDI_TX_N2
73 DP_DDI_TX_P2
73 DP_DDI_TX_N3
73 DP_DDI_TX_P3

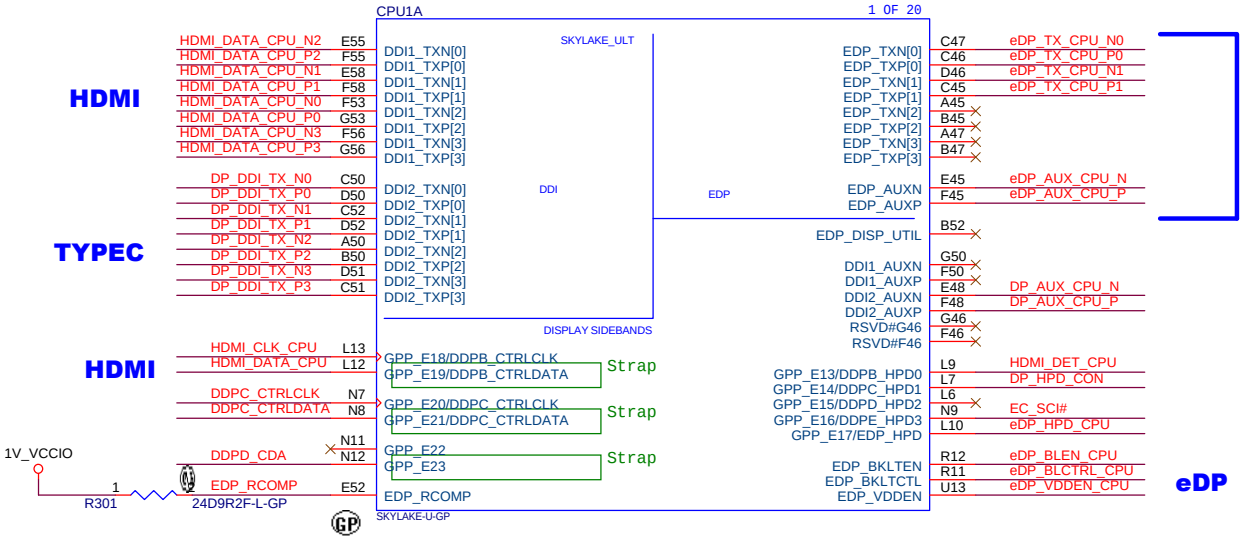
73 DP_AUX_CPU_N
73 DP_AUX_CPU_P

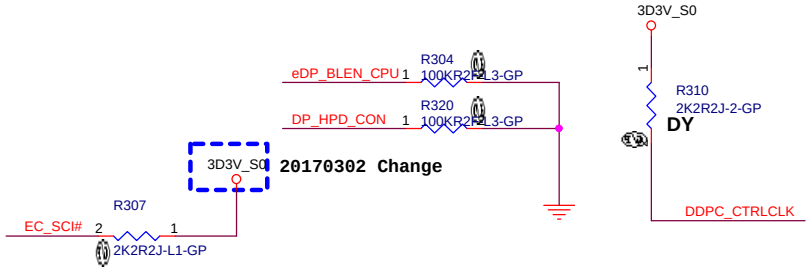
14 DDPC_CTRLDATA
73 DP_HPD_CON

OTHER

14 DDPD_CDA

24 EC_SCI#





(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title: CPU_(DISPLAY)

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 3 of 106

Main Func = CPU

DATA

12 M_A_DQ[63:0]

M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63

DQS

12 M_A_DQS_DP[7:0]

M_A_DQS_DP0 M_A_DQS_DP1 M_A_DQS_DP2 M_A_DQS_DP3 M_A_DQS_DP4 M_A_DQS_DP5 M_A_DQS_DP6 M_A_DQS_DP7

12 M_A_DQS_DN[7:0]

M_A_DQS_DN0 M_A_DQS_DN1 M_A_DQS_DN2 M_A_DQS_DN3 M_A_DQS_DN4 M_A_DQS_DN5 M_A_DQS_DN6 M_A_DQS_DN7

CMD

12 M_A_CA_A[9:0]

M_A_CA_A0 M_A_CA_A1 M_A_CA_A2 M_A_CA_A3 M_A_CA_A4 M_A_CA_A5 M_A_CA_A6 M_A_CA_A7 M_A_CA_A8 M_A_CA_A9

12 M_A_CA_B[9:0]

M_A_CA_B0 M_A_CA_B1 M_A_CA_B2 M_A_CA_B3 M_A_CA_B4 M_A_CA_B5 M_A_CA_B6 M_A_CA_B7 M_A_CA_B8 M_A_CA_B9

CLK

12 M_A_CLK0
12 M_A_CLK#0
12 M_A_CLK1
12 M_A_CLK#1

CKE

12 M_A_CKE0
12 M_A_CKE1
12 M_A_CKE2
12 M_A_CKE3

CTRL

12 M_A_CS#0
12 M_A_CS#1
12 M_A_ODT0

VREF

12 V_DDR_CA_VREF
12 DDR_VREFDQ01_CHA
13 DDR_VREFDQ02_CHB

VTT CTRL

51 DDR_VTT_CTRL_Q

CPU1B — 2 OF 20 — SKYLAKE_ULT

M_A_DQ[0:7]	M_A_DQ0 AL71	DDR0_DQ[0]	
	M_A_DQ1 AL68	DDR0_DQ[1]	
	M_A_DQ2 AN68	DDR0_DQ[2]	
	M_A_DQ3 AN69	DDR0_DQ[3]	
	M_A_DQ4 AL70	DDR0_DQ[4]	
	M_A_DQ5 AL69	DDR0_DQ[5]	
	M_A_DQ6 AN70	DDR0_DQ[6]	
	M_A_DQ7 AN71	DDR0_DQ[7]	
M_A_DQ[8:15]	M_A_DQ8 AR70	DDR0_DQ[8]	
	M_A_DQ9 AR68	DDR0_DQ[9]	
	M_A_DQ10 AU71	DDR0_DQ[10]	
	M_A_DQ11 AU68	DDR0_DQ[11]	
	M_A_DQ12 AR71	DDR0_DQ[12]	
	M_A_DQ13 AR69	DDR0_DQ[13]	
	M_A_DQ14 AU70	DDR0_DQ[14]	
	M_A_DQ15 AU69	DDR0_DQ[15]	
M_A_DQ[16:23]	M_A_DQ16 AF65	DDR1_DQ[0]/DDR0_DQ[16]	
	M_A_DQ17 AF64	DDR1_DQ[1]/DDR0_DQ[17]	
	M_A_DQ18 AK65	DDR1_DQ[2]/DDR0_DQ[18]	
	M_A_DQ19 AK64	DDR1_DQ[3]/DDR0_DQ[19]	
	M_A_DQ20 AF66	DDR1_DQ[4]/DDR0_DQ[20]	
	M_A_DQ21 AF67	DDR1_DQ[5]/DDR0_DQ[21]	
	M_A_DQ22 AK67	DDR1_DQ[6]/DDR0_DQ[22]	
	M_A_DQ23 AK66	DDR1_DQ[7]/DDR0_DQ[23]	
M_A_DQ[24:31]	M_A_DQ24 AF70	DDR1_DQ[8]/DDR0_DQ[24]	
	M_A_DQ25 AF68	DDR1_DQ[9]/DDR0_DQ[25]	
	M_A_DQ26 AH71	DDR1_DQ[10]/DDR0_DQ[26]	
	M_A_DQ27 AH68	DDR1_DQ[11]/DDR0_DQ[27]	
	M_A_DQ28 AF71	DDR1_DQ[12]/DDR0_DQ[28]	
	M_A_DQ29 AF69	DDR1_DQ[13]/DDR0_DQ[29]	
	M_A_DQ30 AH70	DDR1_DQ[14]/DDR0_DQ[30]	
	M_A_DQ31 AH69	DDR1_DQ[15]/DDR0_DQ[31]	
M_A_DQ[32:39]	M_A_DQ32 BB65	DDR0_DQ[16]/DDR0_DQ[32]	
	M_A_DQ33 AW65	DDR0_DQ[17]/DDR0_DQ[33]	
	M_A_DQ34 AW63	DDR0_DQ[18]/DDR0_DQ[34]	
	M_A_DQ35 AY63	DDR0_DQ[19]/DDR0_DQ[35]	
	M_A_DQ36 BA65	DDR0_DQ[20]/DDR0_DQ[36]	
	M_A_DQ37 AY65	DDR0_DQ[21]/DDR0_DQ[37]	
	M_A_DQ38 BA63	DDR0_DQ[22]/DDR0_DQ[38]	
	M_A_DQ39 BB63	DDR0_DQ[23]/DDR0_DQ[39]	
M_A_DQ[40:47]	M_A_DQ40 BA61	DDR0_DQ[24]/DDR0_DQ[40]	
	M_A_DQ41 AW61	DDR0_DQ[25]/DDR0_DQ[41]	
	M_A_DQ42 BB59	DDR0_DQ[26]/DDR0_DQ[42]	
	M_A_DQ43 AW59	DDR0_DQ[27]/DDR0_DQ[43]	
	M_A_DQ44 BB61	DDR0_DQ[28]/DDR0_DQ[44]	
	M_A_DQ45 AY61	DDR0_DQ[29]/DDR0_DQ[45]	
	M_A_DQ46 BA59	DDR0_DQ[30]/DDR0_DQ[46]	
	M_A_DQ47 AY59	DDR0_DQ[31]/DDR0_DQ[47]	
M_A_DQ[48:55]	M_A_DQ48 AT66	DDR1_DQ[16]/DDR0_DQ[48]	
	M_A_DQ49 AU66	DDR1_DQ[17]/DDR0_DQ[49]	
	M_A_DQ50 AP65	DDR1_DQ[18]/DDR0_DQ[50]	
	M_A_DQ51 AN65	DDR1_DQ[19]/DDR0_DQ[51]	
	M_A_DQ52 AN66	DDR1_DQ[20]/DDR0_DQ[52]	
	M_A_DQ53 AP66	DDR1_DQ[21]/DDR0_DQ[53]	
	M_A_DQ54 AT65	DDR1_DQ[22]/DDR0_DQ[54]	
	M_A_DQ55 AU65	DDR1_DQ[23]/DDR0_DQ[55]	
M_A_DQ[56:63]	M_A_DQ56 AT61	DDR1_DQ[24]/DDR0_DQ[56]	
	M_A_DQ57 AU61	DDR1_DQ[25]/DDR0_DQ[57]	
	M_A_DQ58 AP60	DDR1_DQ[26]/DDR0_DQ[58]	
	M_A_DQ59 AN60	DDR1_DQ[27]/DDR0_DQ[59]	
	M_A_DQ60 AN61	DDR1_DQ[28]/DDR0_DQ[60]	
	M_A_DQ61 AP61	DDR1_DQ[29]/DDR0_DQ[61]	
	M_A_DQ62 AT60	DDR1_DQ[30]/DDR0_DQ[62]	
	M_A_DQ63 AU60	DDR1_DQ[31]/DDR0_DQ[63]	

DDR CH - A

CPU

071.SKYLA.000U

SKYLAKE-U-GP

DDR0_CKN[0]	AU53	M_A_CLK#0
DDR0_CKP[0]	AT53	M_A_CLK0
DDR0_CKN[1]	AU55	M_A_CLK#1
DDR0_CKP[1]	AT55	M_A_CLK1
	BA56	M_A_CKE0
DDR0_CKE[0]	BB56	M_A_CKE1
DDR0_CKE[1]	AW56	M_A_CKE2
DDR0_CKE[2]	AY56	M_A_CKE3
DDR0_CKE[3]		
	AU45	M_A_CS#0
DDR0_CS#[0]	AU43	M_A_CS#1
DDR0_CS#[1]	AT45	M_A_ODT0
DDR0_ODT[0]	AT43	
DDR0_ODT[1]		
	BA51	M_A_CA_A0
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BB54	M_A_CA_A1
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BA52	M_A_CA_A2
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	AY52	M_A_CA_A3
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AW52	M_A_CA_A4
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AY55	M_A_CA_A5
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AW54	M_A_CA_A6
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	BA54	M_A_CA_A7
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA55	M_A_CA_A8
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	AY54	M_A_CA_A9
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]		
	AU46	M_A_CA_B0
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU48	M_A_CA_B1
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AT46	M_A_CA_B2
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AU50	M_A_CA_B3
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU52	M_A_CA_B4
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AY51	M_A_CA_B5
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AT48	M_A_CA_B6
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT50	M_A_CA_B7
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	BB50	M_A_CA_B8
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	AY50	M_A_CA_B9
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	BA50	
DDR0_MA[3]	BB52	
DDR0_MA[4]		
	AM70	M_A_DQS_DN0
DDR0_DQSN[0]	AM69	M_A_DQS_DP0
DDR0_DQSP[0]	AT69	M_A_DQS_DN1
DDR0_DQSN[1]	AT70	M_A_DQS_DP1
DDR0_DQSP[1]	AH66	M_A_DQS_DN2
DDR1_DQSN[0]/DDR0_DQSN[2]	AH65	M_A_DQS_DP2
DDR1_DQSP[0]/DDR0_DQSP[2]	AG69	M_A_DQS_DN3
DDR1_DQSN[1]/DDR0_DQSN[3]	AG70	M_A_DQS_DP3
DDR1_DQSP[1]/DDR0_DQSP[3]	BA64	M_A_DQS_DN4
DDR0_DQSN[2]/DDR0_DQSN[4]	AY64	M_A_DQS_DP4
DDR0_DQSP[2]/DDR0_DQSP[4]	AY60	M_A_DQS_DN5
DDR0_DQSN[3]/DDR0_DQSN[5]	BA60	M_A_DQS_DP5
DDR0_DQSP[3]/DDR0_DQSP[5]	AR66	M_A_DQS_DN6
DDR1_DQSN[2]/DDR0_DQSN[6]	AR65	M_A_DQS_DP6
DDR1_DQSP[2]/DDR0_DQSP[6]	AR61	M_A_DQS_DN7
DDR1_DQSN[3]/DDR0_DQSN[7]	AR60	M_A_DQS_DP7
DDR1_DQSP[3]/DDR0_DQSP[7]		
	AW50	
DDR0_ALERT#	AT52	
DDR0_PAR		
	AY67	V_DDR_CA_VREF
DDR_VREF_CA	AY68	DDR_VREFDQ01_CHA
DDR0_VREF_DQ	BA67	DDR_VREFDQ02_CHB
DDR1_VREF_DQ		
	AW67	DDR_VTT_CTRL
DDR_VTT_CNTL		

A-CLK
A-CKE
A-CTRL
A-CMD (A, B)
M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7

1D2V_S3 3D3V_S0

R401
220KR2F-GP

DDR_VTT_CTRL — S G D — DDR_VTT_CTRL_Q

Q401
DMN5L06K-7-GP
84.05067.031

2nd = 084.00138.0A31

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DDR)

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 4 of 106

Main Func = CPU

DATA

13 M_B_DQ[63:0]

M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63

CMD

13 M_B_CA_A[9:0]

M_B_CA_A0 M_B_CA_A1 M_B_CA_A2 M_B_CA_A3 M_B_CA_A4 M_B_CA_A5 M_B_CA_A6 M_B_CA_A7 M_B_CA_A8 M_B_CA_A9

13 M_B_CA_B[9:0]

M_B_CA_B0 M_B_CA_B1 M_B_CA_B2 M_B_CA_B3 M_B_CA_B4 M_B_CA_B5 M_B_CA_B6 M_B_CA_B7 M_B_CA_B8 M_B_CA_B9

CLK

13 M_B_CLK0
13 M_B_CLK#0
13 M_B_CLK1
13 M_B_CLK#1

CKE

13 M_B_CKE0
13 M_B_CKE1
13 M_B_CKE2
13 M_B_CKE3

CTRL

13 M_B_CS#0
13 M_B_CS#1
13 M_B_ODT0

DQS

13 M_B_DQS_DP[7:0]

M_B_DQS_DP0 M_B_DQS_DP1 M_B_DQS_DP2 M_B_DQS_DP3 M_B_DQS_DP4 M_B_DQS_DP5 M_B_DQS_DP6 M_B_DQS_DP7

13 M_B_DQS_DN[7:0]

M_B_DQS_DN0 M_B_DQS_DN1 M_B_DQS_DN2 M_B_DQS_DN3 M_B_DQS_DN4 M_B_DQS_DN5 M_B_DQS_DN6 M_B_DQS_DN7

CPU1C — 3 OF 20 — SKYLAKE_ULT

M_B_DQ[0:7]	M_B_DQ0	AY39
	M_B_DQ1	AW39
	M_B_DQ2	AY37
	M_B_DQ3	AW37
	M_B_DQ4	BB39
	M_B_DQ5	BA39
	M_B_DQ6	BA37
	M_B_DQ7	BB37
M_B_DQ[8:15]	M_B_DQ8	AY35
	M_B_DQ9	AW35
	M_B_DQ10	AY33
	M_B_DQ11	AW33
	M_B_DQ12	BB35
	M_B_DQ13	BA35
	M_B_DQ14	BA33
	M_B_DQ15	BB33
M_B_DQ[16:23]	M_B_DQ16	AU40
	M_B_DQ17	AT40
	M_B_DQ18	AT37
	M_B_DQ19	AU37
	M_B_DQ20	AR40
	M_B_DQ21	AP40
	M_B_DQ22	AP37
	M_B_DQ23	AR37
M_B_DQ[24:31]	M_B_DQ24	AT33
	M_B_DQ25	AU33
	M_B_DQ26	AU30
	M_B_DQ27	AT30
	M_B_DQ28	AR33
	M_B_DQ29	AP33
	M_B_DQ30	AR30
	M_B_DQ31	AP30
M_B_DQ[32:39]	M_B_DQ32	AY31
	M_B_DQ33	AW31
	M_B_DQ34	AY29
	M_B_DQ35	AW29
	M_B_DQ36	BB31
	M_B_DQ37	BA31
	M_B_DQ38	BA29
	M_B_DQ39	BB29
M_B_DQ[40:47]	M_B_DQ40	AY27
	M_B_DQ41	AW27
	M_B_DQ42	AY25
	M_B_DQ43	AW25
	M_B_DQ44	BB27
	M_B_DQ45	BA27
	M_B_DQ46	BA25
	M_B_DQ47	BB25
M_B_DQ[48:55]	M_B_DQ48	AU27
	M_B_DQ49	AT27
	M_B_DQ50	AT25
	M_B_DQ51	AU25
	M_B_DQ52	AP27
	M_B_DQ53	AN27
	M_B_DQ54	AN25
	M_B_DQ55	AP25
M_B_DQ[56:63]	M_B_DQ56	AT22
	M_B_DQ57	AU22
	M_B_DQ58	AU21
	M_B_DQ59	AT21
	M_B_DQ60	AN22
	M_B_DQ61	AP22
	M_B_DQ62	AP21
	M_B_DQ63	AN21

DDR0_DQ[32]/DDR1_DQ[0] … DDR0_DQ[63]/DDR1_DQ[47]
DDR1_DQ[48] … DDR1_DQ[63]

DDR1_CKN[0] AN45 M_B_CLK#0
DDR1_CKN[1] AN46 M_B_CLK#1
DDR1_CKP[0] AP45 M_B_CLK0
DDR1_CKP[1] AP46 M_B_CLK1 — B-CLK

DDR1_CKE[0] AN56 M_B_CKE0
DDR1_CKE[1] AP55 M_B_CKE1
DDR1_CKE[2] AN55 M_B_CKE2
DDR1_CKE[3] AP53 M_B_CKE3 — B-CKE

DDR1_CS#[0] BB42 M_B_CS#0
DDR1_CS#[1] AY42 M_B_CS#1
DDR1_ODT[0] BA42 M_B_ODT0
DDR1_ODT[1] AW42 — B-CTRL

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5] AY48 M_B_CA_A0
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9] AP50 M_B_CA_A1
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6] BA48 M_B_CA_A2
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8] BB48 M_B_CA_A3
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7] AP48 M_B_CA_A4
DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0] AP52 M_B_CA_A5
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12] AN50 M_B_CA_A6
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11] AN48 M_B_CA_A7
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT# AN53 M_B_CA_A8
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1] AN52 M_B_CA_A9 — A

DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13] BA43 M_B_CA_B0
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15] AY43 M_B_CA_B1
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14] AY44 M_B_CA_B2
DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16] AW44 M_B_CA_B3
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0] BB44 M_B_CA_B4
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2] AY47 M_B_CA_B5
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1] BA44 M_B_CA_B6
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10] AW46 M_B_CA_B7
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1] AY46 M_B_CA_B8
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0] BA46 M_B_CA_B9 — B
DDR1_MA[3] BB46
DDR1_MA[4] BA47 — B-CMD

DDR0_DQSN[4]/DDR1_DQSN[0] BA38 M_B_DQS_DN0
DDR0_DQSP[4]/DDR1_DQSP[0] AY38 M_B_DQS_DP0 — M_B_DQS0
DDR0_DQSN[5]/DDR1_DQSN[1] AY34 M_B_DQS_DN1
DDR0_DQSP[5]/DDR1_DQSP[1] BA34 M_B_DQS_DP1 — M_B_DQS1
DDR1_DQSN[4]/DDR1_DQSN[2] AT38 M_B_DQS_DN2
DDR1_DQSP[4]/DDR1_DQSP[2] AR38 M_B_DQS_DP2 — M_B_DQS2
DDR1_DQSN[5]/DDR1_DQSN[3] AT32 M_B_DQS_DN3
DDR1_DQSP[5]/DDR1_DQSP[3] AR32 M_B_DQS_DP3 — M_B_DQS3
DDR0_DQSN[6]/DDR1_DQSN[4] BA30 M_B_DQS_DN4
DDR0_DQSP[6]/DDR1_DQSP[4] AY30 M_B_DQS_DP4 — M_B_DQS4
DDR0_DQSN[7]/DDR1_DQSN[5] AY26 M_B_DQS_DN5
DDR0_DQSP[7]/DDR1_DQSP[5] BA26 M_B_DQS_DP5 — M_B_DQS5
DDR1_DQSN[6] AR25 M_B_DQS_DN6
DDR1_DQSP[6] AR27 M_B_DQS_DP6 — M_B_DQS6
DDR1_DQSN[7] AR22 M_B_DQS_DN7
DDR1_DQSP[7] AR21 M_B_DQS_DP7 — M_B_DQS7

DDR1_ALERT# AN43
DDR1_PAR AP43
DRAM_RESET# AT13
DDR_RCOMP[0] AR18 SM_RCOMP_0 — R501 1 — 200R2F-L-GP
DDR_RCOMP[1] AT18 SM_RCOMP_1 — R502 1 — 80D6R2F-L-GP
DDR_RCOMP[2] AU18 SM_RCOMP_2 — R503 1 — 162R2F-GP

CPU
071.SKYLA.000U

DDR CH - B

SKYLAKE-U-GP

Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)			Min Trace Spacing (mils)				Max (mils) Length		R (Ω±1%)	Notes
						Diff	Single Ended	Tolerance (%)	Diff	Group	Group to Group[1&2]	Byte [1&2]	Region	Total		
RCOMP[0]	M	MS/SL	VSS	5	12-15					20	25		500	500	200	
RCOMP[1]	M	MS/SL	VSS	5	12-15					20	25		500	500	80.6	
RCOMP[2]	M	MS/SL	VSS	5	12-15					20	25		500	500	162	

<Core Design>

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Main Func = PCH

DETECT&RESET

55 TOUCH_DET#
25 RTC_DET#

DEBUG PORT

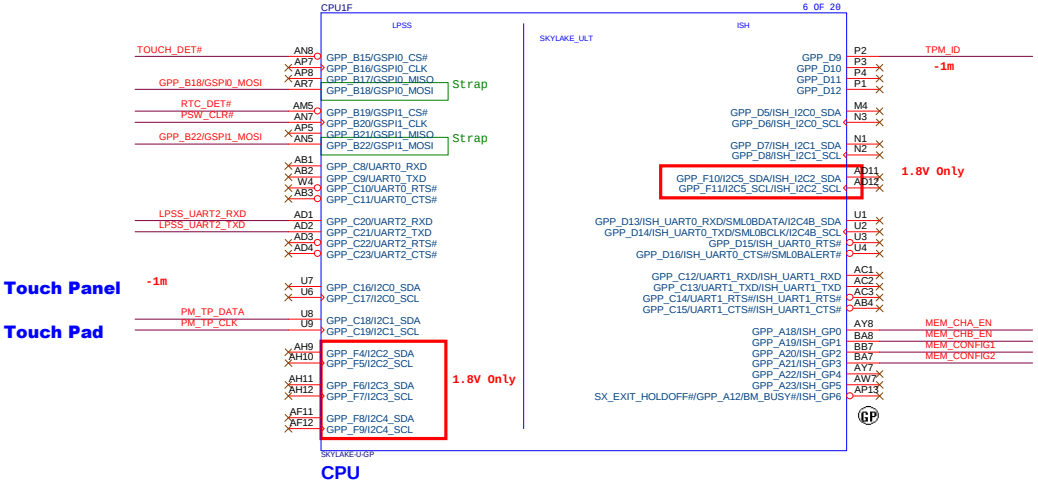
68 LPSS_UART2_RXD
68 LPSS_UART2_TXD

I2C

65 PM_TP_DATA
65 PM_TP_CLK

OTHER

14 GPP_B18/GSPI0_MOSI
14 GPP_B22/GSPI1_MOSI



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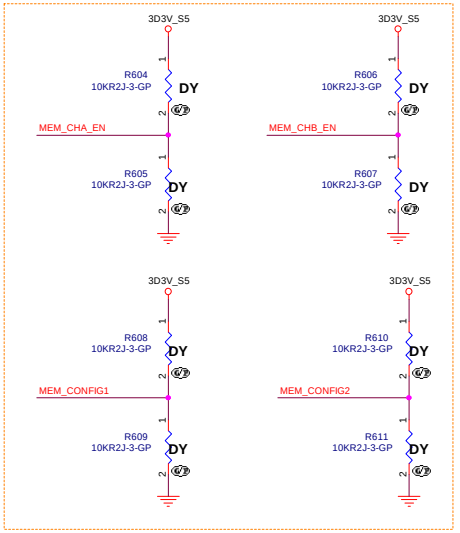

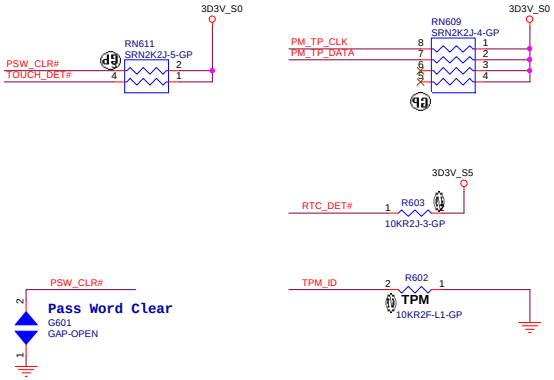

Vender	Config4 (GPIO_A19)	Config3 (GPIO_A18)	Config2 (GPIO_A21)	Config1 (GPIO_A20)	MF.PN	Wistron PN	Capacity	Total Capacity
SK HYNIX	0	0	0	0	H9CCNNN8GTALAR-NUD LF+HF	KN.1GB0G.030	1GB	4GB
SK HYNIX	0	0	0	1	H9CCNNNBLTBLAR-NUD LF+HF	KN.0160G.006	2GB	8GB
SK HYNIX	0	0	1	0	H9CCNNNBJTALAR-NUD LF+HF	KN.2GB0G.053	2GB	8GB
MICRON SG	0	0	1	1	MT52L256M32D1PF-107 LF+HF	KN.8GB04.016	1GB	4GB
MICRON SG	0	1	0	0	MT52L512M32D2PF-107 LF+HF	KN.01604.002	2GB	8GB
MICRON SG	0	1	0	1	MT52L1G32D4PG-107 LF+HF	KN.4GB04.014	4GB	16GB
SK HYNIX	0	1	1	0	H9CCNNNCLGALAR-NUD LF+HF	KN.4GB0G.048	4GB	16GB
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

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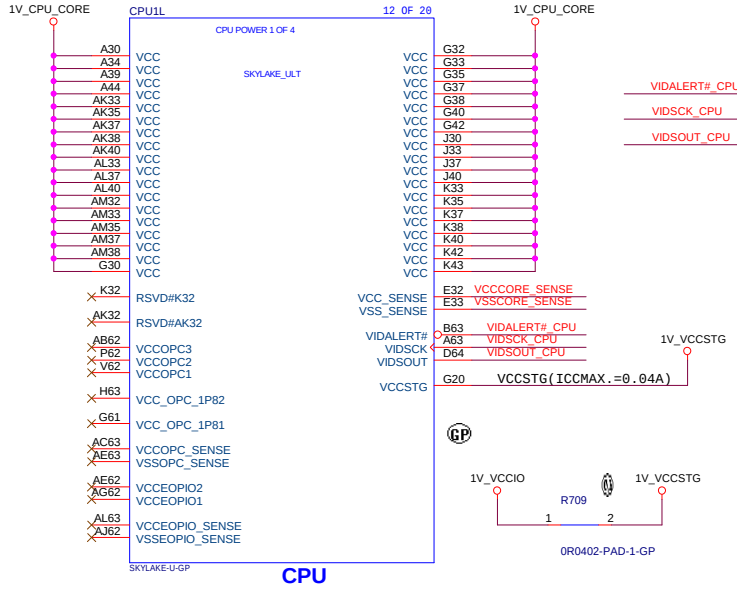
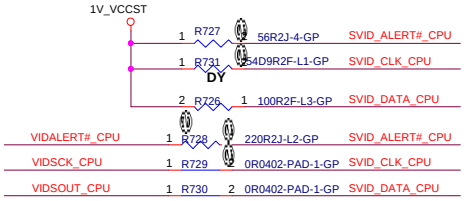
Date: Wednesday, November 01, 2017 | Sheet 6 of 106

Main Func = CPU

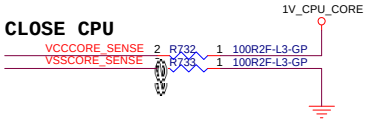
SVID

46 SVID_ALERT#_CPU
46 SVID_CLK_CPU
46 SVID_DATA_CPU
46 VCCCORE_SENSE
46 VSSCORE_SENSE





CLOSE CPU



1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology

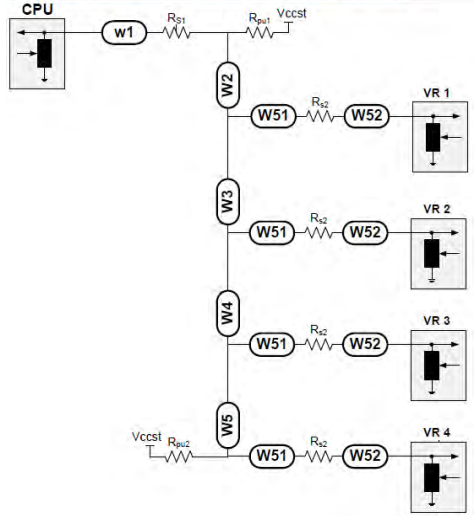


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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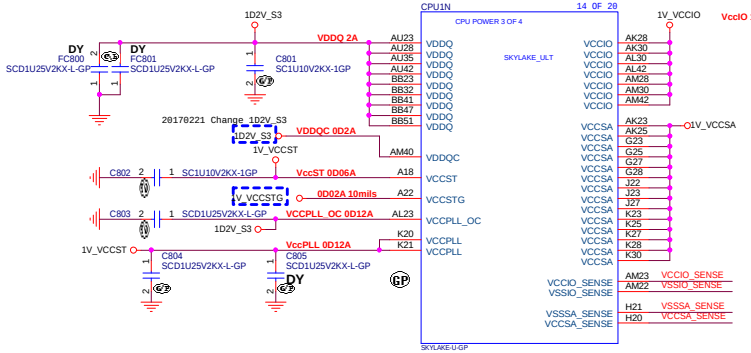
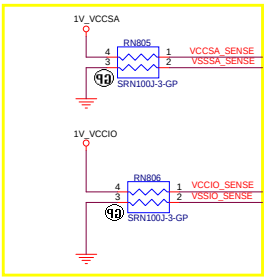
Rev: -1M
Date: Wednesday, November 01, 2017
Sheet 7 of 106

Main Func = CPU

46 VSSSA_SENSE
46 VCCSA_SENSE
46 VCCGT_SENSE
46 VSSGT_SENSE

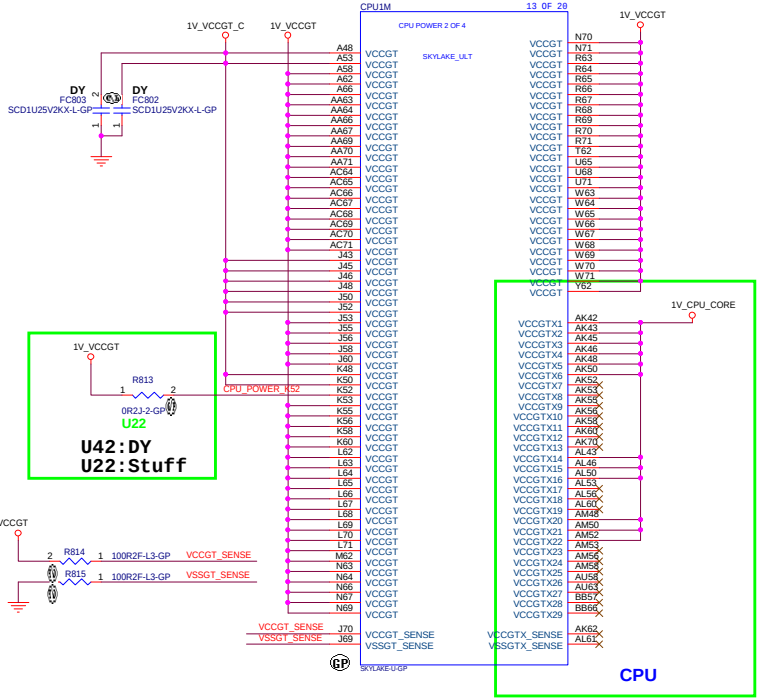


CPU



20170223 Delete

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 44, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.

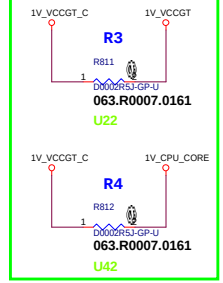


CPU

U42 and U22 power co-lay

If no plan to use U 2+3e in the same platform. These balls can be connected to VccCore. No shunting resistor needed.

20170208 ENG R811 Change to 063.R0007.0161



KBL U42 Board Compatibility with KBL U22/23e

- 4 Rshunts Required
- R1 – between VCCGTU VR and VCCGTU
- R2 – between VCCGTU and VCCCORE
- R3 – between VCCGT and VCCGT VR
- R4 – between VCCGT and VCCCORE
- Stuff R1 and R3 when U22 or U23e mount on board
- Stuff R2 and R4 and de-pop R1 and R3 when U42 mount on board

U22	R1	X	R3	X
U42	X	R2	X	R4

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Sheet 8 of 106

Blanking

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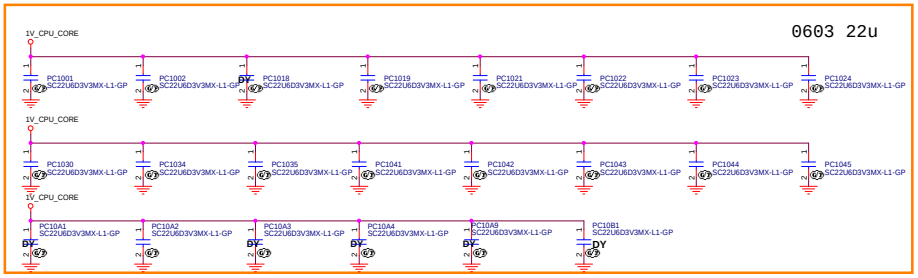
Main Func = CPU

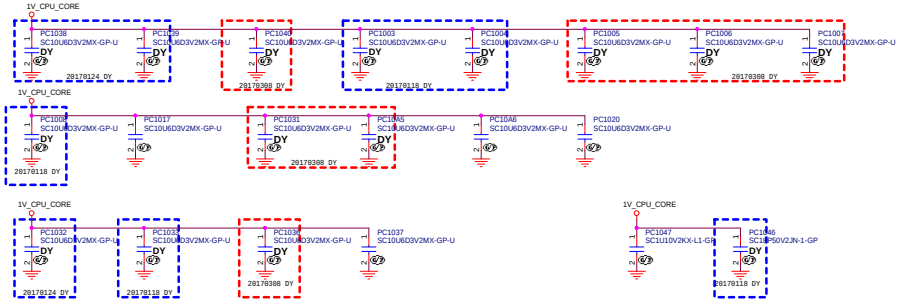
1V_CPU_CORE

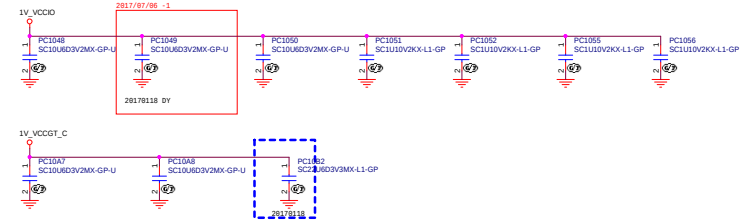
U22 0603 22uF *22 , 0402 10uF*11 , 1uF*1

U42 0603 22uF *4 , 0402 10uF*15

0603 22u

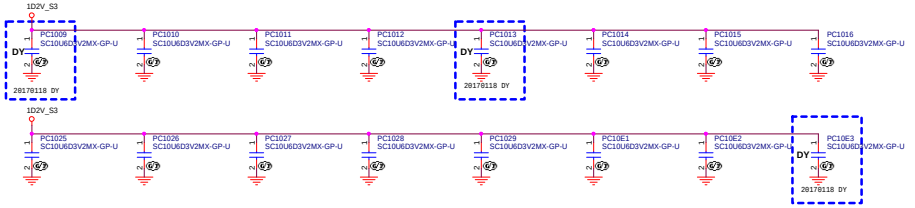




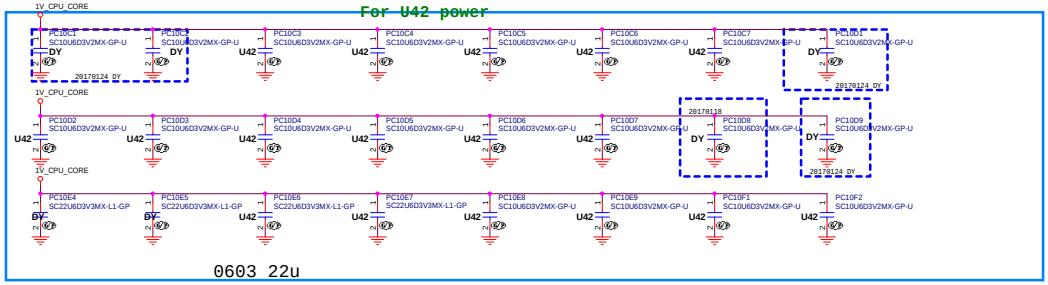


1D2V_S3

0402 10uF*13



For U42 power



0603 22u

1V_VCCIO

10uF * 2 1uF *4

Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)	1x 220 uF (@4.5mΩ ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mΩ ESR)		Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mΩ ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

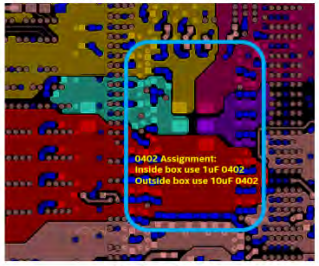
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/Vcc_{GT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0201	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{GT} closest adjacent layer over any power net other than ground.
Vcc_{GT}		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.



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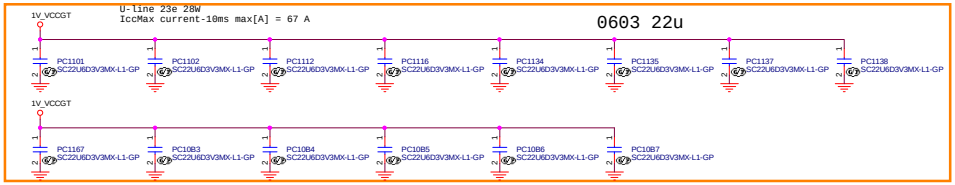
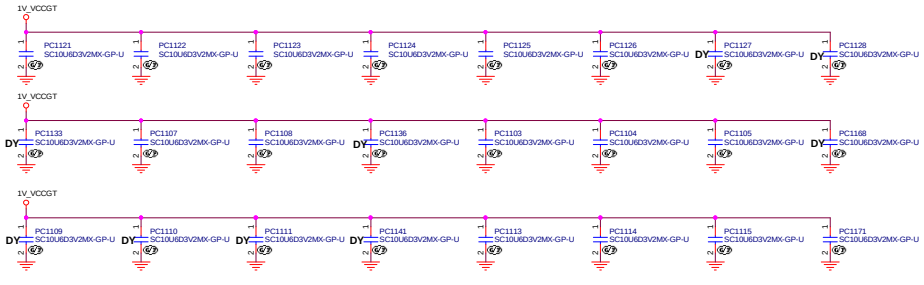
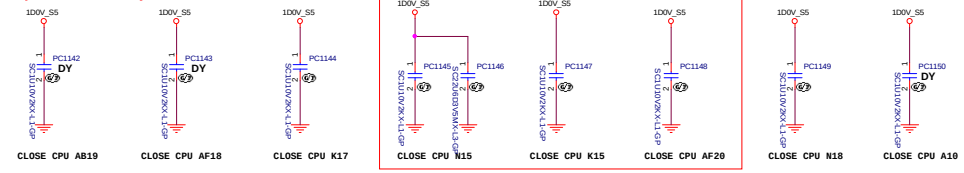
Main Func = CPU

SLICED GT







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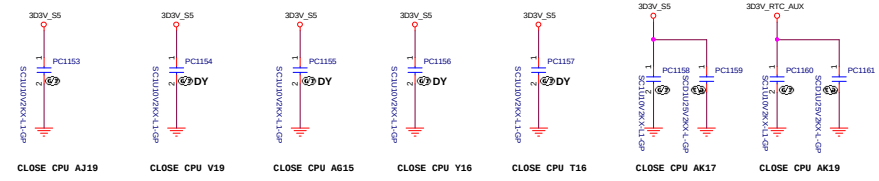

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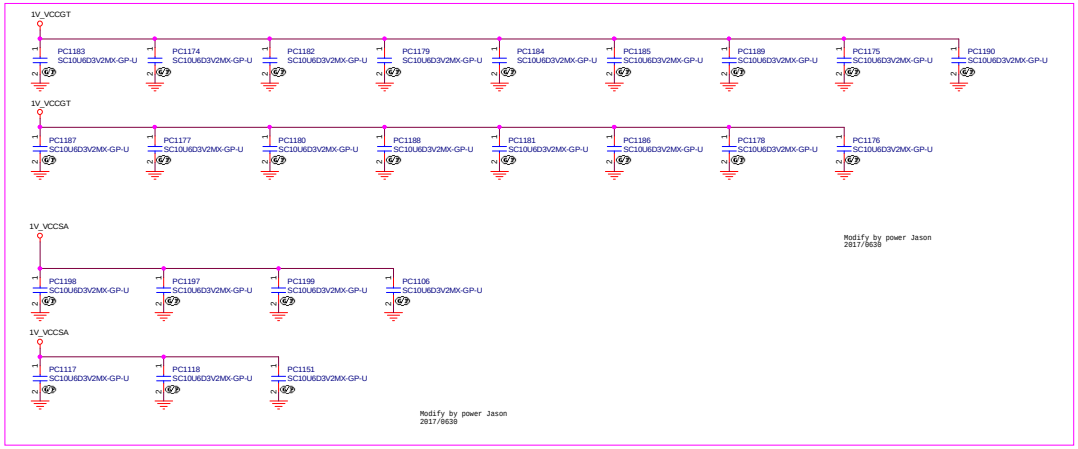
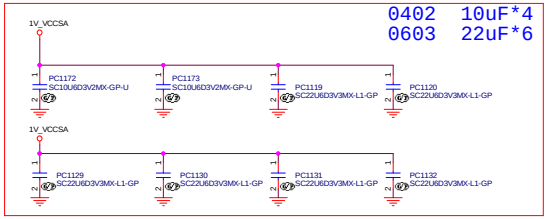


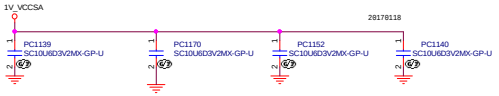
1V_VCCGT

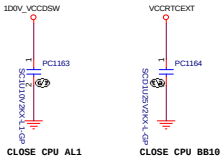
0603 22uF *14 , 0402 10uF*28

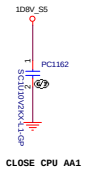
1V_VCCSA

2017/05/16 - SB
2017/05/19 - SB









U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	3X22uF	
								0r	1x330uF/9mW	3X22uF	
	GT	750MHz	40A (31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	2X22uF	
								0r	1x330uF/9mW	3X22uF	
	SA	750MHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF	

<Core Design>
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Title: CPU_(Power CAP2)

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 11 of 106

Channel A

DATA

4 M_A_DQ[63:0]

M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ3 M_A_DQ4 M_A_DQ5 M_A_DQ6 M_A_DQ7 M_A_DQ8 M_A_DQ9 M_A_DQ10 M_A_DQ11 M_A_DQ12 M_A_DQ13 M_A_DQ14 M_A_DQ15 M_A_DQ16 M_A_DQ17 M_A_DQ18 M_A_DQ19 M_A_DQ20 M_A_DQ21 M_A_DQ22 M_A_DQ23 M_A_DQ24 M_A_DQ25 M_A_DQ26 M_A_DQ27 M_A_DQ28 M_A_DQ29 M_A_DQ30 M_A_DQ31 M_A_DQ32 M_A_DQ33 M_A_DQ34 M_A_DQ35 M_A_DQ36 M_A_DQ37 M_A_DQ38 M_A_DQ39 M_A_DQ40 M_A_DQ41 M_A_DQ42 M_A_DQ43 M_A_DQ44 M_A_DQ45 M_A_DQ46 M_A_DQ47 M_A_DQ48 M_A_DQ49 M_A_DQ50 M_A_DQ51 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ56 M_A_DQ57 M_A_DQ58 M_A_DQ59 M_A_DQ60 M_A_DQ61 M_A_DQ62 M_A_DQ63

DQS

4 M_A_DQS_DP[7:0]

M_A_DQS_DP0 M_A_DQS_DP1 M_A_DQS_DP2 M_A_DQS_DP3 M_A_DQS_DP4 M_A_DQS_DP5 M_A_DQS_DP6 M_A_DQS_DP7

4 M_A_DQS_DN[7:0]

M_A_DQS_DN0 M_A_DQS_DN1 M_A_DQS_DN2 M_A_DQS_DN3 M_A_DQS_DN4 M_A_DQS_DN5 M_A_DQS_DN6 M_A_DQS_DN7

CMD

4 M_A_CA_A[9:0]

M_A_CA_A0 M_A_CA_A1 M_A_CA_A2 M_A_CA_A3 M_A_CA_A4 M_A_CA_A5 M_A_CA_A6 M_A_CA_A7 M_A_CA_A8 M_A_CA_A9

4 M_A_CA_B[9:0]

M_A_CA_B0 M_A_CA_B1 M_A_CA_B2 M_A_CA_B3 M_A_CA_B4 M_A_CA_B5 M_A_CA_B6 M_A_CA_B7 M_A_CA_B8 M_A_CA_B9

CLK

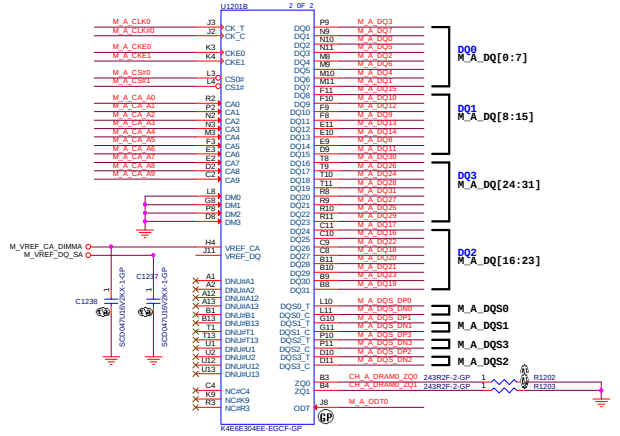
4 M_A_CLK0
4 M_A_CLK#0
4 M_A_CLK1
4 M_A_CLK#1

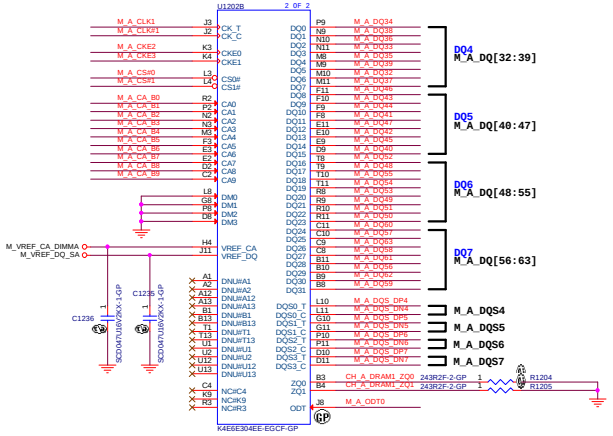
CKE

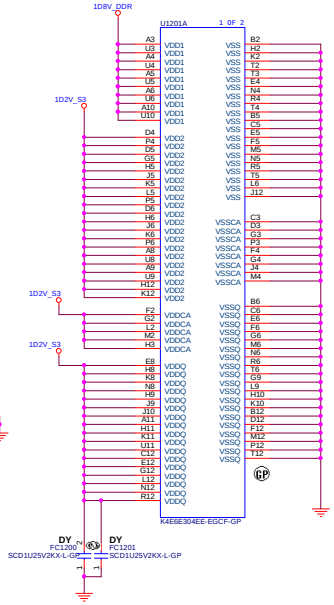
4 M_A_CKE0
4 M_A_CKE1
4 M_A_CKE2
4 M_A_CKE3

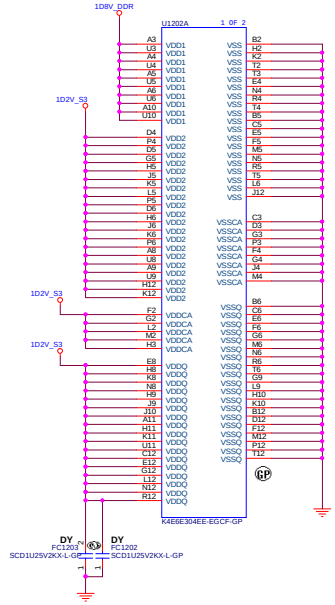
CTRL

4 M_A_CS#0
4 M_A_CS#1
4 M_A_ODT0



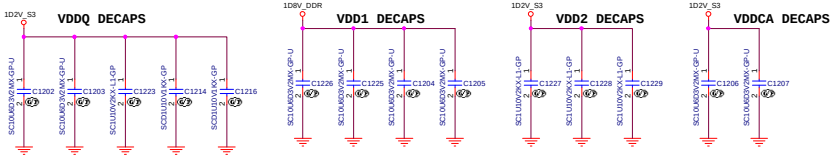




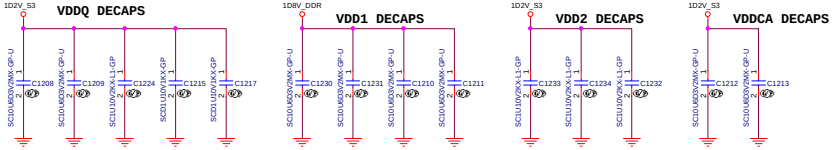


LPDDR3 DECAPS follow SkyLake U/Y PDG Table 4-58

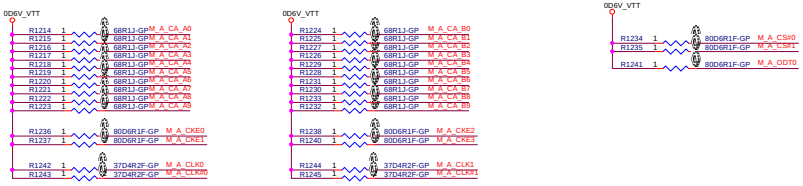
Layout Note: Place these Caps near U1201



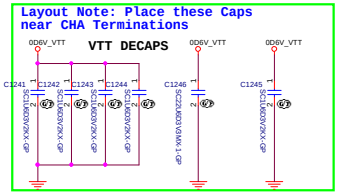
Layout Note: Place these Caps near U1202



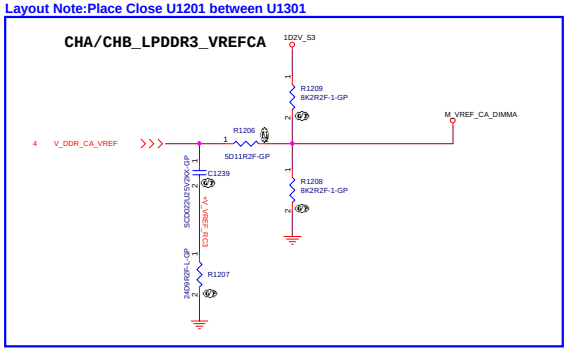
CHA TERMINATIONS



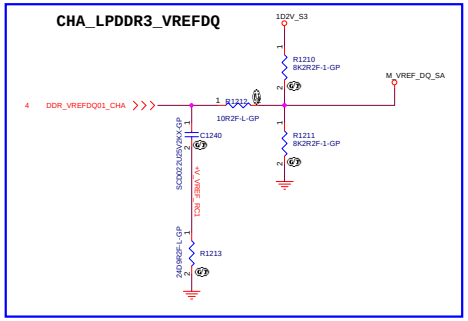
Layout Note: Place these Caps near CHA Terminations



Layout Note:Place Close U1301 between U1301



Layout Note:Place Close U1201



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Title: LPDDR3 CHA

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 12 of 106

Channel B

DATA

DQS

CMD

CLK

CKE

CTRL

LPDDR3 DECAPS follow SkyLake U/Y PDG Table 4-58

Layout Note: Place these Caps near U1301

Layout Note: Place these Caps near U1302

Layout Note: Place these Caps near CHB Terminations

Layout Note:Place Close U1301

CHB TERMINATIONS

Wistron Corporation
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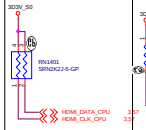
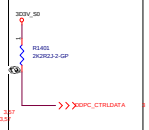
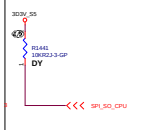
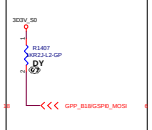
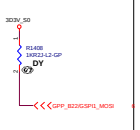
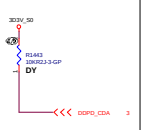
Title: LPDDR3_CHB

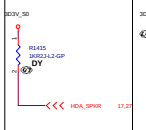
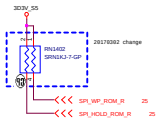
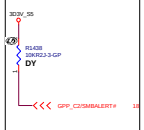
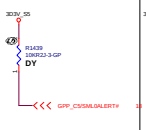
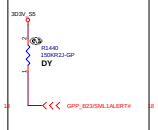
Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 13 of 106

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. BIT 10 — Boot BIOS Destination 0 — SPI 1 — LPC *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. *Notes:* 1. The internal pull-down is disabled after RSMRST# de asserts. 2. This signal is in the primary well.
SMLOALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected for EC. 1 = **eSPI** is selected for EC. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2) Input	De-Glitch (Note 2) Output	Multiplexed With	Default	NMI or SMI Capable	Note
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts
GPP_B23	20K PD (see note)	Yes	No	SML1ALERT#/ PCHHOT#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio Interface					
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLK	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Driven Low		OFF
HDA_SDI[1:0]	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	Off
SPI0_MOSI	Primary	Internal Pull-up/ Pull-down (See Note 1 &2)	Driven Low	Driven Low	Off
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	Off
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	Off
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	Off
SPI1_CLK	Primary	Undriven	Undriven	Undriven	Off
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	Off
SPI1_MISO	Primary	Undriven	Undriven	Undriven	Off
SPI1_CS#	Primary	Undriven	Undriven	Undriven	Off
SPI_IO[2:3]	Primary	Undriven	Undriven	Undriven	Off

Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.
2. Weak internal pull-down is enabled on assertion RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

<Core Design>

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Title: (Reserved)_SODIMM_SODIMM4

Size: A1 | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 14 of 105

Main Func = PCH

USB3 port1

35 USB1_USB30_RX_N
35 USB1_USB30_RX_P
35 USB1_USB30_TX_N
35 USB1_USB30_TX_P
35 USB1_USB20_N
35 USB1_USB20_P

USB3 port2

35 USB2_USB30_RX_N
35 USB2_USB30_RX_P
35 USB2_USB30_TX_N
35 USB2_USB30_TX_P
36 USB2_USB20_N
36 USB2_USB20_P

USB Type-C

73 USB30_RX_CPU_N3
73 USB30_RX_CPU_P3
73 USB30_TX_CPU_N3
73 USB30_TX_CPU_P3
73 TYPEC_USB20_N
73 TYPEC_USB20_P

USB2.0

61,89 BT_USB20_N
61,89 BT_USB20_P
55 TS_USB20_N
55 TS_USB20_P
55 CCD_USB20_N
55 CCD_USB20_P
92 FP_USB20_N
92 FP_USB20_P

M.2 SSD1

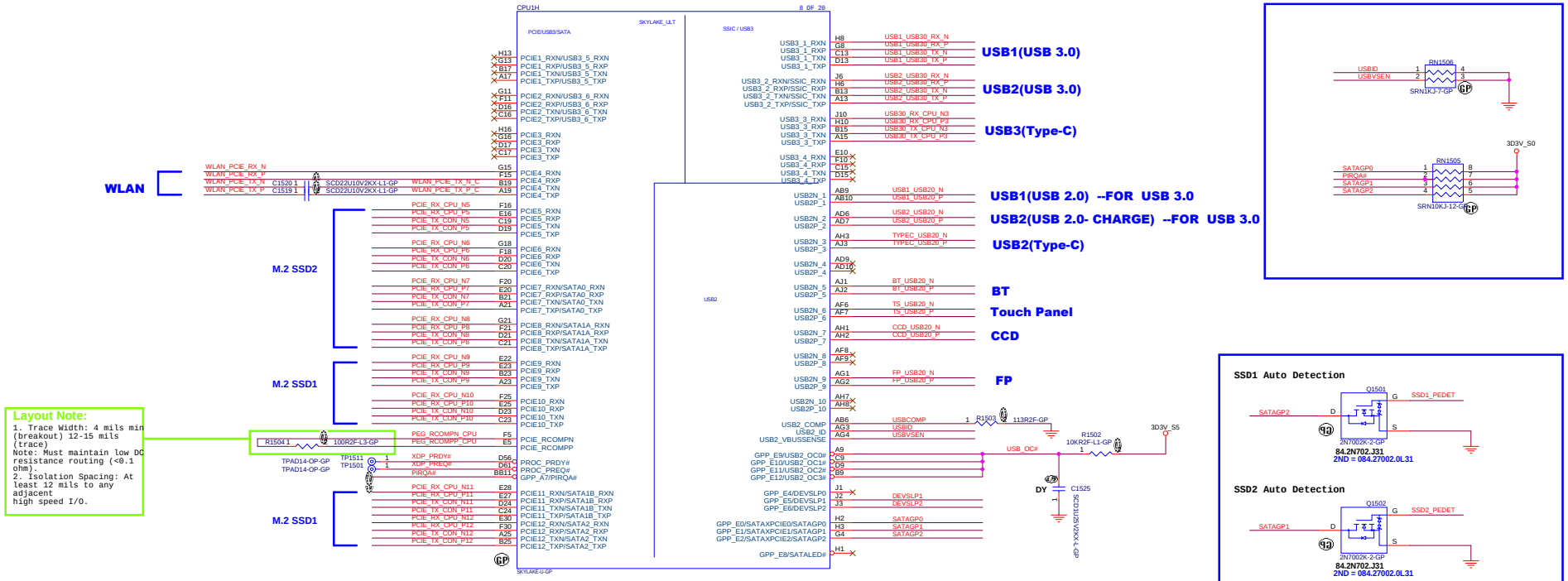
62 PCIE_RX_CPU_N9
62 PCIE_RX_CPU_P9
62 PCIE_TX_CON_N9
62 PCIE_TX_CON_P9
62 PCIE_RX_CPU_N10
62 PCIE_RX_CPU_P10
62 PCIE_TX_CON_N10
62 PCIE_TX_CON_P10
62 PCIE_RX_CPU_N11
62 PCIE_RX_CPU_P11
62 PCIE_TX_CON_N11
62 PCIE_TX_CON_P11
62 PCIE_RX_CPU_N12
62 PCIE_RX_CPU_P12
62 PCIE_TX_CON_N12
62 PCIE_TX_CON_P12
63 DEVSLP1
62 SSD1_PEDET

M.2 SSD2

63 PCIE_RX_CPU_N5
63 PCIE_RX_CPU_P5
63 PCIE_TX_CON_N5
63 PCIE_TX_CON_P5
63 PCIE_RX_CPU_N6
63 PCIE_RX_CPU_P6
63 PCIE_TX_CON_N6
63 PCIE_TX_CON_P6
63 PCIE_RX_CPU_N7
63 PCIE_RX_CPU_P7
63 PCIE_TX_CON_N7
63 PCIE_TX_CON_P7
63 PCIE_RX_CPU_N8
63 PCIE_RX_CPU_P8
63 PCIE_TX_CON_N8
63 PCIE_TX_CON_P8
62 DEVSLP2
63 SSD2_PEDET

WLAN

61,89 WLAN_PCIE_RX_N
61,89 WLAN_PCIE_RX_P
61,89 WLAN_PCIE_TX_N
61,89 WLAN_PCIE_TX_P



071.SKYLA.000U

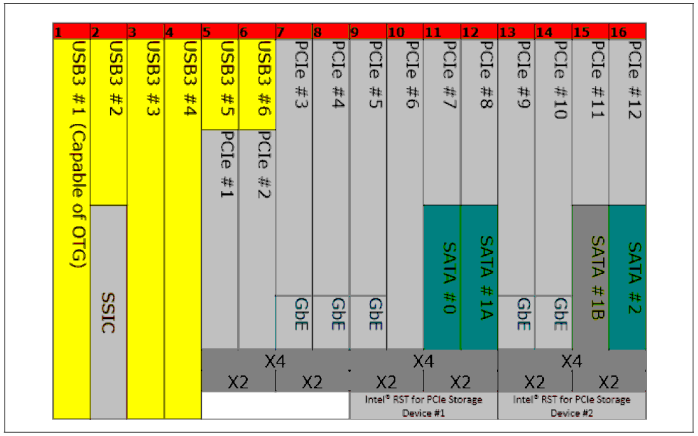
CPU

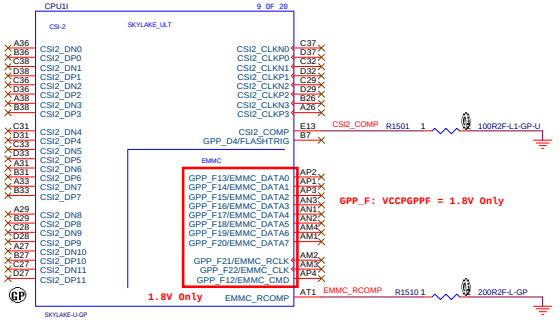
Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in KBL R U PCH-LP





CPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(PCIE/SATA/USB)

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 15 of 106

Main Func = PCH

WLAN
61,89 WLAN_CLK_CPU#
61,89 WLAN_CLK_CPU
61,89 WLAN_CLKREQ_CPU#

SSD1
62 SSD1_CLK_CPU_N
62 SSD1_CLK_CPU_P
62 SSD1_CLKREQ_CPU_N

SSD2
63 SSD2_CLK_CPU_N
63 SSD2_CLK_CPU_P
63 SSD2_CLKREQ_CPU_N

KBC
24 RTCRST_ON

WLAN
61 SUS_CLK_CPU

CPU

CPU1J — 10 OF 20 — CLOCK SIGNALS — SKYLAKE_ULT — SKYLAKE-U-GP

WLAN
PEG_CLKREQ_CPU# D42 C42 AR10 CLKOUT_PCIE_N0 CLKOUT_PCIE_P0 GPP_B5/SRCCLKREQ0#
LAN_CLKREQ_CPU# B42 A42 AT7 CLKOUT_PCIE_N1 CLKOUT_PCIE_P1 GPP_B6/SRCCLKREQ1#
WLAN_CLK_CPU# D41
WLAN_CLK_CPU C41
WLAN_CLKREQ_CPU# AT8 CLKOUT_PCIE_N2 CLKOUT_PCIE_P2 GPP_B7/SRCCLKREQ2#

SSD1
SSD1_CLK_CPU_N D40
SSD1_CLK_CPU_P C40
SSD1_CLKREQ_CPU_N AT10 CLKOUT_PCIE_N3 CLKOUT_PCIE_P3 GPP_B8/SRCCLKREQ3#

SSD2
SSD2_CLK_CPU_N B40
SSD2_CLK_CPU_P A40
SSD2_CLKREQ_CPU_N AU8 CLKOUT_PCIE_N4 CLKOUT_PCIE_P4 GPP_B9/SRCCLKREQ4#

SRCCLKREQ5# E40 E38 AU7 CLKOUT_PCIE_N5 CLKOUT_PCIE_P5 GPP_B10/SRCCLKREQ5#

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43
GPD8/SUSCLK BA17 SUS_CLK_CPU
XTAL24_IN E37 XTL_24M_X1_CPU
XTAL24_OUT E35 XTL_24M_X2_CPU
XCLK_BIASREF E42 XCLK_BIASREF
RTCX1 AM18 XTL_32K_X1_CPU
RTCX2 AM20 XTL_32K_X2_CPU
SRTCRST# AN18 SRTC_RST#
RTCRST# AM16 RTC_RST#

1D0V_S5
R1603 2K7R2F-GP
3D3V_RTC_AUX
SRN20KJ-1-GP RN1601
C1607 SC1U50V3KX-GP
G1601 GAP-OPEN
C1606 SC1U50V3KX-GP

RTC Reset

For AFR
RTCRST_ON
Q1603 2N7002K-2-GP
RTC_RST#_R
RTC_RST#
R1618 100KR2F-L3-GP
R1621 2K2R2J-L1-GP
84.2N702.J31
2ND = 084.27002.0L31

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1615 10MR2J-L-GP
20170210 change
X1602 XTAL-32D768KHZ-91-GP
082.30003.0221
2ND = 082.30003.0301
C1603 SC15P50V2JN-L-GP
C1604 SC15P50V2JN-L-GP

XTL_24M_X1_CPU
U22 C1601 SC15P50V2JN-L-GP
R1602 1MR2F-L-GP
INPUT/OUTPUT#1
NC#2
INPUT/OUTPUT#3
X1601 XTAL-24MHZ-135-GP
082.30006.0041
2nd = 82.30004.A01
XTL_24M_X2_CPU
U22 C1602 SC15P50V2JN-L-GP

X1601 P/N:082.30006.0041

close to CPU
2017/05/18 - SB
3D3V_S0
SSD1_CLKREQ_CPU_N
SSD2_CLKREQ_CPU_N
WLAN_CLKREQ_CPU#
RN1608 SRN10KJ-12-GP
PEG_CLKREQ_CPU#
LAN_CLKREQ_CPU#
SRCCLKREQ5#
RN1609 SRN10KJ-12-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP_CLOCK
Size: Custom
Document Number: Carlsberg_KL
Rev: -1M
Date: Wednesday, November 01, 2017
Sheet 16 of 106

Main Func = PCH

Audio Code

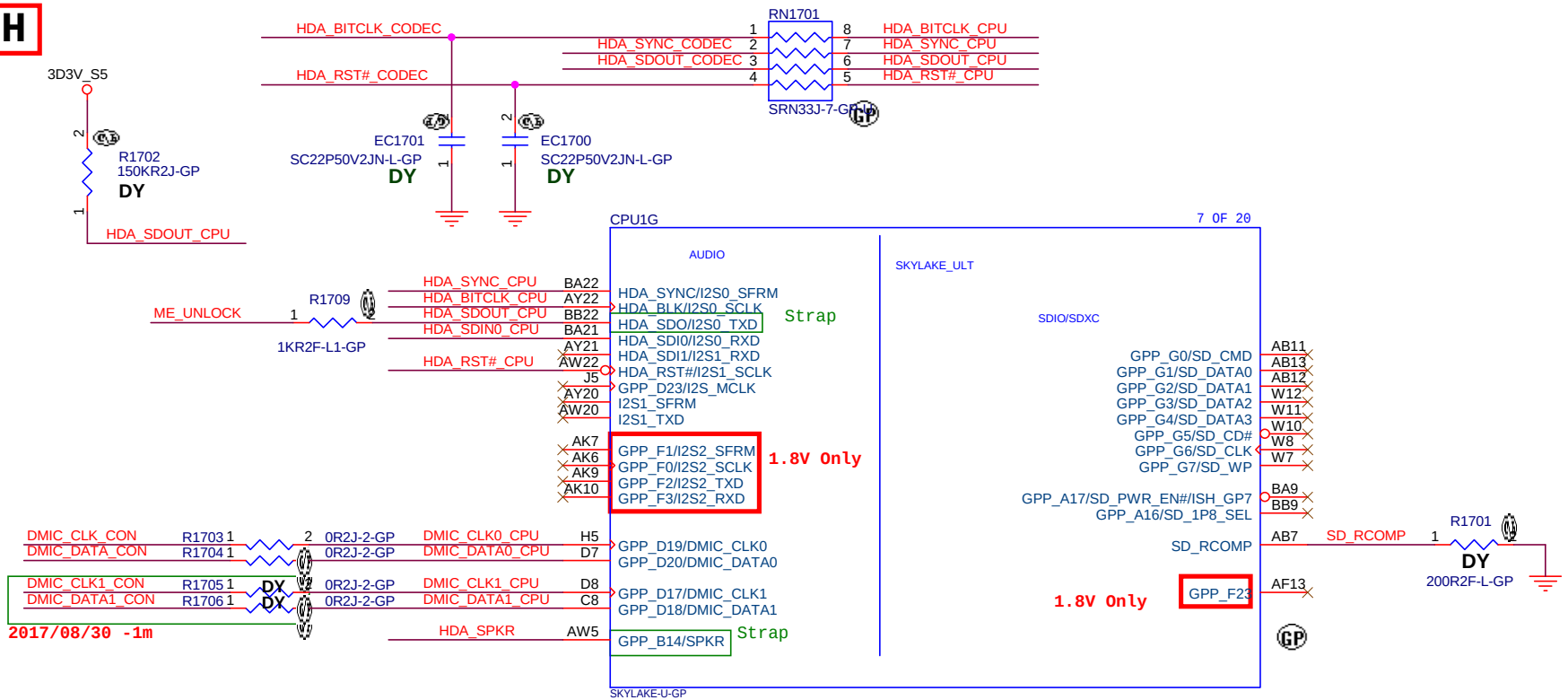
27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
27 HDA_SDOUT_CODEC
27 HDA_SDIN0_CPU
14,27 HDA_SPKR
27 HDA_RST#_CODEC

24 ME_UNLOCK

DMIC

27,55 DMIC_DATA_CON
27,55 DMIC_CLK_CON

55 DMIC_DATA1_CON
55 DMIC_CLK1_CON



CPU

18.3 Terminating Unused SDXC Signals

SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(AUDIO/SDIO/SDXC)		
Size: Custom	Document Number: Carlsberg_KL		Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 17 of 106		

Main Func = PCH

LPC

24,68,91 LPC_AD_CPU_P0
24,68,91 LPC_AD_CPU_P1
24,68,91 LPC_AD_CPU_P2
24,68,91 LPC_AD_CPU_P3
24,68,91 LPC_FRAME#_CPU
18,24 LPC_CLK_KBC
18,68 LPC_CLK_DBG

SPI

24,25 SPI_CS_CPU_N0
24,25 SPI_CLK_ROM
25 SPI_WP_ROM
25 SPI_HOLD_ROM
24,25 SPI_SO_ROM
24,25 SPI_SI_ROM
14 SPI_SO_CPU
14 SPI_SI_CPU

SMBUS

24,73 SML1_CLK
24,73 SML1_DATA

KBC

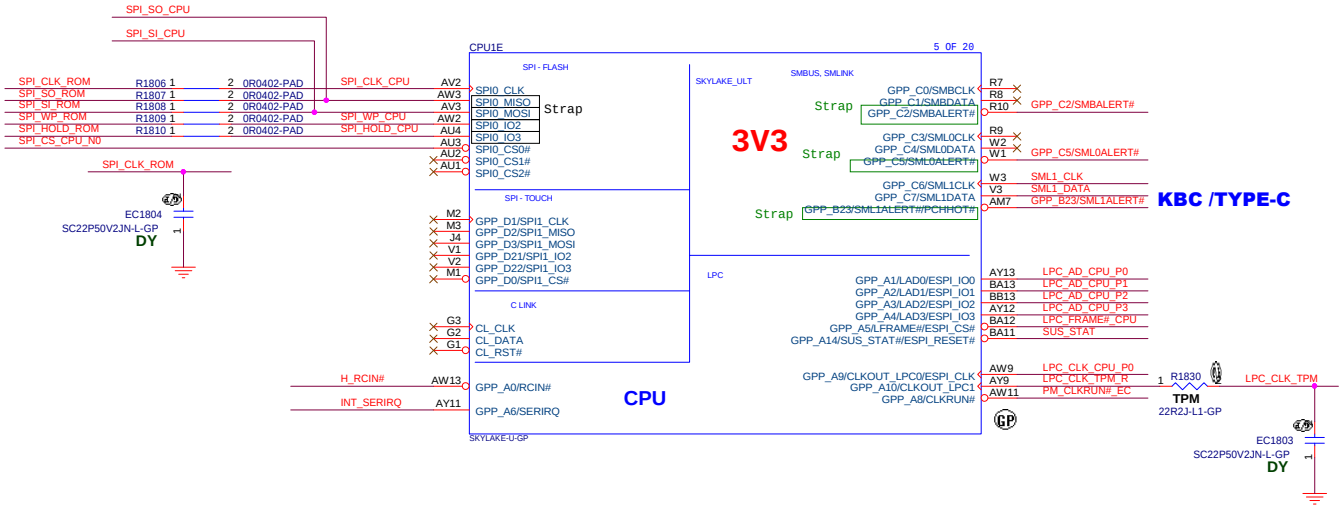
24 H_RCIN#
24,68,91 INT_SERIRQ

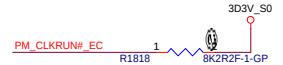
TPM

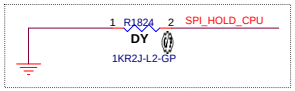
91 LPC_CLK_TPM
91 SUS_STAT
24,91 PM_CLKRUN#_EC

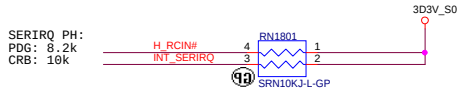
OTHER

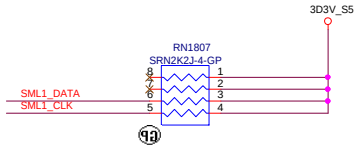
14 GPP_C2/SMBALERT#
14 GPP_C5/SML0ALERT#
14 GPP_B23/SML1ALERT#

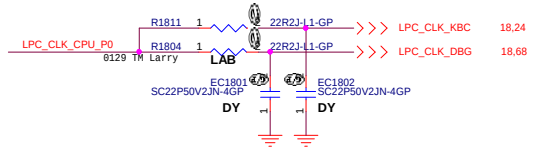












Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

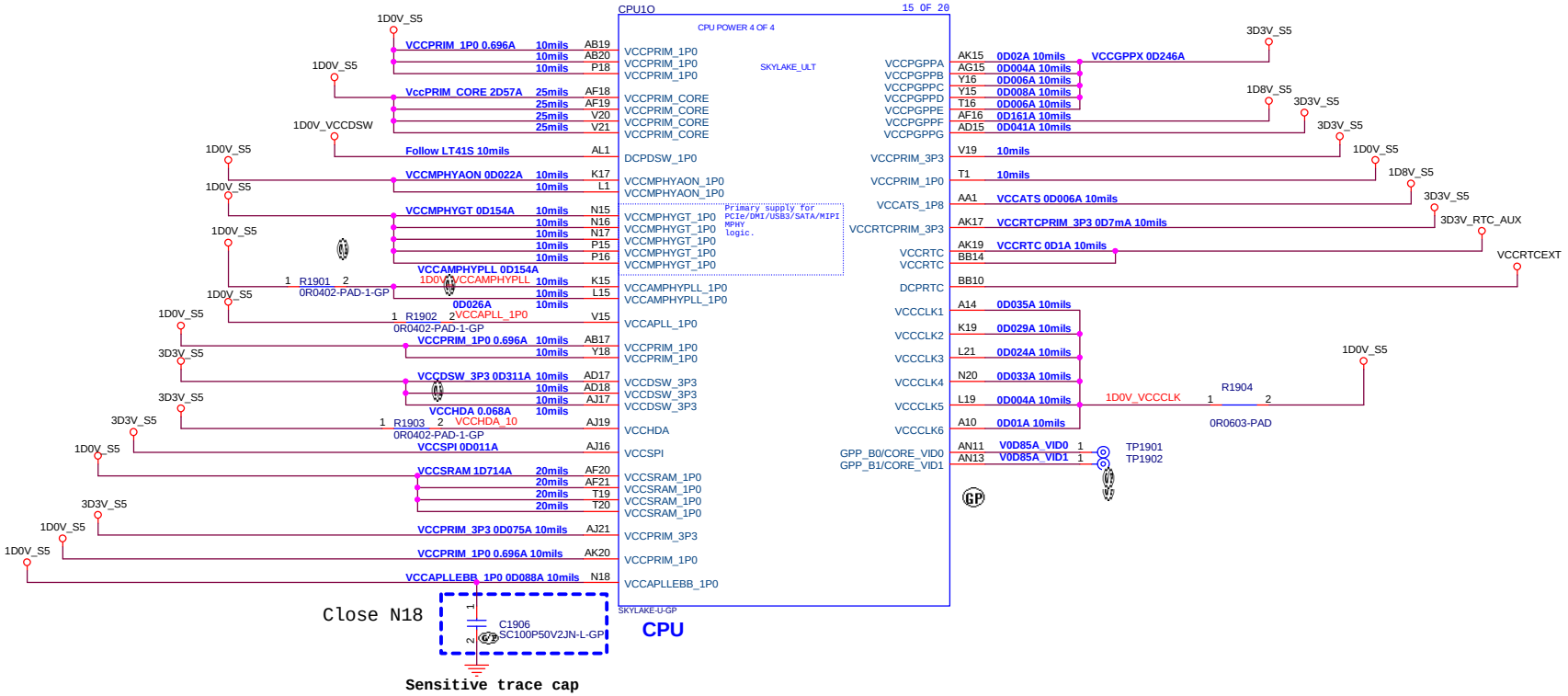
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LPC,SPI,SMBUS,CLINK

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 18 of 106



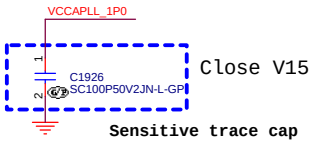


Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SMLOALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 19 of 106

Main Func = PCH

24	SYS_PWROK
40	PCH_PWROK
24,61,62,63	PCIE_WAKE#
24,40	ALL_SYS_PWRGD
24,61,62,63,68,89,91	PLT_RST#
24	RSMRST#_KBC
45,53,73	3V_5V_POK
24,40	PM_SLP_S0#
24,40,45,53	PM_SLP_S3#
24,40,51	PM_SLP_S4#
24	PM_PWRBTN#
24	AC_PRESENT

CPU1K — SYSTEM POWER MANAGEMENT — SKYLAKE_ULT — 11 OF 20

GPP_B13/PLTRST# (AN10) ← PLT_RST#, XDP_DBRESET#, PM_RSMRST#
SYS_RESET# (AY17) ← RSMRST#
PROCPWRGD (A68) ← VCCST_PWRGD
VCCST_PWRGD (B65)
SYS_PWROK (B6) ← SYS_PWROK, PM_PCH_PWROK
PCH_PWROK (BA20) ← PCH_PWROK
DSW_PWROK (BB20) ← PCH_DPWROK
GPP_A13/SUSWARN#/SUSPWRDNACK (AR13) ← PM_SUSWARN#
GPP_A15/SUSACK# (AP11) ← PM_SUSACK#
WAKE# (BB15) ← PCIE_WAKE#
GPD2/LAN_WAKE# (AM15)
GPD11/LANPHYPC (AW17)
GPD7/RSVD#AT15 (AT15)

GPP_B12/SLP_S0# (AT11) → PM_SLP_S0#
GPD4/SLP_S3# (AP15) → PM_SLP_S3#
GPD5/SLP_S4# (BA16) → PM_SLP_S4#
GPD10/SLP_S5# (AY16)
SLP_SUS# (AN15)
SLP_LAN# (AW15)
GPD9/SLP_WLAN# (BB17)
GPD6/SLP_A# (AN16)
GPD3/PWRBTN# (BA15) → PM_PWRBTN#
GPD1/ACPRESENT (AY15) → AC_PRESENT
GPD0/BATLOW# (AU13) → BATLOW#
GPP_A11/PME#/INTRUDER# (AU11, AP16) → SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# (AM10) → EXT_PWR_GATE#
GPP_B2/VRALERT# (AM11)

SKYLAKE-U-GP

CPU

2017/05/11-SB
PCH_PWROK — R2008 0R0402-PAD — PM_RSMRST# — R2006 0R0402-PAD

BATLOW#: Pull-up required even if not implemented.

3D3V_S5
BATLOW# / PM_PWRBTN# — RN2005 SRN10KJ-L-GP
PCIE_WAKE# / AC_PRESENT — RN2006 SRN10KJ-L-GP

PM_SUSACK# — R2017 DY 0R2J-2-GP — PM_SUSWARN#

3D3V_S0
R2024 1KR2F-L1-GP
分壓
ALL_SYS_PWRGD — R2020 10KR2F-L1-GP — VCCST_PWRGD
R2021 4K7R2J-L-GP
C2001 SC100P50V2JN-L-GP
Sensitive trace

-SB 20170316
U2001 U74LVC1G08GW-R-GP-U
RSMRST#_KBC, 3V_5V_POK → PM_RSMRST#
C2002 SCD1U25V2KX-L-GP
73.01G08.EHG
2nd = 73.7SZ08.DAH

3D3V_S5
PM_SUSWARN# — R2030 10KR2F-L1-GP
EXT_PWR_GATE# — R2031 20KR2F-L3-GP
20170217 Change 20k

3D3V_RTC_AUX
SM_INTRUDER# — R2019 1MR2F-L-GP

PM_RSMRST# — R2010 10KR2F-L1-GP
PM_PCH_PWROK — R2011 10KR2J-L-GP

3D3V_AUX_S5
R2004 100KR2F-L3-GP
R2005 10KR2F-L1-GP — 3V_5V_POK_#
Q2001 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.063D1.007C

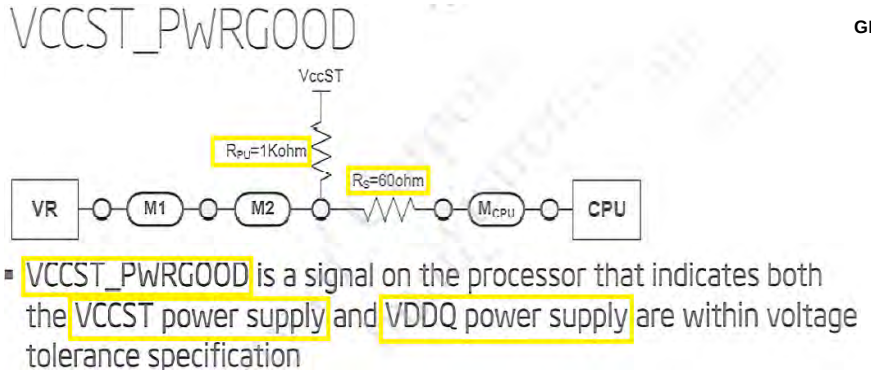
R2001 1KR2F-L1-GP
PM_RSMRST# → 3V_5V_POK_C — R2002 0R0402-PAD — 3V_5V_POK
RSMRST#_KBC
2017/05/11-SB
ED2000 AZ5725-01FDR7G-GP
ED2001 AZ5725-01FDR7G-GP

3D3V_S0
R2014 10KR2F-L1-GP — XDP_DBRESET#

PLT_RST# — EC2020 SC22P50V2JN-L-GP
PM_PCH_PWROK — EC2002 SC10P50V2JN-L-GP

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

VCCST_PWRGD / HWM201:



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

GPP_A13-15 pin(LPC/eSPI):

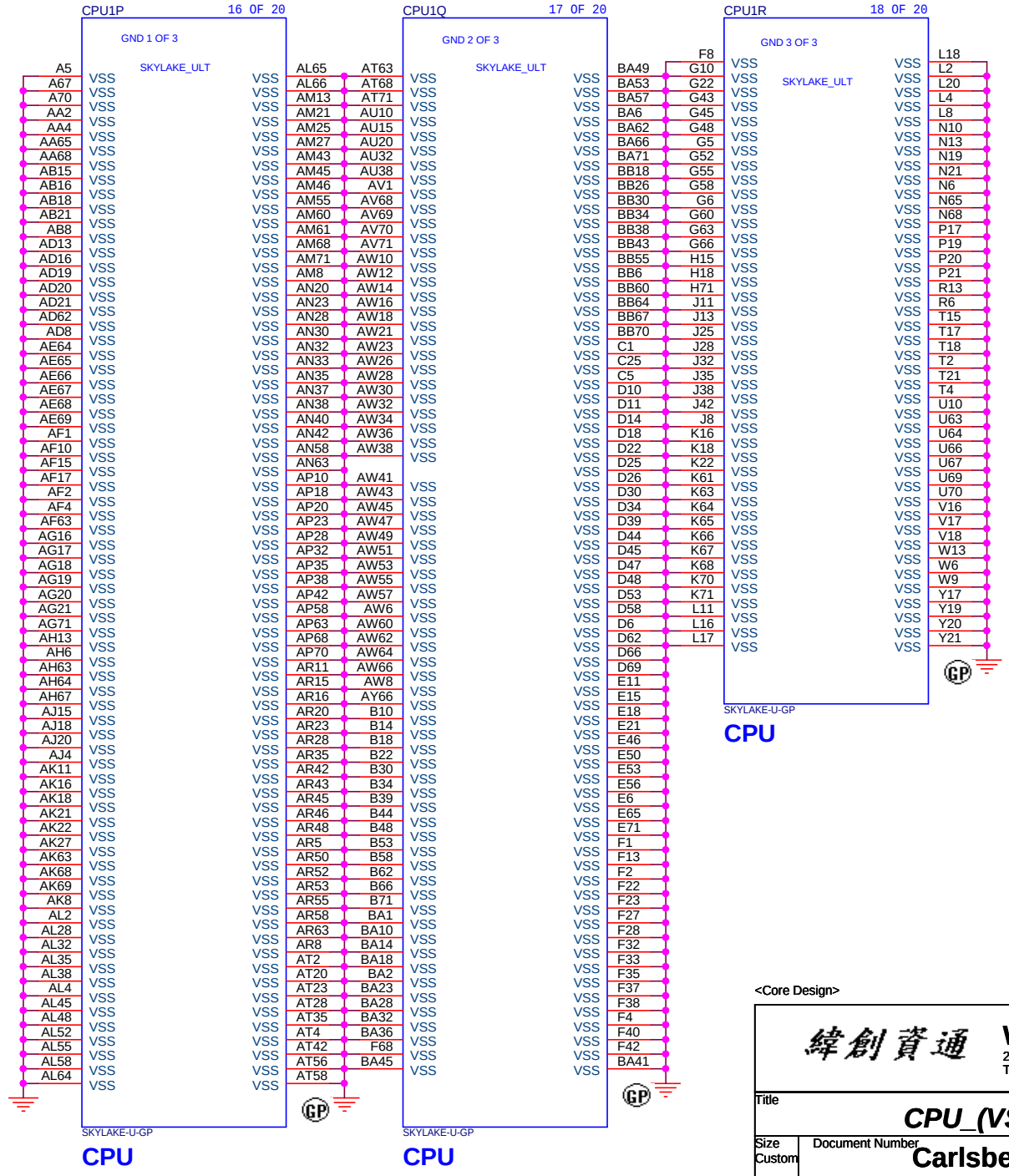
Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: Custom | Document Number: Carlsberg_KL | Rev: -1M
Date: Wednesday, November 01, 2017 | Sheet 20 of 106

Main Func = PCH



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

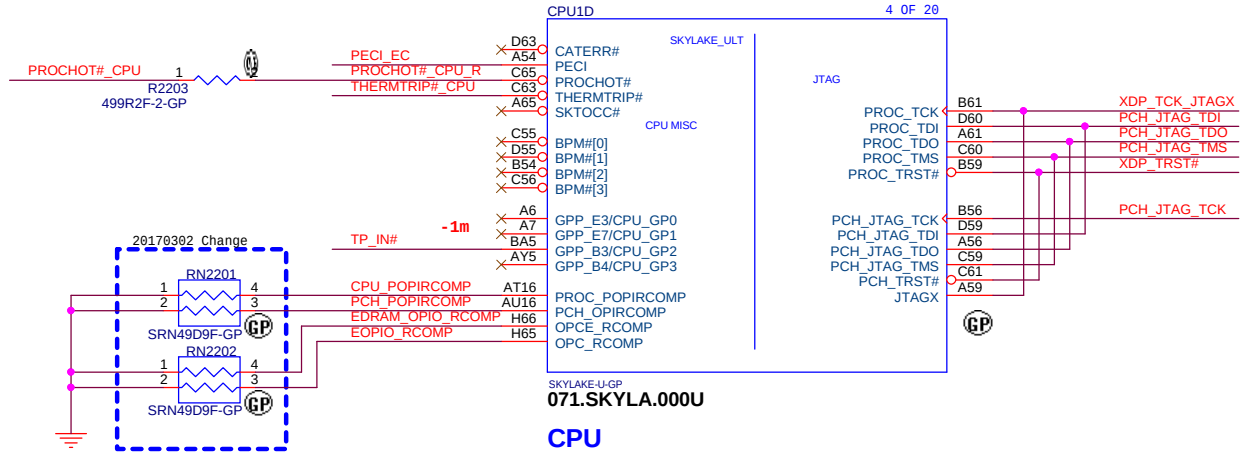
Date: Wednesday, November 01, 2017 | Sheet 21 of 106

Main Func = CPU

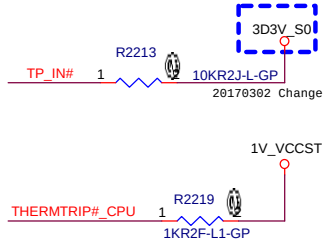
24 PECI_EC

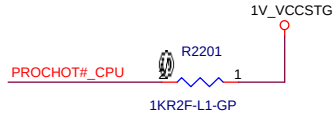
24,44,46 PROCHOT#_CPU

65 TP_IN#



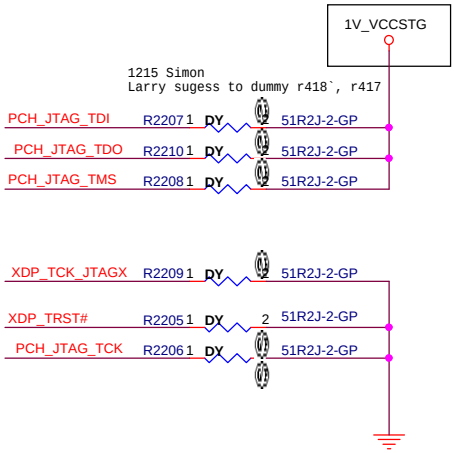
CPU





PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

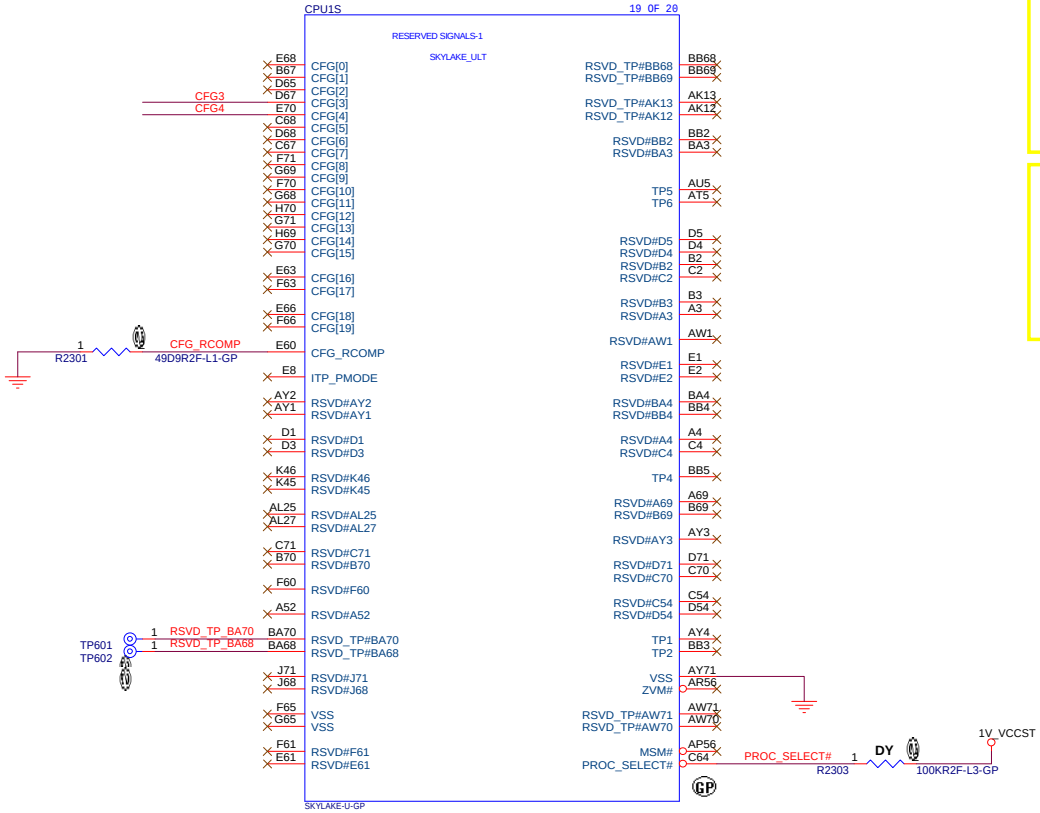
+VCCSTG = 1.0 V



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_(JTAG/CPU SIDE BAND)
Size: Custom	Document Number: Carlsberg_KL
Rev	-1M
Date: Wednesday, November 01, 2017	Sheet 22 of 106

Main Func = CPU



CPU

PCH strap pin:

CFG3 — R2305 1KR2J-1-GP — DY

[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

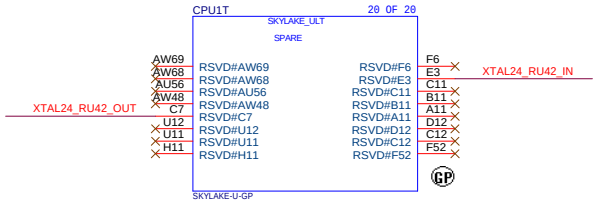
PCH strap pin:

CFG4 — R2304 1KR2J-1-GP

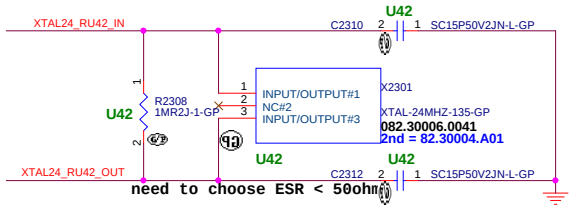
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines



CPU



P/N: 082.30006.0041

<Core Design>

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Title: ***CPU_RESERVED,CFG***

Size: Custom | Document Number: **Carlsberg_KL** | Rev: **-1M**

Date: Wednesday, November 01, 2017 | Sheet 23 of 106

SSID = KBC

Power

- 3D3V_AUX_S5
- 3D3V_S0
- 3D3V_RTC_AUX

Signal

- H_RCIN# 18
- FUN_OFF# 65,89
- LPC_FRAME#_CPU 18,68,91
- LPC_AD_CPU_P3 18,68,91
- LPC_AD_CPU_P2 18,68,91
- LPC_AD_CPU_P1 18,68,91
- LPC_AD_CPU_P0 18,68,91
- LPC_CLK_KBC 18
- PLT_RST# 20,61,62,63,68,89,91
- WLAN_PCIE_WAKE# 24,61
- LID_CLOSE# 66
- PTP_PWR_EN# 65
- PURE_HW_SHUTDOWN# 26,40
- PM_CLKRUN#_EC 18,91
- ES1_TXD 61,68
- EC_TP_IN# 24,65
- KBC_BEEP 27
- KB_BL_DET 65
- FAN1_PWM 26,89
- FAN_TACH1 26,89
- KSI0 65,89
- KSI1 65,89
- KSI2 65,89
- KSI3 65,89
- KSI4 65,89
- KSI5 65,89
- KSI6 65,89
- KSI7 65,89
- KSO0 65,89
- KSO1 65,89
- KSO2 65,89
- KSO3 65,89
- KSO4 65,89
- KSO5 65,89
- KSO6 65,89
- KSO7 65,89
- KSO8 65,89
- KSO9 65,89
- KSO10 65,89
- KSO11 65,89
- KSO12 65,89
- KSO13 65,89
- KSO14 65,89
- KSO15 65,89
- KSO16 65,89
- KSO17 65,89
- AC_IN# 44,74
- DC_Protect_EC 44
- KBC_PWRBTN# 65,89
- BAT_IN# 43,44
- DC_IN_OK 44,73,74
- AD_IA 44
- BT_IA 44
- ALL_SYS_PWRGD 20,40
- STDBY_LED 66,89
- POWER_LED 66,89
- CHARGE_LED 66,89
- DC_BATFULL 66,89
- SML1_CLK 18,73
- SML1_DATA 18,73
- BAT_SCL 43,44
- BAT_SDA 43,44
- SPI_WP_ROM 18,25
- EC_TPCLK 65
- EC_TPDATA 65
- ME_UNLOCK 17
- EC_TP_IN# 24,65
- RTCRST_ON 16
- BLON_OUT 55
- AD_OFF 43
- VD_IN1 26
- VD_OUT1 26
- PROCHOT#_CPU 22,44,46
- RSMRST#_KBC 20
- AMP_MUTE# 27
- 5V_EN 40,45
- KB_BL_PWM 65
- TOUCH_EN 55
- **3V_5S_ENABLE 24,40**
- TYPEC_ILIM 74

2017 05/22 -SB

- PM_SLP_S0# 20,40
- VCCSTG_EN_EC 40

- AC_PRESENT 20
- eDP_BLEN_CPU 3
- PM_PWRBTN# 20
- PCIE_WAKE# 20,61,62,63
- INT_SERIRQ 18,68,91
- EC_SCI# 3

3.3V

- PM_SLP_S3# 20,40,45,53
- PM_SLP_S4# 20,40,51

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

- PD_INT# 73

Type_C

- USB_CHAR_SEL 36
- USB_CHARGER_EN 36
- USB_CHAR_CT1 36

Charger

- WIFI_RF_EN 61
- BLUETOOTH_EN 61,89
- USB_PWR_EN# 35
- WLAN_PCIE_WAKE# 24,61
- CHG_ON# 44
- PECI_EC 22
- WLAN_PERST# 61
- WLAN_PWR_EN# 61
- SYS_PWROK 20
- SPI_SO_ROM 18,25
- SPI_SI_ROM 18,25
- SPI_CLK_ROM 18,25
- SPI_CS_CPU_N0 18,25

Close to the EC

1KR2F-L1-GP R2453 — AD_OFF

PLT_RST# — R2460 47KR2J-L2-GP

RN2412 — 5V_EN — 3V_5S_ENABLE — SRN10KJ-L-GP

3D3V_S0 — RN2410 — FAN_TACH1 — FUN_OFF# — SRN10KJ-L-GP

3D3V_AUX_KBC — RN2413 — BAT_IN# — CHG_ON# — 100KJ-6-GP

3D3V_AUX_S5 — RN2414 — LID_CLOSE# — SRN10KJ-L-GP

3D3V_S0 — R2401 — TOUCH_EN — DY — 10KR2J-L-GP

3D3V_AUX_KBC — R2451 — ECRST# — DY — 10KR2J-3-GP

R2454 — USB_PWR_EN# — DY — 10KR2J-3-GP

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3D3V_S5 — R2402 — TYPEC_ILIM — 10KR2J-3-GP

CPU/Type C --->
BATTER /CHARGER --->
Touch Pad--->

3D3V_S5 — R2441 330KR2J-L-GP — KBC_PWRBTN# — R2414 — KBC_PWRBTN#_R — 470R2F-GP — G2402 GAP-OPEN

EC_SCI# — R2465 — ECSCI#_KBC — 0R0402-PAD-1-GP

PURE_HW_SHUTDOWN# — RN2407 — ECRST# Q — 3D3V_AUX_S5 — SRN10K-J-GP

Q2403 PMBS3906-GP — ECRST# — C2428 SC1U10V2KX-L1-GP

84.03906.F11
2nd = 84.T3906.E11

GPIO0 High Active

PROCHOT_EC — R2408 100KR2F-L3-GP — C2405 SC1U10V2KX-1-GP — Q2404 2N7002K-2-GP — PROCHOT#_CPU

84.2N702.J31
2ND = 084.27602.0L31

Sensitive trace cap

VCC_LPC(Pin9)

3D3V_AUX_KBC — R2435 0R0402-PAD-1-GP — VCC_LPC

For EC power consumption reserver

3D3V_AUX_KBC — 1 R2406 2 — 3D3V_AUX_S5 — 0R0603-PAD-1-GP-U

L2401 BLM15AG121SN-1GP — EC_AGND

68.00084.921
2nd = 68.00217.401

2017 05/22 -SB

U2401 KB9028Q-C-GP

3.3V / 1.8V

LPC_CLK_KBC, LPC_FRAME#_CPU, LPC_AD_CPU_P1, LPC_AD_CPU_P0, LPC_AD_CPU_P3, INT_SERIRQ, TYPEC_ILIM, H_RCIN#, PLT_RST#, ECSCI#_KBC, PM_CLKRUN#_EC, ECRST#

KBC_BEEP, KB_BL_PWM, DC_BATFULL, FAN1_PWM, FAN_TACH1

KSO0–KSO17, KSI0–KSI7

SML1_DATA, SML1_CLK, BAT_SCL

DC_IN_OK, EC_TPCLK, EC_TPDATA, 5V_EN, CHG_ON#, LID_CLOSE#, WLAN_PERST#, STDBY_LED, ES1_TXD, PM_SLP_S0#, ME_UNLOCK, CHARGE_LED, WIN_for_En

3D3V_AUX_KBC, 3D3V_RTC_AUX, VCC_LPC, AVCC, VCC_IO2, AGND, EC_AGND

C2429 SC1U10V2KX-L-GP

AMP_MUTE#, PM_SLP_S4#, WLAN_PCIE_WAKE#, AD_IA, PCB_VER_AD, ADT_TYPE_AD, BT_IA, USB_CHARGER_EN, KB_BL_DET, BLON_OUT, AD_OFF, 3V_5S_ENABLE, TOUCH_EN, RSMRST#_KBC, VD_OUT1, USB_PWR_EN#, SYS_PWROK, RTCRST_ON, PD_INT#, VD_IN1, AC_IN#, USB_CHAR_SEL, KBC_PWRBTN#_R, ALL_SYS_PWRGD, USB_CHAR_CT1, DC_PROTECT_EC, PECI_EC

H_PECI_KBC — 43R2F-2-GP — R2448

WLAN_PWR_EN#, BAT_IN#, POWER_LED

eDP_BLEN_CPU, PM_PWRBTN#, PCIE_WAKE# — R2415 DY 1 0R2J-L-GP — PCIE_WAKE_R

AC_PRESENT, VCCSTG_EN_EC, PHP_PWR_EN#, PROCHOT#_EC, BLUETOOTH_EN, PM_SLP_S3#

SPI_CS_KBC_N0 — R2412 — SPI_CS_CPU_N0
SPI_SI_KBC — R2407 — SPI_SI_ROM
SPI_SO_KBC — R2418 — SPI_SO_ROM
SPI_CLK_KBC — R2411 — SPI_CLK_ROM

071.09028.000G

3D3V_AUX_KBC — R2429 20KR2F-L3-GP **Module_ID** — MODEL_ID_AD — R2431 100KR2F-L3-GP **Module_ID** — EC_AGND

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
CPU_U22	100.0 K	10.0 K	3.000 V
CPU_U42	100.0 K	20.0 K	2.750 V
Reserved for project use	100.0 K	33.0 K	2.481 V
Reserved for project use	100.0 K	47.0 K	2.245 V
Reserved for project use	100.0 K	64.9 K	2.001 V
Reserved for project use	100.0 K	76.8 K	1.867 V
Reserved for project use	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

3D3V_AUX_KBC — R2428 64KR2F-L-GP **PCB_VER** — PCB_VER_AD — 2017/10/17 -LH — R2427 100KR2F-L3-GP **PCB_VER** — EC_AGND

3D3V_AUX_KBC — R2425 100KR2F-L3-GP **Adapter** — ADT_TYPE_AD — R2430 20KR2F-L3-GP **Adapter** — EC_AGND

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.335 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.599 V	>= 0.425 V	< 0.694 V
120W	33.0 K	100.0 K	0.819 V	0.931 V	>= 0.694 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.399 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.399 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.942 V

3D3V_AUX_KBC, 3D3V_AVCC, 3D3V_KBC

L2407 BLM15AG121SN-1GP

C2421 SC1U10V2KX-L-GP, C2424 SC1U10V2KX-L-GP, C2425 SC1U10V2KX-L-GP, C2426 SC1U10V2KX-L-GP, C2420 SC1U10V2KX-L-GP, C2416 SC1U10V2KX-L-GP

C2422 SC1U10V2KX-L-GP, C2427 SC1U10V2KX-L-GP

EC_AGND

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

PM_PWRBTN#, ALL_SYS_PWRGD, SYS_PWROK, AMP_MUTE#, PURE_HW_SHUTDOWN# — ED2401, ED2402, ED2403, ED2404, ED2405 — DY — AZ5725-04F-8R7R-GP

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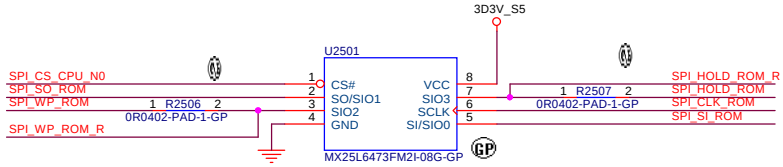
Title: KBC_KB9028
Size: Document Number: Carlsberg_KL — Rev: -1M
Date: Wednesday, November 01, 2017 — Sheet 24 of 106

18,24 SPI_CS_CPU_N0
18,24 SPI_SO_ROM
18 SPI_WP_ROM
14 SPI_WP_ROM_R
14 SPI_HOLD_ROM_R
18 SPI_HOLD_ROM
18,24 SPI_CLK_ROM
18,24 SPI_SI_ROM
6 RTC_DET#

Main Func = SPI Flash

SPI FLASH ROM (8M byte) for PCH

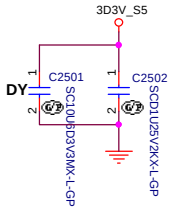
SPI ROM Equal length need to less than 500mil

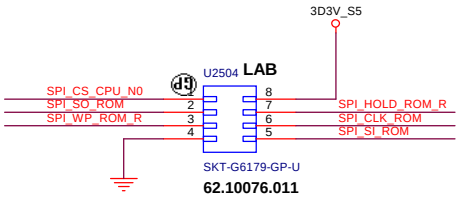


072.25647.000D

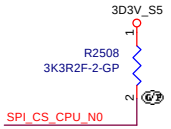
2nd = 072.25Q64.0H01 20170308 Change

072.25647.000D_MX25L6473FM2I-08G_MXIC
072.25Q64.0H01_W25Q64FVSSIQ_WINBOND

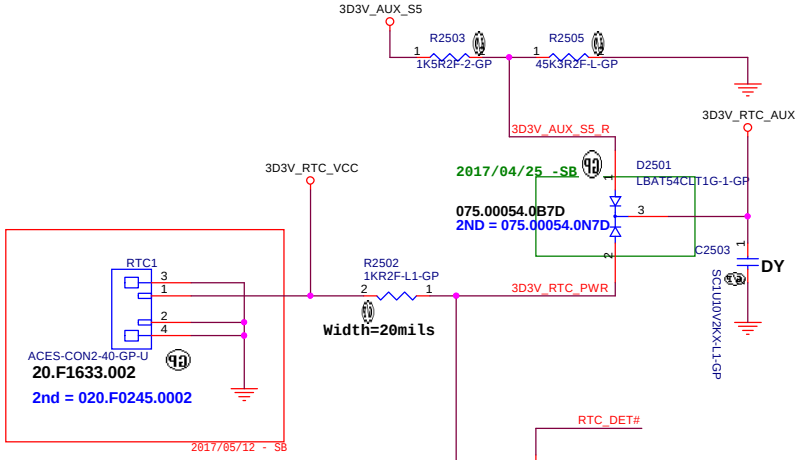




62.10076.011



Main Func = RTC



RTC BATTERY
1st= 023.21220.1101

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Title	*Flash(KBC+PCH)/RTC*	
Size: Custom	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 25 of 106	

24 VD_IN1

24,26,89 FAN1_PWM

24,89 FAN_TACH1

24,40 PURE_HW_SHUTDOWN#

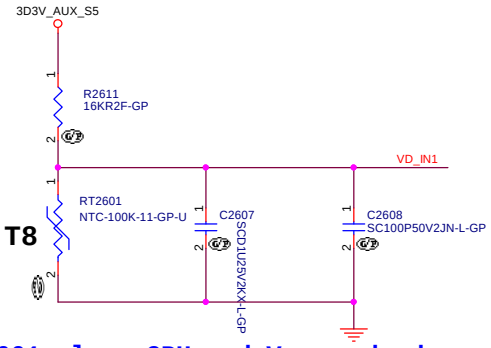
24 VD_OUT1

40,46 VR_RDY

89 FAN_TACH1_C

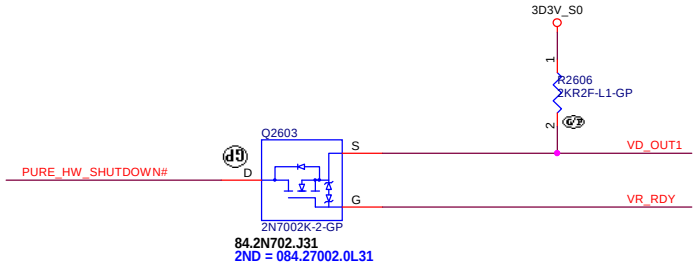
24,26,89 FAN1_PWM

SSID = Thermal

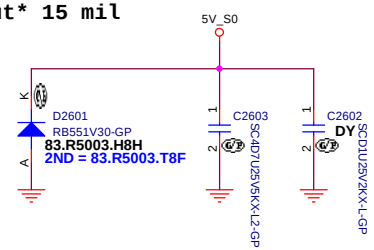


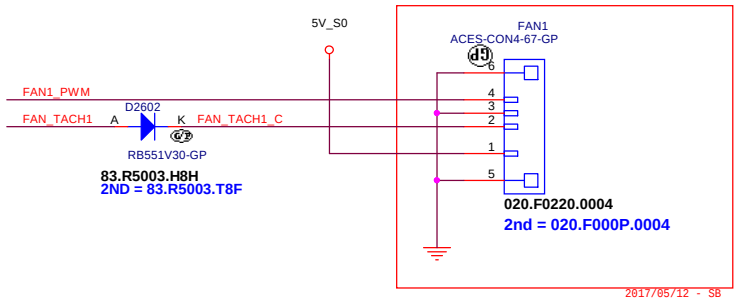
RT2601 close CPU and Vcore chock

VD_IN1 trace 10 mli



***Layout* 15 mil**





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Title: ***Thermal 7718/Fan Controllor P2793***

Size: Custom | Document Number: **Carlsberg_KL** | Rev: **-1M**

Date: Wednesday, November 01, 2017 | Sheet 26 of 106

From CPU

17 HDA_SDOUT_CODEC
17 HDA_BITCLK_CODEC
17 HDA_SDIN0_CPU
17 HDA_SYNC_CODEC
17 HDA_RST#_CODEC

DMIC to eDP Con.

17,55 DMIC_DATA_CON
17,55 DMIC_CLK_CON

Speaker to audio box

29 AUD_SPK1_L+
29 AUD_SPK1_L-
29 AUD_SPK1_R-
29 AUD_SPK1_R+

Universal Jack via IO Board

66,89 SELEEVE
66,89 AUD_HP1_JACK_L2
66,89 AUD_HP1_JACK_R2
66,89 RING2
66,89 AUD_HP1_JD#

24 AMP_MUTE#
24 KBC_BEEP
14,17 HDA_SPKR

SSID = AUDIO

Close to Pin46

Close to Pin41

Close pin36

Close pin40

AUD_AGND close to codec IC

TO Audio BOX

071.00255.0003

TO DB

TO CPU

Close to Pin1

placed nearby codec PIN12

Layout Note:
Place close to Pin 26

Layout Note:
Width>40mil, to improve Headphone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.

<Core Design>

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Title: Audio Codec ALC255

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 27 of 186

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Title: *AUDIO AMP_ALC1001*		
Size: A3	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 28 of 106	

SSID = AUDIO

Speaker

2017/05/16 - SB

27 AUD_SPK1_L-
27 AUD_SPK1_L+
27 AUD_SPK1_R-
27 AUD_SPK1_R+

AUD_SPK1_L- R2914 1 2 0R0603-PAD
AUD_SPK1_L+ R2915 1 2 0R0603-PAD
AUD_SPK1_R- R2916 1 2 0R0603-PAD
AUD_SPK1_R+ R2917 1 2 0R0603-PAD

AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON

SPK1
ACES-CON4-17-GP-U1
20.F1621.004
2nd = 20.F1937.004

EC2901 1 2 SC22P50V2JN-L-GP DY
EC2902 1 2 SC22P50V2JN-L-GP DY
EC2915 1 2 SC22P50V2JN-L-GP DY
EC2920 1 2 SC22P50V2JN-L-GP DY

Layout Note:
Trace width=40mil

AFTP TESTPOINT

89 AUD_SPK1_L-_CON
89 AUD_SPK1_L+_CON
89 AUD_SPK1_R-_CON
89 AUD_SPK1_R+_CON

AUD_SPK1_L-_CON
AUD_SPK1_L+_CON
AUD_SPK1_R-_CON
AUD_SPK1_R+_CON

ED2901
AZ5125-02S-R7G-GP
DY

ED2902
AZ5125-02S-R7G-GP
DY

<Core Design>

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Title: Speaker/ALC255

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 29 of 106

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Title: ***Reserved***

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 30 of 106

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Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 31 of 106

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Title
Reserved

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 32 of 106

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Title: ***Reserved***

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 33 of 106

Blanking

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Title: ***Reserved***

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 34 of 106

USB1

15 USB1_USB20_N
15 USB1_USB20_P

15 USB1_USB30_RX_N
15 USB1_USB30_RX_P

15 USB1_USB30_TX_N
15 USB1_USB30_TX_P

89 USB1_CON_USB20_N
89 USB1_CON_USB20_P

USB2

36 USB2_CHAR_N
36 USB2_CHAR_P

15 USB2_USB30_RX_N
15 USB2_USB30_RX_P

15 USB2_USB30_TX_N
15 USB2_USB30_TX_P

89 USB2_CON_USB20_N
89 USB2_CON_USB20_P

USB Power enable

24 USB_PWR_EN#

Low Active 2A

5V_S5 — C3501 SC1U10V2KX-L1-GP — USB_PWR_EN# — U3501 SY6288DAAC-GP (IN, EN#, OUT, GND, OC#) — 5V_USB30 — C3502 SCD1U10V2KX-GP

074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

5V_USB30 — C3504 SC100U6D3V6MX-GP
5V_USB30_CHARGER — C3516 SC100U6D3V6MX-GP

2017/06/27 -1

5V_USB30_CHARGER — EC3501 SCD1U10V2KX-GP

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

2017/06/29 -1

USB1_USB30_RX_CON_N / USB1_USB30_RX_CON_P / USB1_USB30_TX_N1 (SCD1U25V2KX-L-GP, C3508) / USB1_USB30_TX_P1 (SCD1U25V2KX-L-GP, C3509) — EU3501 L05ESDL5V0NA-4-GP — USB1_USB30_RX_CON_N / USB1_USB30_RX_CON_P / USB1_USB30_TX_CON_N / USB1_USB30_TX_CON_P

075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30 — USB1 — VBUS, D-, D+, CHASSIS#10, CHASSIS#11, CHASSIS#12, CHASSIS#13, GND, GND_DRAIN, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+ — SKT-USB13-355-GP

022.10005.09H1
2nd = 022.10005.09I1

2017/06/29 -1

USB1_USB30_RX_P/N — ER3501 0R2J-2-GP — EL3503 — FILTER-4P-201-GP — ER3502 0R2J-2-GP — USB1_USB30_RX_CON_P/N

USB1_USB30_TX_P/N — ER3503 0R2J-2-GP — EL3504 — FILTER-4P-201-GP — ER3504 0R2J-2-GP — USB1_USB30_TX_P1/N1

USB2_CHAR_N / USB2_CHAR_P — EL3502 FILTER-4P-137-GP-U — USB2_CON_USB20_N / USB2_CON_USB20_P

68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

USB1_CON_USB20_N / USB1_CON_USB20_P — EU3503 AZC099-04S-2-GP (I/O1, I/O2, I/O3, I/O4, GND, VDD) — 5V_S5 — USB2_CON_USB20_N / USB2_CON_USB20_P

075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

2017/06/29 -1

USB2_USB30_RX_CON_N / USB2_USB30_RX_CON_P / USB2_USB30_TX_N1 (SCD1U25V2KX-L-GP, C3510) / USB2_USB30_TX_P1 (SCD1U25V2KX-L-GP, C3511) — EU3502 L05ESDL5V0NA-4-GP — USB2_USB30_RX_CON_N / USB2_USB30_RX_CON_P / USB2_USB30_TX_CON_N / USB2_USB30_TX_CON_P

075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

5V_USB30_CHARGER — USB2 — VBUS, D-, D+, CHASSIS#10, CHASSIS#11, CHASSIS#12, CHASSIS#13, GND, GND_DRAIN, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+ — SKT-USB13-355-GP

022.10005.09H1
2nd = 022.10005.09I1

2017/06/29 -1

USB2_USB30_RX_P/N — ER3505 0R2J-2-GP — EL3505 — FILTER-4P-201-GP — ER3506 0R2J-2-GP — USB2_USB30_RX_CON_P/N

USB2_USB30_TX_N/P — ER3507 0R2J-2-GP — EL3506 — FILTER-4P-201-GP — ER3508 0R2J-2-GP — USB2_USB30_TX_N1/P1

USB1_USB20_N / USB1_USB20_P — EL3501 FILTER-4P-137-GP-U — USB1_CON_USB20_N / USB1_CON_USB20_P

68.01012.20B
2nd = 68.00396.001
3rd = 068.24900.2001

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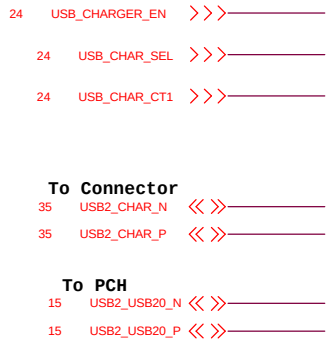
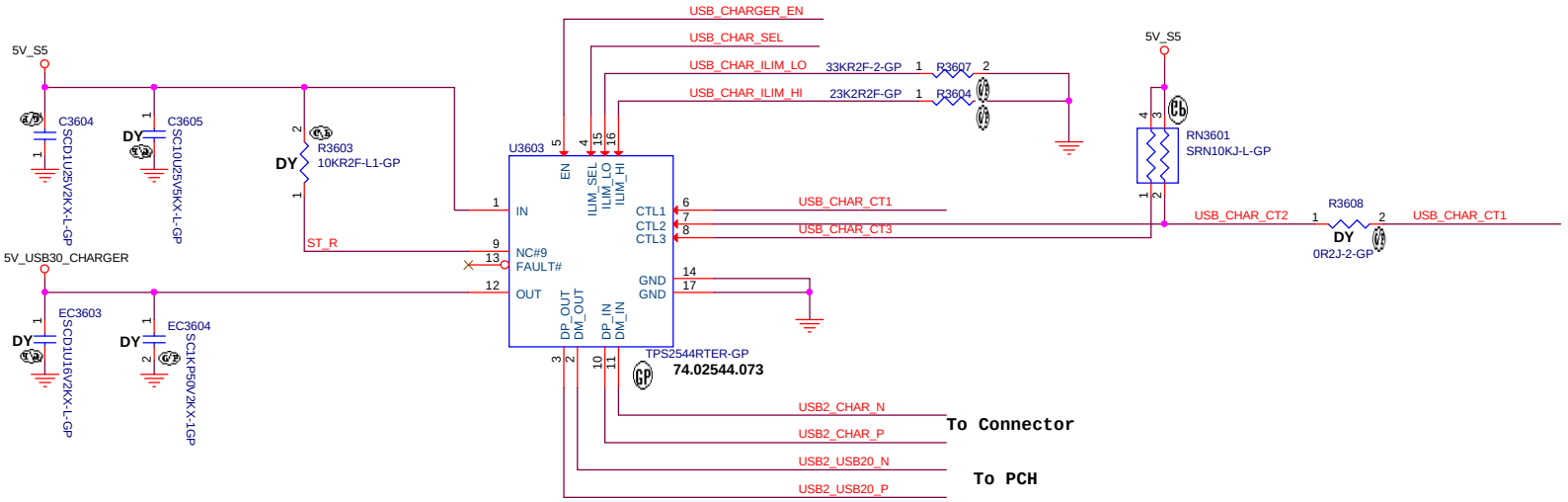
Title: USB 3.0

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 35 of 106





074.52544.0093 need to verify on SA

CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

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Date: Wednesday, November 01, 2017 | Sheet 36 of 106

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Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 37 of 106

Blanking

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Title
USB RE_DRIVER_3D CAMERA

Size	Document Number	Rev
A3	Carlsberg_KL	-1M
Date: Wednesday, November 01, 2017	Sheet 38 of 106	

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Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 39 of 106

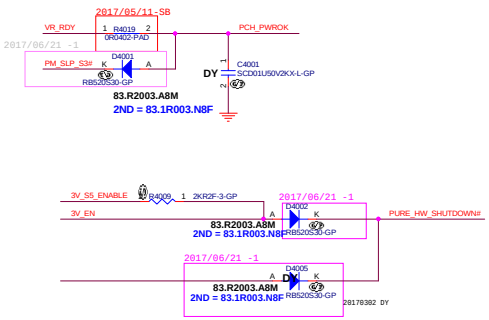
Power Sequence

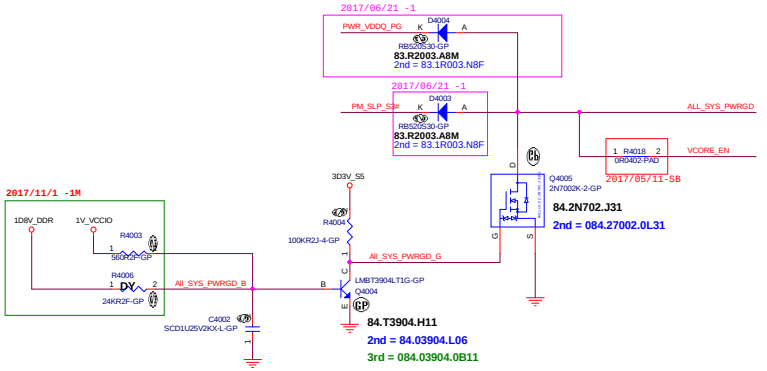
26,46 VR_RDY
20 PCH_PWROK
20,24 PM_SLP_S0#
20,24,40,45,53 PM_SLP_S3#
24 3V_S5_ENABLE
45 3V_EN
24,45 5V_EN
24,26 PURE_HW_SHUTDOWN#
20,24 ALL_SYS_PWRGD
46 VCORE_EN
51 PWR_VDDQ_PG

Run Power

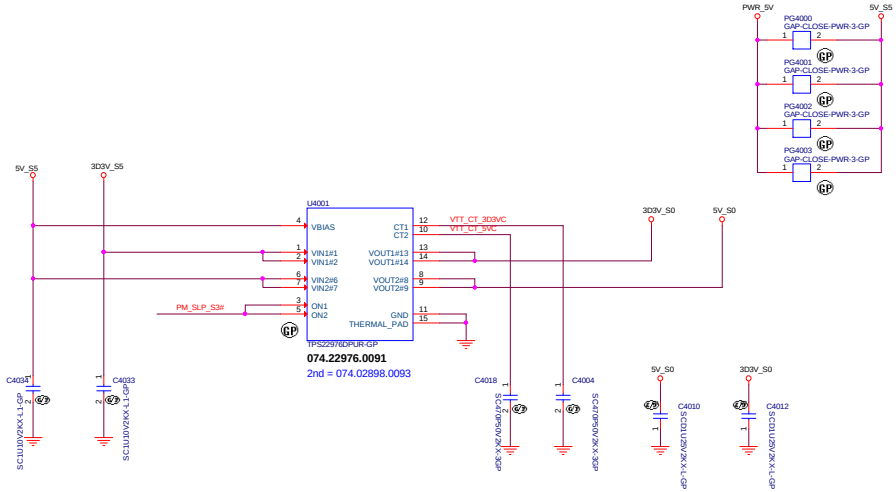
20,24,51 PM_SLP_S4#
20,24,40,45,53 PM_SLP_S3#
24 VCCSTG_EN_EC

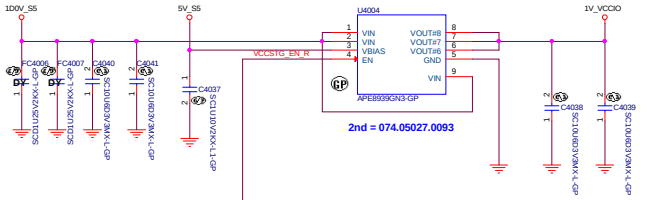
Power Sequence

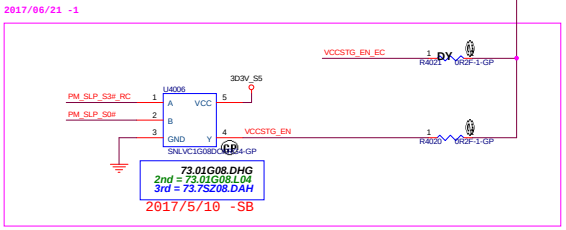


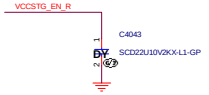


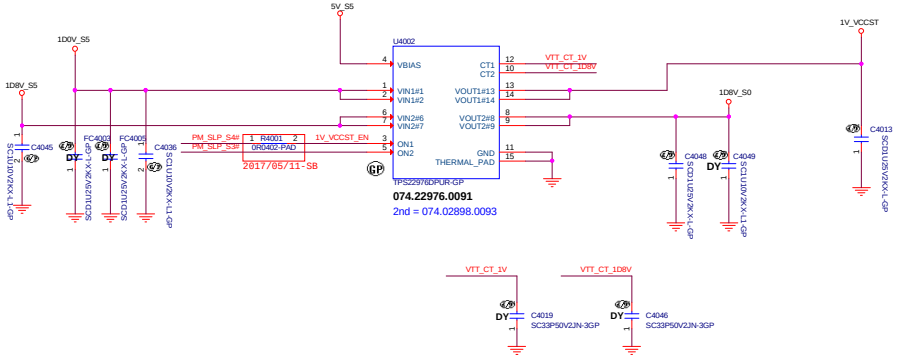
ANNIE Run Power

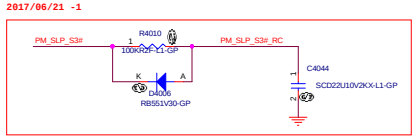












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Title: Power Plane Enable & SEQUENCE

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Date: Wednesday, November 01, 2017 | Sheet 40 of 106

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Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 41 of 106

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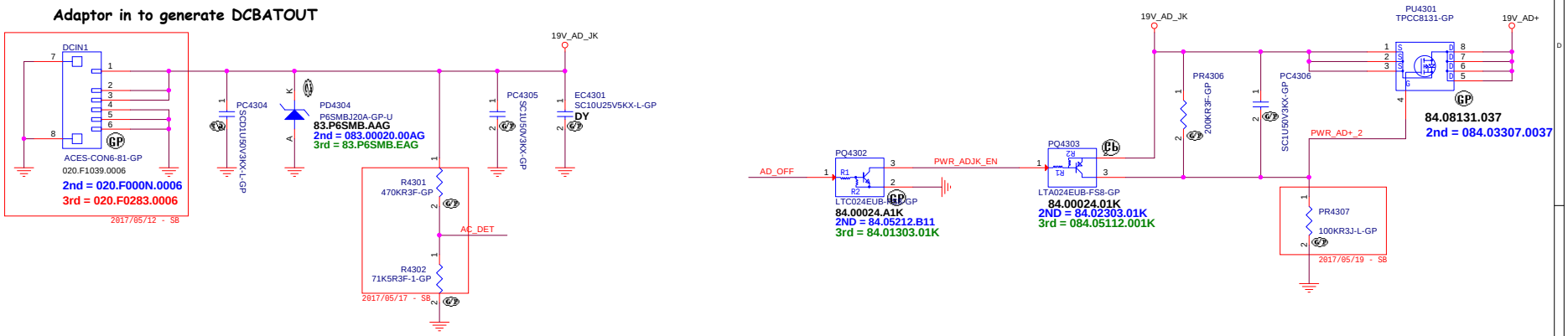
Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 42 of 106

DC IN



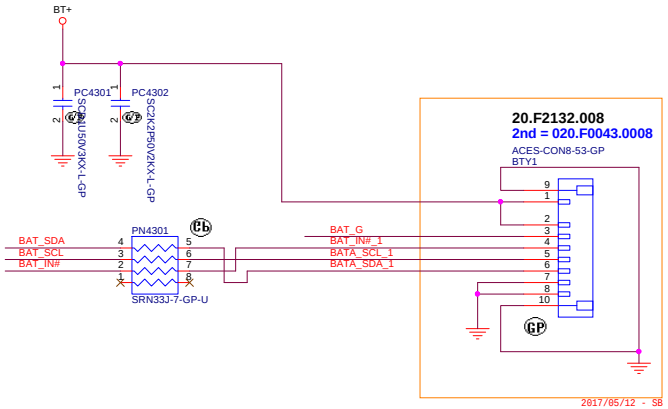
24,44 BAT_IN#
24,44 BAT_SCL
24,44 BAT_SDA
24 AD_OFF
74 AC_DET
24,65,89 KBC_PWRBTN#

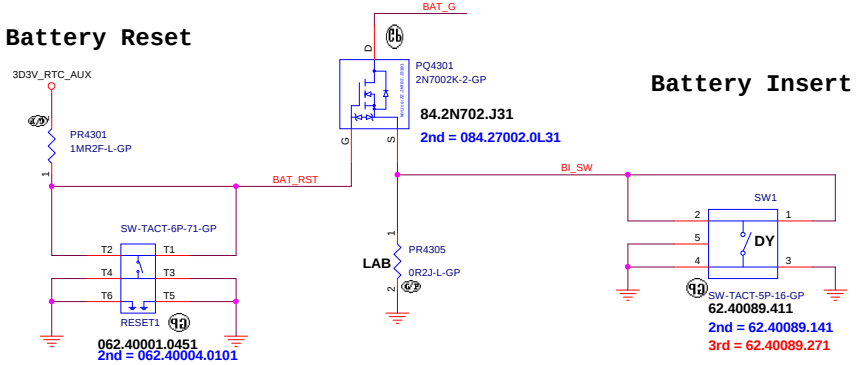
AFTP

89 BAT_G
89 BAT_IN#_1
89 BATA_SCL_1
89 BATA_SDA_1

Power Button

BATTERY CONNECTOR





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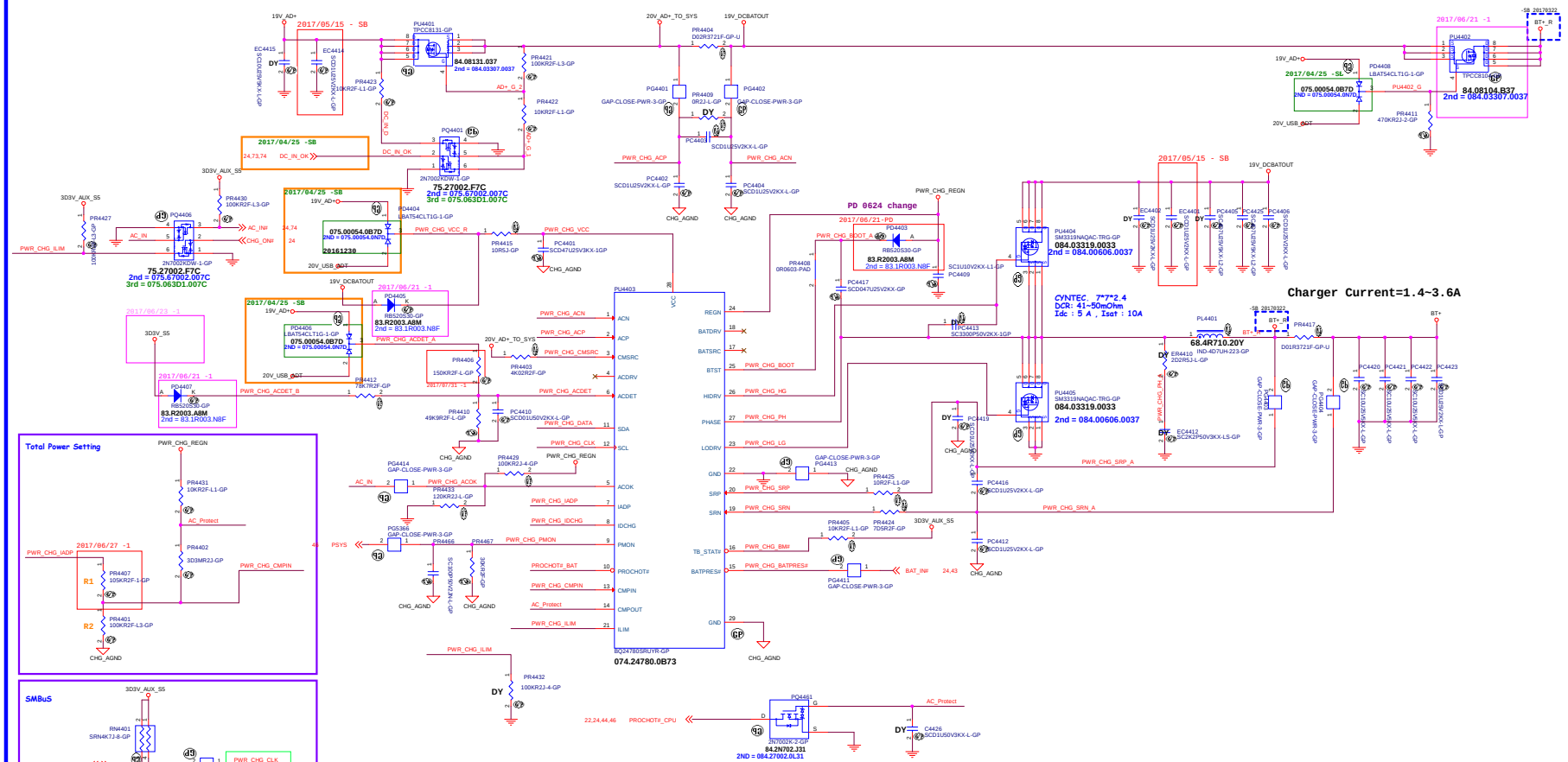
Title	***BATT CONN***	
Size: Custom	Document Number: **Carlsberg_KL**	Rev: **-1M**
Date: Wednesday, November 01, 2017	Sheet 43 of 106	

SSID = Charger



Adapter	AC Protect	PR4407
45W	110%	73.2K
45W	130%	105K
65W	110%	150K
65W	130%	196K

45 Watt AC Protect 110% ▸ PR4407 change 73.2K ohm.(64.73225.6DL)
65 Watt AC Protect 110% ▸ PR4407 change 150K ohm.(64.15035.6DL)

IDCHG : Discharge detect current :
= 8 or 16 x (Vsrn - Vsrp)

IADP : AC adapter detect current :
= 20 or 40 x (Vacp - Vacn) / 10mohm

PMON : Total system power

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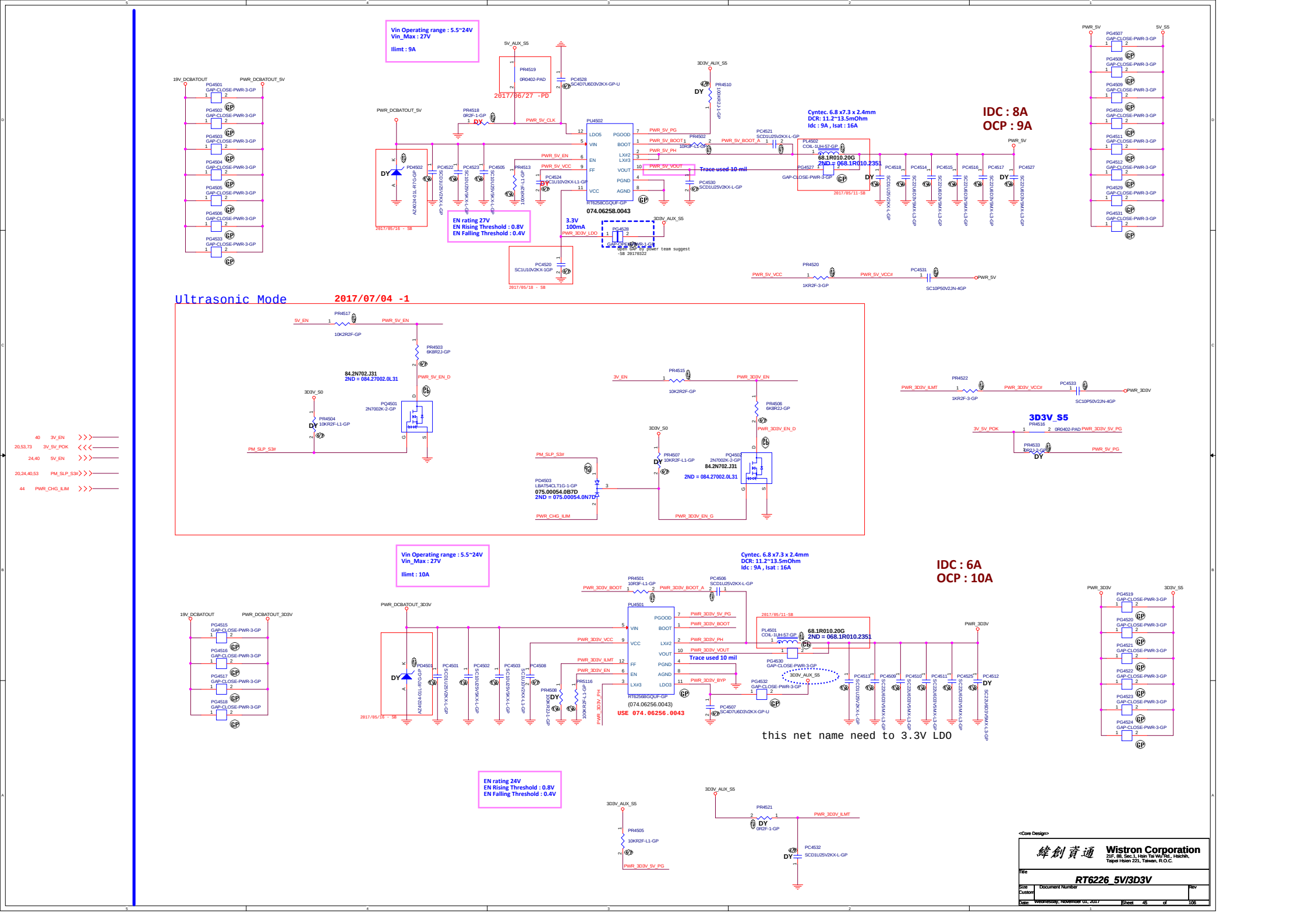
Title: CHARGER HPA02224
Size: Custom | Document Number: Carlsberg_KL | Rev: -1M
Date: Wednesday, November 01, 2017 | Sheet 44 of 106


Vin Operating range : 5.5~24V
Vin_Max : 27V
Ilimt : 9A
RT6258CGQUF-GP
074.06258.0043
EN rating 27V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
3.3V
100mA
Cyntec. 6.8 x7.3 x 2.4mm
DCR: 11.2~13.5mOhm
Idc : 9A , Isat : 16A
68.1R010.20G
2ND = 068.1R010.2351
IDC : 8A
OCP : 9A
Trace used 10 mil
Ultrasonic Mode
2017/07/04 -1
Vin Operating range : 5.5~24V
Vin_Max : 27V
Ilimt : 10A
IDC : 6A
OCP : 10A
RT6256BGQUF-GP
(074.06256.0043)
USE 074.06256.0043
this net name need to 3.3V LDO
EN rating 24V
EN Rising Threshold : 0.8V
EN Falling Threshold : 0.4V
3D3V_S5
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RT6226_5V/3D3V
Wednesday, November 01, 2017
Sheet 45 of 106

Main Func = CPU_CORE

OFFPAGE

22,24,44 PROCHOT#_CPU
7 SVID_ALERT#_CPU
7 SVID_CLK_CPU
7 SVID_DATA_CPU
26,40 VR_RDY
40 VCORE_EN
7 VSSCORE_SENSE
7 VCCCORE_SENSE
8 VCCGT_SENSE
8 VSSGT_SENSE
8 VSSSA_SENSE
8 VCCSA_SENSE
44 PSYS

50 PWR_VCCSA_ISUMP
50 PWR_VCCSA_ISUMN
48 PWR_VCCGT_ISUMP
48 PWR_VCCGT_ISUMN
47 PWR_VCORE_ISUMP_A
47 PWR_VCORE_ISUMN_A
47 PWR_VCORE_ISUMP_B
47 PWR_VCORE_ISUMN_B

50 PWR_VCCSA_PWM
48 PWR_VCCGT_PWM
47 PWR_VCORE_PWMA
46,47 PWR_VCORE_PWMB
46,47 PWR_VCORE_PWMB
47,48,50 PWR_VCORE_FCCM#

PSYS PR4643 2 PWR_VCORE_PSYS 0R0402-PAD-1-GP
VCCSA_SENSE 2 PR4634 1 PWR_VCCSA_FB2 0R0402-PAD-1-GP
VSSSA_SENSE 2 PR4631 1 PWR_VCCSA_RTN 0R0402-PAD-1-GP
VSSGT_SENSE PR4625 PWR_VCCGT_RTN 0R0402-PAD-1-GP
VCCGT_SENSE 1 PR4623 2 PWR_VCCGT_VSEN 0R0402-PAD-1-GP
VCCCORE_SENSE 2 PR4627 1 PWR_VCORE_VSEN 0R0402-PAD-1-GP
VSSCORE_SENSE PR4617 1 PWR_VCORE_RTN 0R0402-PAD-1-GP
VCORE_EN PR4616 2 PWR_VR_EN 0R0402-PAD
VR_RDY 1 PR4612 2 PWR_IMVP_PWRGD 0R0402-PAD-1-GP
SVID_DATA_CPU PR4608 2 VIDSOUT_CPU_R 0R0402-PAD-1-GP
SVID_CLK_CPU 1 PR4607 2 VIDSCK_CPU_R 0R0402-PAD-1-GP
SVID_ALERT#_CPU PR4603 2 PWR_VCORE_ALERT# 0R0402-PAD-1-GP
PROCHOT#_CPU PR4602 2 PWR_CPU_PROCHOT# 0R0402-PAD-1-GP

1V_VCCST
PR4609 DY
PR4610 DY
PR4611 DY
PC4602 SCD1U25V2KX-L-GP
VIDSOUT_CPU_R
PWR_VCORE_ALERT#
VIDSCK_CPU_R

1V_VCCST
PR4619 1KR2F-3-GP DY
PR4601 100R2F-L3-GP
PWR_CPU_PROCHOT#
PWR_VCORE_VRHOT#

PWR_VREF
PR4604 4K42R2F-GP
PR4605 9K53R2F-GP
PR4606 39K7R3F-GP
PR4613 60D4R2F-GP
PR4614 0R0402-PAD-1-GP
PR4615 464R2F-GP
PR4620 4K32R2F-GP
PR4621 9K1R2F-1-GP
PR4622 18K2R2F-L-GP
PR4629 24D9R2F-L-GP
PR4630 143R2F-1-GP
PR4626 130R2F-1-GP
PWR_VCORE_SET1_A
PWR_VCORE_SET2_A
PWR_VCORE_SET3_A
PWR_VCORE_SET1_B
PWR_VCORE_SET2_B
PWR_VCORE_SET3_B

1V_CPU_CORE DY
PR4633 2 PWR_VCORE_VSEN 1 PWR_VCORE_RTN SRN100F-1-GP

1V_VCCGT DY
PR4637 4 PWR_VCCGT_VSEN 3 PWR_VCCGT_RTN SRN100F-1-GP

1V_VCCSA DY
PR4644 2 PWR_VCCSA_FB2 1 PWR_VCCSA_RTN SRN100F-1-GP

PWR_VREF
PR4624 27KR2F-L-GP
19V_DCBATOUT
PR4628 2D2R3F-L-GP
PC4606 SCD22U25V2KX-GP
PC4608 SC1K50V2JN-2GP DY
2017687/31 -1m

5V_S5
PR4618 8D2R3F-GP
PC4603 SC4D7U6D3V3KX-L-GP

PWR_VREF
PR4635 42K2R2F-GP
PC4610 SC1KP50V2JN-2GP DY
3D3V_S0
PR4636 10KR2F-L1-GP
PR4638 49D9R2F-L1-GP
PR4639 10R2F-L1-GP
PC4604 SCD47U25V3KX-1GP
PR4632 3D9R2F-GP
PWR_VREF_A

PWR_VREF
PR4640 31K6R2F-GP
PR4641 2K94R2F-GP
PC4612 SC1K50V2JN-2GP DY
PR4678 NTC-100K-12-GP-U B = 4250
PR4642 48D7KR2F-GP
PWR_VCORE_IMON_A
PWR_VCORE_IMON_B

PR4645 0R0402-PAD-1-GP
PR4648 10KR2F-L1-GP
PR4649 0R0402-PAD-1-GP
PR4650 2BK7R2F-GP
PR4651 0R0402-PAD-1-GP
PC4616 SC220P50V2KX-3GP
PC4617 SC68P50V2JN-1GP
PC4618 SC1KP50V2JN-2GP DY
PR4653 0R2F-1-GP DY
PWR_VCCGT_FB_A

PR4657 10KR2F-L1-GP
PR4658 0R0402-PAD-1-GP
PR4659 52K3R2F-L-GP
PR4660 0R0402-PAD-1-GP
PC4621 SC1KP50V2JN-2GP DY
PC4619 SC220P50V2KX-3GP
PC4620 SC68P50V2JN-1GP
PR4663 0R2F-1-GP DY
PWR_VCORE_FB_A

PR4666 10KR2F-L1-GP
PR4667 0R0402-PAD-1-GP
PR4668 91KR2F-GP -1m
PR4669 0R0402-PAD-1-GP
PC4622 SC330P50V2KX-3GP
PC4623 SC68P50V2JN-1GP
PC4624 SC1KP50V2JN-2GP DY
PR4673 0R2F-1-GP DY
PWR_VCCSA_FB2
PWR_VCCSA_FB_A

PU4601 RT3602AEGQW-GP 074.03602.0073

Pin	Net
46	PSYS
13	VCC
2	SET1
5	SET2
6	SET3
12	VIN
42	VREF
30	IMON_AUXI
1	IMON_MAIN
39	IMON_SA
38	VR_READY
31	VR_HOT#
34	VCLK
32	VDIO
33	ALERT#
37	EN
27	VSEN_AUXI
26	COMP_AUXI
24	FB_AUXI
25	RGND_AUXI
18	DRVEN_SET
4	COMP_MAIN
3	FB_MAIN
48	RGND_MAIN
47	VSEN_MAIN
43	COMP_SA
45	FB_SA
44	RGND_SA
14,15,19,20,21	NC#14,NC#15,NC#19,NC#20,NC#21
49	GND
36	PWM_SA
40	ISENP_SA
41	ISENN_SA
22	PWM_AUXI
29	ISENP_AUXI
28	ISENN_AUXI
16	PWM1_MAIN
10	ISEN1P_MAIN
7	ISEN1N_MAIN
17	PWM2_MAIN
9	ISEN2P_MAIN
8	ISEN2N_MAIN
35	DRVEN
23	TSEN_AUXI
11	TSEN_MAIN

PWR_VCORE_PSYS
PWR_VCORE_VCC
PWR_VCORE_SET1
PWR_VCORE_SET2
PWR_VCORE_SET3
PWR_VCORE_VIN
PWR_VREF
PWR_VCCGT_IMON
PWR_VCORE_IMON
PWR_VCCSA_IMON
PWR_IMVP_PWRGD
PWR_VCORE_VRHOT#
PWR_VCORE_SCLK
PWR_VCORE_SDIO
PWR_VCORE_ALERT#
PWR_VR_EN
PWR_VCCGT_VSEN
PWR_VCCGT_COMP
PWR_VCCGT_FB
PWR_VCCGT_RTN
PWR_VCORE_DRVEN_SET
PWR_VCORE_COMP
PWR_VCORE_FB
PWR_VCORE_RTN
PWR_VCORE_VSEN
PWR_VCCSA_COMP
PWR_VCCSA_FB
PWR_VCCSA_RTN

PWR_VCCSA_PWM
PWR_VCCSA_ISUMP
PWR_VCCSA_ISUMN
PWR_VCCGT_PWM
PWR_VCCGT_ISUMP
PWR_VCCGT_ISUMN
PWR_VCORE_PWMA
PWR_VCORE_ISUMP_A
PWR_VCORE_ISEN1N_A
PWR_VCORE_ISUMN_A
PWR_VCORE_PWMB
PWR_VCORE_ISUMP_B
PWR_VCORE_ISEN2N_B
PWR_VCORE_ISUMN_B
PWR_VCORE_FCCM#
PWR_VCCGT_TSEN
PWR_VCORE_TSEN

PC4601 SC1KP50V2JN-2GP DY
PC4605 SCD1U25V2KX-L-GP 28178112
PC4607 SC1KP50V2JN-2GP DY
PC4609 SCD1U25V2KX-L-GP
PC4611 SC1KP50V2JN-2GP DY
PR4683 1R2F-GP
PC4613 SCD1U25V2KX-L-GP 28178112
PR4682 0R2F-1-GP
PR4684 0R2F-1-GP
PR4652 2R2F-1-GP
PC4615 SCD1U25V2KX-L-GP 28178112
Jason 0104
U42
U22

	PR4652	PR4682
U22	0	0
U42	DY	DY

	PR4684
U22	DY
U42	1R

PR4676 NTC-100K-12-GP-U B = 4250
PR4664 110KR2F-L-GP
PR4681 NTC-100K-12-GP-U B = 4250
PR4677 110KR2F-L-GP

PR4654 8K45R2F-2-GP
PR4655 8K45R2F-2-GP
PR4661 191R2F-GP
PR4662 187R2F-GP
PR4670 180KR2F-4-L-GP
PR4671 178KR2F-GP
PR4674 357R2F-GP
PR4675 715R2F-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_VCORE(1/3)
Size: Custom
Document Number: Carlsberg_KL
Rev: -1M
Date: Wednesday, November 01, 2017
Sheet 46 of 106

Main Func = CPU_CORE

46 PWR_VCORE_ISUMP_A
46 PWR_VCORE_ISUMN_A
46 PWR_VCORE_PWMA
46,48,50 PWR_VCORE_FCCM#
46 PWR_VCORE_ISUMP_B
46 PWR_VCORE_ISUMN_B
46 PWR_VCORE_PWMB

19V_DCBATOUT PWR_DCBATOUT_VCOREA
PG4702 PG4703 PG4704 PG4705 PG4706 PG4707 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCOREA
PC4702 PC4703 PC4704 PC4705 SC10U25V5KX-GP

PU4702 AOZ5049QI-1-GP
PWR_VCORE_BOOTA PWR_VCORE_PHASEDA PWR_VCORE_SWA PWR_VCORE_PWM_RA PWR_VCORE_FCCMRA PWR_VCORE_PWMA PWR_VCORE_FCCMA
5V_S5 PR4702 2D2R2F-GP PC4706 SC1U10V2KX-L1-GP
PC4707 SCD22U25V3KX-GP PR4703 2D2R3-1-U-GP PR4704 0R0402-PAD-1-GP PR4705 0R0402-PAD-1-GP
074.05049.0A73

SKL_U42
Icc(max)=64A
TDC=42A
Confirm with EE
22uF/0805 total 32pcs
(78.22610.L2L)

Cyntec, 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A
2017/05/11-SB
PL4702 COIL-D15UH-8-GP
068.R1510.2091
2ND = 068.R1510.2111
PG4706 PG4707 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISEN1P_GA

1V_CPU_CORE
2017/05/12-SB
PT4702 SE330U2VDM-4-GP 79.33719.20C
2ND = 077.53371.0081
PANASONIC
ESR: 9 mohm

PR4708 360R2F-GP PC4708 SCD47U25V3KX-1GP PR4709 10KR2F-L1-GP
PWR_VCORE_ISUMP_A
PWR_VCORE_ISUMN_A
CLOSE to IC

PWR_VCORE_SWA PR4707 2D2R6J-3-GP PWR_VCORE_SNB PC4709 SC1KP50V2KX-L-1-GP

19V_DCBATOUT PWR_DCBATOUT_VCOREB
PG4708 PG4709 PG4710 PG4711 PG4712 PG4713 GAP-CLOSE-PWR-3-GP

PWR_DCBATOUT_VCOREB
PC4701 PC4711 PC4712 PC4710 U42 SC10U25V5KX-L-GP

PU4701 U42 AOZ5049QI-1-GP
PWR_VCORE_BOOTB PWR_VCORE_PHASEDB PWR_VCORE_SWB PWR_VCORE_PWM_RB PWR_VCORE_FCCMRB PWR_VCORE_PWMB PWR_VCORE_FCCMB
5V_S5 PR4710 2D2R2F-GP PC4713 SC1U10V2KX-L1-GP
PC4714 SCD22U25V3KX-GP PR4711 2D2R3-1-U-GP PR4701 0R0402-PAD-1-GP PR4712 0R0402-PAD-1-GP
074.05049.0A73

SKL_U42
Icc(max)=64A
TDC=42A
Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)

Cyntec, 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A
2017/05/11-SB
PL4701 COIL-D15UH-8-GP
068.R1510.2091
2ND = 068.R1510.2111
PG4713 PG4714 GAP-CLOSE-PWR-3-GP
PWR_VCORE_ISEN2P_GA

1V_CPU_CORE
2017/05/12-SB
PT4702 SE330U2VDM-4-GP 79.33719.20C
2ND = 077.53371.0081
PANASONIC
ESR: 9 mohm

PR4715 360R2F-GP PC4715 SCD47U25V3KX-1GP PR4716 10KR2F-L1-GP
PWR_VCORE_ISUMP_B
PWR_VCORE_ISUMN_B
CLOSE to IC

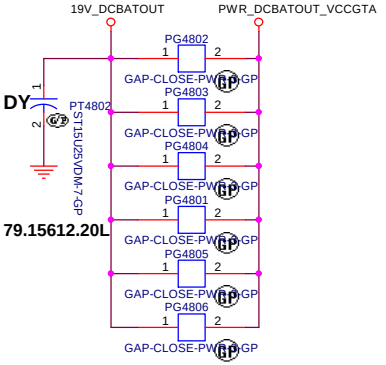
PWR_VCORE_SWB PR4714 2D2R6J-3-GP PWR_VCORE_SNB_B PC4716 SC1KP50V2KX-L-1-GP

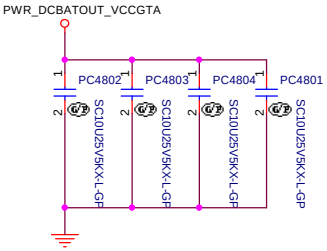
<Core Design>

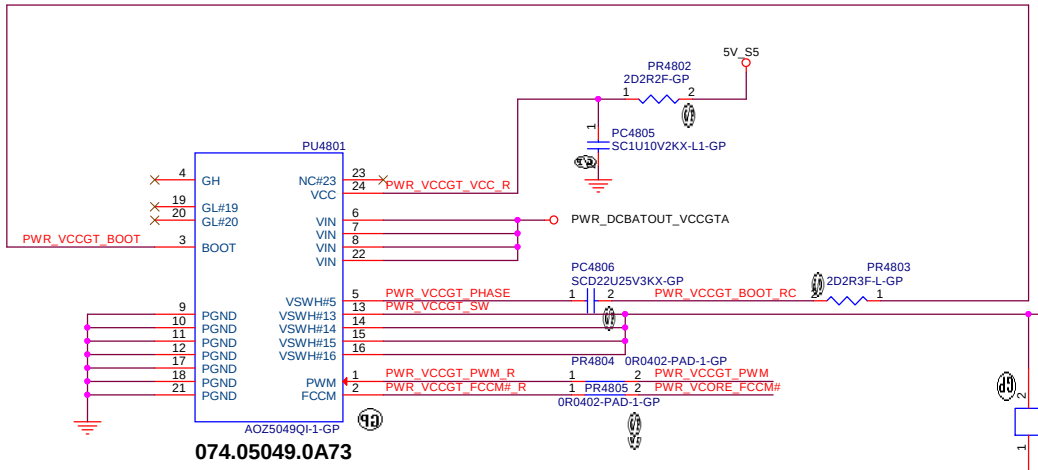
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_VCORE(2/3)	
Size: Custom	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 02, 2017	Sheet 47 of 106	

Main Func = CPU_CORE

46 PWR_VCCGT_ISUMP
46 PWR_VCCGT_ISUMN
46 PWR_VCCGT_PWM
46,47,50 PWR_VCORE_FCCM#



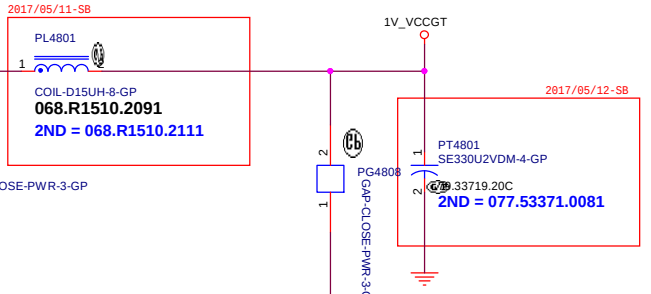


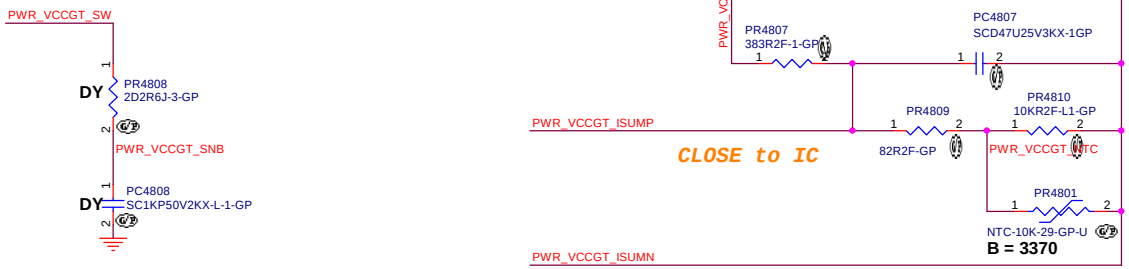


SKL_U42
Icc(max)=28A
TDC=12A

Confirm with EE
22uF/0805 total 26pcs
(78.22610.L2L)

Cyntec. 6.8mm x7.6mmx2.4mm
DCR: 0.9m Ohm+/-7%
Idc : 32A , Isat : 41A





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_VCCGT(3/3)	
Size A3	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 48 of 106	

Blanking

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 49 of 106

Main Func = CPU_CORE

46,47,48 PWR_VCORE_FCCM#
46 PWR_VCCSA_PWM
46 PWR_VCCSA_ISUMP
46 PWR_VCCSA_ISUMN

19V_DCBATOUT
PWR_DCBATOUT_VCCSA
PG5002 GAP-CLOSE-PWR-3-GP
PG5003 GAP-CLOSE-PWR-3-GP

SKL_U42/U22/U23e
Icc(max)=5.1A
TDC=5A

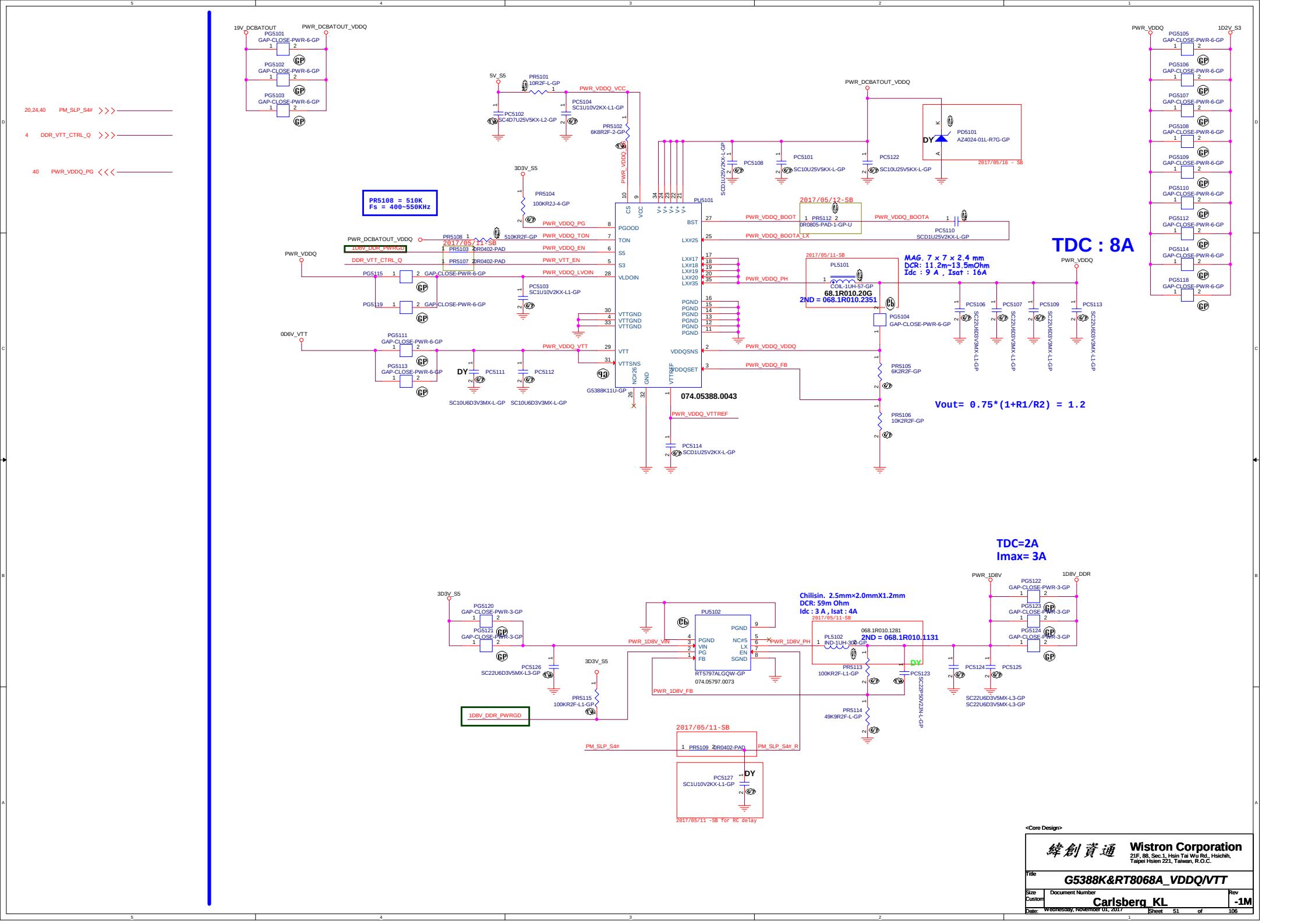
Confirm with EE
22uF/0805 total 5pcs
(78.22610.L2L)

5V_S5
5V_S0
2017/05/11-SB
PR5003 0R0402-PAD
PR5002 0R2J-2-GP
DY
VCCSA_POWER
PC5001 SC2D2U10V3KX-L-GP
PR5001 2D2R3F-L-GP
PWR_VCCSA_BST
PWR_VCCSA_BST_RC
PC5005 SCD22U25V3KX-GP
PU5004
VCC BOOT
EN UGATE
PWM PHASE
GND LGATE
GND
RT9610BZQW-GP
74.09610.0E3
PWR_VCORE_FCCM#
PWR_VCCSA_FCCM#
PR5010 0R0402-PAD
PWR_VCCSA_PWM
PWR_VCCSA_PWM_A
PR5011 0R0402-PAD
2017/06/27 -PD
PR5008 100KR2F-L3-GP
PWR_VCCSA_DRVH
PWR_VCCSA_SW
PWR_VCCSA_DRVL
PR5009 2D2R6J-3-GP
PWR_VCCSA_SNB
PC5007 SC1KP50V2KX-L-1-GP
PU5001 SM3319NAQAC-TRG-GP
084.03319.0033
2nd = 084.00606.0037
PU5003 SM3319NAQAC-TRG-GP
084.03319.0033
2nd = 084.00606.0037
PC5002 SC10U25V5KX-L-GP
PC5003 SC10U25V5KX-L-GP
PC5004 SCD1U25V2KX-L-GP
MAG. 7 x 7 x 2.4 mm
DCR: 4.5m~5.1 mOhm
Idc : 15 A , Isat : 22A
2017/05/11-SB
PL5001 COIL-D47UH-20-GP
068.R4710.2011
2ND = 068.R4710.2201
1V_VCCSA
TC5001 SE330U2VDM-4-GP
DY
PG5011 GAP-CLOSE-PWR-3-GP
PG5001 GAP-CLOSE-PWR-3-GP
PWR_VCCSA_ISEN1P_GB
PR5005 324R2F-GP
PC5006 SCD47U25V3KX-1GP
PR5007 1R2F-L-GP
PR5006 3KR2F-GP
PWR_VCCSA_ISUMP
PWR_VCCSA_ISEN1P_GB
CLOSE to IC
PR5004 NTC-10K-29-GP-U
B = 3370
PWR_VCCSA_ISUMN

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VCCSA	
Size: Custom	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 50 of 106	



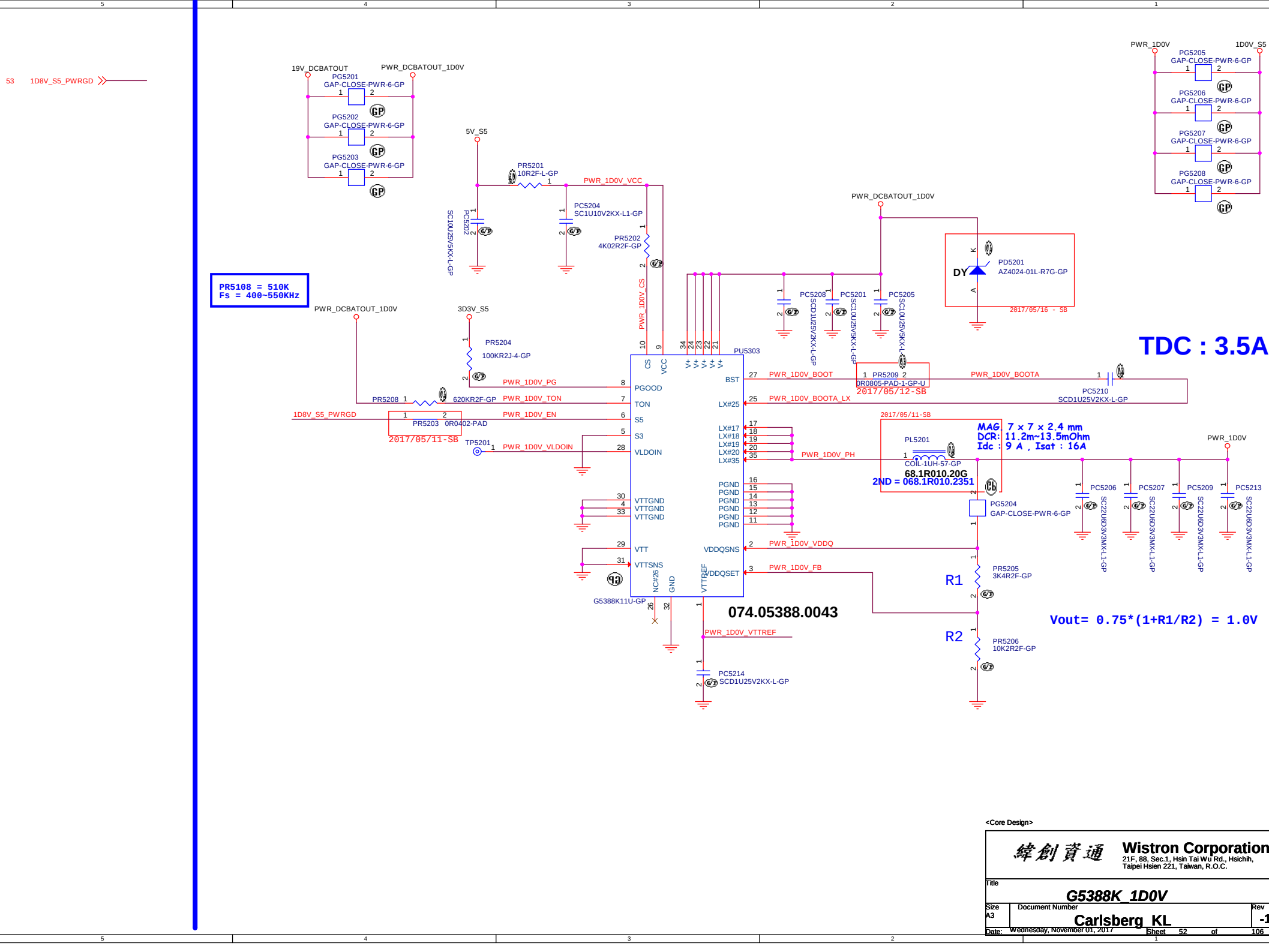
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: G5388K&RT8068A_VDDQ/VTT

Size	Document Number	Rev
Custom	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 51 of 106



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: G5388K_1D0V

Size: A3 | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 52 of 106

20,24,40,45 PM_SLP_S3#

52 1D8V_S5_PWRGD

20,45,73 3V_5V_POK

20160608 -1M

1D8V_S5

PD = (Vin_Vout) x Iout
= (3.3 - 1.8) x 0.3A = 0.45W
PD de-rating(%) = 0.45W/1.33W = 33.8%

1125 Simon
Vendor suggest to replace 74.09025.A3D by 74.09025.D3D

3D3V_S5
PG5301 GAP-CLOSE-PWR-6-GP
PG5302 GAP-CLOSE-PWR-6-GP
5V_S5
PR5302 2D2R2F-GP
PC5302 SC1U10V2KX-L1-GP
PC5303 SC10U6D3V3MX-L-GP
DY
PC5304 SC10U6D3V3MX-L-GP

PU5301
PWR_1D8V_S5_PWRGD
PWR_1D8V_S5_EN
PWR_1D8V_S5_PVDD
PWR_1D8V_S5_VDD
POK VEN VIN VPP GND GND ADJ VO NC#5
PWR_1D8V_S5_FB
G9661-25ADJF11U-GP-U
74.09661.07D

PWR_S5_1D8V
PG5303 GAP-CLOSE-PWR-6-GP
PG5304 GAP-CLOSE-PWR-6-GP
1D8V_S5

PC5306 SC10U6D3V3MX-L-GP
DY
PC5301 SC10U6D3V3MX-L-GP

R1
PR5303 12K7R2F-GP
PC5305 SC22P50V2JN-L-GP
PWR_1D8V_S5_FB
R2
PR5304 10KR2F-L1-GP

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

3V_5V_POK
PR5301 0R0402-PAD
PWR_1D8V_S5_EN
2017/05/11-SB
PC5307 SC1U10V2KX-L1-GP
DY

3D3V_S5
PR5305 10KR2F-L1-GP
PR5312 0R0402-PAD-1-GP
PWR_1D8V_S5_PWRGD
1D8V_S5_PWRGD

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

Iomax=120mA

3D3V_S5
PC5309 SC1U10V2KX-L1-GP
PU5302
VIN VSS ON/OFF VOUT NC#4
S-1339D15-M5001-GP
74.01339.B3F
2nd = 074.09078.0A3F
1D5V_S0
PC5308 SC1U10V2KX-L1-GP

2017/05/11-SB
PM_SLP_S3#
PR5315 0R0402-PAD
PWR_1D5V_S0_EN
1D5V_PWR_EN
PC5310 SC22P50V2JN-L-GP
DY
PR5314 100KR2J-L-GP

Fix Vout=1D5V
Imax=300mA
OCP = 400mA

<Core Design>

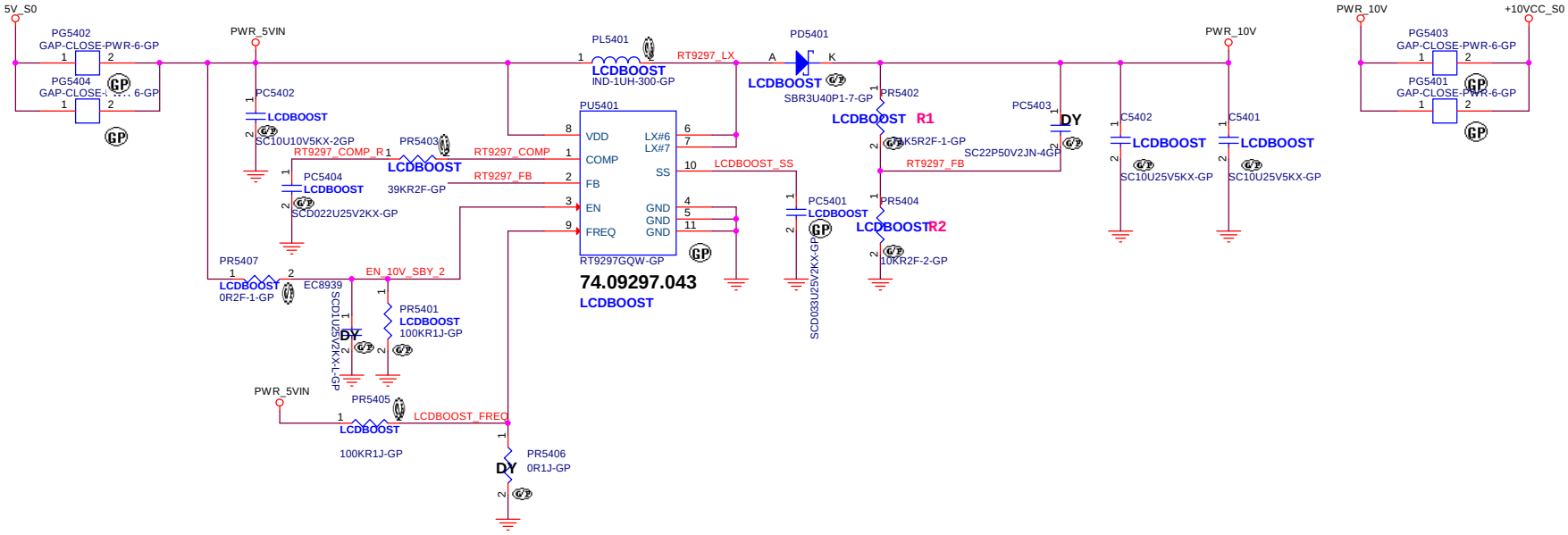
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8068_1D8V
Size: Custom
Document Number: Carlsberg_KL
Rev: -1M
Date: Wednesday, November 01, 2017
Sheet 53 of 106

2017/05/12 - SB new add

Cyntec 1.0uH 2520 Size
Idc=3.0A, Isat=4.0A

+10VCC , Imax= 1.5A



Control Inputs						
EN, FREQ Input Low Voltage	V_{IL}		--	--	0.3 x V_{DD}	V
EN, FREQ Input High Voltage	V_{IH}		0.7 x V_{DD}	--	--	V
EN, FREQ Input Hysteresis			--	0.1 x V_{DD}	--	V
FREQ Pull-down Current			--	6	--	µA
EN Input Current	I_{EN}	EN = GND	--	0.001	1	µA

<Core Design>

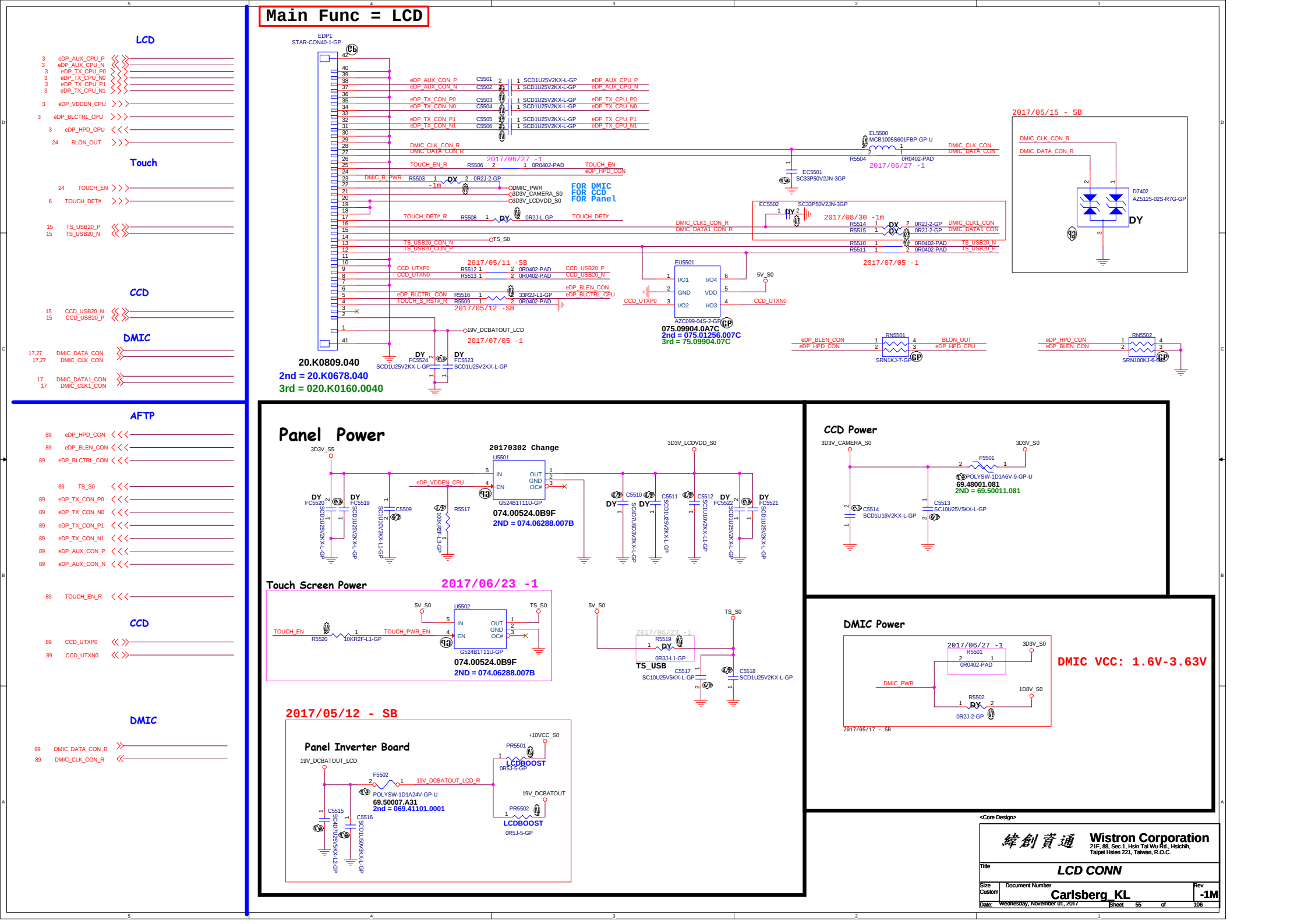
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD Backlight Boost**

Size: A3 | Document Number: **Carlsberg_KL** | Rev: **-1M**

Date: Wednesday, November 01, 2017 | Sheet 54 of 106

Main Func = LCD



<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 55 of 106

Blanking

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

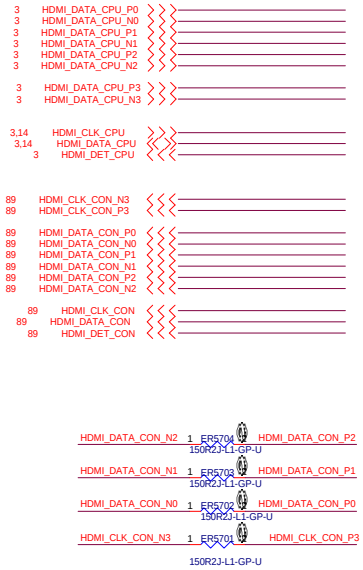
Title: ***Reserved***

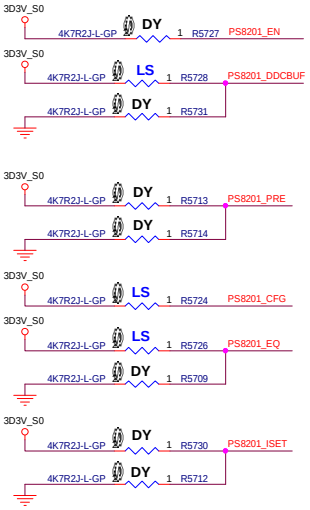
Size	Document Number	Rev
A4	Carlsberg_KL	-1M

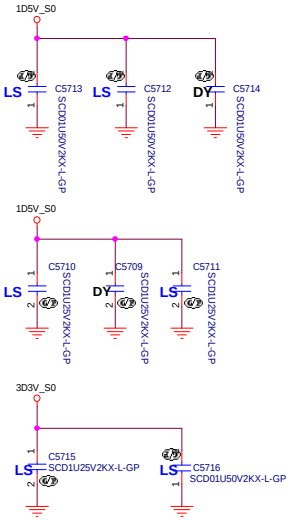
Date: Wednesday, November 01, 2017 Sheet 56 of 106

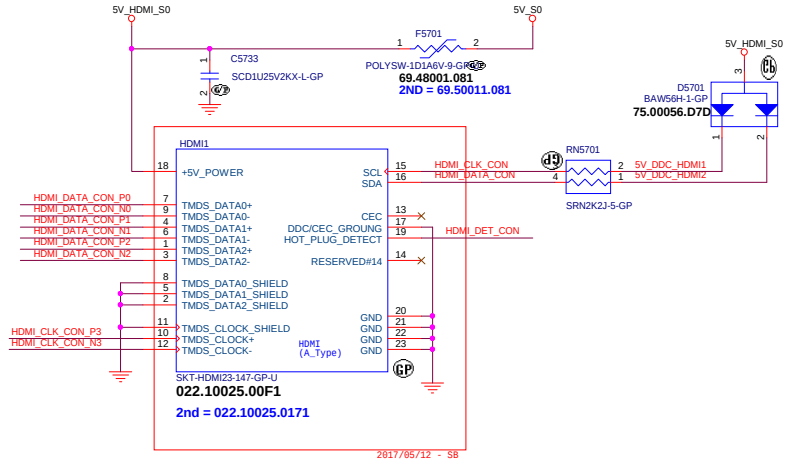
SSID = VIDEO

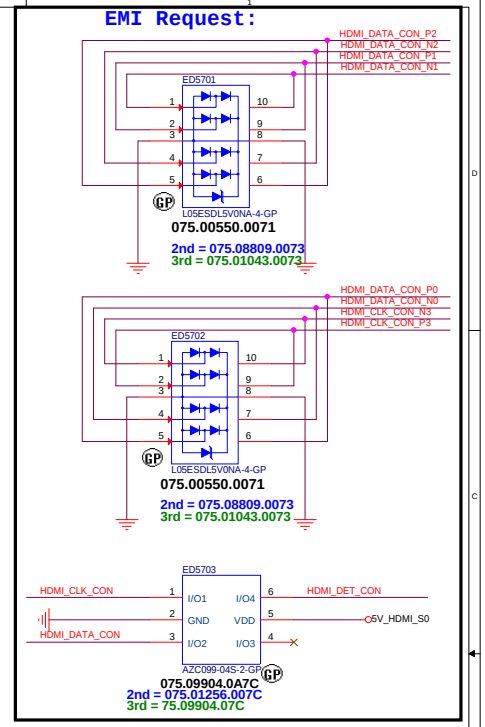
HDMI Level Shifter & CONNECTOR

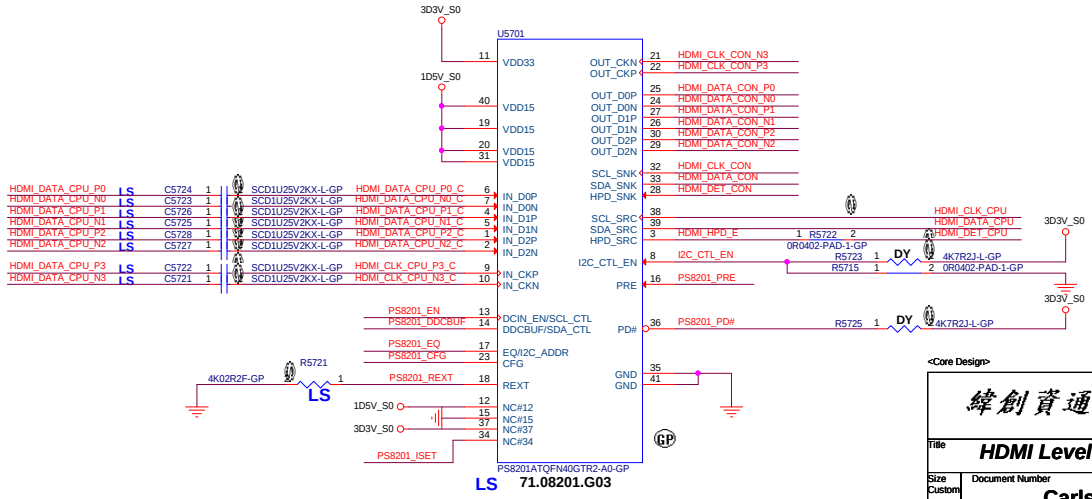












<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 57 of 106

Blanking

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**		
Size: A	Document Number: **Carlsberg_KL**	Rev: **-1M**
Date: Wednesday, November 01, 2017	Sheet 58 of 106	

Blanking

<Core Design>

緯創資通 **Wistron Corporation**
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Title	***DVI(Reserved)***	
Size: A4	Document Number: **Carlsberg_KL**	Rev: **-1M**
Date: Wednesday, November 01, 2017	Sheet 59 of 106	

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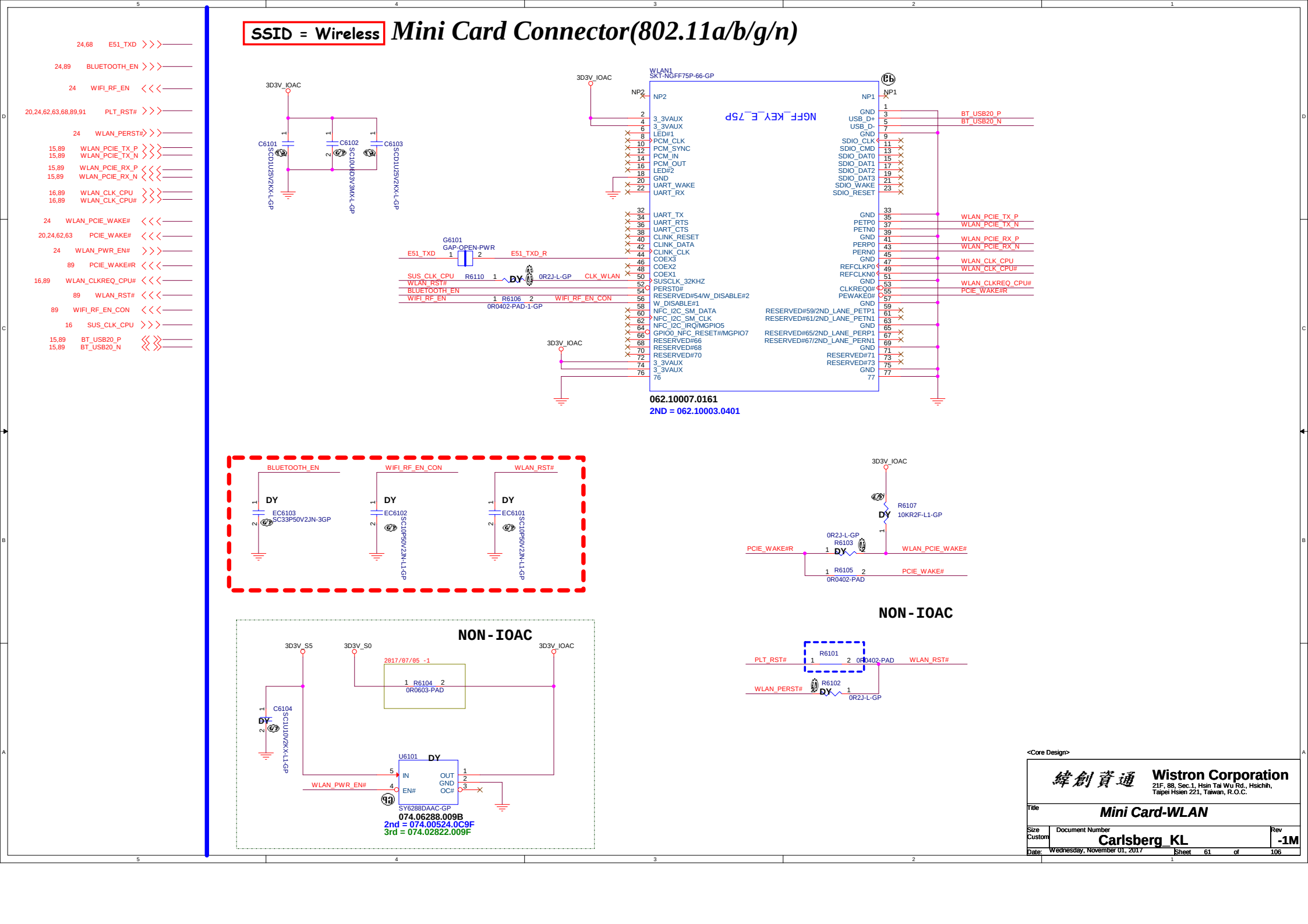
Title: ***HDD_GSENSOR***

Size	Document Number	Rev
Custom	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 60 of 106

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



<Core Design>

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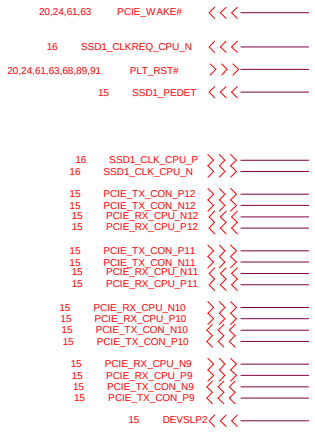
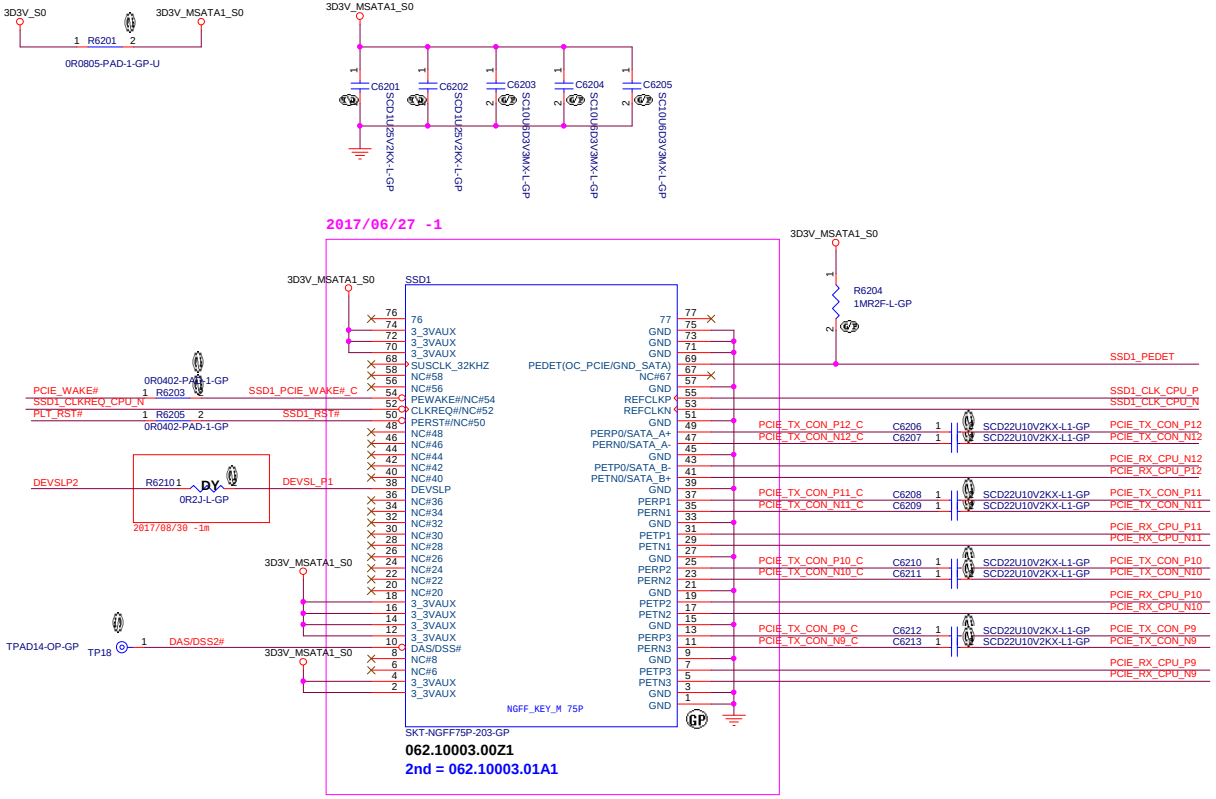
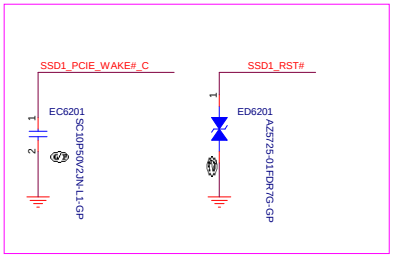
Title	Mini Card-WLAN	
Size: Custom	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 61 of 106	

SSID = mSATA





2017/06/27 -1



Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer t(Chapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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Title: SSD1

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 62 of 106

SSID = mSATA

15 PCIE_RX_CPU_N5
15 PCIE_RX_CPU_P5
15 PCIE_TX_CON_N5
15 PCIE_TX_CON_P5

15 PCIE_RX_CPU_N6
15 PCIE_RX_CPU_P6
15 PCIE_TX_CON_N6
15 PCIE_TX_CON_P6

15 PCIE_RX_CPU_N7
15 PCIE_RX_CPU_P7
15 PCIE_TX_CON_N7
15 PCIE_TX_CON_P7

15 PCIE_RX_CPU_N8
15 PCIE_RX_CPU_P8
15 PCIE_TX_CON_N8
15 PCIE_TX_CON_P8

15 DEVSLP1
15 SSD2_PEDET
20,24,61,62 PCIE_WAKE#

16 SSD2_CLK_CPU_N
16 SSD2_CLK_CPU_P
16 SSD2_CLKREQ_CPU_N

20,24,61,62,68,89,91 PLT_RST#

3D3V_S0 — R6301 0R0805-PAD-1-GP-U — 3D3V_MSATA1_S0

3D3V_MSATA1_S0
C6301 SCD1U25V2KX-L-GP
C6302 SCD1U25V2KX-L-GP
C6303 SC10U6D3V3MX-L-GP
C6304 SC10U6D3V3MX-L-GP
C6305 SC10U6D3V3MX-L-GP

2017/06/27 -1

3D3V_MSATA1_S0 — R6302 1MR2F-L-GP

SSD2

76	76	77	77
74	3_3VAUX	75	GND
72	3_3VAUX	73	GND
70	3_3VAUX	71	GND
68	SUSCLK_32KHZ	69	PEDET(OC_PCIE/GND_SATA)
58	NC#58	67	NC#67
56	NC#56	57	GND
54	PEWAKE#/NC#54	55	REFCLKP
52	CLKREQ#/NC#52	53	REFCLKN
50	PERST#/NC#50	51	GND
48	NC#48	49	PERP0/SATA_A+
46	NC#46	47	PERN0/SATA_A-
44	NC#44	45	GND
42	NC#42	43	PETP0/SATA_B-
40	NC#40	41	PETN0/SATA_B+
38	DEVSLP	39	GND
36	NC#36	37	PERP1
34	NC#34	35	PERN1
32	NC#32	33	GND
30	NC#30	31	PETP1
28	NC#28	29	PETN1
26	NC#26	27	GND
24	NC#24	25	PERP2
22	NC#22	23	PERN2
20	NC#20	21	GND
18	3_3VAUX	19	PETP2
16	3_3VAUX	17	PETN2
14	3_3VAUX	15	GND
12	3_3VAUX	13	PERP3
10	DAS/DSS#	11	PERN3
8	NC#8	9	GND
6	NC#6	7	PETP3
4	3_3VAUX	5	PETN3
2	3_3VAUX	3	GND
		1	GND

NGFF_KEY_M 75P

SKT-NGFF75P-203-GP

062.10003.00Z1
2nd = 062.10003.01A1

PCIE_WAKE# — R6303 0R0402-PAD-1-GP — SSD2_PCIE_WAKE#_C
SSD2_CLKREQ_CPU_N
PLT_RST# — R6304 0R0402-PAD-1-GP — SSD2_RST#
DEVSLP1 — R6305 0R2J-L-GP — DEVSLP_R
2017/08/30 -1m
TP19 TPAD14-OP-GP — DAS/DSS2_2#

SSD2_PEDET
SSD2_CLK_CPU_P
SSD2_CLK_CPU_N

PCIE_TX_CON_P8_C	C6306	SCD22U10V2KX-L1-GP	PCIE_TX_CON_P8
PCIE_TX_CON_N8_C	C6307	SCD22U10V2KX-L1-GP	PCIE_TX_CON_N8
PCIE_TX_CON_P7_C	C6308	SCD22U10V2KX-L1-GP	PCIE_TX_CON_P7
PCIE_TX_CON_N7_C	C6309	SCD22U10V2KX-L1-GP	PCIE_TX_CON_N7
PCIE_TX_CON_P6_C	C6310	SCD22U10V2KX-L1-GP	PCIE_TX_CON_P6
PCIE_TX_CON_N6_C	C6311	SCD22U10V2KX-L1-GP	PCIE_TX_CON_N6
PCIE_TX_CON_P5_C	C6312	SCD22U10V2KX-L1-GP	PCIE_TX_CON_P5
PCIE_TX_CON_N5_C	C6313	SCD22U10V2KX-L1-GP	PCIE_TX_CON_N5

PCIE_RX_CPU_N8
PCIE_RX_CPU_P8
PCIE_RX_CPU_P7
PCIE_RX_CPU_N7
PCIE_RX_CPU_P6
PCIE_RX_CPU_N6
PCIE_RX_CPU_P5
PCIE_RX_CPU_N5

2017/06/27 -1

PCIE_WAKE# — ED6302 AZ5725-01FDR7G-GP
PLT_RST# — ED6301 AZ5725-01FDR7G-GP

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Title: **SSD2**

Size	Document Number	Rev
Custom	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 63 of 106

SSID = User.Interface

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Title: LED Bard/Power Button

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

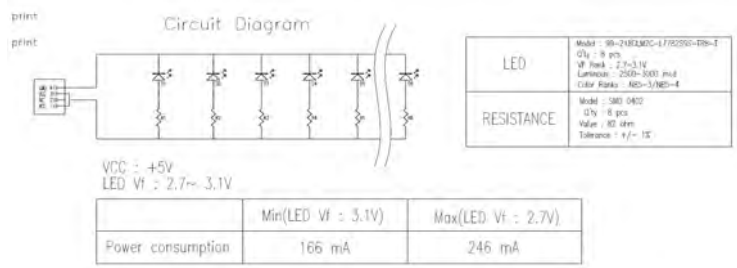
Date: Wednesday, November 01, 2017 | Sheet 64 of 106

SSID = KBC

TOUCH PAD

Internal KeyBoard Connector

20170208 ENG R6521 chage short PAD



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 65 of 106

LED Status

24,89 STDBY_LED
24,89 POWER_LED
24,89 CHARGE_LED
24,89 DC_BATFULL

Audio

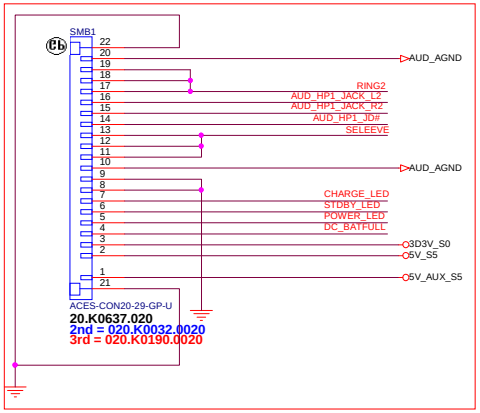
27,66,89 SELEEVE
27,66,89 AUD_HP1_JACK_L2
27,66,89 AUD_HP1_JACK_R2
27,66,89 RING2
27,66,89 AUD_HP1_JD#

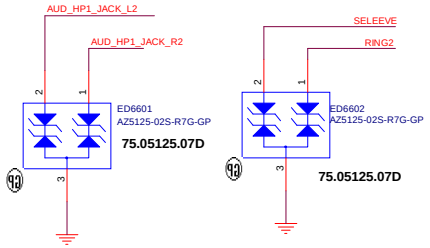
AFTP TESTPOINT

27,66,89 SELEEVE
27,66,89 AUD_HP1_JACK_L2
27,66,89 AUD_HP1_JACK_R2
27,66,89 RING2
27,66,89 AUD_HP1_JD#
89 LID_CLOSE#_1

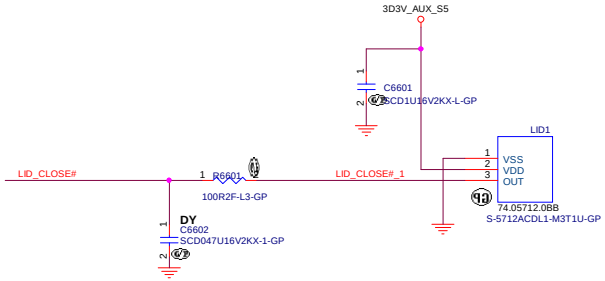
24 LID_CLOSE#

2017/05/03 -SB
2017/05/16 - SB change connector pindefine





HALL SENSOR



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Title	IO Board Connector
Size: Custom	Document Number: Carlsberg_KL
Rev: -1M	
Date: Wednesday, November 01, 2017	Sheet 66 of 106

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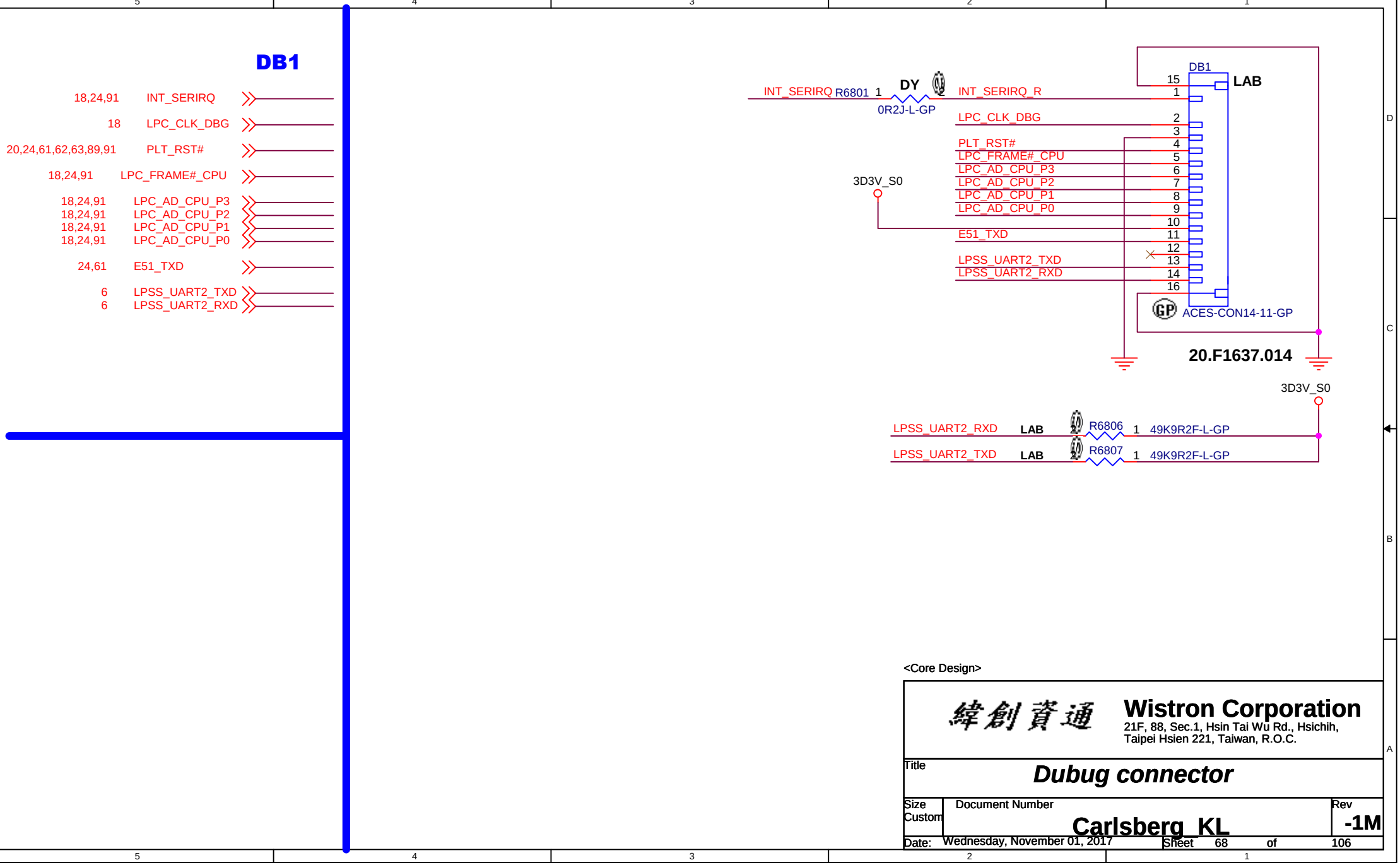
Title: ***Reserved***

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 67 of 106



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Title: ***Dubug connector***

Size	Document Number	Rev
Custom	Carlsberg_KL	-1M
Date: Wednesday, November 01, 2017	Sheet 68 of 106	

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Title	***HDD_G_Sensor***	
Size: Custom	Document Number: **Carlsberg_KL**	Rev: **-1M**
Date: Wednesday, November 01, 2017	Sheet 69 of 106	

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Title
G SENSOR

Size	Document Number	Rev
Custom	**Carlsberg_KL**	**-1M**
Date: Wednesday, November 01, 2017	Sheet 70 of 106	

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Title: ***Reserved***

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 71 of 106

Blanking

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Title: ***Reserved***

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 72 of 106

DDI2 From CPU

- DP_DDI_TX_N0 / DP_DDI_TX_P0
- DP_DDI_TX_N1 / DP_DDI_TX_P1
- DP_DDI_TX_N2 / DP_DDI_TX_P2
- DP_DDI_TX_N3 / DP_DDI_TX_P3
- DP_AUX_CPU_P / DP_AUX_CPU_N
- DP_HPD_CON

USB3 Port 3 From CPU

- USB30_RX_CPU_N3
- USB30_RX_CPU_P3
- USB30_TX_CPU_N3
- USB30_TX_CPU_P3

USB 2.0 From CPU

- TYPEC_USB20_N
- TYPEC_USB20_P

Control Signal

- PD_INT#
- PD_VBUS_C_CTRL1
- NXP3290_EN
- PD_VBUS_P_CTRL1
- NXP3290_FO
- DC_IN_OK
- PD_VBUS_DISCHG
- 3V_5V_POK
- 3V_EN

SMBUS

- SML1_DATA
- SML1_CLK

OTHER

Type-C Controller

Connect 'LOC_PWR' net to local power for F/W to decide if C port can become provider via PR_SWAP. Leave floating if no local power exists in the system or in the application that 544x can only be powered on by local power.

U7301

071.05450.M001

2017/05/22-SB

Type-C Port Protector

2017/06/26 -1

U7302

TPD8S300RUKR-1-GP

075.8S300.0073

From System

2017/05/03 -SB

VBUS to 3.3V

U7303

AP2204K-ADJTRG1-GP

74.02204.03F

Vo=1.24×(1+R1/R2)
=1.24×(1+5.6K/3.16K)
=3.43

ESD FOR USB Interface

Close TYPEC1

ED7301 AZ5125-02S-R7G-GP

75.05125.07D

2nd = 075.05125.007D

EU7302 AZC099-04S-2-GP

075.09904.0A7C

2nd = 075.01256.007C

3rd = 75.09904.07C

U7305 L05ESDL5V0NA-4-GP

075.00550.0071

2nd = 075.08809.0073

3rd = 075.01043.0073

U7306 L05ESDL5V0NA-4-GP

075.00550.0071

2nd = 075.08809.0073

3rd = 075.01043.0073

TYPE C CONNECTOR

TYPEC1

SKT-USB36-14-GP

022.10005.03Y1

2nd = 022.10005.02R1

L7301 FILTER-4P-137-GP-U

68.01012.20B

2nd = 68.00396.001

3rd = 068.24900.2001

Part Balance

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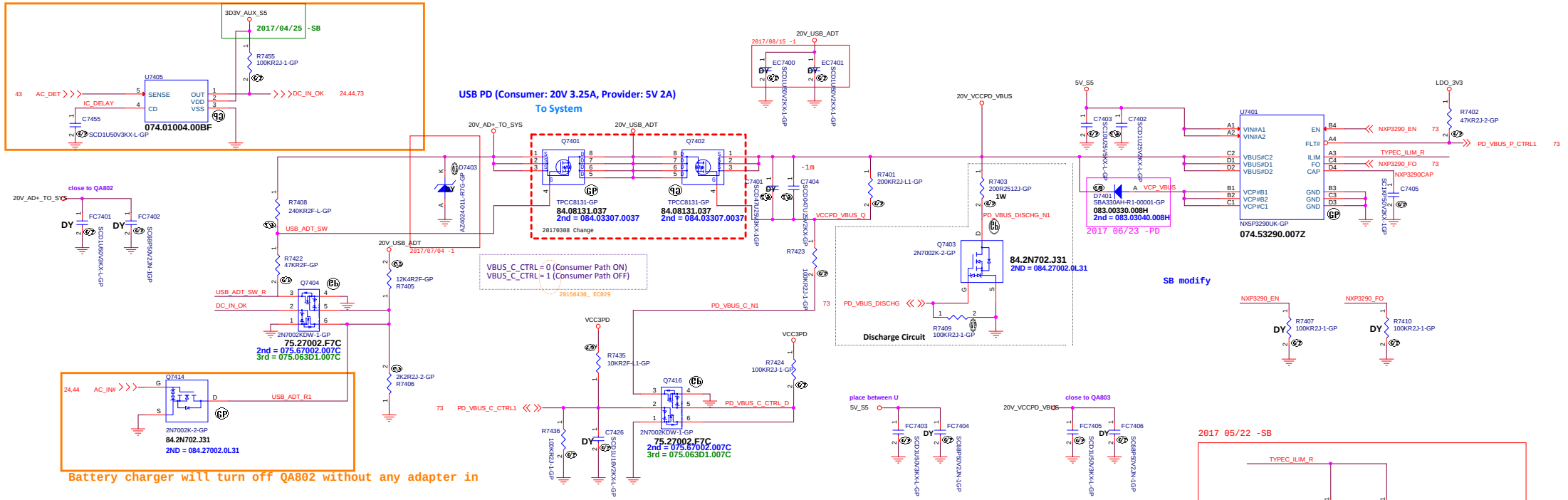
Title: TYPEC_RTS5450

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 73 of 106



19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	
					Q7402	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT

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Title: TYPEC_Control

Size: Custom | Document Number: Carlsberg_KL | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 74 of 106

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Title: ***Reserved***

Size	Document Number	Rev
A4	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 75 of 106

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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU_PEG(Reserved)***	
Size	Project Name **Carlsberg_KL**	Rev *-1M*
Date: Wednesday, November 01, 2017	Sheet 76 of 106	

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<Core Design>

緯創資通 **Wistron Corporation**
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Title	***GPU_DIGITALOUT(Reserved)***	
Size: A4	Document Number: **Carlsberg_KL**	Rev: **-1M**
Date: Wednesday, November 01, 2017	Sheet 77 of 106	

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Title: *Reserved*

Size | Project Name: **Carlsberg_KL** | Rev: -1M

Date: Wednesday, November 01, 2017 | Sheet 78 of 106

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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	***GPU_GPIO/STRAP(Reserved)***	
Size	Project Name **Carlsberg_KL**	Rev *-1M*
Date: Wednesday, November 01, 2017	Sheet 79 of 106	

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_POWER/GND(Reserved)
Size	Project Name: Carlsberg_KL — Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 80 of 106

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Title	***Reserved***	
Size A4	Document Number **Carlsberg_KL**	Rev **-1M**
Date: Wednesday, November 01, 2017	Sheet 81 of 106	

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緯創資通 **Wistron Corporation**
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Title	***GPU-VRAM3,4(Reserved)***	
Size A4	Document Number **Carlsberg_KL**	Rev **-1M**
Date: Wednesday, November 01, 2017	Sheet 82 of 106	

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU-VRAM5,6(Reserved)***	
Size A4	Document Number **Carlsberg_KL**	Rev **-1M**
Date: Wednesday, November 01, 2017	Sheet 83 of 106	

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<Core Design>

緯創資通 **Wistron Corporation**
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Title	***GPU-VRAM7,8(Reserved)***	
Size: A4	Document Number: **Carlsberg_KL**	Rev: **-1M**
Date: Wednesday, November 01, 2017	Sheet 84 of 106	

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<Core Design>

緯創資通 **Wistron Corporation**
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Title	***VGA_CORE(Reserved)***	
Size: A4	Document Number: **Carlsberg_KL**	Rev: **-1M**
Date: Wednesday, November 01, 2017	Sheet 85 of 106	

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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DIS VGA POWER(Reserved)***
Size: A4	Document Number: **Carlsberg_KL**
Rev: **-1M**	
Date: Wednesday, November 01, 2017	Sheet 86 of 106

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GFX_LCD(1/2)(Reserved)***

Size	Document Number	Rev
A4	**Carlsberg_KL**	**-1M**
Date: Wednesday, November 01, 2017	Sheet 87 of 106	

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<Core Design>

緯創資通 **Wistron Corporation**
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Title	*GFX_LCD(2/2)(Reserved)*	
Size A4	Document Number **Carlsberg_KL**	Rev **-1M**
Date: Wednesday, November 01, 2017	Sheet 88 of 106	

DCIN

19V_AD_JK → TP2
19V_AD_JK → AFTP3
AFTP4
AFTP5

Battery

BT+ → TP6
BT+ → AFTP11
AFTP13
AFTP14
43 BAT_G → TP21
43 BAT_INI_1 → TP22
43 BATA_SCL_1 → TP23
43 BATA_SDA_1 → AFTP36

EDP

55 eDP_TX_CON_P0 → TP37
55 eDP_TX_CON_N0 → AFTP38
55 eDP_TX_CON_P1 → TP73
55 eDP_TX_CON_N1 → AFTP74
55 eDP_AUX_CON_P → TP86
55 eDP_AUX_CON_N → AFTP87
55 eDP_BLCTRL_CON → TP89
55 eDP_HPD_CON → TP83
55 eDP_BLEN_CON → TP92
3D3V_CAMERA_S0 → TP93
3D3V_LCDVDD_S0 → TP81
19V_DCBATOUT_LCD → TP15
AFTP17
3D3V_S0 → TP88
55 CCD_UTXP0 → TP69
55 CCD_UTXN0 → TP70
55 DMIC_CLK_CON_R → TP95
55 DMIC_DATA_CON_R → TP110
55 TOUCH_EN_R → AFTP158
55 TS_S0 → AFTP155

Touch PAD

AFTP148
65 EC_TP_CLK_C → TP56
65 EC_TP_DATA_C → TP57
65 I2C1_DATA_TP → TP58
65 I2C1_CLK_TP → TP59
65 TP_INT_R → TP90
3D3V_TP_S3 → TP91
24,65 FUN_OFF# → AFTP85

FAN

AFTP147
24,26 FAN_TACH1 → TP61
5V_S0 → TP41
26 FAN_TACH1_C → AFTP2
24,26 FAN1_PWM → AFTP3

Daughter BD

24,66 POWER_LED → TP151
24,66 STDBY_LED → TP35
3D3V_S0 → TP46
24,66 CHARGE_LED → TP47
24,66 DC_BATFULL → AFTP67
5V_S5 → TP97
AFTP98

20,24,61,62,63,68,91 PLT_RST# → AFTPB6

WLAN

61,89 PCIE_WAKE#R → TP76
15,61 BT_USB20_P → TP77
15,61 BT_USB20_N → AFTP78
61 WLAN_RST# → TP80
16,61 WLAN_CLKREQ_CPU# → TP44
16,61 WLAN_CLK_CPU# → TP45
16,61 WLAN_CLK_CPU → TP46
15,61 WLAN_PCIE_TX_P → TP47
15,61 WLAN_PCIE_TX_N → TP48
15,61 WLAN_PCIE_RX_P → TP49
15,61 WLAN_PCIE_RX_N → TP51
24,61 BLUETOOTH_EN → TP83
61,89 PCIE_WAKE#R → TP84
61 WIFI_RF_EN_CON → TP85
3D3V_IOAC → AFTP84

LOUT

27,66 SELEEVE → TP62
27,66 AUD_HP1_JACK_R2 → TP63
27,66 AUD_HP1_JD# → TP64
27,66 AUD_HP1_JACK_L2 → TP65
27,66 RING2 → AFTP66

FP

FP_5V_S0 → TP141
92 FP_USB20_CON_N → TP142
92 FP_USB20_CON_P → TP140
AFTP143

USB3.0

5V_USB30_CHARGER → TP150
5V_USB30 → TP118
35 USB1_CON_USB20_N → TP119
35 USB1_CON_USB20_P → AFTP120
35 USB2_CON_USB20_N → TP106
35 USB2_CON_USB20_P → TP107
AFTP144

Check test point

3D3V_S0 → TP1
3D3V_AUX_S5 → TP7
3D3V_S5 → TP8
5V_S5 → AFTP9

Top side

KB

KSO0 → TP24
KSO1 → TP26
KSO2 → TP25
KSO3 → TP27
KSO4 → TP28
KSO5 → TP30
KSO6 → TP29
KSO7 → TP32
KSO8 → TP33
KSO9 → TP40
KSO10 → TP39
KSO11 → TP41
KSO12 → TP42
KSO13 → TP44
KSO14 → TP43
KSO15 → TP45
KSO16 → TP156
KSO17 → TP157

KSI0 → TP48
KSI1 → TP50
KSI2 → TP49
KSI3 → TP51
KSI4 → TP53
KSI5 → TP52
KSI6 → TP54
KSI7 → AFTP55
KBC_PWRBTN# → AFTP149
KSI[0..7] 24,65
KSO[0..17] 24,65
AFTP145

HDMI

57 HDMI_CLK_CON_N3 → TP121
57 HDMI_CLK_CON_P3 → AFTP122
57 HDMI_DATA_CON_P0 → TP124
57 HDMI_DATA_CON_N0 → TP123
57 HDMI_DATA_CON_P1 → TP126
57 HDMI_DATA_CON_N1 → TP125
57 HDMI_DATA_CON_P2 → TP128
57 HDMI_DATA_CON_N2 → TP127
57 HDMI_CLK_CON → TP130
57 HDMI_DATA_CON → TP129
57 HDMI_DET_CON → TP132
5V_HDMI_S0 → TP131
AFTP146

Speaker

29 AUD_SPK1_L-_CON → TP16
29 AUD_SPK1_L+_CON → TP18
29 AUD_SPK1_R-_CON → TP19
29 AUD_SPK1_R+_CON → AFTP20

66 LID_CLOSE#_1 → AFTP31

Screw hole

H2 HT85B95X975R29-S-GP — ZZ.00PAD.D71
H3 HT85B95X975R29-S-GP — ZZ.00PAD.D71
H4 HT85B95X975R29-S-GP — ZZ.00PAD.D71
H5 HT85B95X975R29-S-GP — ZZ.00PAD.D71
H6 HOLE256R115-GP — ZZ.00PAD.D11

For CPU Standoff

HS2 STF236R128H22-GP — 434.00X01.0001
HS3 STF236R128H22-GP — 434.00X01.0001
HS4 STF236R128H22-GP — 434.00X01.0001
HS5 STF236R128H22-GP — 434.00X01.0001

WLAN Card Standoff

HS1 STF236R128H22-GP — 434.00X01.0001

H10 HOLE130R99-GP — ZZ.SCREW.T01
H11 HOLE170X130R138X99-GP — ZZ.SCREW.S91
H12 HOLE170X130R138X99-GP — ZZ.SCREW.S91

EMI Soluation

19V_DCBATOUT — 2017/05/15 - SB
3D3V_AUX_S5 — 2017/05/17 - SB
PWR_DCBATOUT_1D0V
PWR_DCBATOUT_VCOREB
PWR_DCBATOUT_VCOREA
PWR_DCBATOUT_VCCGTA
5V_S5

RF Soluation

5V_S5
5V_S0
3D3V_S5
PWR_3D3V
BT+
PWR_DCBATOUT_5V
1V_CPU_CORE
19V_AD+ — 2017/05/14 - SB
19V_DCBATOUT
1V_VCCGT
3D3V_IOAC
PWR_5V
3D3V_MSATA1_S0
20V_AD+_TO_SYS
PWR_DCBATOUT_3D3V
1V_VCCSA

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Date: Wednesday, November 01, 2017 | Sheet 89 of 106

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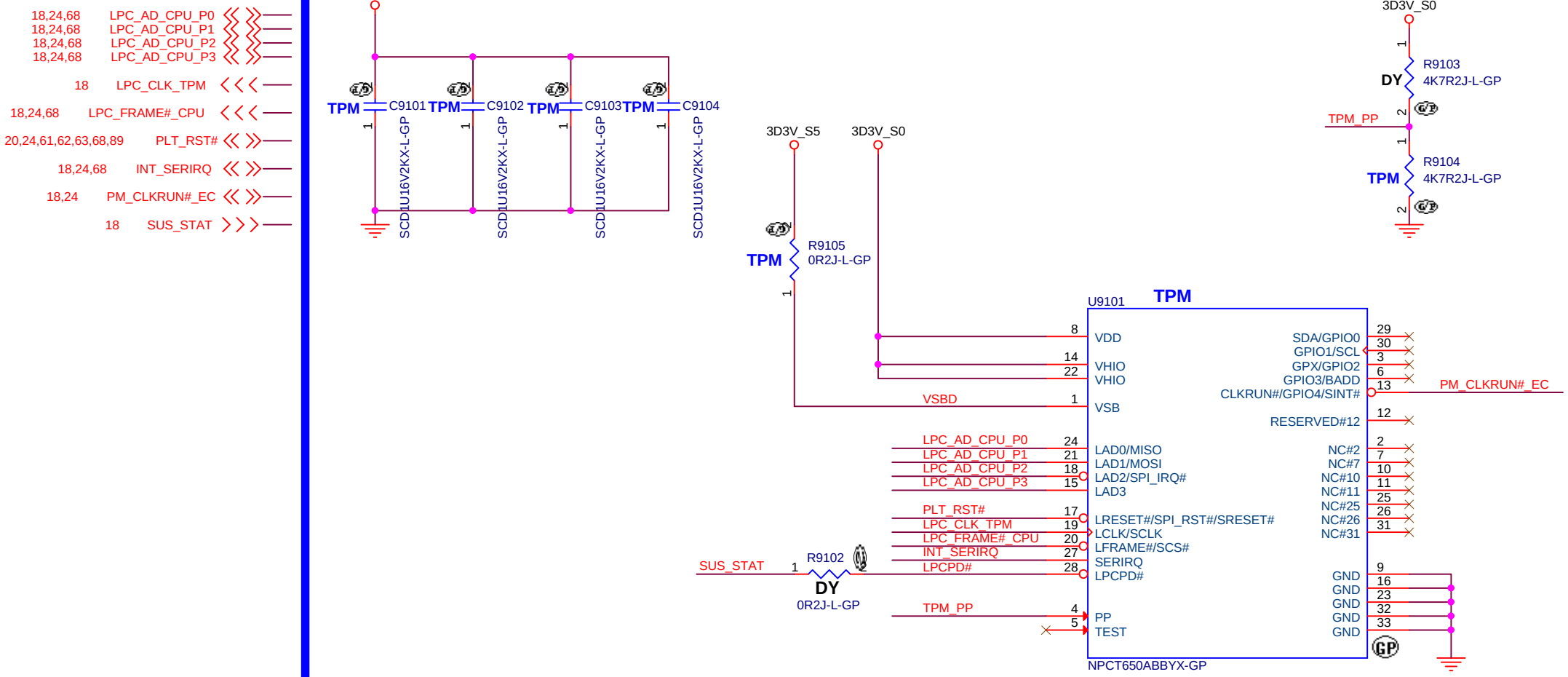
Date: Wednesday, November 01, 2017 Sheet 90 of 106



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P/N: 071.00650.0N03

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Title	***TPM***	
Size A4	Document Number **Carlsberg_KL**	Rev **-1M**
Date: Wednesday, November 01, 2017	Sheet 91 of 106	

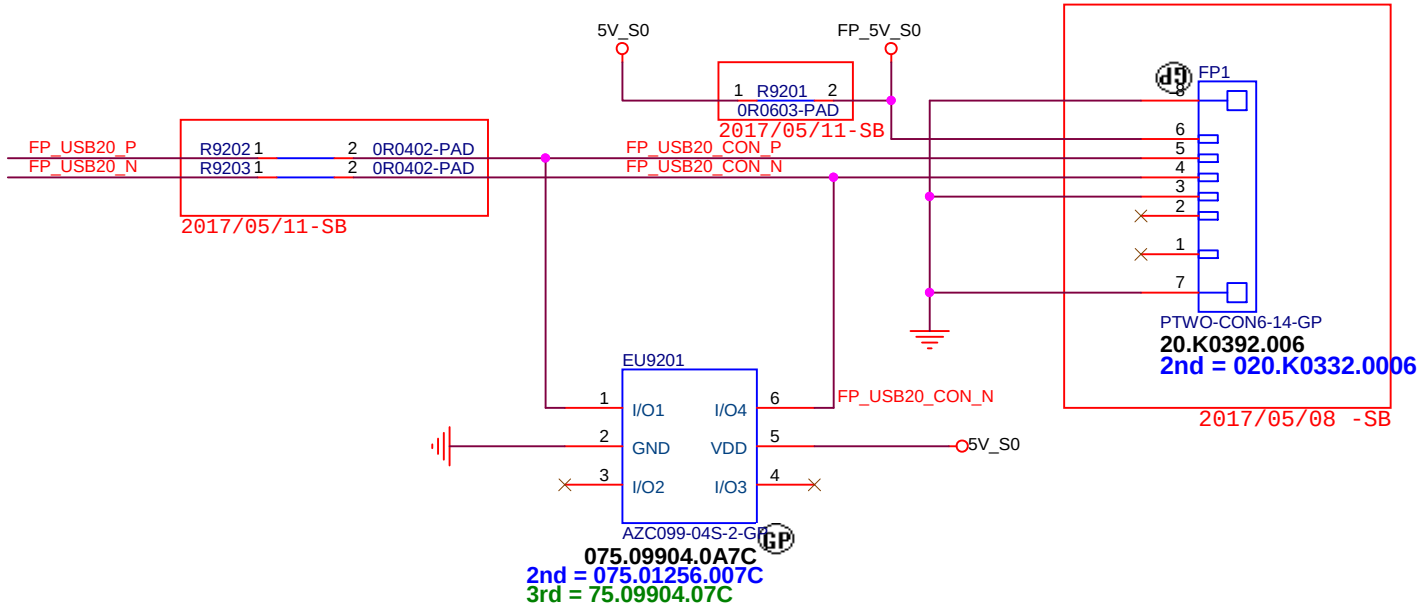
15 FP_USB20_N

15 FP_USB20_P

AFTP

89 FP_USB20_CON_N

89 FP_USB20_CON_P



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Title: ***Finger Print***

Size	Document Number	Rev
Custom	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 92 of 106

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Date: Wednesday, November 01, 2017	Sheet 93 of 106	

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Title	***Smart Card scoket(Reserved)***	
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Date: Wednesday, November 01, 2017	Sheet 94 of 106	

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Title	***GFX eDP(Reserved)***	
Size A	Document Number **Carlsberg_KL**	Rev **-1M**
Date: Wednesday, November 01, 2017	Sheet 95 of 106	

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Title: ***Bottom Docking(Reserved)***

Size	Document Number	Rev
A	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 96 of 106

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Title: ***Inter LAN WG1217LM(Reservrd)***

Size	Document Number	Rev
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Date: Wednesday, November 01, 2017	Sheet 97 of 106	

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Title	***CPU_CFG STRAP(Reserved)***	
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Date: Wednesday, November 01, 2017	Sheet 98 of 106	

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Title: ***CPU_XDP(Reserved)***

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Date: Wednesday, November 01, 2017 Sheet 99 of 106

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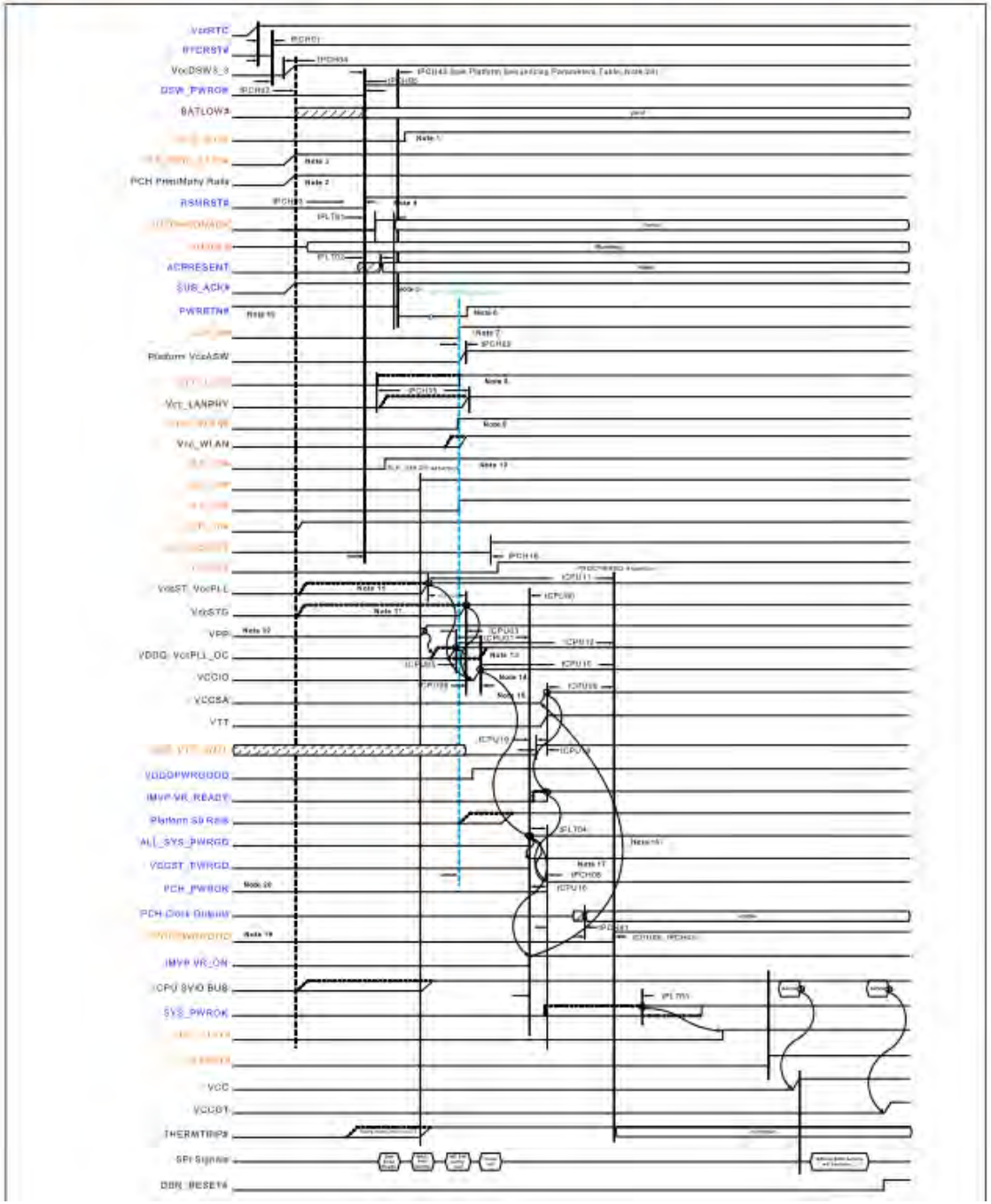
Title	*table of content*	
Size A4	Document Number **Carlsberg_KL**	Rev **-1M**
Date: Wednesday, November 01, 2017	Sheet 100 of 106	

Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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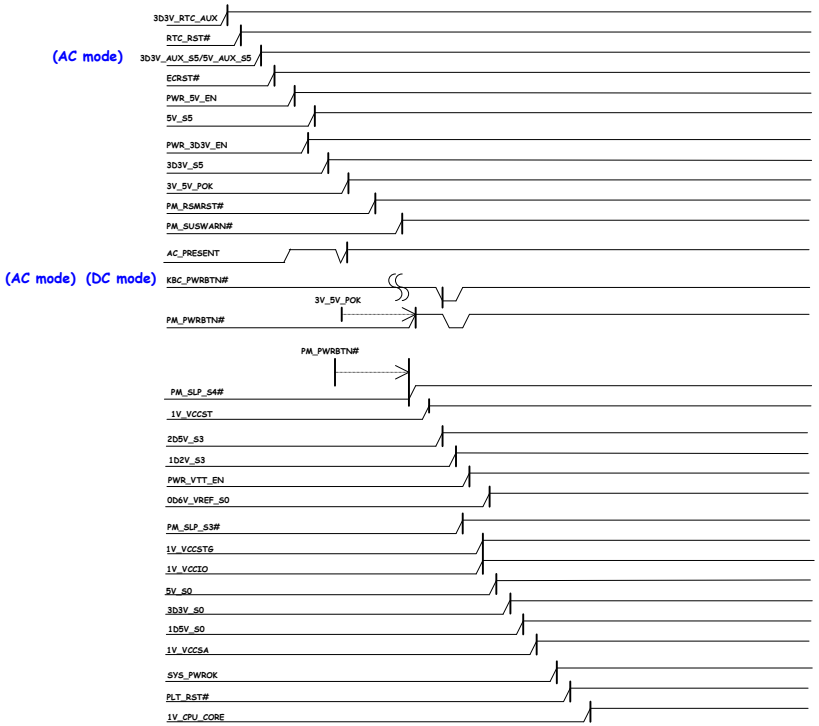
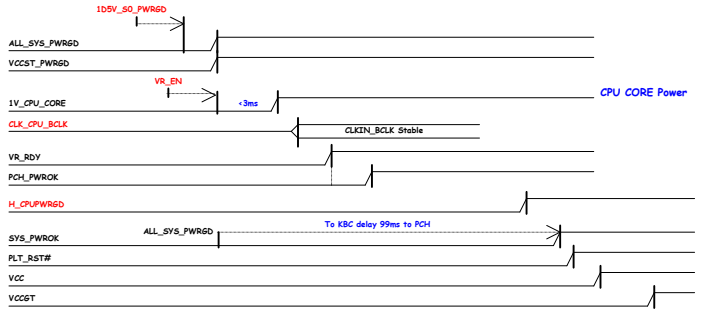
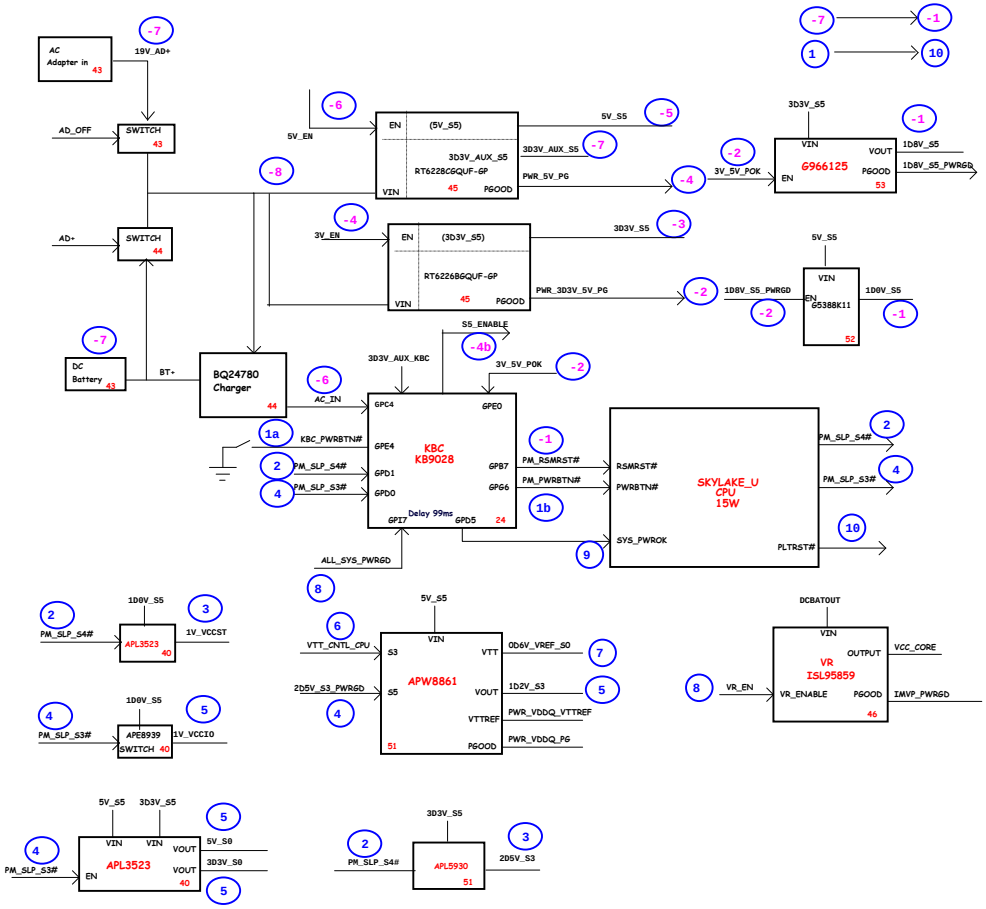
Title: *Change History*		
Size: A4	Document Number: Carlsberg_KL	Rev: -1M
Date: Wednesday, November 01, 2017	Sheet 101 of 106	

Intel-Power Up Sequence







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Title: **Power Sequence**

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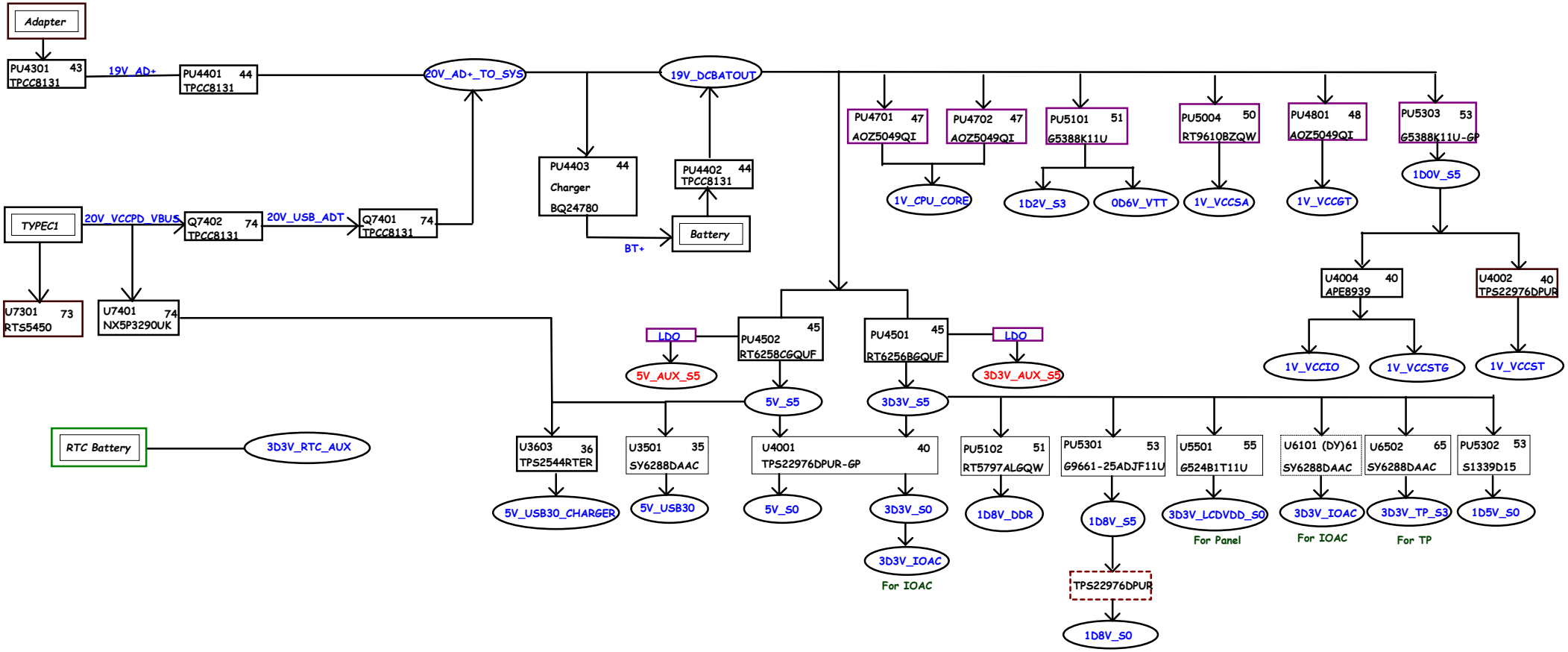
Date: Wednesday, November 01, 2017 Sheet 102 of 106



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Title: Power Block Diagram

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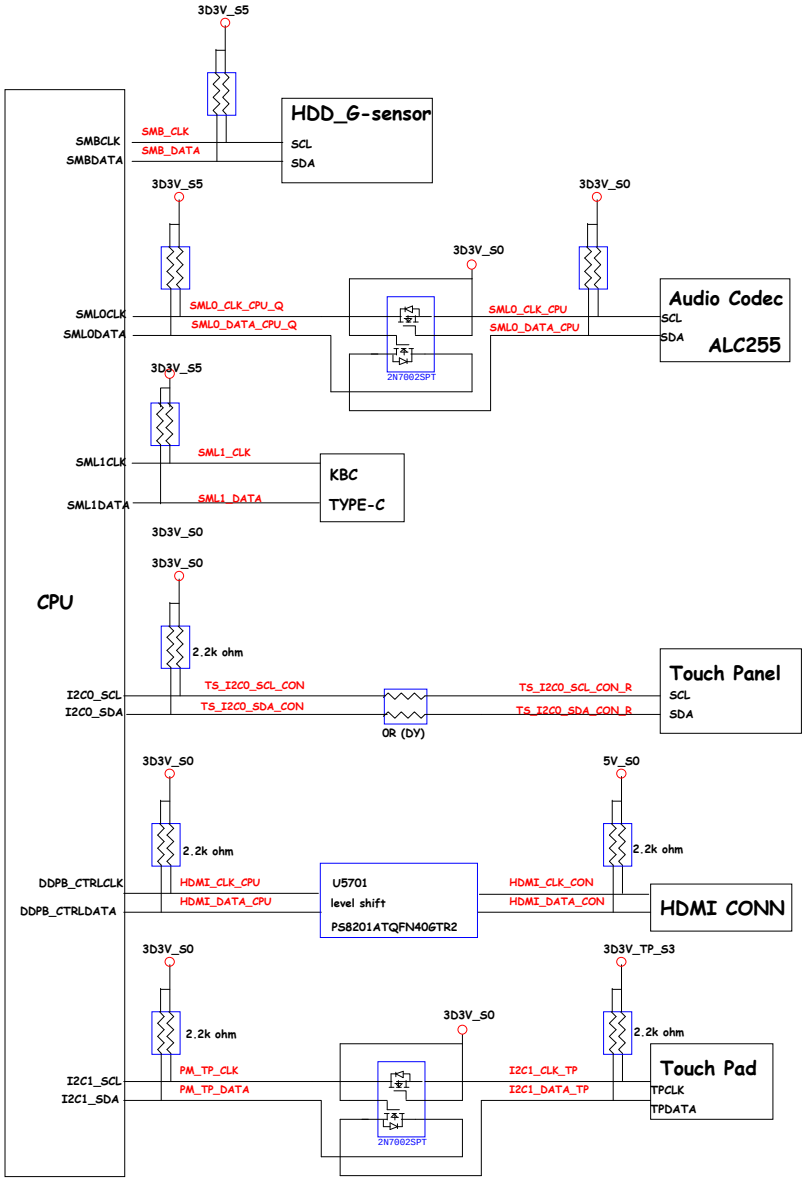
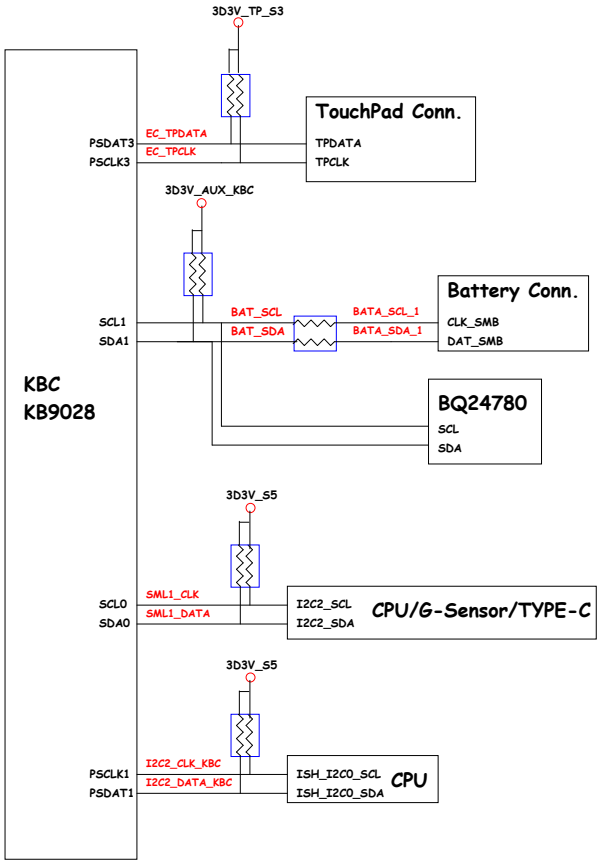
Date: Wednesday, November 01, 2017 Sheet 103 of 106

PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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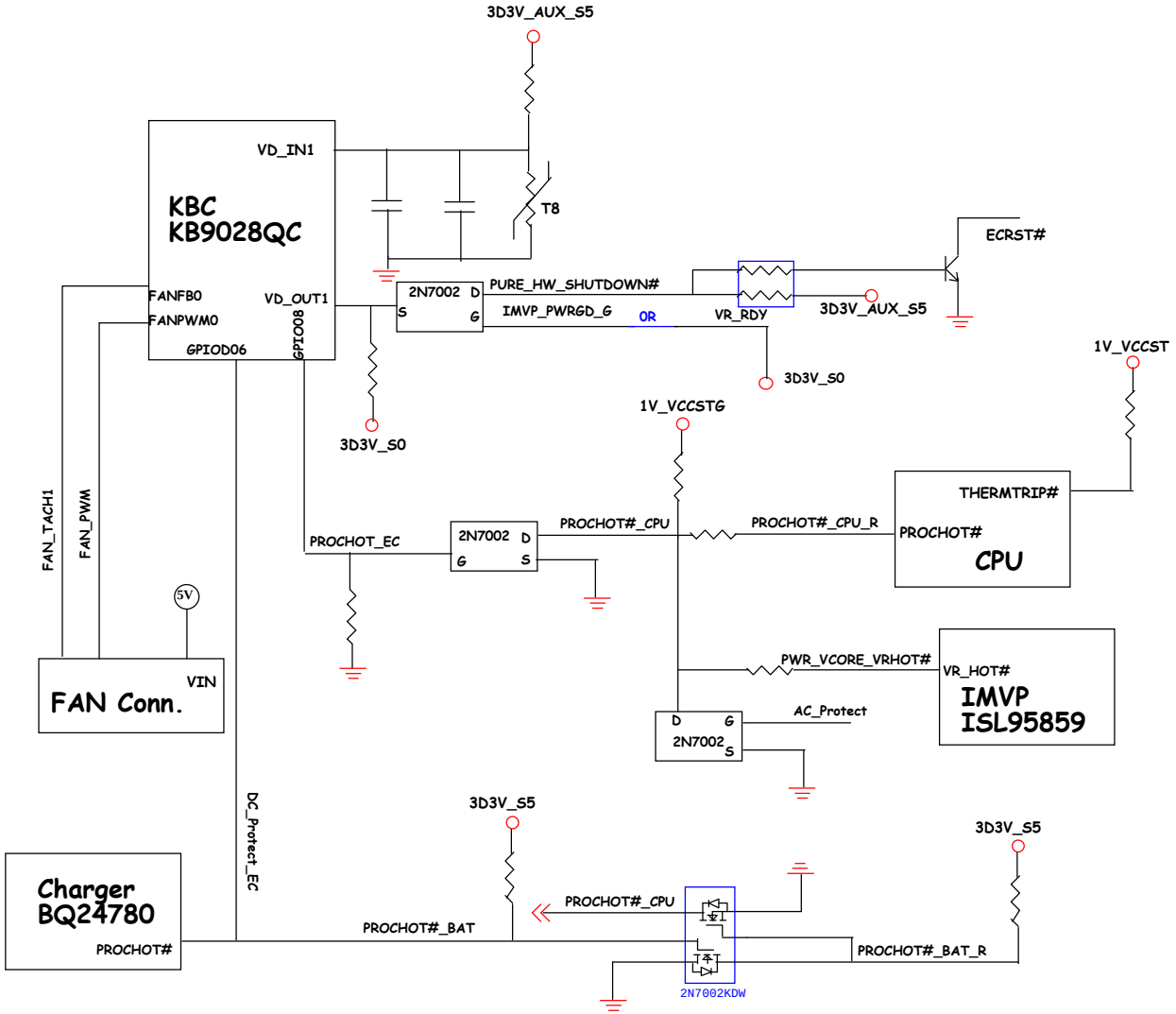
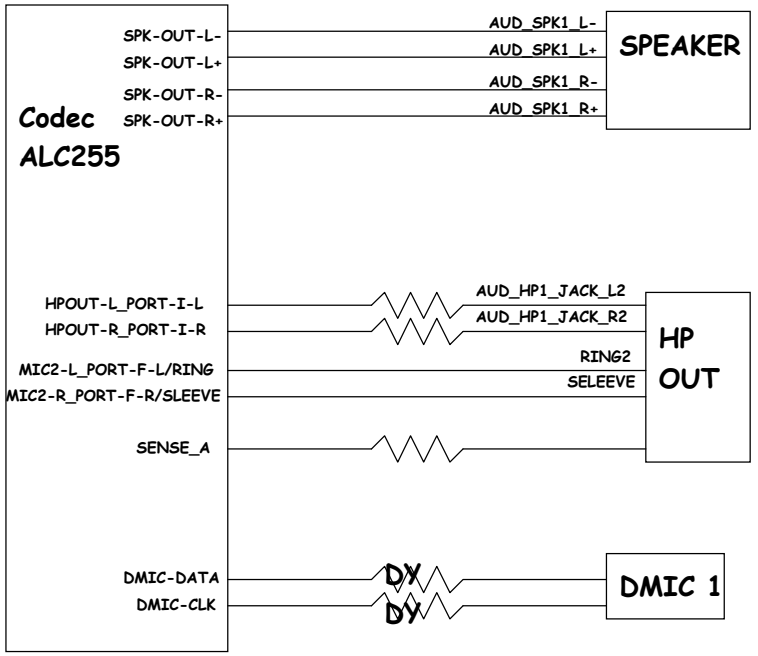
Date: Wednesday, November 01, 2017 | Sheet 104 of 106

Thermal Block Diagram



Audio Block Diagram



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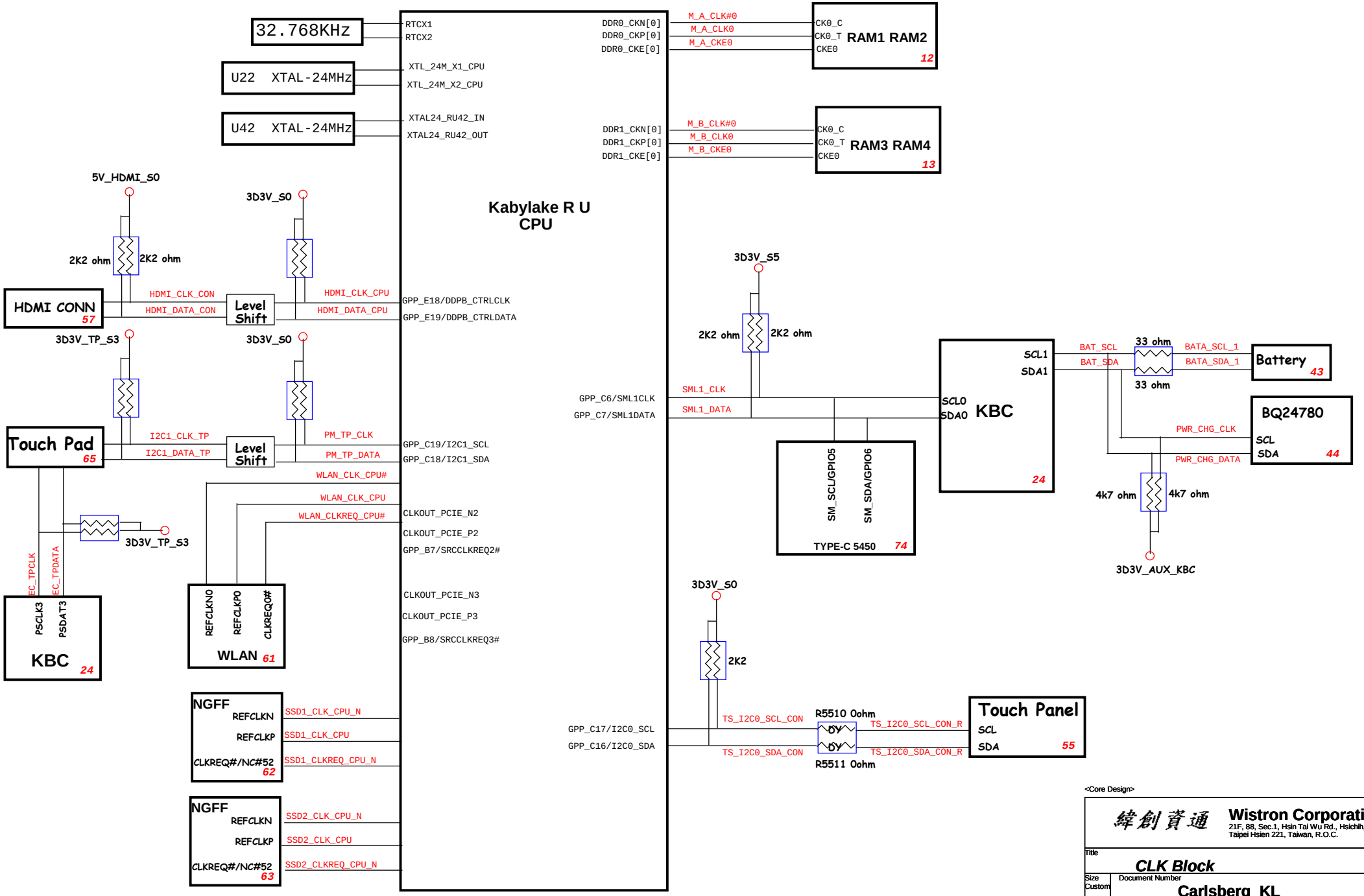
Title: THERMAL/AUDIO BLOCK DIAGRAM

Size	Document Number	Rev
Custom	Carlsberg_KL	-1M

Date: Wednesday, November 01, 2017 Sheet 105 of 106

CLOCK BLOCK DIAGRAM



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Title: CLK Block

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Date: Wednesday, November 01, 2017 | Sheet 106 of 106