

A8E/A8S Merom/GM965/PM965 BLOCK DIAGRAM

Sub block Diagram /
BOM option

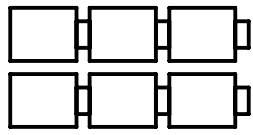
64

CLOCK GEN
ICS9LPR363AGLF-T

29

BATTERY
TYPE

3S2P



CPU
MEROM

3, 4

CPU
CAP

5

POWER
SEQUENCE

2

HOST BUS

...

DVI Dual
CH.

47

CRT & TV
CON

46

LVDS & INV
CON

45



LFB LFB LFB LFB
Nvidia
NB8x series
ATI
M7x series

VGA BAORD



PCI-E
x16

70

CRESTLINE
GM965/PM965

11~15

DDR2 SDRAM 533/667MHz

DDR2 533/667
SODIMM X2
+1.8V
+0.9VS

7, 8

DDR
CAP/RES

9

DCIN
RTC
FAN CON.

THERMAL
CONTROL

50

X4 DMI

VCORE
SYSTEM
1.5VS & 1.05VS
DDR & VTT
+3VAO & +2.5VS
CHARGER
PIC
DETECT
PROTECT
LOAD SWITCH
FLOWCHART
SIGNAL

USB x4

52

USB2.0

SATA

PATA

B/T
Camera
FingerPrint

61
68

SATA HDD

51

ODD Master

51

ICH8M

20~24

PCI EXPRESS X1

PCI BUS

3.3V, 33MHz

ACZ

Azalia
ALC660

OP
TPA0212

MDC
CON

4 IN 1
CARD
READER

42

CARBUS
RICOH
R5C833

1394

LAN 1G
RTL8111B

33

MINI CARD
x2

53

NEW
CARD

43

LAN IO

RJ11,RJ45
CON

34

SW & LED

56

AC & BAT CON
FAN CTRL

60

50

LPC, 33MHz

KBC
IT8511E

KB
ISA
ROM
T/P

30, 31

TPM
Module

62

NEW CARD
(DEBUG)

SIO
LPC47N217

55

FIR

PHONE

MIC_IN

USB x1

67

1394
SLOT

40

<Variant Name>



Title : BLOCKDIAGRAM

ASUSTeK COMPUTER INC

Engineer:

Size Custom

Project Name

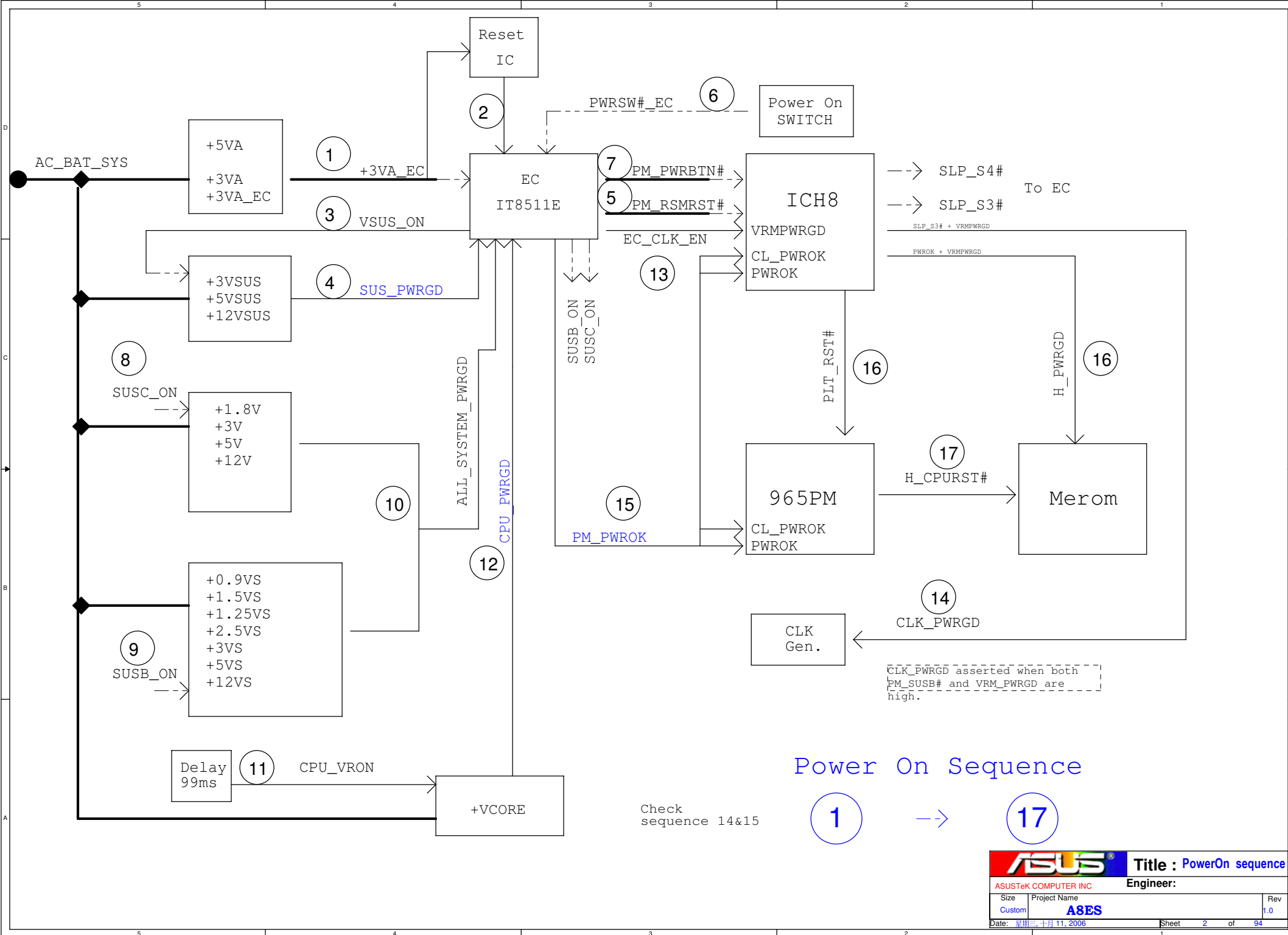
A8ES

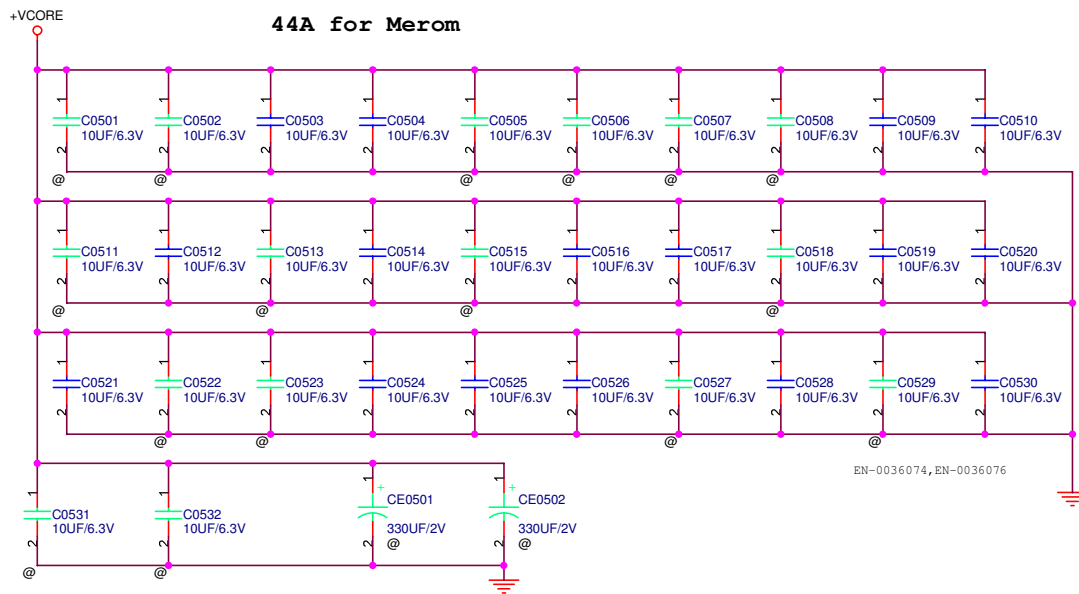
Rev

2.0

Date: 星期一, 一月 29, 2007

Sheet 1 of 94



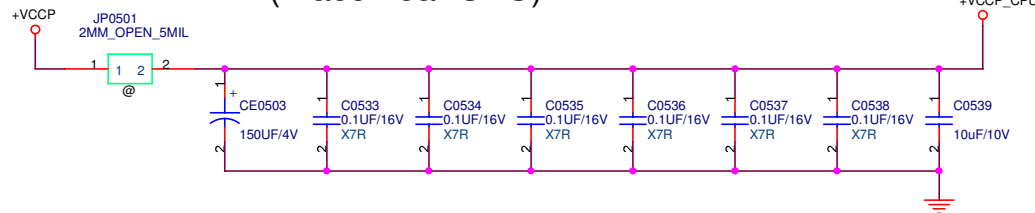


Decoupling guide from INTEL


VCCP	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

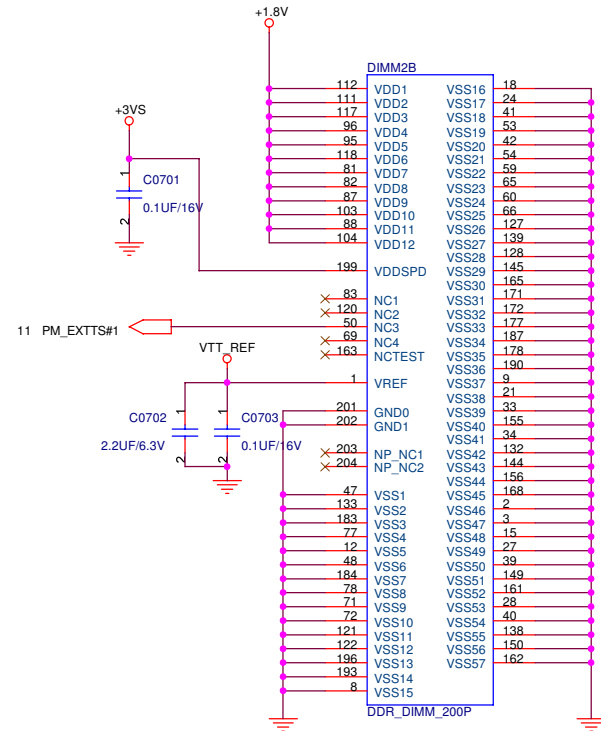
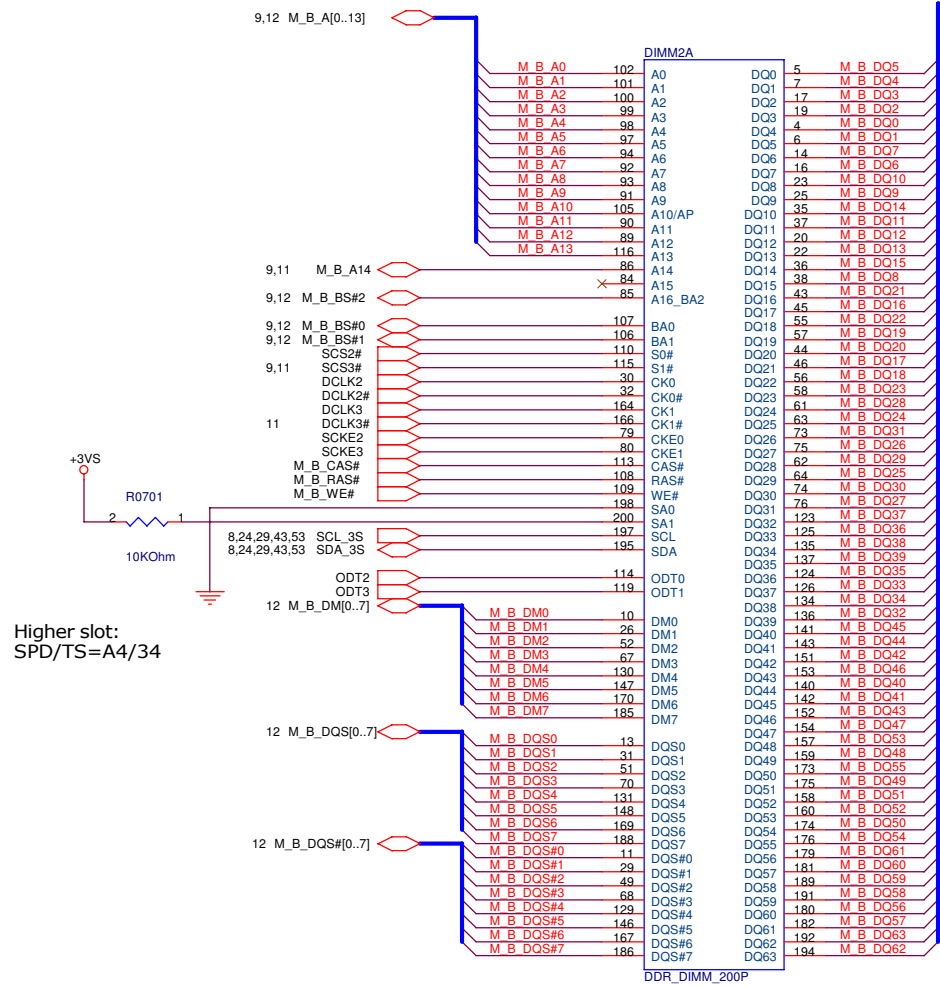
VCCP	10uF/10V	* 32pcs
	330uF/2V	* 0pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
	10uF/10V	* 1pcs

**+VCCP Decoupling Capacitor
(Place near CPU)**

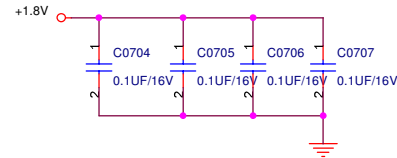


	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

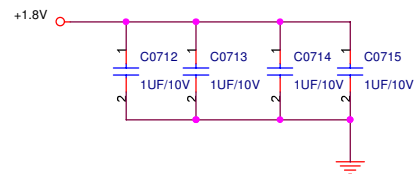
		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name A8ES	Rev 0
Date: 星期三, 十月 11, 2006		Sheet 6 of 94



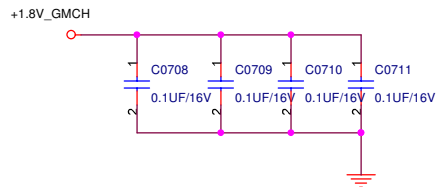
Layout Note: Place these Caps near SO DIMM 0



Layout Note: Place these Caps near SO DIMM 0



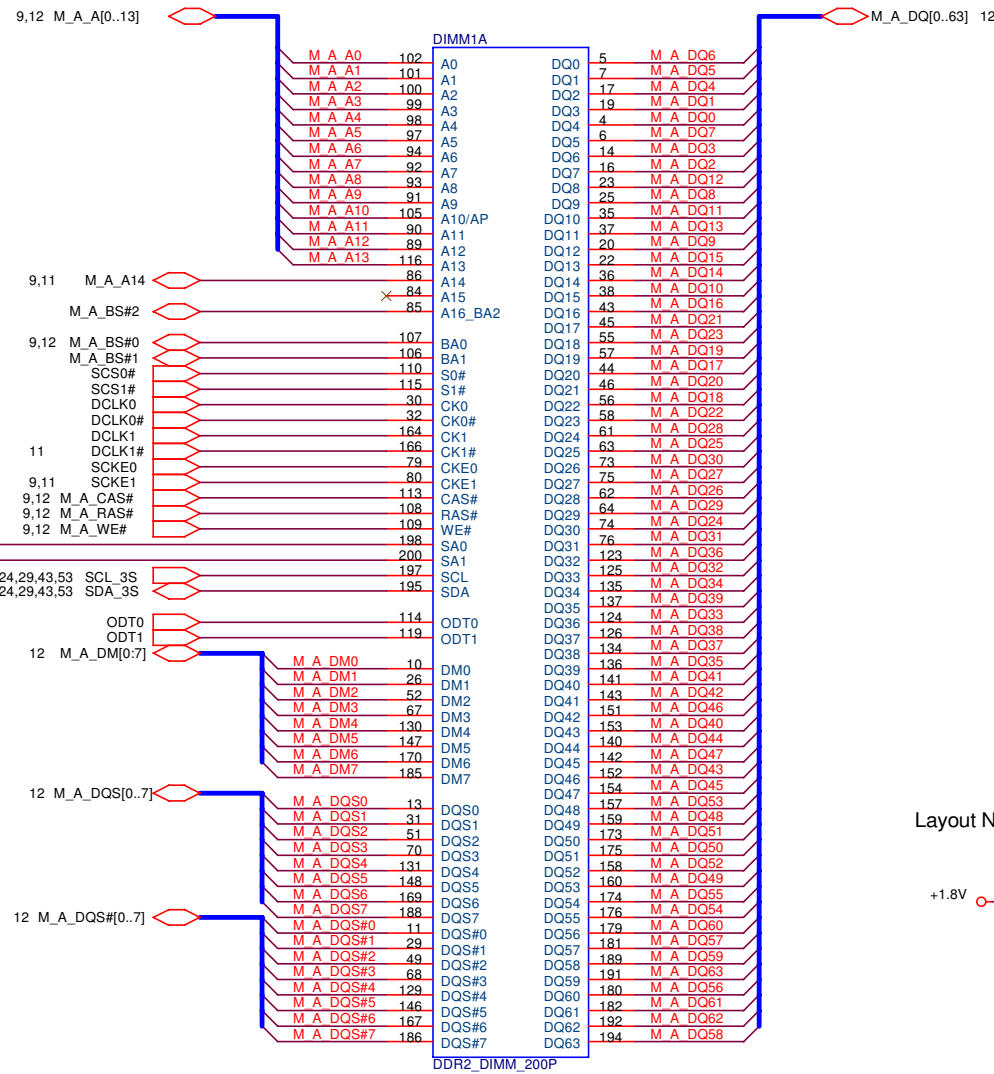
Layout Note: Place these High-Freq decoupling Caps near the GMCH



Upper:Channel B

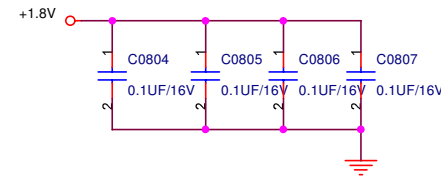
ASUS		Title :DDR SO-DIMM	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES	Rev 1.0	
Date: 星期二, 三月 06, 2007		Sheet 7 of 94	

Lower slot:
SPD/TS=A0/30

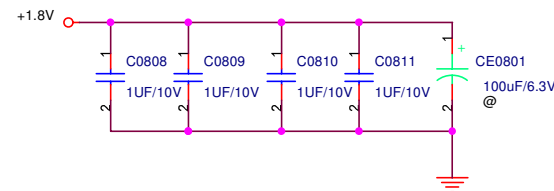


12G025022004 A8ES.PR

Layout Note: Place these Caps near SO DIMM 1

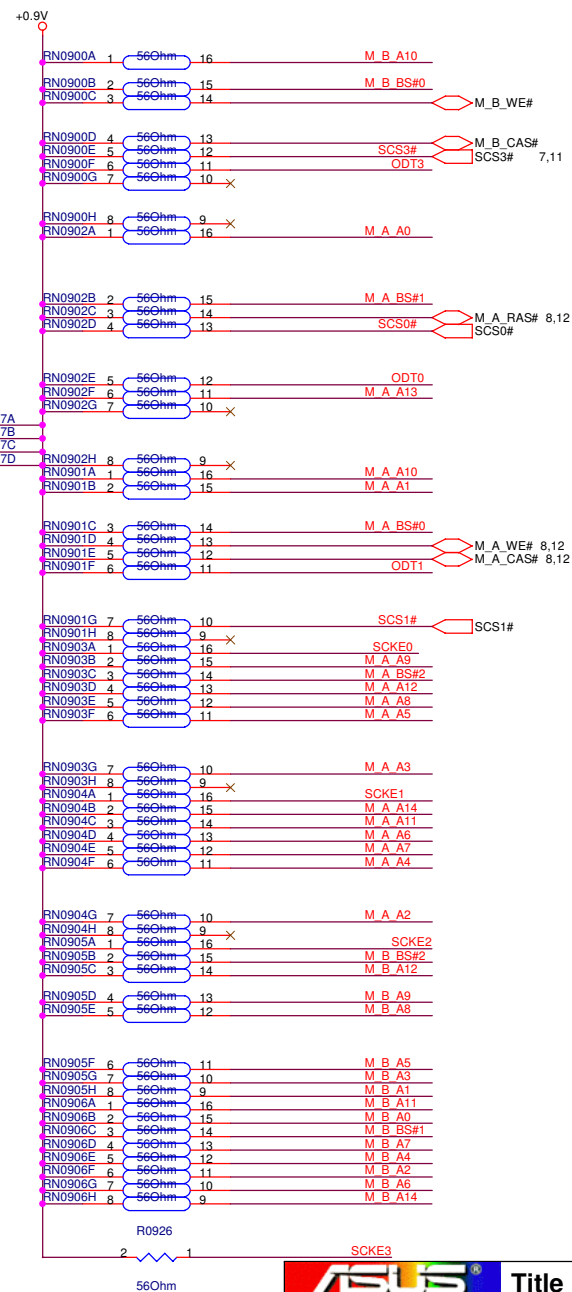
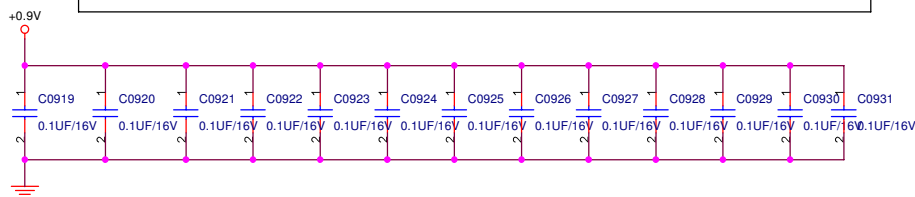
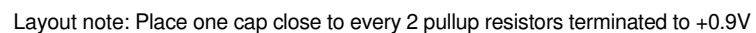
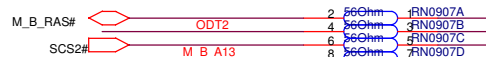
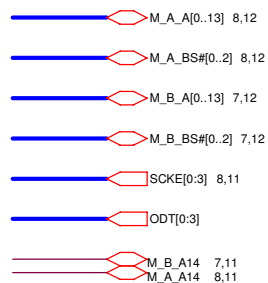


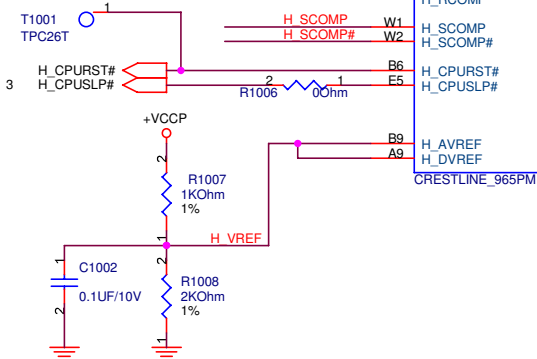
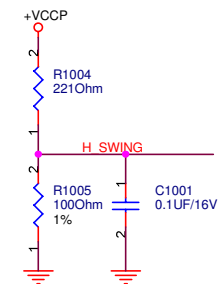
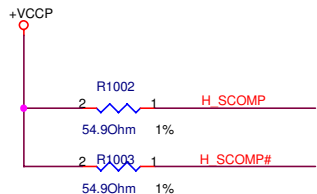
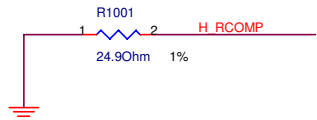
Layout Note: Place these Caps near SO DIMM 1



Lower:Channel A

ASUS		Title :DDR SO-DIMM_TOP	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 星期三, 06月06, 2007		Sheet 8 of 94	





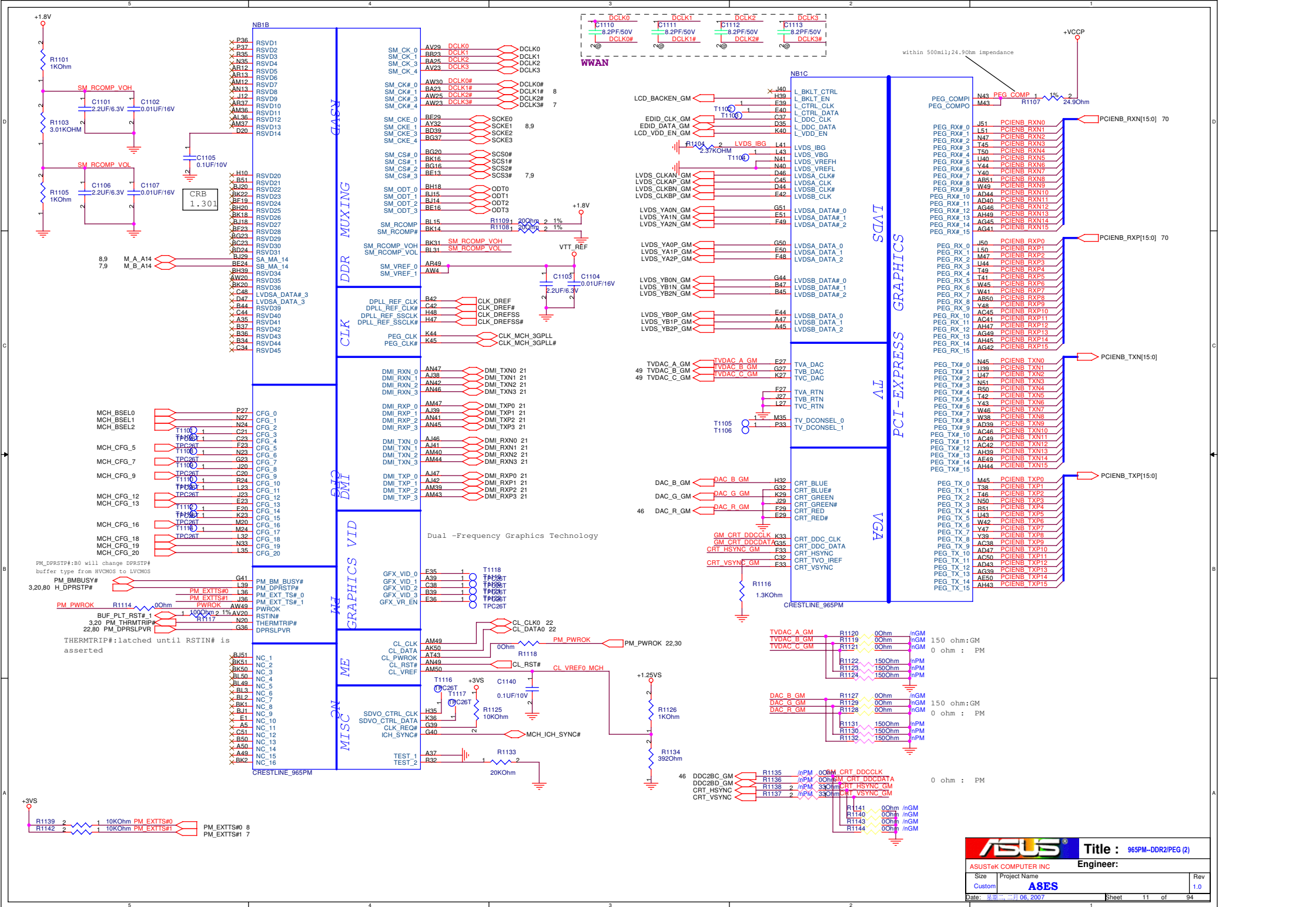
H_D#0	E2	H_D#_0	H_A#_3	J13	H_A#3
H_D#1	G2	H_D#_1	H_A#_4	B11	H_A#4
H_D#2	G2	H_D#_2	H_A#_5	C11	H_A#5
H_D#3	M6	H_D#_3	H_A#_6	M11	H_A#6
H_D#4	H7	H_D#_4	H_A#_7	C15	H_A#7
H_D#5	H3	H_D#_5	H_A#_8	E16	H_A#8
H_D#6	G4	H_D#_6	H_A#_9	L13	H_A#9
H_D#7	F3	H_D#_7	H_A#_10	G17	H_A#10
H_D#8	N8	H_D#_8	H_A#_11	C14	H_A#11
H_D#9	H2	H_D#_9	H_A#_12	K16	H_A#12
H_D#10	M10	H_D#_10	H_A#_13	B13	H_A#13
H_D#11	N12	H_D#_11	H_A#_14	L16	H_A#14
H_D#12	N9	H_D#_12	H_A#_15	J17	H_A#15
H_D#13	H5	H_D#_13	H_A#_16	B14	H_A#16
H_D#14	P13	H_D#_14	H_A#_17	K19	H_A#17
H_D#15	K9	H_D#_15	H_A#_18	P15	H_A#18
H_D#16	M2	H_D#_16	H_A#_19	B17	H_A#19
H_D#17	W10	H_D#_17	H_A#_20	B16	H_A#20
H_D#18	Y8	H_D#_18	H_A#_21	H20	H_A#21
H_D#19	V4	H_D#_19	H_A#_22	L19	H_A#22
H_D#20	M3	H_D#_20	H_A#_23	D17	H_A#23
H_D#21	J1	H_D#_21	H_A#_24	M17	H_A#24
H_D#22	N5	H_D#_22	H_A#_25	N16	H_A#25
H_D#23	N3	H_D#_23	H_A#_26	J19	H_A#26
H_D#24	W6	H_D#_24	H_A#_27	B18	H_A#27
H_D#25	W9	H_D#_25	H_A#_28	E19	H_A#28
H_D#26	N2	H_D#_26	H_A#_29	B17	H_A#29
H_D#27	Y7	H_D#_27	H_A#_30	B15	H_A#30
H_D#28	Y9	H_D#_28	H_A#_31	E17	H_A#31
H_D#29	P4	H_D#_29	H_A#_32	C18	H_A#32
H_D#30	W3	H_D#_30	H_A#_33	A19	H_A#33
H_D#31	N1	H_D#_31	H_A#_34	B19	H_A#34
H_D#32	AD12	H_D#_32	H_A#_35	N19	H_A#35
H_D#33	AE3	H_D#_33	H_ADS#	G12	H_ADS#
H_D#34	AD9	H_D#_34	H_ADSTB#_0	H17	H_ADSTB#0
H_D#35	AC9	H_D#_35	H_ADSTB#_1	G20	H_ADSTB#1
H_D#36	AC7	H_D#_36	H_BNR#	C8	H_BNR#
H_D#37	AC14	H_D#_37	H_BPRI#	E8	H_BPRI#
H_D#38	AD11	H_D#_38	H_BREQ#	F12	H_BR0#
H_D#39	AC11	H_D#_39	H_DEFER#	D6	H_DEFER#
H_D#40	AB2	H_D#_40	H_DBSY#	C10	H_DBSY#
H_D#41	AD7	H_D#_41	HPLL_CLK	AM5	CLK_MCH_BCLK
H_D#42	AB1	H_D#_42	HPLL_CLK#	AM7	CLK_MCH_BCLK#
H_D#43	Y3	H_D#_43	H_DPWR#	H8	H_DPWR#
H_D#44	AC6	H_D#_44	H_DRDY#	K7	H_DRDY#
H_D#45	AE2	H_D#_45	H_DRDY#	E4	H_HITM#
H_D#46	AC5	H_D#_46	H_HITM#	C6	H_HITM#
H_D#47	AG3	H_D#_47	H_LOCK#	G10	H_LOCK#
H_D#48	AJ8	H_D#_48	H_TRDY#	B7	H_TRDY#
H_D#49	AH8	H_D#_49	H_DINV#_0	K5	H_DINV#0
H_D#50	AJ14	H_D#_50	H_DINV#_1	L2	H_DINV#1
H_D#51	AE9	H_D#_51	H_DINV#_2	AD13	H_DINV#2
H_D#52	AE11	H_D#_52	H_DINV#_3	AE13	H_DINV#3
H_D#53	AH12	H_D#_53	H_DSTBN#_0	M7	H_DSTBN#0
H_D#54	AJ5	H_D#_54	H_DSTBN#_1	K3	H_DSTBN#1
H_D#55	AH5	H_D#_55	H_DSTBN#_2	AD2	H_DSTBN#2
H_D#56	AJ6	H_D#_56	H_DSTBN#_3	AH11	H_DSTBN#3
H_D#57	AE7	H_D#_57	H_DSTBP#_0	L7	H_DSTBP#0
H_D#58	AJ7	H_D#_58	H_DSTBP#_1	K2	H_DSTBP#1
H_D#59	AJ2	H_D#_59	H_DSTBP#_2	AC2	H_DSTBP#2
H_D#60	AE5	H_D#_60	H_DSTBP#_3	AJ10	H_DSTBP#3
H_D#61	AJ3	H_D#_61	H_REQ#_0	M14	H_REQ#0
H_D#62	AH2	H_D#_62	H_REQ#_1	E13	H_REQ#1
H_D#63	AH13	H_D#_63	H_REQ#_2	A11	H_REQ#2
			H_REQ#_3	H13	H_REQ#3
			H_REQ#_4	B12	H_REQ#4
			H_RS#_0	E12	H_RS#0
			H_RS#_1	D7	H_RS#1
			H_RS#_2	D8	H_RS#2

HOST

3 H_A#[35:3] H_A#[35:3]

3 H_REQ#[4:0] H_REQ#[4:0]

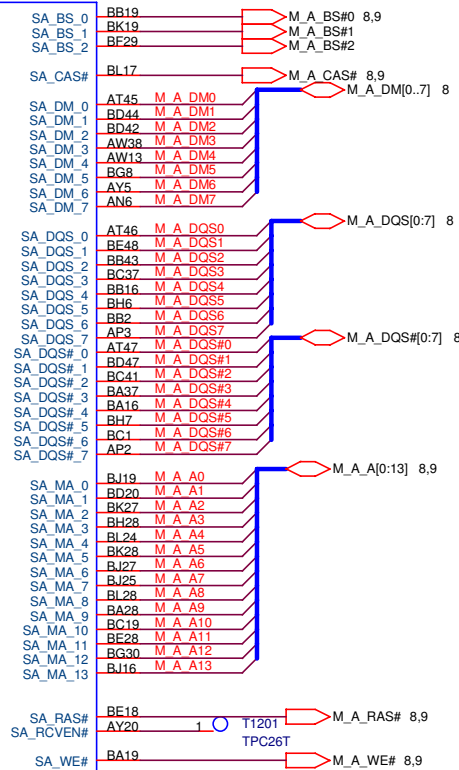
3 H_D#[63:0] H_D#[63:0]



8 M_A_DQ[0:63]



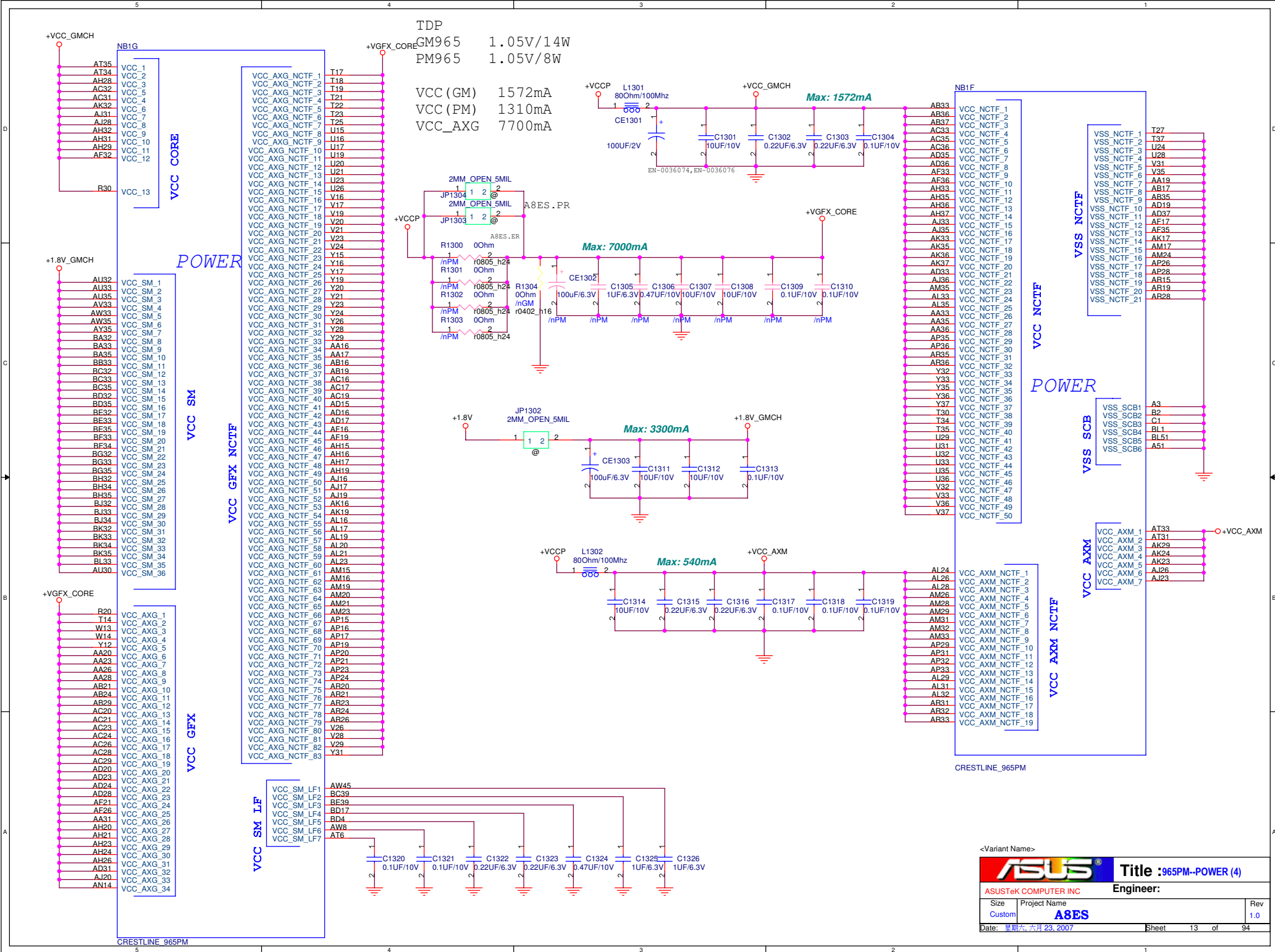
CRESTLINE_965PM




7 M_B_DQ[0:63]




CRESTLINE_965PM



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 16 of 94	


	5	4	3	2	1
D					
C					
B					
A					

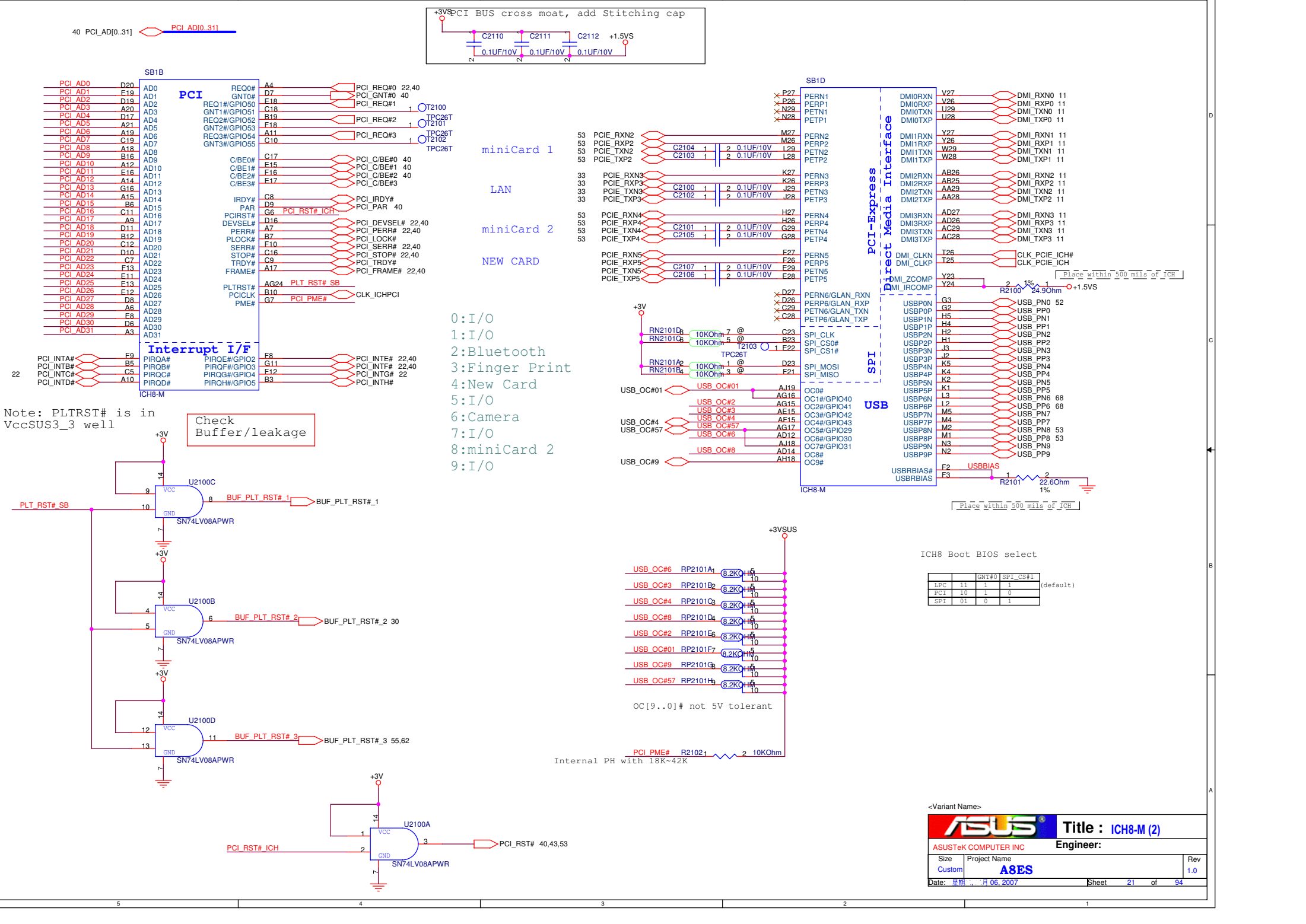
 Title : BLANK	
ASUSTeK COMPUTER INC Engineer:	
Size A	Project Name A8ES
Date: 星期三, 十月 11, 2006 Sheet 17 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 18 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 19 of 94	



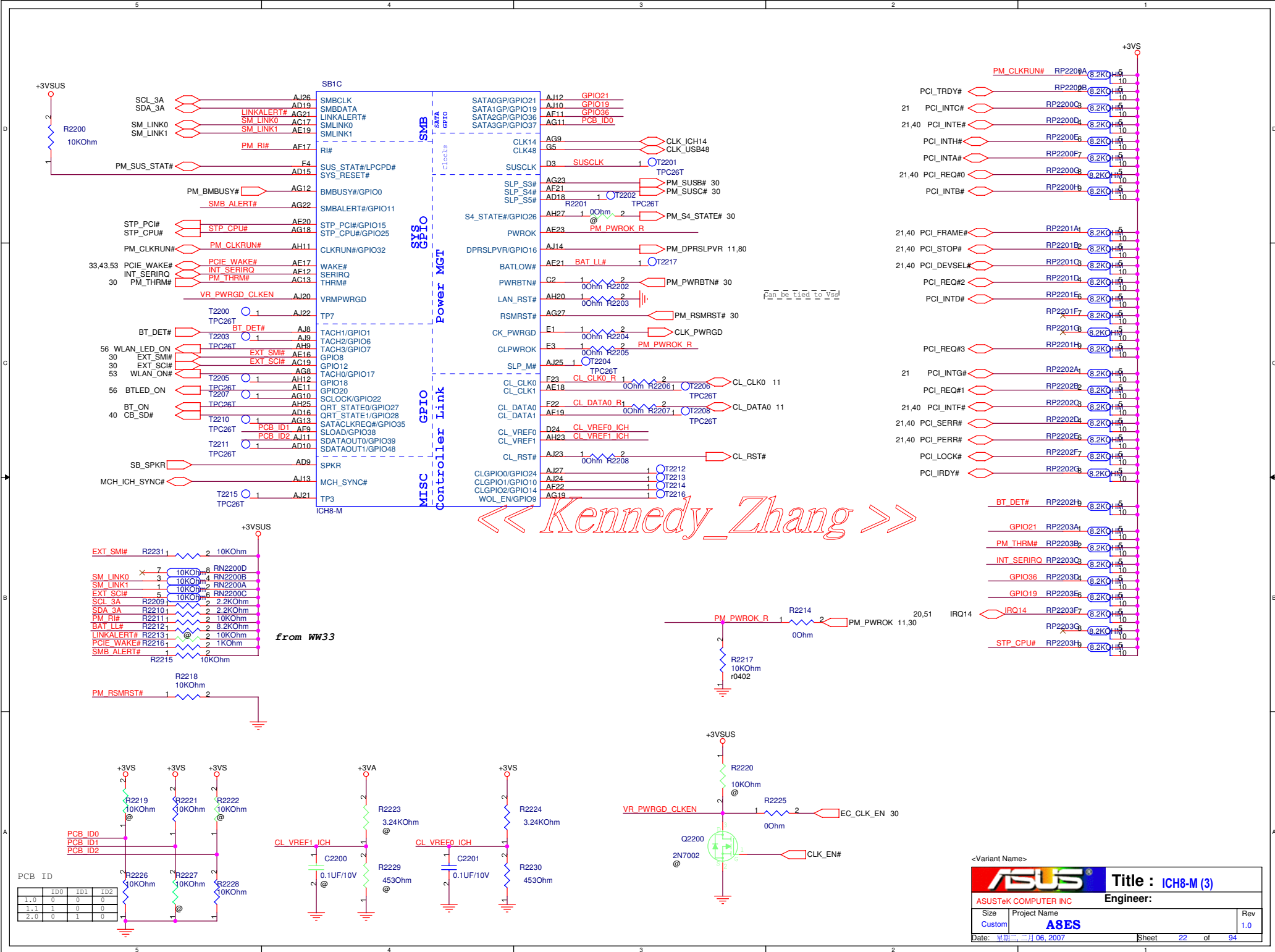
Note: PLTRST# is in VccSUS3_3 well

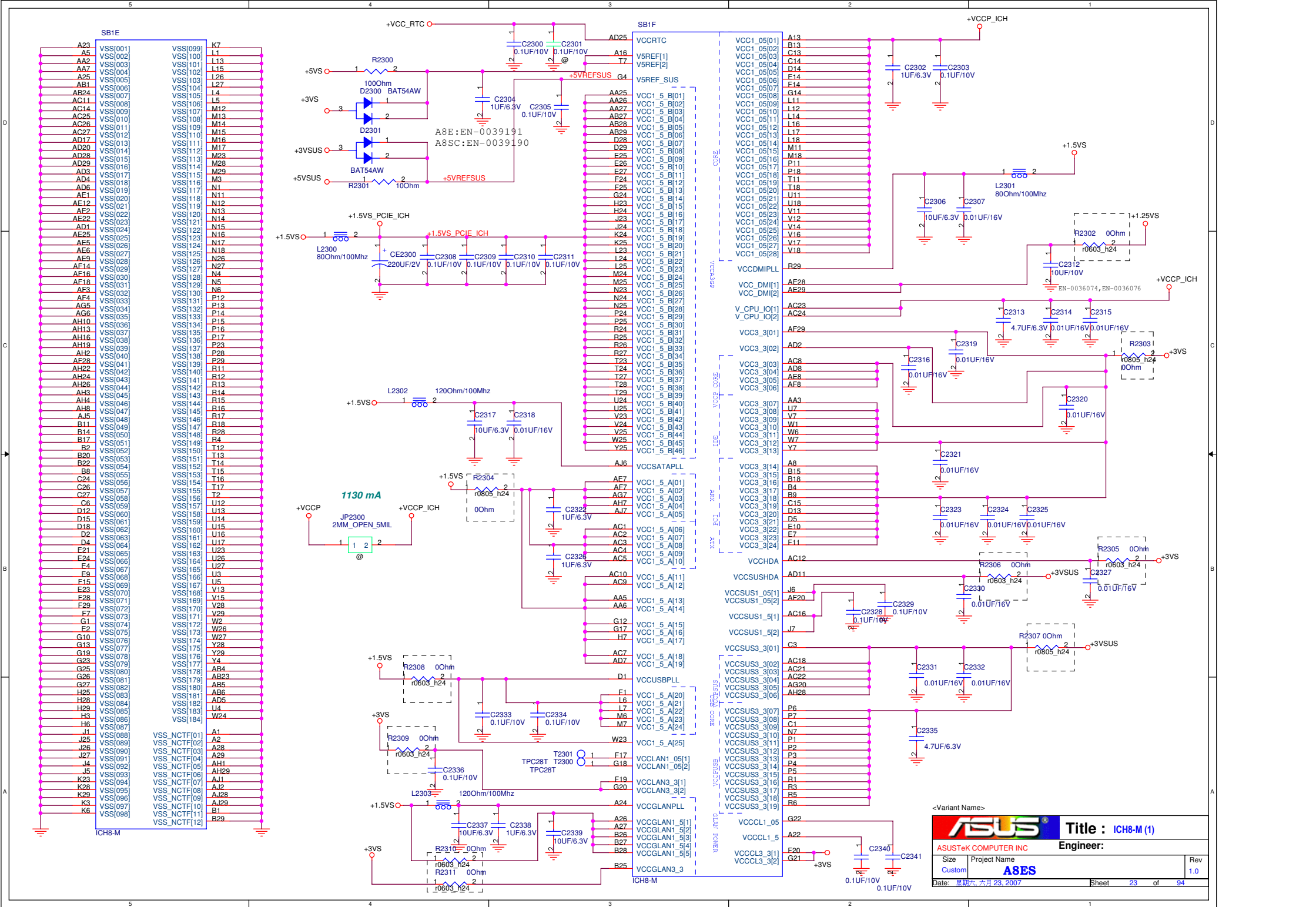
Check Buffer/leakage

ICH8 Boot BIOS select

LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)





ICH8-M

ICH8-M

SM_LINK0

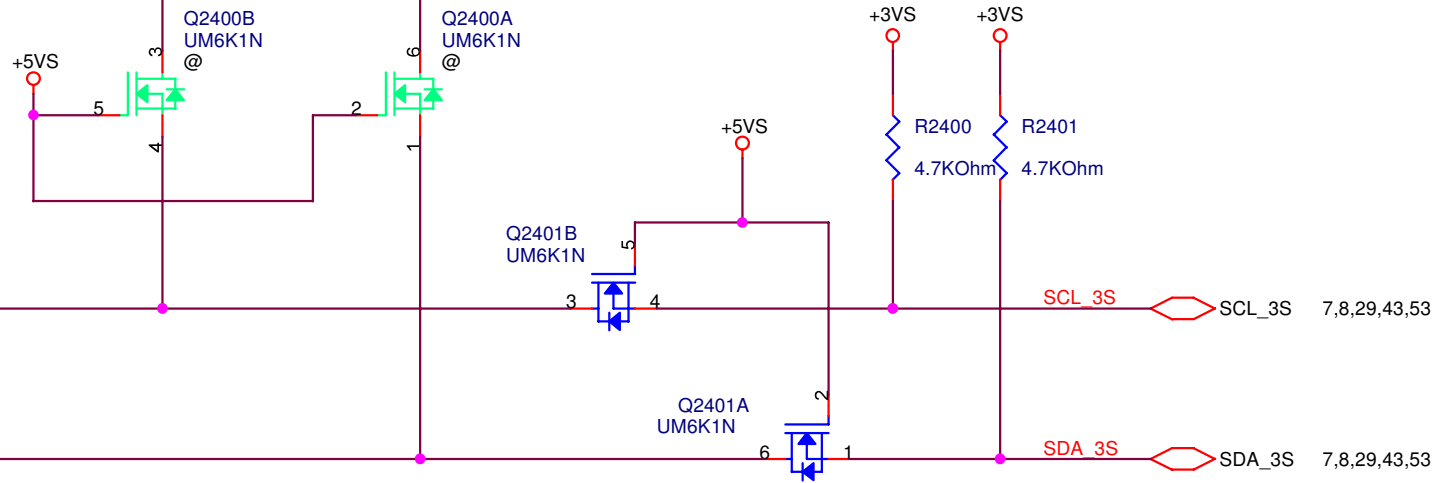
SM_LINK1

SCL_3A


SDA_3A

Check

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.



<Variant Name>

		Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: 星期二, 二月 06, 2007		Sheet 24	of 94

ICH8-M GPIO Assignment

Name	H/W Pin Definition	Type	Tolerance	Power Wel	Default	Mux	Native Name	Real Name	Note
GPIO0	PM_BMBUSY#	IO	3.3V	Core	GPI	Yes	BMBUSY	PM_BMBUSY#	
GPIO1	BT_DET#	IO	3.3V	Core	GPI	No			
GPIO2	PCI_INTE#	IOD	5V	Core	GPI	Yes	PIRQE#	PCI_INTE#	
GPIO3	PCI_INTF#	IOD	5V	Core	GPI	Yes	PIRQF#	PCI_INTF#	
GPIO4	PCI_INTG#	IOD	5V	Core	GPI	Yes	PIRQG#	PCI_INTG#	
GPIO5	PCI_INTH#	IOD	5V	Core	GPI	Yes	PIRQH#	PCI_INTH#	
GPIO6	BIOS_REC	IO	3.3V	Core	GPI	No			
GPIO7	WLAN_LED_ON	IO	3.3V	Core	GPI	No			
GPIO8	EXT_SM#	IO	3.3V	Resume	GPI	No			
GPIO9	LAN_WOL_EN	IO	3.3V	Resume	GPI	Yes	WOL_EN		
GPIO10	ME_ALERT#	IO	3.3V	Resume	GPI	Yes	CLGPIO1		
GPIO11		IO	3.3V	Resume	Native	Yes	SMBALERT#	pull high +3VSUS	
GPIO12	EXT_SCI#	IO	3.3V	Resume	GPI	No			
GPIO13	ODD_DET	IO	3.3V	Resume	Native	Yes	GLAN_DOCK#		removing from EC
GPIO14	NETDETECT	IO	3.3V	Resume	GPI	Yes	CLGPIO2		
GPIO15	STP_PCI#	IO	3.3V	Resume	Native	No	STP_PCI#	STP_PCI#	
GPIO16	PM DPRSLPVR	IO	3.3V	Core	Native	Yes	DPRSLPVR	PM DPRSLPVR	
GPIO17	WLAN_ON#	IO	3.3V	Core	GPI	No			
GPIO18		IO	3.3V	Core	GPO	No			
GPIO19		IO	3.3V	Core	GPI	Yes	SATA1GP		
GPIO20	BTLED_ON	IO	3.3V	Core	GPO	No			
GPIO21		IO	3.3V	Core	GPI	Yes	SATA0GP		
GPIO22		IO	3.3V	Core	GPI	Yes	SCLOCK		
GPIO23		IO	3.3V	Core	Native	Yes	LDRQ1#		
GPIO24	PS_CPPE#	IO	3.3V	Resume	GPO	Yes	CLGPIO0		removing from EC; note by Alan
GPIO25	STP_CPU#	IO	3.3V	Resume	Native	No	STP_CPU#	STP_CPU#	
GPIO26	PM_S4_STATE#	IO	3.3V	Resume	Native	Yes	S4_STATE#		
GPIO27	BT_ON#BT_ON	IO	3.3V	Resume	GPO	Yes	QRT_STATE0		
GPIO28	CB_SD#	IO	3.3V	Resume	GPO	Yes	QRT_STATE1		Cardbus_Shutdown#
GPIO29	OC5#	IO	3.3V	Resume	Native	Yes	OC5#		OC#
GPIO30	OC6#	IO	3.3V	Resume	Native	Yes	OC6#		OC#
GPIO31	OC7#	IO	3.3V	Resume	Native	Yes	OC7#		OC#
GPIO32	PM_CLKRUN#	IO	3.3V	Core	Native	No	CLKRUN#	PM_CLKRUN#	
GPIO33		IO	3.3V	Core	GPO	Yes	HDA_DOCK_EN#		
GPIO34		IO	3.3V	Core	GPO	Yes	HDA_DOCK_RST#		
GPIO35	SATACLKREQ#	IO	3.3V	Core	GPO	Yes	SATACLKREQ#		
GPIO36	EMAIL_LED#	IO	3.3V	Core	GPI	Yes	SATA2GP		
GPIO37	PCB_ID0	IO	3.3V	Core	GPI	Yes	SATA3GP		
GPIO38	PCB_ID1	IO	3.3V	Core	GPI	Yes	SLOAD		
GPIO39	PCB_ID2	IO	3.3V	Core	GPI	Yes	SDATAOUT0		
GPIO40	OC4#	IO	3.3V	Resume	Native	Yes	OC4#		OC#
GPIO41	OC3#	IO	3.3V	Resume	Native	Yes	OC3#		OC#
GPIO42	OC2#	IO	3.3V	Resume	Native	Yes	OC2#		OC#
GPIO43	OC1#	IO	3.3V	Resume	Native	Yes	OC1#		OC#
GPIO44		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO45		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO46		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO47		IO	N/A	N/A	N/A	N/A	N/A	N/A	
GPIO48		IO	3.3V	Core	GPI	Yes	SDATAOUT1		
GPIO49	H_PWRGD	IO	V_CPU_IO	V_CPU_IO	Native	Yes	CPUPWRGD	H_PWRGD	
GPIO50	PCI_REQ1#	IO	5.5V	Core	Native	Yes	REQ1#		
GPIO51	PCI_GNT1#	IO	3.3V	Core	Native	Yes	GNT1#		
GPIO52	PCI_REQ2#	IO	5.5V	Core	Native	Yes	REQ2#		
GPIO53	PCI_GNT2#	IO	3.3V	Core	Native	Yes	GNT2#		
GPIO54		IO	5.5V	Core	Native	Yes	REQ3#		reserved for GPIO
GPIO55		IO	3.3V	Core	Native	Yes	GNT3#		reserved for GPIO

Title : BLANK

Engineer:

ASUSTek COMPUTER INC

Project Name
A8ES


Rev
0

Date: 星期三, 十月 11, 2006 Sheet 25 of 94

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

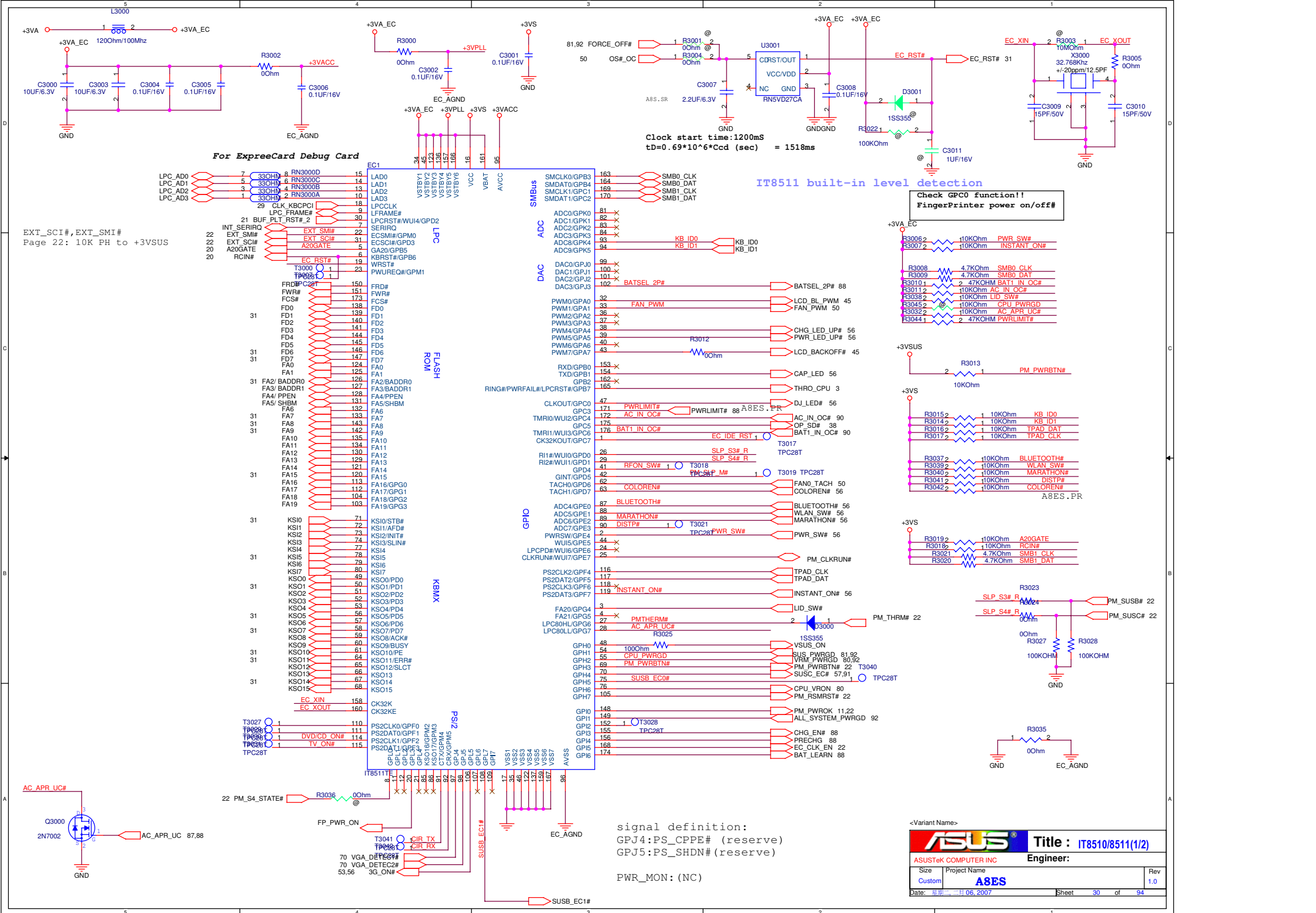
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 26 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

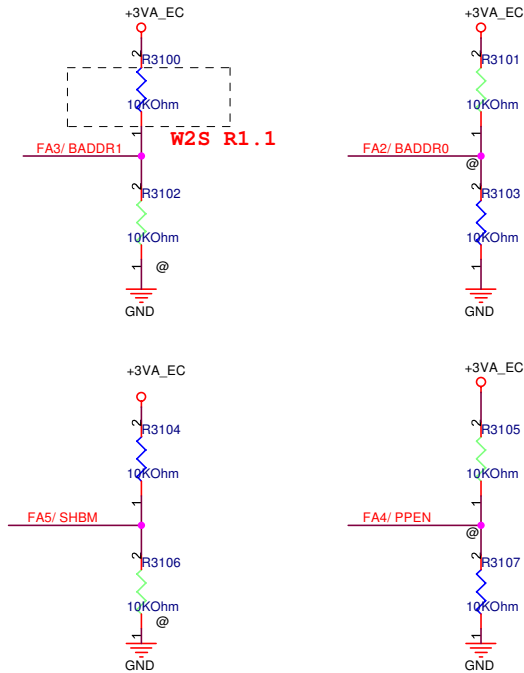
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 27 of 94	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 28 of 94	



10:Determined by EC

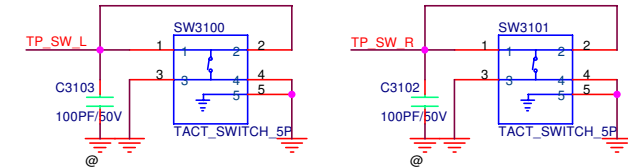
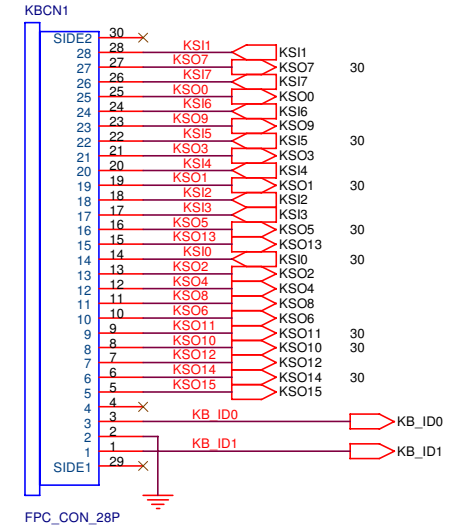


SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

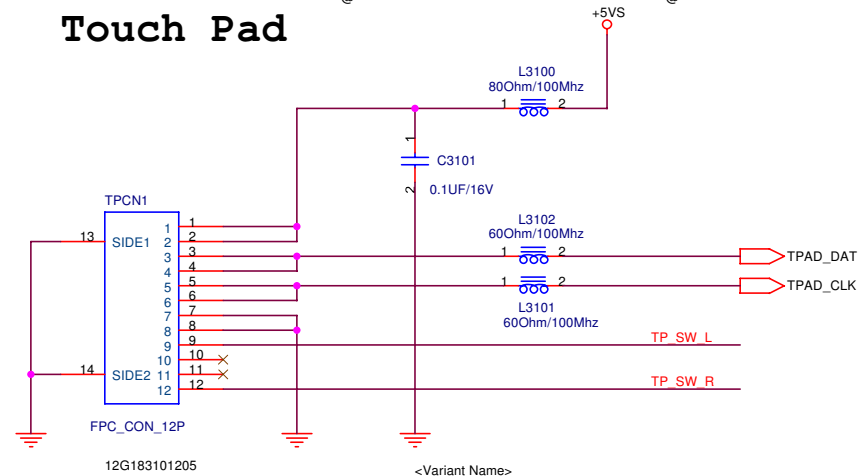
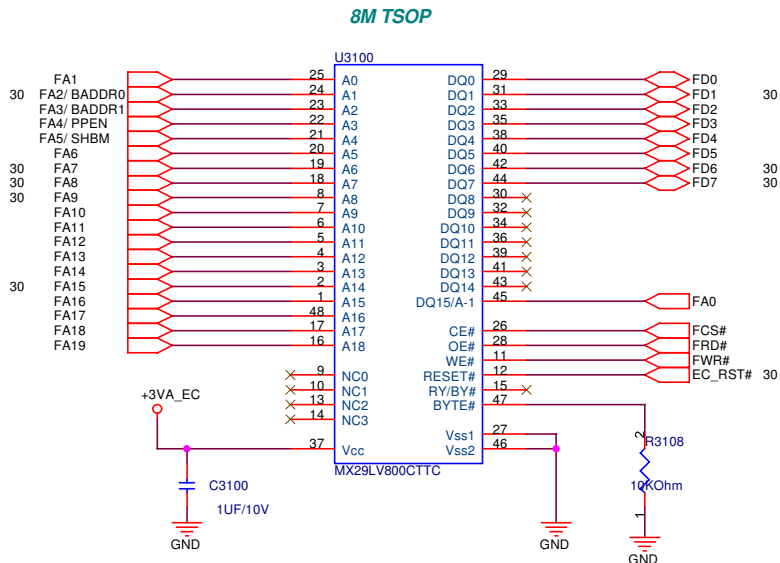
BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

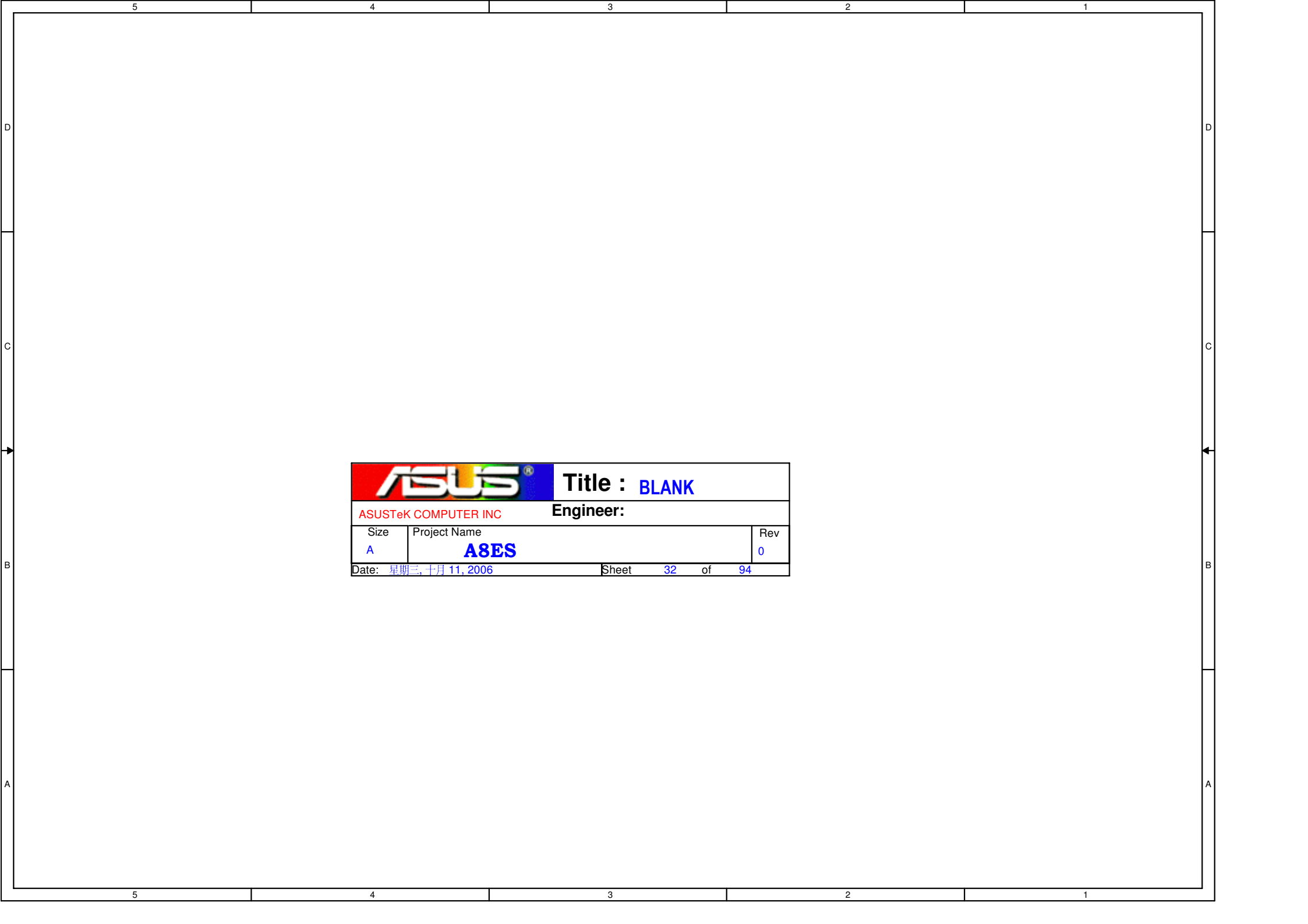



Touch Pad



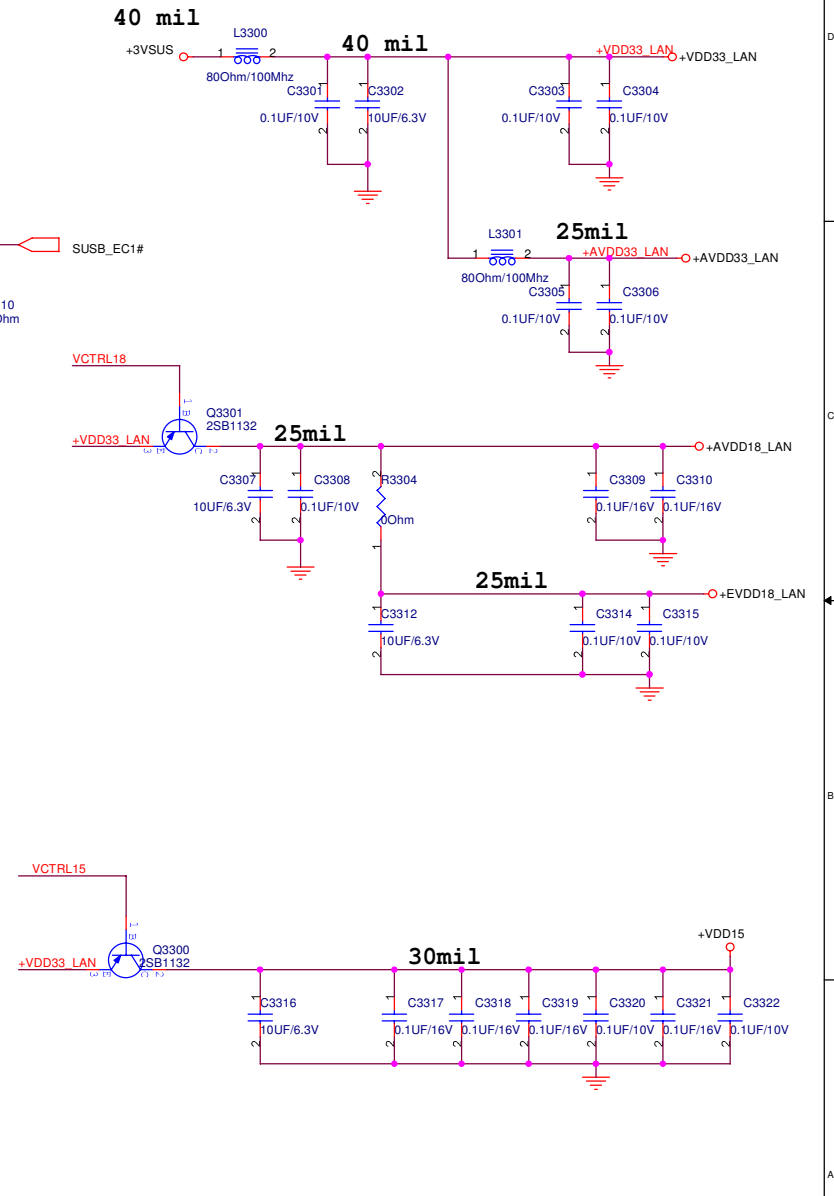
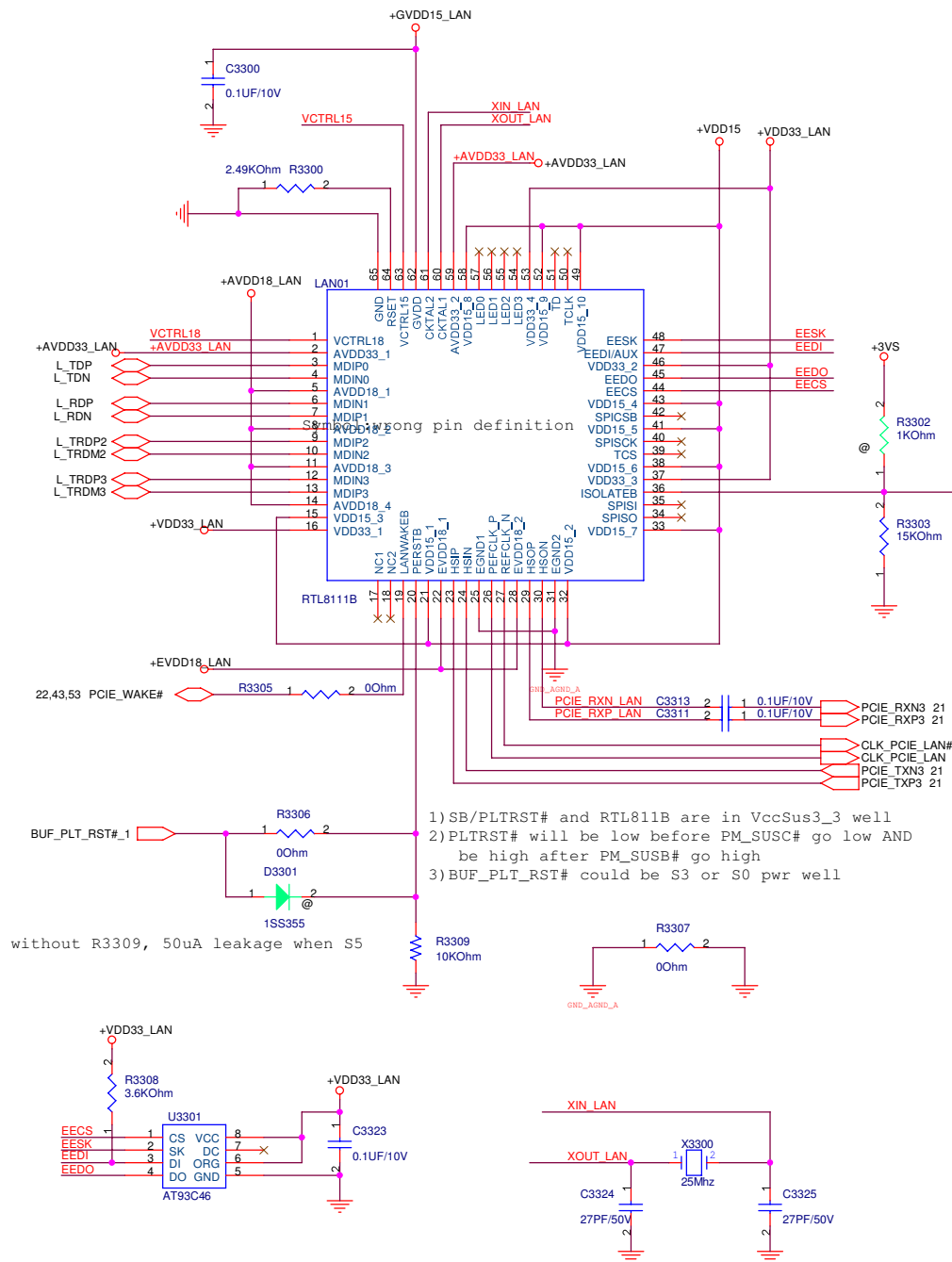
<Variant Name>

ASUS		Title : IT8510/8511(2/2)	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 星期二, 二月 06, 2007		Sheet 31 of 94	



		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		0
Date: 星期三, 十月 11, 2006		Sheet 32 of 94	

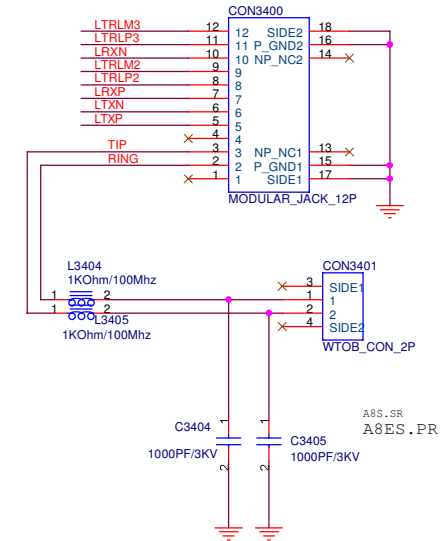
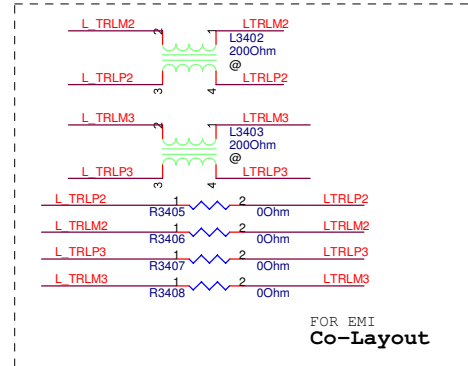
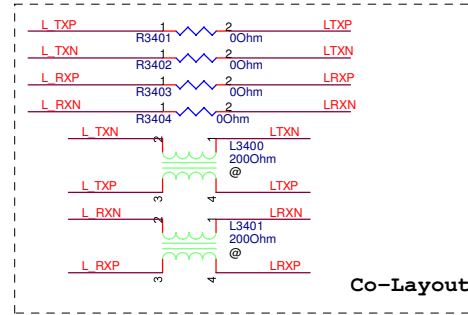
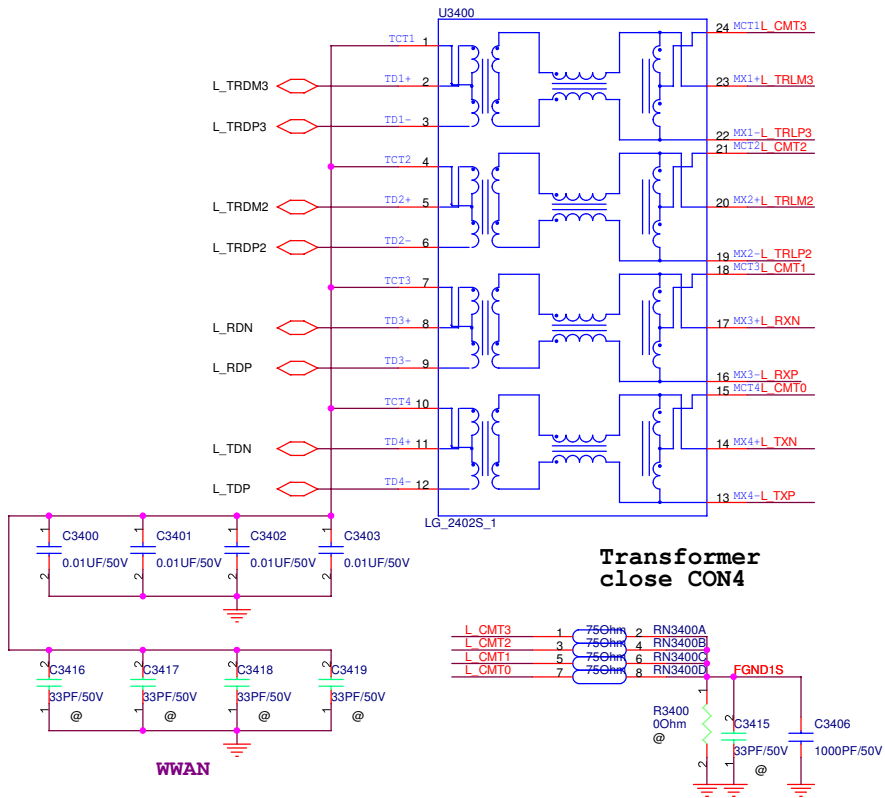
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA



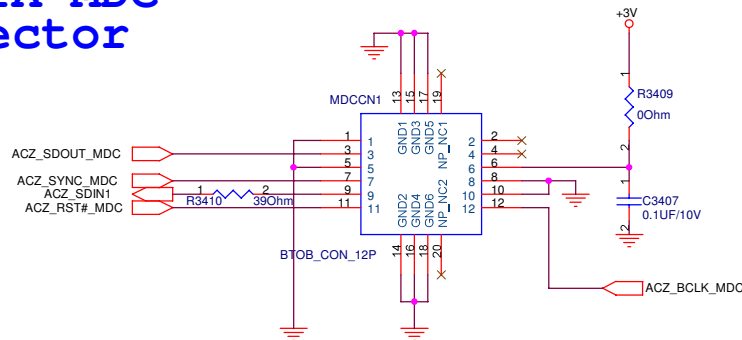
<Variant Name>

ASUS		Title : GigaLAN	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 2007.06.06		Sheet: 33 of 94	

2402S have issue after IR reflow,
alternative part:LG-2410S-1




AZALIA MDC Connector

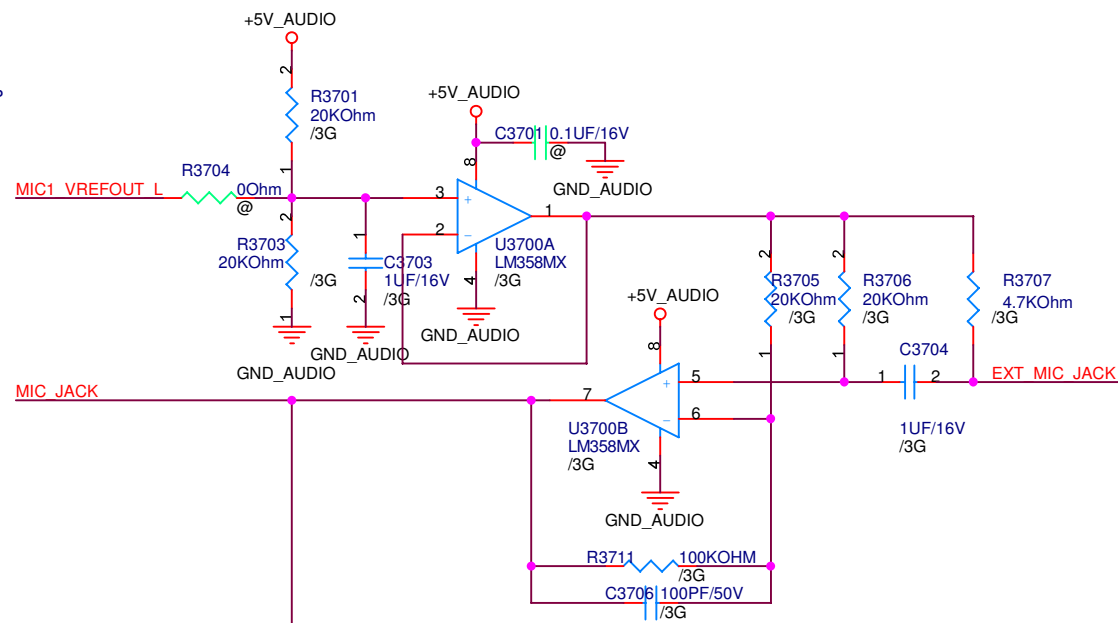
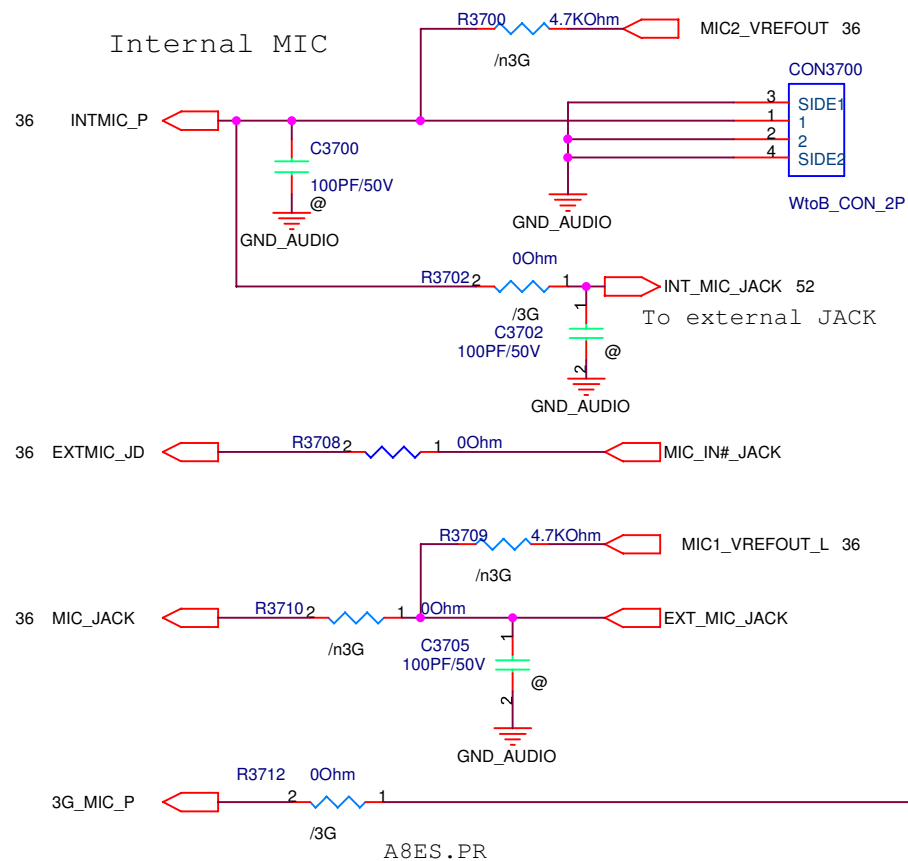


<Variant Name>

ASUS		Title : RJ11+45 ,MDC	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 星期日, 月 06, 2007	Sheet 34	of 94	


5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 35 of 94	

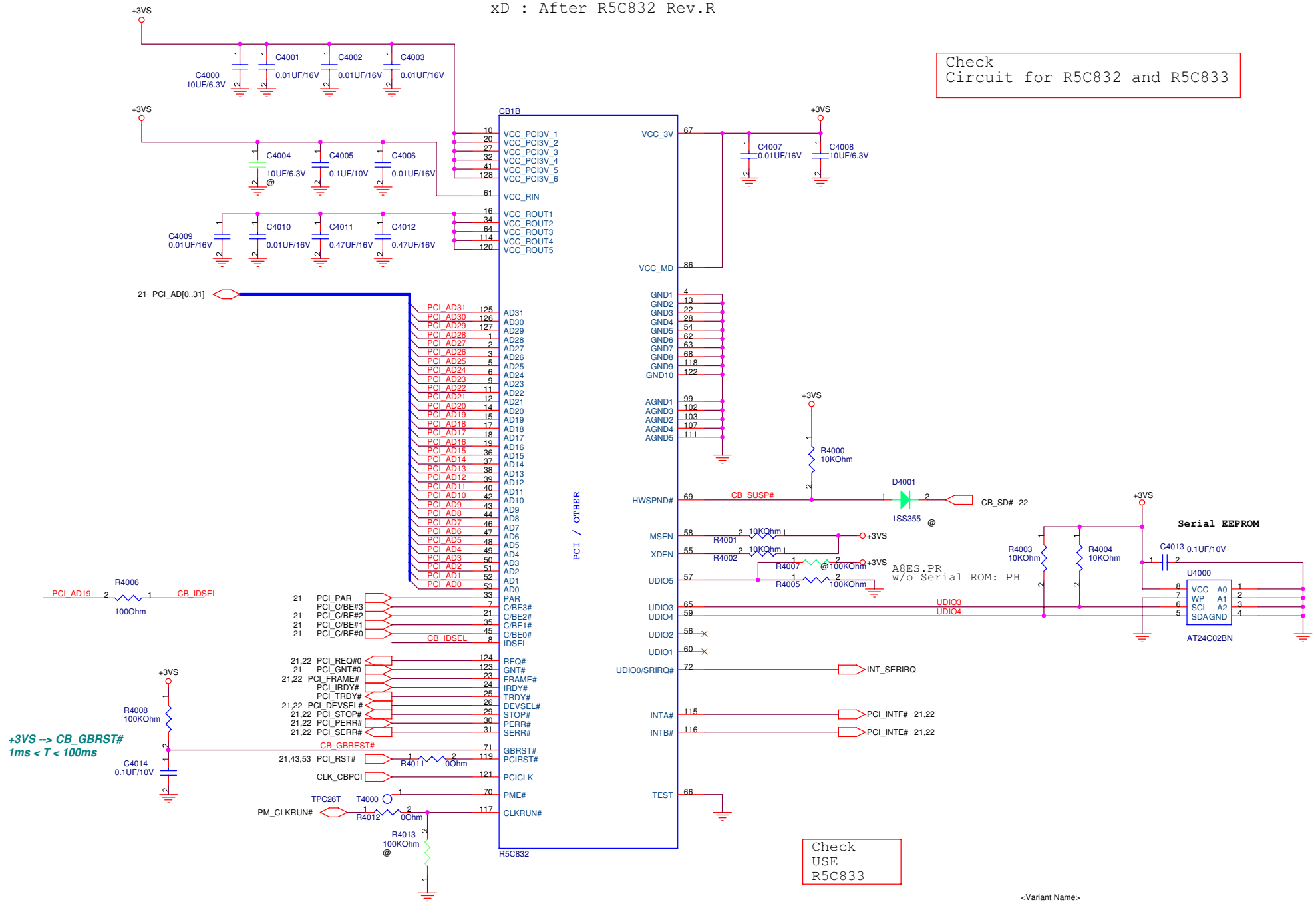


ASUS		Title : AUDIO-MIC	
ASUSTeK COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES		Rev 1.0
Date: 星期二, 三月 06, 2007		Sheet 37 of 94	

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 39 of 94	

Check
Circuit for R5C832 and R5C833

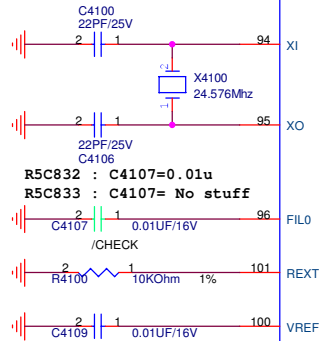


Check
USE
R5C833

<Variant Name>

ASUS		Title : RICOH R5C832/PCI B	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES	Rev 1.0	
Date: 早期三月06, 2007	Sheet 40 of 94		

as close as possible to R5C832

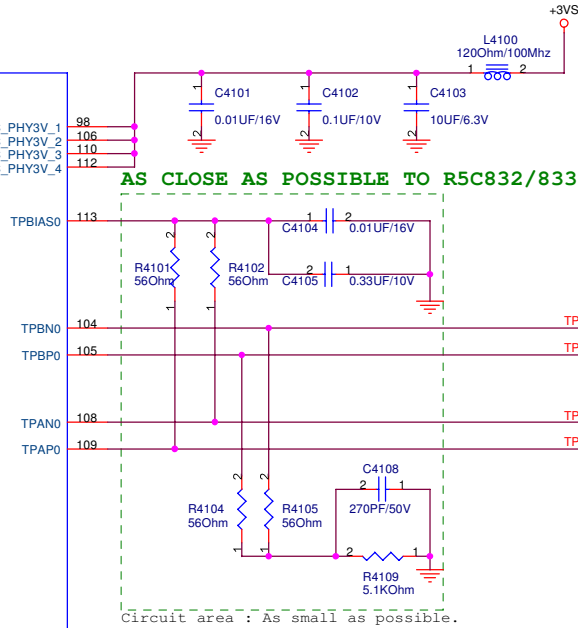


CB1A

IEEE1394/SD

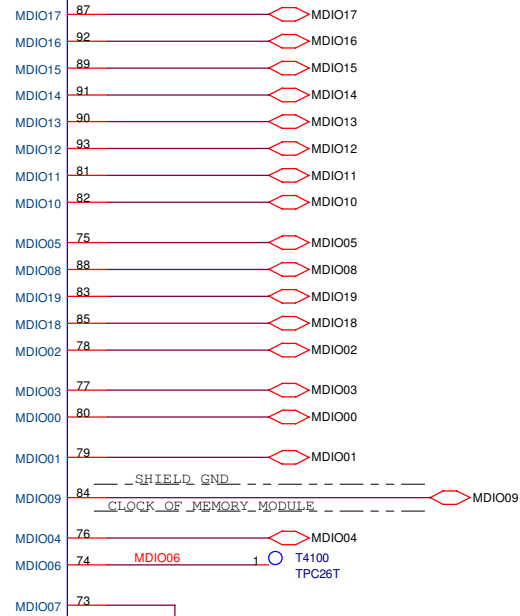
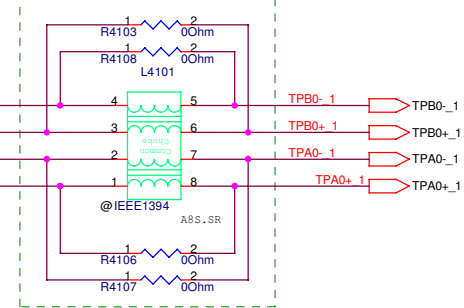
AVCC_PHY3V_1
 AVCC_PHY3V_2
 AVCC_PHY3V_3
 AVCC_PHY3V_4

AS CLOSE AS POSSIBLE TO R5C832/833



Circuit area : As small as possible.

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

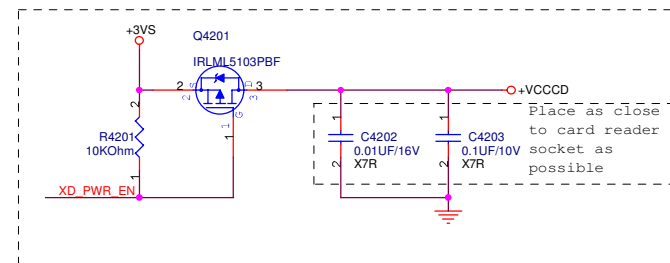


MDIO02--> xDCE#
 MDIO05--> SD Power Control 1 / xDWP
 MDIO06--> xD/MS/SD LED Control
 MDIO14--> xD Data
 MDIO15--> xD Data
 MDIO16--> xD Data
 MDIO17--> xD Data
 MDIO18--> xD CLE
 MDIO19--> xD ALE

MDIO01--> MS Card Detect
 MDIO03--> SD Write Protect
 MDIO04--> SD Card Power0 Control/
 MS Power Control
 MDIO07--> SD External Clock/
 MS External Clock
 MDIO08--> SD Command/MS Bus State
 MDIO09--> SD Clock/MS Clock
 MDIO10--> SD Data 0/MS Data 0
 MDIO11--> SD Data 1/MS Data 1
 MDIO12--> SD Data 2/MS Data 2
 MDIO13--> SD Data 3/MS Data 3

<Variant Name>

ASUS		Title : RICOH R5C832/PCI A	
ASUSTek COMPUTER INC		Engineer:	
Size Custom	Project Name A8ES	Rev 1.0	
Date: 早期	2月06, 2007	Sheet	41 of 94



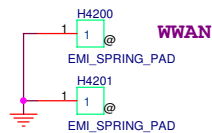
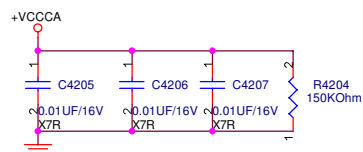
The schematic diagram illustrates the MDIO driver circuit. It features three MDIO lines: MDIO00, MDIO12, and MDIO11. MDIO00 is connected to the drain of MOSFET Q4204 (2N7002K). MDIO12 is connected to the drain of MOSFET Q4203 (2N7002K). MDIO11 is connected to the drain of MOSFET Q4202 (2N7002K). The gates of Q4204 and Q4203 are driven by SDCDAT1, and the gate of Q4202 is driven by SDCDAT2. A 10KOhm resistor (R4202) is connected between MDIO12 and MDIO11. The source of Q4204 is connected to ground. The sources of Q4203 and Q4202 are connected to a common node that is pulled up to +12V.

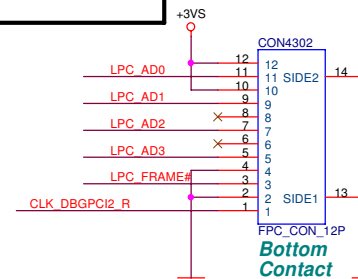
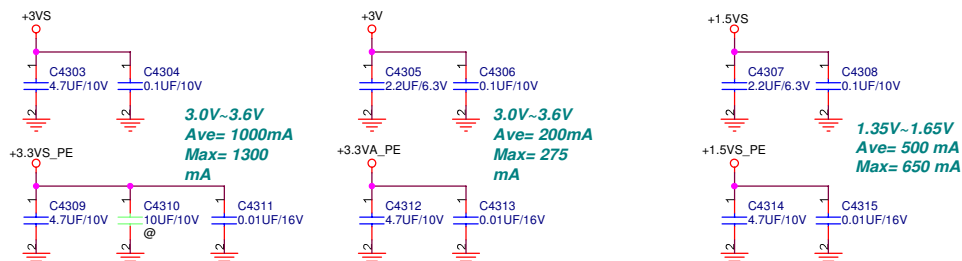
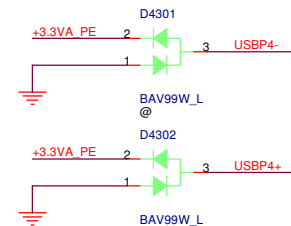
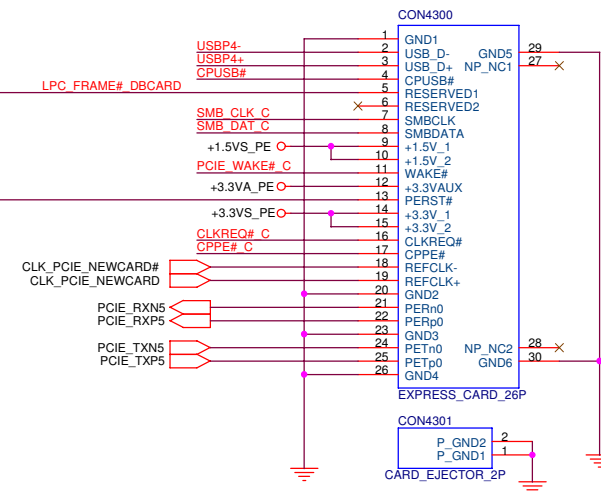
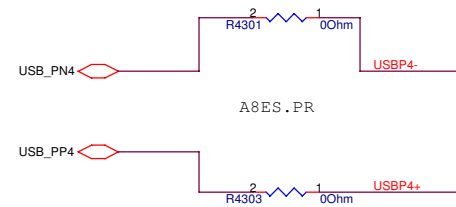
```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
           MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```


The schematic diagram illustrates the electrical connections for the SD card interface and WWAN module on the ESP8266 module. The SD card interface is implemented using a 4IN1CN1 SD card connector, which is connected to the SD_CARD_38P header. The SD card's pins are connected to the module's pins as follows:

- SD Card Pins:**
 - NP_NC2 (Pin 2): Connected to S9 (SDCARD2), S1 (MDIO13), S2 (MDIO08), S3 (M10), M9 (M8), M7 (MDIO13), M6 (Reserved1), M5 (Reserved2), M4 (MDIO12), M3 (MDIO10), M2 (MDIO08), M1 (MDIO09), S4 (MDIO09), S5 (MDIO10), S6 (SDCARD1), S7 (MDIO09), S8 (MDIO00).
 - NP_NC1 (Pin 1): Connected to SD_CARD_38P pin 1.
- Module Pins:**
 - SD_CARD_38P: Pins 1 through 6.
 - CD_SW: Connected to pin 3.
 - COMMON: Connected to pin 4.
 - WP_SW: Connected to pin 5.
 - GND3: Connected to pin 6.
- Power and Grounding:**
 - VCCCA: Connected to the module's VCC pin.
 - GND1: Connected to the module's GND pin.
 - GND2: Connected to the module's GND pin.
 - GND3: Connected to the module's GND pin.
 - VCC3: Connected to the module's VCC pin.
- WWAN Module:**
 - The WWAN module is connected to the module's pins via a 4200 pin header.
 - The WWAN module's pins are connected to the module's pins as follows:
 - Pin 1: Connected to the module's pin 1.
 - Pin 2: Connected to the module's pin 2.
 - Pin 3: Connected to the module's pin 3.
 - Pin 4: Connected to the module's pin 4.
 - Pin 5: Connected to the module's pin 5.
 - Pin 6: Connected to the module's pin 6.
 - Pin 7: Connected to the module's pin 7.
 - Pin 8: Connected to the module's pin 8.
 - Pin 9: Connected to the module's pin 9.
 - Pin 10: Connected to the module's pin 10.
 - Pin 11: Connected to the module's pin 11.
 - Pin 12: Connected to the module's pin 12.
 - Pin 13: Connected to the module's pin 13.
 - Pin 14: Connected to the module's pin 14.
 - Pin 15: Connected to the module's pin 15.
 - Pin 16: Connected to the module's pin 16.
 - Pin 17: Connected to the module's pin 17.
 - Pin 18: Connected to the module's pin 18.

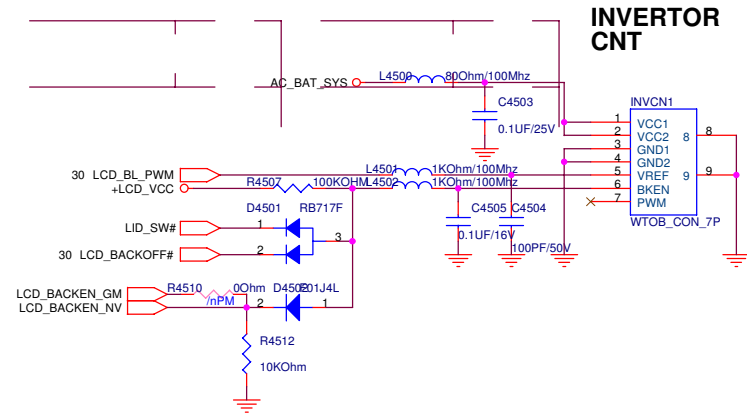
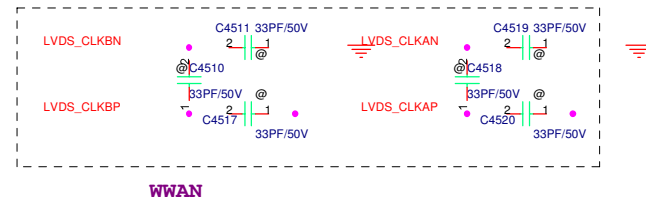
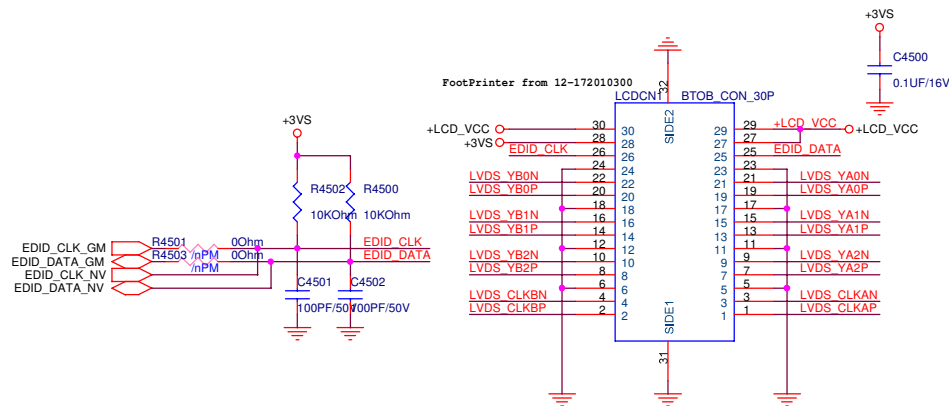
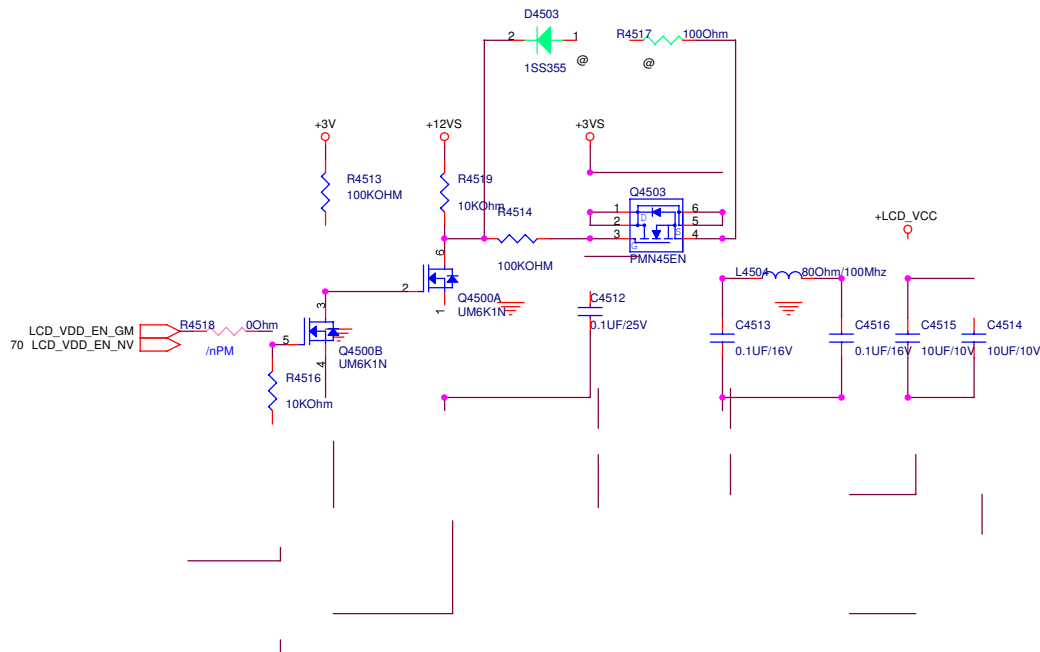
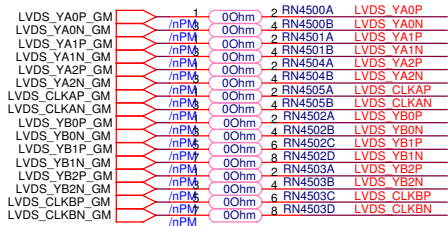
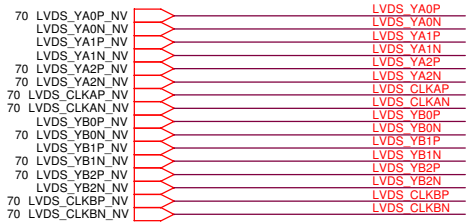
```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```



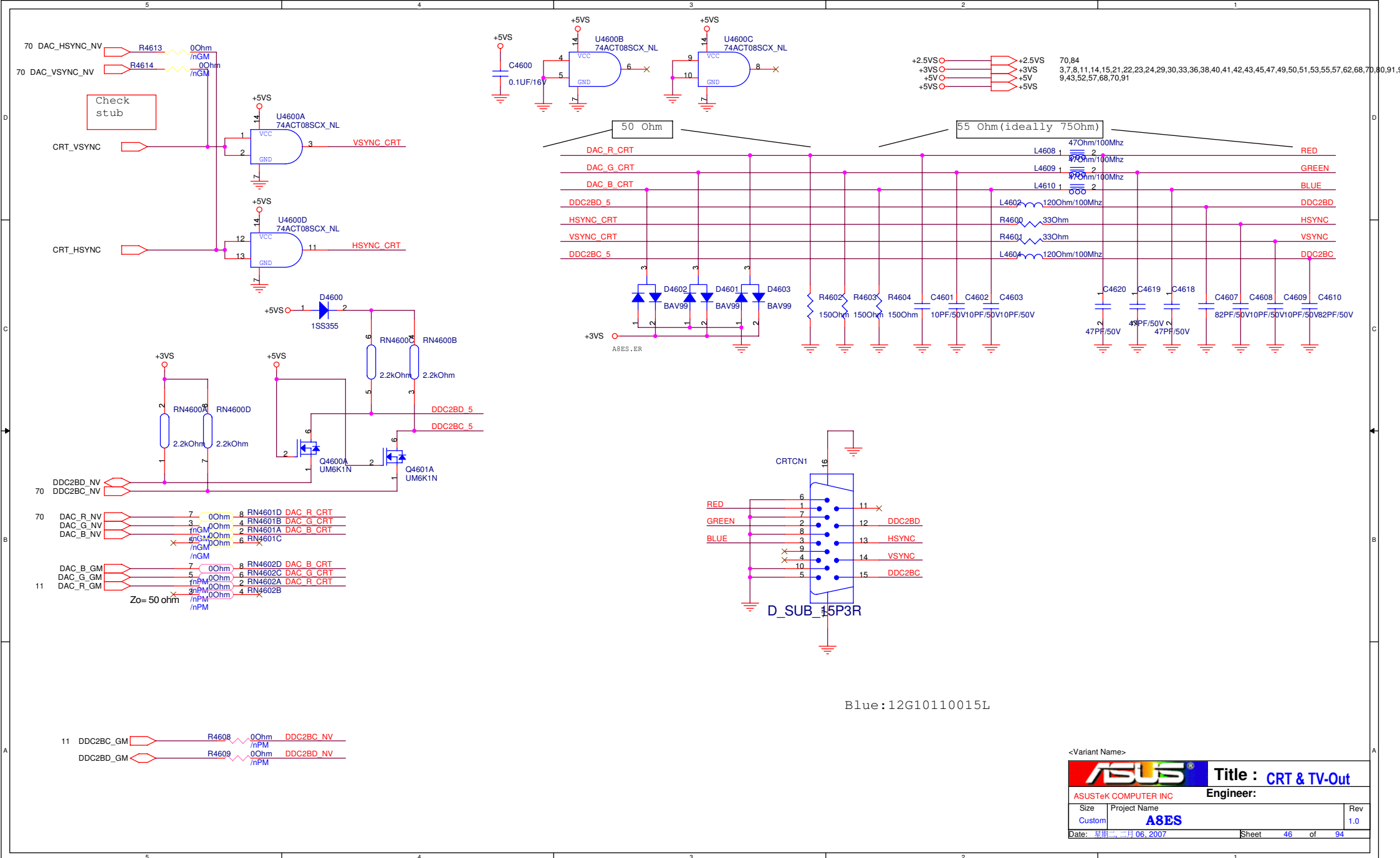


	5	4	3	2	1									
D														
C														
B														
A	<div><div></div><div><div>Title : Blank</div><div>Engineer:</div></div></div> <table><tr><td>Size</td><td>Project Name</td><td>Rev</td></tr><tr><td>A</td><td>A8ES</td><td>1.0</td></tr><tr><td colspan="2">Date: 星期三, 十月 11, 2006</td><td>Sheet 44 of 94</td></tr></table>					Size	Project Name	Rev	A	A8ES	1.0	Date: 星期三, 十月 11, 2006		Sheet 44 of 94
Size	Project Name	Rev												
A	A8ES	1.0												
Date: 星期三, 十月 11, 2006		Sheet 44 of 94												
	5	4	3	2	1									

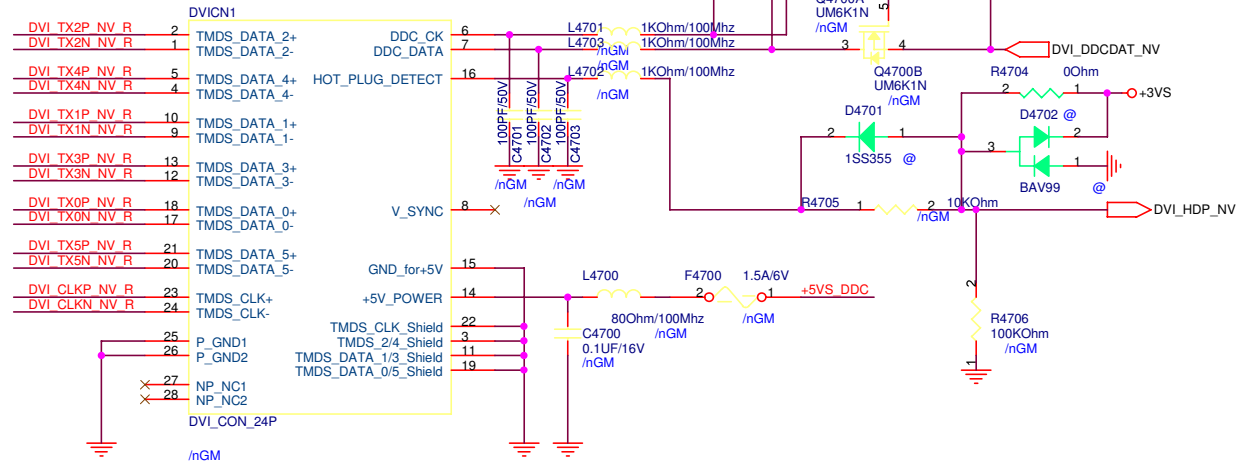
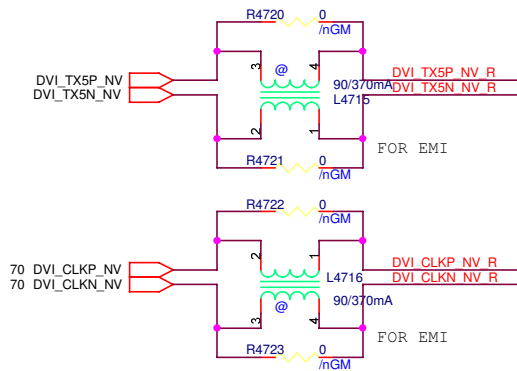
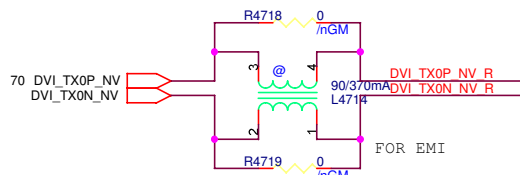
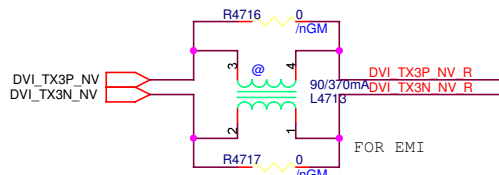
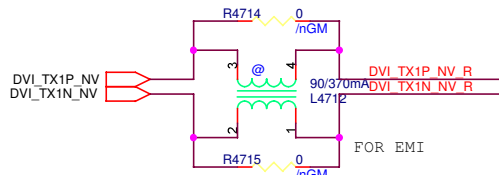
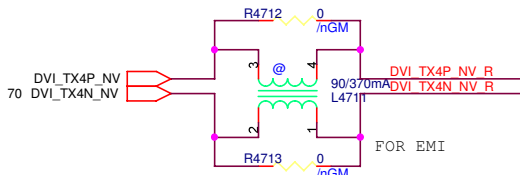
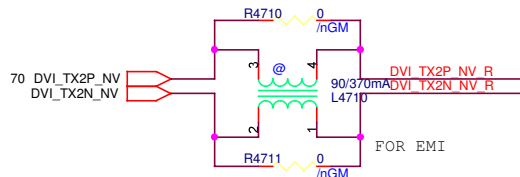
Check stub



<Variant Name>



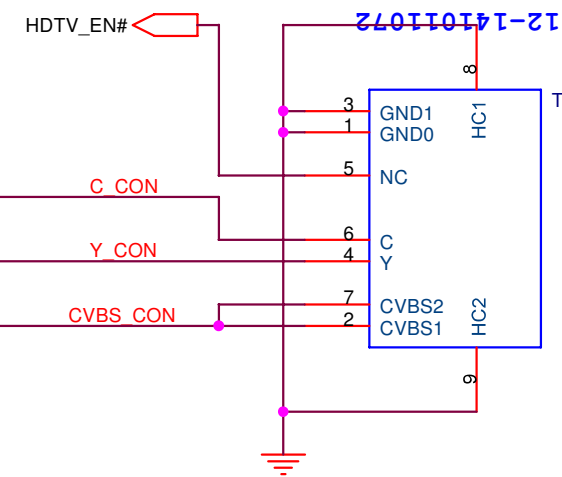
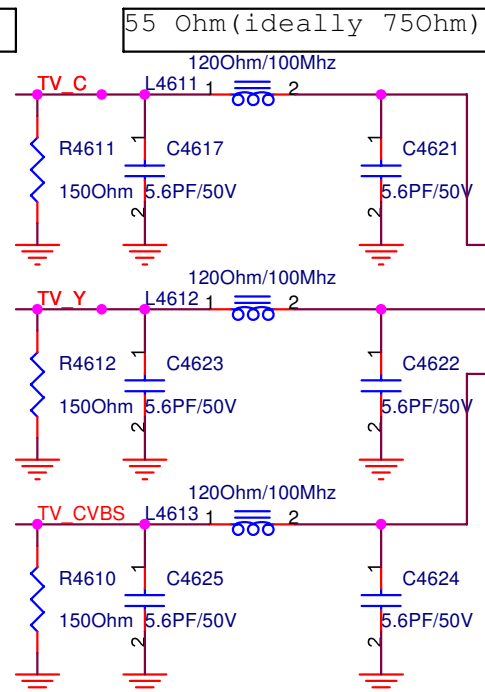
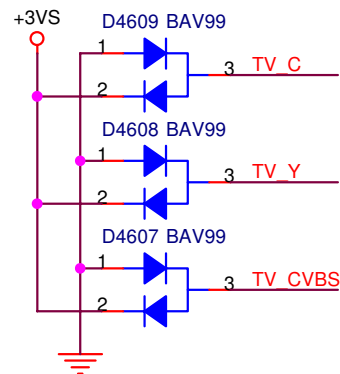
Add DVI Choke 09G092145000 for EMI



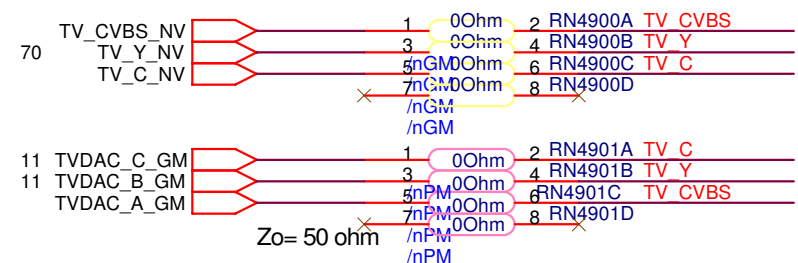
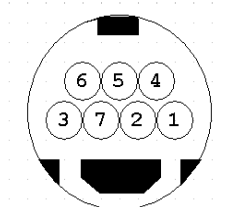
+5VS +5VS

	5	4	3	2	1
D					
C					
B					
A					

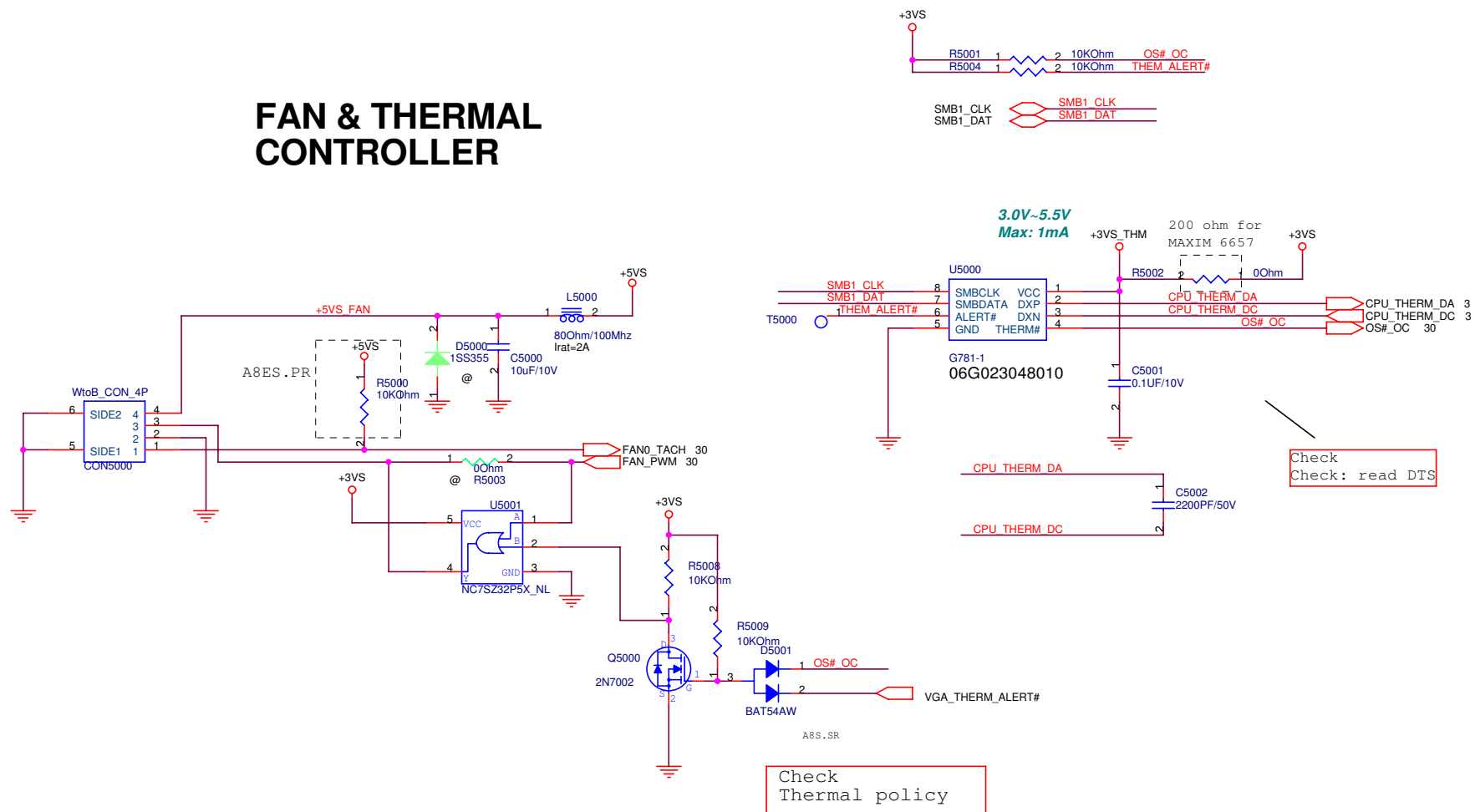
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 48 of 94	



TVSCN1
MINI_DIN_7P
12G141011077



FAN & THERMAL CONTROLLER



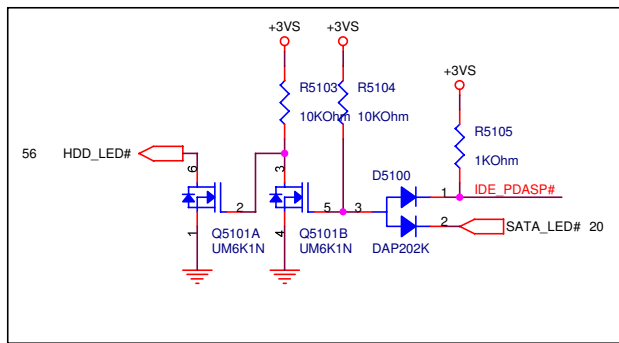
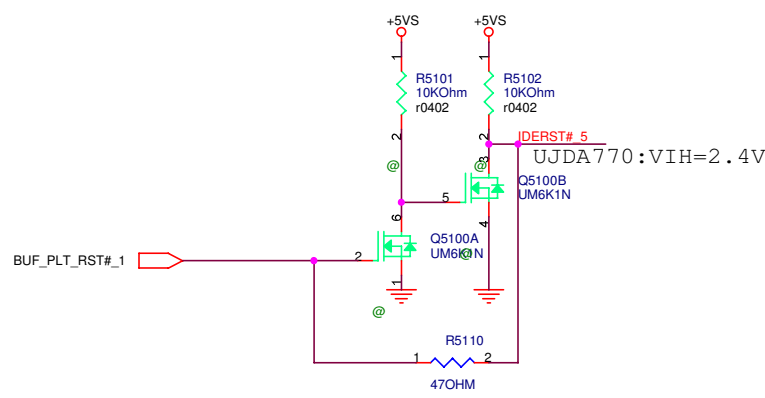
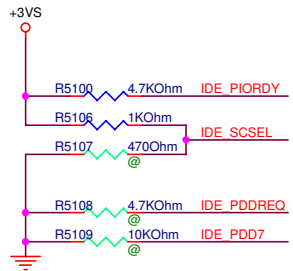
Check
Thermal policy

Check
Check: read DTS

G781-1 (0x9A)
06G023048010
G781 (0x98)
06G023048011

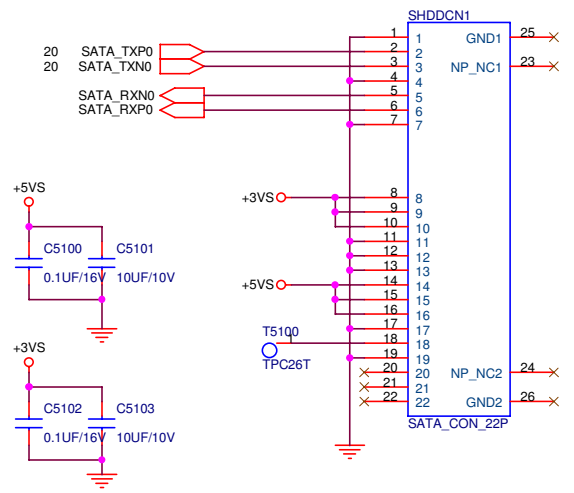
<Variant Name>

ASUS		Title : FAN & THERMAL	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES	Rev 1.0	
Date: 星期二, 三月 06, 2007		Sheet 50 of 94	



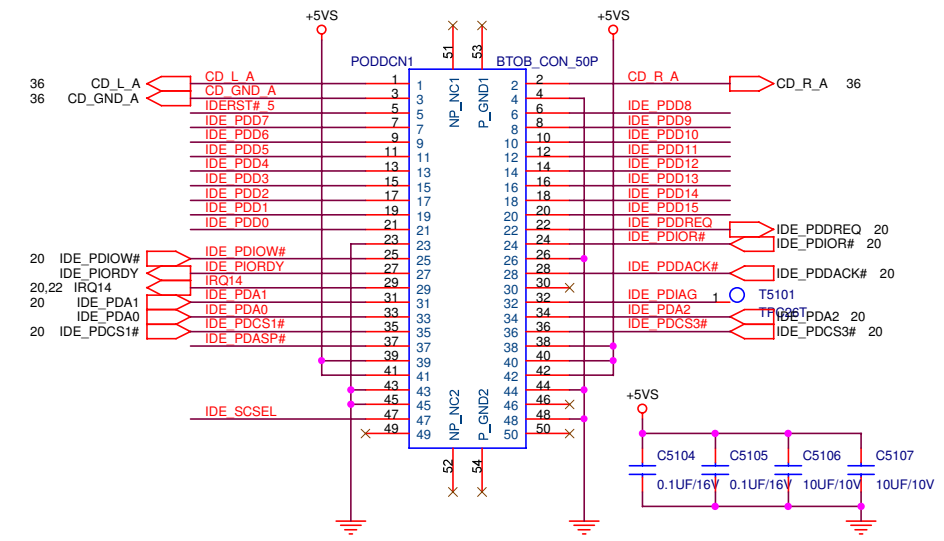
20 IDE_PDD[0..15] IDE_PDD[0..15]

SATA HDD CON



+3VS +3VS 3,7,8,11,14,15,21,22,23,24,29,30,33,36,38,40,41,42,43,45,46,47,49,50,53,55,57,62,68,70,80,91,92
 +5VS +5VS 9,43,52,57,68,70,91
 +5V +5V

PATA CD-ROM CON

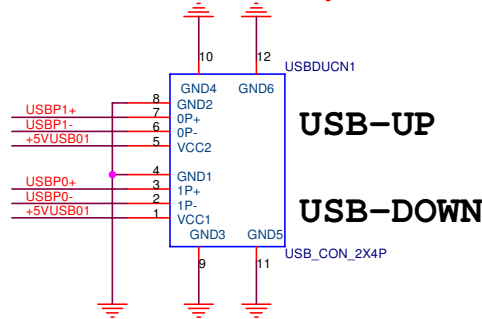
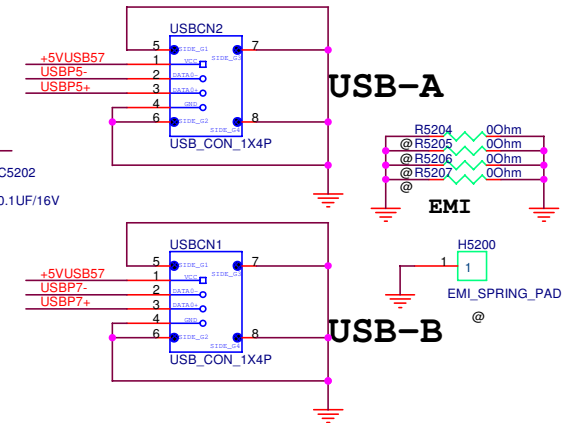
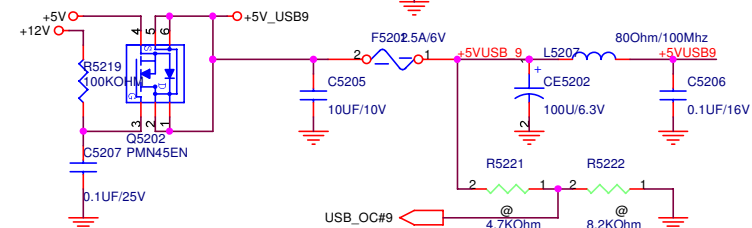
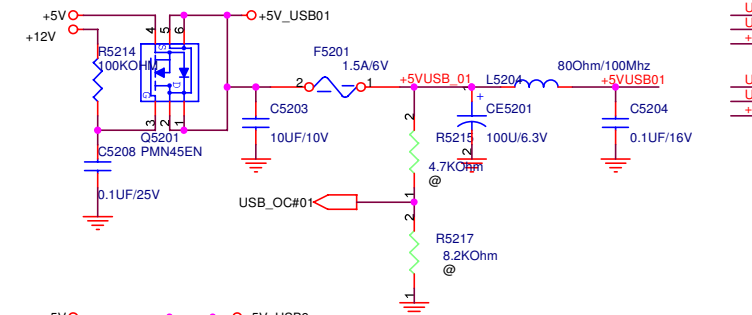
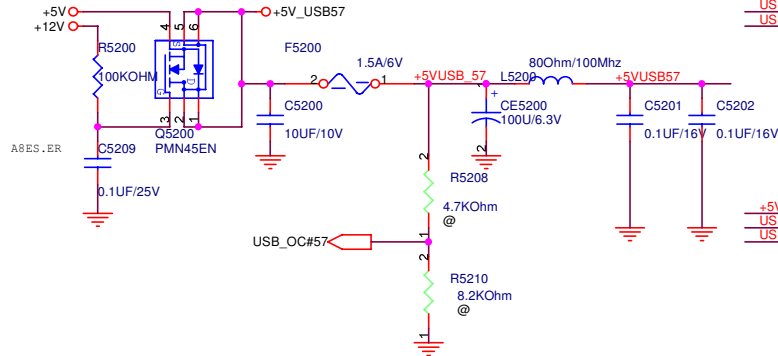
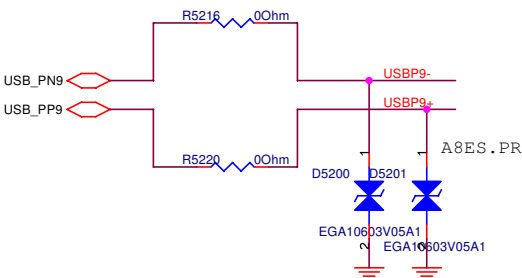
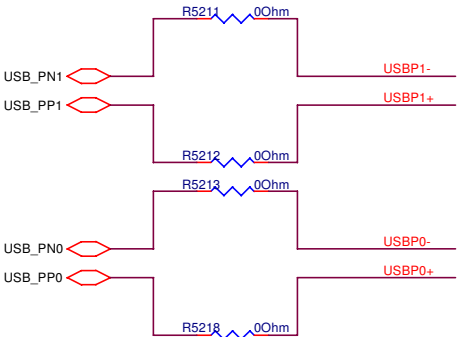
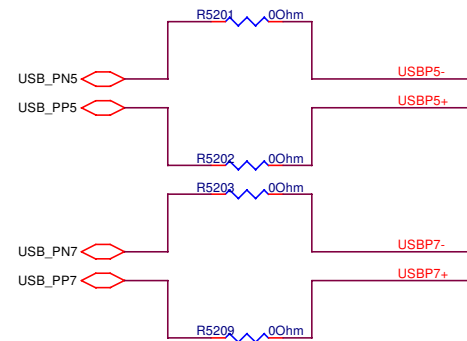
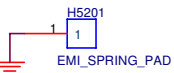


ASUS		Title : HDD & ODD	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	A8ES	1.0	
Date: 星期 三月 06, 2007	Sheet 51	of 94	

A8ES.PR

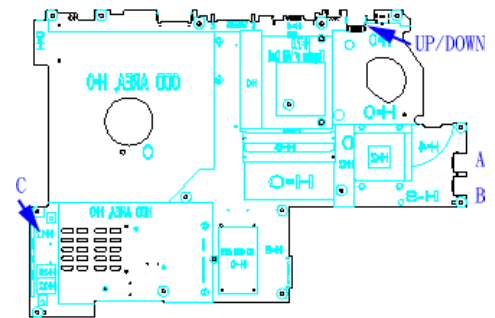
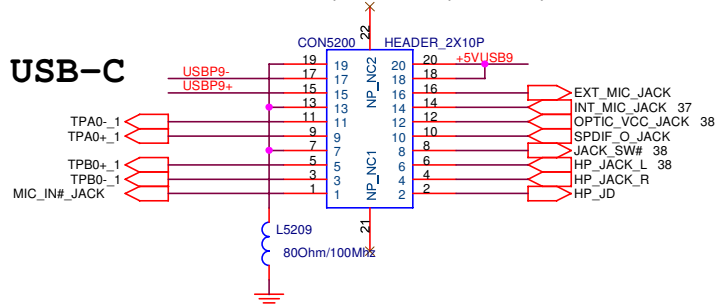
Remove USB
common
choke
co-lay

A8ES.PR EMI



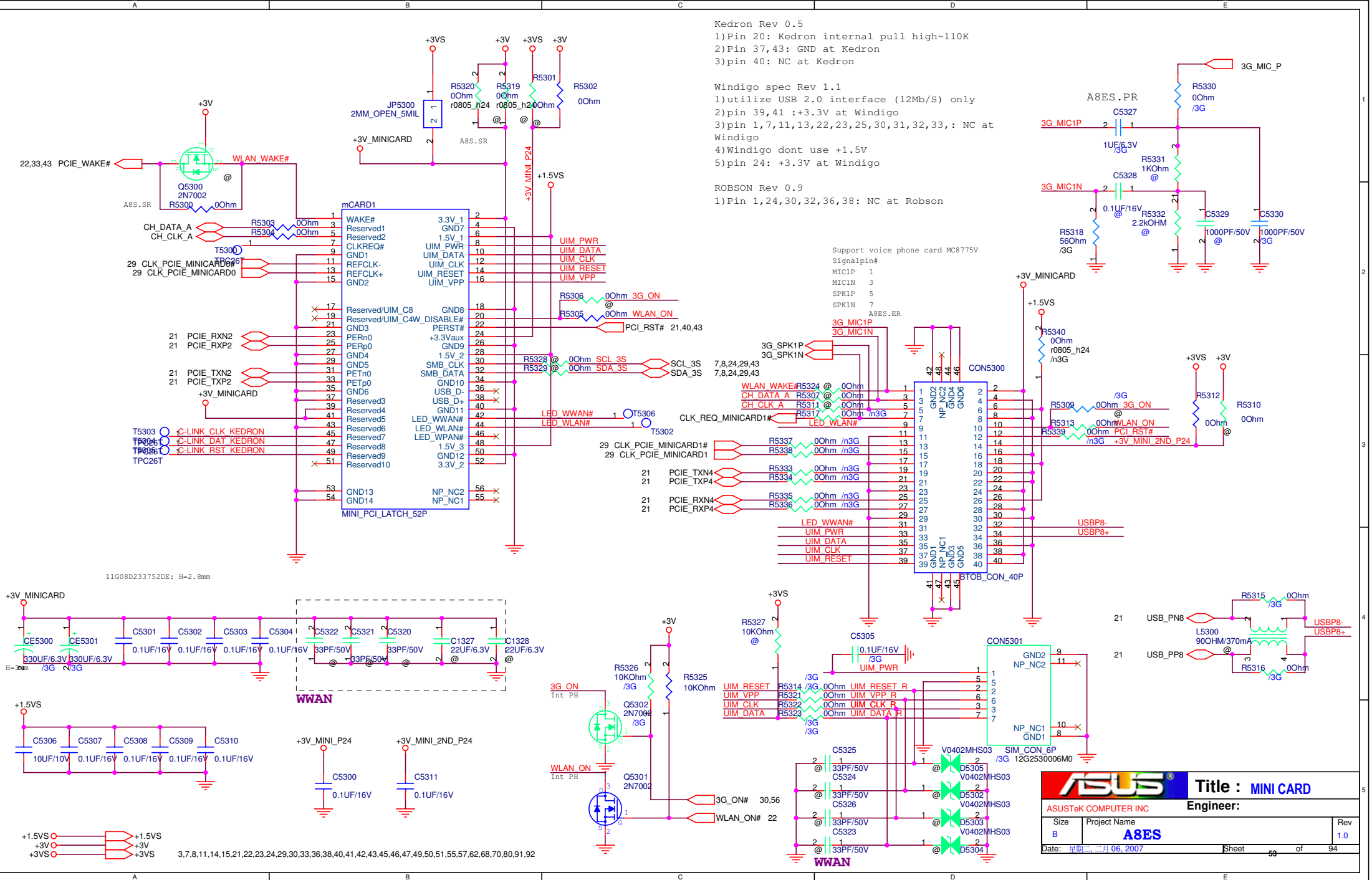
+5V 9,43,57,68,70,91

SUB-PCB: USB/1394/MIC/EARPHONE



<Variant Name>

ASUS		Title : USB/SUB PCB	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8ES	1.0	
Date: 2007.06.06	Sheet 52	of 94	




Kedron Rev 0.5
1)Pin 20: Kedron internal pull high~110K
2)Pin 37,43: GND at Kedron
3)pin 40: NC at Kedron

Windigo spec Rev 1.1
1)utilize USB 2.0 interface (12Mb/S) only
2)pin 39,41 :+3.3V at Windigo
3)pin 1,7,11,13,22,23,25,30,31,32,33,: NC at Windigo
4)Windigo dont use +1.5V
5)pin 24: +3.3V at Windigo

ROBSON Rev 0.9
1)Pin 1,24,30,32,36,38: NC at Robson


Support voice phone card MC8775V
Signalpin#
MIC1P 1
MIC1N 3
SPK1P 5
SPK1N 7
A8ES.ER

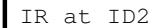
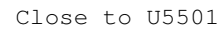
**Title : MINI CARD**

ASUSTek COMPUTER INC **Engineer:**

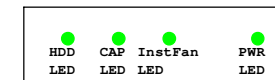
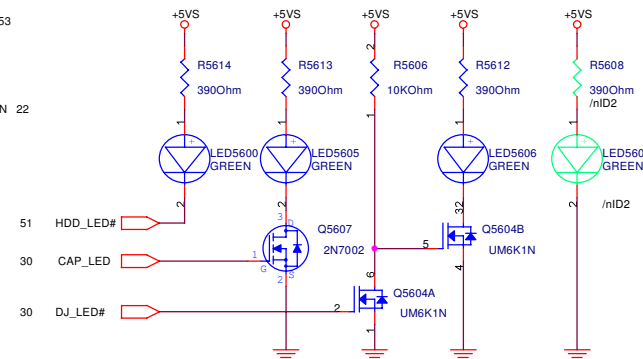
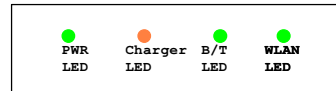
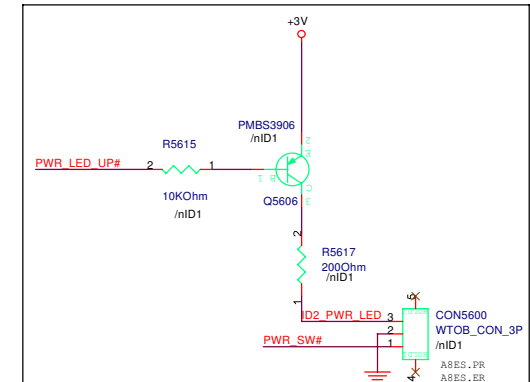
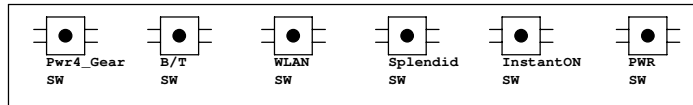
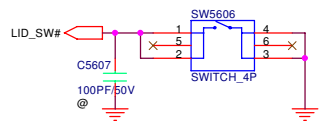
Size B	Project Name A8ES	Rev 1.0
Date: 星期日, 三月 06, 2007		Sheet 59 of 94

5	4	3	2	1
D				
C				
B				
A				
5	4	3	2	1

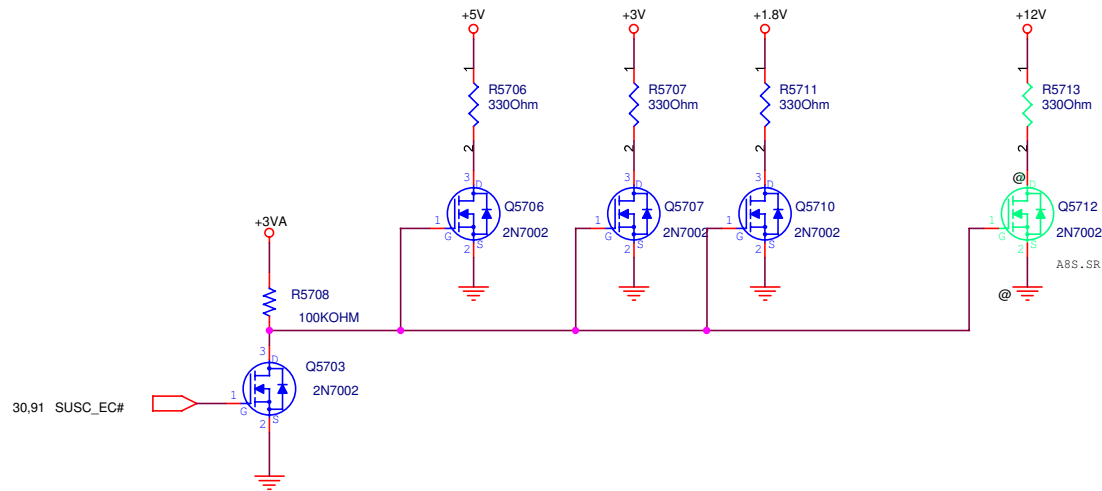
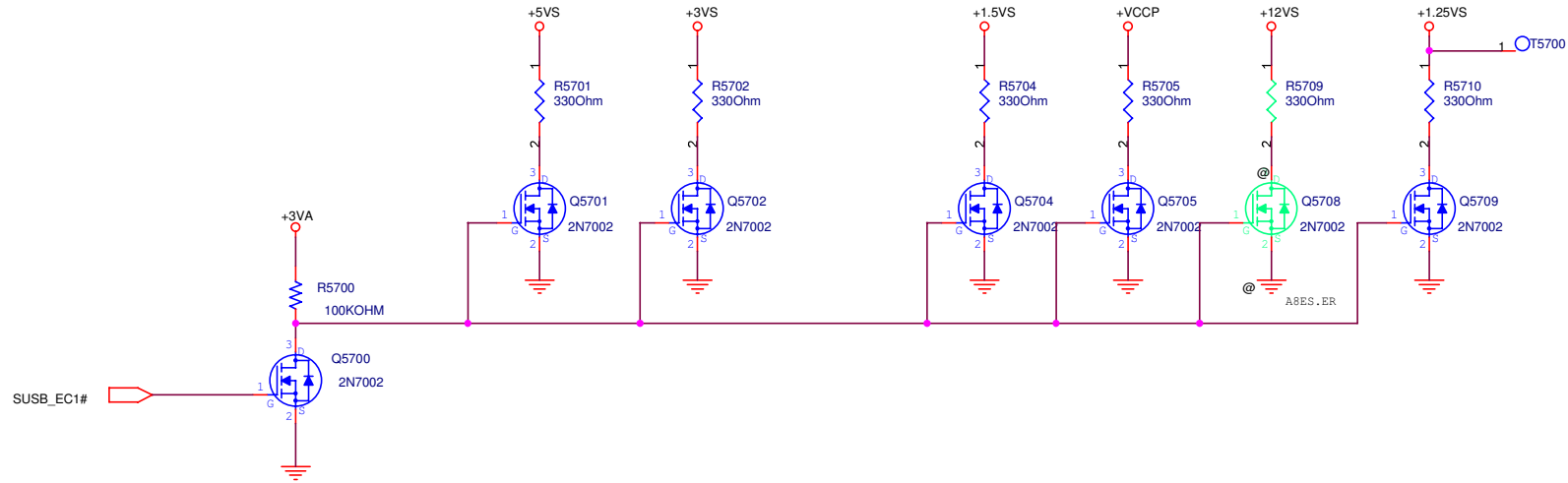
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	ABES	0	
Date: 2006. 1 月 11, 2006		Sheet 54 of 94	



Sheet 55 of 94



Discharge Circuit




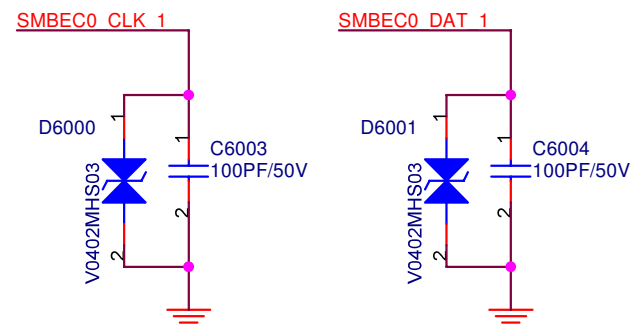
<Variant Name>


ASUS		Title : Discharge	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES		Rev 1.0
Date: 星期二, 二月 06, 2007	Sheet 57	of 94	

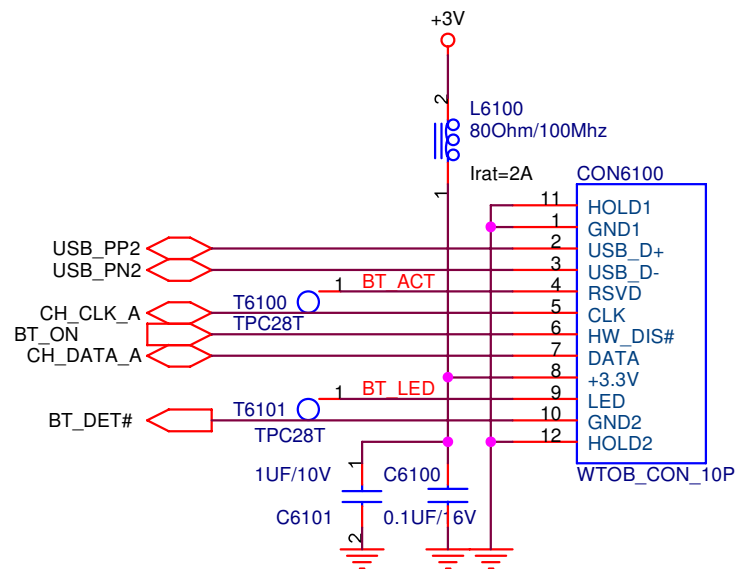
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

<Variant Name>

		Title :	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: 星期三, 十月 11, 2006		Sheet	of 94



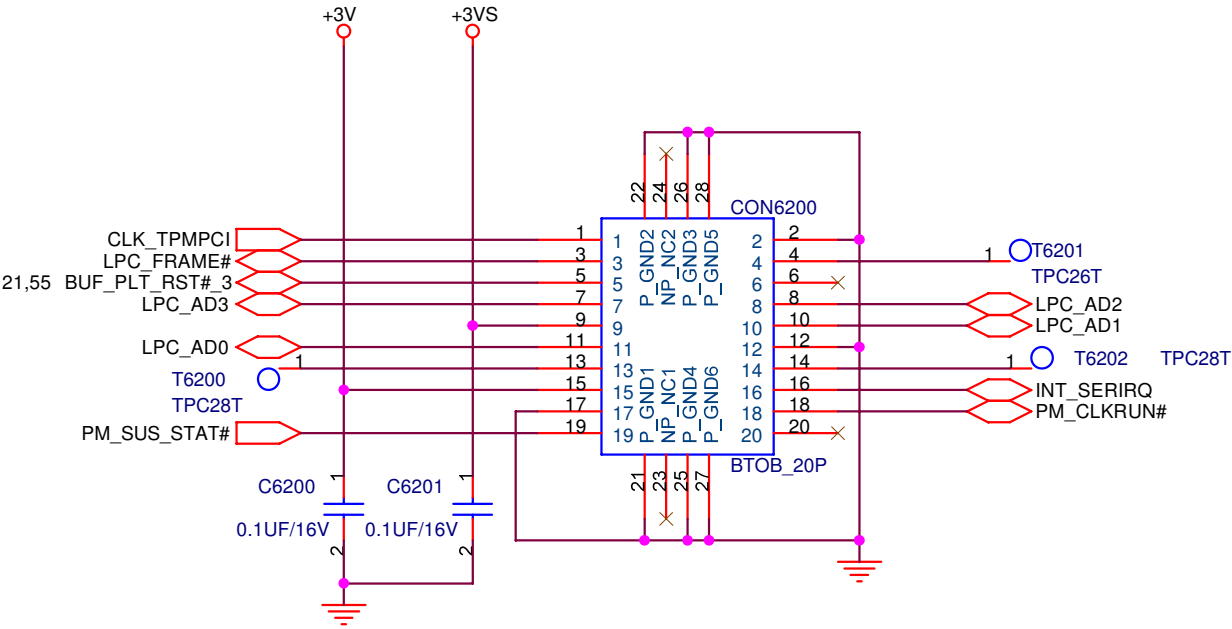
		Title : DC IN / BAT	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES	Rev 1.0	
Date: 星期二, 三月 06, 2007		Sheet of 94	




Bluetooth Module CON

ASUS		Title :BT/CAMERA	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		1.0
Date: 星期二, 二月 06, 2007		Sheet	61 of 94


TPM 1.2 Module



<Variant Name>

		Title :TPM	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8ES		1.0
Date: 星期二, 二月 06, 2007		Sheet	62 of 94

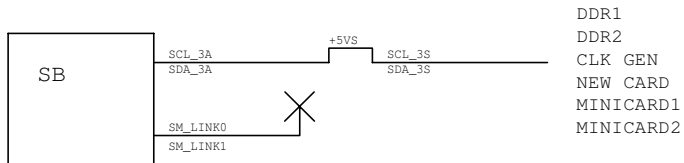
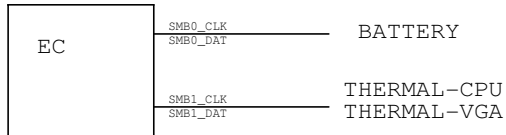
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 63 of 94	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARDBUS	AD19	0	F,E

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0 (low)	
SPD/TS	A0/30
SO-DIMM 1(high)	
SPD/TS	A4/34
G781-1	9A
G781(VGA board)	98

Thermal Sensor (CPU)
SM-Bus Mapping 1001100



BOM option

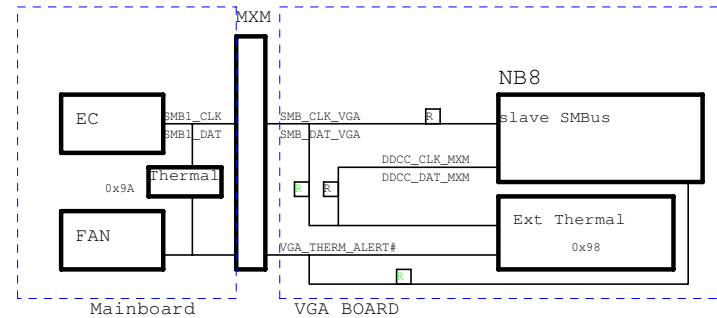
nGM:yellow
nPM:light red

=====
@ : no stuff for all
nGM :no stuff for A8E
nPM :no stuff for A8S
nGM1:no stuff for A8E, A8E/SR mount for debugging A8S in advance
3G :for Windigo,SIERRA MC8775V
nA8E :no stuff Irda for A8E

Support ID2:

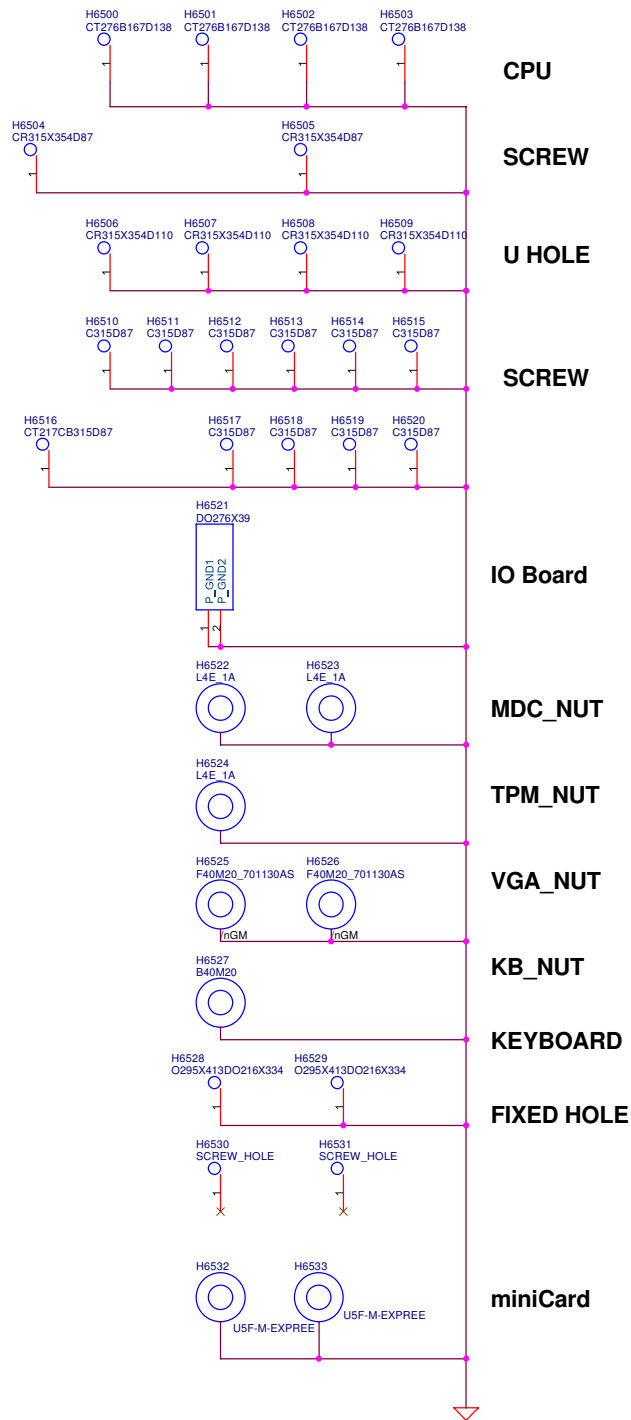
Support ID2:
page 68,Finger print
page 55,IR
Page 56,pwr switch and LED

Thermal block diagram




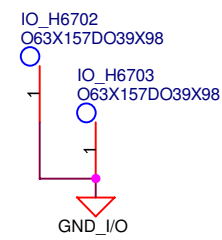
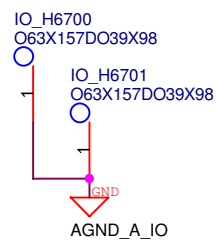
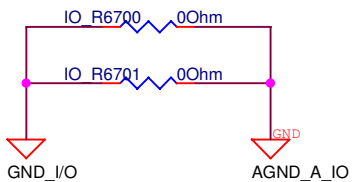
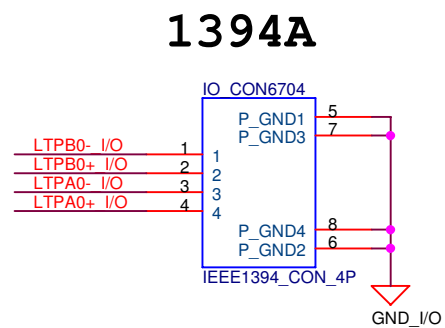
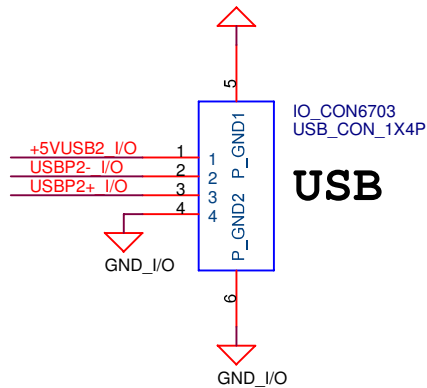
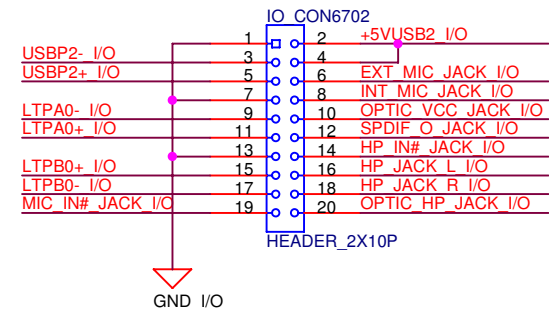
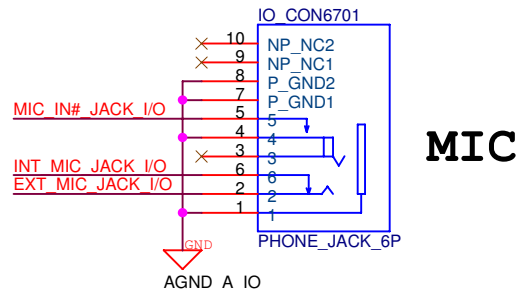
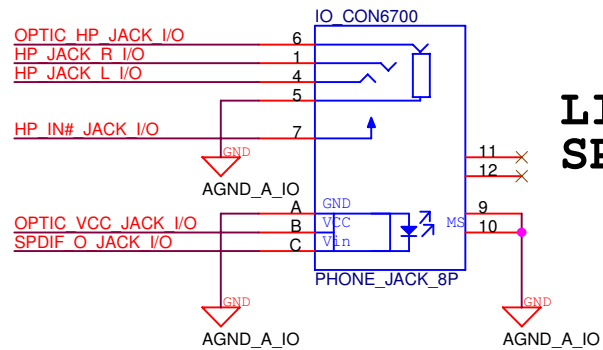
<Variant Name>

ASUS		Title :	
ASUSTeK COMPUTER INC		Engineer:	
Size B	Project Name A8ES	Rev 1.0	
Date: 星期二, 三月 06, 2007		Sheet	64 of 94



Title		
<Title>		
Size	Document Number	Rev
CustomW2S		1.1
Date:	星期二, 十二月 26, 2006	Sheet 65 of 94

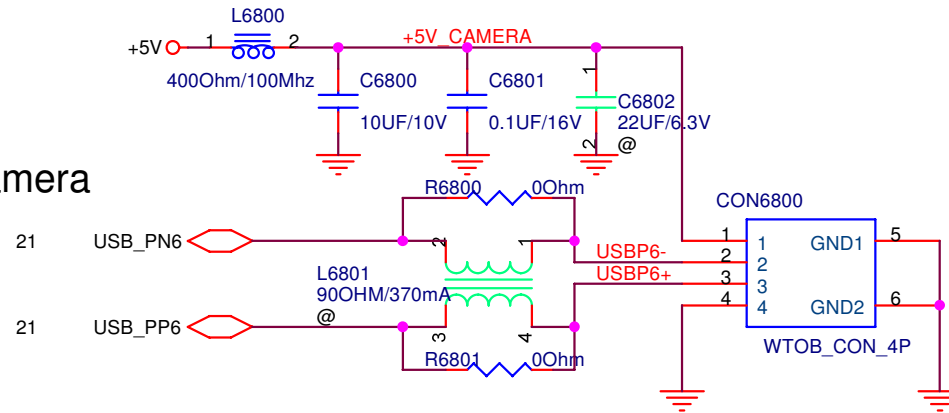
		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	A8ES	0	
Date: 星期三, 十月 11, 2006		Sheet	66 of 94



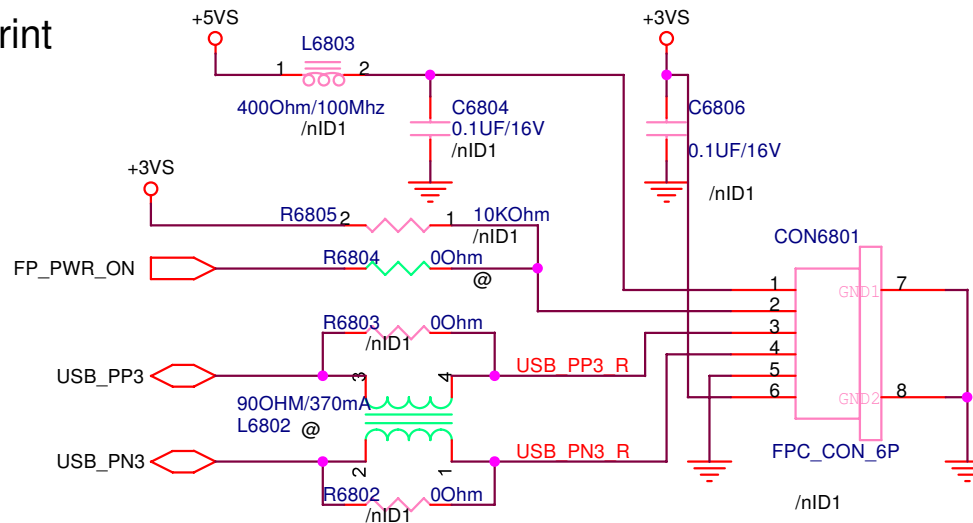
<Variant Name>

ASUS		Title :SUB_PCB	
ASUSTeK COMPUTER INC		Engineer:	
Size A4	Project Name A8ES		Rev 1.0
Date: 星期二, 一月 30, 2007		Sheet	67 of 94

Camera



Finger Print

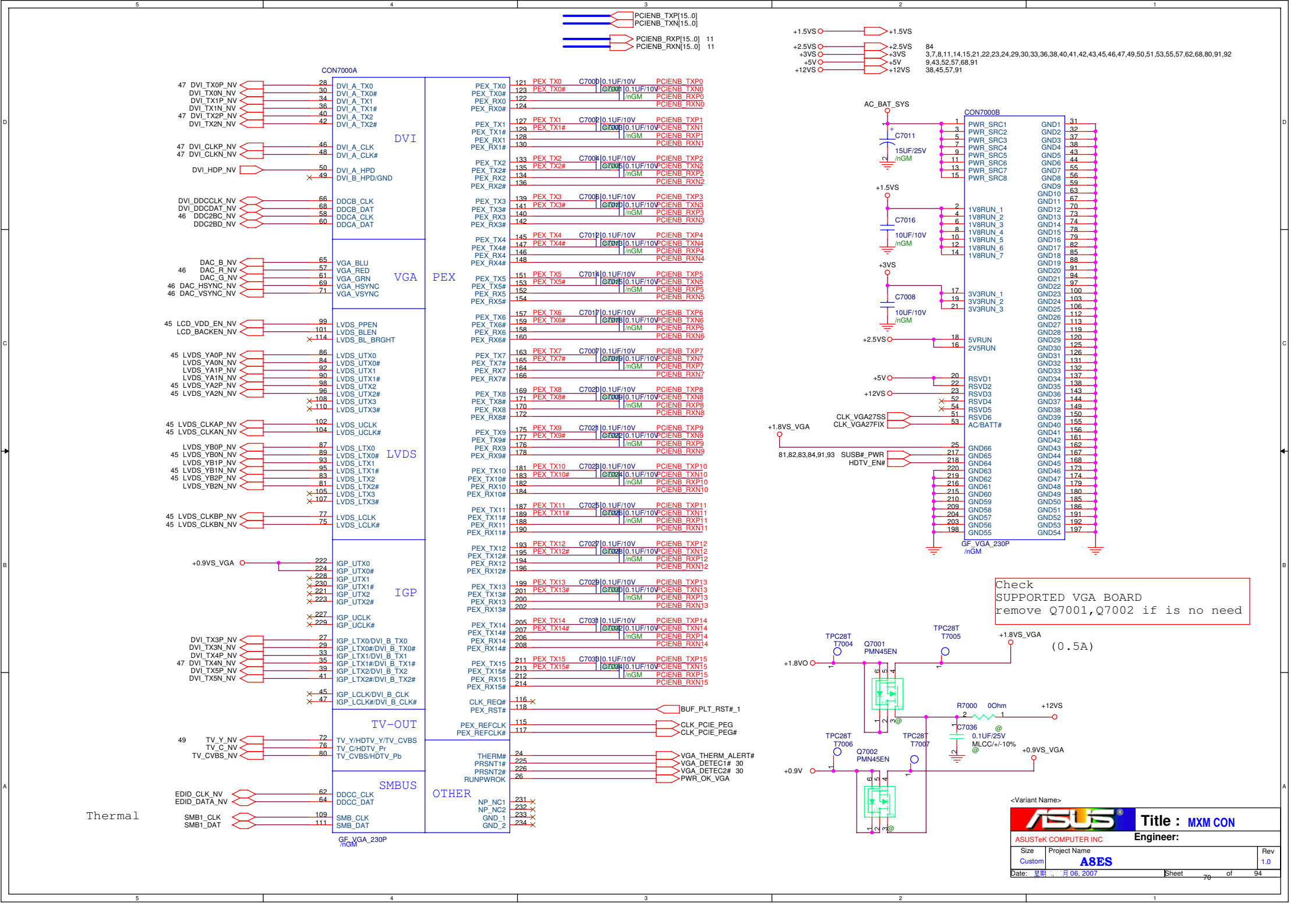


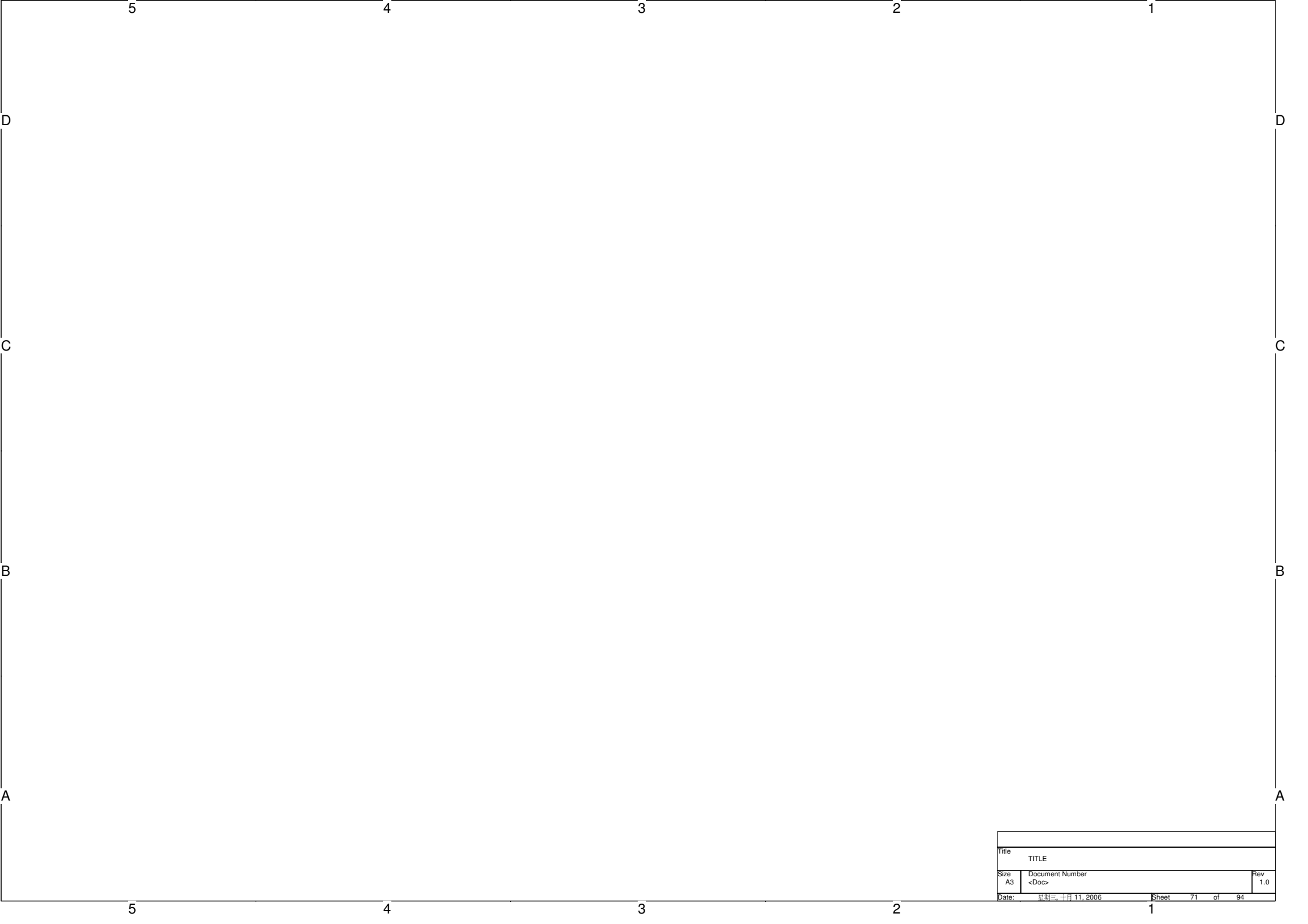
<Variant Name>

ASUS		Title :CAMERA/FingerPrinter	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 1.0
Date: 星期二, 二月 06, 2007		Sheet 60	of 94

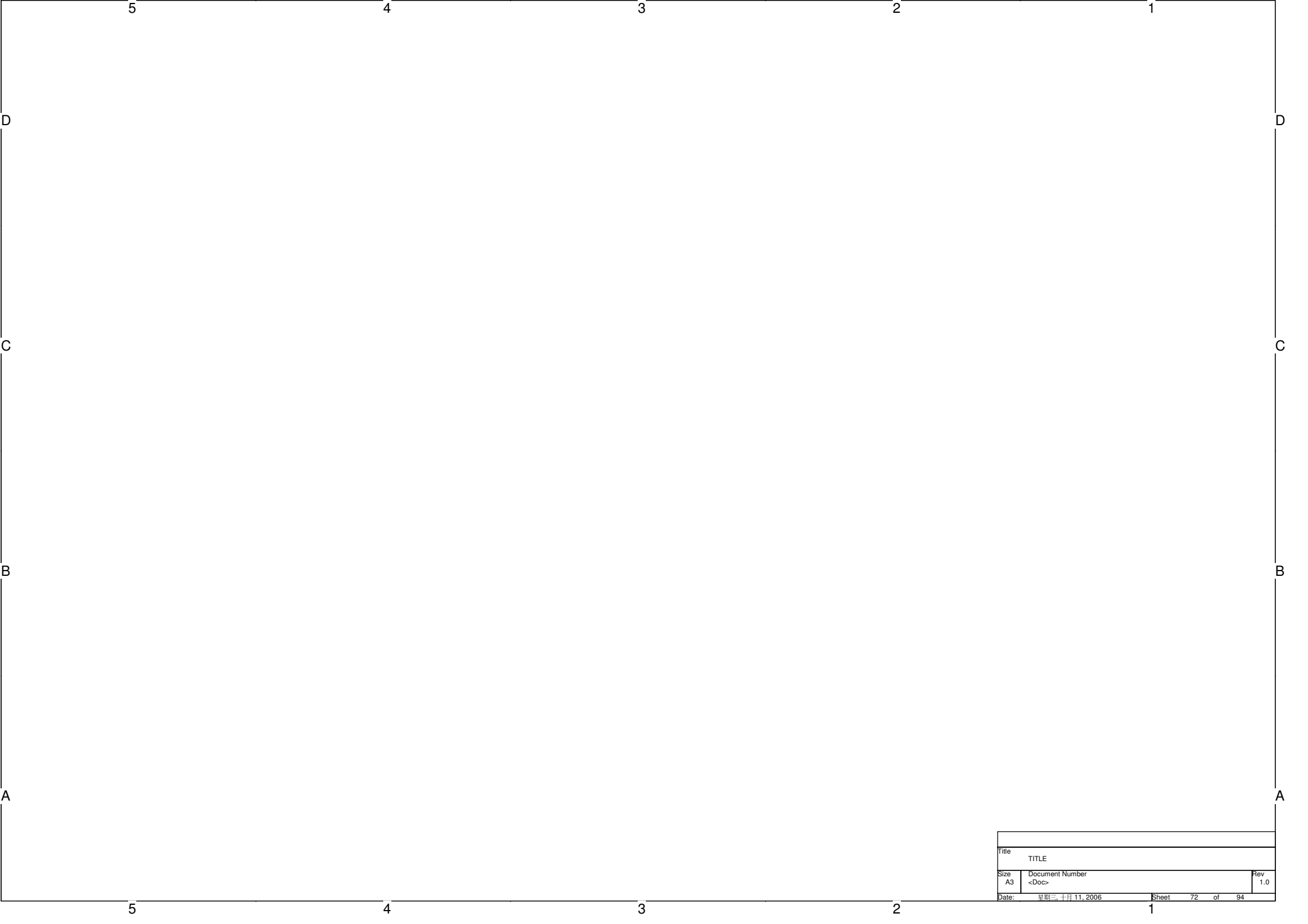
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8ES		Rev 0
Date: 星期三, 十月 11, 2006		Sheet 69 of 94	

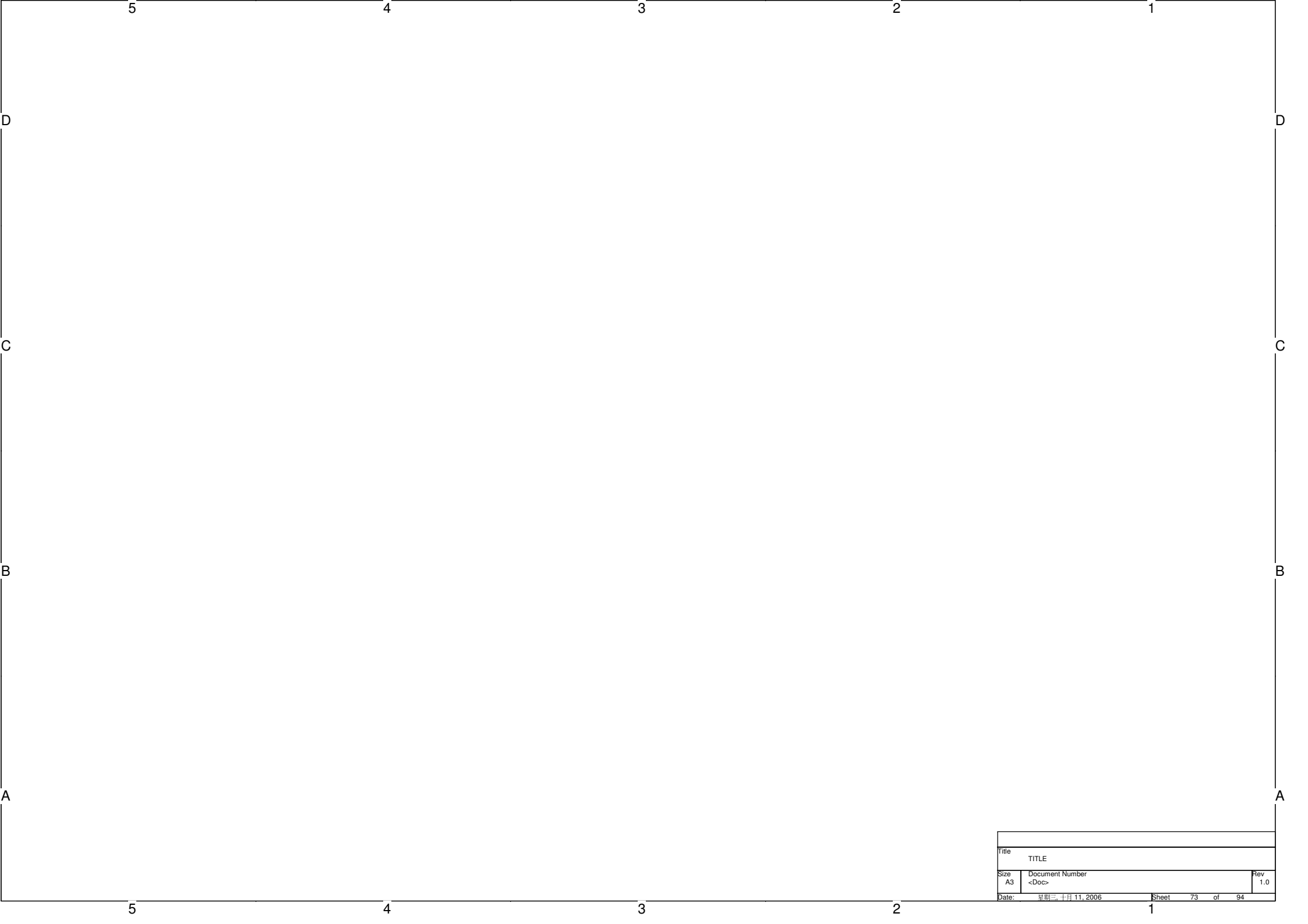




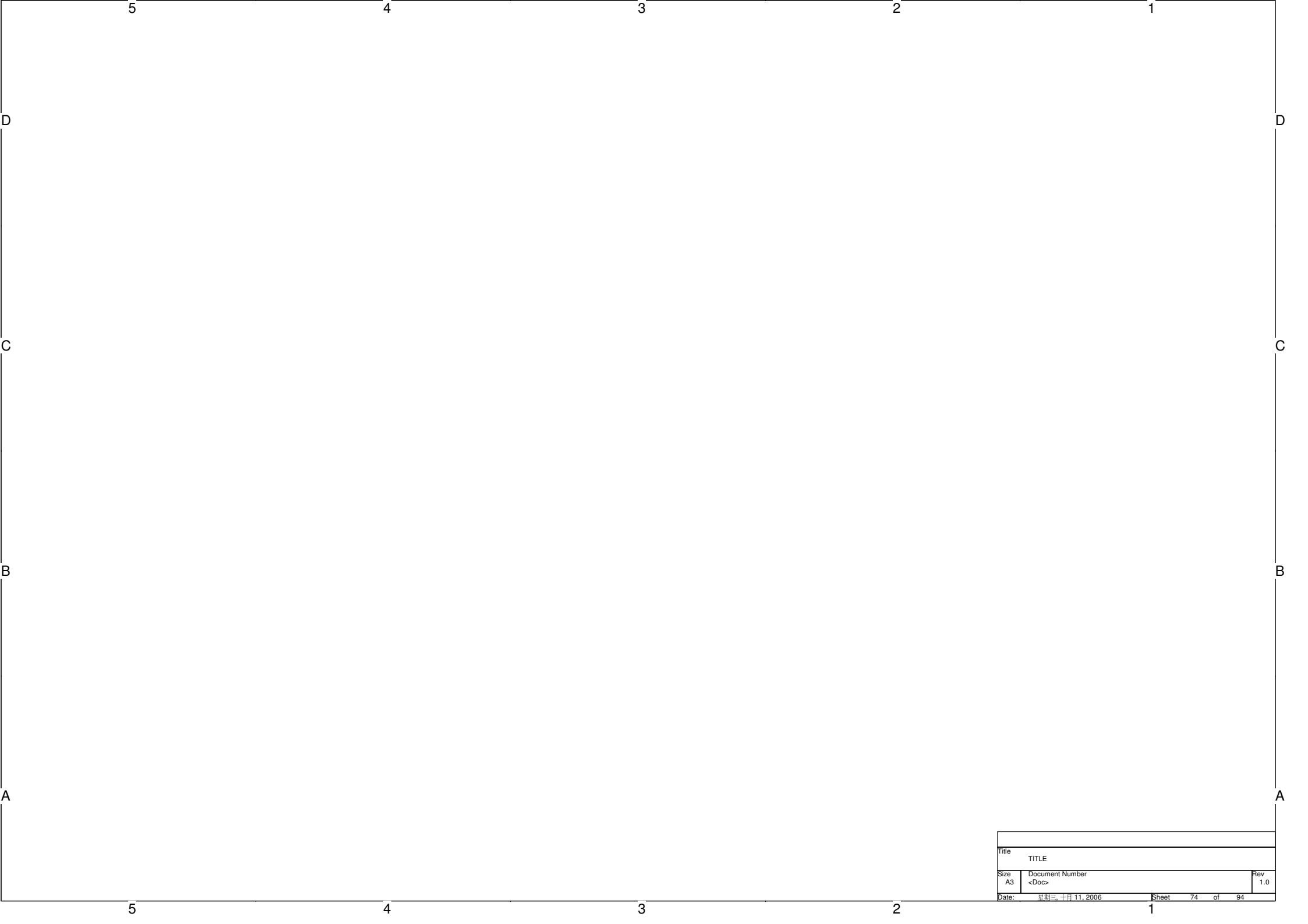
Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date: 星期二, 十月 11, 2006		
Sheet 71 of 94		



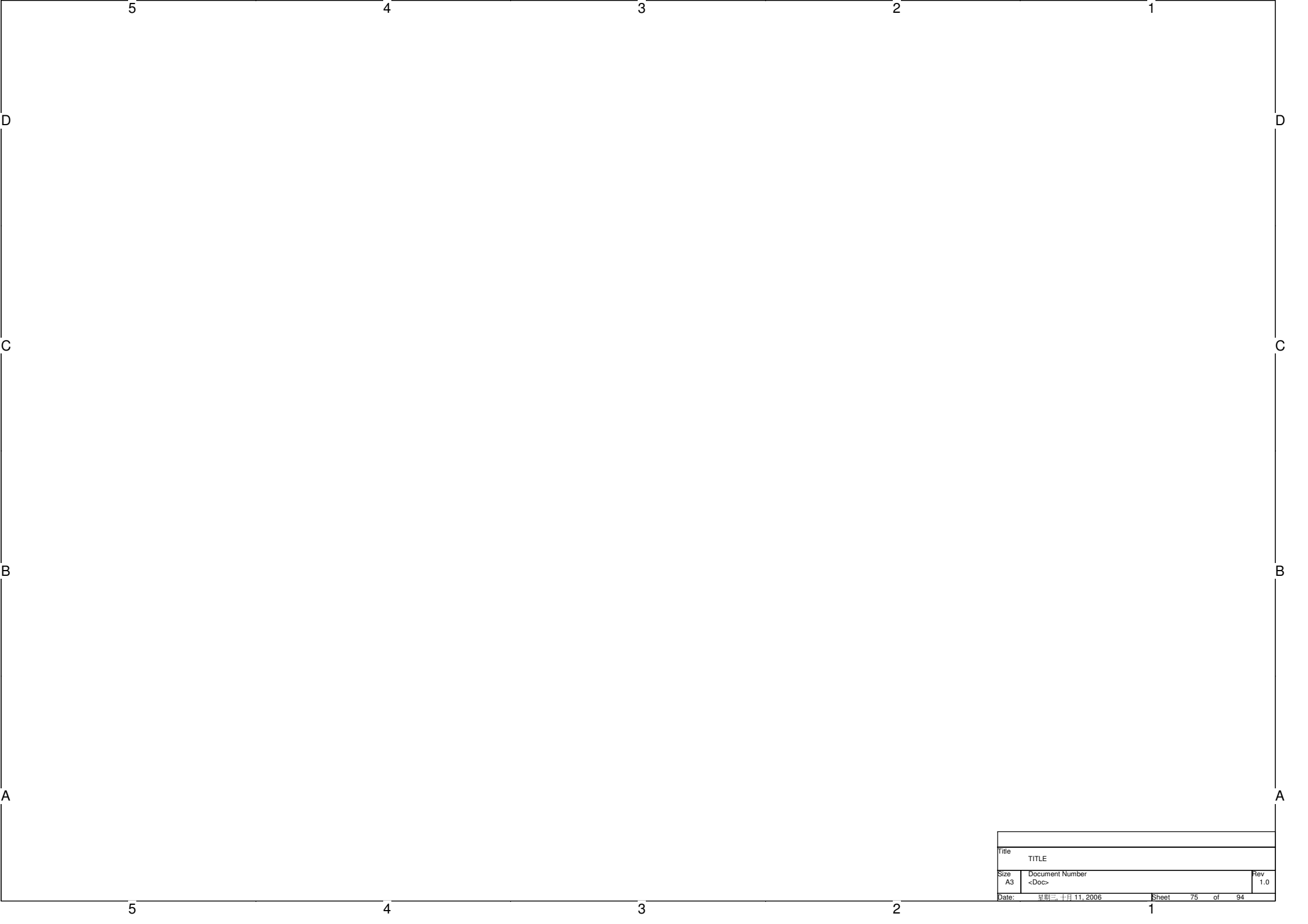
Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date: 星期二, 十月 11, 2006		
Sheet 72 of 94		



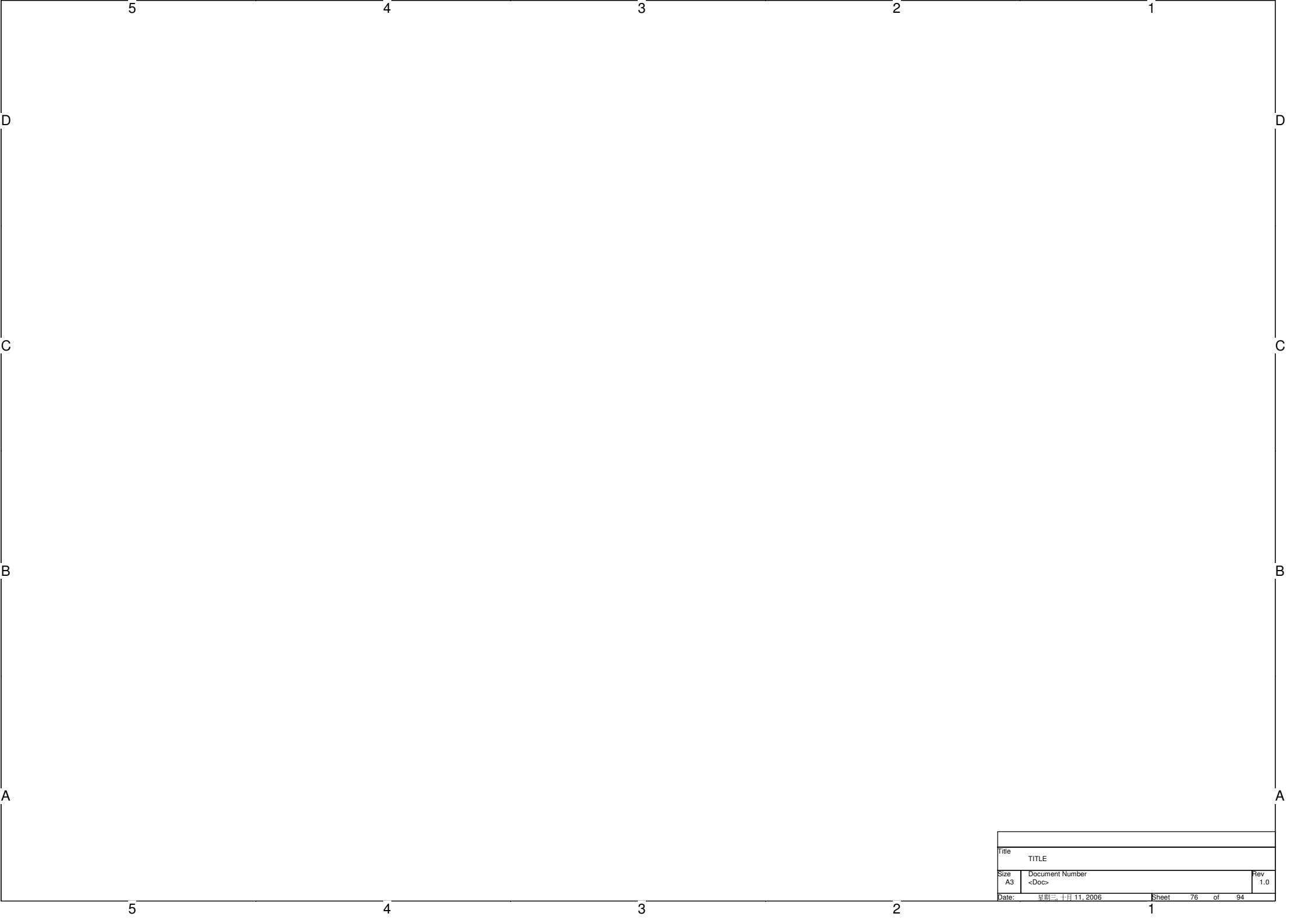
Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	星期二, 十月 11, 2006	Sheet 73 of 94



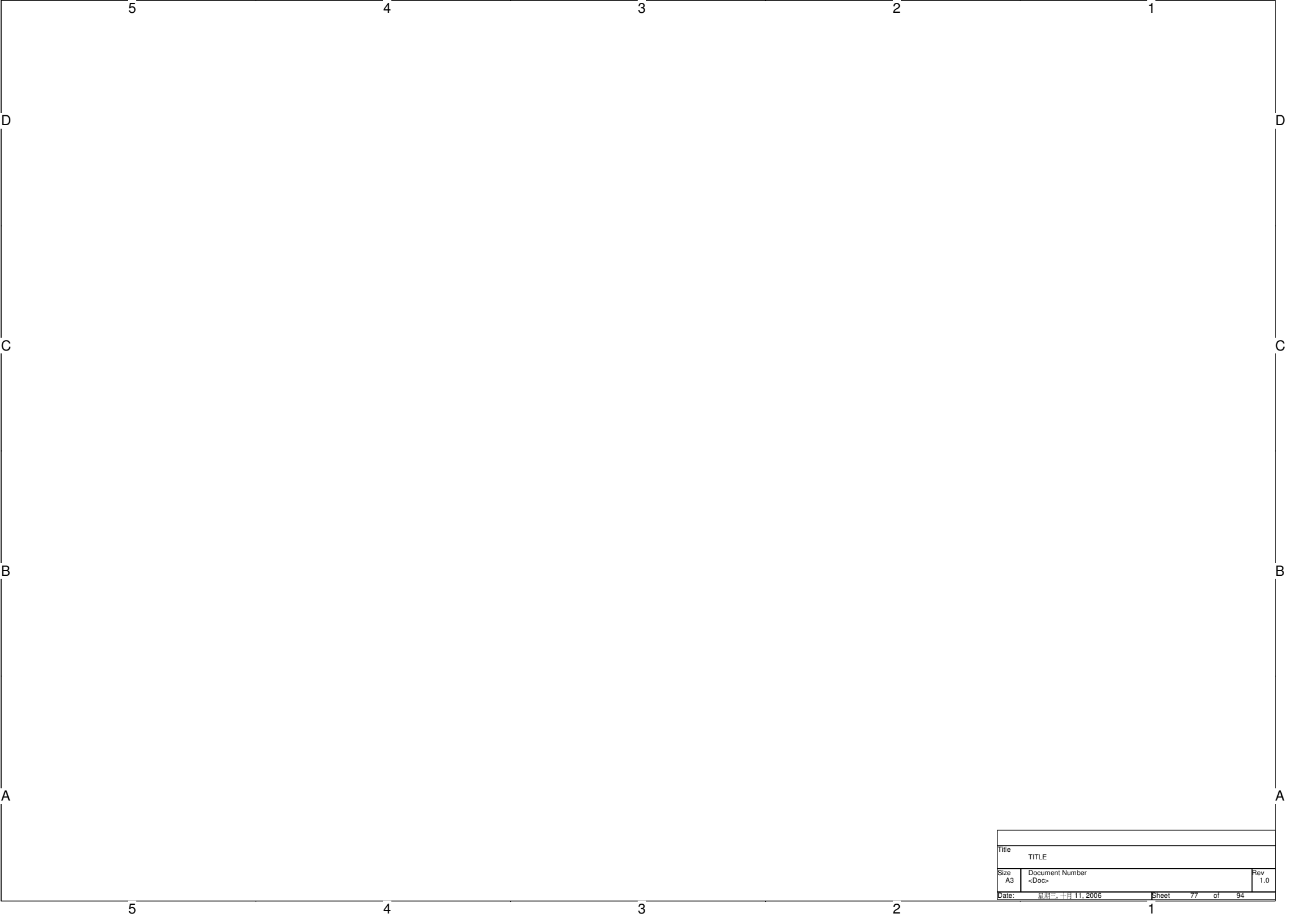
Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date: 星期二, 十月 11, 2006		
Sheet 74 of 94		



Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date:	星期二, 十月 11, 2006	Sheet 75 of 94



Title		
TITLE		
Size	Document Number	Rev
A3	<Doc>	1.0
Date: 星期二, 十月 11, 2006		
Sheet 76 of 94		



Title		
TITLE		
Size A3	Document Number <Doc>	Rev 1.0
Date: 星期二, 十月 11, 2006	Sheet 77 of 94	

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
B	A8ES		0
Date: 星期三, 十月 11, 2006		Sheet	78 of 94

W2S

Change Note:
EE :

1. 965PM pin defined modification, C48/D47/BJ29/BE24 from RSVD pin to LVDSA_DATA#_3 / LVDSA_DATA_3 / SA_MA_14 / SB_MA_14
2. CE46 / CE25 --> 11G08D210791
3. Rst button circuit
4. BT_SW pull-high to different plane issue.
5. Remove RN3104
6. VTT_REF reserve in S3.
7. VTT stop in S3.
8. CIR PME# function.


Layout :

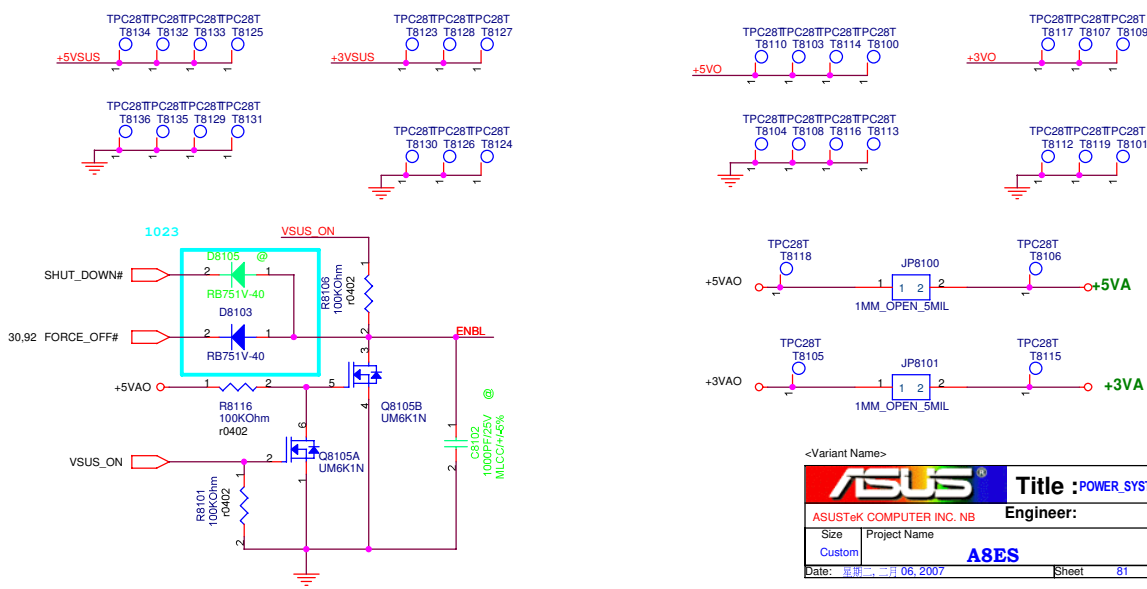
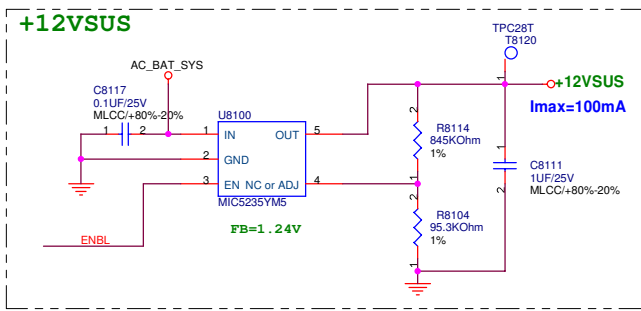
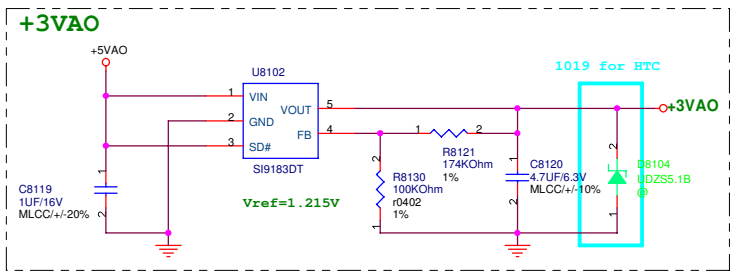
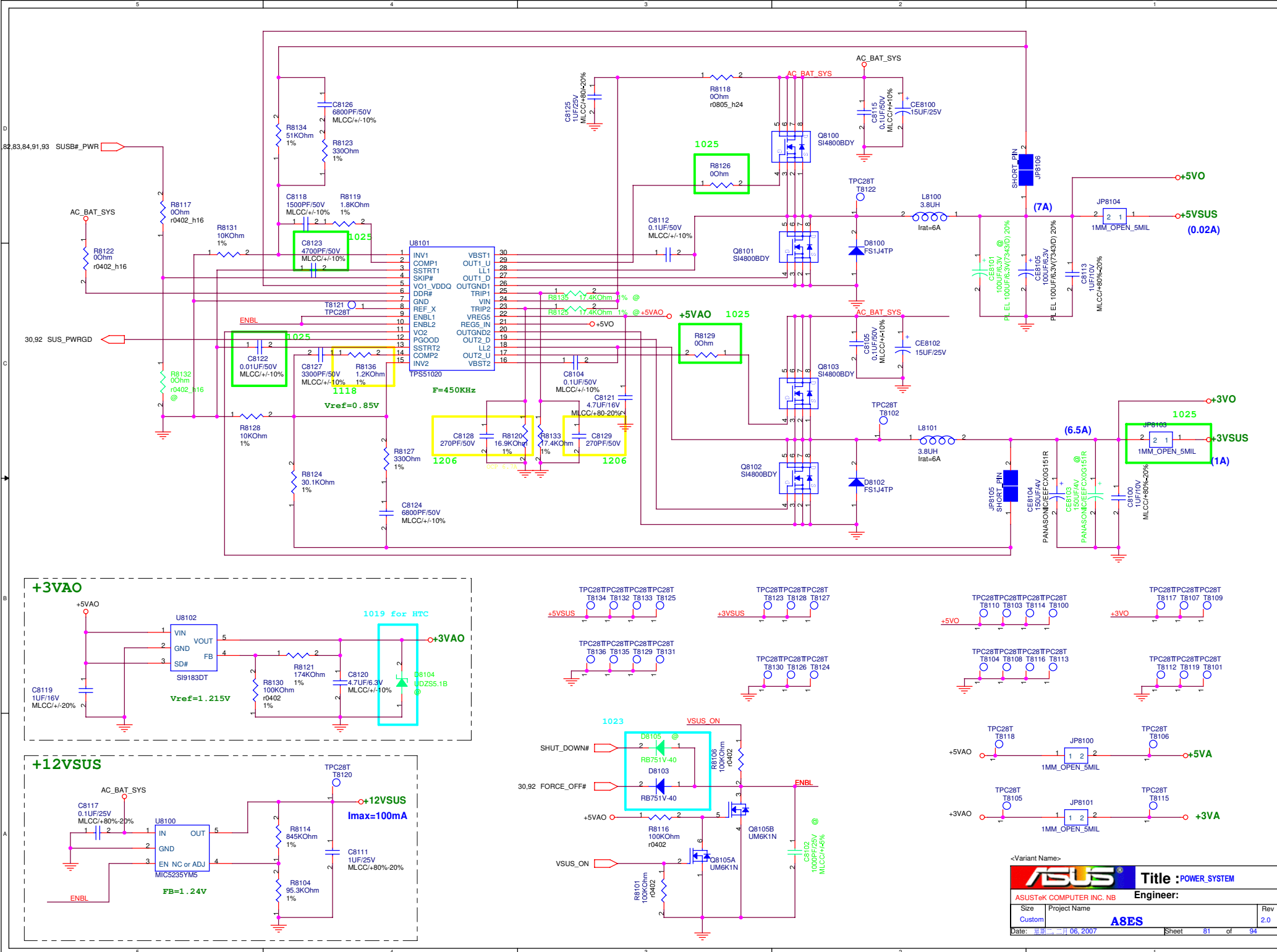
1. CPU side, per GND pin within per Via, don't share vias.
2. 0.9V_VTT_REF trace width.
3. single end trace width more than 3.5mil

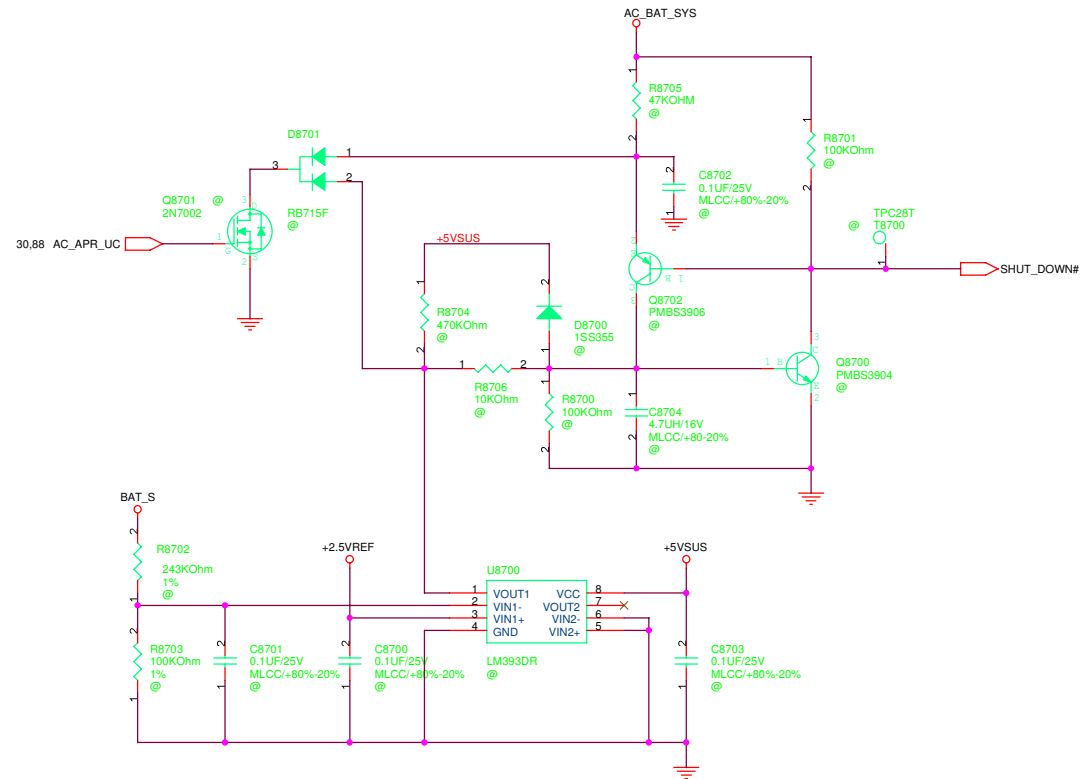
SMT :

1. 開鋼板JP1, JP2

<Variant Name>

		Title : History	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	ASES		1.0
Date: 星期一, 1月11, 2006		Sheet	79 of 94





<Variant Name>



Title : POWER_SHUTDOWN#

<OrgName>

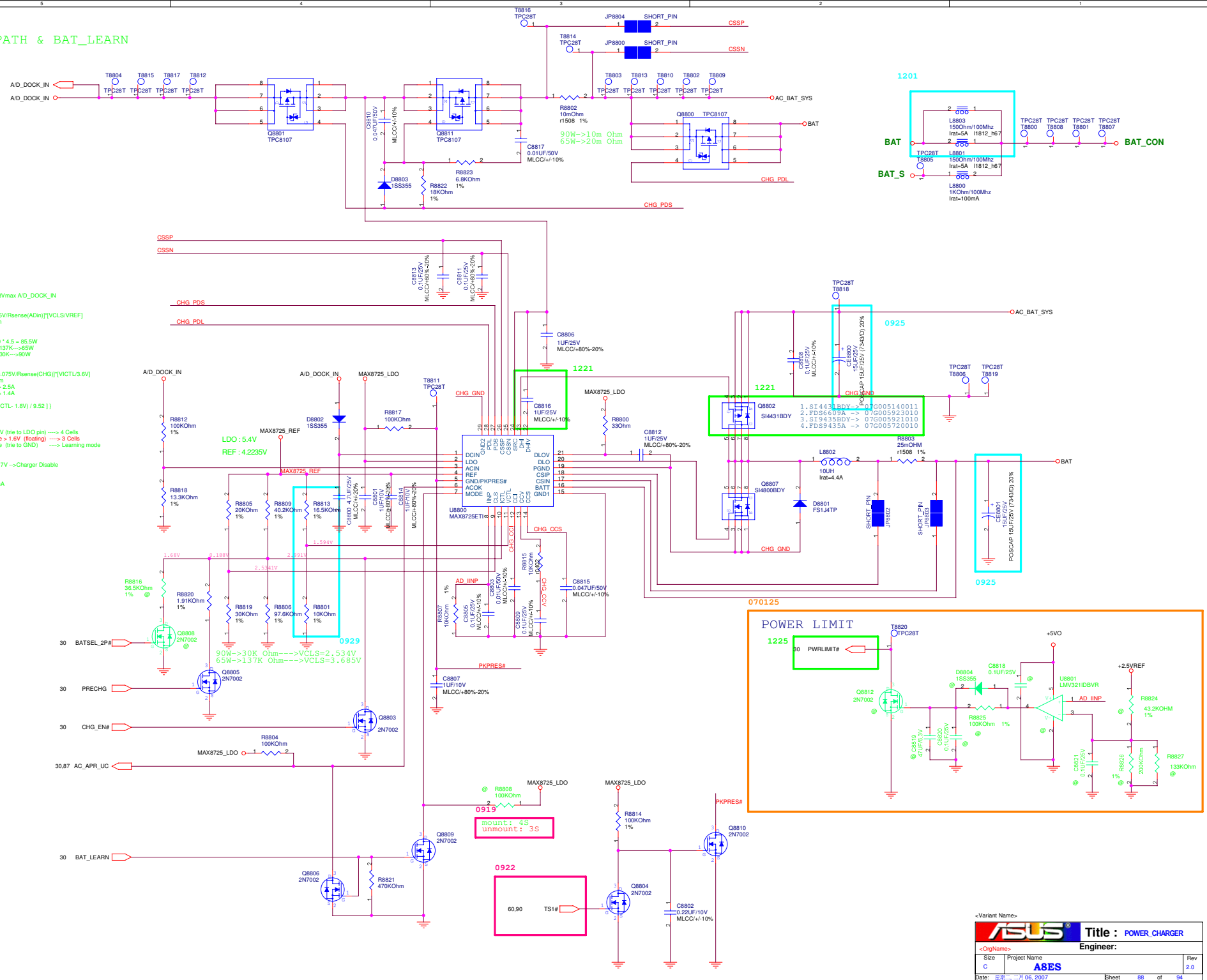
Size	Project Name
Custom	A81

Rev
2.0

Date: 星期二, 二月 06, 2007

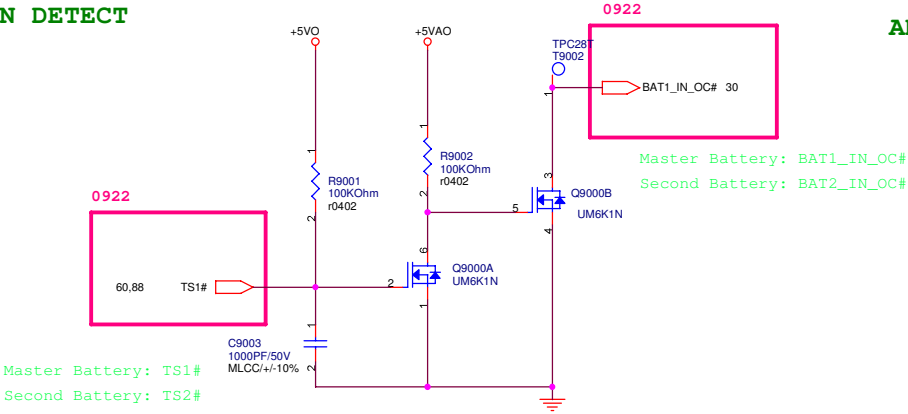
Sheet 87 of 94

POWER PATH & BAT_LEARN

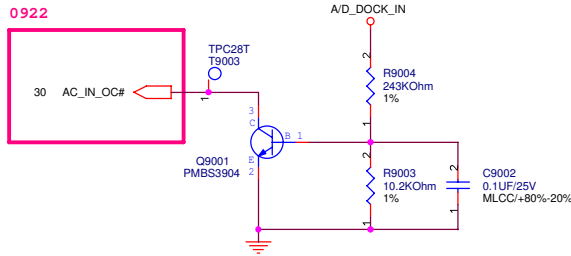


5					4					3					2					1												
D																																
C																																
B																																
A																																
<div><Variant Name><div><div><div>ASUS®</div><div>Title : N/A</div></div><div><div><OrgName></div><div>Engineer:</div></div><table><tr><td>Size</td><td colspan="2">Project Name</td><td>Rev</td></tr><tr><td>Custom</td><td colspan="2">ROSA</td><td>1.1</td></tr></table><div>Date: 星期五, 一月 25, 2007Sheet 89 of 94</div></div></div>																									Size	Project Name		Rev	Custom	ROSA		1.1
Size	Project Name		Rev																													
Custom	ROSA		1.1																													
5					4					3					2					1												

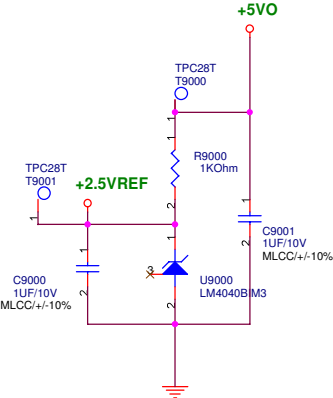
BATTERY IN DETECT



ADAPTER IN DETECT

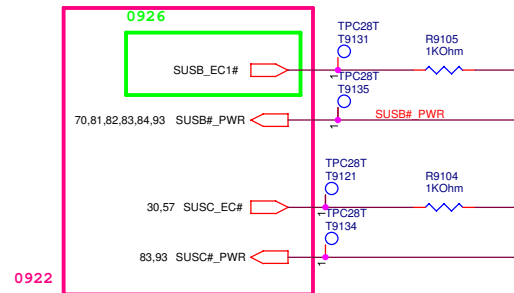
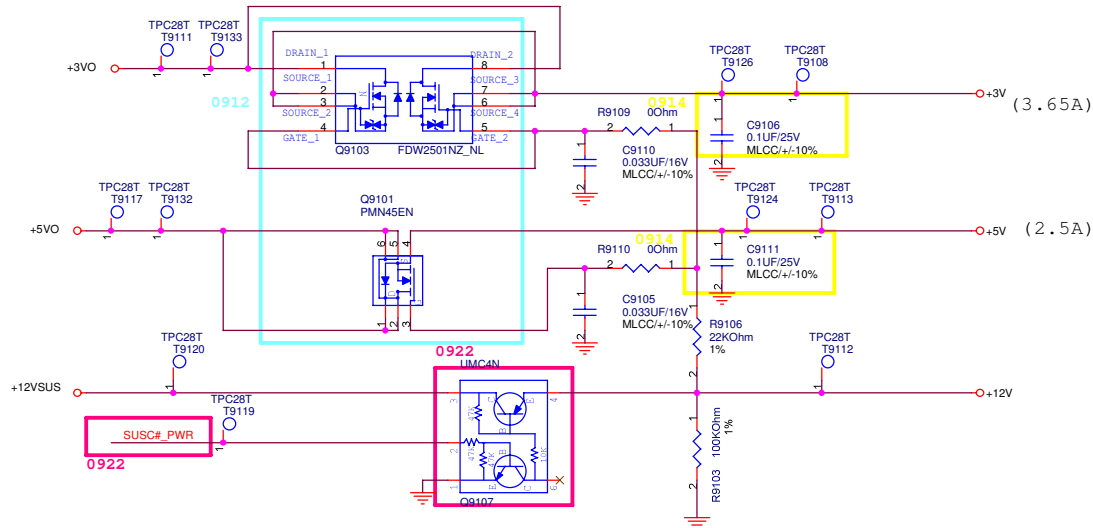


+2.5VREF



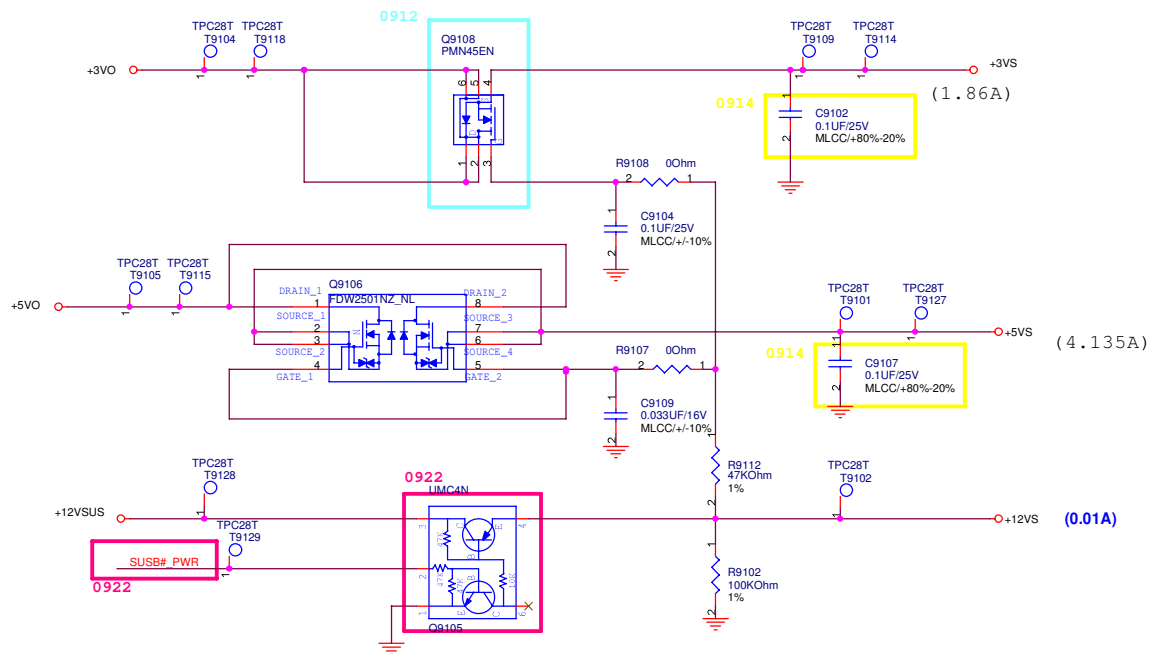
SUSC#_PWR POWER

0922



SUSB#_PWR POWER

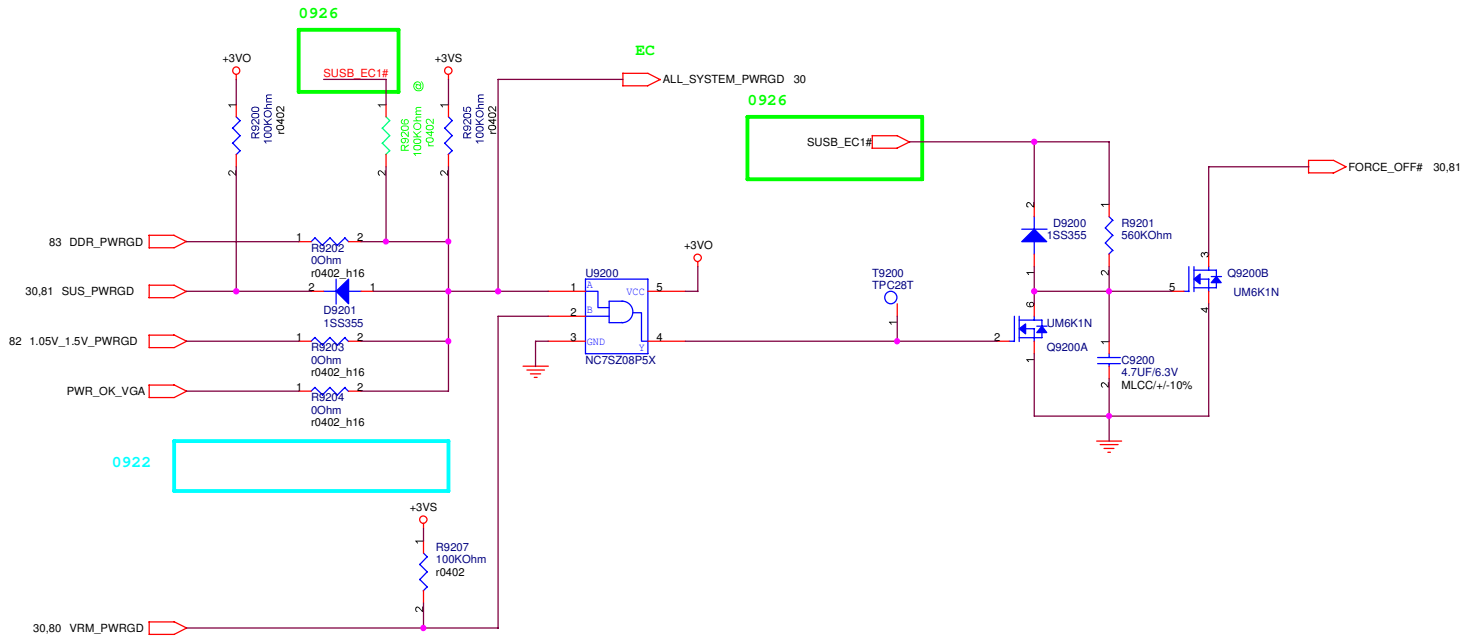
0922

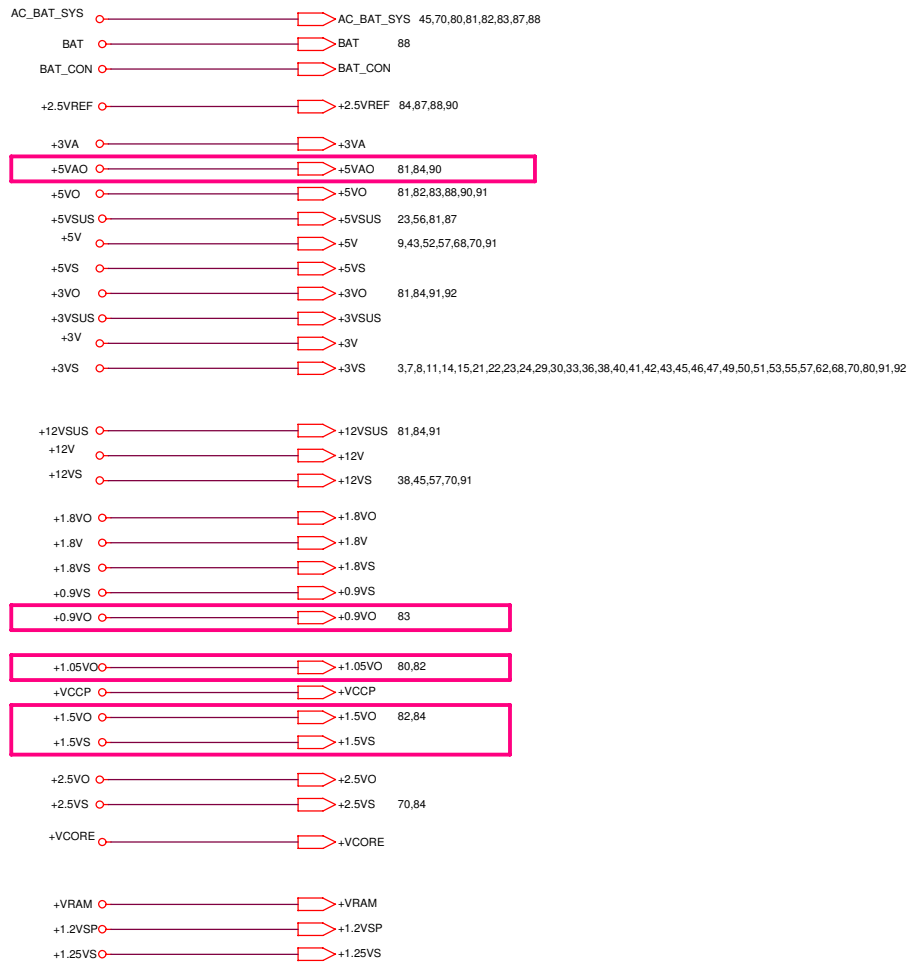


<Variant Name>

ASUS		Title : POWER_LOAD SWITCH	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	ASUS	2.0	
Date: 2007-06-06	Sheet 91	of 94	

POWER GOOD DETECTOR





FOR POWER TEST

