

Model Name :

File Name :

# Compal Confidential

## *ULC UMA M/B LA-A994P Schematics Document*

Intel Bay Trail M VC

Project Code : ZSO50

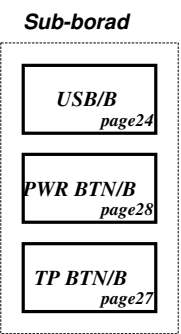
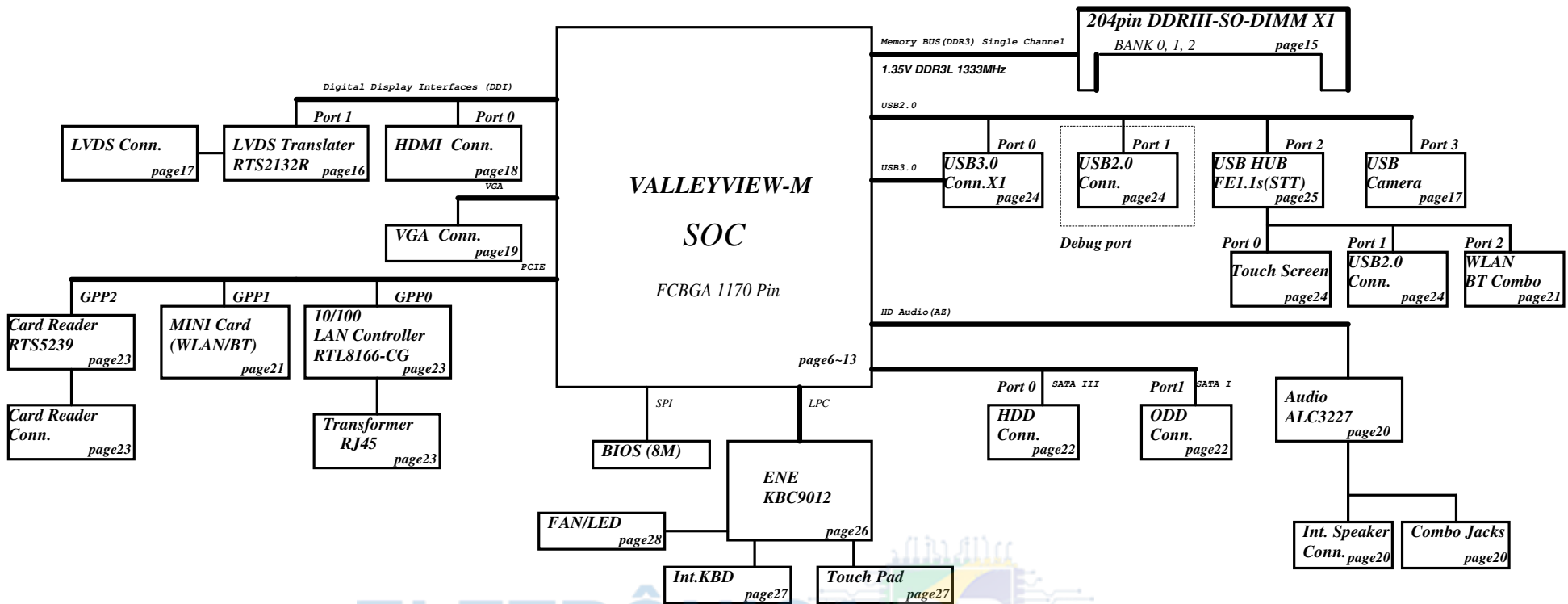
2014/02/05

MV Rev. 1.0

DAX ZSO50 BayTrail-M

| Part Number | Description                 |
|-------------|-----------------------------|
| DAZ14Z00200 | PCB 14Z LA-A994P REV0 M/B 4 |

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|   |            |                    |            | Date:                    | Friday, February 21, 2014 |
|   |            |                    |            | Sheet                    | 2 of 43                   |

## Voltage Rails

| Power Plane | Description   | S0 | S3  | S4/S5 |
|-------------|---|----|-----|-------|
| VIN         | 19V Adapter power supply                                | ON | ON  | ON    |
| BATT+       | 12V Battery power supply                                | ON | ON  | ON    |
| B+          | AC or battery power rail for power circuit. (19V/12V)   | ON | ON  | ON    |
| +VSB        | +VSBP to +VSB always on power rail for sequence control | ON | ON  | ON    |
| +RTCVCC     | RTC Battery Power                                       | ON | ON  | ON    |
| +1.0VALW    | +1.0v Always power rail                                 | ON | ON  | ON    |
| +1.2VALW    | +1.2v Always power rail                                 | ON | ON  | ON    |
| +1.8VALW    | +1.8v Always power rail                                 | ON | ON  | ON    |
| +3VALW      | +3.3v Always power rail                                 | ON | ON  | ON    |
| +5VALW      | +5.0v Always power rail                                 | ON | ON  | ON    |
| +1.35V      | +1.35V power rail for DDR3L                             | ON | ON  | OFF   |
| +SOC_VCC    | Core voltage for SOC                                    | ON | OFF | OFF   |
| +SOC_VNN    | GFX voltage for SOC                                     | ON | OFF | OFF   |
| +0.675VS    | +0.675V power rail for DDR3L Terminator                 | ON | OFF | OFF   |
| +1.0VS      | +1.0v system power rail                                 | ON | OFF | OFF   |
| +1.05VS     | +1.05v system power rail                                | ON | OFF | OFF   |
| +1.35VS     | +1.35v system power rail                                | ON | OFF | OFF   |
| +1.5VS      | +1.5v system power rail                                 | ON | OFF | OFF   |
| +1.8VS      | +1.8v system power rail                                 | ON | OFF | OFF   |
| +3VS        | +3.3v system power rail                                 | ON | OFF | OFF   |
| +5VS        | +5.0v system power rail                                 | ON | OFF | OFF   |
|             |   |    |     |       |
|             |   |    |     |       |
|             |   |    |     |       |

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| DB       | 0.1          |
| SI       | 0.2          |
| PV       | 0.3          |
| MV       | 1.0          |

## BOM Option Table

| BTO Item              | BOM Structure |
|-----------------------|---------------|
| Unpop                 | @             |
| Connector             | CONN@         |
| XDP (Debug Port)      | XDP@          |
| EMI requirement       | EMI@          |
| EMI requirement unpop | @EMI@         |
| ESD requirement       | ESD@          |
| ESD requirement unpop | @ESD@         |
| 8161 LAN controller   | 8161@         |
| 8166 LAN controller   | 8166@         |
| LVDS                  | LVDS@         |
| LVDS LDO mode         | LVDSLDO@      |
| LVDS SWR mode         | LVDSWR@       |
| Translator RTS2132S   | 2132S@        |
| Translator RTS2132R   | 2132R@        |
| Short Pad             | RS@           |
| Clean CMOS            | CMOS@         |
| Jump                  | JP@           |

|  |  |
|--|--|
| USOC1 217@<br>B3 2.17G<br>SA00007E920                    | USOC1 186@<br>B3 1.86G<br>SA00007E010                    |
| USOC1 CR1@<br>CeleronR N2815 Dual 7.5W 2C<br>SA00007E030 | USOC1 PR1@<br>PentiumR N3520 Quad 7.5W 4C<br>SA00007E940 |
| USOC1 CR3@<br>CeleronR N2815 Dual 7.5W 2C<br>SA00007E060 | USOC1 PR3@<br>PentiumR N3520 Quad 7.5W 4C<br>SA00007E950 |

## EC SM Bus1 address

## EC SM Bus2 address

| Device        | Address     | Device | Address |
|---------------|-------------|--------|---------|
| Smart Battery | 0001 011X b |        |         |

## SOC SM Bus address

| Device            | Address               |
|-------------------|-----------------------|
| ChannelA DIMM0 A0 | 1010 000X JDIMM1(SPD) |

## 43 level BOM table

| 43 Level    | Description             | BOM Structure |
|-------------|-------------------------|---------------|
| 4319P6BOL01 | SMT MB AA231 V1UE3 HDMI |               |
|             |                         |               |
|             |                         |               |

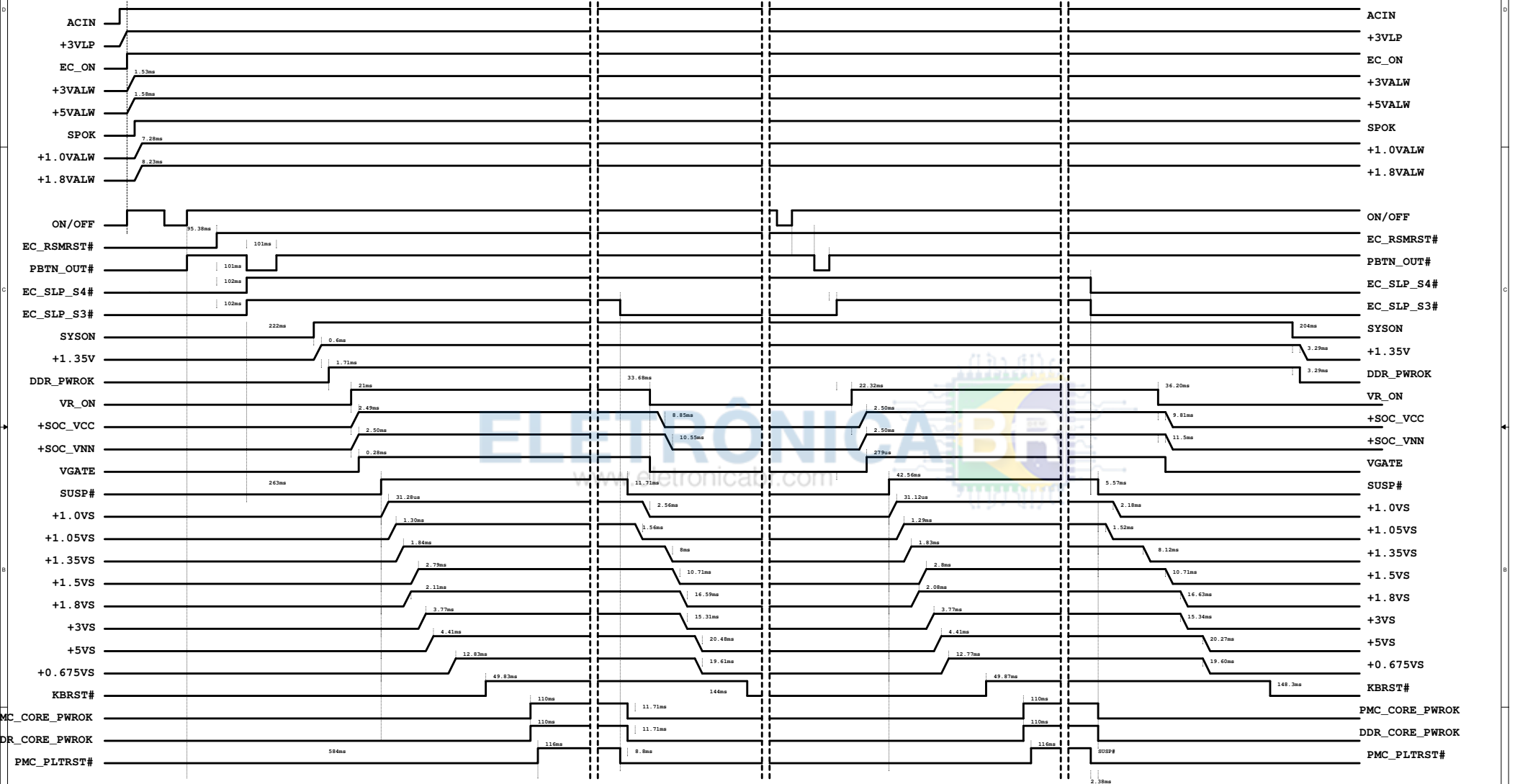
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G3-&gt;S0

S0-&gt;S3

S3-&gt;S0

S0-&gt;S5

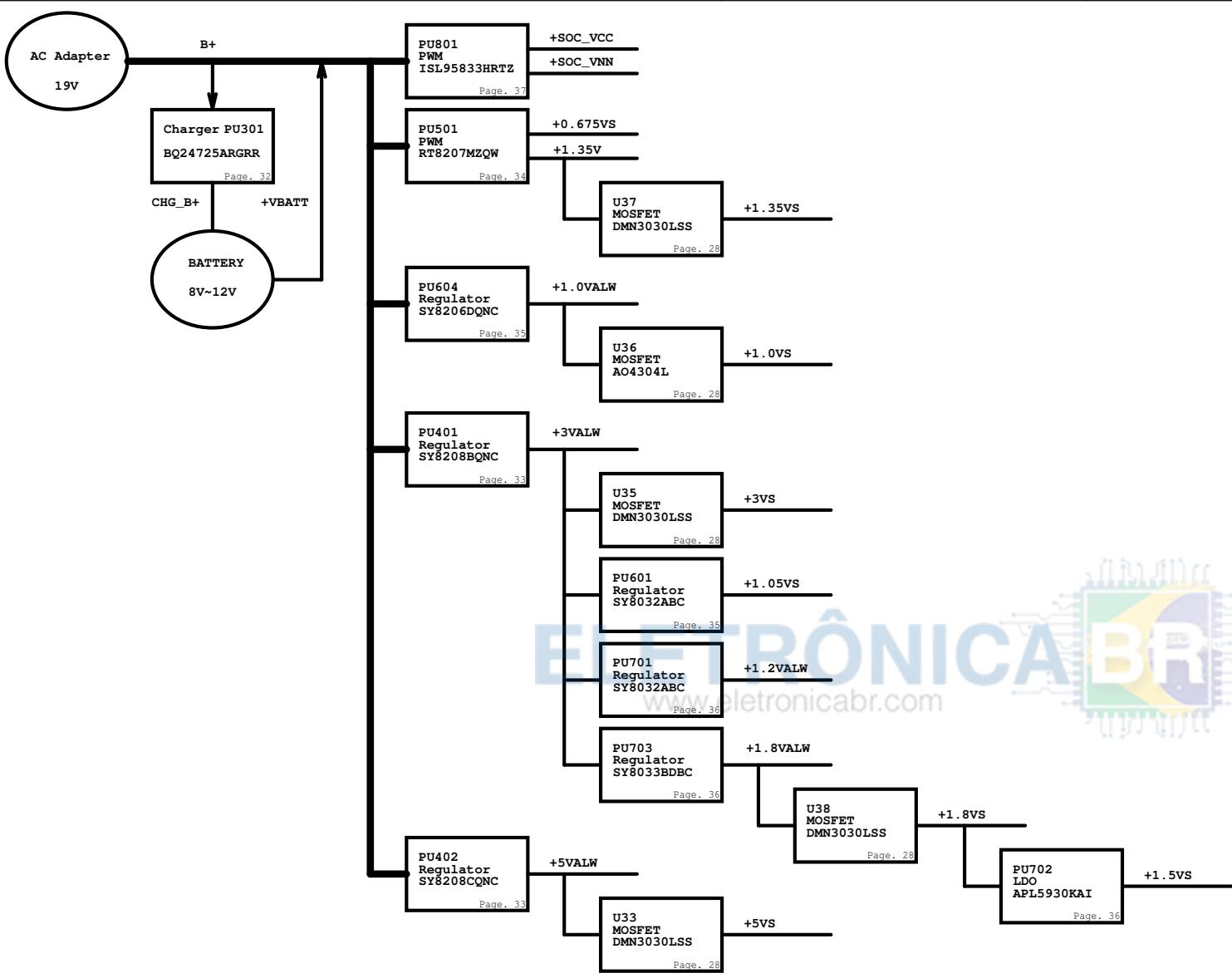


## NOTE:

1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

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|   |                    |                 |            | LA-A994P                        | 4 of 43 |
|   |                    |                 |            | Date: Friday, February 21, 2014 |         |

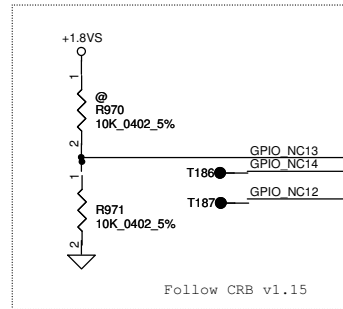


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HDMI

Follow CRB v1.15 0ohm till to GND

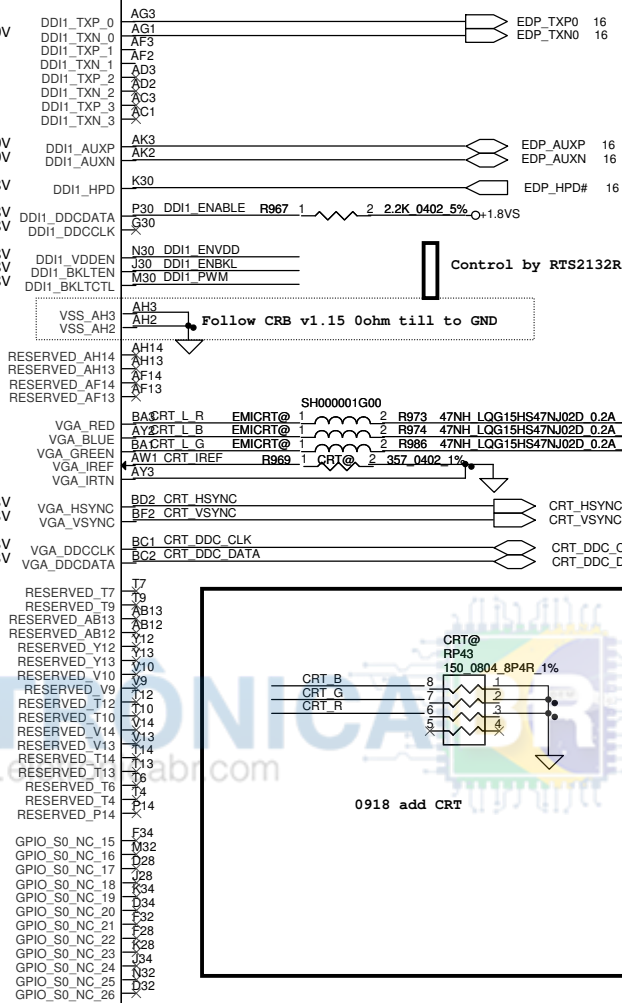


GPIO\_S0\_NC[13]:  
Multiplexed with Hardware Straps Pin:MDSI\_DDCDATA

USOC1C

FH8065301546401\_FCBGA131170

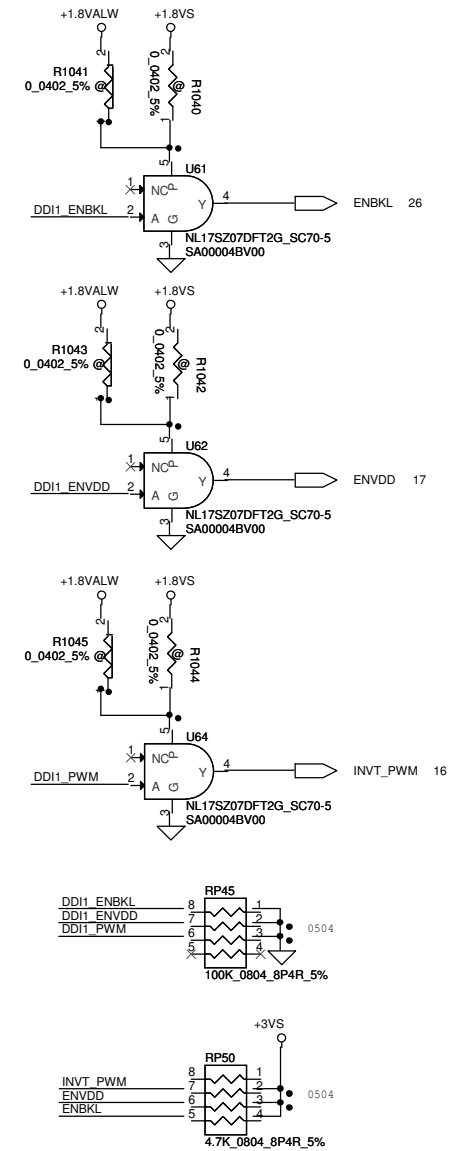
3 OF 10



eDP Panel

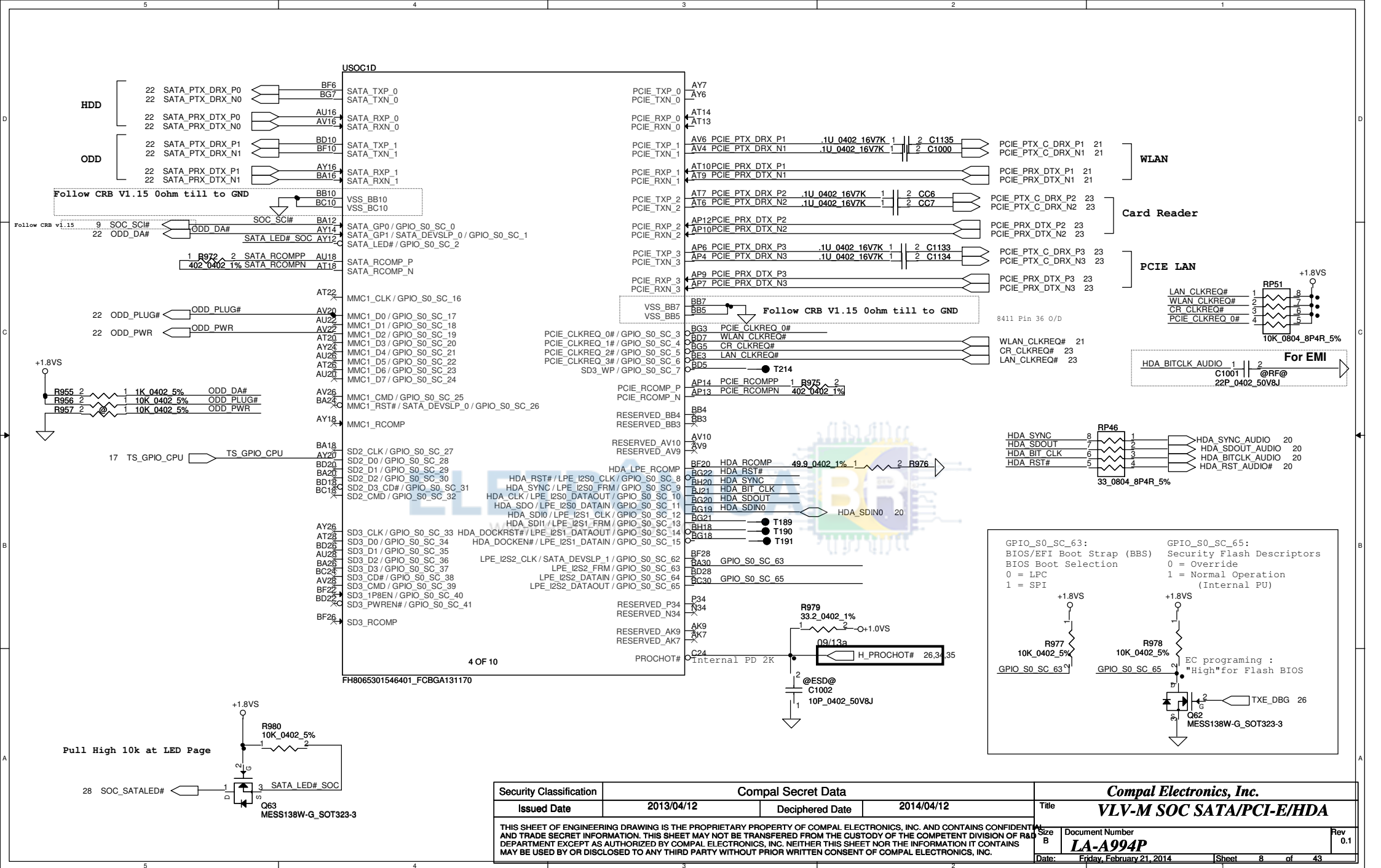
CRT

0918 add CRT

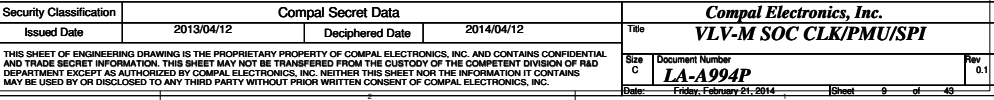


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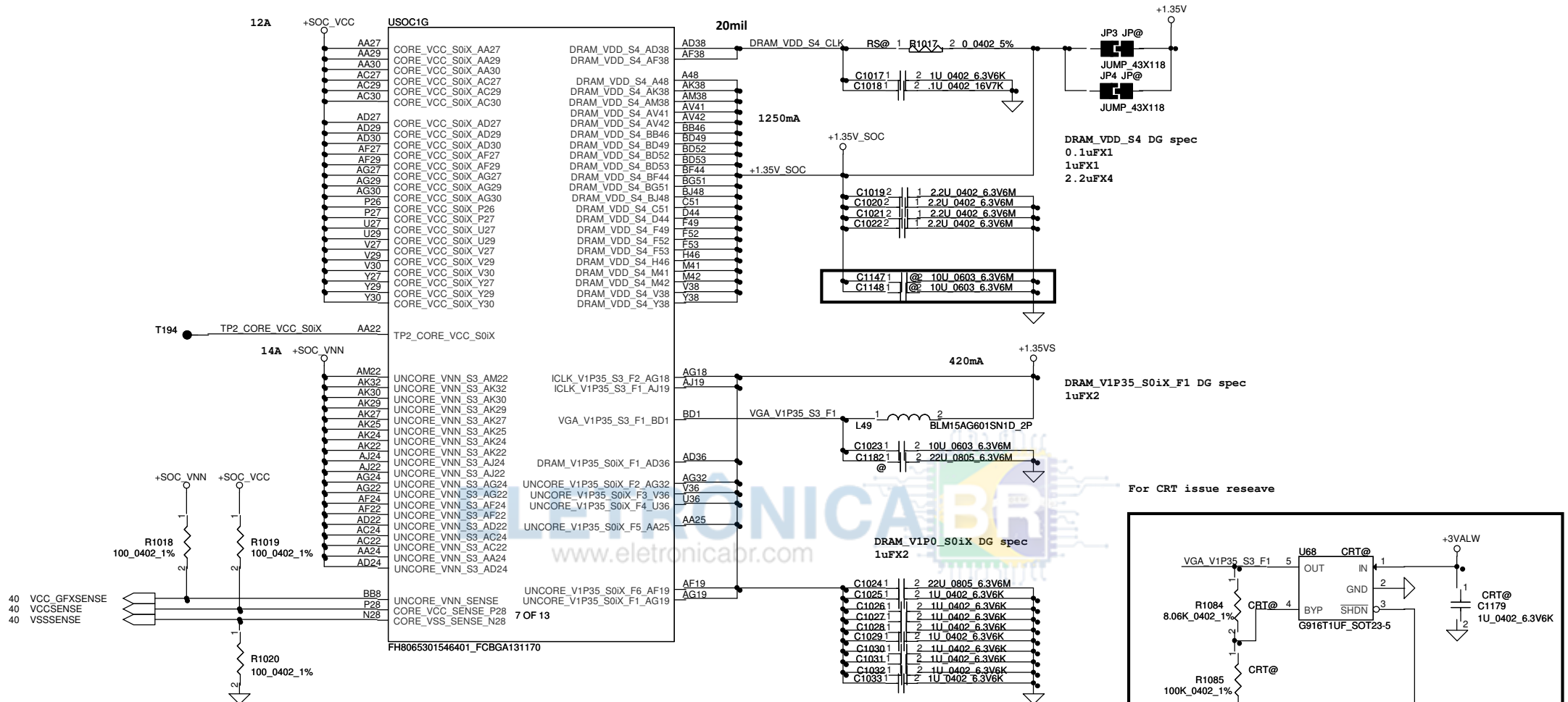




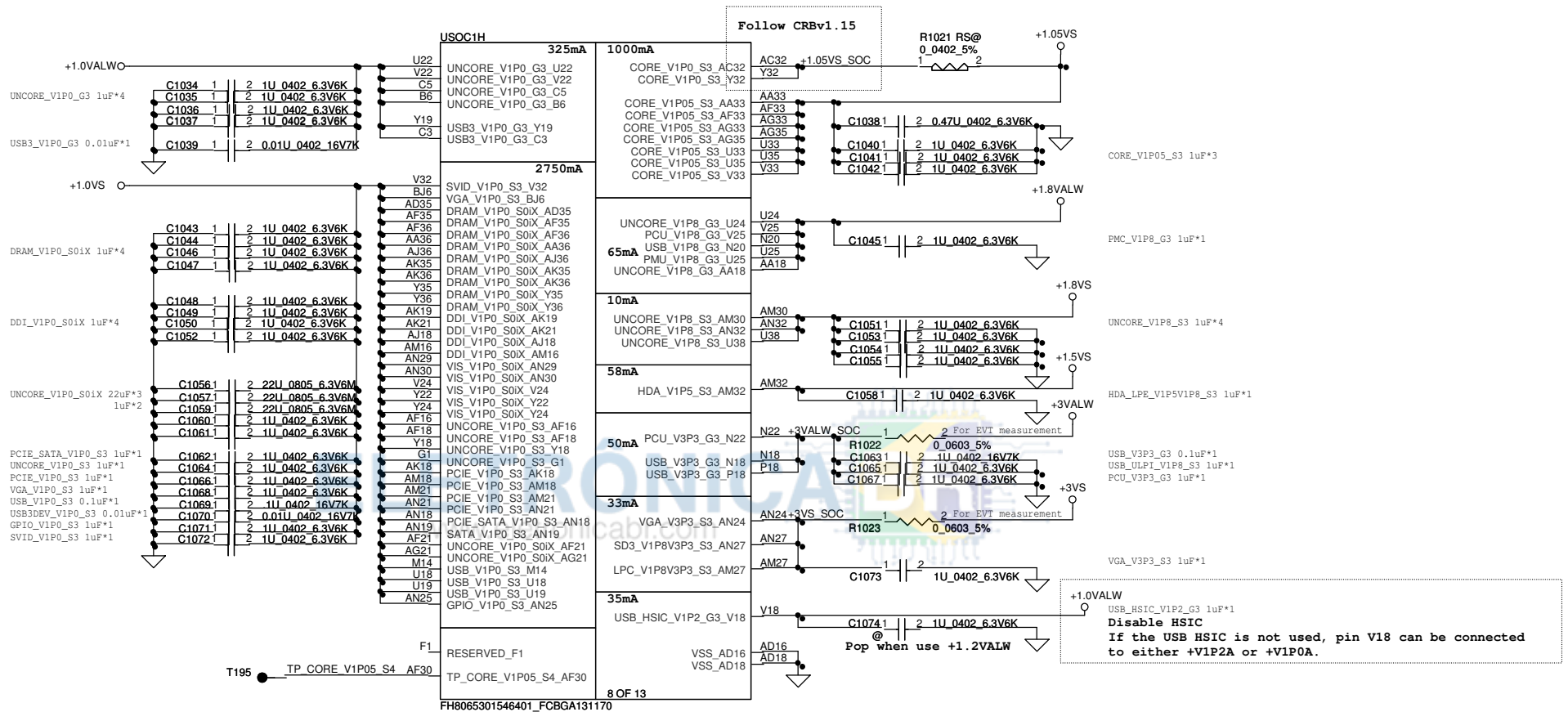




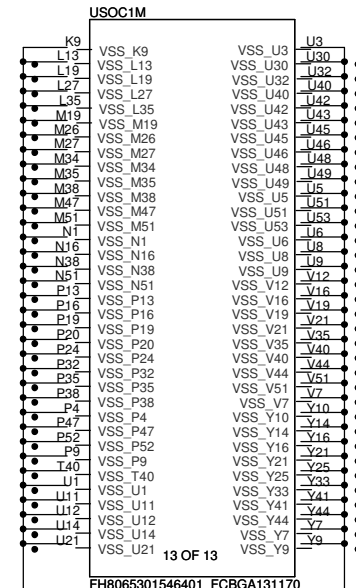
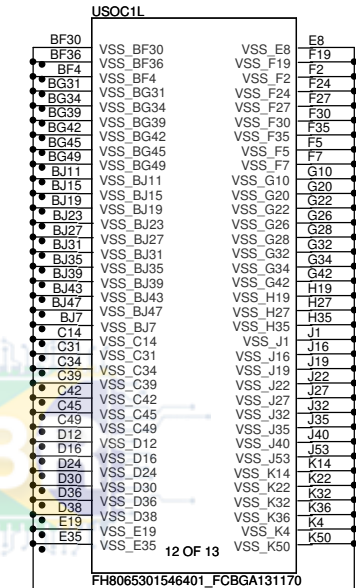
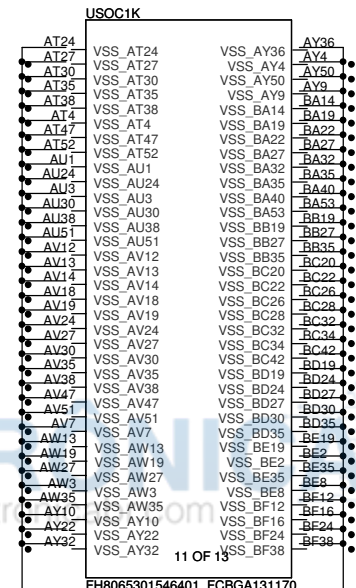
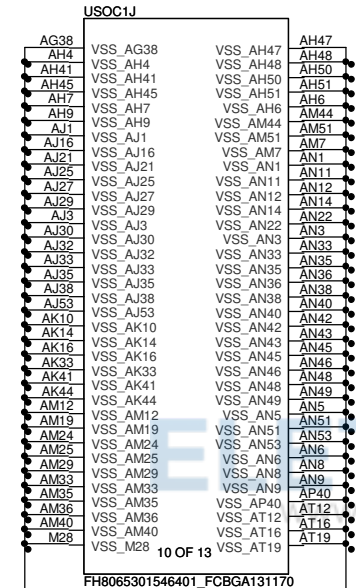
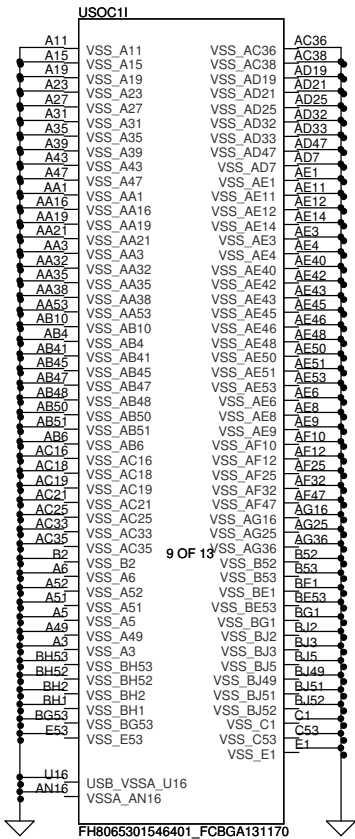




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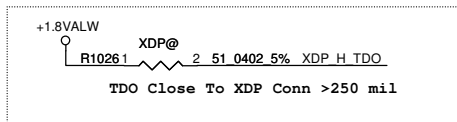
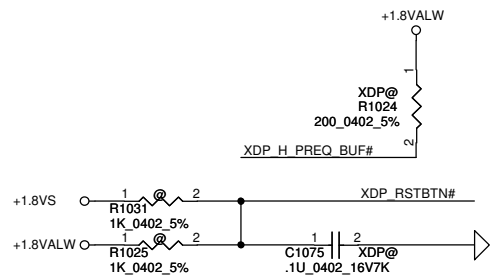


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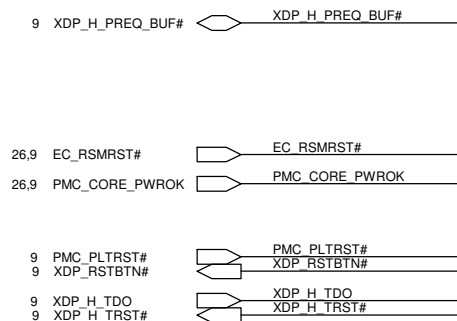


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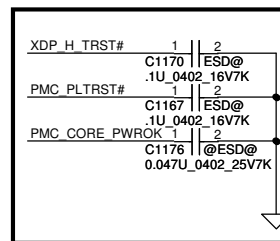




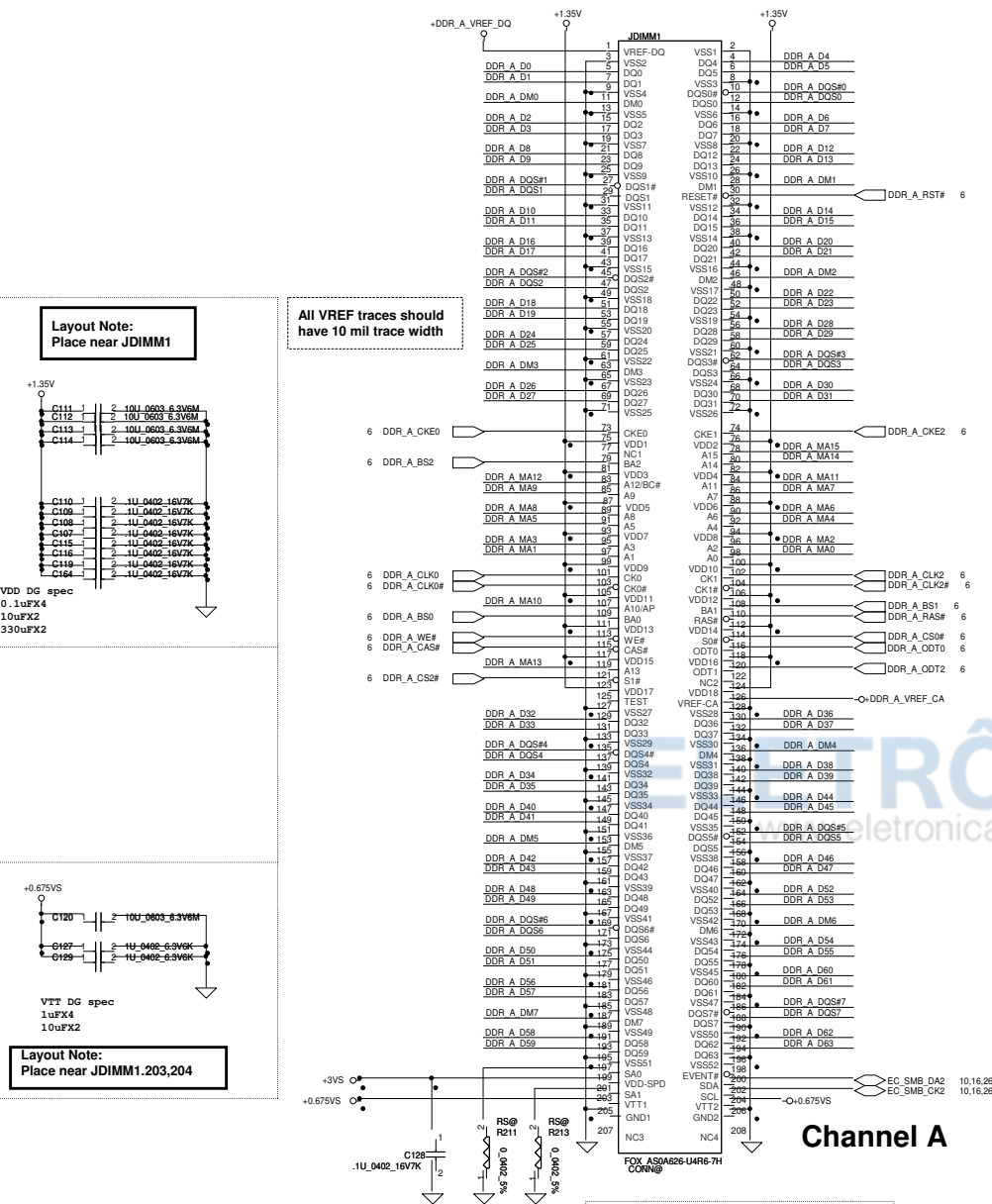
## XDP-SFF-26Pin



0927:for ESD request



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Layout Note:  
Place near JDIMM1

VDD DG spec  
0.1uFX4  
10uFX2  
330uFX2

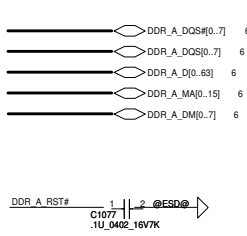
VTT DG spec  
1uFX4  
10uFX2

Layout Note:  
Place near JDIMM1.203,204

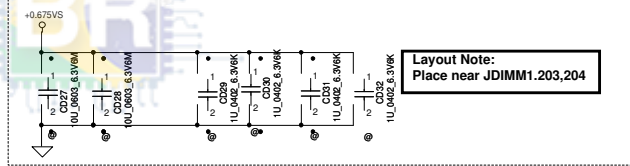
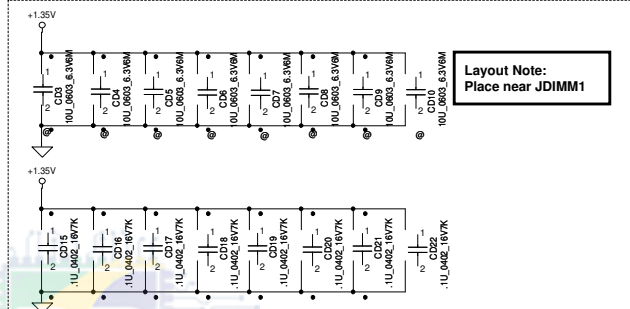
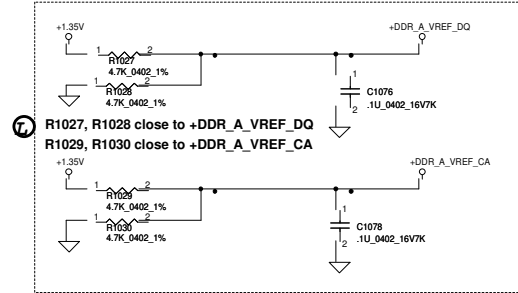
All VREF traces should  
have 10 mil trace width

Channel A

<Address: SA1:SA0=00 (A0H)>  
DIMM\_1 STD H:4mm



Signal voltage level = 0.675 V  
PLACE TWO 4.7K RESISTORS CLOSE TO  
DIMMS ON DIMM\_VREF\_CA / DIMM\_VREF\_DQ  
Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.

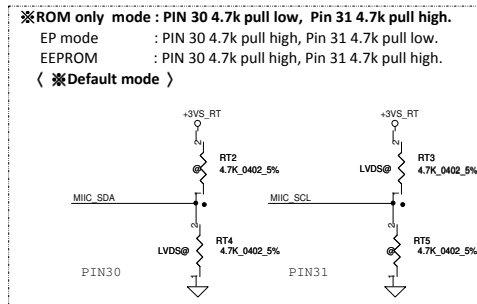
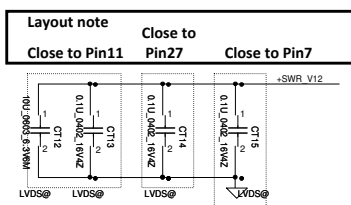
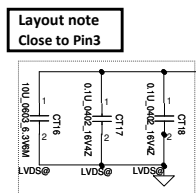


Layout Note:  
Place near JDIMM1

Layout Note:  
Place near JDIMM1.203,204

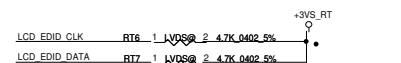
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|   |            |                    |            | Date:                    | Friday, February 21, 2014 |
|   |            |                    |            | Sheet                    | 16 of 48                  |





|       |                |           |
|-------|----------------|-----------|
|       | LDO            | SWR       |
| 2132S | Do not support | mount LT7 |
| 2132R | Use 0 ohm      | mount LT7 |

※ If use 2132R, please select LDO mode as default.

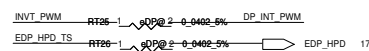
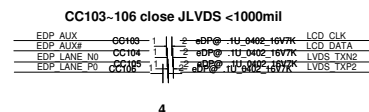
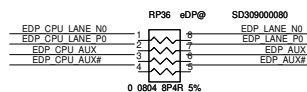
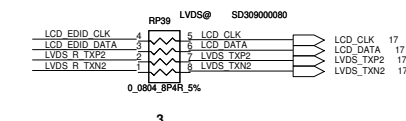
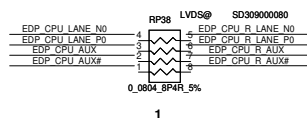
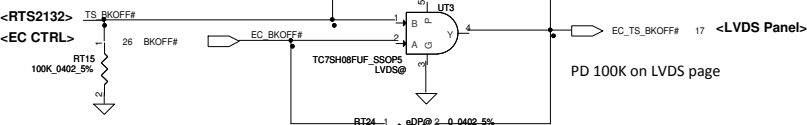
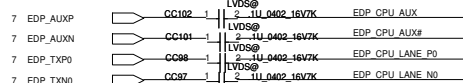
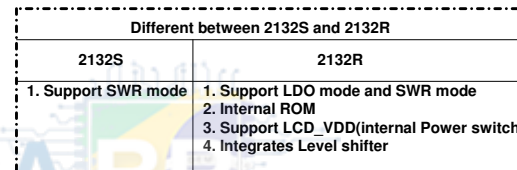
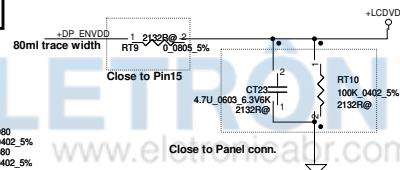
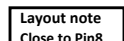
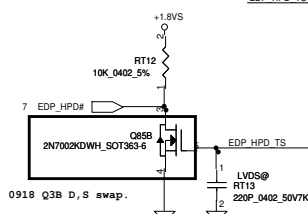


|       |            |
|-------|------------|
|       | PIN15      |
| 2132S | TL_ENVDD   |
| 2132R | +LCD_VDD * |

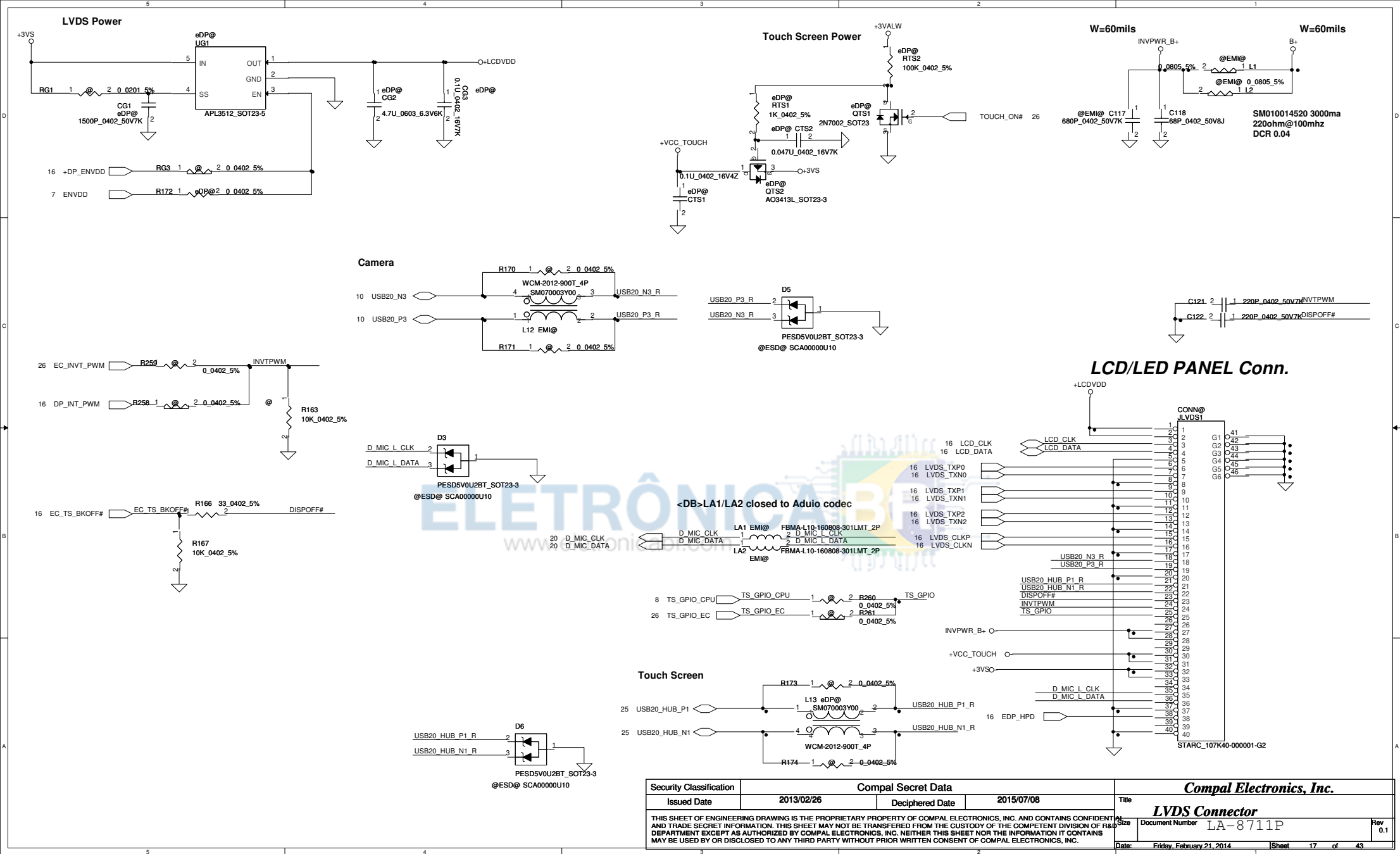
\* Version R internal Power Switch, can output 1A. Rds(on)=0.2 ohm

|       |                                   |
|-------|-----------------------------------|
| PIN16 | Accept voltage input (high level) |
| 2132S | 3.3V                              |
| 2132R | 1.5~3.3V                          |

\* Version R has internal level shifter, remove level shifter circuit on AMD platform

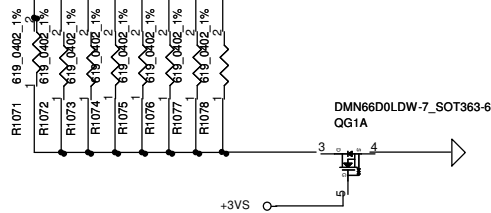


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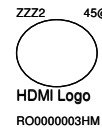
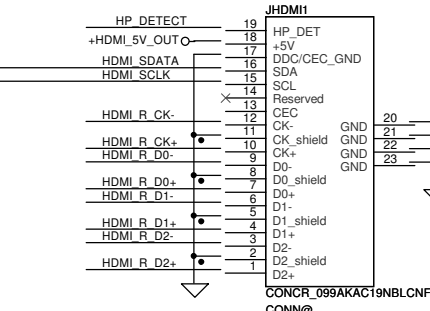
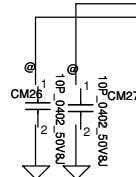
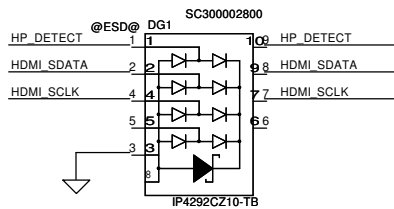
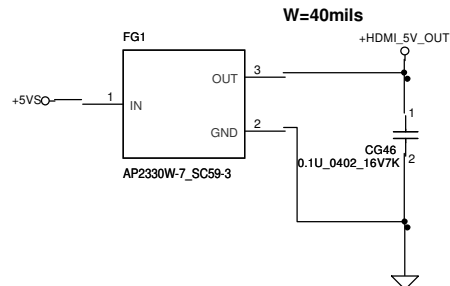
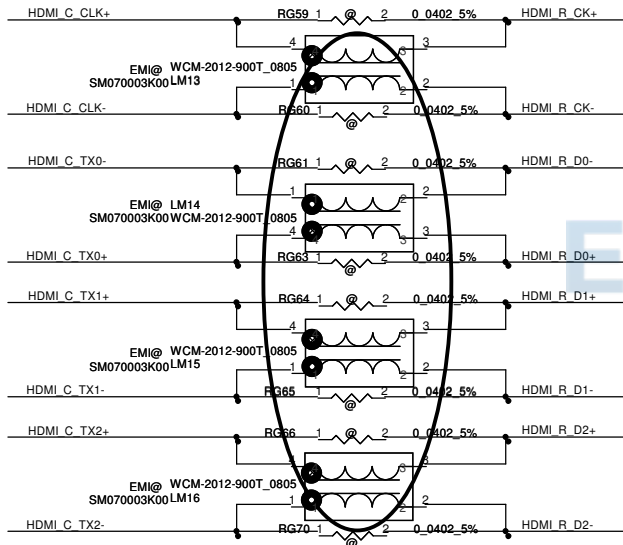


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|   |            |                    |            | Document Number                 |                |
|   |            |                    |            | Date: Friday, February 21, 2014 | Sheet 17 of 43 |

<CPU>

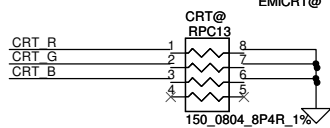
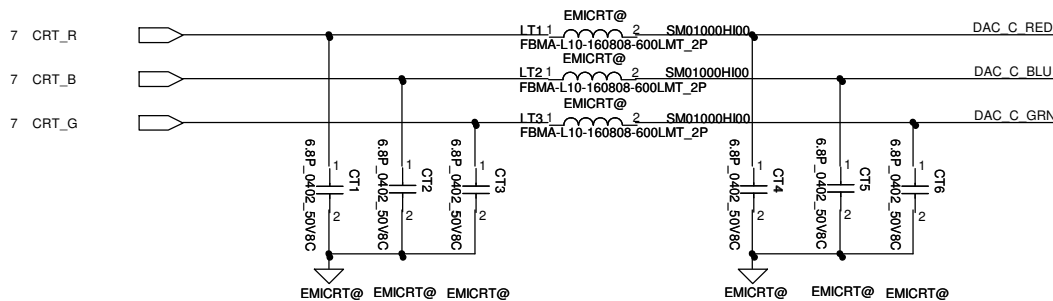
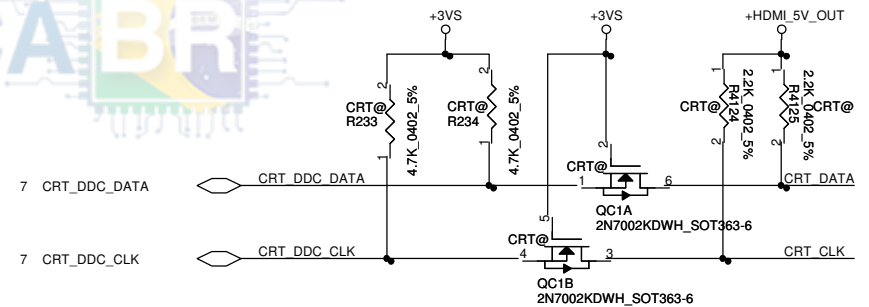
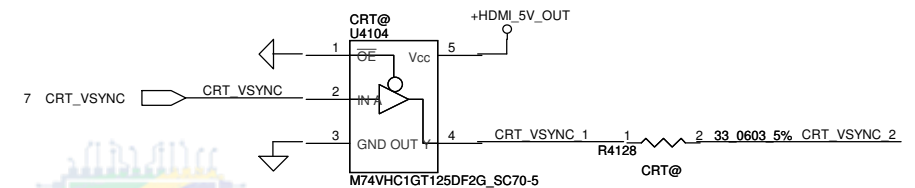
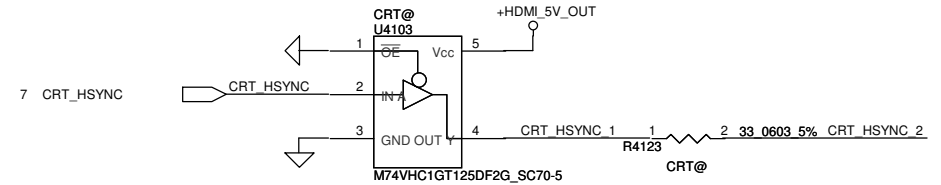
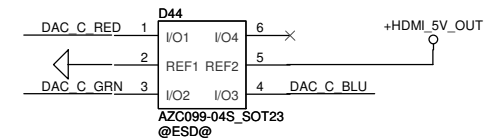
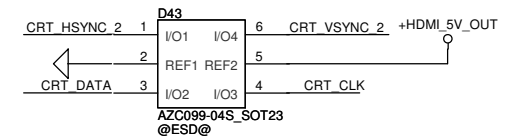
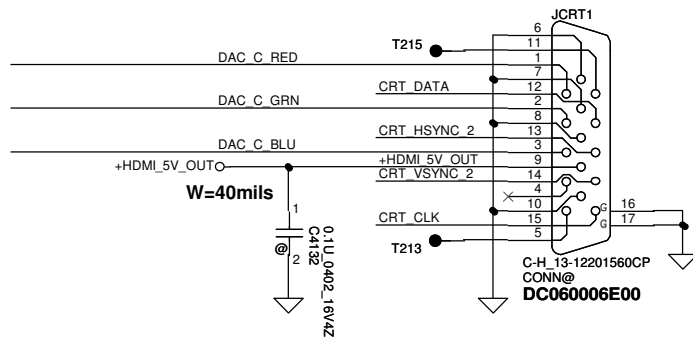


10/21 BOM change SM070003K00



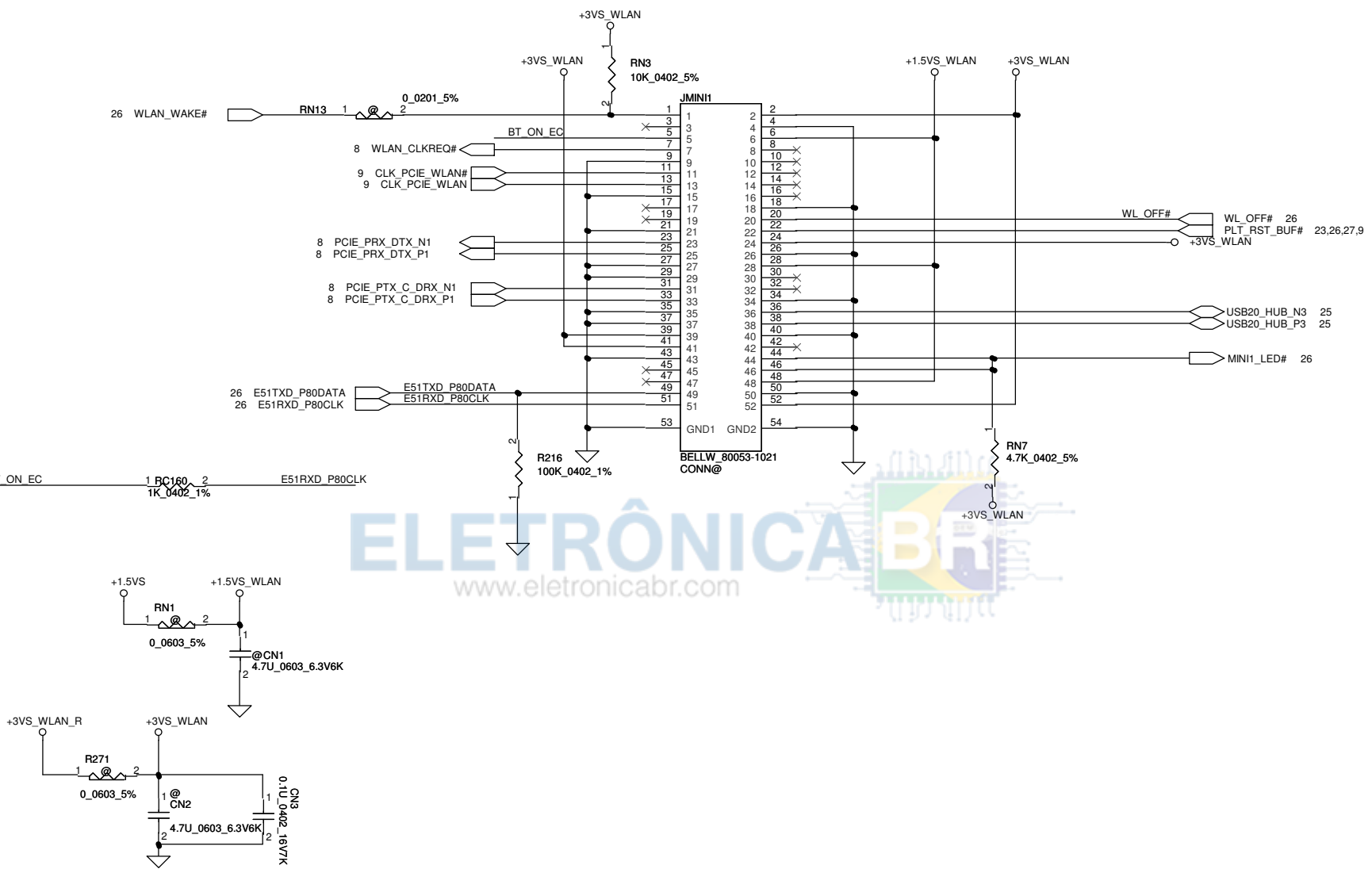
HDMI Conn.

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|   |            |                    |            | Document Number                 | Rev            |
|   |            |                    |            | LA-A994P                        | 0.1            |
|   |            |                    |            | Date: Friday, February 21, 2014 | Sheet 19 of 43 |





|   |            |                    |            |                          |                           |
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|   |            |                    |            | Sheet                    | 21 of 43                  |
|   |            |                    |            | Rev                      | 0.1                       |

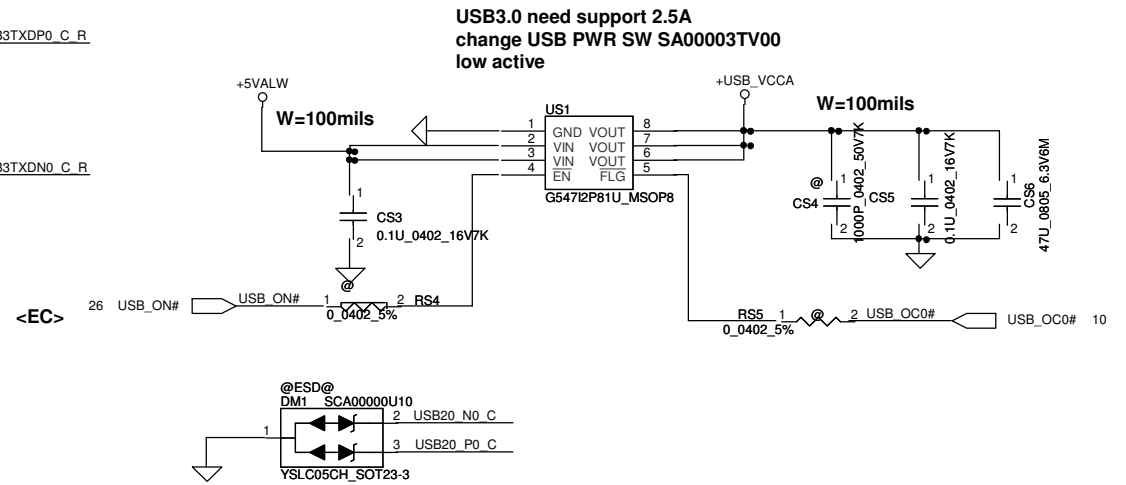
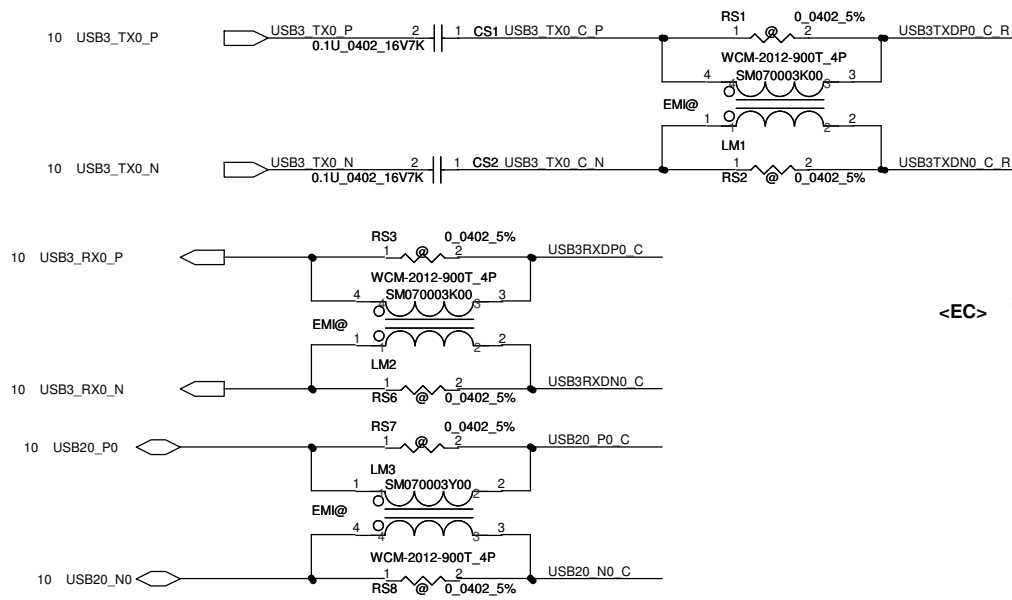
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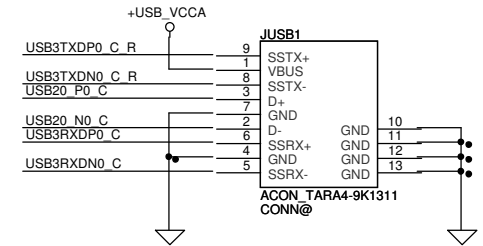
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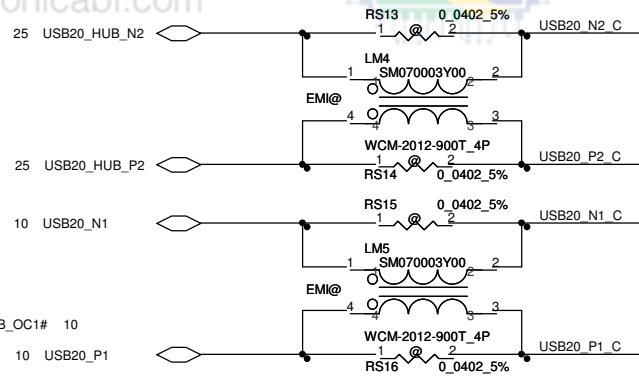
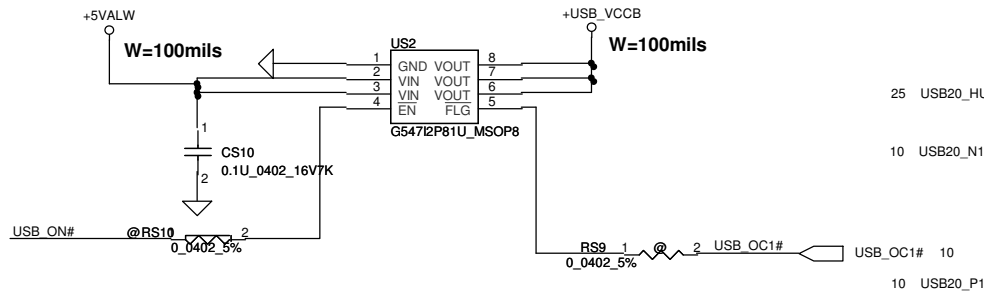




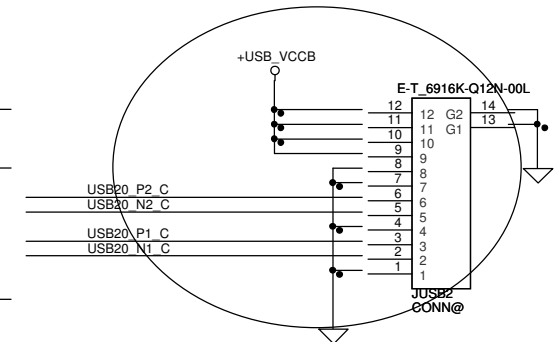
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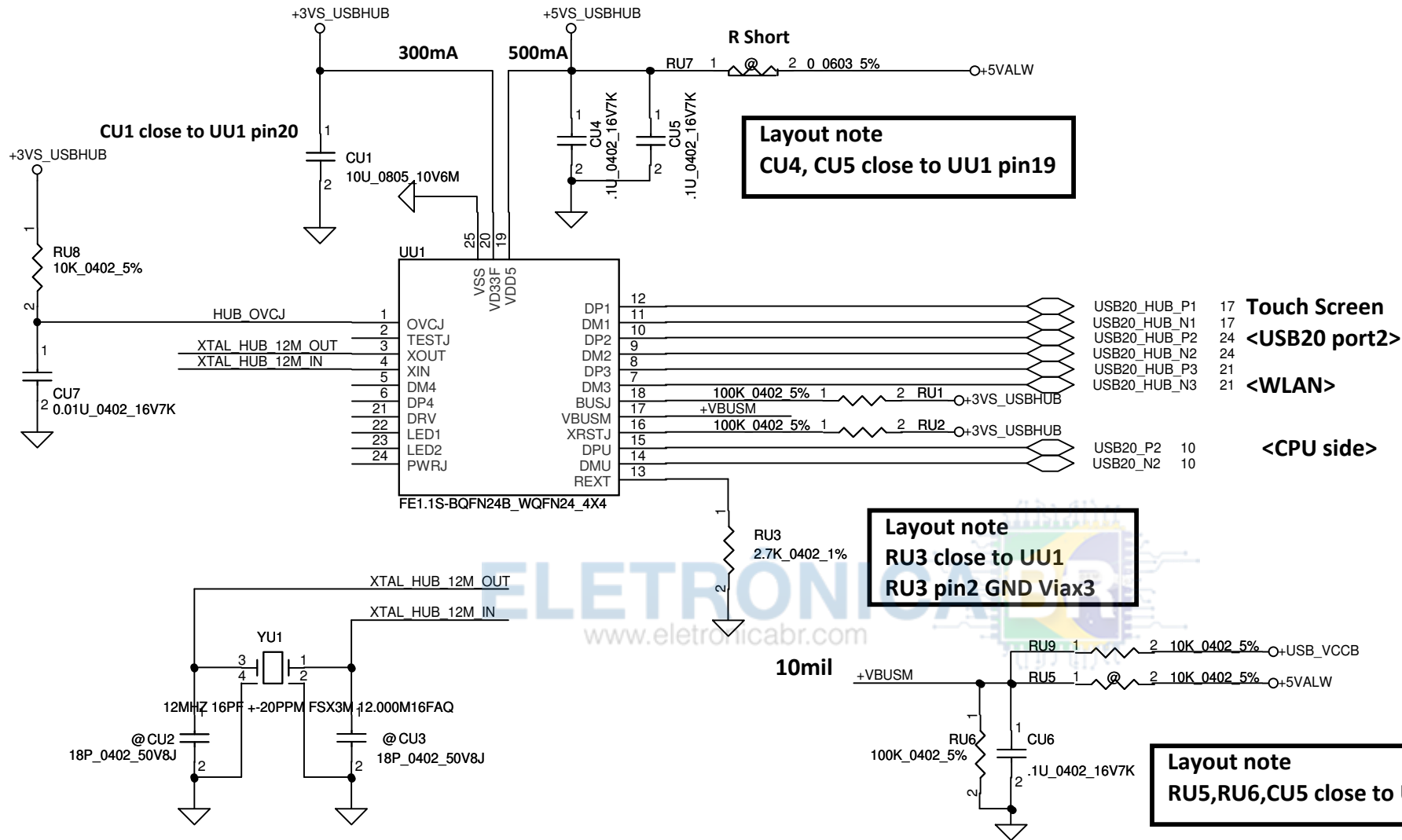
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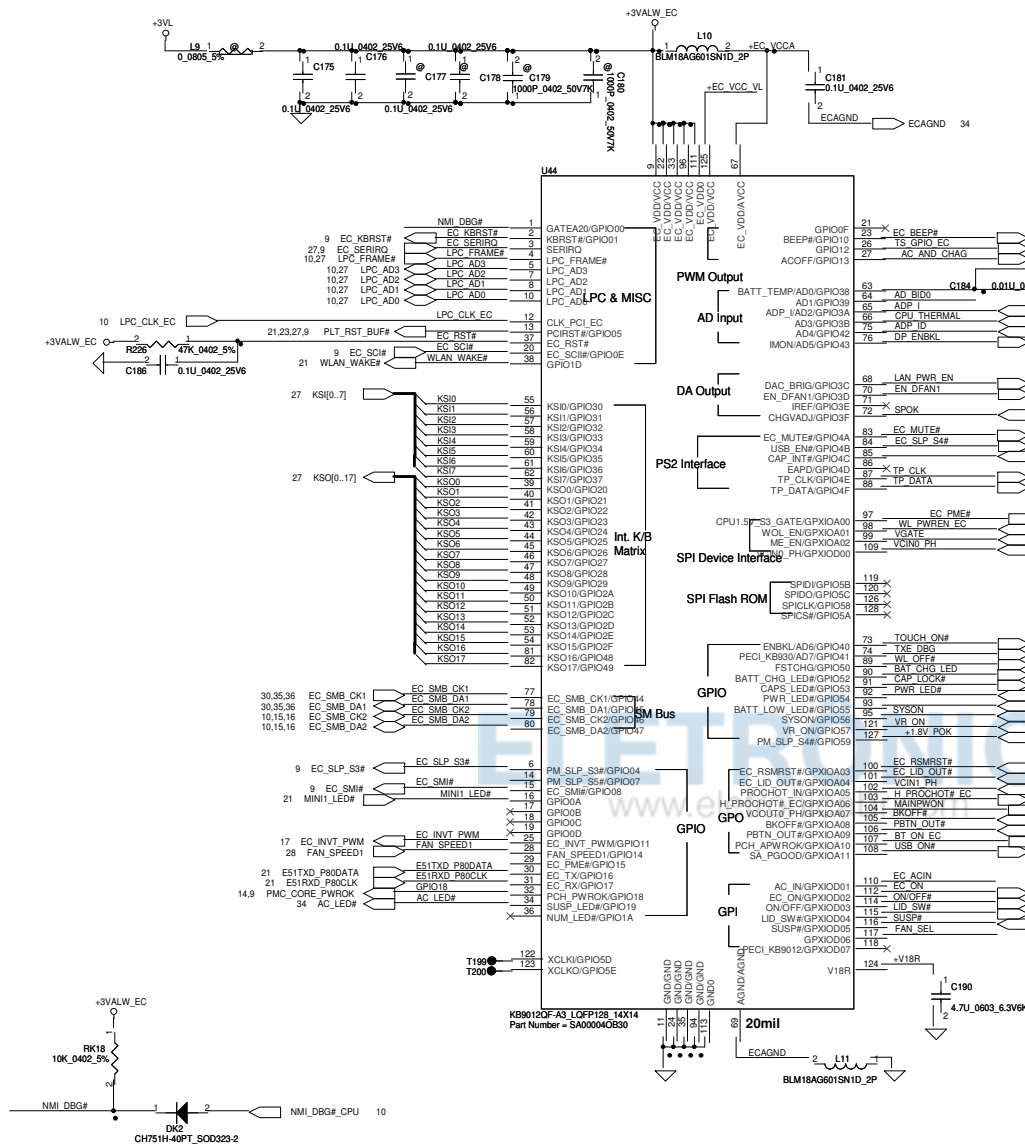
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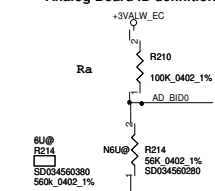
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|   |            |                    |            | Rev                      | 0.1                       |



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|   |            |                    |            | Size<br>Custom           | Document Number<br>LA-A994P |
|   |            |                    |            | Date:                    | Friday, February 21, 2014   |
|   |            |                    |            | Sheet                    | 25 of 43                    |
|   |            |                    |            | Rev                      | 0.1                         |



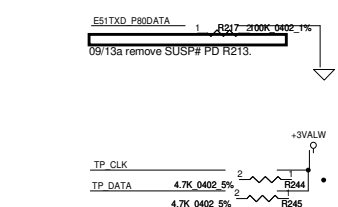
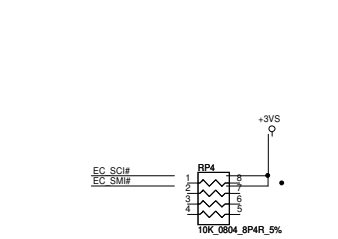
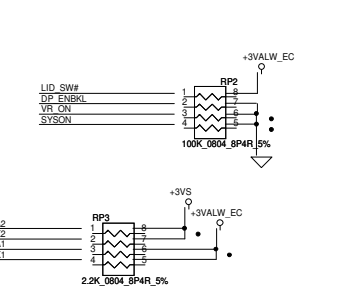
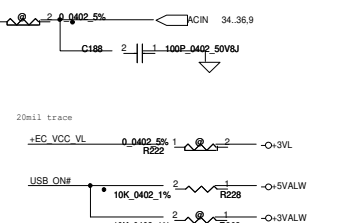
# Analog Board ID definition



| 15"             | DB       | SI       | PV       | MV       |
|-----------------|----------|----------|----------|----------|
| Board ID R214   | 12K ohm  | 20K ohm  | 33K ohm  | 56K ohm  |
| Project ID R210 | 100K ohm | 100K ohm | 100K ohm | 100K ohm |

| 15" TS          | DB       | SI       | PV       | MV       |
|-----------------|----------|----------|----------|----------|
| Board ID R214   | NA       | 100K ohm | 160K ohm | 240K ohm |
| Project ID R210 | 100K ohm | 100K ohm | 100K ohm | 100K ohm |

| 15" 6U          | DB | SI | PV       | MV       |
|-----------------|----|----|----------|----------|
| Board ID R214   | NA | NA | 330K ohm | 560K ohm |
| Project ID R210 | NA | NA | 100K ohm | 100K ohm |



Latest design guide suggest change to 74LVC1G06.

# TPM1.2

The schematic diagram illustrates the connection of the TPM1.2 module to the SLB 9656 TT 1.2 chip. The chip is represented by a central block with various pins and internal components.

**Power and Ground Connections:**

- +3V5:** Connected to VDD pins (24, 19, 10) and the VSB pin (5).
- Ground:** Connected to GND pins (4, 11, 18, 25) and the bottom terminals of capacitors C1081, C1080, and C1079.

**Capacitors:**

- C1081, C1080, C1079:** 0.1uF 0402 16V4Z capacitors connected between VDD and ground.
- C1082:** 0.1uF 0402 16V4Z capacitor connected between VSB and ground.

**Signal Connections:**

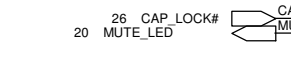
- LPC AD0-AD3:** Connected to LAD0-LAD3 pins (26, 23, 20, 17).
- LPC CLK\_TPM:** Connected to LCLK pin (21).
- LPC\_FRAME#:** Connected to LFRAME# pin (22).
- PLT\_RST\_BUF#:** Connected to LRESET# pin (16).
- EC\_SERIRQ:** Connected to SERIRQ pin (27).
- PP:** Connected to PP pin (15).
- XTALO/XTALI:** Connected to XTALO and XTALI pins (14, 13).
- GPIO2/GPIO:** Connected to GPIO2 and GPIO pins (2, 6).
- NC:** Connected to NC pins (1, 3, 12).

**Internal Chip Components:**

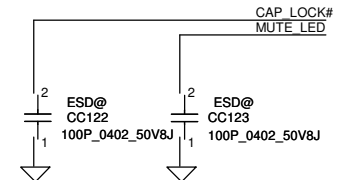
- TPM SLB 9656 TT 1.2:** The main chip block.
- R1380:** 4.7K 0402 5% resistor connected between +3V5 and PP.
- R1409:** 0.0402 5% resistor connected between PP and ground.
- R1412:** 0.0402 5% resistor connected between BADD pin (9) and PLT\_RST\_BUF#.

**Other Labels:**

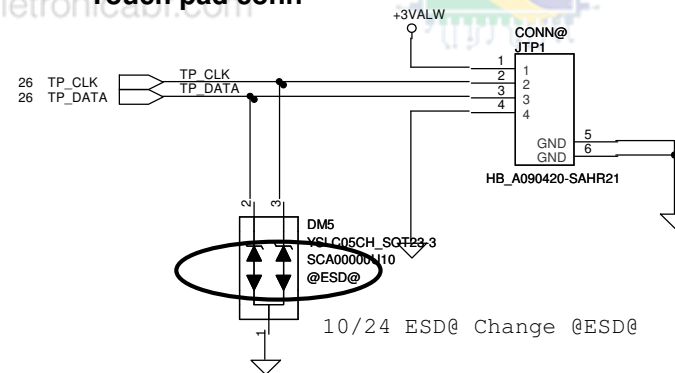
- TPM1.2:** Large text label at the top left.
- SLB 9656 TT 1.2:** Label for the chip block.
- TPM:** Label for the TPM module.
- TPM1.2:** Label for the TPM module.



|            | CONN@ JKB1 |
|------------|------------|
| KS1        | 1          |
| KS7        | 2          |
| KS16       | 3          |
| KS09       | 4          |
| KS14       | 5          |
| KS15       | 6          |
| KS00       | 7          |
| KS12       | 8          |
| KS13       | 9          |
| KS05       | 10         |
| KS01       | 11         |
| KS10       | 12         |
| KS02       | 13         |
| KS04       | 14         |
| KS07       | 15         |
| KS08       | 16         |
| KS06       | 17         |
| KS03       | 18         |
| KS012      | 19         |
| KS013      | 20         |
| KS014      | 21         |
| KS011      | 22         |
| KS010      | 23         |
| KS015      | 24         |
| KS016      | 25         |
| KS017      | 26         |
|            | 27         |
| 3K 0402 5% | 28         |
| 3K 0402 5% | 29         |
|            | 30         |
|            | 31         |
|            | 32         |

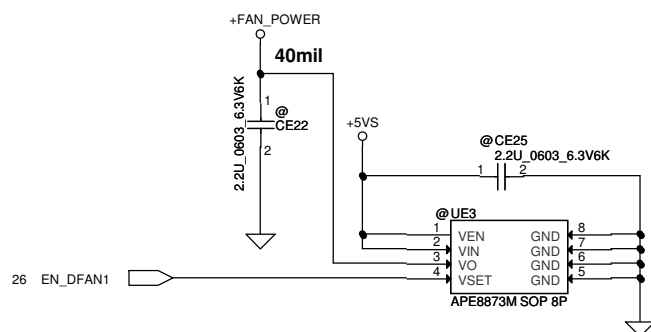
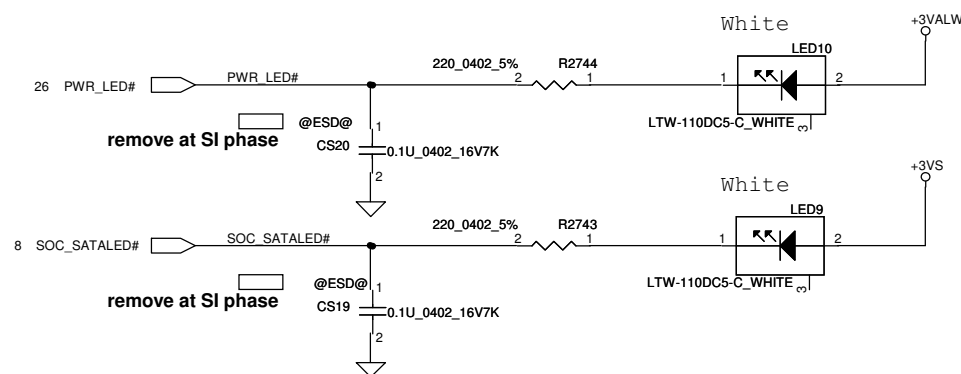
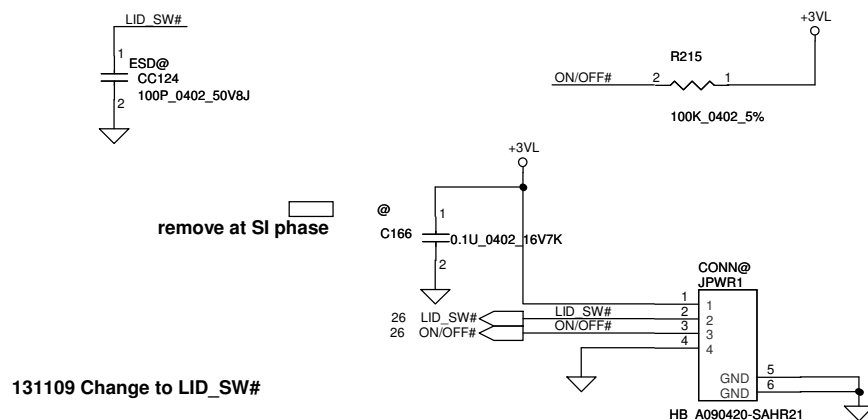


**Touch pad conn**

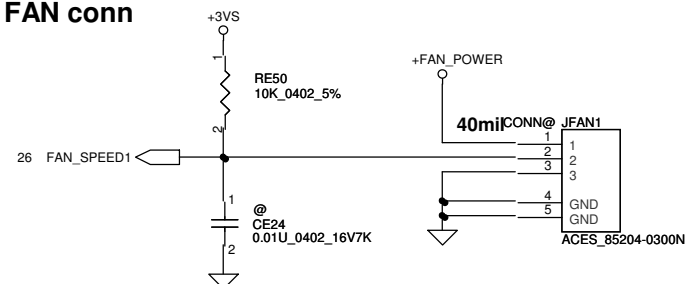


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|   |                    |                 |            | LA-A992P                 |                 |         |
| Date: Friday, February 21, 2014   |                    |                 |            | Sheet                    | 27              | of 43   |

# Power Button Connector

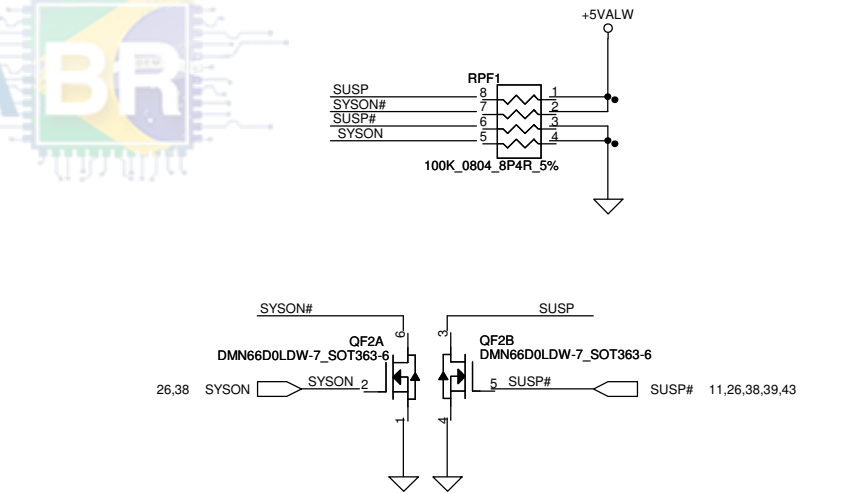
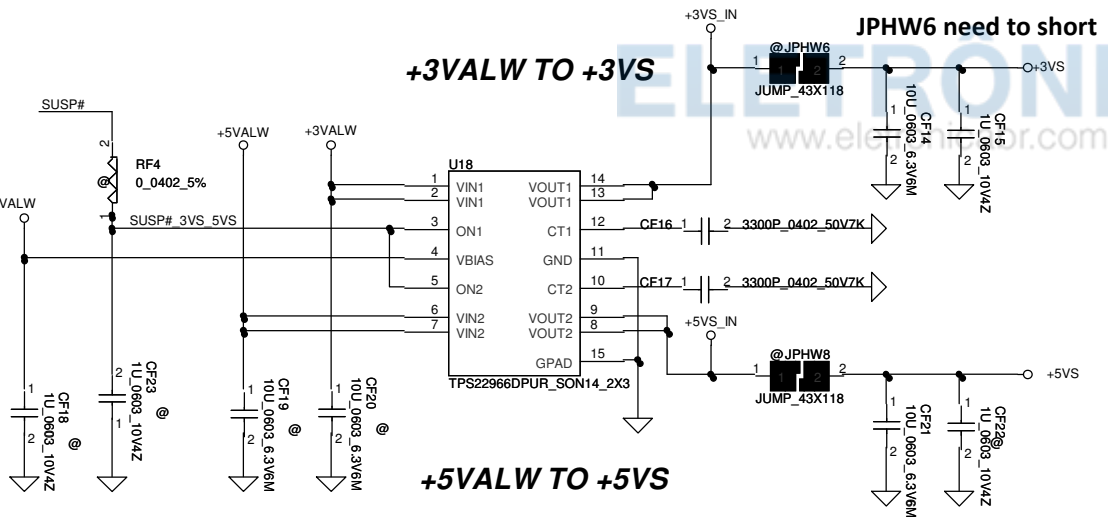
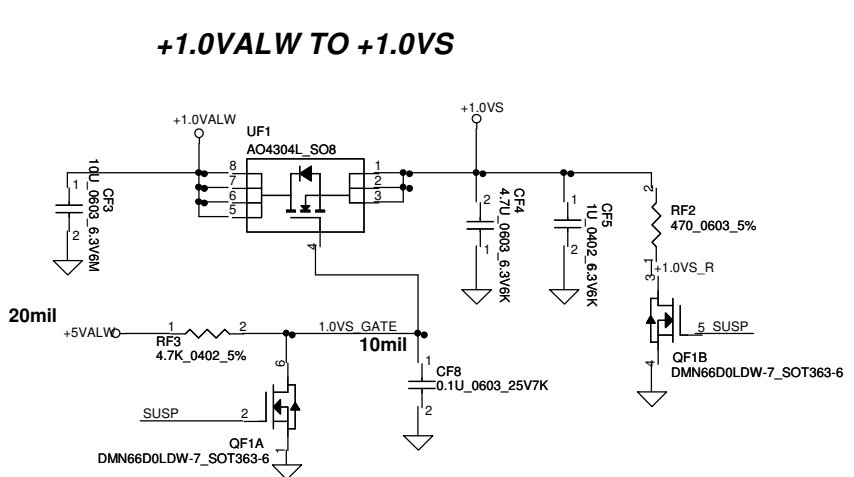
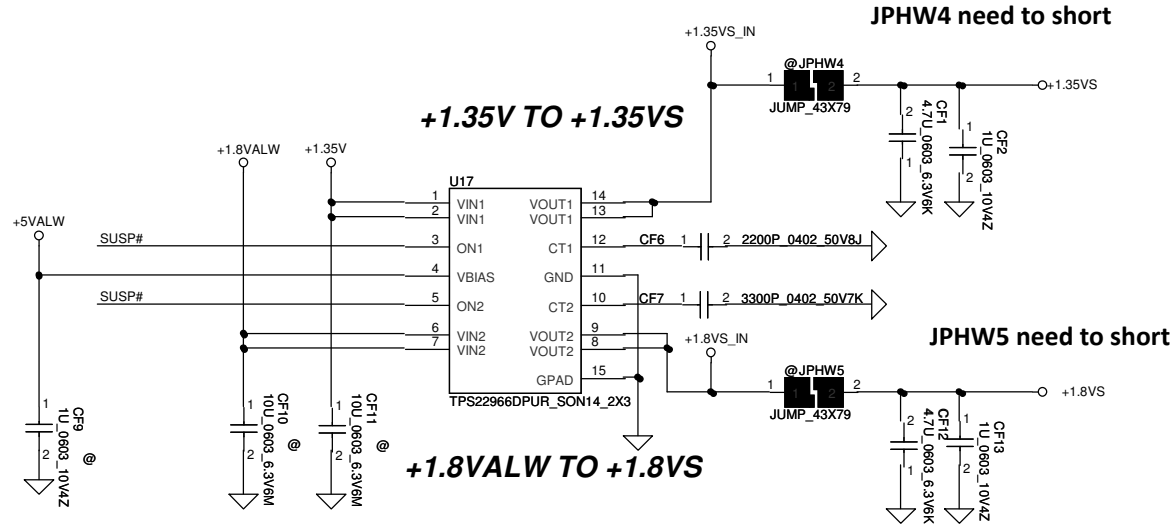


## FAN conn



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|   |                    |                 |                          | 0.1                          |
|   |                    |                 |                          | Date: Friday, March 14, 2014 |
|   |                    |                 |                          | Sheet 28 of 43               |

# Bay trail M new power up sequence

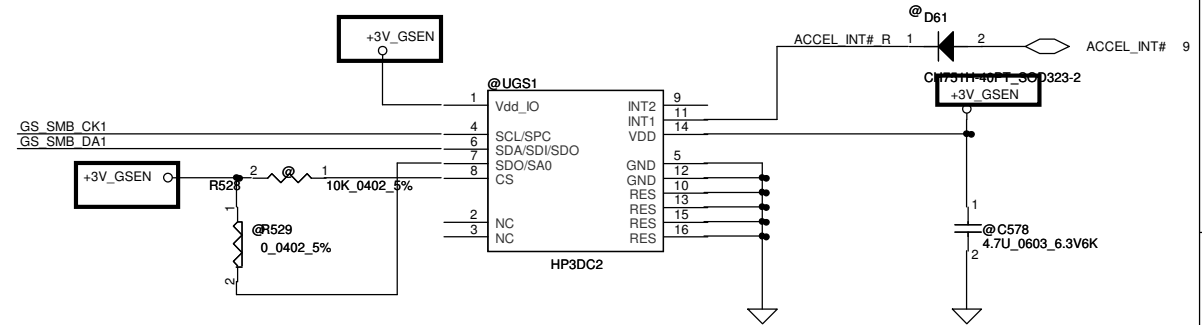


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|   |            |                    |            | Document Number          | Rev 0.1 |
| Date: Friday, February 21, 2014   |            | Sheet 29 of 43     |            |                          |         |



10/21 +3VALW Change +3VL

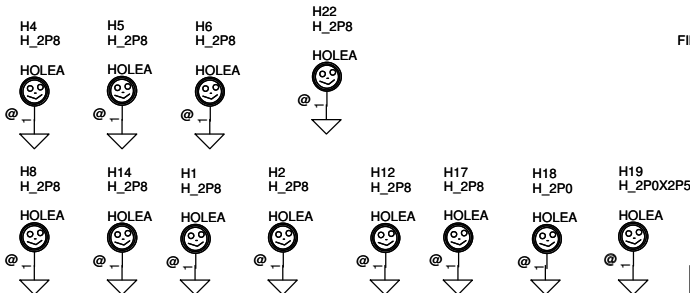
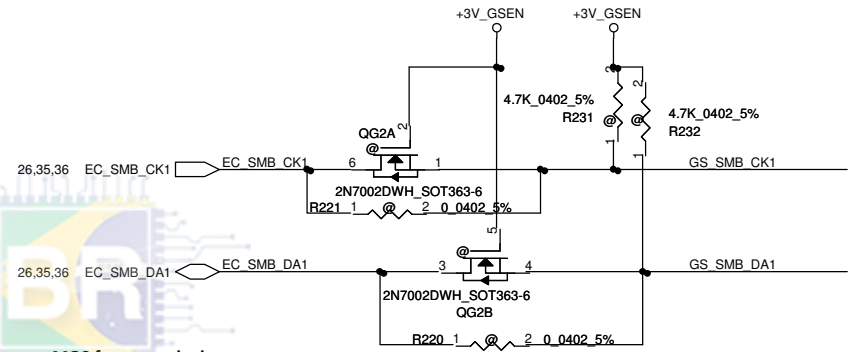
# ACCELEROMETER



Must be placed in the center of the system.

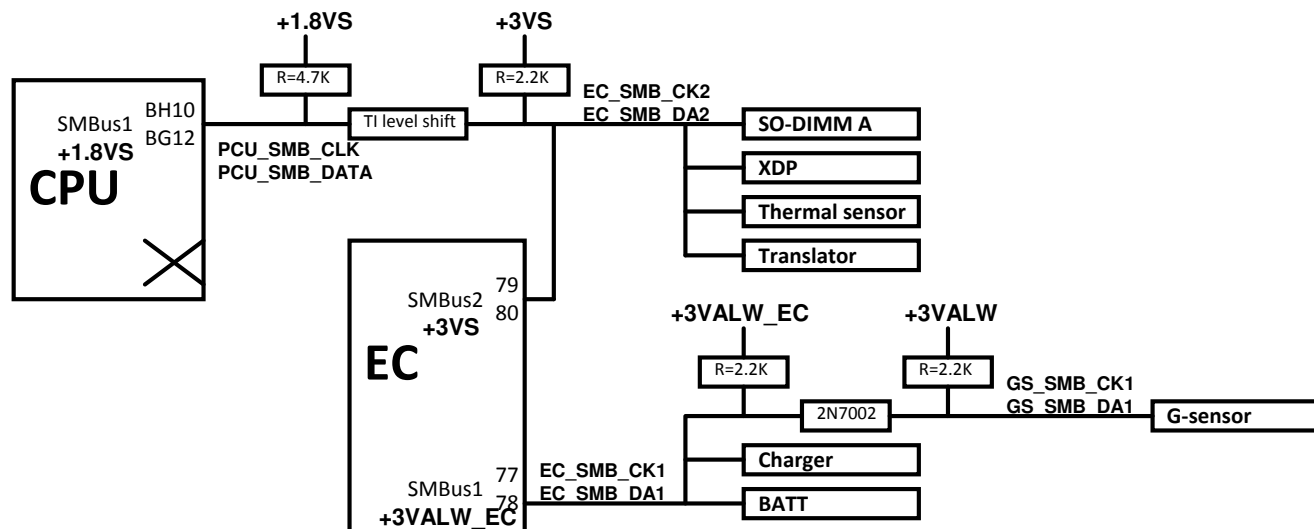
**ELETRÔNICA BR**  
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Reserve MOS for power leakage



|   |                    |                 |            |                          |                           |
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|   |                    |                 |            | Sheet                    | 30 of 43                  |
|   |                    |                 |            | Rev                      | 0.1                       |
|   |                    |                 |            | LA-A992P                 |                           |

## <SMBus Routing>



<USB2.0/3.0 port>

| USB2.0 | USB3.0   | Function                  | Note         |
|--------|----------|---------------------------|--------------|
| 0      | <b>X</b> | Left port (USB2.0)        |              |
| 1      | 0        | Right port-1 (USB2.0/3.0) |              |
| 2      | <b>X</b> | Right port-2 (USB2.0)     |              |
| 3      | <b>X</b> | WLAN                      | USB2.0x4 Hub |
| 4      | <b>X</b> | Touch screen              | USB2.0x4 Hub |
| 5      | <b>X</b> | Camera                    | USB2.0x4 Hub |
| 6      | <b>X</b> | NC                        | USB2.0x4 Hub |

<PCI-E port>

| PCI-E | Function    | Note |
|-------|-------------|------|
| 0     | LAN         |      |
| 1     | WLAN        |      |
| 2     | Card reader |      |
| 3     | NC          |      |

<SATA port>

| PCI-E | Function | Note |
|-------|----------|------|
| 0     | HDD      |      |
| 1     | NC       |      |

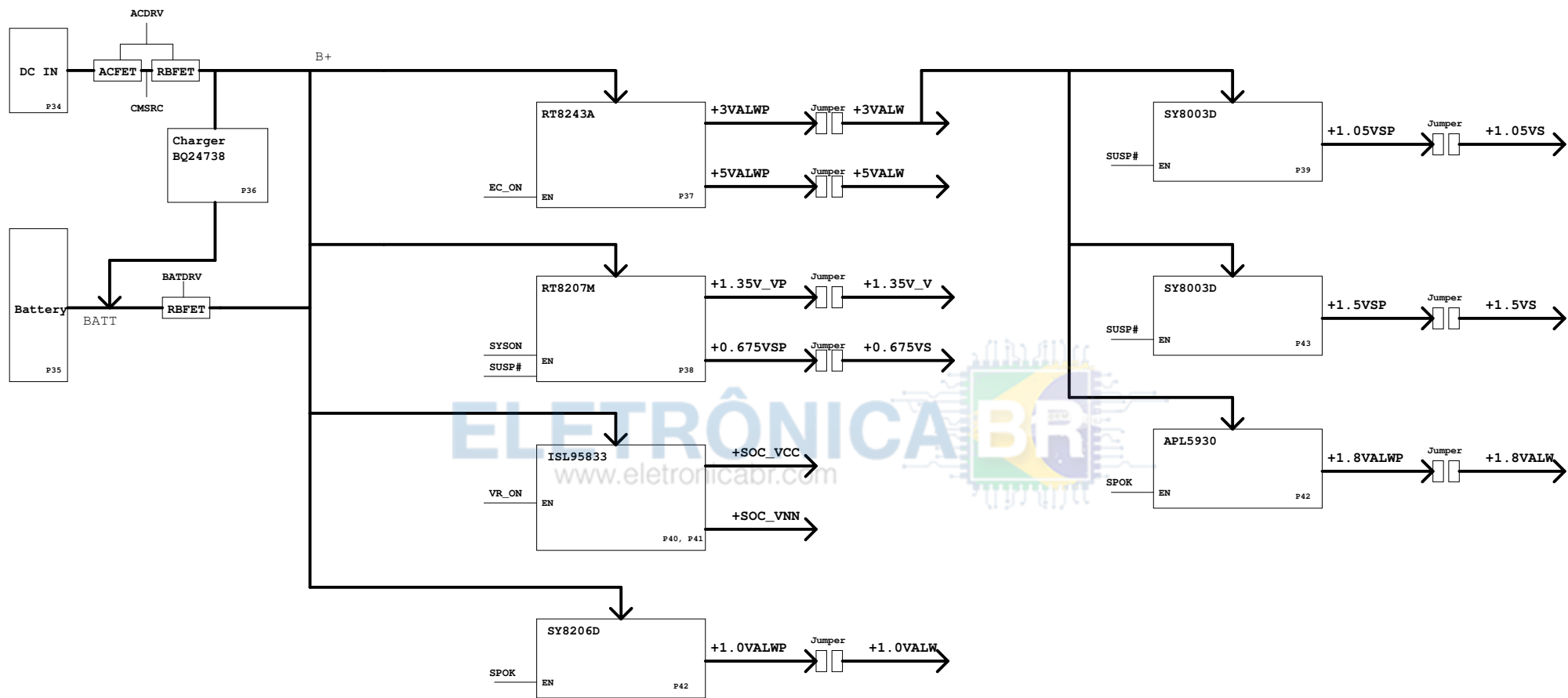


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| Date:   |          |                    |          | Sheet                    | 31              | of 43 |

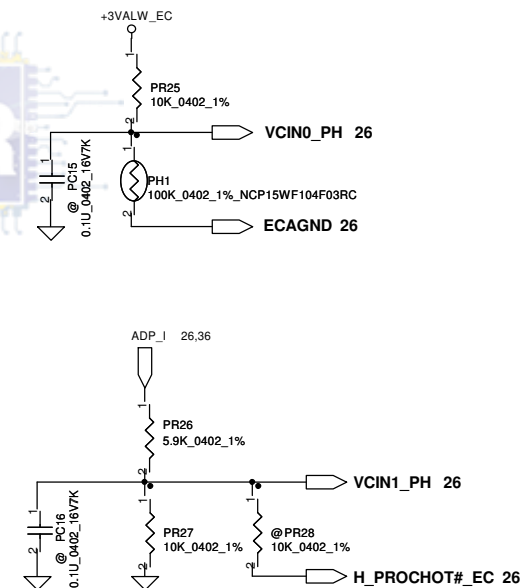
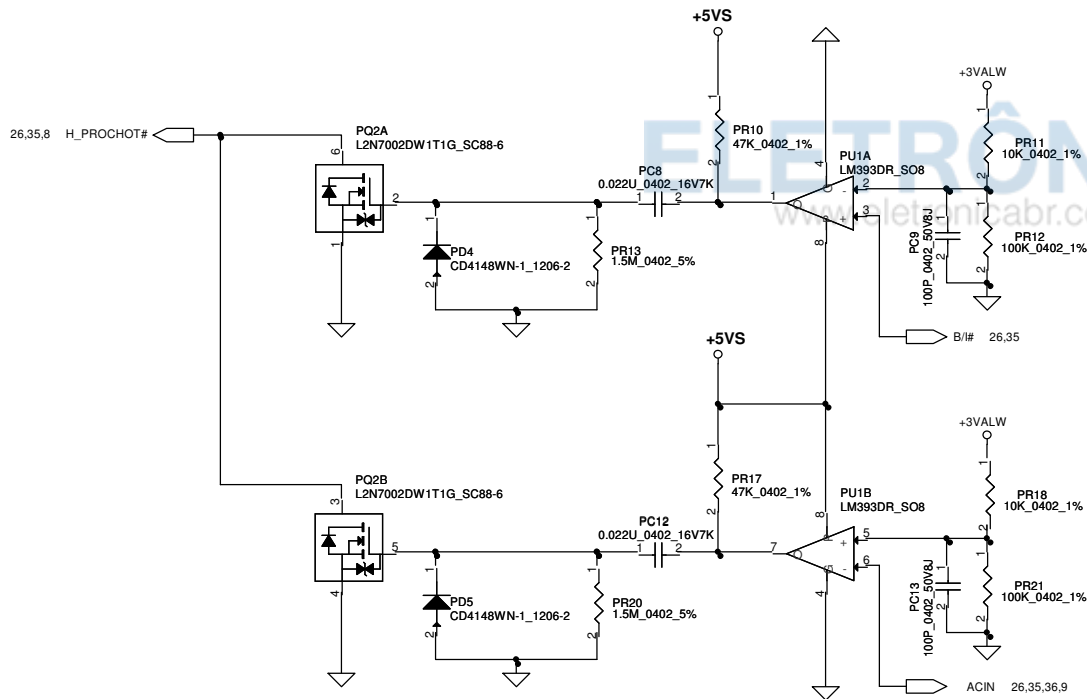
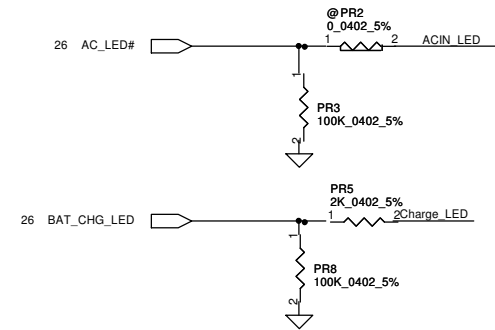
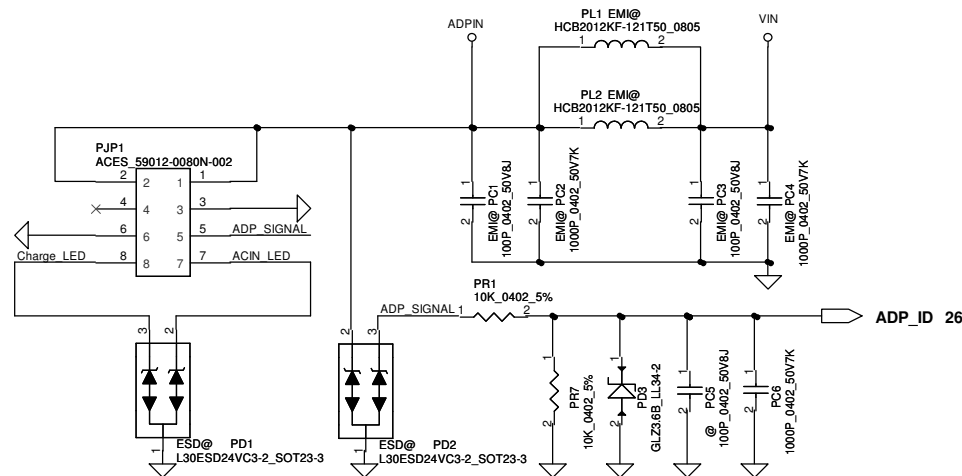
| Item | Page# | Title | Date   | Request<br>Owner | Issue Description  | Solution Description | Rev. |
|------|-------|-------|--------|------------------|--|----------------------|------|
| 1    | 29    |       | 131107 |                  | 1.Change PN of RPF1 from SD302100380 to SD309100380                  |                      |      |
| 2    | 28    |       | 131109 |                  | 1.Change Control pin of LID from NEW_LID_SW(R218) to LID_SW#(R219)   |                      |      |
| 3    | 24    |       | 131109 |                  | 1.Follow 14" Haswell LA-A993PRO2's USB2 Conn.                        |                      |      |
| 4    | 16    |       | 131111 |                  | 1.Update UT3 footprint follow Haswell platform                       |                      |      |
| 5    | 22    |       | 131111 |                  | 1.Delete R954 ,Q84 for ODD_DA# 2.unpop RS11                          |                      |      |
| 6    | 18    |       | 131111 |                  | 1.Change PN of LM13,LM14,LM15 & LM16 from SM070001V00 to SM070003K00 |                      |      |
| 7    | 30    |       | 131111 |                  | 1.Change Power Rail of G sensor from +3VALW to +3VL & unpop QG2      |                      |      |
| 8    | 30    |       | 131111 |                  | 1.pop DM5  |                      |      |
| 9    | 26    |       | 131111 |                  | 1.change Board ID to SI phase  |                      |      |
| 10   | 16    |       | 131111 |                  | 1.add PD 100K RT15K for power sequence                               |                      |      |



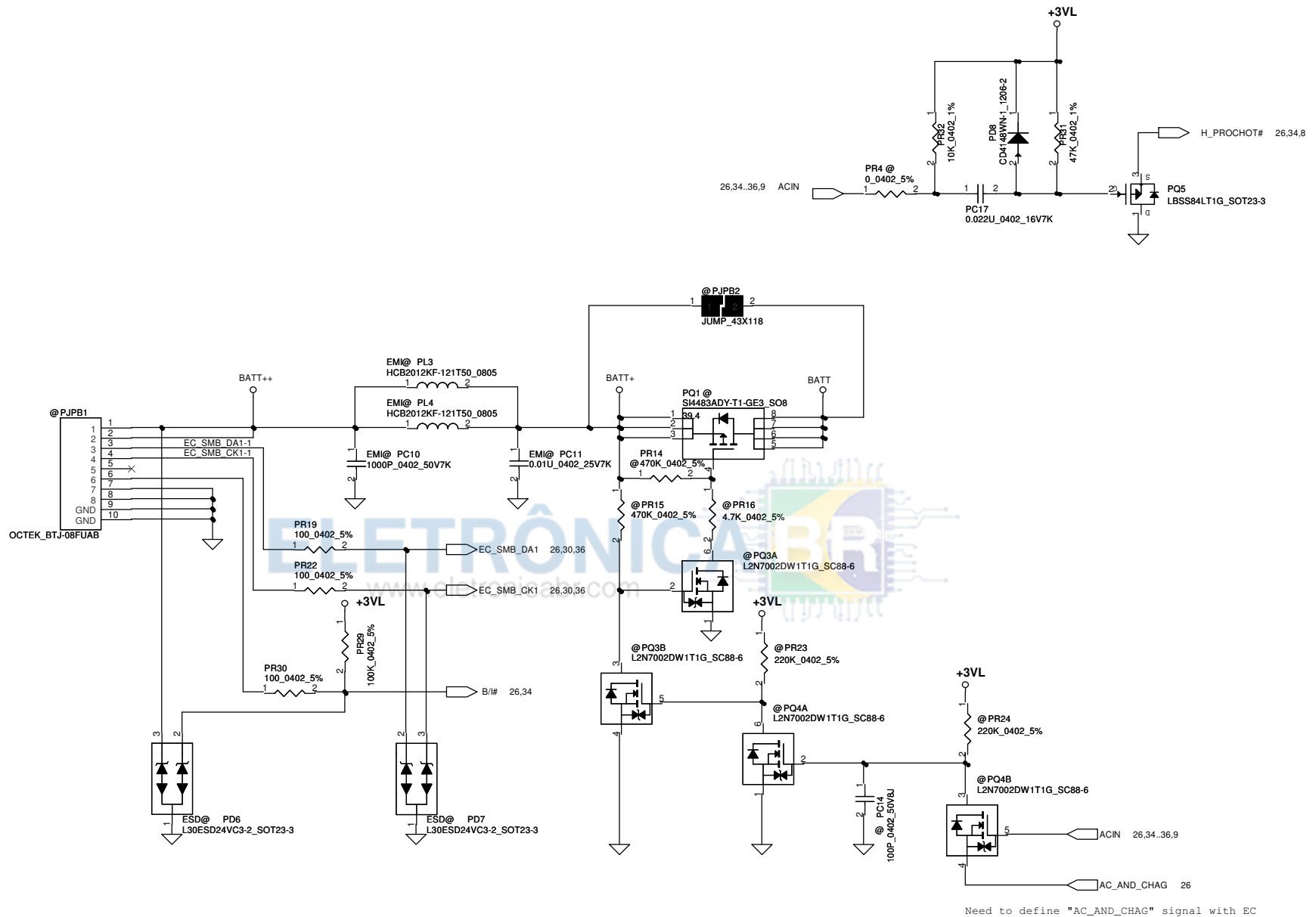
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|   |                    |                 |            | Sheet                    | 32                        | of 43 |



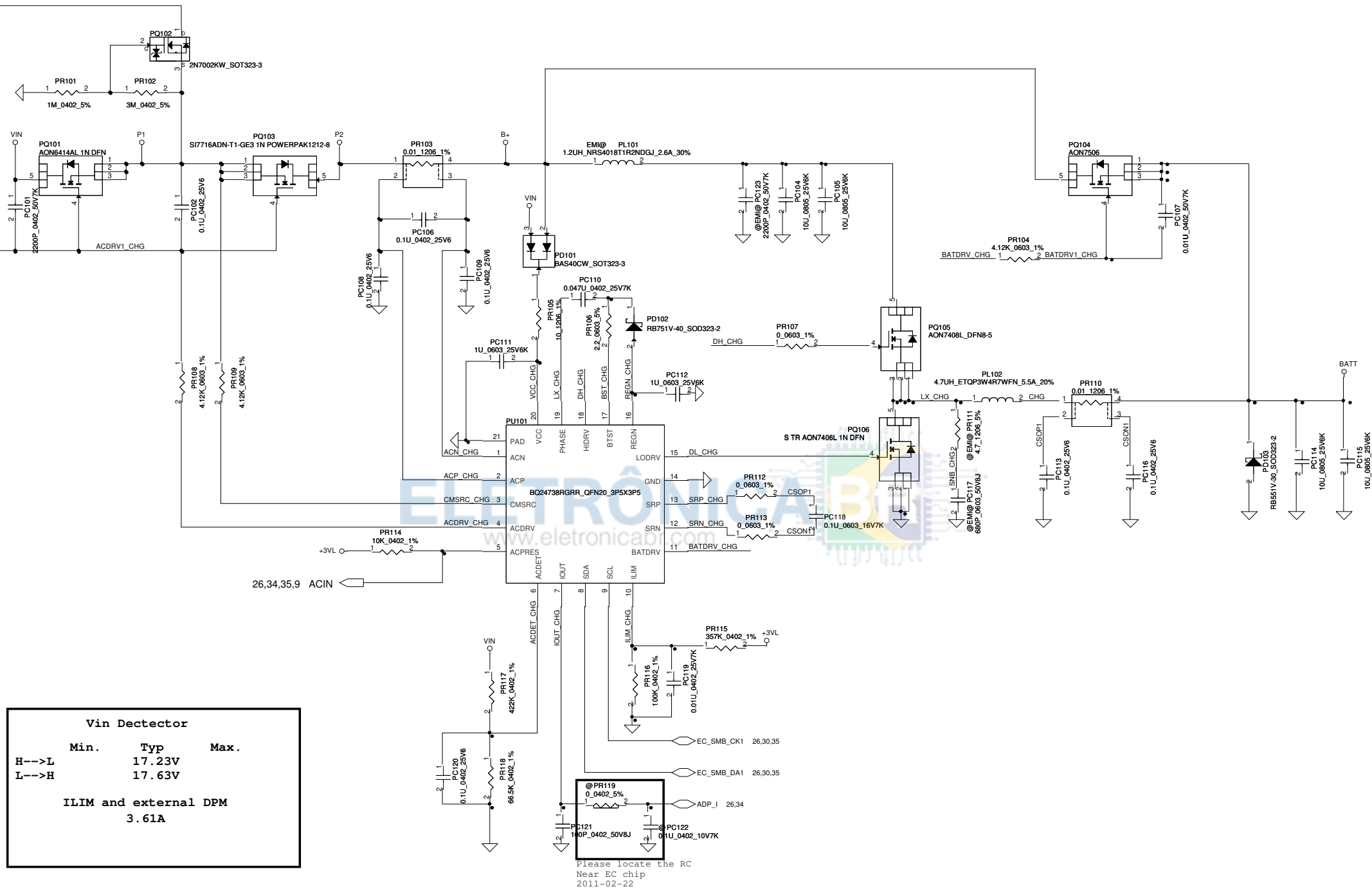
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|   |            |                    |            | Sheet                    | 34 of 43                  |



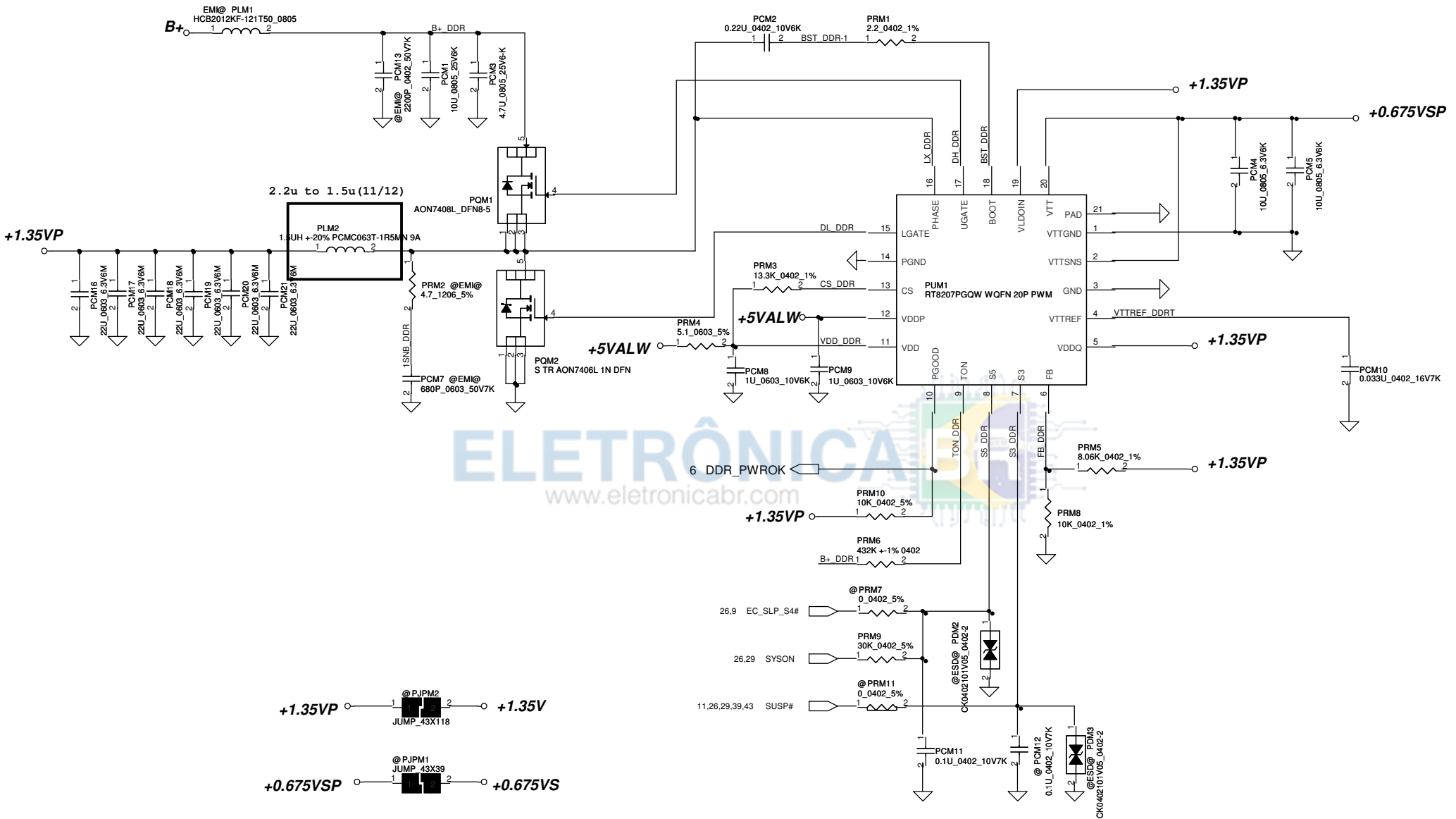
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| Size  | Custom                    | Document Number    | LA-A521P   | Rev                      | 0.1 |
| Date:   | Monday, February 24, 2014 | Sheet              | 38         | of                       | 43  |



**Design Note**  
 This circuit is for ULC 1+1 7.5W.  
 CPU: Icc=12A  
 Loadline: -5.9 m V/A  
 GFX(GT2): Icc=14A  
 Loadline: -5.9 m V/A

For VR\_HOT#, already  
 pull high at power side.

PR18 and PR30  
 27.4K ohm for 100 degree  
 61.9K ohm for 110 degree

**Layout Note**  
 SVID routing  
 1. Alert# signal must be routed between the Clock and Date lines to reduce the cross talk between them. Signal order arrangement: mobile order is Clock-Alert-Date.  
 2. SVID spacing requirement is 18mils(0.475mm)/VSSSENSE  
 3. Maximum total microstrip routing length of each SVID signal must not exceed 6000mils(152.4mm).  
 4. The SVID bus must be ground reference, It cannot be referenced to input (Vbat or 12V) power plans as they can couple noise into the SVID bus as power states change.  
 5. Avoid routing under noisy circuit, e.g. switch node, Gate driver, B+, Vin, high speed signal.  
 6. When SVID signal changes Layer, GND return path may be changed also. We need add GND via for GND reference.

Close GFX choke

Close GFX L/S MOS

Close CPU L/S MOS

$C_n = L / ((R_{ntcnet} * R_{sum}) / (R_{ntcnet} + R_{sum})) * DCR$   
 If  $C_n$  is correctly selected, when the load current has a square change, the output voltage also has a square response.

**Layout Note**  
 Reduce Acoustic Noise  
 1. The AL bulk capacitor of B+ should be very close to CPU\_CORE MOSFET.  
 2. Input ceramic caps must place on symmetry same location on top side and bottom side.

MDV1525 Vds=30V  
 Rds(on)=11.5-14m ohm@Vgs=4.5V

MDU1511 Vds=30V  
 Rds(on)=2.7-3.3m ohm@Vgs=4.5V

VDD source use +5VS and PG00D source use +3VS  
 Please confirm power on and down sequence, make sure VGATE after CPU\_CORE on.

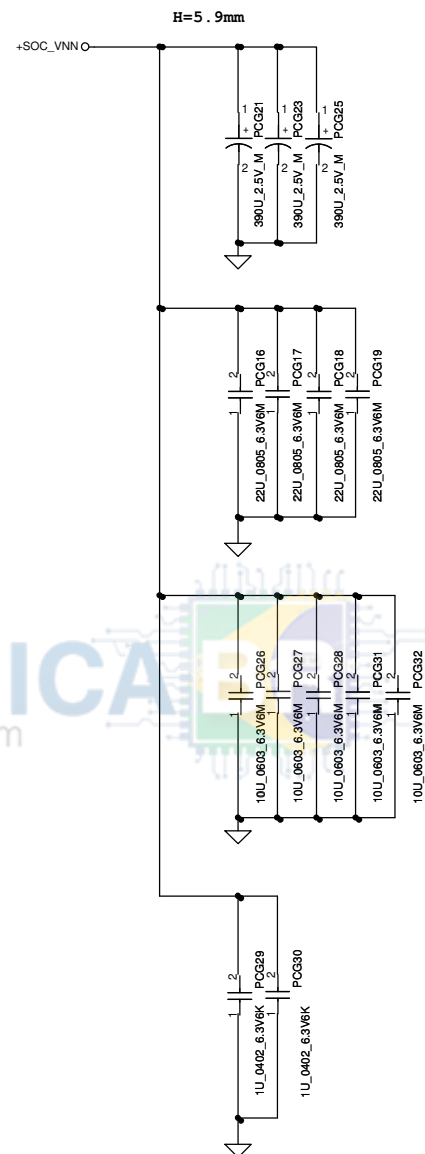
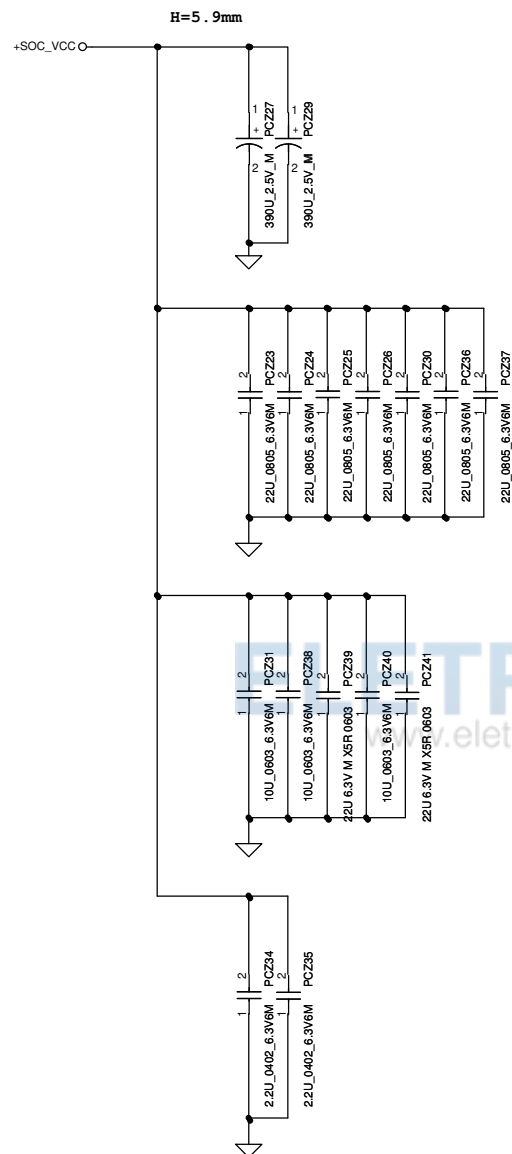
MDV1525 Vds=30V  
 Rds(on)=11.5-14m ohm@Vgs=4.5V

MDU1511 Vds=30V  
 Rds(on)=2.7-3.3m ohm@Vgs=4.5V

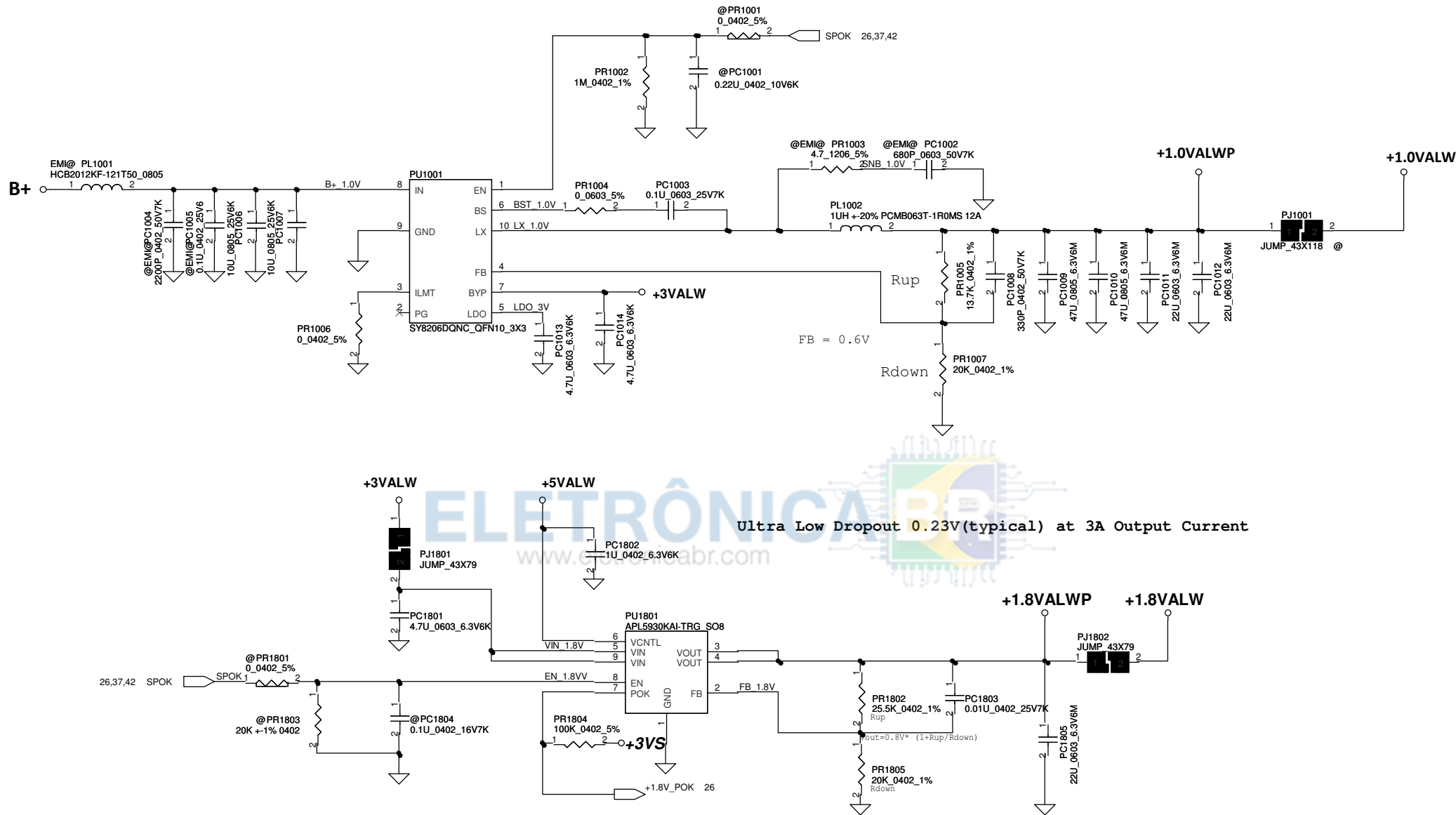
OCP setting=-20A

OCP setting=-18A

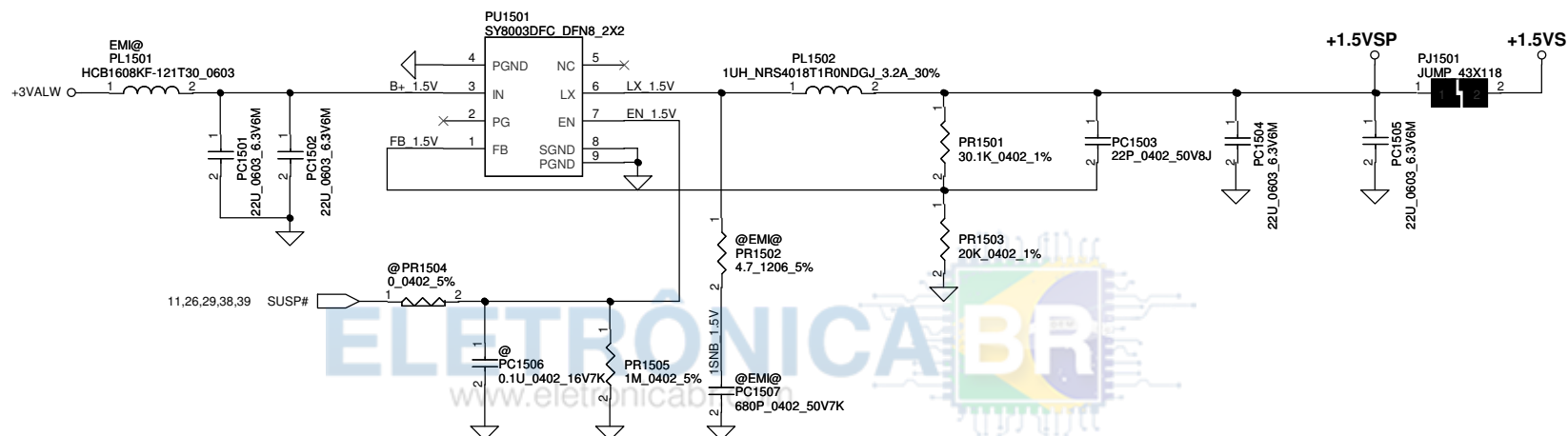
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| Sheet  |                    |                 | 40 of 43                  |
| Rev  |                    |                 | 0.1                       |



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|   |            |                    |            | Sheet                    | 43 of 43                  |
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