MS-7120

Version 1.0

INTEL (R) Brookdale-GV Chipset
Willamette/Northwood/533Prescott 478pin mPGA-B Processor Schematics

CPU: **Willamette/Northwood/533Prescott mPGA-478B Processor**

System Chipset:

INTEL Brookdale-GV GMCH + ICH4

On Board Chipset:

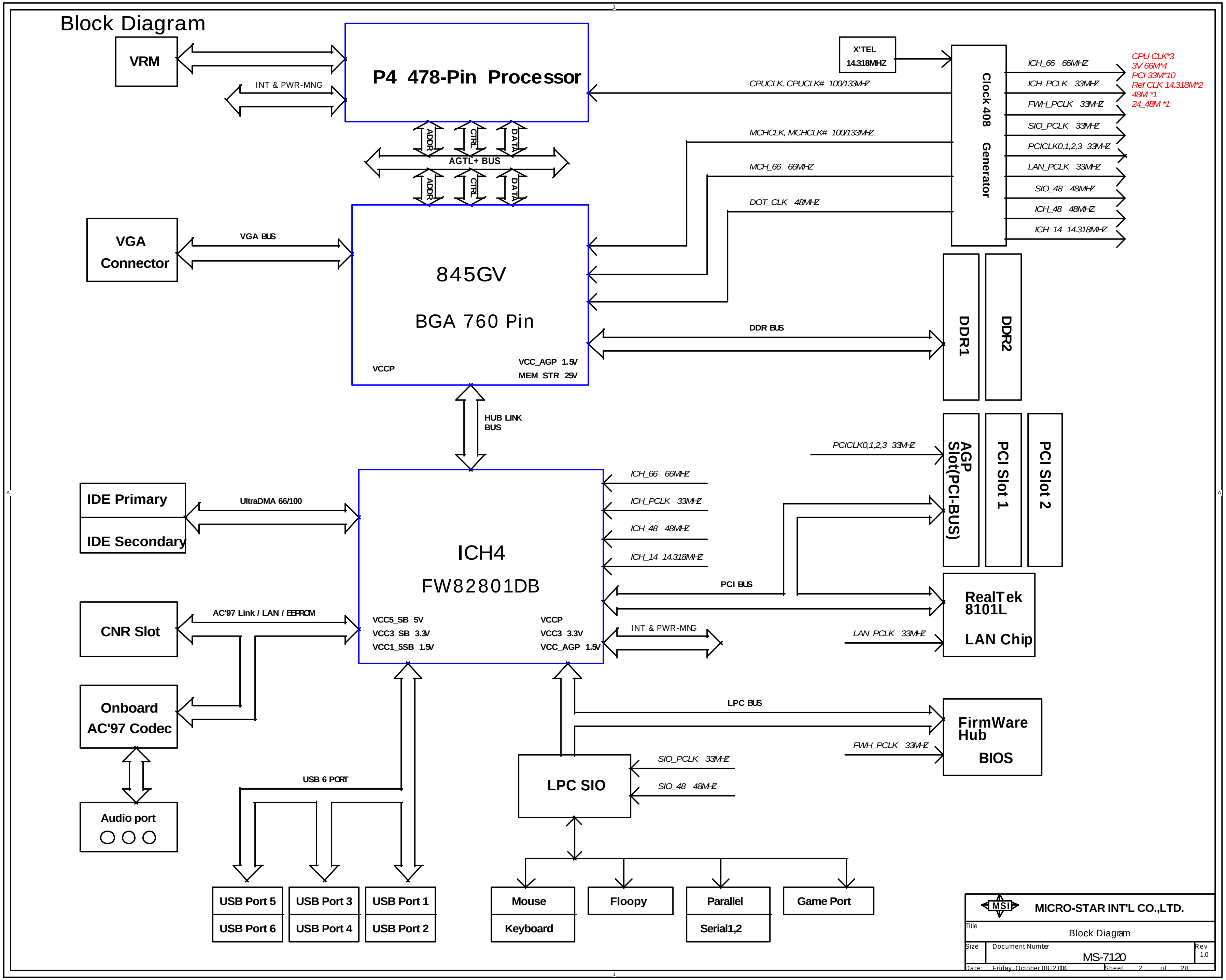
- **BIOS -- FWH**
- **LPC Super I/O -- W83627HF-AW**
- **Clock Generator -- CY28349**
- **AC'97 Codec -- RealTek ALC650/655**
- **Onboard Lan Chipset-- RealTek RTL8101L**

Expansion Slots:

- **AGP2.0 SLOT * 1 (PCI-BUS)**
- **PCI2.2 SLOT * 2**

Platform: **Micro ATX**

MODEL Config.	ORCAD Config.	Function	Option	ERP Number
MS7120-0A	cfg7120GV-LAN	GV+LAN+Com2	L	601-7120-A10
MS7120-100	cfg7120GV-LAN	GV+LAN+Com2	L	601-7120-???


Block Diagram
VRM
INT & PWR-MNG
P4 478-Pin Processor
X'TEL
14.318MHZ
Clock 408 Generator
CPUCLK, CPUCLK# 100/133MHZ
MCHCLK, MCHCLK# 100/133MHZ
MCH_66 66MHZ
DOT_CLK 48MHZ
ICH_66 66MHZ
ICH_PCLK 33MHZ
FWH_PCLK 33MHZ
SIO_PCLK 33MHZ
PCICLK0,1,2,3 33MHZ
LAN_PCLK 33MHZ
SIO_48 48MHZ
ICH_48 48MHZ
ICH_14 14.318MHZ
CPU CLK*3
3V 66M*4
PCI 33M*10
Ref CLK 14.318M*2
48M *1
24_48M *1
ADDR
CTRL
DATA
AGTL+ BUS
VGA Connector
VGA BUS
845GV
BGA 760 Pin
VCCP
VCC_AGP 1.5V
MEM_STR 2.5V
DDR BUS
DDR1
DDR2
HUB LINK BUS
PCICLK0,1,2,3 33MHZ
AGP Slot(PCI-BUS)
PCI Slot 1
PCI Slot 2
IDE Primary
IDE Secondary
UltraDMA 66/100
ICH4
FW82801DB
VCC5_SB 5V
VCC3_SB 3.3V
VCC1_5SB 1.5V
VCCP
VCC3 3.3V
VCC_AGP 1.5V
ICH_66 66MHZ
ICH_PCLK 33MHZ
ICH_48 48MHZ
ICH_14 14.318MHZ
PCI BUS
RealTek 8101L
LAN Chip
LAN_PCLK 33MHZ
INT & PWR-MNG
CNR Slot
AC'97 Link / LAN / EEPROM
Onboard AC'97 Codec
Audio port
LPC BUS
FirmWare Hub
BIOS
FWH_PCLK 33MHZ
LPC SIO
SIO_PCLK 33MHZ
SIO_48 48MHZ
USB 6 PORT
USB Port 5
USB Port 6
USB Port 3
USB Port 4
USB Port 1
USB Port 2
Mouse
Keyboard
Floopy
Parallel
Serial1,2
Game Port
MSI
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Block Diagram
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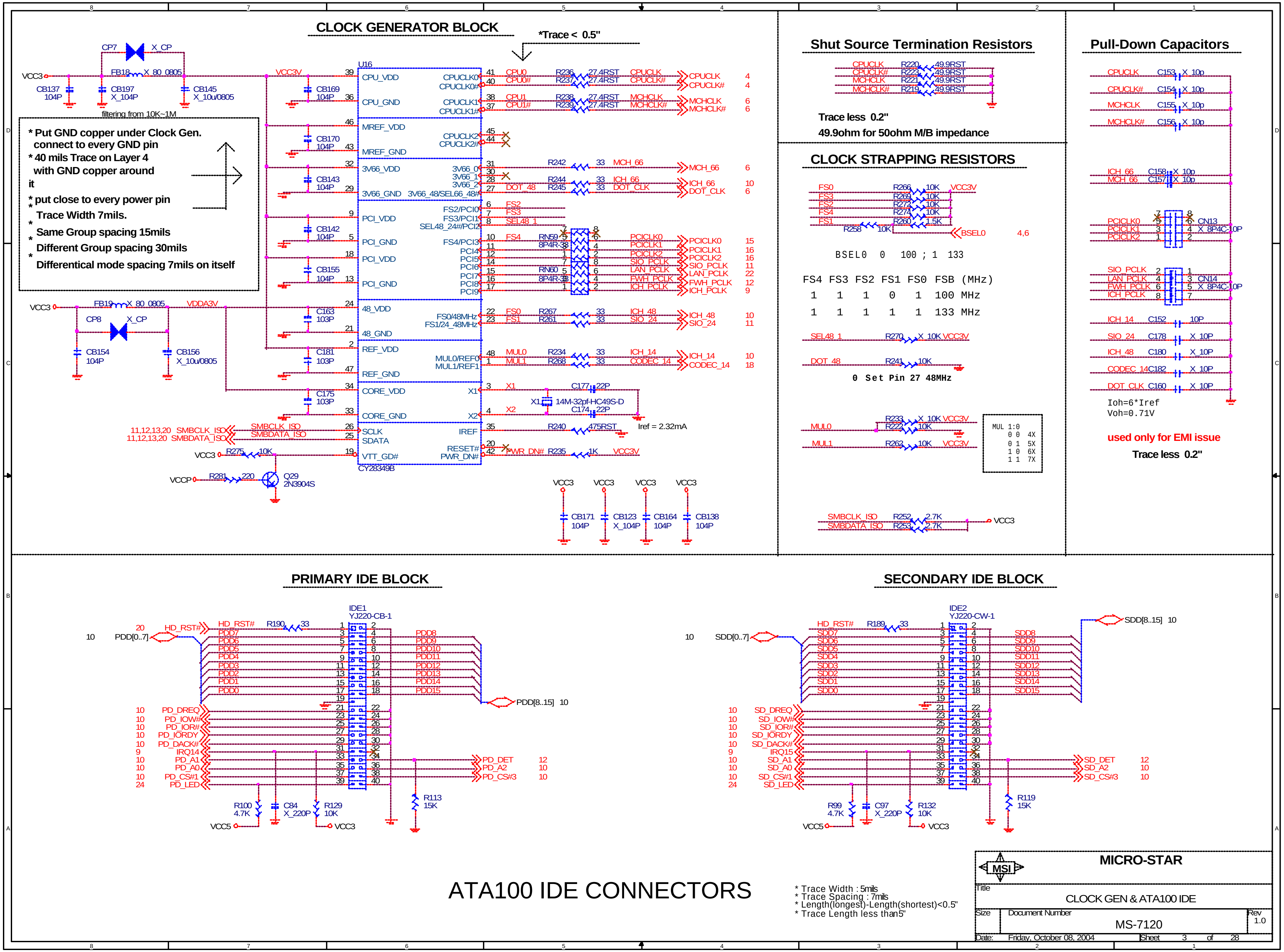
CLOCK GENERATOR BLOCK
*Trace < 0.5"
* Put GND copper under Clock Gen. connect to every GND pin
* 40 mils Trace on Layer 4 with GND copper around it
* put close to every power pin
* Trace Width 7mils.
* Same Group spacing 15mils
* Different Group spacing 30mils
* Differential mode spacing 7mils on itself
filtering from 10K~1M
U16
CY28349B
Iref = 2.32mA
Shut Source Termination Resistors
Trace less 0.2"
49.9ohm for 50ohm M/B impedance
CLOCK STRAPPING RESISTORS
BSEL0 0 100 ; 1 133
FS4 FS3 FS2 FS1 FS0 FSB (MHz)
1 1 1 0 1 100 MHz
1 1 1 1 1 133 MHz
0 Set Pin 27 48MHz
MUL 1:0
0 0 4X
0 1 5X
1 0 6X
1 1 7X
Pull-Down Capacitors
Ioh=6*Iref
Voh=0.71V
used only for EMI issue
Trace less 0.2"
PRIMARY IDE BLOCK
IDE1
YJ220-CB-1
SECONDARY IDE BLOCK
IDE2
YJ220-CW-1
ATA100 IDE CONNECTORS
* Trace Width : 5mils
* Trace Spacing : 7mils
* Length(longest)-Length(shortest)<0.5"
* Trace Length less than5"
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CLOCK GEN & ATA100 IDE
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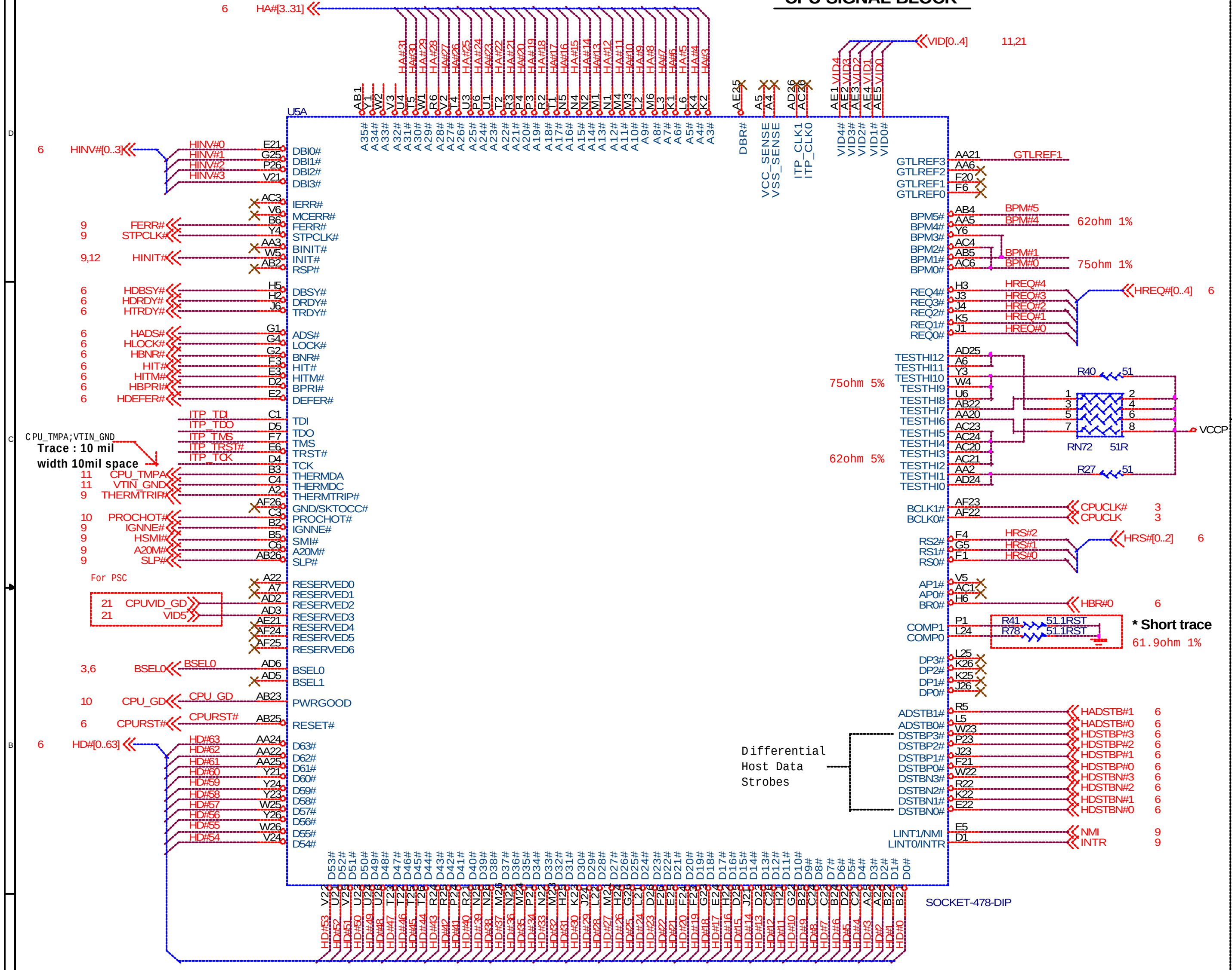
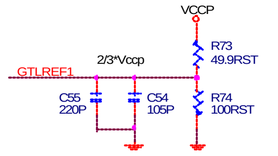
CPU SIGNAL BLOCK



CPU GTL REFERNCE VOLTAGE BLOCK

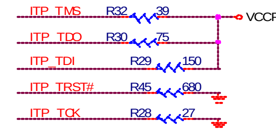


Every pin put one 220pF cap near it.

Trace Width 10mils, Space 15mils.

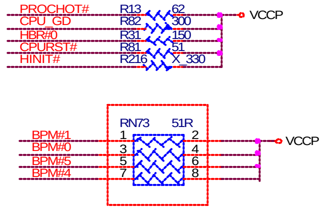
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

CPU ITP BLOCK



ALL COMPONENTS CLOSE TO CPU

CPU STRAPPING RESISTORS



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Title	INTEL mPG478 CPU1	
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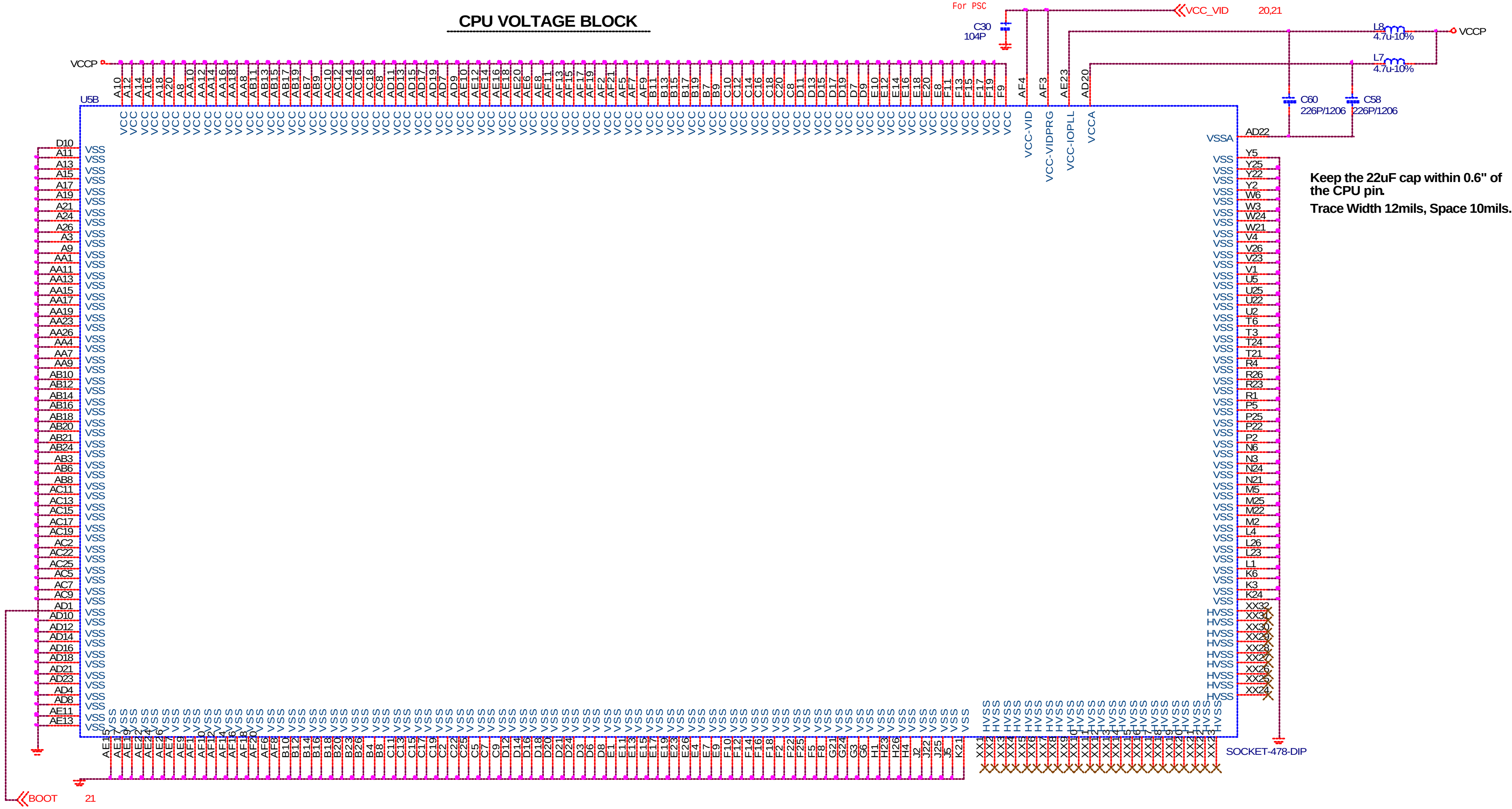
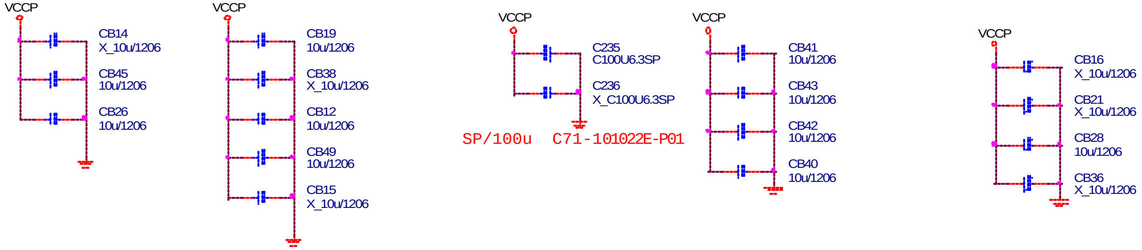
CPU VOLTAGE BLOCK



Keep the 22uF cap within 0.6" of the CPU pin.

Trace Width 12mils, Space 10mils.

CPU DECOUPLING CAPACITORS



SP/100u C71-101022E-P01

MICRO-STAR

Title	INTEL mPGA478-B CPU2
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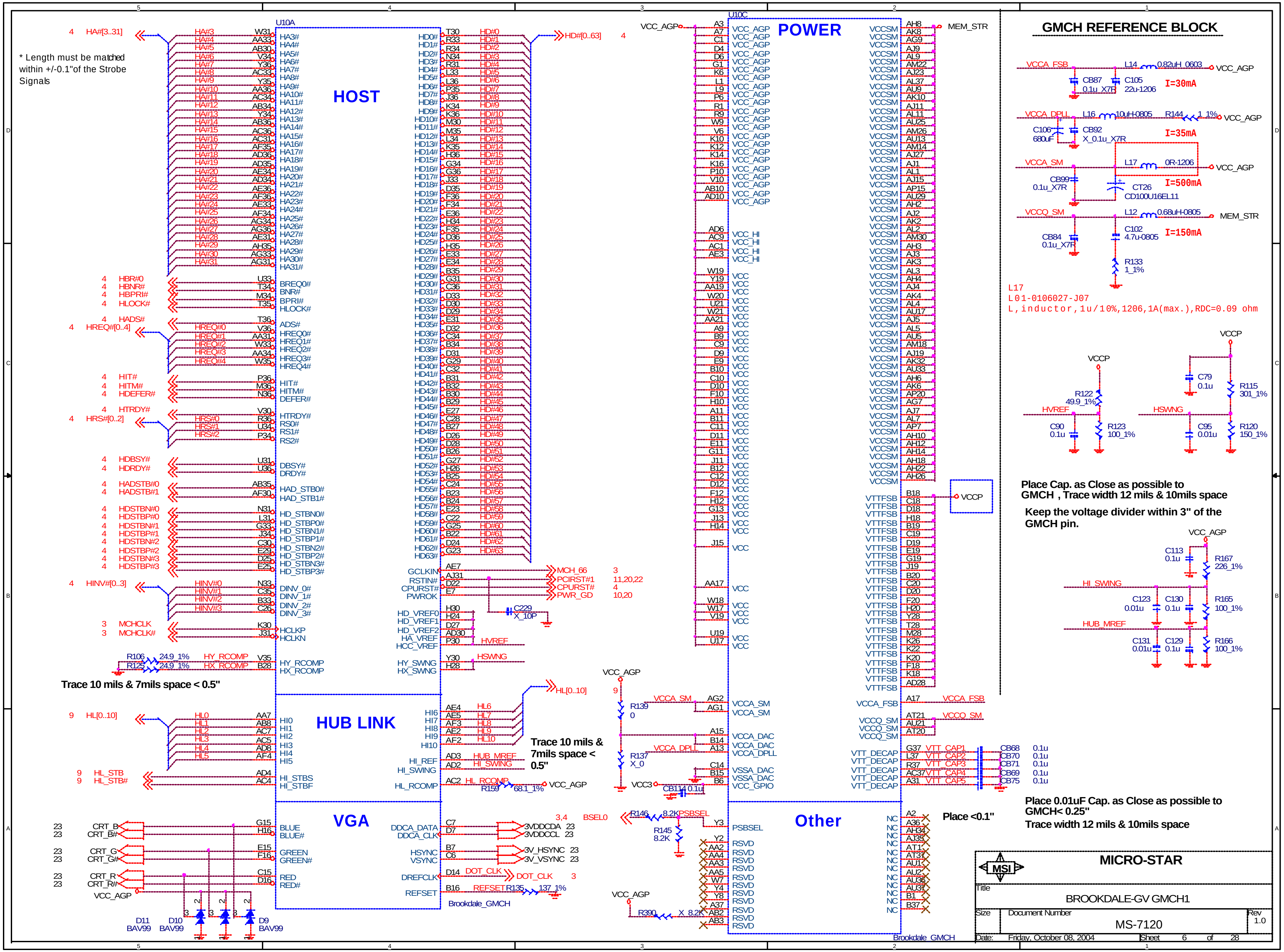

* Length must be matched within +/-0.1"of the Strobe Signals

Trace 10 mils & 7mils space < 0.5"

Trace 10 mils & 7mils space < 0.5"

Place Cap. as Close as possible to GMCH , Trace width 12 mils & 10mils space

Keep the voltage divider within 3" of the GMCH pin.

Place <0.1"

Place 0.01uF Cap. as Close as possible to GMCH< 0.25"
Trace width 12 mils & 10mils space

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Title	BROOKDALE-GV GMCH1
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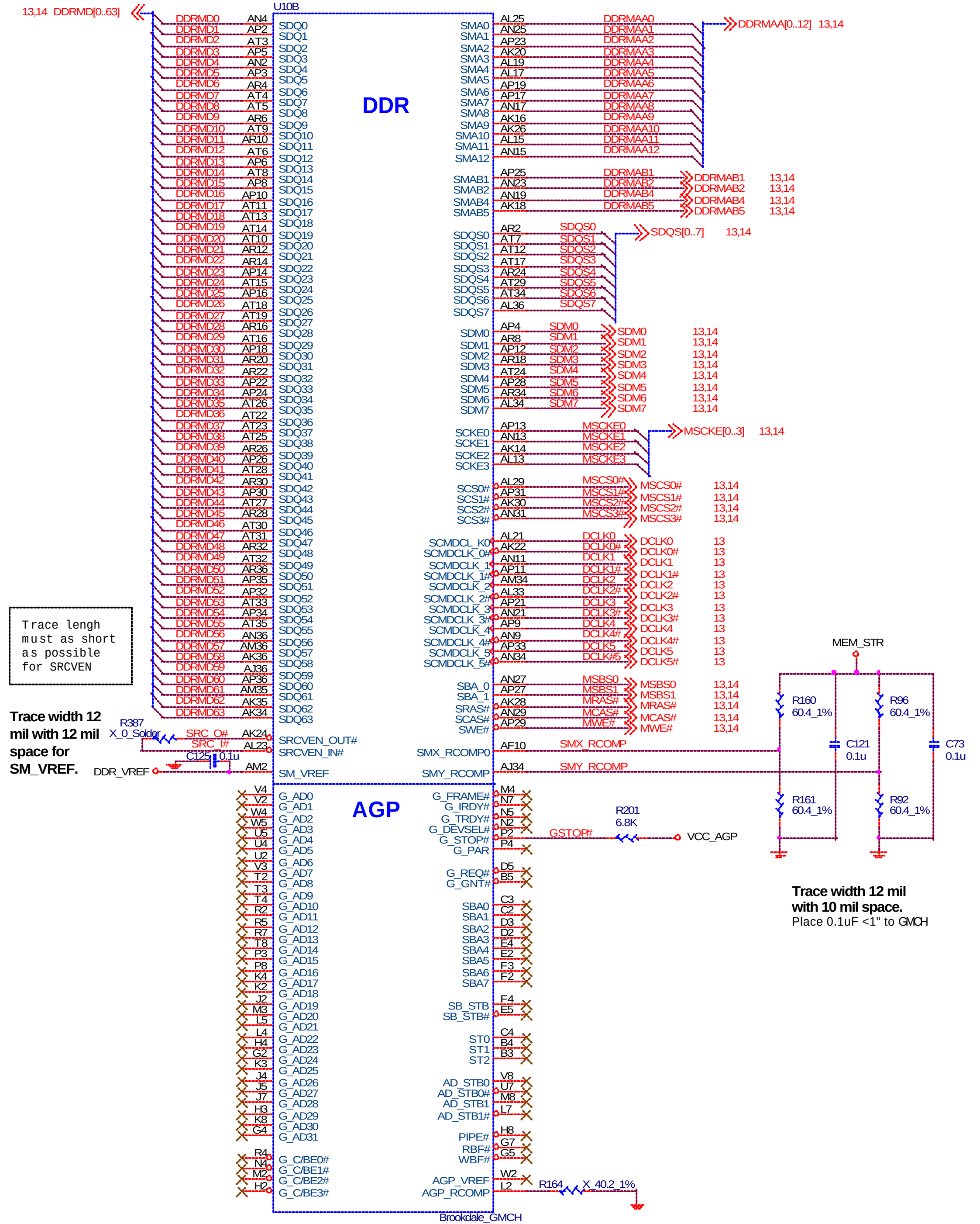

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Title: BROOKDALE-GV GMCH2

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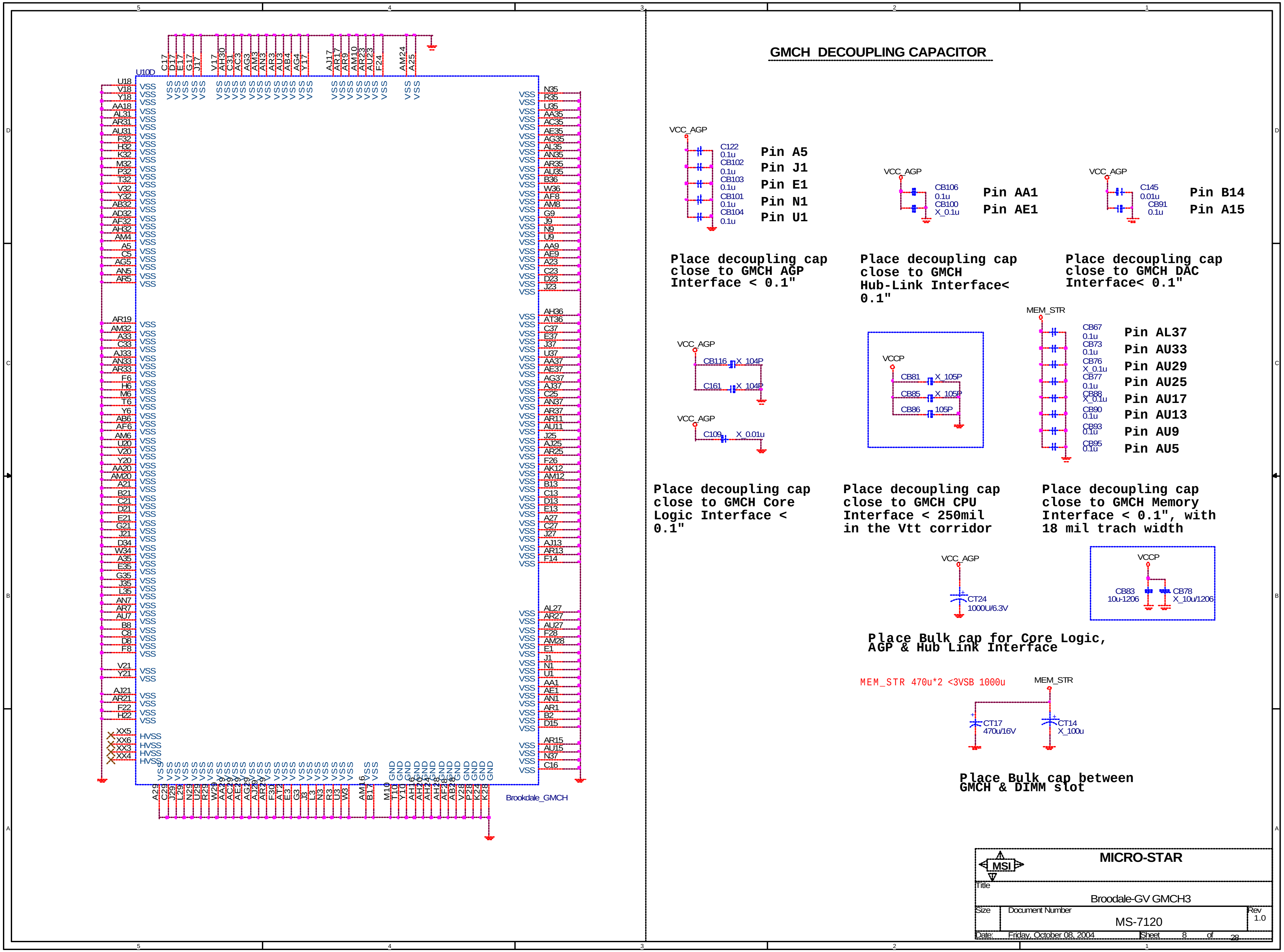

GMCH DECOUPLING CAPACITOR
U10D
Brookdale_GMCH
VCC_AGP
C122 0.1u
CB102 0.1u
CB103 0.1u
CB101 0.1u
CB104 0.1u
Pin A5
Pin J1
Pin E1
Pin N1
Pin U1
CB106 0.1u
CB100 X_0.1u
Pin AA1
Pin AE1
C145 0.01u
CB91 0.1u
Pin B14
Pin A15
Place decoupling cap close to GMCH AGP Interface < 0.1"
Place decoupling cap close to GMCH Hub-Link Interface< 0.1"
Place decoupling cap close to GMCH DAC Interface< 0.1"
CB116 X_104P
C161 X_104P
C109 X_0.01u
VCCP
CB81 X_105P
CB85 X_105P
CB86 105P
MEM_STR
CB67 0.1u
CB73 0.1u
CB76 X_0.1u
CB77 0.1u
CB88 X_0.1u
CB90 0.1u
CB93 0.1u
CB95 0.1u
Pin AL37
Pin AU33
Pin AU29
Pin AU25
Pin AU17
Pin AU13
Pin AU9
Pin AU5
Place decoupling cap close to GMCH Core Logic Interface < 0.1"
Place decoupling cap close to GMCH CPU Interface < 250mil in the Vtt corridor
Place decoupling cap close to GMCH Memory Interface < 0.1", with 18 mil trach width
CT24 1000U/6.3V
CB83 10u-1206
CB78 X_10u/1206
Place Bulk cap for Core Logic, AGP & Hub Link Interface
MEM_STR 470u*2 <3VSB 1000u
CT17 470u/16V
CT14 X_100u
Place Bulk cap between GMCH & DIMM slot
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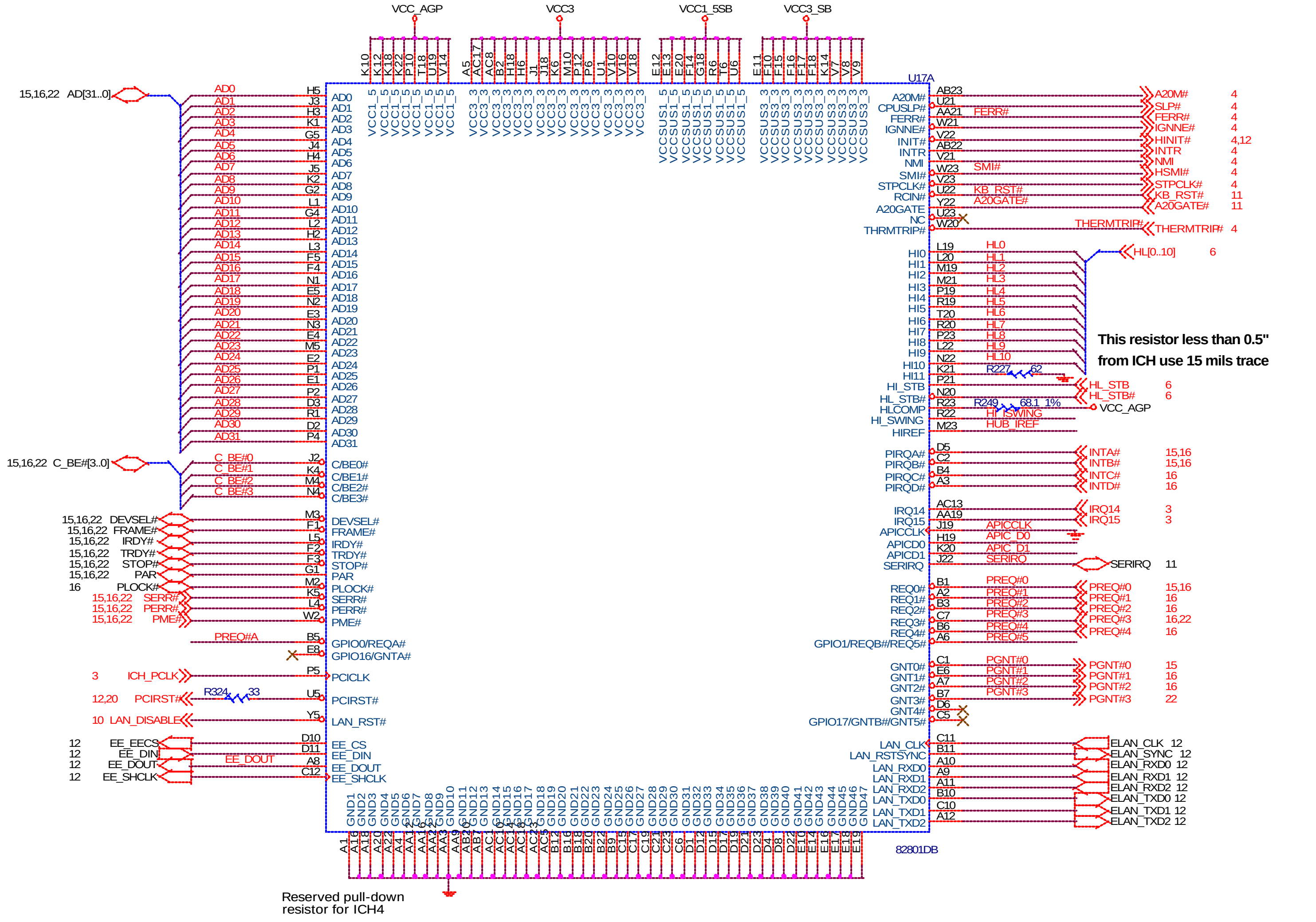
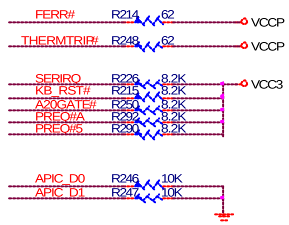
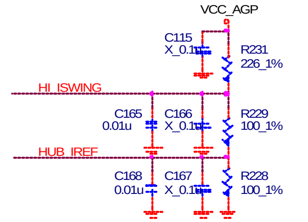
ICH4 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



ICH4 PULL-UP/DOWN RESISTORS

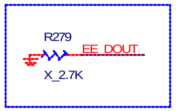


ICH4 REFERENCE VOLTAGE



Place Cap. as Close as possible to ICH4 < 0.25"

Trace width use 12 mils and 10mils space



ICH4 DECOUPLING CAPACITORS

Place one 0.1u close to ICH4 <100 mil

Pin A1 Pin H1 Pin AC10

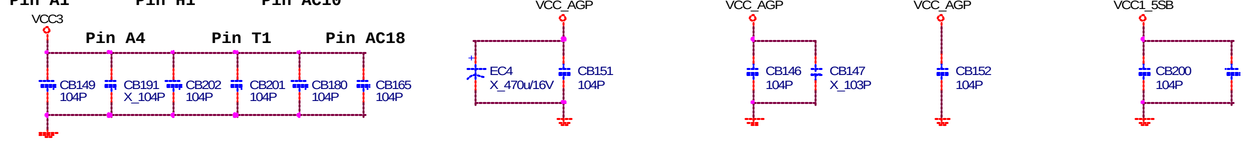
Pin A4 Pin T1 Pin AC18

Pin K23 Pin C23

Pin C22 Pin C22

Pin T23 Pin N23

Pin A16 Pin AC1



FOR Core Logic FOR PLL FOR Hub Interface

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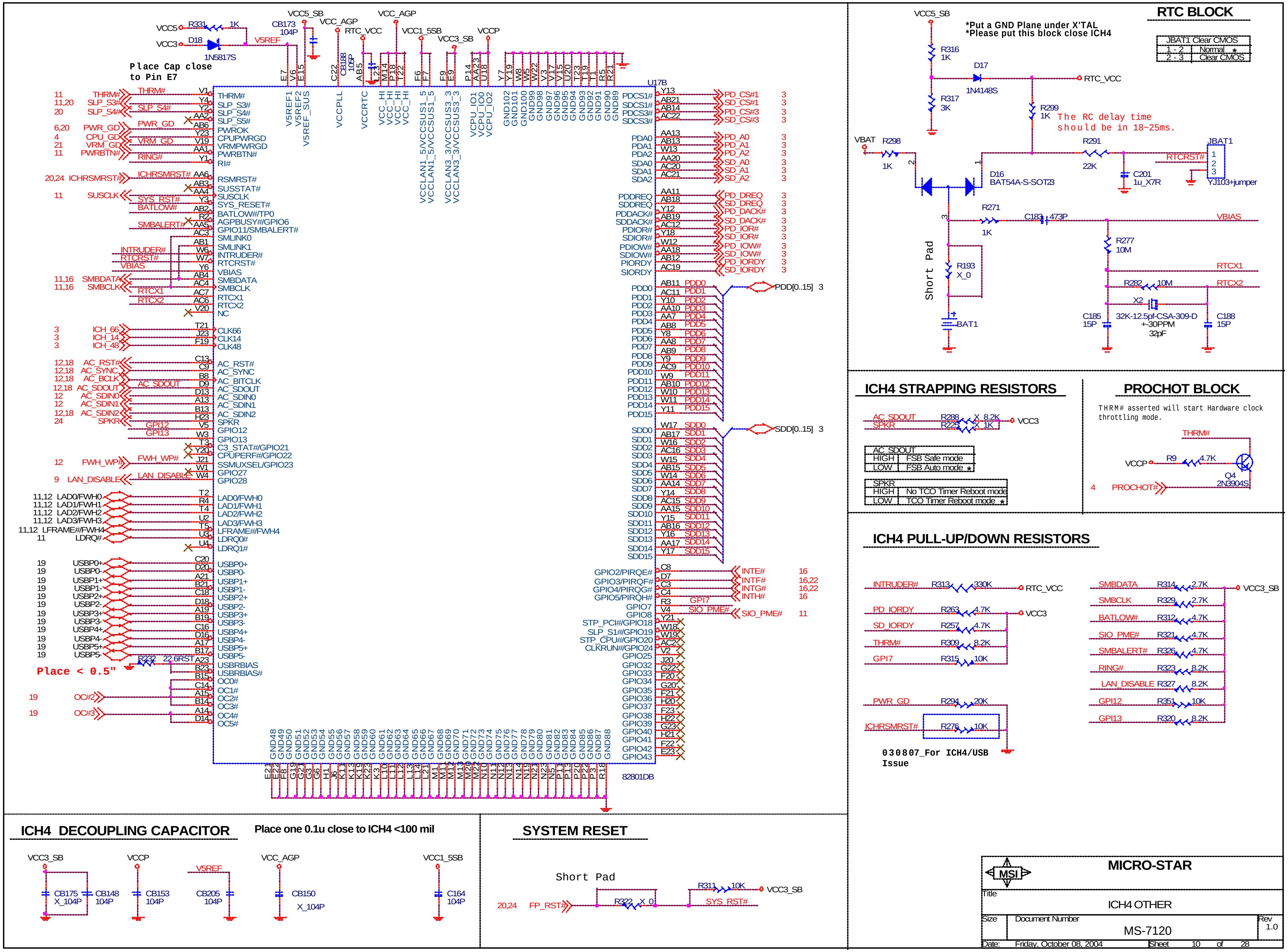

Place Cap close
to Pin E7
U17B
82801DB
Place < 0.5"
RTC BLOCK
*Put a GND Plane under X'TAL
*Please put this block close ICH4
JBAT1 Clear CMOS
1 - 2 Normal ★
2 - 3 Clear CMOS
The RC delay time
should be in 18~25ms.
Short Pad
ICH4 STRAPPING RESISTORS
AC_SDOUT
HIGH FSB Safe mode
LOW FSB Auto mode ★
SPKR
HIGH No TCO Timer Reboot mode
LOW TCO Timer Reboot mode ★
PROCHOT BLOCK
THRM# asserted will start Hardware clock
throttling mode.
ICH4 PULL-UP/DOWN RESISTORS
030807_For ICH4/USB
Issue
ICH4 DECOUPLING CAPACITOR
Place one 0.1u close to ICH4 <100 mil
SYSTEM RESET
Short Pad
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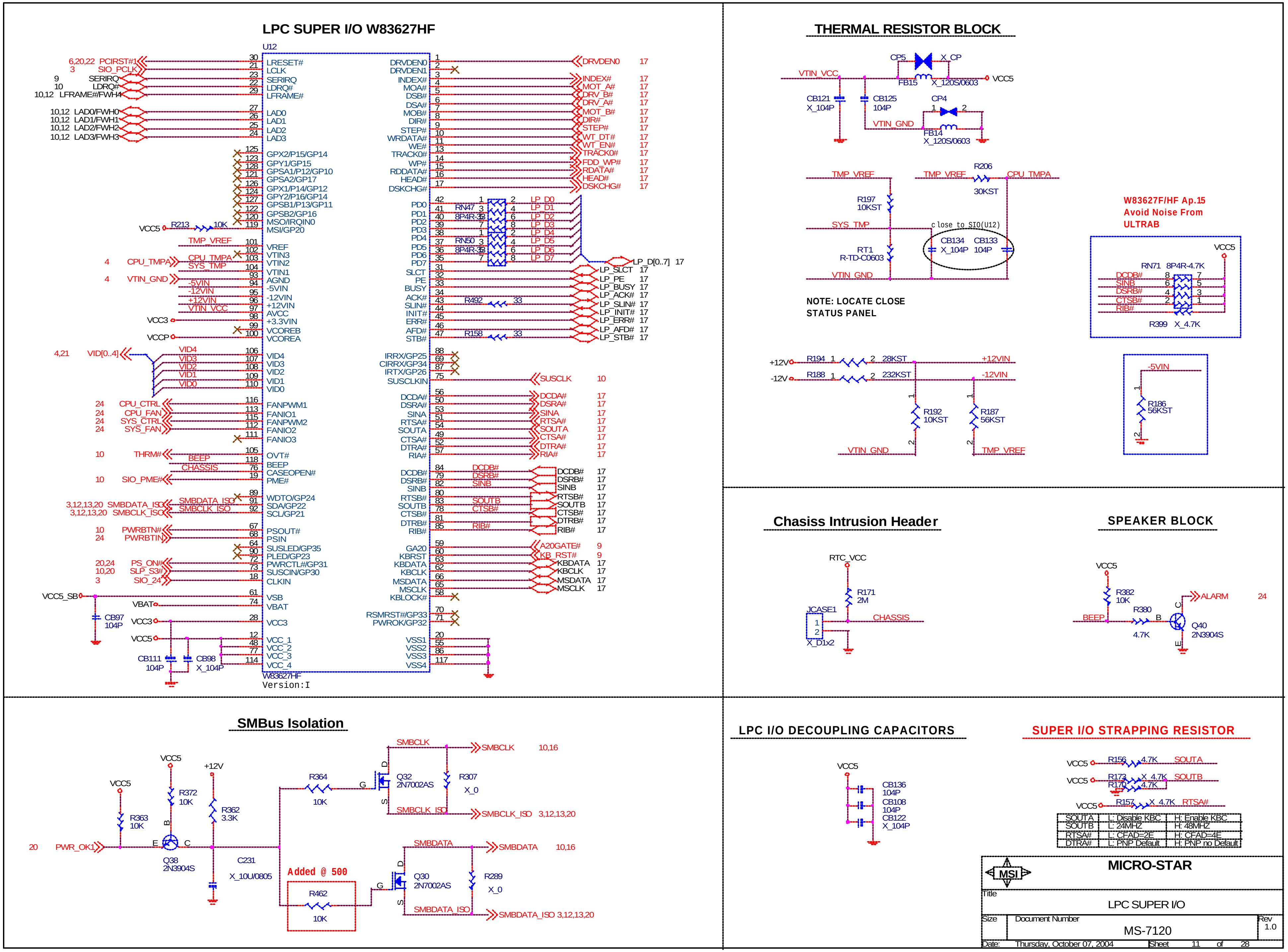
LPC SUPER I/O W83627HF
U12
W83627HF
Version:I
THERMAL RESISTOR BLOCK
VTIN_VCC
VCC5
FB15 X_120S/0603
FB14 X_120S/0603
CB121 X_104P
CB125 104P
CP4
CP5
X_CP
VTIN_GND
TMP_VREF
R206
30KST
CPU_TMPA
R197 10KST
SYS_TMP
close to SIO(U12)
CB134 X_104P
CB133 104P
RT1 R-TD-C0603
NOTE: LOCATE CLOSE
STATUS PANEL
W83627F/HF Ap.15
Avoid Noise From
ULTRAB
RN71 8P4R-4.7K
DCDB#
SINB
DSRB#
CTSB#
RIB#
R399 X_4.7K
R194 28KST
R188 232KST
+12VIN
-12VIN
R192 10KST
R187 56KST
-5VIN
R186 56KST
Chasiss Intrusion Header
RTC_VCC
R171 2M
JCASE1
X_D1x2
CHASSIS
SPEAKER BLOCK
R382 10K
R380 4.7K
BEEP
ALARM
Q40 2N3904S
SMBus Isolation
VCC5
+12V
R372 10K
R363 10K
R362 3.3K
PWR_OK1
Q38 2N3904S
C231 X_10U/0805
R364 10K
Q32 2N7002AS
R307 X_0
SMBCLK
SMBCLK_ISO 3,12,13,20
Q30 2N7002AS
R289 X_0
SMBDATA
SMBDATA_ISO 3,12,13,20
Added @ 500
R462 10K
LPC I/O DECOUPLING CAPACITORS
CB136 104P
CB108 104P
CB122 X_104P
SUPER I/O STRAPPING RESISTOR
R156 4.7K SOUTA
R173 X_4.7K SOUTB
R170 4.7K
R157 X_4.7K RTSA#
SOUTA | L: Disable KBC | H: Enable KBC
SOUTB | L: 24MHZ | H: 48MHZ
RTSA# | L: CFAD=2E | H: CFAD=4E
DTRA# | L: PNP Default | H: PNP no Default
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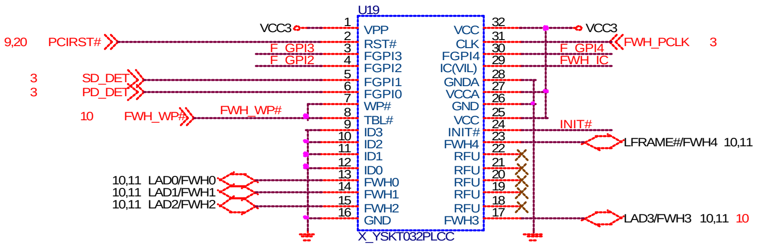
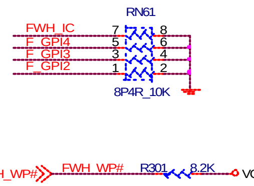
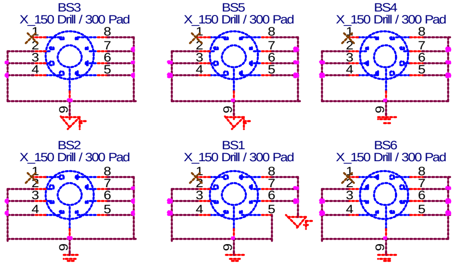
Firware Hub (FWH)



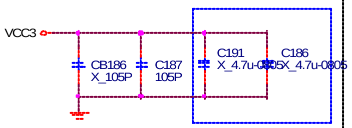
FWH RESISTORS



PCB Mounting Holes



FWH DECOUPLING CAPACITORS

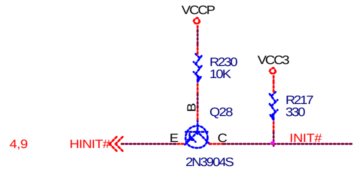


Place Cap. as Close to
FWH< 350 mil

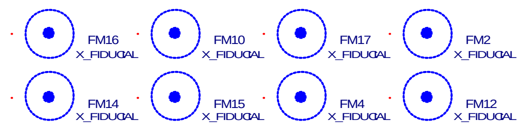
FWH write protect

	BIOS_WP	BIOS Update
SHORT		Flash Write Disable
OPEN		Flash Write Enable (Default)

FWH INIT Signal Voltage Translation Block



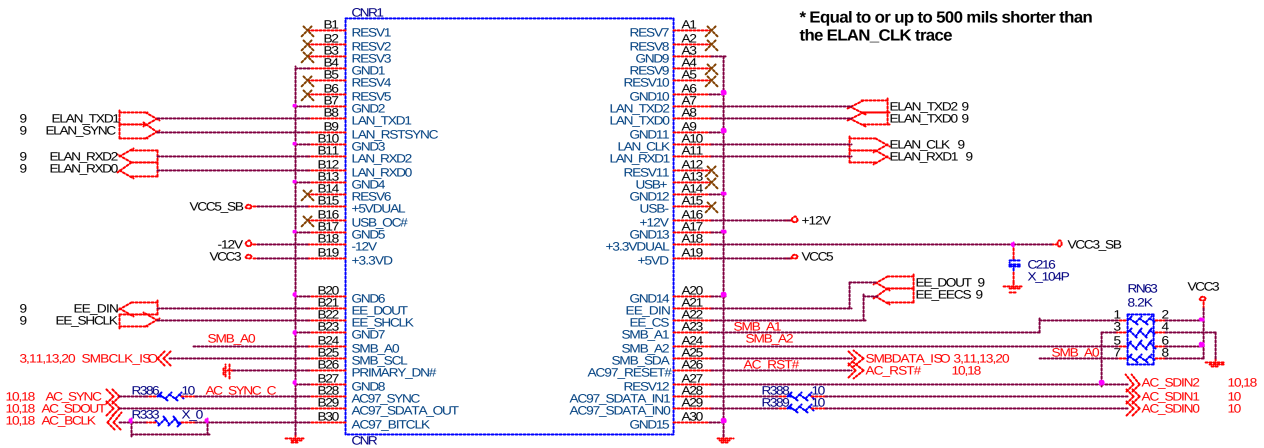
PCB Fiducials



SIMULATION TRACE

CNR RISER

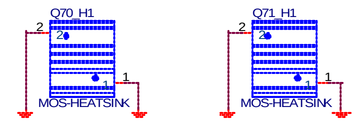
* LAN Trace width : 5 mils
* AC'97 Trace Spacing : 10 mils
* Maxium trace length < 9.5"
* Equal to or up to 500 mils shorter than the ELAN_CLK trace



M1 remove

M1 remove

MOSFET HEATSINK



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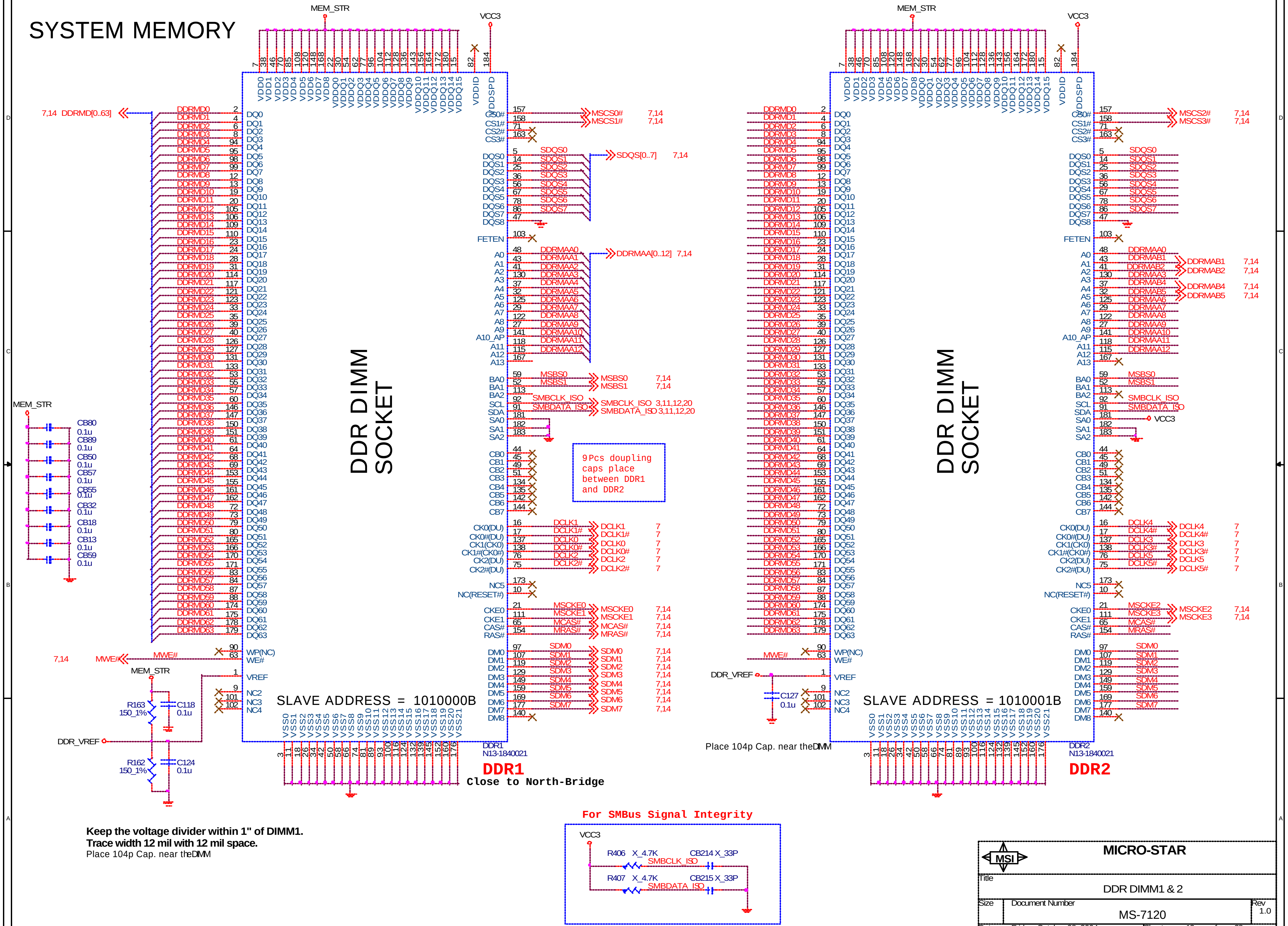
SYSTEM MEMORY



Keep the voltage divider within 1" of DIMM1.
Trace width 12 mil with 12 mil space.
Place 104p Cap. near theDIMM

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Title: DDR DIMM1 & 2

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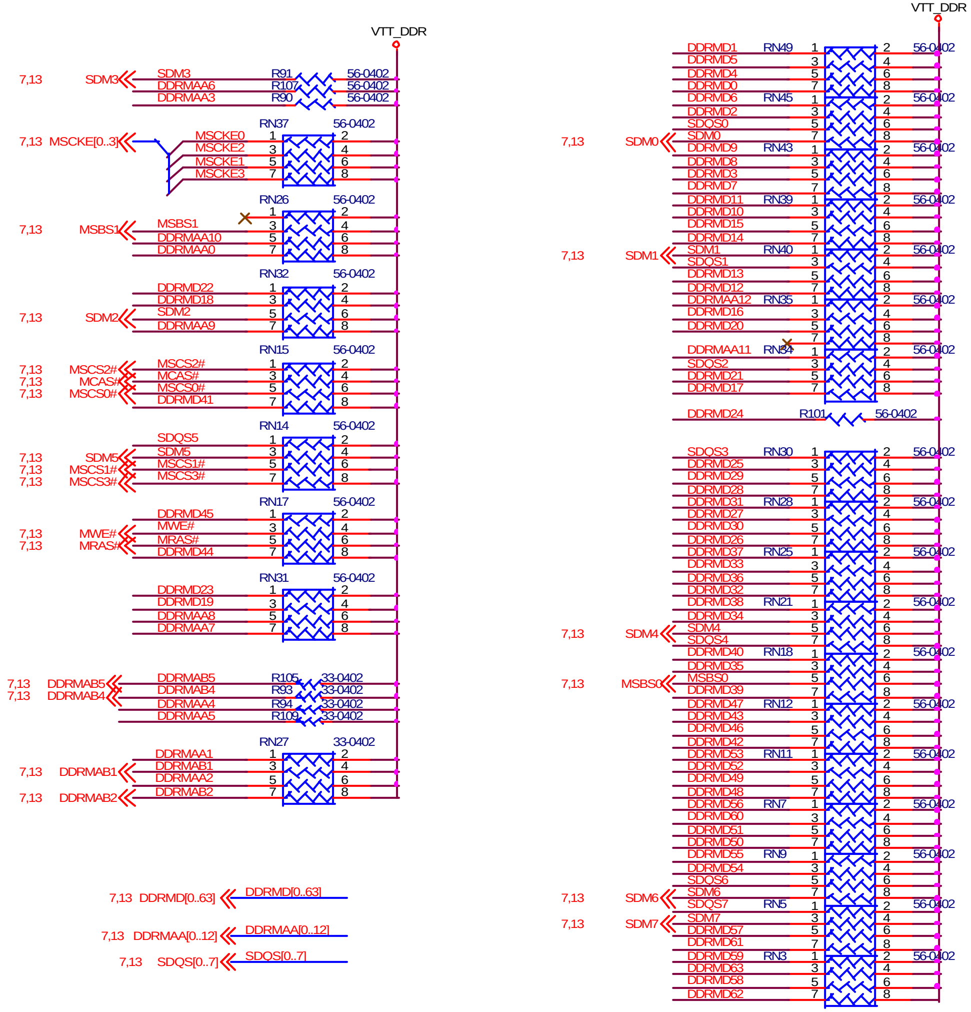
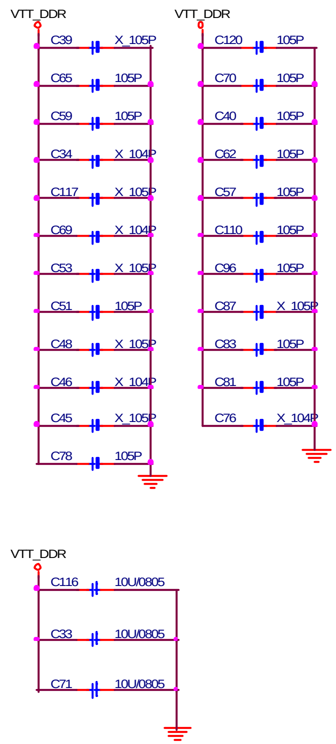
DDR TERMINATORS



TERMINATION DECOUPLING



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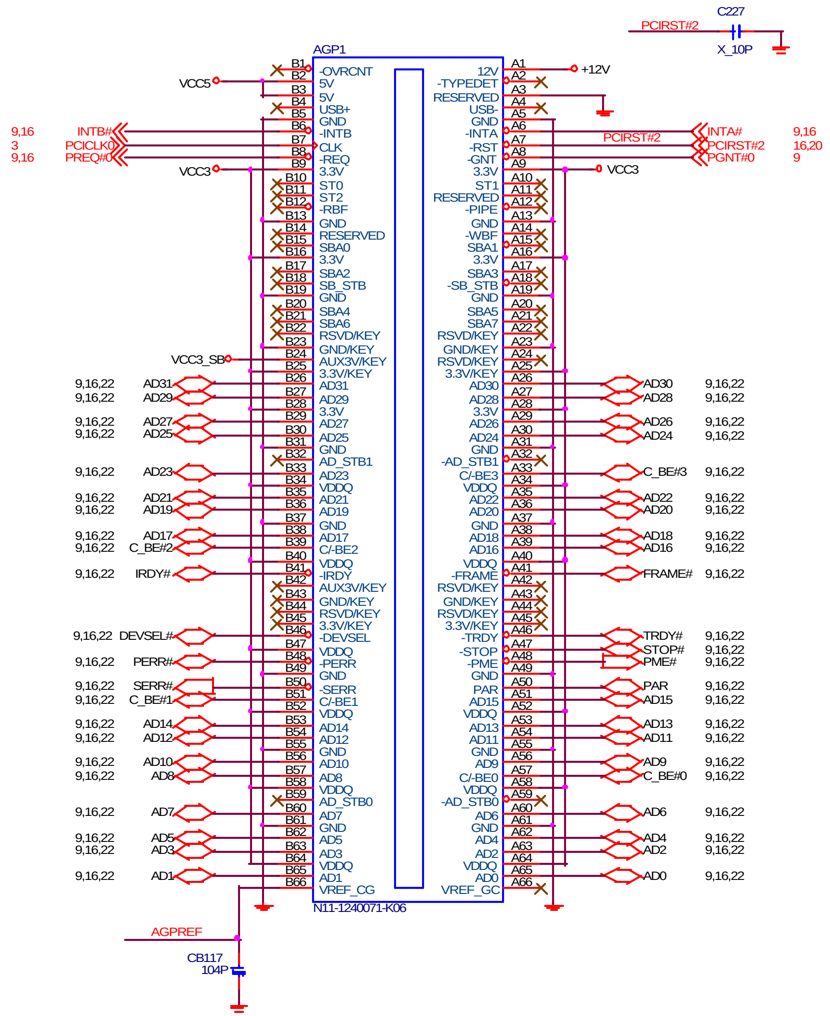
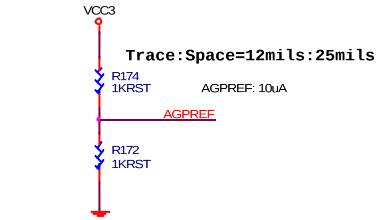
AGP UNIVERSAL 2X/4X SLOT

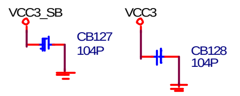


MASTER = PREQ0
INTA#

AGP SIGNAL REFERENCE CIRCUIT



AGP SLOT DECOUPLING CAPACITORS



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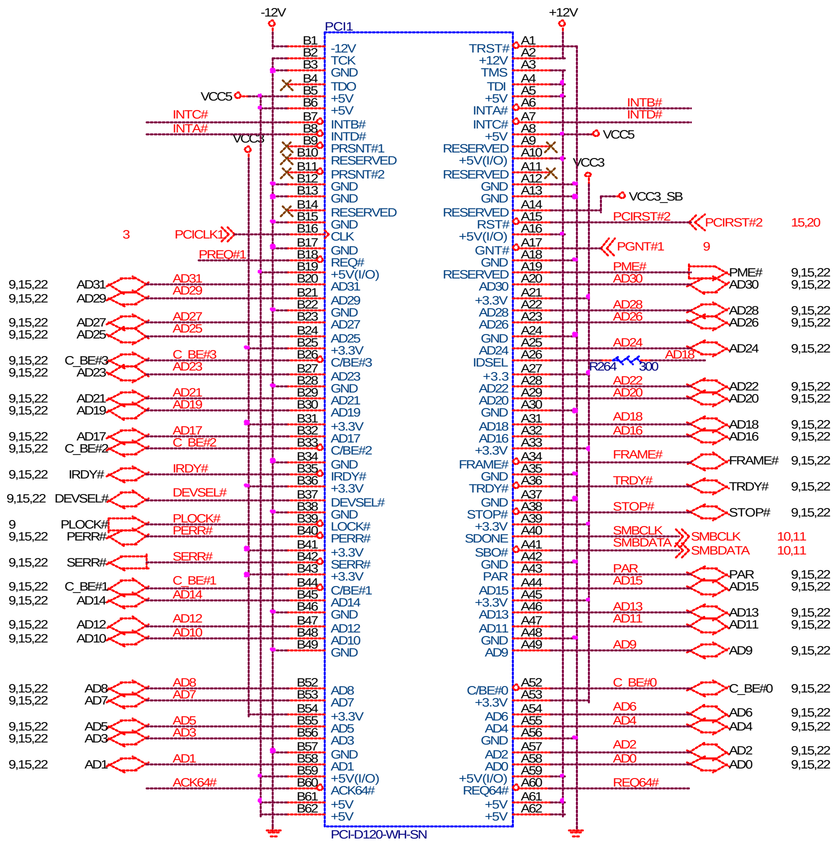
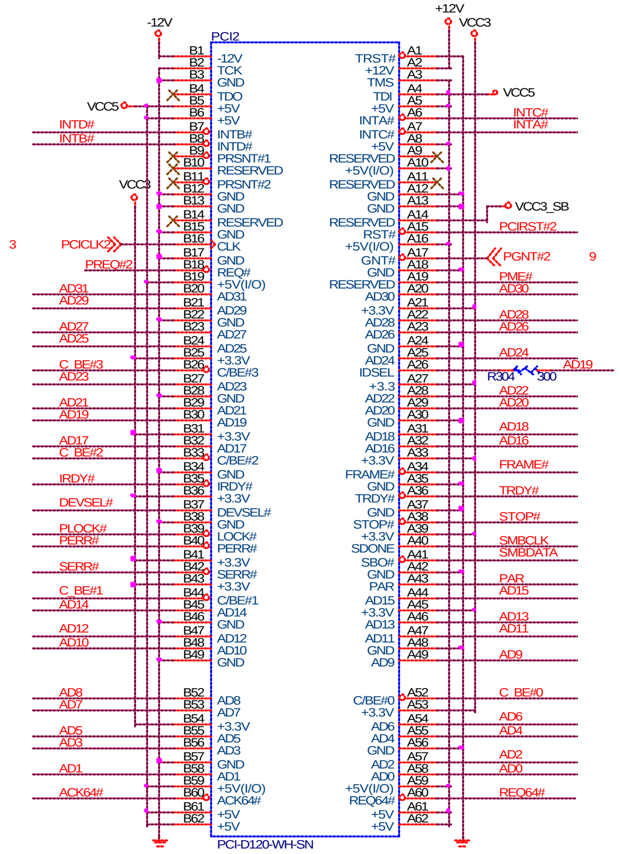
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



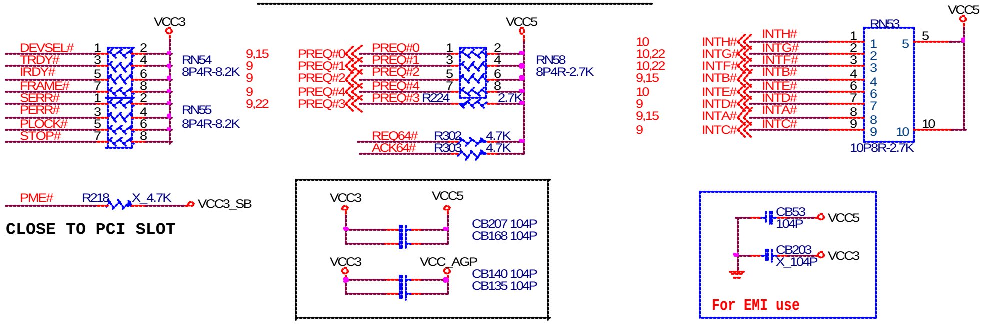
IDSEL = AD18
MASTER = PREQ1
INTB#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



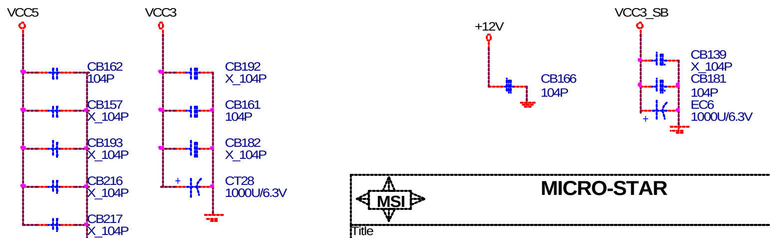
IDSEL = AD19
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



CLOSE TO PCI SLOT

PCI SLOT DECOUPLING CAPACITORS



MICRO-STAR		
Title: PCI SLOT 1,2		
Size	Document Number: MS-7120	Rev 1.0
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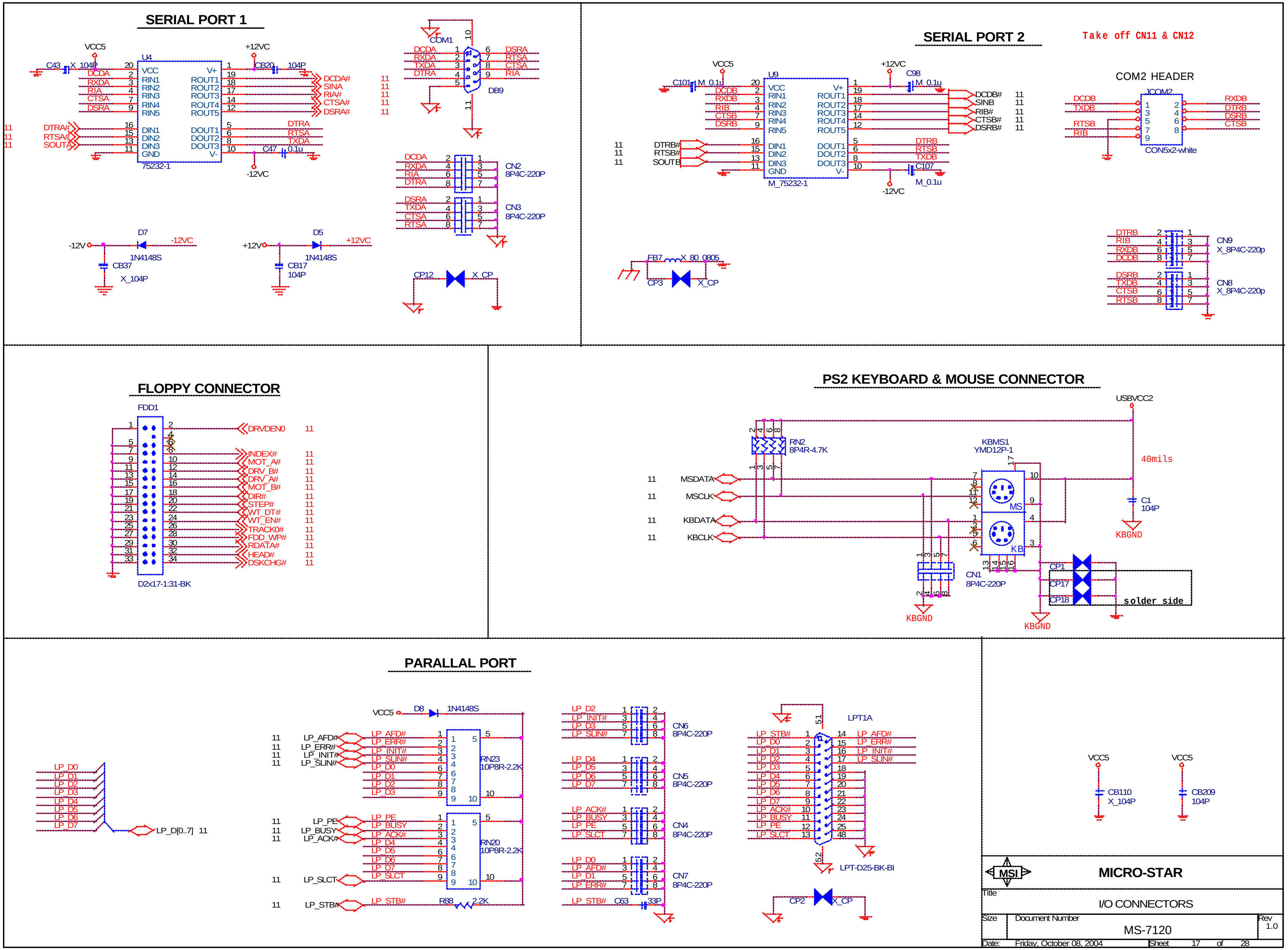
SERIAL PORT 1
SERIAL PORT 2
Take off CN11 & CN12
COM2 HEADER
FLOPPY CONNECTOR
PS2 KEYBOARD & MOUSE CONNECTOR
40mils
solder side
PARALLEL PORT
MICRO-STAR
Title
I/O CONNECTORS
Size
Document Number
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1.0
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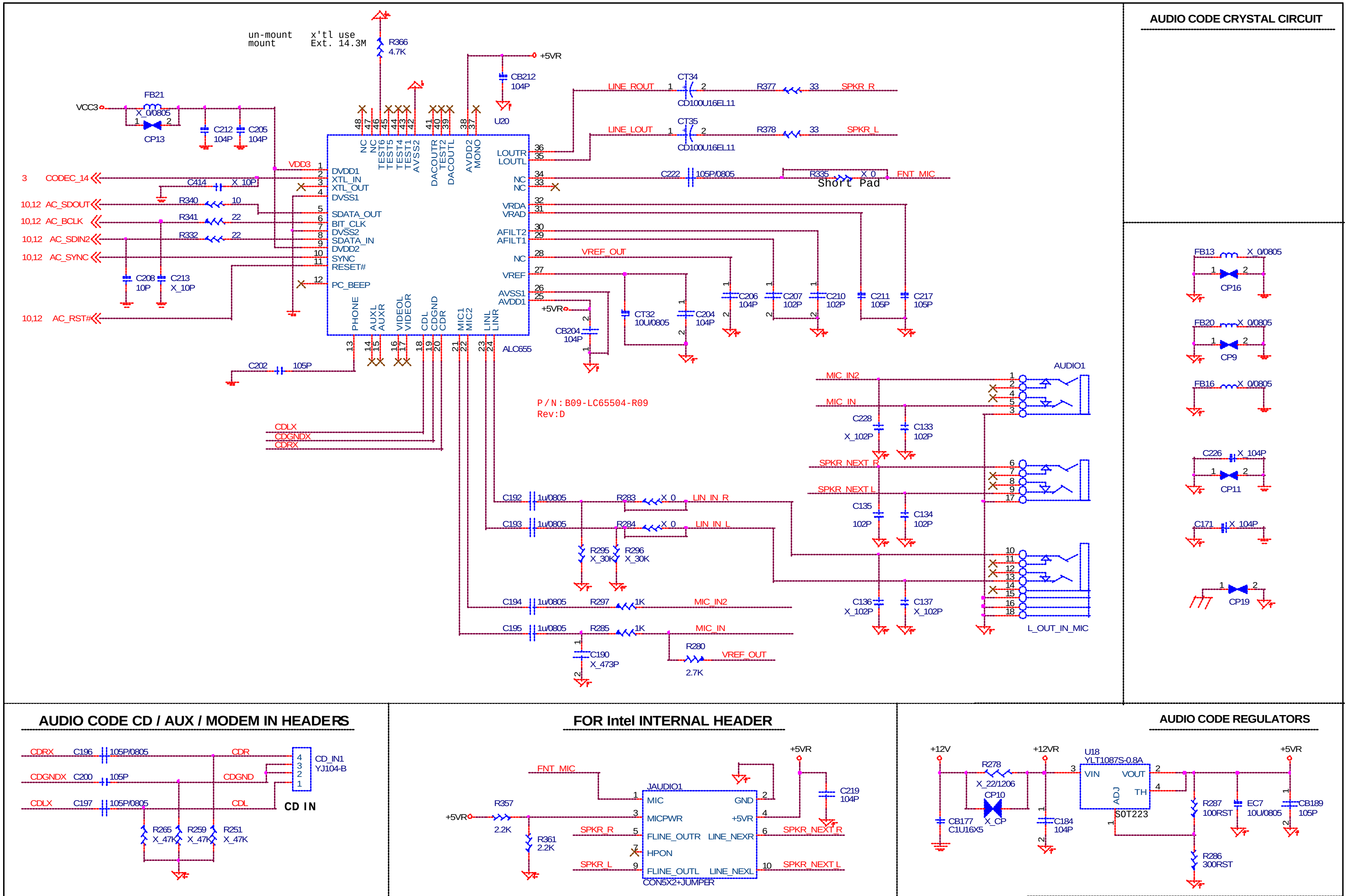

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Title	AC97 CODEC	
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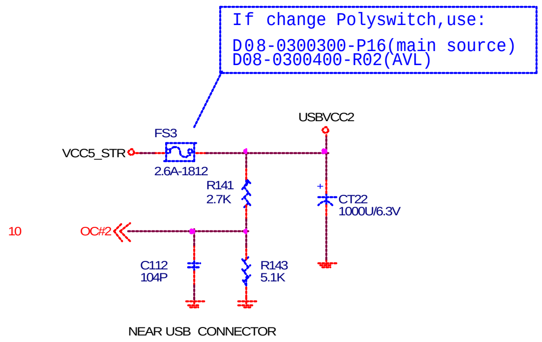
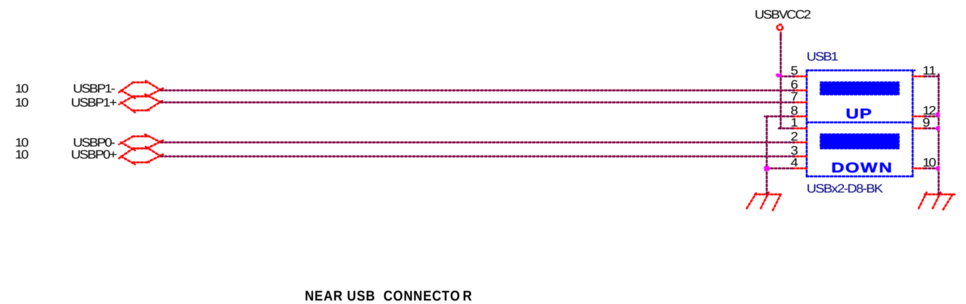
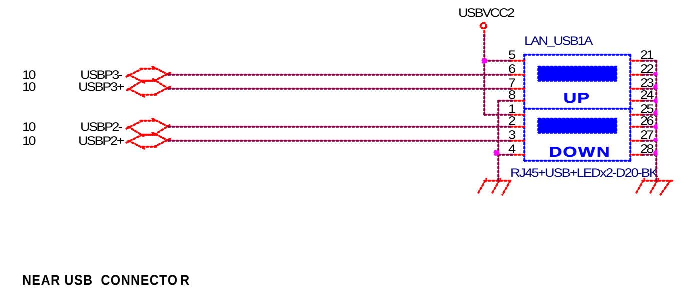
POWER CIRCUIT FOR USB PORT 0~3



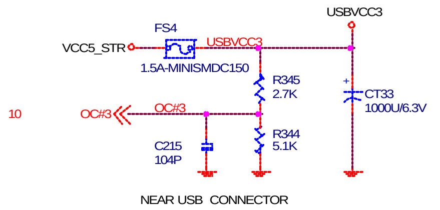
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 4,5



FRONT PANEL USB CONNECTOR FOR USB PORT 4,5

* USB Trace width : 7.5 mils
* USB Trace Spacing : 20 mils
* Differential USB Signlas Trace, Spacing : 7.5 mils
* USB Power Trace must be 50mils width

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Title	USB CONNECTORS	
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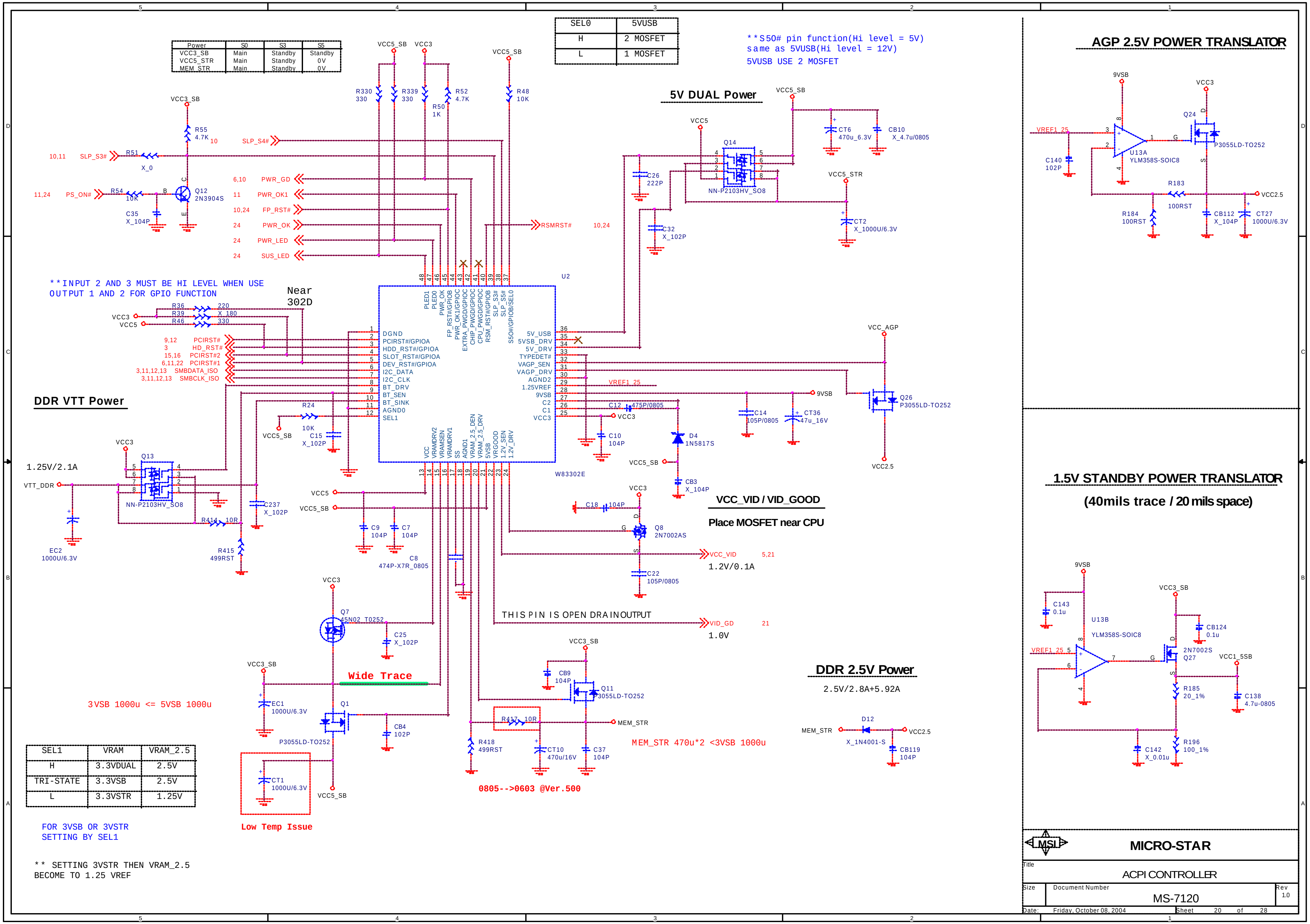
Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

SEL0	5VUSB
H	2 MOSFET
L	1 MOSFET

**S50# pin function(Hi level = 5V)
same as 5VUSB(Hi level = 12V)
5VUSB USE 2 MOSFET



SEL1	VRAM	VRAM_2.5
H	3.3VDUAL	2.5V
TRI-STATE	3.3VSB	2.5V
L	3.3VSTR	1.25V

FOR 3VSB OR 3VSTR
SETTING BY SEL1

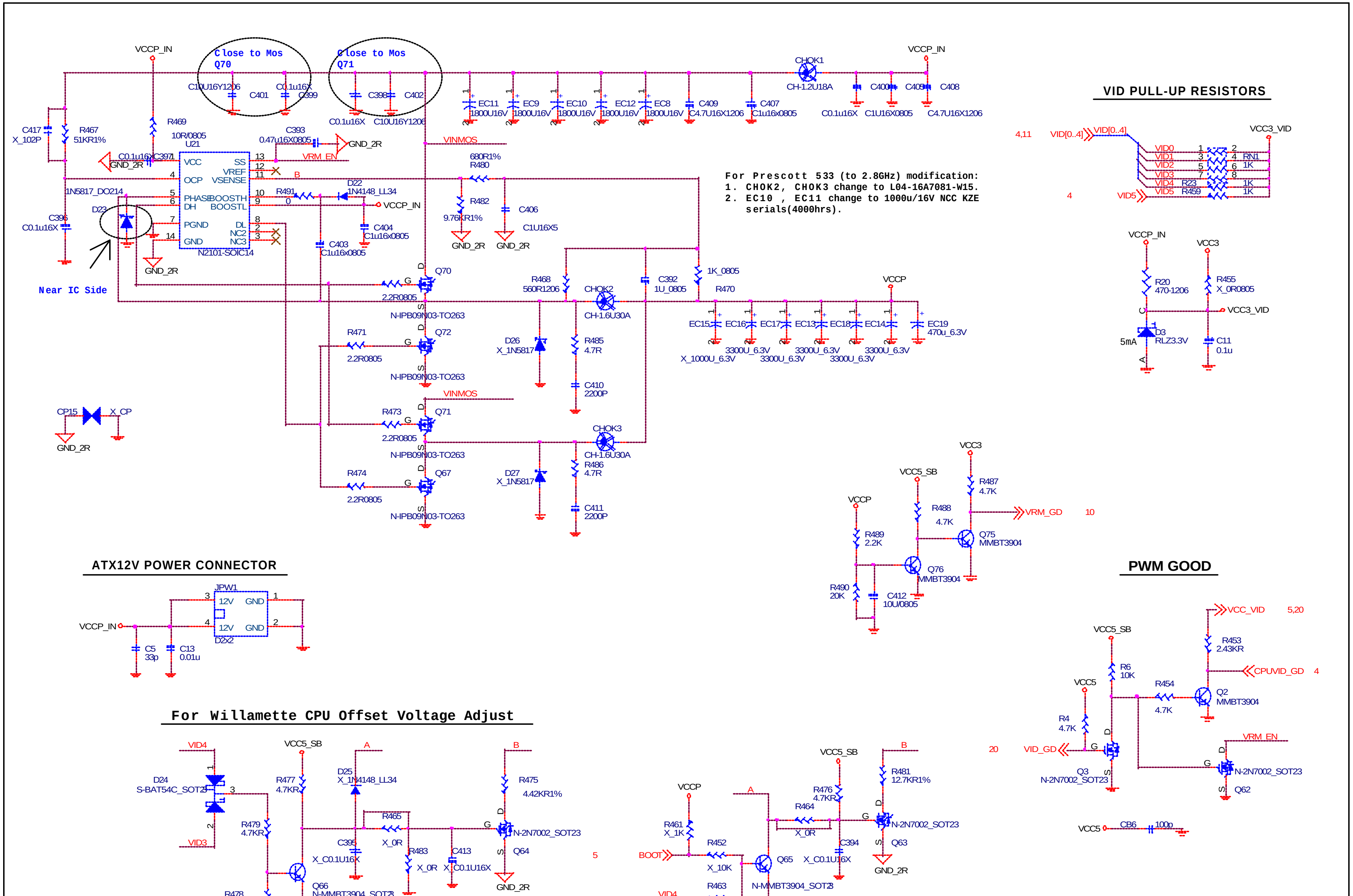
** SETTING 3VSTR THEN VRAM_2.5
BECOME TO 1.25 VREF

MICRO-STAR

Title: ACPI CONTROLLER

Size | Document Number: MS-7120 | Rev 1.0

Date: Friday, October 08, 2004 | Sheet 20 of 28



CPU	VID4	VID3
Northwood	0	1
Willamette	0	0
Prescott	1	0

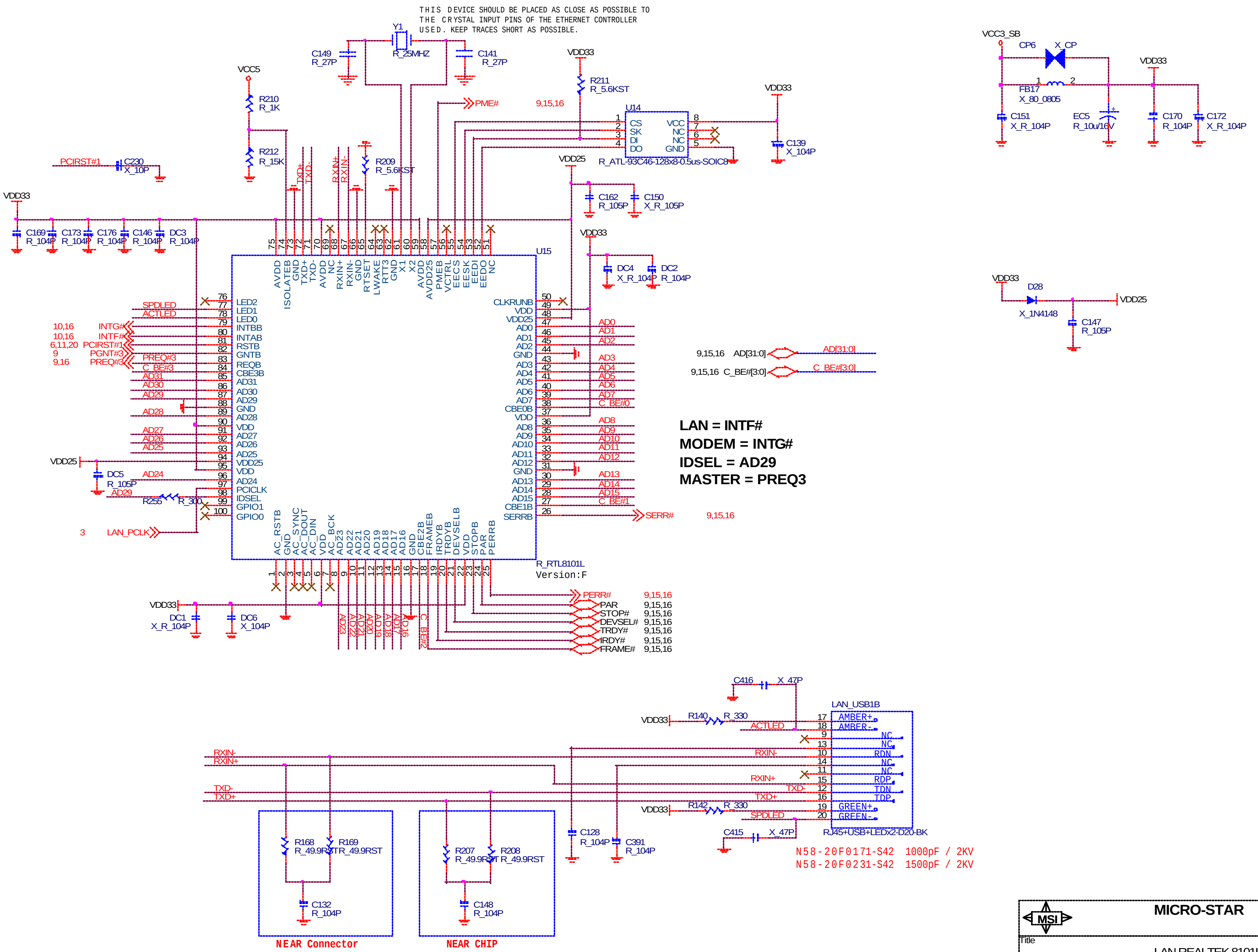
BOOTSEL	CPU
LOW	Northwood
HIGH	Prescott

MICRO-STAR INT'L CO.,LTD.

Title: VRM 9.0 NIKO N2101

Size | Document Number: MS-7120 | Rev 1.0

Date: Friday, October 08, 2004 | Sheet 21 of 28



MICRO-STAR

Title: LAN REALTEK 8101L

Size	Document Number	Rev
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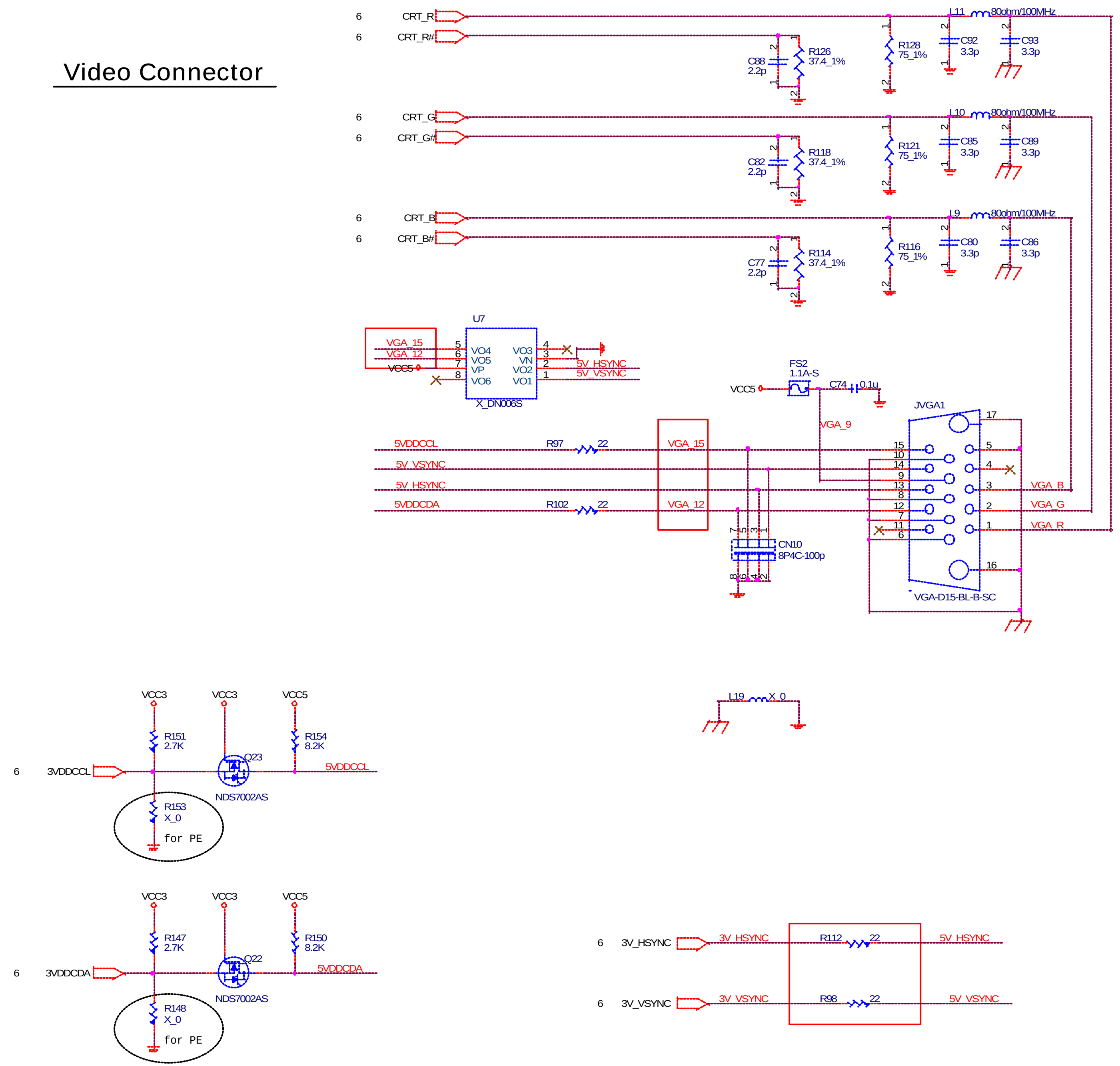
Video Connector



MSI	**MICRO-STAR**	
Title	VGA CONNECTOR	
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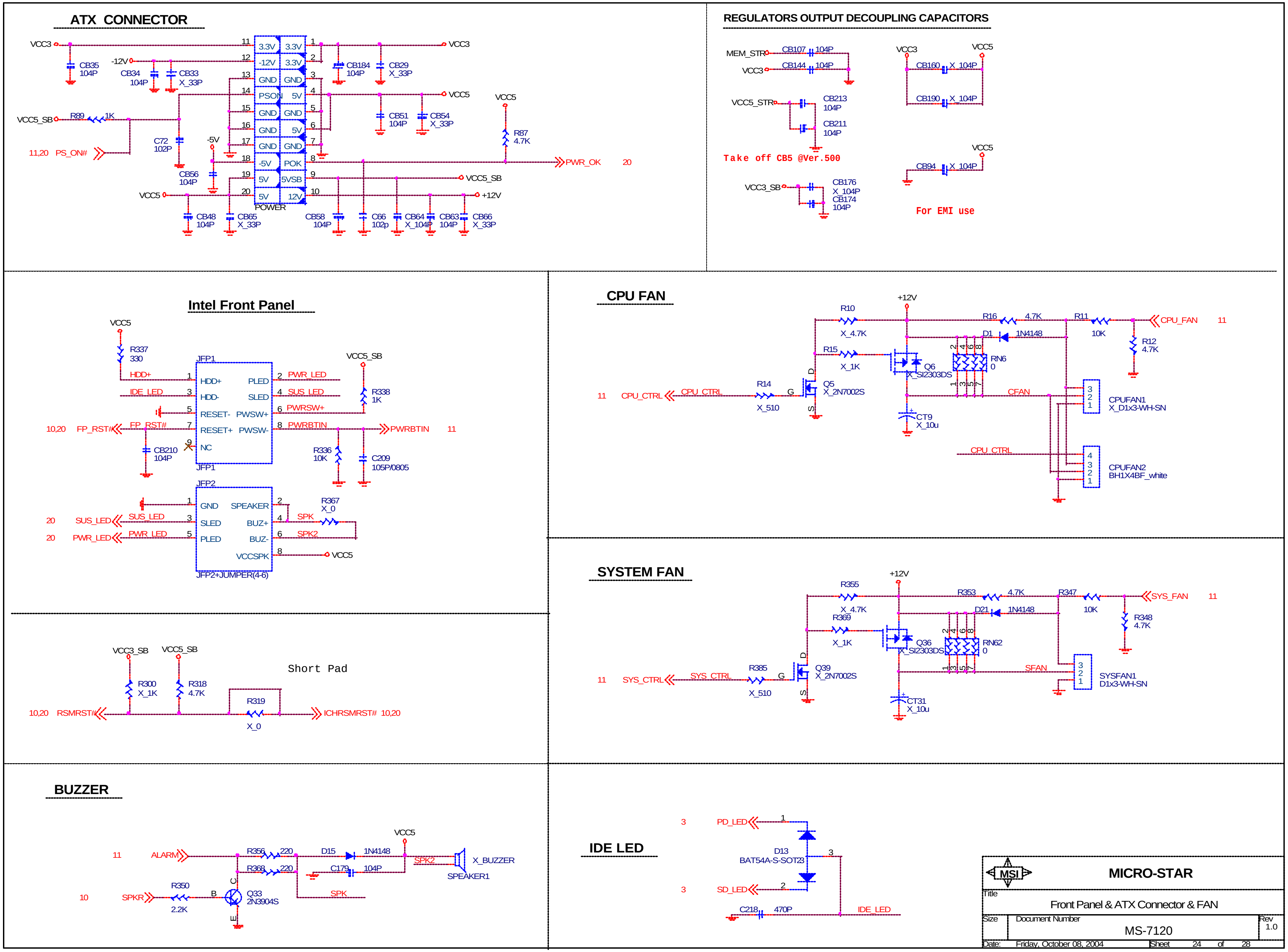

MSI	MICRO-STAR			
Title	Front Panel & ATX Connector & FAN			
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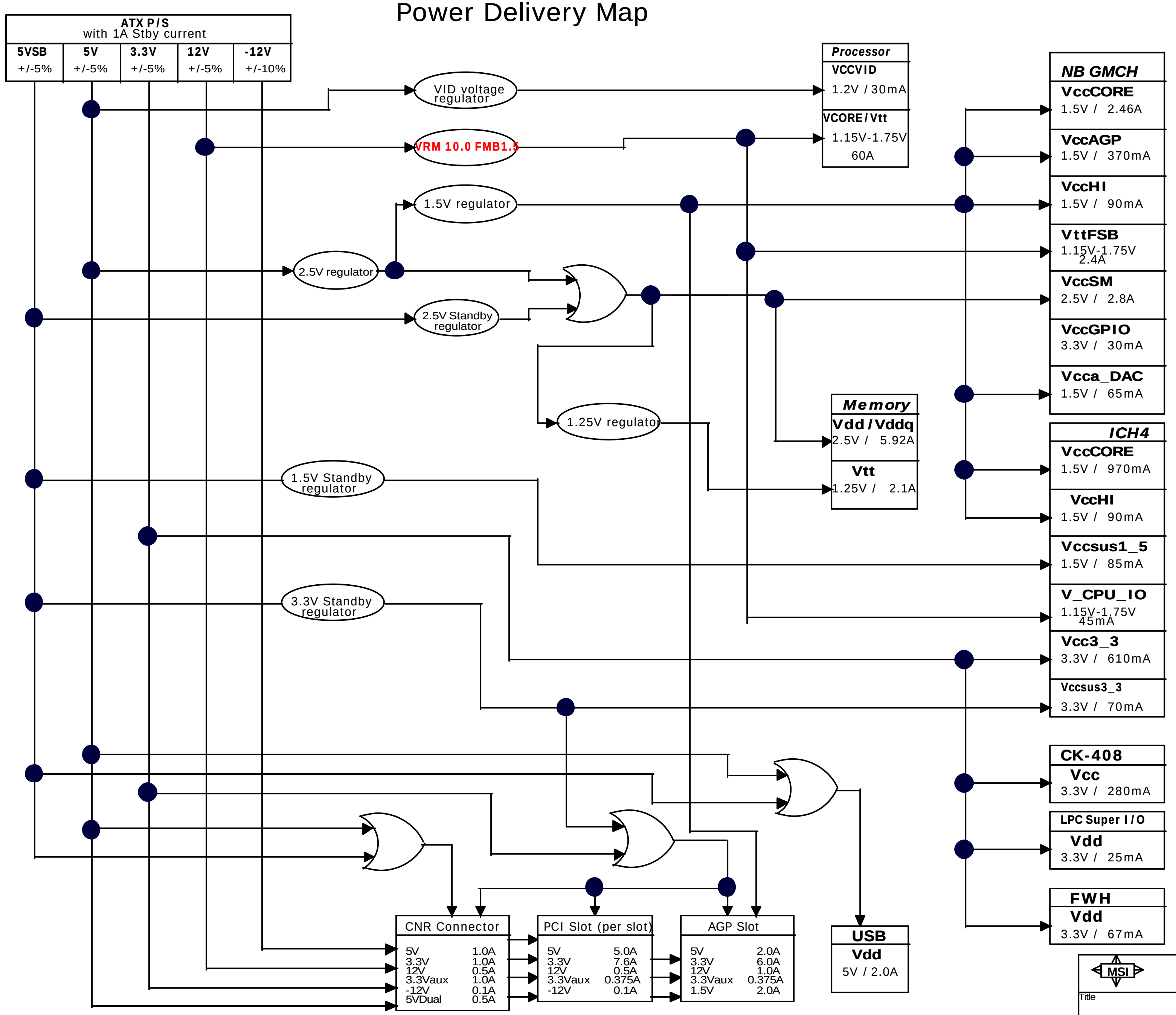
Power Delivery Map



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Title	Power Delivery Map	
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GPIO SPEC

ICH4

GPIO Pin	Type	Function
GPIO 0	I	REQ#A (multifunction pin)
GPIO 1	I	REQ#B (multifunction pin)
GPIO 2	I	Pull up through 8.2K ohms (PIRQE#)
GPIO 3	I	Pull up through 8.2K ohms (PIRQF#)
GPIO 4	I	Pull up through 8.2K ohms (PIRQG#)
GPIO 5	I	Pull up through 8.2K ohms (PIRQH#)
GPIO 6	I	Pull down through 10K ohms (unused)
GPIO 7	I	Pull down through 10K ohms (unused)
GPIO 8	I	Pull Up to 3.3VSBY through 4.7K ohms (SIO_PME)
GPIO 9	I	Not Implemented
GPIO 10	I	Not Implemented
GPIO 11	I	SMB_ALERT (multifuntion pin)
GPIO 12	I	EXTSMI# with Pull up 10K ohms to VCC3_SB
GPIO 13	I	Pull down through 10K ohms (unused)
GPIO 14~15	I	Not Implemented
GPIO 16	O	GNT#A (multifunction pin)
GPIO 17	O	GNT#B (multifunction pin)
GPIO 18	O	No Connected
GPIO 19	O	No Connected
GPIO 20	O	No Connected
GPIO 21	O	No Connected
GPIO 22	OD	No Connected
GPIO 23	O	Pull Up to 3.3V through 8.2K ohms (BIOS protect)
GPIO 24	I/O	GPIO 24
GPIO 25	I/O	GPIO 25
GPIO 26	I/O	Not Implemented
GPIO 27	I/O	No Connected
GPIO 28	I/O	No Connected
GPIO 29~31	O	Not Implemented
GPIO 32	I/O	No Connected
GPIO 33	I/O	No Connected
GPIO 34	I/O	Primary IDE ATA66/100 detection (PD_DET)
GPIO 35	I/O	Secondary IDE ATA66/100 detection (SD_DET)
GPIO 36	I/O	No Connected
GPIO 37	I/O	No Connected
GPIO 38	I/O	No Connected
GPIO 39	I/O	No Connected
GPIO 40	I/O	No Connected
GPIO 41	I/O	No Connected
GPIO 42	I/O	No Connected
GPIO 43	I/O	No Connected
GPIO 44~47	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	Pull down through 8.2K ohms (unused)
GPI 1	I	Pull down through 8.2K ohms (unused)
GPI 2	I	P1 customer defined
GPI 3	I	P1 customer defined
GPI 4	I	Pull down through 8.2K ohms (unused)

PCI Config.

DEVICE	ICH INT Pin	IDSEL	CLOCK	CLK GEN PIN OUT
AGP1	INTA# INTB#	AD16	PCICLK0	10 (PCI3/FS4)
PCI Slot 1	INTB# INTC# INTD# INTA#	AD18	PCICLK1	11 (PCI4)
PCI Slot 2	INTC# INTD# INTA# INTB#	AD19	PCICLK2	12 (PCI5)
PCI LAN	INTF# INTG#	AD29	LAN_PCLK	17 (PCI9)

**ICH4 reserved PCI address line AD22 for the PCI-to-ISA Bridge's IDSEL input.*

DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	DCLK0/DCLK0# DCLK1/DCLK1# DCLK2/DCLK2#
DIMM 2	1010001B	DCLK3/DCLK3# DCLK4/DCLK4# DCLK5/DCLK5#

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Title	GPIO SPEC	
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Jumper Setting & Connector Setting

STD	U10_A B01-845GE15-I06 **845GE B1**; U17_A B01-801DB55-I06 **ICH4 B0**; LAN_USB1_A USB X 2 - 8pin Only USB*2	U19_B1 FLASH 4M; LABEL1_A G51-LA00830 **845GE**
LAN	LAN_USB1_B USB X2 +RJ45 N58-16F0041-S42 1000pF / 2KV LAN & Tramsformer + USB*2	Onboard VGA :Yes; R135_A 137_1%; R126_A 37.4_1%; R118_A 37.4_1%; R114_A 37.4_1%; R128_A 75_1%; R121_A 75_1%; R116_A 75_1%
GV	U10_B B01-845GV15-I06 **845GV B1**; U17_B B01-801DB55-I06 **ICH4 B0**	U19_A1 FLASH 2M; LABEL1_B G51-LA00828 **845GV**
G	U10_C B01-0845G65-I06 **845G B1**; U17_C B01-801DB55-I06 **ICH4 B0**	LABEL1_C G51-LA00829 **845G(B)**
GL	U10_D B01-845GL15-I06 **845GL B1**; U17_D B01-801DB55-I06 **ICH4 B0**	LABEL1_D G51-LA00831 **845GL**
B	U10_E B01-845PE15-I06 **845PE B1**; U17_E B01-801DB55-I06 **ICH4 B0**	Onboard VGA :No; CB92_B 0 ohm; R135_B 0; C160_B 0; R126_B 0; R118_B 0; R114_B 0; R128_B 0; R121_B 0; R116_B 0
OPT:A **OPT:B**		L9_A 60ohm/100MHz; L10_A 60ohm/100MHz; L11_A 60ohm/100MHz; C80_A 10p; C86_A 10p; C85_A 10p; C89_A 10p; C92_A 10p; C93_A 10p

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Title	JUMPER SETTING & MANUAL PARTS	
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0A change to 1.0 note :

1. Change AGP-slot pin-A11 to floating for AGP8X support. ---- page 15
2. Add 0.1u cap for CPU_TMP to GND to avoid noise when SIO detect CPU temperature.(also reserved one for SYS_TMP) ---- page 11
3. Audio Line-in damping-resistor change to 0-ohm from 24K-ohm to meet audio-precision THD+N spec. ---- page 18
4. Change USB power fuse from 0-ohm resistor to polyswitch. ---- page 19
5. Add pci-slot ACK64# & REQ64# pull-up resistor for 64Bit PCI-card compatibility. ---- page 16

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Title: JUMPER SETTING & MANUAL PARTS			
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