MS-7114

Version 2.0
2/21/2005 Update

CPU:

Intel LGA775 Processor

System Chipset:

SIS 656 + SiS 964

On Board Chipset:

LPC Super I/O -- W83697HF
LAN PHY -- VT6103
IEEE1394 -- VT6307
AC97 CODEC -- RealTek ALC850

CLOCK Chip :

ICS953401+ Buffer ICS9P932

Main Memory:

DDR2 DIMM Slot *4

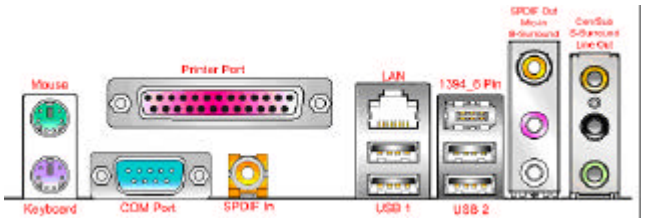
Expansion Slots:

PCI EXPRESS x16 Slot *1

PCI2.2 Slot *3

PWM:

INTERSIL ISL6565ACV



PCI Routing

PCI 1	INTB# IDSEL=AD17 MASTER=PREQ#0 PGNT#0 PCICLK1		
PCI 2	INTC# IDSEL=AD18 MASTER=PREQ#1 PGNT#1 CPICLK4	INTB# IDSEL=AD21 MASTER=PREQ#3 PGNT#3 PCICLK3	INTA# IDSEL=AD20 MASTER=PREQ#5 PGNT#5 PCICLK0
PCI 3	INTD# IDSEL=AD19 MASTER=PREQ#2 PGNT#2 PCICLK2		
1394	INTC# IDSEL=AD22 MASTER=PREQ#4 PGNT#4 1394PCLK		

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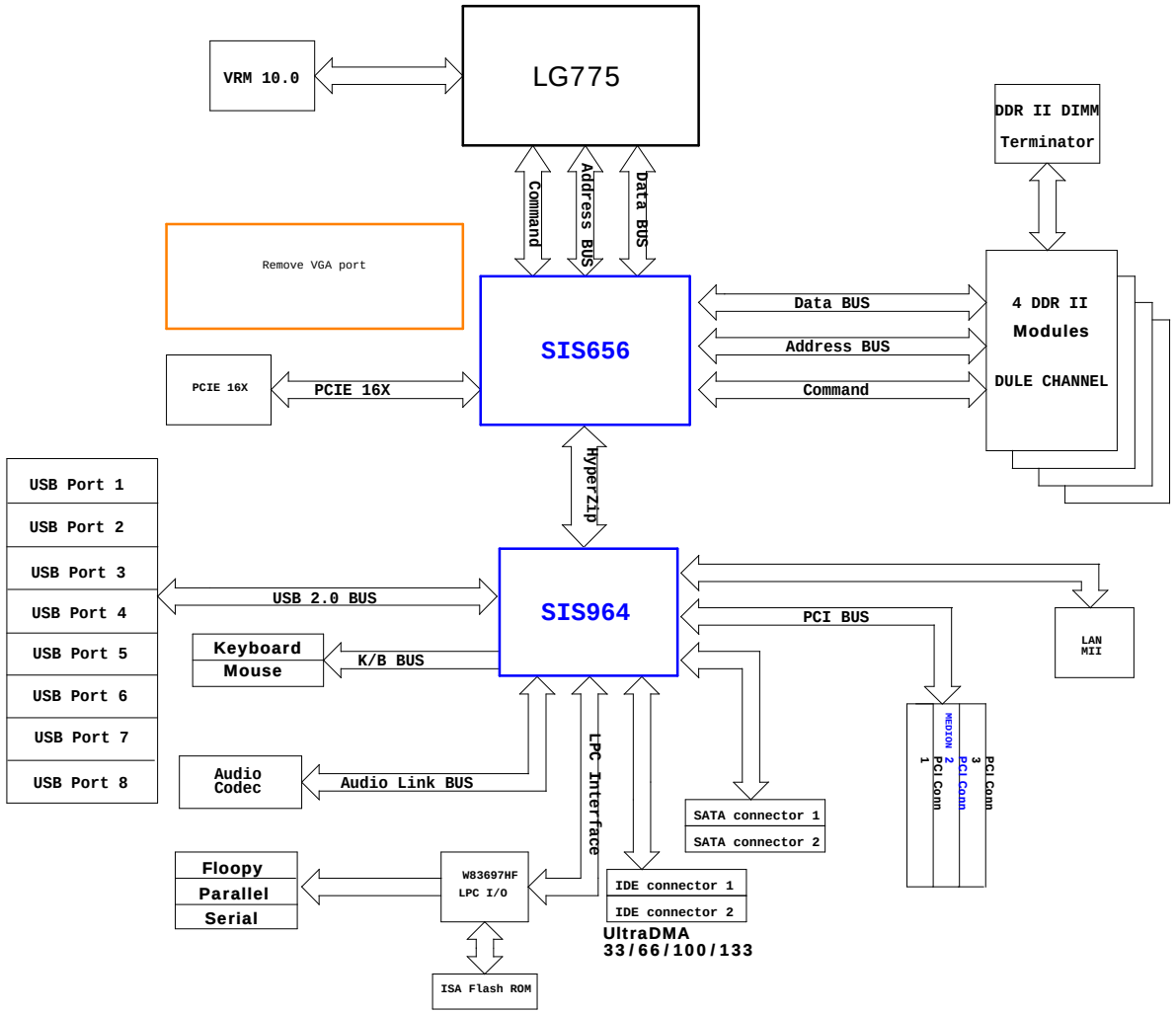
Title: Cover Sheet

Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 1 of 36

Block Diagram

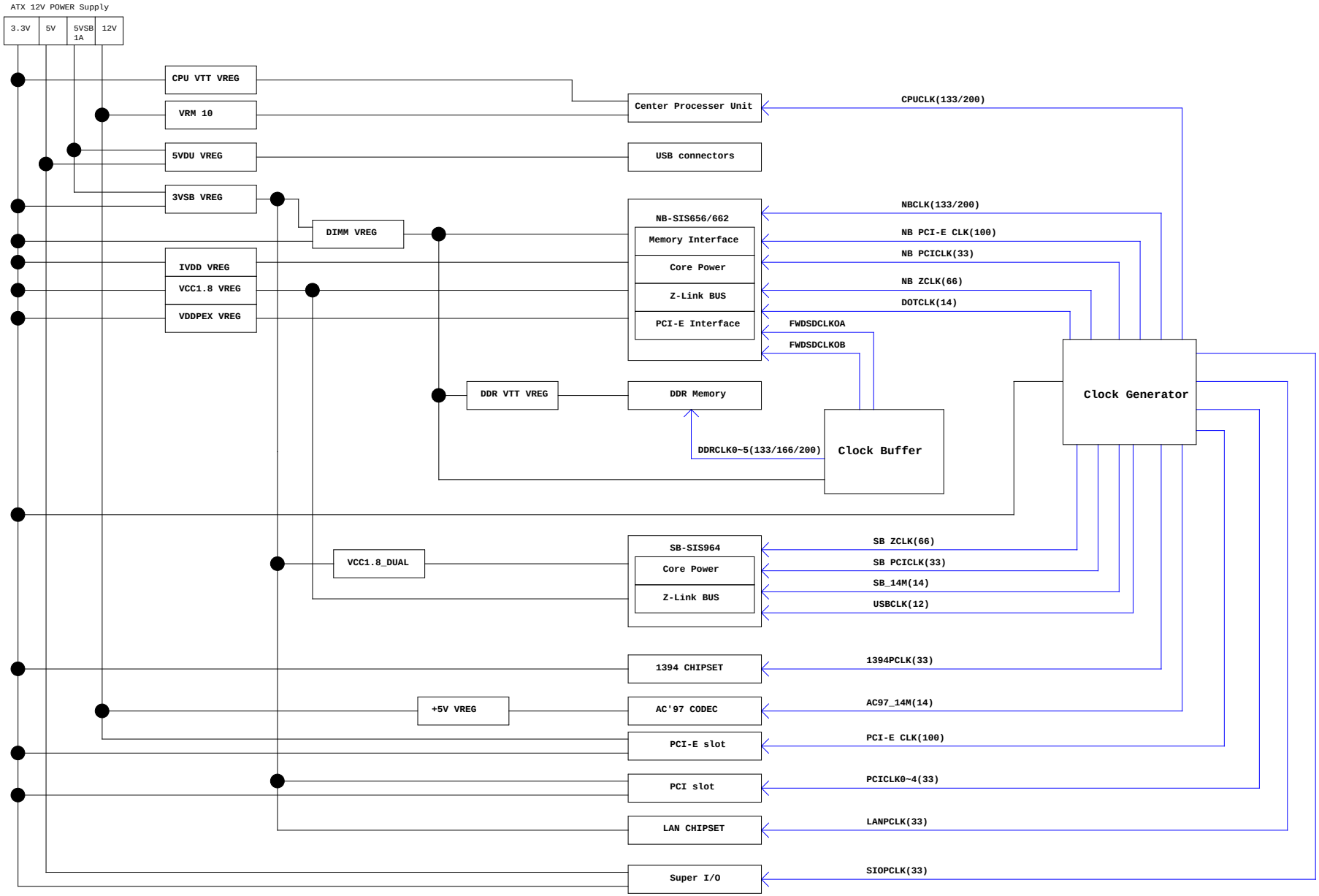
MS-7114 Ver:2.0



MSI	MICRO-STAR	
Title	Block Diagram	
Size	Document Number: MS-7114	Rev: 2A
Date: Wednesday, May 18, 2005	Sheet 2 of 36	

Power Delivery Map

CLOCK Delivery Map



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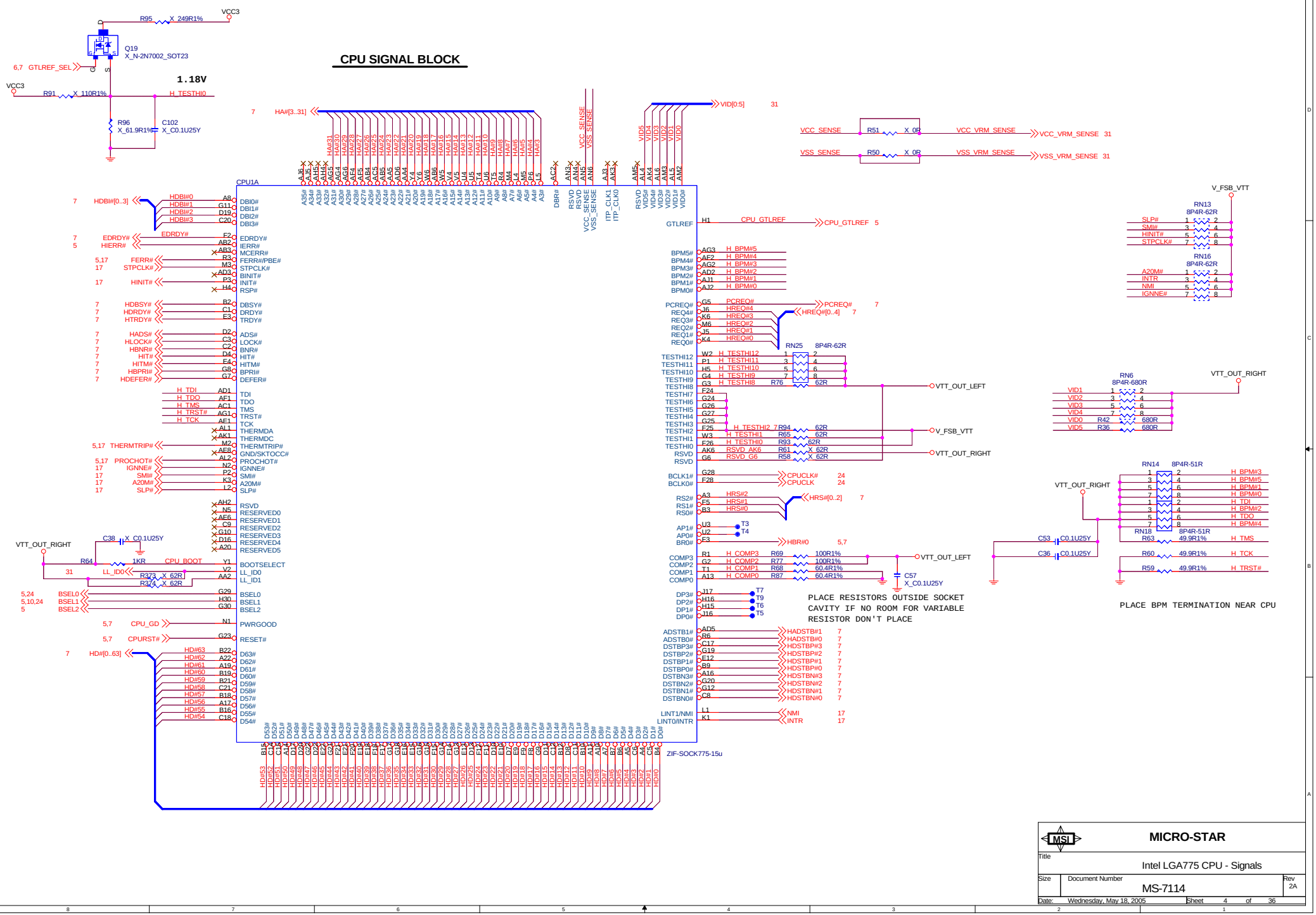
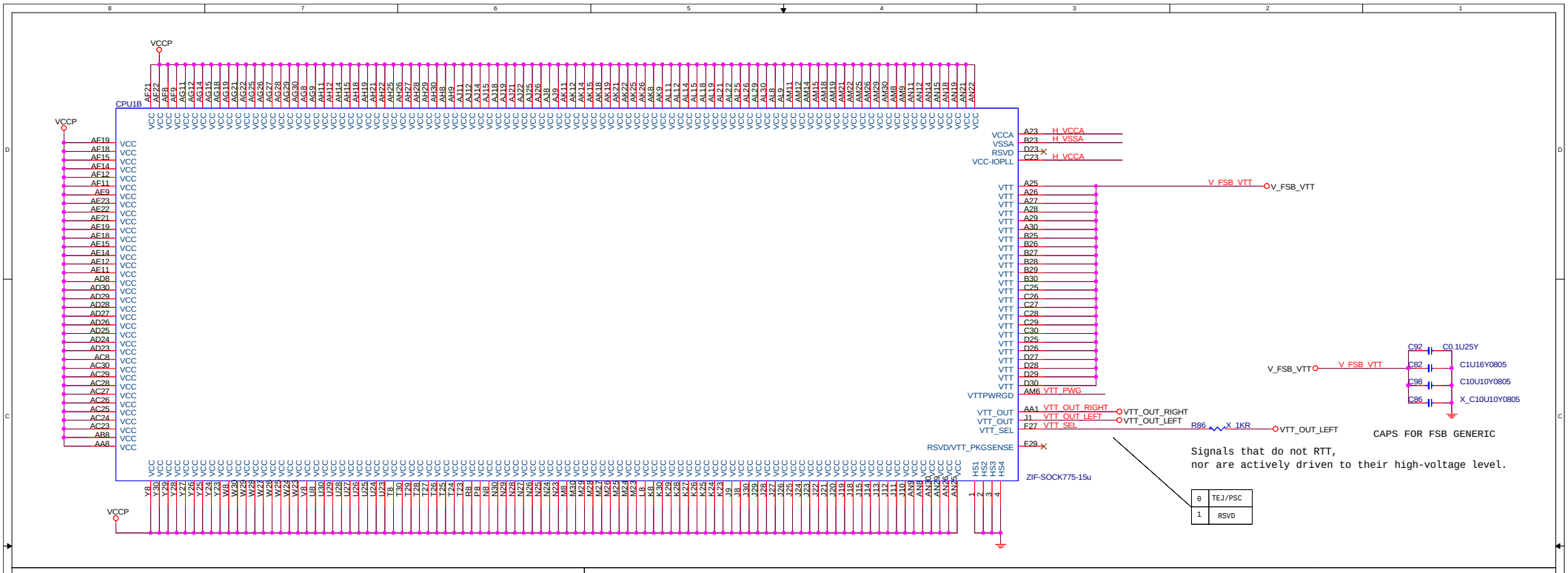
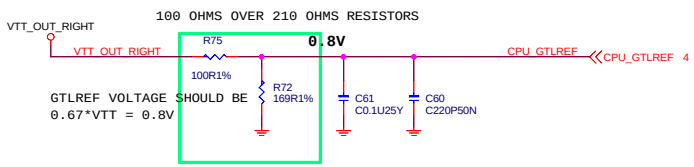
Title: Power & Clock delivery

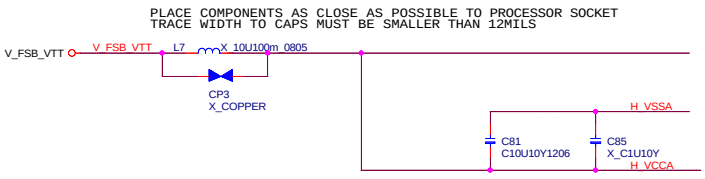
Size | Document Number: MS-7114 | Rev 2A

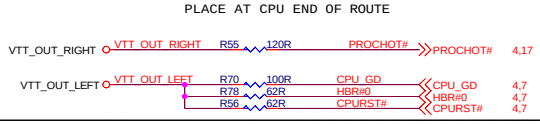
Date: Wednesday, May 18, 2005 | Sheet 3 of 36

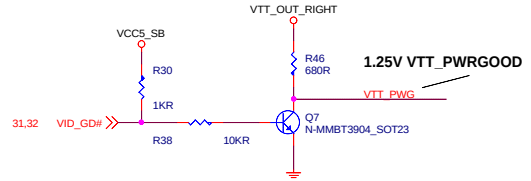

CPU SIGNAL BLOCK
1.18V
VCC3
R95 X_249R1%
Q19 X_N-2N7002_SOT23
6,7 GTLREF_SEL
R91 X_110R1%
H_TESTHI0
R96 X_61.9R1%
C102 X_C0.1U25Y
CPU1A
ZIF-SOCK775-15u
HA#[3..31]
HDBI#[0..3]
EDRDY#
HIERR#
FERR#
STPCLK#
HINIT#
HDBSY#
HDRDY#
HTRDY#
HADS#
HLOCK#
HBNR#
HIT#
HITM#
HBPRI#
HDEFER#
H_TDI
H_TDO
H_TMS
H_TRST#
H_TCK
THERMTRIP#
PROCHOT#
IGNNE#
SMI#
A20M#
SLP#
RESERVED0
RESERVED1
RESERVED2
RESERVED3
RESERVED4
RESERVED5
BOOTSELECT
LL_ID0
LL_ID1
BSEL0
BSEL1
BSEL2
PWRGOOD
RESET#
HD#[0..63]
VID[0:5]
VCC_SENSE
VSS_SENSE
R51 X_0R
R50 X_0R
VCC_VRM_SENSE
VSS_VRM_SENSE
GTLREF
CPU_GTLREF
BPM5#
BPM4#
BPM3#
BPM2#
BPM1#
BPM0#
PCREQ#
REQ4#
REQ3#
REQ2#
REQ1#
REQ0#
HREQ#[0..4]
TESTHI12
TESTHI11
TESTHI10
TESTHI9
TESTHI8
TESTHI7
TESTHI6
TESTHI5
TESTHI4
TESTHI3
TESTHI2
TESTHI1
TESTHI0
RSVD
BCLK1#
BCLK0#
CPUCLK#
CPUCLK
RS2#
RS1#
RS0#
HRS#[0..2]
AP1#
AP0#
BR0#
HBR#0
COMP3
COMP2
COMP1
COMP0
DP3#
DP2#
DP1#
DP0#
ADSTB1#
ADSTB0#
DSTBP3#
DSTBP2#
DSTBP1#
DSTBP0#
DSTBN3#
DSTBN2#
DSTBN1#
DSTBN0#
LINT1/NMI
LINT0/INTR
RN25 8P4R-62R
RN6 8P4R-680R
RN13 8P4R-62R
RN16 8P4R-62R
RN14 8P4R-51R
RN18 8P4R-51R
VTT_OUT_LEFT
VTT_OUT_RIGHT
V_FSB_VTT
C57 X_C0.1U25Y
C53 C0.1U25Y
C36 C0.1U25Y
C38 X_C0.1U25Y
R64 1KR
R373 X_62R
R374 X_62R
PLACE RESISTORS OUTSIDE SOCKET CAVITY IF NO ROOM FOR VARIABLE RESISTOR DON'T PLACE
PLACE BPM TERMINATION NEAR CPU
MICRO-STAR
Intel LGA775 CPU - Signals
MS-7114
Rev 2A
Wednesday, May 18, 2005
Sheet 4 of 36

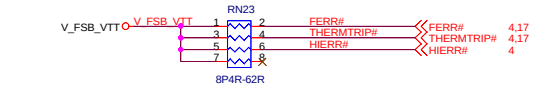


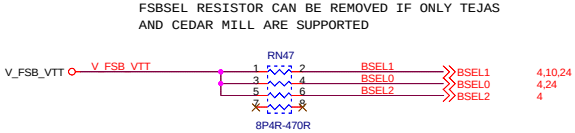










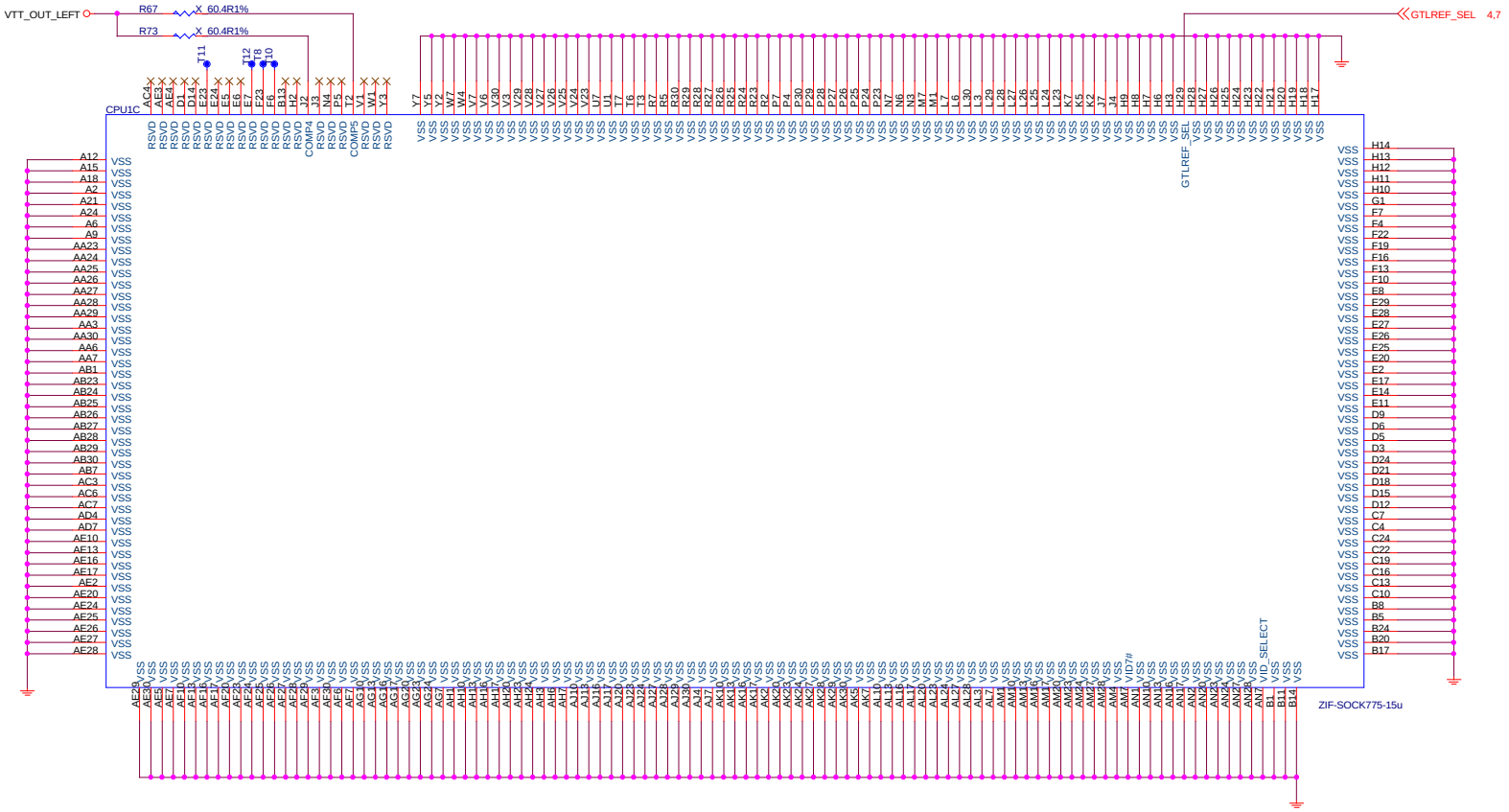


MICRO-STAR

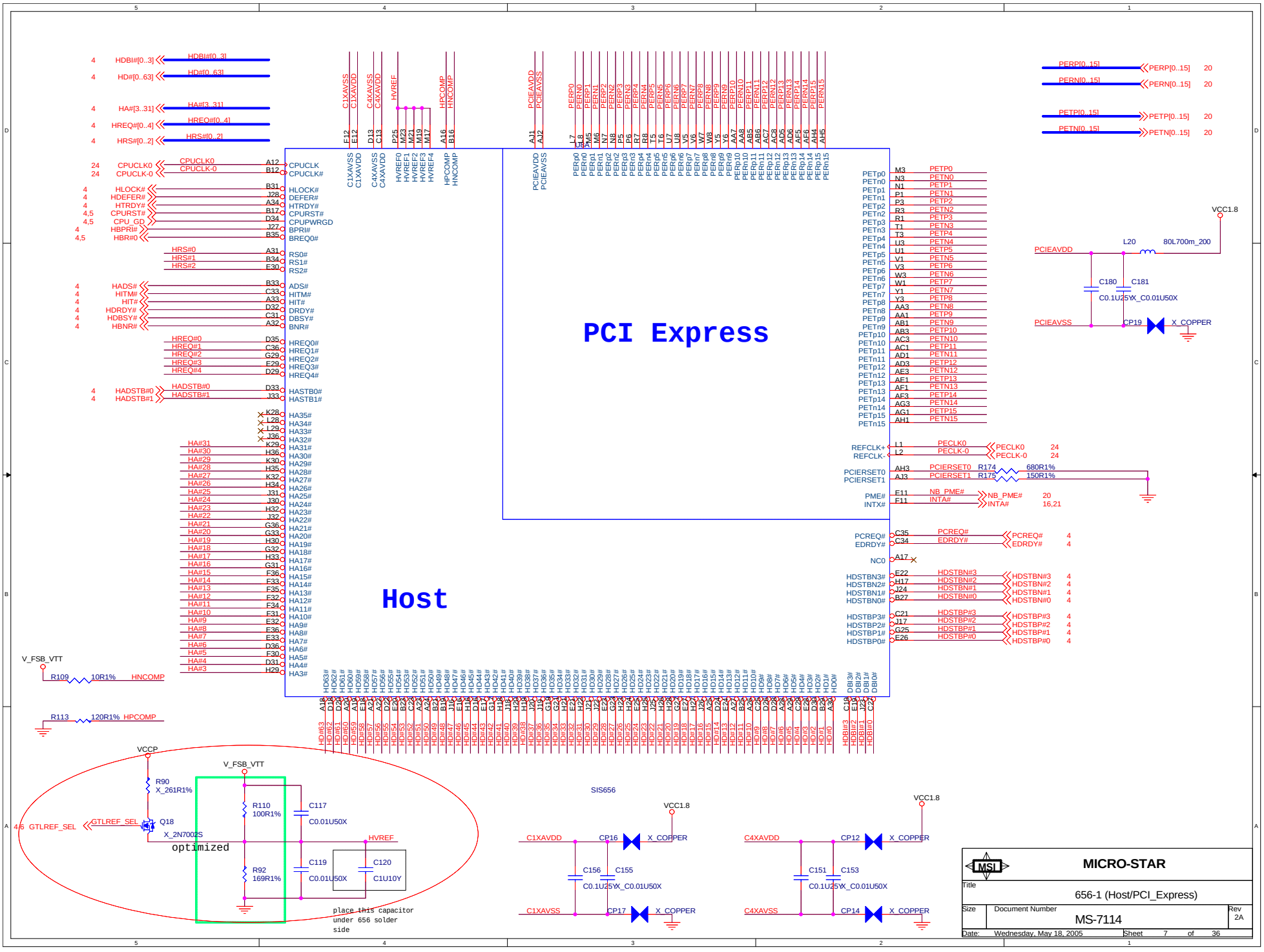
Title: Intel LGA775 CPU - Power

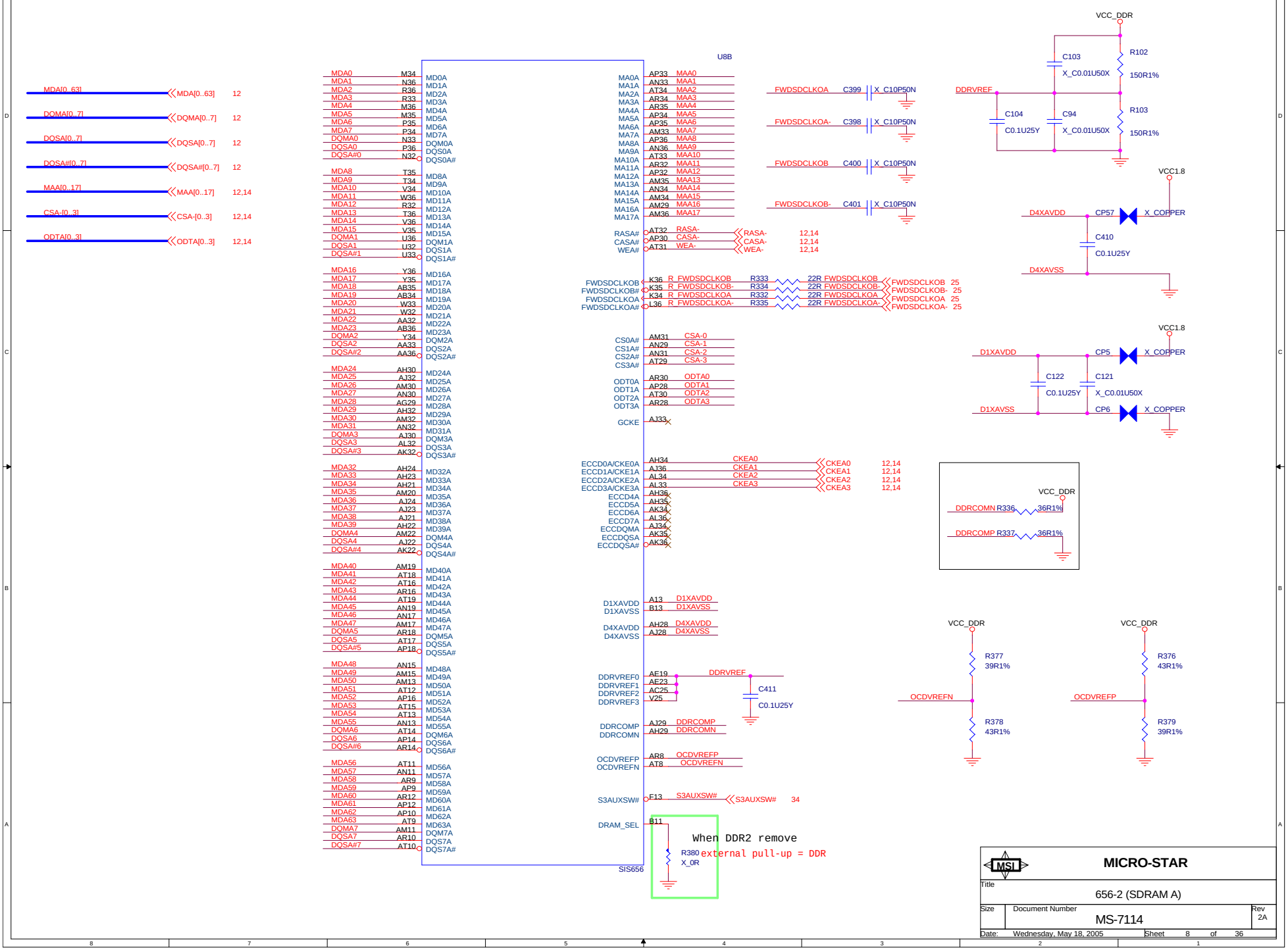
Size | Document Number: MS-7114 | Rev: 2A

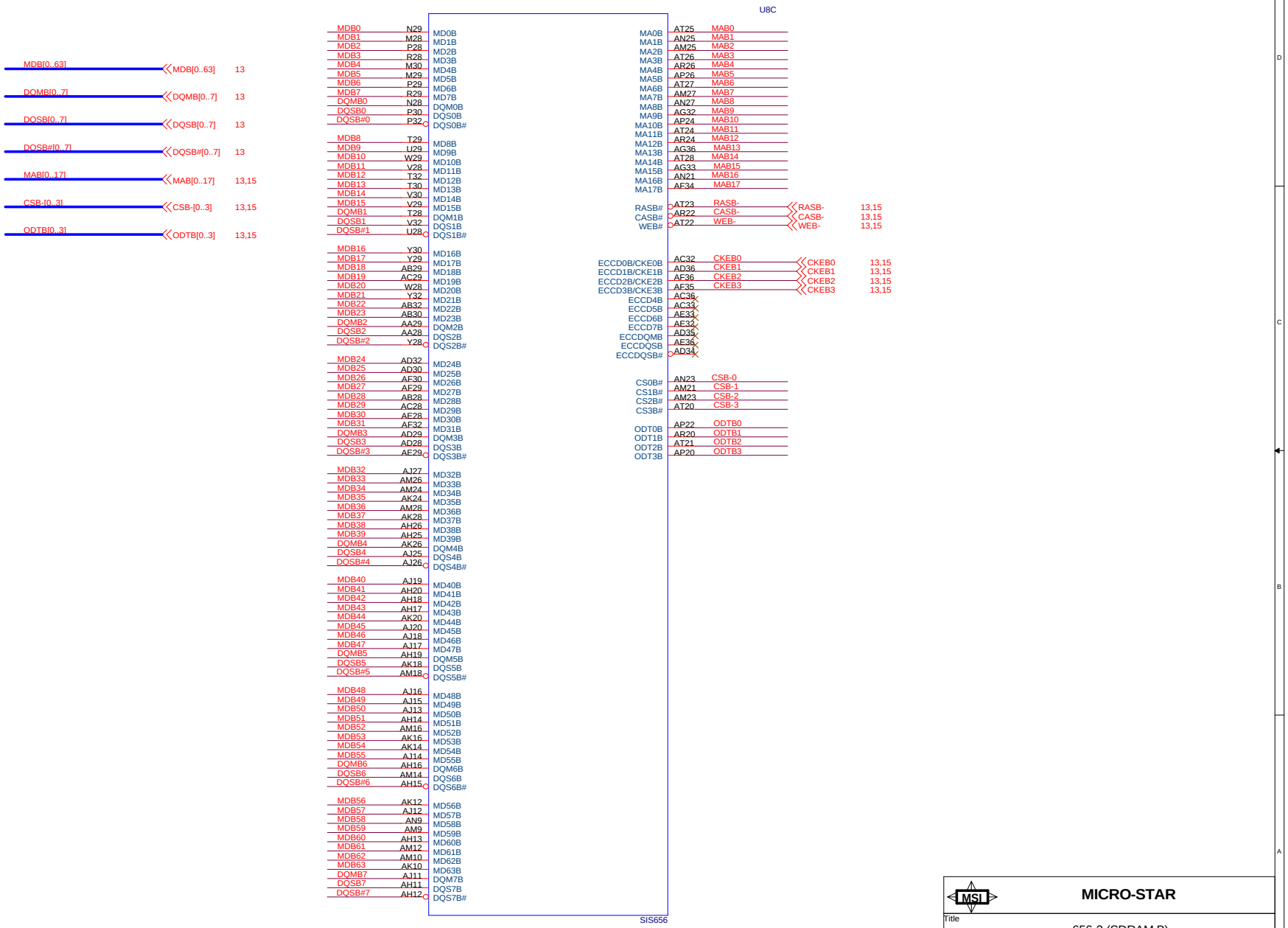
Date: Wednesday, May 18, 2005 | Sheet 5 of 36



MSI	MICRO-STAR		
Title	Intel LGA775 CPU - GND		
Size	Document Number MS-7114		Rev 2A
Date: Wednesday, May 18, 2005	Sheet 6 of 36		

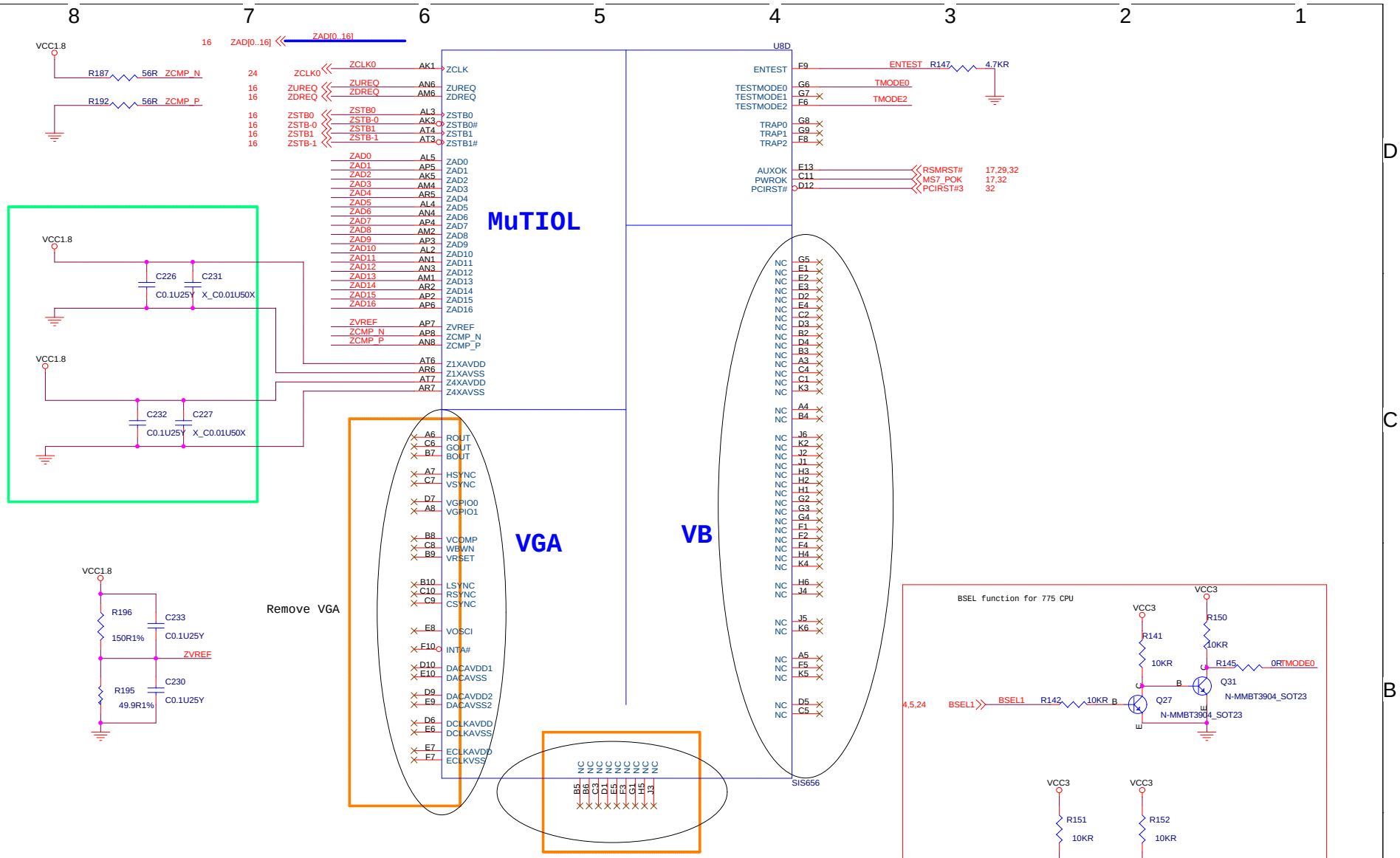

PCI Express
Host
HDBI#[0..3]
HD#[0..63]
HA#[3..31]
HREQ#[0..4]
HRS#[0..2]
CPUCLK0
CPUCLK-0
HLOCK#
HDEFER#
HTRDY#
CPURST#
CPU_GD
HBPRI#
HBR#0
HRS#0
HRS#1
HRS#2
HADS#
HITM#
HIT#
HDRDY#
HDBSY#
HBNR#
HREQ#0
HREQ#1
HREQ#2
HREQ#3
HREQ#4
HADSTB#0
HADSTB#1
C1XAVSS
C1XAVDD
C4XAVSS
C4XAVDD
HVREF
HPCOMP
HNCOMP
PCIEAVDD
PCIEAVSS
PERP[0..15]
PERN[0..15]
PETP[0..15]
PETN[0..15]
REFCLK+
REFCLK-
PCIERSET0
PCIERSET1
PME#
INTX#
PCREQ#
EDRDY#
NC0
HDSTBN3#
HDSTBN2#
HDSTBN1#
HDSTBN0#
HDSTBP3#
HDSTBP2#
HDSTBP1#
HDSTBP0#
V_FSB_VTT
R109 10R1% HNCOMP
R113 120R1% HPCOMP
VCCP
R90 X_261R1%
GTLREF_SEL
Q18 X_2N7002S
R110 100R1%
R92 169R1%
C117 C0.01U50X
C119 C0.01U50X
C120 C1U10Y
HVREF
optimized
place this capacitor under 656 solder side
SIS656
VCC1.8
C1XAVDD
C4XAVDD
C1XAVSS
C4XAVSS
CP16 X_COPPER
CP17 X_COPPER
CP12 X_COPPER
CP14 X_COPPER
C156 C155 C0.1U25%X_C0.01U50X
C151 C153 C0.1U25%X_C0.01U50X
L20 80L700m_200
C180 C181 C0.1U25%X_C0.01U50X
CP19 X_COPPER
MICRO-STAR
Title
656-1 (Host/PCI_Express)
Size
Document Number
MS-7114
Rev 2A
Date: Wednesday, May 18, 2005
Sheet 7 of 36


MDA[0..63] MDA[0..63] 12
DQMA[0..7] DQMA[0..7] 12
DQSA[0..7] DQSA[0..7] 12
DQSA#[0..7] DQSA#[0..7] 12
MAA[0..17] MAA[0..17] 12,14
CSA-[0..3] CSA-[0..3] 12,14
ODTA[0..3] ODTA[0..3] 12,14
U8B
SIS656
VCC_DDR
C103
X_C0.01U50X
R102
150R1%
DDRVREF
C104
C0.1U25Y
C94
X_C0.01U50X
R103
150R1%
VCC1.8
D4XAVDD
CP57
X_COPPER
C410
C0.1U25Y
D4XAVSS
VCC1.8
D1XAVDD
CP5
X_COPPER
C122
C0.1U25Y
C121
X_C0.01U50X
D1XAVSS
CP6
X_COPPER
DDRCOMN R336 36R1%
DDRCOMP R337 36R1%
R377 39R1%
R378 43R1%
OCDVREFN
R376 43R1%
R379 39R1%
OCDVREFP
C411
C0.1U25Y
When DDR2 remove
R380 X_0R
external pull-up = DDR
MICRO-STAR
Title
656-2 (SDRAM A)
Size
Document Number
MS-7114
Rev 2A
Date: Wednesday, May 18, 2005
Sheet 8 of 36

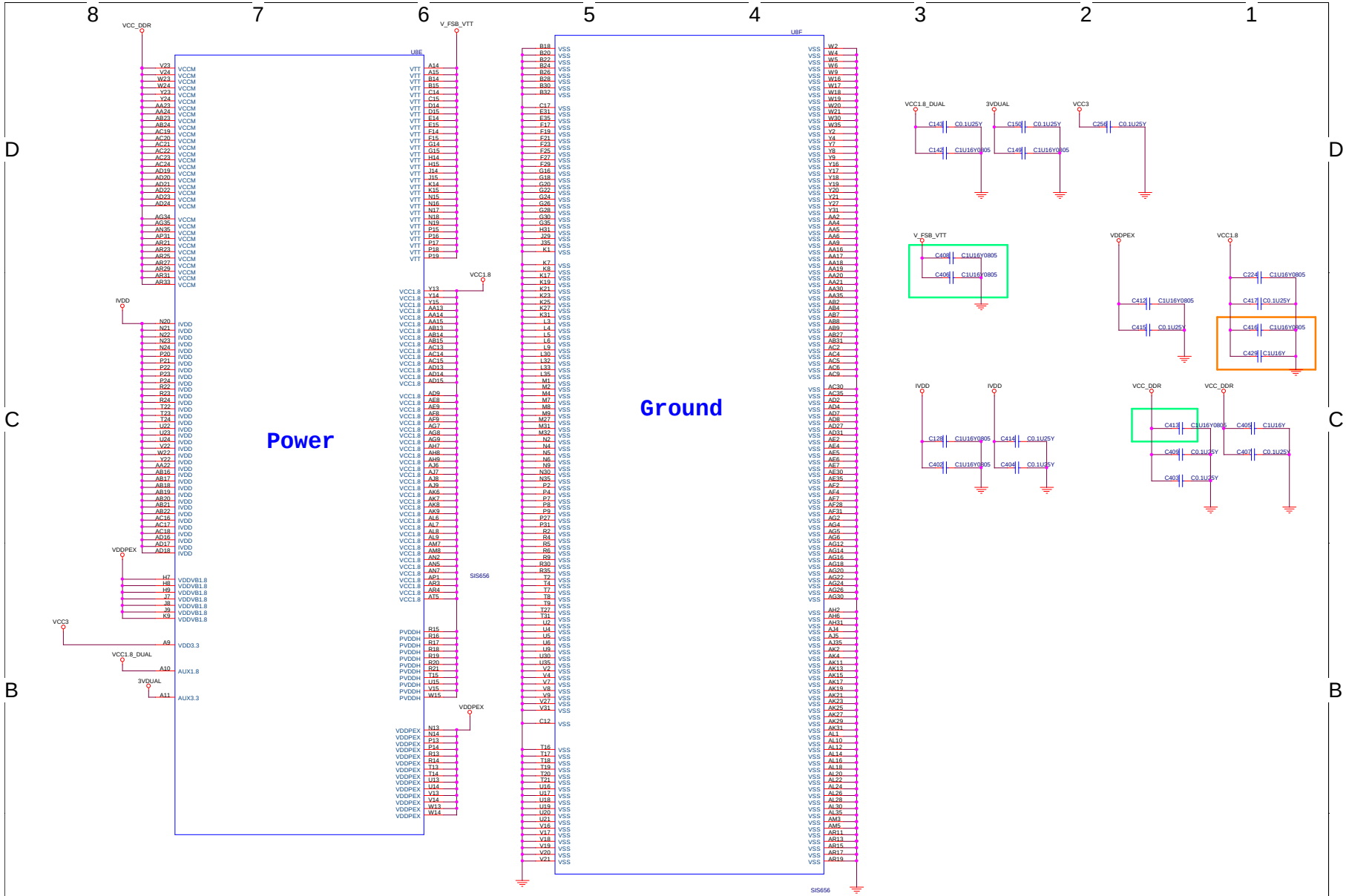


MSI **MICRO-STAR**

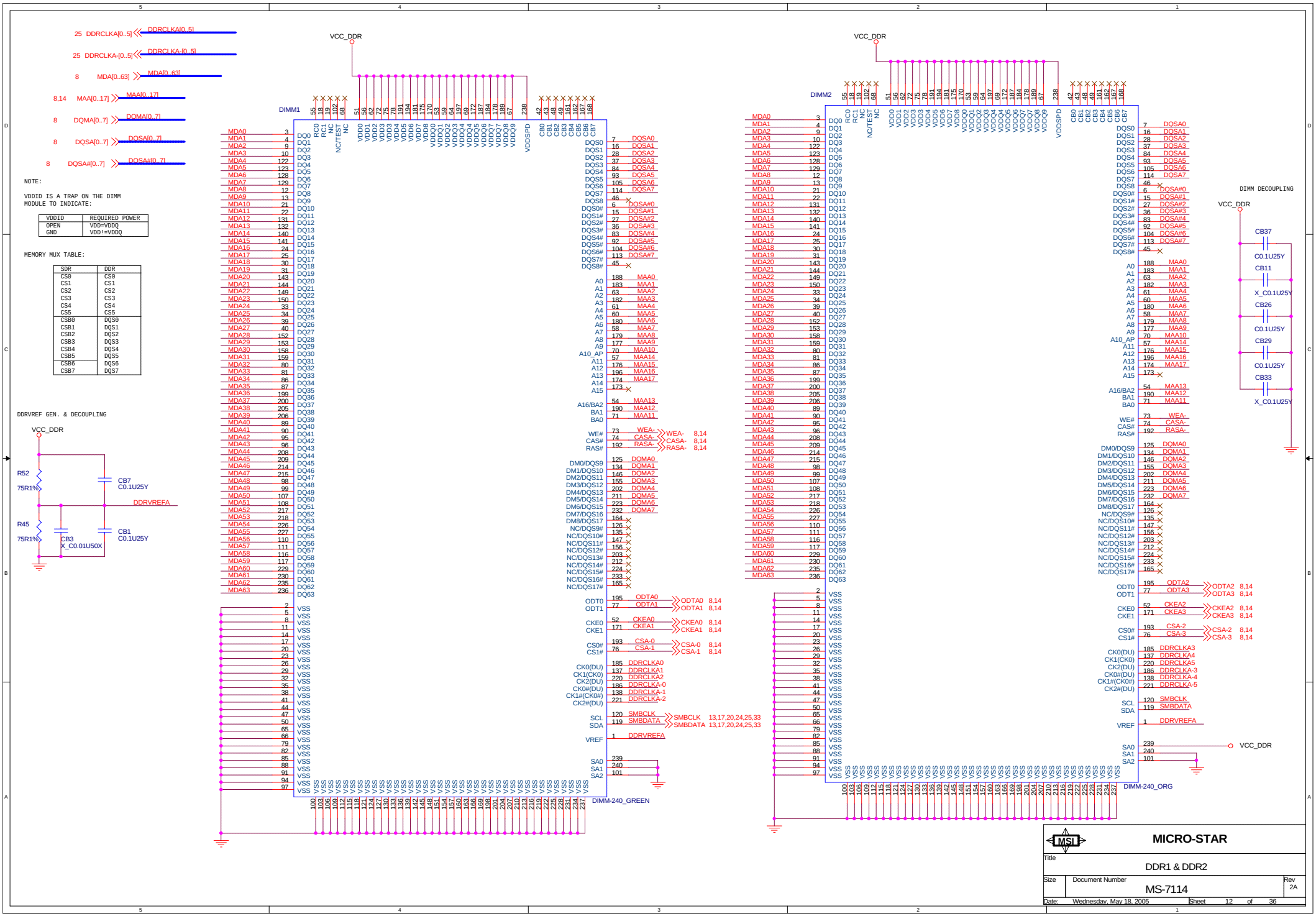
Title	656-2 (SDRAM B)	
Size	Document Number MS-7114	Rev 2A
Date: Wednesday, May 18, 2005	Sheet 9 of 36	

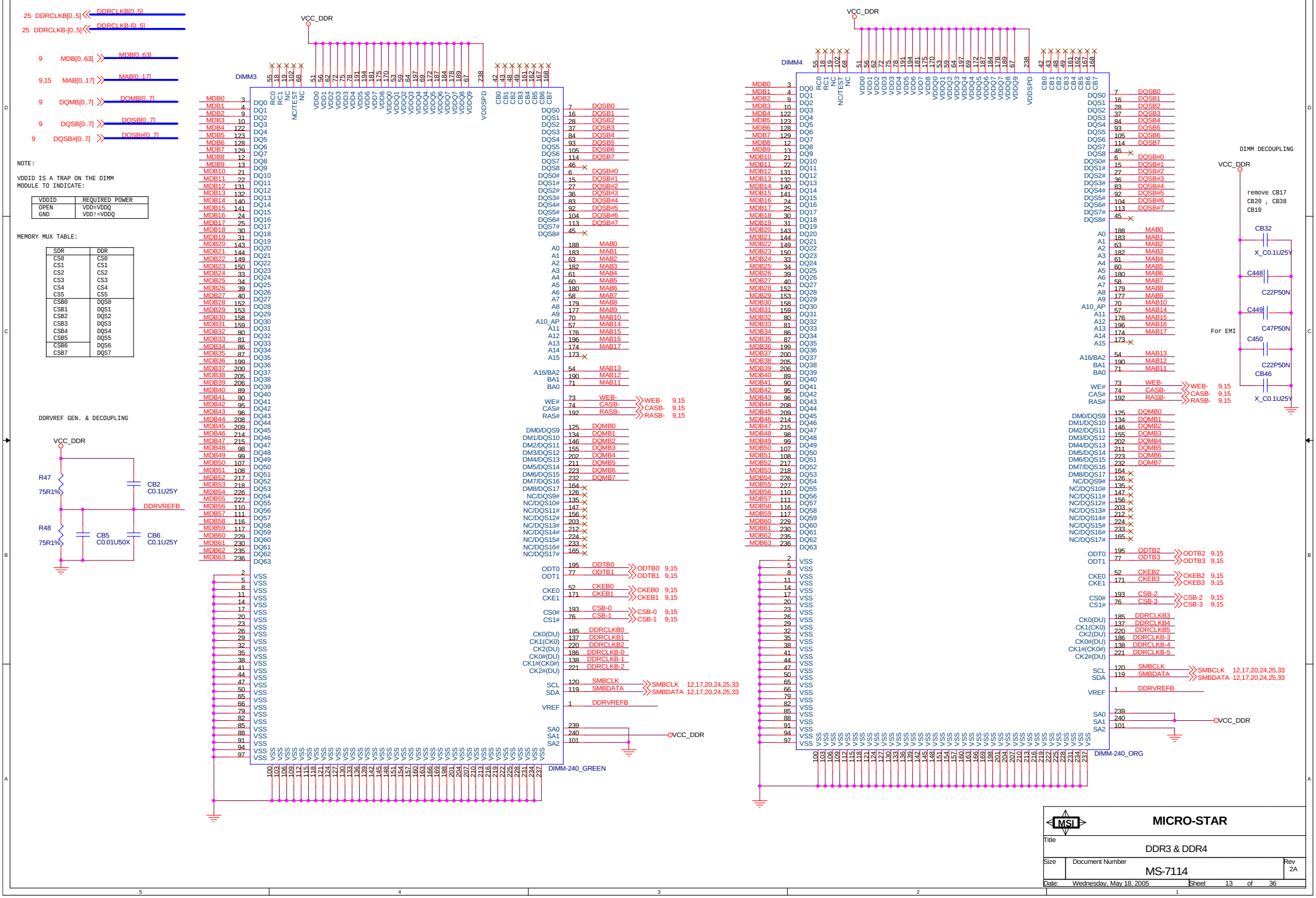


MSI	MICRO-STAR
Title	656-4 (HyperZip/Misc)
Size	Document Number: MS-7114
Rev	2A
Date:	Wednesday, May 18, 2005
Sheet	10 of 36



MSI	MICRO-STAR	
Title	656-5 (Power)	
Size	Document Number	Rev
	MS-7114	2A
Date: Wednesday, May 18, 2005	Sheet 11 of 36	


25 DDRCLKA[0..5]
DDRCLKA[0..5]
25 DDRCLKA-[0..5]
DDRCLKA-[0..5]
8 MDA[0..63]
MDA[0..63]
8,14 MAA[0..17]
MAA[0..17]
8 DQMA[0..7]
DQMA[0..7]
8 DQSA[0..7]
DQSA[0..7]
8 DQSA#[0..7]
DQSA#[0..7]
NOTE:
VDDID IS A TRAP ON THE DIMM MODULE TO INDICATE:
VDDID | REQUIRED POWER
OPEN | VDD=VDDQ
GND | VDD!=VDDQ
MEMORY MUX TABLE:
SDR | DDR
CS0 | CS0
CS1 | CS1
CS2 | CS2
CS3 | CS3
CS4 | CS4
CS5 | CS5
CSB0 | DQS0
CSB1 | DQS1
CSB2 | DQS2
CSB3 | DQS3
CSB4 | DQS4
CSB5 | DQS5
CSB6 | DQS6
CSB7 | DQS7
DDRVREF GEN. & DECOUPLING
VCC_DDR
R52
75R1%
R45
75R1%
CB7
C0.1U25Y
DDRVREFA
CB1
C0.1U25Y
CB3
X_C0.01U50X
DIMM1
VCC_DDR
DIMM-240_GREEN
DIMM2
VCC_DDR
DIMM-240_ORG
DIMM DECOUPLING
VCC_DDR
CB37
C0.1U25Y
CB11
X_C0.1U25Y
CB26
C0.1U25Y
CB29
C0.1U25Y
CB33
X_C0.1U25Y
MSI
MICRO-STAR
Title
DDR1 & DDR2
Size
Document Number
MS-7114
Rev
2A
Date: Wednesday, May 18, 2005
Sheet 12 of 36


25 DDRCLKB[0..5]
DDRCLKB[0..5]
25 DDRCLKB-[0..5]
DDRCLKB-[0..5]
9 MDB[0..63]
MDB[0..63]
9,15 MAB[0..17]
MAB[0..17]
9 DQMB[0..7]
DQMB[0..7]
9 DQSB[0..7]
DQSB[0..7]
9 DQSB#[0..7]
DQSB#[0..7]
NOTE:
VDDID IS A TRAP ON THE DIMM MODULE TO INDICATE:
VDDID | REQUIRED POWER
OPEN | VDD=VDDQ
GND | VDD!=VDDQ
MEMORY MUX TABLE:
SDR | DDR
CS0 | CS0
CS1 | CS1
CS2 | CS2
CS3 | CS3
CS4 | CS4
CS5 | CS5
CSB0 | DQS0
CSB1 | DQS1
CSB2 | DQS2
CSB3 | DQS3
CSB4 | DQS4
CSB5 | DQS5
CSB6 | DQS6
CSB7 | DQS7
DDRVREF GEN. & DECOUPLING
VCC_DDR
R47
75R1%
CB2
C0.1U25Y
DDRVREFB
R48
75R1%
CB5
C0.01U50X
CB6
C0.1U25Y
VCC_DDR
DIMM3
DIMM-240_GREEN
DIMM4
DIMM-240_ORG
DIMM DECOUPLING
remove CB17
CB20 , CB38
CB10
CB32
X_C0.1U25Y
C448
C22P50N
C449
C47P50N
For EMI
C450
C22P50N
CB46
X_C0.1U25Y
MSI
MICRO-STAR
Title
DDR3 & DDR4
Size
Document Number
MS-7114
Rev
2A
Date: Wednesday, May 18, 2005
Sheet 13 of 36

DDR TERMINATOR

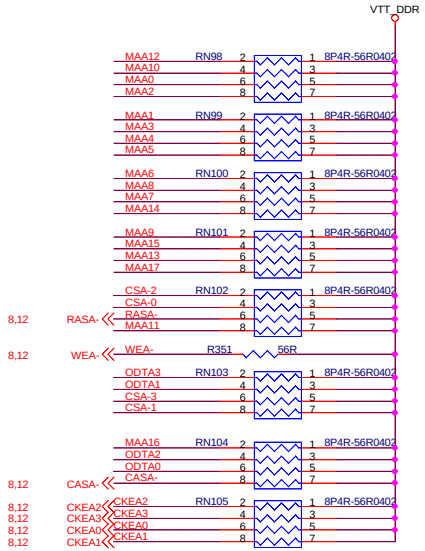
SSTL-2 Termination Resistors

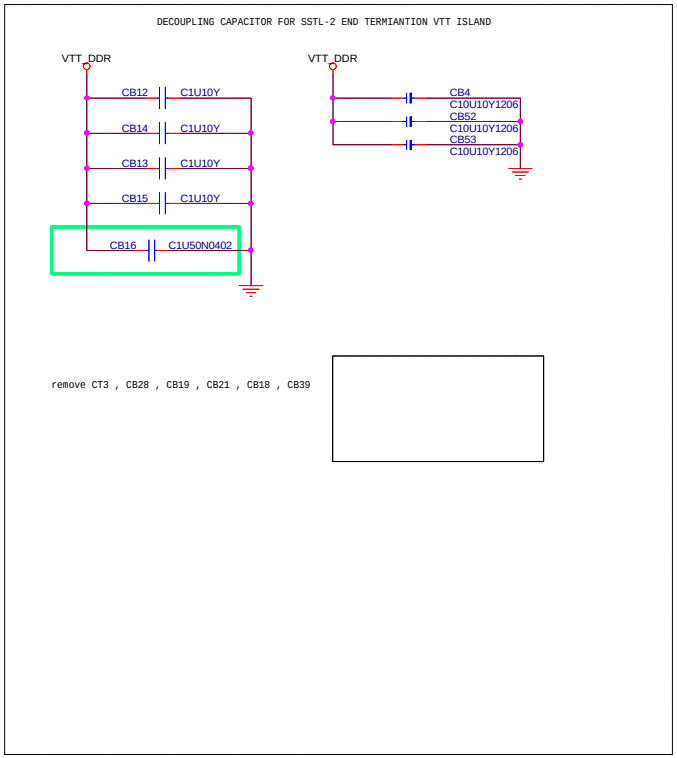
MAA[0..17] — MAA[0..17] 8,12

CSA-[0..3] — CSA-[0..3] 8,12

ODTA[0..3] — ODTA[0..3] 8,12

	SDR		DDR		
		Rs		Rs	Rtt
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	10	33
MA/Control	LV-CMOS	10	SSTL-2	0	33
CS	LV-CMOS	0	SSTL-2	0	47
CKE	OD 3.3V		OD 2.5V		





MICRO-STAR

Title: DDRA TERMINATOR

Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 14 of 36

DDR TERMINATOR

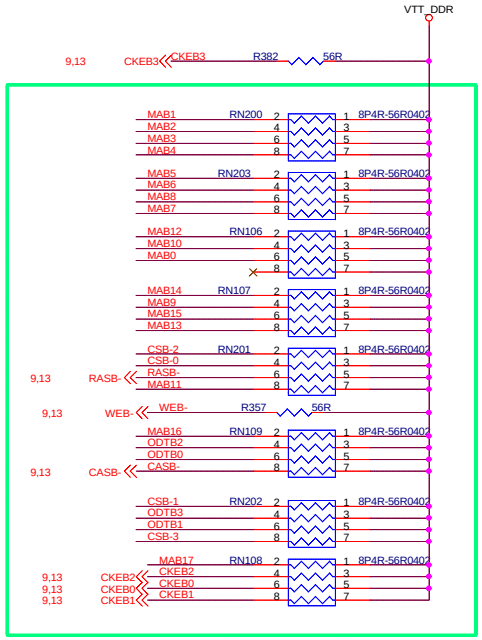
SSTL-2 Termination Resistors

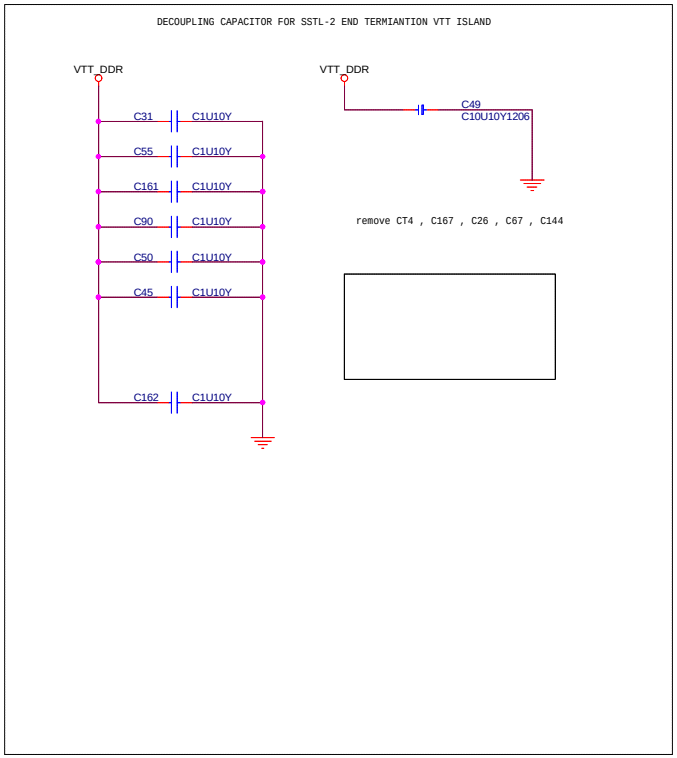
	SDR		DDR		
		Rs		Rs	Rtt
MD/DQM(/DQS)	LV-CMOS	0/10/-	SSTL-2	10	33
MA/Control	LV-CMOS	10	SSTL-2	0	33
CS	LV-CMOS	0	SSTL-2	0	47
CKE	DD 3.3V		DD 2.5V		

MAB[0..17] → MAB[0..17] 9,13

CSB-[0..3] → CSB-[0..3] 9,13

ODTB[0..3] → ODTB[0..3] 9,13



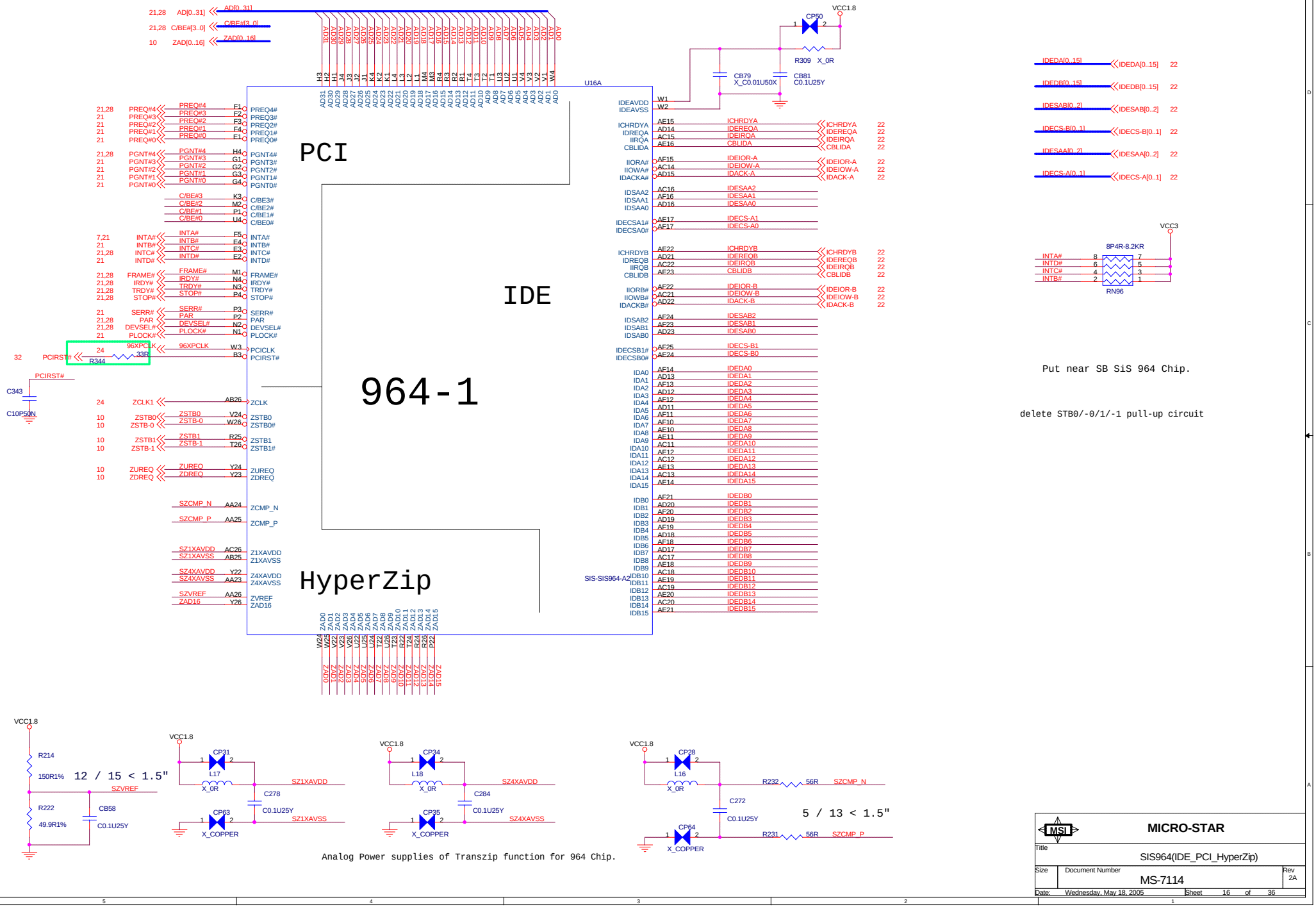


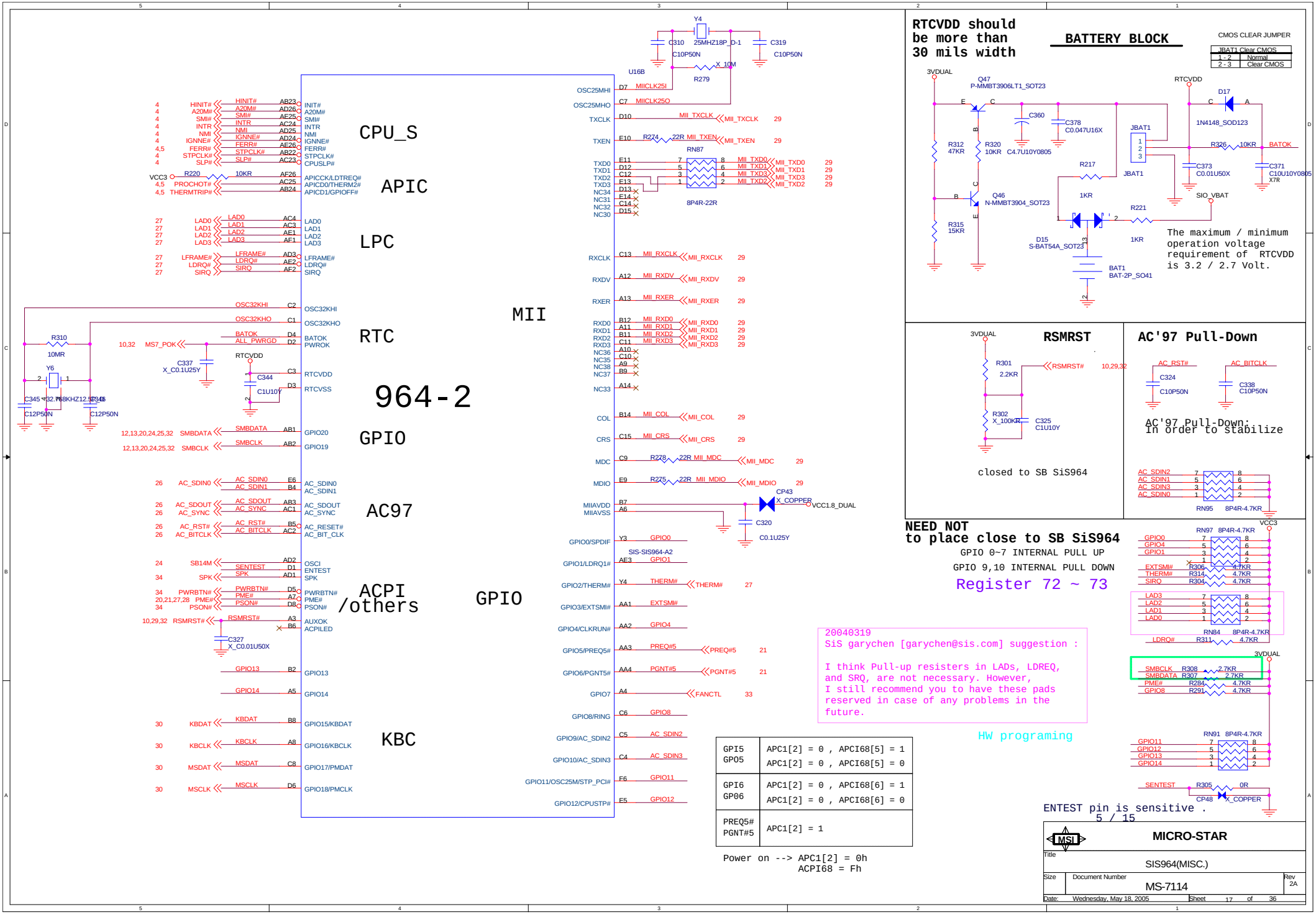
MICRO-STAR

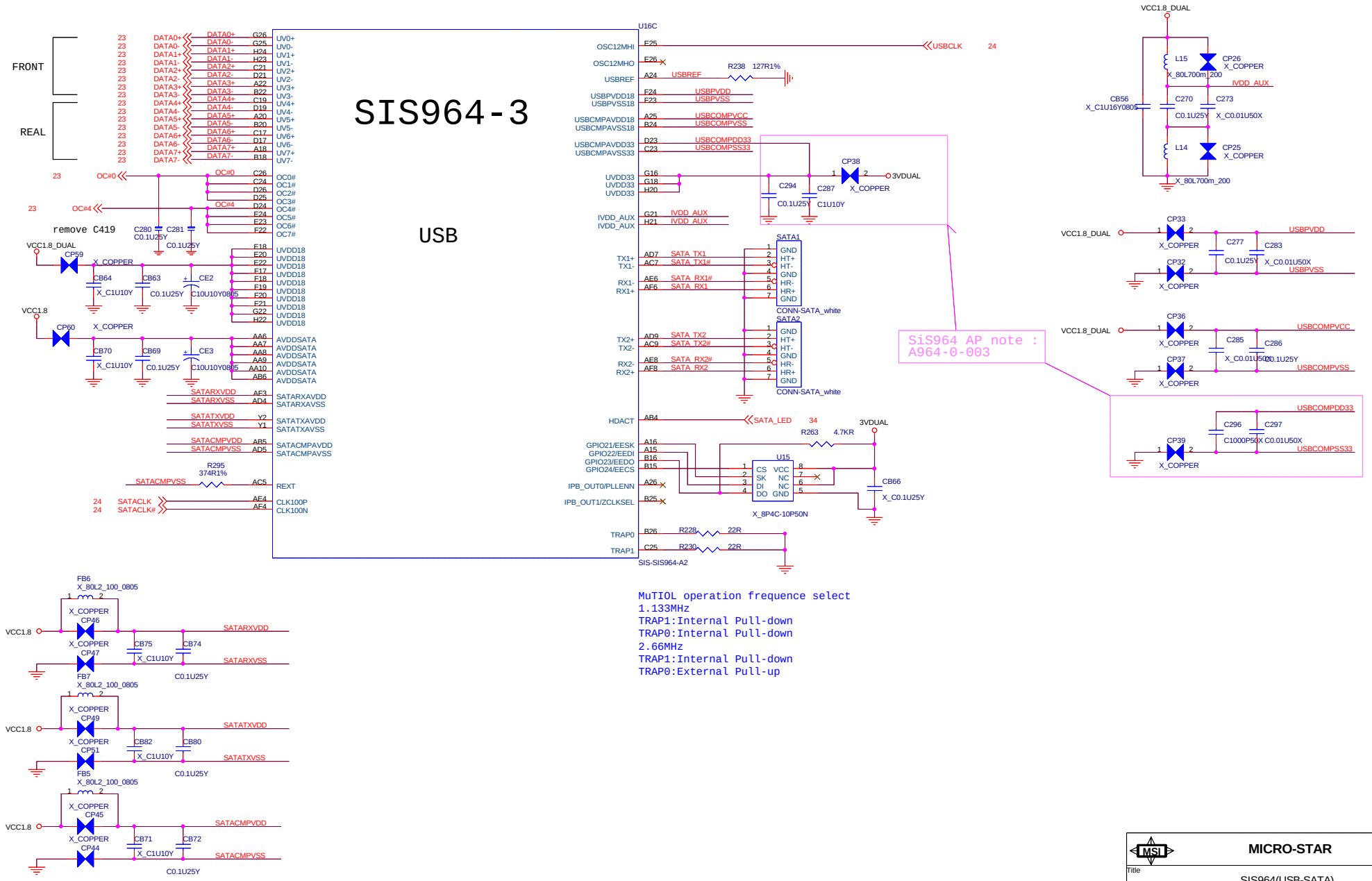
Title: DDRB TERMINATOR

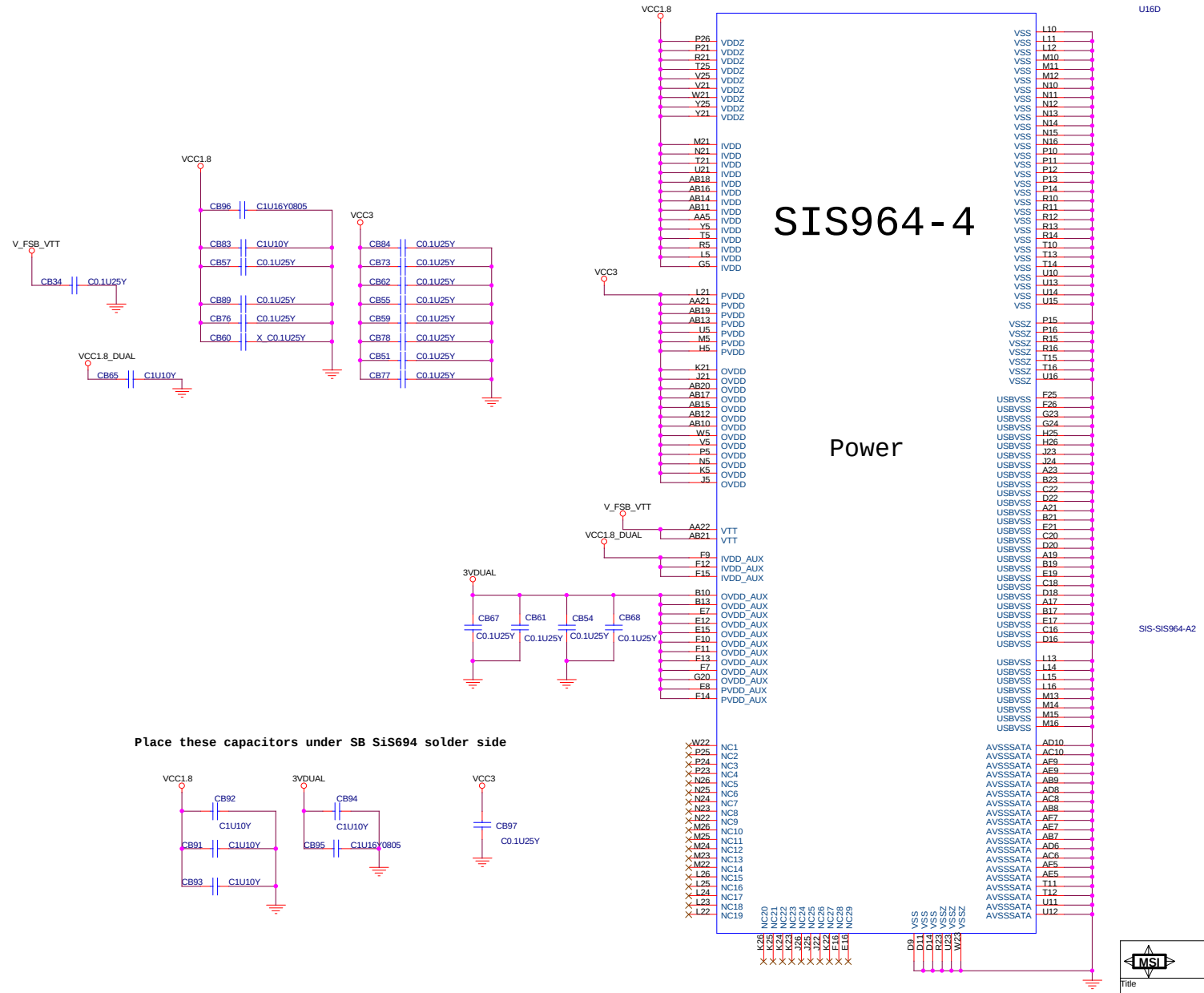
Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 15 of 36

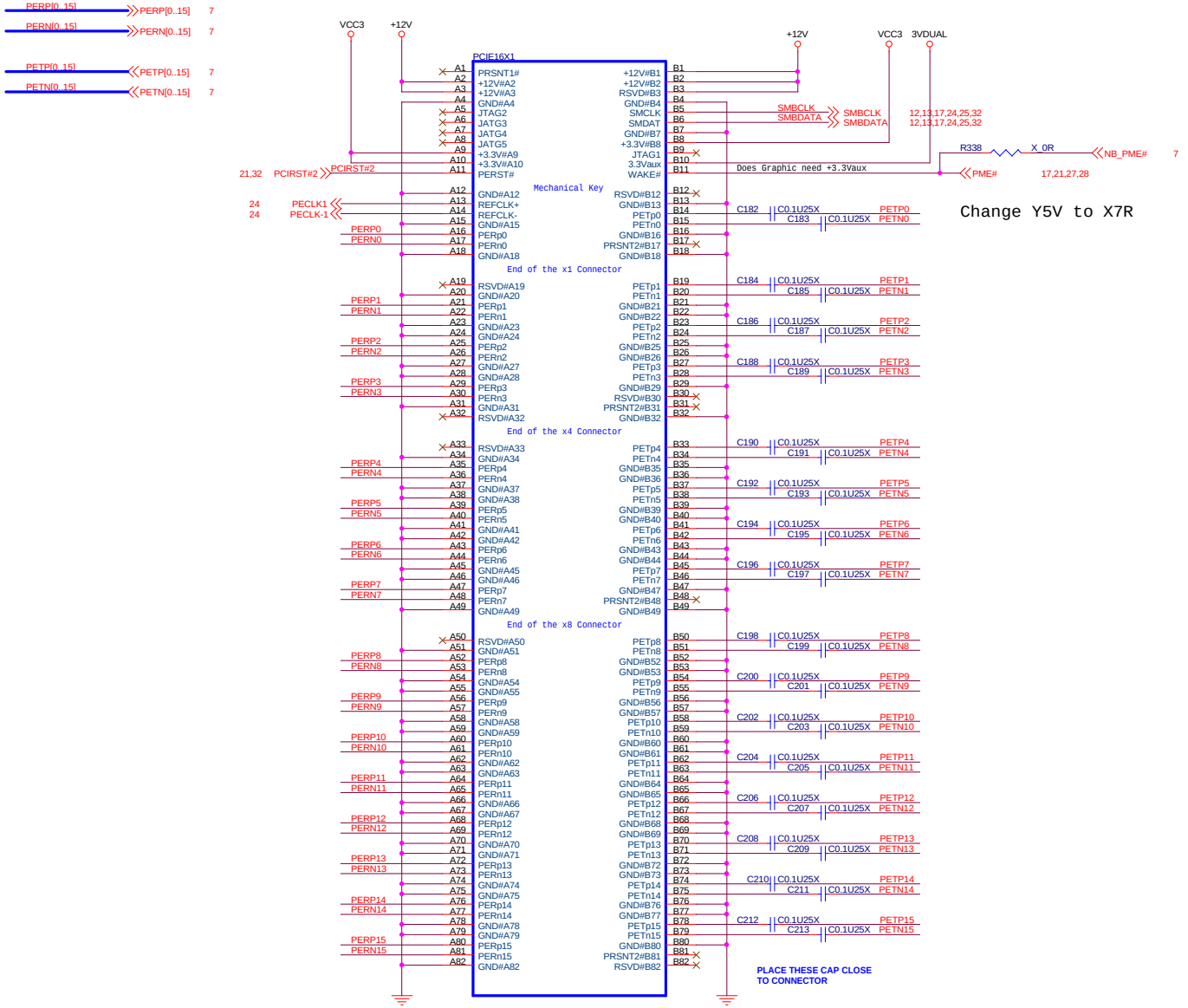

PCI
IDE
964-1
HyperZip
U16A
AD[0..31]
C/BE#[3..0]
ZAD[0..16]
PCIRST#
R344 33R
C343
C10P50N
R309 X_0R
CB79 X_C0.01U50X
CB81 C0.1U25Y
CP50
VCC1.8
IDEDA[0..15]
IDEDB[0..15]
IDESAB[0..2]
IDECS-B[0..1]
IDESAA[0..2]
IDECS-A[0..1]
8P4R-8.2KR
RN96
VCC3
Put near SB SiS 964 Chip.
delete STB0/-0/1/-1 pull-up circuit
R214 150R1%
R222 49.9R1%
CB58 C0.1U25Y
SZVREF
12 / 15 < 1.5"
CP31
L17 X_0R
C278 C0.1U25Y
CP63 X_COPPER
SZ1XAVDD
SZ1XAVSS
CP34
L18 X_0R
C284 C0.1U25Y
CP35 X_COPPER
SZ4XAVDD
SZ4XAVSS
CP28
L16 X_0R
C272 C0.1U25Y
CP64 X_COPPER
R232 56R SZCMP_N
R231 56R SZCMP_P
5 / 13 < 1.5"
Analog Power supplies of Transzip function for 964 Chip.
MICRO-STAR
SIS964(IDE_PCI_HyperZip)
MS-7114
Wednesday, May 18, 2005
Sheet 16 of 36


964-2
CPU_S
APIC
LPC
RTC
GPIO
AC97
ACPI /others
KBC
MII
GPIO
BATTERY BLOCK
RTCVDD should be more than 30 mils width
CMOS CLEAR JUMPER
JBAT1 Clear CMOS
1 - 2 Normal
2 - 3 Clear CMOS
The maximum / minimum operation voltage requirement of RTCVDD is 3.2 / 2.7 Volt.
RSMRST
closed to SB SiS964
AC'97 Pull-Down
AC'97 Pull-Down: In order to stabilize
NEED NOT to place close to SB SiS964
GPIO 0~7 INTERNAL PULL UP
GPIO 9,10 INTERNAL PULL DOWN
Register 72 ~ 73
20040319
SiS garychen [garychen@sis.com] suggestion :
I think Pull-up resisters in LADs, LDREQ, and SRQ, are not necessary. However, I still recommend you to have these pads reserved in case of any problems in the future.
HW programing
GPI5 GPO5 | APC1[2] = 0 , APCI68[5] = 1 | APC1[2] = 0 , APCI68[5] = 0
GPI6 GP06 | APC1[2] = 0 , APCI68[6] = 1 | APC1[2] = 0 , APCI68[6] = 0
PREQ5# PGNT#5 | APC1[2] = 1
Power on --> APC1[2] = 0h
ACPI68 = Fh
ENTEST pin is sensitive .
5 / 15
MICRO-STAR
SIS964(MISC.)
MS-7114
Wednesday, May 18, 2005
17 of 36


SIS964-3
USB
FRONT
REAL
remove C419
SiS964 AP note : A964-0-003
MuTIOL operation frequence select
1.133MHz
TRAP1:Internal Pull-down
TRAP0:Internal Pull-down
2.66MHz
TRAP1:Internal Pull-down
TRAP0:External Pull-up
SIS-SIS964-A2
MICRO-STAR
SIS964(USB-SATA)
MS-7114
Wednesday, May 18, 2005



MSI	MICRO-STAR		
Title	SIS964(POWER)		
Size	Document Number	MS-7114	Rev 2A
Date: Wednesday, May 18, 2005	Sheet 19 of 36		



Title	PCI EXPRESS
Size	Document Number: MS-7114
Rev	2A
Date:	Wednesday, May 18, 2005
Sheet	20 of 36

MICRO-STAR

PCI SLOT 1,2,3(PCI VER:2.2 COMPLY)

PCI1 = INTB#
IDSEL = AD17
MASTER = PREQ#0

PCI2 = INTC# and INTB#
IDSEL = AD18 and AD21
MASTER = PREQ#1 and PREQ#3

PCI3 = INTD#
IDSEL = AD19
MASTER = PREQ#2

16,28 AD[0..31]
16,28 C/BE#[3..0]

SLOT-PCI

SLOT-PCI120_green

SLOT-PCI

20040319
SiS DG06 Page 55/44
All PREQ# signals should pull high even the corresponding PCI slot is not mounted

PCI BUS PULL-UP

RESERVED

Remove ACK64# and REQ64# and SB0#

MICRO-STAR

Title: PCI slot 1 & 2 & 3

Size: | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 21 of 36

IDE BOOT TIME ISSUE ,VER:1

IDE1 & IDE2

20040319
SiS AP note : A964008

20040319
SiS DG06 Page 53/42

IDEDA7 — R277 5.6KR

16 IDEDA[0..15] — IDEDA[0..15]

32 HDDRST# — HDDRST# — R183 22R — HDRSTP# — IDE1

VCC3 — R120 X_4.7KR

IDEDA7 IDEDA6 IDEDA5 IDEDA4 IDEDA3 IDEDA2 IDEDA1 IDEDA0
IDEDA8 IDEDA9 IDEDA10 IDEDA11 IDEDA12 IDEDA13 IDEDA14 IDEDA15

16 IDEREQA
16 IDEIOW-A
16 IDEIOR-A
16 ICHRDYA
16 IDACK-A
16 IDEIRQA

R108 X_10KR — R138 X_5.6KR

IDESAA1 IDESAA0 IDECS-A0

34 IDEACTP# — R104 4.7KR — VCC

CONN-IDE(20)V_blue
ATA66/100/133

N32-2201061-H06 Blue

CBLIDA — R106 X_15KR — CBLIDA 16

16 IDESAA[0..2] — IDESAA[0..2]
16 IDECS-A[0..1] — IDECS-A[0..1]

IDE BOOT TIME ISSUE ,VER:1
IDEDB7 — R264 5.6KR

PLANE CAP

16 IDEDB[0..15] — IDEDB[0..15]

HDDRST# — R182 22R — HDRSTS# — IDE2

VCC3 — R115 X_4.7KR

IDEDB7 IDEDB6 IDEDB5 IDEDB4 IDEDB3 IDEDB2 IDEDB1 IDEDB0
IDEDB8 IDEDB9 IDEDB10 IDEDB11 IDEDB12 IDEDB13 IDEDB14 IDEDB15

16 IDEREQB
16 IDEIOW-B
16 IDEIOR-B
16 ICHRDYB
16 IDACK-B
16 IDEIRQB

R112 X_10KR — R128 X_5.6KR

16 IDESAB1
16 IDESAB0
16 IDECS-B0

34 IDEACTS# — R100 4.7KR — VCC

CONN-20P-IDE-white
ATA66/100/133

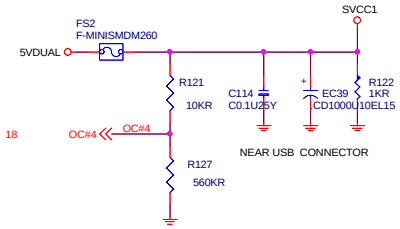
N32-2201071-H06 White

CBLIDB — R105 X_15KR — CBLIDB 16

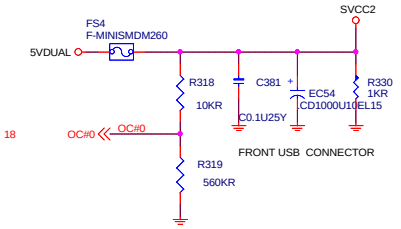
16 IDESAB[0..2] — IDESAB[0..2]
16 IDECS-B[0..1] — IDECS-B[0..1]

MSI	MICRO-STAR	
Title	IDE-ATA	
Size	Document Number MS-7114	Rev 2A
Date: Wednesday, May 18, 2005	Sheet 22 of 36	

POWER CIRCUIT FOR USB PORT 4,5,6,7

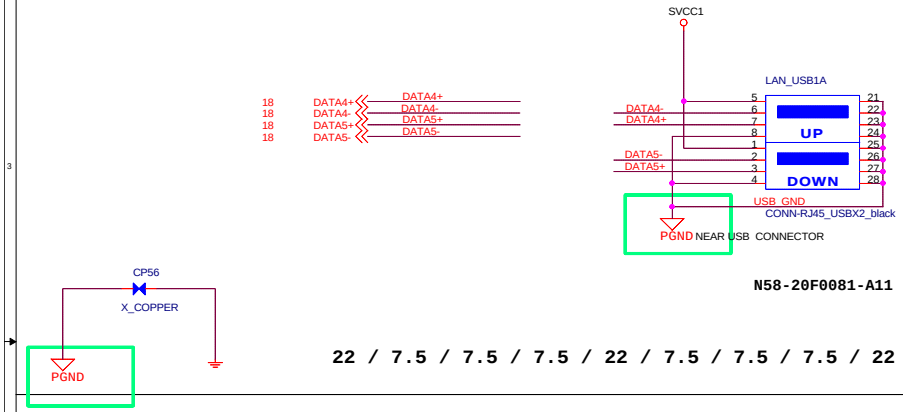


POWER CIRCUIT FOR USB PORT 0,1,2,3



Cheange location and remove

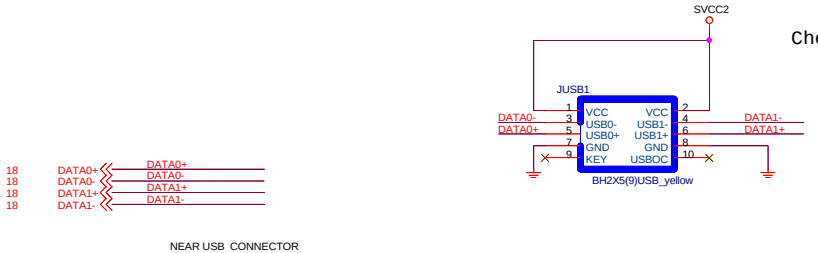
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



N58-20F0081-A11

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

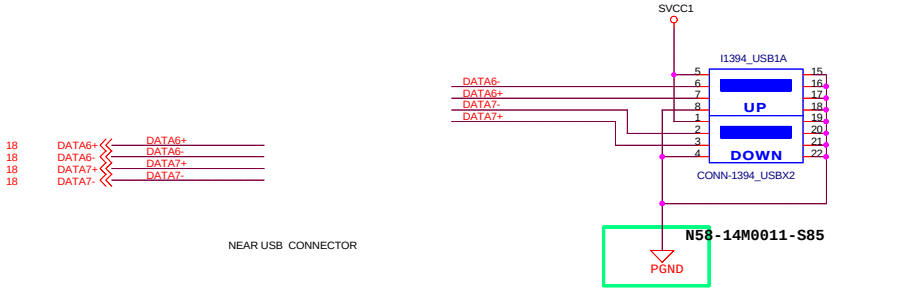
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



Cheange location and remove

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

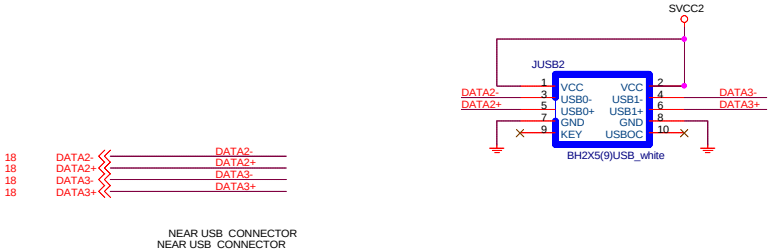
REAR PANEL USB CONNECTOR FOR USB PORT 6,7



N58-14M0011-S85

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

MSI MICRO-STAR

Title: USB CONNECTORS

Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 23 of 36

Main Clock Generator

OPTIONS

1. ICS953401

add bead

U9
CS953401CF

FS4	FS3	FS2	FS1	FS0	CPU	PCI
0	0	0	0	0	266.66	33.33
0	0	0	0	1	133.33	33.33
0	0	0	1	0	200.00	33.33
0	0	0	1	1	166.66	33.33

PCICLK0	PCI2 master3
PCICLK1	PCI1
PCICLK2	PCI3
PCICLK3	PCI2 master2
PCICLK4	PCI2 master1

0 = 48M
1 = 12M

0 = enable PCIEXCLK3/4
1 = PCICLK5

0 = Desktop
1 = noteboot

Remove level shift circuit

Frequency Selection

By-Pass Capacitors
Place near to the Clock Outputs

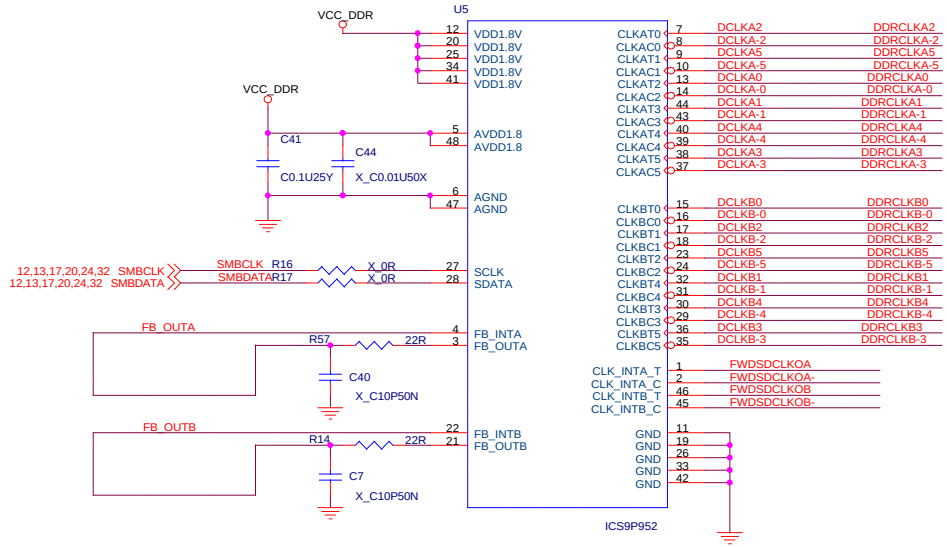
Title	Main Clock Generator
Size	Document Number: MS-7114
Rev	2A
Date:	Wednesday, May 18, 2005
Sheet	24 of 36

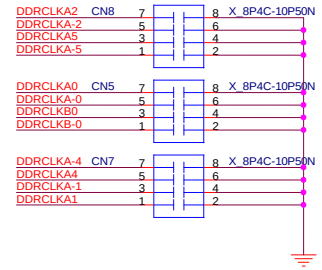
MICRO-STAR

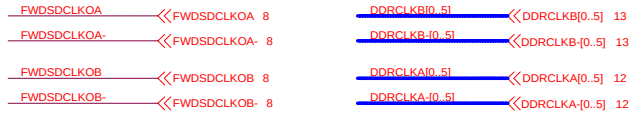
Clock Buffer (DDR II)

By-Pass Capacitors
Place near to the Clock Buffer

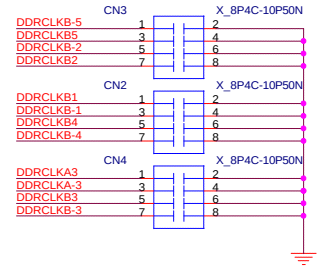
Remove demping resister



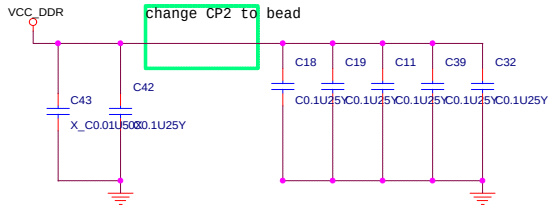




By-Pass Capacitors
Place near to the Clock Buffer

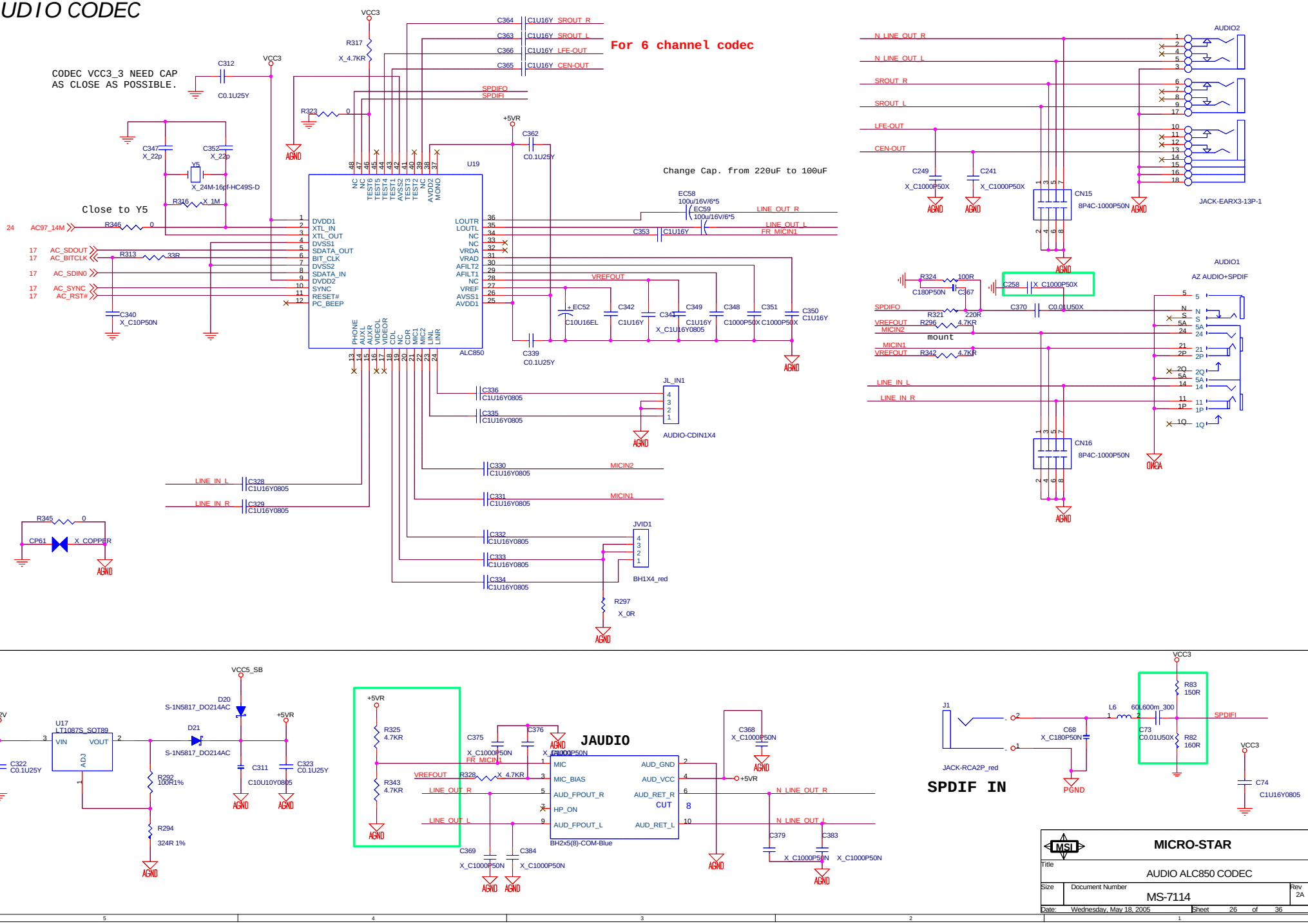


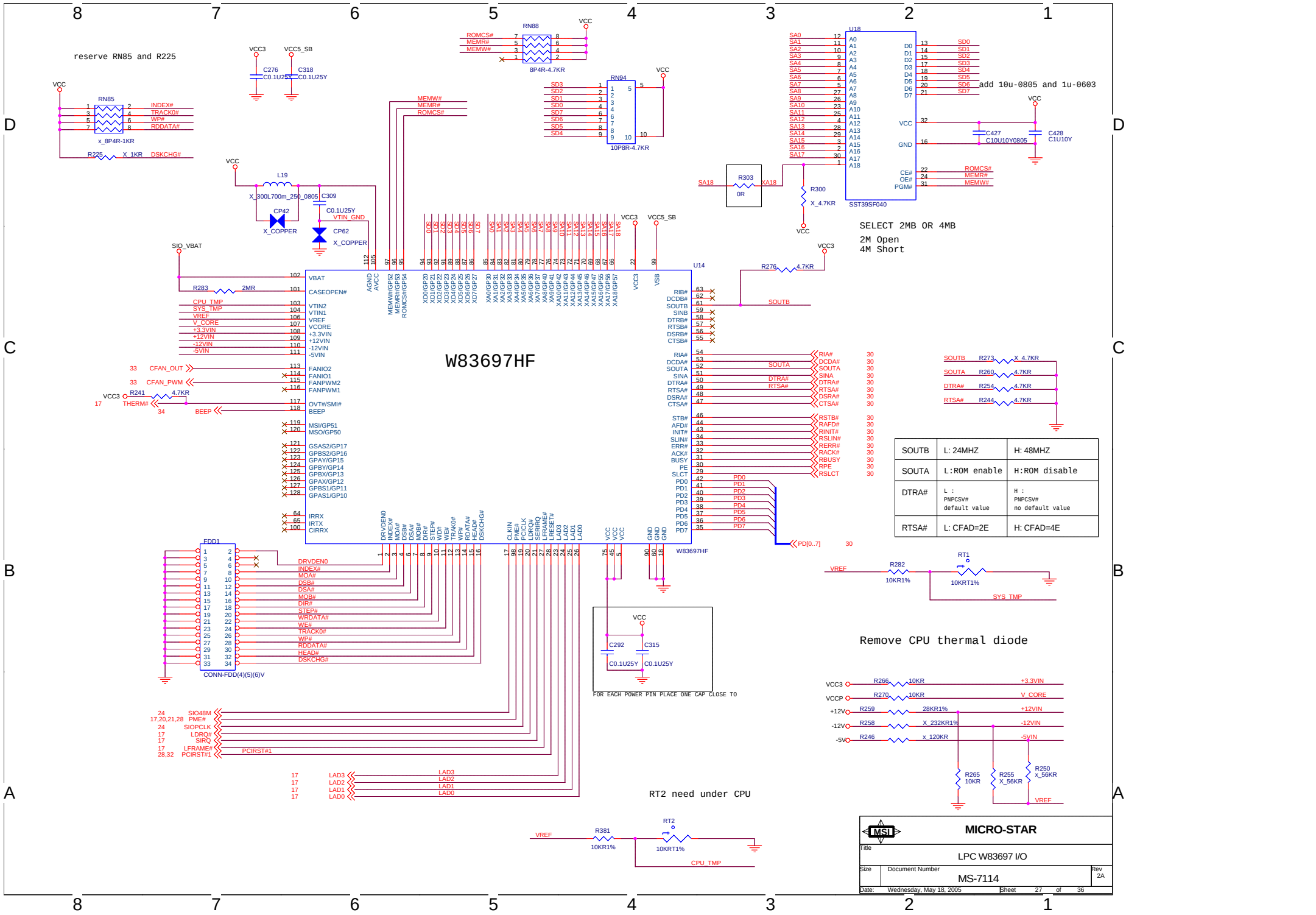
DDRVREF GEN. & DECOUPLING



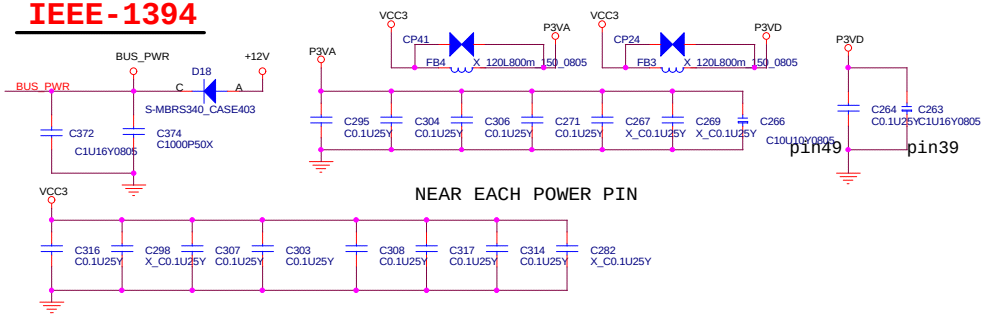
MSI	MICRO-STAR		
Title	Clock Buffer		
Size	Document Number		Rev
	MS-7114		2A
Date:	Wednesday, May 18, 2005	Sheet 25 of 36	

AUDIO CODEC

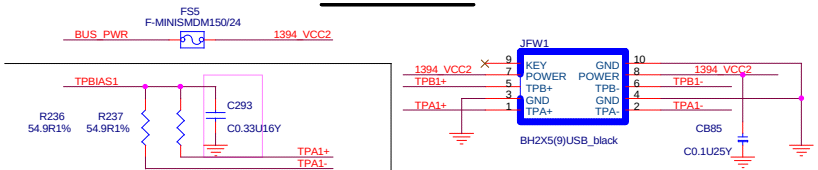

For 6 channel codec
CODEC VCC3_3 NEED CAP AS CLOSE AS POSSIBLE.
Close to Y5
Change Cap. from 220uF to 100uF
ALC850
AUDIO-CDIN1X4
BH1X4_red
JACK-EARX3-13P-1
8P4C-1000P50N
mount
JAUDIO
BH2x5(8)-COM-Blue
JACK-RCA2P_red
SPDIF IN
MICRO-STAR
AUDIO ALC850 CODEC
MS-7114
Wednesday, May 18, 2005

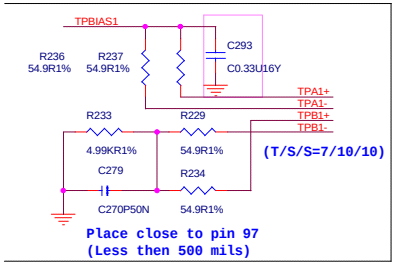

reserve RN85 and R225
RN85
x_8P4R-1KR
R225 X_1KR DSKCHG#
C276 C0.1U25Y
C318 C0.1U25Y
RN88
8P4R-4.7KR
RN94
10P8R-4.7KR
U18
SST39SF040
add 10u-0805 and 1u-0603
C427 C10U10Y0805
C428 C1U10Y
R303 0R
R300 X_4.7KR
SELECT 2MB OR 4MB
2M Open
4M Short
L19 X_300L700m_250_0805
C309 C0.1U25Y
CP42 X_COPPER
CP62 X_COPPER
VTIN_GND
SIO_VBAT
W83697HF
U14
R283 2MR
R276 4.7KR
R241 4.7KR
R273 X_4.7KR
R260 4.7KR
R254 4.7KR
R244 4.7KR
SOUTB L: 24MHZ H: 48MHZ
SOUTA L:ROM enable H:ROM disable
DTRA# L : PNPCSV# default value H : PNPCSV# no default value
RTSA# L: CFAD=2E H: CFAD=4E
FDD1
CONN-FDD(4)(5)(6)V
C292 C0.1U25Y
C315 C0.1U25Y
FOR EACH POWER PIN PLACE ONE CAP CLOSE TO
R282 10KR1%
RT1 10KRT1%
Remove CPU thermal diode
R266 10KR
R270 10KR
R259 28KR1%
R258 X_232KR1%
R246 x_120KR
R265 10KR
R255 X_56KR
R250 x_56KR
RT2 need under CPU
R381 10KR1%
RT2 10KRT1%
MICRO-STAR
LPC W83697 I/O
MS-7114
Wednesday, May 18, 2005
Sheet 27 of 36

IEEE-1394

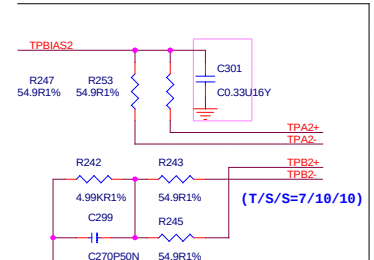


FRONT 1394 PORT 1

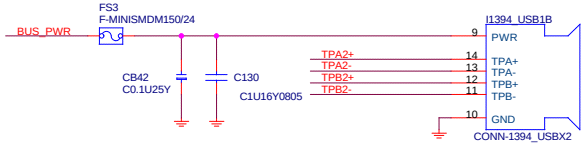




Place close to pin 97
(Less then 500 mils)

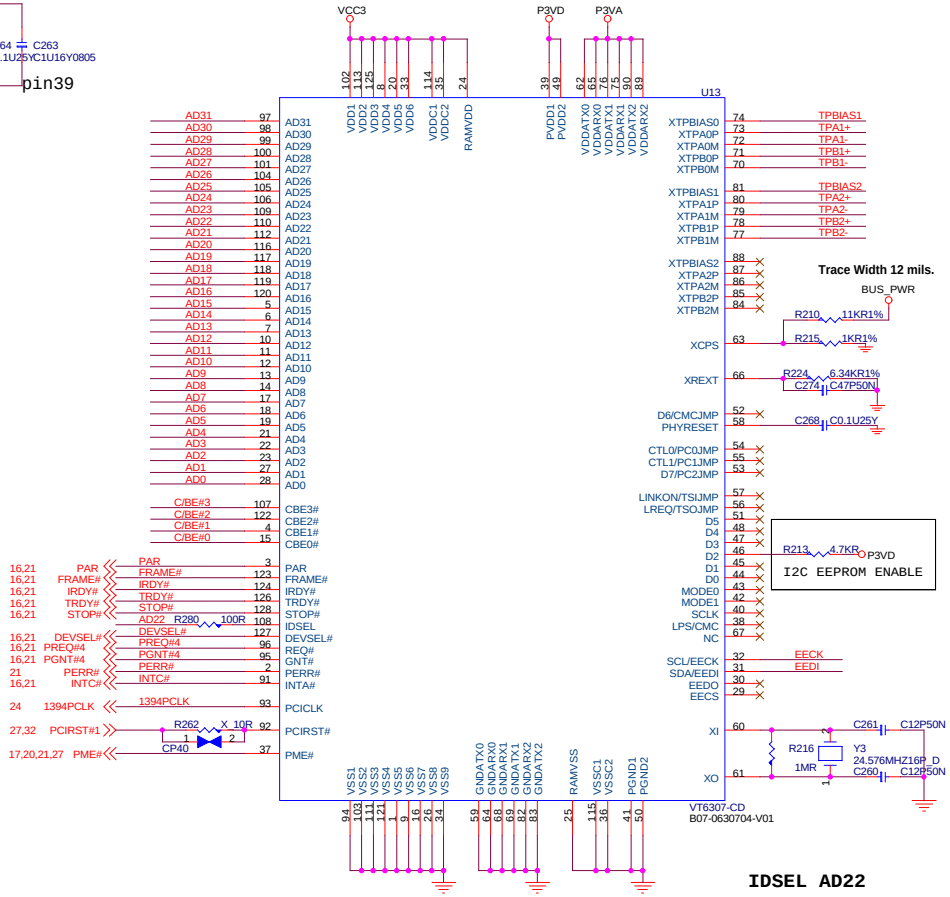


Place close to pin 111
(Less then 500 mils)



N58-14M0011-S85
Change to STARCONN

Trace Width 20 mils.



Trace Width 12 mils.

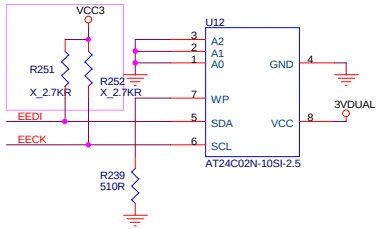
BUS_PWR

Eeprom Select	
4.7K	24C02
Remove	93C46S

IDSEL AD22
MASTER = PREQ#4
INTD#

20040312
JuneWu@vntek.com.tw
suggestion modify

1394-EEPROM 24C02

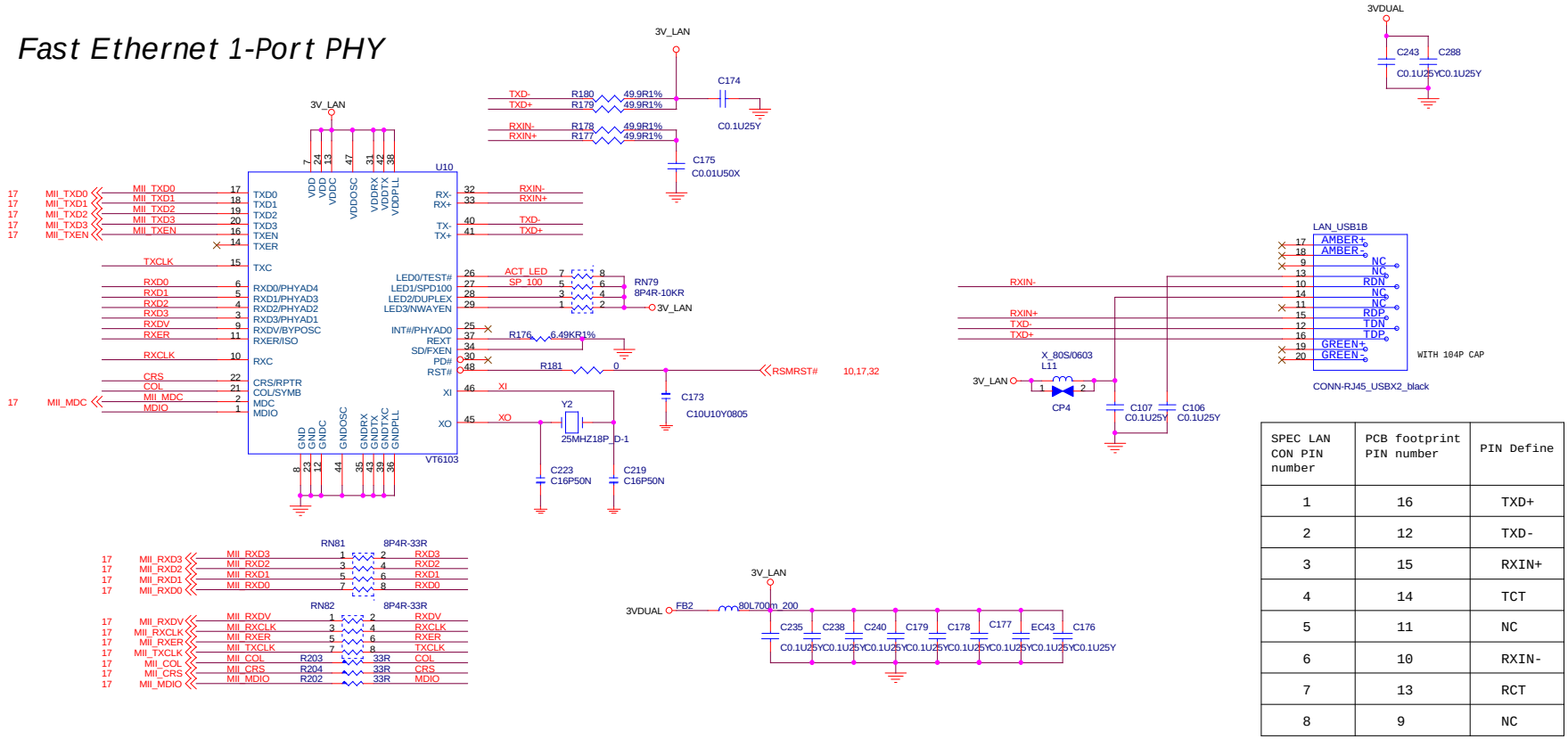


16,21 AD[0..31] AD[0..31]

16,21 C/BE#[3..0] C/BE#[3..0]

MSI	MICRO-STAR	
Title	1394 - VIA VT-6307	
Size	Document Number MS-7114	Rev 2A
Date: Wednesday, May 18, 2005	Sheet 28 of 36	

Fast Ethernet 1-Port PHY



SPEC LAN CON PIN number	PCB footprint PIN number	PIN Define
1	16	TXD+
2	12	TXD-
3	15	RXIN+
4	14	TCT
5	11	NC
6	10	RXIN-
7	13	RCT
8	9	NC

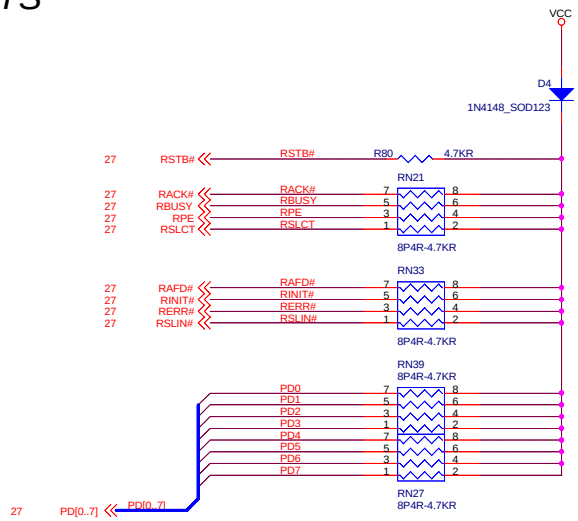
MSI MICRO-STAR

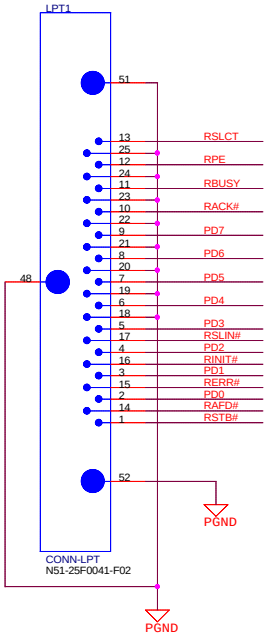
Title: LAN

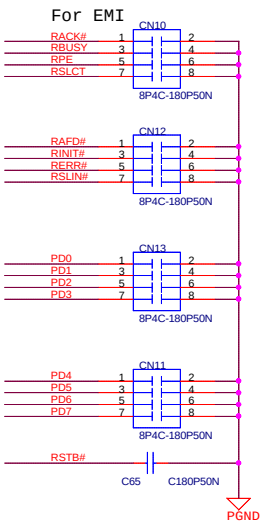
Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 29 of 36

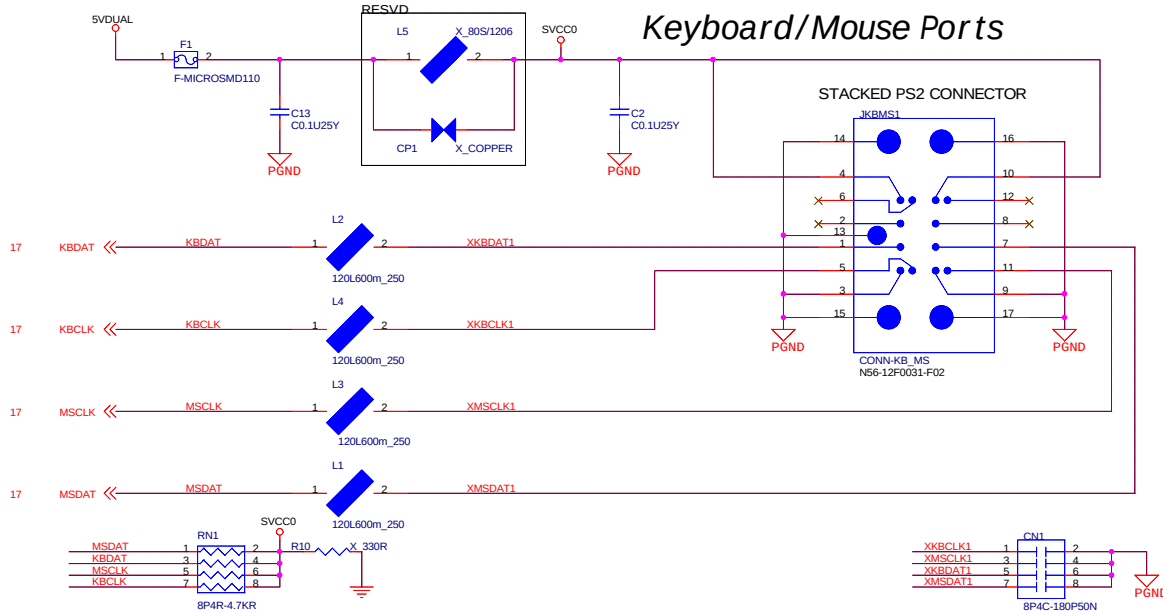
LPT PORTS



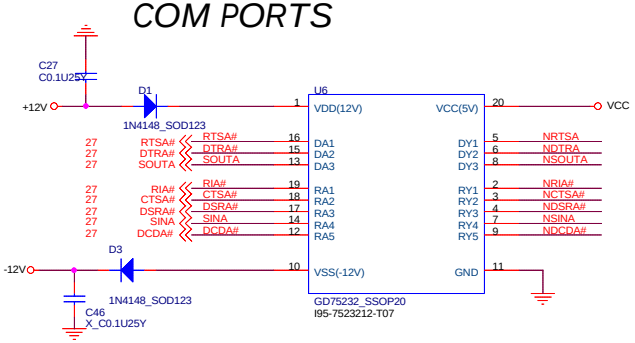




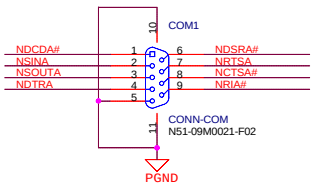
Keyboard/Mouse Ports

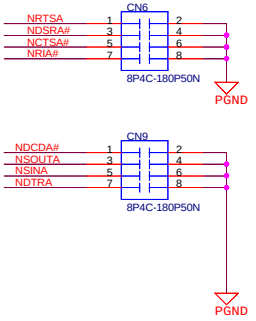


COM PORTS



Multiple RS232 Drivers and Receivers





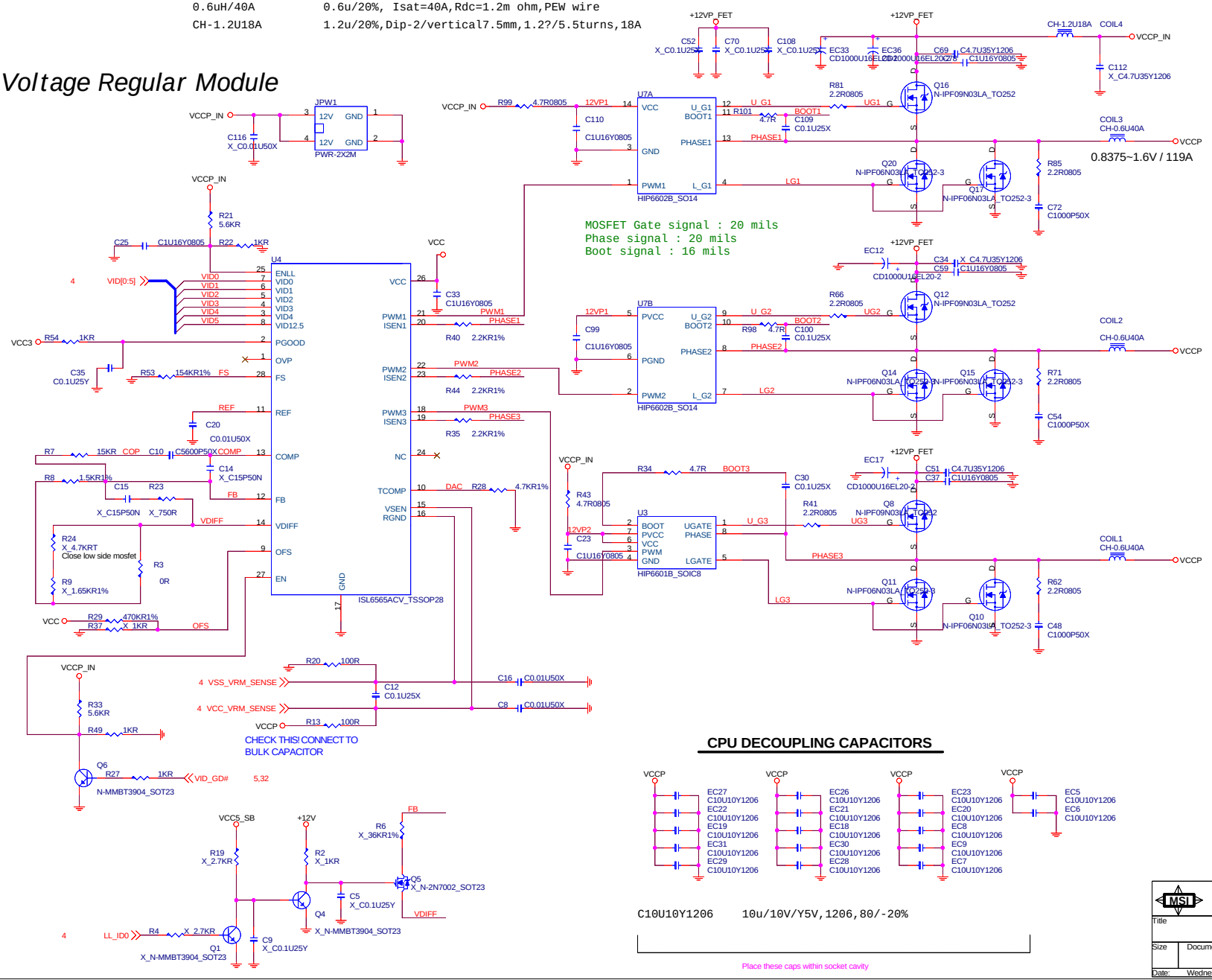
MSI **MICRO-STAR**

Title	LPT/COM PORT	
Size	Document Number MS-7114	Rev 2A
Date: Wednesday, May 18, 2005	Sheet 30 of 36	

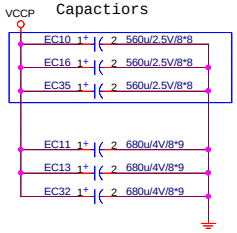
IPF06N03LA	Rds(on)=8.7mO(@4.5V,30A),Vgs(on)=1.2~2V,Id=50A,Ciss=3110pf,Qg=10nC,Vds=25V,Vgs=±20V
C100U2SP	ESR<13mO,Ripple cur.<2.7A,LC<12uA,105C
.CD3300U6.3EL25	ESR<12mO,Ripplecur.<2800mA,105C,longlife3000hrs,KZGSeries
560u_2.5V	ESR=6mO,Ripplecur.=4400mA,Lc.<500uA,105C/2000hrs
1800UF/6.3V	ESR<12mO, Ripplecur<2350mA,105C, longlife change from 2000hrs to 3000hrs ,KZJ series
0.6uH/40A	0.6u/20%, Isat=40A,Rdc=1.2m ohm,PEW wire
CH-1.2U18A	1.2u/20%,Dip-2/vertical7.5mm,1.2?/5.5turns,18A

TDP = 115 W
VR_TDC = 101 A
Icc(max) = 119 A
Tejas Tcase = [P x 0.213] + 43.3
Prescott Tcase = [P x 0.25] + 43.3

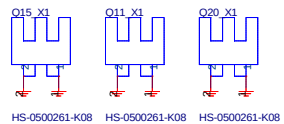
Voltage Regular Module



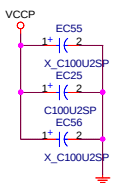
OS-CON Capactiors



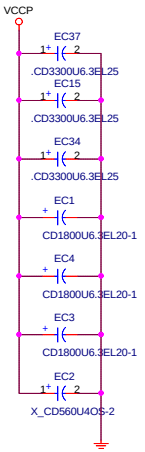
MOSFET Heatsinks



SP Capacitors



EL Capacitors



Solder Side

MSI	MICRO-STAR	
Title	VRM 10.1 - Intersil 6565ACV 3 Phase	
Size	Document Number MS-7114	Rev 2A
Date: Wednesday, May 18, 2005	Sheet 31 of 36	

ACPI Controller

ICH5 300mA
PCI 375+20+20= 415mA
VCC3_SB 715mA

1.7V@250mA

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

Pin48 pull-up 5VSB for DDR2

1.8V STAND BY POWER

3VDUAL, Q43 LT1087S_SOT89, VCC1.8_DUAL, CE1 C10U10Y1206, R211 220R1%, R212 100R1%, C262 X_C10U10Y0805

VCC3, VR2 APL1084UC_TO252, VCC1.8, C275 C4.7U10Y0805, C248 X_C0.1U25Y, R206 220R1%, R205 100R1%, EC46 .CD1000U6.3EL15

5V DUAL Power

C361 C2200P50X, Q48 NN-P07D03LV_SO8, 5V_DRV, C357 X_C1000P50X, Q2 40N03, 5VDUAL, C359 X_C0.1U25Y, C22 X_C0.1U25Y

Low RDS ON MOSFET

DDRTYPE

Pull-up 1.8V
Pull-down 2.6V

R372 1K, 8P4R-1KR RN83

SMBCLK, SMBDATA, FP_RST#, MS7_POK, PWR_OK

U11 MS7-RBC

CHARGE PUMP VOLTAGE OUTPUT 16V

C245 C0.22U16X0805 X7R

C246 C1U16Y0805, C216 C1U16Y0805, C217 C1U16Y0805

EC61 .CD1000U6.3EL15

VCC_VID / VID_GOOD

Place MOSFET near CPU

VID_GD# R199 0R

V_FSB_VTT 1.2V/5A

EC38 .CD1000U6.3EL15

Q21 40N03

R190 3.3R0805, C236 C1U10Y

IVDD

Wide Trace

EC51 .CD1000U6.3EL15

C430 102P, R361 33 RAM_VREF, C431 102P

Close to MS6+

VLR2_DRV, Q22 N-P50N03LS_TO263, VLR2_SEN R118 110R1%, R184 100R1%, Q24 N-P50N03LS_TO263, C123 X_C0.1U25Y

Change MOSFET to TO263

R186 300R1%, CB98 X_C0.1U25Y, R111 49.9R1%, EC40 .CD1000U6.3EL15, C118 X_C0.1U25Y

Q42, C231 C1000P50X, NN-P07D03LV_SO8, EC48 .CD1000U6.3EL15

change CAP 6.3v to 10v

5VDIMM

VR1 APL1084UC_TO252, VDDPEX, C172 C4.7U10Y0805, C160 X_C0.1U25Y, R155 220R1%, EC42 .CD1000U6.3EL15, R154 100R1%

Q50 NN-P2103HV_SO8, X_222P RAM_SBDRV, RAM_DRV, C437 X_104P, EC64 470u/10V/6.3*11.5

DDR VTT Power

1.25V/2.1A

3VDUAL, U2 W83310DS_SOIC8, C444 104P, 1.25V/2.9A

VCC_DDR, remove EC65, R25 1KR1%, C445 104P, R32 1KR1%, remove EC14, VTT_DDR, EC44 .CD1000U6.3EL15

R362 5.1KST, R365 X_33RST, R366 5.1KST, R367 51KST, C439 222P, C440 X_103P, R369 X_0, R370 200, 5VDIMM

C433 X_104P, R364 49.9KST, U20 MS-6+/SOP14, C441 104P, C442 R371 10/0805, CLOSE TO CHIP

5VDIMM, +12V, R363 X_0, C434 X_224P, D22 1N5817S, C435 475P/0805, C436 X_104P, C438 224P, R368 2.55KST

Change 4.7K to 2K

3.3uH/4A/5mm/0.7 CHOKE1, EC62 CD1000u10EL12.5

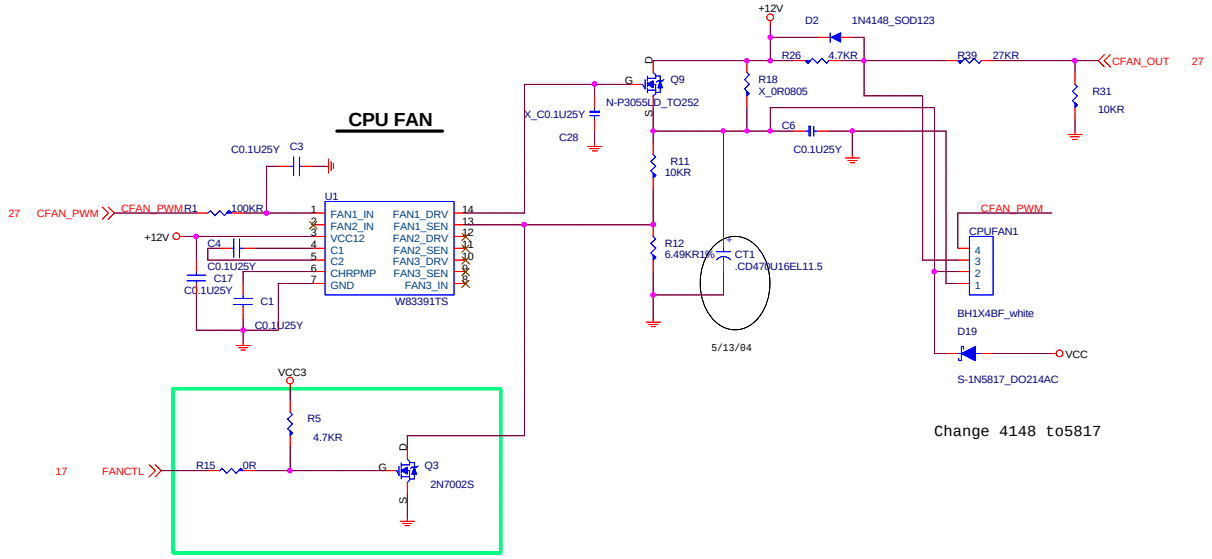
remove EC63 , EC69

Q51 P50N03LD/50A/12m/TO252 CHOKE2, Q52 P50N03LD/50A/12m/TO252, 4.2uH/12A/6mm/1

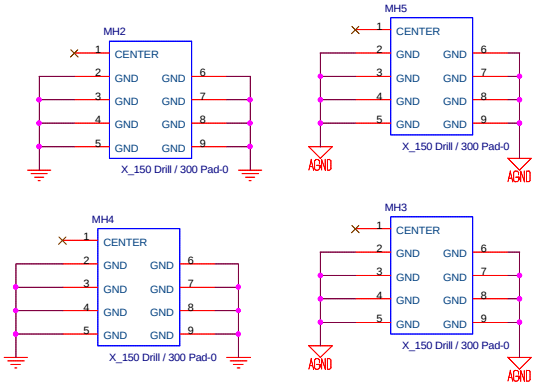
VCC_DDR, EC66 1000u/6.3V/8*11.5, EC67 1000u/6.3V/8*11.5, EC68 1000u/6.3V/8*11.5

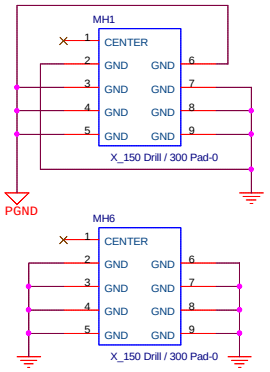
Title	MICRO-STAR
	ACPI Controller MS7
Size	Document Number: MS-7114
Rev	2A
Date:	Wednesday, May 18, 2005
Sheet	32 of 36

ATX VIA-Hole * 9

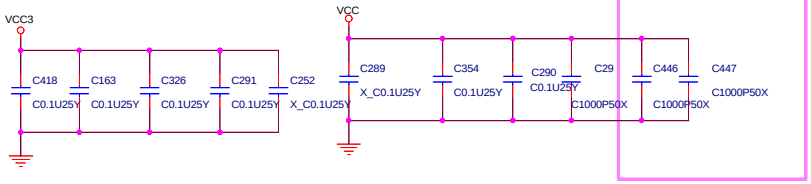


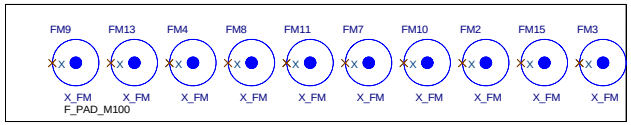
Change 4148 to5817

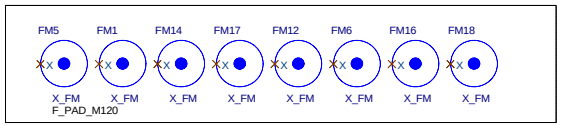


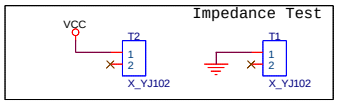


BULK / Decopuling









MSI **MICRO-STAR**

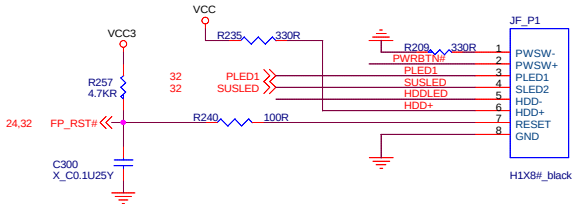
Title: FAN

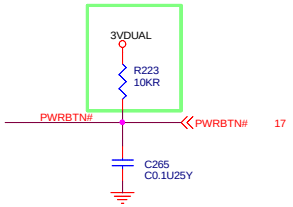
Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 33 of 36

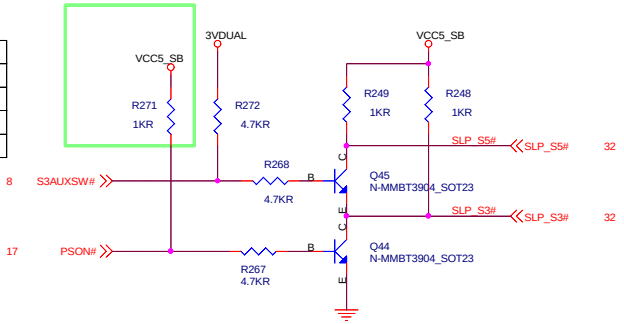
FRONT PANEL

For MSI / Front Panel

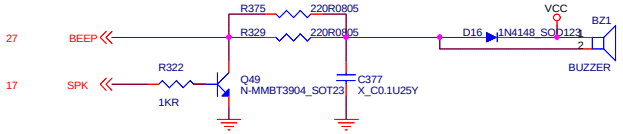




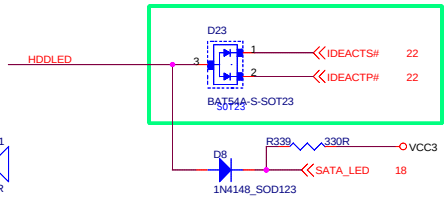
	S0	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S5#	1	1	0
SLP_S3#	1	0	0



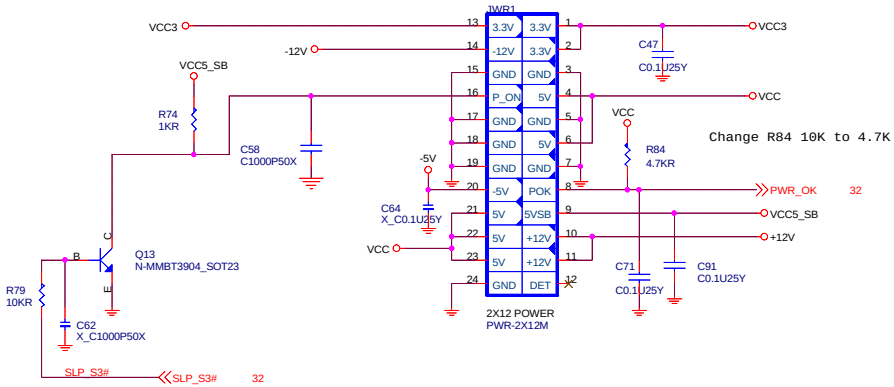
Add 220R 0805



Change 8148*2 to BAT54A



ATX Connector



MSI **MICRO-STAR**

Title: FRONT PANEL

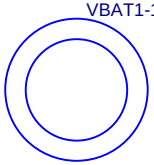
Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 34 of 36

PCB1

P00-071142A-E48

VBAT1-1



BAT-BCR2032P
D06-0100101-P01

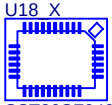
U8_HS

NB-HEATSINK
E31-0401580-E25

U16_HS

X_SB-HEATSINK
E31-0400890-E25

U18_X



SST39SF040-70-4C-NH

MICRO-STAR		
Title: OPTION PARTS		
Size	Document Number: MS-7114	Rev: 2A
Date: Wednesday, May 18, 2005	Sheet 35 of 36	

MS-7114 *SCHEMATIC HISTORY*

Rev	Date	Page		Description
0B	2004		?	Transfer from OEM3
1.00	2005/02/05	-19-	?	Add bypass CAP 1u under SB solder side
		-18-	?	Remove SIS964 OC#4 C419
		-24-	?	Clock generator VCC3 add bead and CT2
			?	Remove BSEL0,1 level shift circuit
		-25-	?	Add a bead between VCC_DDR and CBVDD
		-27-	?	Reserver FDD signal pull-up RN85
			?	Firmware U18 power add C427 , C428
		-33-	?	Change Q22 , Q24 , Q50 , Q51 type to T0263
			?	Change MS7 ver:RAC to RBC and remove patch circuit
			?	Change VTT_DDR reference R25 , R32 to 1K
		-4-	?	Remove R50 , R51 direct short
		-7-	?	Change R174 to 680R , R175 to 150R
		-8-	?	Add a bypass CAP C411 0.1u with DDRVREF
		-10-	?	Remove VGA part
		-15-	?	DDR terminator CAP all in
		-16-	?	Add R344 33R for PCIRST# and remove ZSTB pull-up
		-25-	?	Remove RN2 , RN3 , RN4 , RN5 , RN7 , RN8
		-26-	?	Add D20 , D21 for Audio 5VSB
			?	Change EC58 , EC59 to 100u
			?	Add CN15 , CN16 , R342 , R296 , R232 , R346
		-32-	?	Change C110 and C23 to 1u
			?	Change R8 to 1.5K
			?	Add EC10 , EC16 , EC35 to 560u
			?	Add EC11 , EC13 , EC32 to 680u
		-7-	?	SIS suggest Change R109 to 10R1% , R113 to 120R1% , R90 to 261R1% R110 to 49.9R1% , R92 to 100R1% , C310 to 10p , C319 to 10p , add C117 , C119 to 103p
		-27-	?	Remove -5V circuit R246 , R250
		-24-	?	Change C154 , C147 to 22p

Rev	Date	Page	Description
2.00	2005/03/09		change DDR to DDR2 change CLK buffer to ICS9P952
	2005/03/23		change DDR2 slot 1/3 PN
2A	2005/05/08		change Hvref voltage with R72 R75 R92 R110
			Add MS6+ VDD 5VDIMM voltage

MSI **MICRO-STAR**

Title: HISTORY

Size | Document Number: MS-7114 | Rev: 2A

Date: Wednesday, May 18, 2005 | Sheet 36 of 36