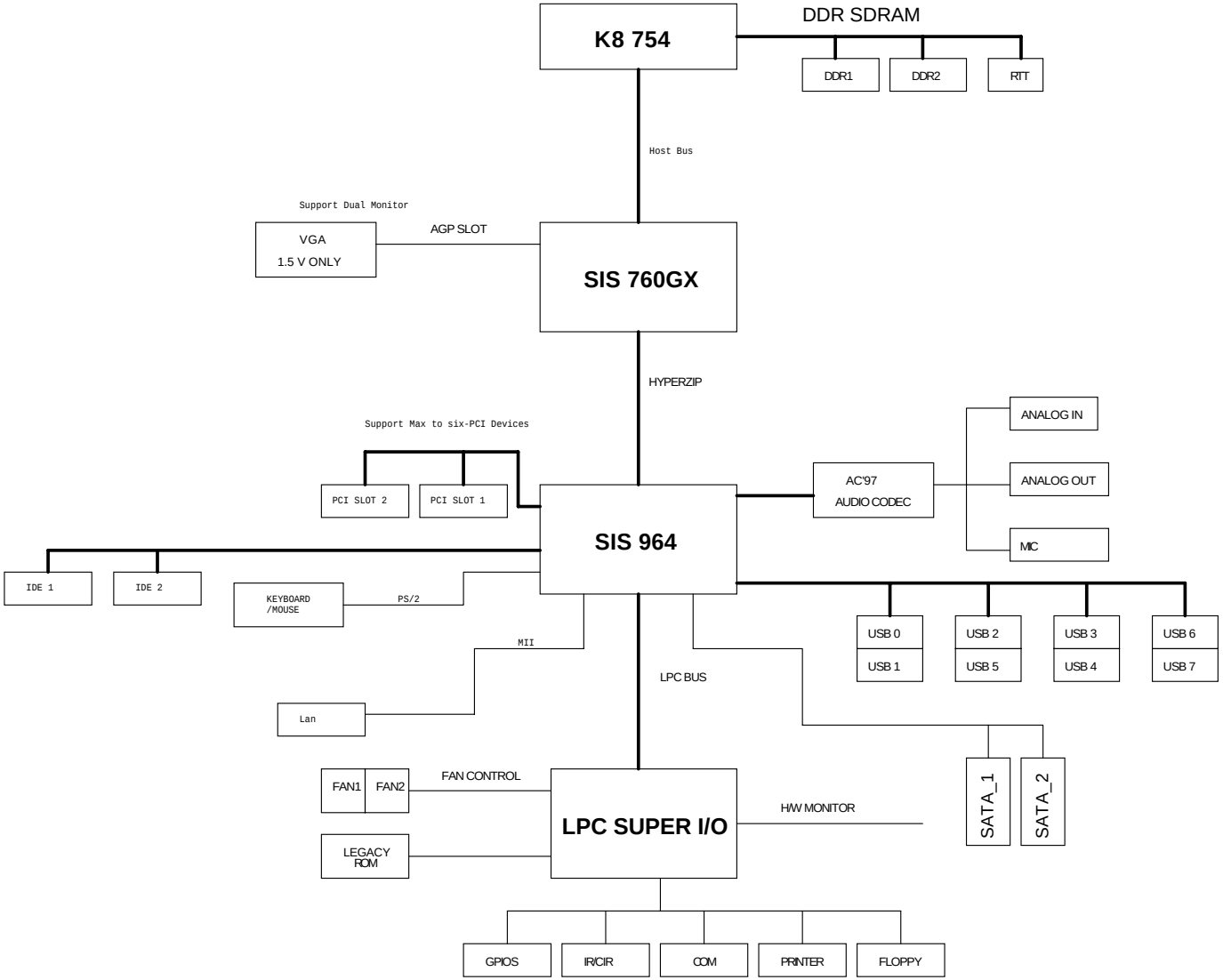
MS-7112

* *AMD K8 Socket754*
* *SIS 760GX + 964*
* *REALTEK RTL8201CL LAN*
* *Winbond 83687THF I/O*
* *USB 2.0 support x8*
* *ALC 655 AC97 CODEC*

ERP BOM	Function Description	

Micro-Star	Title: MS-7112	Rev: 0A
Document Number: Cover Sheet		
Last Revision Date: Monday, August 23, 2004	Sheet 1 of 31	

System Block Diagram



GPIO Table on SIS964

GPIO_0	I/O	MAIN	NC
GPIO_1	I/O	MAIN	CPU fan initial speed control reserved
GPIO_2	I/O	MAIN	THERM#
GPIO_3	I/O	MAIN	GPIO3, pull-down reserved
GPIO_4	I/O	MAIN	GPIO4, pull-down reserved
GPIO_5	I/O	MAIN	NC
GPIO_6	I/O	MAIN	NC
GPI_7	I/O	RESUME	NC
GPI_8	I/O	RESUME	RING
GPI_9	I/O	RESUME	NC
GPI_10	I/O	RESUME	NC
GPIO_11	I/O	RESUME	NC
GPIO_12	I/O	RESUME	NC
GPIO_13	I/O	RESUME	NC
GPIO_14	I/O	RESUME	S3AUXSW#
GPIO_15	I/O	RESUME	KBDAT
GPIO_16	O	RESUME	KBCLK
GPIO_17	O	RESUME	MSDAT
GPIO_18	O	RESUME	MSCLK
GPIO_19	OD	MAIN	SMBCLK
GPIO_20	OD	MAIN	SMBDAT
GPIO_21	I	RESUME	EESK
GPIO_22	I	RESUME	EEDI
GPIO_23	I	RESUME	DDEO
GPIO_24	I	RESUME	EECS

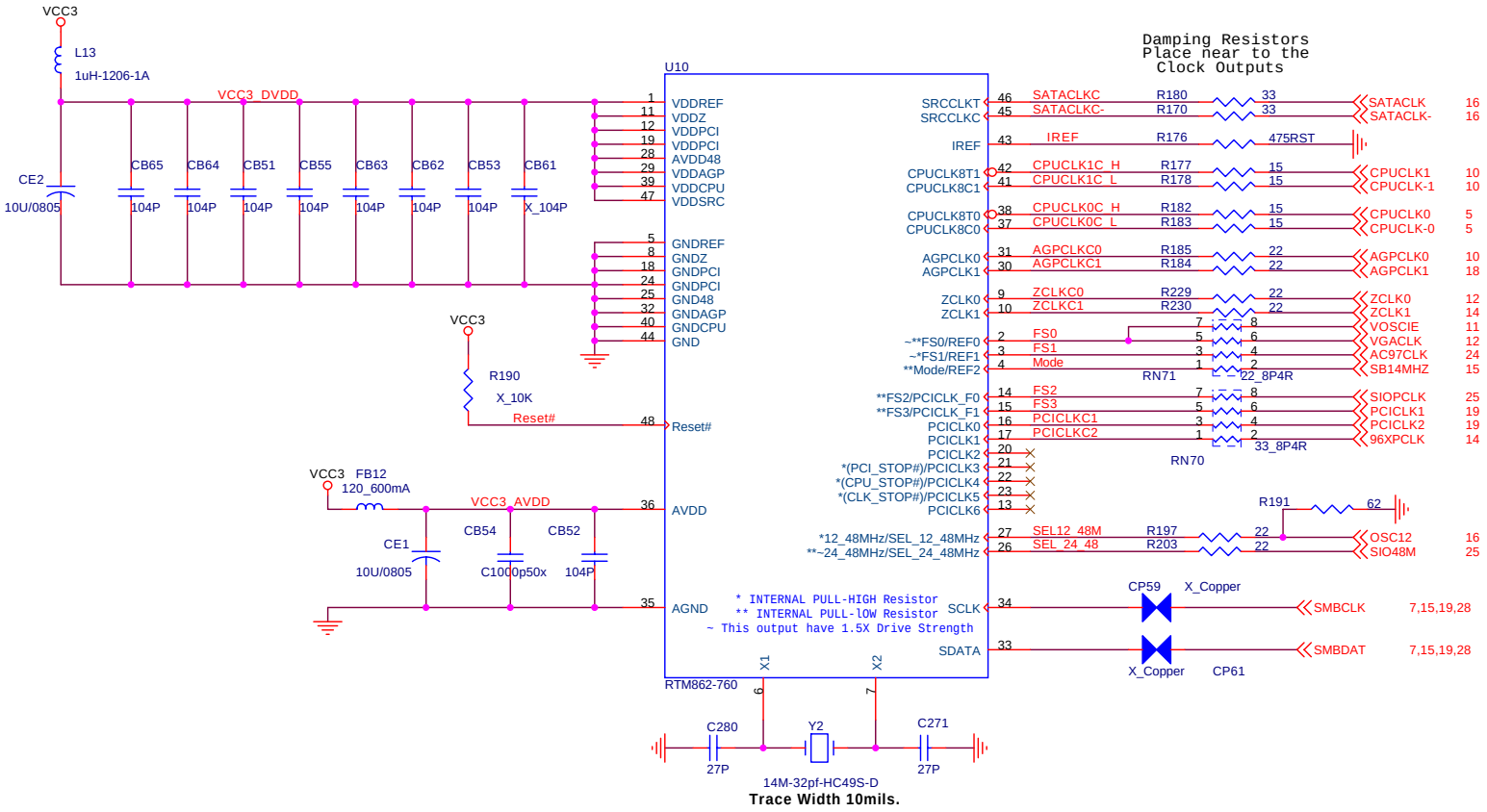
PCI Config.

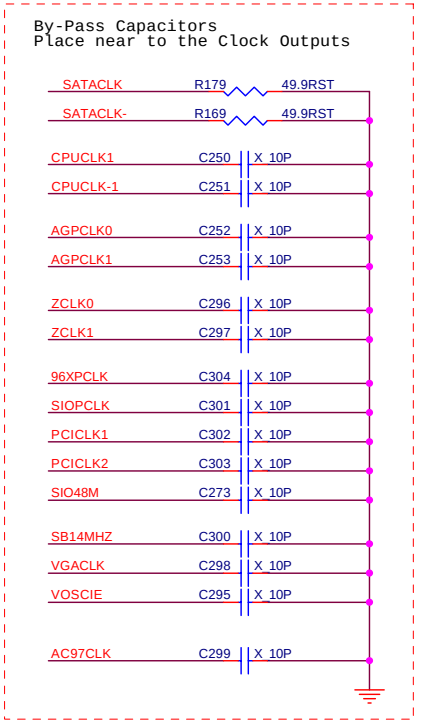
DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PCI_REQ#0 PCI_GNT#0	AD17	PCICLK1
PCI Slot 2	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PCI_REQ#1 PCI_GNT#1	AD18	PCICLK2

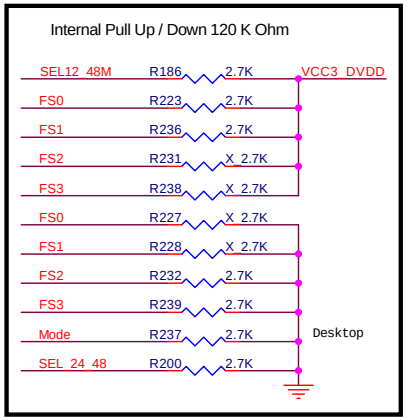
PCI RESET DEVICE

Signals	Target
PCIRST#1	Northbridge,S/IO
PCIRST#2	PCI1~2
PCIRST_964	AGP
HDDRST#	Primary, Scondary IDE

Micro-Star	Title: MS-7112	Rev: 0A
Document Number: System Block Diagram		
Last Revision Date: Monday, August 23, 2004	Sheet 2 of 31	







CLK Table for SiS760 (Different clock generator with different frequency defin table)

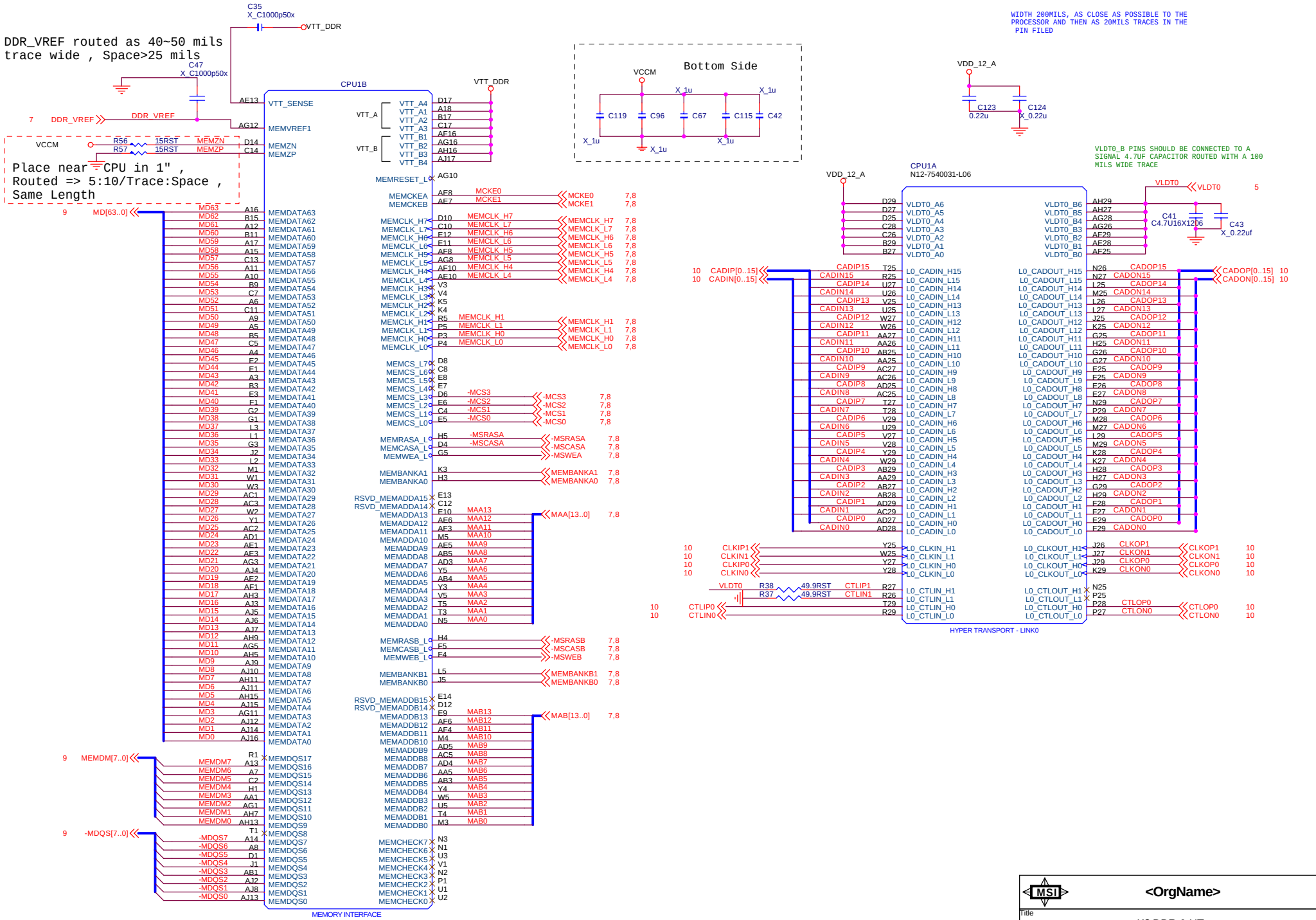
SiS 760 CLOCK

Bit 4	Bit 3 (FS3)	Bit 2 (FS2)	Bit 1 (FS1)	Bit 0 (FS0)	VCO (MHz)	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
0	0	0	0	0	800.00	100.00	100.00	133.33	66.67	33.33
0	0	0	0	1	807.92	100.99	100.99	134.65	67.33	33.66
0	0	0	1	0	800.00	200.00	100.00	133.33	66.67	33.33
0	0	0	1	1	807.92	201.98	100.99	134.65	67.33	33.66
0	0	1	0	0	799.98	133.33	100.00	133.33	66.67	33.33
0	0	1	0	1	803.94	133.99	100.49	133.99	67.00	33.50
0	0	1	1	0	699.99	233.33	100.00	140.00	70.00	35.00
0	0	1	1	1	707.22	235.74	101.03	141.44	70.72	35.36
0	1	0	0	0	799.98	160.00	100.00	133.33	66.67	33.33
0	1	0	0	1	833.30	166.66	104.16	134.11	69.44	34.72
0	1	0	1	0	799.98	266.66	100.00	133.33	66.67	33.33
0	1	0	1	1	807.90	269.30	100.99	134.65	67.33	33.66
0	1	1	0	0	800	200	100.00	133.33	66.67	33.33
0	1	1	0	1	807.92	201.98	100.99	134.65	67.33	33.66
0	1	1	1	0	999.96	166.66	100.00	125.00	66.66	33.33
0	1	1	1	1	999.96	166.66	100.00	142.85	66.66	33.33

SiS 760 CLOCK

Bit 4	Bit 3 (FS3)	Bit 2 (FS2)	Bit 1 (FS1)	Bit 0 (FS0)	VCO (MHz)	CPU (MHz)	SRC (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
1	0	0	0	0	824.00	103.00	103.00	137.33	68.67	34.33
1	0	0	0	1	840.00	105.00	105.00	140.00	70.00	35.00
1	0	0	1	0	824.00	206.00	103.00	137.33	68.67	34.33
1	0	0	1	1	840.00	210.00	105.00	140.00	70.00	35.00
1	0	1	0	0	823.98	137.33	103.00	137.33	68.66	34.33
1	0	1	0	1	839.98	140.00	105.00	140.00	70.00	35.00
1	0	1	1	0	720.99	240.33	103.00	144.20	72.10	36.05
1	0	1	1	1	734.99	245.00	105.00	147.00	73.50	36.75
1	1	0	0	0	823.98	164.80	103.00	137.33	68.66	34.33
1	1	0	0	1	839.98	168.00	105.00	140.00	70.00	35.00
1	1	0	1	0	823.98	274.66	103.00	137.33	68.66	34.33
1	1	0	1	1	839.98	279.99	105.00	140.00	70.00	35.00
1	1	1	0	0	824.00	206.00	103.00	137.33	68.67	34.33
1	1	1	0	1	840.00	210.00	105.00	140.00	70.00	35.00
1	1	1	1	0	1029.96	171.66	103.00	128.74	68.66	34.33
1	1	1	1	1	1049.96	174.99	105.00	131.24	70.00	35.00

Micro-Star	Title: MS-7112	Rev: 0A
Document Number: MAIN CLOCK GEN		
Last Revision Date: Monday, August 23, 2004	Sheet 3 of 31	

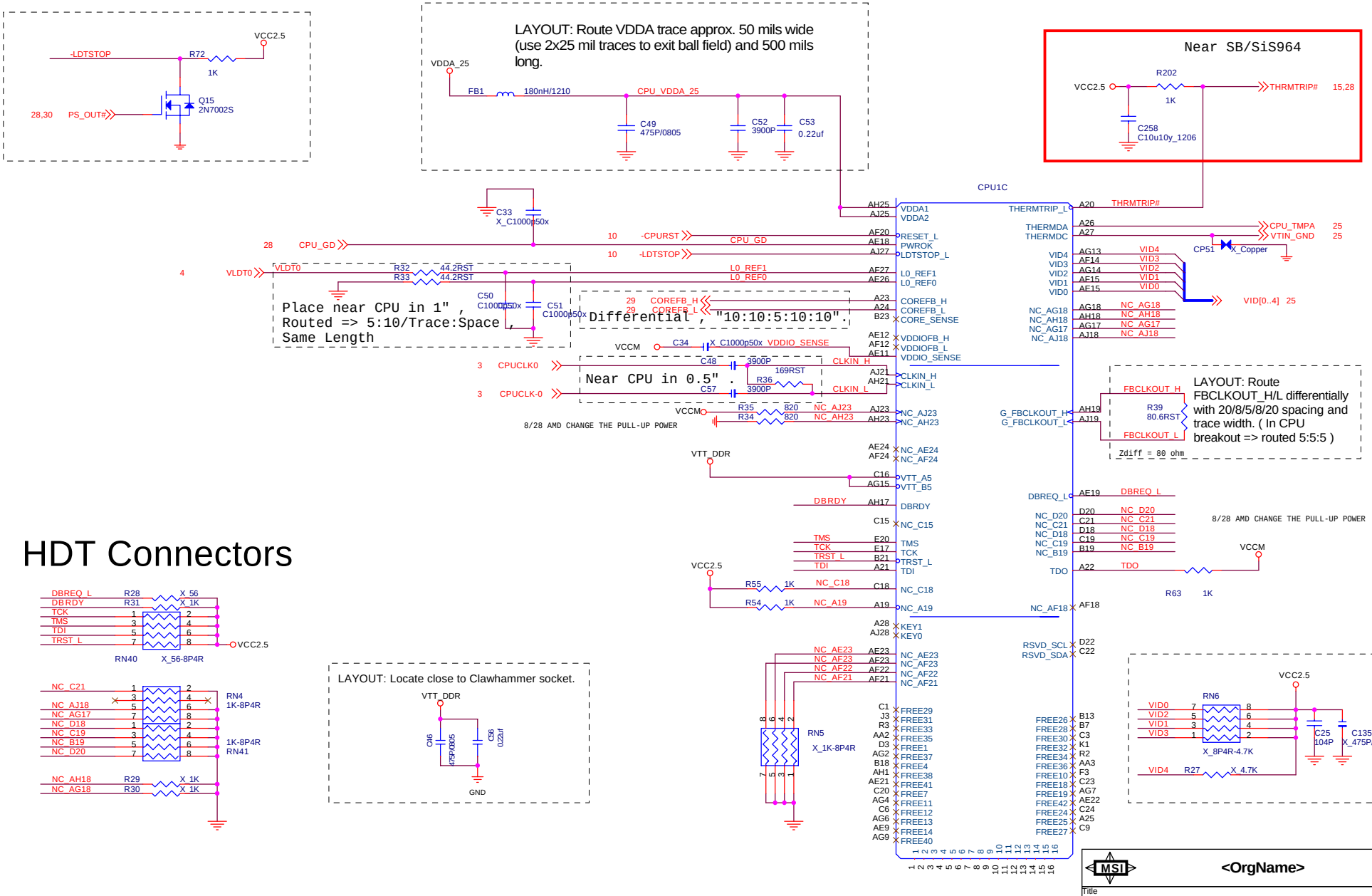

DDR_VREF routed as 40~50 mils
trace wide , Space>25 mils
Place near CPU in 1" ,
Routed => 5:10/Trace:Space ,
Same Length
Bottom Side
WIDTH 200MILS, AS CLOSE AS POSSIBLE TO THE PROCESSOR AND THEN AS 20MILS TRACES IN THE PIN FILED
VLDT0_B PINS SHOULD BE CONNECTED TO A SIGNAL 4.7UF CAPACITOR ROUTED WITH A 100 MILS WIDE TRACE
CPU1B
CPU1A
N12-7540031-L06
MEMORY INTERFACE
HYPER TRANSPORT - LINK0
<OrgName>
K8 DDR & HT
MS-7112
Monday, August 23, 2004

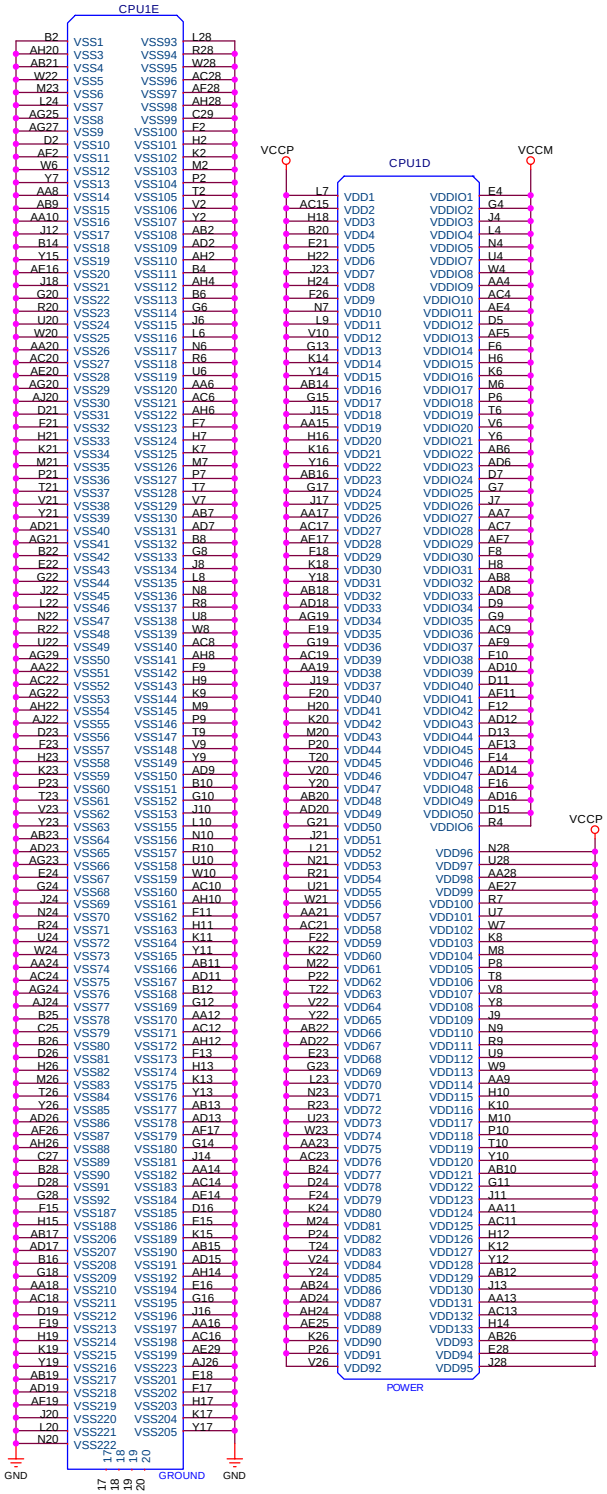
VCCA_PLL trace length from the VR1 to the PGA must be 0.75".

Place al filters close to the PGA.

Keep all power and signal trce away from the VR1.

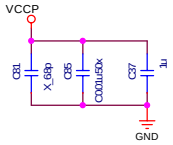
Place a cut in the GND plane around the VCCA_PLL regulator circuit.



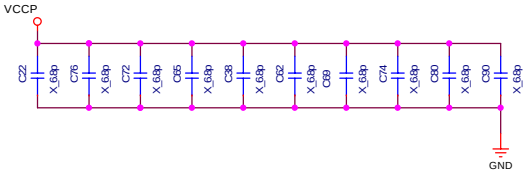


EMI

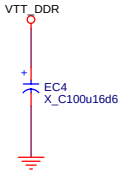
LAYOUT: Place 1 capacitor every 1-1.5" along VDD_CORE perimiter.



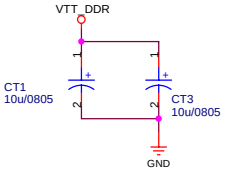
LAYOUT: Place 6 EMI caps along bottom right side of Clawhammer, 2 in middle of HT link, and 12 along bottom left side of Clawhammer.

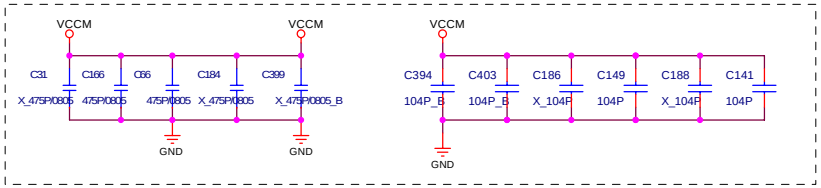


LAYOUT: Locate close to Clawhammer socket.

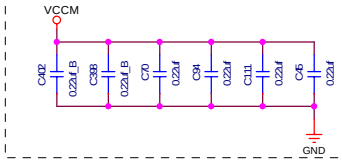


LAYOUT: Place one 1210 10uF capacitor on each end of the VTT island.



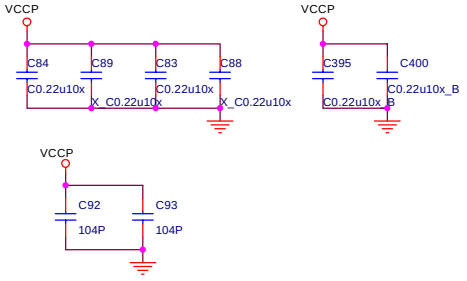


LAYOUT: Place beside processor.



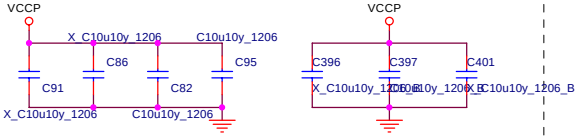
CPU

Place on inside of CPU Cavity (5 * 0.22uF/0603 X7R high-freq decoupling Cap.)



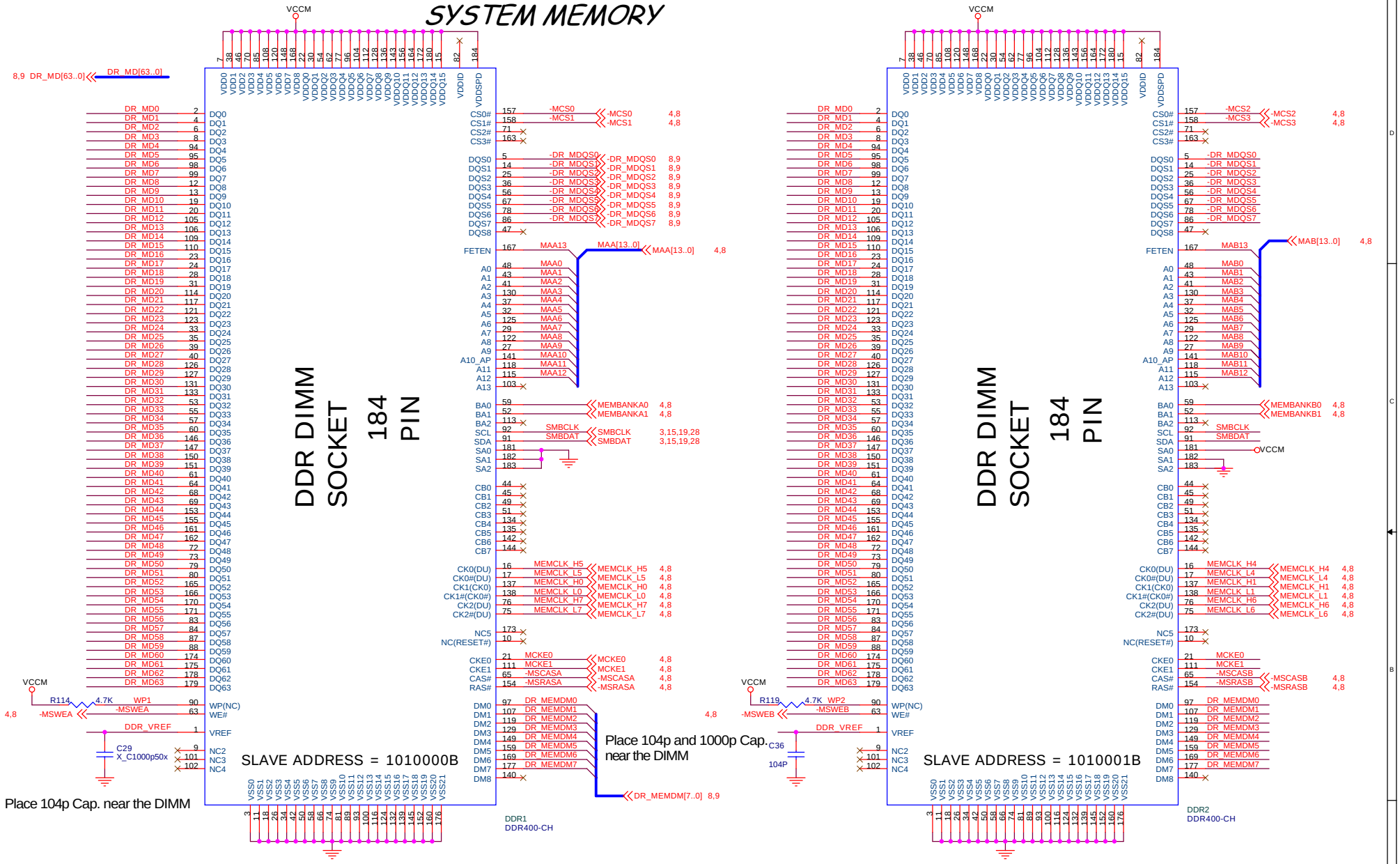
LAYOUT: Place 1000pF capacitors between VRM & CPU

RECOMMEND 4 PLACEDIN TOP SOCKET CAVITY
AND 2 ON THE BOTTOM DIRECTLY UNDER SOCKET CAVITY



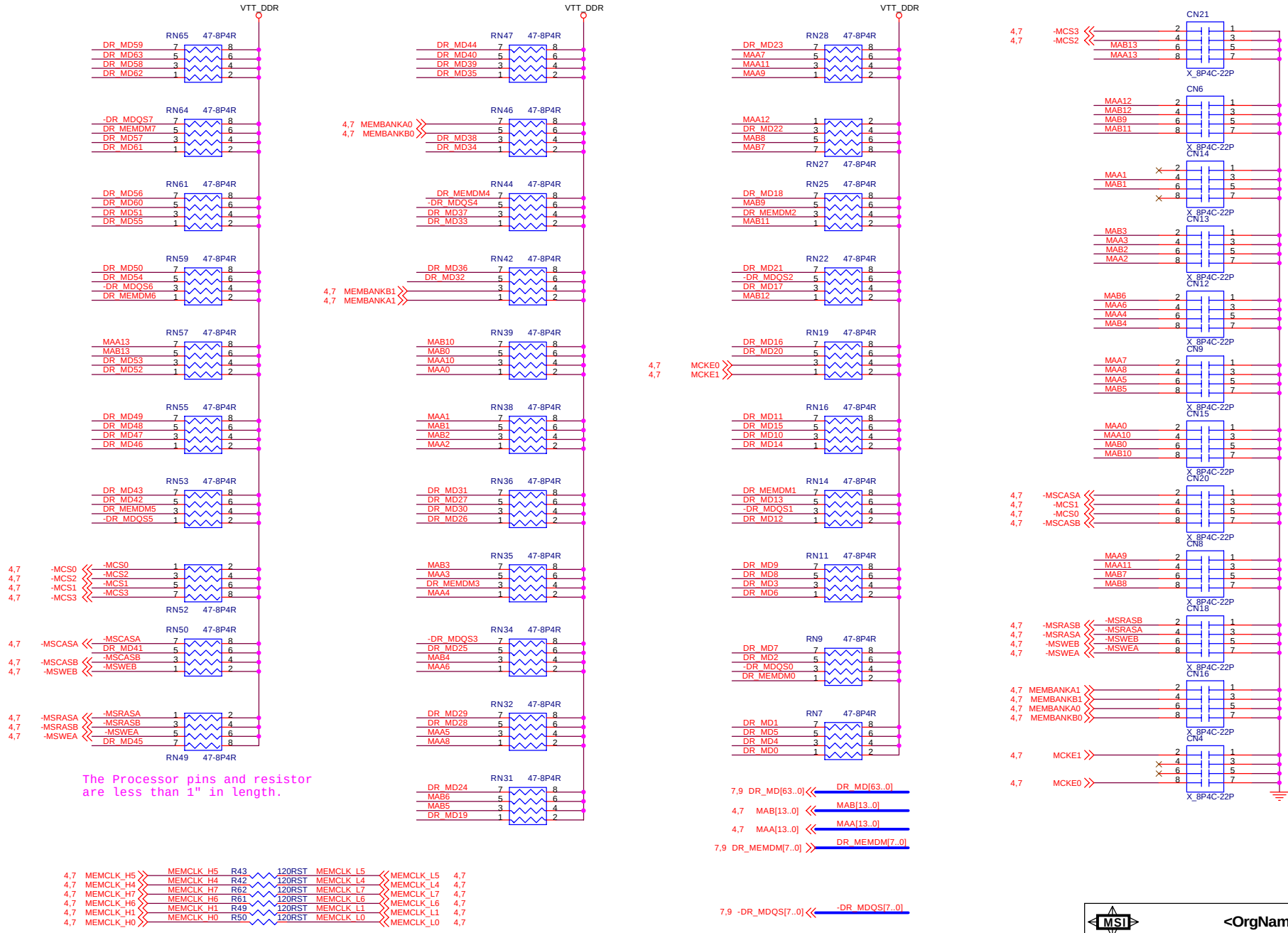
<OrgName>			
Title	K8 POWER & GND		
Size	Document Number MS-7112		Rev 0A
Date: Monday, August 23, 2004	Sheet 6 of 31		

SYSTEM MEMORY



MSI	<OrgName>	
Title	DDR DIMM1, 2	
Size	Document Number MS-7112	Rev 0A
Date: Monday, August 23, 2004	Sheet 7 of 31	

DDR Terminations

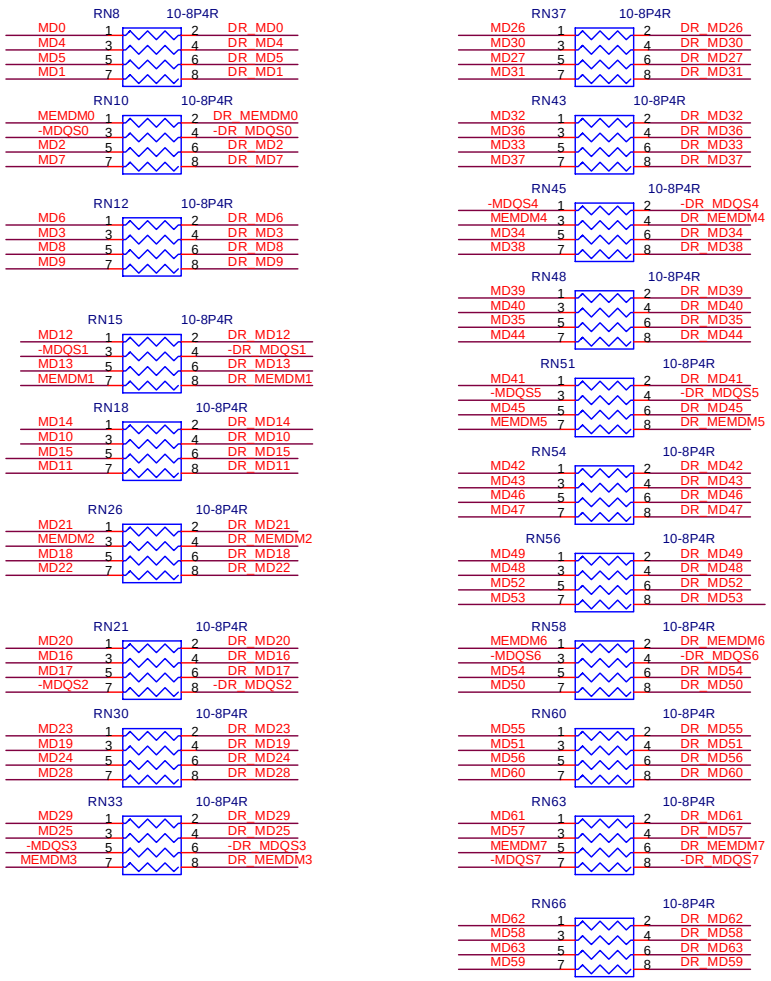


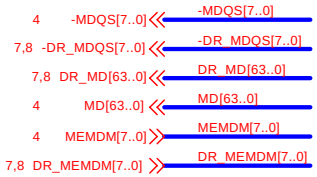
The Processor pins and resistor are less than 1" in length.

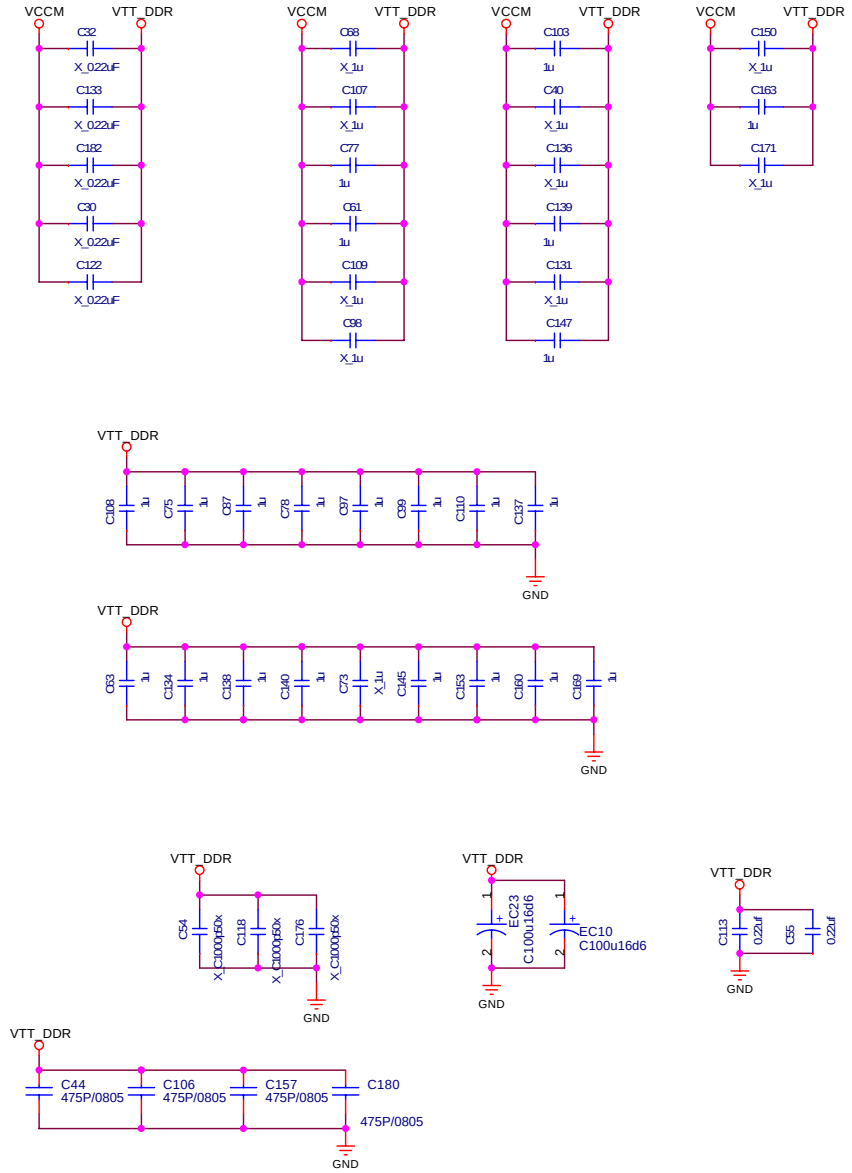
<MSI> <OrgName>

Title	DDR Terminations Part 1	
Size	Document Number MS-7112	Rev 0A
Date: Monday, August 23, 2004	Sheet 8 of 31	

DDR Terminations

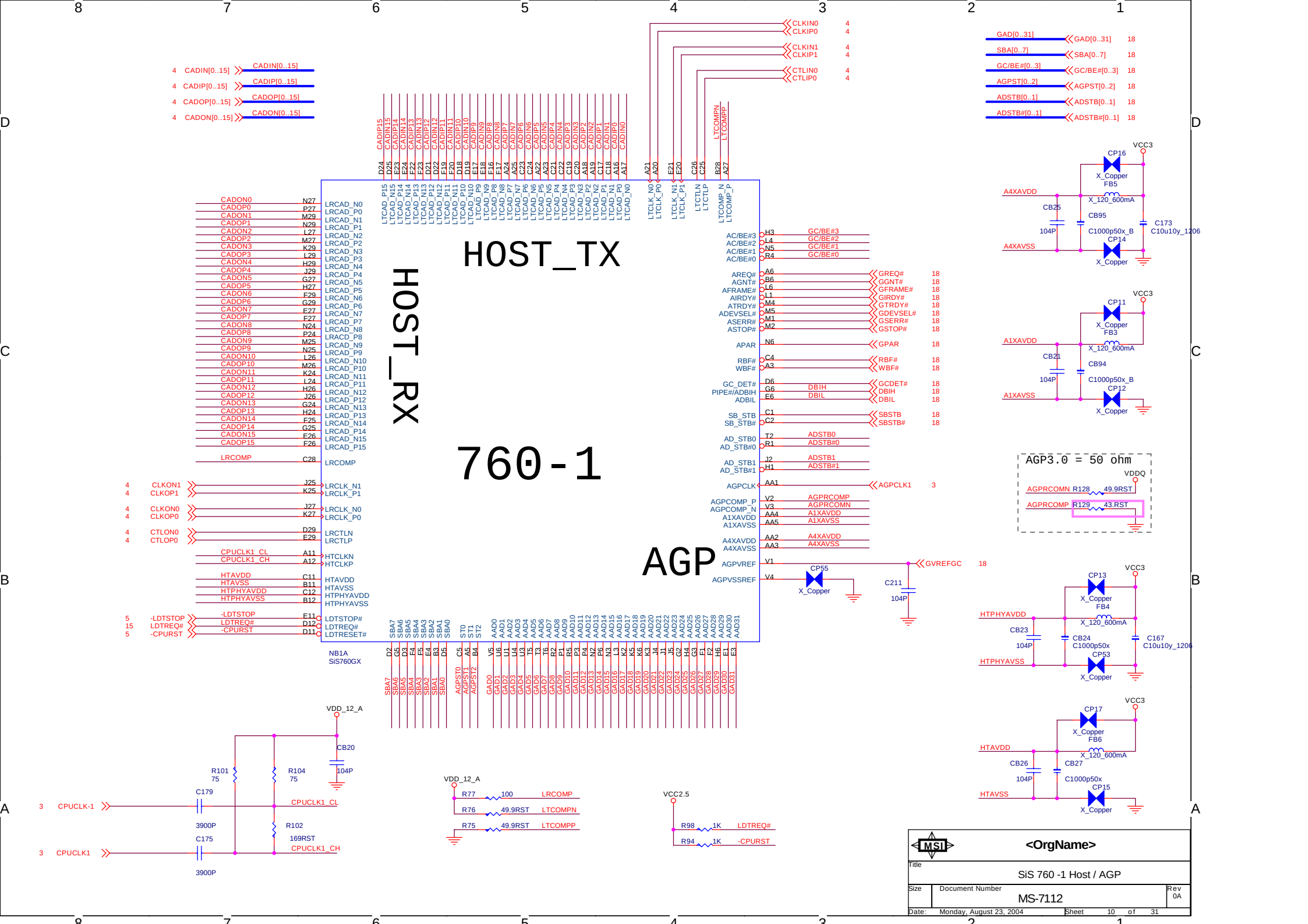






LAYOUT: Add 100pF and 1000pF on VTT fill near Clawhammer and near DIMMs (both sides).

<OrgName>		
Title	DDR Terminations Part 2	
Size	Document Number MS-7112	Rev 0A
Date: Monday, August 23, 2004	Sheet 9 of 31	


HOST_TX
HOST_RX
760-1
AGP
NB1A
SiS760GX
AGP3.0 = 50 ohm
<OrgName>
SiS 760 -1 Host / AGP
MS-7112
Rev 0A
Monday, August 23, 2004
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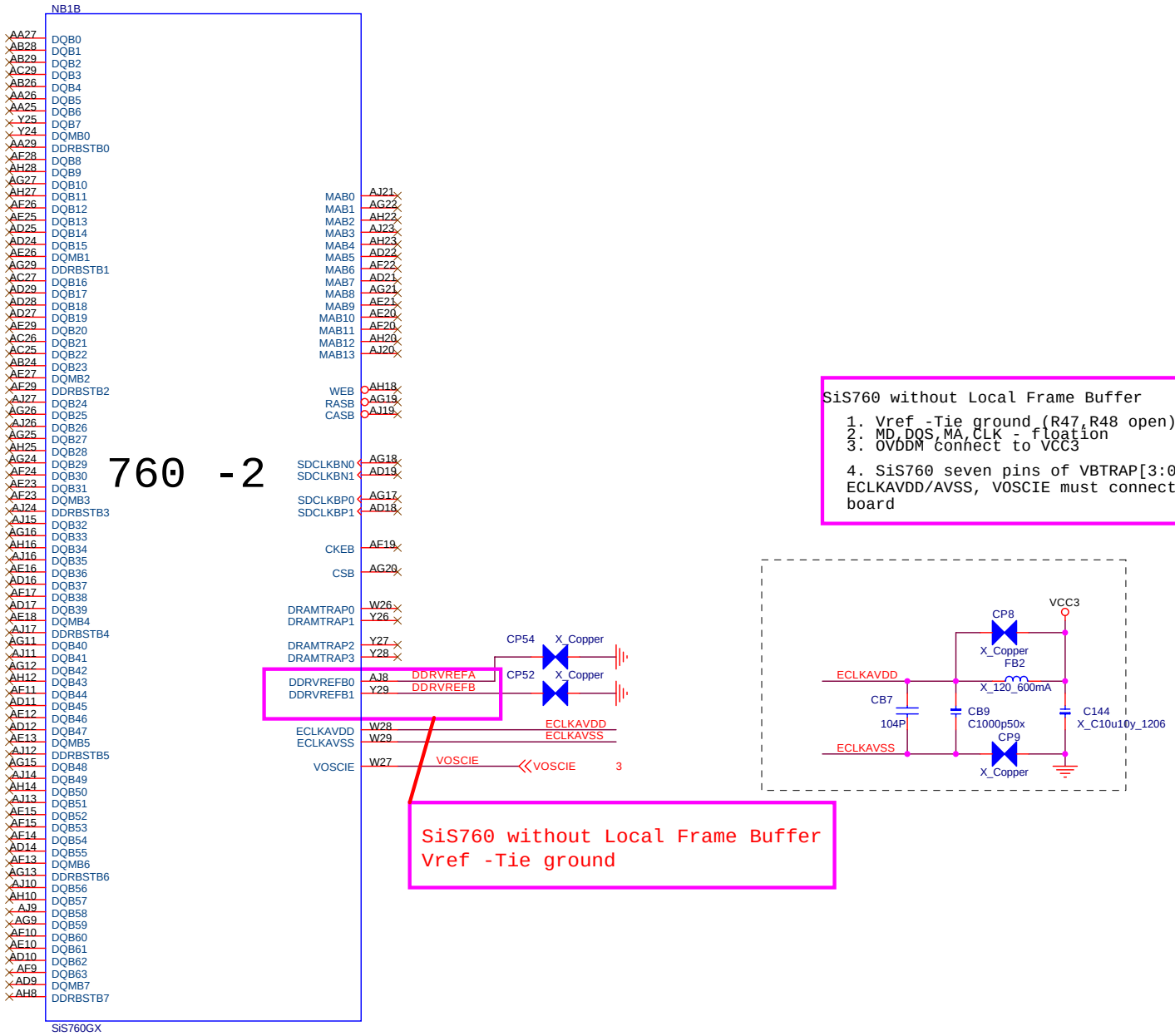


MSI	<OrgName>	
Title	SiS 760-2 Frame Buffer	
Size	Document Number: MS-7112	Rev: 0A
Date: Monday, August 23, 2004	Sheet 11 of 31	

		Enable	Disable
RSYNC	VGA	1	0
LSYNC	panel link	1	0
CSYNC	VB	1	0

The differences between the traces of MuTIOL Strobes and Data in each group should be smaller than 0.05",and strobes need guide GND trace

The differences between the traces of MuTIOL Strobes and Data should be smaller than 0.05"

760-3

MuTIOL

VGA (For 760 Only)

Control & Hardware Trap

SiS760GX

NB solder side

Place near 760 chip.

<OrgName>	
Title	SiS 760-3 MuTIOL/Other
Size	Document Number: MS-7112
Rev	0A
Date:	Monday, August 23, 2004
Sheet	12 of 31

Ref SiS AP103 Page 78
If only support SiS 760 , VDDQ = IVDD = 1.5V

OVDDM connect to VCC3 when use
SiS760 without Local Frame Buffer.

760-4
Power

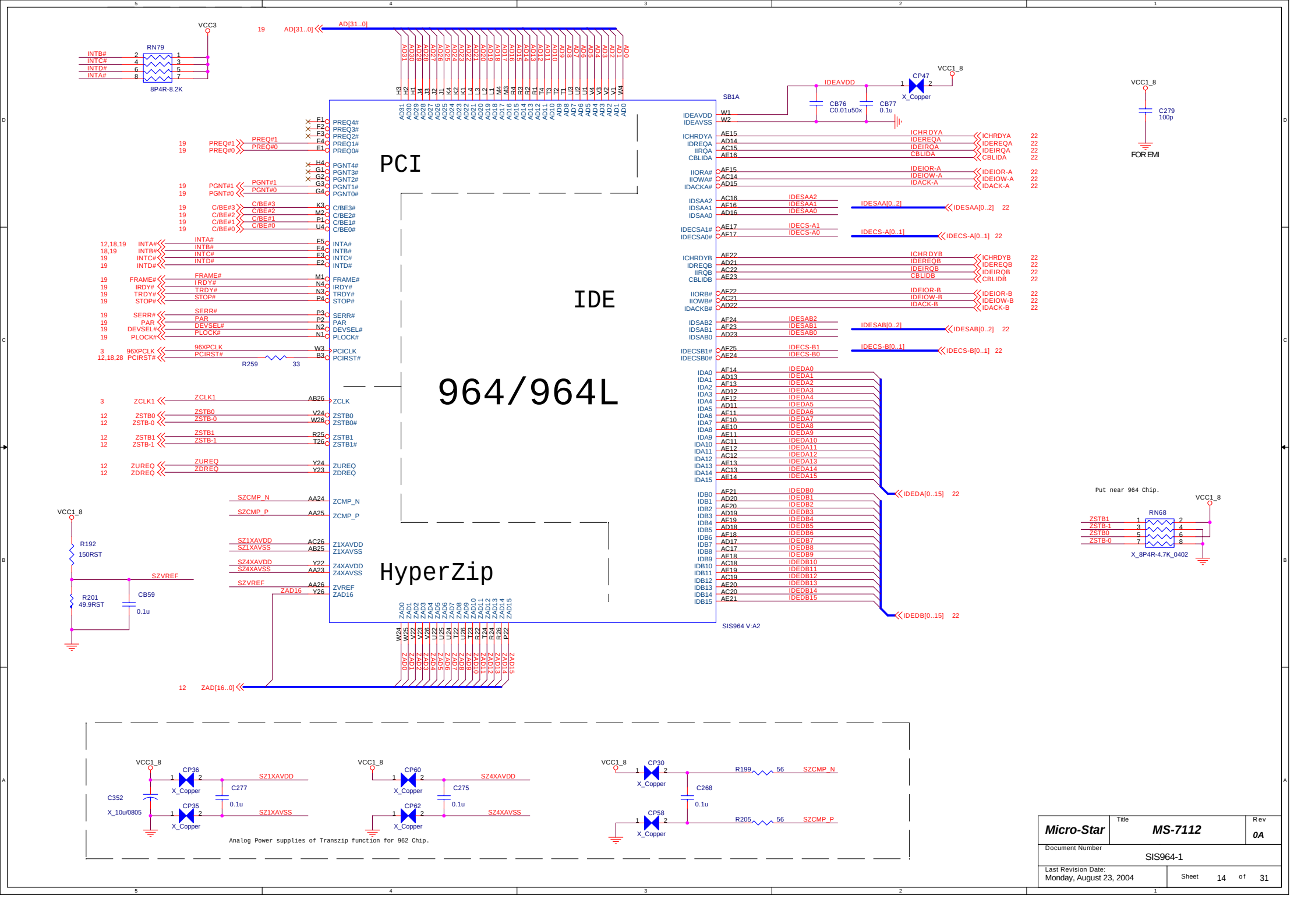
760-5
Power

LAYOUT: Place HT bypass caps on topside newr connected lokar HT link.

C142	X_4.7u_0805	
CB6	X_0.022u	
CB8	0.022u	
C114	4.7u_0805	
CB4	1500P	
CB19	104p	
CB83	C0.01u50x_B	
CB80	104P_B	
CB82	C0.01u50x_B	
CB89	104P_B	
CB79	X_C0.01u50x_B	
C212	C10u10y_1206	
CB43	104P	
CB44	104P	
CB50	C0.01u50x	
CB45	C0.01u50x	
C404	C10u10y_1206_B	
CB86	104P_B	
CB92	104P_B	
CB93	C0.01u50x_B	
CB88	C0.01u50x_B	
C178	1u	
C204	1u	
CB90	104P_B	
CB91	X_104P_B	
CB16	104P	
CB17	C0.01u50x	
CB81	104P_B	
CB85	104P_B	
CB84	C0.01u50x_B	
CB87	C0.01u50x_B	

Solder side

<OrgName>			
Title: SiS 760-4 Power			
Size	Document Number: MS-7112		Rev 0A
Date: Monday, August 23, 2004	Sheet 13 of 31		


PCI
IDE
964/964L
HyperZip
SIS964 V:A2
RN79
8P4R-8.2K
R259
33
R192
150RST
R201
49.9RST
CB59
0.1u
CP47
X_Copper
CB76
C0.01u50x
CB77
0.1u
C279
100p
FOR EMI
RN68
X_8P4R-4.7K_0402
Put near 964 Chip.
CP36
CP35
CP60
CP62
CP30
CP58
C352
X_10u/0805
C277
C275
C268
R199
R205
56
Analog Power supplies of Transzip function for 962 Chip.
Micro-Star
MS-7112
0A
SIS964-1
Monday, August 23, 2004
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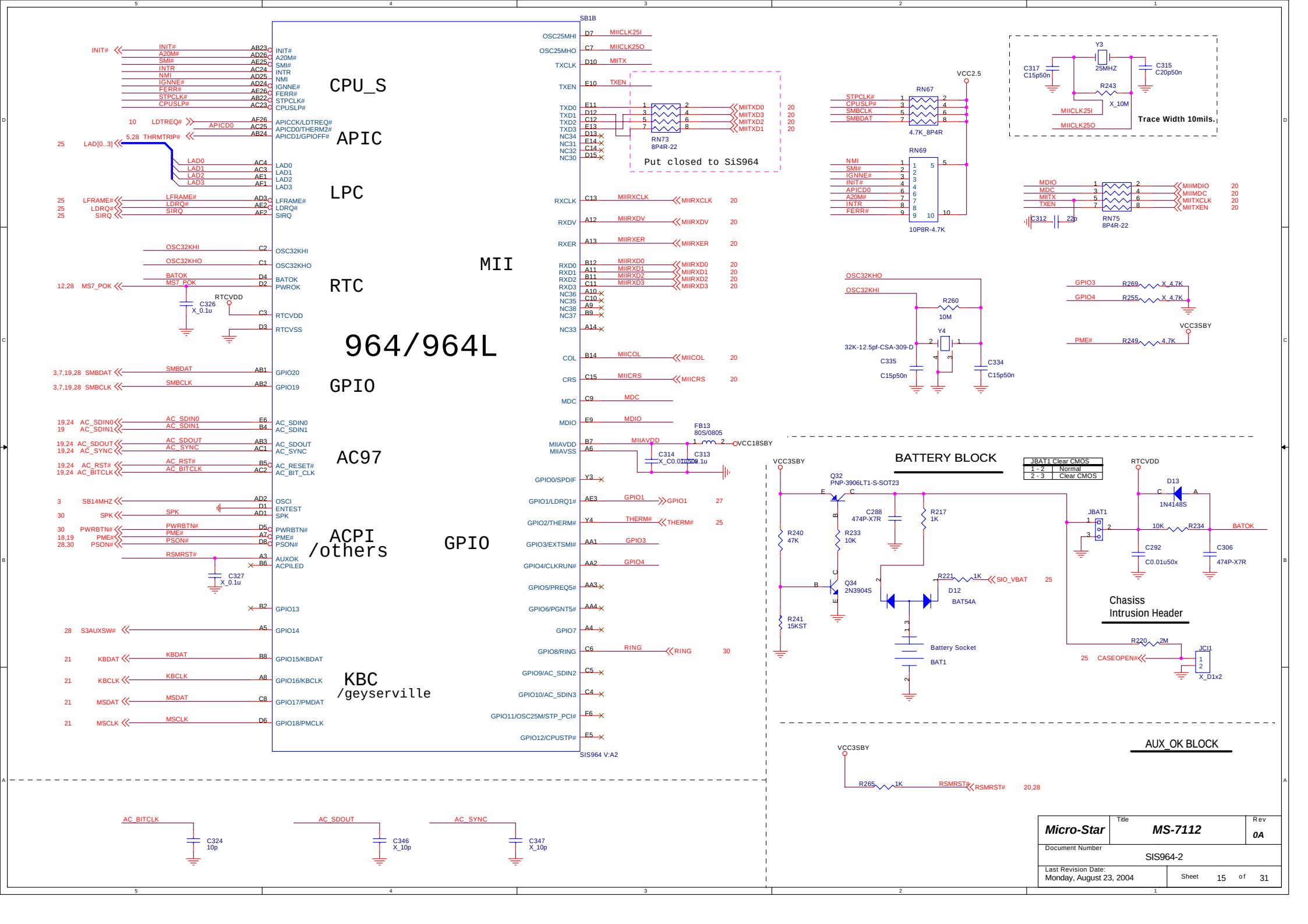
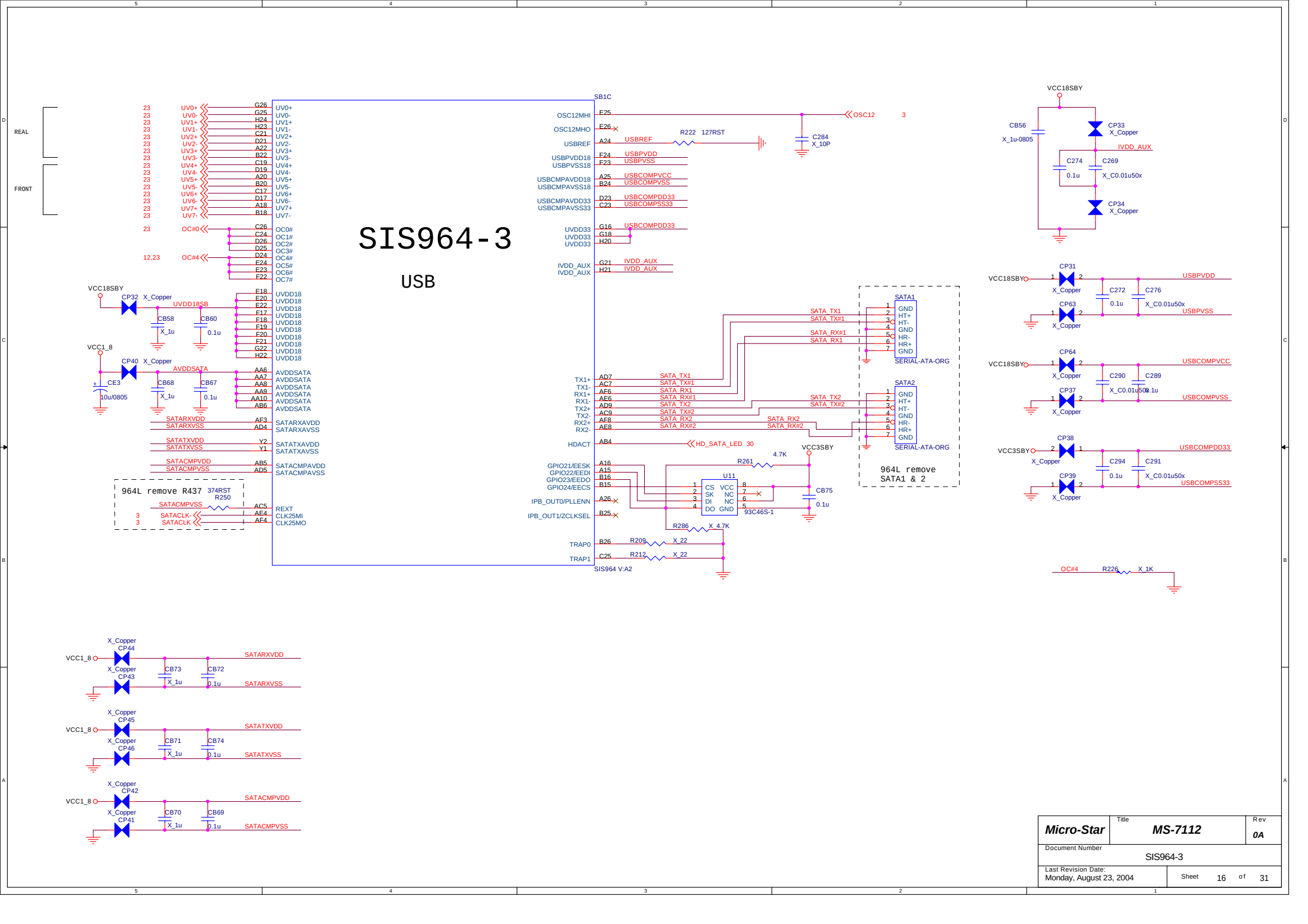
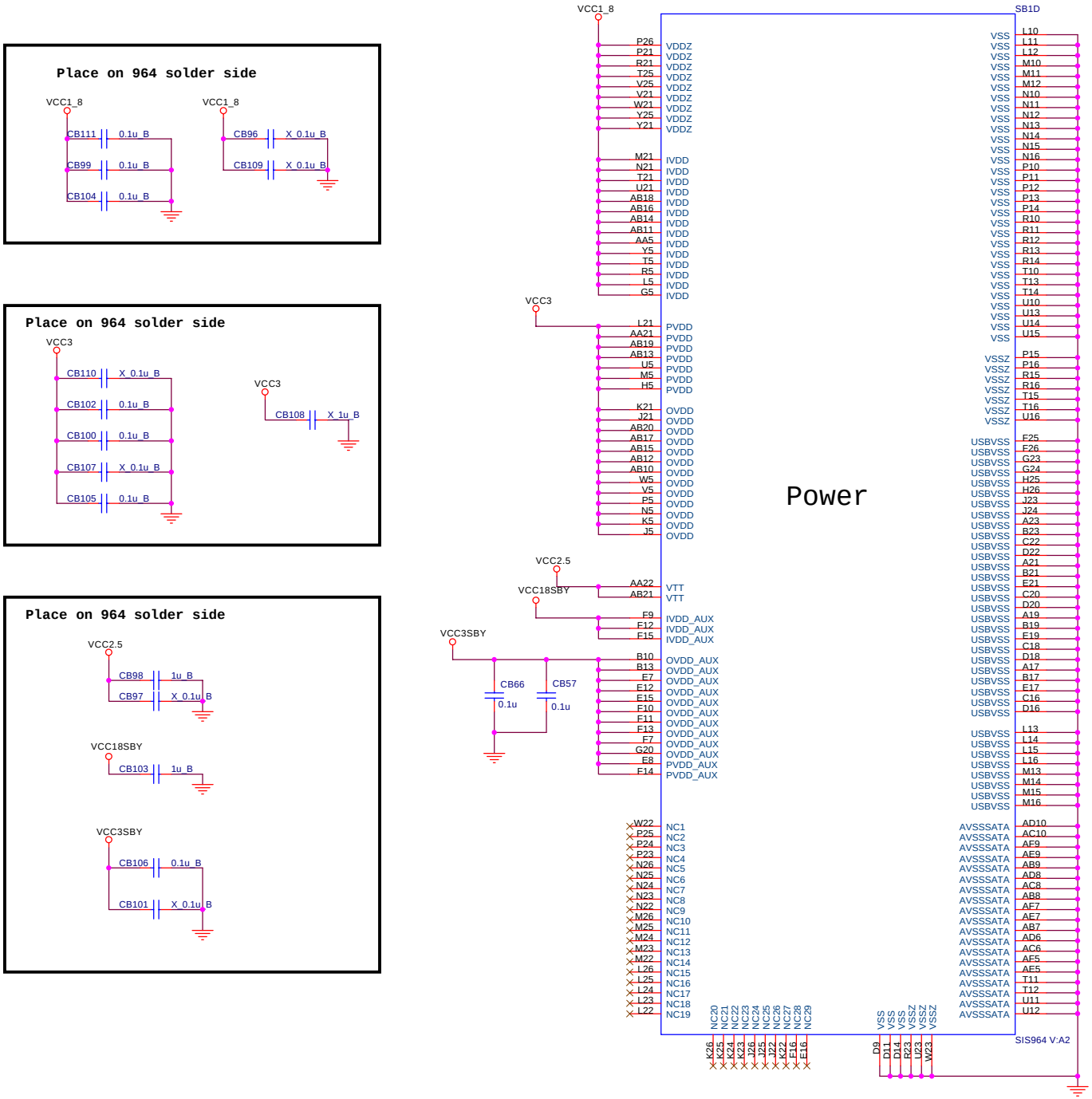
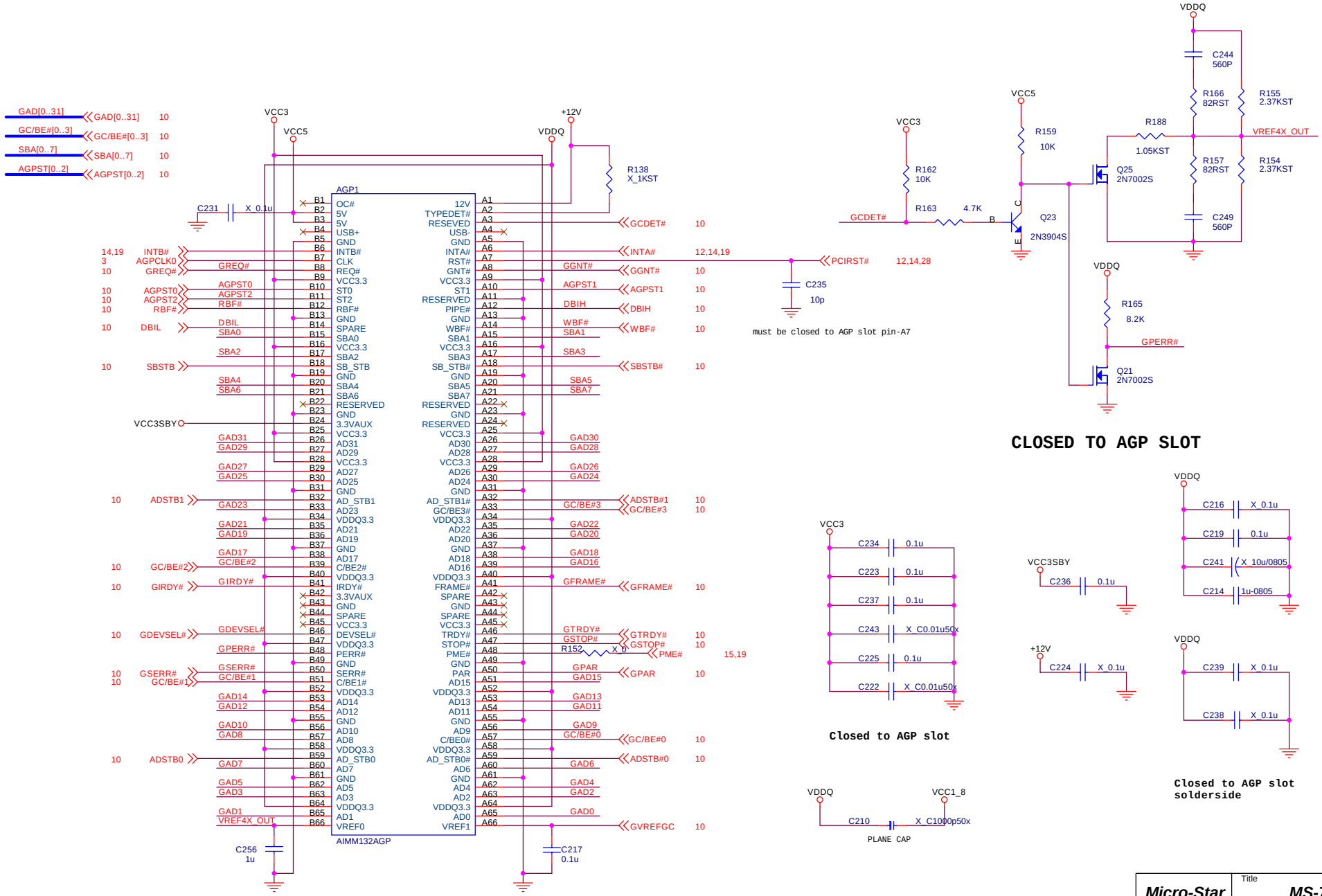

CPU_S
APIC
LPC
RTC
964/964L
GPIO
AC97
ACPI
/others
GPIO
KBC
/geyserville
MII
SB1B
SIS964 V:A2
Put closed to SiS964
Trace Width 10mils.
BATTERY BLOCK
AUX_OK BLOCK
Chasiss
Intrusion Header
Micro-Star
MS-7112
0A
SIS964-2
Monday, August 23, 2004
Sheet 15 of 31


SIS964-3
USB
SB1C
REAL
FRONT
964L remove R437
374RST
R250
964L remove
SATA1 & 2
SERIAL-ATA-ORG
93C46S-1
SIS964 V:A2
Micro-Star
MS-7112
0A
Document Number
SIS964-3
Last Revision Date:
Monday, August 23, 2004
Sheet 16 of 31



Micro-Star	Title: MS-7112	Rev: 0A
Document Number: SIS964-4		
Last Revision Date: Monday, August 23, 2004	Sheet 17 of 31	



Micro-Star	Title: MS-7112	Rev: 0A
Document Number: AGP Slot & Pull up/dn resistor		
Last Revision Date: Monday, August 23, 2004	Sheet 18 of 31	

PCI1:AD17
INTB#

PCI1:AD18
INTC#

CNR RISER

PCI BUS PULL-UP

PCI-D120-WH-SN

PCI-D120-WH-SN

CNR

8P4R-2.7K

X_8P4R-4.7K

10P8R-2.7K

RESERVED

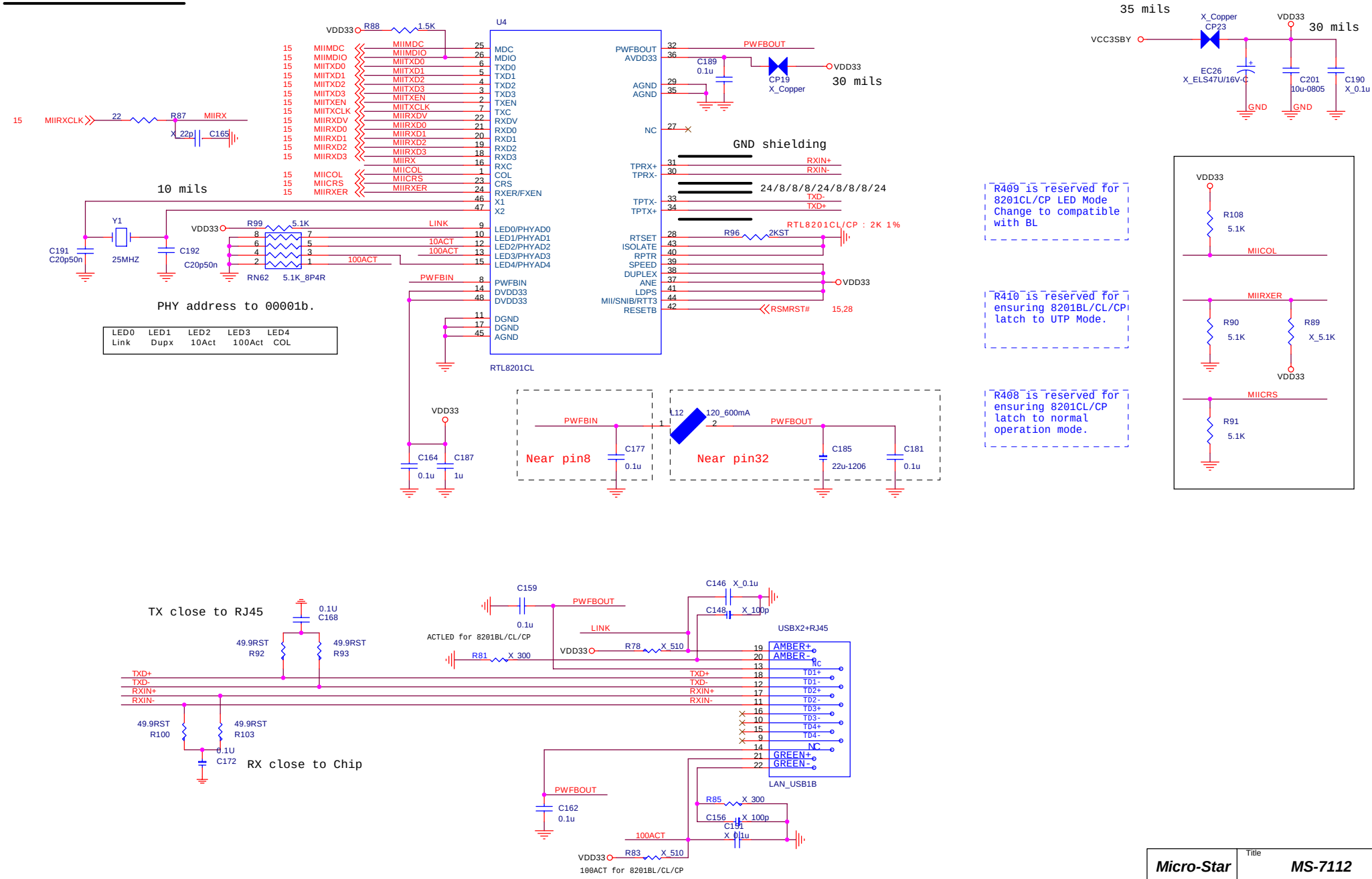
CLOSED TO CNR

* AC'97 Trace Spacing : 10 mils

Micro-Star	Title: MS-7112	Rev: 0A
Document Number: PCI 1,2 & CNR		
Last Revision Date: Monday, August 23, 2004	Sheet 19 of 31	

REALTEK 8201BL MII PHY

MIITXCLK , MIIRXCLK 14 / 7 / 14



R409 is reserved for 8201CL/CP LED Mode Change to compatible with BL

R410 is reserved for ensuring 8201BL/CL/CP latch to UTP Mode.

R408 is reserved for ensuring 8201CL/CP latch to normal operation mode.

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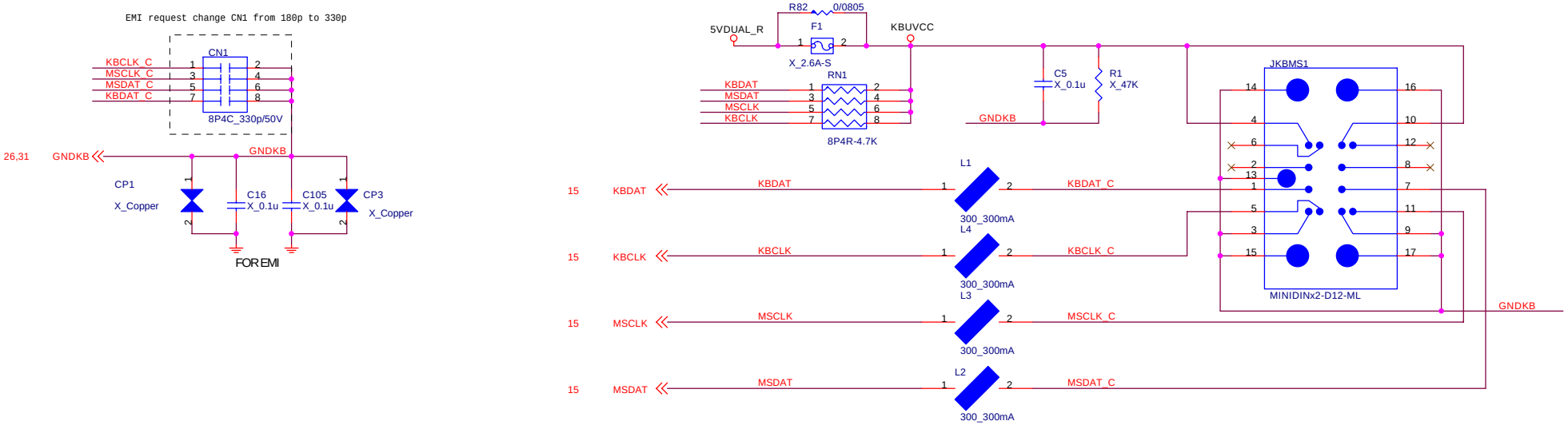
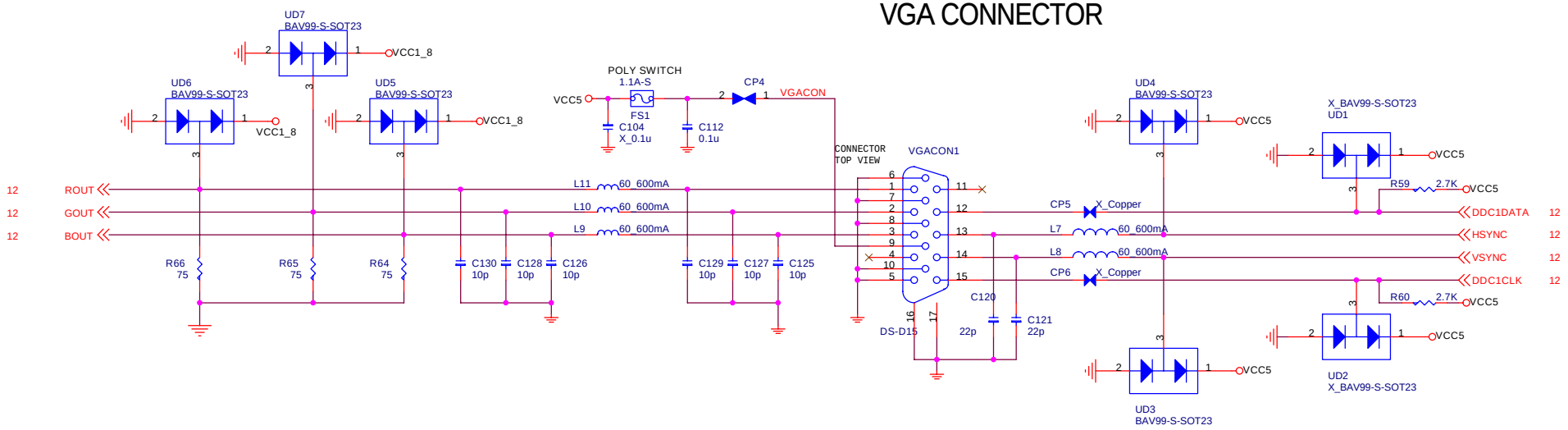
KEYBOARD/MOUSE PORTS



VGA CONNECTOR



Micro-Star	Title: MS-7112	Rev: 0A
	Document Number: PS/2 & VGA Conn.	
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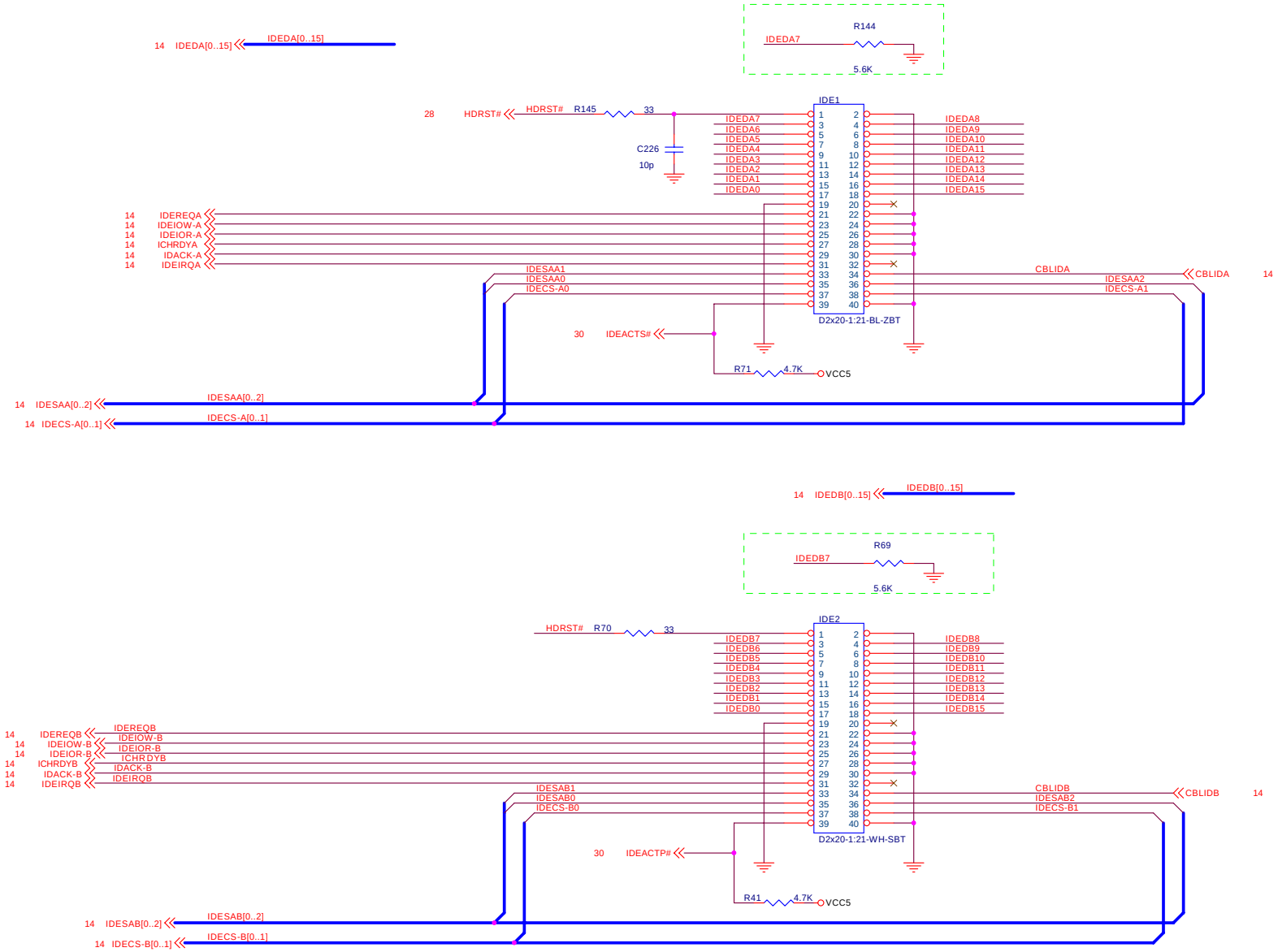

Micro-Star	Title: MS-7112	Rev: 0A
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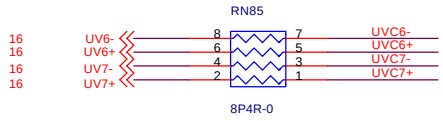
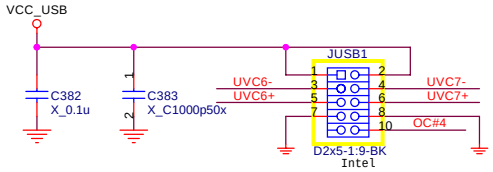
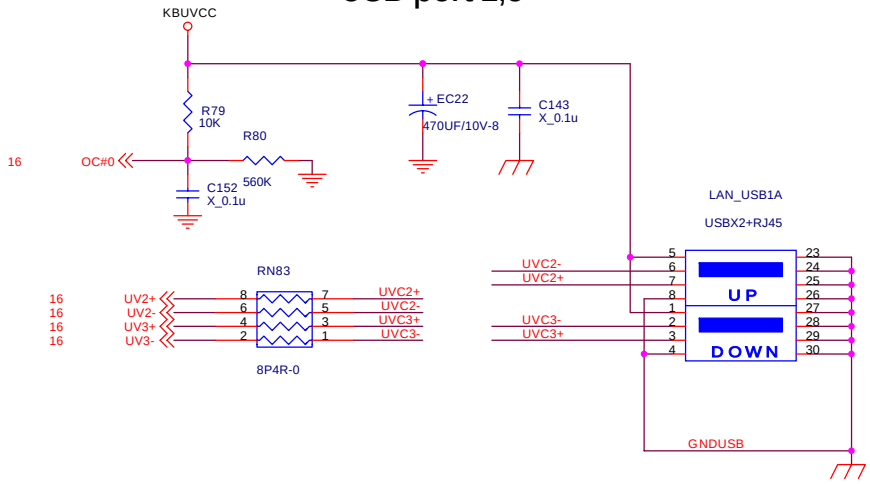
USB port 6,7

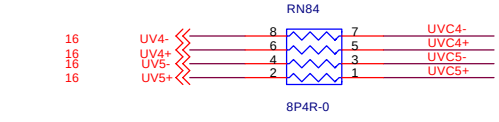


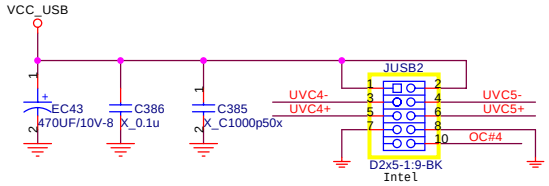


USB port 2,3

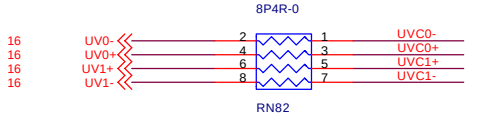


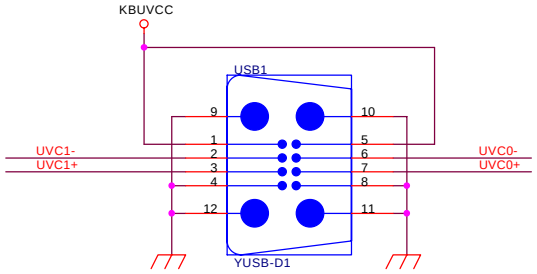
USB port 4,5

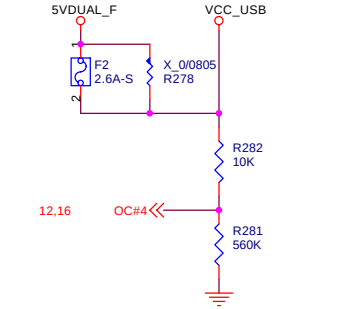


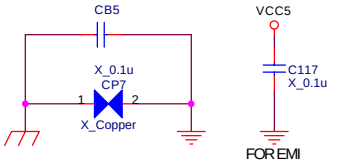


USB port 0,1









Micro-Star	Title: MS-7112	Rev: 0A
Document Number: USB CONNECTOR		
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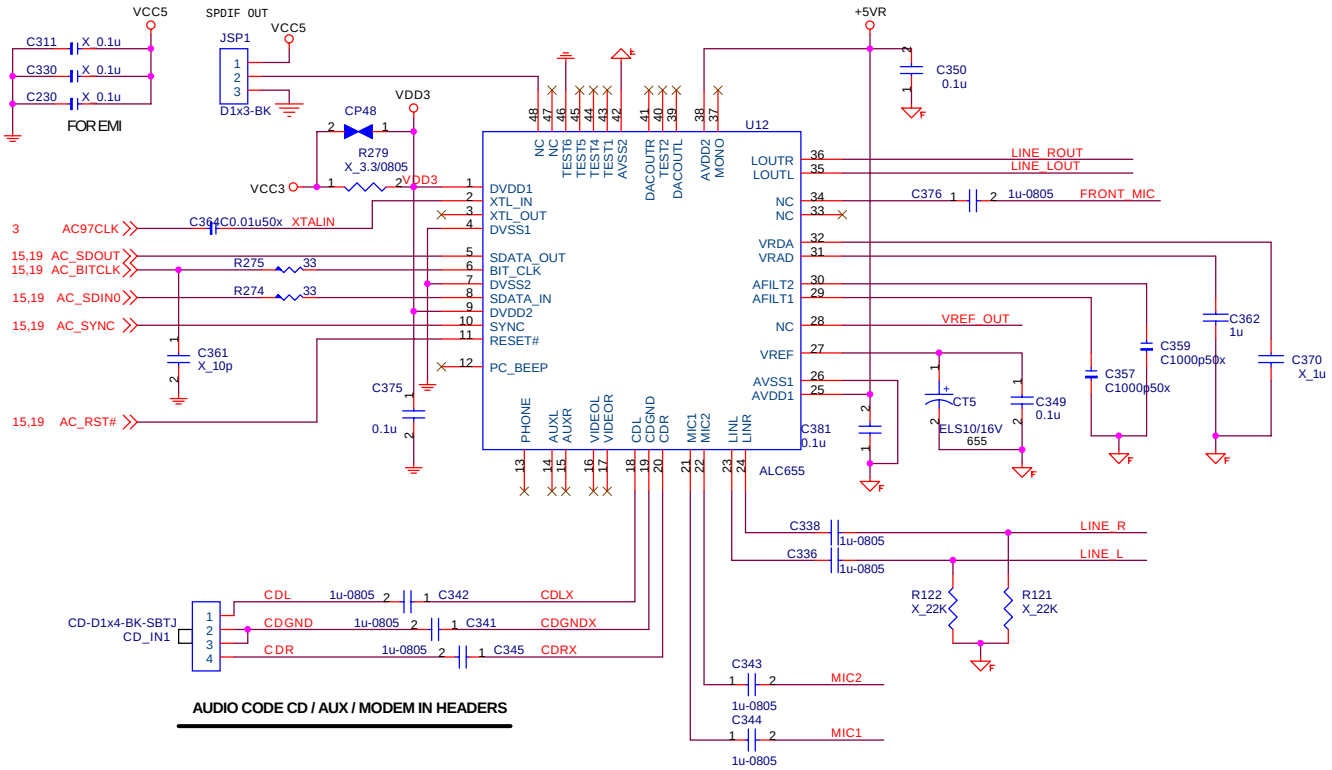
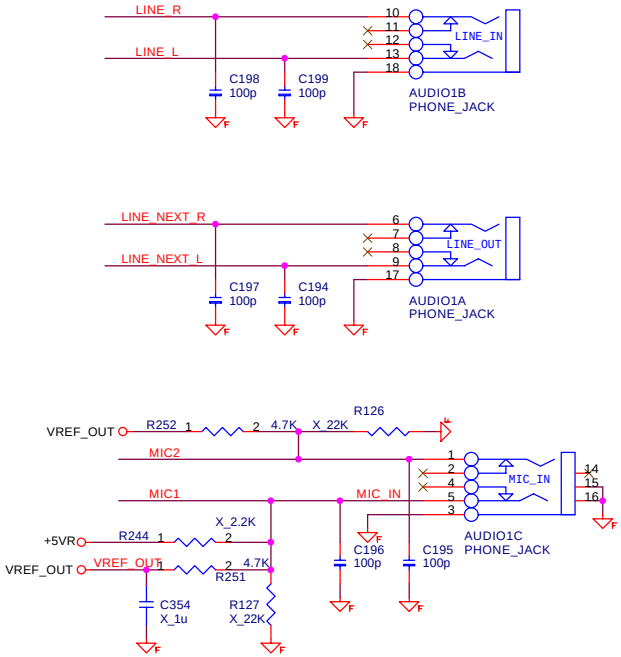
ALC655 AC97 CODEC

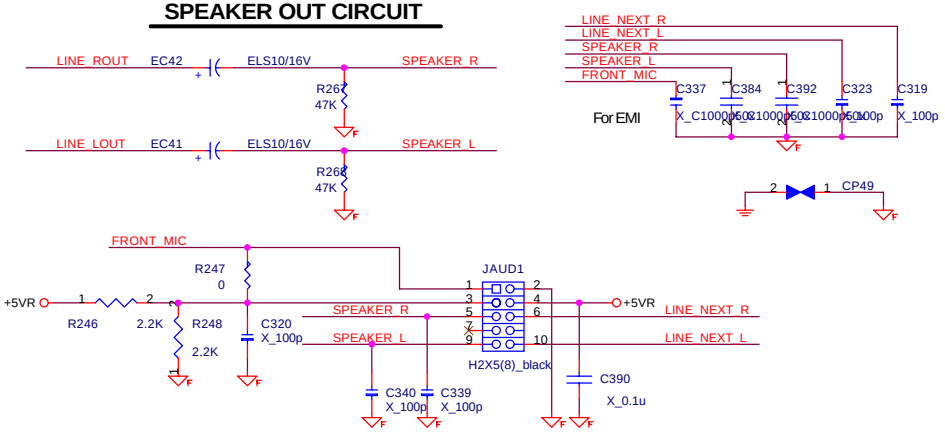


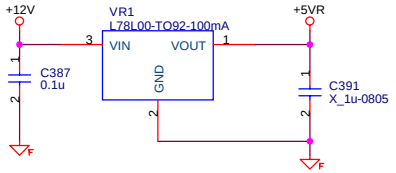
AUDIO CODE CD / AUX / MODEM IN HEADERS

SPEAKER OUT JACK

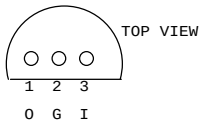


SPEAKER OUT CIRCUIT

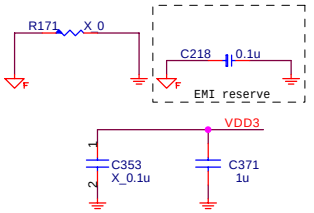




AUDIO CODE REGULATORS



DECOUPLING CAPACITOR



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Flash Rom

RTSA#	L: CFAD=2E	H: CFAD=4E
IRTX	L: 24MHZ	H: 48MHZ
SOUTA	L: ISA ROM	H: NO ISA ROM
DTRA#	L: PNP Default	H: PNP No Default

C99 near U10 pin 32

Hardware Monitor

C11-3322013-Y01

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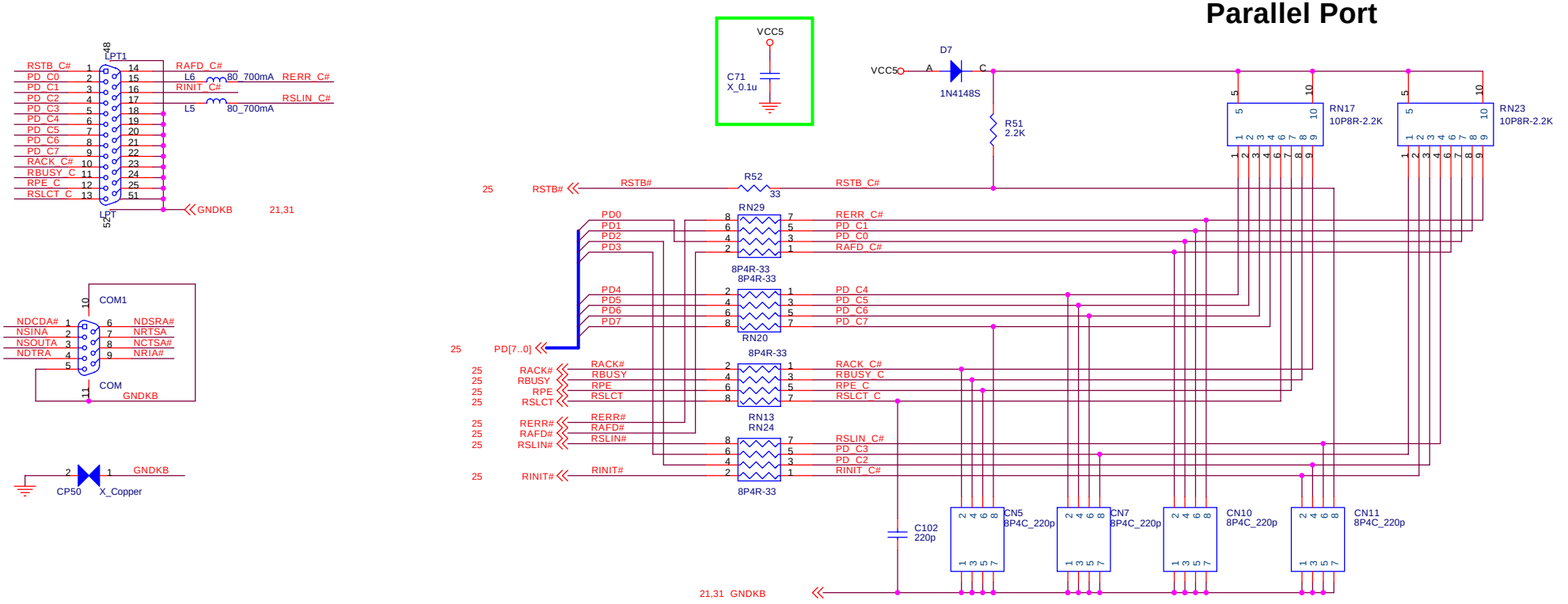
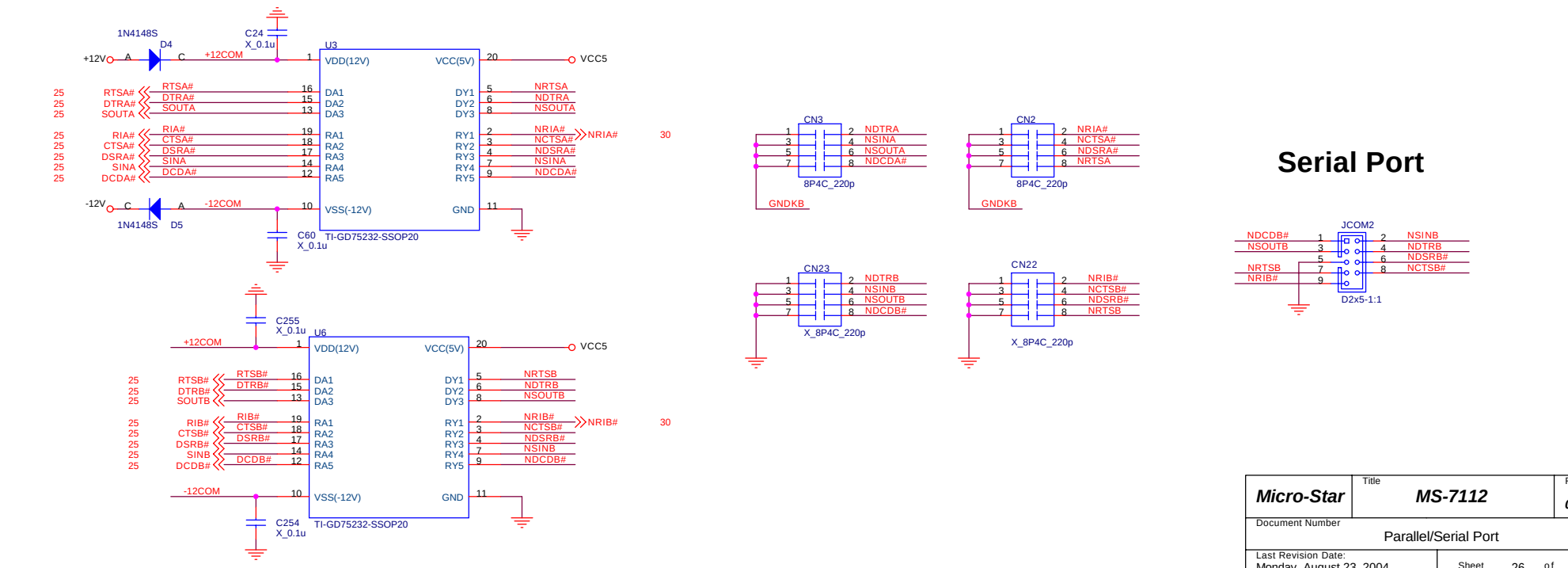
Parallel Port



Serial Port



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Document Number: Parallel/Serial Port		
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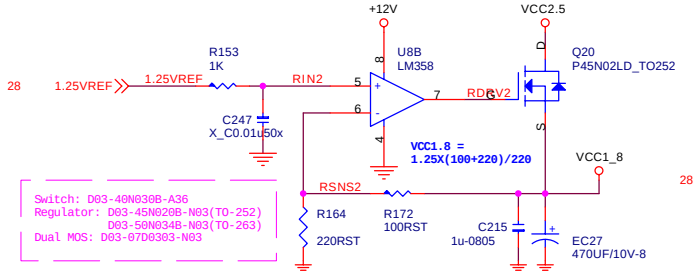
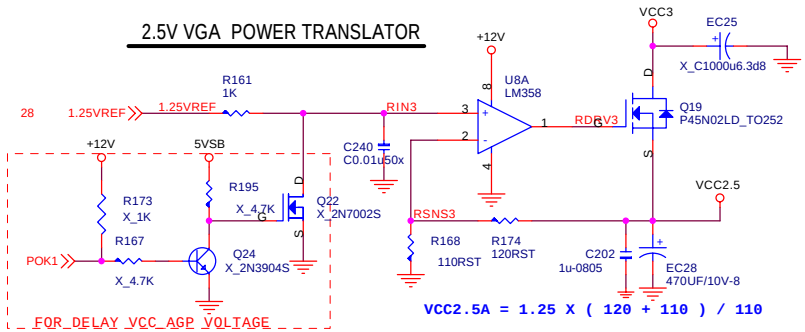
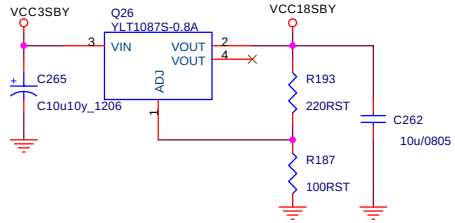
1.8V POWER TRANSLATOR

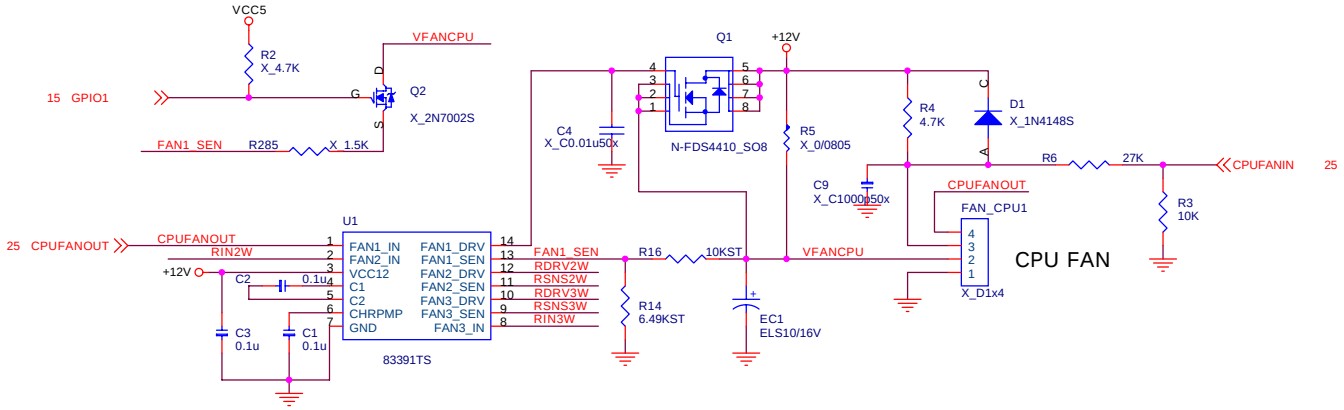


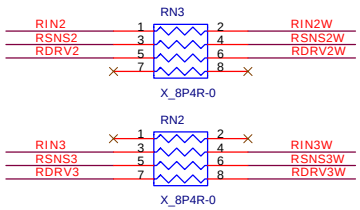
2.5V VGA POWER TRANSLATOR

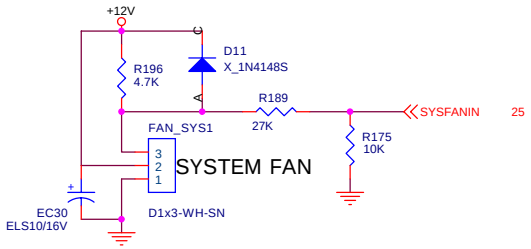


1.8V POWER TRANSLATOR









Micro-Star	Title: MS-7112	Rev: 0A
Document Number: Regulators & Fans		
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Pin 47 Difinition

MS6 VERSION: RAC
3VSB MODE SELECT

3VSB MODE	PIN 47
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

MS6 VERSION: RBD
VAGP SEQUENCE MODE SELECT

VAGP SEQUENCE MODE	PIN 47
VAGP ON BEFORE PWR_OK L TO H	PULL LOW
VAGP ON AFTER PWR_OK L TO H	PULL HIGH

Linear Mode

	S0	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S5#	1	1	0
SLP_S3#	1	0	0

THESE OUTPUT AND INPUT PIN MUST BE PULL HIGH

CPU_GD — 5 — CPU PWR_GD OUTPUT
MS7_POK — 12,15 — CHIP PWR_GD OUTPUT
SMBCLK — 3,7,15,19 — I2C BUS
SMBDAT — 3,7,15,19 — I2C BUS
RSMRST# — 15,20 — CONNECT TO SOUTH BRIDGE RSMRST# SIGNAL
SLP_S5# — SOUTH BRIDGE POWER CONTROL(SLP_S4# OR SUSB#) SIGNAL
SLP_S3# — SOUTH BRIDGE POWER CONTROL(SLP_S3# OR SUSC#) SIGNAL
SLP_S3# — 30 — ATX POWER OK INPUT
PWR_OK — 30

VDIMM LINEAR OR PWM SELECT

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

20040319 ADV : jason suggestion : Pin 9 (SLOT_RST#) add serial resister (10 Ohm) and decouple cap (20P)

FRONT PANEL RESET BUTTON
PCIRST# INPUT
PCIRST# BUFFER OUTPUT

PCI SOLT PCIRST# BUFFER OUTPUT

VDDA_25

VDDA_25 To CPU Copper trace width > 50mils

CLOSE TO MS6

CHARGE PUMP VOLTAGE OUTPUT

5V_DUAL

VDDQ 3396mW

VDD_12_A

Routed as pour to CPU width > 250mils

CONNECT TO CPU

WATCHING DOG TIMER SELECT

WD_DET	TIMER
PULL LOW	OFF
PULL HIGH	ON

THE TWO MODE ONLY ONE MODE PRESENT

DUAL MODE
THIS MODE SELECT BY PIN 47 PULL LOW

3VSB REGULATE BY 5VSB AND VCC3

3VDUAL

THE VDIMM_HSEN IN LINEAR MODE

DDRTYPE	VDIMM_HSEN VREF
DDR	2.0V
DDR II	1.7V

20040319 ADV : jason suggestion : Pin 16 (SS) use 0.22uF X7R.

THE TWO BLOCK CHOICE ONE SUPPORT SYSTEM POWER CONTROL

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils

DDR_VTT 1. 25V

DDR TERMINATION

DDR_AND_DDR_II_VOLT_SELECT

DDRTYPE	VDIMM
PULL LOW	2.5V
PULL HIGH	1.8V

RAC: R26=1K Ohm, R25=2.2K Ohm
RBF: R26=100 Ohm, R25=100 Ohm

Q10,Q11:Imax=7A(P45N02LD)
Please refer P5 list 2
"MOS select method"

THIS POINT VOLT CAN'T SETTING BELOW 2.9V

MS-6/RAC

<OrgName>	
Title	ACPI Power MS-6
Size	Document Number: MS-7112
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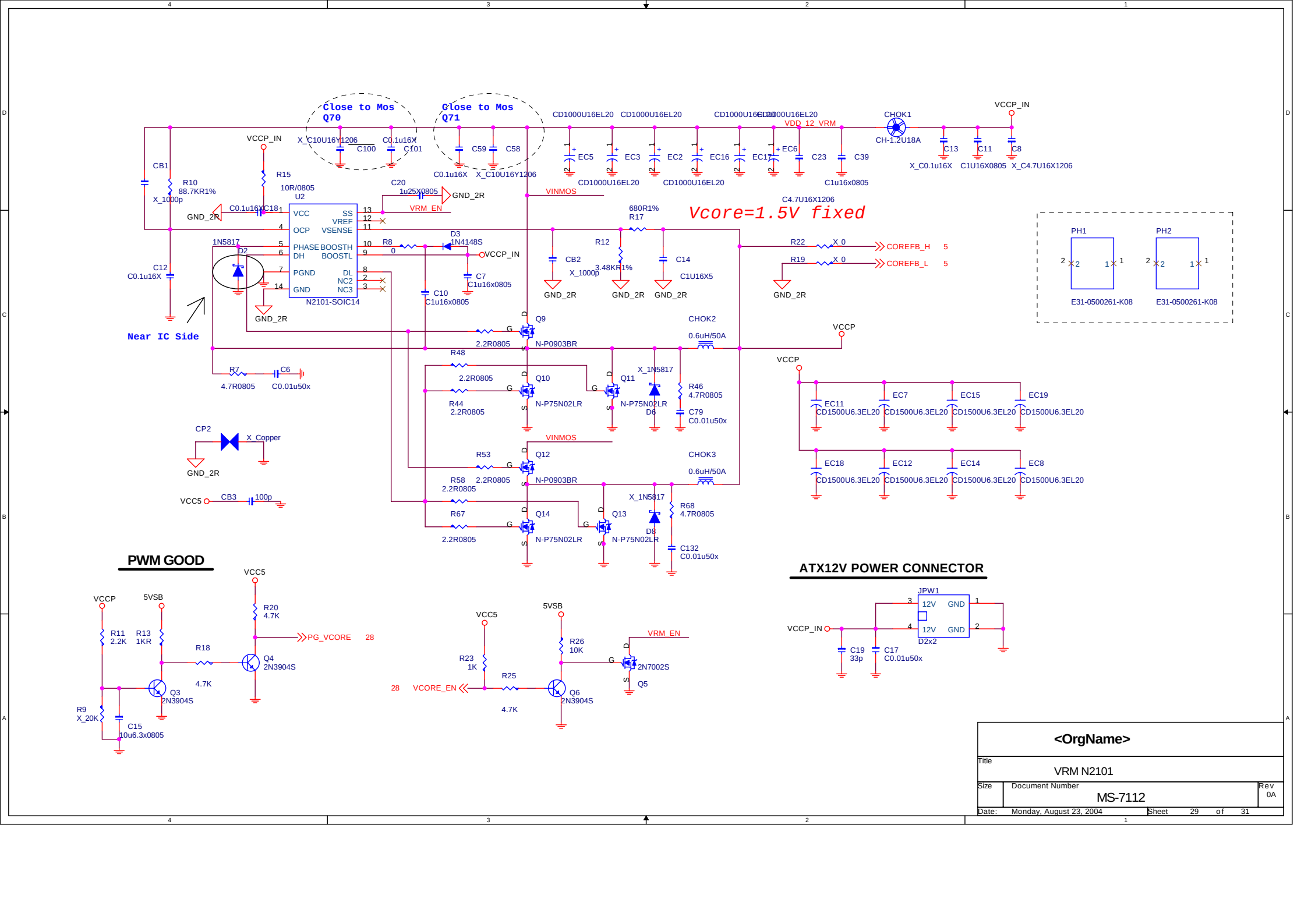

<OrgName>		
Title: VRM N2101		
Size	Document Number: MS-7112	Rev: 0A
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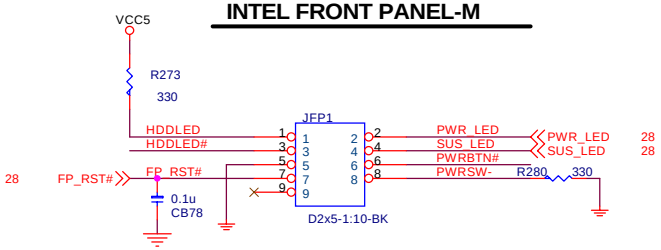
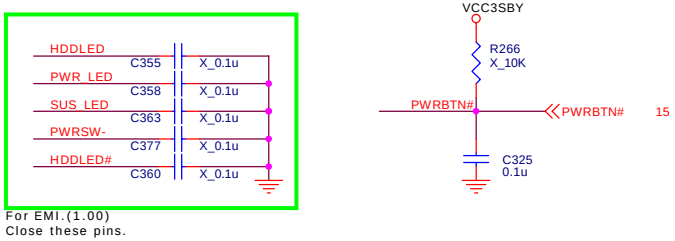
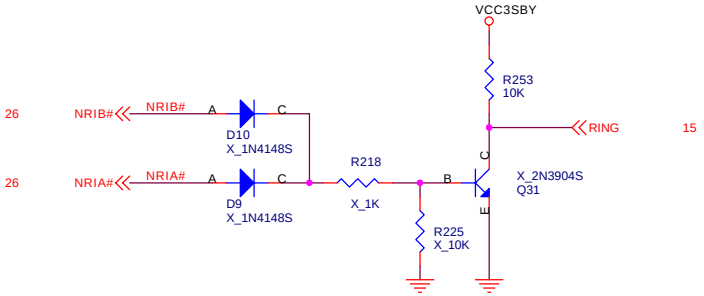
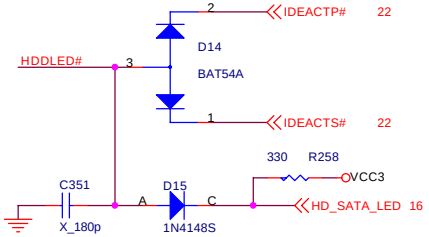
INTEL FRONT PANEL-M

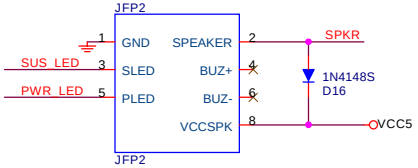




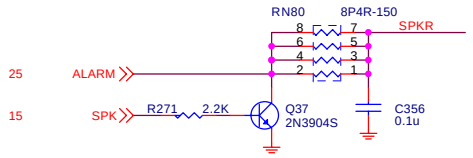
Wake by Modem



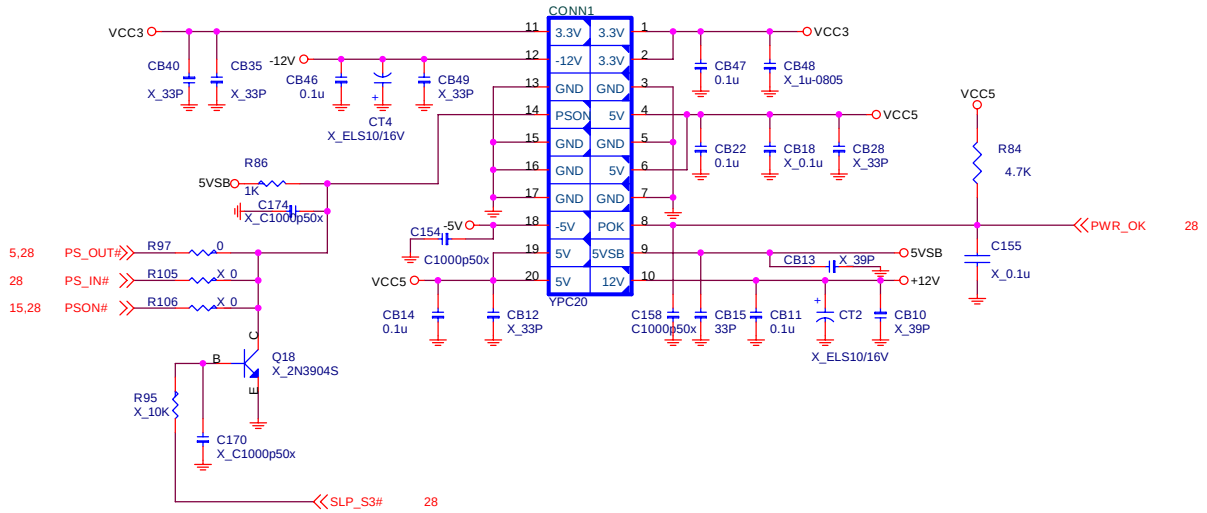




SPEAKER



ATX CONNECTOR



Micro-Star	Title: MS-7112	Rev: 0A
Document Number: FRONT PANEL & ATX Conn.		
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PCB OTHER COMPONENT

BS1_X1 BS2_X1 BS3_X1 BS4_X1 BS5_X1

J1 X_PIN1*2 CPU

J2 VCC5 X_PIN1*2 AGP

21,26 GNDKB

MH1 MH2 MH3 MH4 MH5 MH6

FM15 FM17 FM20 FM18
FM16 FM1 FM19 FM2
FM8 FM12 FM13 FM10
FM7 FM9 FM5 FM4
FM6 FM11 FM3 FM14
X_FM

MS7103PCB

PCB1
7112 0A

SB1_H
X_SB Heatsink

SB1_L
SIS 964L UA
X_SIS-964L V: A2

BAT SOCKET
BAT1
BATTERY
Battery-CR2032-3V-210mAh

NB1_A
NB-Heat Sink

BIOS1_A
Flash-2M
Winbond
49F002U

BIOS1_B
X_Flash-4M
SST39SF040

BIOS1_C
X_Flash-4M
W29C040P
SST39SF040

System Decoupling Capacitors

+12V: EC37 X_ELS10/16V, C329 X_0.1u

VCC5: EC34 X_ELS10/16V, C378 0.1u, C332 X_0.1u, C348 X_0.1u, C365 X_0.1u, C318 X_0.1u, C367 X_0.1u, C307 X_0.1u

-12V: EC36 X_ELS10/16V, C328 0.1u, C64 X_0.1u

VCC3: EC40 X_ELS10/16V, C316 X_0.1u, C308 X_0.1u, C309 X_0.1u, C333 X_0.1u

VCC3SBY: C331 0.1u, C267 X_0.1u

VCC3: C368 X_0.1u, C310 X_0.1u, C380 X_0.1u

5VSB: C393 0.1u

High Freq. return current decoupling

VCC5 C228 VCC3 X_C1000p50x
VCCM C116 X_C1000p50x
VCCM C206 VCC3 X_C1000p50x
VCC3 C193 VCC1_8 X_C1000p50x
VCC3 C369 VCC5 X_C1000p50x
R242 X_0
R283 X_0

Micro-Star	Title: MS-7112	Rev: 0A
	Document Number: DECOUPLING CAPACIROT	
	Last Revision Date: Monday, August 23, 2004	Sheet 31 of 31