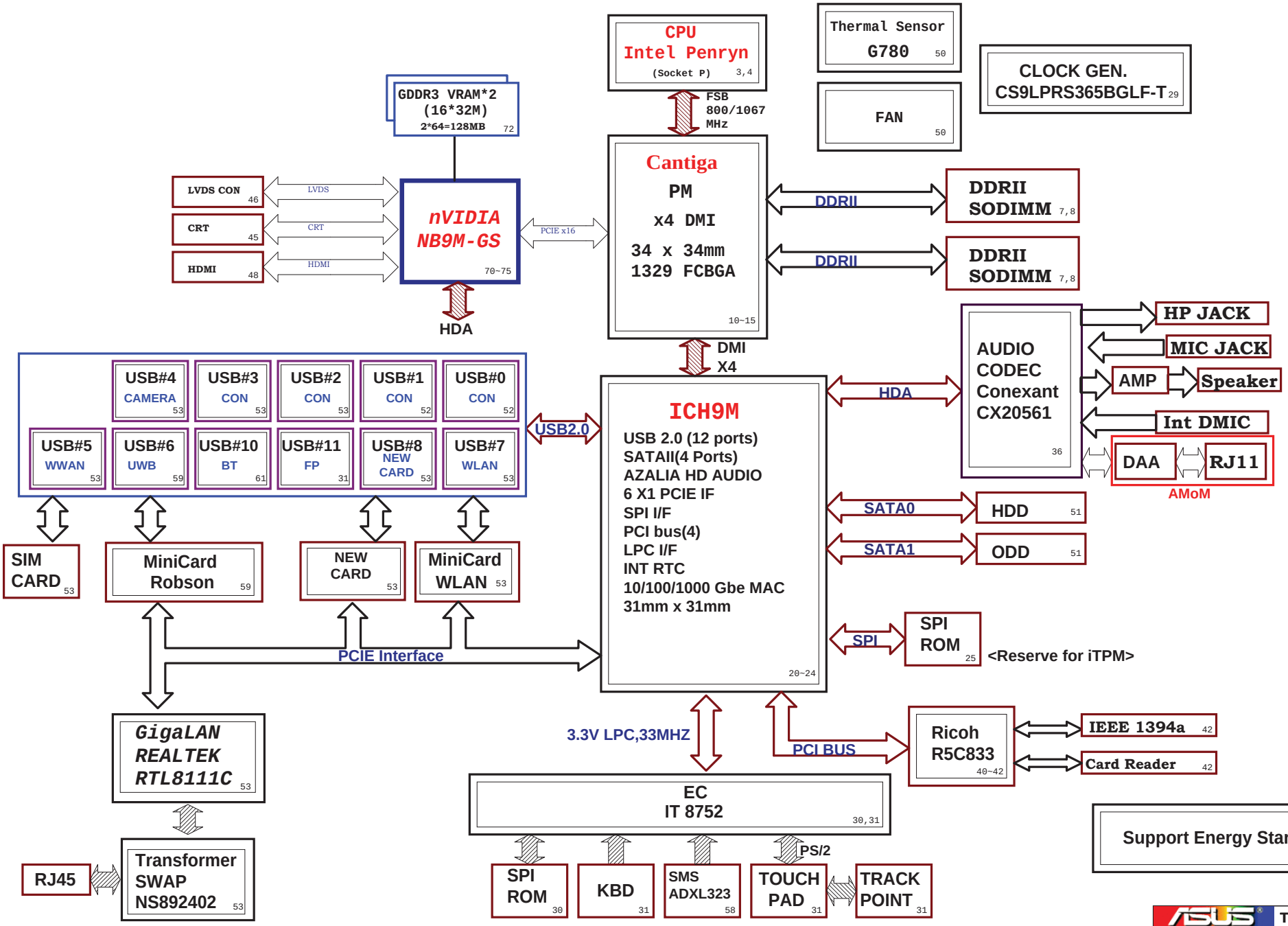
Rocky40/50 Discrete VGA Block Diagram
2007/12/20



Title : Block Diagram			
Engineer: Tina Lee			
Size: Custom	Project Name: Rocky 40/50		Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 1 of 94		

Rocky 40/50 Schematic Index

Page	System page Ref.
01	Block Diagram
02	Schematic Information
03-05	CPU-Penryn
07-09	DDR III SO-DIMM
10-15	Cantiga
20-24	ICH9M
25	SPI ROM
29	CLK-ICS9LPRS365BGLFT
30-31	EC_IT8752
32	POWER-ON SEQUENCE
33	LAN_RTL811C***
34	RJ45***
35	MDC***
36	CODEC-CX20561
37	AUDIO_AMP-G1431F2U
38	MICROPHONE & SPEAKER CONN
39	DSP***
40	CARDBUS R5C833(PCI I/F)
41	CARDBUS R5C833(1394 & SD)
42	IEEE1394A & 4 IN1 CON
43	NewCard PWR SW & CON***
44	Debug
45	CRT
46	LVDS & INVERTER CONNECTOR
47	TV OUT CONN***
50	THER SENSOR & FAN
51	HDD & CDROM
52	USB Port x 2
53	IO BOARD
54	PORT Docking***
55	Super I/O & FIR
56	LED
57	DISCHARGE
58	SMS
60	DC power jack, Batter conn.
61	Blue Tooth
62	TPM***
65	MDC NUT & Hinksink NUT***
66	E-SATA***
68	XDP***
80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.8VS & VCCP
83	POWER_I/O_DDR & VTT
84	POWER_I/O_***
85	PWR_VGA_CORE & 1.1V
87	POWER_SHUTDOWN#
88	POWER_CHARGER
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI		+3VS
GPIO 07	GPI		+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	UWB_ON	+3VSUS
GPIO 10	GPI	-	+3VSUS
GPIO 11	Native	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#	+3VSUS
GPIO 14	GPI	RTLAN_DSM#	+3VSUS
GPIO 15	Native	-	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_LED	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	BT_DET#	+3VS
GPIO 23	Native	-	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	-	+3VSUS
GPIO 26	Native	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	GPO	-	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	CLK_SATA_REQ#	+3VS
GPIO 36	GPI	-	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	GPU_RST#	**+3VS**
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	GPI	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	-	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	NOVO_CARE_LED#	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	GPO	-	
GPA7	GPO	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	-	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	-	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	-	
GPE6	GPI	LID_SW#	
GPE7	GPO	MEDIA_KEY#	
GPF0	GPI	-	
GPF1	GPI	NOVO_CARE#	
GPF2	ALT	TP1_CLK	
GPF3	ALT	TP1_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	SUSPEND_LED#	
GPG0	GPI	PM_THERM#_EC	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

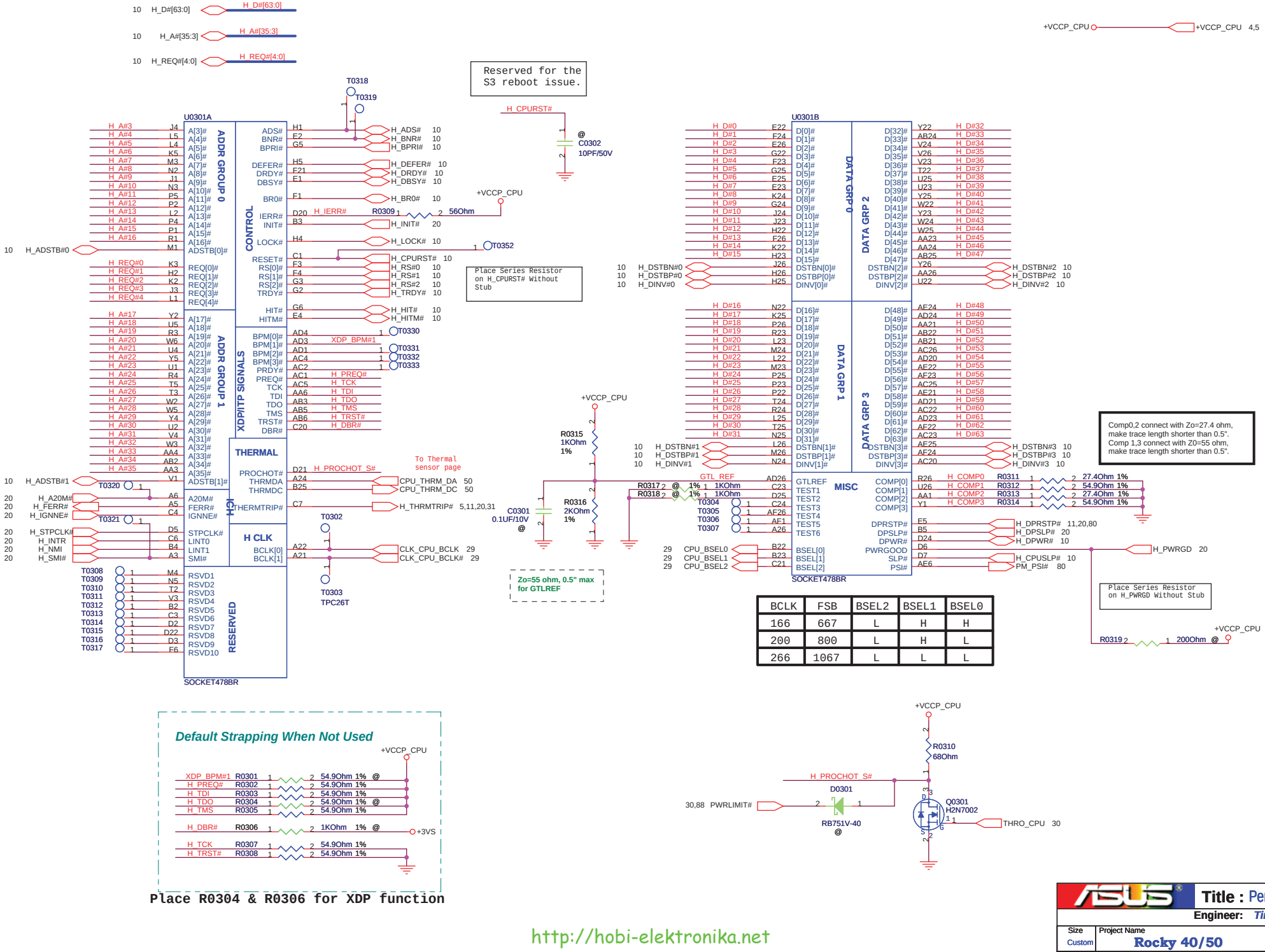
EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	3G_ON#	
GPH2	ALT	LOGO_LED#	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED#	
GPH6	GPO	CAP_LED#	
-	-	-	
GPI0	GPI	NV_OVERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	XOUT	
GPI5	GPI	YOUT	
GPI6	GPI	-	
GPI7	GPI	-	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	PWR_LED#	
GPK0	GPI	-	
GPK1	GPI	-	
GPK2	GPI	-	
GPK3	GPI	-	
GPK4	GPI	-	
GPK5	GPI	-	
GPL0	GPI	APS_PWR_CNT#	
GPL1	GPI	APS_ST#	
GPL2	GPO	USB_PWR_EN#	
GPL3	GPO	-	
GPL4	GPO	-	
GPL5	GPO	AC_ID	
GPL6	GPO	AC_65W	
GPL7	GPO	CHG_LOW_LED#	
GPK6	GPO	-	
GPK7	GPI	-	

ASUS Title : Schematic Information

Engineer: Tina Lee

Size	Project Name	Rev
Custom	Rocky 40/50	1.0

Date: Wednesday, December 19, 2007 Sheet 2 of 94



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Title :	Penryn CPU (1)
Engineer:	Tina Lee
Size: Custom	Project Name: Rocky 40/50
Rev:	1.0
Date:	Thursday, December 20, 2007
Sheet	3 of 94

+VCORE +VCORE 5,80

+VCCP_CPU +VCCP_CPU 3,5

+1.5VS +1.5VS 14,23,53,57,59,82

+VCORE +VCORE

U0301C

SOCKET478BR

+VCCP_CPU

+VCCA_CPU
120 mA

+1.5VS

RX0403
0Ohm

C0402
0.01UF/16V

C0401
10UF/6.3V

VID[0] H_VID0 VR_VID0 80
VID[1] H_VID1 VR_VID1 80
VID[2] H_VID2 VR_VID2 80
VID[3] H_VID3 VR_VID3 80
VID[4] H_VID4 VR_VID4 80
VID[5] H_VID5 VR_VID5 80
VID[6] H_VID6 VR_VID6 80

R0401
100Ohm 1%

VCCSENSE 80
VSSSENSE 80

R0402
100Ohm
1%

VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

U0301D

SOCKET478BR

Title : Penryn CPU (2)

Engineer: Tina Lee

Size	Project Name	Rev
Custom	Rocky 40/50	1.0

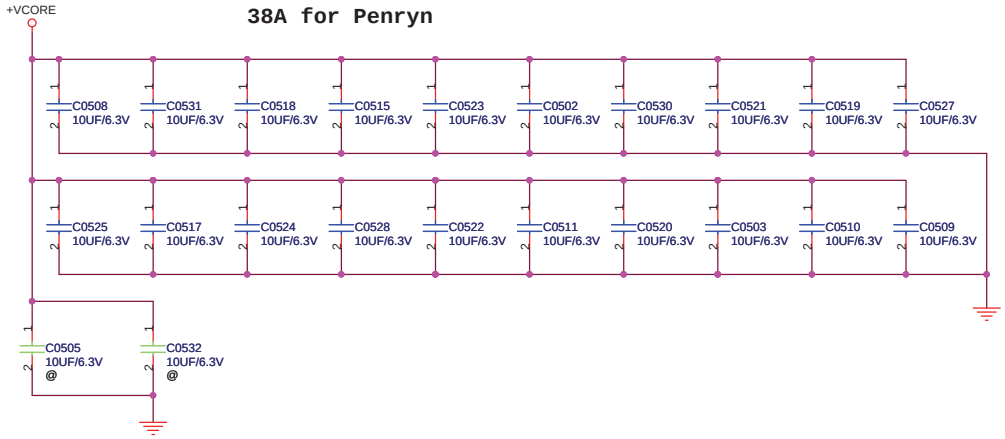
Date: Thursday, December 20, 2007 Sheet 4 of 94

+VCORE +VCORE 4,80

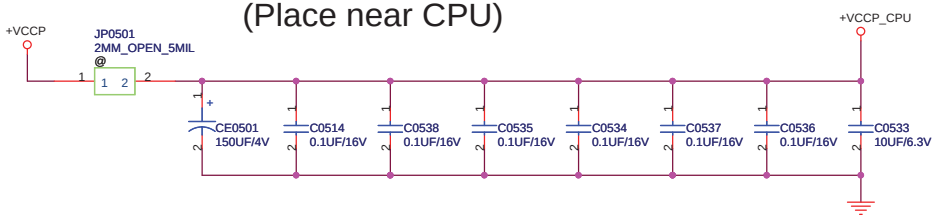
+VCCP +VCCP 10,11,13,14,20,23,29,80,82

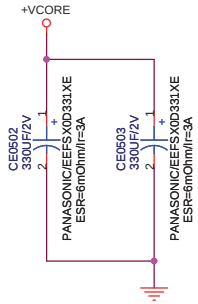
+VCCP_CPU +VCCP_CPU 3,4

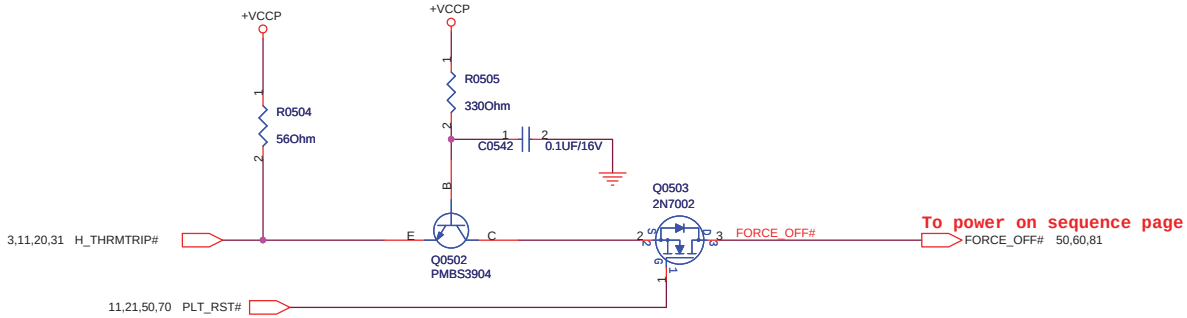
38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)







Thermal Trip signal(From CPU to ICH-9M and sequence)

Title : CPU CAPS		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 5 of 94	

ASUS	Title :	
	Engineer: *Tina Lee*	
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 6 of 94	

+3VS → +3VS 3,8,11,14,15,20,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92

+1.8V → +1.8V 8,9,11,13,83,91

M_VREF_MCH → M_VREF_MCH 8,9,11

SMBus Slave Address:A0H

temp_5886_tl01
(12G025M22000LVwith 12G025C2200WLV
co-lay symbol)

SMBus Slave Address: A0H

9,12 M_A_A[0..14]

M_A_A0 102 A0
M_A_A1 101 A1
M_A_A2 100 A2
M_A_A3 99 A3
M_A_A4 98 A4
M_A_A5 97 A5
M_A_A6 94 A6
M_A_A7 92 A7
M_A_A8 93 A8
M_A_A9 91 A9
M_A_A10 105 A10/AP
M_A_A11 90 A11
M_A_A12 89 A12
M_A_A13 116 A13
M_A_A14 86 A14
84 A15
9,12 M_A_BS2 85 A16_BA2

9,12 M_A_BS0 107 BA0
9,12 M_A_BS1 106 BA1
9,11 M_CS#0 110 S0#
9,11 M_CS#1 115 S1#
11 M_CLK_DDR0 30 CK0
11 M_CLK_DDR#0 32 CK0#
11 M_CLK_DDR1 164 CK1
11 M_CLK_DDR#1 166 CK1#
9,11 M_CKE0 79 CKE0
9,11 M_CKE1 80 CKE1
9,12 M_A_CAS# 113 CAS#
9,12 M_A_RAS# 108 RAS#
9,12 M_A_WE# 109 WE#
M_A_SA0 198 SA0
M_A_SA1 200 SA1
8,24,25,29 SMB_CLK_M 197 SCL
8,24,25,29 SMB_DAT_M 195 SDA
9,11 M_ODT0 114 ODT0
9,11 M_ODT1 119 ODT1

12 M_A_DM[0..7]
M_A_DM0 10 DM0
M_A_DM1 26 DM1
M_A_DM2 52 DM2
M_A_DM3 67 DM3
M_A_DM4 130 DM4
M_A_DM5 147 DM5
M_A_DM6 170 DM6
M_A_DM7 185 DM7

12 M_A_DQS[0..7]
M_A_DQS0 13 DQS0
M_A_DQS1 31 DQS1
M_A_DQS2 51 DQS2
M_A_DQS3 70 DQS3
M_A_DQS4 131 DQS4
M_A_DQS5 148 DQS5
M_A_DQS6 169 DQS6
M_A_DQS7 188 DQS7

12 M_A_DQS#[0..7]
M_A_DQS#0 11 DQS#0
M_A_DQS#1 29 DQS#1
M_A_DQS#2 49 DQS#2
M_A_DQS#3 68 DQS#3
M_A_DQS#4 129 DQS#4
M_A_DQS#5 146 DQS#5
M_A_DQS#6 167 DQS#6
M_A_DQS#7 186 DQS#7

J0701A

M_A_DQ4 5 DQ0
M_A_DQ0 7 DQ1
M_A_DQ6 17 DQ2
M_A_DQ7 19 DQ3
M_A_DQ1 4 DQ4
M_A_DQ5 6 DQ5
M_A_DQ2 14 DQ6
M_A_DQ3 16 DQ7
M_A_DQ13 23 DQ8
M_A_DQ12 25 DQ9
M_A_DQ15 35 DQ10
M_A_DQ10 37 DQ11
M_A_DQ9 20 DQ12
M_A_DQ8 22 DQ13
M_A_DQ14 36 DQ14
M_A_DQ11 38 DQ15
M_A_DQ18 43 DQ16
M_A_DQ21 45 DQ17
M_A_DQ22 55 DQ18
M_A_DQ16 57 DQ19
M_A_DQ17 44 DQ20
M_A_DQ20 46 DQ21
M_A_DQ19 56 DQ22
M_A_DQ23 58 DQ23
M_A_DQ28 61 DQ24
M_A_DQ24 63 DQ25
M_A_DQ30 73 DQ26
M_A_DQ31 75 DQ27
M_A_DQ29 62 DQ28
M_A_DQ25 64 DQ29
M_A_DQ26 74 DQ30
M_A_DQ27 76 DQ31
M_A_DQ33 123 DQ32
M_A_DQ37 125 DQ33
M_A_DQ38 135 DQ34
M_A_DQ39 137 DQ35
M_A_DQ32 124 DQ36
M_A_DQ36 126 DQ37
M_A_DQ35 134 DQ38
M_A_DQ34 136 DQ39
M_A_DQ45 141 DQ40
M_A_DQ44 143 DQ41
M_A_DQ43 151 DQ42
M_A_DQ46 153 DQ43
M_A_DQ40 140 DQ44
M_A_DQ41 142 DQ45
M_A_DQ42 152 DQ46
M_A_DQ47 154 DQ47
M_A_DQ53 157 DQ48
M_A_DQ52 159 DQ49
M_A_DQ51 173 DQ50
M_A_DQ54 175 DQ51
M_A_DQ48 158 DQ52
M_A_DQ49 160 DQ53
M_A_DQ50 174 DQ54
M_A_DQ55 176 DQ55
M_A_DQ56 179 DQ56
M_A_DQ63 181 DQ57
M_A_DQ57 189 DQ58
M_A_DQ62 191 DQ59
M_A_DQ60 180 DQ60
M_A_DQ61 182 DQ61
M_A_DQ59 192 DQ62
M_A_DQ58 194 DQ63

DDR2_DIMM_200P

M_A_DQ[0..63] 12

Place near SO-DIMM_0

M_CLK_DDR0 → C0701 10PF/50V @ → M_CLK_DDR#0
M_CLK_DDR1 → C0702 10PF/50V @ → M_CLK_DDR#1

R0703 10KOhm
R0704 10KOhm

Layout Note: Place these caps near SO DIMM 0

Layout Note: Place these caps near SO DIMM 0

+1.8V
C0703 0.1UF/10V
C0704 0.1UF/10V
C0705 0.1UF/10V
C0706 0.1UF/10V

+3VS
C0712 2.2UF/6.3V
C0713 0.1UF/10V

11 PM_EXTTS#0 → RX0702 0Ohm @ → PM_EXTTS#0_R

M_VREF_MCH
C0715 2.2UF/6.3V
C0714 0.1UF/10V

VREF -> 10/10 mils

J0701B

112 VDD1
111 VDD2
117 VDD3
96 VDD4
95 VDD5
118 VDD6
81 VDD7
82 VDD8
87 VDD9
103 VDD10
88 VDD11
104 VDD12
199 VDDSPD
83 NC1
120 NC2
50 NC3
69 NC4
163 NCTEST
1 VREF
201 GND0
202 GND1
203 NP_NC1
204 NP_NC2
47 VSS1
133 VSS2
183 VSS3
77 VSS4
12 VSS5
48 VSS6
184 VSS7
78 VSS8
71 VSS9
72 VSS10
121 VSS11
122 VSS12
196 VSS13
193 VSS14
8 VSS15
18 VSS16
24 VSS17
41 VSS18
53 VSS19
42 VSS20
54 VSS21
59 VSS22
65 VSS23
60 VSS24
66 VSS25
127 VSS26
139 VSS27
128 VSS28
145 VSS29
165 VSS30
171 VSS31
172 VSS32
177 VSS33
187 VSS34
178 VSS35
190 VSS36
9 VSS37
21 VSS38
33 VSS39
155 VSS40
34 VSS41
132 VSS42
144 VSS43
156 VSS44
168 VSS45
2 VSS46
3 VSS47
15 VSS48
27 VSS49
39 VSS50
149 VSS51
161 VSS52
28 VSS53
40 VSS54
138 VSS55
150 VSS56
162 VSS57

DDR2_DIMM_200P

SO-DIMM 0 is placed nearer the GMCH than SO-DIMM 1

+1.8V
C0716 2.2UF/6.3V
C0717 2.2UF/6.3V
C0718 2.2UF/6.3V
C0719 2.2UF/6.3V

Layout Note: Place these Caps near SO DIMM 0

+1.8V
CE0701 220UF/4V @ ESR=40mOhm/Ir=1.9A

PLACE NEAR SO-DIMM_0 / SO-DIMM_1

Title	DDR2 SO-DIMM_0	
Engineer:	Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 7 of 94	

+3VS → +3VS 3,7,11,14,15,20,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92

+1.8V → +1.8V 7,9,11,13,83,91

M_VREF_MCH → M_VREF_MCH 7,9,11

temp_5886_tl02
(12G025032005LV with 12G025022004LV
CO-LAY symbol)

SMBus Slave Address:A4H

Place near SO-DIMM_1

M_CLK_DDR3 — C0801 10PF/50V @ — M_CLK_DDR#3

M_CLK_DDR2 — C0802 10PF/50V @ — M_CLK_DDR#2

9,12 M_B_A[0..14]

9,12 M_B_BS2

9,12 M_B_BS0
9,12 M_B_BS1
9,11 M_CS#2
9,11 M_CS#3
11 M_CLK_DDR2
11 M_CLK_DDR#2
11 M_CLK_DDR3
11 M_CLK_DDR#3
9,11 M_CKE2
9,11 M_CKE3
9,12 M_B_CAS#
9,12 M_B_RAS#
9,12 M_B_WE#

M_B_SA0 — R0804 10KOhm M_B_SA1 — +3VS — R0803 10KOhm

7,24,25,29 SMB_CLK_M
7,24,25,29 SMB_DAT_M

9,11 M_ODT2
9,11 M_ODT3

12 M_B_DM[0..7]

12 M_B_DQS[0..7]

12 M_B_DQS#[0..7]

M_B_DQ[0..63] 12

J0801A

M_B_A0	102	A0	
M_B_A1	101	A1	
M_B_A2	100	A2	
M_B_A3	99	A3	
M_B_A4	98	A4	
M_B_A5	97	A5	
M_B_A6	94	A6	
M_B_A7	92	A7	
M_B_A8	93	A8	
M_B_A9	91	A9	
M_B_A10	105	A10/AP	
M_B_A11	90	A11	
M_B_A12	89	A12	
M_B_A13	116	A13	
M_B_A14	86	A14	
	84	A15	
	85	A16_BA2	
	107	BA0	
	106	BA1	
	110	S0#	
	115	S1#	
	30	CK0	
	32	CK0#	
	164	CK1	
	166	CK1#	
	79	CKE0	
	80	CKE1	
	113	CAS#	
	108	RAS#	
	109	WE#	
	198	SA0	
	200	SA1	
	197	SCL	
	195	SDA	
	114	ODT0	
	119	ODT1	
M_B_DM0	10	DM0	
M_B_DM1	26	DM1	
M_B_DM2	52	DM2	
M_B_DM3	67	DM3	
M_B_DM4	130	DM4	
M_B_DM5	147	DM5	
M_B_DM6	170	DM6	
M_B_DM7	185	DM7	
M_B_DQS0	13	DQS0	
M_B_DQS1	31	DQS1	
M_B_DQS2	51	DQS2	
M_B_DQS3	70	DQS3	
M_B_DQS4	131	DQS4	
M_B_DQS5	148	DQS5	
M_B_DQS6	169	DQS6	
M_B_DQS7	188	DQS7	
M_B_DQS#0	11	DQS#0	
M_B_DQS#1	29	DQS#1	
M_B_DQS#2	49	DQS#2	
M_B_DQS#3	68	DQS#3	
M_B_DQS#4	129	DQS#4	
M_B_DQS#5	146	DQS#5	
M_B_DQS#6	167	DQS#6	
M_B_DQS#7	186	DQS#7	
	5	DQ0	M_B_DQ1
	7	DQ1	M_B_DQ4
	17	DQ2	M_B_DQ3
	19	DQ3	M_B_DQ2
	4	DQ4	M_B_DQ0
	6	DQ5	M_B_DQ5
	14	DQ6	M_B_DQ6
	16	DQ7	M_B_DQ7
	23	DQ8	M_B_DQ8
	25	DQ9	M_B_DQ9
	35	DQ10	M_B_DQ15
	37	DQ11	M_B_DQ14
	20	DQ12	M_B_DQ12
	22	DQ13	M_B_DQ13
	36	DQ14	M_B_DQ10
	38	DQ15	M_B_DQ11
	43	DQ16	M_B_DQ19
	45	DQ17	M_B_DQ16
	55	DQ18	M_B_DQ23
	57	DQ19	M_B_DQ21
	44	DQ20	M_B_DQ17
	46	DQ21	M_B_DQ20
	56	DQ22	M_B_DQ18
	58	DQ23	M_B_DQ22
	61	DQ24	M_B_DQ29
	63	DQ25	M_B_DQ28
	73	DQ26	M_B_DQ26
	75	DQ27	M_B_DQ27
	62	DQ28	M_B_DQ25
	64	DQ29	M_B_DQ24
	74	DQ30	M_B_DQ31
	76	DQ31	M_B_DQ30
	123	DQ32	M_B_DQ32
	125	DQ33	M_B_DQ36
	135	DQ34	M_B_DQ37
	137	DQ35	M_B_DQ38
	124	DQ36	M_B_DQ34
	126	DQ37	M_B_DQ33
	134	DQ38	M_B_DQ35
	136	DQ39	M_B_DQ39
	141	DQ40	M_B_DQ44
	143	DQ41	M_B_DQ45
	151	DQ42	M_B_DQ42
	153	DQ43	M_B_DQ43
	140	DQ44	M_B_DQ40
	142	DQ45	M_B_DQ41
	152	DQ46	M_B_DQ47
	154	DQ47	M_B_DQ46
	157	DQ48	M_B_DQ53
	159	DQ49	M_B_DQ52
	173	DQ50	M_B_DQ54
	175	DQ51	M_B_DQ51
	158	DQ52	M_B_DQ48
	160	DQ53	M_B_DQ50
	174	DQ54	M_B_DQ55
	176	DQ55	M_B_DQ49
	179	DQ56	M_B_DQ57
	181	DQ57	M_B_DQ56
	189	DQ58	M_B_DQ59
	191	DQ59	M_B_DQ62
	180	DQ60	M_B_DQ61
	182	DQ61	M_B_DQ63
	192	DQ62	M_B_DQ60
	194	DQ63	M_B_DQ58

DDR2_DIMM_200P

+1.8V

Layout Note: Place these Caps near the SO-DIMM_1

C0816 2.2UF/6.3V — C0817 2.2UF/6.3V — C0818 2.2UF/6.3V — C0819 2.2UF/6.3V

+1.8V

Layout Note: Place these Caps near SO DIMM 1

C0807 0.1UF/10V — C0808 0.1UF/10V — C0809 0.1UF/10V — C0810 0.1UF/10V

+3VS

C0811 2.2UF/6.3V — C0812 0.1UF/10V

11 PM_EXTTS#1 — RX0802 N/A 0Ohm — PM_EXTTS#1_R

M_VREF_MCH

C0821 2.2UF/6.3V — C0820 0.1UF/10V

Layout Note: Place these Caps near SO DIMM 1

VREF -> 10/10 mils

J0801B

	112	VDD1	VSS16 18
	111	VDD2	VSS17 24
	117	VDD3	VSS18 41
	96	VDD4	VSS19 53
	95	VDD5	VSS20 42
	118	VDD6	VSS21 54
	81	VDD7	VSS22 59
	82	VDD8	VSS23 65
	87	VDD9	VSS24 60
	103	VDD10	VSS25 66
	88	VDD11	VSS26 127
	104	VDD12	VSS27 139
			VSS28 128
	199	VDDSPD	VSS29 145
			VSS30 165
	83	NC1	VSS31 171
	120	NC2	VSS32 172
	50	NC3	VSS33 177
	69	NC4	VSS34 187
	163	NCTEST	VSS35 178
			VSS36 190
	1	VREF	VSS37 9
			VSS38 21
	201	GND0	VSS39 33
	202	GND1	VSS40 155
			VSS41 34
	203	NP_NC1	VSS42 132
	204	NP_NC2	VSS43 144
			VSS44 156
	47	VSS1	VSS45 168
	133	VSS2	VSS46 2
	183	VSS3	VSS47 3
	77	VSS4	VSS48 15
	12	VSS5	VSS49 27
	48	VSS6	VSS50 39
	184	VSS7	VSS51 149
	78	VSS8	VSS52 161
	71	VSS9	VSS53 28
	72	VSS10	VSS54 40
	121	VSS11	VSS55 138
	122	VSS12	VSS56 150
	196	VSS13	VSS57 162
	193	VSS14	
	8	VSS15	

DDR2_DIMM_200P

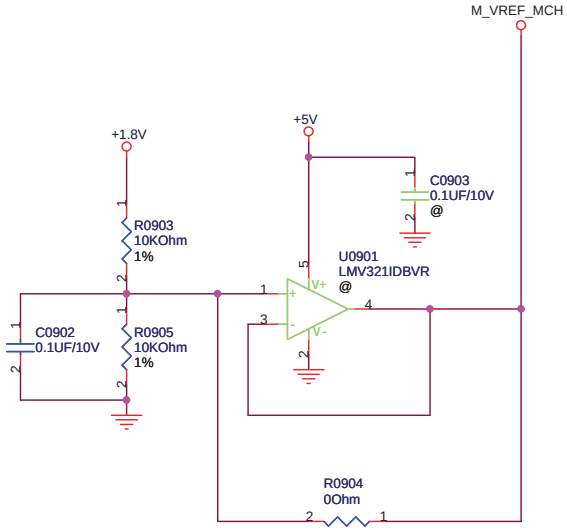
Title : DDR2 SO-DIMM_1		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 8 of 94	

+5V +5V 44,56,57,91

+1.8V +1.8V 7,8,11,13,83,91

M_VREF_MCH M_VREF_MCH 7,8,11

+0.9VS +0.9VS 83



M_A_A[0..13] 7,12

M_A_BS[0..2] 7,12

M_A_CAS# 7,12

M_A_RAS# 7,12

M_A_WE# 7,12

M_B_A[0..13] 8,12

M_B_BS[0..2] 8,12

M_B_CAS# 8,12

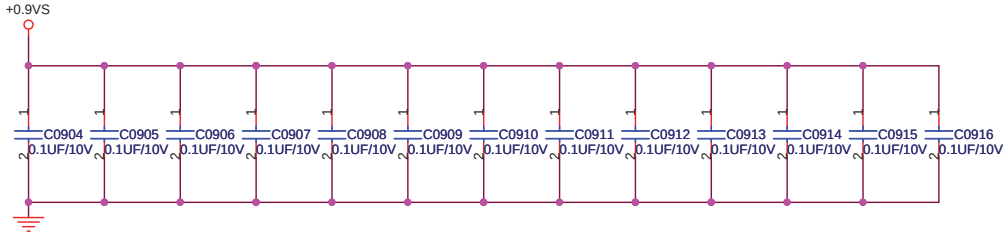
M_B_RAS# 8,12

M_B_WE# 8,12

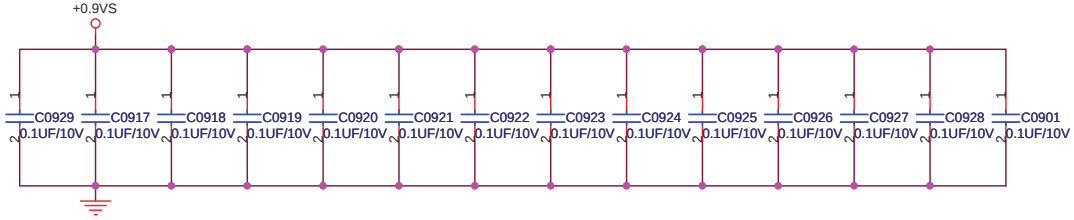
M_CS#[0..3] 7,8,11

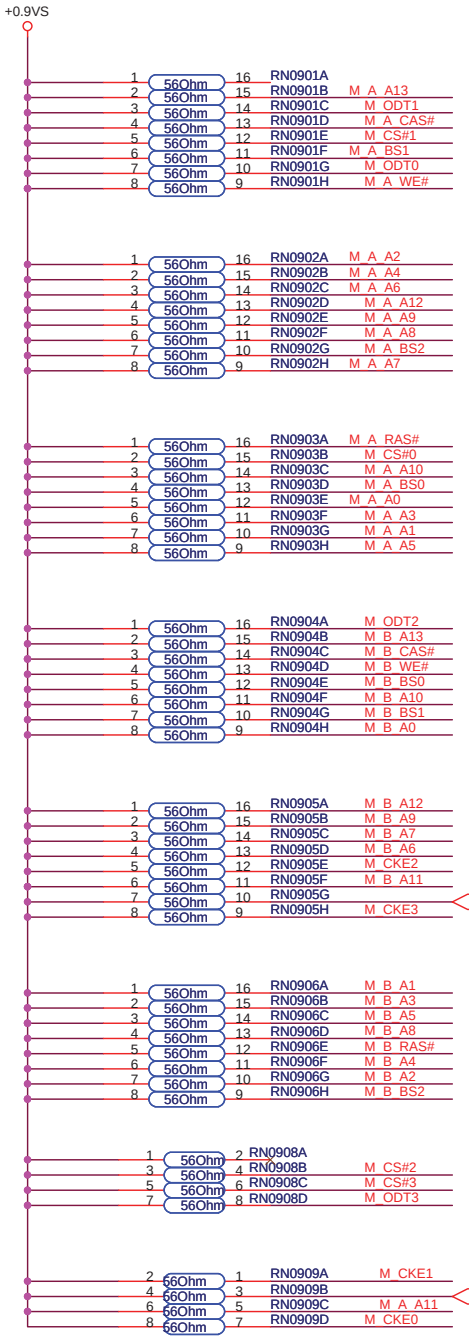
M_ODT[0..3] 7,8,11

M_CKE[0..3] 7,8,11



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





http://hobi-elektronika.net

ASUS	Title : DDR2 VREF	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 9 of 94	

+VCCP +VCCP 5,11,13,14,20,23,29,80,82

U1001A

R1001 24.9Ohm 1% H_RCOMP

+VCCP

R1004 221Ohm 1% H_SWING

R1005 100Ohm 1%

C1002 0.1UF/10V

T1001

R1008 1KOhm 1%

RX1006 0Ohm

C1001 0.1UF/10V @

R1007 2KOhm 1%

HVREF

CAP 0.1U within 100 mils from GMCH

HOST

H_D#0	F2	H_D#_0	
H_D#1	G8	H_D#_1	
H_D#2	F8	H_D#_2	
H_D#3	E6	H_D#_3	
H_D#4	G2	H_D#_4	
H_D#5	H6	H_D#_5	
H_D#6	H2	H_D#_6	
H_D#7	F6	H_D#_7	
H_D#8	D4	H_D#_8	
H_D#9	H3	H_D#_9	
H_D#10	M9	H_D#_10	
H_D#11	M11	H_D#_11	
H_D#12	J1	H_D#_12	
H_D#13	J2	H_D#_13	
H_D#14	N12	H_D#_14	
H_D#15	J6	H_D#_15	
H_D#16	P2	H_D#_16	
H_D#17	L2	H_D#_17	
H_D#18	R2	H_D#_18	
H_D#19	N9	H_D#_19	
H_D#20	L6	H_D#_20	
H_D#21	M5	H_D#_21	
H_D#22	J3	H_D#_22	
H_D#23	N2	H_D#_23	
H_D#24	R1	H_D#_24	
H_D#25	N5	H_D#_25	
H_D#26	N6	H_D#_26	
H_D#27	P13	H_D#_27	
H_D#28	N8	H_D#_28	
H_D#29	L7	H_D#_29	
H_D#30	N10	H_D#_30	
H_D#31	M3	H_D#_31	
H_D#32	Y3	H_D#_32	
H_D#33	AD14	H_D#_33	
H_D#34	Y6	H_D#_34	
H_D#35	Y10	H_D#_35	
H_D#36	Y12	H_D#_36	
H_D#37	Y14	H_D#_37	
H_D#38	Y7	H_D#_38	
H_D#39	W2	H_D#_39	
H_D#40	AA8	H_D#_40	
H_D#41	Y9	H_D#_41	
H_D#42	AA13	H_D#_42	
H_D#43	AA9	H_D#_43	
H_D#44	AA11	H_D#_44	
H_D#45	AD11	H_D#_45	
H_D#46	AD10	H_D#_46	
H_D#47	AD13	H_D#_47	
H_D#48	AE12	H_D#_48	
H_D#49	AE9	H_D#_49	
H_D#50	AA2	H_D#_50	
H_D#51	AD8	H_D#_51	
H_D#52	AA3	H_D#_52	
H_D#53	AD3	H_D#_53	
H_D#54	AD7	H_D#_54	
H_D#55	AE14	H_D#_55	
H_D#56	AF3	H_D#_56	
H_D#57	AC1	H_D#_57	
H_D#58	AE3	H_D#_58	
H_D#59	AC3	H_D#_59	
H_D#60	AE11	H_D#_60	
H_D#61	AE8	H_D#_61	
H_D#62	AG2	H_D#_62	
H_D#63	AD6	H_D#_63	
H_SWING	C5	H_SWING	
H_RCOMP	E3	H_RCOMP	
H_CPURST#	C12	H_CPURST#	
H_CPUSLP#	E11	H_CPUSLP#	
HVREF	A11	H_AVREF	
	B11	H_DVREF	

CANTIGA_CHIPSET

H_A#_3	A14	H_A#3
H_A#_4	C15	H_A#4
H_A#_5	F16	H_A#5
H_A#_6	H13	H_A#6
H_A#_7	C18	H_A#7
H_A#_8	M16	H_A#8
H_A#_9	J13	H_A#9
H_A#_10	P16	H_A#10
H_A#_11	R16	H_A#11
H_A#_12	N17	H_A#12
H_A#_13	M13	H_A#13
H_A#_14	E17	H_A#14
H_A#_15	P17	H_A#15
H_A#_16	F17	H_A#16
H_A#_17	G20	H_A#17
H_A#_18	B19	H_A#18
H_A#_19	J16	H_A#19
H_A#_20	E20	H_A#20
H_A#_21	H16	H_A#21
H_A#_22	J20	H_A#22
H_A#_23	L17	H_A#23
H_A#_24	A17	H_A#24
H_A#_25	B17	H_A#25
H_A#_26	L16	H_A#26
H_A#_27	C21	H_A#27
H_A#_28	J17	H_A#28
H_A#_29	H20	H_A#29
H_A#_30	B18	H_A#30
H_A#_31	K17	H_A#31
H_A#_32	B20	H_A#32
H_A#_33	F21	H_A#33
H_A#_34	K21	H_A#34
H_A#_35	L20	H_A#35
H_ADS#	H12	H_ADS# 3
H_ADSTB#_0	B16	H_ADSTB#0 3
H_ADSTB#_1	G17	H_ADSTB#1 3
H_BNR#	A9	H_BNR# 3
H_BPRI#	F11	H_BPRI# 3
H_BREQ#	G12	H_BR0# 3
H_DEFER#	E9	H_DEFER# 3
H_DBSY#	B10	H_DBSY# 3
HPLL_CLK	AH7	CLK_MCH_BCLK 29
HPLL_CLK#	AH6	CLK_MCH_BCLK# 29
H_DPWR#	J11	H_DPWR# 3
H_DRDY#	F9	H_DRDY# 3
H_HIT#	H9	H_HIT# 3
H_HITM#	E12	H_HITM# 3
H_LOCK#	H11	H_LOCK# 3
H_TRDY#	C9	H_TRDY# 3
H_DINV#_0	J8	H_DINV#0 3
H_DINV#_1	L3	H_DINV#1 3
H_DINV#_2	Y13	H_DINV#2 3
H_DINV#_3	Y1	H_DINV#3 3
H_DSTBN#_0	L10	H_DSTBN#0 3
H_DSTBN#_1	M7	H_DSTBN#1 3
H_DSTBN#_2	AA5	H_DSTBN#2 3
H_DSTBN#_3	AE6	H_DSTBN#3 3
H_DSTBP#_0	L9	H_DSTBP#0 3
H_DSTBP#_1	M8	H_DSTBP#1 3
H_DSTBP#_2	AA6	H_DSTBP#2 3
H_DSTBP#_3	AE5	H_DSTBP#3 3
H_REQ#_0	B15	H_REQ#0
H_REQ#_1	K13	H_REQ#1
H_REQ#_2	F13	H_REQ#2
H_REQ#_3	B13	H_REQ#3
H_REQ#_4	B14	H_REQ#4
H_RS#_0	B6	H_RS#0 3
H_RS#_1	F12	H_RS#1 3
H_RS#_2	C8	H_RS#2 3

3 H_A#[35:3] H_A#[35:3]

3 H_REQ#[4:0] H_REQ#[4:0]

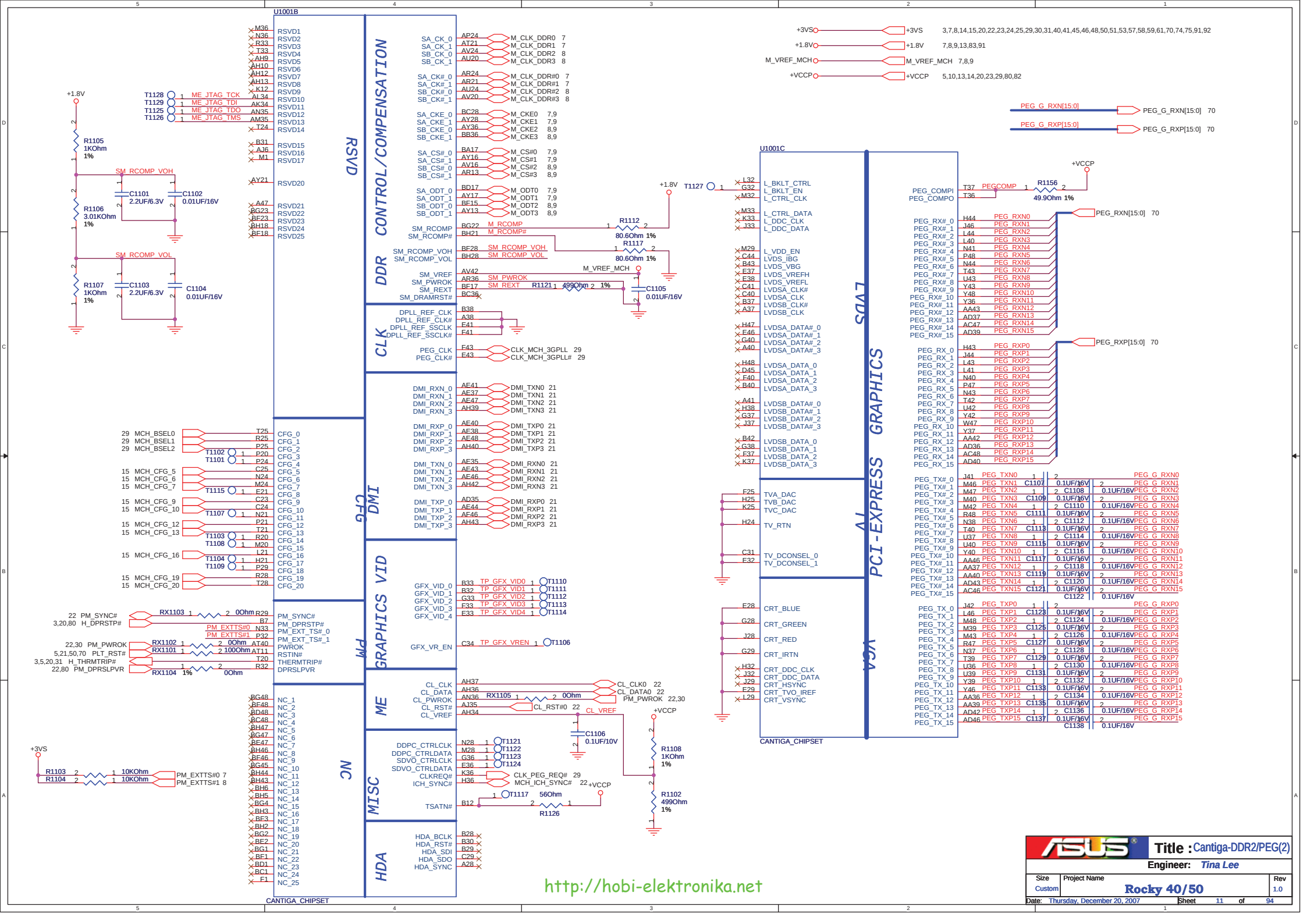
3 H_D#[63:0] H_D#[63:0]

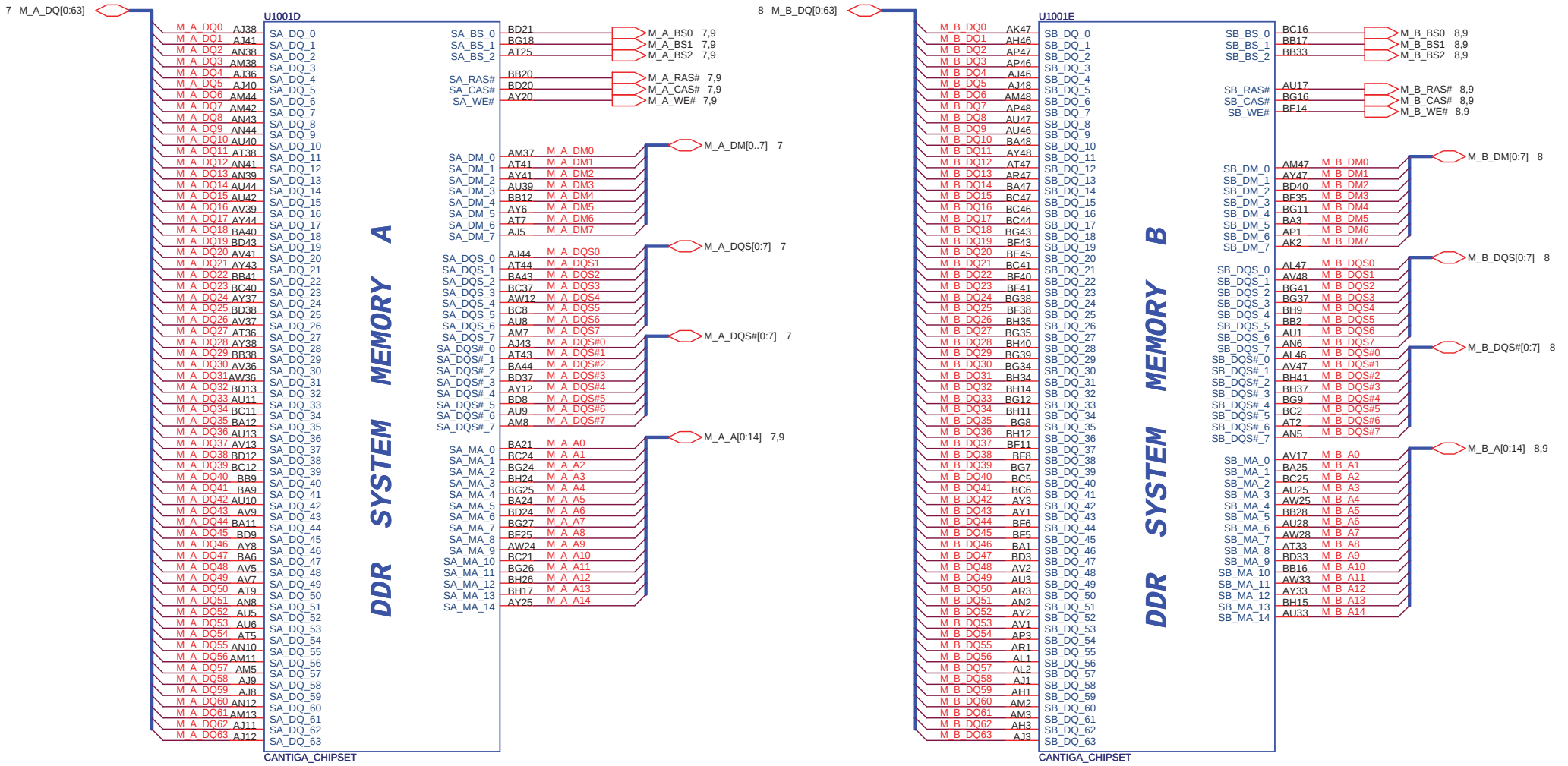
Title : Cantiga -- CPU (1)

Engineer: Tina Lee

Size	Project Name	Rev
Custom	Rocky 40/50	1.0

Date: Thursday, December 20, 2007 Sheet 10 of 94


U1001B
RSVD
CONTROL/COMPENSATION
DDR
CLK
DMI
CFG
VID
GRAPHICS
PM
ME
MISC
HDA
NC
U1001C
LVDS
GRAPHICS
PCI-EXPRESS
TV
VGA
CANTIGA_CHIPSET
Title : Cantiga-DDR2/PEG(2)
Engineer: Tina Lee
Size
Custom
Project Name
Rocky 40/50
Rev
1.0
Date: Thursday, December 20, 2007
Sheet 11 of 94
http://hobi-elektronika.net

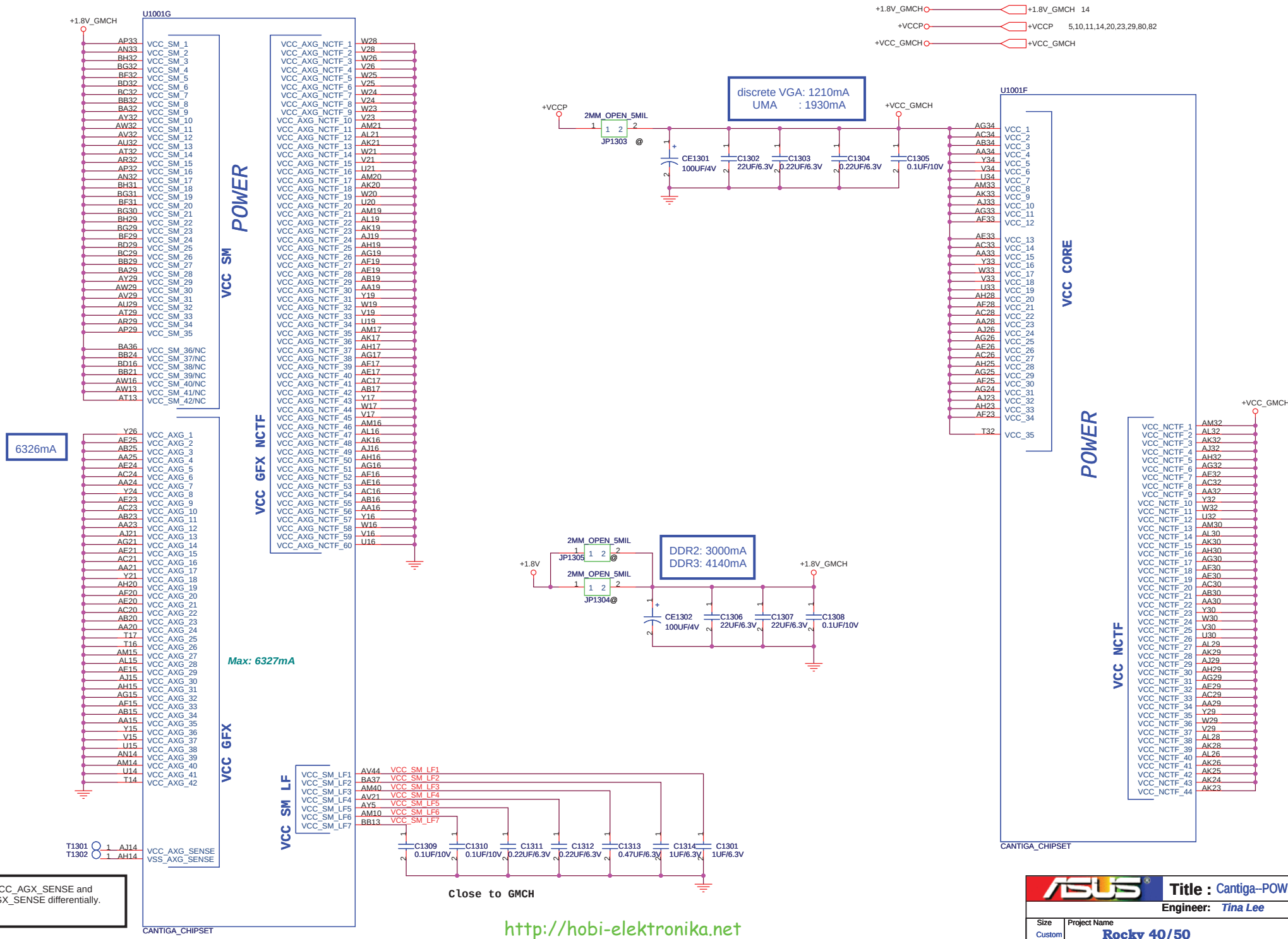


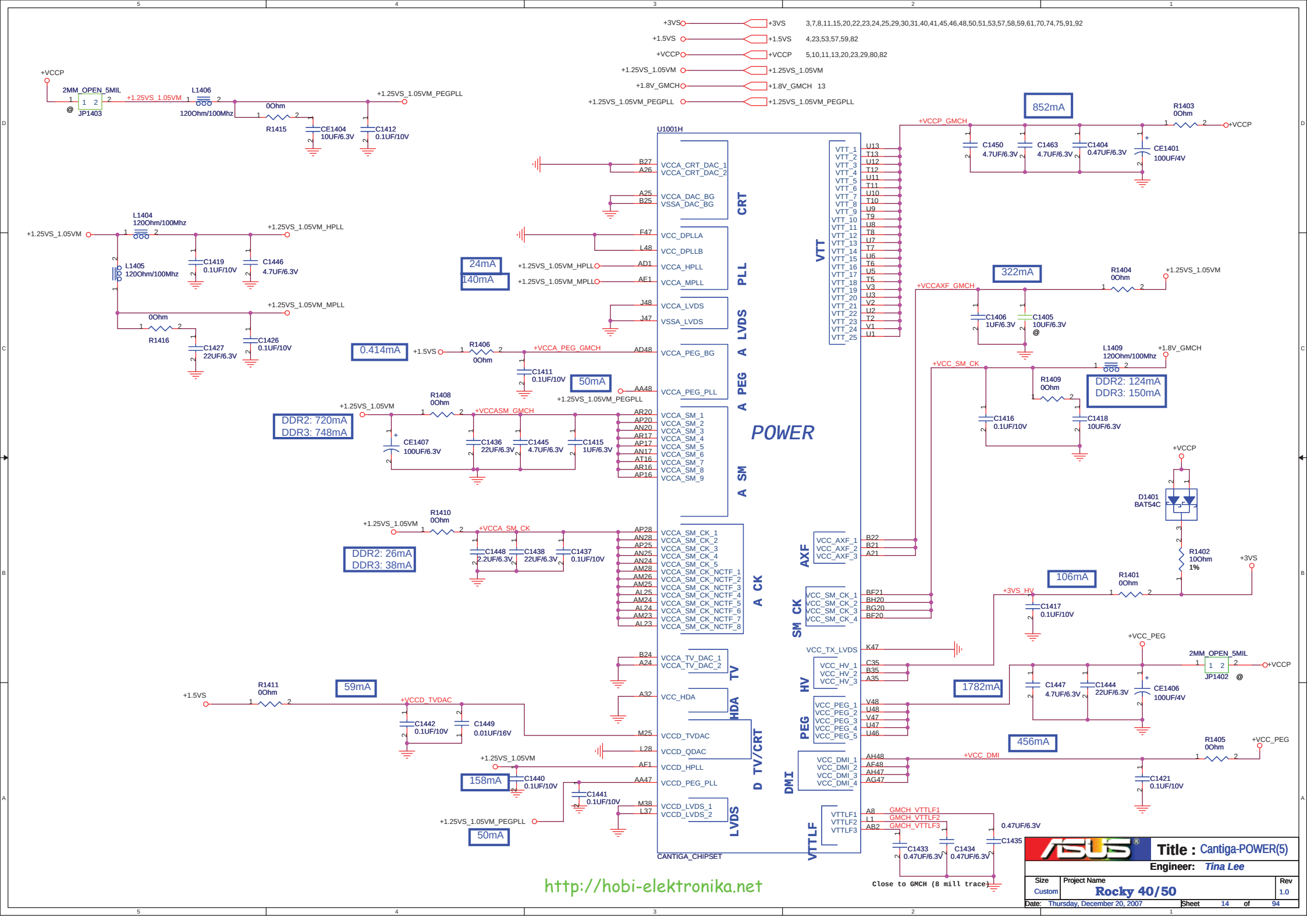
Title : Cantiga--DDR3 (3)

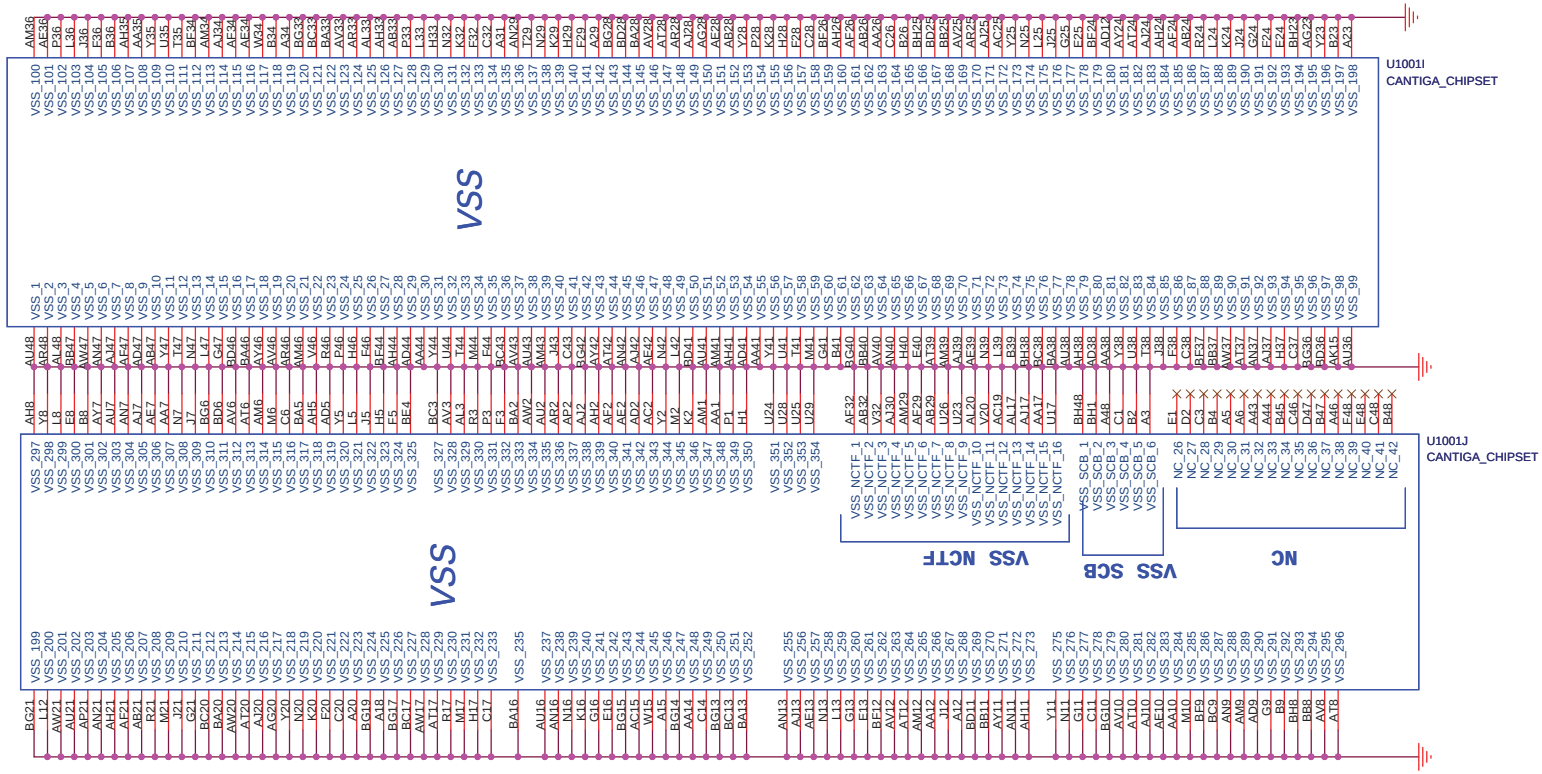
Engineer: Tina Lee

Size	Project Name	Rev
Custom	Rocky 40/50	1.0

Date: Thursday, December 20, 2007 Sheet 12 of 94


+1.8V_GMCH
U1001G
VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35
VCC_SM_36/NC VCC_SM_37/NC VCC_SM_38/NC VCC_SM_39/NC VCC_SM_40/NC VCC_SM_41/NC VCC_SM_42/NC
VCC SM POWER
VCC_AXG_NCTF_1 VCC_AXG_NCTF_2 VCC_AXG_NCTF_3 VCC_AXG_NCTF_4 VCC_AXG_NCTF_5 VCC_AXG_NCTF_6 VCC_AXG_NCTF_7 VCC_AXG_NCTF_8 VCC_AXG_NCTF_9 VCC_AXG_NCTF_10 VCC_AXG_NCTF_11 VCC_AXG_NCTF_12 VCC_AXG_NCTF_13 VCC_AXG_NCTF_14 VCC_AXG_NCTF_15 VCC_AXG_NCTF_16 VCC_AXG_NCTF_17 VCC_AXG_NCTF_18 VCC_AXG_NCTF_19 VCC_AXG_NCTF_20 VCC_AXG_NCTF_21 VCC_AXG_NCTF_22 VCC_AXG_NCTF_23 VCC_AXG_NCTF_24 VCC_AXG_NCTF_25 VCC_AXG_NCTF_26 VCC_AXG_NCTF_27 VCC_AXG_NCTF_28 VCC_AXG_NCTF_29 VCC_AXG_NCTF_30 VCC_AXG_NCTF_31 VCC_AXG_NCTF_32 VCC_AXG_NCTF_33 VCC_AXG_NCTF_34 VCC_AXG_NCTF_35 VCC_AXG_NCTF_36 VCC_AXG_NCTF_37 VCC_AXG_NCTF_38 VCC_AXG_NCTF_39 VCC_AXG_NCTF_40 VCC_AXG_NCTF_41 VCC_AXG_NCTF_42 VCC_AXG_NCTF_43 VCC_AXG_NCTF_44 VCC_AXG_NCTF_45 VCC_AXG_NCTF_46 VCC_AXG_NCTF_47 VCC_AXG_NCTF_48 VCC_AXG_NCTF_49 VCC_AXG_NCTF_50 VCC_AXG_NCTF_51 VCC_AXG_NCTF_52 VCC_AXG_NCTF_53 VCC_AXG_NCTF_54 VCC_AXG_NCTF_55 VCC_AXG_NCTF_56 VCC_AXG_NCTF_57 VCC_AXG_NCTF_58 VCC_AXG_NCTF_59 VCC_AXG_NCTF_60
VCC GFX NCTF
6326mA
VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42
Max: 6327mA
VCC GFX
T1301 T1302
VCC_AXG_SENSE VSS_AXG_SENSE
Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.
CANTIGA_CHIPSET
VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7
VCC SM LF
C1309 0.1UF/10V C1310 0.1UF/10V C1311 0.22UF/6.3V C1312 0.22UF/6.3V C1313 0.47UF/6.3V C1314 1UF/6.3V C1301 1UF/6.3V
Close to GMCH
+1.8V_GMCH +1.8V_GMCH 14
+VCCP +VCCP 5,10,11,14,20,23,29,80,82
+VCC_GMCH +VCC_GMCH
discrete VGA: 1210mA
UMA : 1930mA
+VCCP
2MM_OPEN_5MIL JP1303 @
CE1301 100UF/4V C1302 22UF/6.3V C1303 0.22UF/6.3V C1304 0.22UF/6.3V C1305 0.1UF/10V
+VCC_GMCH
U1001F
AG34 AC34 AB34 AA34 Y34 V34 U34 AM33 AK33 AJ33 AG33 AF33 AE33 AC33 AA33 Y33 W33 V33 U33 AH28 AF28 AC28 AA28 AJ26 AG26 AE26 AC26 AH25 AG25 AE25 AG24 AJ23 AH23 AF23 T32
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35
VCC CORE
DDR2: 3000mA
DDR3: 4140mA
+1.8V
2MM_OPEN_5MIL JP1305 @
2MM_OPEN_5MIL JP1304@
+1.8V_GMCH
CE1302 100UF/4V C1306 22UF/6.3V C1307 22UF/6.3V C1308 0.1UF/10V
+VCC_GMCH
VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38 VCC_NCTF_39 VCC_NCTF_40 VCC_NCTF_41 VCC_NCTF_42 VCC_NCTF_43 VCC_NCTF_44
AM32 AL32 AK32 AJ32 AH32 AG32 AF32 AC32 AA32 Y32 W32 U32 AM30 AL30 AK30 AH30 AG30 AF30 AE30 AC30 AB30 AA30 Y30 W30 V30 U30 AL29 AK29 AJ29 AH29 AG29 AE29 AC29 AA29 Y29 W29 V29 AL28 AK28 AL26 AK26 AK25 AK24 AK23
VCC NCTF
POWER
CANTIGA_CHIPSET
http://hobi-elektronika.net
Title : Cantiga--POWER (4)
Engineer: Tina Lee
Size Custom
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 13 of 94


+3VS +3VS 3,7,8,11,15,20,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92
+1.5VS +1.5VS 4,23,53,57,59,82
+VCCP +VCCP 5,10,11,13,20,23,29,80,82
+1.25VS_1.05VM +1.25VS_1.05VM
+1.8V_GMCH +1.8V_GMCH 13
+1.25VS_1.05VM_PEGPLL +1.25VS_1.05VM_PEGPLL
POWER
U1001H
CANTIGA_CHIPSET
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
852mA
322mA
106mA
1782mA
456mA
24mA
140mA
0.414mA
50mA
DDR2: 720mA
DDR3: 748mA
DDR2: 26mA
DDR3: 38mA
59mA
158mA
50mA
DDR2: 124mA
DDR3: 150mA
Close to GMCH (8 mill trace)
http://hobi-elektronika.net
Title : Cantiga-POWER(5)
Engineer: Tina Lee
Size Custom
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 14 of 94



+3VS +3VS 3,7,8,11,14,20,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53

11 MCH_CFG_5 — R1509 2.21KOhm @ 1%

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

11 MCH_CFG_6 — R1514 2.21KOhm @ 1%

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

11 MCH_CFG_7 — R1511 2.21KOhm @ 1%

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

11 MCH_CFG_9 — R1512 2.21KOhm @ 1%

CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

11 MCH_CFG_16 — R1507 2.21KOhm @ 1%

CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable

11 MCH_CFG_10 — R1508 2.21KOhm @ 1%

CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

11 MCH_CFG_12 — R1513 2.21KOhm @ 1%

11 MCH_CFG_13 — R1510 2.21KOhm @ 1%

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

+3VS — R1503 4.02KOhm @ 1% — 11 MCH_CFG_19

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

+3VS — R1506 4.02KOhm @ 1% — 11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

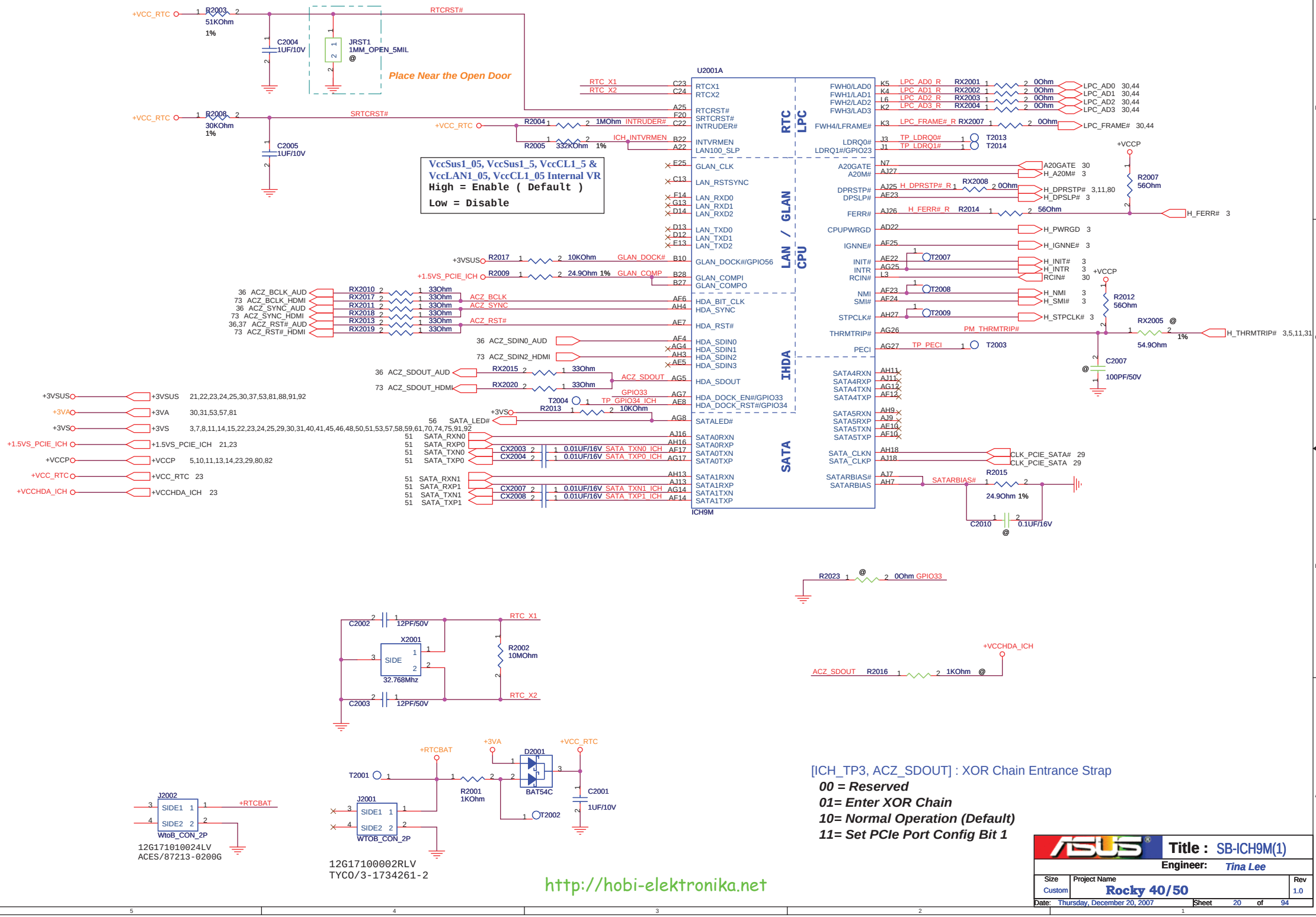
ASUS	Title : Cantiga-GND	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 15 of 94	

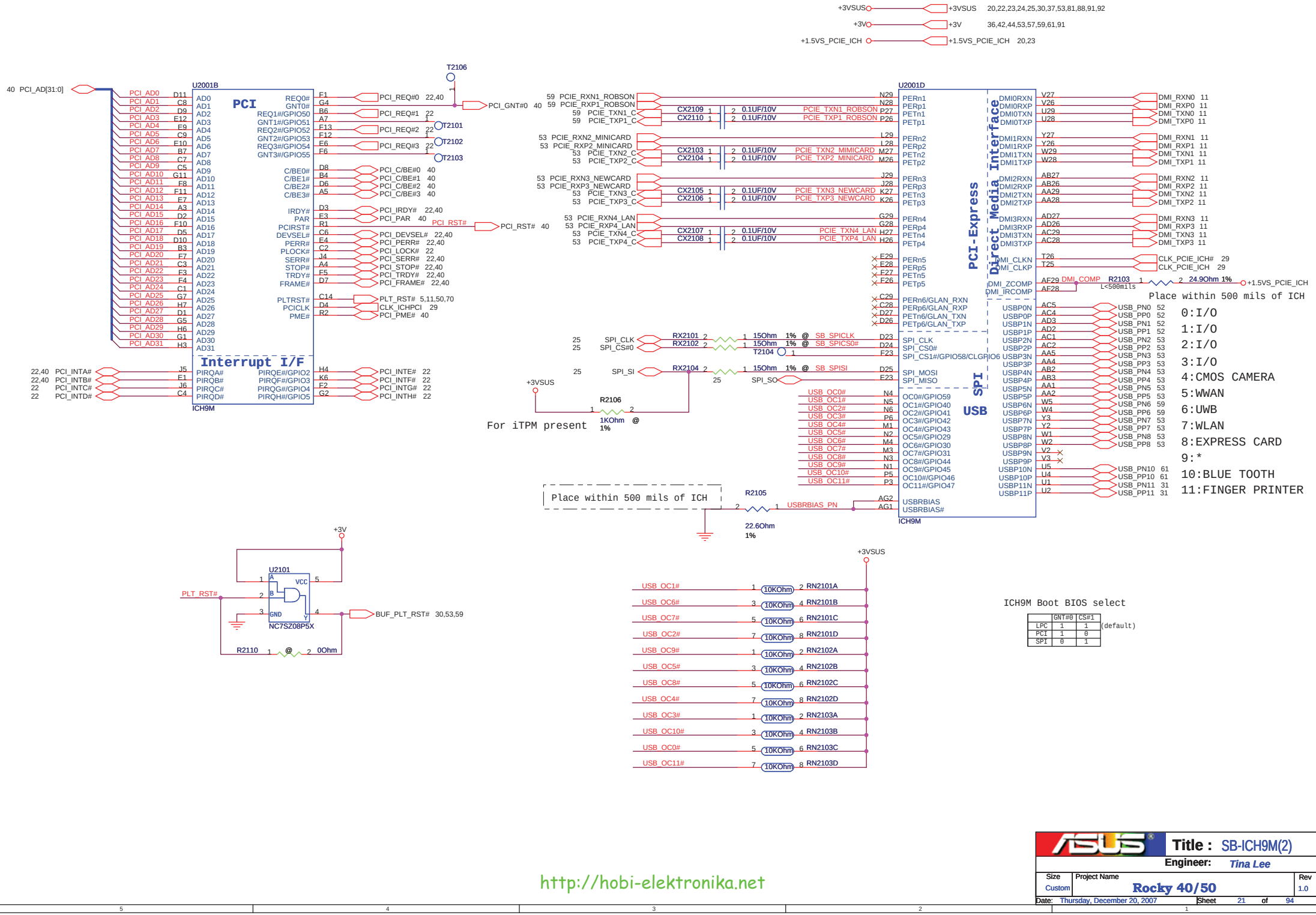
Title :	***
Engineer:	Tina Lee
Size: A4	Project Name: Rocky 40/50
Rev: 1.0	
Date: Monday, December 17, 2007	Sheet 16 of 94

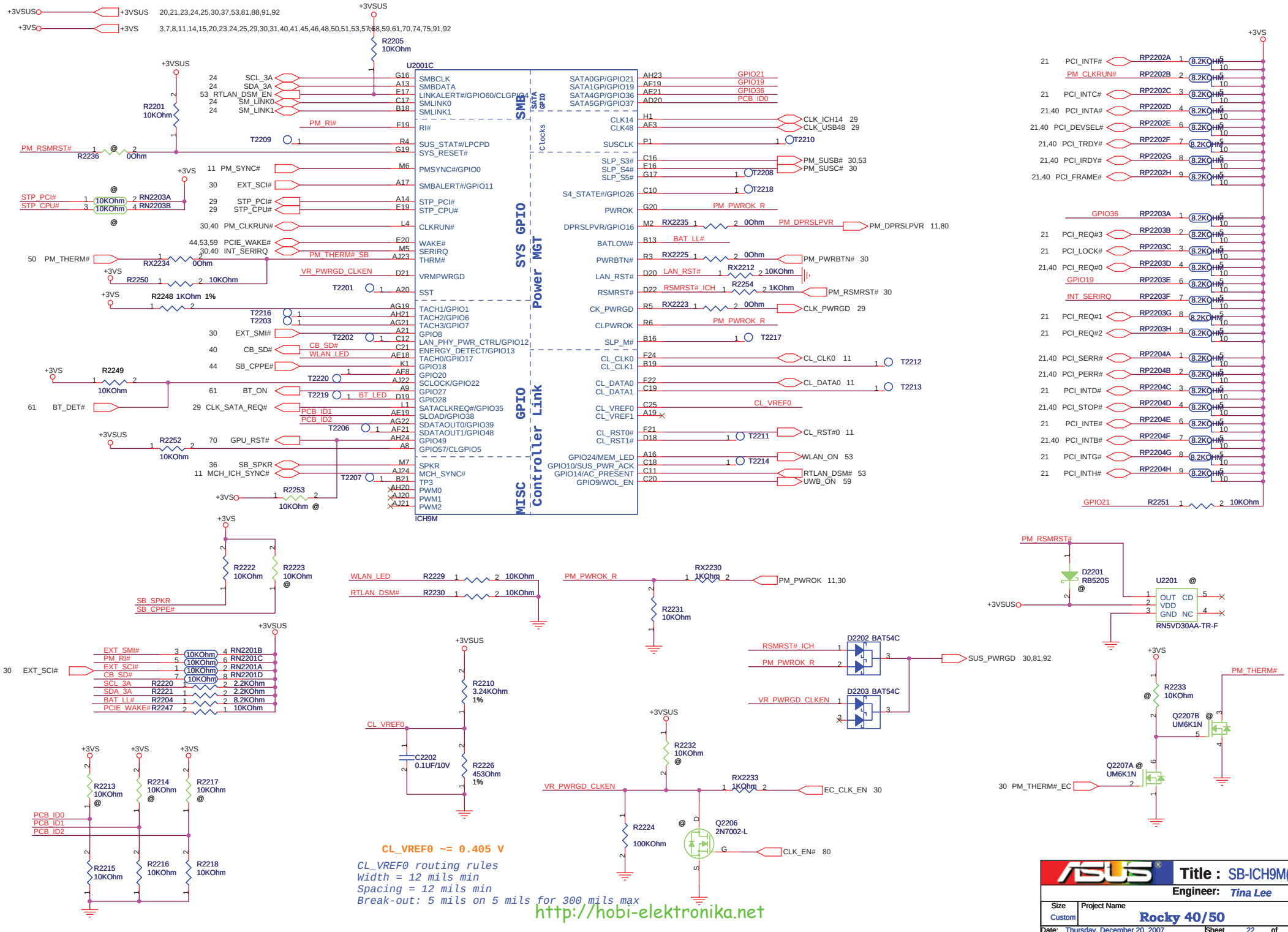
Title : ***		
Engineer: Tina Lee		
Size: A4	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 17 of 94	

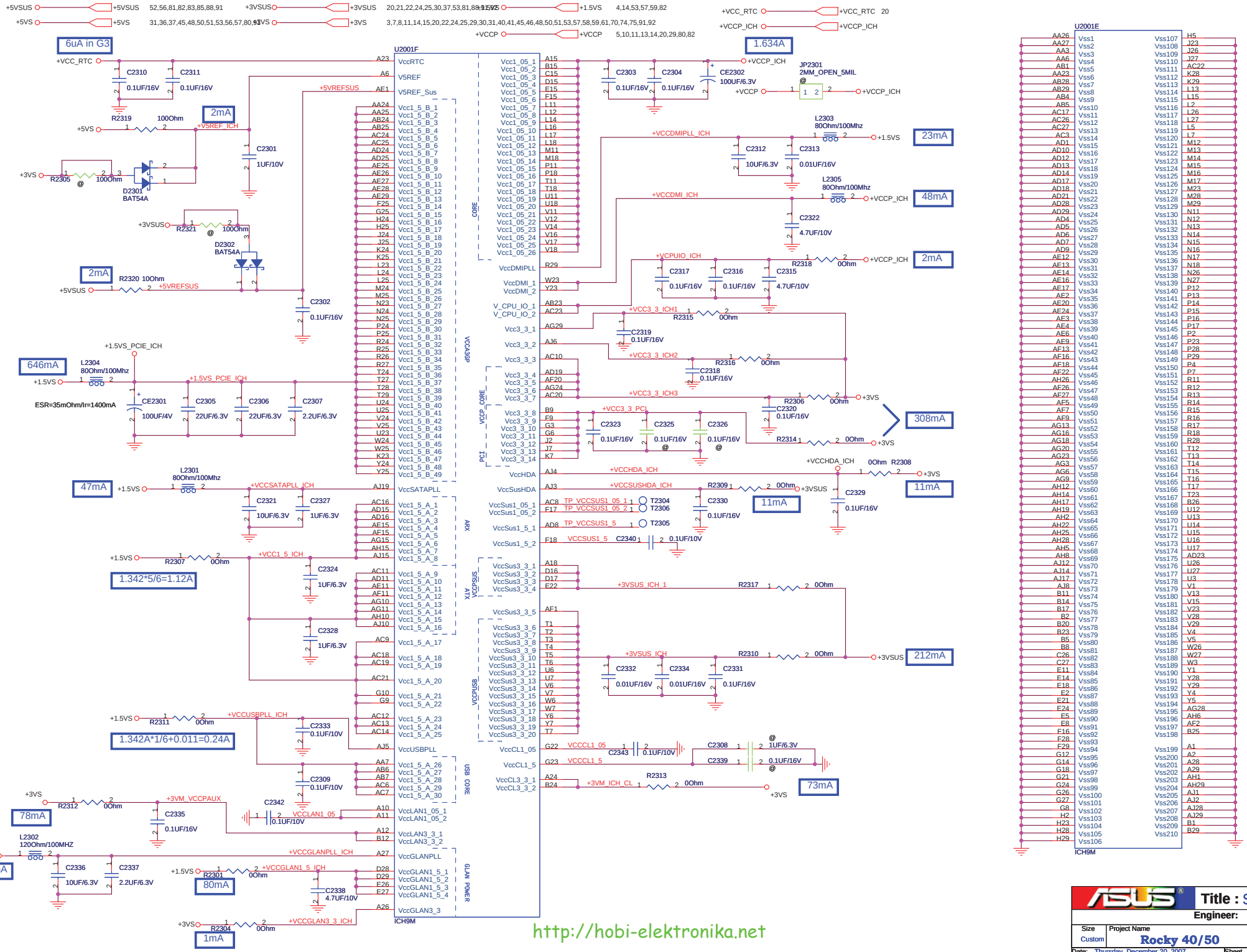
Title : ***		
Engineer: Tina Lee		
Size: A4	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 18 of 94	

Title : ***		
Engineer: Tina Lee		
Size: A4	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 19 of 94	


Place Near the Open Door
VccSus1_05, VccSus1_5, VccCL1_5 & VccLAN1_05, VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
U2001A
ICH9M
RTC
LPC
GLAN
LAN / CPU
IHDA
SATA
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
12G171010024LV
ACES/87213-0200G
12G17100002RLV
TYCO/3-1734261-2
http://hobi-elektronika.net
Title : SB-ICH9M(1)
Engineer: Tina Lee
Size Custom
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 20 of 94

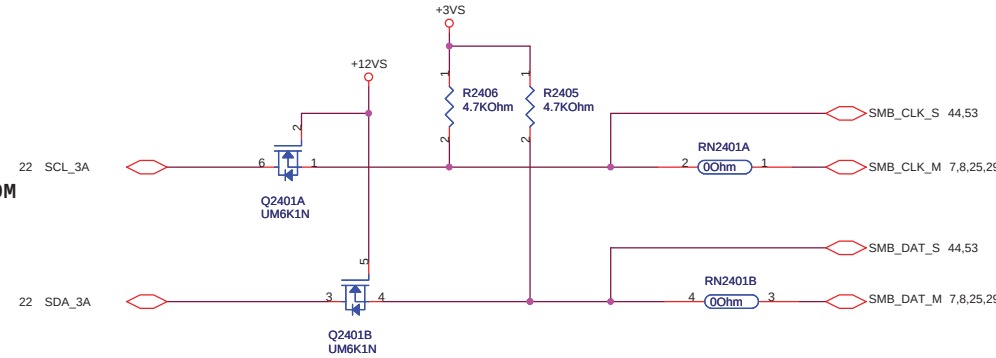

+3VSUS +3VSUS 20,22,23,24,25,30,37,53,81,88,91,92
+3V +3V 36,42,44,53,57,59,61,91
+1.5VS_PCIE_ICH +1.5VS_PCIE_ICH 20,23
U2001B
PCI
Interrupt I/F
ICH9M
U2001D
PCI-Express
Direct Media Interface
SPI
USB
ICH9M
T2106
T2101
T2102
T2103
Place within 500 mils of ICH
For iTPM present
R2106 1KOhm @ 1%
R2105 22.6Ohm 1%
R2103 24.9Ohm 1%
0:I/O
1:I/O
2:I/O
3:I/O
4:CMOS CAMERA
5:WWAN
6:UWB
7:WLAN
8:EXPRESS CARD
9:*
10:BLUE TOOTH
11:FINGER PRINTER
U2101
NC7SZ08P5X
R2110 @ 0Ohm
ICH9M Boot BIOS select
LPC 1 1 (default)
PCI 1 0
SPI 0 1
http://hobi-elektronika.net
Title : SB-ICH9M(2)
Engineer: Tina Lee
Size Custom
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 21 of 94


+3VSUS
+3VS
20,21,23,24,25,30,37,53,81,88,91,92
3,7,8,11,14,15,20,23,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92
R2205 10KOhm
U2001C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
SMB
SCL_3A
SDA_3A
RTLAN_DSM_EN
SM_LINK0
SM_LINK1
R2201 10KOhm
PM_RI#
T2209
PM_RSMRST#
R2236 0Ohm
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PM_SYNC#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
EXT_SCI#
STP_PCI#
STP_CPU#
RN2203A
RN2203B
CLKRUN#
PCIE_WAKE#
INT_SERIRQ
WAKE#
SERIRQ
THRM#
PM_THERM#
RX2234 0Ohm
PM_THERM#_SB
SYS GPIO
R2250 10KOhm
VR_PWRGD_CLKEN
VRMPWRGD
T2201
SST
R2248 1KOhm 1%
Power MGT
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
T2216
T2203
EXT_SMI#
T2202
CB_SD#
WLAN_LED
SB_CPPE#
T2220
BT_ON
T2219
BT_LED
BT_DET#
CLK_SATA_REQ#
PCB_ID1
PCB_ID2
T2206
R2249 10KOhm
R2252 10KOhm
GPU_RST#
GPIO
Controller Link
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
MISC
SB_SPKR
MCH_ICH_SYNC#
T2207
R2253 10KOhm @
ICH9M
SATA GPIO
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
GPIO21
GPIO19
GPIO36
PCB_ID0
I/C locks
CLK14
CLK48
SUSCLK
CLK_ICH14 29
CLK_USB48 29
T2210
SLP_S3#
SLP_S4#
SLP_S5#
PM_SUSB# 30,53
PM_SUSC# 30
T2208
S4_STATE#/GPIO26
T2218
PWROK
PM_PWROK_R
DPRSLPVR/GPIO16
RX2235 0Ohm
PM_DPRSLPVR
PM_DPRSLPVR 11,80
BATLOW#
BAT_LL#
PWRBTN#
RX2225 0Ohm
PM_PWRBTN# 30
LAN_RST#
RX2212 10KOhm
RSMRST#
RSMRST# ICH
R2254 1KOhm
PM_RSMRST# 30
CK_PWRGD
RX2223 0Ohm
CLK_PWRGD 29
CLPWROK
SLP_M#
T2217
CL_CLK0
CL_CLK1
CL_CLK0 11
T2212
CL_DATA0
CL_DATA1
CL_DATA0 11
T2213
CL_VREF0
CL_VREF1
CL_VREF0
CL_RST0#
CL_RST1#
T2211
CL_RST#0 11
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
T2214
WLAN_ON 53
RTLAN_DSM# 53
UWB_ON 59
PCI_INTF#
PM_CLKRUN#
PCI_INTC#
PCI_INTA#
PCI_DEVSEL#
PCI_TRDY#
PCI_IRDY#
PCI_FRAME#
RP2202A
RP2202B
RP2202C
RP2202D
RP2202E
RP2202F
RP2202G
RP2202H
8.2KOHM
PCI_REQ#3
PCI_LOCK#
PCI_REQ#0
RP2203A
RP2203B
RP2203C
RP2203D
RP2203E
RP2203F
RP2203G
RP2203H
PCI_REQ#1
PCI_REQ#2
PCI_SERR#
PCI_PERR#
PCI_INTD#
PCI_STOP#
PCI_INTE#
PCI_INTB#
PCI_INTG#
PCI_INTH#
RP2204A
RP2204B
RP2204C
RP2204D
RP2204E
RP2204F
RP2204G
RP2204H
R2251 10KOhm
R2222 10KOhm
R2223 10KOhm @
WLAN_LED
RTLAN_DSM#
R2229 10KOhm
R2230 10KOhm
PM_PWROK_R
RX2230 1KOhm
PM_PWROK 11,30
R2231 10KOhm
RN2201B
RN2201C
RN2201A
RN2201D
2.2KOhm
8.2KOHm
R2210 3.24KOhm 1%
R2226 453Ohm 1%
C2202 0.1UF/10V
CL_VREF0
CL_VREF0 ~= 0.405 V
R2232 10KOhm @
RX2233 1KOhm
EC_CLK_EN 30
R2224 100KOhm
Q2206 2N7002-L
CLK_EN# 80
D2202 BAT54C
D2203 BAT54C
RSMRST# ICH
PM_PWROK_R
VR_PWRGD_CLKEN
SUS_PWRGD 30,81,92
D2201 RB520S
U2201
OUT CD
VDD
GND NC
RN5VD30AA-TR-F
R2233 10KOhm
Q2207B UM6K1N
Q2207A @ UM6K1N
PM_THERM#
30 PM_THERM#_EC
R2213 10KOhm @
R2214 10KOhm @
R2217 10KOhm @
R2215 10KOhm
R2216 10KOhm
R2218 10KOhm
PCB_ID0
PCB_ID1
PCB_ID2
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
http://hobi-elektronika.net
Title : SB-ICH9M(3)
Engineer: Tina Lee
Size Custom
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 22 of 94


+5VSUS 52,56,81,82,83,85,88,91
+5VS 31,36,37,45,48,50,51,53,56,57,80,91
+3VSUS 20,21,22,24,25,30,37,53,81,88,91,95
+3VS 3,7,8,11,14,15,20,22,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92
+1.5VS 4,14,53,57,59,82
+VCCP 5,10,11,13,14,20,29,80,82
+VCC_RTC 20
+VCCP_ICH
U2001F
U2001E
ICH9M
6uA in G3
1.634A
2mA
23mA
48mA
646mA
308mA
47mA
11mA
1.342*5/6=1.12A
212mA
1.342A*1/6+0.011=0.24A
78mA
73mA
80mA
1mA
http://hobi-elektronika.net
Title : SB-ICH9M(PWR)
Engineer: Tina Lee
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 23 of 94

ICH9-M

+12VSUS	+12VSUS	52,81,91
+12VS	+12VS	45,91
+3VA	+3VA	20,30,31,53,57,81
+3VSUS	+3VSUS	20,21,22,23,25,30,37,53,81,88,91,92
+3VS	+3VS	3,7,8,11,14,15,20,22,23,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92



ICH9M

NEWCARD,
SMALL BOARD(WLAN)

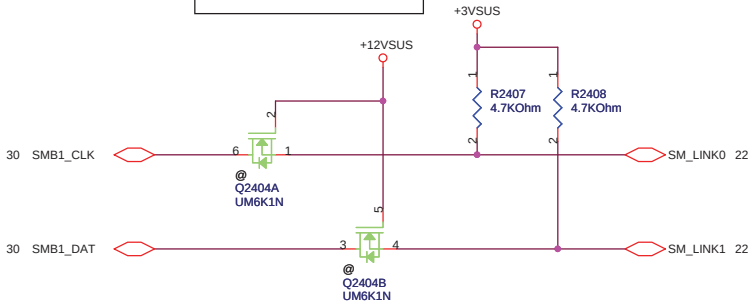
CLOCK GEN
SO-DIMM0, SO-DIMM1

NEWCARD,
SMALL BOARD(WLAN)

CLOCK GEN
SO-DIMM0, SO-DIMM1

EC

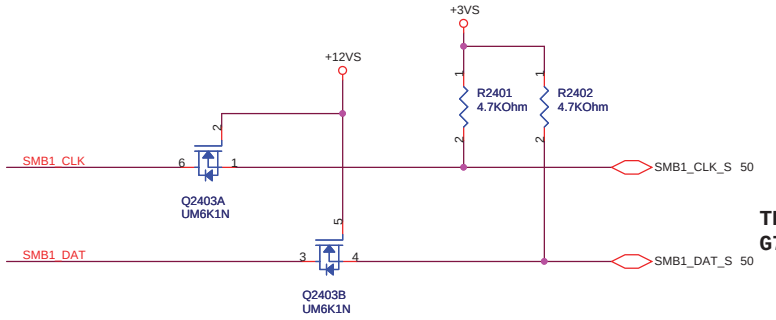
Don't support iAMT
Remove ME-EC SMBus.



EC

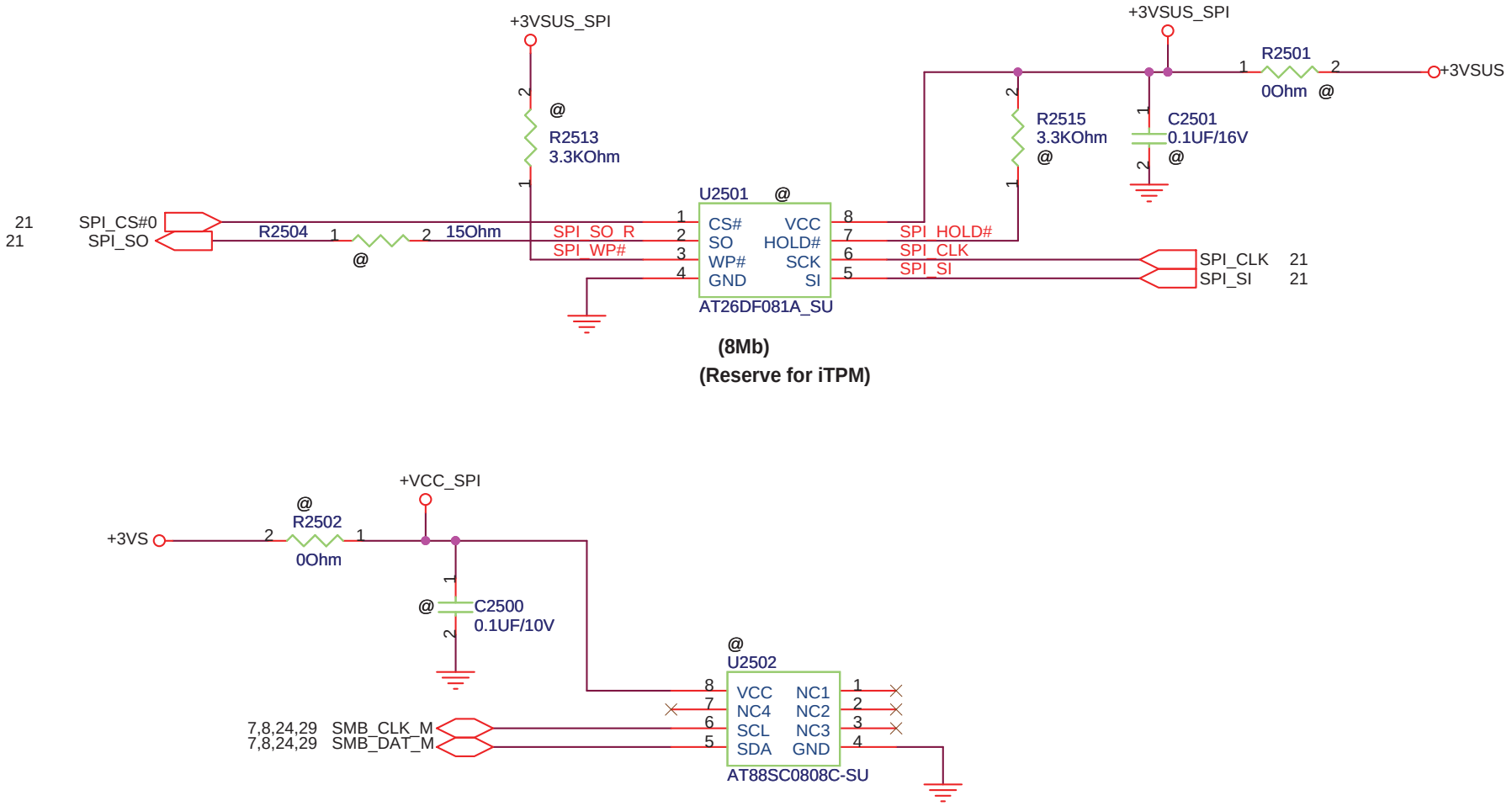
SB

EC



THERMAL IC
G781, G781-1

Title : ICH9M-Other		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 24 of 94	



http://hobi-elektronika.net

Title : SPI ROM		
Engineer: *Tina Lee*		
Size: Custom	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 25 of 94	

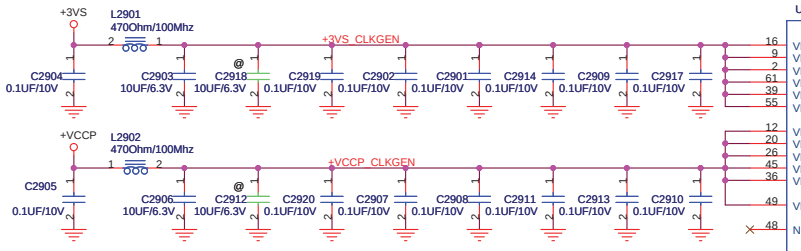
Title :		
Engineer: *Tina Lee*		
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 26 of 94	

ASUS	Title :	
	Engineer: *Tina Lee*	
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 27 of 94	

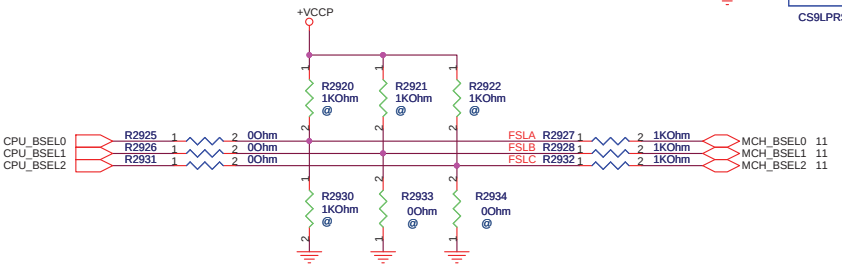
Title :	
Engineer:	*Tina Lee*
Size: A4	Project Name: **Rocky 40/50**
Rev: 1.0	
Date: Monday, December 17, 2007	Sheet 28 of 94

+VCCP +VCCP 5,10,11,13,14,20,23,80,82

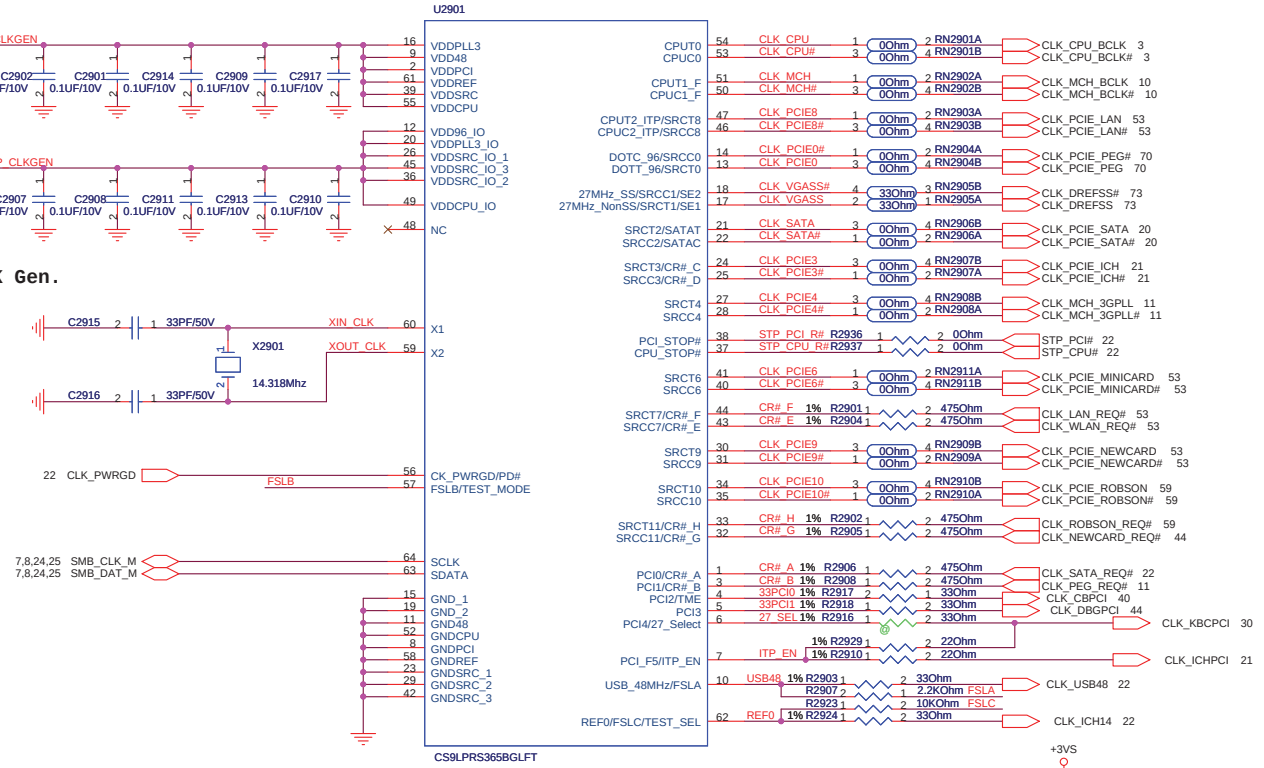
+3VS +3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92

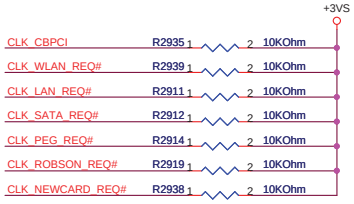


C2917, C2918, C2919 near CLK Gen.

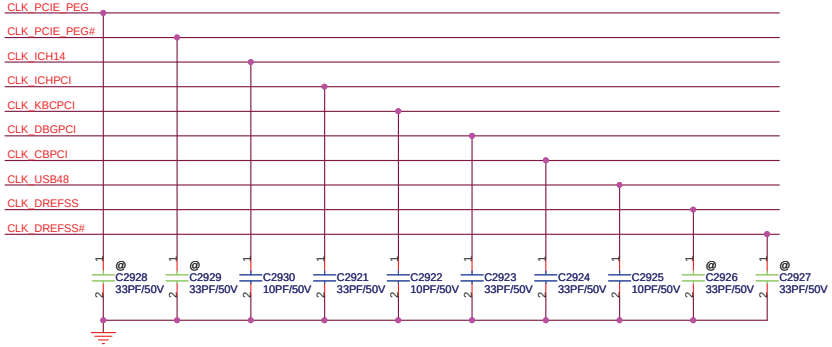


		FSLC	FSLB	FSLA
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0





C2921, C2922, C2923, C2924, C2925, C2926,
C2927, C2928, C2929, C2930 near CLK Gen.

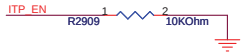


CR#_A	0 = SRC 0 1 = SRC 2 SATA
CR#_B	0 = SRC 1 1 = SRC 4 MCH
CR#_C	0 = SRC 0 1 = SRC 2
CR#_D	0 = SRC 1 1 = SRC 4
CR#_E	SRC 6 WLAN
CR#_F	SRC 8 LAN
CR#_G	SRC 9 New Card
CR#_H	SRC 10 Robson

Latched Input Select

0 = SRC 8
1 = CPU_ITP CLK

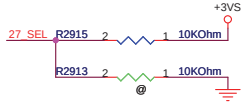
Decide pin 46,47



27_Select =0,
pin#13/14=DOT96;
pin#17/18=LCD_SST;

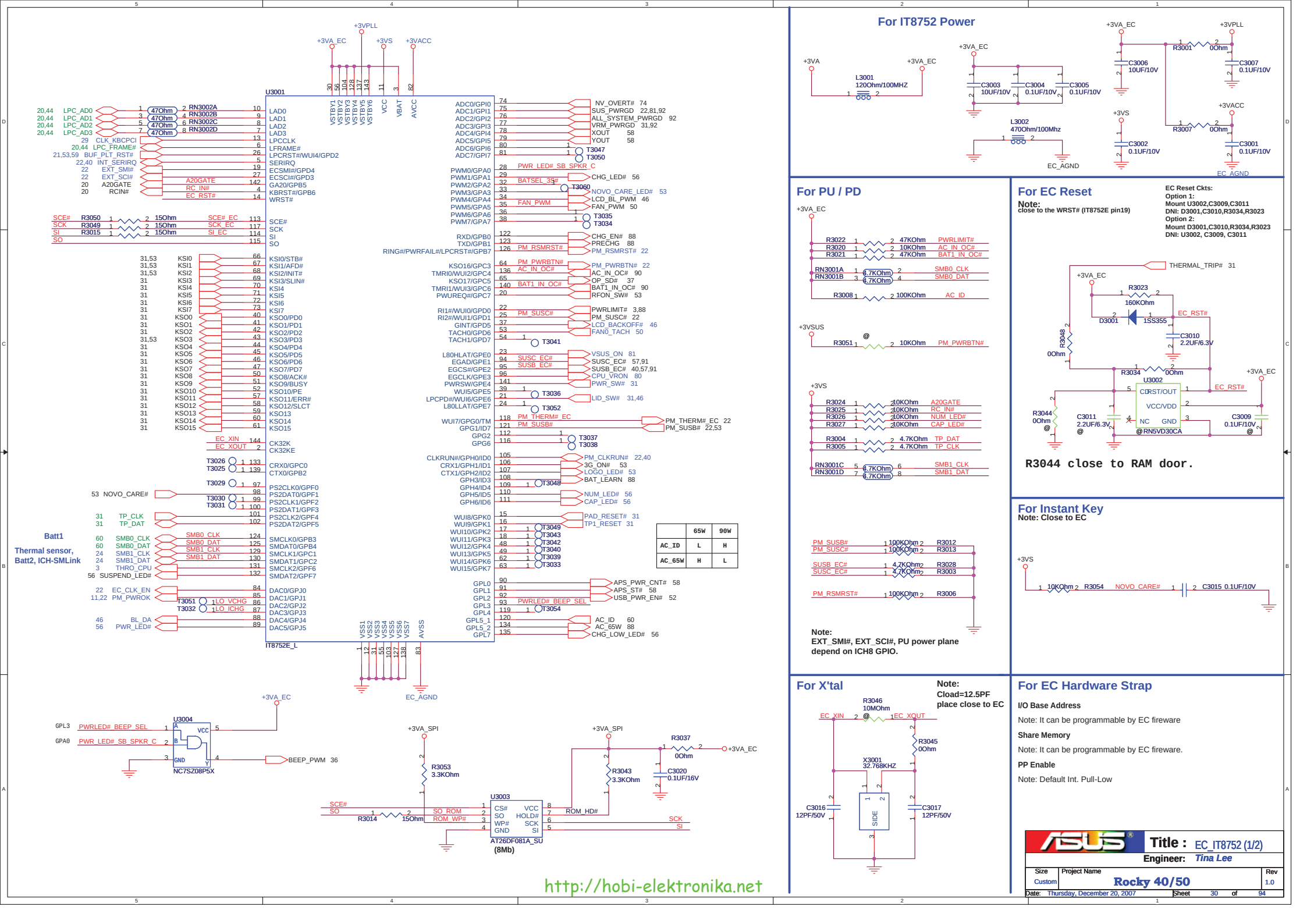
Decide pin 13/14,17/18

27_Select =1,
pin#13/14=SRC0;
pin#17/18=27MHz non-spread SE clock;



For GM/GL, need to PD for 96MHz output.
For PM, need to PU for 27MHz output.

Title : ICS9LPR365
Engineer: Tina Lee
Size: Custom
Project Name: Rocky 40/50
Rev: 1.0
Date: Thursday, December 20, 2007
Sheet 29 of 94



For IT8752 Power

For PU / PD

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R3044 close to RAM door.

For Instant Key

Note: Close to EC

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

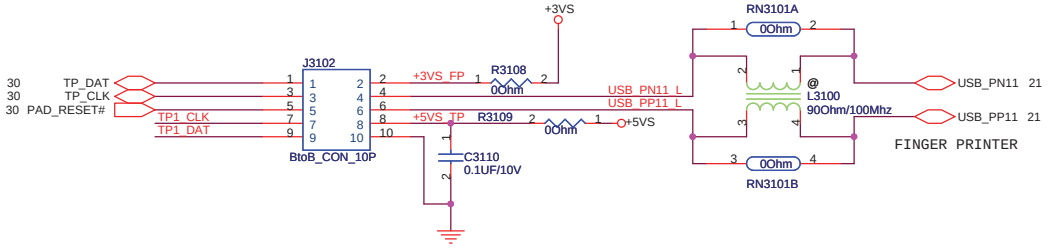
Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

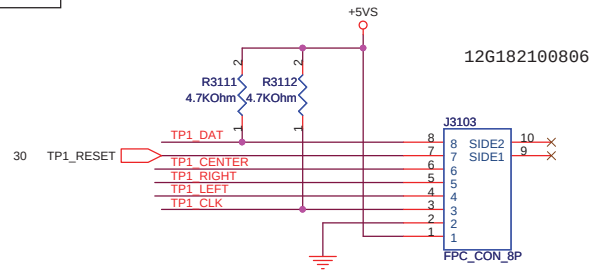
ASUS	Title :	EC_IT8752 (1/2)
	Engineer:	Tina Lee
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 30 of 94	

TOUCH PAD CONN



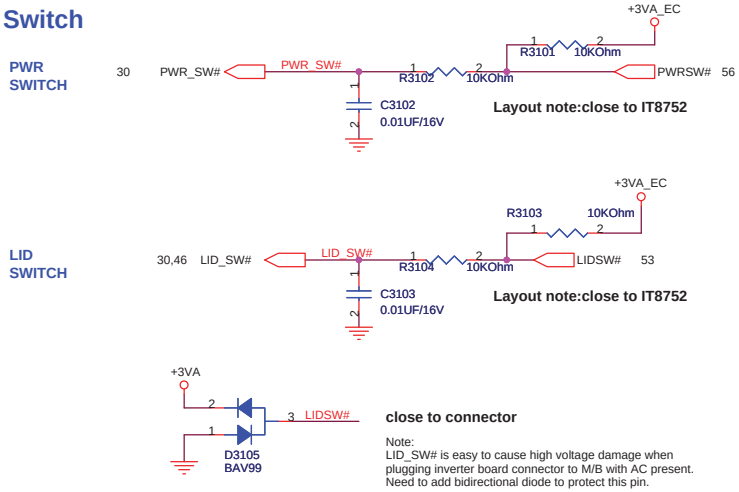
TP : Touch Pad
TP1: Track Point

TRACK POINT CONN

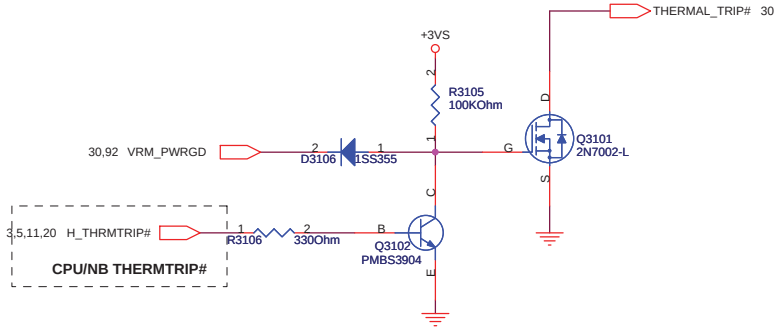


12G182100806

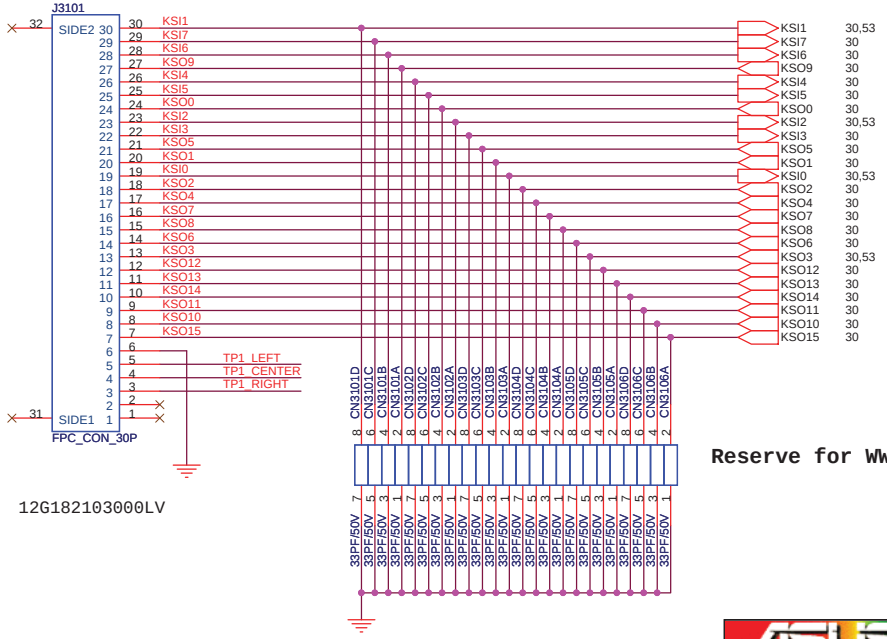
For Switch



For Thermal Control Method



Keyboard Connector



12G182103000LV

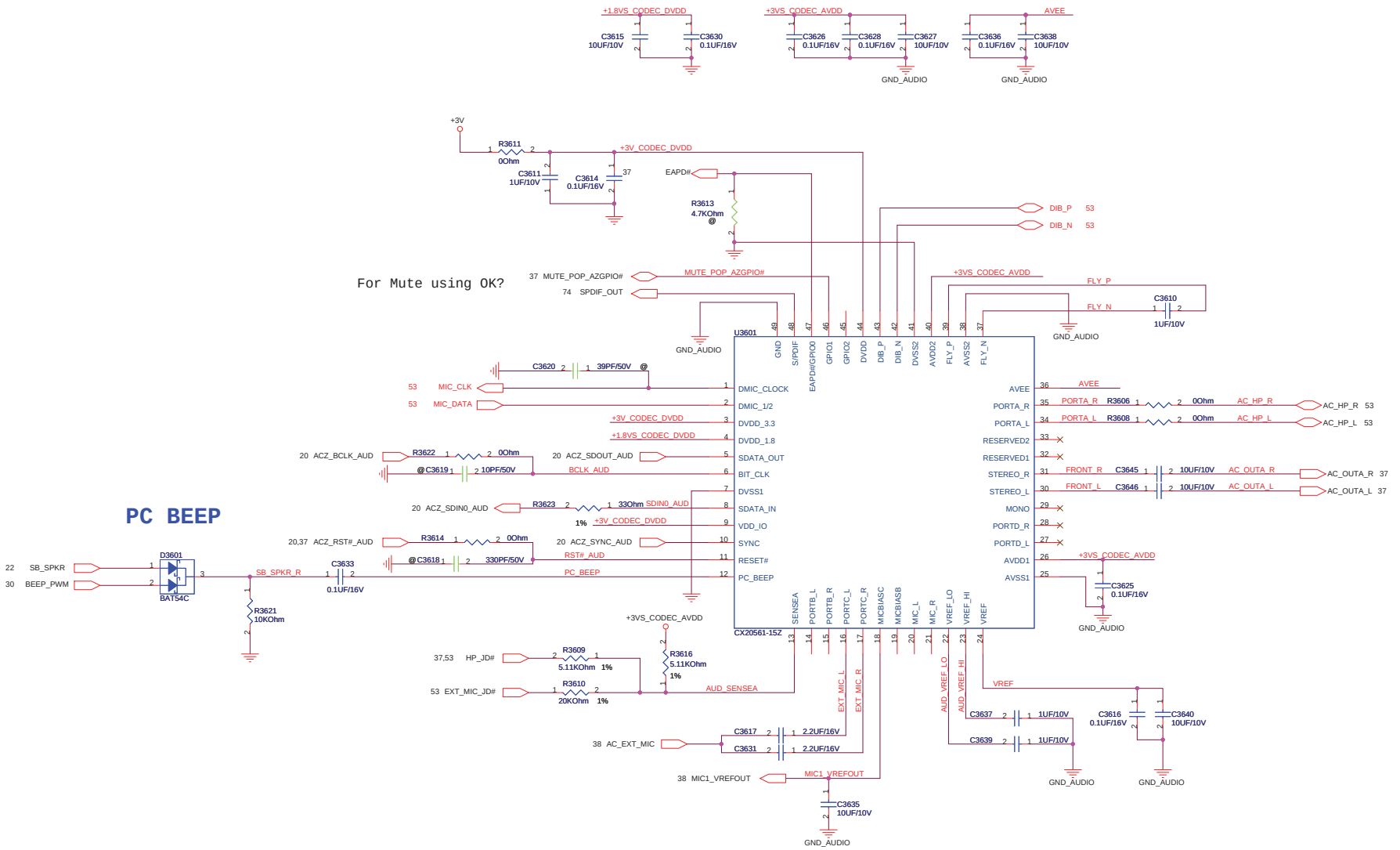
Title : EC_IT8752 (2/2)		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 31 of 94	

ASUS	Title : POWER-ON SEQUENCE	
	Engineer: *Tina Lee*	
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 32 of 94	

Title :	*****
Engineer:	Tina Lee
Size	A4
Project Name	Rocky 40/50
Rev	1.0
Date:	Monday, December 17, 2007
Sheet	33 of 94

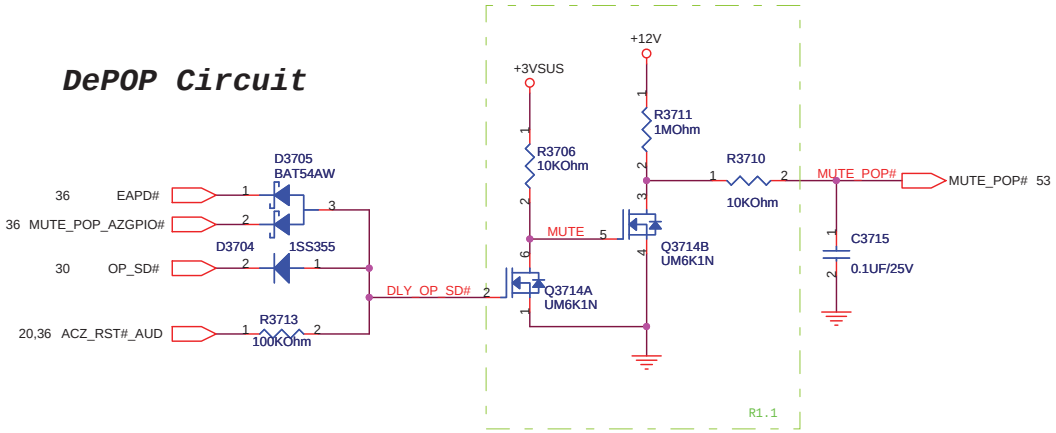
Title :	****	
Engineer:	*Tina Lee*	
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 34 of 94	

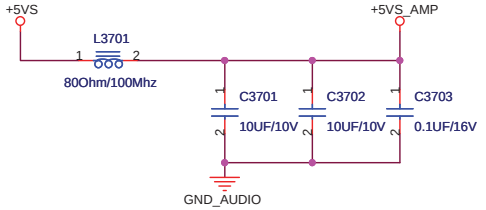
ASUS	Title : MDC	
	Engineer: *Tina Lee*	
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 35 of 94	



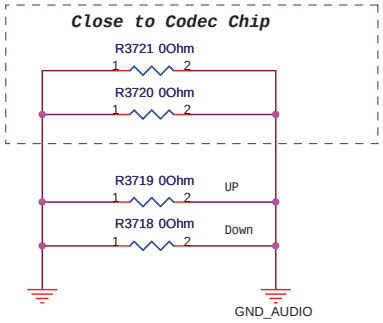
ASUS	Title : CODEC CX20561	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 36 of 94	

DePOP Circuit



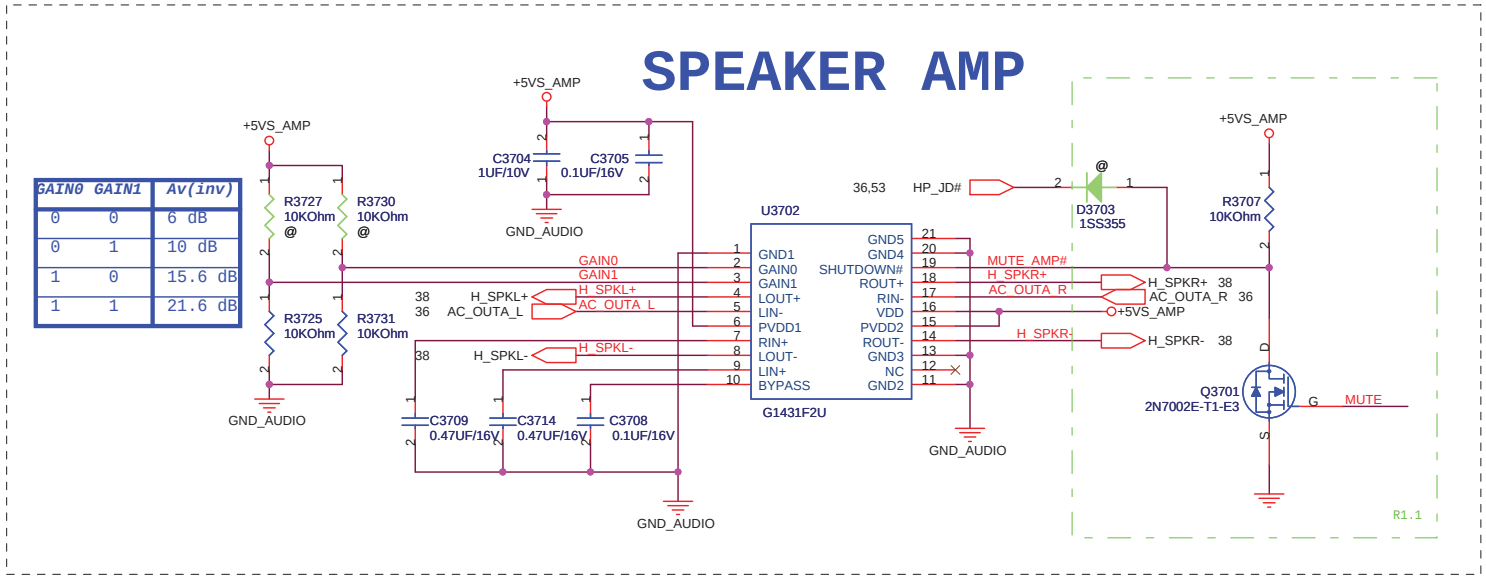


JACK GND



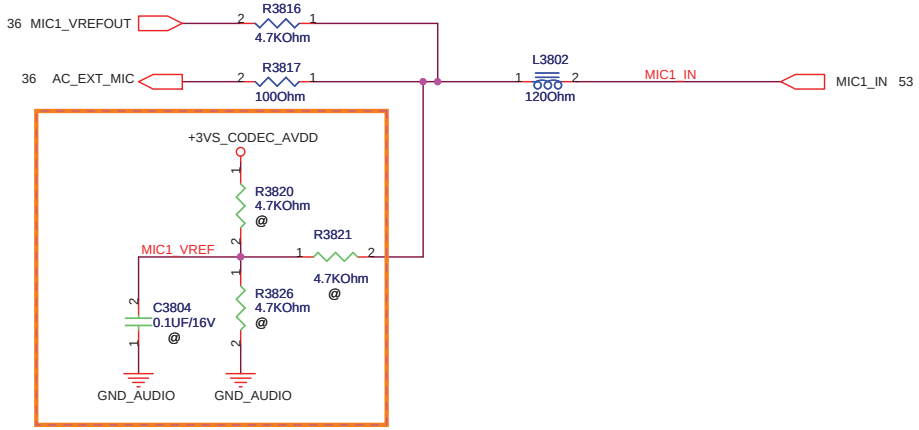
SPEAKER AMP

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



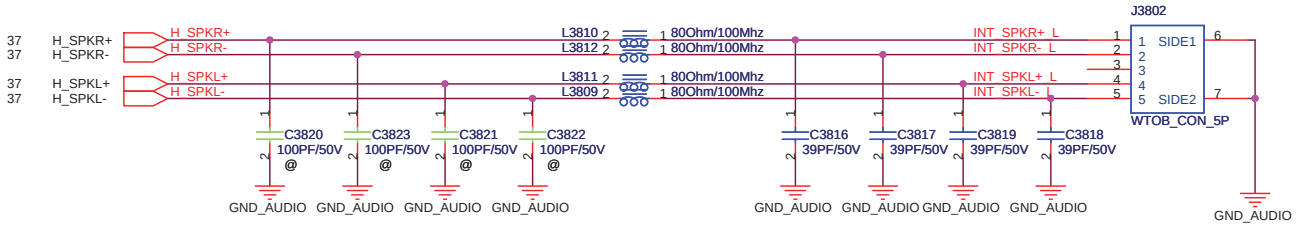
Title : AUDIO AMP		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 37 of 94	

EXT MICROPHONE

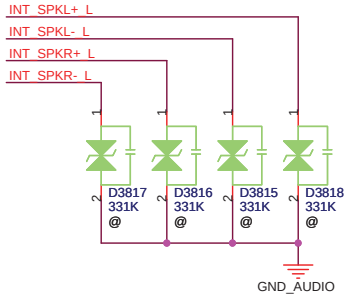


Reserved the external MIC bias(T filter).

SPEAKER CONNECTOR

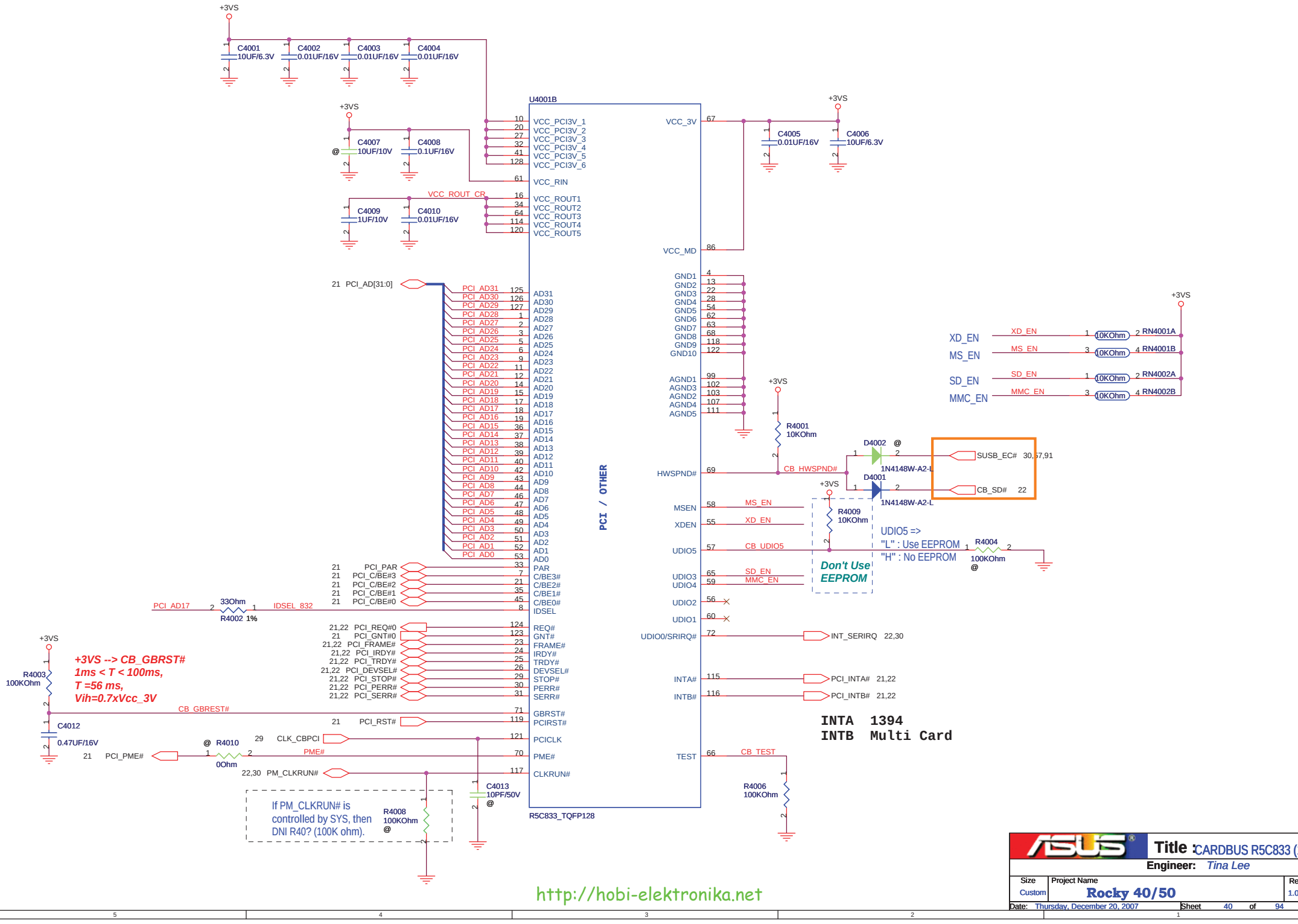


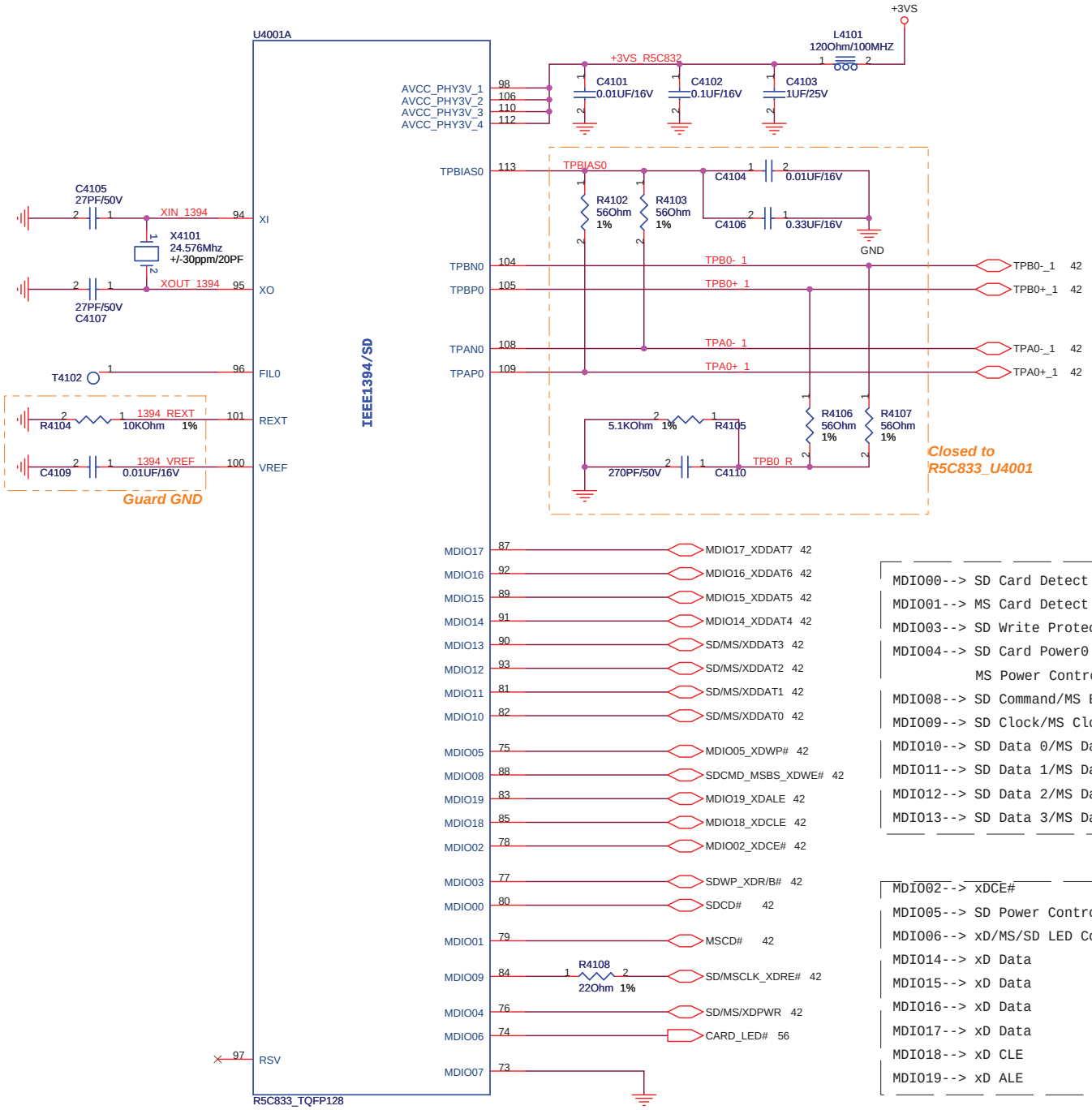
12G171010050LV
ACES/87213-0500G



ASUS	Title : MIC&LINEIN	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 38 of 94	

Title :	FM2010 DSP
Engineer:	*Tina Lee*
Size: A4	Project Name: **Rocky 40/50**
Rev: 1.0	
Date: Monday, December 17, 2007	Sheet 39 of 94


+3VS
C4001 10UF/6.3V
C4002 0.01UF/16V
C4003 0.01UF/16V
C4004 0.01UF/16V
C4007 @ 10UF/10V
C4008 0.1UF/16V
C4009 1UF/10V
C4010 0.01UF/16V
C4005 0.01UF/16V
C4006 10UF/6.3V
U4001B
VCC_PCI3V_1
VCC_PCI3V_2
VCC_PCI3V_3
VCC_PCI3V_4
VCC_PCI3V_5
VCC_PCI3V_6
VCC_RIN
VCC_ROUT_CR
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND3
AGND2
AGND4
AGND5
21 PCI_AD[31:0]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PCI / OTHER
21 PCI_PAR
21 PCI_C/BE#3
21 PCI_C/BE#2
21 PCI_C/BE#1
21 PCI_C/BE#0
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
PCI_AD17
33Ohm
R4002 1%
IDSEL_832
IDSEL
21,22 PCI_REQ#0
21 PCI_GNT#0
21,22 PCI_FRAME#
21,22 PCI_IRDY#
21,22 PCI_TRDY#
21,22 PCI_DEVSEL#
21,22 PCI_STOP#
21,22 PCI_PERR#
21,22 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
+3VS --> CB_GBRST#
1ms < T < 100ms,
T =56 ms,
Vih=0.7xVcc_3V
R4003 100KOhm
CB_GBREST#
C4012 0.47UF/16V
21 PCI_RST#
GBRST#
PCIRST#
29 CLK_CBPCI
PCICLK
@ R4010
0Ohm
PME#
21 PCI_PME#
PME#
22,30 PM_CLKRUN#
CLKRUN#
C4013 10PF/50V @
If PM_CLKRUN# is controlled by SYS, then DNI R40? (100K ohm).
R4008 100KOhm @
R5C833_TQFP128
HWSPND#
CB_HWSPND#
R4001 10KOhm
D4002 @
1N4148W-A2-L
D4001
SUSB_EC# 30,57,91
CB_SD# 22
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
MS_EN
XD_EN
CB_UDIO5
SD_EN
MMC_EN
R4009 10KOhm
Don't Use EEPROM
UDIO5 =>
"L" : Use EEPROM
"H" : No EEPROM
R4004 100KOhm @
INT_SERIRQ 22,30
INTA#
INTB#
PCI_INTA# 21,22
PCI_INTB# 21,22
INTA 1394
INTB Multi Card
TEST
CB_TEST
R4006 100KOhm
XD_EN
MS_EN
SD_EN
MMC_EN
10KOhm
RN4001A
RN4001B
RN4002A
RN4002B
http://hobi-elektronika.net
Title : CARDBUS R5C833 (1)
Engineer: Tina Lee
Size Custom
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 40 of 94

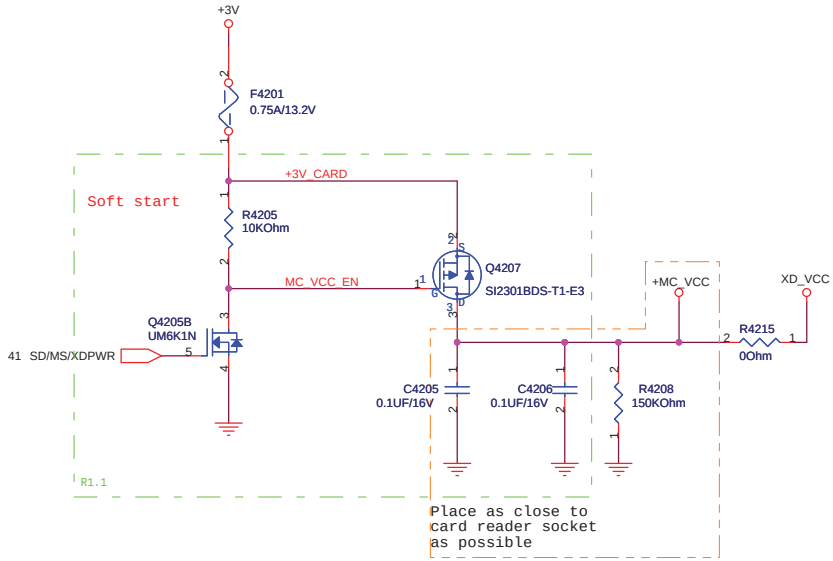


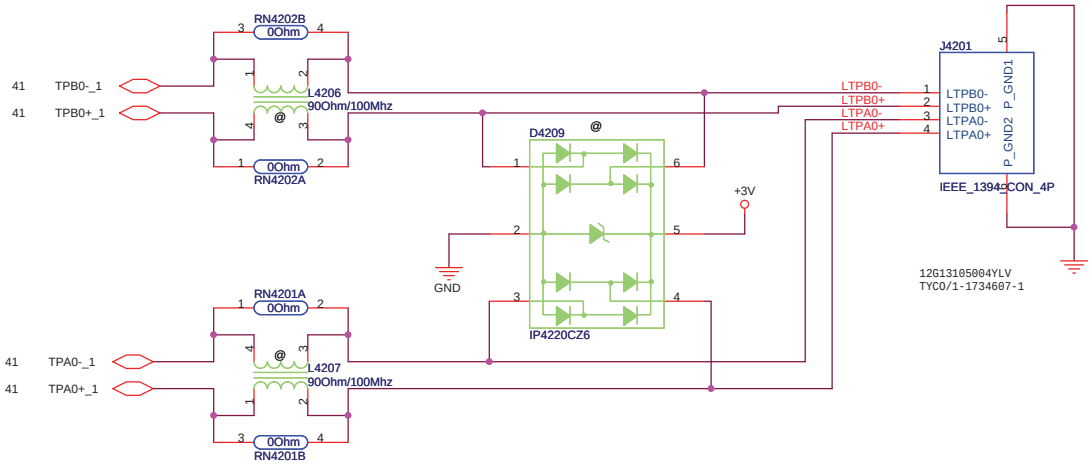
Title : CARDBUS R5C833 (2)

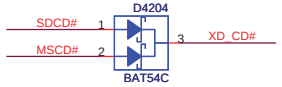
Engineer: Tina Lee

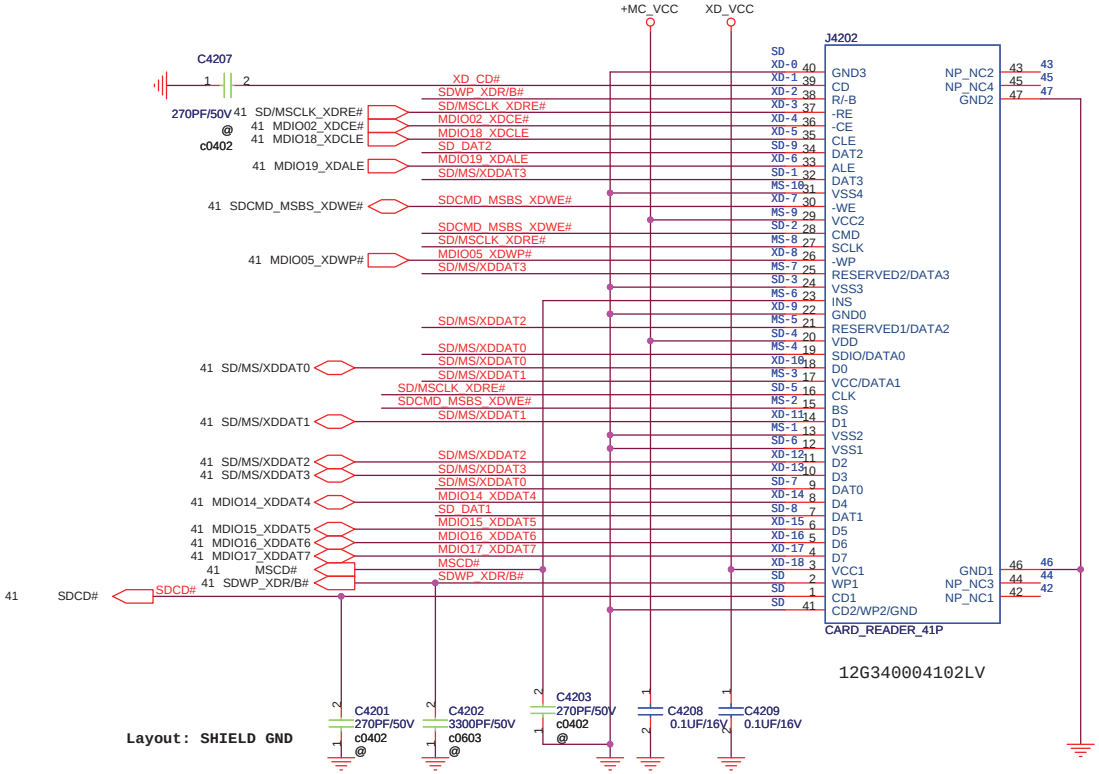
Size	Project Name	Rev
Custom	Rocky 40/50	1.0

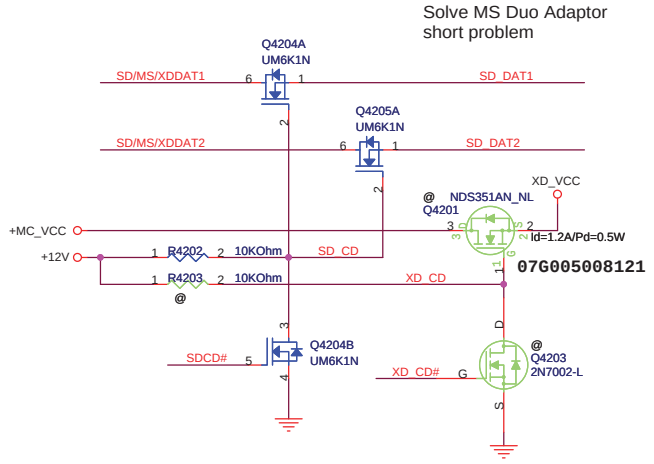
Date: Thursday, December 20, 2007 Sheet 41 of 94









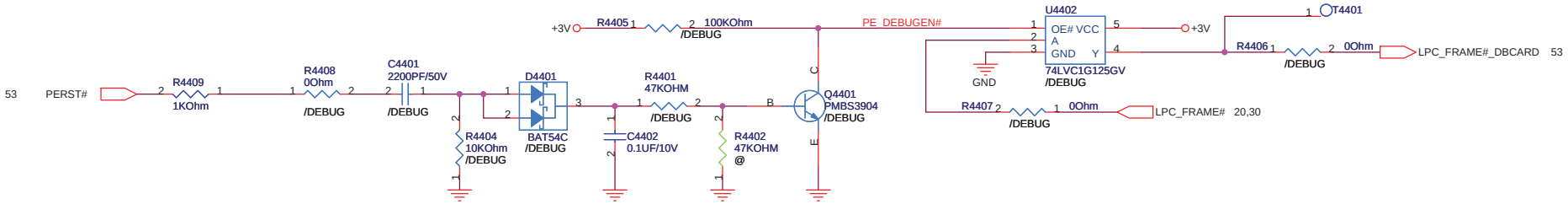


http://hobi-elektronika.net

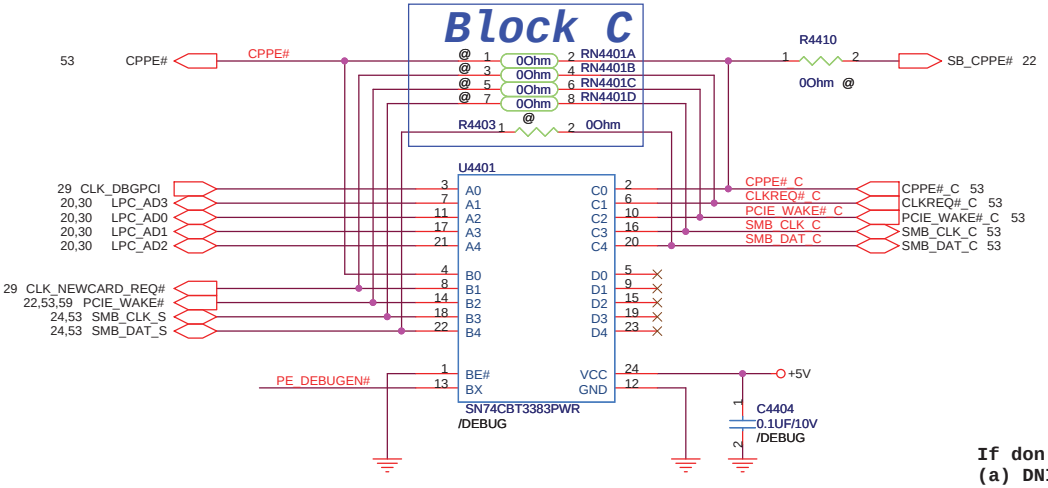
ASUS	Title : 1394 & CardReader	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 42 of 94	

Title :	NEW CARD
Engineer:	*Tina Lee*
Size: A4	Project Name: **Rocky 40/50**
Rev: 1.0	
Date: Monday, December 17, 2007	Sheet 43 of 94

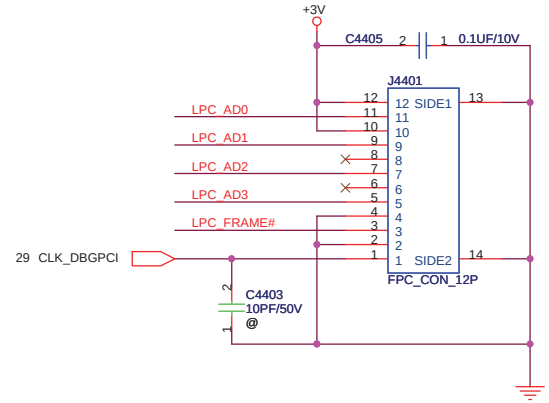
Block A



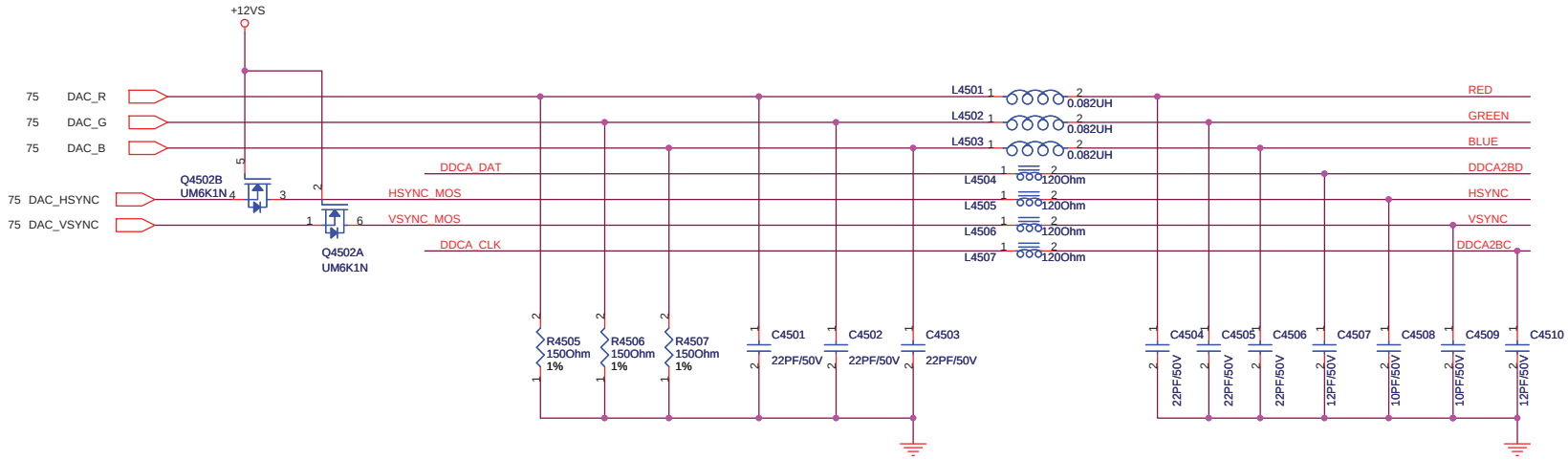
Block C

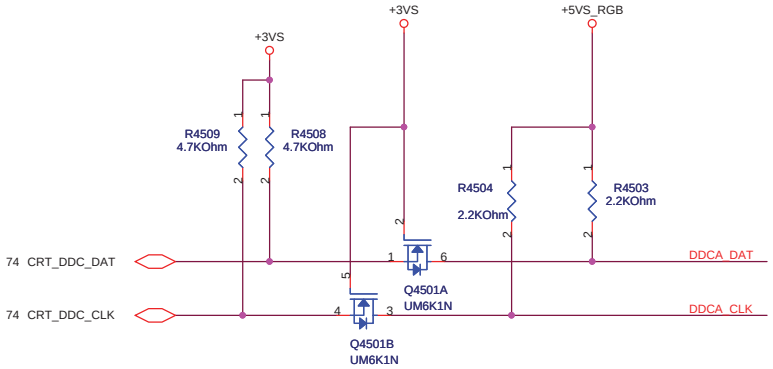


If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

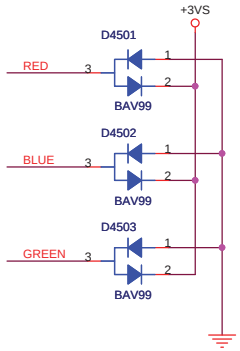


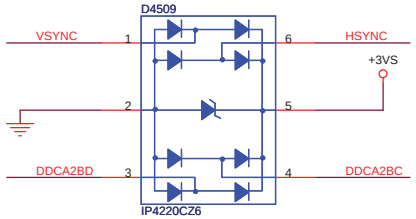
ASUS	Title : DEBUG	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 44 of 94	



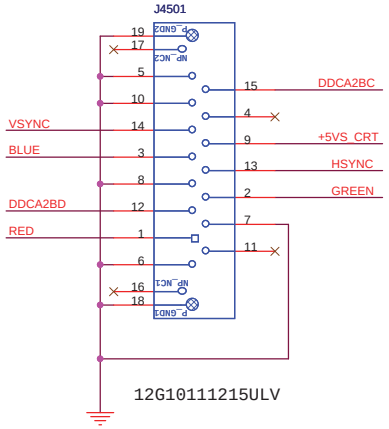


PLACE ESD Diodes near VGA port





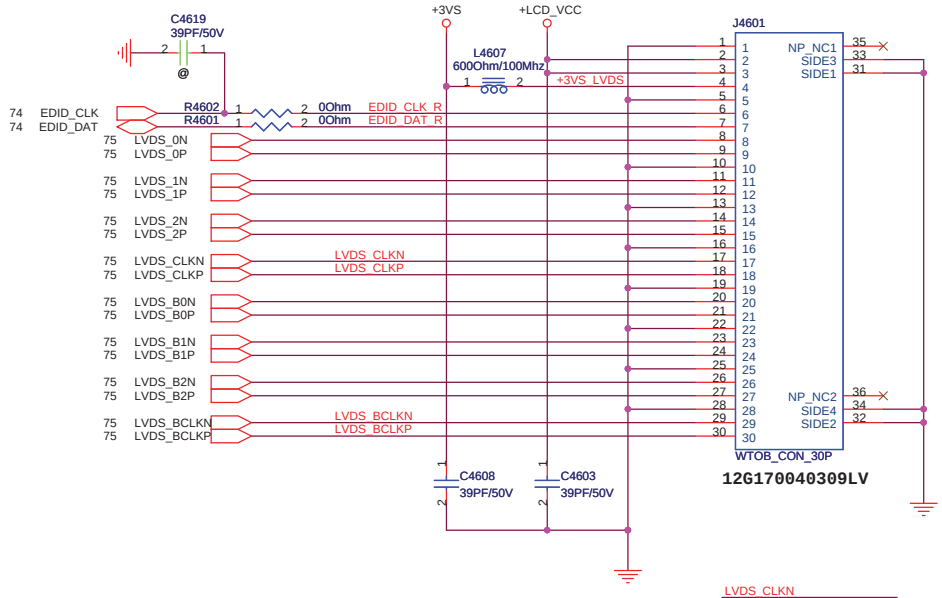
D_SUB_15P

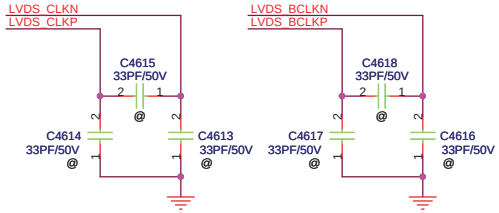


12G10111215ULV

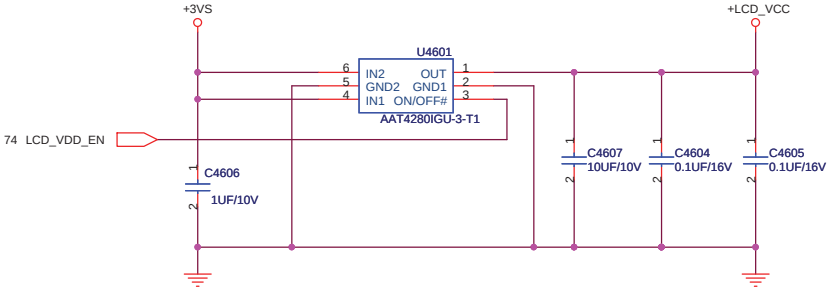
ASUS	Title : CRT	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 45 of 94	

LVDS CNT

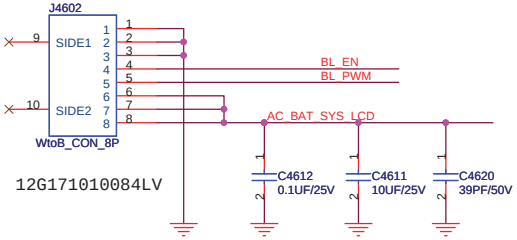


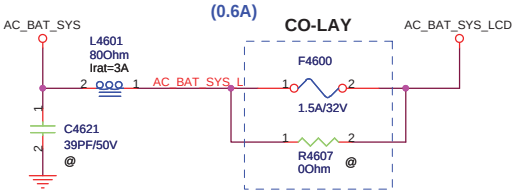


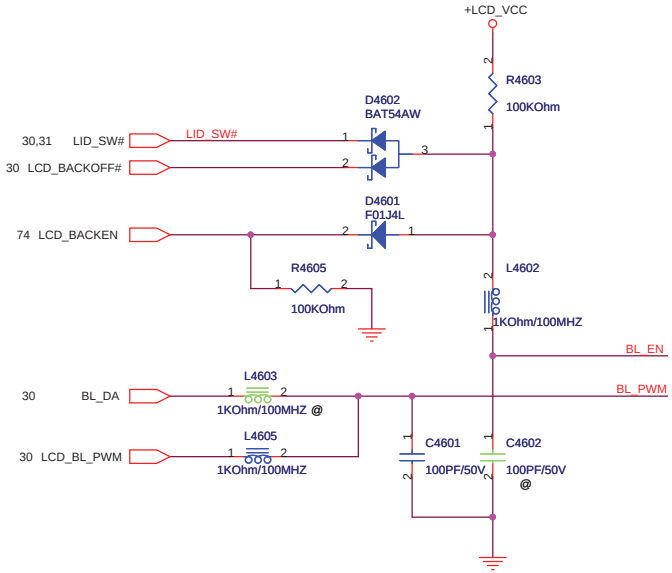
Power Switch for LCD Power



INVERTER CNT







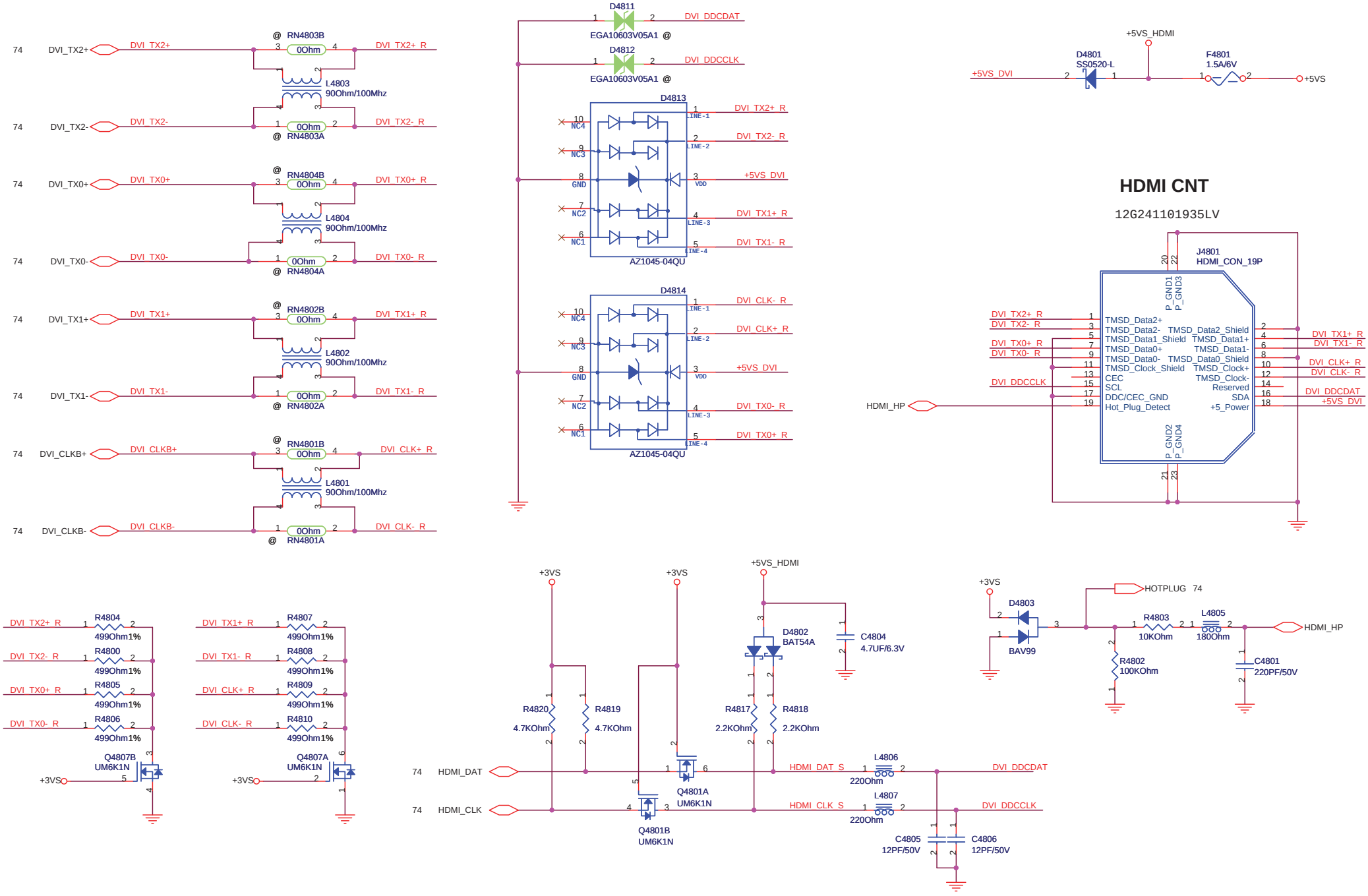
Title: LVDS & Inverter CON		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 46 of 94	

Title : TV_OUT CON

Engineer: *Tina Lee*

Size	Project Name	Rev
A4	**Rocky 40/50**	1.0

Date: Monday, December 17, 2007 Sheet 47 of 94

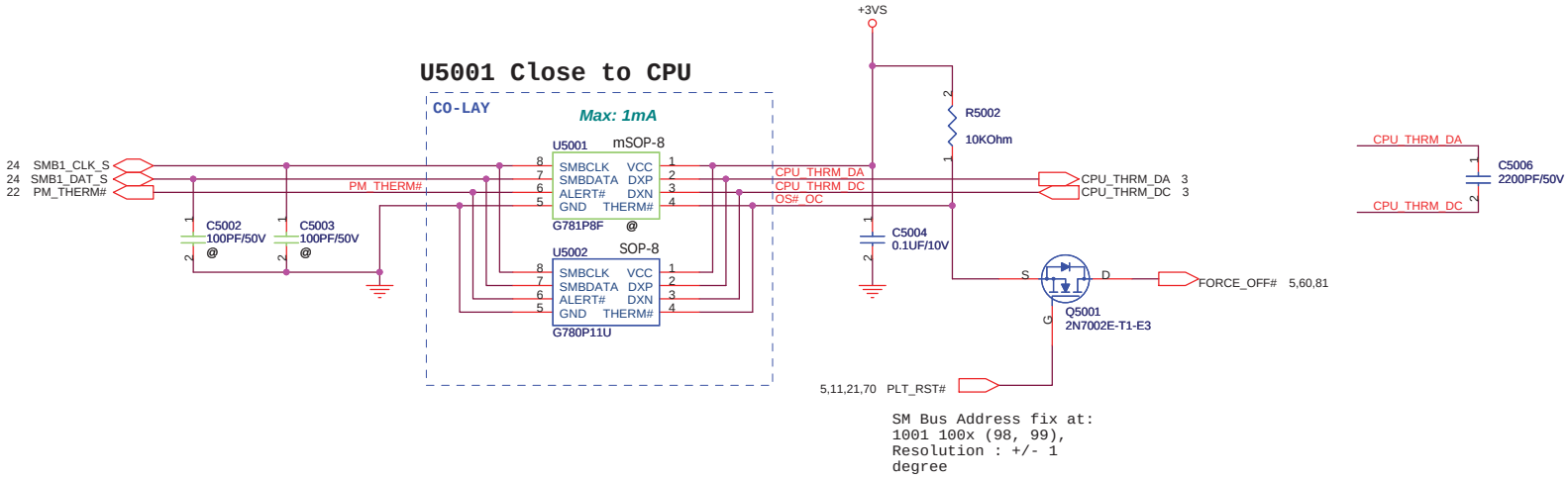


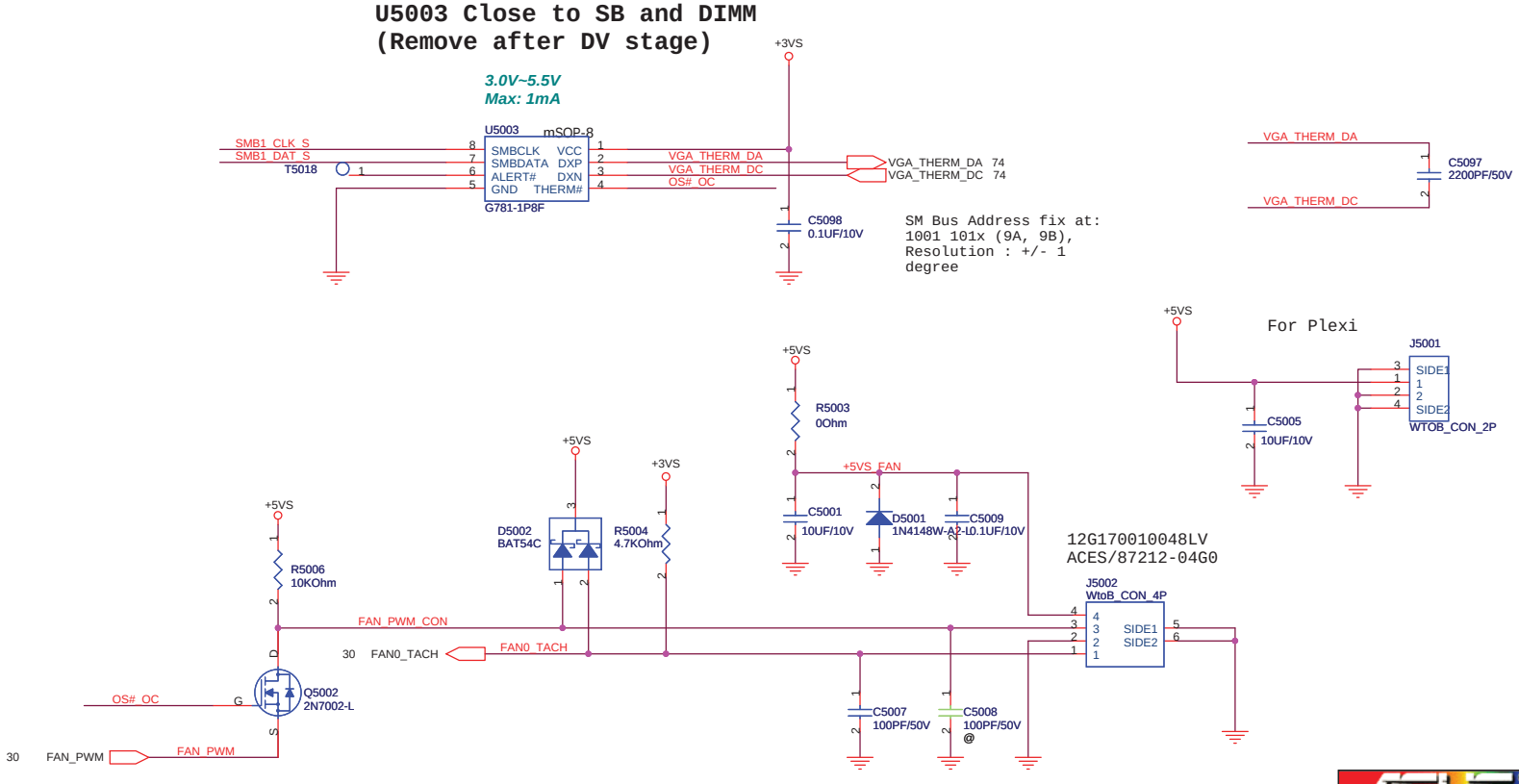
http://hobi-elektronika.net

Title : HDMI		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 48 of 94	

ASUS	Title :	
	Engineer: *Tina Lee*	
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 49 of 94	

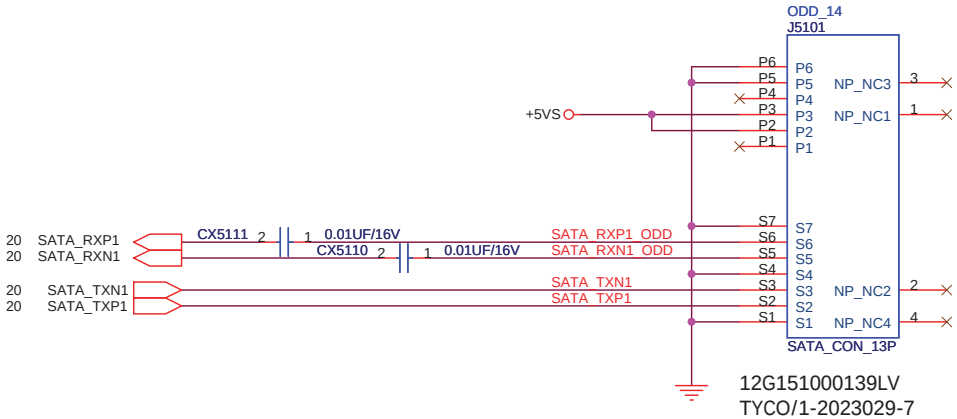
Thermal Sensor





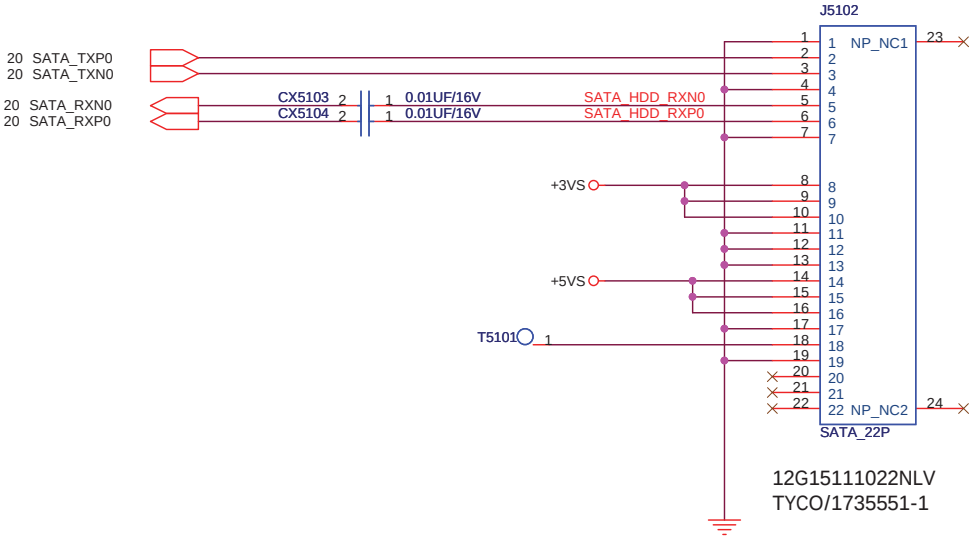
Title : Thermal & Fan		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 50 of 94	

ODD CON

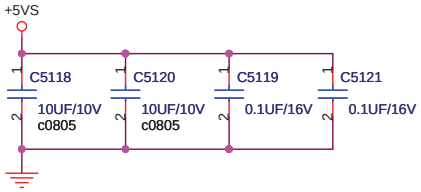


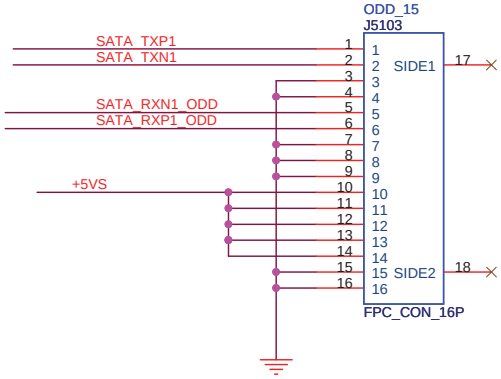
12G151000139LV
TYCO/1-2023029-7

SATA HDD CON

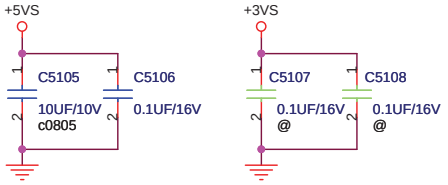


12G15111022NLV
TYCO/1735551-1

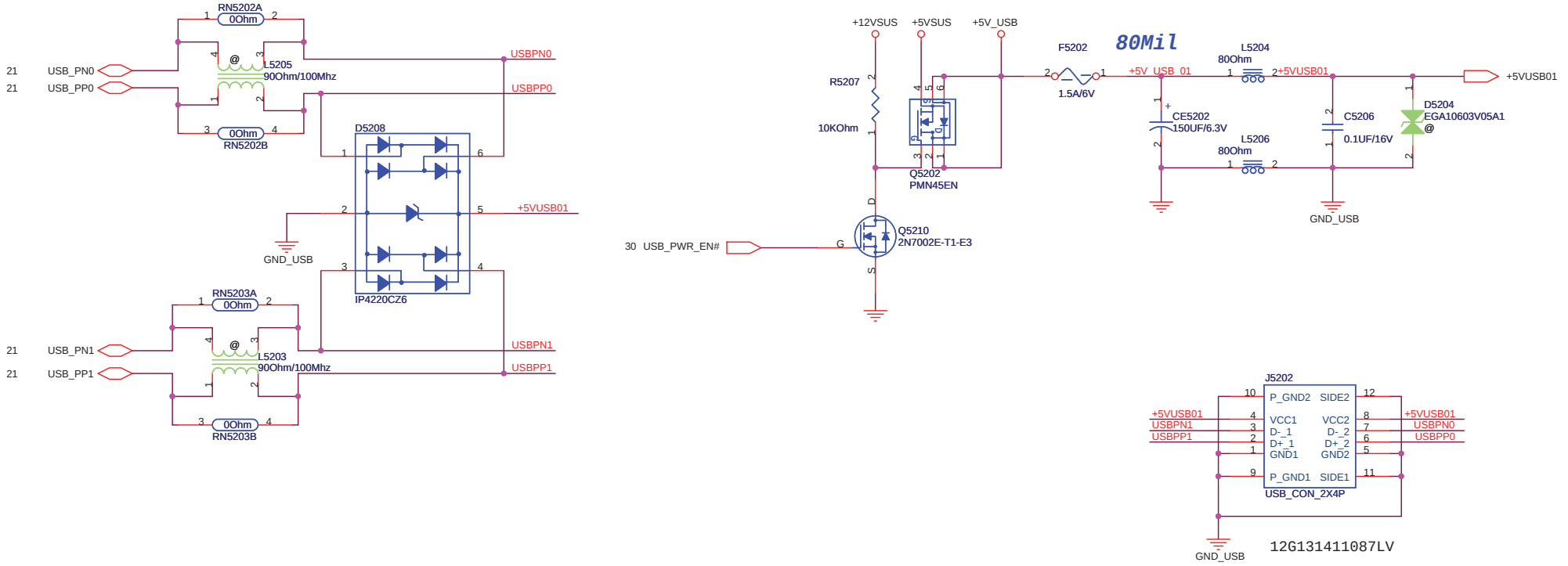




12G183101602LV
ACES/88278-16001

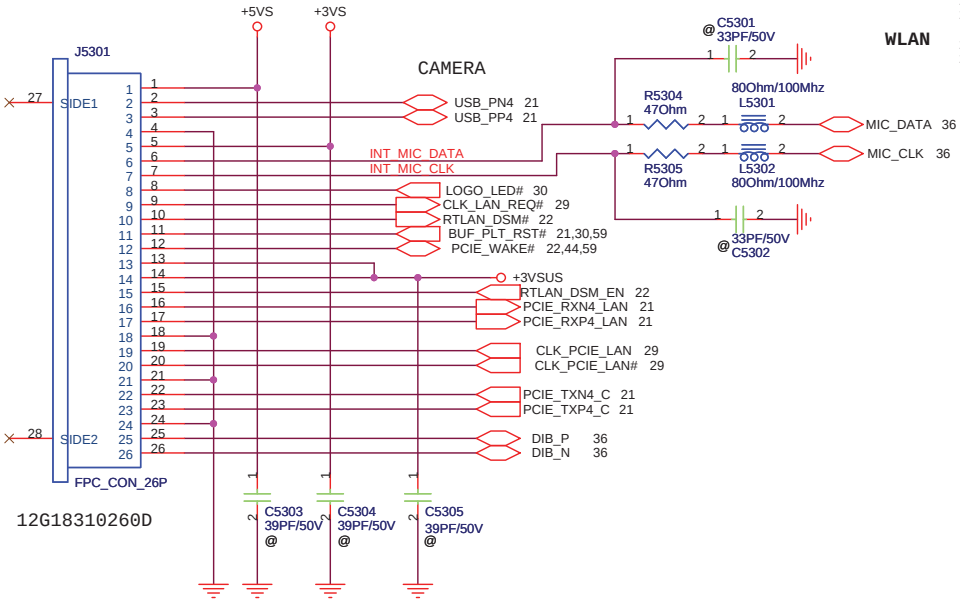


Title : Sata HDD & Swap Bay		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 51 of 94	



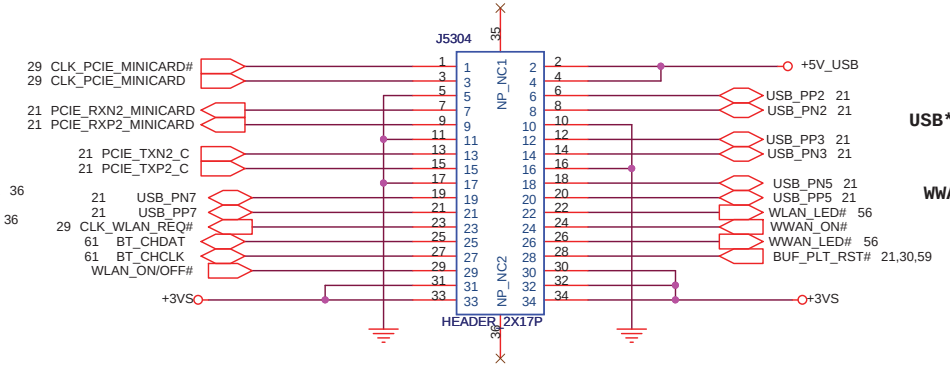
Title : USB CONN X 4		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 52 of 94	

IO BOARD

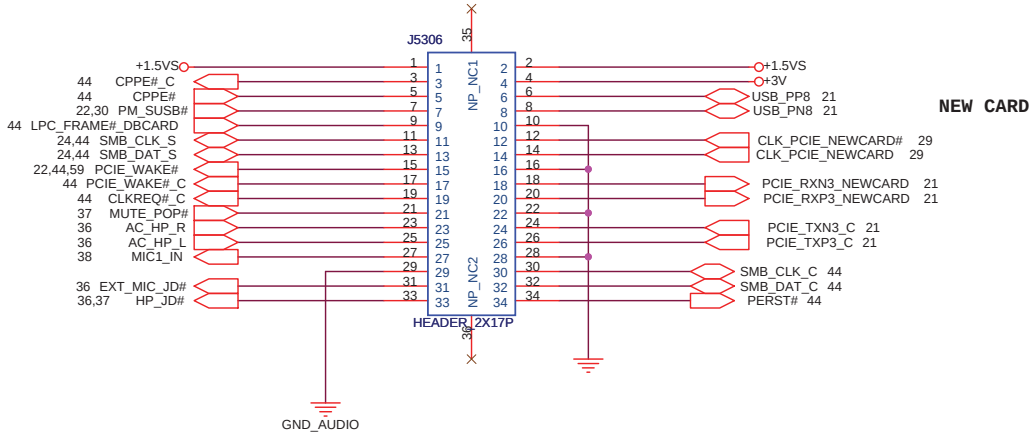


12G18310260D

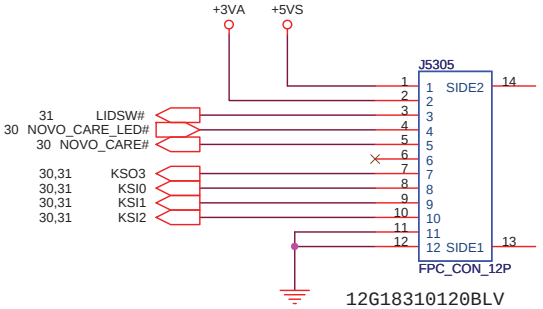
SMALL BOARD



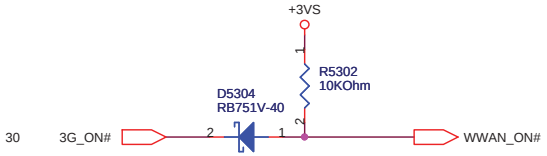
12G0612003441V

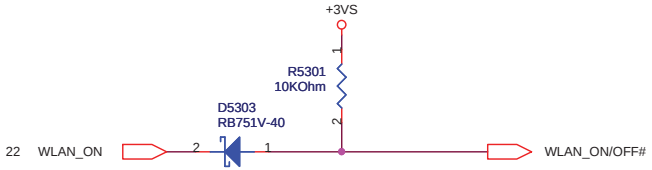


For Media Control Board

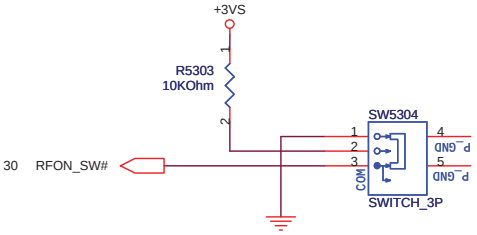


12G18310120BLV





Wireless Switch



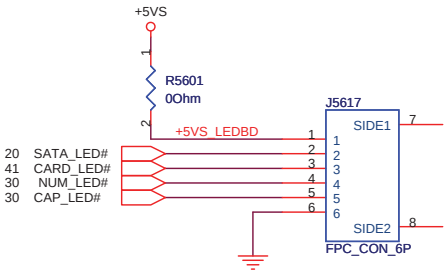
12G0910700311V
ALPS/SSSS710603

Title : IO BOARD		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 53 of 94	

Title :	Port Docking
Engineer:	*Tina Lee*
Size: A4	Project Name: **Rocky 40/50**
Rev: 1.0	
Date: Monday, December 17, 2007	Sheet 54 of 94

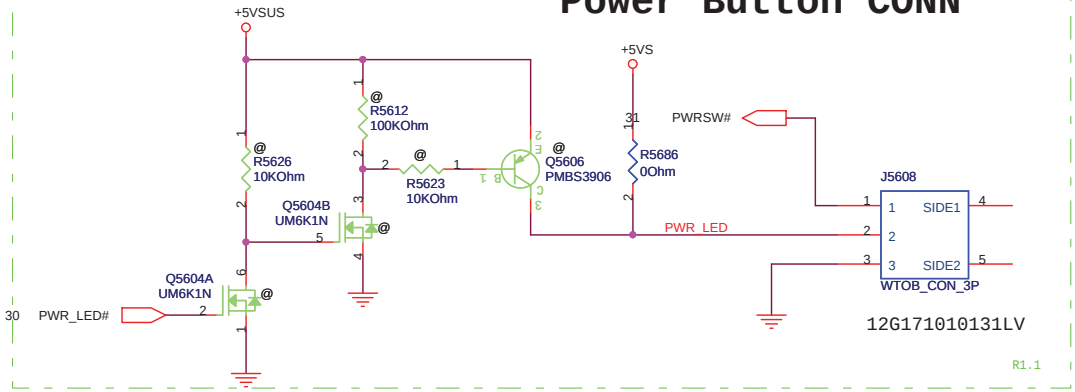
Title : Super I/O & FIR		
Engineer: *Tina Lee*		
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 55 of 94	

LED CONN



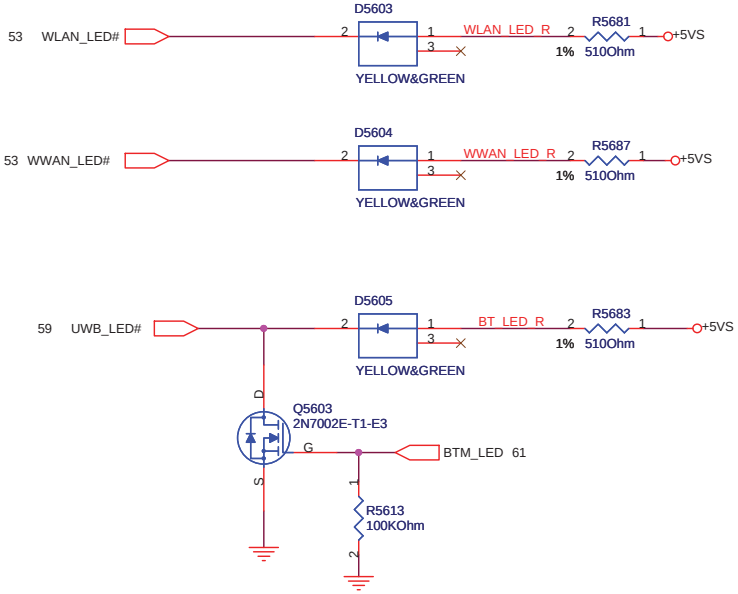
12G183100603

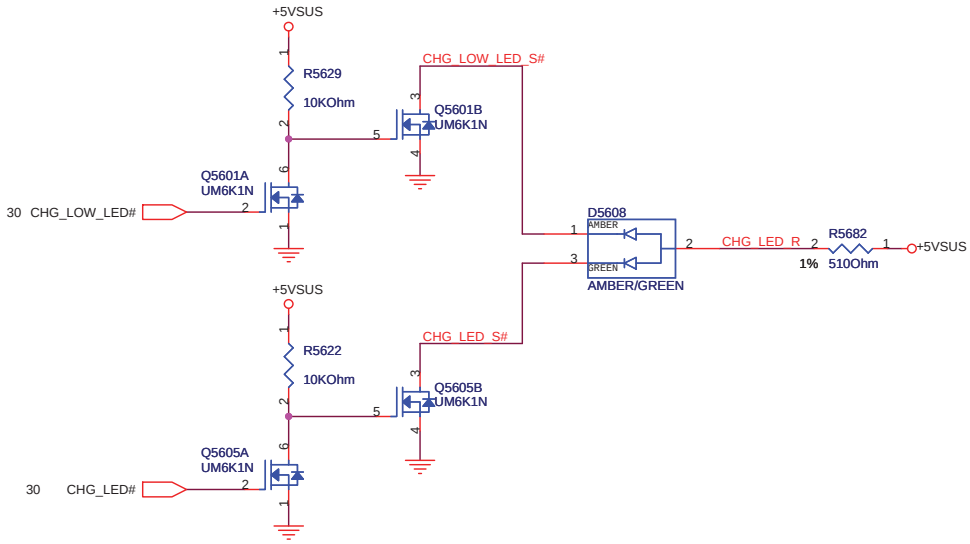
Power Button CONN

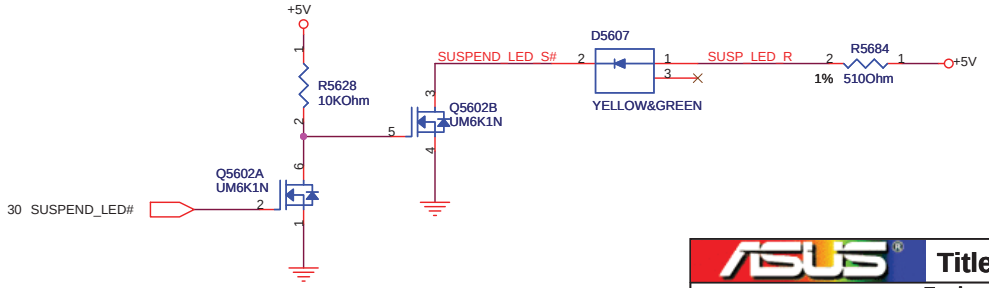


12G171010131LV

R1.1





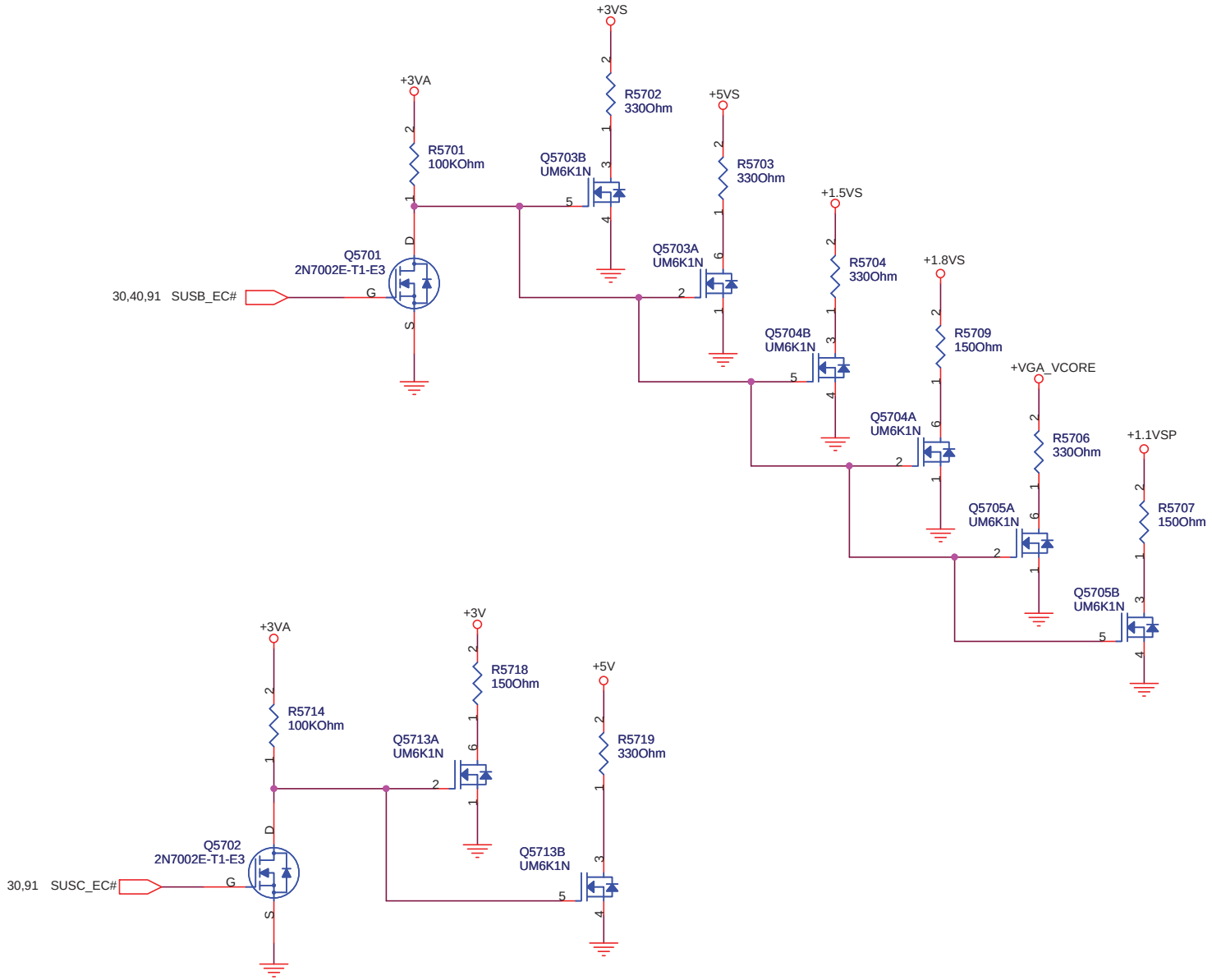


Title : LED/TP/SW

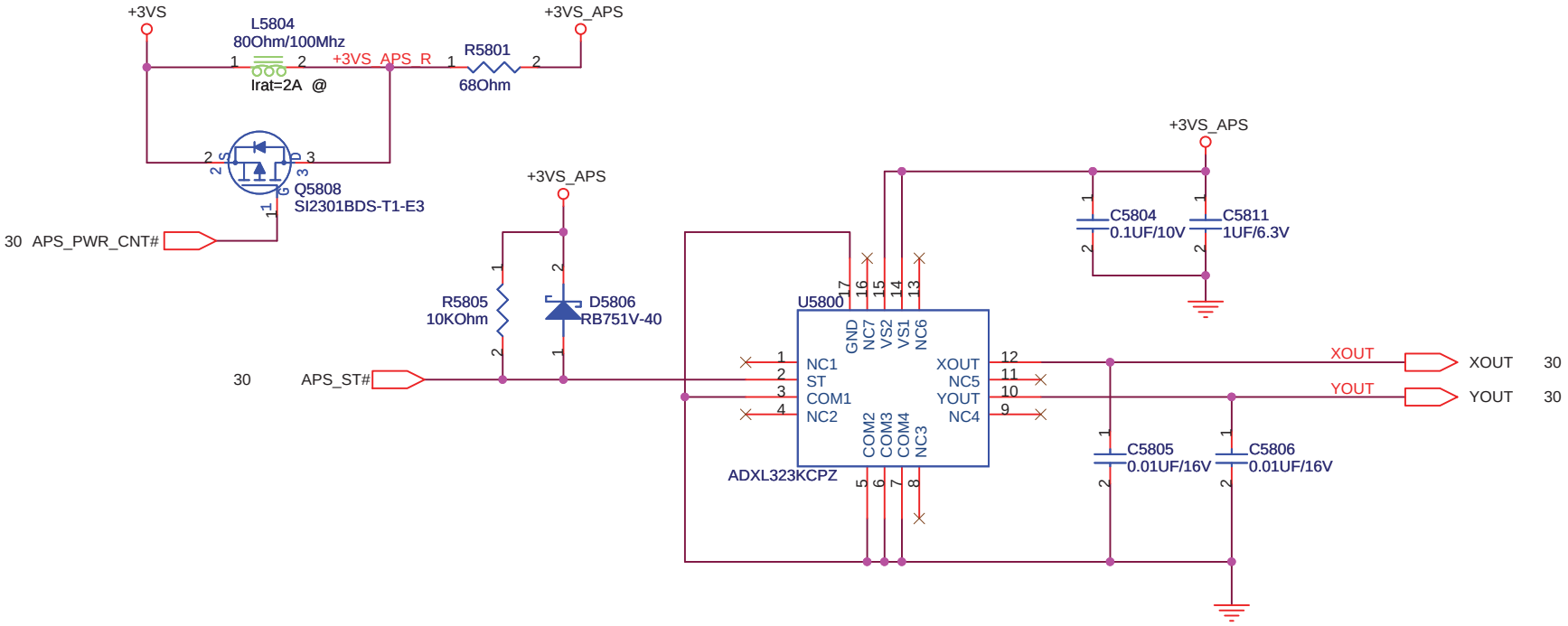
Engineer: Tina Lee

Size	Project Name	Rev
Custom	Rocky 40/50	1.0

Date: Thursday, December 20, 2007 Sheet 56 of 94

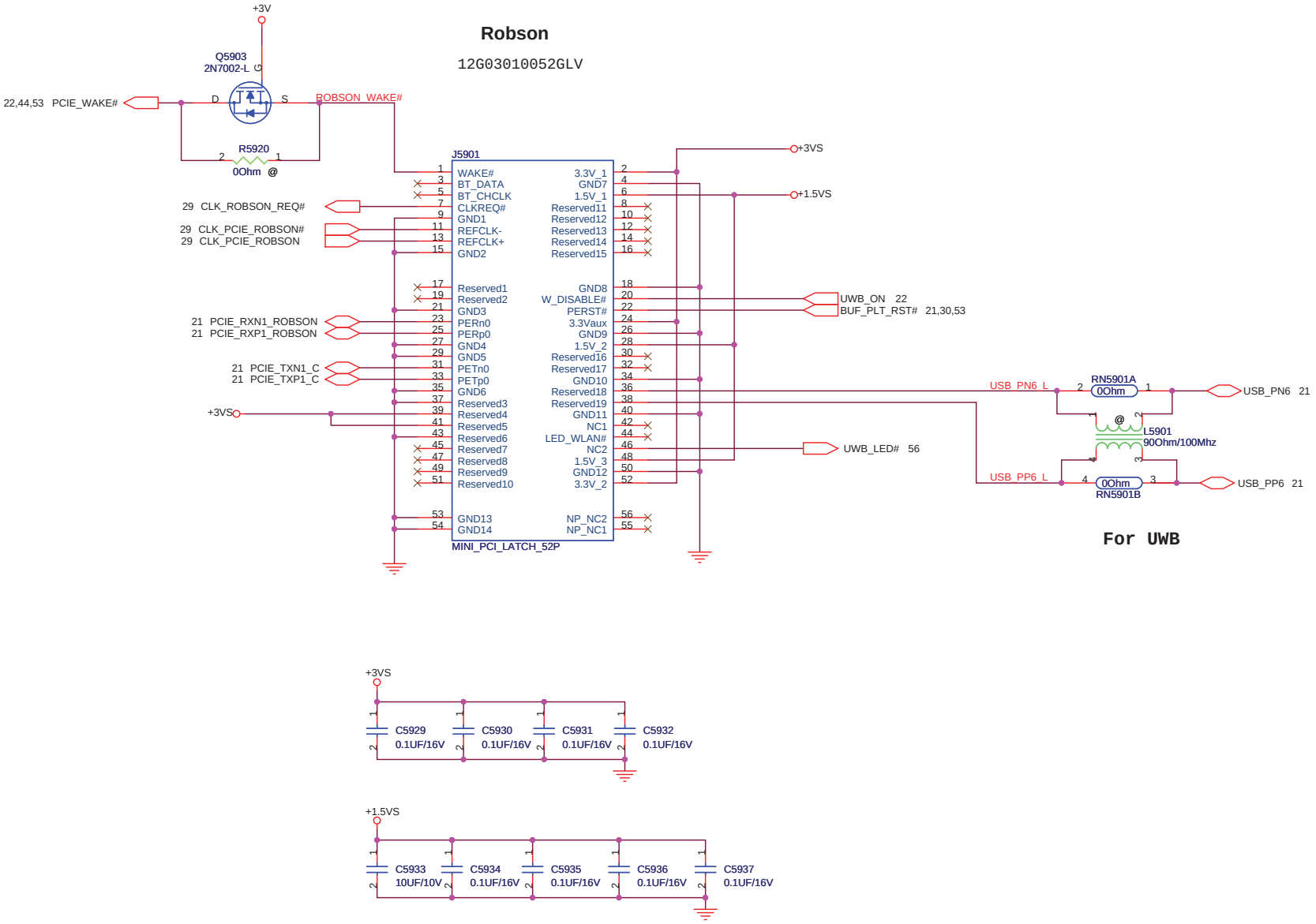


Title : DISCHARGE		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 57 of 94	



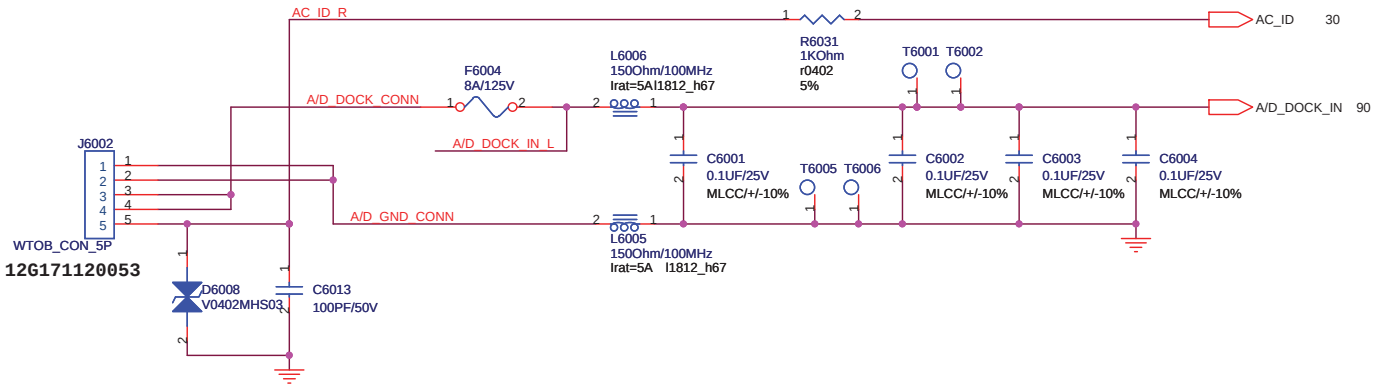
http://hobi-elektronika.net

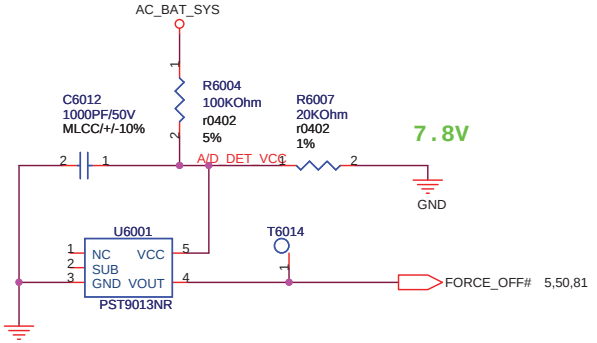
ASUS	Title : SMS	
	Engineer: *Tina Lee*	
Size A4	Project Name **Rocky 40/50**	Rev 1.0
Date: Thursday, December 20, 2007	Sheet 58 of 94	



Title : Mini Card		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 59 of 94	

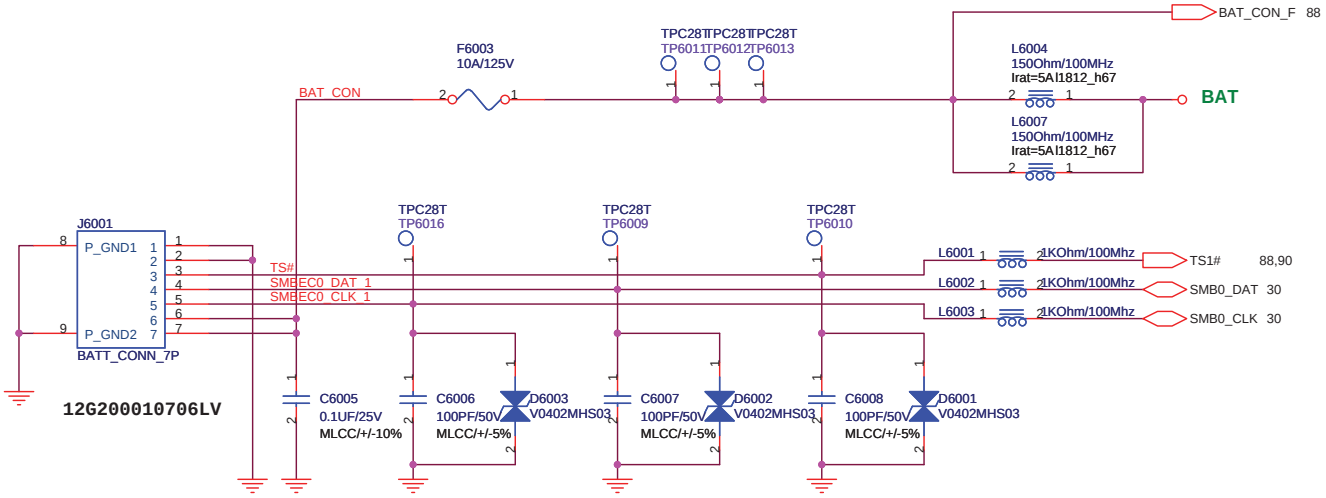
DC IN CONN





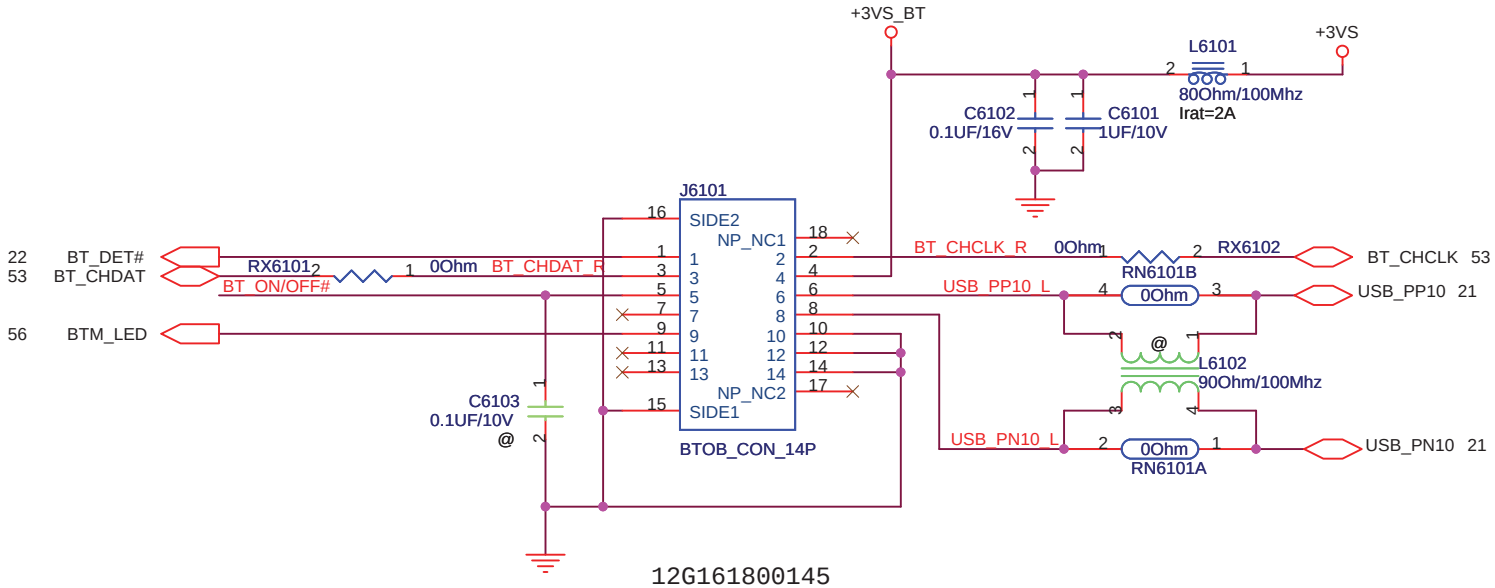
Without Battery & Pull out Adapter

Battery CONN

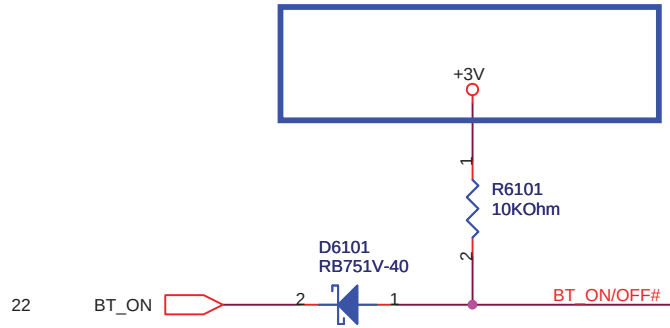


Title : DC Jack & Battery CONN		
Engineer: Morris Tseng		
Size: Custom	Project Name: Rocky40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 60 of 94	

Blue Tooth



12G161800145



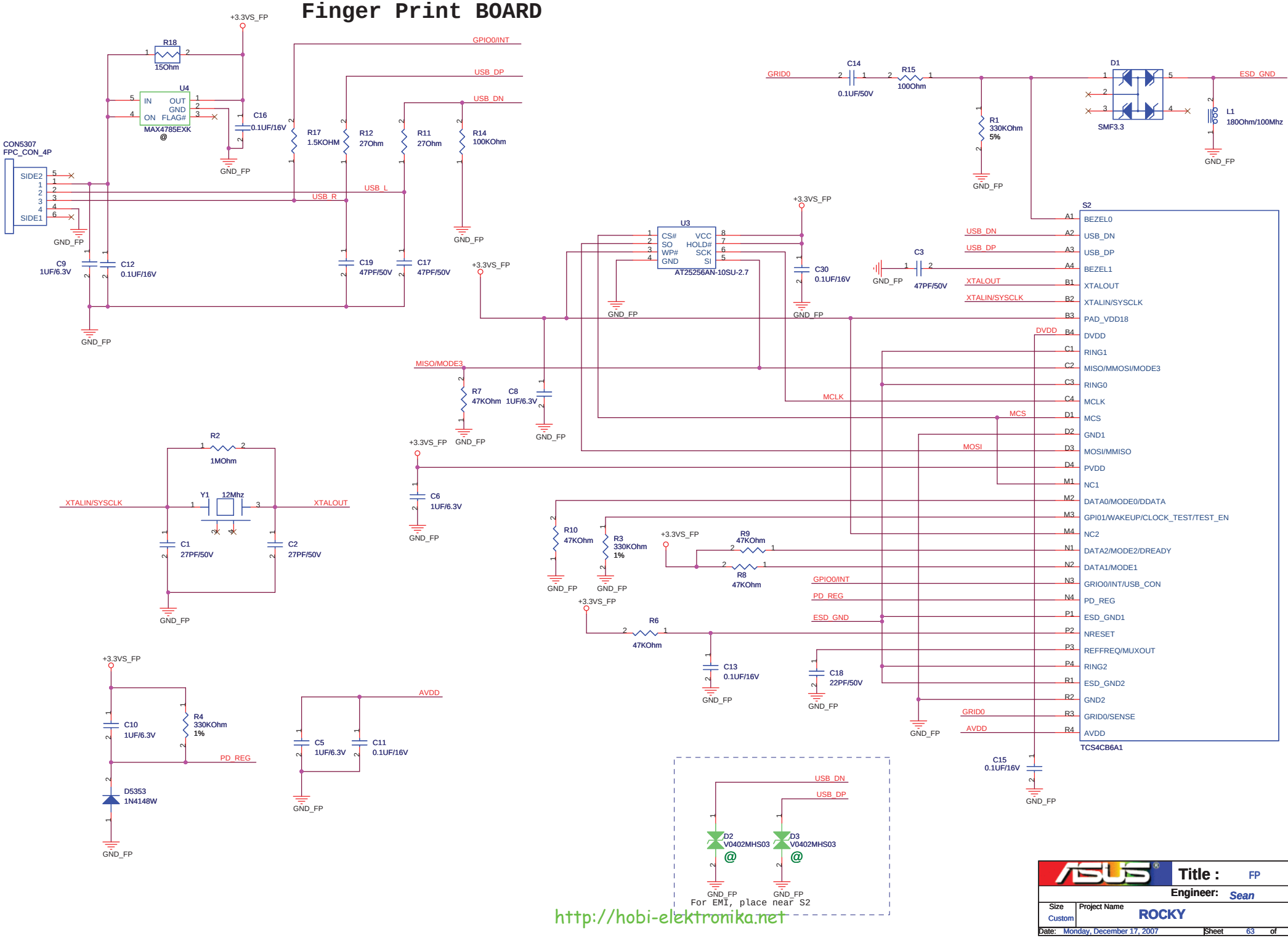
To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

From GPIO27 ICH-9

Title : BlueTooth		
Engineer: Tina Lee		
Size: A4	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 61 of 94	

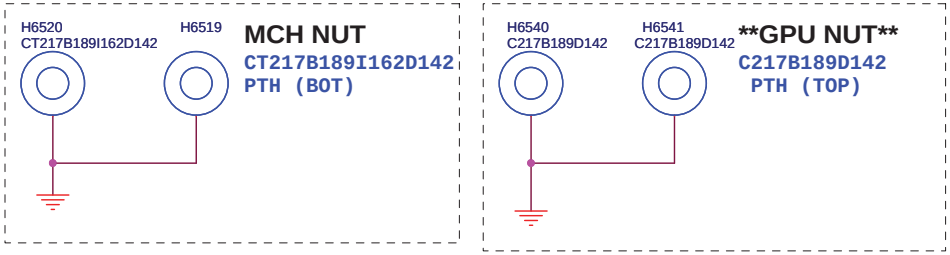
Title : TPM		
Engineer: *Tina Lee*		
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 62 of 94	

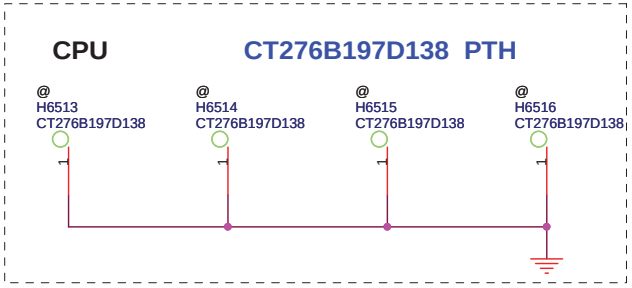
Finger Print BOARD

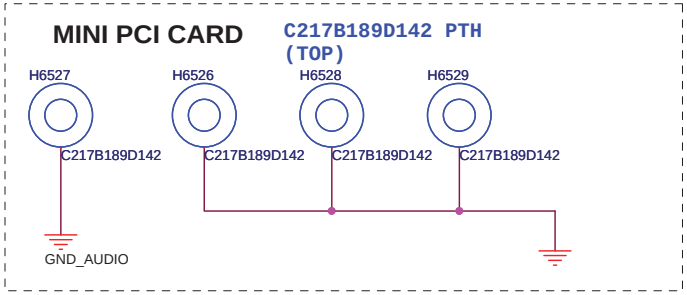


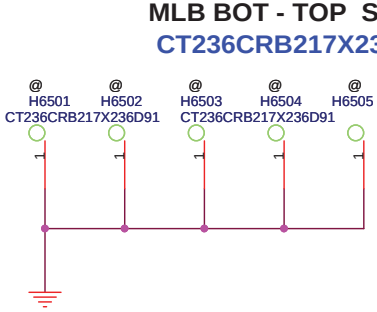
Title : FP		
Engineer: Sean		
Size: Custom	Project Name: ROCKY	Rev: 1.3
Date: Monday, December 17, 2007	Sheet 63 of 94	

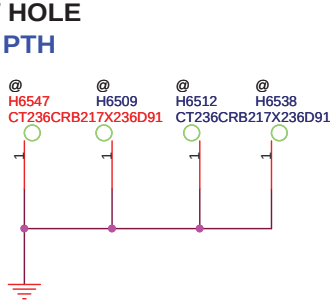
ASUS	Title :	
	Engineer: *Tina Lee*	
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 64 of 94	

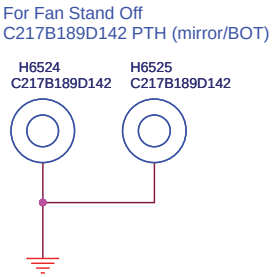


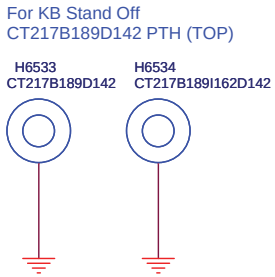


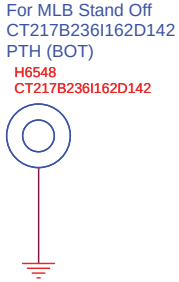


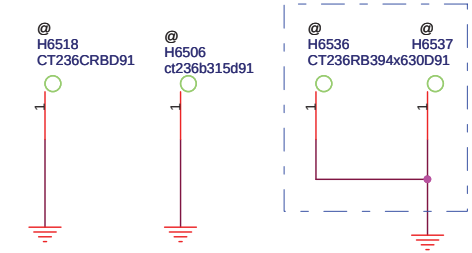


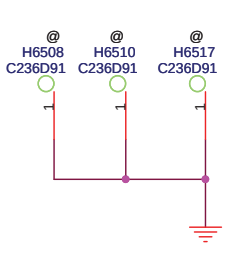


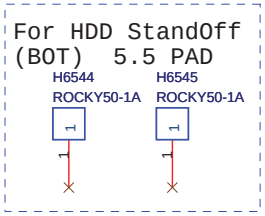


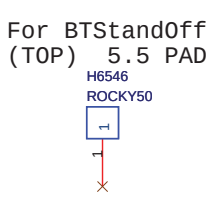


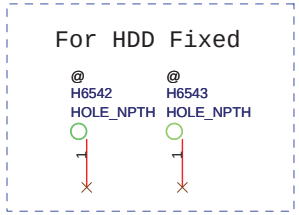


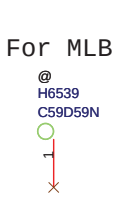


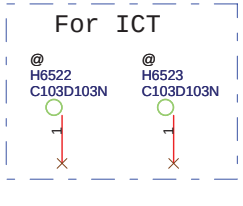


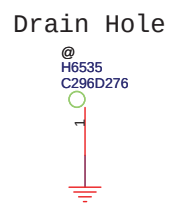










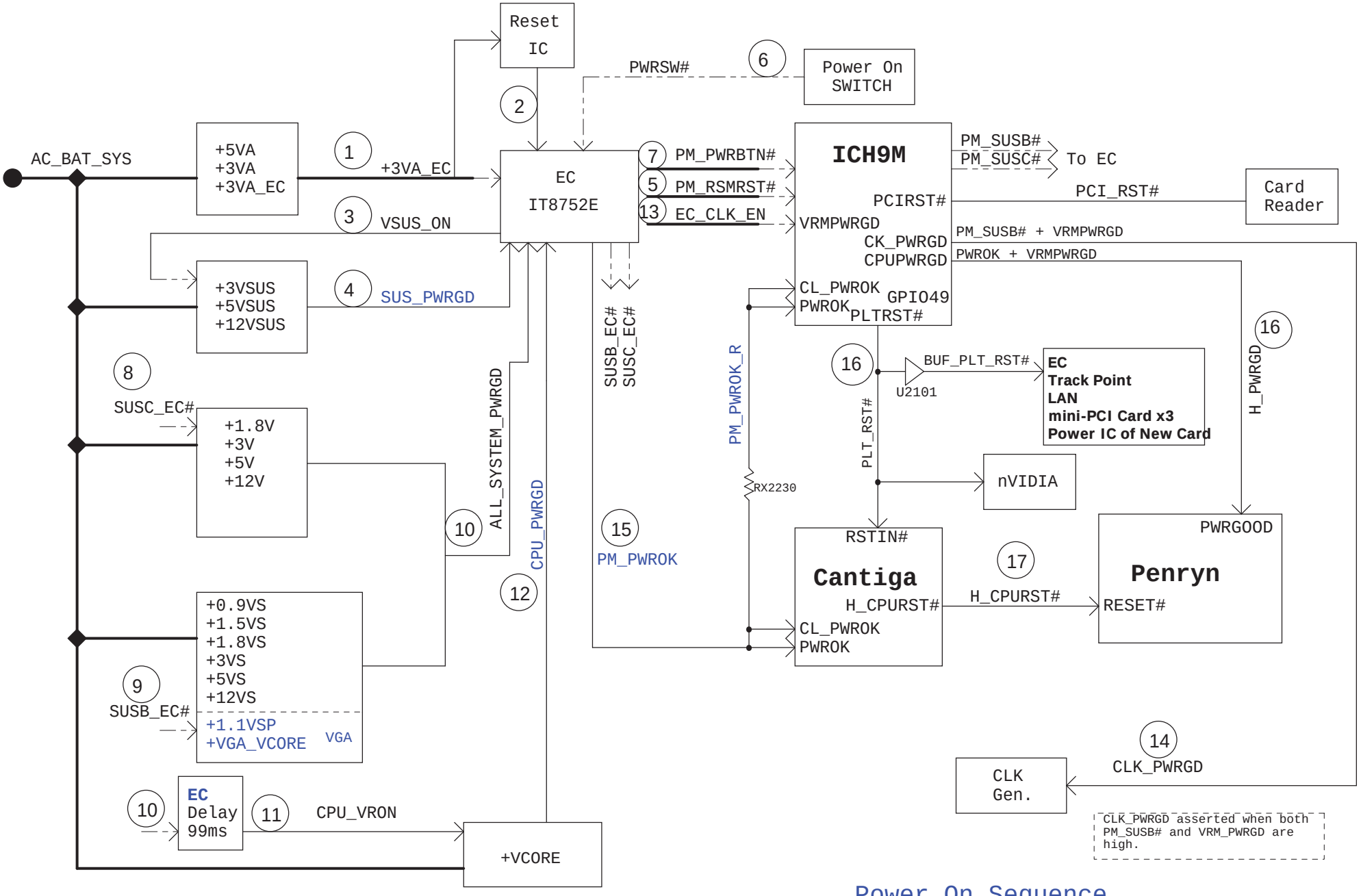


Title	MDC NUT & Hinksink NUT	
Engineer:	Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 65 of 94	

Title : E-SATA		
Engineer: *Tina Lee*		
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 66 of 94	

Title :	Minicard card & Nut
Engineer:	Tina Lee
Size: A4	Project Name: Rocky 40/50
Rev: 1.0	
Date: Monday, December 17, 2007	Sheet 67 of 94

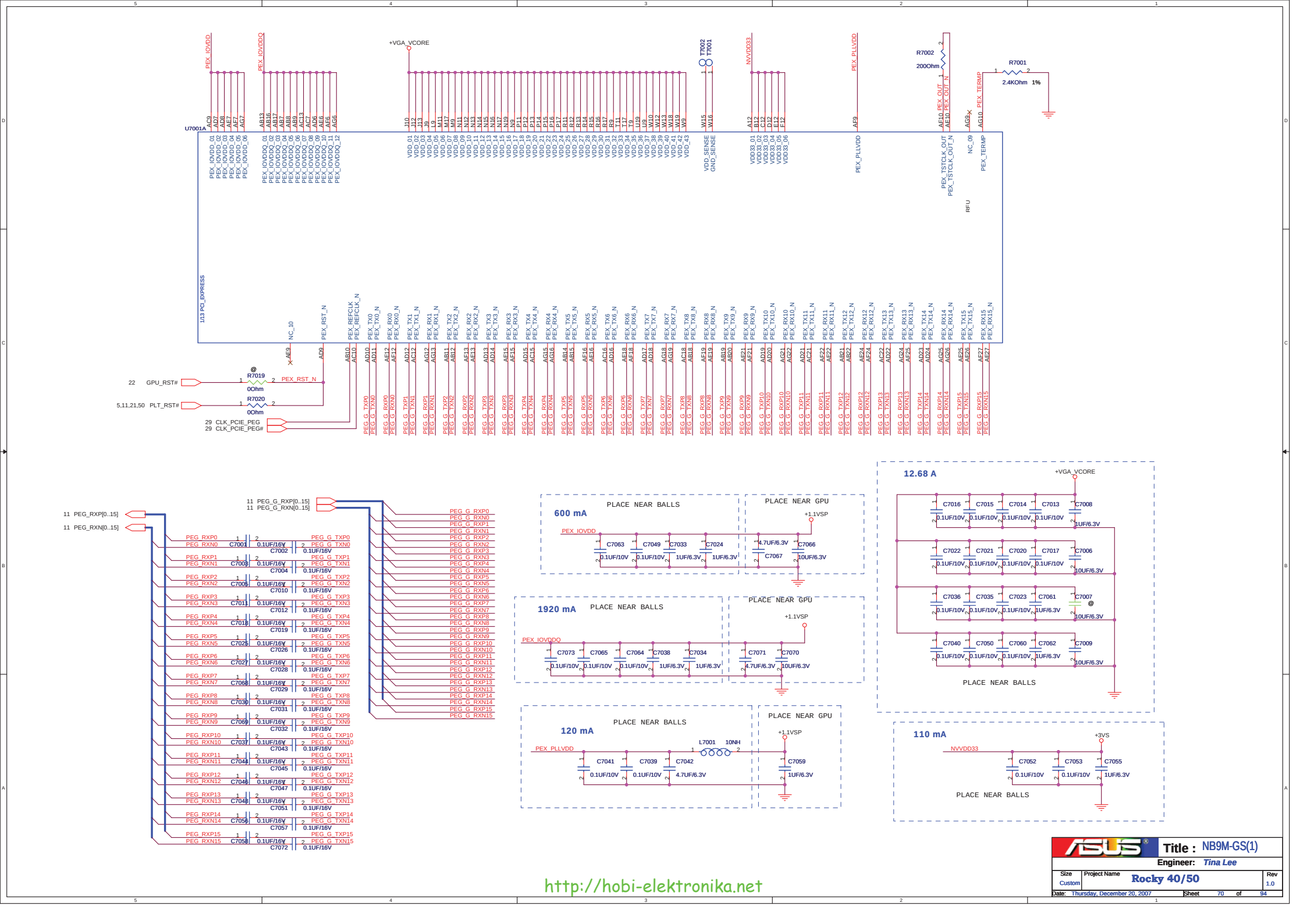
Title : XDP		
Engineer: *Tina Lee*		
Size: A4	Project Name: **Rocky 40/50**	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 68 of 94	



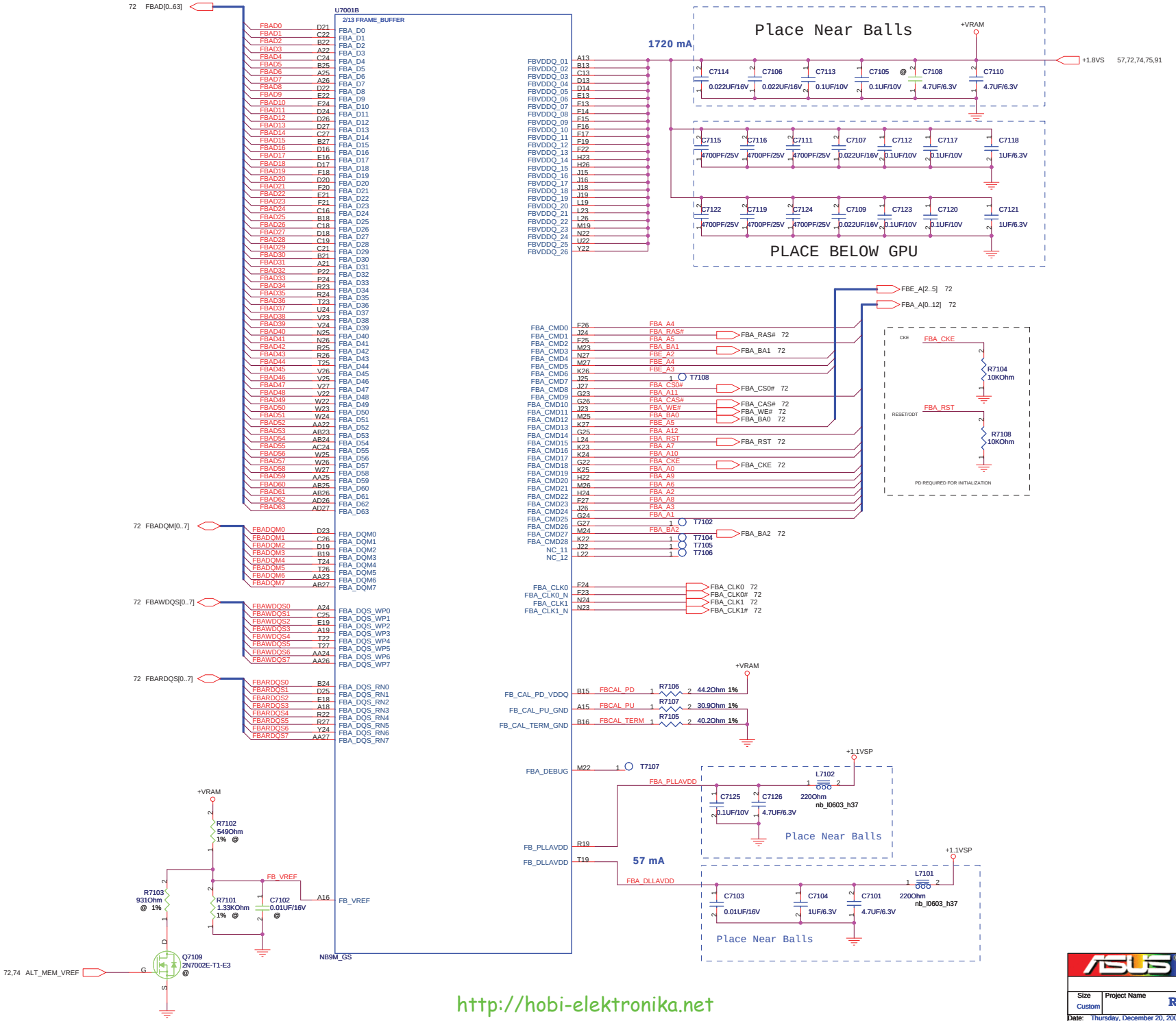
Power On Sequence

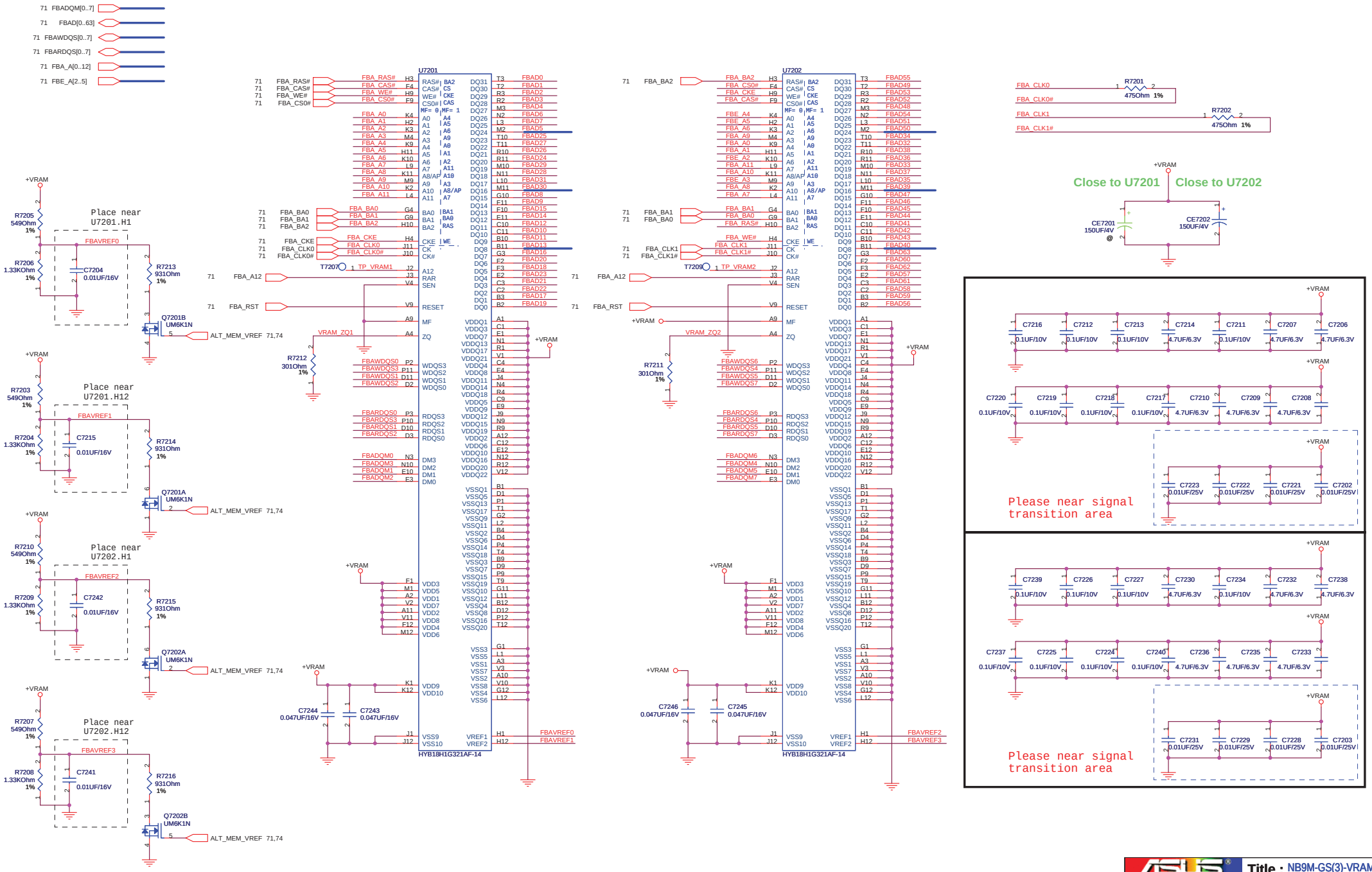
1 → 17

ASUS	Title : Power Sequence	
	Engineer: Tina Lee	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 69 of 94	



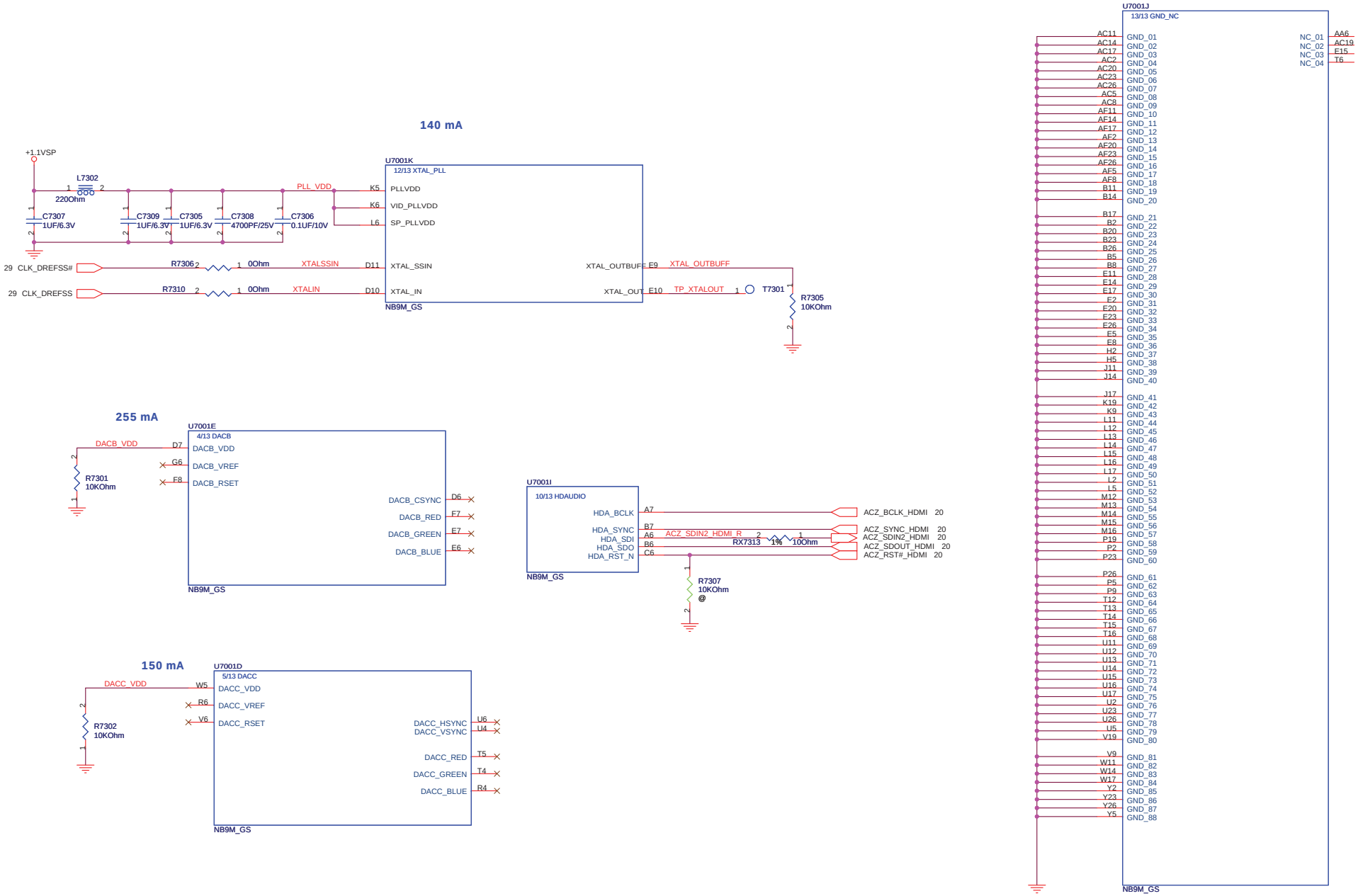
Title : NB9M-GS(1)			
Engineer: Tina Lee			
Size: Custom	Project Name: Rocky 40/50		Rev: 1.0
Date: Thursday, December 20, 2007		Sheet 70 of 94	


72 FBAD[0..63]
U7001B
2/13 FRAME_BUFFER
FBAD0 D21
FBAD1 C22
FBAD2 B22
FBAD3 A22
FBAD4 C24
FBAD5 B25
FBAD6 A25
FBAD7 A26
FBAD8 D22
FBAD9 E22
FBAD10 E24
FBAD11 D24
FBAD12 D26
FBAD13 D27
FBAD14 C27
FBAD15 B27
FBAD16 D16
FBAD17 E16
FBAD18 D17
FBAD19 E18
FBAD20 D20
FBAD21 F20
FBAD22 E21
FBAD23 F21
FBAD24 C16
FBAD25 B18
FBAD26 C18
FBAD27 D18
FBAD28 C19
FBAD29 C21
FBAD30 B21
FBAD31 A21
FBAD32 P22
FBAD33 P24
FBAD34 R23
FBAD35 R24
FBAD36 T23
FBAD37 U24
FBAD38 V23
FBAD39 V24
FBAD40 N25
FBAD41 N26
FBAD42 R25
FBAD43 R26
FBAD44 T25
FBAD45 V26
FBAD46 V25
FBAD47 V27
FBAD48 V22
FBAD49 W22
FBAD50 W23
FBAD51 W24
FBAD52 AA22
FBAD53 AB23
FBAD54 AB24
FBAD55 AC24
FBAD56 W25
FBAD57 W26
FBAD58 W27
FBAD59 AA25
FBAD60 AB25
FBAD61 AB26
FBAD62 AD26
FBAD63 AD27
FBA_D0
FBA_D1
FBA_D2
FBA_D3
FBA_D4
FBA_D5
FBA_D6
FBA_D7
FBA_D8
FBA_D9
FBA_D10
FBA_D11
FBA_D12
FBA_D13
FBA_D14
FBA_D15
FBA_D16
FBA_D17
FBA_D18
FBA_D19
FBA_D20
FBA_D21
FBA_D22
FBA_D23
FBA_D24
FBA_D25
FBA_D26
FBA_D27
FBA_D28
FBA_D29
FBA_D30
FBA_D31
FBA_D32
FBA_D33
FBA_D34
FBA_D35
FBA_D36
FBA_D37
FBA_D38
FBA_D39
FBA_D40
FBA_D41
FBA_D42
FBA_D43
FBA_D44
FBA_D45
FBA_D46
FBA_D47
FBA_D48
FBA_D49
FBA_D50
FBA_D51
FBA_D52
FBA_D53
FBA_D54
FBA_D55
FBA_D56
FBA_D57
FBA_D58
FBA_D59
FBA_D60
FBA_D61
FBA_D62
FBA_D63
72 FBADQM[0..7]
FBADQM0 D23
FBADQM1 C26
FBADQM2 D19
FBADQM3 B19
FBADQM4 T24
FBADQM5 T26
FBADQM6 AA23
FBADQM7 AB27
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
72 FBAWDQS[0..7]
FBAWDQS0 A24
FBAWDQS1 C25
FBAWDQS2 E19
FBAWDQS3 A19
FBAWDQS4 T22
FBAWDQS5 T27
FBAWDQS6 AA24
FBAWDQS7 AA26
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
72 FBARDQS[0..7]
FBARDQS0 B24
FBARDQS1 D25
FBARDQS2 E18
FBARDQS3 A18
FBARDQS4 R22
FBARDQS5 R27
FBARDQS6 Y24
FBARDQS7 AA27
FBA_DQS_RN0
FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7
NB9M_GS
1720 mA
FBVDDQ_01 A13
FBVDDQ_02 B13
FBVDDQ_03 C13
FBVDDQ_04 D13
FBVDDQ_05 D14
FBVDDQ_06 E13
FBVDDQ_07 F13
FBVDDQ_08 F14
FBVDDQ_09 F15
FBVDDQ_10 F16
FBVDDQ_11 F17
FBVDDQ_12 F19
FBVDDQ_13 F22
FBVDDQ_14 H23
FBVDDQ_15 H26
FBVDDQ_16 J15
FBVDDQ_17 J16
FBVDDQ_18 J18
FBVDDQ_19 J19
FBVDDQ_20 L19
FBVDDQ_21 L23
FBVDDQ_22 L26
FBVDDQ_23 M19
FBVDDQ_24 N22
FBVDDQ_25 U22
FBVDDQ_26 Y22
Place Near Balls
+VRAM
C7114 0.022UF/16V
C7106 0.022UF/16V
C7113 0.1UF/10V
C7105 @ 0.1UF/10V
C7108 4.7UF/6.3V
C7110 4.7UF/6.3V
+1.8VS 57,72,74,75,91
C7115 4700PF/25V
C7116 4700PF/25V
C7111 4700PF/25V
C7107 0.022UF/16V
C7112 0.1UF/10V
C7117 0.1UF/10V
C7118 1UF/6.3V
C7122 4700PF/25V
C7119 4700PF/25V
C7124 4700PF/25V
C7109 0.022UF/16V
C7123 0.1UF/10V
C7120 0.1UF/10V
C7121 1UF/6.3V
PLACE BELOW GPU
FBE_A[2..5] 72
FBA_A[0..12] 72
FBA_CMD0 F26 FBA_A4
FBA_CMD1 J24 FBA_RAS# FBA_RAS# 72
FBA_CMD2 F25 FBA_A5
FBA_CMD3 M23 FBA_BA1 FBA_BA1 72
FBA_CMD4 N27 FBE_A2
FBA_CMD5 M27 FBE_A4
FBA_CMD6 K26 FBE_A3
FBA_CMD7 J25 T7108
FBA_CMD8 J27 FBA_CS0# FBA_CS0# 72
FBA_CMD9 G23 FBA_A11
FBA_CMD10 G26 FBA_CAS# FBA_CAS# 72
FBA_CMD11 J23 FBA_WE# FBA_WE# 72
FBA_CMD12 M25 FBA_BA0 FBA_BA0 72
FBA_CMD13 K27 FBE_A5
FBA_CMD14 G25 FBA_A12
FBA_CMD15 L24 FBA_RST FBA_RST 72
FBA_CMD16 K23 FBA_A7
FBA_CMD17 K24 FBA_A10
FBA_CMD18 G22 FBA_CKE FBA_CKE 72
FBA_CMD19 K25 FBA_A0
FBA_CMD20 H22 FBA_A9
FBA_CMD21 M26 FBA_A6
FBA_CMD22 H24 FBA_A2
FBA_CMD23 F27 FBA_A8
FBA_CMD24 J26 FBA_A3
FBA_CMD25 G24 FBA_A1
FBA_CMD26 G27 T7102
FBA_CMD27 M24 FBA_BA2 FBA_BA2 72
FBA_CMD28 K22 T7104
NC_11 J22 T7105
NC_12 L22 T7106
CKE
FBA_CKE
R7104 10KOhm
RESET/ODT
FBA_RST
R7108 10KOhm
PD REQUIRED FOR INITIALIZATION
FBA_CLK0 F24 FBA_CLK0 72
FBA_CLK0_N F23 FBA_CLK0# 72
FBA_CLK1 N24 FBA_CLK1 72
FBA_CLK1_N N23 FBA_CLK1# 72
+VRAM
FB_CAL_PD_VDDQ B15 FBCAL_PD R7106 44.2Ohm 1%
FB_CAL_PU_GND A15 FBCAL_PU R7107 30.9Ohm 1%
FB_CAL_TERM_GND B16 FBCAL_TERM R7105 40.2Ohm 1%
FBA_DEBUG M22 T7107
+1.1VSP
FBA_PLLAVDD
L7102 220Ohm nb_l0603_h37
C7125 0.1UF/10V
C7126 4.7UF/6.3V
Place Near Balls
FB_PLLAVDD R19
FB_DLLAVDD T19
57 mA
FBA_DLLAVDD
+1.1VSP
L7101 220Ohm nb_l0603_h37
C7103 0.01UF/16V
C7104 1UF/6.3V
C7101 4.7UF/6.3V
Place Near Balls
+VRAM
R7102 549Ohm 1% @
R7103 931Ohm @ 1%
R7101 1.33KOhm 1% @
FB_VREF
C7102 0.01UF/16V @
A16 FB_VREF
72,74 ALT_MEM_VREF
Q7109 2N7002E-T1-E3 @
G
D
S
http://hobi-elektronika.net
ASUS
Title : NB9M-GS(2)
Engineer: Tina Lee
Size Custom
Project Name Rocky 40/50
Rev 1.0
Date: Thursday, December 20, 2007
Sheet 71 of 94



http://hobi-elektronika.net

Title : NB9M-GS(3)-VRAM			
Engineer: Tina Lee			
Size: Custom	Project Name: Rocky 40/50		Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 72 of 94		



Title : NB9M-GS(4)		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 73 of 94	

DDCA: CRT
DDCB: HDMI
DDCC: LVDS/THERMAL

U7001M
9/13 I2C_GPIO_THERM_JTAG

50 VGA_THERM_DC — VGA_THERM_DC — D8 THERMDN
50 VGA_THERM_DA — VGA_THERM_DA — D9 THERMDP

T7415 TP_JTAG_TCK AF3 JTAG_TCK
T7416 TP_JTAG_TMS AF4 JTAG_TMS
T7417 TP_JTAG_TDI AG4 JTAG_TDI
T7402 TP_JTAG_TDO AE4 JTAG_TDO
R7409 1KOhm JTAG_TRST_N AG3 JTAG_TRST_N

+3VS — R7445 10KOhm I2CS_SCL_VGA T1 I2CS_SCL
+3VS — R7444 10KOhm I2CS_SDA_VGA T2 I2CS_SDA

I2CA_SCL / I2CA_SDA — R1 I2CA_SCL_VGA 1% — R7415 33Ohm — CRT_DDC_CLK 45
T3 I2CA_SDA_VGA 1% — R7416 33Ohm — CRT_DDC_DAT 45

I2CB_SCL / I2CB_SDA — R2 I2CB_SCL_VGA 1% — R7423 33Ohm — HDMI_CLK 48
R3 I2CB_SDA_VGA 1% — R7425 33Ohm — HDMI_DAT 48

I2CC_SCL / I2CC_SDA — A2 I2CC_SCL_VGA — R7405 33Ohm
B1 I2CC_SDA_VGA — R7406 33Ohm

+3VS — R7404 2.2KOhm — R7403 2.2KOhm — EDID_CLK 46 / EDID_DAT 46

I2CD_SCL / I2CD_SDA — N2 I2CD_SCL_VGA — R7440 10KOhm
N3 I2CD_SDA_VGA — R7441 10KOhm

I2CE_SCL / I2CE_SDA — Y6 I2CE_SCL_VGA — R7443 10KOhm
W6 I2CE_SDA_VGA — R7442 10KOhm

GPIO0 N1 TP_GPU_GPIO0 — T7407 — HOTPLUG 48
GPIO1 G1 HOTPLUG
GPIO2 C1 TP_GPU_GPIO2 — T7401
GPIO3 M2 LCD_VDD_EN
GPIO4 M3 LCD_BACKEN
GPIO5 K3 GPU_VID0 — GPU_VID0 85
GPIO6 K2 GPU_VID1 — GPU_VID1 85
GPIO7 J2 TP_GPU_VID2 — T7409
GPIO8 C2 NV_OVERT# R — R7401 0Ohm — NV_OVERT# 30
GPIO9 M1 TP_GPU_GPIO9 — T7403
GPIO10 D2 ALT_MEM_VREF_VGA — R7434 0Ohm — ALT_MEM_VREF 71,72
GPIO11 D1 TP_GPU_GPIO11 — T7405
GPIO12 J3 TP_GPU_GPIO12 — T7406
GPIO13 J1
GPIO14 K1
GPIO15 F3
GPIO16 G3
GPIO17 G2
GPIO18 F1
GPIO19 F2

+3VS — R7414 2KOhm 1% — R7448 2KOhm 1%
+3VS — R7402 10KOhm @
C7423 0.1UF/10V — R7435 10KOhm

NB9M_GS

LCD_VDD_EN — LCD_VDD_EN 46
LCD_BACKEN — LCD_BACKEN 46
R7412 10KOhm — R7413 10KOhm

U7001L
11/13 MISC

+3VS — R7424 10KOhm 1% — R7428 10KOhm 1% @ — R7430 45.3KOhm 1%
R7427 10KOhm 1% @ — R7429 10KOhm 1% — R7431 10KOhm 1% @

STRAP0_VGA — C7 STRAP0
STRAP1_VGA — B9 STRAP1
STRAP2_VGA — A9 STRAP2

R7407 40.2KOhm 1% — F11 STRAP_REF_3V3
R7408 40.2KOhm 1% — F10 STRAP_REF_MIOB

+3VS — R7410 24.3KOhm 1% — SPDIF_VGA — F9 SPDIF
36 SPDIF_OUT — C7422 0.1UF/10V @ — R7419 3.4KOhm 1%
C15 NC_05
D15 NC_06

ROM_CS_N — B10 — T7410
ROM_SI — A10 — ROM_SI_VGA
ROM_SO — C10 — ROM_SO_VGA
ROM_SCLK — C9 — ROM_SCLK_VGA

+3VS — R7436 10KOhm 1% @ — R7438 4.99KOhm 1% — R7432 10KOhm 1% @
+3VS — R7437 30KOhm 1% — R7439 10KOhm 1% @ — R7433 15KOhm 1%

I2CH_SCL / I2CH_SDA — A3 / A4
+3VS — R7421 10KOhm — R7446 10KOhm
I2CH_SCL_VGA
I2CH_SDA_VGA

BUFRST_N — N5 — T7414
NC_07 — J5
NC_08 — F6
TESTMODE — AD25 TESTMODE — R7411 10KOhm
GND_89 — AC6

+3VS — C7402 0.1UF/10V — +3VS_HDCP

HDCP ROM
U7401
VCC NC1
NC4 NC2
SCL NC3
SDA GND
AT88SC0808C-SU

R7422 10KOhm @

NB9M_GS

U7001G
8/13 IFPE

IFPE_PLLVDD_VGA — N6 IFPE_PLLVDD
M6 IFPE_RSET
R7447 10KOhm

IFPE_IOVDD_VGA — H6 IFPE_IOVDD
R7420 1KOhm

DVI / DP
E
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2

IFPE_AUX_N — D4
IFPE_AUX — D3
IFPE_L3_N — B4
IFPE_L3 — B3
IFPE_L2_N — C4
IFPE_L2 — C3
IFPE_L1_N — D5
IFPE_L1 — E4
IFPE_L0_N — F4
IFPE_L0 — F5

NB9M_GS

STRAP2 (R7424)	
5K	GE
10K	GS

ROM-SI (R7437)	
10K	Qimonda 16M*32
15K	Hynix 16M*32
20K	Samsung 16M*32
30K	Qimonda 32M*32
35K	Hynix 32M*32
45K	Samsung 32M*32

HDMI

+1.8VS — L7402 220Ohm — 160 mA
IFPC_PLLVDD — C7411 1UF/6.3V — C7412 1UF/6.3V — C7413 4700PF/25V — C7414 470PF/50V
IFPC_RSET — R7426 1KOhm

+1.1VSP — L7403 220Ohm — 385 mA
IFPC_IOVDD — C7415 1UF/6.3V — C7416 4.7UF/6.3V — C7417 1UF/6.3V — C7418 1UF/6.3V — C7419 4700PF/25V — C7420 470PF/50V — C7421 470PF/50V

U7001H
7/13 IFPC

IFPC_PLLVDD — P6
IFPC_RSET — R5
IFPC_IOVDD — J6

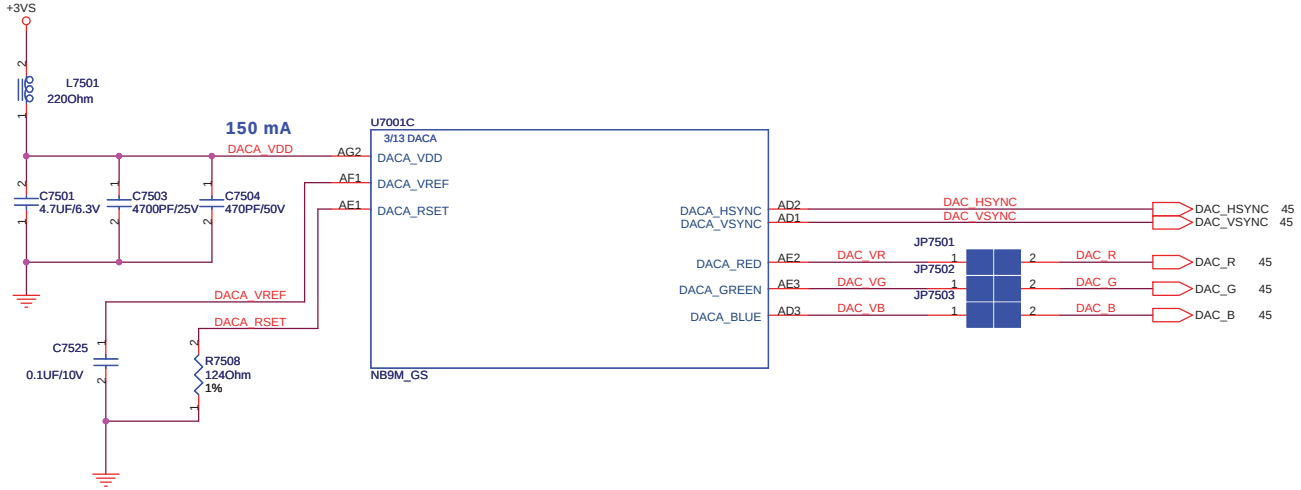
DVI / DP
C
TXC TXC
TXD0 TXD0
TXD1 TXD1
TXD2 TXD2

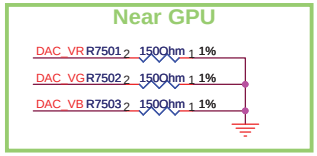
IFPC_AUX_N — G5
IFPC_AUX — G4
IFPC_L3_N — J4
IFPC_L3 — H4
IFPC_L2_N — K4
IFPC_L2 — L4
IFPC_L1_N — M4
IFPC_L1 — M5
IFPC_L0_N — N4
IFPC_L0 — P4

DVI_CLKB- C — C7409 0.1UF/10V — DVI_CLKB-
DVI_CLKB+ C — C7410 0.1UF/10V — DVI_CLKB+ — DVI_CLKB- 48 / DVI_CLKB+ 48
DVI_TX0- C — C7403 0.1UF/10V — DVI_TX0-
DVI_TX0+ C — C7404 0.1UF/10V — DVI_TX0+ — DVI_TX0- 48 / DVI_TX0+ 48
DVI_TX1- C — C7407 0.1UF/10V — DVI_TX1-
DVI_TX1+ C — C7408 0.1UF/10V — DVI_TX1+ — DVI_TX1- 48 / DVI_TX1+ 48
DVI_TX2- C — C7405 0.1UF/10V — DVI_TX2-
DVI_TX2+ C — C7406 0.1UF/10V — DVI_TX2+ — DVI_TX2- 48 / DVI_TX2+ 48

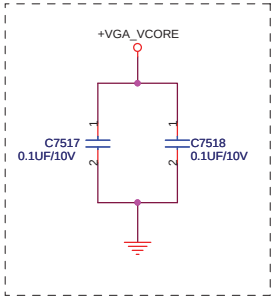
NB9M_GS

ASUS
Title : NB9M-GS(5)
Engineer: Tina Lee
Size: Custom | Project Name: Rocky 40/50 | Rev: 1.0
Date: Thursday, December 20, 2007 | Sheet 74 of 94

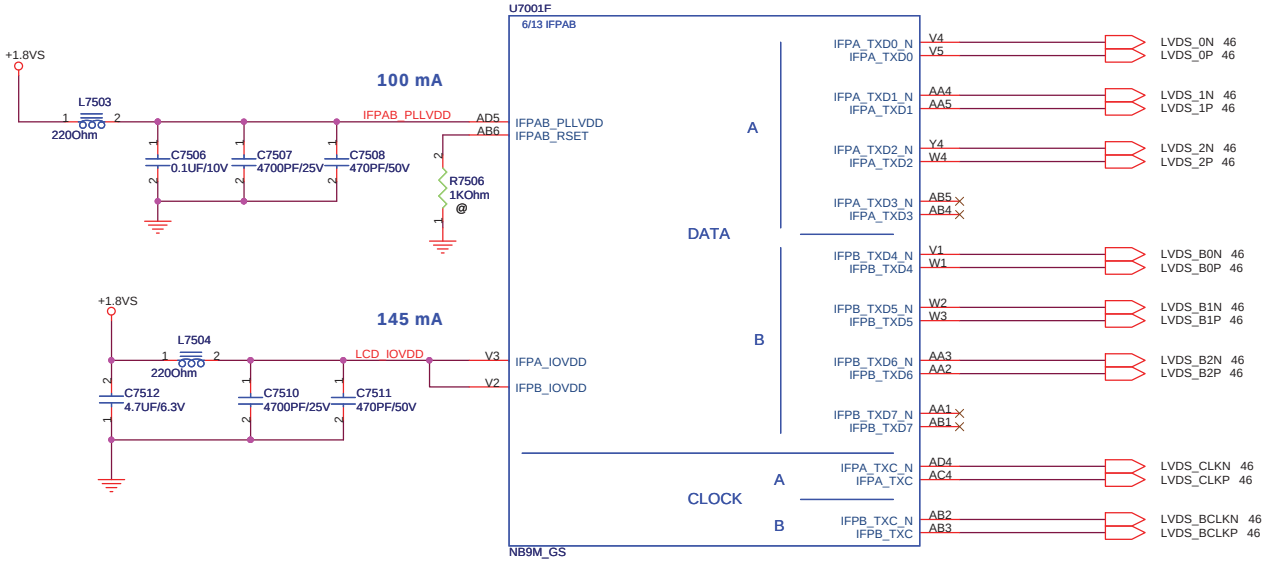




TRANSITION CAPS FOR VSYNC & HSYNC

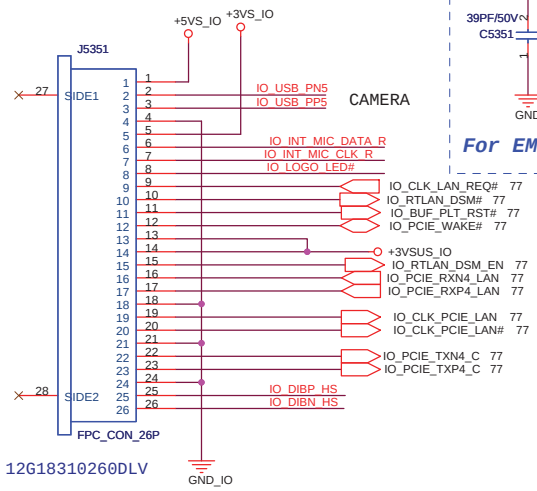


LVDS

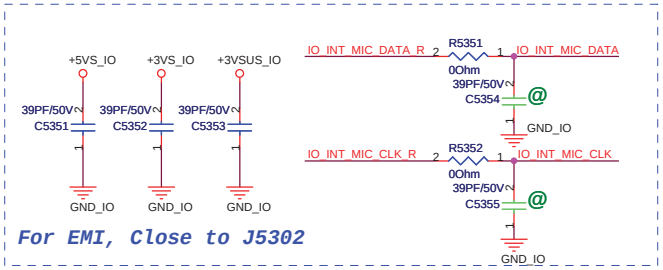


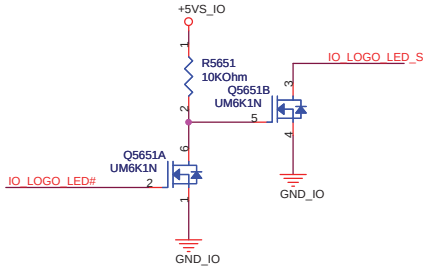
Title : NB9M-GS(6)		
Engineer: Tina Lee		
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 75 of 94	

IO BOARD

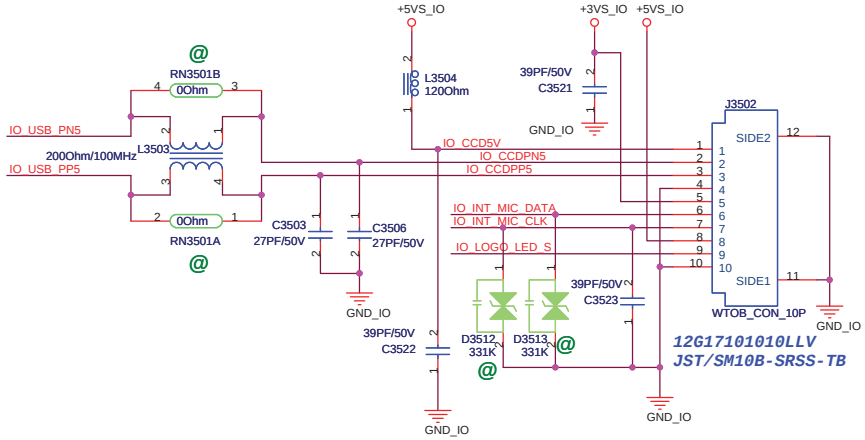


12G18310260DLV

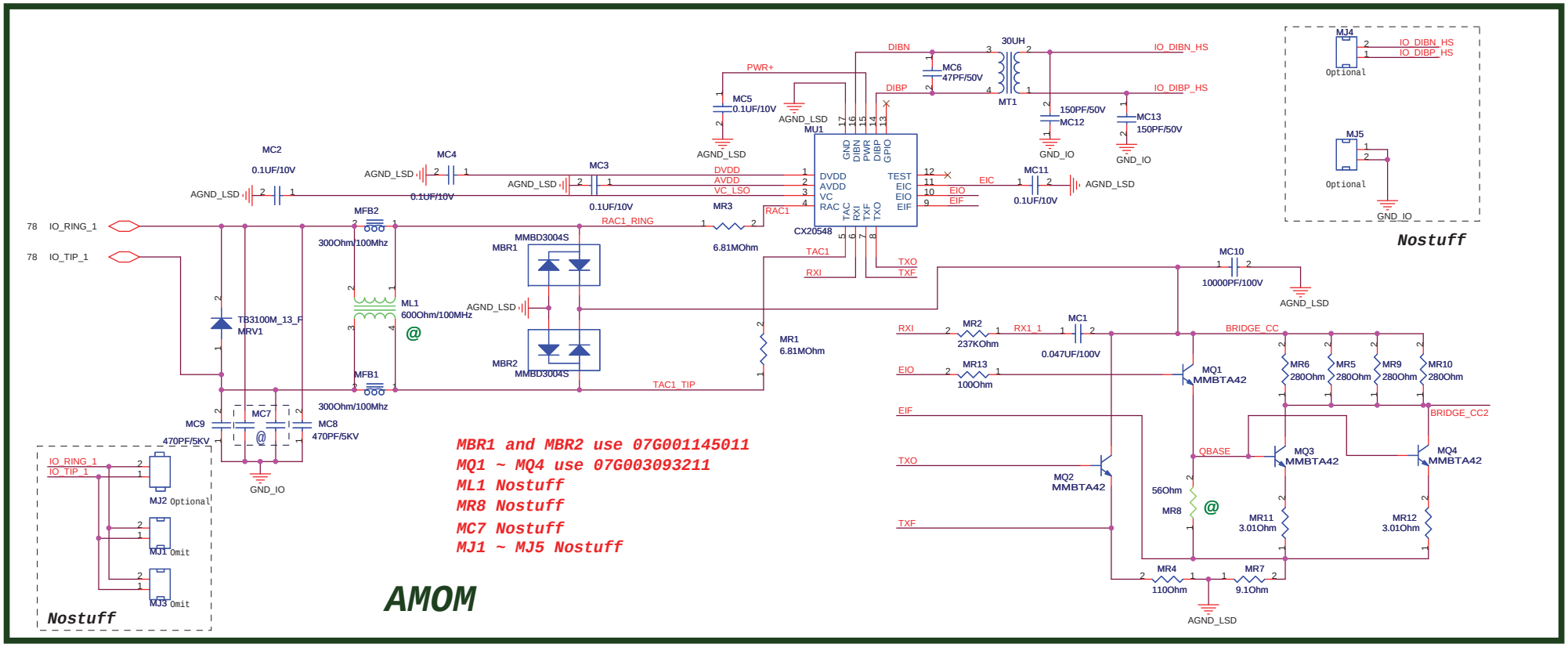




CAMERA

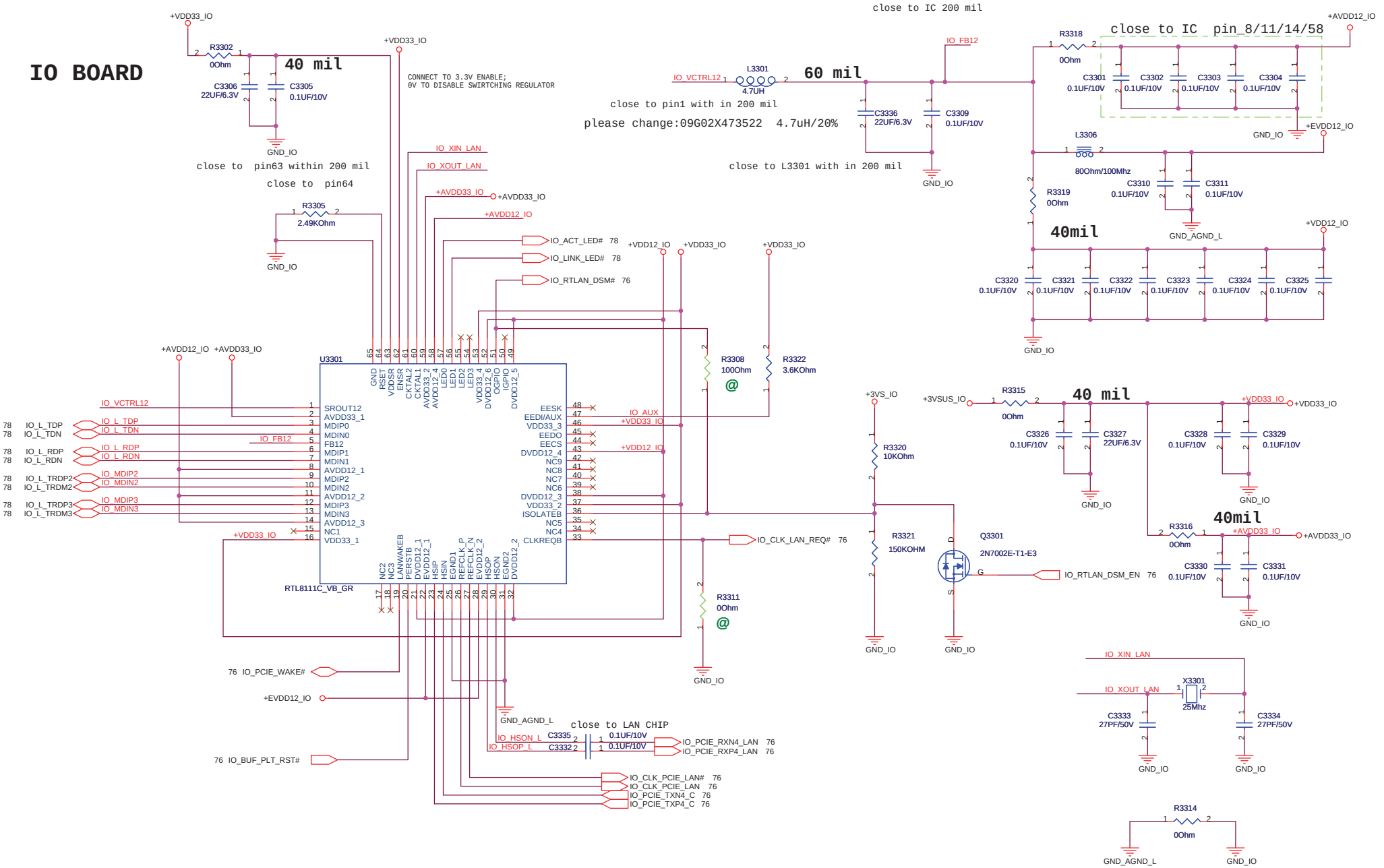


12G17101010LLV
JST/SM10B-SRSS-TB



ASUSALPHA ODM NB1	Title : IO BRD CONN&DAA	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 50 IO Board	Rev: 1.1
Date: Thursday, December 20, 2007	Sheet 76 of 94	

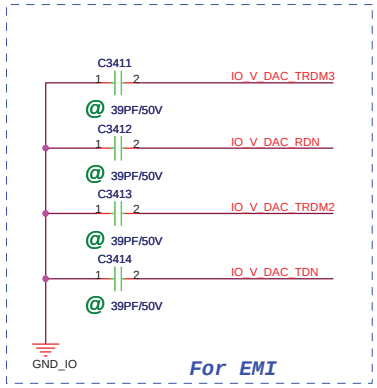
IO BOARD

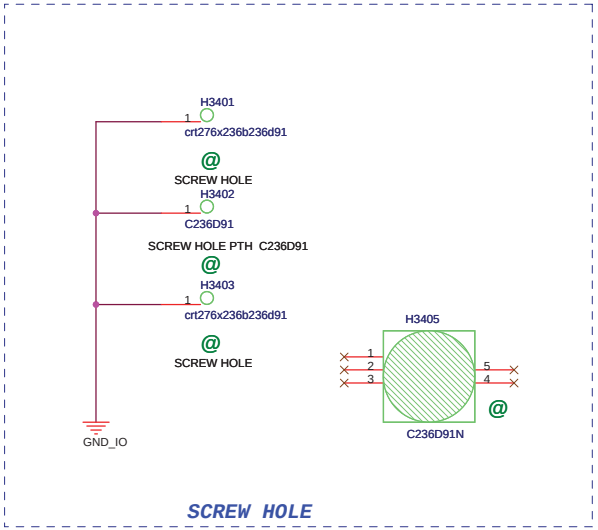


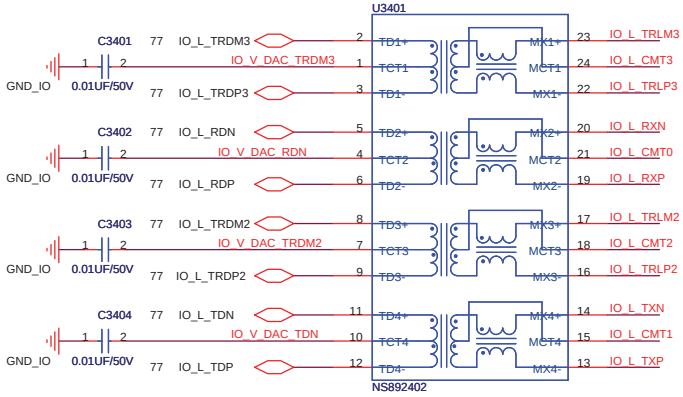
<Variant Name>

ASUSTeK COMPUTER INC	Title : REALTEK 8111C	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 50 IO Board	Rev: 1.1
Date: Thursday, December 20, 2007	Sheet 77 of 94	

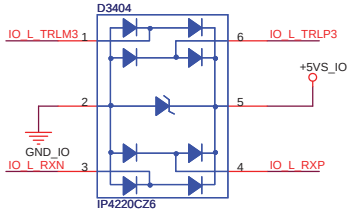
IO BOARD

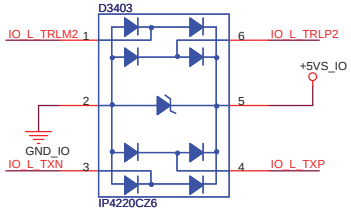


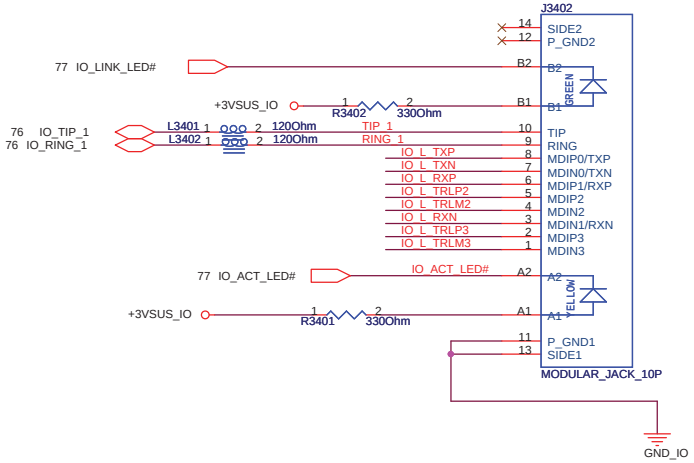


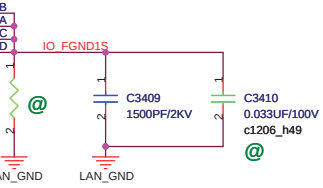


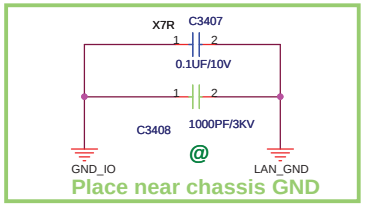
Transformer close CN3402











<variant_name>

ASUSTeK COMPUTER INC	Title : LAN-RJ45	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 50 IO Board	Rev: 1.1
Date: Thursday, December 20, 2007	Sheet 78 of 94	

Title : History

Engineer: Tina Lee

Size	Project Name	Rev
A	Rocky 40/50	1.0

Date: Monday, December 17, 2007 Sheet 79 of 94

IMVP6 CPU VCORE REGULATOR

3.3V level logic level: DPRSLPVR, SHDN#

1.05V level logic: VID, PSI#, DPRSTP#

POUT=(VCSN2-VGNDS)x(CSP1-CNS1+CSP2-CSN2)/16.67mV

FSW=297.8kHz

Slewrate=12.5mV/us

VPS=-2.1mV/A

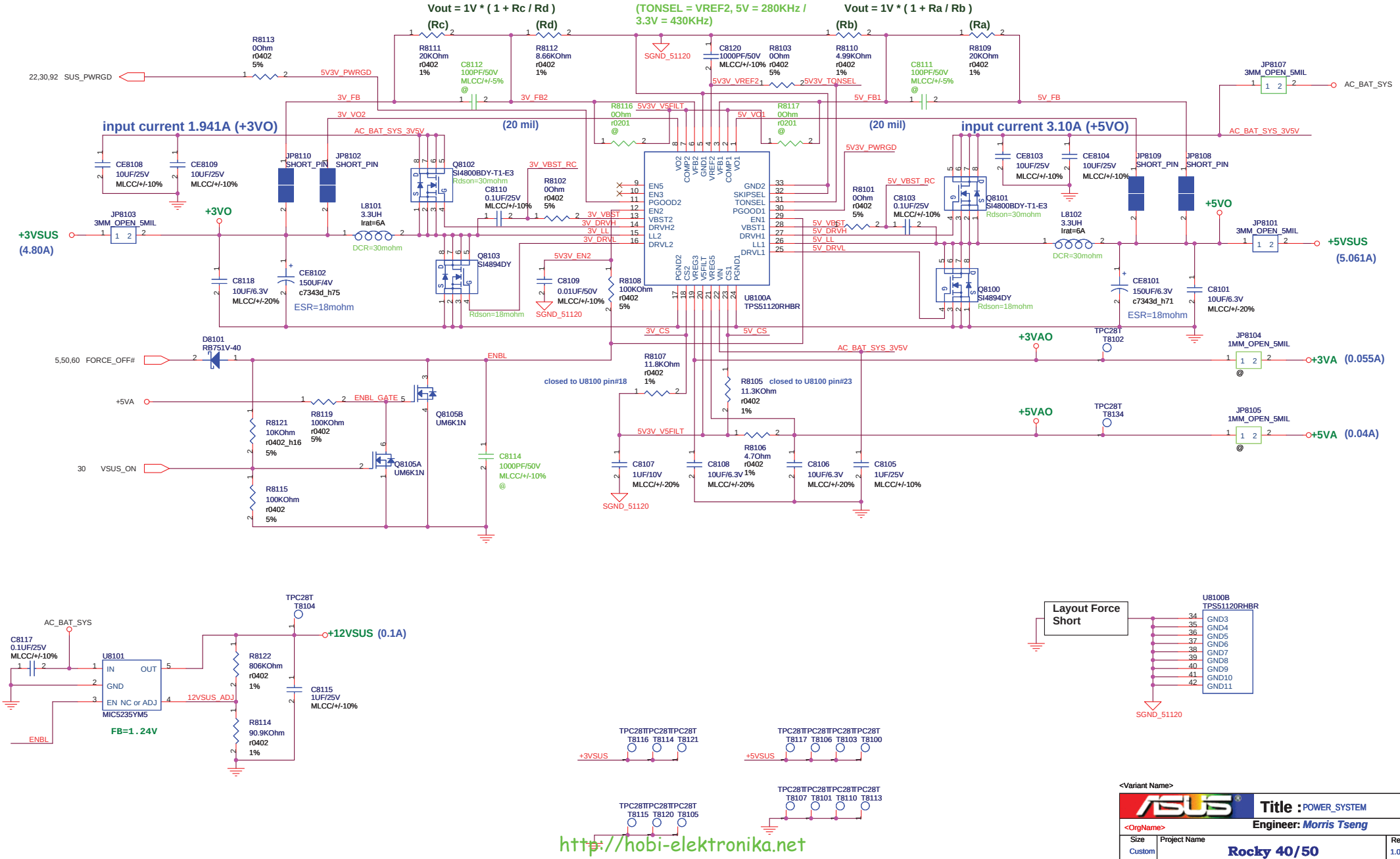
Max input ripple: 5.59A

Max input ripple: 5.59A

Layout Force Short

Title :	POWER_VCORE
<OrgName>	Engineer: Morris Tseng
Size: Custom	Project Name: Rocky 40/50
Rev: 1.0	
Date: Thursday, December 20, 2007	Sheet 80 of 94

+5V / +3.3V POWER SUPPLY



<Variant Name>

Title : POWER_SYSTEM

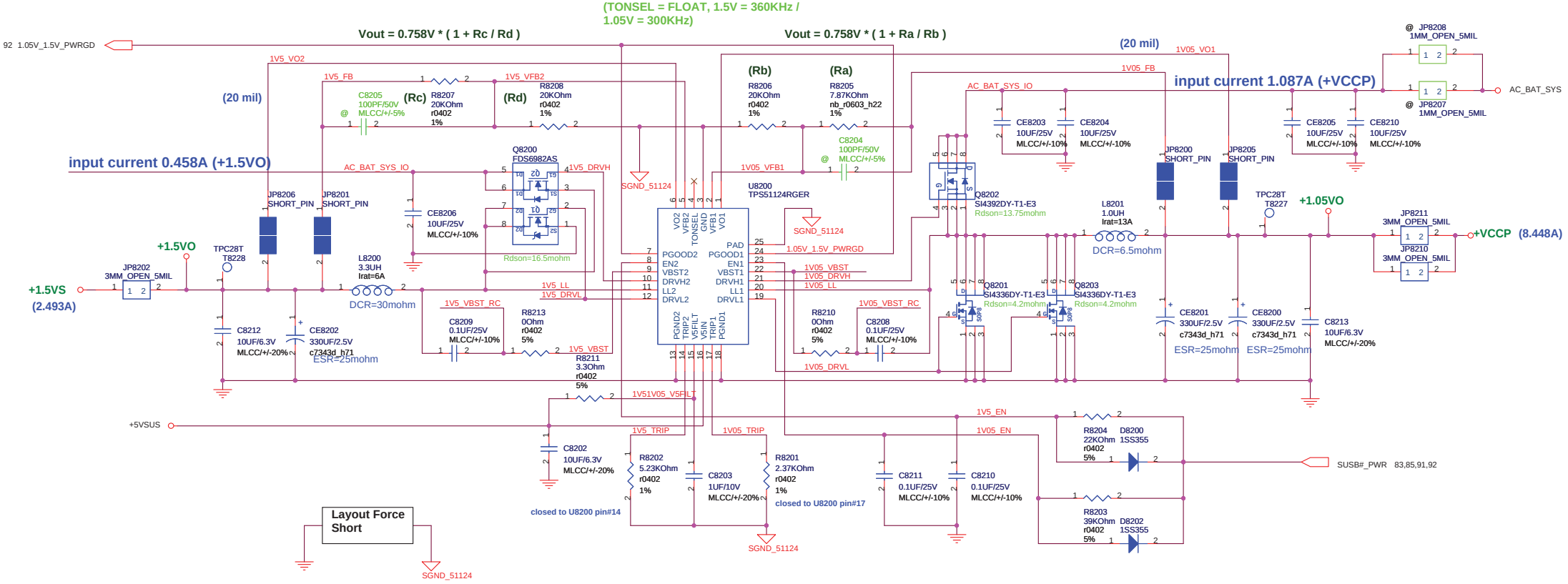
<OrgName>

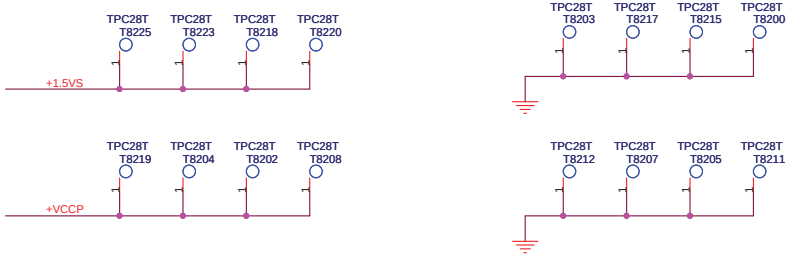
Engineer: Morris Tseng

Size	Project Name	Rev
Custom	Rocky 40/50	1.0

Date: Thursday, December 20, 2007 Sheet 81 of 94

+1.5VS / +VCCP POWER SUPPLY

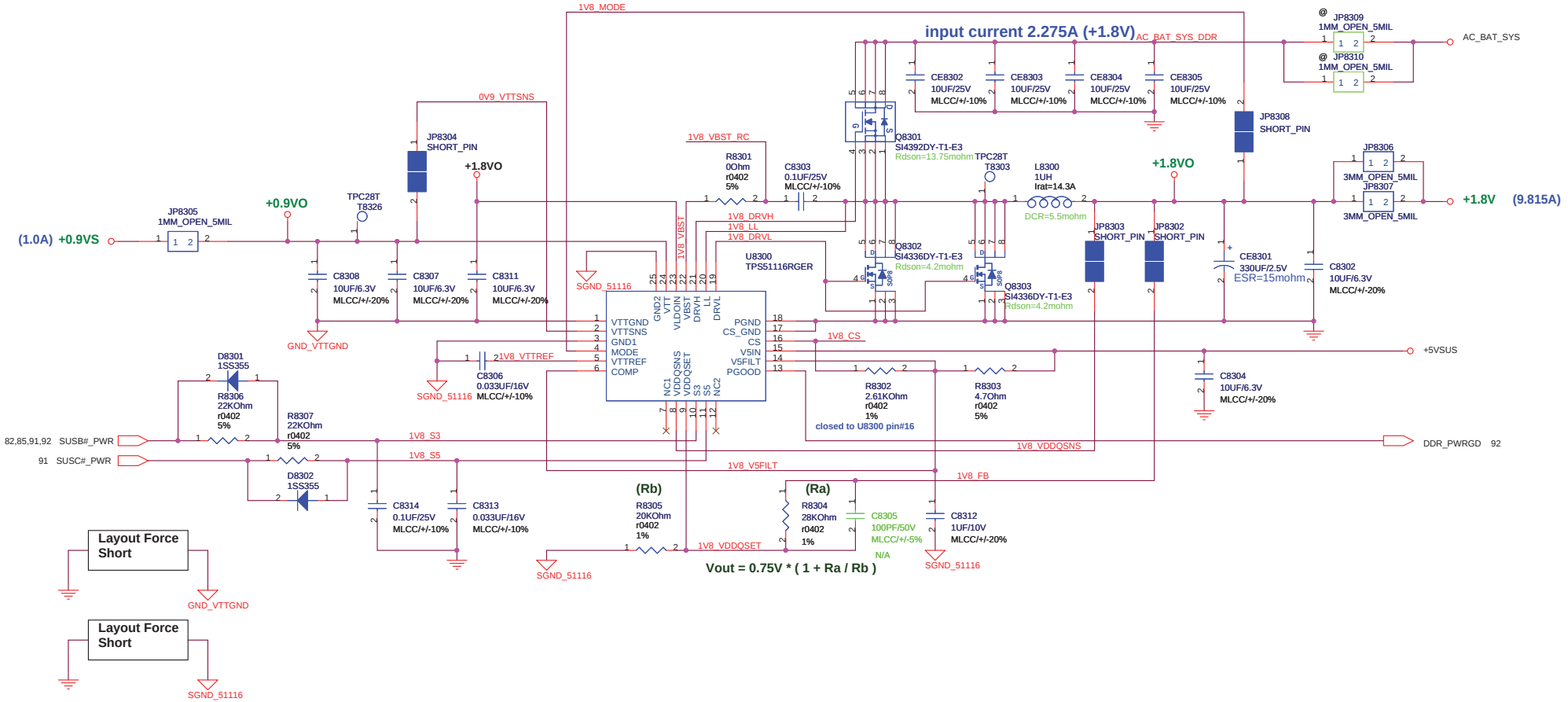


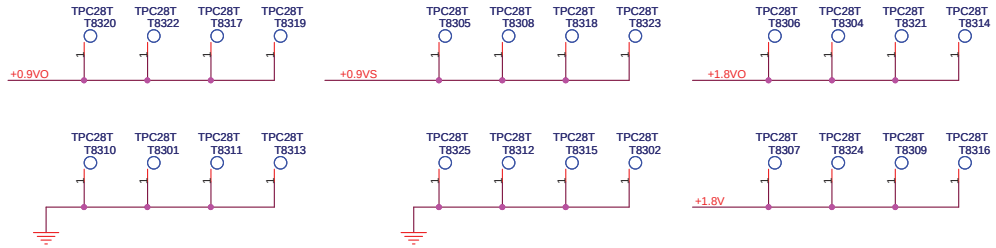


<Variant Name>

Title : POWER_I/O_1.5VS & 1.05VS		
<OrgName>	Engineer: Morris Tseng	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 82 of 94	

+1.8V / +0.9VS POWER SUPPLY





<Variant Name>

Title : POWER_I/O_DDR & VTT

<OrgName>

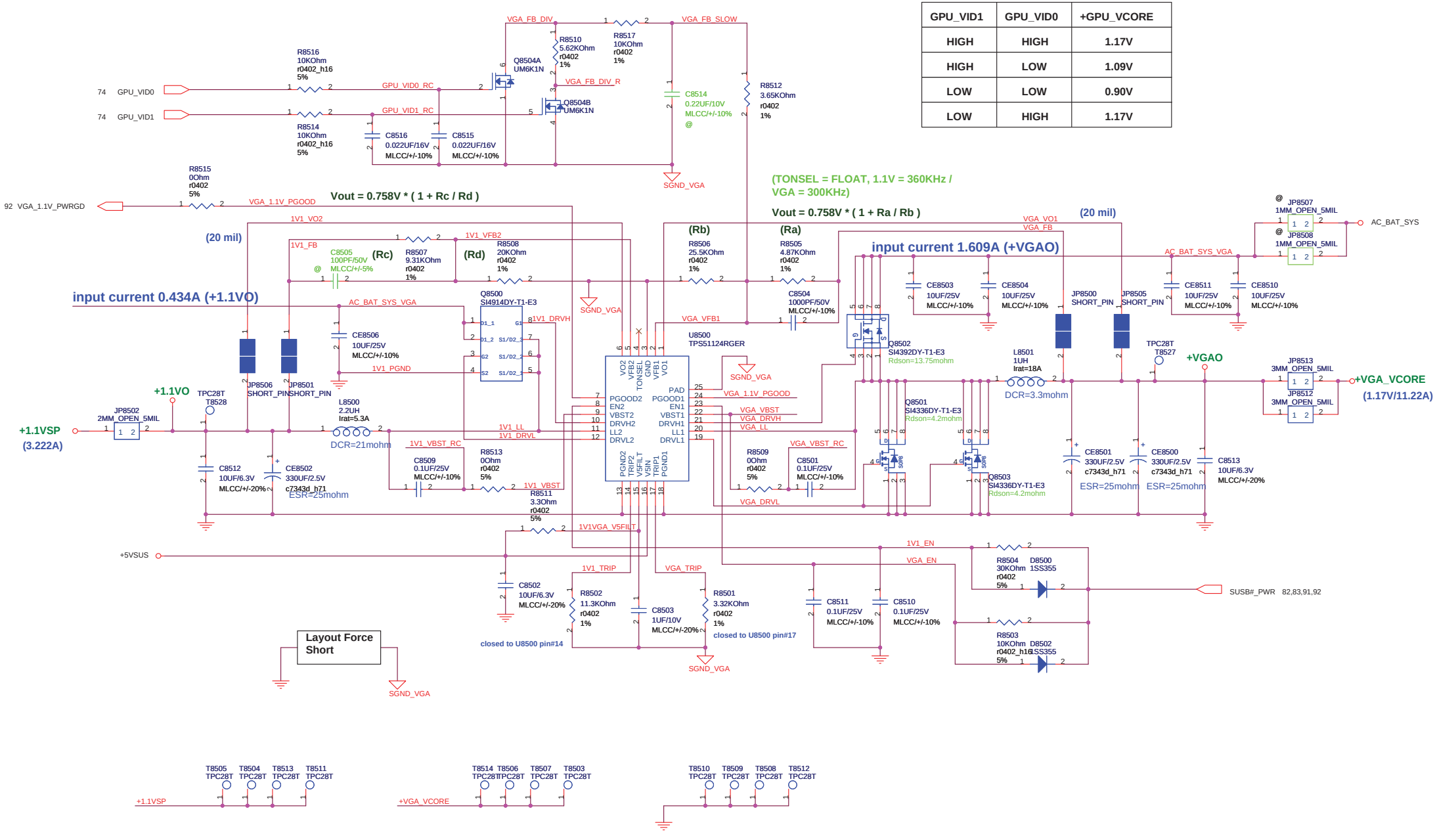
Engineer: Morris Tseng

Size	Project Name	Rev
Custom	Rocky 40/50	1.0

Date: Thursday, December 20, 2007 Sheet 83 of 94

VGA / +1.1V POWER SUPPLY

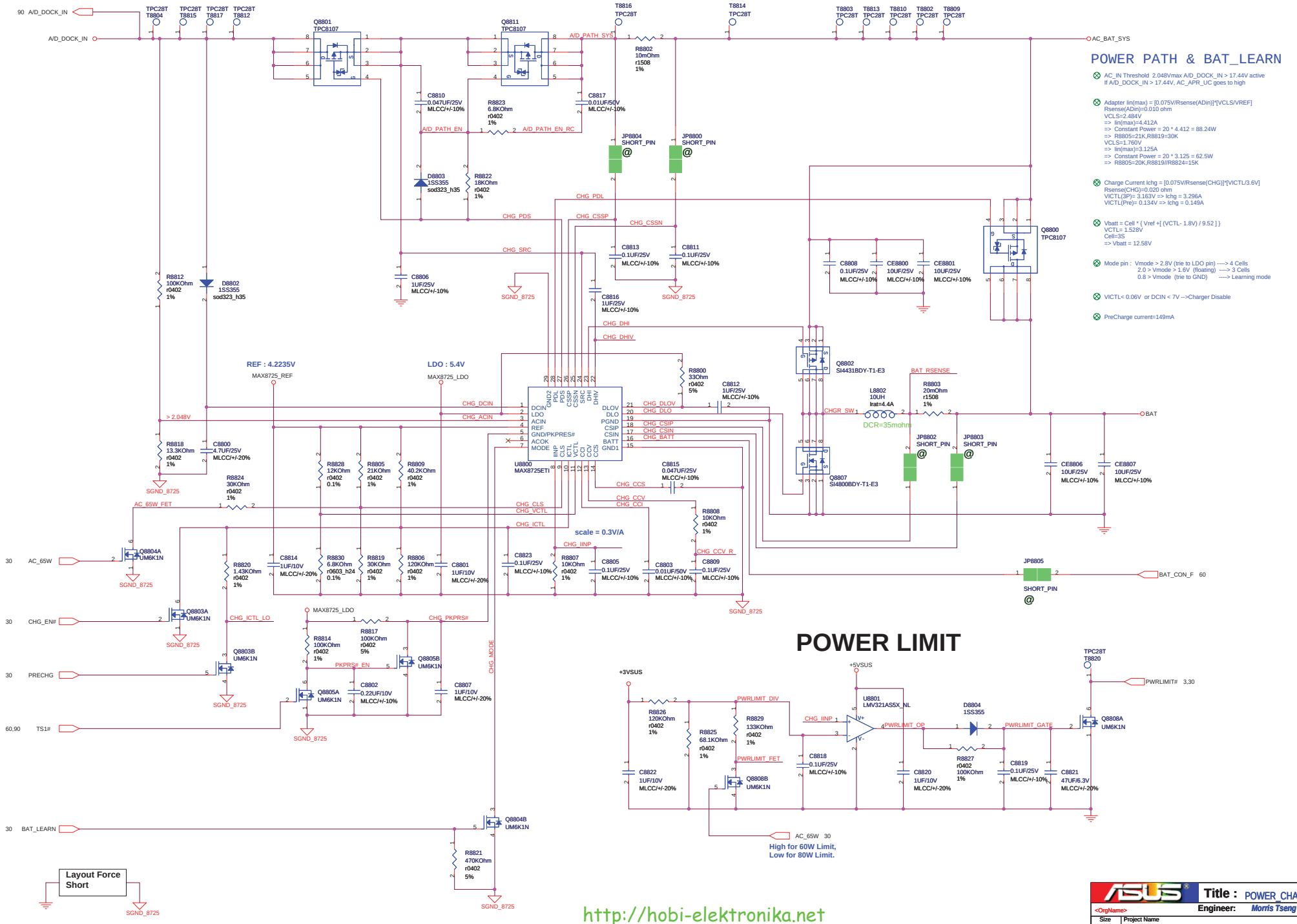
GPU_VID1	GPU_VID0	+GPU_VCORE
HIGH	HIGH	1.17V
HIGH	LOW	1.09V
LOW	LOW	0.90V
LOW	HIGH	1.17V



<OrgName>	Title : PWR_-****	
	Engineer: Morris Tseng	
Size: A4	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 86 of 94	

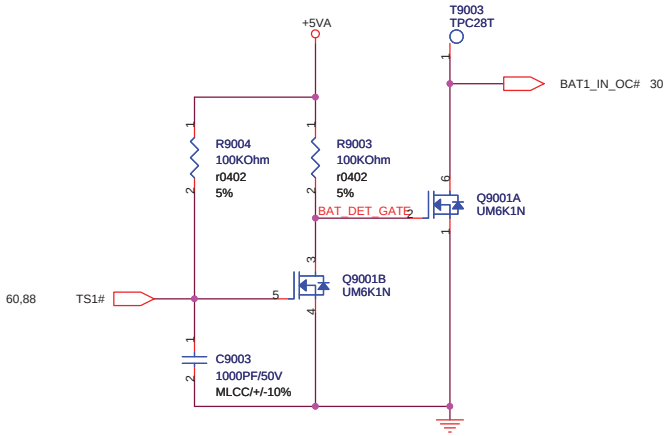
ASUS	Title : POWER_SHUTDOWN#	
<OrgName>	Engineer: Morris Tseng	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 87 of 94	

BATTERY CHARGER

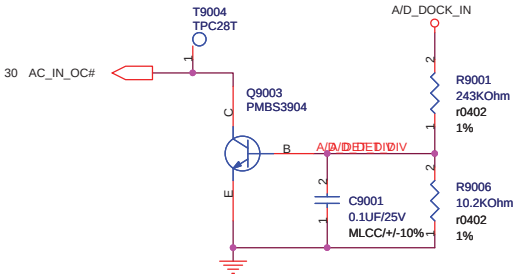


ASUS	Title : POWER_CHARGER	
<OrgName>	Engineer: Morris Tseng	
Size: C	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 88 of 94	

BATTERY IN DETECT

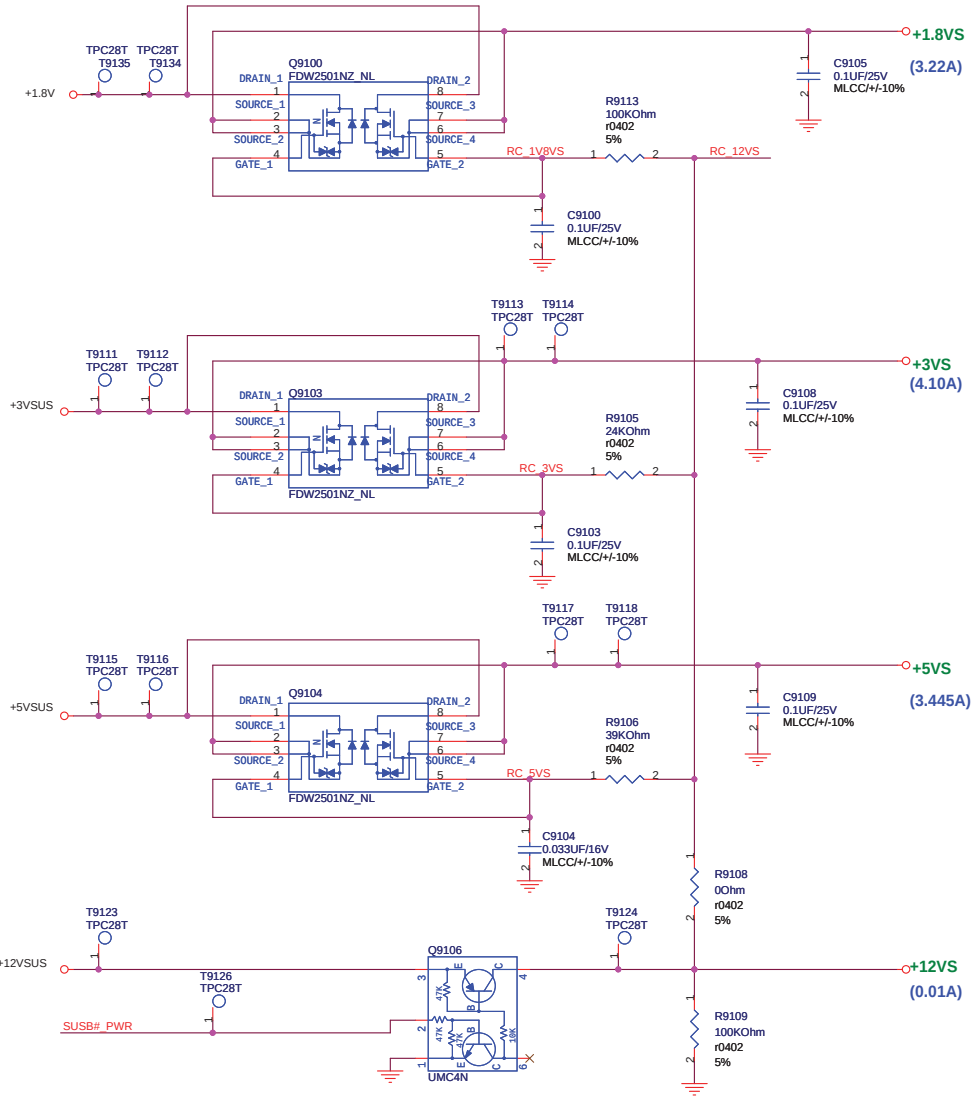


ADAPTER IN DETECT

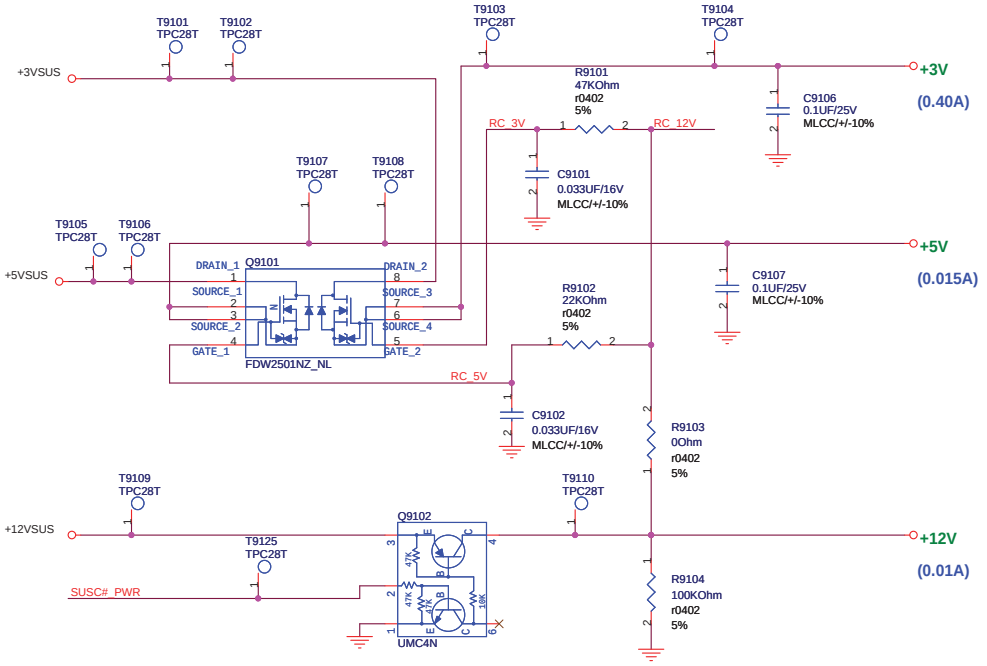


<OrgName>	Title : POWER_DETECT	
	Engineer: Morris Tseng	
Size: A3	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 90 of 94	

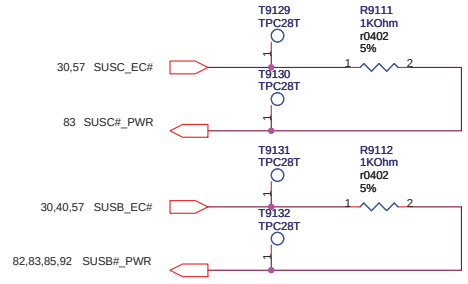
SUSB#_PWR Load SW



SUSC#_PWR Load SW

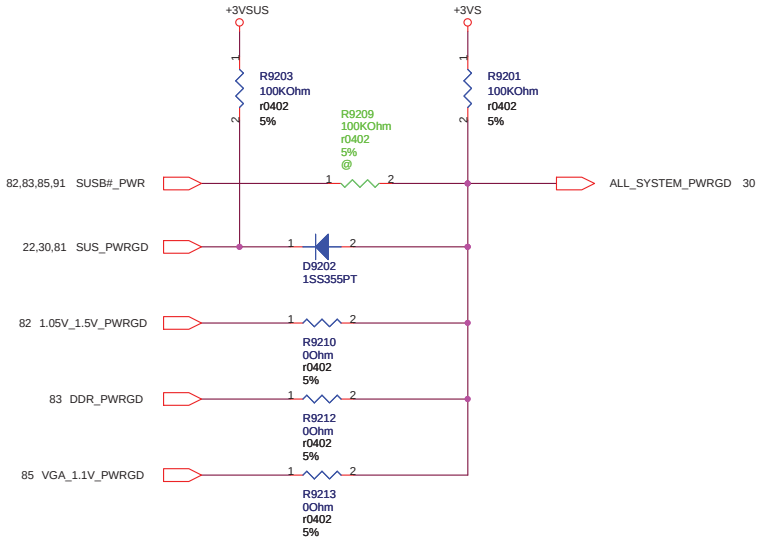


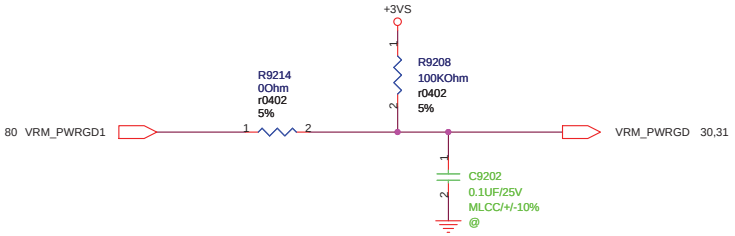
Enable Signal



ASUS	Title :	POWER_LOAD SWITCH
<OrgName>	Engineer:	Morris Tseng
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 91 of 94	

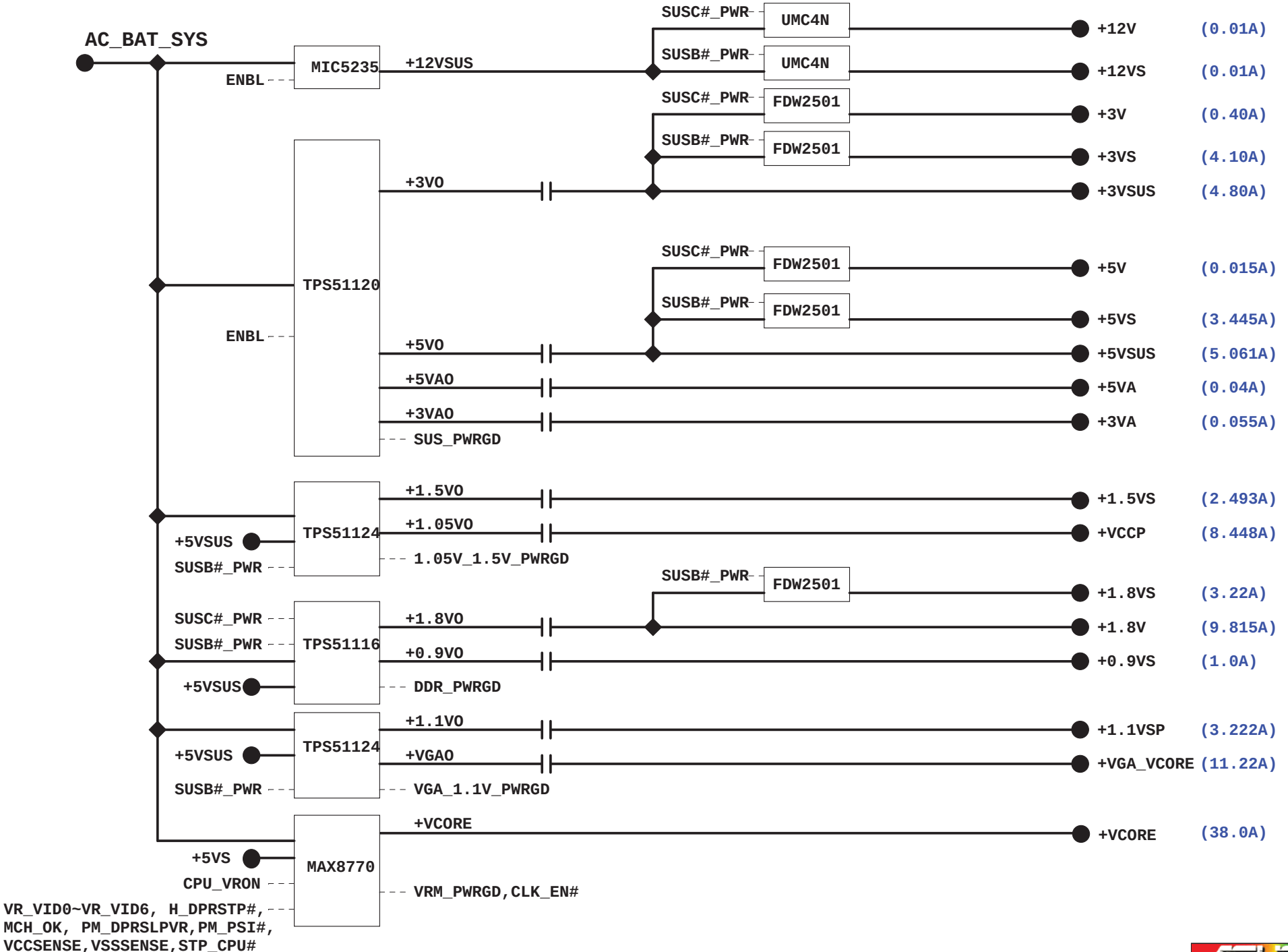
POWER GOOD DETECTER





ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer: Morris Tseng	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 92 of 94	

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer: Morris Tseng	
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Thursday, December 20, 2007	Sheet 93 of 94	



ASUS	Title :	POWER_FLOWCHART
<OrgName>	Engineer:	Morris Tseng
Size: Custom	Project Name: Rocky 40/50	Rev: 1.0
Date: Monday, December 17, 2007	Sheet 94 of 94	