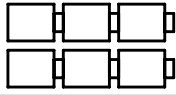


A8N_A8Dc AMD/MCP67MV/MCP67D BLOCK DIAGRAM

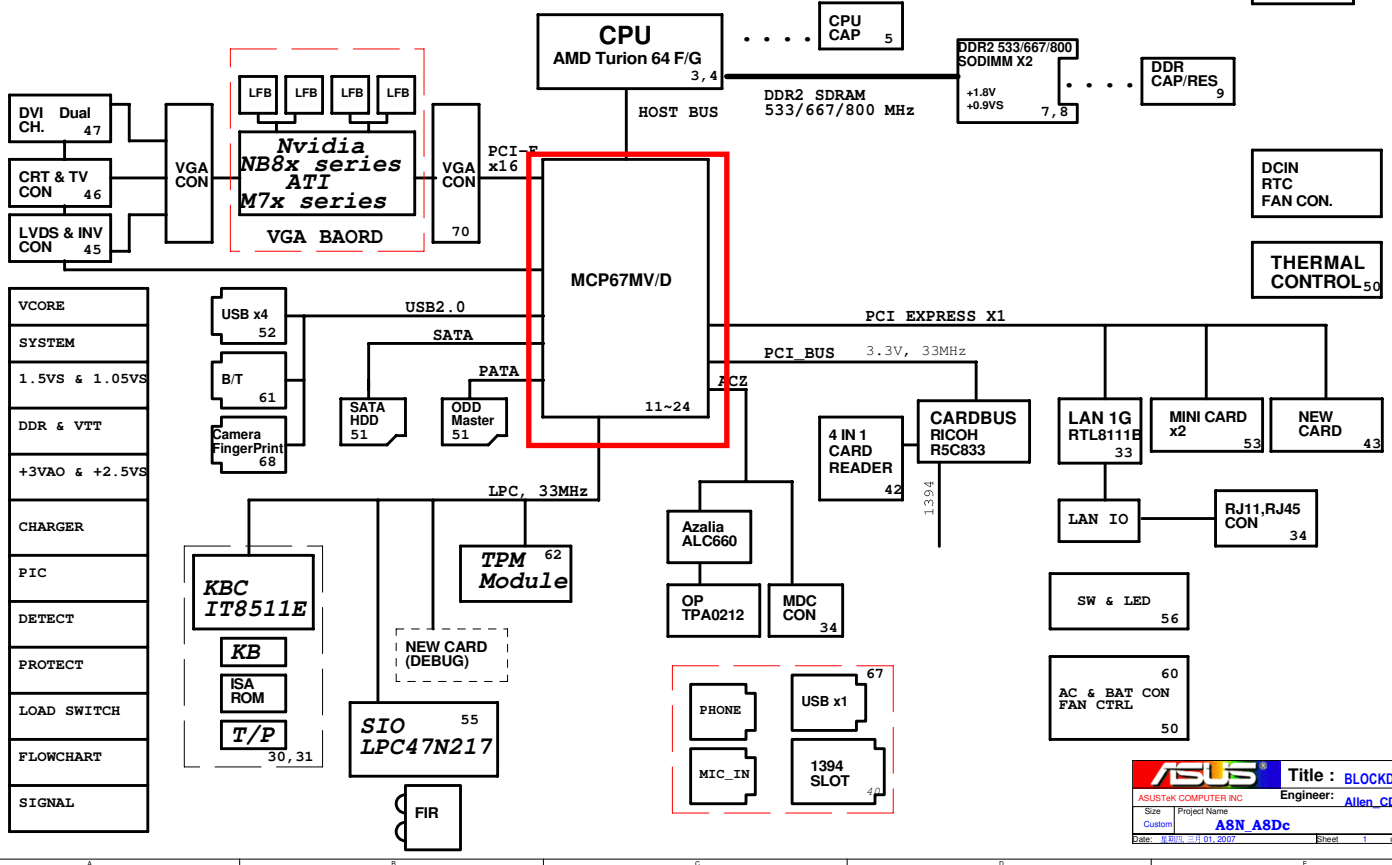
Sub block Diagram /
BOM option

64

BATTERY
TYPE
3S2P

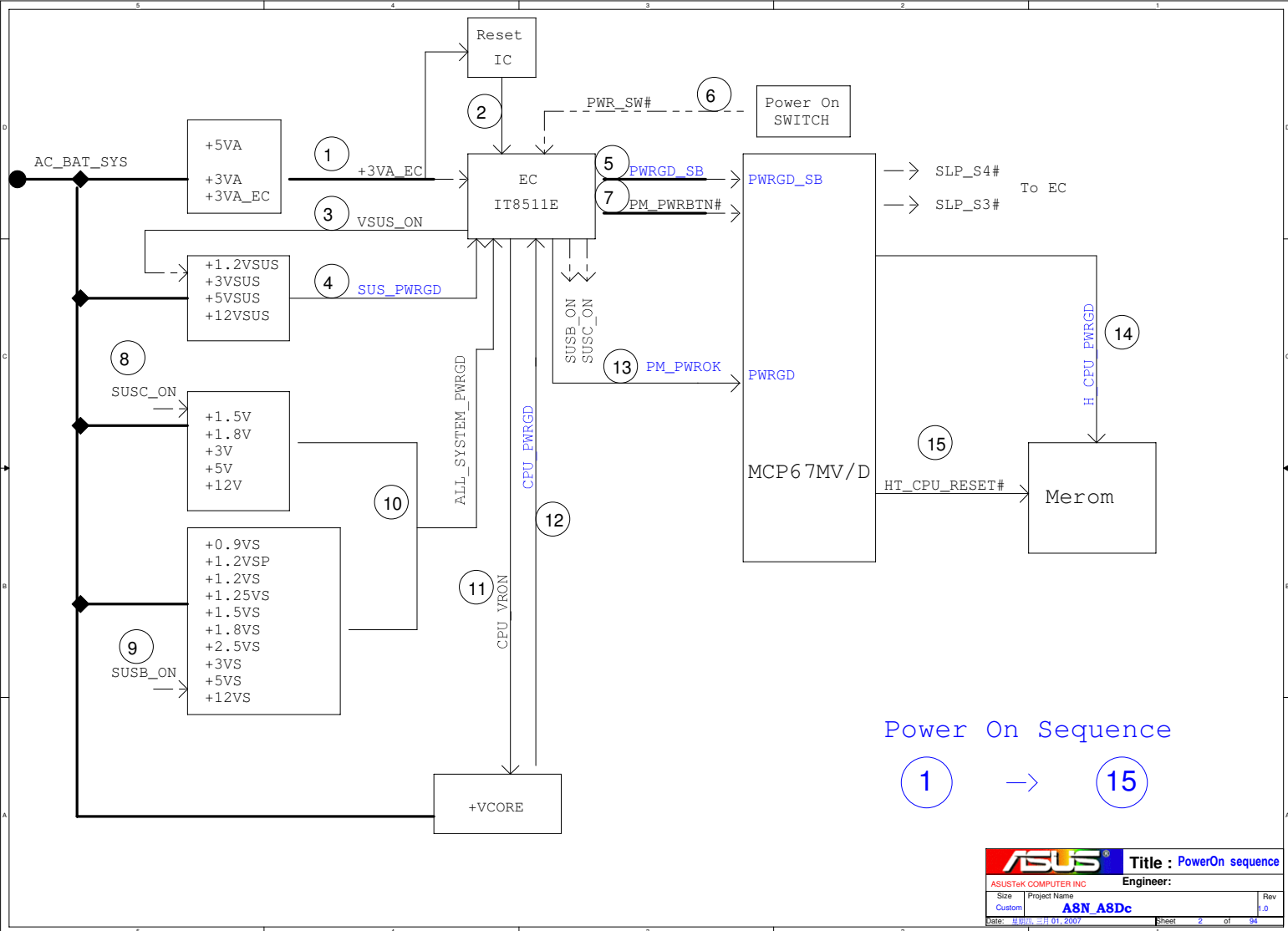


POWER
SEQUENCE
2

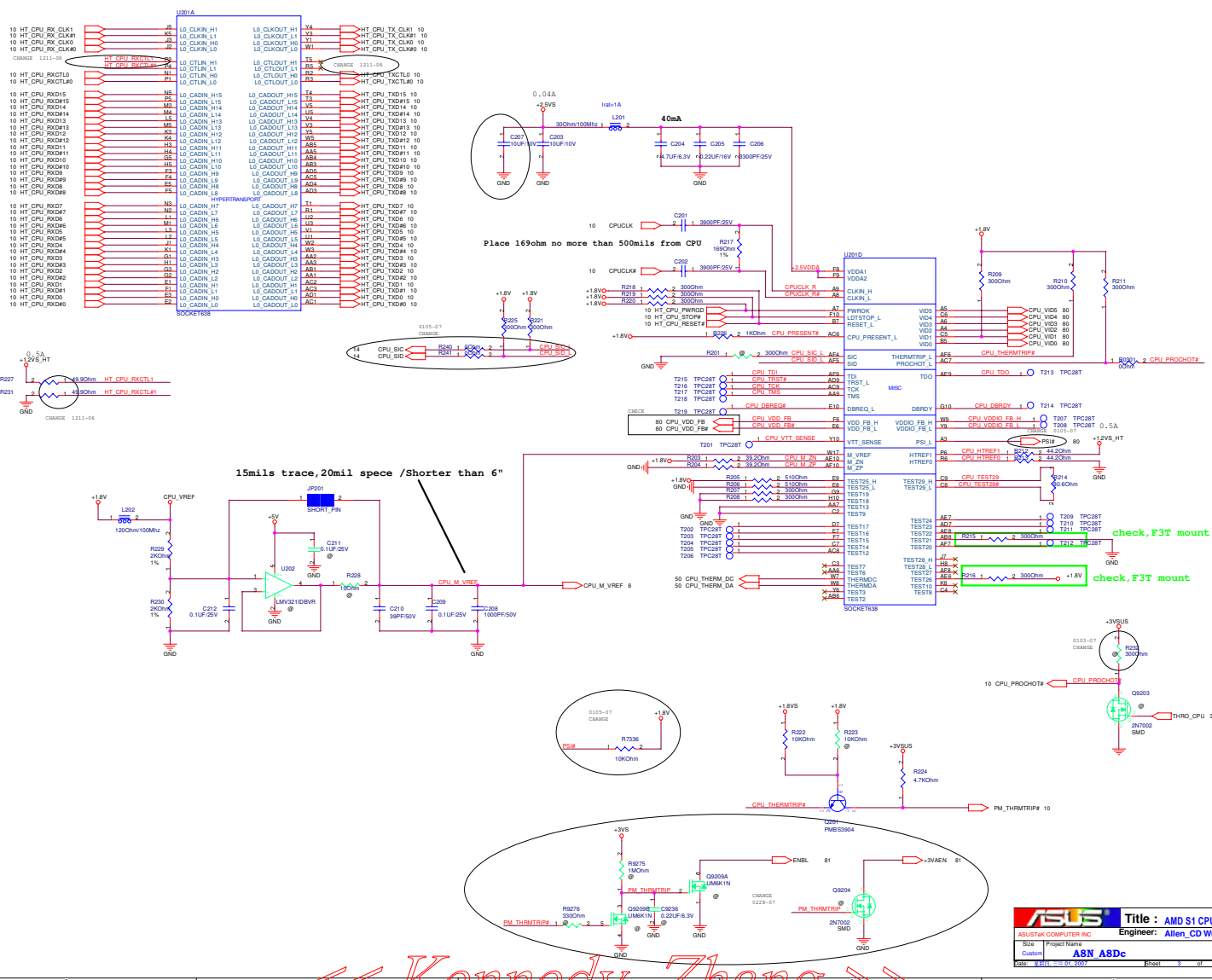


ASUS		Title : BLOCKDIAGRAM	
ASUSTeK COMPUTER INC.		Engineer: Allen_CD Wu	
Size	Project Name		Rev
Custom	A8N_A8Dc		1.0
Date: 10/10/2007		Sheet 1 of 94	

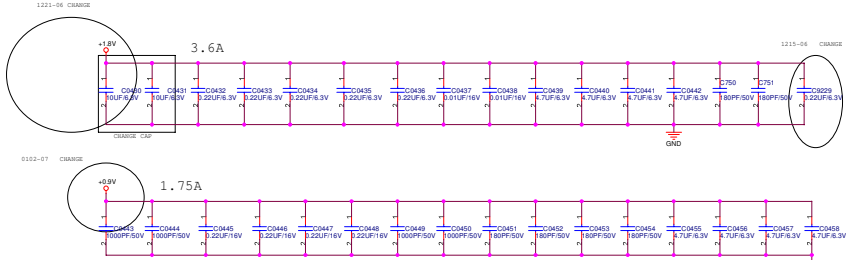
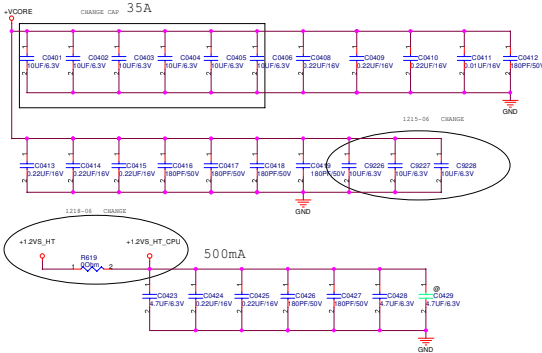
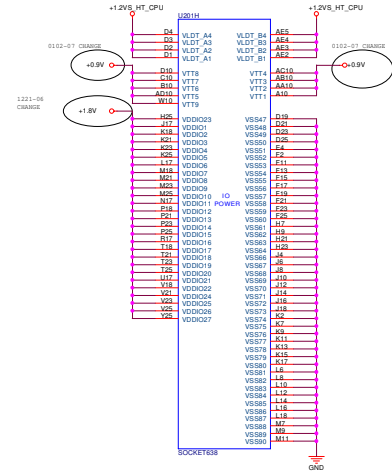
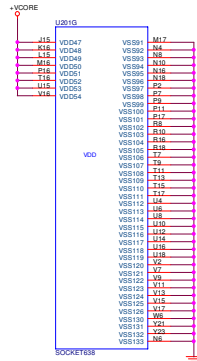
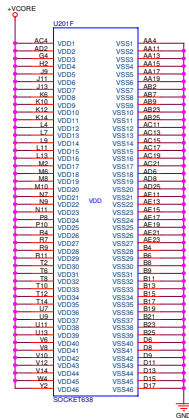
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>




Kennedy_Zhang

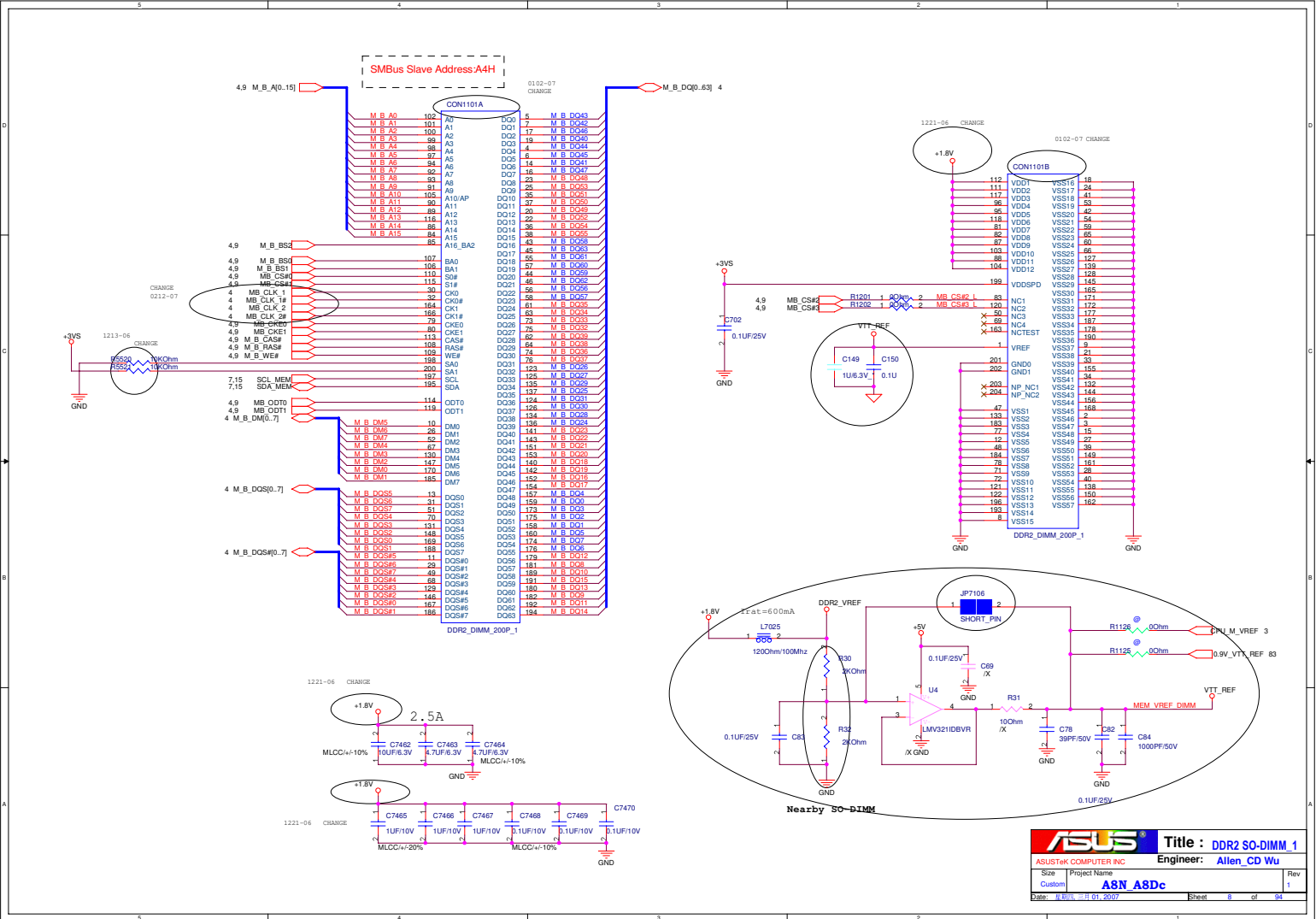


<< Kennedy_Zhang >>

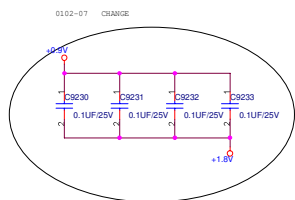
	5	4	3	2	1
D					
C					
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A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 6 of 94	

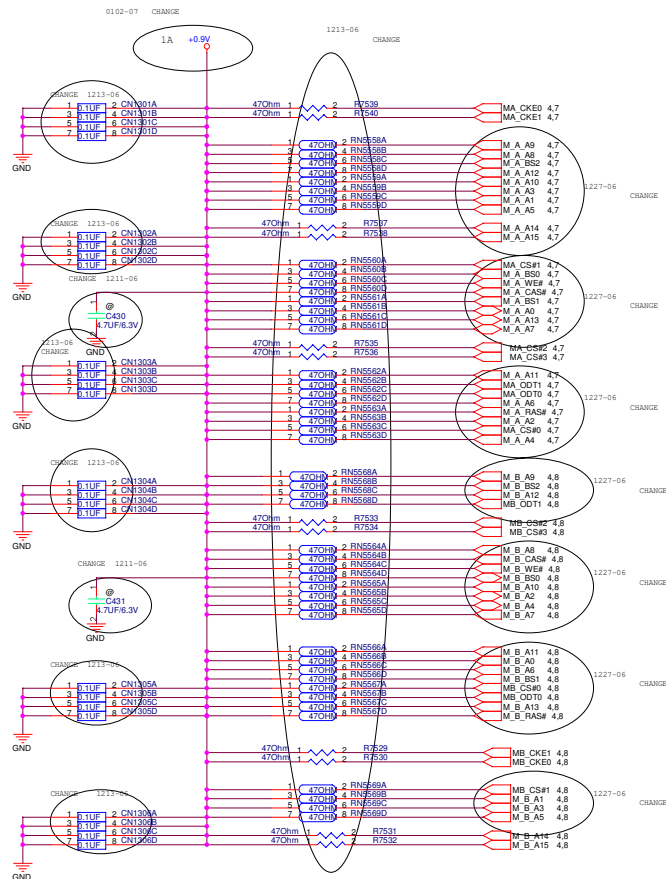
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



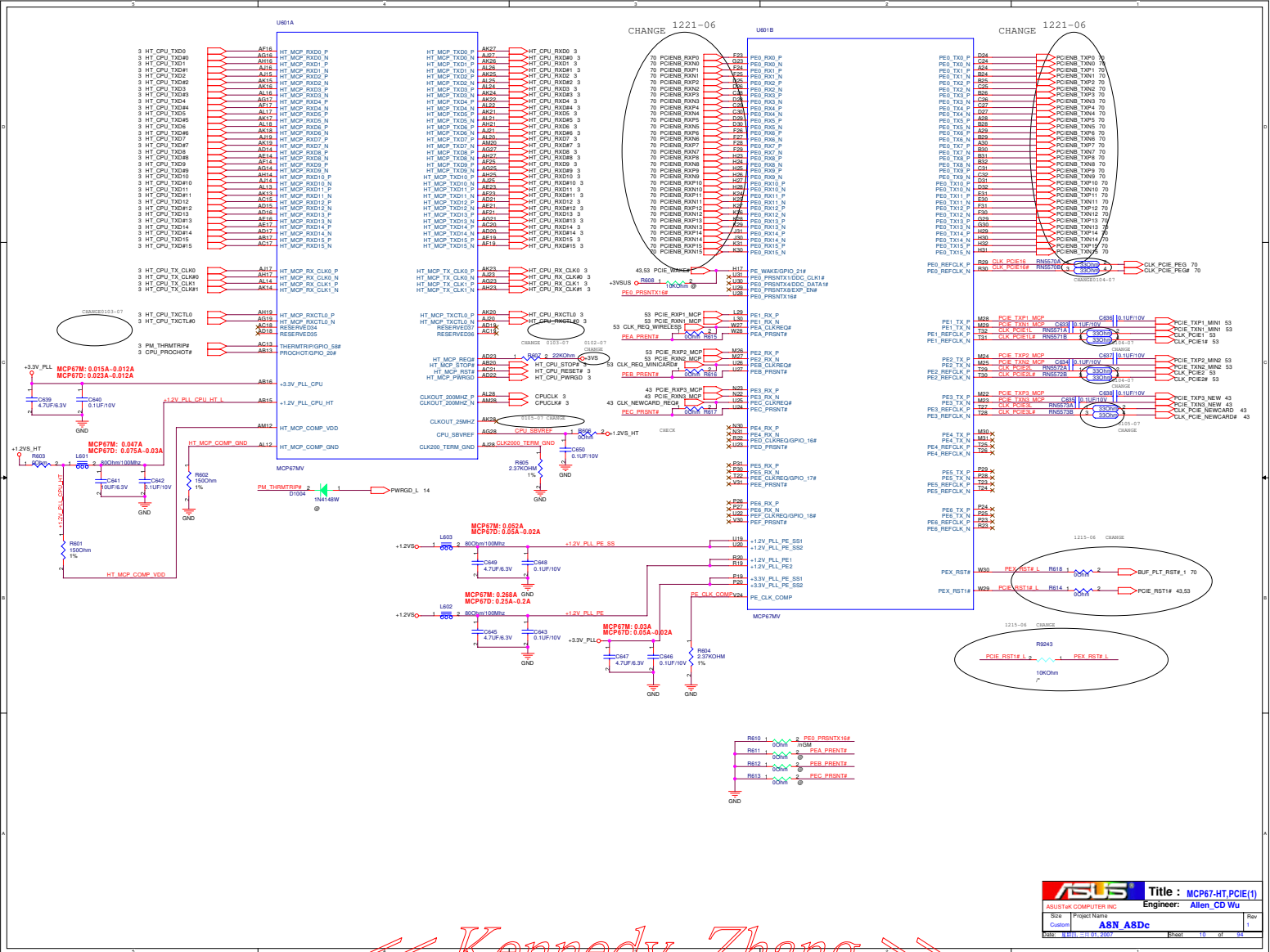
For Address/Command close to the area of plane switched



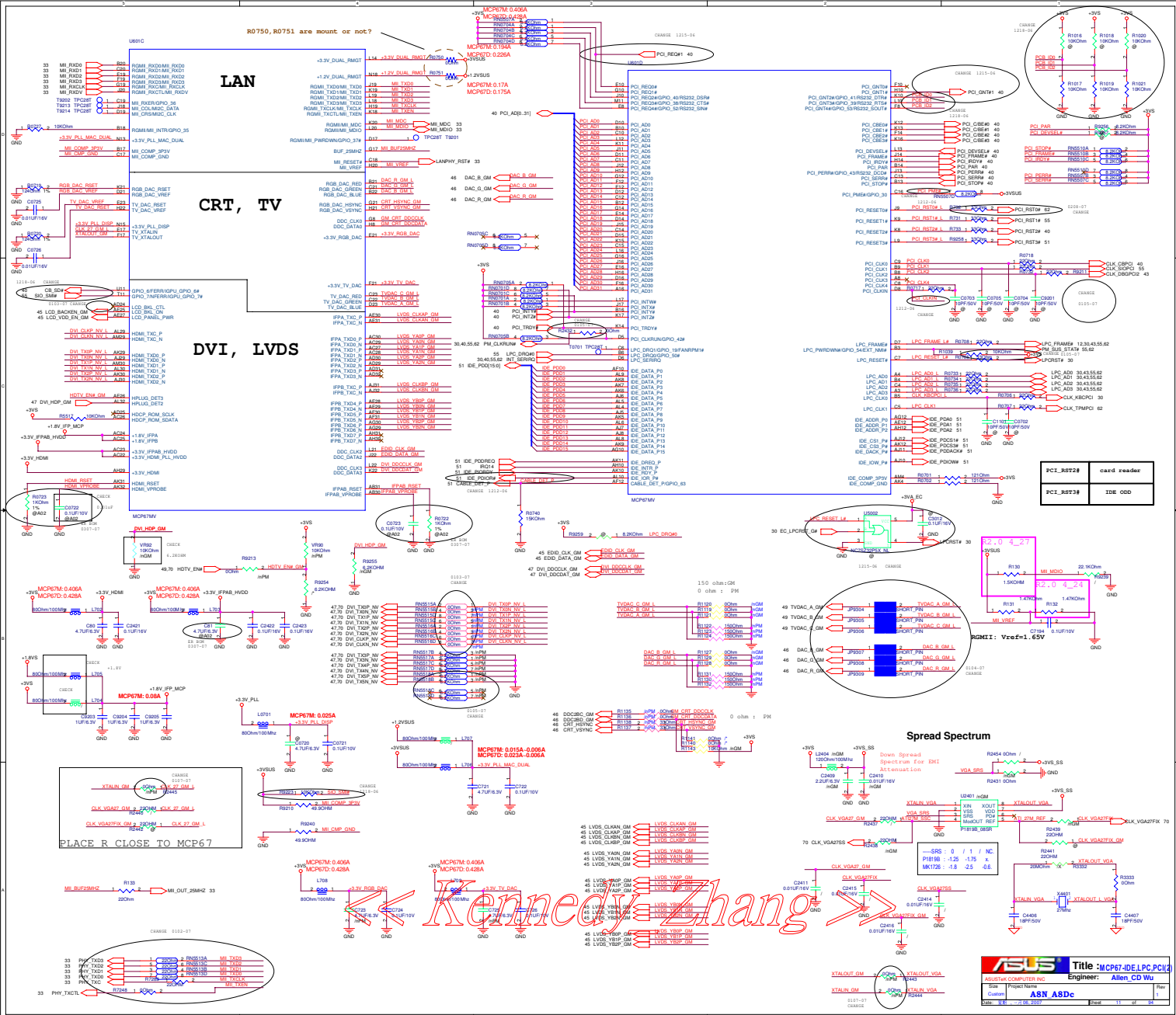
Layout note: Place array cap close to each pullup resistor terminated to +0.9V

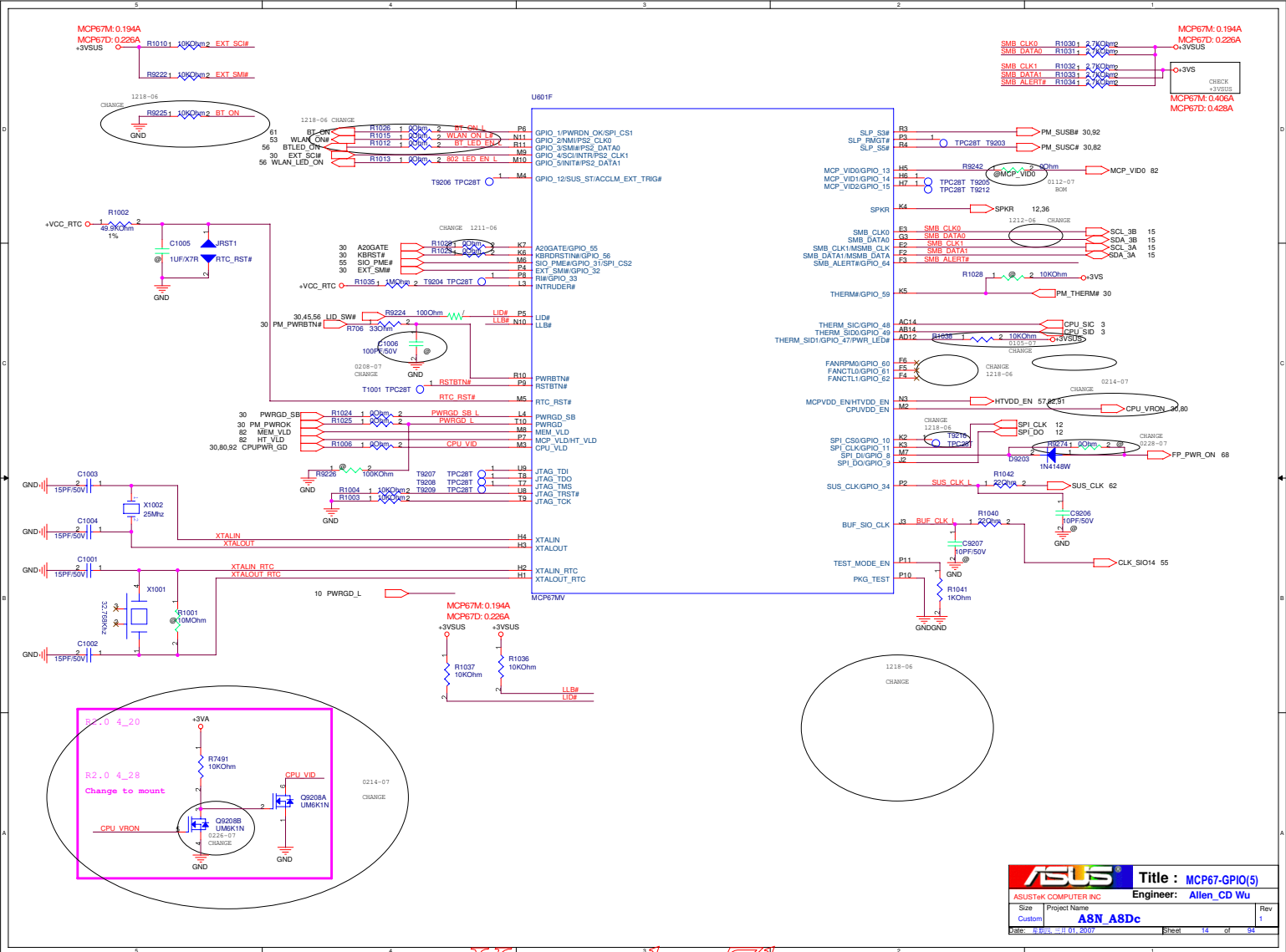
ASUS			Title :DDR2 TERMINATION	
ASUSTek COMPUTER INC			Engineer: Allen_CD Wu	
Size	Project Name			Rev
Custom	A8N_A8Dc			1
Date: 10/10/07			Sheet 6 of 94	

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>





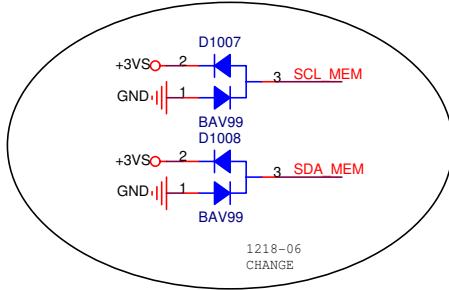
<< Kennedy_Zhang >>

Check

Connect SMLINK and SMBUS
for SMBus 2.0 compliance.

ICH8-M

ICH8-M



1218-06
CHANGE

		Title : LEVEL SHIFTER	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size A	Project Name A8N_A8Dc		Rev 1.0
Date: 星期四, 三月 01, 2007		Sheet 15	of 94


<< Kennedy_Zhang >>

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 16 of 94	

<< Kennedy_Zhang >>

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D					
C					
B					
A					

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 17 of 94	


<< Kennedy_Zhang >>

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D					
C					
B					
A					


		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8N_A8Dc		0
Date: 星期四, 三月 01, 2007		Sheet	18 of 94

<< Kennedy_Zhang >>


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D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8N_A8Dc		0
Date: 星期四, 三月 01, 2007		Sheet	19 of 94


<< Kennedy_Zhang >>

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ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8N_A8Dc		0
Date: 10月01, 2007		Sheet 20 of 94	


<< Kennedy_Zhang >>

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8N_A8De	0	
Date: 11/11/2007		Sheet 21 of 94	

<< Kennedy_Zhang >>


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ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
Custom	A8N_A8Dc	0	
Date: 8/20/04 - 11/01/2007		Sheet 22 of 94	

<< Kennedy_Zhang >>

		Title : BLANK	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8N_A8Dc		0
Date: 星期日 01, 2007		Sheet 23 of 94	

<< Kennedy_Zhang >>

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D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 24 of 94	


<< Kennedy_Zhang >>

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D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet	25 of 94


<< Kennedy_Zhang >>

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 26 of 94	

<< Kennedy_Zhang >>

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D					
C					
B					
A					
	5	4	3	2	1


		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8N_A8Dc		0
Date: 星期四, 三月 01, 2007		Sheet	27 of 94

<< Kennedy_Zhang >>

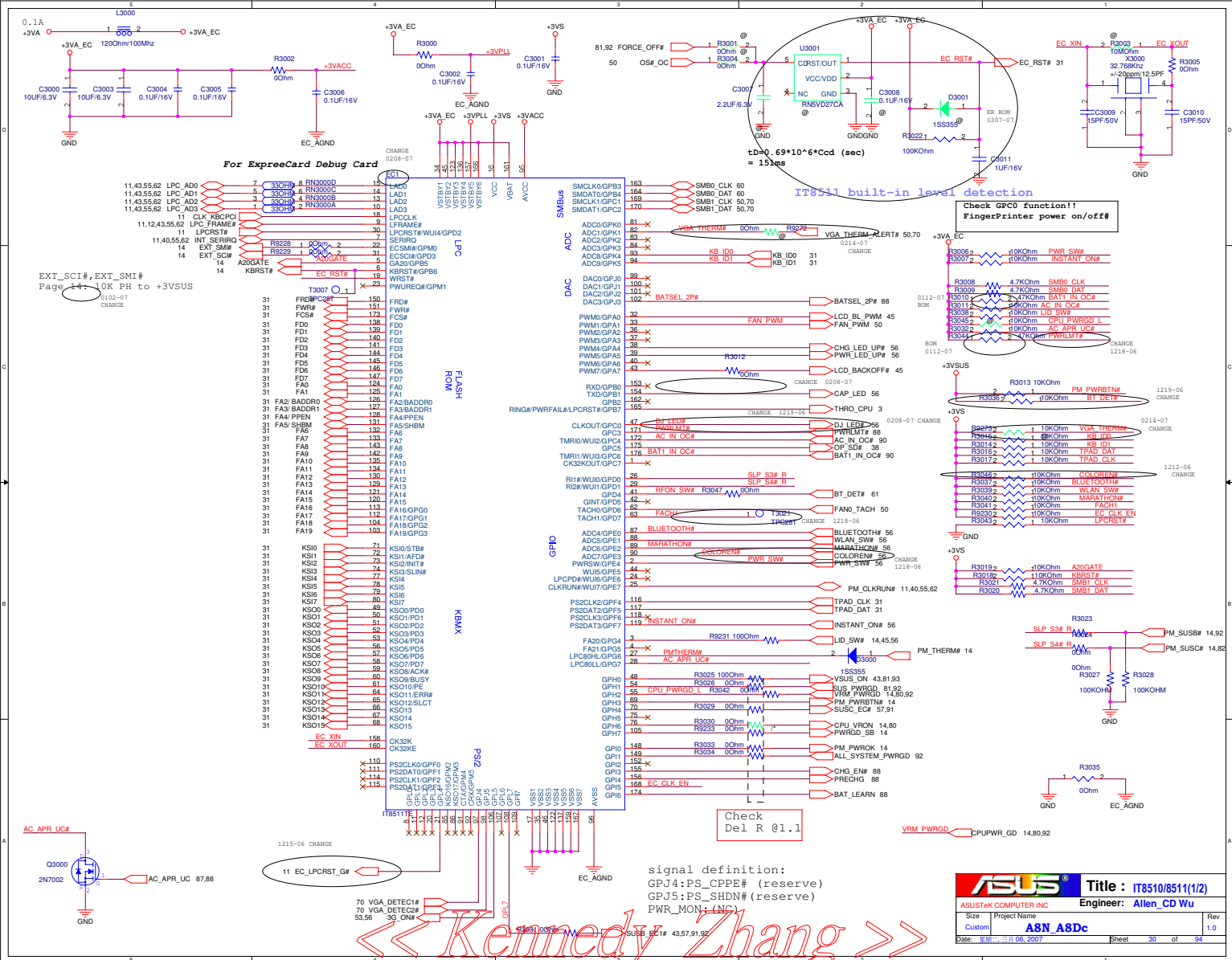
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D					
C					
B					
A					

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ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 28 of 94	

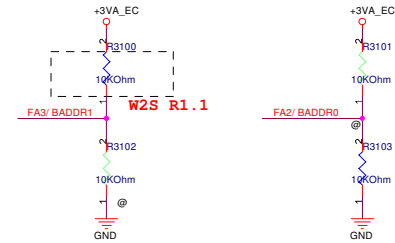
<< Kennedy_Zhang >>

		Title : BLANK	
ASUSTek COMPUTER INC. Engineer:			
Size	Project Name		Rev
Custom	A8N_A8Dc		1.0
Date	8/29/2007	Sheet	29 of 84

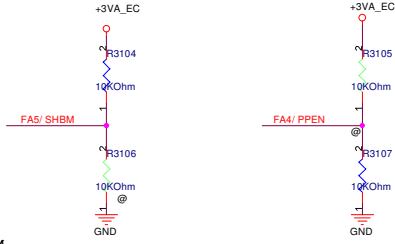
<< Kennedy_Zhang >>



10:Determined by EC



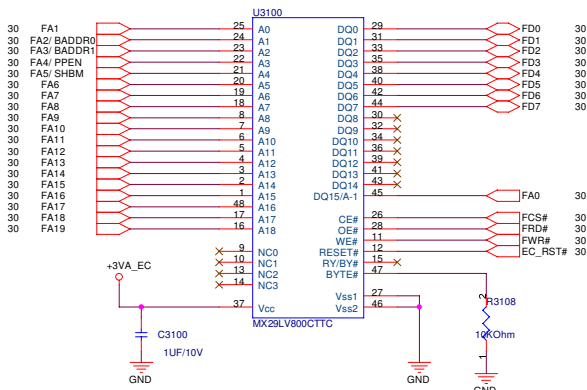
BADDR[1:0]
No pull up:
The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:
The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.



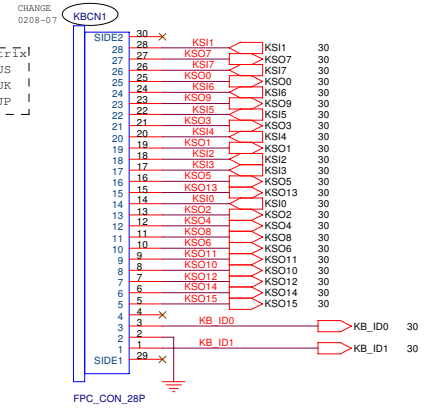
SHBM
No pull up:
disable shared memory with host BIOS
Ext 10K up:
enable shared memory with host BIOS

PPEN
No pull up:
Normal
Ext 10K up:
KBS interface pins are switched to parallel port interface for in-system programming.

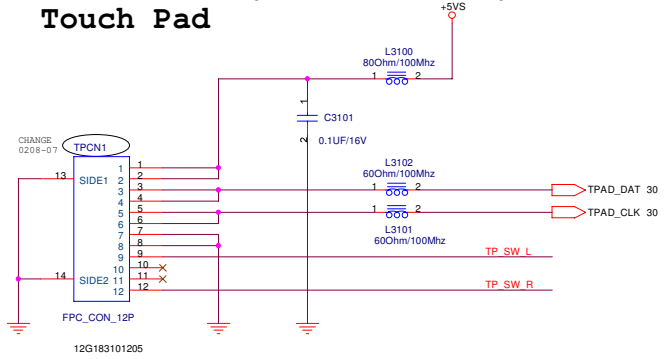
8M TSOP



KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP




Touch Pad



ASUS		Title : IT8510/8511(2/2)	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name		Rev
Custom	A8N A8Dc		1.0
Date: 01/01/2007	Sheet 31 of 94		

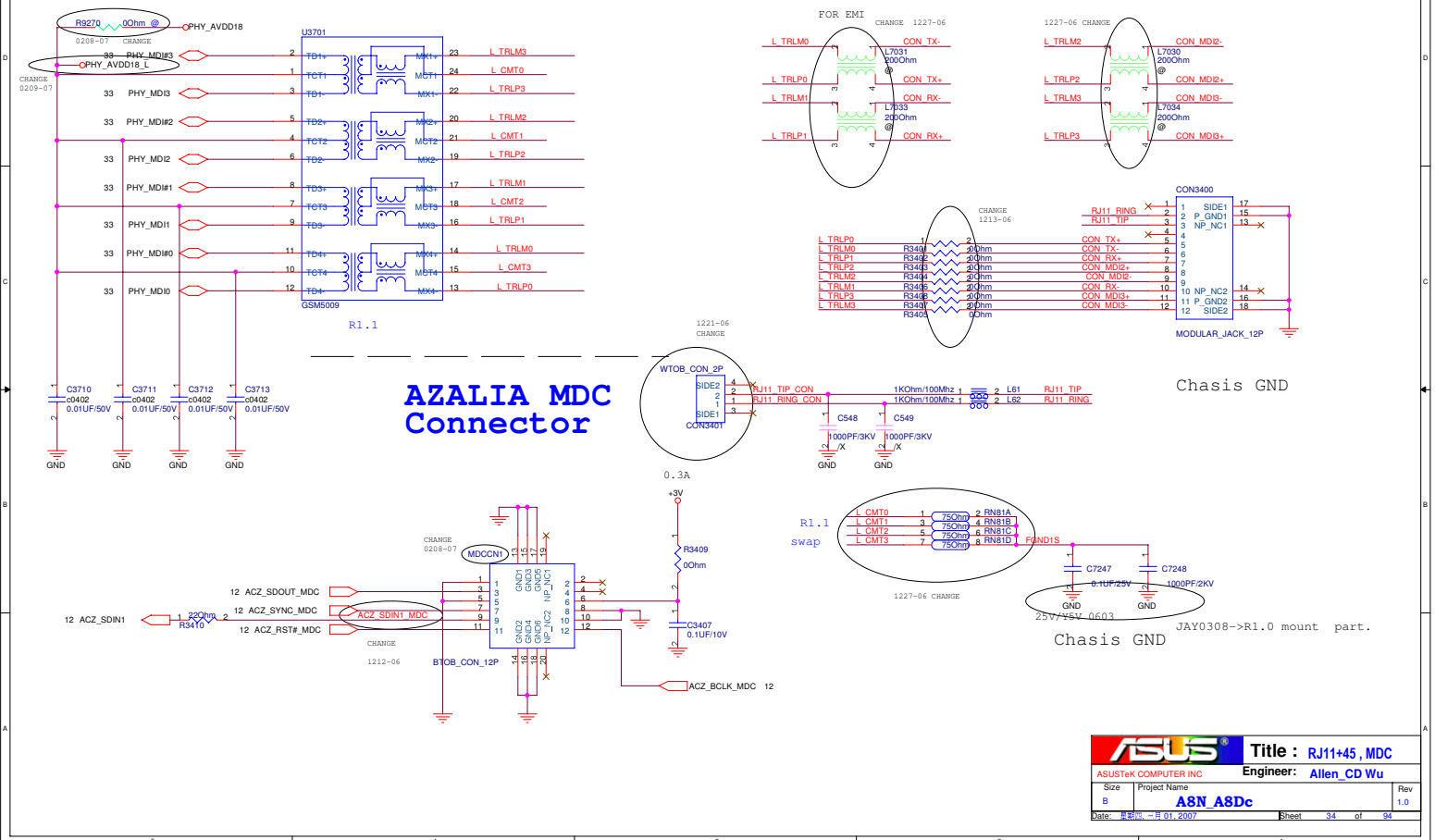
« Kennedy_Zhang »

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 32 of 94	


<< Kennedy_Zhang >>

LAN PORT



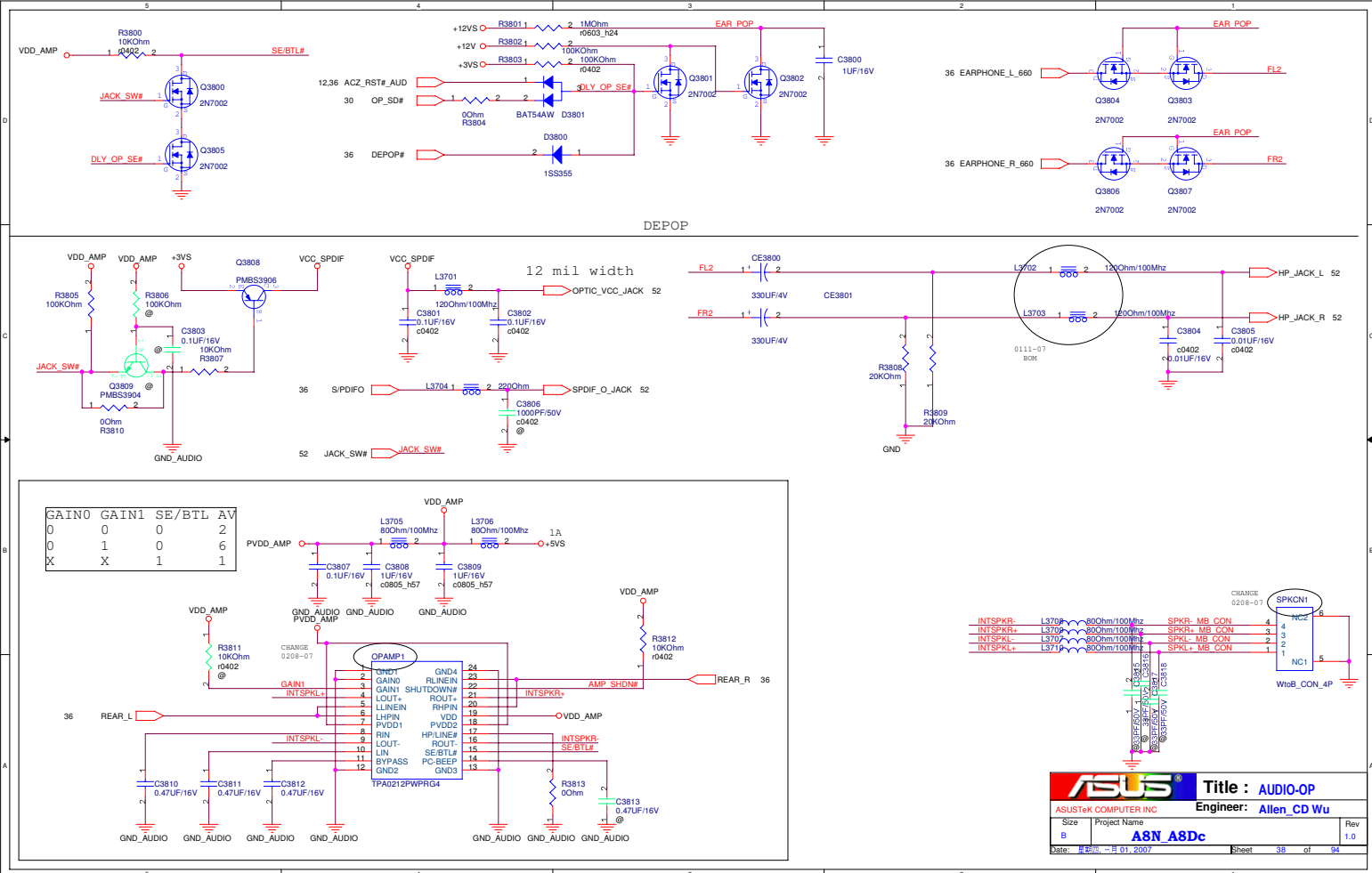
<< Kennedy_Zhang >>

	5	4	3	2	1
D					
C					
B					
A					

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8N_A8Dc		0
Date: 星期四, 三月 01, 2007		Sheet	35 of 94

<< Kennedy_Zhang >>



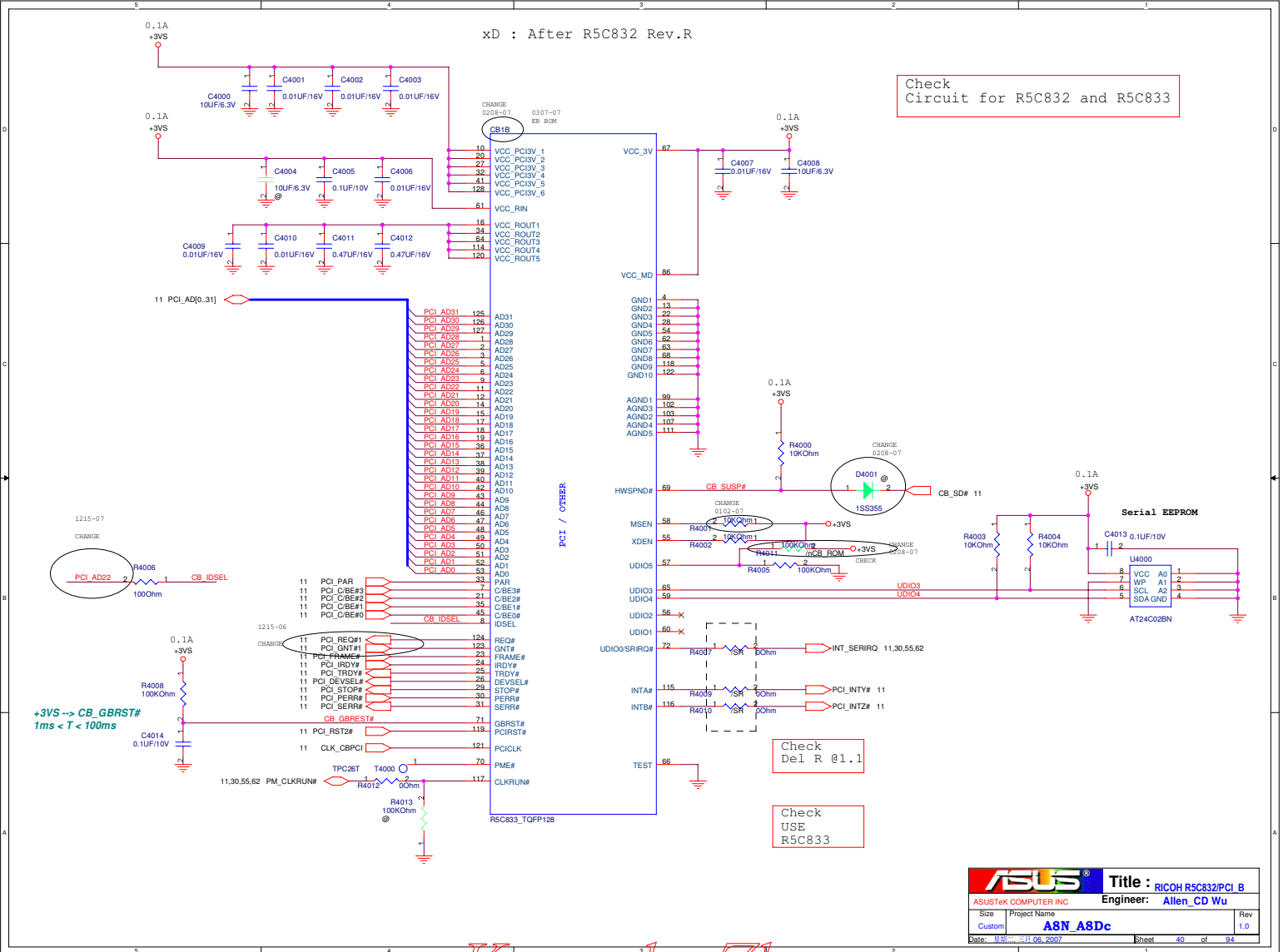


<< Kennedy_Zhang >>

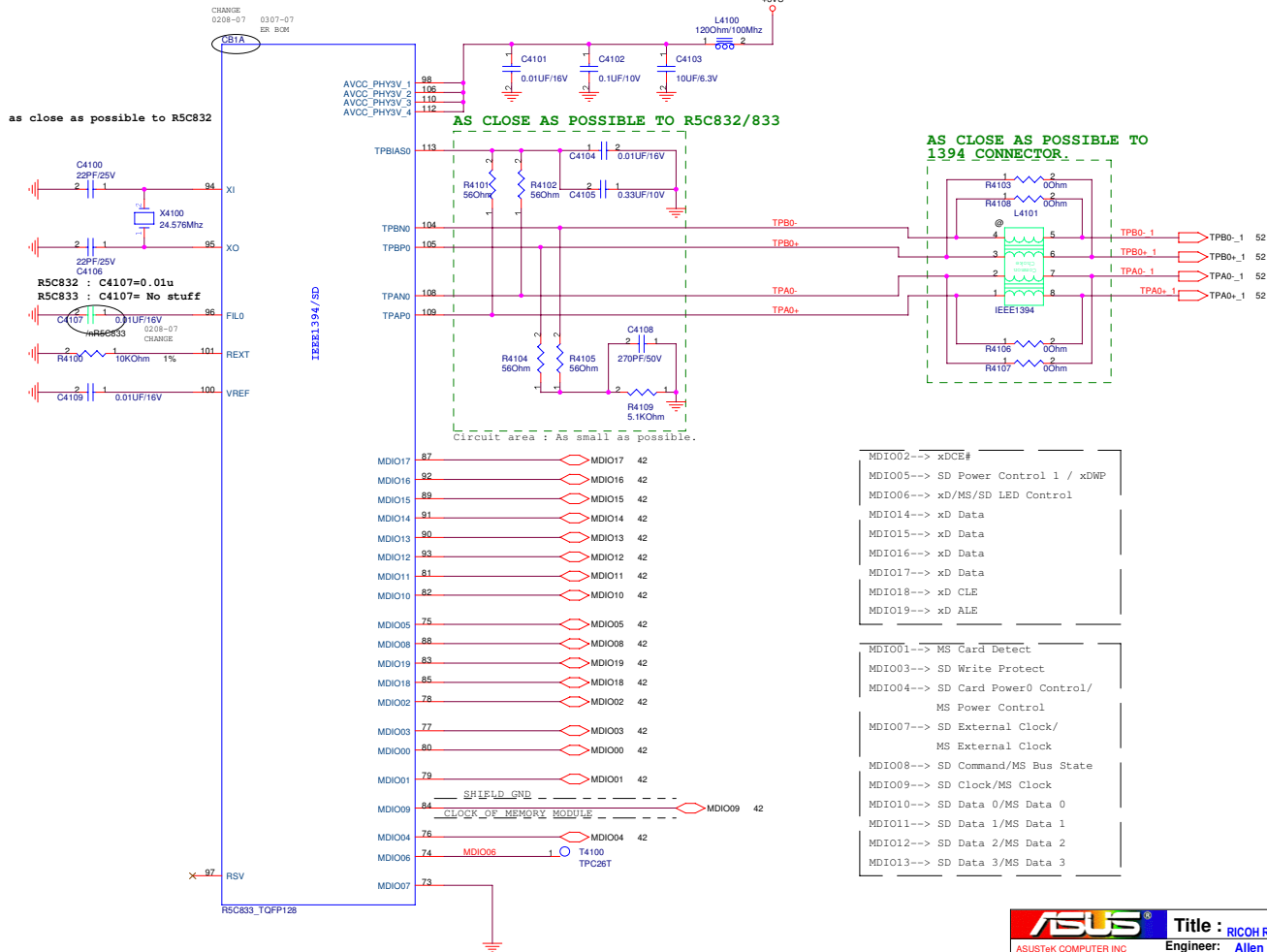
	5	4	3	2	1
D					
C					
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A					

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 39 of 94	

<< Kennedy_Zhang >>

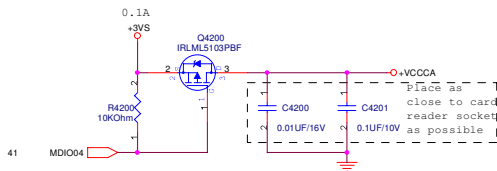


<< Kennedy_Zhang >>

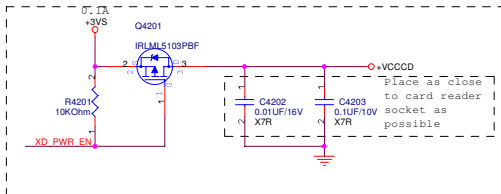


<< Kennedy_Zhang >>

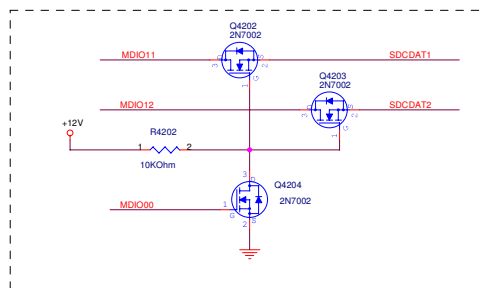
ASUS		Title : RICOH R5C832/PCI A	
ASUSTek COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name	Rev	
Custom	A8N A8Dc	1.0	
Date: 星期日 05/06/2007	Sheet 41 of 94		



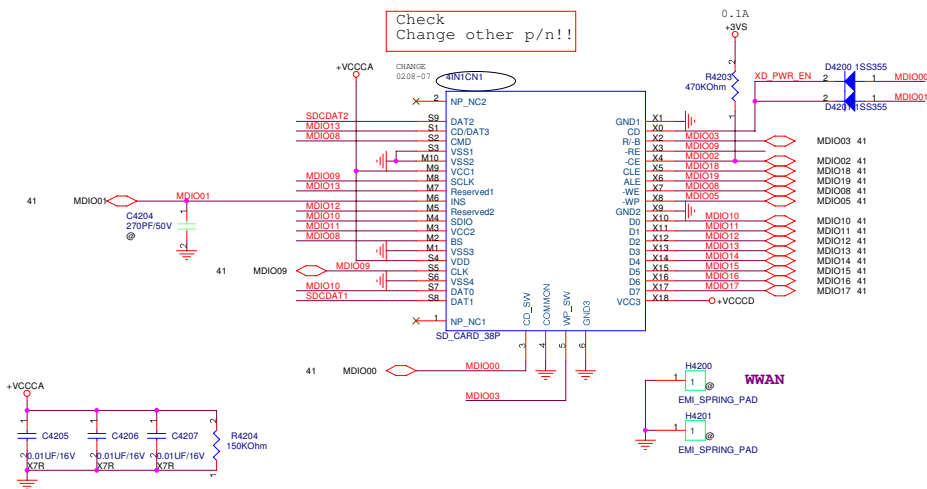
To correct the problem when MS Duo adaptor is in use.



Solve MS Duo Adaptor short issue.



Check
Change other p/n!!



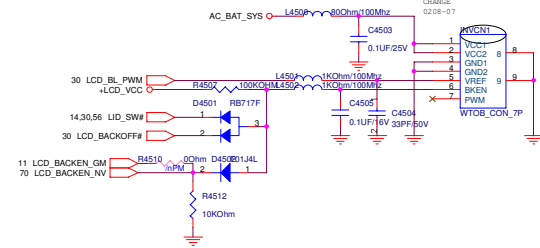
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

ASUS		Title : CardReader	
ASUSTek COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name	Rev	
Custom	A8N A8Dc	1.0	
Date: 2007.01.01		Sheet 42 of 94	

<< Kennedy_Zhang >>

5		4		3		2		1	
D									
C									
B									
A									



		Title : <u>LVDS & Inverter</u>	
ASUSTeK COMPUTER INC		Engineer: <u>Allen_CD Wu</u>	
Size Custom	Project Name A8N A8Dc		Rev 1.0
Date: <u>8 APR 2007</u>		Sheet <u>45</u> of <u>94</u>	

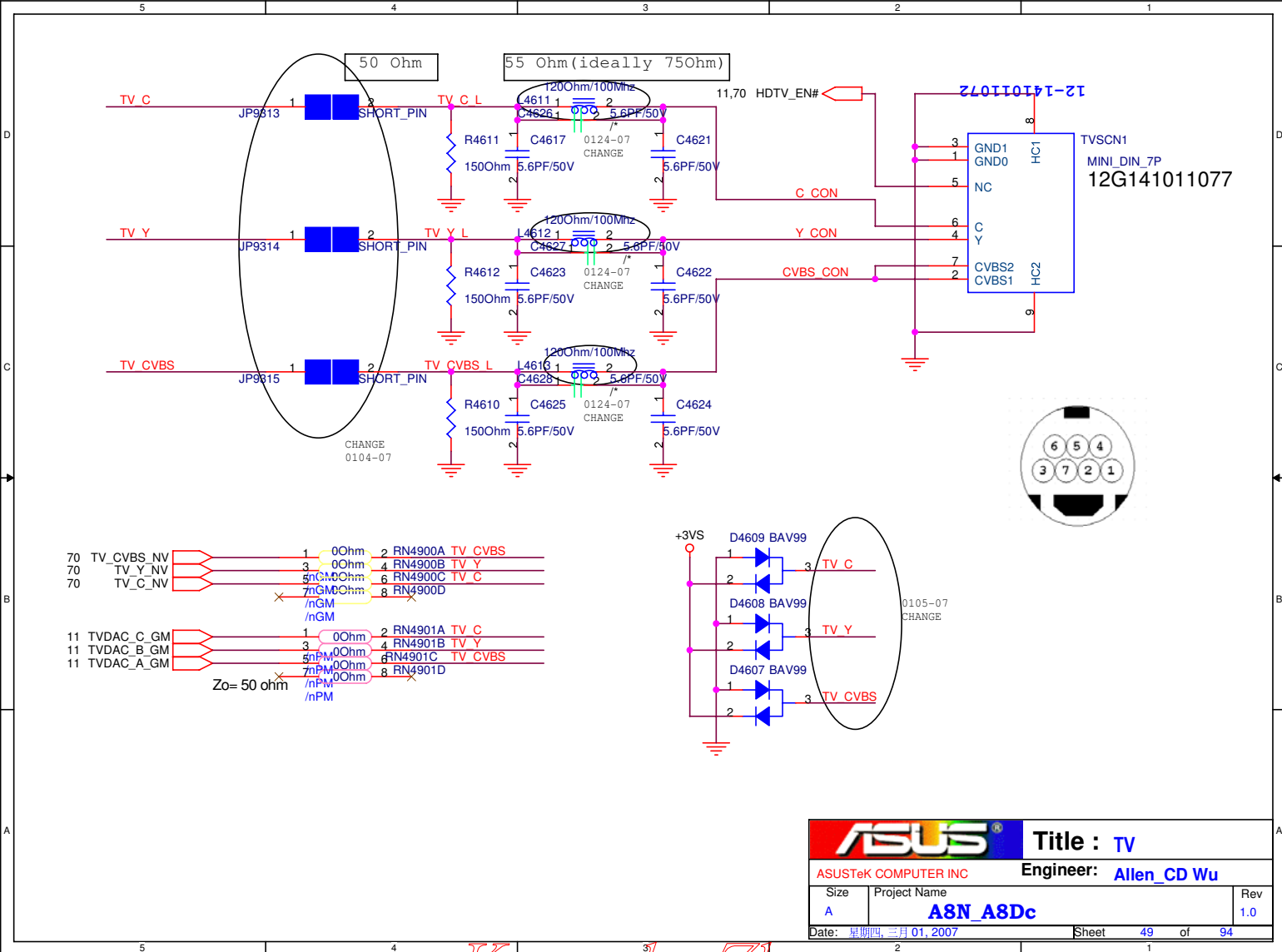
<< Kennedy_Zhang >>



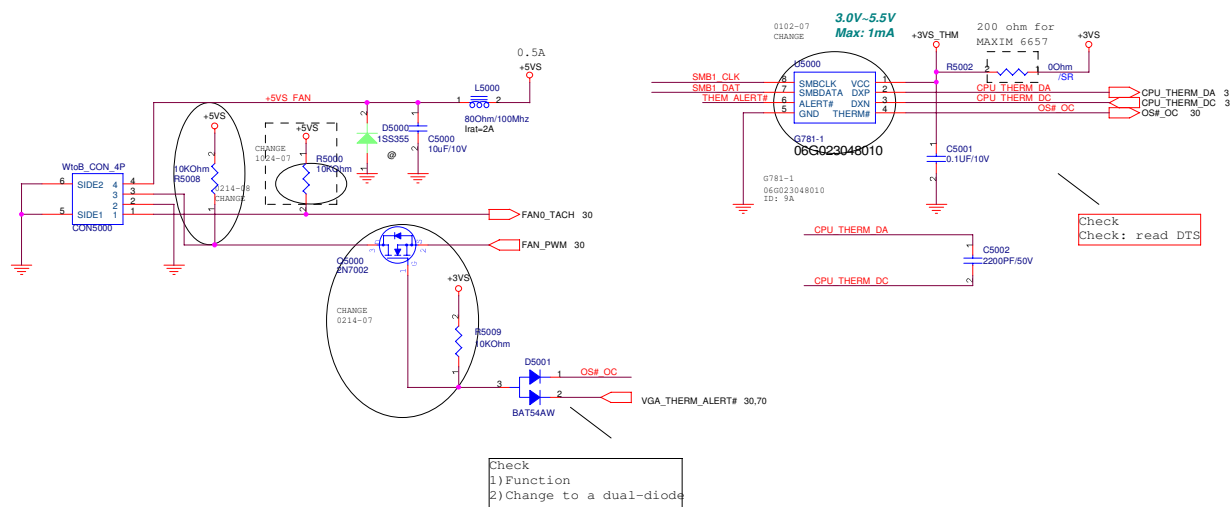
	5	4	3	2	1
D					
C					
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		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 48 of 94	

<< Kennedy_Zhang >>

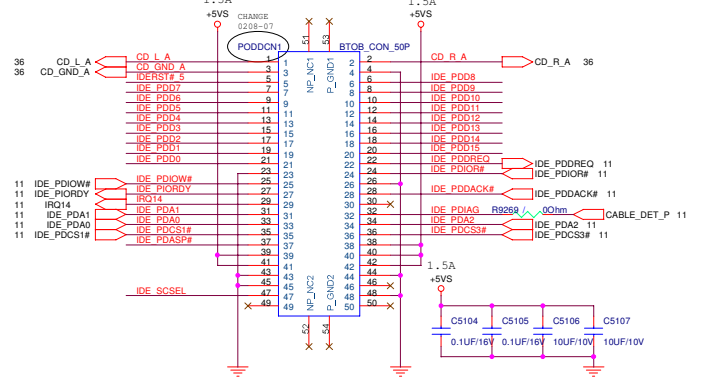
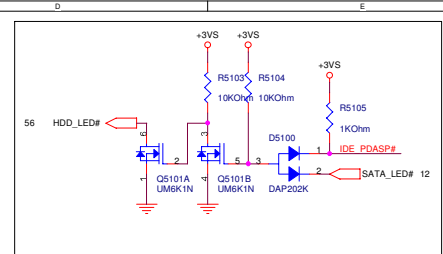


<< Kennedy_Zhang >>

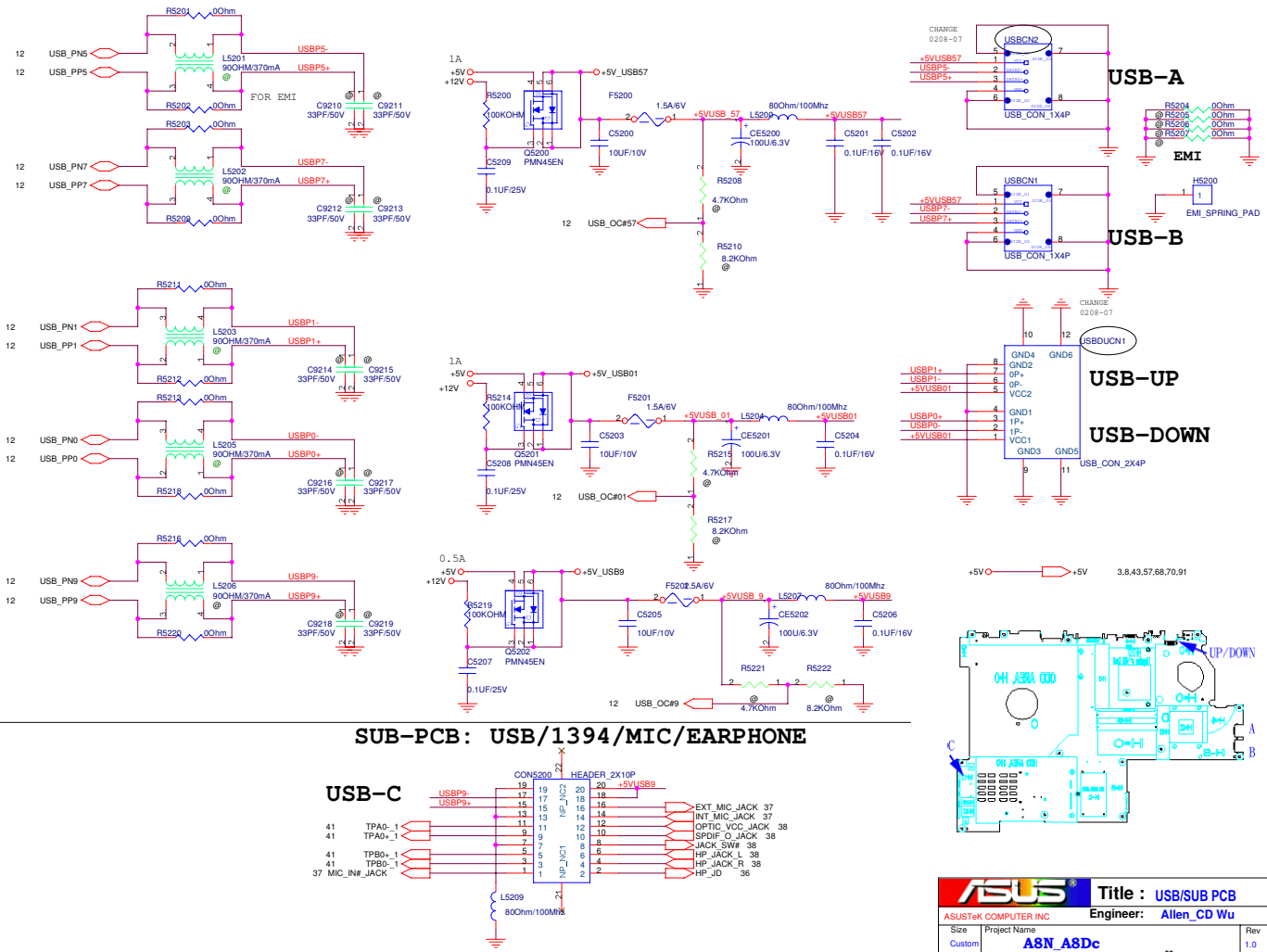


		Title : FAN & THERMAL	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size B	Project Name A8N_A8Dc	Re	
Date: 星期四, 三月 01, 2007		Sheet 50 of 94	


<< Kennedy_Zhang >>



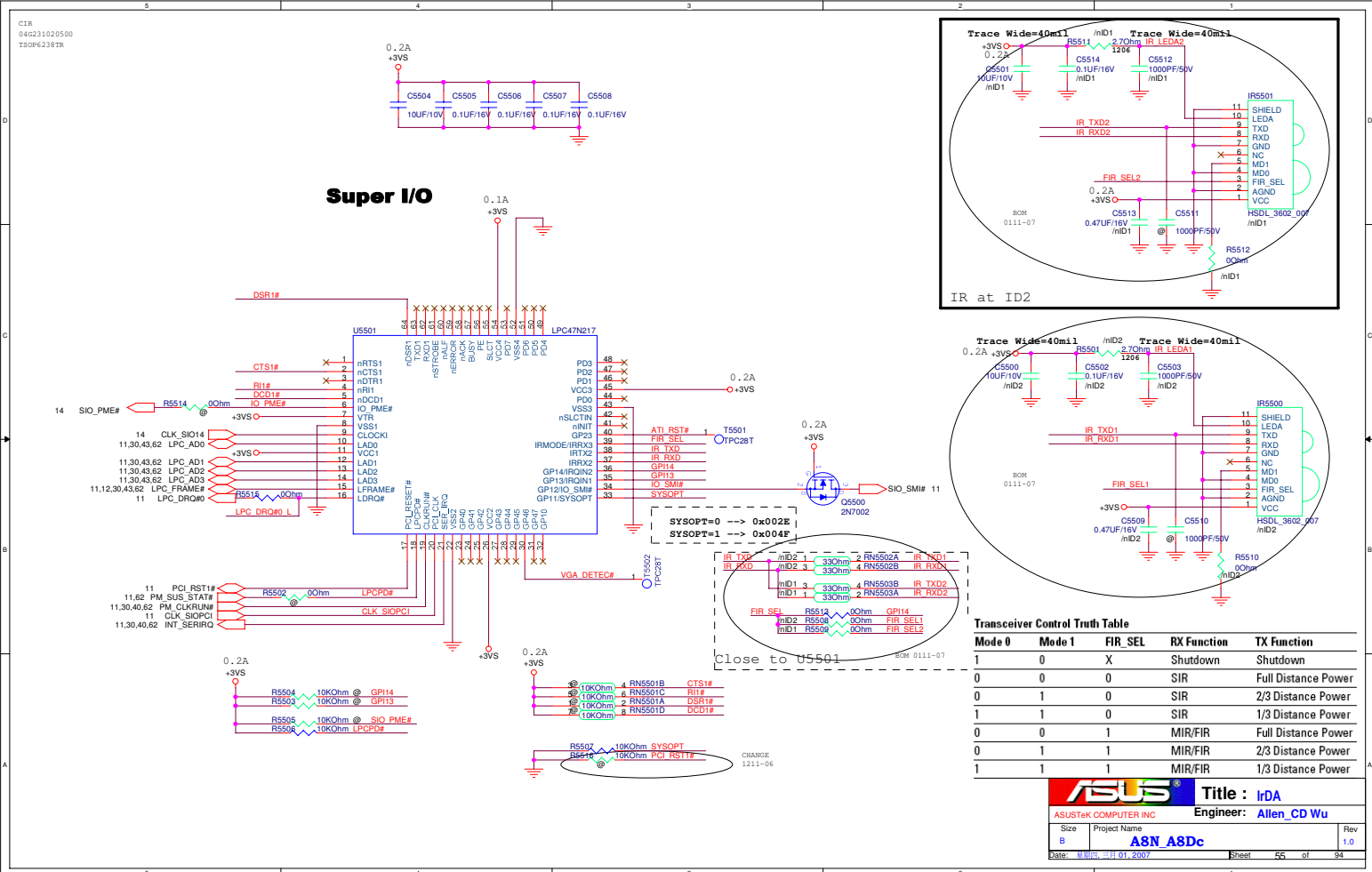
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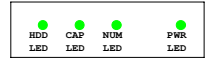
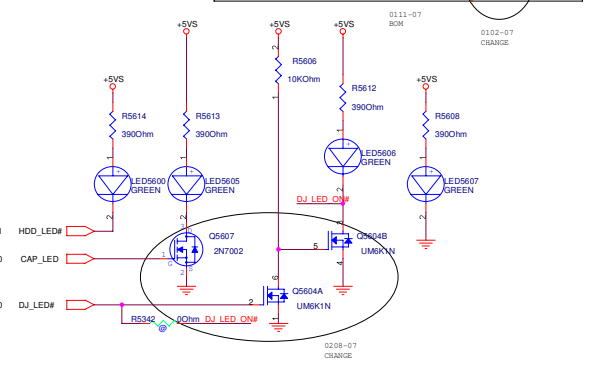
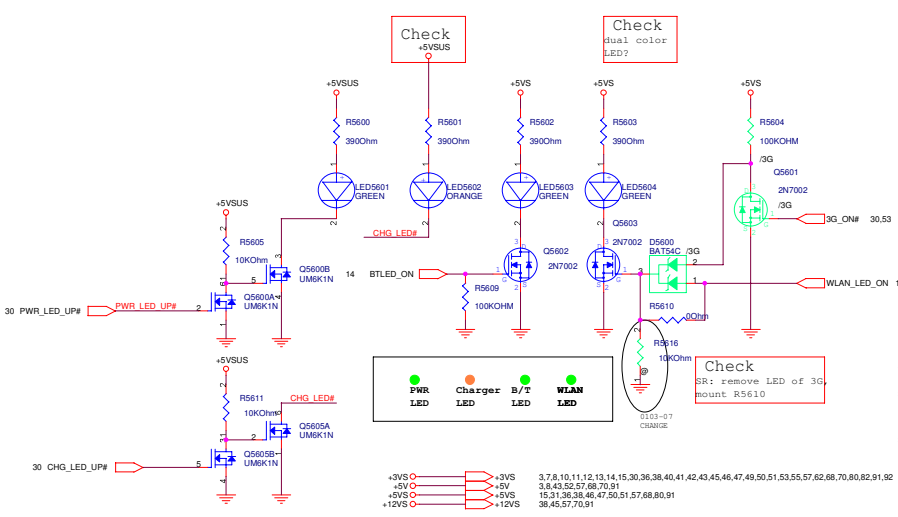
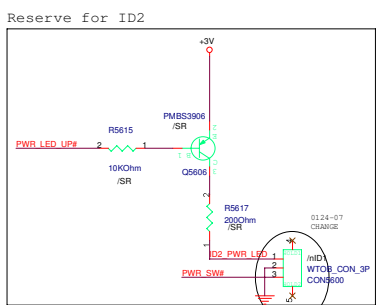
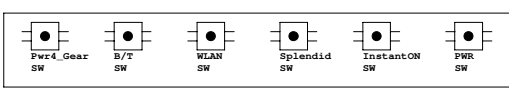
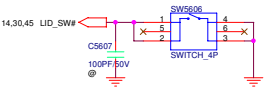
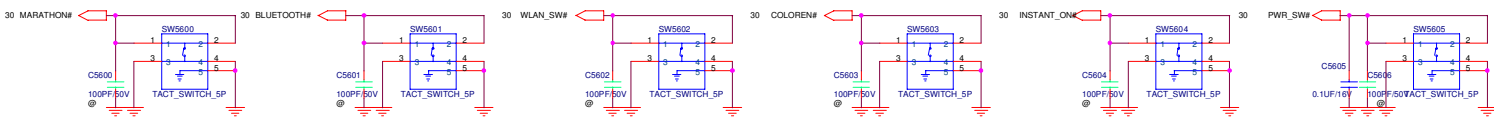


<< Kennedy_Zhang >>

		Title : BLANK	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name		Rev
Custom	A8N_A8Dc		0
Date: 10/25/2007		Sheet	54 of 54

<< Kennedy_Zhang >>

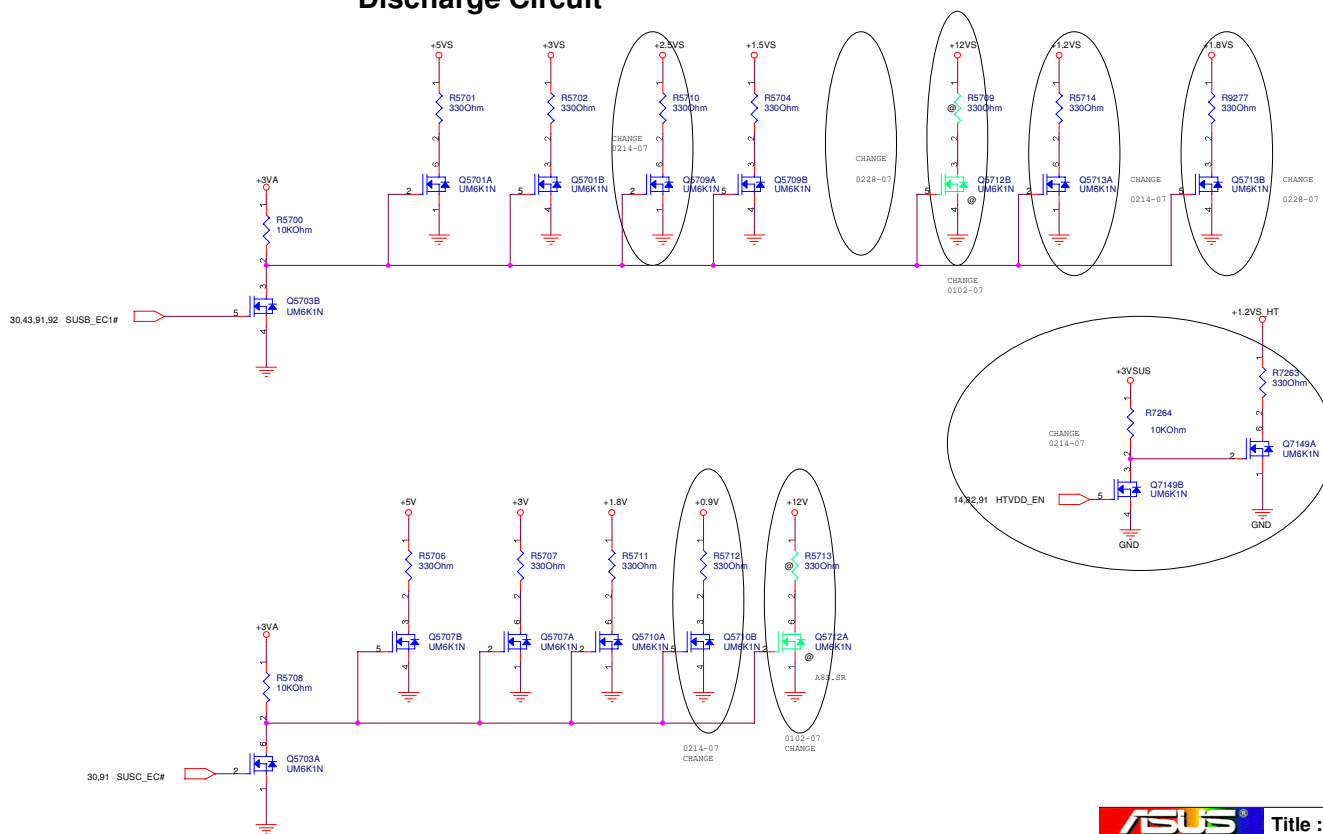




ASUS Title : LED/Instant key
 ASUSTek COMPUTER INC. Engineer: Allen_CD Wu
 Size Project Name
 Custom A8N A8Dc
 Date: 11/01/2007 Sheet 56 of 84

<< Kennedy_Zhang >>

Discharge Circuit




ASUS		Title : Discharge	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name	Rev	
B	A8N A8Dc	1.0	
Date: 11/01/2007	Sheet	67	of 94

<< Kennedy_Zhang >>

	5	4	3	2	1
D					
C					
B					
A					

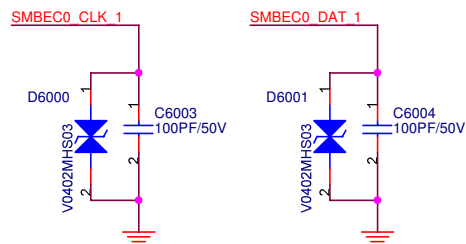
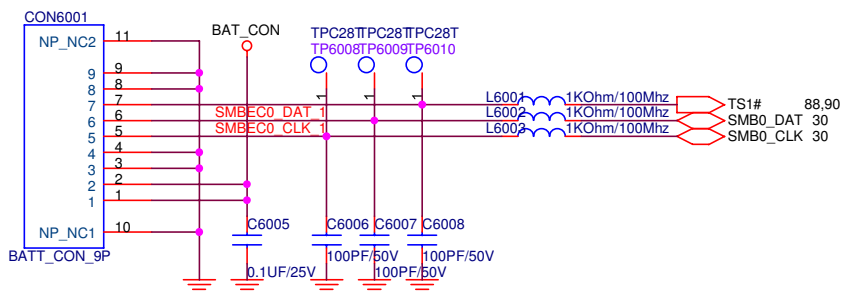
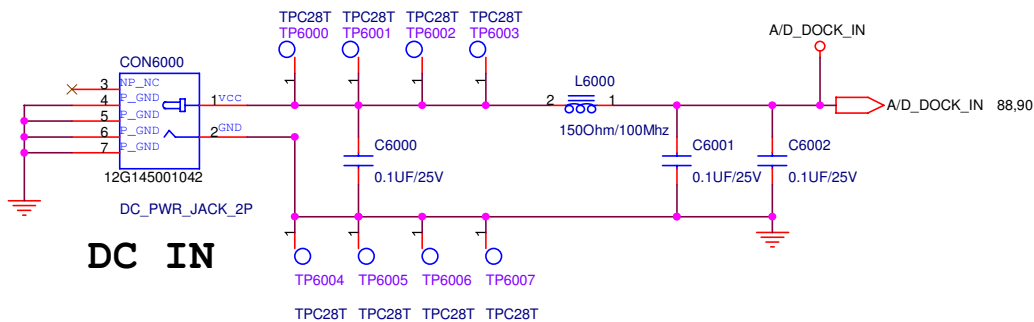
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		Title :	
ASUSTeK COMPUTER INC		Engineer:	
Size	Project Name		Rev
A	A8N_A8Dc		1.0
Date: 星期四, 三月 01, 2007		Sheet	of 94

<< Kennedy_Zhang >>

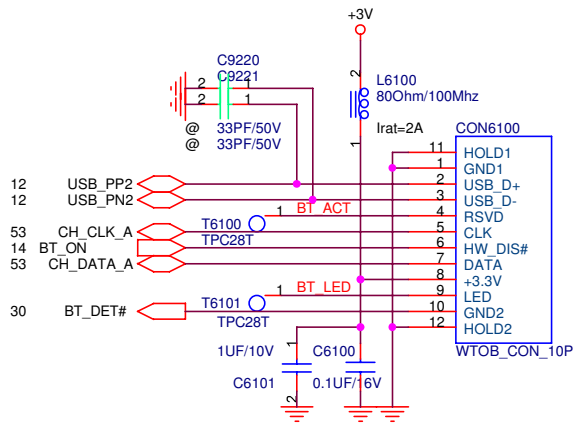
5					4					3					2					1																																																																																																																																																
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Size					Document Number																				Rev																																																																																																																																											
A					ABN_A8Dc																				1.1																																																																																																																																											
Date:										星期四 三月 01, 2007										Sheet					59 of 94																																																																																																																																											
5					4					3					2					1																																																																																																																																																

<< Kennedy_Zhang >>



ASUS		Title : DC IN / BAT	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size A	Project Name A8N_A8Dc		Rev 1.0
Date: 星期四, 三月 01, 2007		Sheet 60 of 94	

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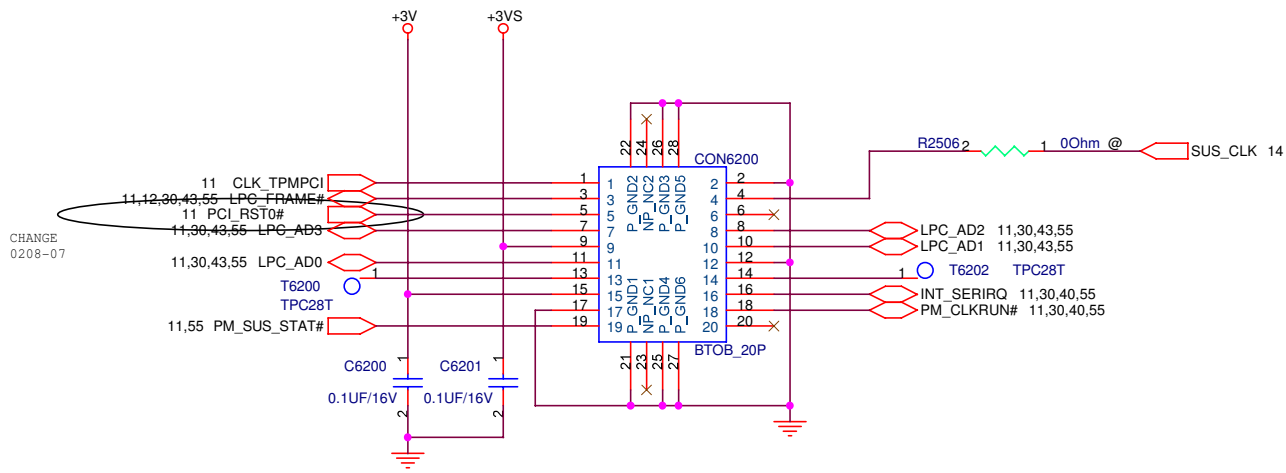


Bluetooth Module CON

ASUS		Title :BT/CAMERA	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name		Rev
A	A8N_A8Dc		1.0
Date: 星期四, 三月 01, 2007		Sheet	61 of 94

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TPM 1.2 Module



		Title :TPM	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size A	Project Name A8N_A8Dc		Rev 1.0
Date: 星期四, 三月 01, 2007		Sheet 62	of 94

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	5	4	3	2	1
D					
C					
B					
A					

		Title : BLANK	
ASUSTeK COMPUTER INC		Engineer:	
Size A	Project Name A8N_A8Dc		Rev 0
Date: 星期四, 三月 01, 2007		Sheet 63 of 94	

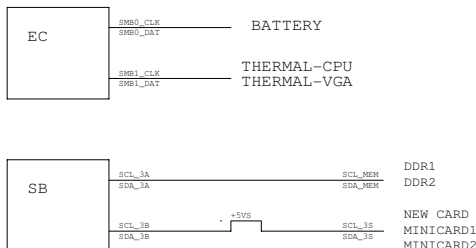
<< Kennedy_Zhang >>

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARDBUS	AD22 CHANGE 1215-06	1	Y, Z

SM-Bus Device	SM-Bus Address
SO-DIMM 0 (low)	
SPD	A0
SO-DIMM 1(high)	
SPD	A4
G781-1	9A
G781(VGA board)	98

CHANGE 0102-07

Thermal Sensor (CPU)
SM-Bus Mapping 1001100



BOM option

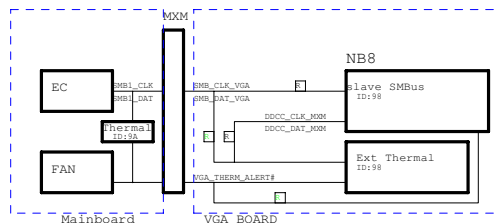
nGM:yellow
nPM:light red
=====

nGM :no stuff for A8N
nPM :no stuff for A8Dc
nGM1:no stuff for A8N, A8N/SR mount for debugging A8S in advance
3G :for Windigo, SR mount for debugging
SR :for SR debugging, should be removed or no stuff @ ER

Support ID2:

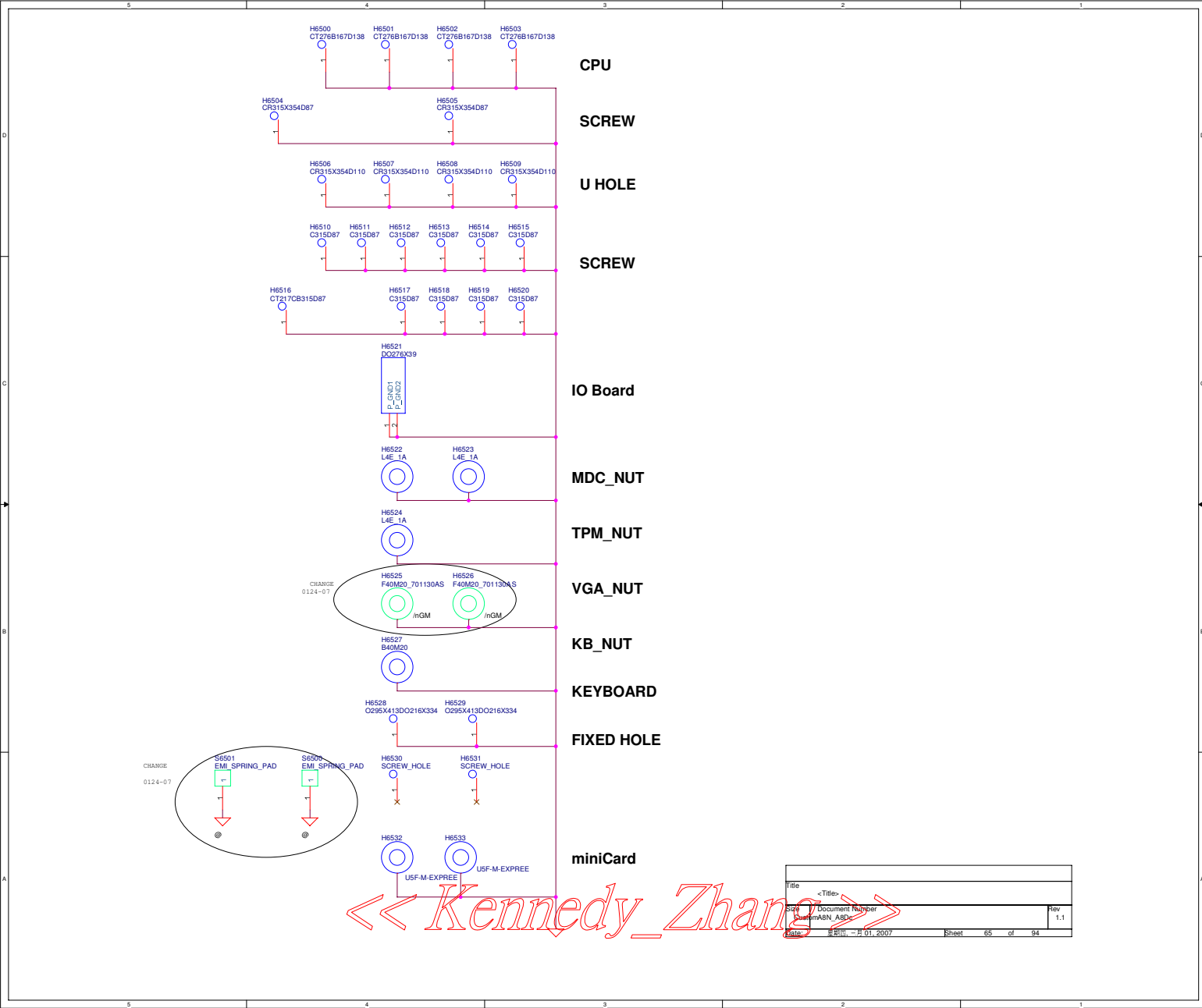
Support ID2:
page 68,Finger print
page 55,IR
Page 56,pwr switch and LED

Thermal block diagram



ASUS		Title :	
ASUSTek COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name		Rev
B	A8N_A8Dc		1.0
Date: 11/01/2007		Sheet 64 of 94	

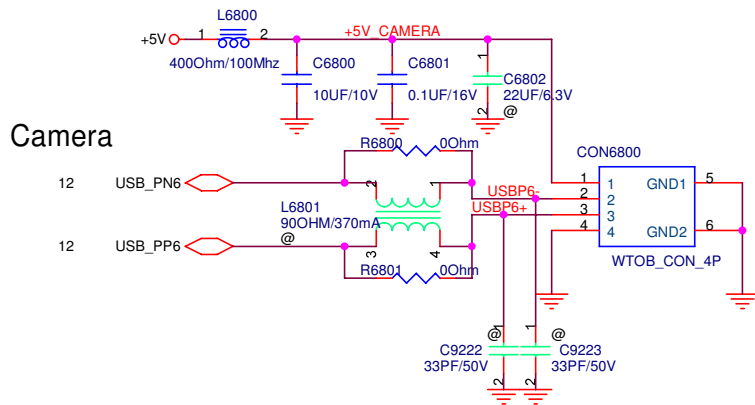
<< Kennedy_Zhang >>



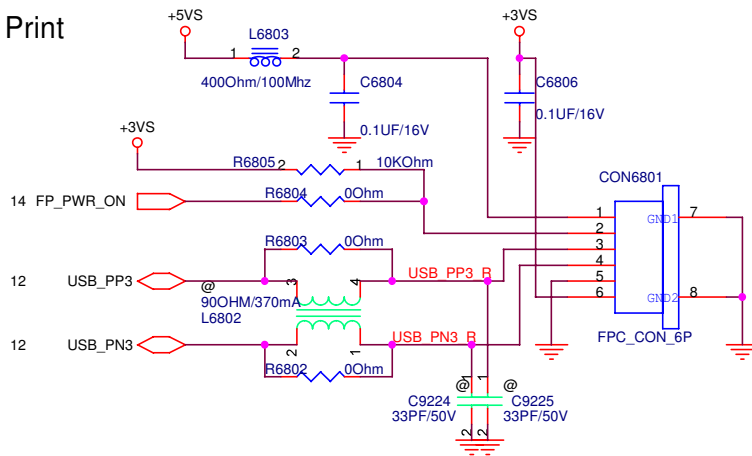
File			<Title>
Size	Document Number	Rev	
Summa8N_A8Dc		1.1	
Date	8/01/2007	Sheet	65 of 94

		Title : BLANK	
ASUSTek COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name		Rev
B	A8N A8Dc		0
Date: 8/20/07 - 01/01/2007		Sheet 66 of 94	

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Finger Print



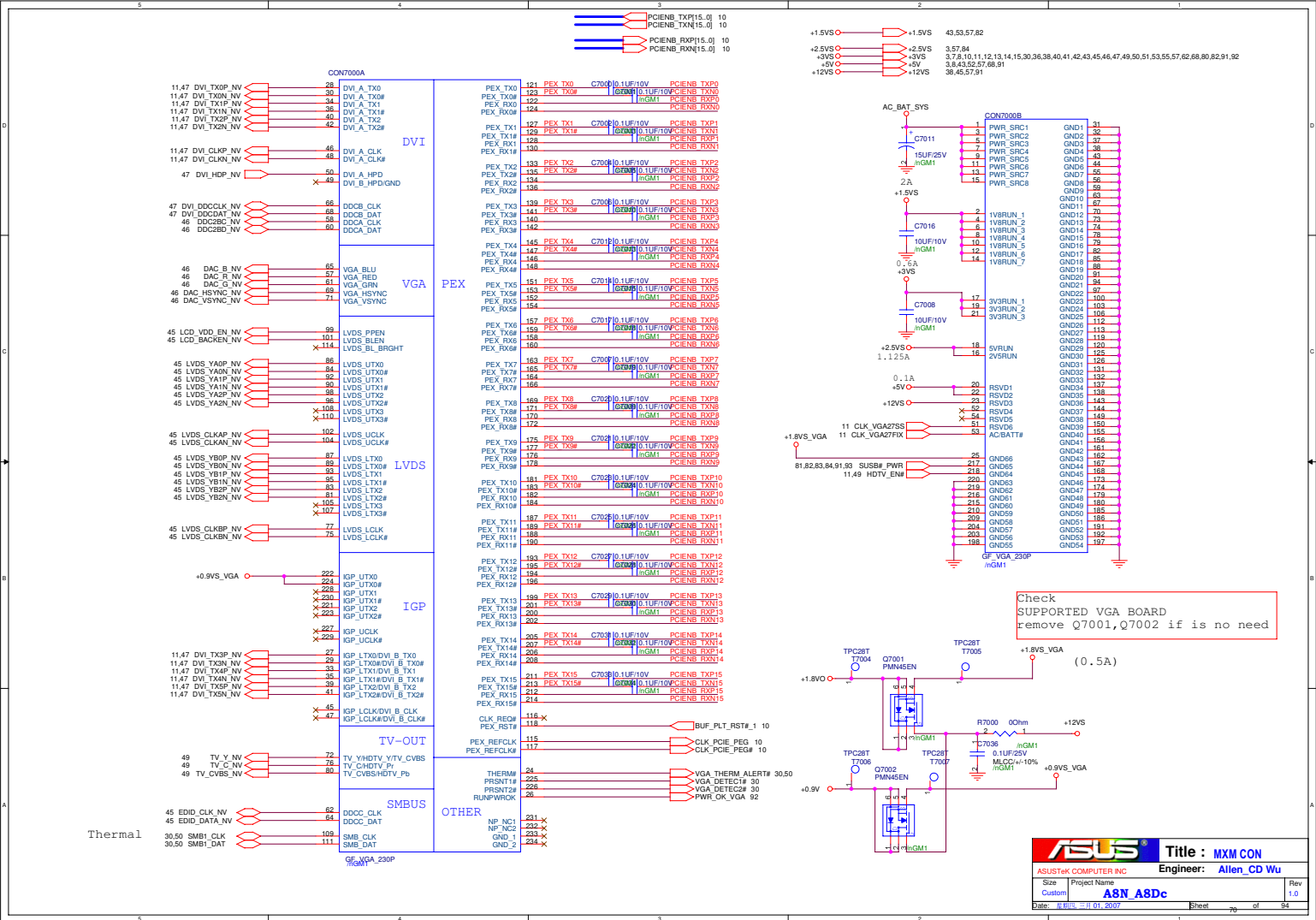
ASUS		Title : CAMERA/FingerPrinter	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name		Rev
A	A8N_A8Dc		1.0
Date: 星期四, 三月 01, 2007		Sheet 60	of 94

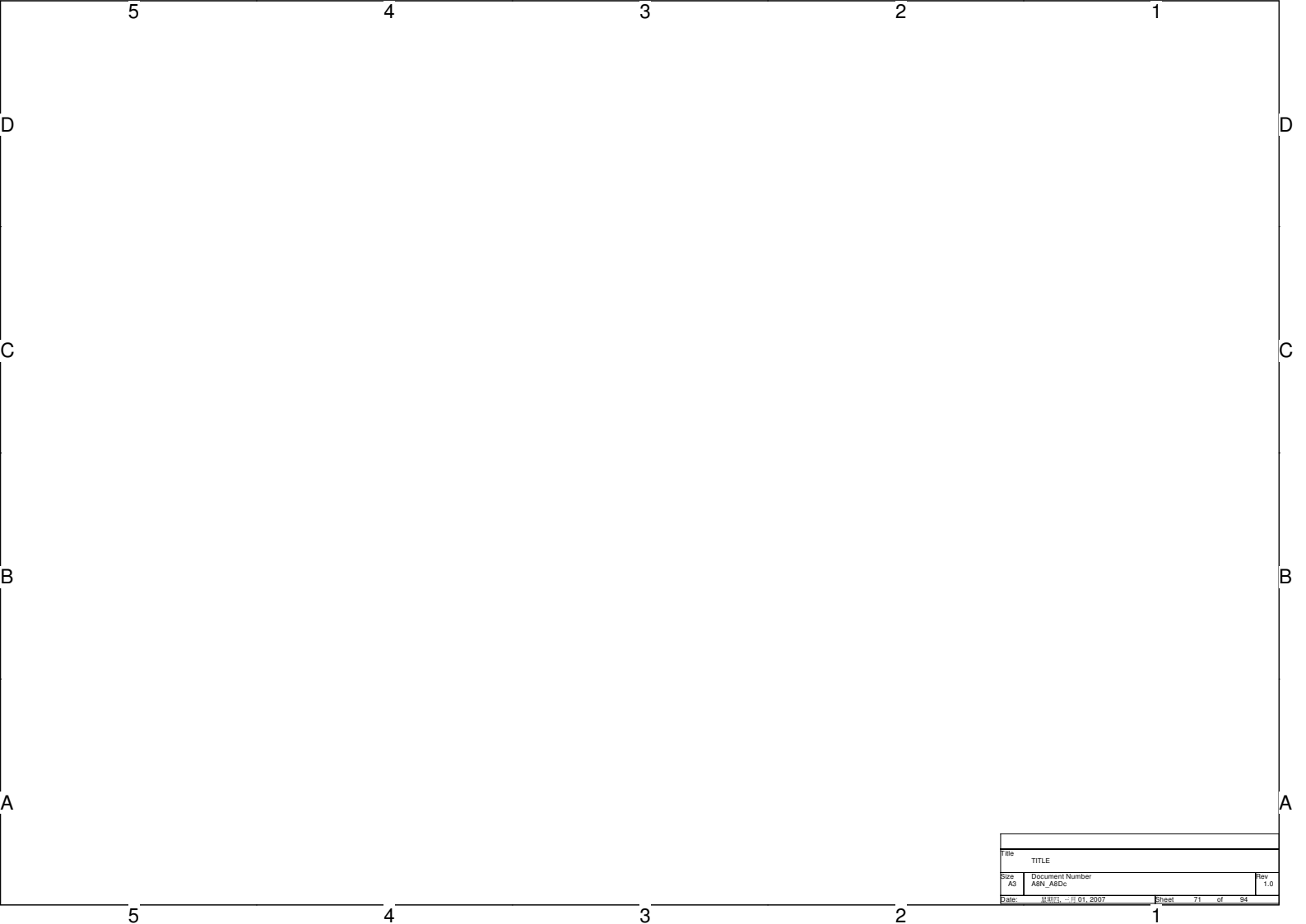
<< Kennedy_Zhang >>

	5	4	3	2	1
D					
C					
B					
A					

		Title : BLANK
ASUSTeK COMPUTER INC		Engineer:
Size A	Project Name A8N_A8Dc	Rev 0
Date: 星期四, 三月 01, 2007		Sheet 69 of 94

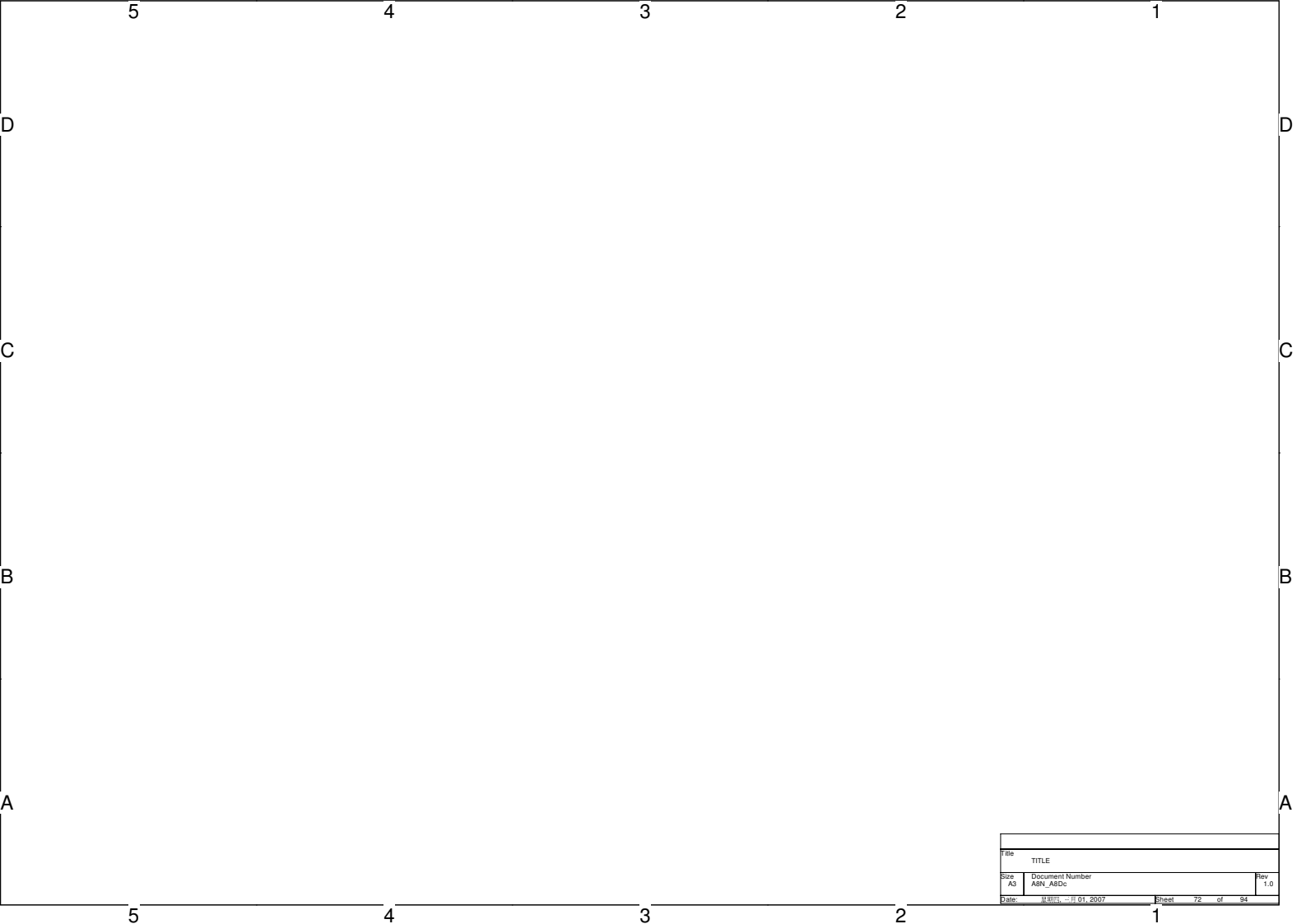
<< Kennedy_Zhang >>





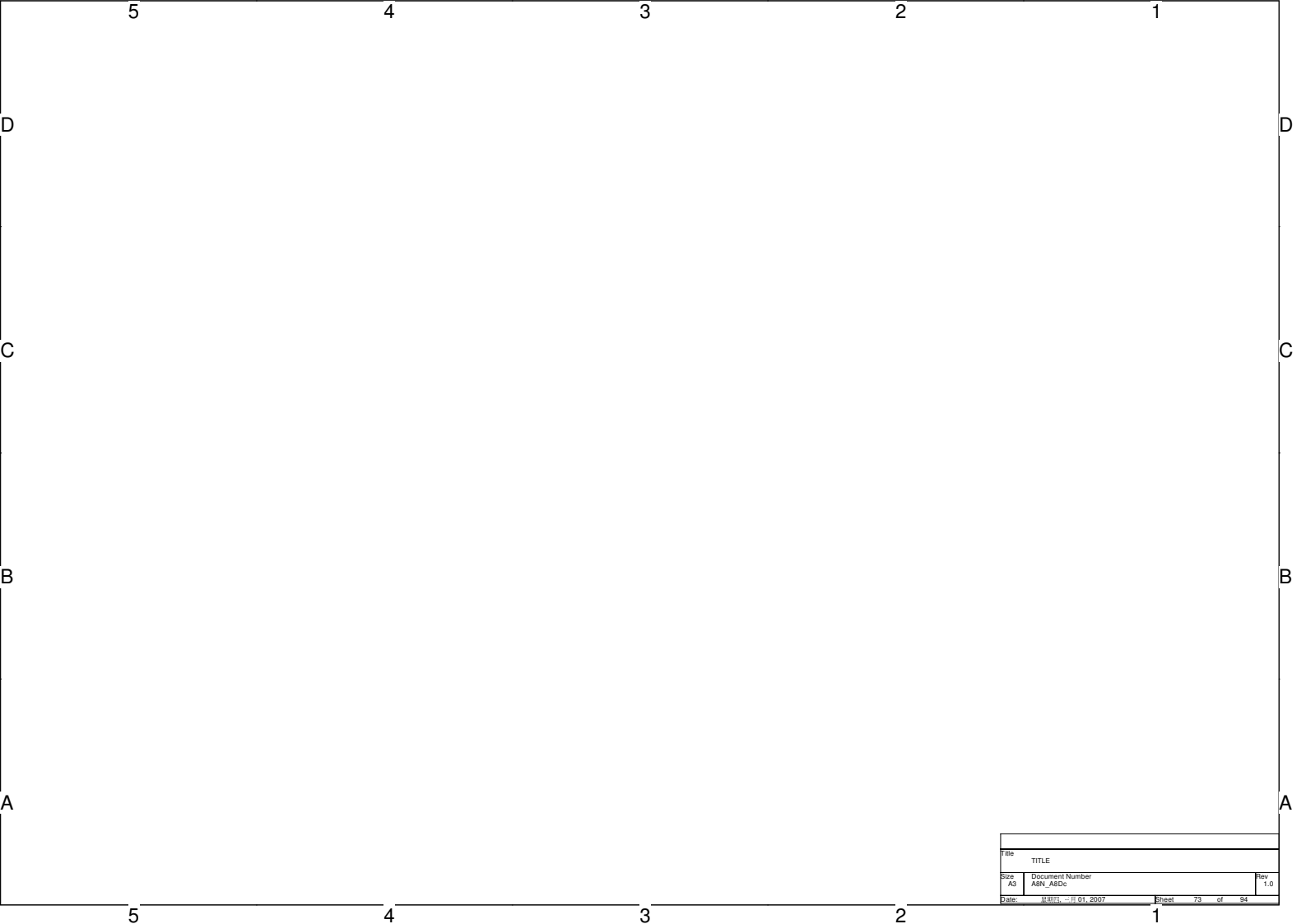
Title		
Size	Document Number	Rev
A3	ABN_ABC	1.0
Date		
Sheet		71 of 94

<< Kennedy_Zhang >>



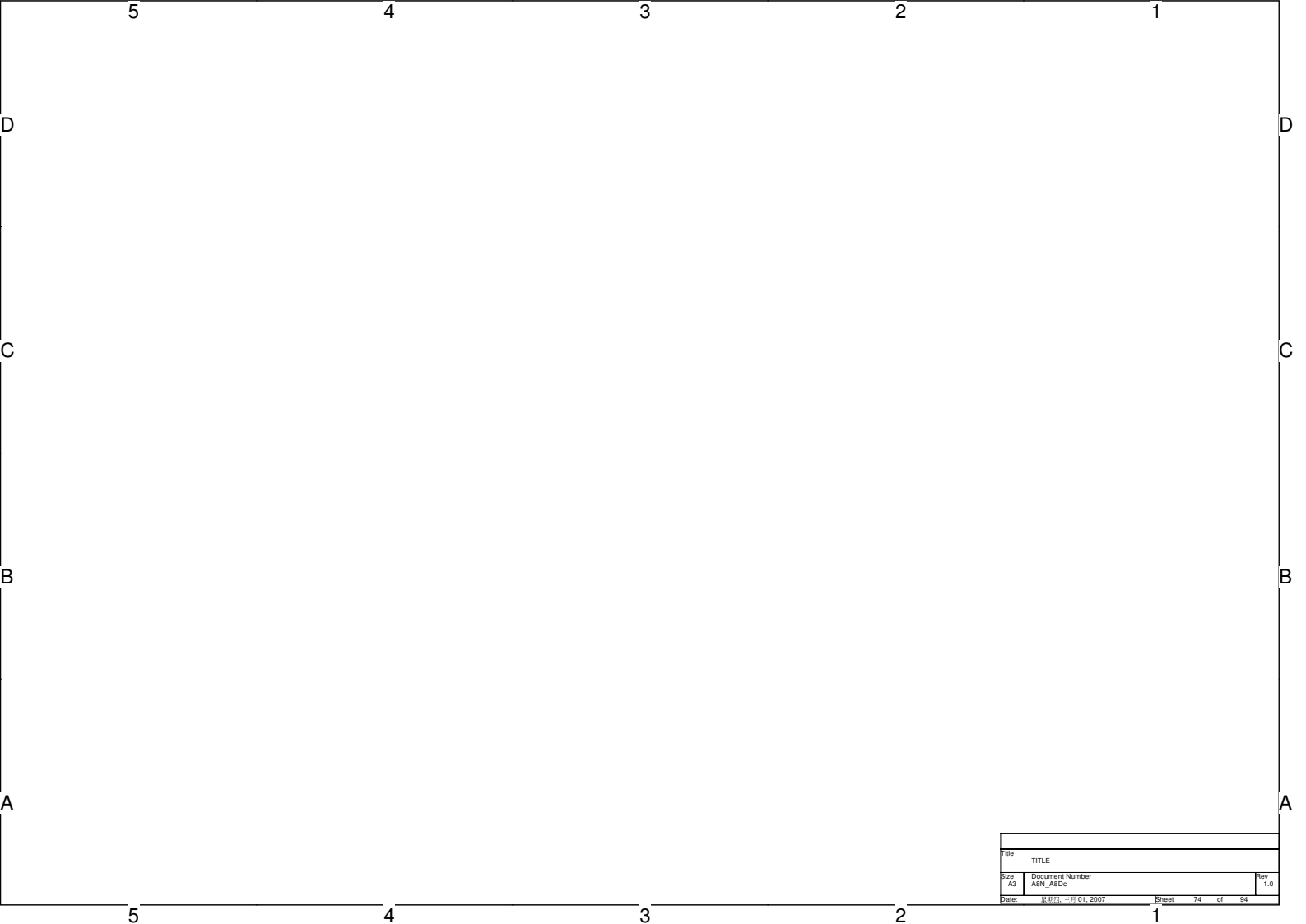
Title		
Size	Document Number	Rev
A3	ABN_ABC	1.0
Date	Sheet 72 of 94	

<< Kennedy_Zhang >>



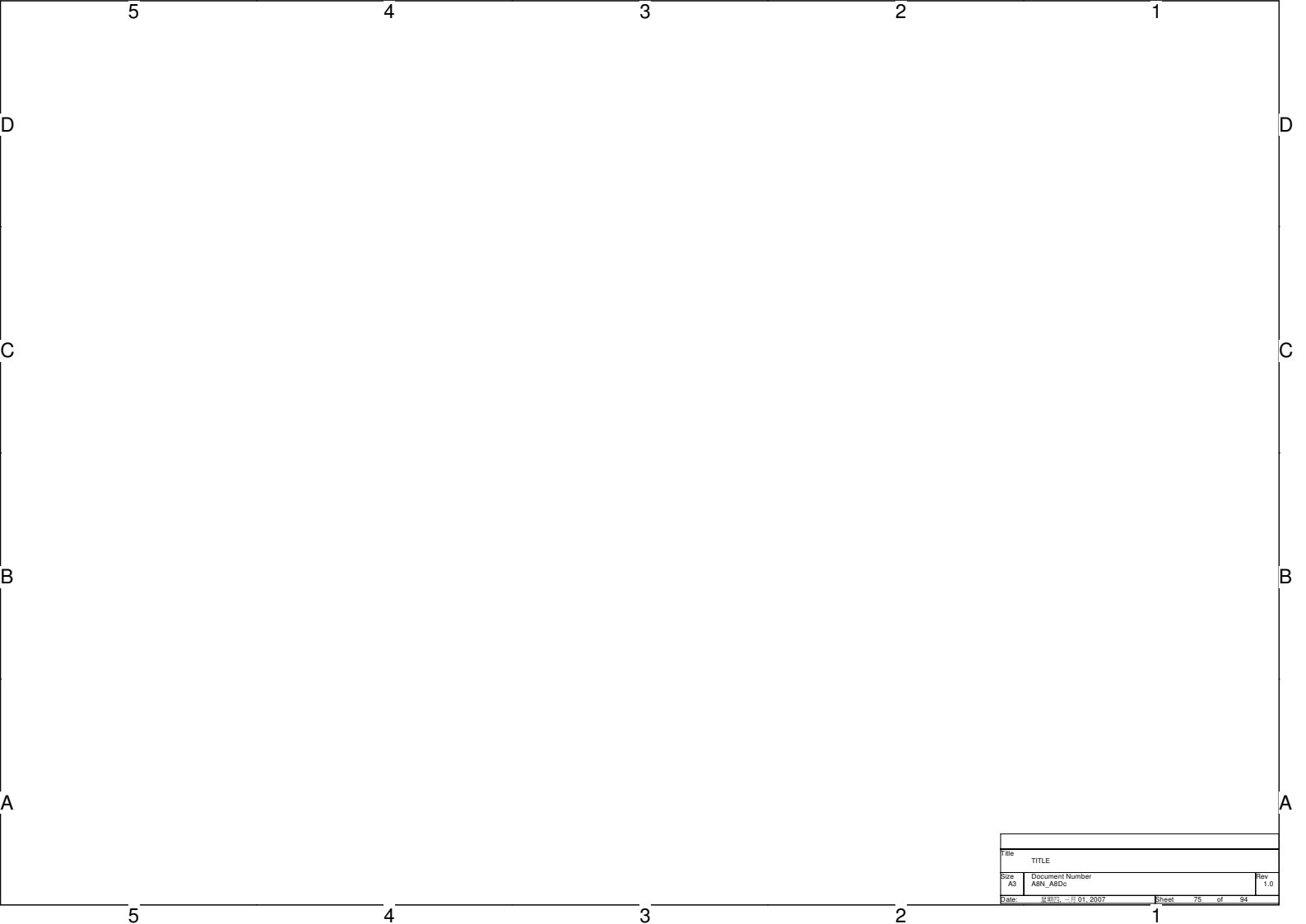
Title		
TITLE		
Size	Document Number	Rev
A3	A8N_A8Dc	1.0
Date:	日期: 一月 01, 2007	
Sheet 73 of 94		

<< Kennedy_Zhang >>



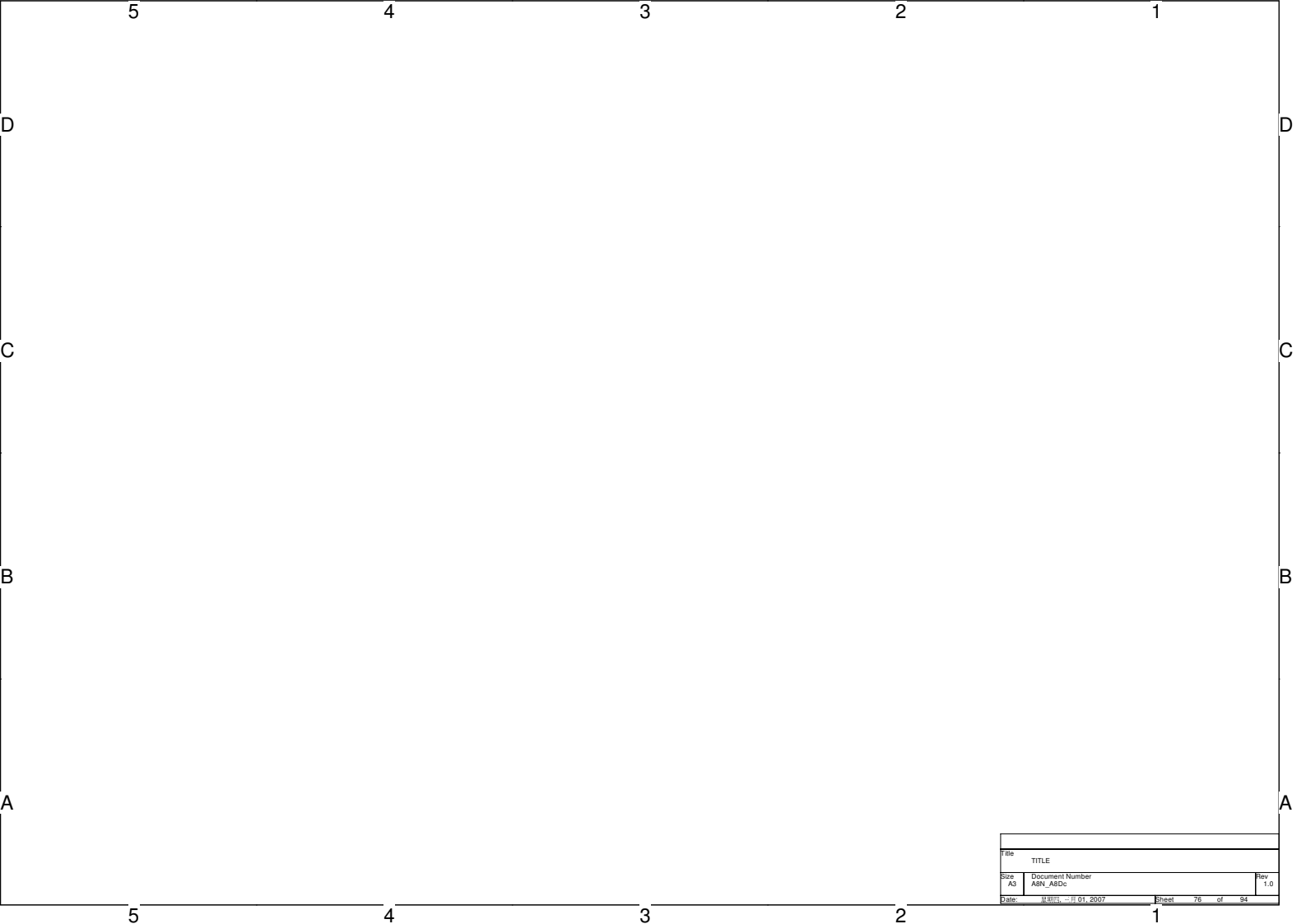
Title		
Size	Document Number	Rev
A3	ABN_ABC	1.0
Date	12/01/2007	
Sheet		74 of 94

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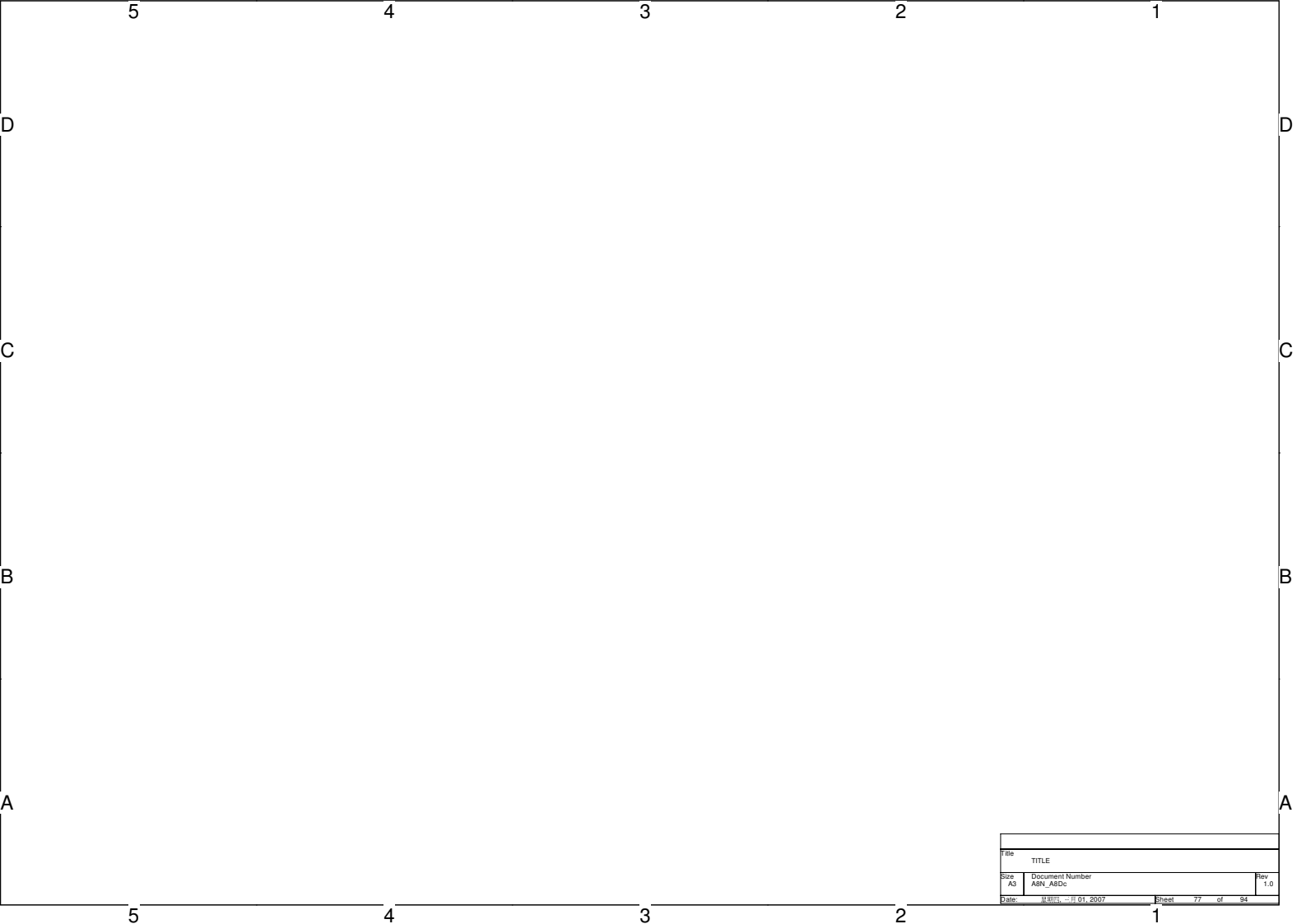
<< Kennedy_Zhang >>

Title		
Size	Document Number	Rev
A3	ABN_ABC	1.0
Date	11/01/2007	Sheet 75 of 94



Title		
Size	Document Number	Rev
A3	ABN_ABC	1.0
Date	Sheet 76 of 94	

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

		Title : BLANK	
ASUSTek COMPUTER INC		Engineer:	
Size	Project Name	Rev	
B	A8N_A8Dc	0	
Date: 01/01/2007		Sheet 78 of 94	

<< Kennedy_Zhang >>

Change Note:

EE :

1. Reference name without 0 tail
2. Synchronize component size and type
3. Remove 0 ohm serial resistor
- 4.
- 5.
- 6.
- 7.
- 8.

Layout :

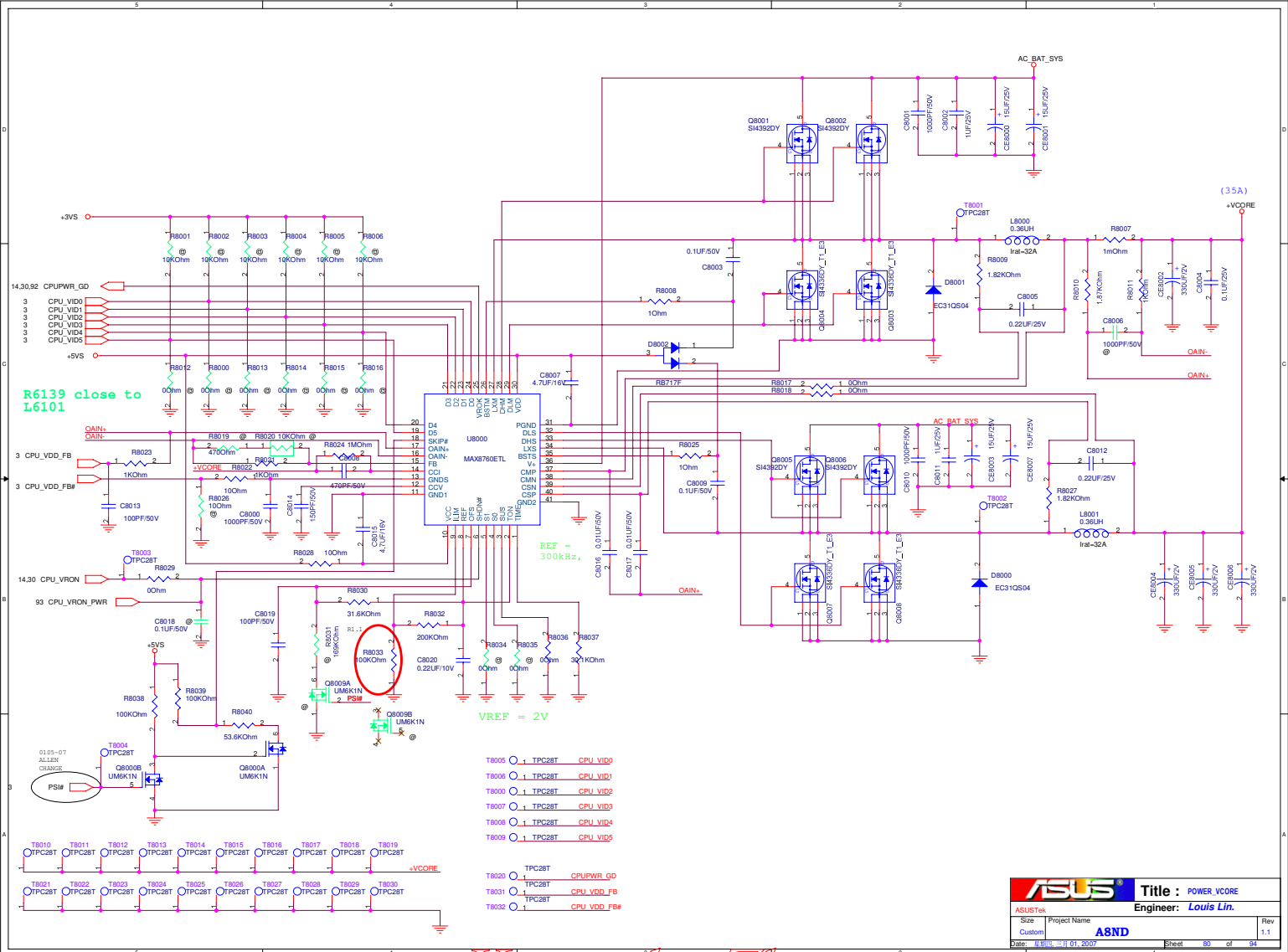
1. PCI MOAT
2. Equalize Crystal and PCI Clock Length
3. VGA Board
4. PCI-E Thread

SMT :

- 1.

		Title : History	
ASUSTeK COMPUTER INC		Engineer: Allen_CD Wu	
Size	Project Name		Rev
Custom	A8N A8Dc		1.0
Date: 星期日, 月 01, 2007		Sheet 79 of 94	

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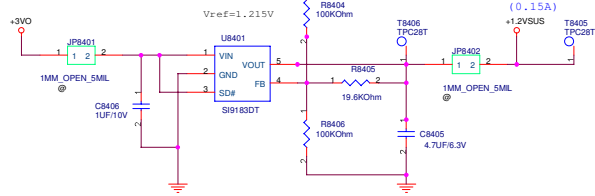


<< Kennedy_Zhang >>

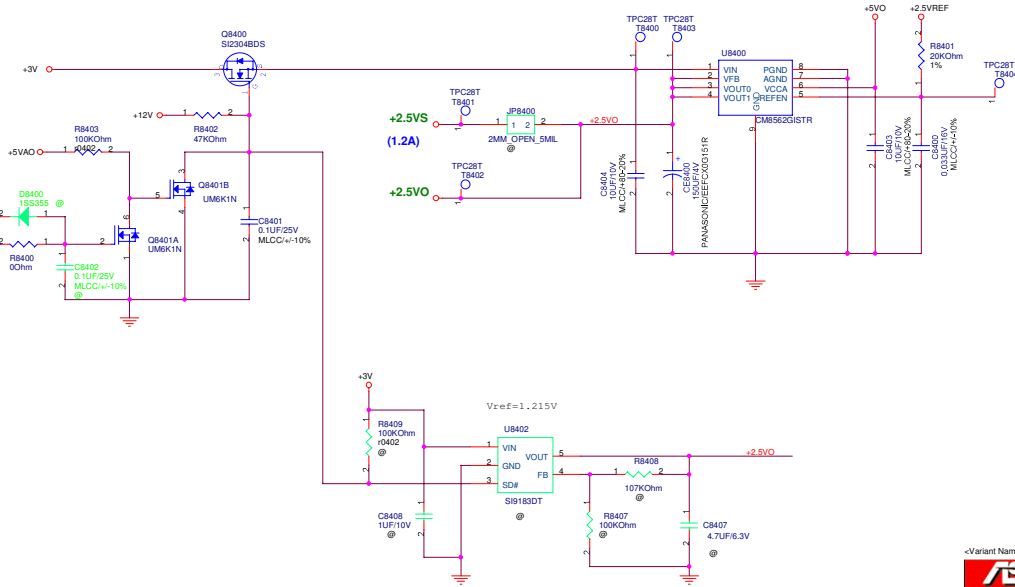


+1.2VSUS

+2.5VREF




+2.5VS



<Variant Name>

ASUS		Title : POWER_IQ_+1.2VSUS & +2.5V	
<OrigName>		Engineer: Louis Lin.	
Size	Project Name	Rev	
Custom	A8ND	1.1	
Date	2007-01-01	Sheet	84 of 84

<< Kennedy_Zhang >>

<Variant Name>				Title : POWER_VGA_CORE & *1.2V0	
<SigName>		Engineer: Louis Lin.			
Size	Project Name			Rev	
C	ARND			1.1	
DATE	2018.12.07			Sheet	85 of 85

<< Kennedy_Zhang >>

<Variant Name>		Title : N/A	
<OrgName>		Engineer:	
Size B	Project Name A8ND		Rev 1.1
Date: 11/02/2007	Sheet 86	of	94

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POWER PATH & BAT_LEARN

● AC_IN Threshold: 2.648Vmax AD_DOCK_IN
 > 17.4W active

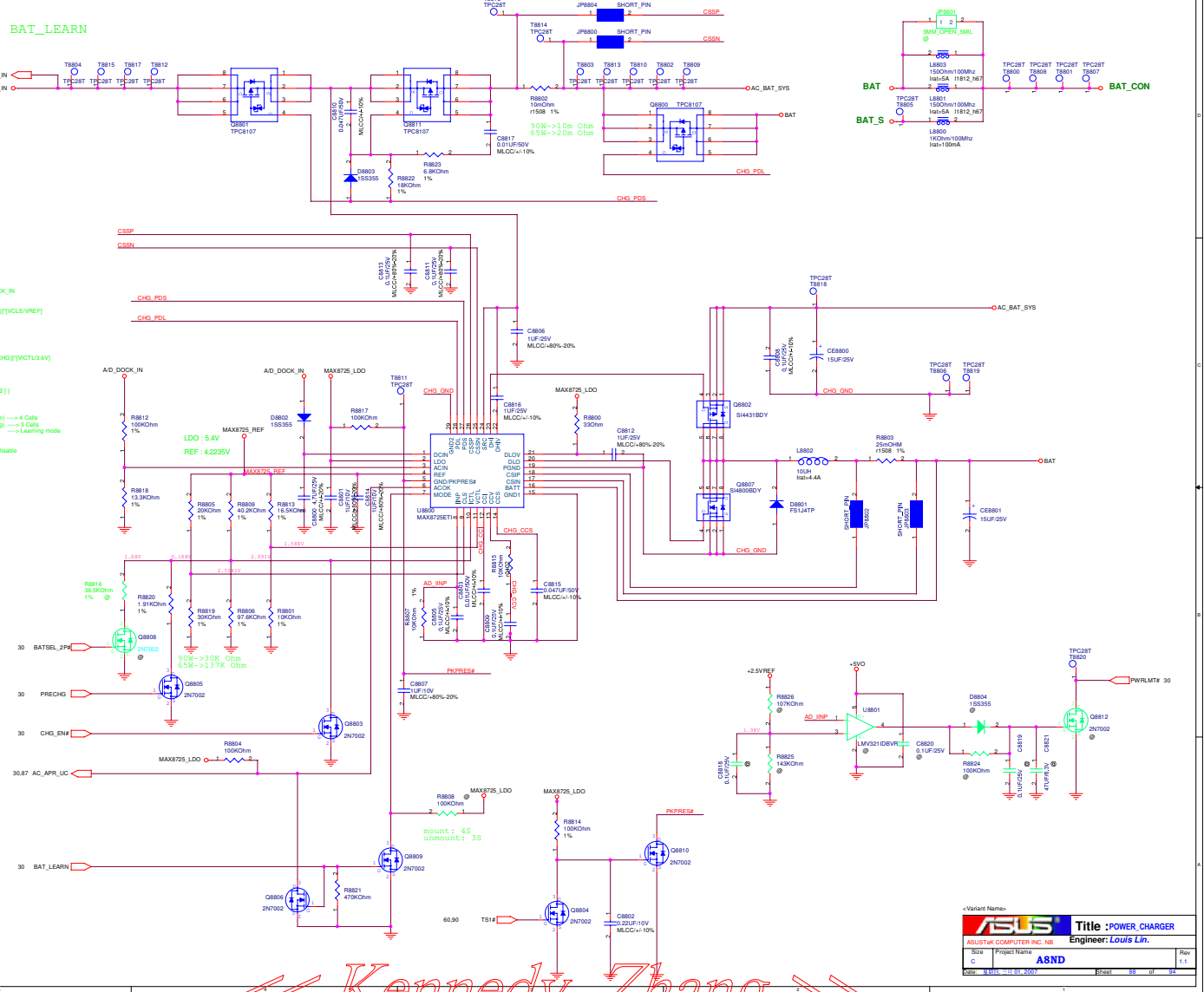
Adapter In(max) = (0.075V/Rsense/ADIN)(VCL5_VREF)
 Resense/ADIN=0.010ohm
 VCL5=5.544V
 => In(max)=4.5A
 => Constant Power = 19 * 4.5 = 85.5W
 => R8805=20K, R8819=30K

Charge Current Ichg = (0.075V/Rsense/CHG5)(VCTL5_VREF)
 Resense/CHG5=0.025ohm
 VCTL5_VREF = 1.0V
 => Ichg = 2.5A
 VCTL5 = 1.68V => Ichg = 1.4A
 => Vbat = 4.2V

Mode pin : Vmode > 2.8V (line to LDO pin) => 4 Cells
 2.8 > Vmode > 1.6V (floating) => 3 Cells
 0.8 > Vmode (line to GND) => Learning mode

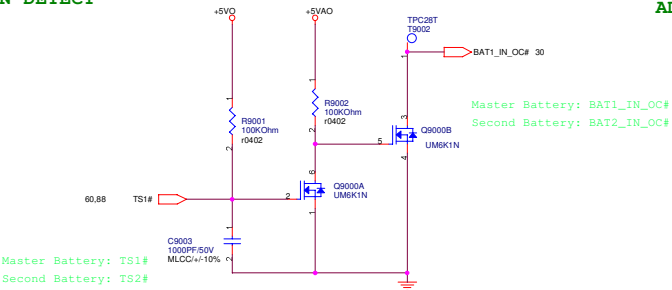
VCTL5 0.8V or DCIN > 7V => Charge Disable

Precharge current=150mA

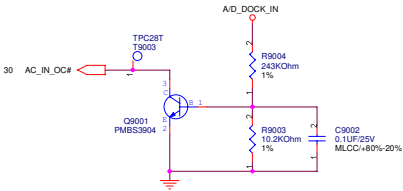


ASUS		Title : POWER CHARGER	
ASUSTeK COMPUTER INC. NE		Engineer: LOUIS LIN.	
Doc	Project Name	Rev	Rev
Doc	ASND	1.1	1.1
Doc	ASND	1.1	1.1

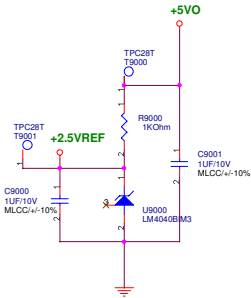
BATTERY IN DETECT



ADAPTER IN DETECT

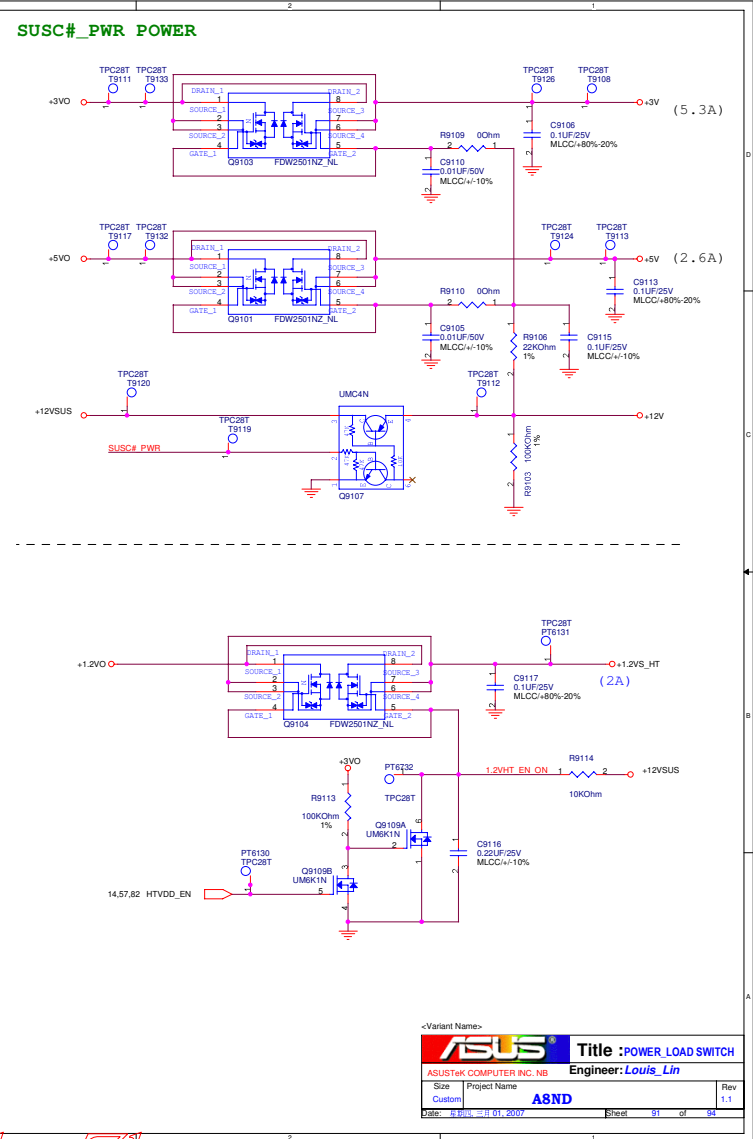
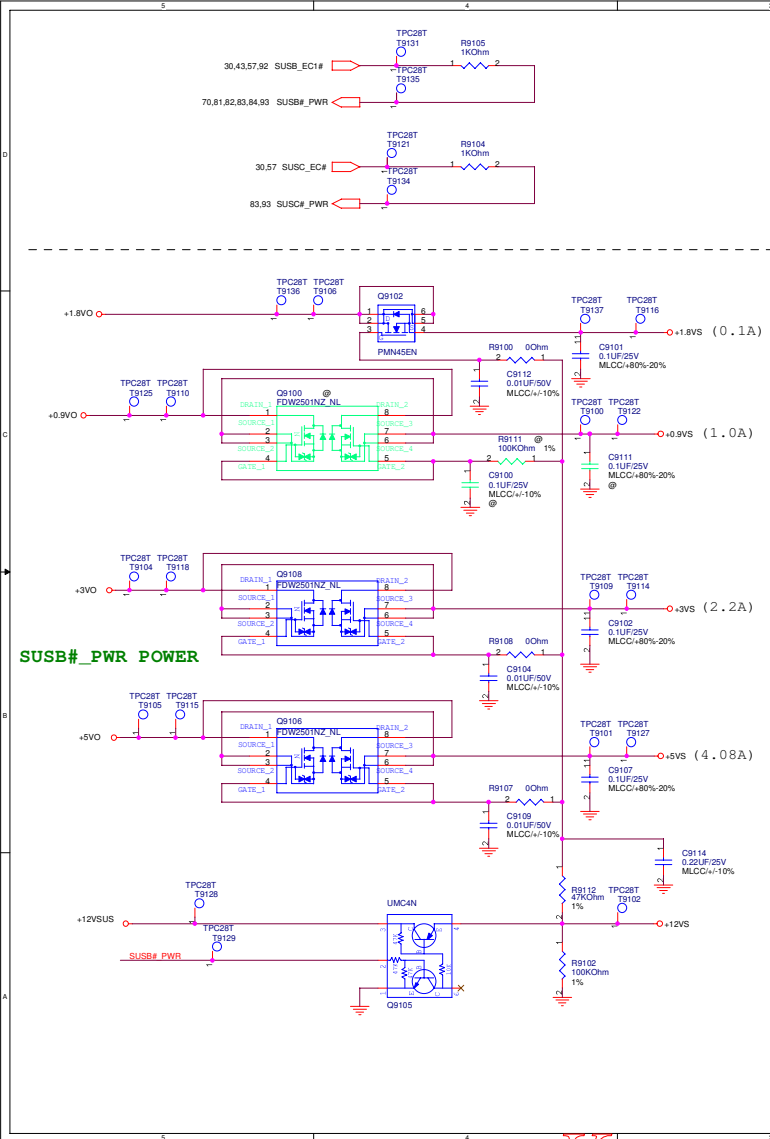


+2.5VREF



<Variant Name>			
		Title :POWER_DETECT	
ASUSTek COMPUTER INC. NB		Engineer: Louis Lin.	
Size	Project Name	Rev	
Custom	A8ND	1.1	
Date: 2007.01.01		Sheet	90 of 94

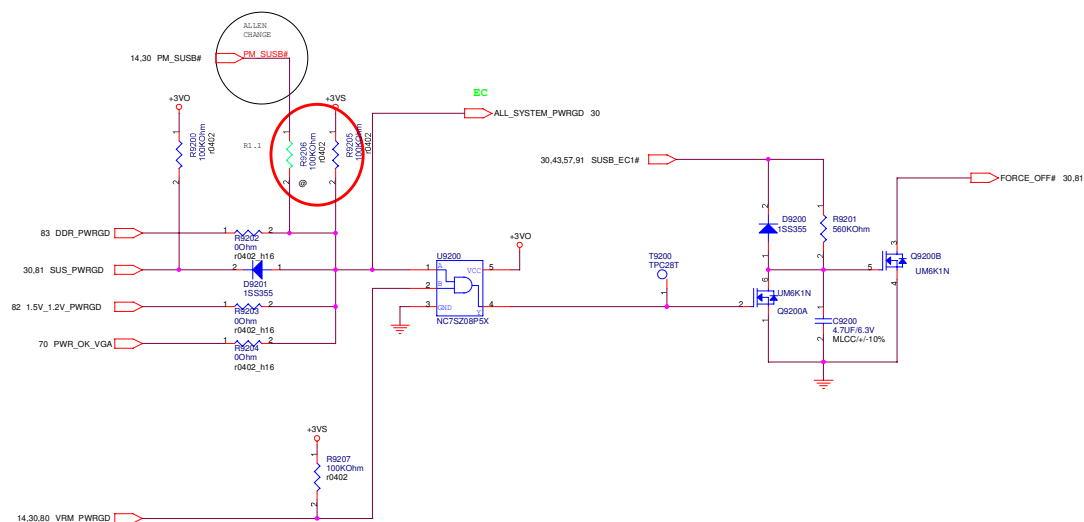
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

ASUS		Title :POWER_LOAD_SWITCH	
ASUSTek COMPUTER INC. NE		Engineer:Louis_Lin	
Size	Project Name	Rev	
Custom	A8ND	1.1	
Date: 2008.01.01		Sheet 81 of 94	

POWER GOOD DETECTOR



<Variant Name>



Title :POWER_PROTECT

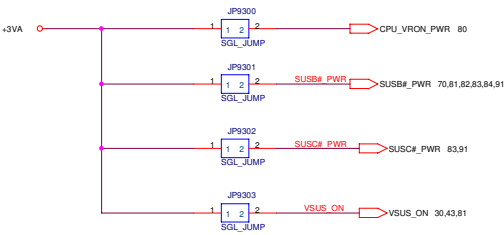
Engineer: *Louis Lin.*

Size	Project Name	Rev
Custom	A8ND	1.1
Date: 星期日, 3月 01, 2007	Sheet 92	of 94

<< Kennedy_Zhang >>

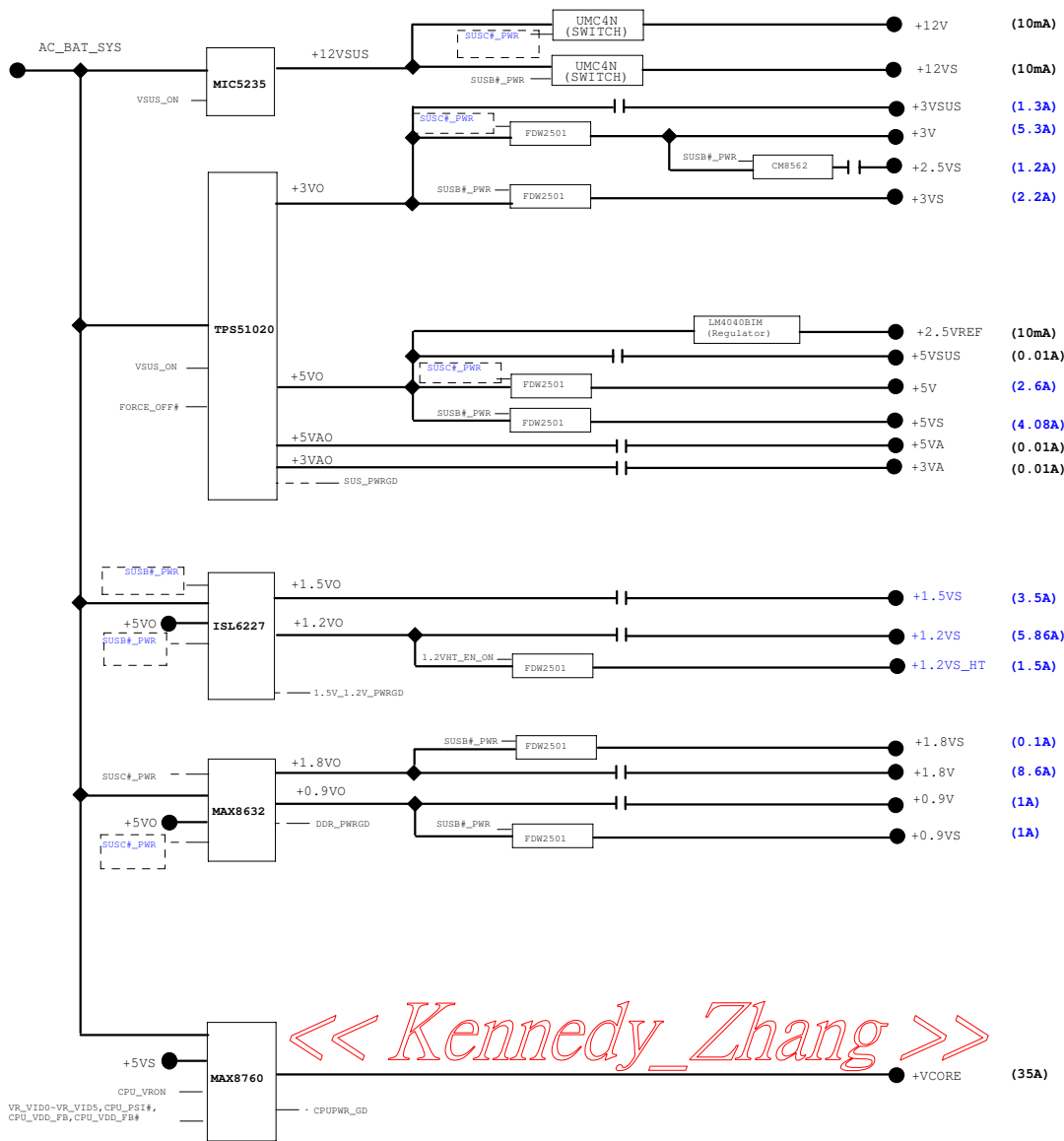
AC_BAT_SYS	AC_BAT_SYS	45,70,80,81,82,83,87,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+2.5VREF	+2.5VREF	84,87,88,90
+3VA	+3VA	13,14,30,57,81,82
+5VAD	+5VAD	81,84,90
+5VO	+5VO	81,82,83,84,88,90,91
+5VSUS	+5VSUS	56,81,87
+5V	+5V	3,8,43,52,57,68,70,91
+5VS	+5VS	15,31,36,38,46,47,50,51,56,57,68,80,91
+3VO	+3VO	81,82,84,91,92
+3VSUS	+3VSUS	3,10,11,12,13,14,30,33,43,53,57,81,82
+3V	+3V	34,43,45,53,56,57,81,82,84,91
+3VS	+3VS	3,7,8,10,11,12,13,14,15,30,36,38,40,41,42,43,45,46,47,49,50,51,53,55,57,62,68,70,80,82,91,92
+12VSUS	+12VSUS	81,91
+12V	+12V	38,42,52,57,84,91
+12VS	+12VS	38,45,57,70,91
+1.8VO	+1.8VO	70,83,91
+1.8V	+1.8V	3,5,7,8,9,57,83
+1.8VS	+1.8VS	3,11,57,91
+0.9VS	+0.9VS	91
+0.9VO	+0.9VO	83,91
+1.5VO	+1.5VO	82
+1.5VS	+1.5VS	43,53,57,70,82
+2.5VO	+2.5VO	84
+2.5VS	+2.5VS	3,57,70,84
+VDDRE	+VDDRE	5,80
+1.25VS	+1.25VS	
+1.2VSUS	+1.2VSUS	11,13,84
+1.2VS	+1.2VS	10,12,13,57,82
+1.2VO	+1.2VO	82,91

FOR POWER TEST



<Variant Name>			
		Title : POWER_SIGNAL	
<OrgName>		Engineer: Louis Lin.	
Size	Project Name		Rev
Custom	A8ND		1.1
Date: 2007.01.01		Sheet	89 of 94

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<< Kennedy_Zhang >>

ASUS		Title : POWER FLOWCHART	
ASUSTeK COMPUTER INC. NB		Engineer: Louis_Lin	
Size	Project Name	Rev	
Custom	A8ND	1.1	
Date: 10/01/2007	Drawn: 01	By: 01	01