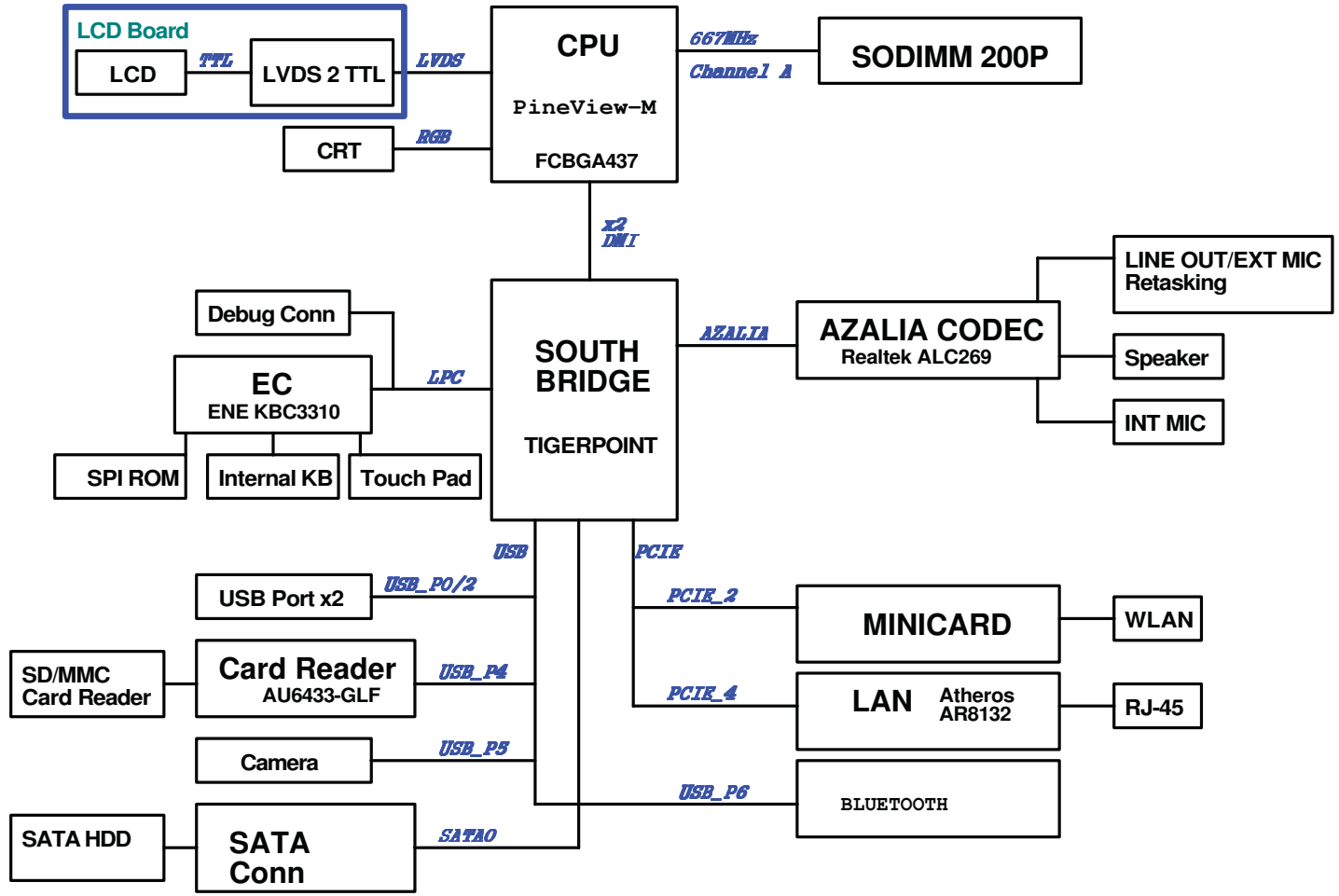
1001PX 1.2G

2010_0428_1600

CLOCK GEN
ICS9LPRS427CGLFT

THERMAL CONTROL



<Core Design>

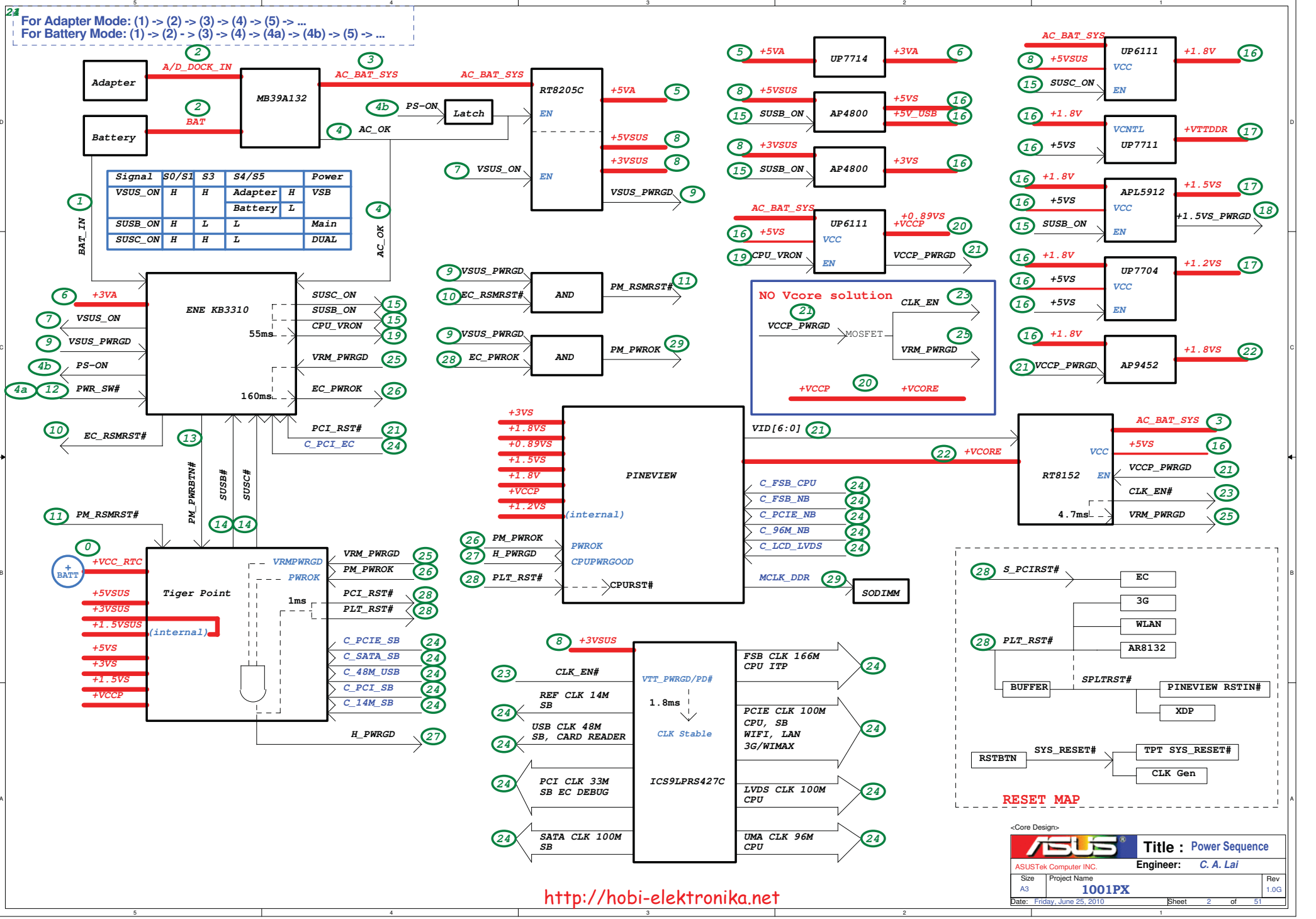
ASUSTek Computer INC.

Title : Block Diagram

Engineer: C. A. Lai

Size	Project Name	Rev
Custom	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 1 of 51


For Adapter Mode: (1) -> (2) -> (3) -> (4) -> (5) -> ...
For Battery Mode: (1) -> (2) - > (3) -> (4) -> (4a) -> (4b) -> (5) -> ...
Adapter
Battery
A/D_DOCK_IN
BAT
MB39A132
AC_BAT_SYS
PS-ON
Latch
AC_OK
RT8205C
EN
+5VA
+5VSUS
+3VSUS
VSUS_PWRGD
VSUS_ON
BAT_IN
Signal | S0/S1 | S3 | S4/S5 | | Power
VSUS_ON | H | H | Adapter | H | VSB
Battery | L
SUSB_ON | H | L | L | Main
SUSC_ON | H | H | L | DUAL
ENE KB3310
55ms
160ms
SUSC_ON
SUSB_ON
CPU_VRON
VRM_PWRGD
EC_PWROK
PCI_RST#
C_PCI_EC
EC_RSMRST#
PM_PWRBTN#
SUSB#
SUSC#
PWR_SW#
AND
PM_RSMRST#
PM_PWROK
UP7714
AP4800
+3VA
+5V
+5V_USB
+3VS
SUSB_ON
UP6111
VCC
+0.89VS
+VCCP
CPU_VRON
VCCP_PWRGD
NO Vcore solution
MOSFET
CLK_EN
VRM_PWRGD
+VCCP
+VCORE
PINEVIEW
(internal)
PWROK
CPUPWRGOOD
CPURST#
VID[6:0]
C_FSB_CPU
C_FSB_NB
C_PCIE_NB
C_96M_NB
C_LCD_LVDS
MCLK_DDR
SODIMM
RT8152
CLK_EN#
4.7ms
UP6111
+1.8V
SUSC_ON
VCNTL
UP7711
+VTTDDR
APL5912
+1.5VS
+1.5VS_PWRGD
UP7704
+1.2VS
AP9452
+1.8VS
Tiger Point
VRMPWRGD
PWROK
1ms
VRM_PWRGD
PM_PWROK
PCI_RST#
PLT_RST#
C_PCIE_SB
C_SATA_SB
C_48M_USB
C_PCI_SB
C_14M_SB
H_PWRGD
+VCC_RTC
BATT
+5VSUS
+3VSUS
+1.5VSUS
+5VS
+3VS
+1.5VS
+VCCP
VTT_PWRGD/PD#
1.8ms
CLK Stable
ICS9LPRS427C
CLK_EN#
REF CLK 14M SB
USB CLK 48M SB, CARD READER
PCI CLK 33M SB EC DEBUG
SATA CLK 100M SB
FSB CLK 166M CPU ITP
PCIE CLK 100M CPU, SB WIFI, LAN 3G/WIMAX
LVDS CLK 100M CPU
UMA CLK 96M CPU
S_PCIRST#
EC
3G
WLAN
AR8132
PLT_RST#
BUFFER
SPLTRST#
PINEVIEW RSTIN#
XDP
RSTBTN
SYS_RESET#
TPT SYS_RESET#
CLK Gen
RESET MAP
<Core Design>
ASUSTek Computer INC.
Title : Power Sequence
Engineer: C. A. Lai
Size A3
Project Name 1001PX
Rev 1.0G
Date: Friday, June 25, 2010
Sheet 2 of 51
http://hobi-elektronika.net

1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

FS4	Function
H	FIXED PLL (Asynchronous)
L	PCI/PCIEX PLL(synchronize)

CR1 1MOhm /X
CX1 14.31818Mhz
C_XIN
C_XOUT
CC12 18PF/50V
CC13 18PF/50V
GND
01/12 fine tune 15p->18p

+3VSUS
CL1
120Ohm/100Mhz N/A
+3V_CLK
CC1 10UF/6.3V c0603
CC58 0.1UF/16V
CC2 0.1UF/16V
CC3 0.1UF/16V
CC4 0.1UF/16V
CC5 0.1UF/16V
CC6 0.1UF/16V
CC7 0.1UF/16V
CC8 0.1UF/16V
CC9 0.1UF/16V
CC10 0.1UF/16V
CL4 120Ohm/100Mhz N/A
+3V_CLK_VDDA
CC48 0.1UF/16V
CC58 for RF , close to pin 42

12/24 reserve for static OC
(24) SOC
CR7 0Ohm /X
C_FSLB
place close CR5

01/21 EMI
C_LAN_25_R
CC555 33PF/50V /EMI/LAN25M

C_SATA_SB CC50 10PF/50V /X
C_SATA_SB# CC51 10PF/50V /X
C_LCD_LVDS# CC54 10PF/50V /X
C_LCD_LVDS CC55 10PF/50V /X
STP_PCI# EC7 10PF/50V /EMI/X
STP_CPU# EC10 10PF/50V /EMI/X
C_PCI_SB_R CC36 10PF/50V /X
FS4 CC37 10PF/50V /X
S_SMBDATA EC14 10PF/50V /EMI/X
S_SMBCLK EC15 10PF/50V /EMI/X
C_DOC_REQ EC16 10PF/50V /EMI/X
C_FSLC CC39 10PF/50V /X
C_FSLA CC40 10PF/50V /X
C_48M_R CC35 10PF/50V /X
For RF,EMI
GND

CU1
ICS9LPRS427CGLFT
+3V_CLK
+3V_CLK_VDDA
01/28 change
12/15 add C_LAN_25M
12/15 del for Lan 25M
12/14 del 3G

Pin		Pin	
1	VDD1	56	25MHz/FREERUN
2	GND1	55	PCI&PCIEX_STOP#
3	PEREQ1#	54	CPU_STOP#
4	PEREQ2#	53	REF0/FSLC
5	FS4/PCICLK0	52	DOC_PEREQ3#
6	GND2	51	GND4
7	VDDPCI	50	X1
8	ITP_EN/PCICLK_F0	49	X2
9	SEL12_48#/12_48MHz	48	VDDREF
10	Vtt_PwrGd/PD#	47	SDATA
11	VDD2	46	SCLK
12	FSLA/USB_48MHz	45	GND5
13	GND3	44	CPUT_LR0
14	DOTT_96MHzLR	43	CPUC_LR0
15	DOTC_96MHzLR	42	VDDCPU
16	FSLB	41	CPUT_LR1
17	PCIeT_LR0	40	CPUC_LR1
18	PCIeC_LR0	39	RESET#
19	PCIeT_LR1	38	GNDA
20	PCIeC_LR1	37	VDDA
21	VDDPCIEX1	36	CPUITPT_LR2/PCIeT_LR6
22	PCIeT_LR2	35	CPUITPC_LR2/PCIeC_LR6
23	PCIeC_LR2	34	VDDPCIEX3
24	PCIeT_LR3	33	PCIeT_LR5
25	PCIeC_LR3	32	PCIeC_LR5
26	SATACLKT_LR	31	PCIeT_LR4
27	SATACLKC_LR	30	PCIeC_LR4
28	VDDPCIEX2	29	GND6

PEREQ1# C_REQ#_WLAN
CR8 33Ohm/DEBUG FS4
CRN8B 22Ohm
CRN8A 22Ohm
CR12 33Ohm
CLK_EN
CR3 33Ohm
C_FSLA
C_FSLB
C_LAN_25_R 47Ohm /LAN25M CR6
C_FSLC 33Ohm CR4
C_DOC_REQ 0Ohm CR22 /X CLK_PEREQ#3
C_XIN
C_XOUT
S_SMBDATA
S_SMBCLK
C_RESET# CR21 /X 0Ohm

(26) C_PCI_DEBUG
(24) C_LPC_EC
(8) C_PCI_SB
(21) C_48M_CARD_READER
C_PCI_SB_R
C_48M_R
(8) C_48M_USB
(5) C_96M_NB
(5) C_96M_NB#
(5) C_LCD_LVDS
(5) C_LCD_LVDS#
(4) C_PCIE_NB
(4) C_PCIE_NB#
(17) C_PCIE_WLAN
(17) C_PCIE_WLAN#
(9) C_SATA_SB
(9) C_SATA_SB#

C_LAN_25M (28)
STP_PCI# (9)
STP_CPU# (9)
C_14M_SB (9)
S_SMBDATA (9)
S_SMBCLK (9)
C_FSB_CPU (4)
C_FSB_CPU# (4)
C_FSB_NB (5)
C_FSB_NB# (5)
SYS_RESET# (7,9)
H_ITP_CLK (7)
H_ITP_CLK# (7)
C_PCIE_LAN (28)
C_PCIE_LAN# (28)
C_PCIE_SB (8)
C_PCIE_SB# (8)

+3V_CLK
C_FSLB CR5 10KOhm
CR32 8.2KOhm /X
GND

+3V_CLK
C_FSLA CR33 8.2KOhm
C_FSLC CR34 8.2KOhm
C_48M_R CR35 8.2KOhm
GND

FSLC	FSLB	FSLA	CPU(MHZ)
0	1	1	166
0	0	1	133

+3V_CLK
CR36 4.7KOhm 1% /X
CR37 4.7KOhm 1% /X
CLK_PEREQ#3
(24) DOC1
CQ2A UM6K1N /X
CR38 39KOHM /X
CQ2B UM6K1N /X
DOC2 (24)
GND

+3VS
CR44 10KOhm
12/15 need check
CLK_EN
CQ4 2N7002 /VCORE
CR14 100KOhm /X
CC34 0.1UF/16V
(35) CLK_EN#
GND

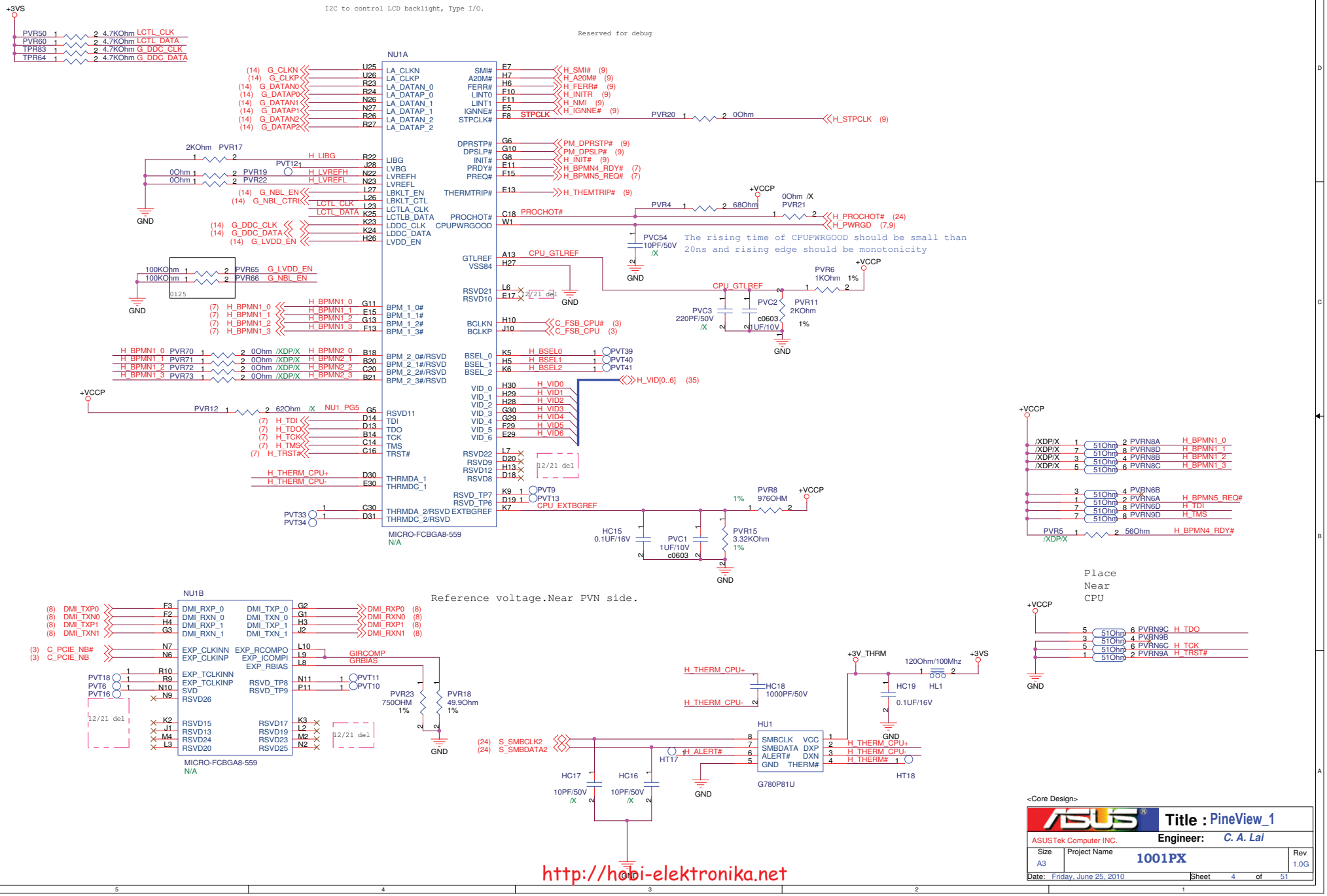
12/17 add CR45 for Free run after power up
+3V_CLK
/LAN25M
C_LAN_25M CR45 8.2KOhm
C_DOC_REQ CR41 8.2KOhm
C_REQ#_WLAN CR42 8.2KOhm
PEREQ1# CR43 8.2KOhm
C_PCI_SB_R CR30 8.2KOhm

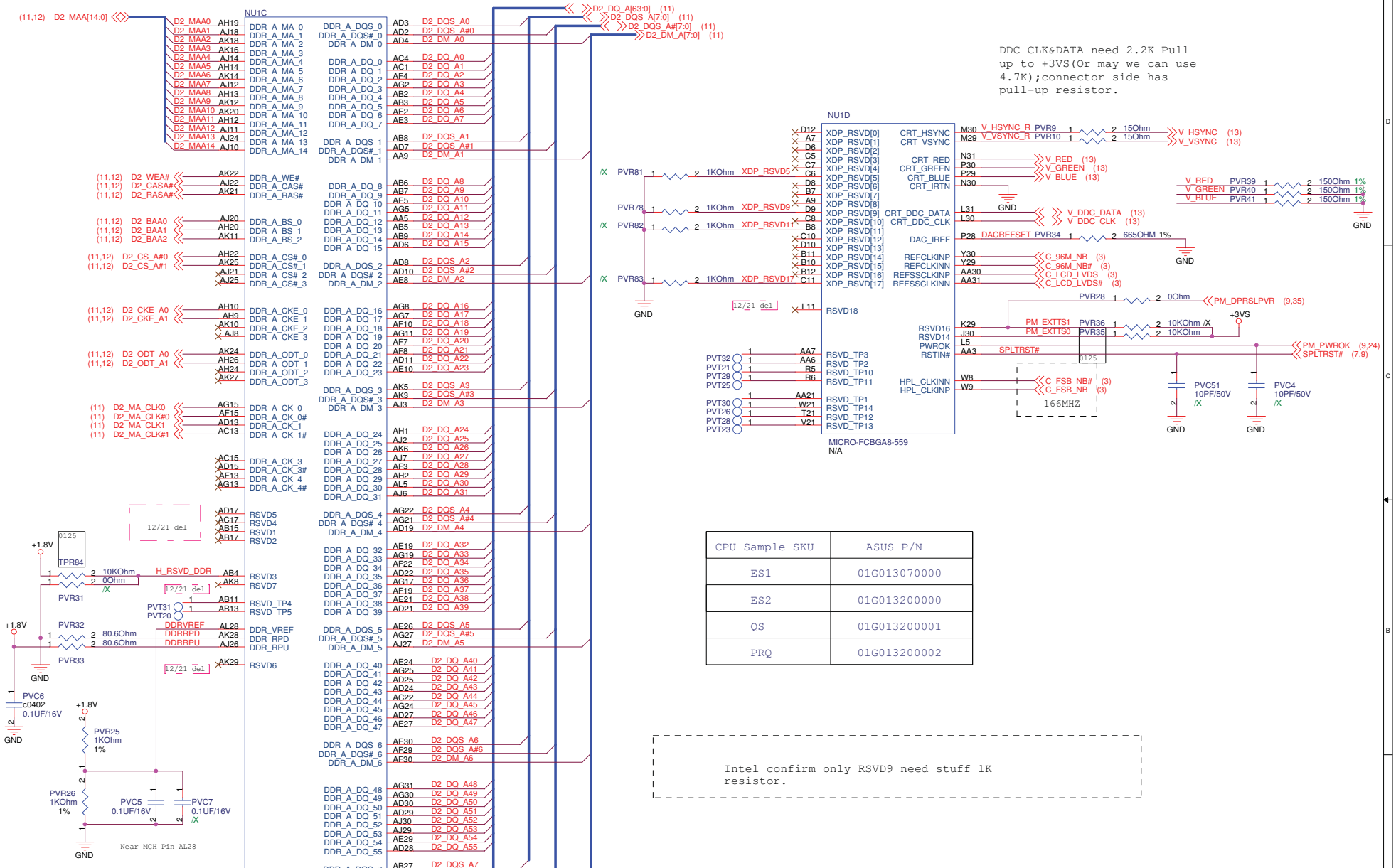
O_DOC1	O_DOC2	Voltage	Status
L	L	2.4-3.3V	Super
L	H	0.5-2.36V	Normal
H	*	0-0.35V	Power saving

CR17 0Ohm /X
CLK_EN
+3V_CLK
CR16 10KOhm
VCCP_OK_R#
CQ1B UM6K1N
CQ1A UM6K1N
(35,37,38,39) VCCP_PWRGD
Clock enable.
GND

+3V_CLK
FS4
/X
CR2 8.2KOhm
CR9 8.2KOhm
GND

<Core Design>
ASUSTek Computer INC.
Title : ICS9LPRS427C
Engineer: C. A. Lai
Size A3
Project Name 1001PX
Rev 1.0G
Date: Friday, June 25, 2010
Sheet 3 of 51


I2C to control LCD backlight, Type I/O.
Reserved for debug
NU1A
MICRO-FCBGA8-559
N/A
The rising time of CPUPWRGOOD should be small than 20ns and rising edge should be monotonicity
Reference voltage.Near PVN side.
Place Near CPU
NU1B
MICRO-FCBGA8-559
N/A
HU1
G780P81U
Title : PineView_1
ASUSTek Computer INC.
Engineer: C. A. Lai
Project Name 1001PX
Rev 1.0G
Date: Friday, June 25, 2010
Sheet 4 of 51
http://hobi-elektronika.net



CPU Sample SKU	ASUS P/N
ES1	01G013070000
ES2	01G013200000
QS	01G013200001
PRQ	01G013200002

Intel confirm only RSVD9 need stuff 1K resistor.

<Core Design>

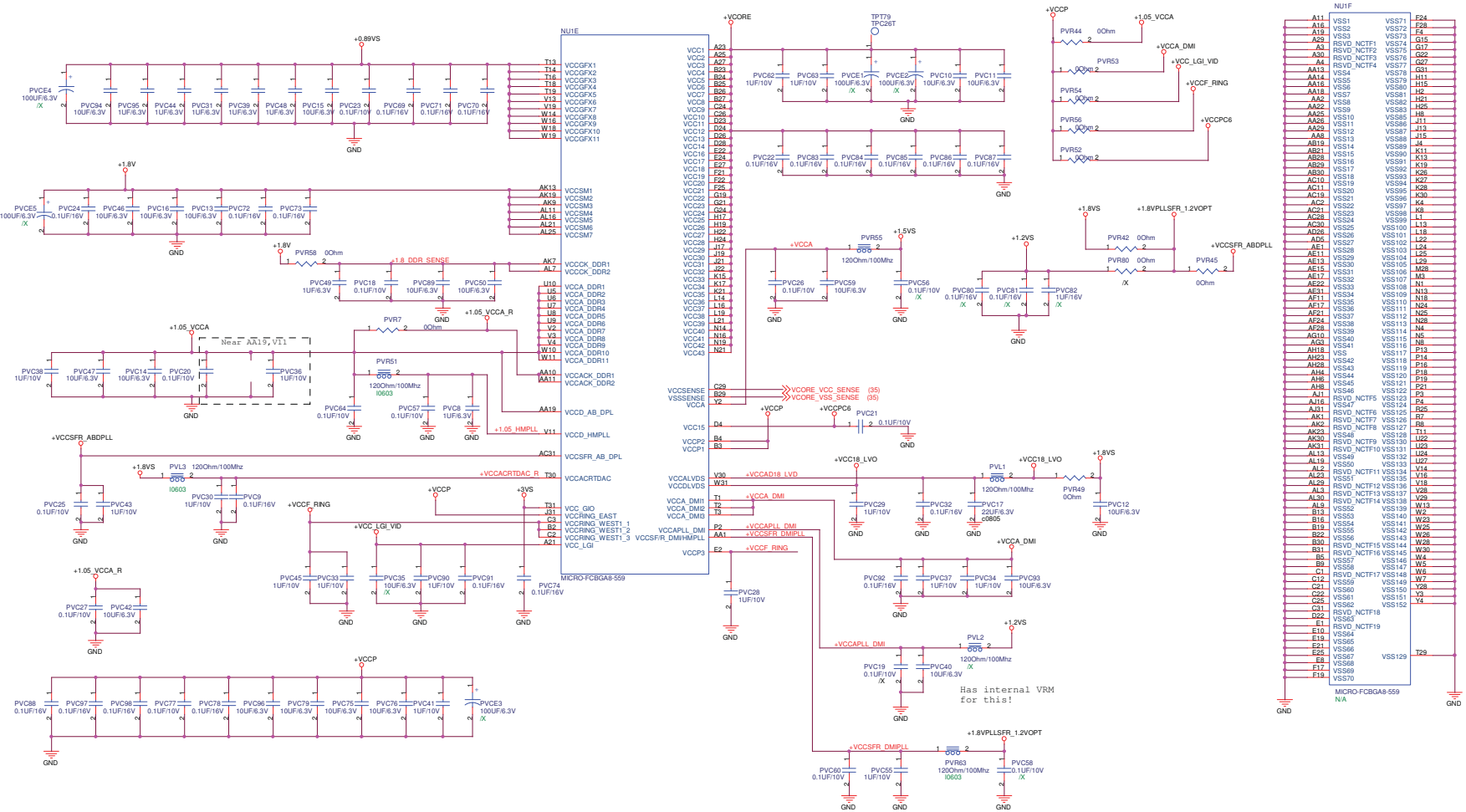
ASUSTek Computer INC.

Title : PineView_2

Engineer: C. A. Lai

Size	Project Name	Rev
A3	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 5 of 51



VCC = 3.5A
VCCA =0.08A
VCCGFX =1.38A
VCCALVDS , VCCDLVDS=0.06A
VCCA_DMI =0.48A
VCCSFR_DMIHMPLL =0.104A
VCCA_DDR and VCCACK_DDR =1.32A
VCCSM and VCCCK_DDR =2.27A
VCCRING_EAST , VCCRING_EAST_WEST , VCC_LGI , VCCD_AB_DPL , VCCD_HMPLL =0.33A
VCC_GIO =0.006A
VCCSFR_AB_DPL , VCCACRTDAC =0.154A

Current for PineView

<Core Design>

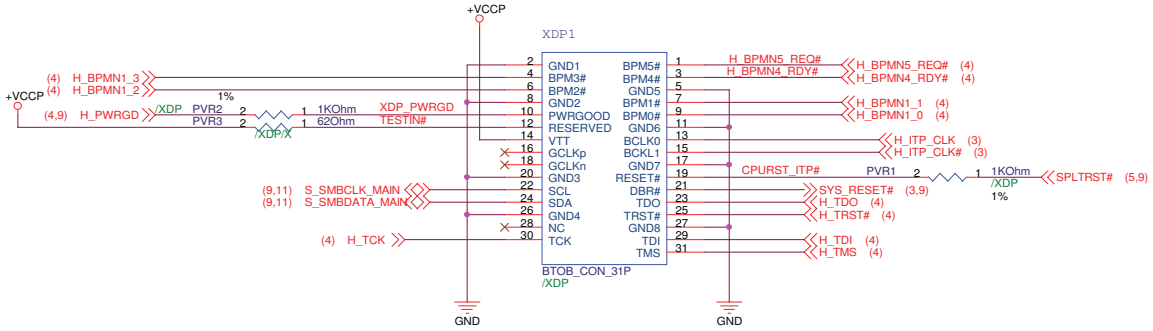
ASUSTek Computer INC.

Title : PineView_3

Engineer: C. A. Lai

Size	Project Name	Rev
A2	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 6 of 51



Change Device and PCB footprint of XDP1 to nomask footprint - nomask solution

新 Layout 機種請 XDP Connector 請畫 12G161300311 (w/ 2 through holes)。

<Core Design>

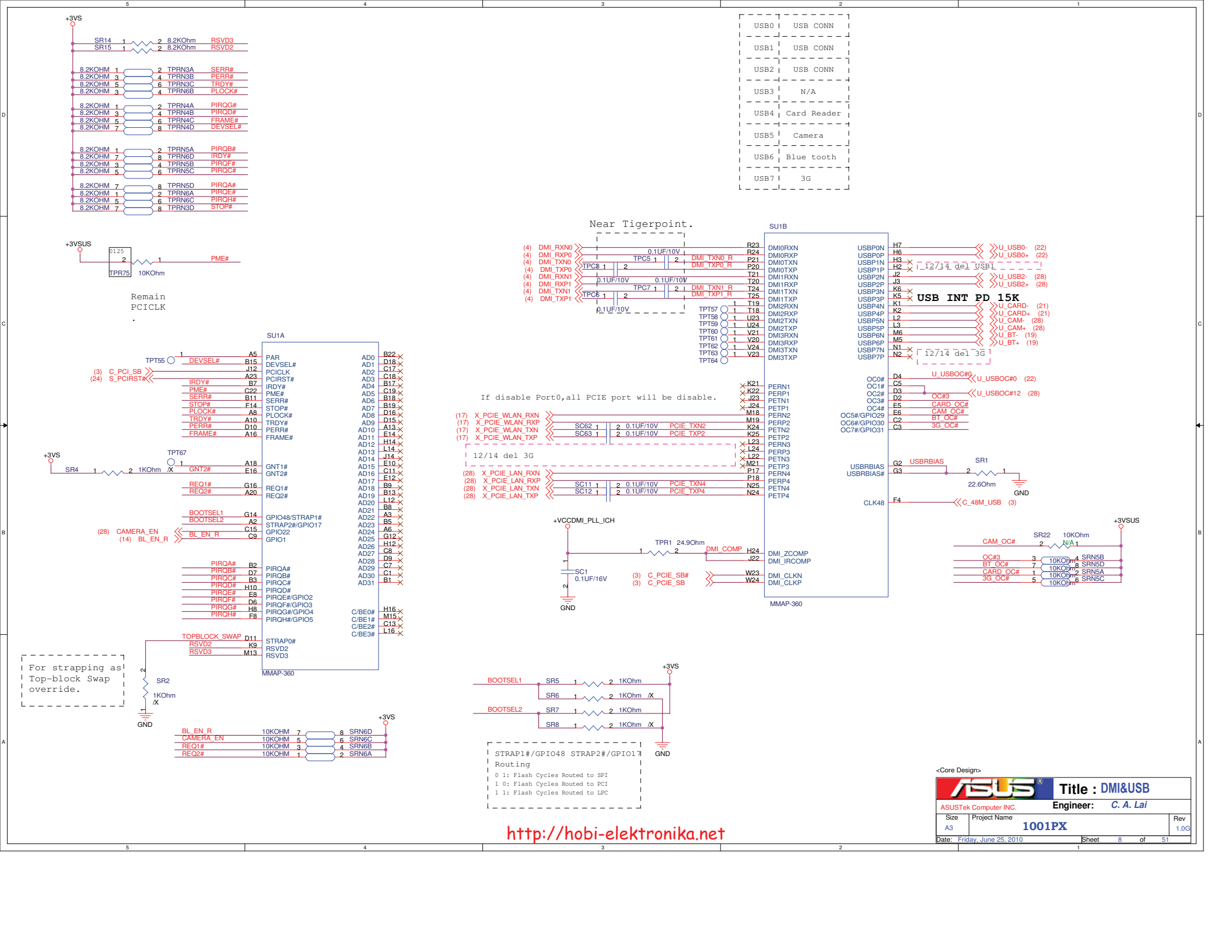
ASUSTek Computer INC.

Title : XDP

Engineer: C. A. Lai

Size	Project Name	Rev
A3	1001PX	1.0G

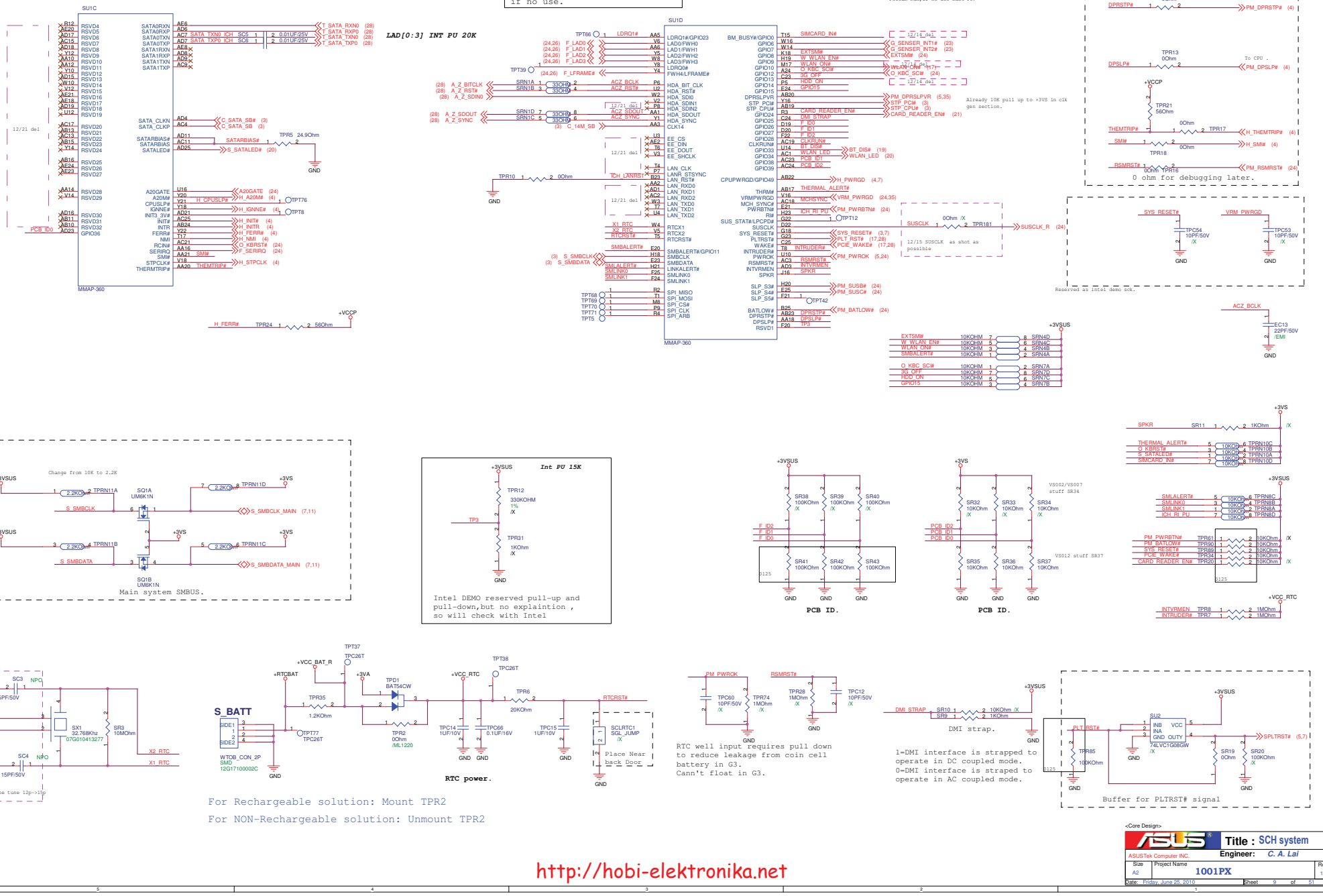
Date: Friday, June 25, 2010 Sheet 7 of 51


+3VS
SR14 1 2 8.2KOhm RSVD3
SR15 1 2 8.2KOhm RSVD2
8.2KOHM 1 2 TPRN3A SERR#
8.2KOHM 3 4 TPRN3B PERR#
8.2KOHM 5 6 TPRN3C TRDY#
8.2KOHM 3 4 TPRN6B PLOCK#
8.2KOHM 1 2 TPRN4A PIRQG#
8.2KOHM 3 4 TPRN4B PIRQD#
8.2KOHM 5 6 TPRN4C FRAME#
8.2KOHM 7 8 TPRN4D DEVSEL#
8.2KOHM 1 2 TPRN5A PIRQB#
8.2KOHM 7 8 TPRN6D IRDY#
8.2KOHM 3 4 TPRN5B PIRQF#
8.2KOHM 5 6 TPRN5C PIRQC#
8.2KOHM 7 8 TPRN5D PIRQA#
8.2KOHM 1 2 TPRN6A PIRQE#
8.2KOHM 5 6 TPRN6C PIRQH#
8.2KOHM 7 8 TPRN3D STOP#
USB0 USB CONN
USB1 USB CONN
USB2 USB CONN
USB3 N/A
USB4 Card Reader
USB5 Camera
USB6 Blue tooth
USB7 3G
+3VSUS
0125
TPR75 10KOhm
PME#
Remain
PCICLK
.
Near Tigerpoint.
SU1B
(4) DMI_RXN0
(4) DMI_RXP0
(4) DMI_TXN0
(4) DMI_TXP0
(4) DMI_RXN1
(4) DMI_RXP1
(4) DMI_TXN1
(4) DMI_TXP1
0.1UF/10V
TPC5
TPC8
TPC7
TPC6
DMI_TXN0_R
DMI_TXP0_R
DMI_TXN1_R
DMI_TXP1_R
TPT57
TPT58
TPT59
TPT60
TPT61
TPT62
TPT63
TPT64
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
12/14 del USB1
12/14 del 3G
USB INT PD 15K
U_USB0- (22)
U_USB0+ (22)
U_USB2- (28)
U_USB2+ (28)
U_CARD- (21)
U_CARD+ (21)
U_CAM- (28)
U_CAM+ (28)
U_BT- (19)
U_BT+ (19)
SU1A
TPT55
DEVSEL#
(3) C_PCI_SB
(24) S_PCIRST#
IRDY#
PME#
SERR#
STOP#
PLOCK#
TRDY#
PERR#
FRAME#
PAR
PCICLK
PCIRST#
GNT1#
GNT2#
REQ1#
REQ2#
GPIO48/STRAP1#
STRAP2#/GPIO17
GPIO22
GPIO1
BOOTSEL1
BOOTSEL2
(28) CAMERA_EN
(14) BL_EN_R
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
TOPBLOCK_SWAP
RSVD2
RSVD3
STRAP0#
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
C/BE0#
C/BE1#
C/BE2#
C/BE3#
MMAP-360
If disable Port0,all PCIE port will be disable.
(17) X_PCIE_WLAN_RXN
(17) X_PCIE_WLAN_RXP
(17) X_PCIE_WLAN_TXN
(17) X_PCIE_WLAN_TXP
SC62 0.1UF/10V PCIE_TXN2
SC63 0.1UF/10V PCIE_TXP2
12/14 del 3G
(28) X_PCIE_LAN_RXN
(28) X_PCIE_LAN_RXP
(28) X_PCIE_LAN_TXN
(28) X_PCIE_LAN_TXP
SC11 0.1UF/10V PCIE_TXN4
SC12 0.1UF/10V PCIE_TXP4
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
OC0#
OC1#
OC2#
OC3#
OC4#
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
U_USBOC#0
U_USBOC#0 (22)
OC#3
U_USBOC#12 (28)
CARD_OC#
CAM_OC#
BT_OC#
3G_OC#
USBRBIAS
USBRBIAS#
SR1
22.6Ohm
GND
CLK48
C_48M_USB (3)
+VCCDMI_PLL_ICH
TPR1 24.9Ohm
DMI_COMP
SC1 0.1UF/16V
(3) C_PCIE_SB#
(3) C_PCIE_SB
DMI_ZCOMP
DMI_IRCOMP
DMI_CLKN
DMI_CLKP
MMAP-360
+3VS
SR4 1 2 1KOhm /X
TPT67
GNT2#
REQ1#
REQ2#
+3VSUS
SR22 10KOhm N/A
CAM_OC#
OC#3
BT_OC#
CARD_OC#
3G_OC#
10KOhm SRN5B
10KOhm SRN5D
10KOhm SRN5A
10KOhm SRN5C
For strapping as
Top-block Swap
override.
SR2
1KOhm
/X
GND
BL_EN_R
CAMERA_EN
REQ1#
REQ2#
10KOHM SRN6D
10KOHM SRN6C
10KOHM SRN6B
10KOHM SRN6A
+3VS
BOOTSEL1
BOOTSEL2
SR5 1KOhm
SR6 1KOhm /X
SR7 1KOhm
SR8 1KOhm /X
GND
STRAP1#/GPIO48 STRAP2#/GPIO17
Routing
0 1: Flash Cycles Routed to SPI
1 0: Flash Cycles Routed to PCI
1 1: Flash Cycles Routed to LPC
http://hobi-elektronika.net
<Core Design>
Title : DMI&USB
ASUSTek Computer INC.
Engineer: C. A. Lai
Size A3
Project Name 1001PX
Rev 1.0G
Date: Friday, June 25, 2010
Sheet 8 of 51

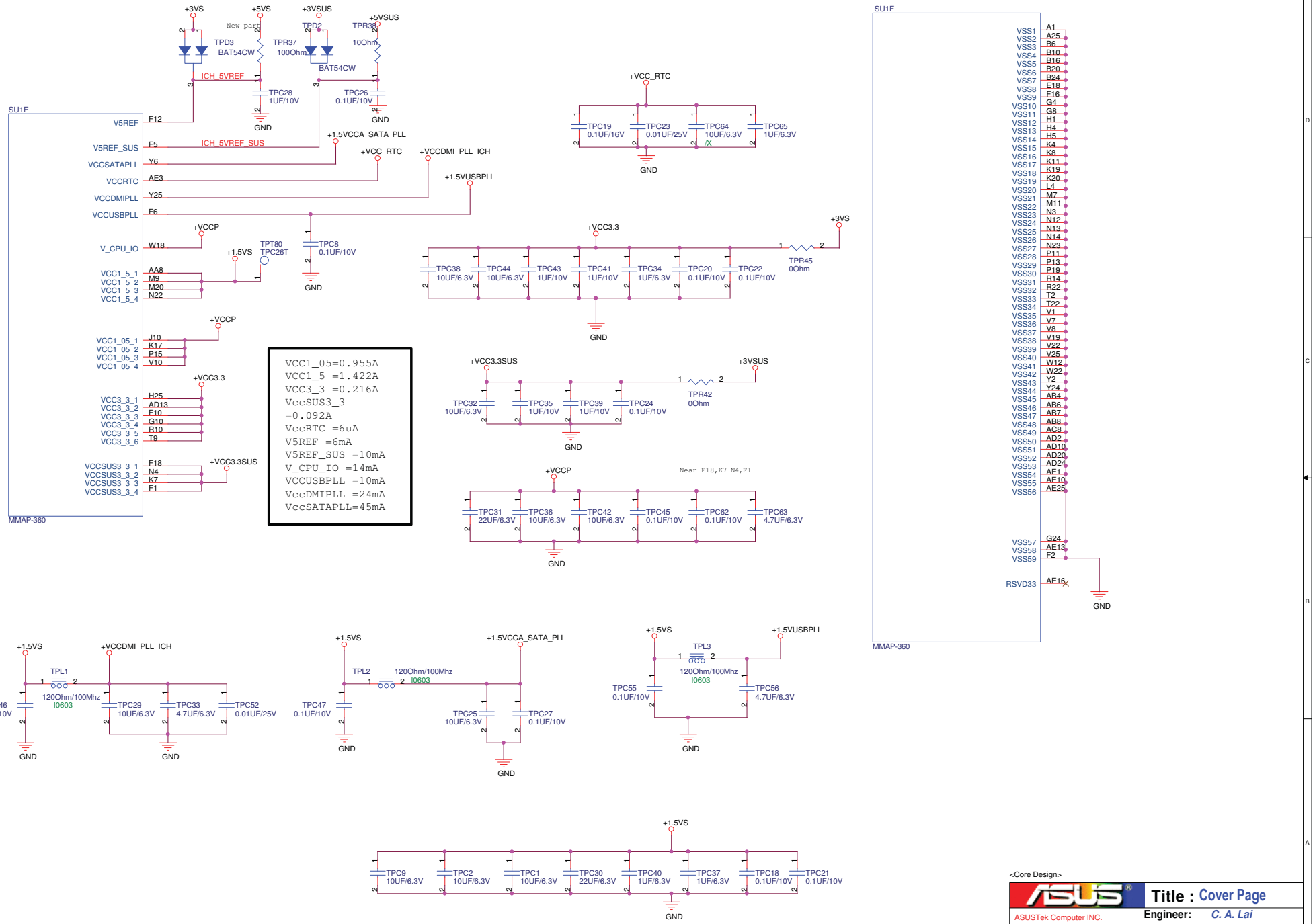
CLK 14MHZ has a 22ohm resistor near clk Gen.

LDRQ0/1 LPC DMA/master request,ICH7M has internal PU, but we need TPT datasheet

SATA RX,TX all need AC couple and place near Connector side for signal quality.And Traces to them should match length. ICH7M need pull down RX, if no use.



<Core Design>
ASUSTek Computer INC.
Title : SCH system
Engineer: C. A. Lai
Size A2 | Project Name 1001PX | Rev 1.0G
Date: Friday, June 25, 2010 | Sheet 9 of 51



<Core Design>

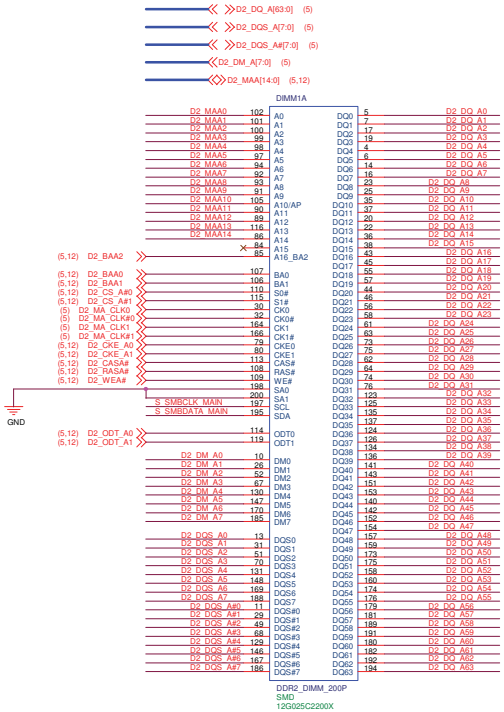
Title : Cover Page

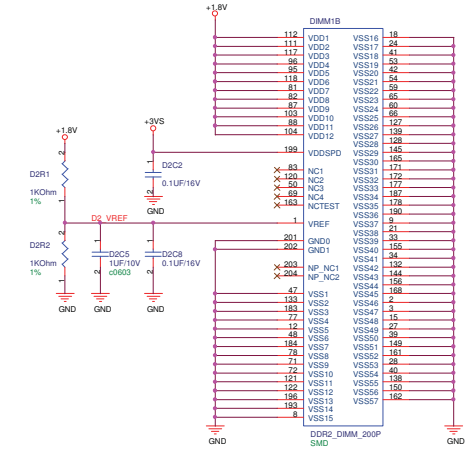
ASUSTek Computer INC.

Engineer: C. A. Lai

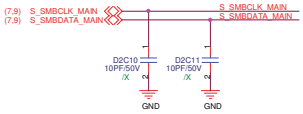
Size	Project Name	Rev
A3	1001PX	1.0G

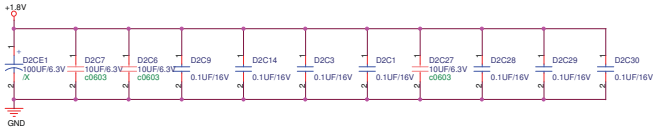
Date: Friday, June 25, 2010 Sheet 10 of 51





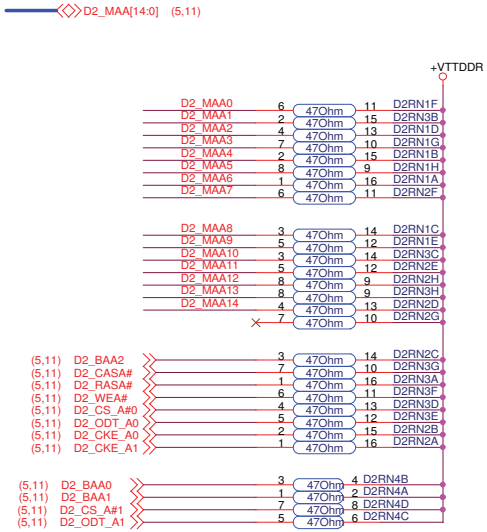
"新 Layout 機種請考量2nd source / 12G025C2200X 的PCB footprint ,以避免2nd DIMM 與週邊零件產生干涉- 2nd source PCB footprint 與main source size 在DIMM寬度有所不同"

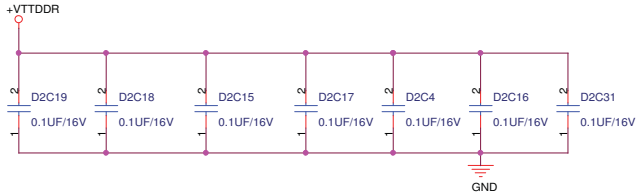


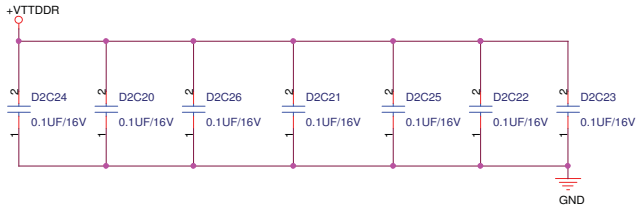


<Core Design>

ASUSTek Computer INC.	Title : DDR2-SO-DIMM	
	Engineer: C. A. Lai	
Size: A2	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 11 of 51	







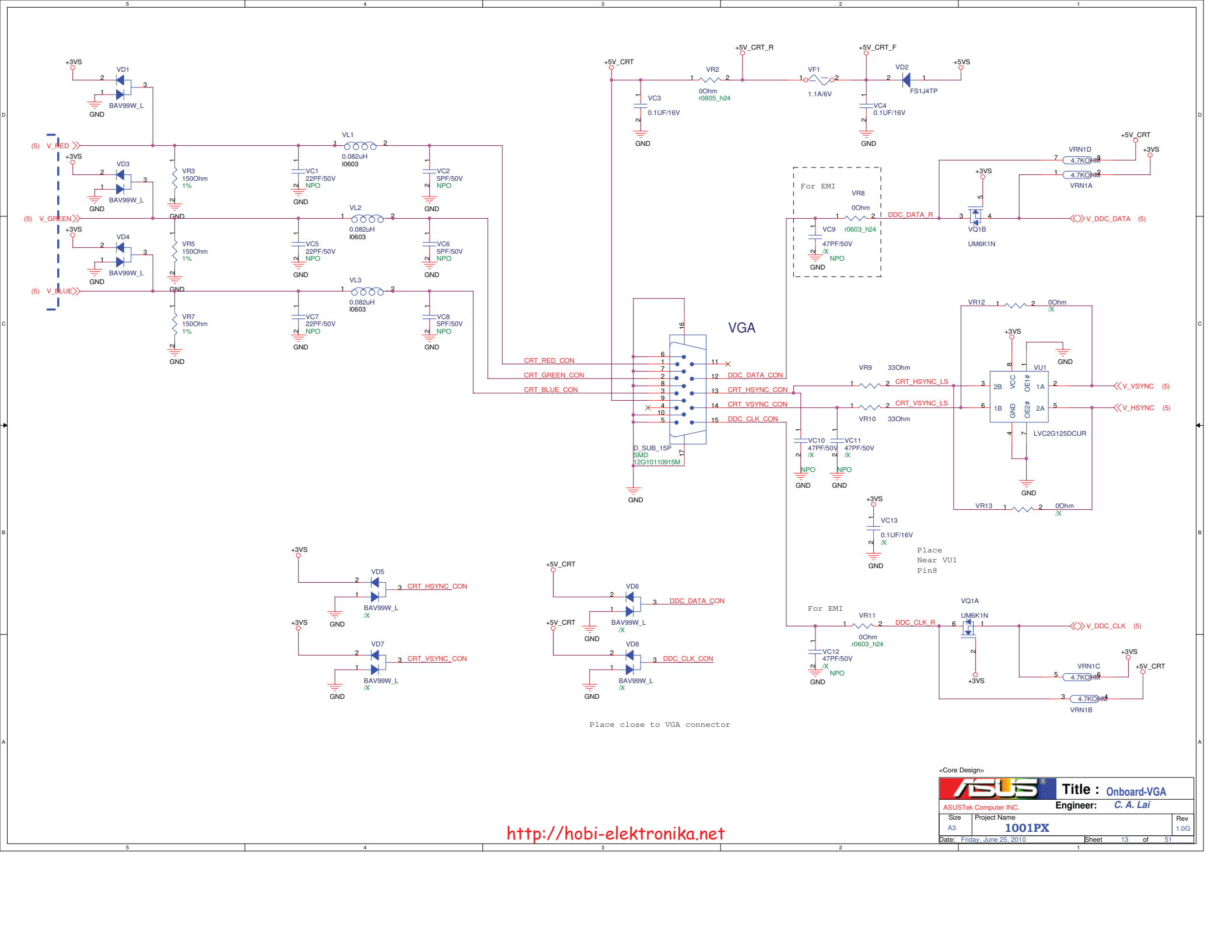
<Core Design>

Title : DDR2-Termination

ASUSTek Computer INC. Engineer: C. A. Lai

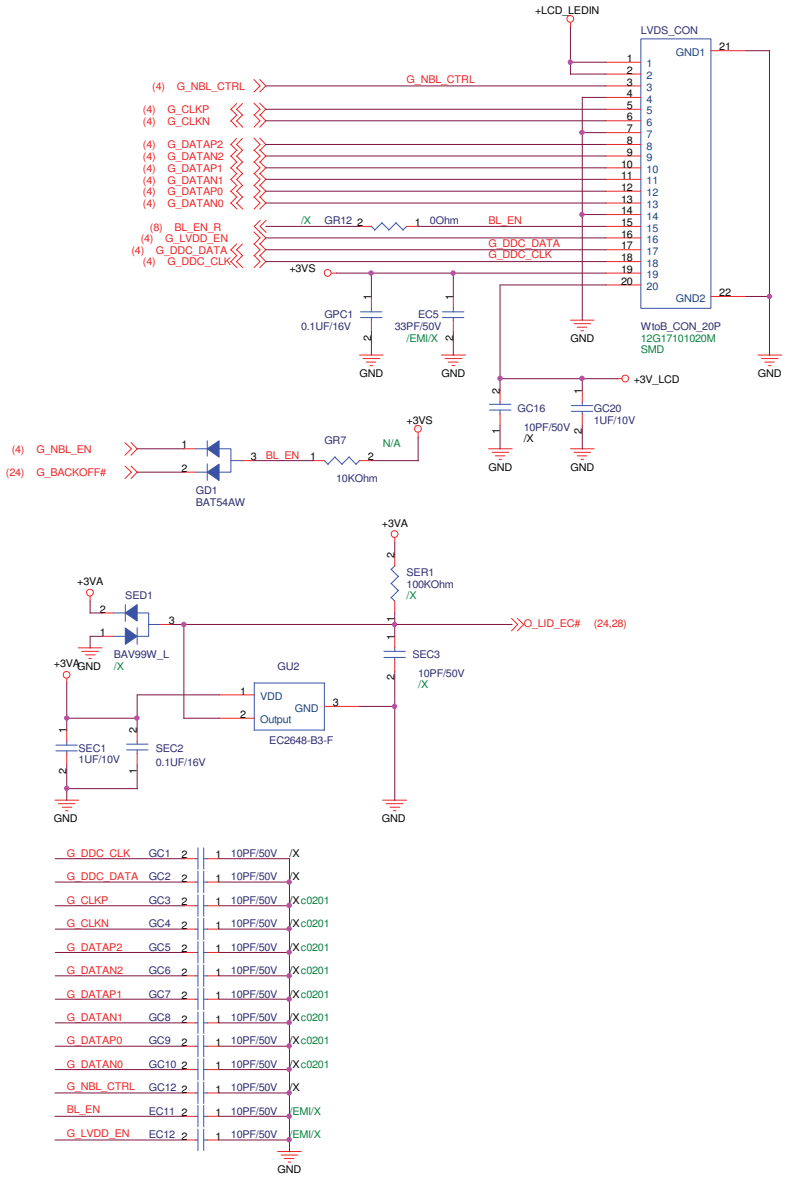
Size	Project Name	Rev
A3	1001PX	1.0G

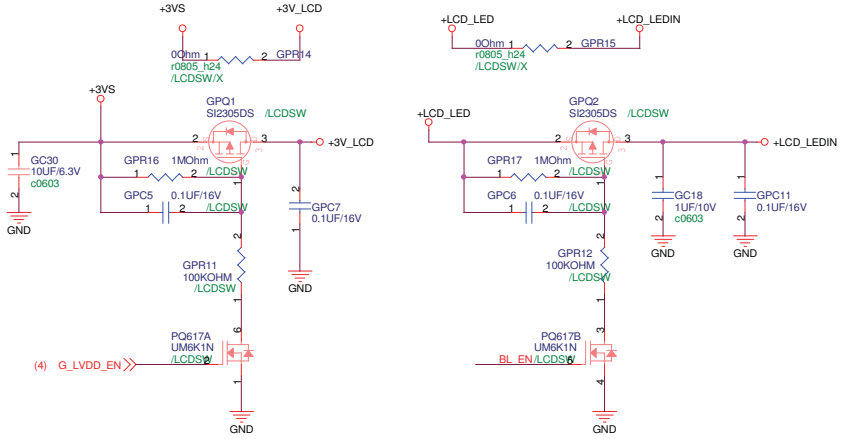
Date: Friday, June 25, 2010 Sheet 12 of 51



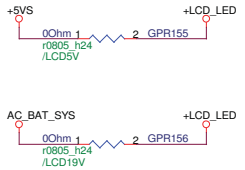
<Core Design>

ASUSTek Computer INC.	Title : Onboard-VGA	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 13 of 51	





	mount	unmount
Panel with SW	/LCDSW/X	/LCDSW
Panel without SW	/LCDSW	/LCDSW/X
Panel backlight 5V	/LCD5V	/LCD19V
Panel backlight 19V	/LCD19V	/LCD5V



<Core Design>

Title : LVDS Conn_LID

ASUSTek Computer INC.

Engineer: C. A. Lai

Size	Project Name	Rev
Custom	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 14 of 51

<Core Design>

ASUSTek Computer INC.	Title : Light_Sensor	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 15 of 51	

<Core Design>

Title : LAN_AR8132

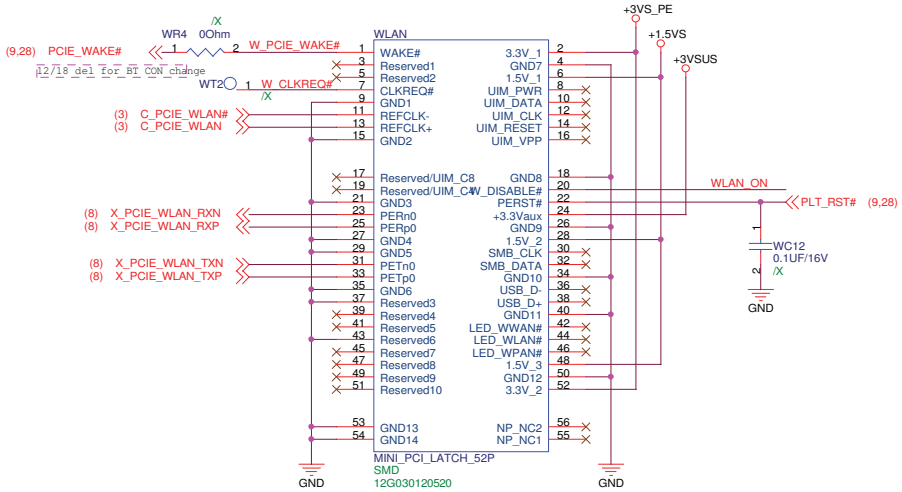
ASUSTek Computer INC.

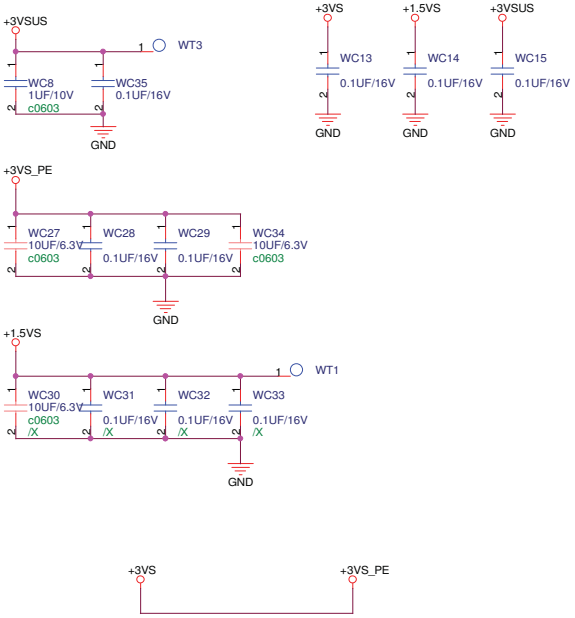
Engineer: C. A. Lai

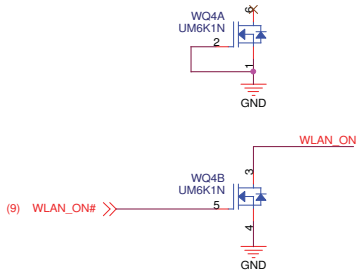
Size	Project Name	Rev
A3	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 16 of 51

WIFI use PCIE 1.1 Spec
+3VS = 1.0A peak / 0.75A Normal
+1.5VS = 0.5A peak / 0.375A Normal
+3VSUS = 0.375A peak / 0.25A Normal







<Core Design>

ASUSTek Computer INC.	Title : WLAN	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 17 of 51	

<Core Design>

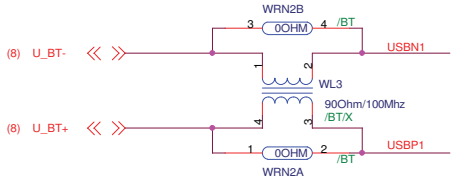
Title : 3G CON

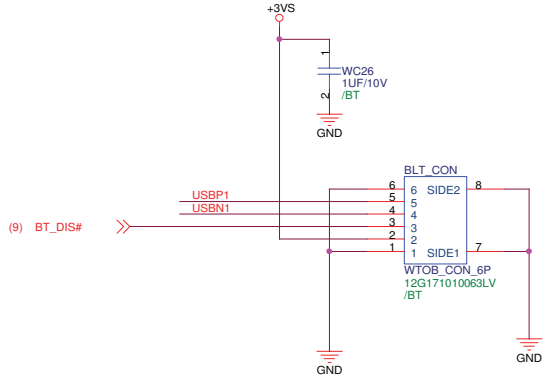
ASUSTek Computer INC.

Engineer: C. A. Lai

Size	Project Name	Rev
A4	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 18 of 51





12/18 12G170030102 change to
12G171010063LV

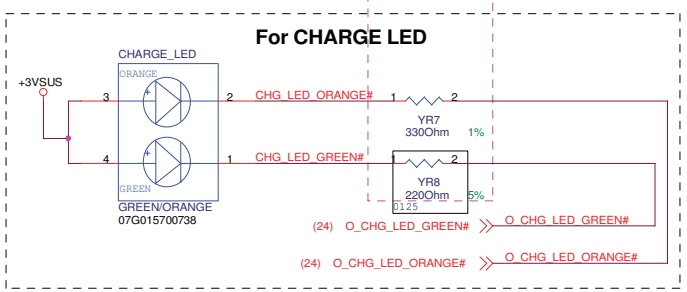
<Core Design>

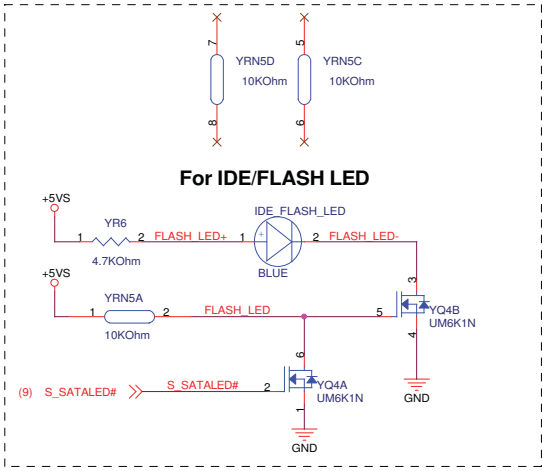
ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 19 of 51	

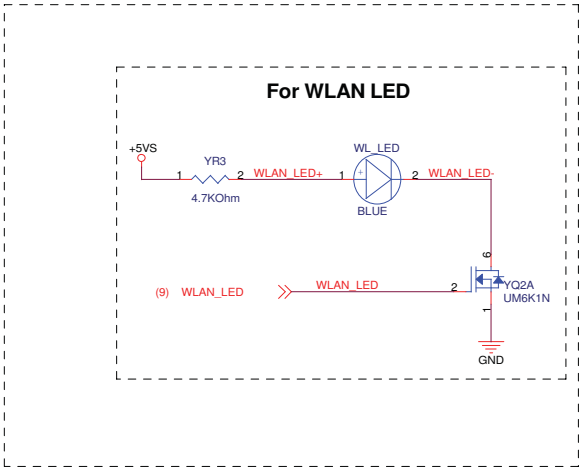
0.1A Beta

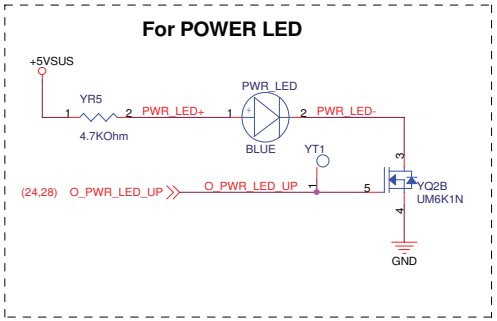
Mode / Scenario	Adapater Mode	Battery Mode
Battery power is between 100%～40%	Orange ON	Green ON
Battery power is between 40%～10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	Green Blinking Quickly
S3/S5 Mode	Scenario the same as above	OFF

1/13 solve 330K->330



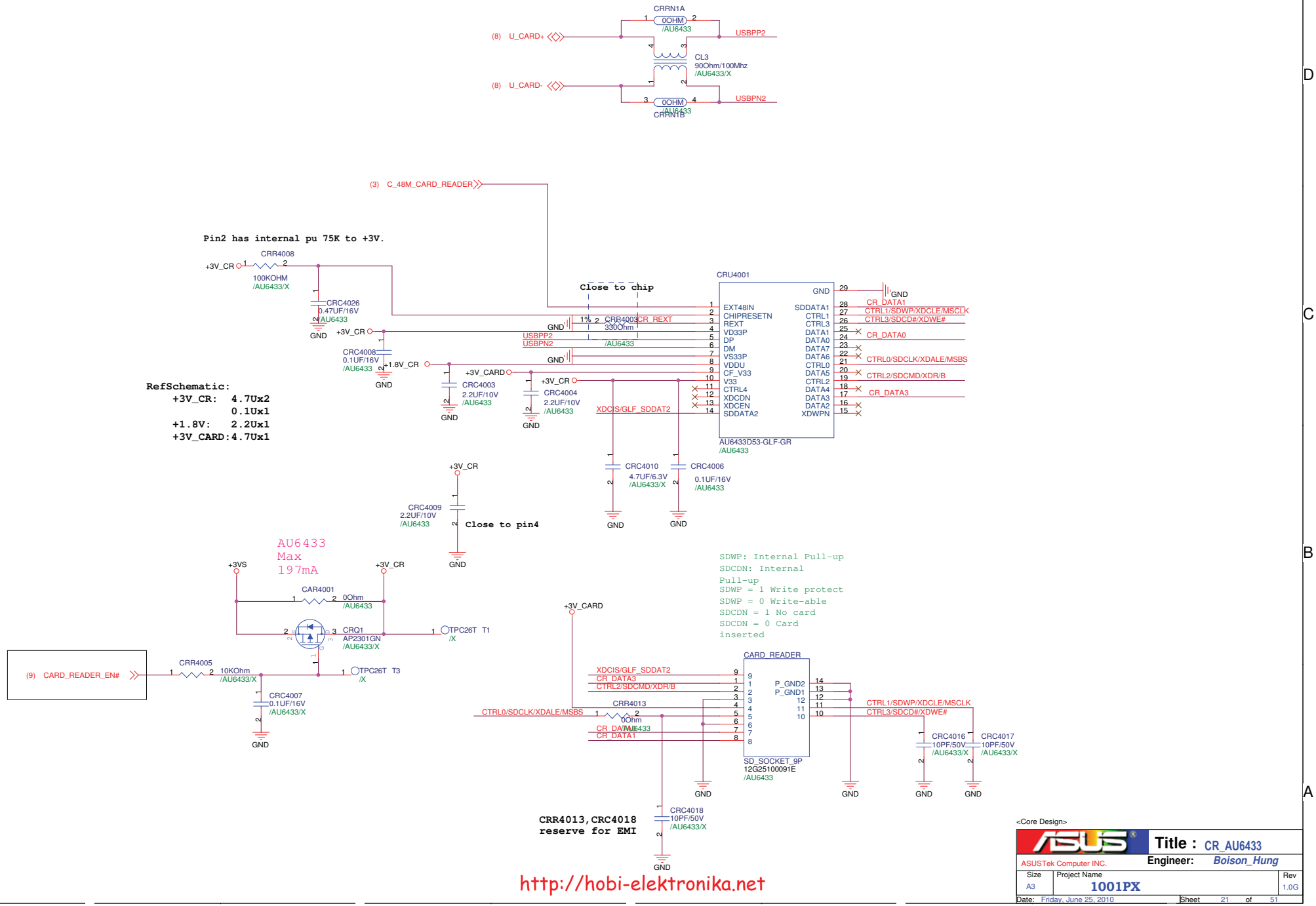


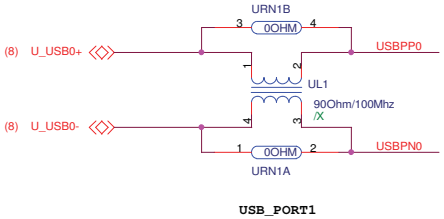




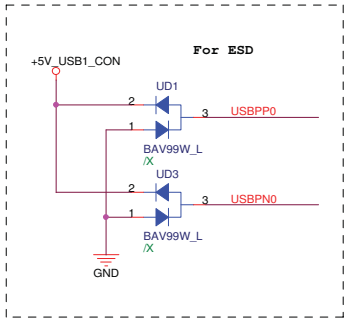
<Core Design>

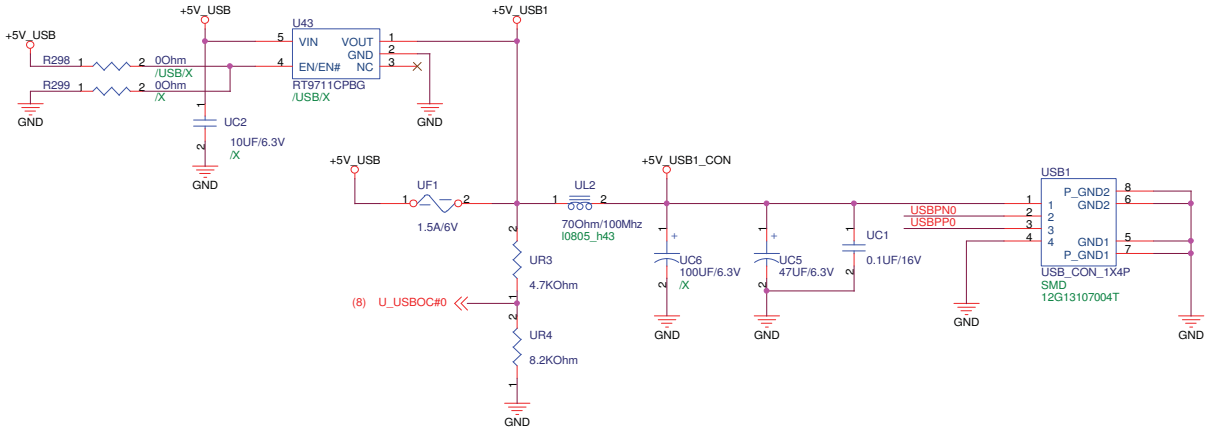
ASUSTek Computer INC.	Title : LED	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 20 of 51	


CRRN1A
0OHM
/AU6433
(8) U_CARD+
USBPP2
CL3
90Ohm/100Mhz
/AU6433/X
(8) U_CARD-
USBPN2
CRRN1B
(3) C_48M_CARD_READER
Pin2 has internal pu 75K to +3V.
CRR4008
+3V_CR
100KOHM
/AU6433/X
CRC4026
0.47UF/16V
/AU6433
GND
Close to chip
CRR4003
330Ohm
CR_REXT
CRU4001
EXT48IN
CHIPRESETN
REXT
VD33P
DP
DM
VS33P
VDDU
CF_V33
V33
CTRL4
XDCDN
XDCEN
SDDATA2
SDDATA1
CTRL1
CTRL3
DATA1
DATA0
DATA7
DATA6
CTRL0
DATA5
CTRL2
DATA4
DATA3
DATA2
XDWPN
CR_DATA1
CTRL1/SDWP/XDCLE/MSCLK
CTRL3/SDCD#/XDWE#
CR_DATA0
CTRL0/SDCLK/XDALE/MSBS
CTRL2/SDCMD/XDR/B
CR_DATA3
AU6433D53-GLF-GR
/AU6433
CRC4008
0.1UF/16V
/AU6433
+1.8V_CR
CRC4003
2.2UF/10V
/AU6433
+3V_CARD
CRC4004
2.2UF/10V
/AU6433
XDCIS/GLF_SDDAT2
CRC4010
4.7UF/6.3V
/AU6433/X
CRC4006
0.1UF/16V
/AU6433
RefSchematic:
+3V_CR: 4.7Ux2
0.1Ux1
+1.8V: 2.2Ux1
+3V_CARD: 4.7Ux1
CRC4009
2.2UF/10V
/AU6433
Close to pin4
AU6433
Max
197mA
+3VS
CAR4001
0Ohm
/AU6433
CRQ1
AP2301GN
/AU6433/X
TPC26T T1
/X
(9) CARD_READER_EN#
CRR4005
10KOhm
/AU6433/X
TPC26T T3
/X
CRC4007
0.1UF/16V
/AU6433/X
SDWP: Internal Pull-up
SDCDN: Internal
Pull-up
SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card
inserted
CARD_READER
P_GND2
P_GND1
CRR4013
0Ohm
/AU6433
SD_SOCKET_9P
12G25100091E
/AU6433
CRC4016
10PF/50V
/AU6433/X
CRC4017
10PF/50V
/AU6433/X
CRR4013,CRC4018
reserve for EMI
CRC4018
10PF/50V
/AU6433/X
http://hobi-elektronika.net
<Core Design>
Title : CR_AU6433
ASUSTek Computer INC.
Engineer: Boison_Hung
Size A3
Project Name 1001PX
Rev 1.0G
Date: Friday, June 25, 2010
Sheet 21 of 51



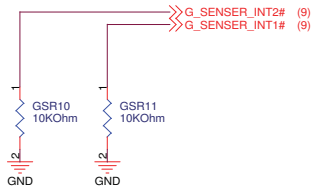
USB_PORT1





<Core Design>

ASUSTek Computer INC.	Title : USB Port1	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 22 of 51	



<Core Design>

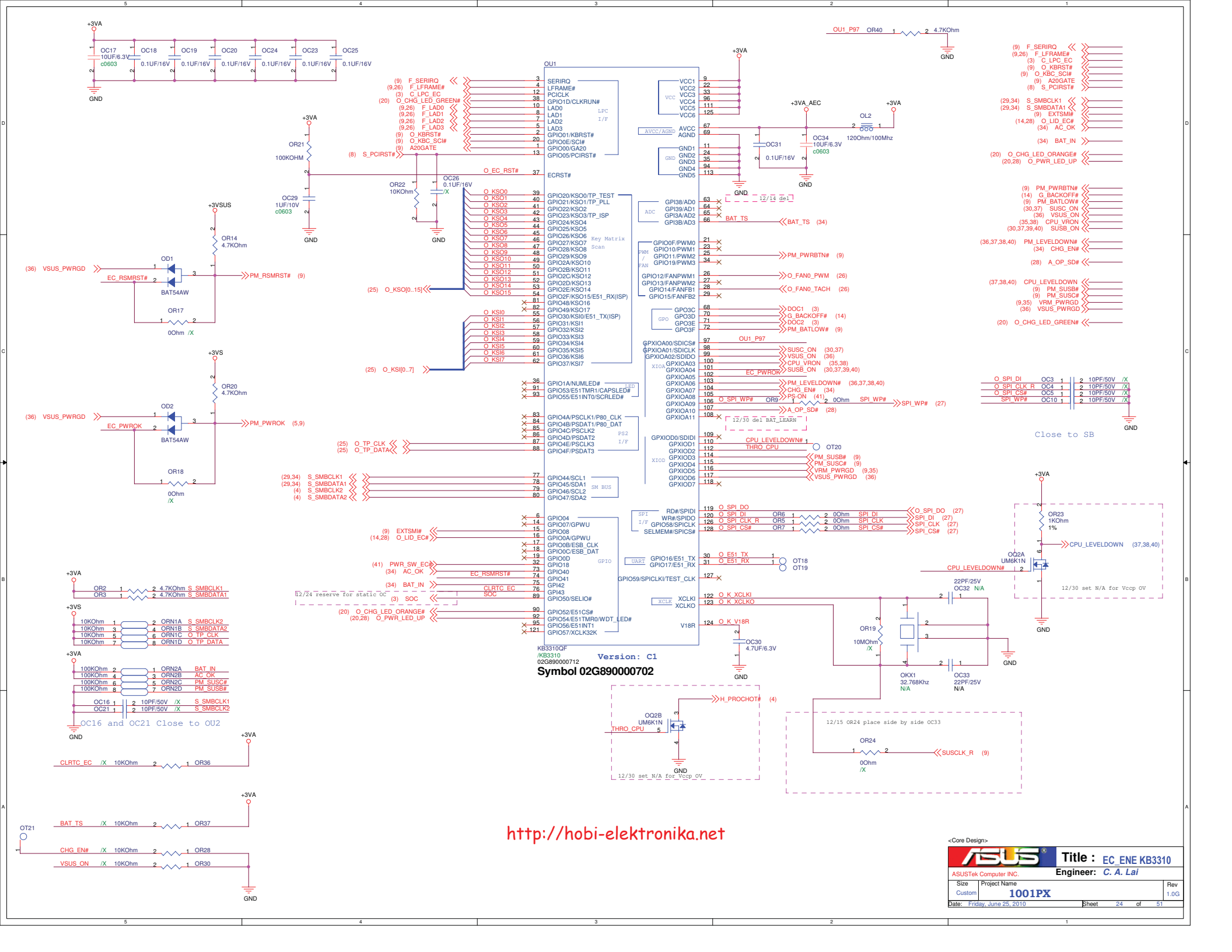
ASUSTek Computer INC.

Title : G_Senser

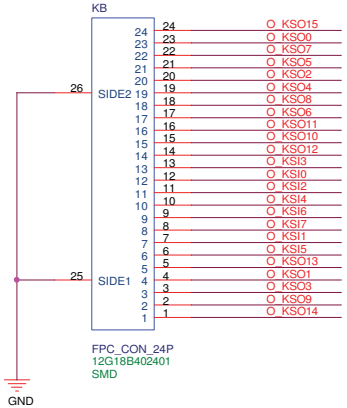
Engineer: C. A. Lai

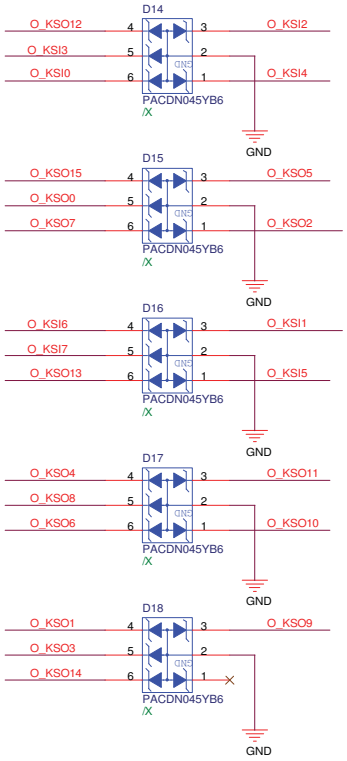
Size	Project Name	Rev
A3	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 23 of 51


OU1
KB3310QF
/KB3310
02G890000712
Version: C1
Symbol 02G890000702
http://hobi-elektronika.net
Close to SB
OC16 and OC21 Close to OU2
12/30 set N/A for Vccp OV
12/15 OR24 place side by side OC33
12/24 reserve for static OC
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: C. A. Lai
Project Name 1001PX
Size Custom
Rev 1.0G
Date: Friday, June 25, 2010
Sheet 24 of 51

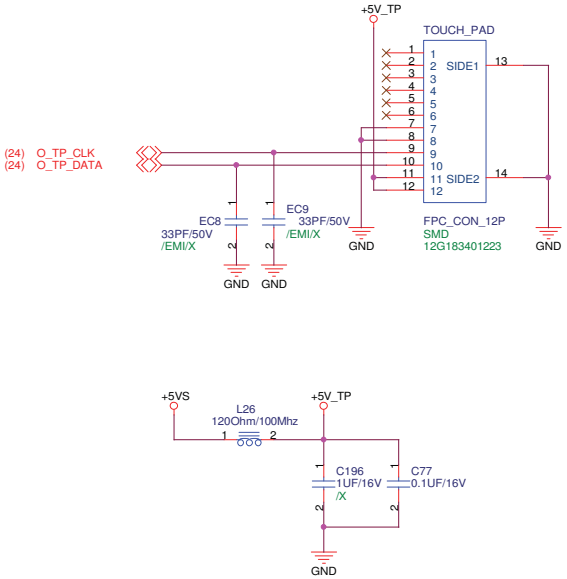
For Keyboard Connector





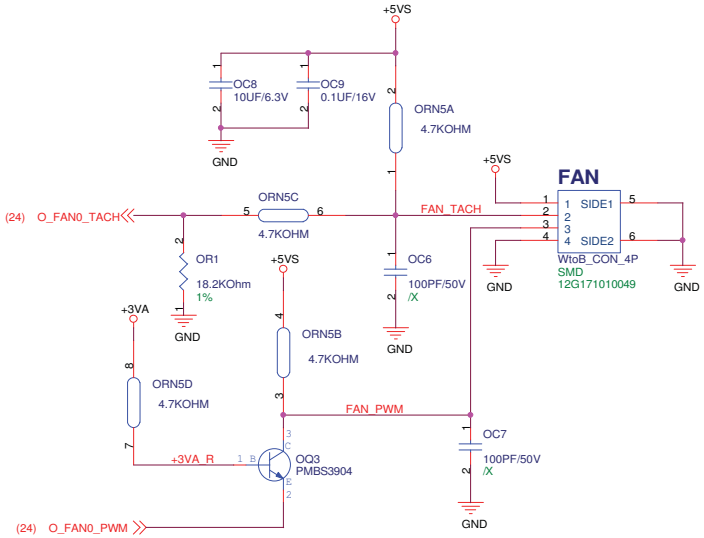
(24) O_KSO[0..15]
(24) O_KSI[0..7]

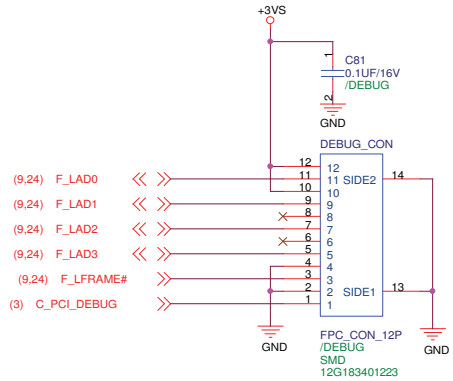
For Touch-Pad



<Core Design>

ASUSTek Computer INC.	Title : KB_TP	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 25 of 51	





<Core Design>

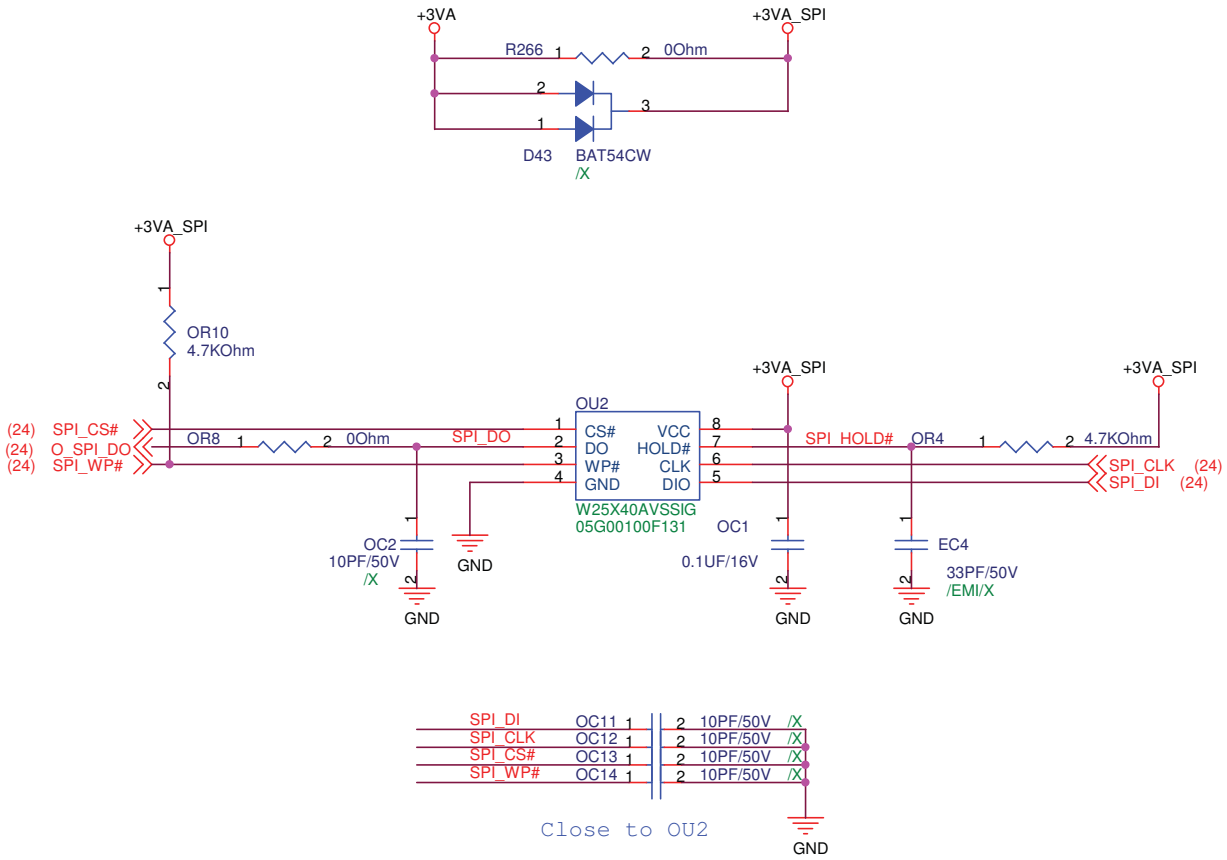
ASUSTek Computer INC.

Title : Fan_Debug

Engineer: C. A. Lai

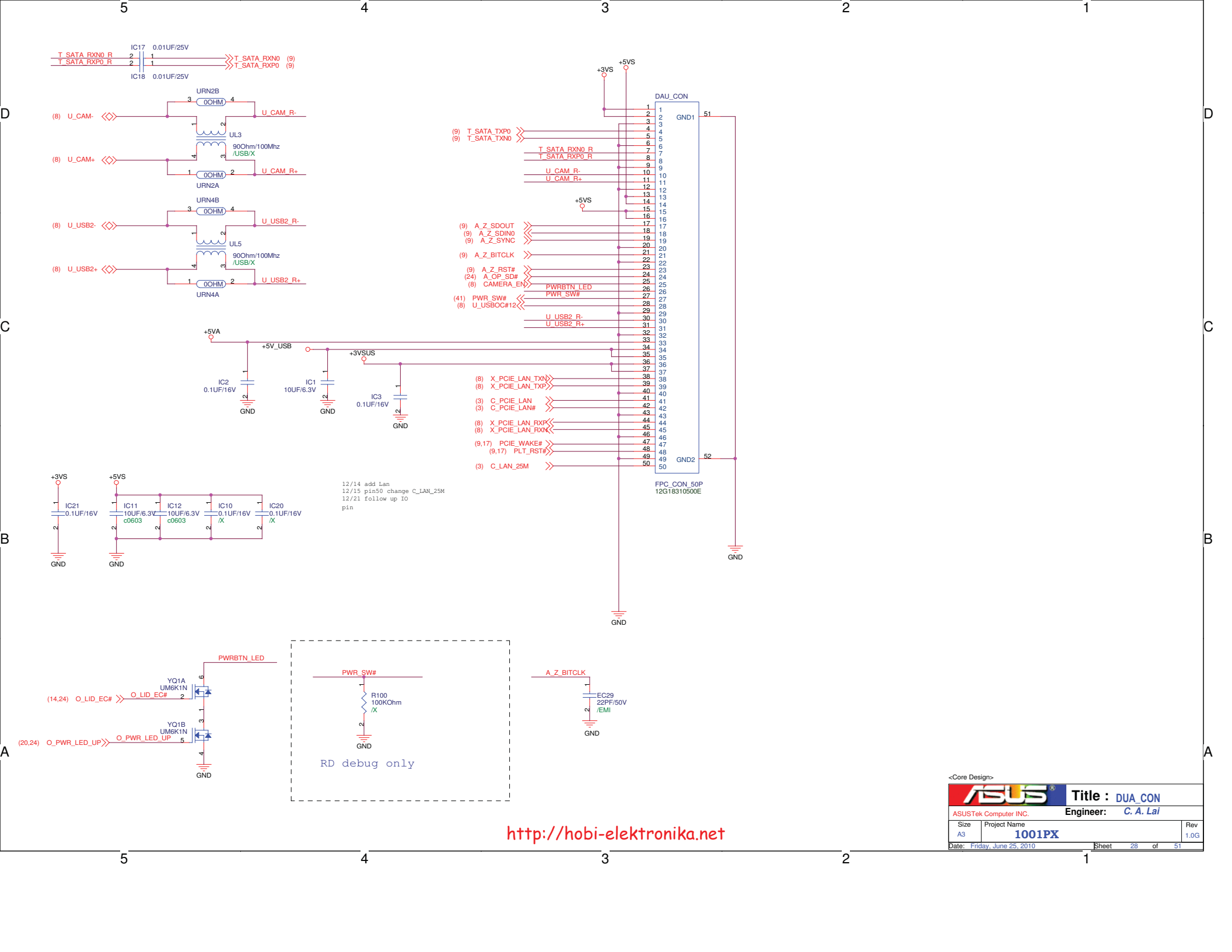
Size	Project Name	Rev
A3	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 26 of 51



<Core Design>

ASUSTek Computer INC.	Title : SPI_ROM	
	Engineer: C. A. Lai	
Size: A4	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 27 of 51	



http://hobi-elektronika.net

<Core Design>

ASUSTek Computer INC.

Title : DUA_CON

Engineer: C. A. Lai

Size	Project Name	Rev
A3	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 28 of 51

0.1B Beta

BAT_IN# (34)
S_SMBCLK1 (24,34)
S_SMBDATA1 (24,34)

DC IN

DC_JACK_IN
DC_PWR
P_GND1
P_GND2
P_GND3
P_GND4 NP_NC
DC_POWER_JACK_3P
12G14501103N
SMD
1/25 rollback
12G14501103N
DCIN_GND
BT1
BT2
BT3
BT4
BT5
BT6
BT7
BT8
BL4 80Ohm/100Mhz
BL2 80Ohm/100Mhz
BL1 80Ohm/100Mhz
BL3 80Ohm/100Mhz
BC1 0.1UF/25V c0603
BD1 P4SMAJ20A
BC2 10UF/25V c1210_rd9
BC3 1UF/25V c0805_h57
BC5 1UF/25V c0603 /X
A/D_DOCK_IN
BC4 0.1UF/25V c0603
GND

1/18 change to
09G012080007

BAT IN

BATT_CON
BAT
TPC26T T136 /X
TPC26T T137 /X
TPC26T T138 /X
TPC26T T139 /X
P_GND1
P_GND2
BATT_CON_9P
12G20001092U
SMD
change from DIP to SMD
R1 0Ohm /X
B_SMB1_CLK
B_SMB1_DATA
B_BAT_IN#
C95 0.1UF/25V c0603
L53 120Ohm/100Mhz
L54 120Ohm/100Mhz
L31 120Ohm/100Mhz
S_SMBCLK1 (24,34)
S_SMBDATA1 (24,34)
BAT_IN# (34)
TPT78
TPC26T
C91 100PF/50V
C139 100PF/50V
C140 100PF/50V
D23 V0402MHS03 /BAT/X
D22 V0402MHS03 /BAT/X
D24 V0402MHS03 /BAT/X
GND

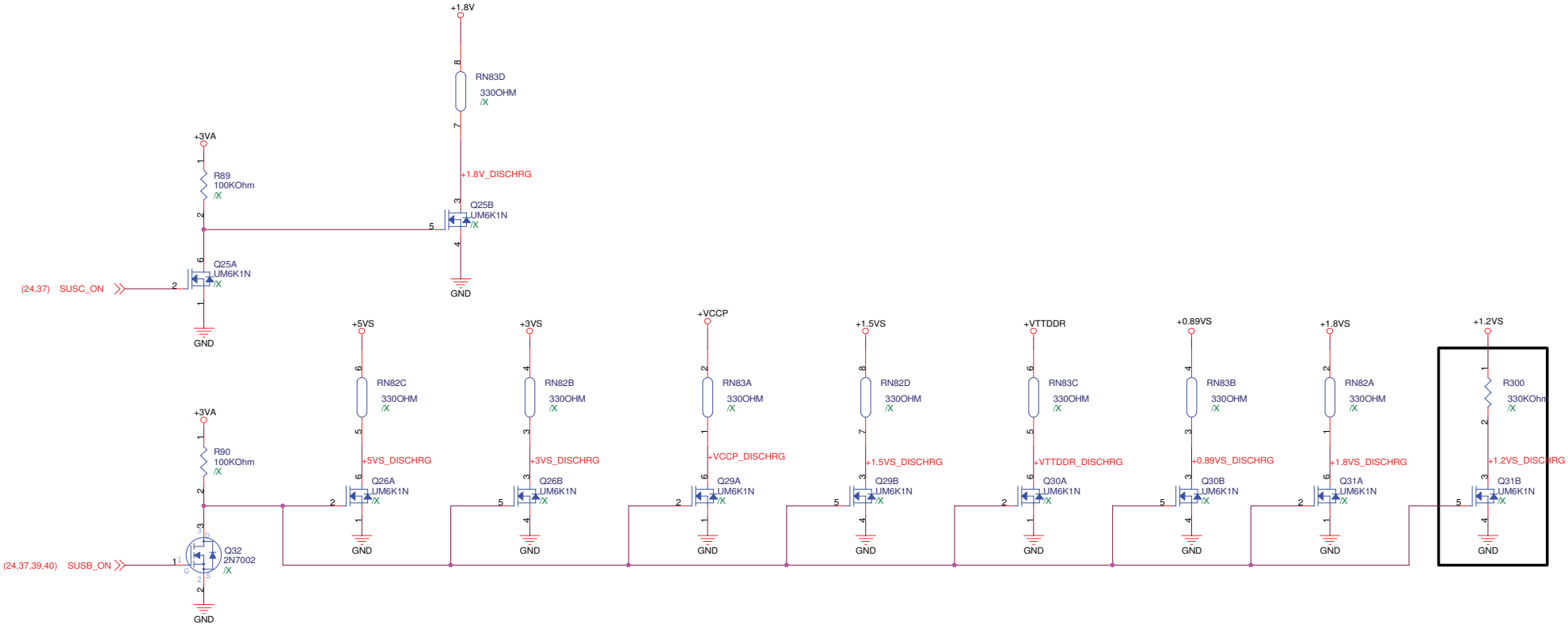
<Core Design>

ASUSTek Computer INC.

Title : PWR Jack
Engineer: C. A. Lai

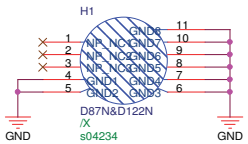
Size	Project Name	Rev
A3	1001PX	1.0G

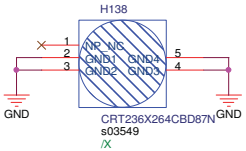
Date: Friday, June 25, 2010 Sheet 29 of 51

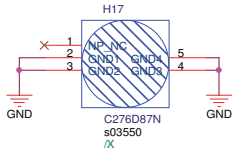


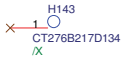
<Core Design>

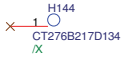
ASUSTek Computer INC.	Title : Discharge	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 30 of 51	

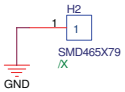


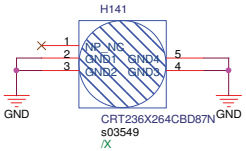


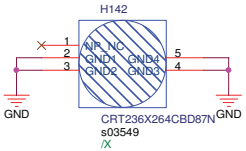






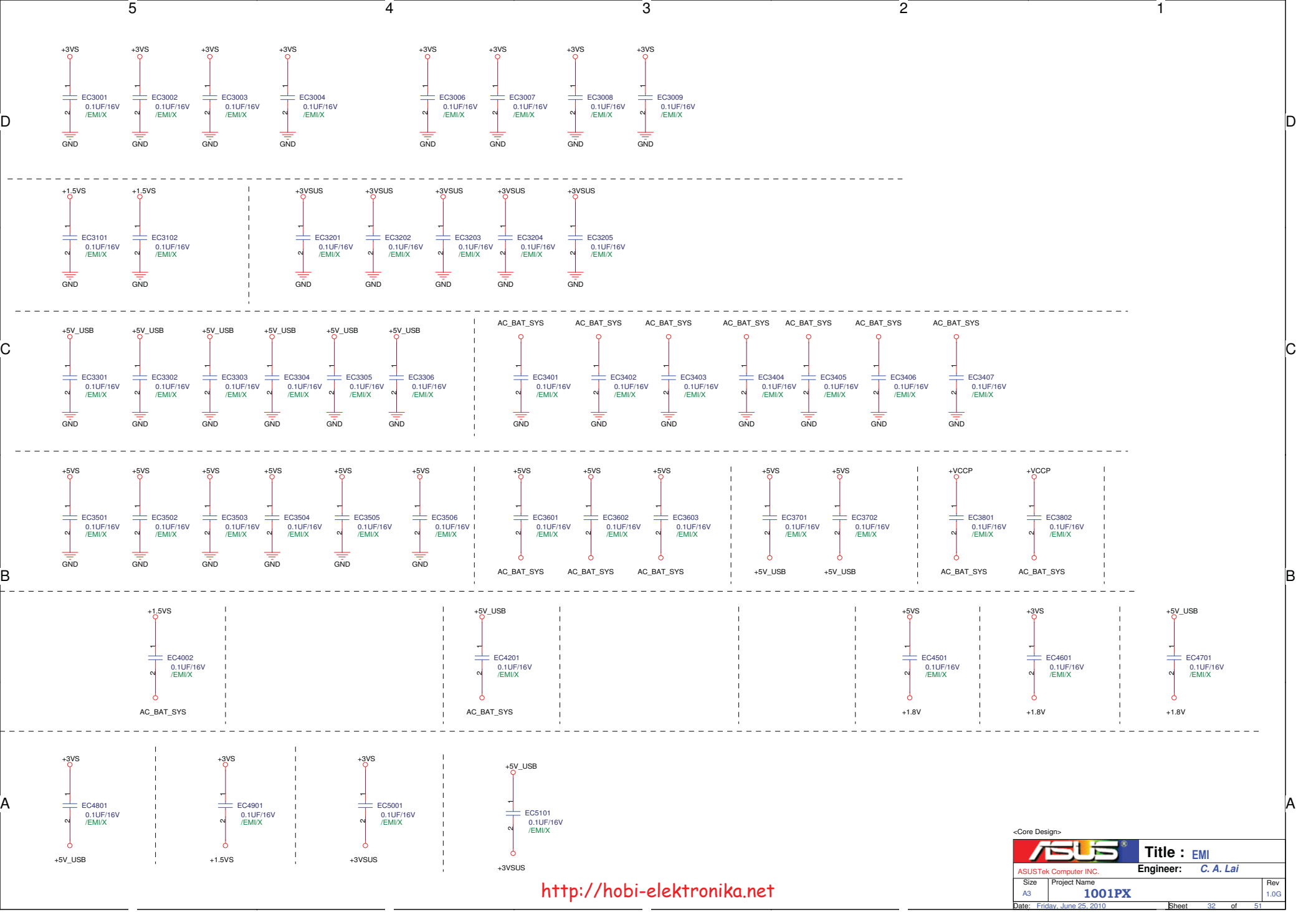






<Core Design>

ASUSTek Computer INC.	Title : Srew Hole	
	Engineer: C. A. Lai	
Size: A3	Project Name: 1001PX	Rev: 1.0G
Date: Friday, June 25, 2010	Sheet 31 of 51	



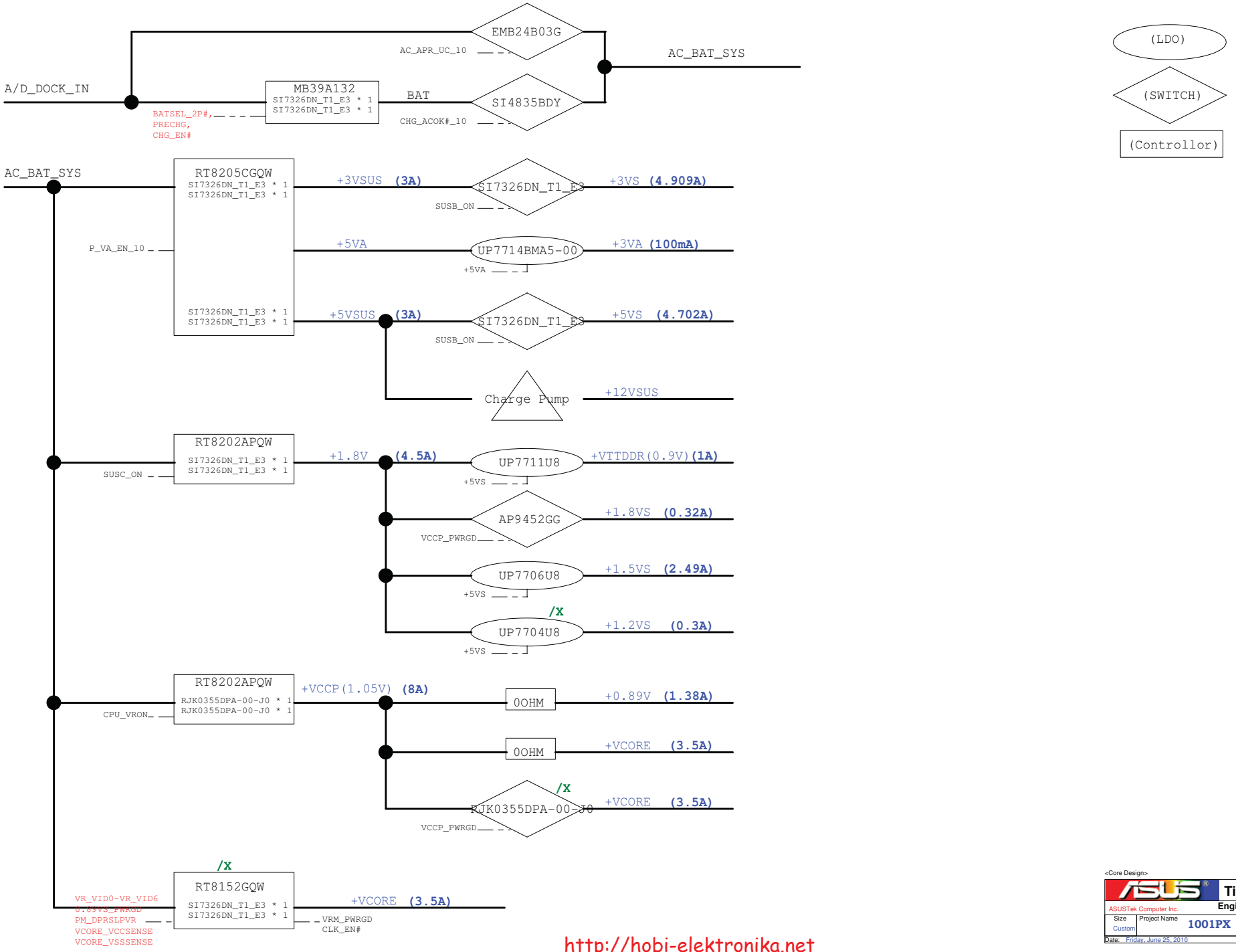
<Core Design>

Title : EMI

ASUSTek Computer INC. Engineer: C. A. Lai

Size	Project Name	Rev
A3	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 32 of 51



<Core Design>

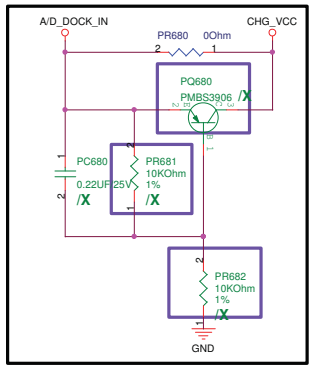
ASUSTek Computer Inc.

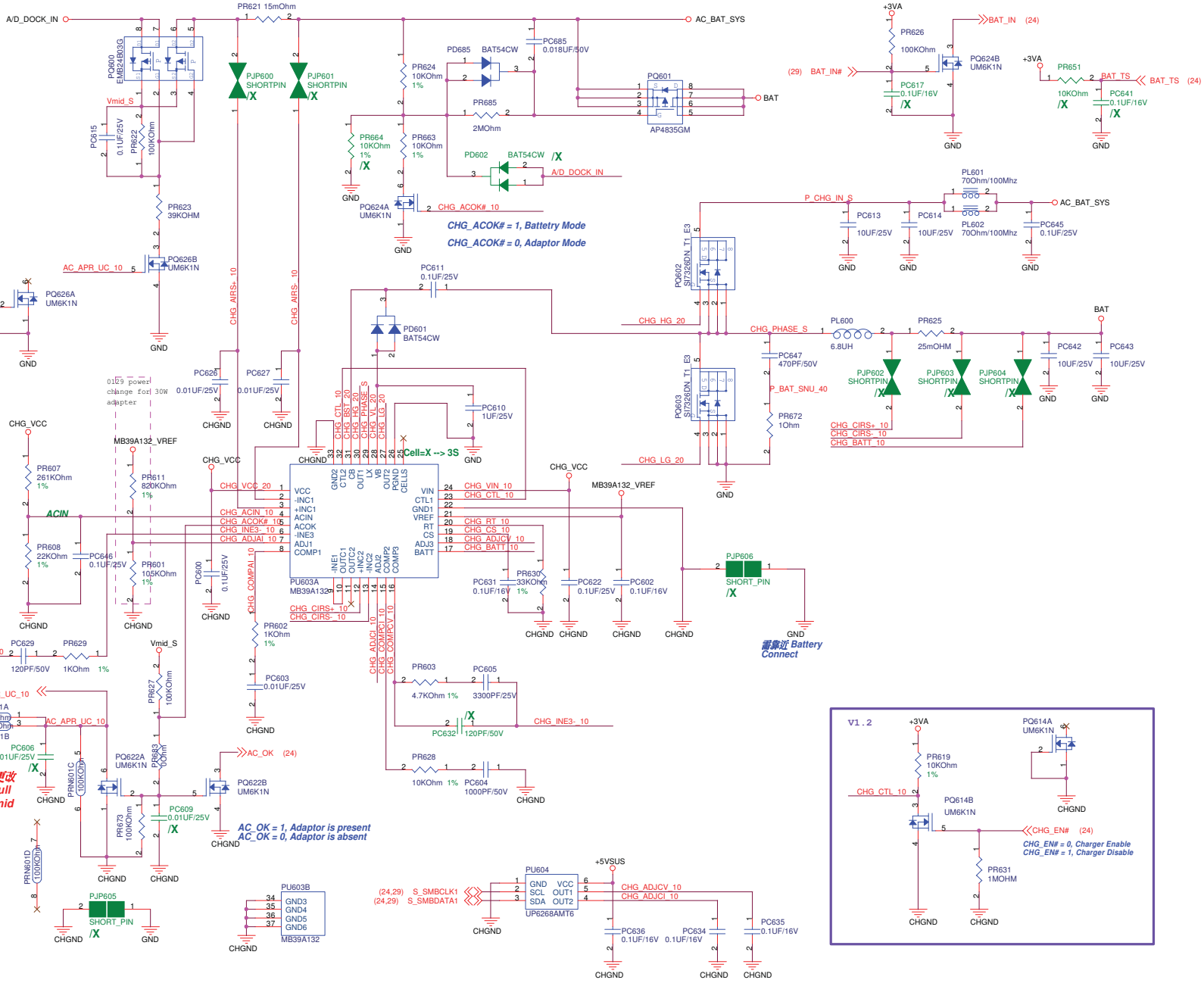
Title : POWER FLOW

Engineer: Justin_Lee

Size	Project Name	Rev
Custom	1001PX	1.0G

Date: Friday, June 25, 2010 Sheet 33 of 51





VREF = 5.0V
Fosc(KHz) = 17000 / RT (KOhm)
= 17000 / 33K = 515K

*Soft start: ts(s) = 0.13 * CS (uF)*
*= 0.13 * 0.1 = 0.013*

Adaptor Max. Current :
34.50W (19V/40W)

ACIN Threshold = 1.25V
Adaptor > 16.08V, System Powered by Adaptor
Adaptor < 16.08V, System Powered by Battery

Battery Charging Voltage :
Vadj3 > 4.1V ==> Vbat = 4.2V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Charging Current :
4.4V > Vadj2 >= 0V ==>
Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
Vadj1 = 5(90.9)/(510+90.9) = 0.756V*
*Ilimit_current = (0.756-0.075) / (25*15m) = 1.816A*
*19V*1.816A = 34.50W*

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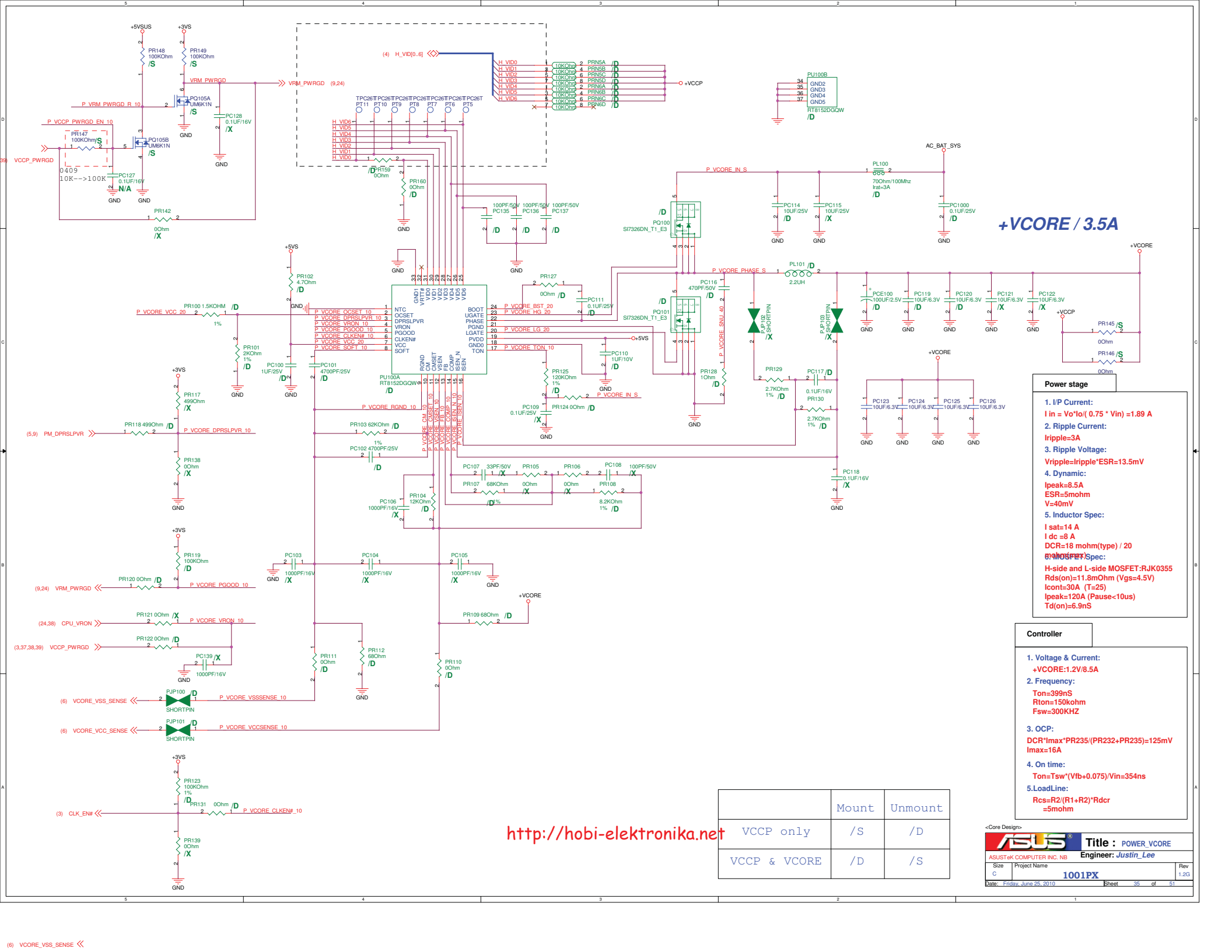
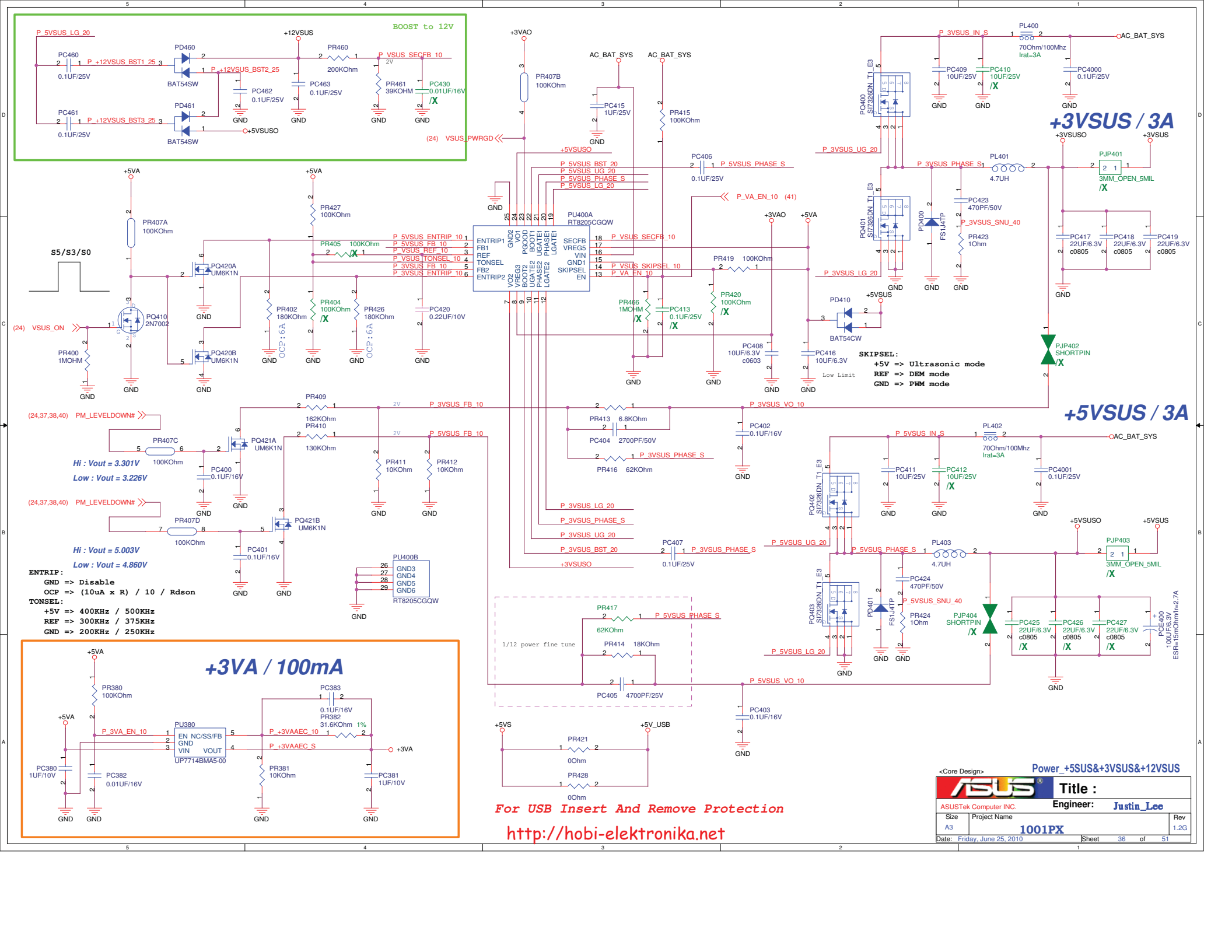
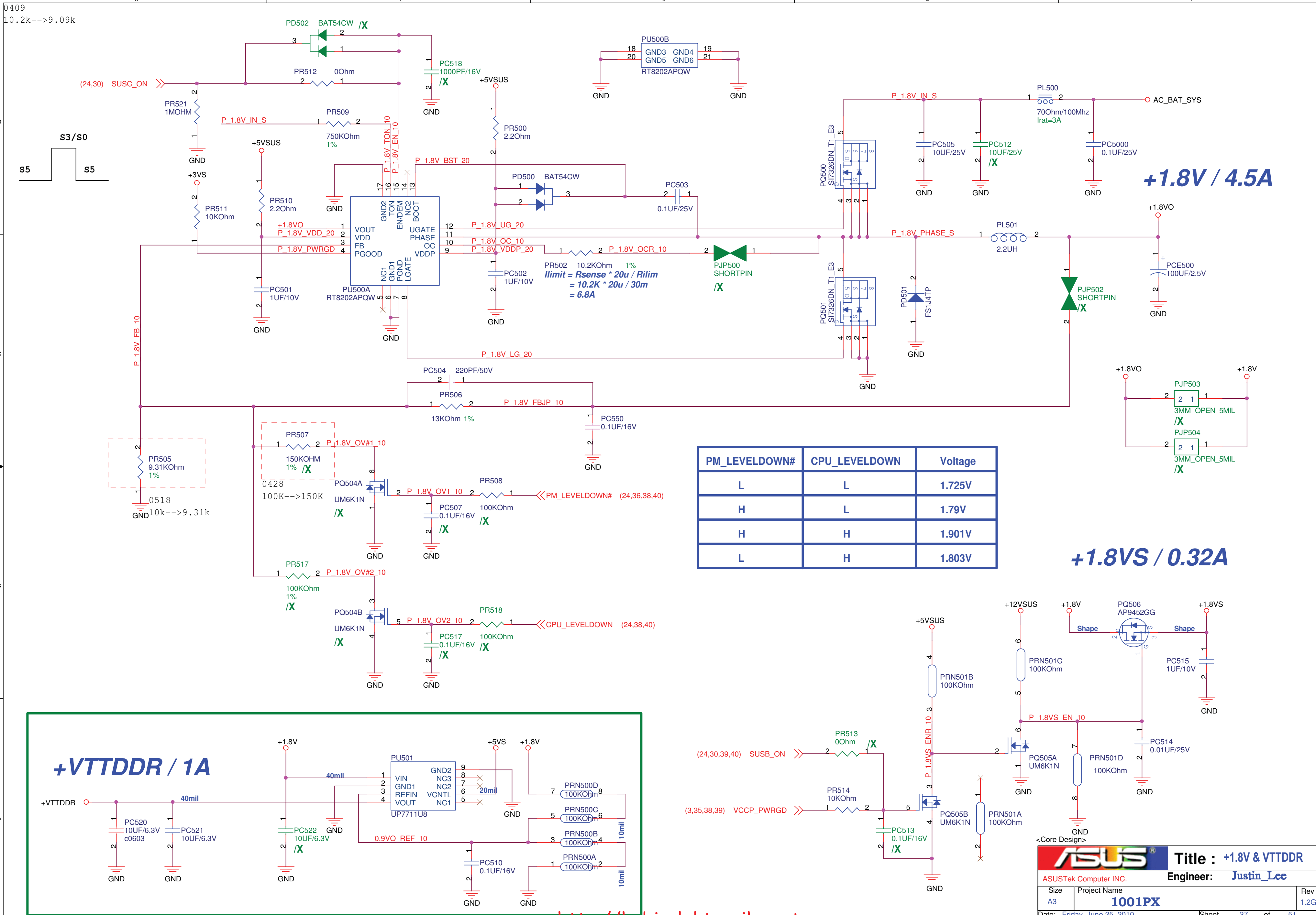
<Core Design>

ASUSTek Computer INC.	Title : CHARGER	
	Engineer: Justin_Lee	
Size: Custom	Project Name: 1001PX	Rev: 1.2G
Date: Friday, June 25, 2010	Sheet 34 of 51	


+VCORE / 3.5A
Power stage
1. I/P Current:
I in = Vo*Io/(0.75 * Vin) =1.89 A
2. Ripple Current:
Iripple=3A
3. Ripple Voltage:
Vripple=Iripple*ESR=13.5mV
4. Dynamic:
Ipeak=8.5A
ESR=5mohm
V=40mV
5. Inductor Spec:
I sat=14 A
I dc =8 A
DCR=18 mohm(type) / 20
6. MOSFET Spec:
H-side and L-side MOSFET:RJK0355
Rds(on)=11.8mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)
Td(on)=6.9nS
Controller
1. Voltage & Current:
+VCORE:1.2V/8.5A
2. Frequency:
Ton=399nS
Rton=150kohm
Fsw=300KHZ
3. OCP:
DCR*Imax*PR235/(PR232+PR235)=125mV
Imax=16A
4. On time:
Ton=Tsw*(Vfb+0.075)/Vin=354ns
5.LoadLine:
Rcs=R2/(R1+R2)*Rdcr
=5mohm
Mount
Unmount
VCCP only
/S
/D
VCCP & VCORE
/D
/S
http://hobi-elektronika.net
Title : POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Justin_Lee
Project Name
1001PX
Rev
1.2G
Date: Friday, June 25, 2010
Sheet 35 of 51


BOOST to 12V
+3VSUS / 3A
+5VSUS / 3A
+3VA / 100mA
S5/S3/S0
SKIPSEL:
+5V => Ultrasonic mode
REF => DEM mode
GND => PWM mode
Hi : Vout = 3.301V
Low : Vout = 3.226V
Hi : Vout = 5.003V
Low : Vout = 4.860V
ENTRIP:
GND => Disable
OCP => (10uA x R) / 10 / Rdson
TONSEL:
+5V => 400KHz / 500KHz
REF => 300KHz / 375KHz
GND => 200KHz / 250KHz
For USB Insert And Remove Protection
http://hobi-elektronika.net
Power_+5SUS&+3VSUS&+12VSUS
ASUSTek Computer INC.
Engineer: Justin_Lee
1001PX
Date: Friday, June 25, 2010
Sheet 36 of 51



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage
L	L	1.725V
H	L	1.79V
H	H	1.901V
L	H	1.803V

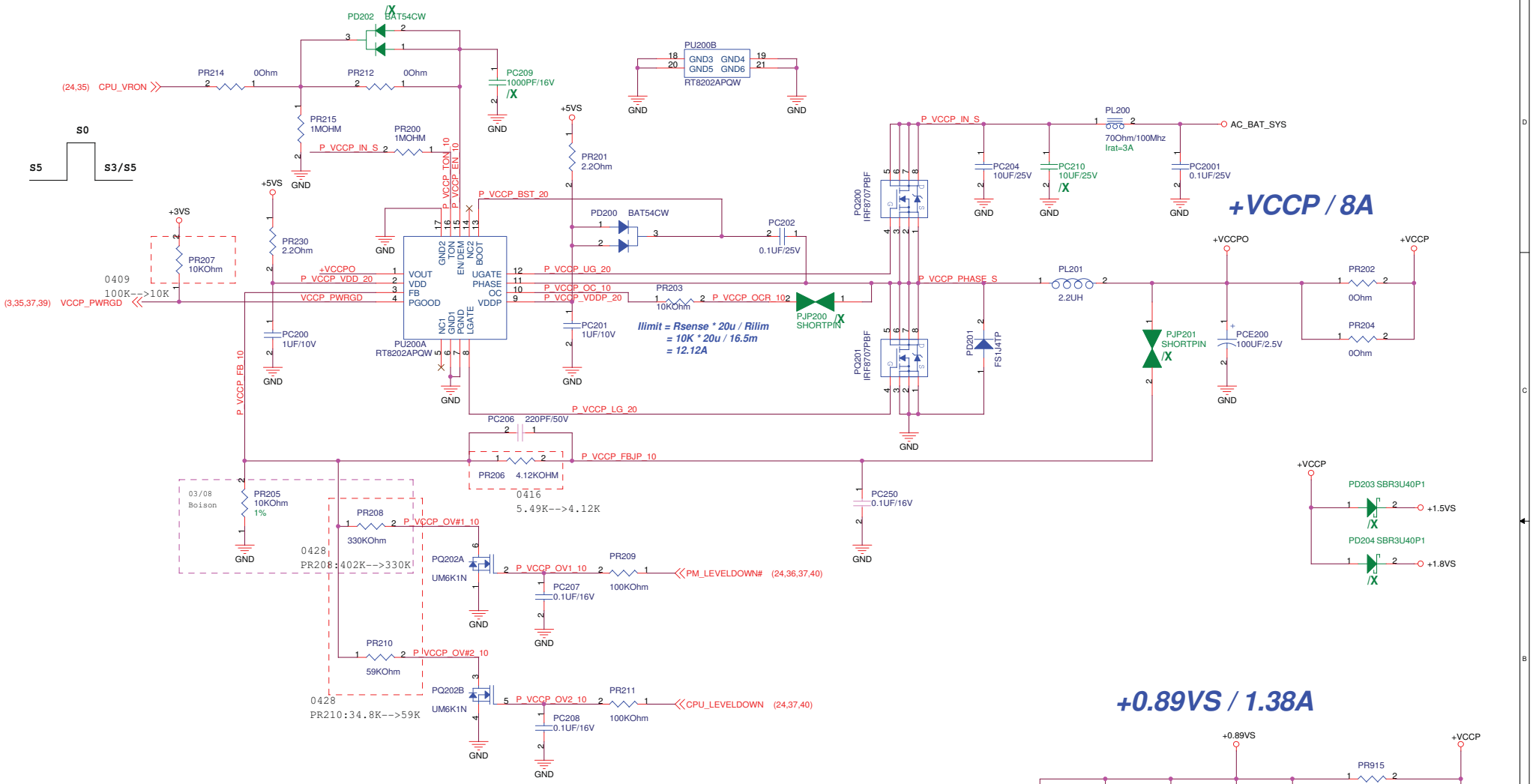
ASUSTek Computer INC.

Title : +1.8V & VTTDDR

Engineer: Justin_Lee

Size: A3 | Project Name: 1001PX | Rev: 1.2G

Date: Friday, June 25, 2010 | Sheet 37 of 51



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage	Status
L	L	1.059V	N/A
L	H	1.111V	Power Saving
H	H	1.121V	Normal

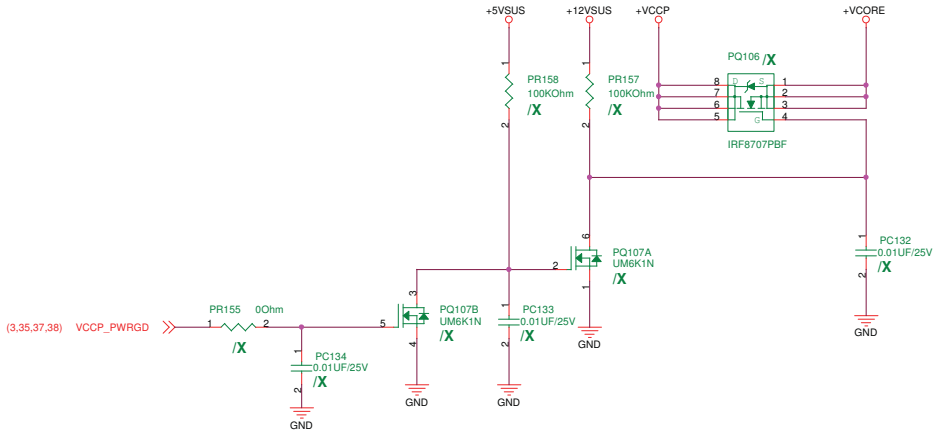
<Core Design>

Title : +VCCP

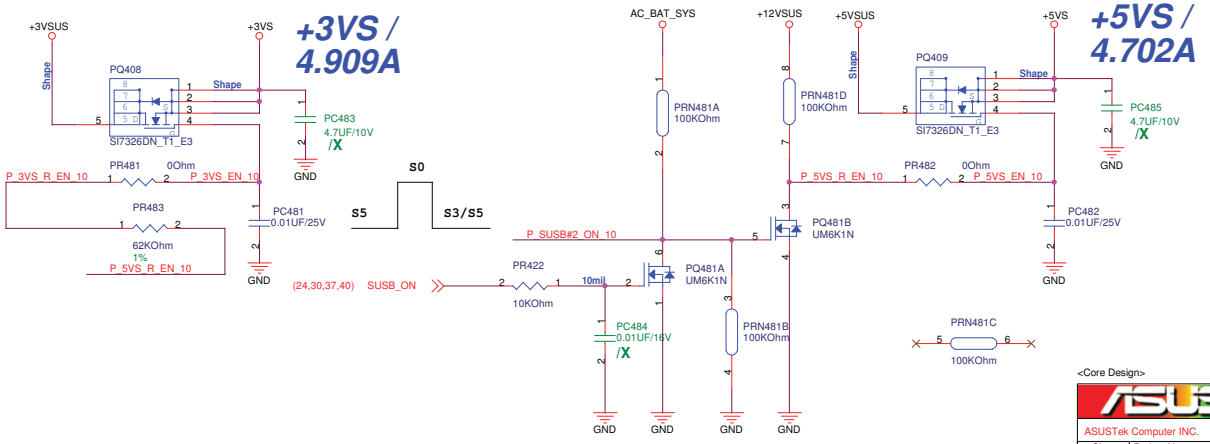
ASUSTek Computer INC. Engineer: Justin_Lee

Size	Project Name	Rev
A3	1001PX	1.2G

Date: Friday, June 25, 2010 Sheet 38 of 51



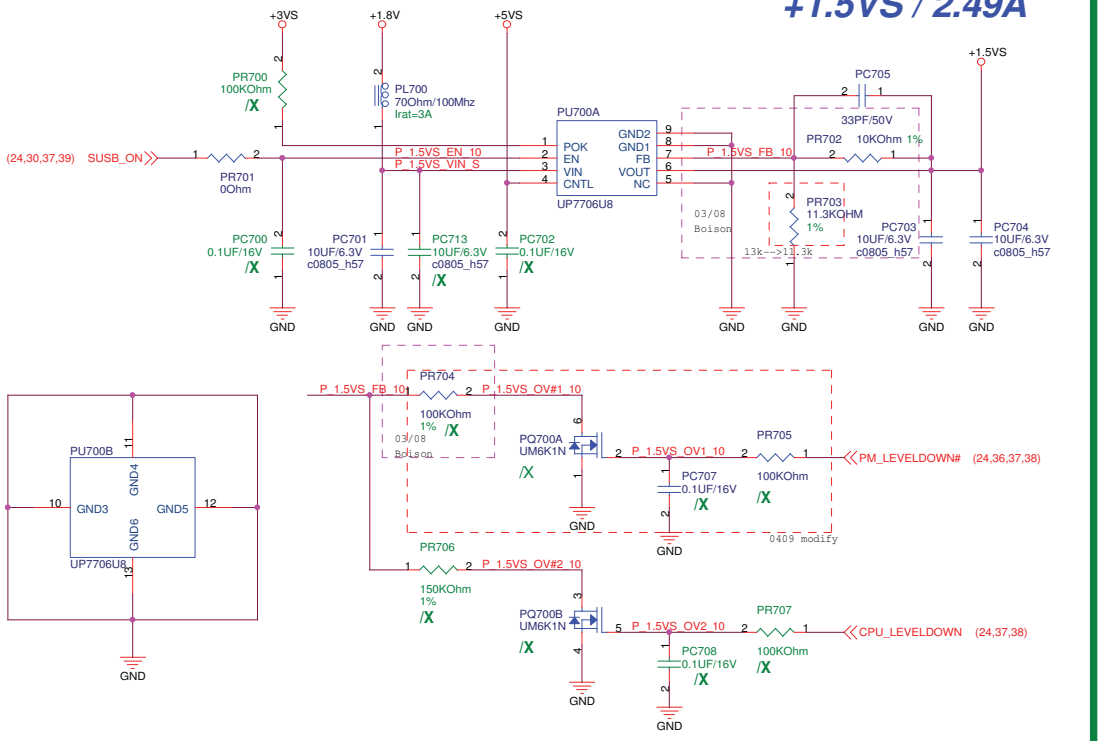
+VCORE / 3.5A



<Core Design>

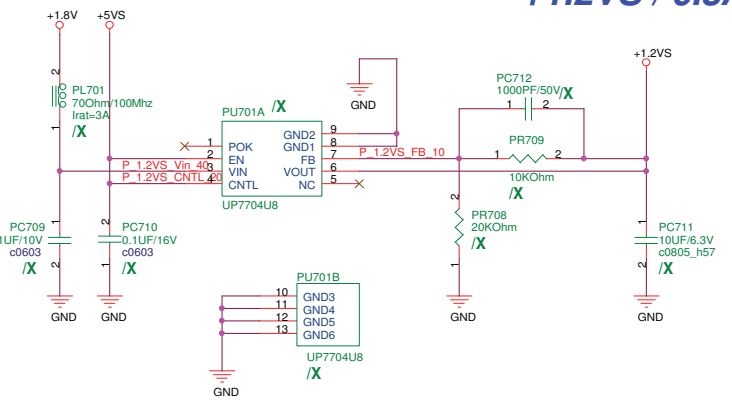
ASUSTek Computer INC.	Title : +0.89VS&+3VS&+5VS	
	Engineer: Justin_Lee	
Size: Custom	Project Name: 1001PX	Rev: 1.2G
Date: Friday, June 25, 2010	Sheet 39 of 51	

+1.5VS / 2.49A



PM_LEVELDOWN#	CPU_LEVELDOWN	Voltage
L	L	1.415V
H	L	1.495V
H	H	1.548V
L	H	1.468V

+1.2VS / 0.3A



<Core Design>

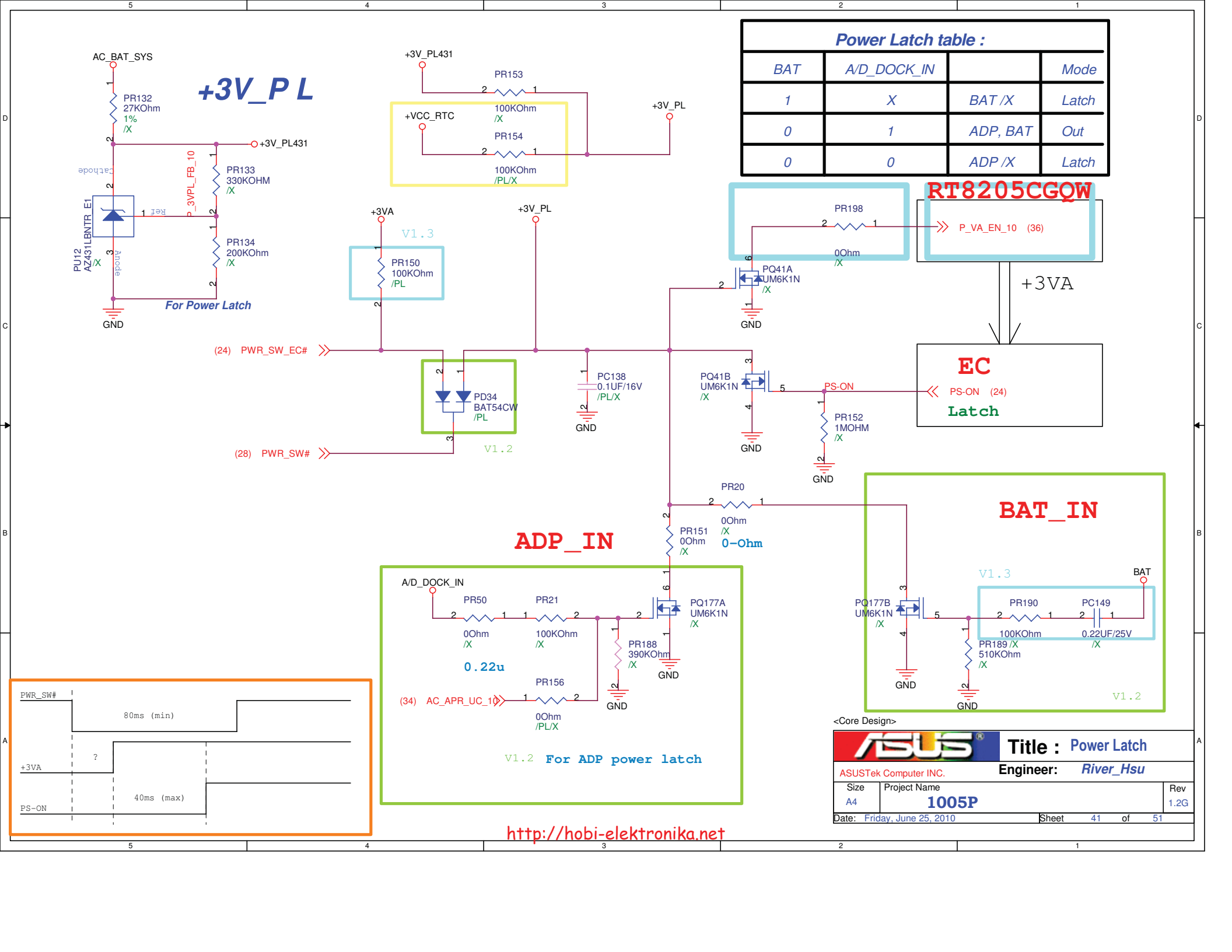
Title : +1.5VS&+1.2VS

ASUSTeK COMPUTER INC. NB

Engineer: Justin_Lee

Size	Project Name	Rev
A3	1001PX	1.2G

Date: Friday, June 25, 2010 Sheet 40 of 51


Power Latch table :
BAT | A/D_DOCK_IN | | Mode
1 | X | BAT /X | Latch
0 | 1 | ADP, BAT | Out
0 | 0 | ADP /X | Latch
+3V_P L
AC_BAT_SYS
PR132 27KOhm 1% /X
+3V_PL431
PR133 330KOHM /X
PR134 200KOhm /X
P_3VPL_FB_10
PU12 AZ431LBNTR_E1 /X
For Power Latch
GND
+3V_PL431
PR153 100KOhm /X
+VCC_RTC
PR154 100KOhm /PL/X
+3V_PL
+3VA
V1.3
PR150 100KOhm /PL
RT8205CGQW
PR198 0Ohm /X
P_VA_EN_10 (36)
PQ41A UM6K1N /X
+3VA
EC
PS-ON (24)
Latch
(24) PWR_SW_EC#
PD34 BAT54CW /PL
V1.2
PC138 0.1UF/16V /PL/X
PQ41B UM6K1N /X
PS-ON
PR152 1MOHM /X
(28) PWR_SW#
PR20 0Ohm /X
PR151 0Ohm /X 0-Ohm
ADP_IN
A/D_DOCK_IN
PR50 0Ohm /X
PR21 100KOhm /X
0.22u
PR188 390KOhm /X
PR156 0Ohm /PL/X
(34) AC_APR_UC_10
PQ177A UM6K1N /X
V1.2 For ADP power latch
BAT_IN
V1.3
BAT
PQ177B UM6K1N /X
PR190 100KOhm
PC149 0.22UF/25V /X
PR189 /X 510KOhm /X
V1.2
PWR_SW#
80ms (min)
+3VA
?
40ms (max)
PS-ON
<Core Design>
Title : Power Latch
ASUSTek Computer INC.
Engineer: River_Hsu
Size A4
Project Name 1005P
Rev 1.2G
Date: Friday, June 25, 2010
Sheet 41 of 51
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